DESIGN AND IMPLEMENTATION OF A 200W MICROINVERTER FOR GRID CONNECTED PHOTOVOLTAIC ENERGY CONVERSION SYSTEM

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ABSTRACT

DESIGN AND IMPLEMENTATION OF A 200W MICROINVERTER FOR GRID CONNECTED PHOTOVOLTAIC ENERGY CONVERSION SYSTEM

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As one type of the grid-connected photovoltaic energy conversion systems, micro-inverters (MI, also known as Module Integrated Inverters, MII) are typically designed for residential applications with energy capacities of 3-5 kW and less, in order to provide PV module level energy generation, plug-N-play operation, minimization of the shading effects occurring on the PV module, and flexibility of installation. For the micro-inverter system which can be designed employing variety of topologies, interleaving flyback converter with grid frequency operated DC/AC unfolding bridge is suggested, analyzed, and modeled. A 200 W single-phase flyback converter and 200 W two-phase interleaved flyback converter topologies are studied with respect to their efficiencies, harmonic isolations and load current regulations through detailed analysis, simulations, and laboratory experiments. In the hardware implementation, with the aid of a digital signal processor advanced control functions are implemented. Maximum power point tracking (MPPT), vector based phase locked loop (PLL) for grid synchronization and grid connection, and grid current control for low harmonic distortion, in addition to the basic connection and protection functions are implemented such that a highly efficient and effective PV conversion system performance is obtained. Design and implementation of 200 W micro-inverters with single-phase and two-phase interleaved flyback converters are realized and detailed laboratory tests are conducted. As a result, correlation among the theory, analysis, simulations, and laboratory experiments is provided and the feasibility of MI systems is proven.

Keywords: control, design, flyback converter, grid connection, interleaving, inverter, maximum power point tracking, micro-inverter, module integrated inverter, phase locked loop, photovoltaic, PV module, unfolding bridge,

ÖZ

ŞEBEKEYE BAĞLANABİLEN FOTOVOLTAİK ENERJİ DÖNÜŞÜM SİSTEMİ İÇİN 200W MİKROEVİRİCİ TASARIMI VE ÜRETİMİ

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Şebeke bağlantılı fotovoltaik enerji dönüşüm sistemleri arasında mikroevirici (Panele bütünleşik evirici, PBE) sistemleri, panel seviyesinde enerji üretimi sağlaması, tak çalıştır özelliği olması, panelin üzerinde oluşan gölgelenme etkisini en aza indirmesi ve esnek kurulum imkanı sağlaması amacı ile özellikle 3-5kW ve altı konut uygulamalarında kullanılmak üzere geliştirilmiştir. Üretiminde birçok farklı topoloji kullanılan PBE için flyback dönüştürücü ve şebeke frekanslı DC/AC dönüştürücü topolojisi önerilmiş, analizi ve modellemesi gerçekleştirilmiştir. 200W tek faz flyback dönüştürücülü PBE yapısı ile 200W faz kaydırmalı iki fazlı flyback dönüştürücülü PBE yapısı; verimi, harmonik yalıtımı ve yük akımı düzeltimi başarımı detaylı benzetimler ve laboratuvar çalışmaları ile incelenmiştir. Donanım uygulamasında, sayısal işaret işlemci kullanılarak ileri derece denetçi fonksiyonları uygulanmıştır. En yüksek güç noktası takibi (EYGNT), şebeke senkronizasyonu ve bağlantısı için vektör tabanlı faz kilitlemeli döngü (FKD), yüksek harmonik yalıtımı başarımı için akım denetimi ve koruma fonksiyonları ile etkili ve verimli bir PV dönüşüm sistemi elde edilmiştir. 200W, tek fazlı ve iki fazlı faz kaydırmalı flyback dönüştürücülü PBE'lerin tasarımı ve üretimi gerçekleştirilerek karşılaştırmalı olarak ayrıntılı laboratuvar çalışmaları yapılmıştır. Yapılan çalışmalar sonucunda benzetim ve deney sonuçlarının birbirleri ile uyumlu olduğu görülmüş ve sistemin uygulanabilirliği kanıtlanmıştır.

Anahtar Kelimeler: denetçi, en yüksek güç noktası takibi, faz kaydırma, faz kilitlemeli döngü, flyback dönüştürücü, fotovoltaik, fotovoltaik panel, mikroevirici, panele bütünleşik evirici, şebeke frekanslı DC/AC dönüştürücü, tasarım,

To My Parents, Süheyla & Bekir
To My Sister, Sena
and To My Niece, Nina Melisa

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
APDC	Active Power Decoupling Circuit
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CdTe	Cadmium Telluride
CI	Copper Indium
CV	Constant Voltage
DCM	Discontinuous Conduction Mode
DLPF	Digital Low Pass Filter
Ds	Diselenide
DSP	Digital Signal Processor
EMI	Electro Magnetic Interference
ESR	Effective Series Resistance
EUT	Equipment Under Test
FIFO	First In First Out
GB	Gigabyte
GS	Gallium Disulfide
GW	Giga watt
HF	High Frequency
IC	Incremental Conductance
LPF	Low Pass Filter
MI	Micro-Inverter
MII	Module Integrated Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MTBF	Mean Time Between Failure
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PLL	Phase Locked Loop
P&O	Perturb and Observe
PV	Photovoltaic
PWM	Pulse Width Modulation

SCRG	Sinusoidal Current Reference Generation
SPMI	Single-phase Micro-Inverter
THD	Total Harmonic Distortion
TPIMI	Two-phase Interleaved Micro-Inverter
UB	Unfolding Bridge
UPS	Uninterruptible Power Supply
USB	Universal Serial Bus
WP	Watt peak

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

At the present time, the rise in population, industrial developments and growing technological opportunities continuously increases the need for energy causing people to gravitate towards new energy sources. In this direction, overall energy consumption of the world is expected to be increased by 42.7% from 2012 to 2035 [1]. Fossil fuels are meeting a great proportion of the energy need of the world today, causing an increase on the effects of global warming. By means of this increase, countries are heading towards renewable energy sources in order to reduce the effects of global warming. Among renewable energy sources such as hydro and wind power, photovoltaic (PV) systems using solar energy stands in third place and its popularity is rising day by day.

While the installed capacity of PV systems all over the world in 2000 was 1.4GW and in 2012, it is increased at a remarkable rate to 102.16 GW power capacity as it is shown in Figure 1.1 [2]. The capacity of the installed PV systems just in 2012 were 31GW. Only in Europe, where the PV system installation of the world mostly takes place, cumulative installed capacity of 130 GW by 2020 is expected according to the baseline scenario which assumes that 4% of the electricity demand is provided by grid-connected PV systems [2].

In case of governments reducing the bureaucratic procedures which slowing down the installation of PV systems especially for residential applications and providing advantages such as tax reduction, 12% of the electricity demand is expected to be provided by PV systems in Europe by 2020 [2].

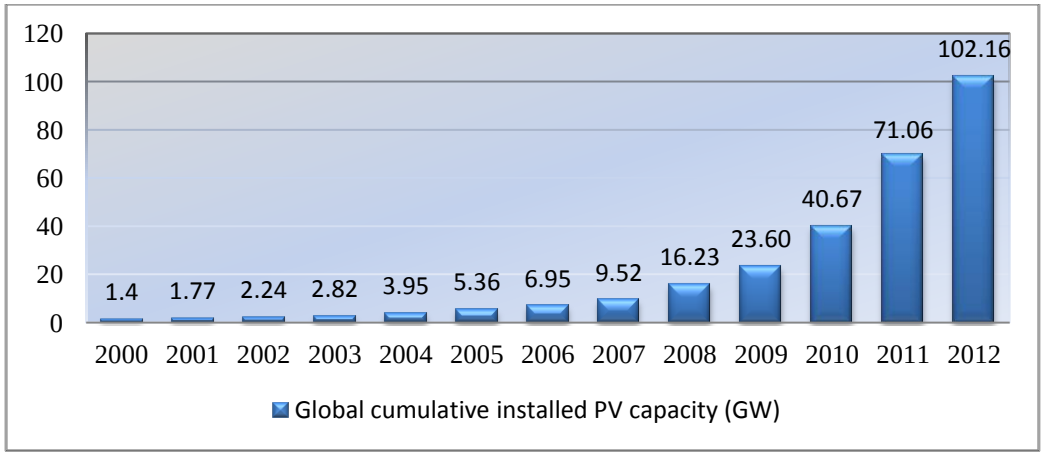

Figure 1.1 Evolution of global cumulative installed PV capacity (2000 - 2012)[2].

Another great impact which increases the installation of PV systems is that, while the energy production cost is increasing continuously, PV system costs are decreasing. PV system costs can be analyzed for residential, commercial and utility scale PV systems [3]. According to over 150,000 installed residential and commercial PV systems in US, the system cost is reduced by 5% - 7% from 1998 to 2011 and by 11% - 14% from 2010 to 2011 [3]. The researches shows that the system price for residential or small-scale commercial rooftop PV systems (<10kW) falls from 6.37$/W to 5.97$/W in the first half of 2012 in California where the most significant cost decline took place.

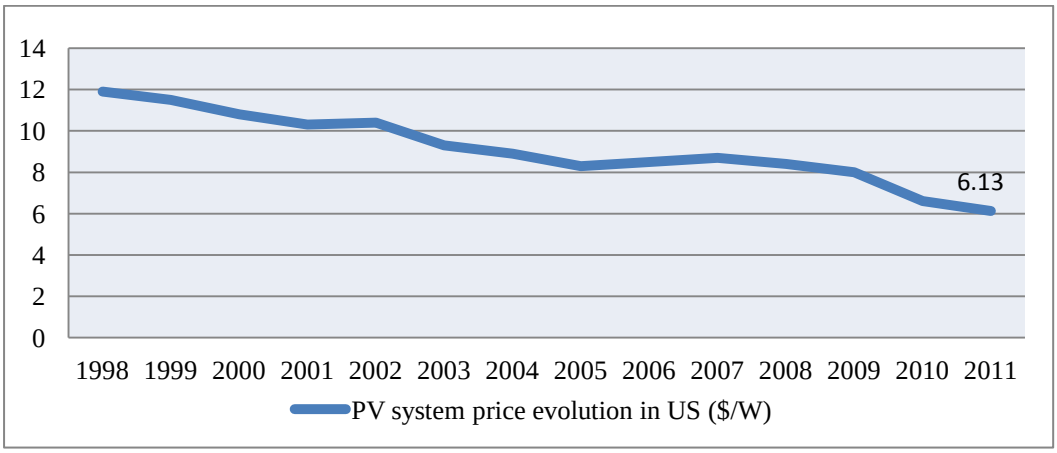

Figure 1.2 Analyst-projected average US PV system price from 1998 to 2011[3].

PV systems are generally installed with grid connection. If the PV system cost decreases, and governments provide advantageous energy production conditions, the payback time of the system will be decreased and the amount of the profit will be satisfactory for the customer which leads to an increase of PV system installations all over the world and a reduction of system payback time.

In accordance with the price reduction, the market share of the small-scale residential PV systems improves continuously. As it is shown in Figure 1.3, the evolution of installed residential PV systems in US from 2000 to 2012 is given [4].

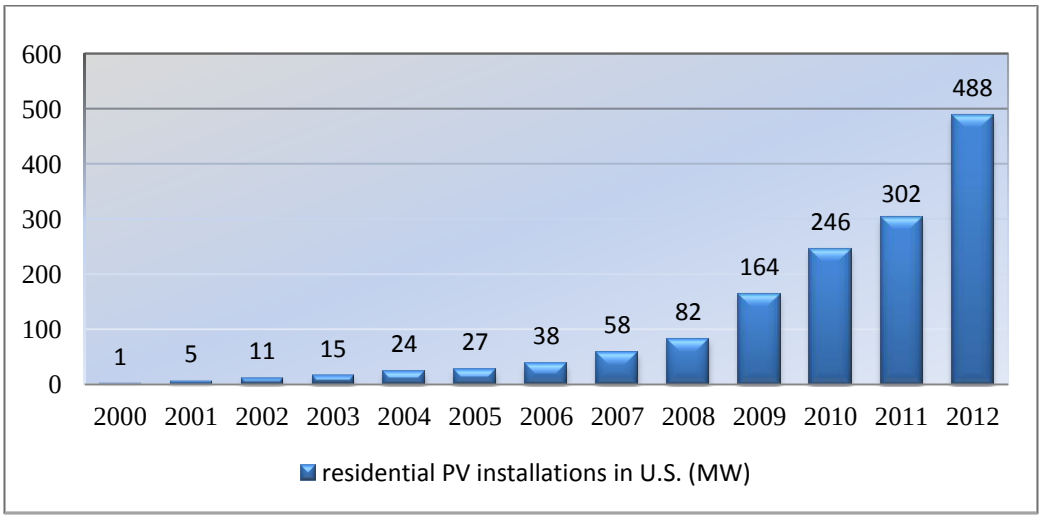

Figure 1.3 Evolution of residential PV installations in US (2000 - 2012)[4].

In accordance with the increase in residential installations, the researches on PV systems are increased considerably. For an efficient PV system, one of the most important part can be stated as the inverter alongside of PV panel forming the interface between the PV panel and the utility grid for on grid systems.

Moreover, the inverter types varies by the power capacity of the PV system which will be explained in detail in Chapter 2. Among these inverters, micro-inverters are the new trend for the residential rooftop solar applications where the power capacity

is relatively small such as 3-5kW or less. Furthermore, there are various topologies used in micro-inverters grouped according to their DC-link configurations, isolation, number of power stages, etc. The most popular micro-inverter topologies are analyzed in Chapter 3.

1.2 Objectives of the Thesis

The main focus of this thesis is to investigate micro-inverters and the topologies designed for small-scale residential grid-connected rooftop applications and achieving the analysis, design, modeling and implementation of a grid-connected single-phase single-stage 200W flyback-based micro-inverter with grid frequency operated unfolding bridge circuit connected to a 220V/50Hz utility grid as shown in Figure 1.4.

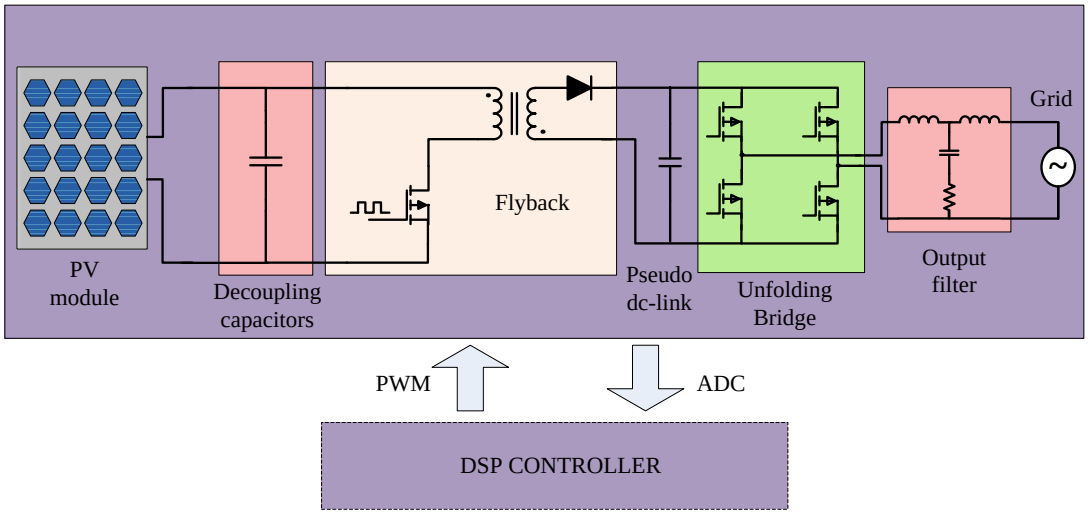

Figure 1.4 200W grid-connected flyback micro-inverter fed by a PV module.

On the other hand, analysis, design, modeling and implementation of a grid-connected two-phase 200W interleaved flyback-based converter connected to a 220V/50Hz utility grid is also another objective of this thesis as it is shown in Figure 1.5. Performance evaluation and the comparison of two micro-inverters with respect to maximum efficiency, euro efficiency, decoupling performance, THD, maximum power point tracking and switching performance will be realized.

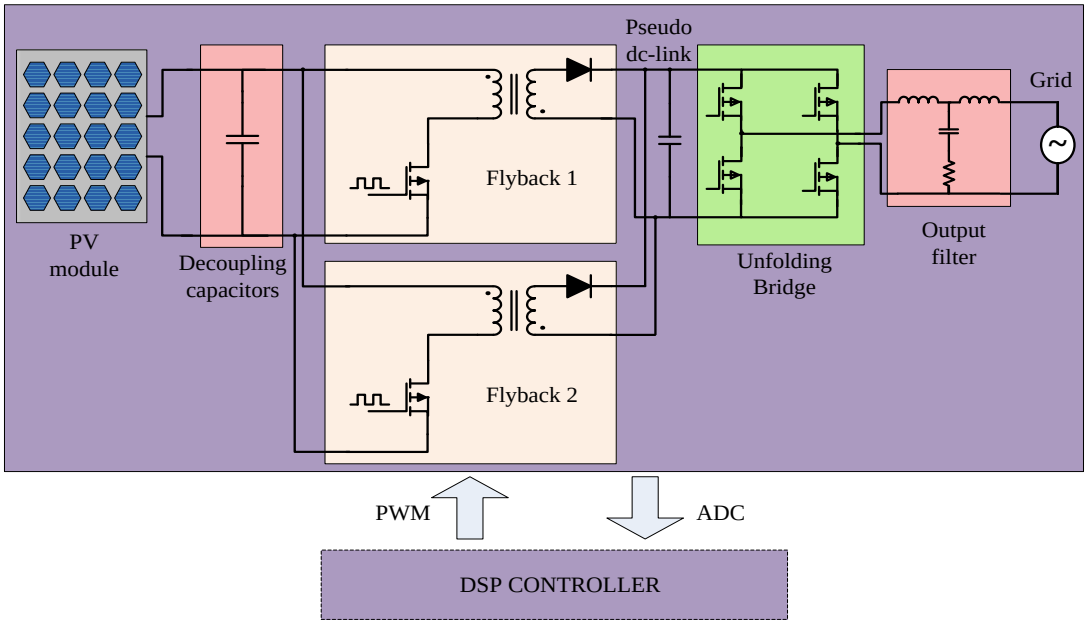

Figure 1.5 Grid-connected two-phase interleaved flyback micro-inverter fed by a PV module.

Moreover, The design of the control techniques such as maximum power point tracking, sinusoidal current reference generation and phase locked loop will be explained in detail. Control strategies are implemented with a DSP controller in order to have efficient systems.

1.3 Thesis Outline

The chapters of the thesis are constituted as follows;

Chapter 2 includes an overview of PV systems and micro-inverter technology explaining parts of the PV system, inverters in use, and the advantages and drawbacks of the micro-inverter system. Besides this, the system requirements and standards for a PV system are also clarified.

In chapter 3, the importance of power decoupling and input capacitor sizing is clarified and classification of widely used micro-inverter topologies is achieved according to their DC-link configurations. A comparison is made between these

topologies with respect to their efficiencies, semiconductor device counts, power capacities and decoupling capacitor sizes.

In the 4th chapter, operating principles and analysis of flyback-based micro-inverter are explained starting with flyback topology. Switching strategies of the flyback inverter such as discontinuous conduction and continuous conduction modes are discussed. Afterwards, benefits of interleaving over single-phase applications is introduced. Control algorithms implemented with a DSP for sinusoidal current reference generation, maximum power point tracking, phase locked loop and the conducted techniques are illustrated.

In the 5th chapter, hardware design and implementation of single-phase and interleaved flyback topologies are introduced. Starting with single-phase flyback-based micro-inverter, magnetics design, snubber design, unfolding bridge circuit structure, decoupling capacitor sizing and output filter design explained respectively. Afterwards, same design processes are achieved for interleaved flyback-based micro-inverter. Finally semiconductor selection and power loss calculation for both topologies are conducted.

In the 6th chapter, detailed performance analysis of single-phase and interleaved two-phase flyback-based micro-inverters are conducted via Ansoft - Simplorer Software simulation program. Simulation results of two topologies are compared. Also, the comparison of the simulation results with the calculated theoretical values is realized.

In the 7th chapter, detailed performance analysis of single-phase and interleaved two-phase flyback-based micro-inverters are conducted via experimental works. The experimental setup is clarified. Simulation results of the previous chapter and experimental results are compared and the practicability of the micro-inverter topology is proved. The compatibility between calculated, simulated and implemented results are verified.

Finally, in the 8th chapter, the conclusion of the thesis is presented and future works are listed.

CHAPTER 2

OVERVIEW OF PV SYSTEMS AND MICROINVERTERS

2.1 Photovoltaic System

The aim of a photovoltaic system is to generate electricity from solar irradiation effectively by means of photovoltaic modules having semiconductors with photovoltaic property. The output of a PV module is direct current electricity. According to the load condition, DC/DC converters or DC/AC inverters can be used in order to transform the output of a PV module into a suitable sort of an electricity.

A photovoltaic system feeds local loads with or without battery storage and with or without grid connection. In a widespread manner, PV systems are installed as grid-connected which can be more economical by means of shortened pay-back time of the system with decreasing system costs and high efficiency. PV modules and PV inverters have various types with respect to the material and topology used these which will be explained in detail in section 2.1.1 and 2.1.3.

2.1.1 PV Module Characteristics

In order to reach the required power levels, a PV module is made up of different numbers of PV cells connected in series which is called string. There are various types of PV cells in use classified according to the materials they include. Besides crystalline silicon PV cells are the most common cells being used, thin film cell is another prevalent technology which can be produced from different materials such as cadmium telluride (CdTe) or copper indium/gallium disulfide/diselenide (CI/GS/Ds) [5]. The efficiency and surface area needed for 1kWp power generation for each type of PV cell can be seen in Table 2.1.

Table 2.1 Module efficiencies and surface area need for 1kWp power production for different types of PV cells [5]

Cell material	Module efficiency	Surface area need for 1kWp
Mono-crystalline silicon	13-19 %	5-8 m^2
Polly-crystalline silicon	11-15 %	7-9 m^2
Micromorphous tandem cell (a-Si/μc-Si)	8-10 %	10-12 m^2
Thin film Copper-indium/gallium-sulfur/diselenide (CI/GS/Se)	10-12 %	8-10 m^2
Thin film cadmium telluride (CdTe)	9-11 %	9-11 m^2
Amorphous silicon (a-Si)	5-8 %	13-20 m^2

Each cell used in a solar PV module is producing nearly 0.5V. Because of this low voltage level, cells are connected in series which makes PV modules very sensitive to partial shading situations. If any of the cells of a module become shaded, instead of producing energy, it starts to consume the energy generated by fully irradiated cells in series causing the shaded cell to heat up and even become damaged. In this case, the efficiency and output power of a PV module will be considerably decreased.

In order to prevent this situation, bypass diodes are used which bypass the shaded (consuming) cell and by means of providing the current another way to flow, the shaded cell does not heat up. The PV module structure with bypass diodes can be seen in Figure 2.1.

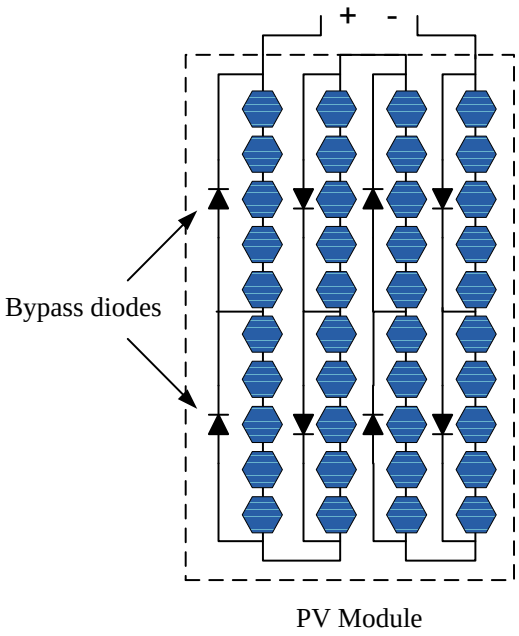

Figure 2.1 PV module structure with bypass diodes**.**

A PV cell is made up of p-n junction semiconductors and can be modeled as a current source in parallel with a diode as shown in Figure 2.2. In the event of no solar irradiation, the PV cell will act like a diode. If the solar irradiation rises, the PV cell starts to generate current. As a non-ideal system, there are parasitic resistances R_P and R_S caused by the internal resistances of conductors, connection points etc. In the equivalent circuit of PV cell, I_{LIGHT} represents light generated current, I_{CELL} and V_{CELL} representing the output current and voltage of the PV cell.

The I-V and P-V characteristics of a PV cell can be seen in Figure 2.3. I_{SC} is the short circuit current of the PV cell occurring when the impedance is very low and output voltage V_{CELL} is equal to zero. The open circuit voltage V_{OC} occurs when there is no load and I_{CELL} is equal to zero. P_{MAX} is the maximum power point (MPP) of the PV cell, and can be reached when output voltage is equal to V_{MAX} and output current is equal to $I_{MAX.}$

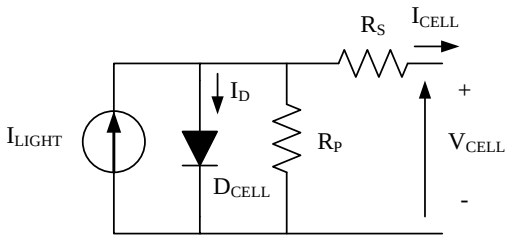

Figure 2.2 Equivalent circuit model of a PV cell**.**

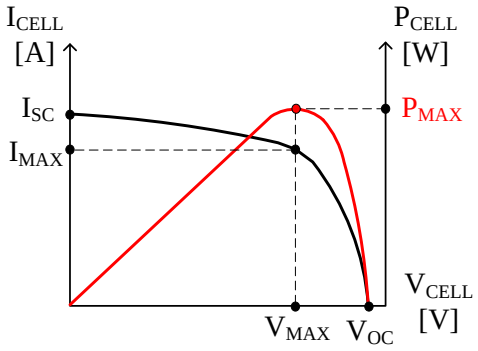

Figure 2.3 I-V and P-V characteristics of a PV cell**.**

It is important to determine the quality of a PV cell. In order to determine the quality of the PV cell, the fill factor (FF) of the PV cell can be calculated from (2.1) which is the ratio between maximum power and theoretical power of the cell. Theoretical power (P_T) is equal to the product of I_{SC} and V_{OC} which is the area of the largest rectangle which will fit in the I-V curve.

$$FF = P_{MAX} / P_T \tag{2.1}$$

The MPP of the solar cell is highly sensitive to atmospheric conditions. Open circuit voltage (V_{OC}) and short circuit current (I_{SC}) varies with respect to temperature and solar irradiation. The temperature coefficient of output voltage of the PV cell is negative and decreases with increasing ambient temperature. On the other hand the temperature coefficient of output current of the PV cell is positive and slightly

changes with varying ambient temperatures. The effect of temperature on V_{OC} and I_{SC} can be seen from Figure 2.4.

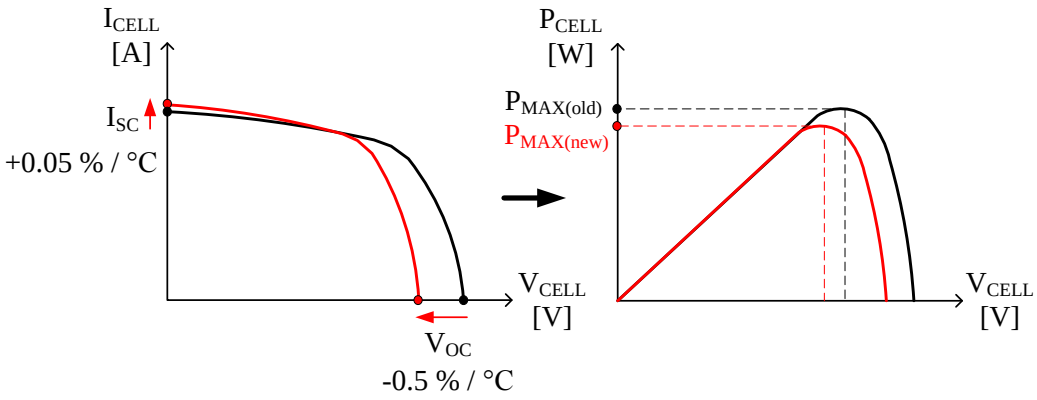

Figure 2.4 Ambient temperature effect on V_{OC} and I_{SC} [5]**.**

Besides this, short circuit current of PV cell increases linearly with increasing solar irradiation level. In Figure 2.5, the effect of solar irradiation on I_{SC} and MPP of the PV cell can be seen.

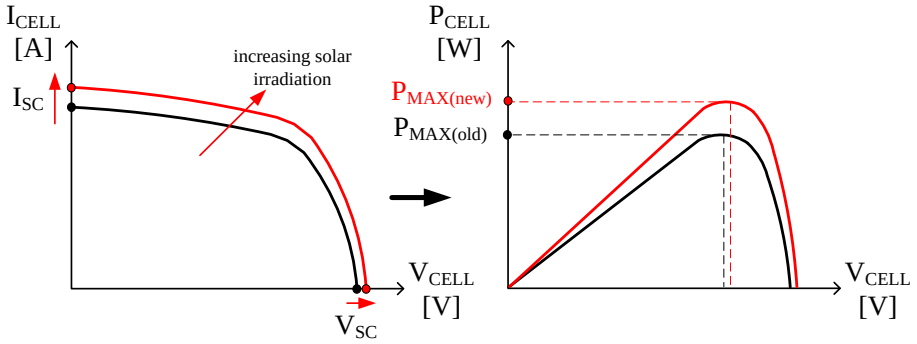

Figure 2.5 The effect of solar irradiation on ISC and MPP of the PV cell**.**

It can be seen from Figure 2.4 and Figure 2.5 that, if the ambient temperature changes, it will mostly influence the open circuit voltage of PV cell. On the other

hand , if the solar irradiation changes, the short circuit current of the PV cell will be influenced which causes the MPP of the cell to slide.

2.1.2 Maximum Power Point Tracking

In the previous section, it has been said that the MPP of a PV module continuously varies because of unstable atmospheric conditions such as ambient temperature, solar irradiation and shading effects of the surrounding objects. For an efficient photovoltaic system, the MPP of the PV module should be tracked in order to transfer the maximum possible energy obtained from the sun to the load which is called maximum power point tracking (MPPT). There are a great number of MPPT methods designed for this purpose. Some of the well known MPPT techniques are listed below as:

- Constant voltage method
- Open circuit voltage method
- Short circuit current method
- Perturb & observe method
- Incremental conductance method

2.1.2.1 Constant Voltage Method

Constant voltage (CV) method is the simplest MPPT method in the literature. This method uses a fixed reference voltage V_{REF} in order to track MPP of the PV module. This reference voltage value is calculated according to the I-V characteristics of the PV module and set to a value which is supposed to be MPP [7]. While implementing this method it is assumed that the atmospheric conditions such as temperature and solar irradiation are constant which leads to a mismatch between actual MPP and calculated MPP causing loss of solar power. The only need for PV module voltage to be sensed makes CV method very simple and economic as well. In some instances temperature sensitive NTC thermistors are being used connected to the control network in order to make V_{REF} value temperature dependent [8].

2.1.2.2 Open Circuit Voltage Method

This method of MPPT uses the linear dependency of open circuit voltage V_{OC} of a PV module to the V_{MPP} voltage in varying atmospheric conditions. In order to specify V_{OC} to V_{MPP} ratio, experimental studies must be performed. In (2.2), the relation between V_{OC} and V_{MPP} can be seen. "*a*" is the proportionality constant and defines the ratio between V_{OC} and V_{MPP}. In general, *a* varies between 0.71 and 0.78 according to the characteristics of the PV module [9].

$$V_{MPP} = a \times V_{OC} \tag{2.2}$$

In order to determine V_{MPP}, V_{OC} voltage value must be measured periodically. Under favor of a static switch connected in series with the PV module, V_{OC} can be measured and by multiplying it with *a* constant, V_{MPP} can be calculated [7]. Besides this, when the switch is opened the circuit, no power can be transferred to the load causing temporary power losses.

2.1.2.3 Short Circuit Current Method

Short circuit current method provides MPP current (I_{MPP}) information to the controller. As is the case with open circuit voltage method, I_{SC} and I_{MPP} of a PV cell has a linear relationship as it is seen in (2.3).

$$I_{MPP} = b \times I_{SC} \tag{2.3}$$

"*b*" is the linearity constant determining the ratio between I_{MPP} and I_{SC} and in general it varies between 0.78 and 0.92 [9]. A drawback of this method is that, in order to measure I_{SC} , a short circuit condition must take place which causes the output voltage of PV module to be zero, causing the control circuit of the converter connected to the PV to be fed by another voltage source. On the other hand, due to the short circuit case, output power of PV module temporarily equals to zero which causes power loss and due to the current measurement requirement, current sensors must be used which increase overall cost of the system.

2.1.2.4 Perturb & Observe (P&O) Method

P&O method is one of the most prevalent MPPT techniques because of its simplicity and high accuracy. This method of MPPT tracks maximum power by continuously perturbing voltage (current) reference value and observing the sign of the alteration of instant PV module power with respect to previous power. After a perturbation step, if PV module power and output voltage increases, which means the actual operating point is on the left hand side of the MPP, perturbation continues in the same direction. On the other hand, if PV module power increases and output voltage decreases, this means that the actual operating point is on the right hand side of the MPP and the direction of the next perturbation step will be in the opposite direction. Likewise, the direction of the perturbation step is decided according to the output voltage value for decreased module power condition. The flowchart of P&O method is shown in Figure 2.6. This method can effectively track MPP of PV module when the atmospheric conditions are constant and is not dependent of the I-V characteristics of the module which means that same algorithm can be applied to various PV modules. But it also has some drawbacks causing power losses.

Determining the perturbation size is very important in order to have an efficient system. If perturbation size is high, the MPP of PV module can be determined by the algorithm very fast but it causes fluctuations around MPP with high magnitudes causing power losses. At the same time fast perturbation increases noise ratio of the measured current. On the other hand if perturbation size is set to a small value, the determination of MPP will be very slow according to rapidly changing atmospheric conditions which causes severe power losses and also wrong decision of perturbation direction, decreasing the system effectiveness [5]. In order to prevent these drawbacks arising from perturbation size selection, variable step size methods can be used [10]. In these methods, variable perturbation step sizes are used with two or more stages . If the actual operating point is far from MPP, perturbation step size is kept high in order to rapidly access MPP area. After reaching MPP area step size will be decremented in order to prevent high amplitude fluctuations around MPP [7][9].

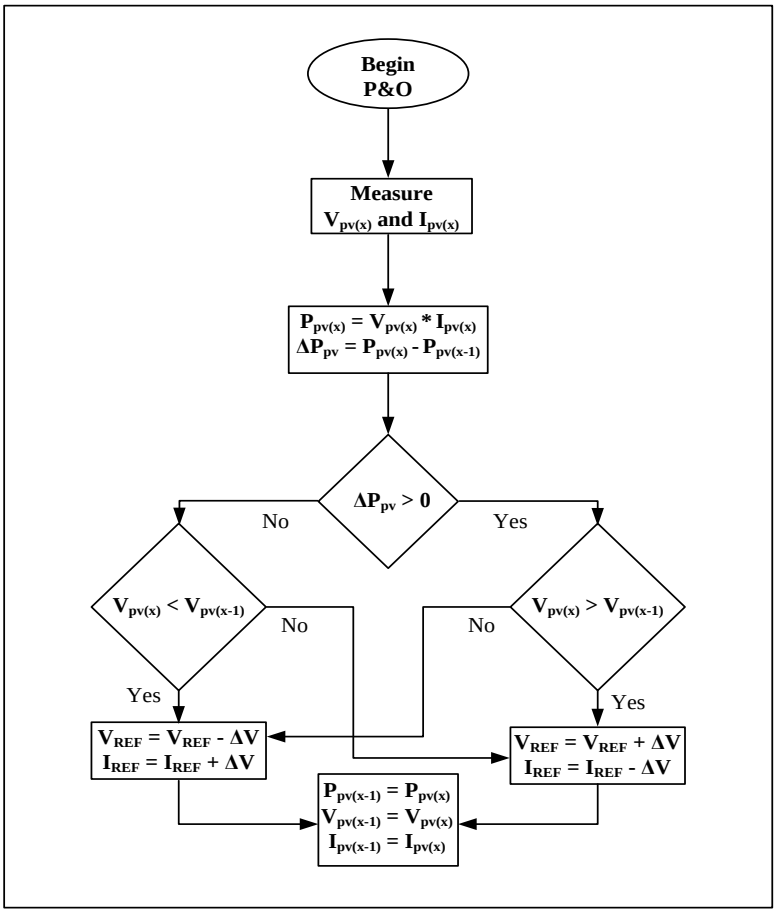

Figure 2.6 P&O method flowchart**.**

Another drawback of this method is the possibility of performing a wrong perturbation direction because of rapidly changing atmospheric conditions. In other respects, in an afford to measure the input voltage and current, sensors will be needed which increases system cost. Certain designers use different converter topologies which eliminate utilization of sensors reducing system cost [11].

2.1.2.5 Incremental Conductance Method

Incremental conductance (IC) method lies on the instruction that the slope of the P-V curve is equal to zero when actual operating point is equal to MPP [9]. It is positive if operating point is on the left hand side of MPP and negative on the right hand side which is shown below in (2.4), (2.5) and (2.6).

$$\frac{dP}{dV} = \frac{d(VI)}{dV} \tag{2.4}$$

$$\frac{d(VI)}{dV} = I\frac{dV}{dV} + V\frac{dI}{dV} = I + V\frac{dI}{dV} \tag{2.5}$$

$$\text{At MPP,} \quad I + V\frac{dI}{dV} = 0, \qquad \frac{dI}{dV} = -\frac{I}{V} \tag{2.6}$$

According to the equations above, $\Delta I/\Delta V$ is equal to -I/V at MPP, $\Delta I/\Delta V$ is greater than -I/V on the left hand side of MPP and $\Delta I/\Delta V$ is smaller than -I/V on the right hand side of MPP. In accordance with this comparison, voltage or current reference is incremented or decremented. I/V ratio is called conductance and $\Delta I/\Delta V$ ratio is known as incremental conductance which forms the name of the method.

IC method determines the MPP of PV module and the actual operating point of the system stays at this point as long as there is no change in temperature, solar irradiation or shading conditions which make changes on ΔI . By means of this method the oscillation problem of P&O method is solved unless the increment step size is too large causing oscillations around MPP. Some of the IC methods also have variable increment size in order to provide fast tracking of MPP and prevent oscillations around MPP [12].

When the operating point is far from MPP, increment size is large and if operating point is close to MPP, a smaller increment size is used. The flowchart of IC method is shown in Figure 2.7. There are also certain drawbacks of this method. Just as in P&O method, while implementing IC method, PV module voltage and current have to be measured in order to achieve MPPT.

Voltage and current sensors significantly increase the cost of overall system. On behalf of economise on the cost of the system, converter topologies without current and voltage sensors are being used. Another drawback of this method is increased control complexity.

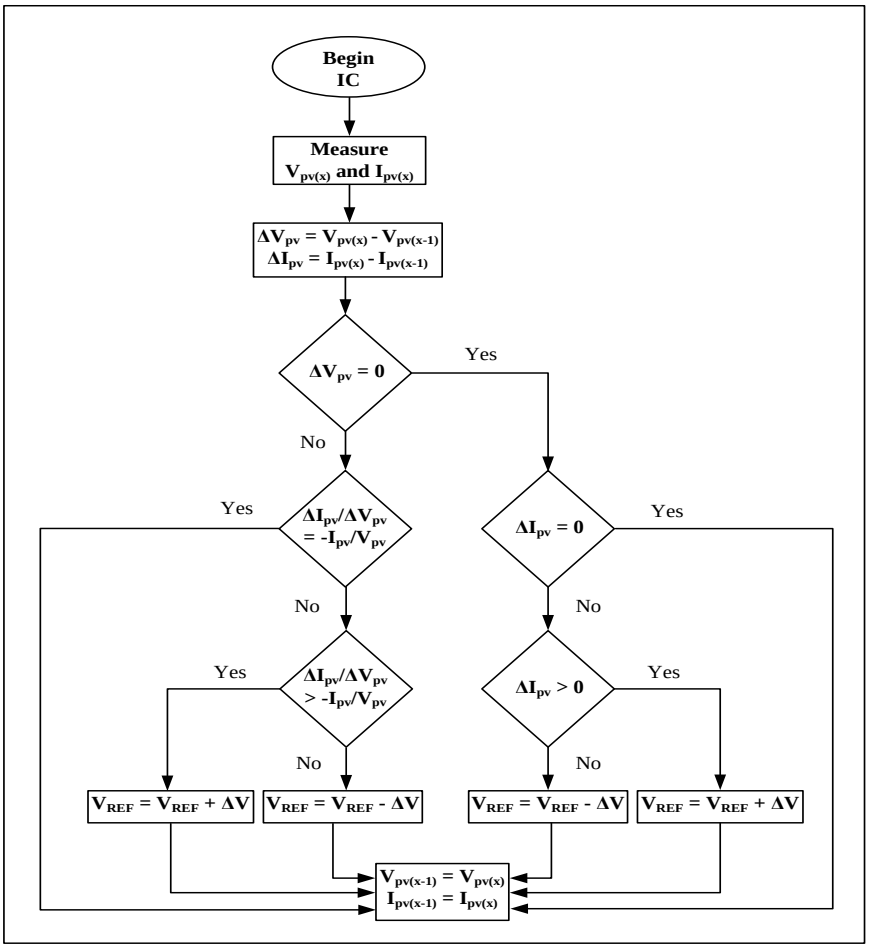

Figure 2.7 Incremental conductance method flowchart [9]**.**

2.1.3 PV Inverters

At the present time, PV systems are substantially implemented with grid connection and the generated energy is sold with a good prize. In this manner, both clean energy is produced and the financier of the PV system economically derive a profit. In grid-connected PV systems, as one of the most important part of the system, the number of inverter oriented researches are rising very fast for the purpose of reducing the cost and the payback period, increasing efficiency and reliability of the system. For today's technology, grid-connected inverters can be classified according to the historical development process as 1) Centralized inverters, 2) String inverters, 3) Multi-string inverters and 4) Micro-inverters (Module integrated inverters, MII) as shown in Figure 2.8 [5].

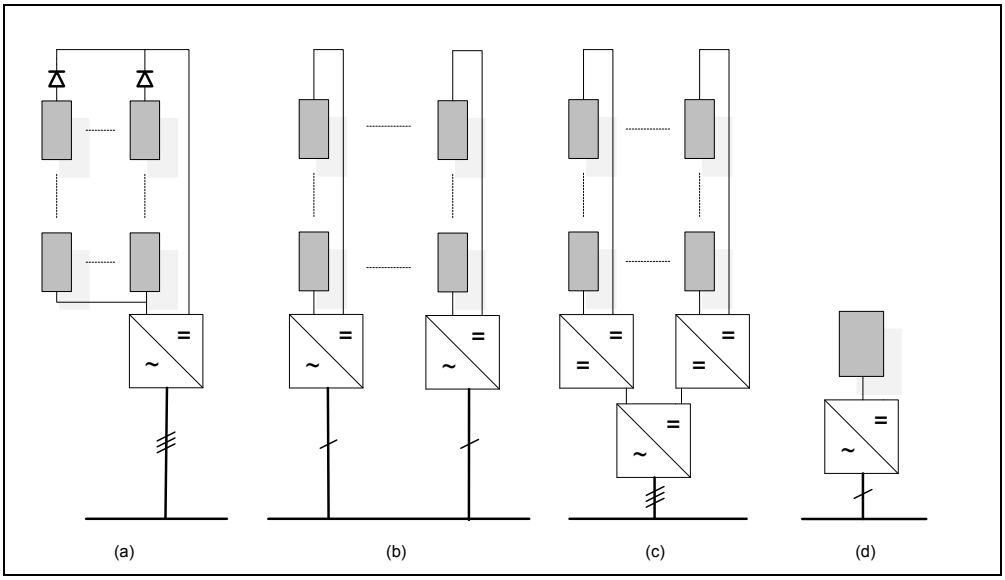

Figure 2.8 Inverters used for grid-connected PV systems (a) Centralized inverter (b) String inverters (c) Multi-string inverters (d) Micro-inverters (MI) [5]**.**

2.1.3.1 Centralized Inverters

Centralized inverters were the first developed inverter types in the literature which can be seen in Figure 2.8(a). In this type of PV systems, in order to reach high voltage levels such as 700V - 1kV, a number of PV modules are connected in series which forms a string. Under favor of paralleling these strings with string diodes, high power capacities can be achieved. The purpose of a centralized inverter is to transfer high voltage DC electricity generated by PV modules to three or one phase grid by transforming it into grid level AC electricity. Because of the series connection of PV modules, the same current passes through all panels of a string. Partial shading situation comes into prominence at this point. In common with the PV cells, when a partial shading case take place on a PV module, the current generated by the shaded module will be diminished making the module a power consumer instead of power generator. On the other hand, the un-shaded modules will keep power generation which forces the current passing through the shaded cell causing it to be overheated and even damaged. In an effort to prevent PV module damage, bypass diodes are used creating an alternative path to the current generated

by un-shaded cells and deactivating the shaded module. This procedure prevents overheating and damage but causes power loss by completely deactivating shaded modules.

As it is discussed before, in order to generate the maximum possible energy from PV module, MPP must be tracked continuously. Centralized inverters are achieving system level MPPT which causes power mismatch between PV modules when a partial shading condition occurs. Some of the disadvantages of centralized inverter systems are utilization of specially designed DC protection equipments with high costs, high switching and conduction losses of semiconductor devices with high voltage and current ratings and impossibility of enlarging the system capacity at will because of the limitation of centralized inverter capacity. These problems comes into prominence especially for low power implementations such as residential applications. Alternative inverter technologies arise in process of time in order to develop more efficient PV systems.

2.1.3.2 String Inverters

The first alternative PV inverter technology taking the place of centralized inverter was string inverter which is shown in Figure 2.8(b). Unlike centralized inverters, PV systems with string inverters include PV module strings with a single-phase inverter connected to each string. By means of strings having individual inverters, MPPT operation can be achieved with string level instead of system level mitigating the effect of power mismatches between PV modules of the whole system but not preventing power mismatches between PV modules of the same string. Conduction and switching losses are decreased with decreasing voltage and current ratings. Removing string diodes from the system decreases overall cost and losses. Also by adding a new string inverter, power capacity of PV system can be increased providing a more flexible system than central inverter system with limitations. Beside these advantages, the use of specially designed DC protection equipments and DC cabling with high costs, power mismatches between PV modules of the same string and conduction and switching losses are still valid for string inverters especially for residential applications which leads to further studies on PV inverters.

2.1.3.3 Multi-String Inverters

As it is seen from Figure 2.8(c), every string has its own DC-DC converter which achieves MPPT operation and also makes possible to form strings with different numbers of PV modules providing flexibility to the system. DC-DC converters are connected to a single inverter achieving DC-AC transformation and three phase grid connection of the system. However, DC cabling and use of DC protection equipments still increase system cost.

2.1.3.4 Micro-inverters (MI)

At the present time, micro-inverter is one of the most newsworthy PV inverter technology. By means of individual micro-inverters connected to each PV module, DC electricity generated by the module is transformed into the single-phase AC electricity with grid connection as it is shown in Figure 2.8(d). In accordance with the power capacity of a PV module, micro-inverters have 100-300W power capacities. By virtue of low power capacities, micro-inverters have a compact structure which gives the possibility to integrate it into the back of a PV module achieving a single solar module. A micro-inverter integrated into the back of a PV module can be seen in Figure 2.9. Individual inverters connected to PV modules offers the possibility of flexibility, PV module level MPPT operation, use of traditional protection equipments operating with AC electricity and elimination of high voltage DC wiring.

By means of various different advantages, utilization of micro-inverters, especially for residential applications of energy capacities with 3-5kW and less, becoming widespread day by day. Increasing number of researches, in order to develop more efficient and economical micro-inverter systems, and micro-inverter producers shows increasing popularity of promising micro-inverter technology. In this study, micro-inverter systems with two different topologies are implemented.

On the other hand, the efficiency of the micro-inverters are still 1-2% lower than central inverters and for the micro-inverter systems having power capacities larger than 5-6kW, system cost and AC cabling losses increases.

Figure 2.9 A micro-inverter integrated into a PV module [13]**.**

2.2 Benefits of Micro-inverters

Especially for residential PV applications with power capacities of 3-5kW and less, micro-inverter technology has various advantages over the other inverter types making micro-inverters very popular. In this chapter these benefits will be discussed. Some of the important specialities of micro-inverters can be listed as follows:

- PV module level MPPT
- AC transmission
- Flexible structure
- Optimization & continuity
- Economics

2.2.1 PV Module Level MPPT

In a PV micro-inverter system, every PV module has its own inverter forming a solar module together. In order to install a PV system with a certain power capacity, these solar modules are connected in parallel as it is shown in Figure 2.10.

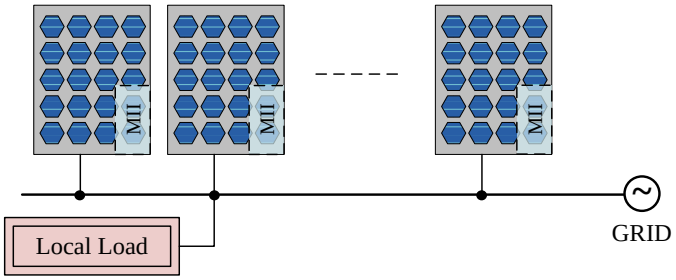

Figure 2.10 Grid-connected solar modules consisting of PV module and a micro-inverter.

By means of individual micro-inverters integrated into each PV module, module level MPPT can be implemented which prevents the power mismatch between modules occurring because of partial shading or pollution. In other words, module level MPPT gives the opportunity to the PV module effected by partial shading or pollution that, in any case maximum possible energy will be generating without being a consumer or completely disabled from the system. As a result, micro-inverters increase system efficiency and prevent PV module to be damaged and as distinct from the other inverter technologies, maximum possible energy generation from the panel is achieved for any physical condition.

2.2.2 AC Transmission

Differently from micro-inverters, the inverters explained above use DC wires in order to transfer DC electricity generated by PV module. Up to a certain power level, DC wires carrying high current cause conduction losses which decreases the efficiency of the system [5]. Micro-inverters transform and amplify low voltage DC electricity to grid level AC electricity right behind the PV module dispensing the need for DC wires carrying high current and high voltage making the system more effective. On the other hand, as it is discussed before, DC wiring makes it essential to use specially designed DC protection equipments which increase the overall cost of the system. The risk of arcing also increases with high voltage DC wires because of stiff environmental conditions causing physical deformations such as corrosion or abrasion. Using AC wires provides the system to be more economical and reliable.

2.2.3 Flexible Structure

In order to minimize the conduction losses taking place due to DC wiring, PV modules must be located very close to each other for centralized and string inverters. In spite of this, for residential applications, available area for installation may be distributed. Under these circumstances, the energy requirement of the building, available area for installation, required capacity of inverter and PV module count must be calculated very carefully. The complexity of installation makes the time taken for the installation to be extended and brings on the need for well educated employees, which causes financial problems. In addition, after the installation of PV systems with centralized or string inverters, the extension of energy capacity of the system by adding extra PV modules becomes a serious problem because of the limited power capacity of the inverter and available area causing additional calculations and time which increases the system cost effectively.

In contrast with this, without DC wiring, module integrated inverters can be distributed to the available areas of the building and grid connection can be achieved at any point by means of AC electricity wiring of the building as it is shown in Figure 2.11. Even smallest suitable areas can be used and the system can be enlarged easily without any calculation and need for educated employees. Instead, even the consumer can perform the installation which considerably decreases the system cost.

2.2.4 Optimization & Continuity

Centralized and string inverters have significant power ratings making it easy to standardize the production. In contrast with this, proper area for PV system installation on a building is limited which makes it necessary to calculate required power capacity of an inverter. For this reason, it is hard to find suitable inverter with rated power feasible for the PV system. Due to the utilization of an inverter with a power capacity considerably larger than the PV system causes the inverter to operate inefficiently under light load condition. None the less, if an inverter with smaller power capacity than potential of the area utilized, the effectiveness of the system will be very low. In any case system cost increases and efficiency decreases considerably.

Figure 2.11 Distributed PV systems with micro-inverters [13].

Due to the module integrated inverters with power capacities feasible with PV modules, there is no need for feasibility studies and optimization will be provided easily without complex calculations.

On the other hand, if a major malfunction occurs during the operation of the system, for centralized inverters the whole system, for string and multi-string inverters a great portion of the system will be lost.

If a micro-inverter has a malfunction, the power lost will be quite few in accordance with the whole system which allows the system to continuously generate solar power increasing the system efficiency and reducing the payback period of the system. The mean time between failure (MTBF) rate of an inverter is determinant for an economical PV system. MTBF rate of a centralized inverter is 10-15 years, but nonetheless, MTBF of a micro-inverter can reach almost 300 years which is allowing a continuous power generation [13].

2.2.5 Economics

The most important factors effecting the choice of a consumer for the installation of a PV system is the payback period of the system and the margin of the profit.

Determination of these factors are dependent on the area of installation. Electricity cost, the amount of the fund which will be paid for the generated PV power and system costs are highly effective parameters that must be considered. System costs can be divided into three sections as;

- Basic costs
- Energy generation capacity
- Maintenance and repair costs

The installation cost together with the cost of PV modules and inverters of a system form basic costs of a PV system. By taking into consideration the cost of inverters, micro-inverter costs are higher than string and central inverters because of their low power capacities. The cost of a string inverter is around 0.5$/Wp, however, the cost of a micro-inverter is around 0.75$/Wp. Therefore, the cost of micro-inverter for a 7kWp PV system is 10% more than the cost of string inverter system with the same power capacity [14]. In other respects, when the installation cost is taken in to consideration, micro-inverter systems are much more economical with respect to the other inverter systems as it has been mentioned before. DC wire with high current ratings, switchboards and DC equipments, long installation periods, the need for well educated employees increase the cost of overall system operating with centralized or string inverters.

With respect to the simple instructions prepared by the supplier, installation of module integrated inverters can be done easily by means of plug-N-play feature of micro-inverters by the consumer without education and with standard AC equipments which reduces the installation time and cost.

When the installation time and workmanship of installation are considered, it is seen that, the installation cost of micro-inverter systems is 20-25% cheaper than string inverter systems which means the basic cost of a micro-inverter is nearly 10% cheaper [14].

Energy generation capacity of a PV system is another important issue which must be considered in detail. It is expected from a PV system that under different environmental conditions energy generation must be achieved with minimum lost and maximum continuity. According to a study experimented with 8kW micro-inverter and string inverter PV systems under 78 different partial shading conditions, it is observed that, PV system with micro-inverters recovers 50% of energy loss of string inverter during one year [15]. At the same time, it is observed that at low percentage partial shading conditions (7%), micro-inverters can generate 3,7% more energy than string inverters. In the event of intermediate percentage shadings (15-19%) and high level shadings (25%), micro-inverters generate 7.8% and 12.3% more energy than string inverters [15]. In this manner, it is seen that, under shading conditions PV systems with micro-inverters can utilize the sun light in a more efficient way. In recent years, by means of technological developments, the efficiencies of micro-inverters are considerably improved.

Despite these improvements, only 94-96% efficiency levels are achieved while string inverters can have efficiency levels up to 98%. Besides this, under favor of efficient energy use of micro-inverters, over the long run, micro-inverter systems become more economical. For example, according to a study the payback period of a 3kW PV system with micro-inverters is 5 years shorter than a PV system with string inverters [16].

The maintenance and repair costs considerably effect the overall cost of a system. Life time and reliability of a system are determinant factors influencing the maintenance and repair cost. The lifetime of a PV module is generally 25 years [29]. In order to have an efficient system, inverters of PV systems must have the lifetime of a PV module. The most important parameter determining the lifetime of an inverter is the type of decoupling capacitors placed on the DC bus of inverter topology in order to keep voltage ripple at a certain level.

For the purpose of reducing voltage ripples, electrolytic capacitors must be used. The lifetime of an electrolytic capacitor is highly effected from the ambient temperature. The ambient temperature at the back side of a PV module can reach

nearly 85 °C. At this temperature the lifetime of an electrolytic capacitor can be reduced to 20000 hours which is shorter than the lifetime of a PV module [17]. Instead of using electrolytic capacitors, certain inverter topologies give the opportunity to use film capacitors which have longer lifetime with the aid of power decoupling circuits [21][22][23].

In the event of film capacitor use, the lifetime of a micro-inverter approaches to the lifetime of a PV module. In the opposite case, a shorter lifetime causes the inverters to be exchanged at least one time during the lifetime of a PV module and reduces the efficiency and increases maintenance costs.

Another important factor effecting the preferability of a system is reliability. In accordance with an experiment performed in North America from 2008 to 2010, the failure rate of micro-inverters is 0.207% (22/10,630) , however, the failure rate of string inverters is 9.43% (318/3,373) [13]. By this way, even the system costs of micro-inverters and string inverters are considerably close, for residential applications with 3-5kW power capacities and less, in the long term, it is observed that micro-inverters are more reliable and cost effective.

2.3 Grid Connection Demands

Since the MIs are designed to be grid-connected, the specifications of the connection must fulfill the requirements stated in the standards such as, IEC 61727 stating the characteristics of the utility interface, EN 50438 stating the requirements for the connection of micro-generators in parallel with the European public low-voltage distribution networks, IEC 61000-3-2 stating the harmonic current limits, IEC 61000-6-3 for electromagnetic emission, IEC 61000-3-3 for voltage fluctuations, etc [24][25][26][27][28]. The design parameters of the implemented MI topologies are selected according to the statements in the standards written above. In the next sections, some of the specifications of the standards are indicated.

2.3.1 Over/Under Voltage

Since the utility grid has a nominal voltage, it can be variable over time in accordance with the power generation and load conditions within certain limits stated in the standards. The inverter must operate between over/under voltage limits without any problem. In addition, in an attempt to fulfill the safety requirements, the inverter must cease operating when the grid voltage deviates outside the specified limits in a given time period stated in Table 2.2.

Table 2.2 Over/under voltage limits [24]

Voltage	Maximum trip time (sec)
$V < 0.5 \times V_{nominal}$	0.1
$50\% \leq V < 85\%$	2.0
$85\% \leq V < 110\%$	Unlimited operation
$110\% < V < 135\%$	2.0
$135\% \leq V$	0.05

2.3.2 Over/Under Frequency

As is the case with the grid voltage, there are over and under frequency limits stated in the standards. According to IEC 61727, the inverter must operate without ant problem when the grid frequency is within the range of ±1 Hz. If the frequency deviates outside of the limits, the inverter must cease to transfer energy to the grid within 0.2 seconds [24].

2.3.3 Current Harmonics

Since lower harmonics and distortions of currents and voltages are desired, there are also specified limits for the harmonic contents of the current injected to the utility grid. The limits for total harmonic distortion and for each individual harmonics are stated in Table 2.3.

Table 2.3 Distortion limits [24]

Harmonic order (h) (odd harmonics)	Distortion limit
THD	5%
3^{rd} through 9^{th}	< 4.0%
11^{th} through 15^{th}	< 2.0%
17^{th} through 21^{st}	< 1.5%
23^{rd} through 33^{rd}	< 0.6%
above 33^{rd}	< 0.3%

In addition to the limits stated in the table, the even harmonics in these ranges shall be less than 25% of the odd harmonic limits [24].

2.3.4 Average Power Factor

The limit for the lagging average power factor of the PV system shall be greater than 0.9, when the output power is greater than 50% of the nominal power [24]. In order to fulfill the PF requirements stated in the standards, the inverters are designed so that the power factor will be close to unity.

2.3.5 Anti-Islanding Operation

The islanding occurs when the utility grid voltage and frequency deviates outside of the specified limits stated in Section 2.3.1 - 2.3.2 and the inverter still continues to transfer energy to the grid. The islanding operation can be hazardous for the utility workers who do not know that the line is energized during the maintenance and repair operation. In order to prevent such accidents, the inverter shall stop operating when the grid voltage and frequency deviates outside of the specified limits in a certain time period [24].

2.4 Production and Utilization of MI Systems in the World and in Turkey

As it has been mentioned before, the number of producers entering the micro-inverter market is increasing day by day. It is indicated that, in the third quarter of 2012, some of the micro-inverter companies enhanced their income by 55 million $

with 36% rate of growth [13]. Due to the increasing market size, worldwide companies started to enter micro-inverter market. Furthermore the installed capacity of MI systems grows every day all over the world. According to a research, the market share of micro-inverter systems is expected to be 1.7 billion $ by the year 2016 [5].

In Turkey, in spite of high potential, there is not enough evolvement of neither production nor installation. The basic reasons of this condition are high taxes come into existence because of being an imported product preventing the technology to be widespread. The residential PV applications are not common in Turkey yet. This circumstance causes the micro-inverter technology to remain hidden. On the other hand, with the aid of more economical systems, investors will drive considerable profits which will make residential PV applications and micro-inverters more popular in the future. Significant investments needed in order to enhance the number of R&D studies.

2.5 Summary

As one of the most popular photovoltaic energy conversion systems, micro-inverters are becoming more effective with advantages of module level MPPT minimizing the shading effects, AC transmission allowing to use conventional AC protection equipments lowering the cost of the system, flexible structure giving opportunity to utilize every single appropriate area of installation and to enlarge the whole PV system at will increasing mass production, optimization and continuity minimizing the effects of failures and allowing continuous energy production for all atmospheric conditions, low installation, maintenance and repair costs reducing the payback time period of the PV system. On the other hand the drawbacks such as high micro-inverter cost because of low power capacities, efficiency of 94-96% which is lower than the efficiencies of string and centralized inverters, complex control structure, low power capacities make it necessary to do scientific researches and make improvements in order to have more efficient, low cost, reliable PV micro-inverter system.

CHAPTER 3

MICROINVERTER TOPOLOGIES

In order to operate effectively under partial shading and pollution conditions, in the literature there are a great number of micro-inverter topologies which convert 25 V – 50 V DC PV module voltage to 220 V_{rms} / 50 Hz (European) or 120 V_{rms} / 60 Hz (American) AC voltage and achieve grid connection with synchronization [18]. Galvanic isolation between PV module and micro-inverter is very important because of the safety concerns. For this reason, for micro-inverter applications, topologies with transformers are used. In Figure 3.1, the internal structure of a micro-inverter is shown. This structure includes input and output filters, DC-DC voltage amplifier stage with transformer, inverter stage, and controller achieving MPPT and PLL operations.

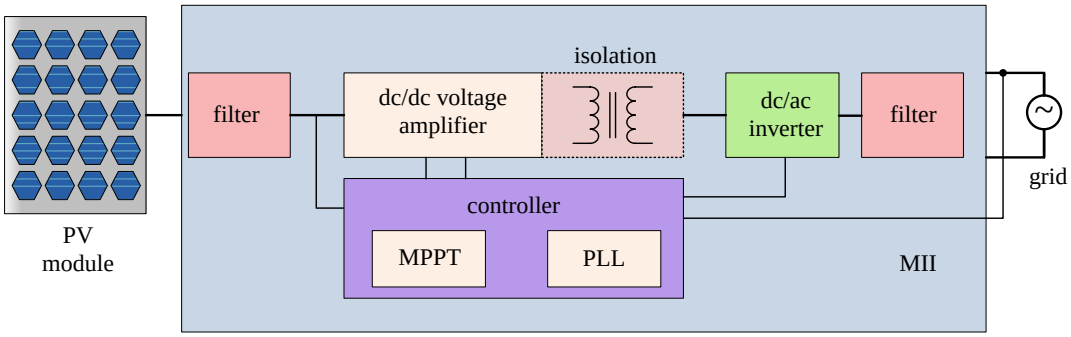

Figure 3.1 Internal structure of a micro-inverter.

Micro-inverter topologies analyzed in this study are classified according to their DC-link configurations as [19]:

- Micro-inverters with DC-link
- Micro-inverters with pseudo DC-link
- Micro-inverters without DC-link

Before explaining MI topologies in detail, an important phenomena called power unbalance and power decoupling which considerably influences the lifetime and efficiency of MI and other single-phase PV inverters will be discussed. Afterwards, popular MI topologies will be classified and compared. Finally commercially used MI topologies will be listed.

3.1 Power Unbalance and Power Decoupling

While PV modules generate DC electricity, utility grid operates with AC electricity. Consequently, MI constitutes interface between PV module and the grid. In steady state operation, while instantaneous input power is constant, power transferred to the grid fluctuates in duplicate of grid frequency as shown in Figure 3.2.

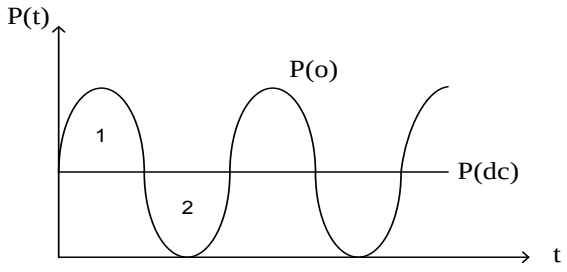

Figure 3.2 Instantaneous input power P_{dc} and instantaneous output power P_o of MI.

PV module power can be written as;

$$P_{pv} = V_{pv} \times I_{pv} \tag{3.1}$$

where, V_{pv} and I_{pv} are voltage and current of the PV module.

Due to sinusoidal current injected to the grid, output power of MI is time varying which is given by;

$$P_o(t) = V(t) \times I(t) = V \sin(w_o t) \times I \sin(w_o t + \emptyset) \quad (3.2)$$

where, ω_o is the grid frequency and Φ is the phase difference between grid voltage and injected current which is equal to zero since unity power factor is expected. In that case instantaneous output power can be rewritten as;

$$P_o(t) = \frac{1}{2}VI + \frac{1}{2}VI\cos(2w_o t) \quad (3.3)$$

As it is seen from (3.3), instantaneous output power consists of two terms. 1st term is the average of output power which is constant and 2nd term is the time varying part of output power fluctuating in duplicate of grid frequency.

In a lossless system, average of the output power is equal to the controlled PV module power P_{pv} (VI/2 = P_{pv}). Besides this together with the time varying oscillation, an instantaneous power mismatch between input and output power arises. For the purpose of handling this power mismatch, capacitors are used as energy storage devices and the name of this procedure is called power decoupling [20].

As it is seen in Figure 3.2, when the input power is greater than the instantaneous output power as it is indicated in region "2", extra energy is stored in the decoupling capacitor. On the other side, when instantaneous input power is less ,as it is indicated in region "1", the energy stored in decoupling capacitor is transferred to the output which balances the power mismatch between input and output. In order to achieve power decoupling effectively, the value of the decoupling capacitor must be calculated very carefully. This value is dependent on the topology used and the region the capacitor placed in the circuit.

From equation (3.3), the difference between input and output power can be given as;

$$\frac{1}{2}VI\cos(2w_o t) = Ppv\ \cos(2w_o t) \quad (3.4)$$

The amount of energy decoupled to the capacitor in an interval of one half cycle, can be found by integrating one of the numbered areas in Figure 3.2 given by;

$$E = 2 \times \int_0^{T/8} Ppv \cos(2w_o t) = \frac{1}{2} C_D \left(V_{CD\_max}^2 - V_{CD\_min}^2\right) \quad (3.5)$$

where C_D is decoupling capacitance, V_{CD_max} and V_{CD_min} are maximum and minimum capacitor voltages.

From (3.5) the required decoupling capacitance can be written as;

$$C_D = \frac{Ppv}{(2\pi f_{grid} V_{CD}\, \Delta V_{CD})} \quad (3.6)$$

where f_{grid} is the grid frequency, V_{CD} is the average decoupling capacitor voltage and ΔV_{CD} is the ripple voltage which is V_{CD_max} - V_{CD_min}. As it is seen from (3.6), the required decoupling capacitance is a function of average and ripple voltages. According to the topology chosen, decoupling capacitor can be placed to the DC-link, between PV module and inverter or to the grid side. Due to the ease of implementation, decoupling capacitors are mostly placed between PV module and the inverter. In this case, the voltage rating on the decoupling capacitor is equal to the PV module output voltage which is typically around 35V. On the purpose of an efficient use of PV module energy, the ripple on the PV module voltage must be lower than 8.5% of the average PV module voltage. When these requirements are taken into consideration, it is seen that a large capacitance is needed. As an example of 200W PV system with 35V input voltage, 3V ripple voltage and 230Vrms/50Hz utility grid, the required capacitance will be around 6.1mF. This capacitance value can be reached only with electrolytic capacitors.

The most important drawback of electrolytic capacitors to be considered is the short lifetime. As it is mentioned before, on a sunny day, the temperature of PV module can reach around 85˚C and a micro-inverter integrated on the back of a module must

withstand this temperature. Increasing temperature considerably effects the capacitance of electrolytic capacitors used on the purpose of ripple cancelling by shortening its lifetime to 20000 hours [17]. On the other hand, within this time period, capacitance value of electrolytic capacitor decreases 15% and effective series resistance (ESR) considerably increases [17]. Shorter lifetime causes the inverters to be exchanged at least one time during the lifetime of a PV module and reduces the efficiency and increases system costs. In order to use small size capacitors, active power decoupling circuits are improved [20][21][22][23]. The purpose of these circuits is to make possible the usage of film capacitors which have longer lifetime than electrolytic capacitors.

On the other part, increased control parameters and semiconductor count effects the efficiency of the system. Different methods can be used such as placing decoupling capacitors at the DC-link or at the grid side in order to achieve power decoupling. While all methods have various benefits and drawbacks, selecting suitable topology and method is very important with the intent of having an efficient and long life PV system.

3.2 Micro-inverter Topologies

In order to have a good performance, micro-inverters must have high power density, high efficiency, reliability and low cost [19]. For the purpose of meeting these requirements, various micro-inverter topologies are developed. In this study, micro-inverter topologies are classified as follows;

3.2.1 Micro-inverters with DC-link

As it is seen from Figure 3.3, there is a DC-link between DC-DC converter, amplifying the PV module voltage to the levels compatible with the grid voltage and achieving MPPT, and the inverter which the power decoupling capacitor is placed at [19]. These topologies with DC-link are also known as multi-stage inverters which the voltage amplification, MPPT operation and sine shaped current generation is achieved with two or more stages. In this study, three micro-inverter topologies with DC-link are analyzed.

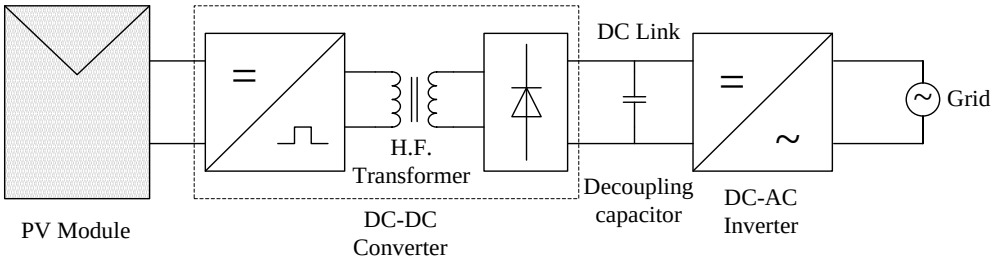

Figure 3.3 Structure of a micro-inverter with DC-link [19].

The topology seen in Figure 3.4 comes out of three stages. The first stage consists of a full-bridge connected to a high frequency transformer and a full-bridge rectifier. This stage is controlled with zero voltage switching phase shifted PWM. At this stage the PV module voltage is amplified to 475V and MPPT operation is succeeded.

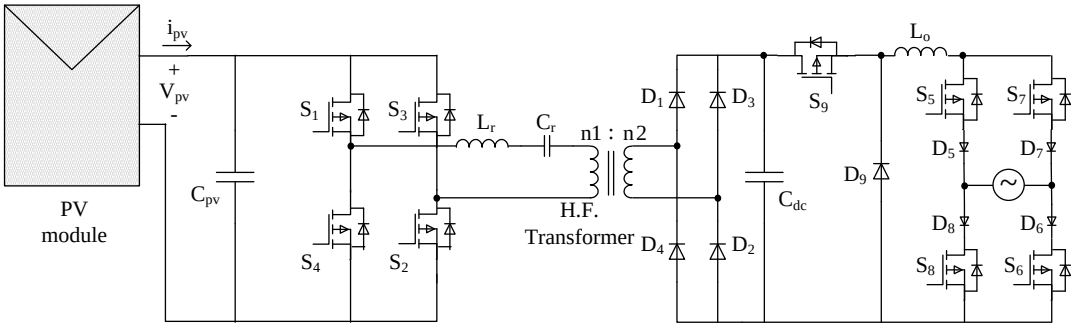

Figure 3.4 A topology consisting of full-bridge connected to a high frequency transformer and a full-bridge rectifier, a buck converter and a full-bridge inverter operating at line frequency [29].

The energy stored in a capacitor is proportional with the square of the voltage. By this means, the capacitance of the decoupling capacitor placed at 475V DC-link can be much lower than the capacitance of a capacitor placed at the input. Under these circumstances, micro-inverter topologies with high voltage DC-link voltages make it possible to utilize film capacitors with long lifetime instead of electrolytic capacitors. In this study, 8.2 µF film capacitor is used at the DC-link. Making use of

a film capacitor with low capacitance causes DC-link voltage to fluctuate with a large amplitude in duplicate frequency of a grid voltage. In order to control the output current properly, instantaneous DC-link voltage has to be greater than peak grid voltage. For this reason, the amplitude of the oscillation on DC-link voltage has to be limited and the selection of the capacitance of decoupling capacitor must be selected by taking these limitations into consideration. In this topology, decoupling capacitor size is selected so that the amplitude of the voltage ripple on DC-link voltage is 125V. The second stage consists of a buck converter which gives the current a rectified sinusoidal shape with current mode control. Finally the third stage consists of a full-bridge inverter that inverts rectified current into sinusoidal form operating at grid frequency. Simulation and experimental work of this topology with power capacity of 150W is achieved and reported euro efficiency is 85.4% [29].

In Figure 3.5, another micro-inverter topology with DC-link is shown. It consists of two stages of a high frequency transformer isolated boost-half-bridge DC-DC converter with a voltage doubler (D_1, D_2, C_3, C_4) on the secondary side of the transformer and a full-bridge pulse width modulated inverter [30][31].

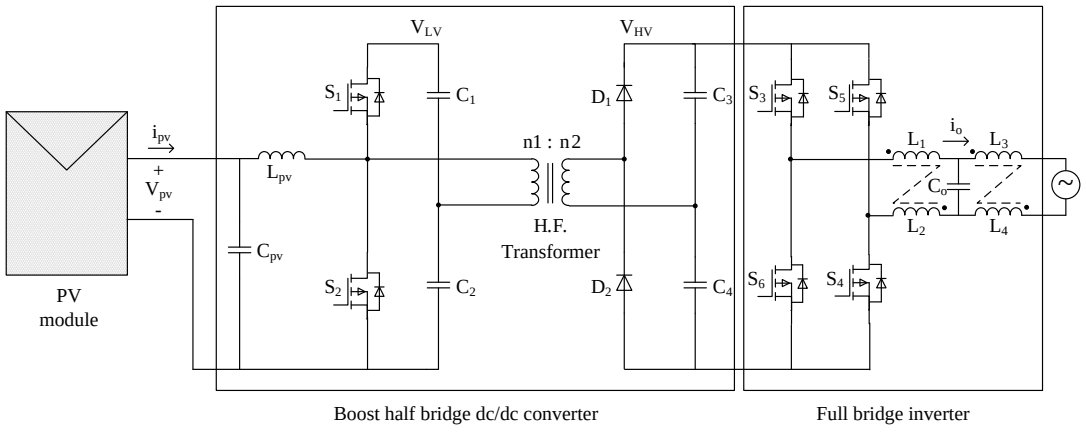

Figure 3.5 A topology consisting of high frequency transformer isolated boost-half-bridge DC-DC converter with a voltage doubler on the secondary side of the transformer and a full-bridge pulse width modulated inverter [30][31].

The first stage performs MPPT operation and voltage amplification. At the same time, with the aid of the leakage inductance of high frequency transformer, S_1 and S_2 MOSFETs are switched at zero voltage. On the other hand, by means of C_1, C_2, C_3 and C_4 capacitors, instantaneous voltage surge on the switches of boost half-bridge converter and diodes of voltage doubler is prevented. The DC-link voltage on the primary side of the high frequency transformer is 65V (V_{LV}) and the DC-link voltage on the secondary side is 380V (V_{HV}).

The second stage consisting of a full-bridge PWM inverter performs repetitive current control achieving sinusoidal current shaping. In Figure 3.6, the control structure of boost half-bridge DC-DC converter and full-bridge inverter.

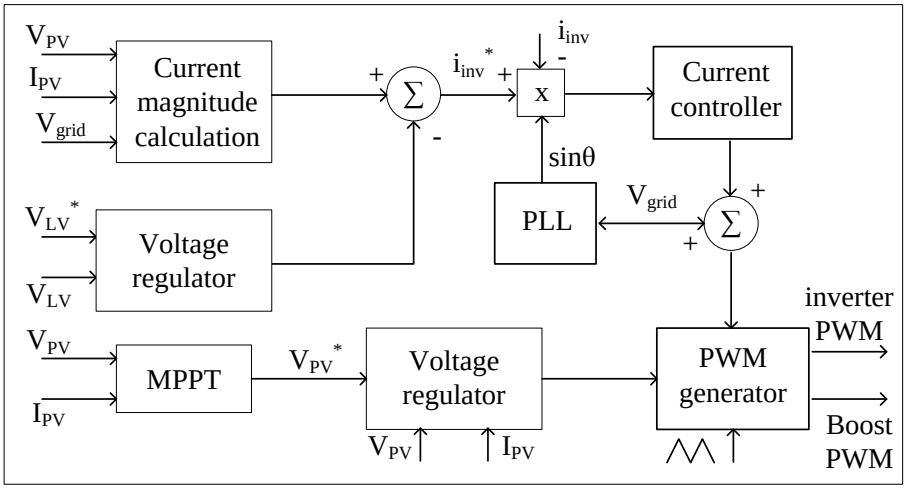

Figure 3.6 The control structure of boost half-bridge DC-DC converter and full-bridge inverter [31].

It is specified that the power capacity of the proposed topology is 210W and the highest efficiency of 95.6% is reported at 160W input power. On the other hand, the efficiency of boost half-bridge DC-DC converter is indicated as 97-98.2% on 30-50V input voltage.

The topology seen in Figure 3.7, comes out of two power stages [19][32]. The first stage is a resonant half-bridge dual converter. Besides this, in order to provide soft switching of S_1 and S_2 MOSFETs, L_r inductor and C_1 and C_2 capacitors are added to the circuit. The second stage is a full-bridge PWM inverter.

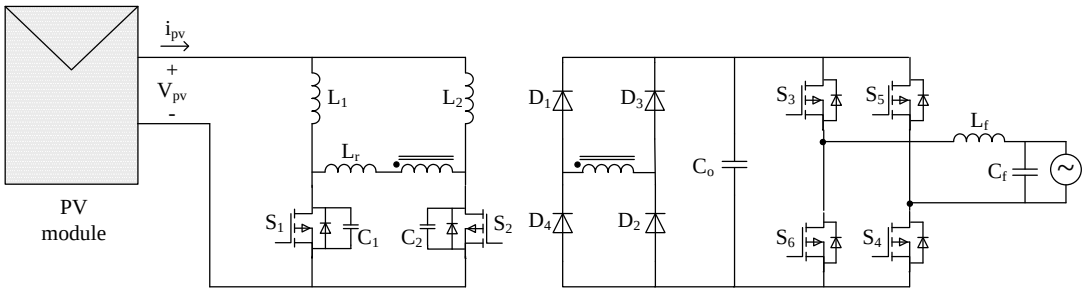

Figure 3.7 The control structure of boost half-bridge DC-DC converter and full-bridge inverter [32].

Simulation and experimental studies are achieved and the reported efficiency of a 100W prototype is 90% [19][32].

Based upon the proposed topologies, it is seen that micro-inverters having more than two stages have lower efficiencies due to the great number of semiconductors. Besides that, for micro-inverters with DC-link, placing the decoupling capacitor at high voltage DC-link gives the opportunity to use film capacitors with low capacitance increasing the lifetime of the micro-inverter.

On the other hand, using film capacitors with low values causes the DC-link voltage to fluctuate with a high amplitude in duplicate of grid frequency. These fluctuations lead to voltage stresses on electrical components of the circuit and make it difficult to control the output current properly. While selecting the value of the film capacitor, these circumstances must be taken into consideration.

3.2.2 Micro-inverters with Pseudo DC-link

Micro-inverters with pseudo DC-link, as it is shown in Figure 3.8, consist of DC-DC converter and an unfolding bridge operating at grid frequency [19]. The difference between micro-inverters with pseudo DC-link and micro-inverters with DC-link is that, DC-DC converter in pseudo DC-link configuration performs both MPPT and rectified sine current shaping operations. For this reason, micro-inverter with pseudo DC-link is also called single-stage inverter.

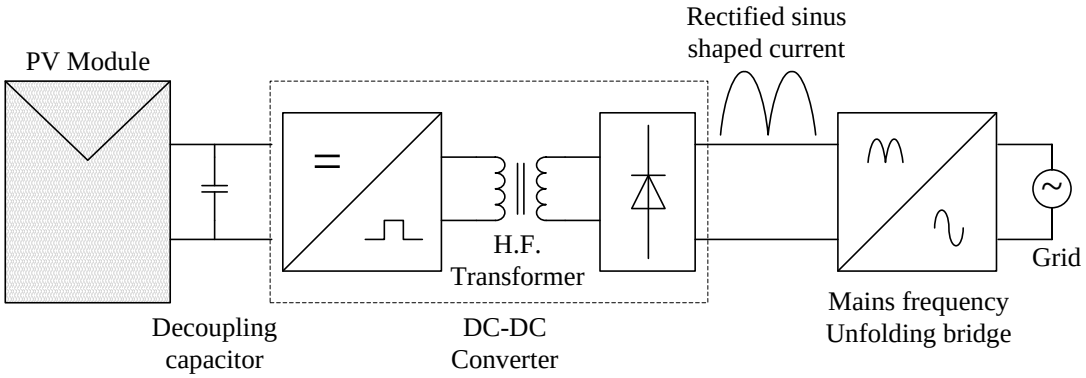

Figure 3.8 Structure of a micro-inverter with pseudo DC-link [19].

The function of mains frequency unfolding bridge is to invert the rectified current into sinusoidal shape and perform the grid connection. Because of the absence of a DC-link, power decoupling capacitors are placed at the input of the inverter in parallel with the PV module.

In the category of micro-inverters with pseudo DC-link, in an effort to make it possible to utilize film capacitors for power decoupling, active power decoupling circuits (APDC) are developed.

In Figure 3.9, a micro-inverter structure of a three port flyback converter with APDC consisting of two diodes, a MOSFET and a decoupling capacitor is shown [21].

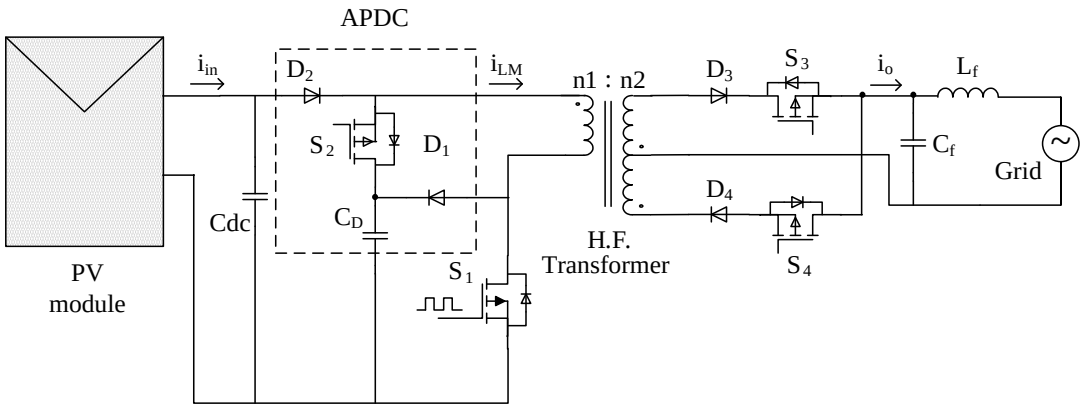

Figure 3.9 Three-port flyback-based micro-inverter with pseudo DC-link [21].

Three ports of the flyback converters are, PV module side achieving MPPT, APDC and the grid side isolated from the PV panel. C_D is used as energy storage device for power decoupling and at the same time recycles the energy of the leakage inductor increasing the system efficiency.

In this topology, as it is shown in Figure 3.10, when input power is greater than the instantaneous output power ($P_o(t)$) , (Mode 1), by means of turning on S_1, the energy is stored in the primary turns of flyback transformer (t_0 - t_1) and by turning S_1 off, the extra energy is stored in C_D through D_1 and D_2 (t_1 - t_2).

Afterwards, according to the polarity of the grid voltage, through turning S_3 or S_4 on, the energy stored in the transformer is transferred to the output (t_2 - T_s) where T_s represents the switching period. On the other hand, when the instantaneous output power is greater (Mode 2), the energy is stored in primary winding of the transformer through S_1 (t_0 - t_1).

Later on, the energy stored in C_D in Mode1 is transferred to the primary winding of the transformer through S_1 and S_2 (t_1 - t_2). Finally, according to the polarity of grid voltage, the energy stored in the transformer is transferred to the output through S_3 or S_4 (t_2 - T_s).

By means of discontinuous conduction mode (DCM) of operation, the efficiency of the inverter is improved under favor of preventing reverse recovery losses of output diodes and soft switching of MOSFETs.

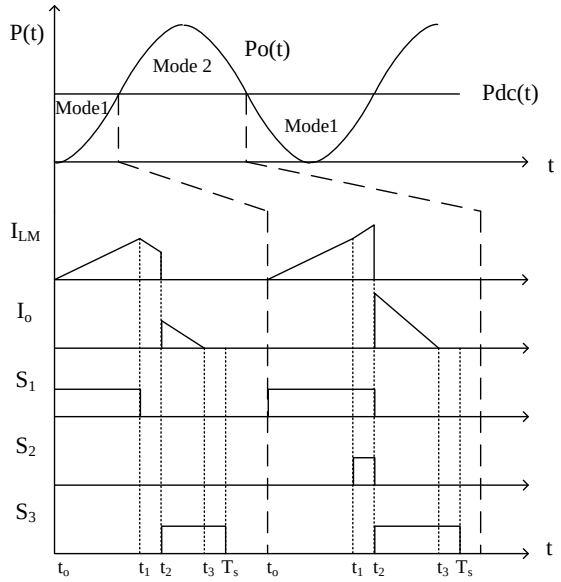

Figure 3.10 Current and switching signal waveforms of three-port flyback-based micro-inverter with pseudo DC-link [21].

According to the experiments performed with 100W prototype, the capacitance of the C_D is reported as 46μF while the efficiency information is not given [21].

The topology seen in Figure 3.11 has similar operating principles like the topology proposed in Figure 3.9. The difference is that, the primary winding of high voltage transformer is center tapped such in secondary winding [22].

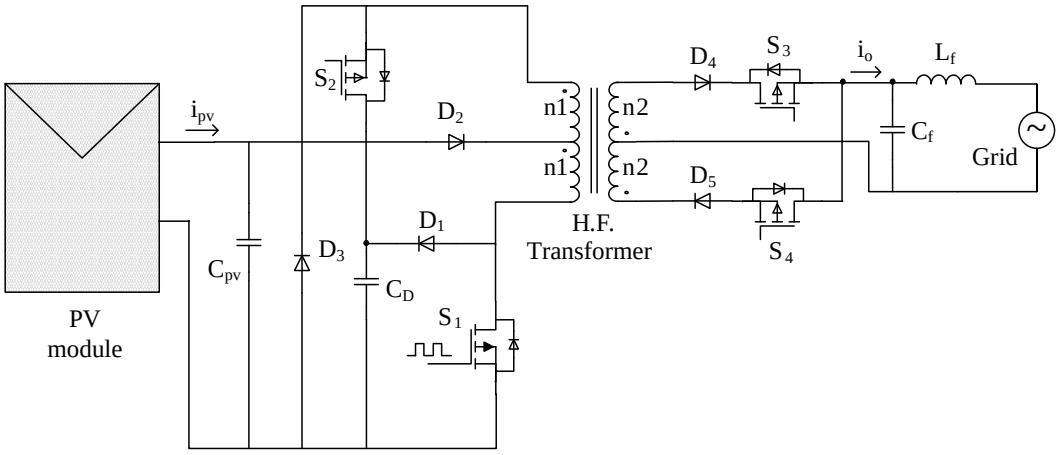

Figure 3.11 Three-port flyback-based micro-inverter with center tapped transformer [22].

By this way, as in Mode 2 of Figure 3.10, in (t_1 - t_2) time interval, the increase in primary winding current of the transformer is prevented which reduces losses as it is shown in Figure 3.12. The experimental work on 100W prototype is achieved and the efficiency is reported as 90.6%. The decoupling capacitor is indicated as 46µF film capacitor [22].

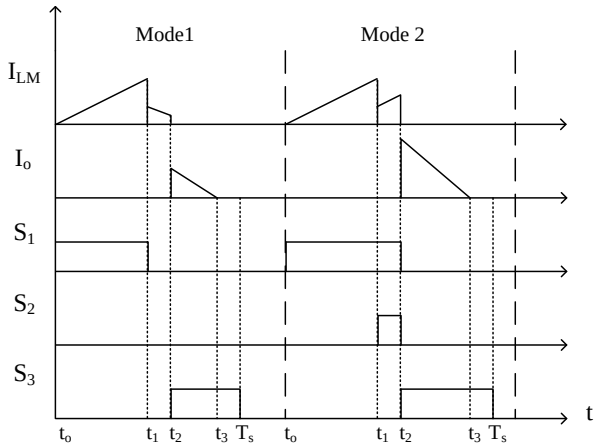

Figure 3.12 Current and switching signal waveforms of three-port flyback with center tapped transformer [20].

In Figure 3.13, another three port flyback type micro-inverter with APDC is shown. On the grid side of the topology, an LC filter and grid frequency operated unfolding bridge inverting rectified current to sinusoidal form can be seen [23].

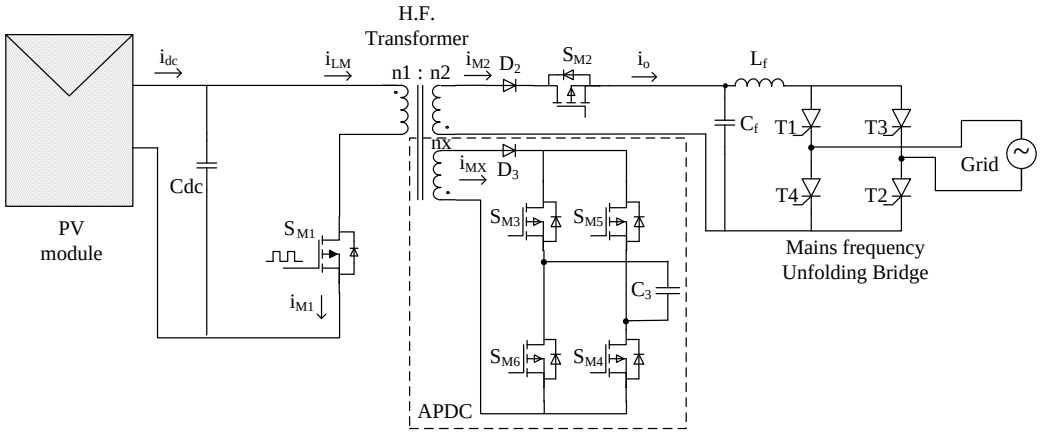

Figure 3.13 Three-port flyback-based micro-inverter with APDC and unfolding bridge [23].

The secondary side of the high frequency transformer includes two windings. One of these windings transfers the solar energy from PV side to grid side. The second winding is connected to APDC and provides charging and discharging of decoupling capacitor.

As in the case with topologies in Figure 3.9 and 3.11, the topology in Figure 3.13 has two operating modes. When the instantaneous output power is lower than input power, extra energy is stored in decoupling capacitor C_3 by means of APDC. The remaining energy is transferred to grid through S_{M2} switch and unfolding bridge thyristors.

When the instantaneous output energy is greater, after storing energy on the primary winding of high frequency transformer, the energy stored on the decoupling capacitor is discharged to the primary winding of the transformer. Finally the energy is transferred to the grid through S_{M2} switch and unfolding bridge thyristors. The

switching sequence of the thyristors is obtained according to the polarity of the grid voltage.

In Figure 3.14, current and switching signal waveforms of the circuit can be seen. By means of the operation steps explained above, the peak value of the PV module current remains constant (I_{M1peak}) but the average of the current transferred to the grid (I_{M2}) has a rectified sinusoidal shape.

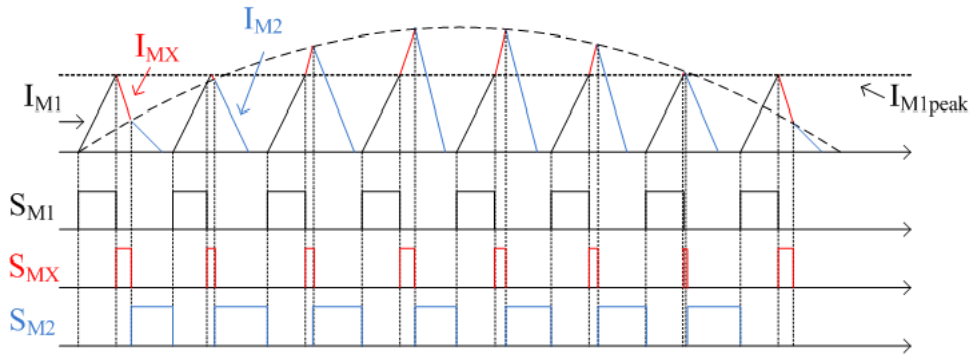

Figure 3.14 Current and switching signal waveforms of three-port flyback APDC and unfolding bridge [20][23].

With the experiments carried out with 200W prototype, it is reported that, in order to improve the efficiency of the system, DCM operation is achieved. It is indicated that 40µF film capacitor is used as decoupling capacitor but no information is given about the efficiency of the topology [23].

The proposed topology in Figure 3.15 involves double winding and double switch on the primary side of the high frequency transformer and on the secondary side, instead of two diodes in traditional forward converter, two switches are used for each diode because of the utility grid voltage shape [33].

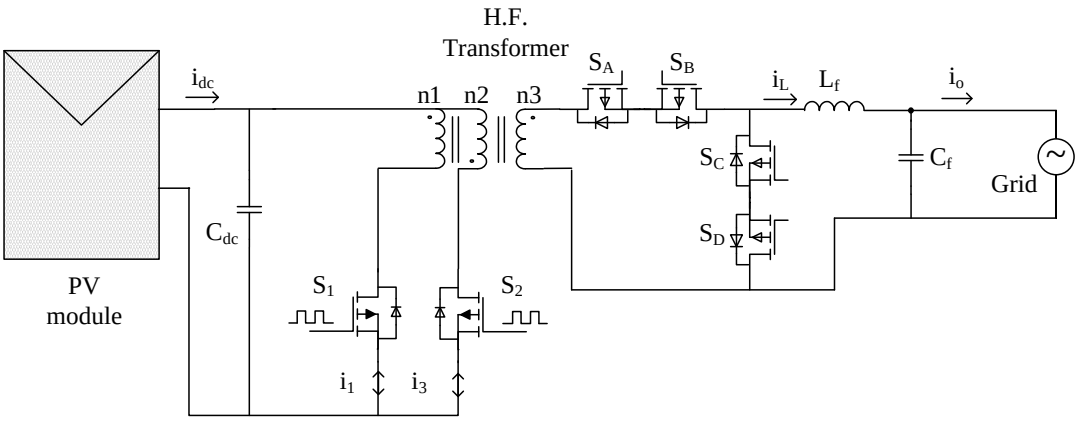

Figure 3.15 Single-stage grid-connected forward micro-inverter with constant off time boundary mode control [33].

As it is seen in Figure 3.16, when the polarity of the grid frequency is positive, S_1, S_A and S_D switches are turned on and when the polarity is negative, S_2,S_B and S_C switches are turned on.

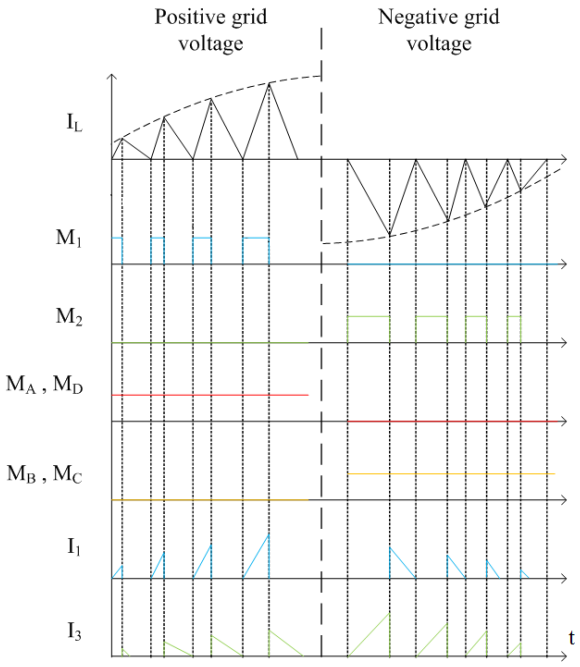

Figure 3.16 Current and switching signal waveforms of single-stage grid-connected forward micro-inverter with constant off time boundary mode control [33].

In order to achieve MPPT operation, and give the output current a sinusoidal shape, constant off time boundary mode control technique is applied. By this technique, the turn-off time of primary switches are kept constant and switching frequency is varied. In the 50W prototype, there is not any APDC so that electrolytic capacitors with high capacitances are utilized. In addition, there is not any reported information about efficiency of the circuit [33].

The topology in Figure 3.17 consists of two-phase interleaved flyback converter with active snubber circuit and mains frequency unfolding bridge circuit. By means of 180° phase shifted switching of flyback MOSFETs, not only the current sharing of two-phases but also reducing of conduction and transformer losses can be achieved [34].

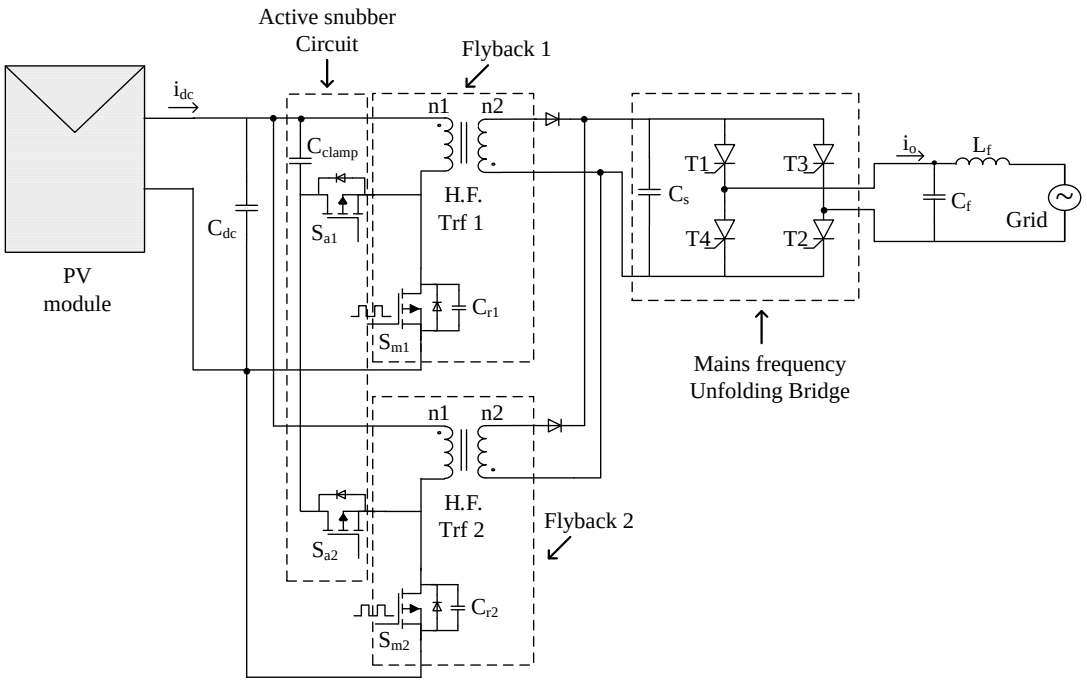

Figure 3.17 Single-stage grid-connected two-phase interleaved flyback-based micro-inverter with active snubber circuit [34].

By means of DCM operation, due to capacitors placed in parallel with S_{m1} and S_{m2} switches and the leakage inductance of the transformer, the switch voltages resonates allowing to achieve zero voltage switching of S_{m1} and S_{m2} MOSFETs. On the other hand, due to S_{a1} and S_{a2} switches and clamp capacitor, the recovery of leakage inductance energy is achieved and the efficiency of the topology is improved.

Under low load condition only one of the phases is active with DCM operation by means of hybrid control method reducing the switching losses, transformer core losses and control circuitry losses. Under high load conditions, two-phases are active controlled with boundary conduction mode (BCM). It is reported that hybrid control method substantially improves the efficiency. It is stated that the efficiency of 200W prototype is 93.5% under full load condition. When the output power is 38W, the efficiency of the micro-inverter is 90.8%. As it is seen from the results by means of hybrid control method, high efficiency can be reached for wide load range [34].

The single-stage micro-inverter topologies including APDC has the possibility of thin film capacitor utilization extending the lifetime of the circuit. On the other hand, extra number of semiconductors and increasing control complexity reduces the efficiency of the circuit. Besides this, the topologies without APDC can achieve high efficiencies for wide load range. But the electrolytic capacitors considerably shortens the lifetime of the inverter. It is seen from the topologies above that, in order to obtain an efficient system, DCM control method is commonly achieved.

3.2.3 Micro-inverters without DC-link

In micro-inverter topologies without DC-link, the DC electricity produced from the PV panel is amplified and transformed into a high frequency AC electricity level compatible with grid voltage by means of a high frequency transformer. Afterwards, under favor of a cyclo-converter, high frequency AC voltage is transformed into AC voltage with grid frequency and finally grid connection is achieved. In Figure 3.18, the structure of a micro-inverter without DC-link is shown [19].

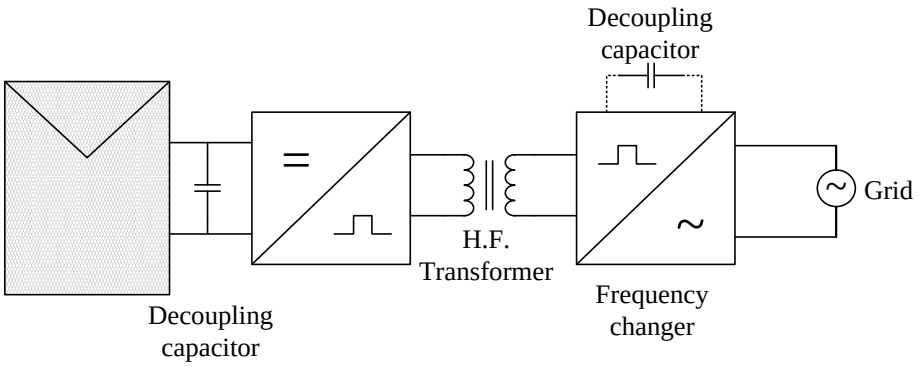

Figure 3.18 Structure of a micro-inverter without DC-link [19].

This kind of micro-inverters, the decoupling circuits are generally placed at the input in parallel with the PV module or at the grid side.

In the topology shown in Figure 3.19, full-bridge series resonant inverter is used as DC-AC inverter stage. The resonant inverter is followed by a frequency changer (cyclo-converter). The full-bridge series resonant inverter is controlled via phase shifted constant frequency control switching method [35].

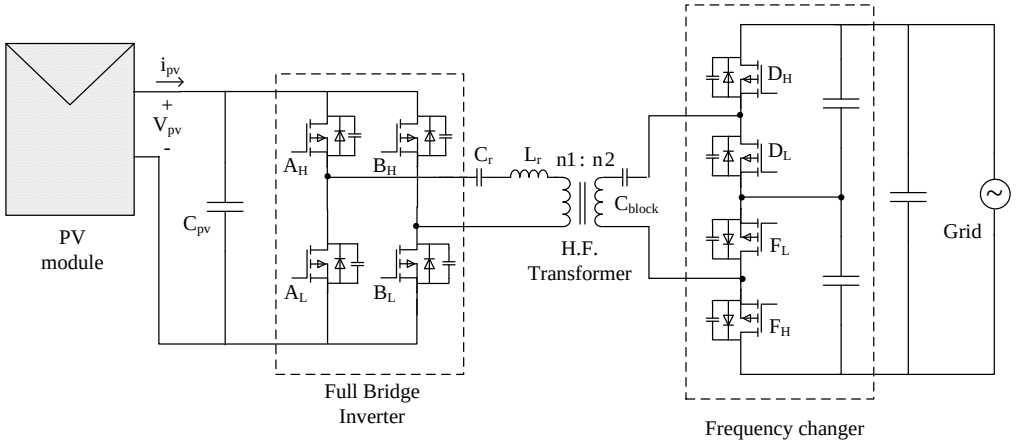

Figure 3.19 Micro-inverter with full-bridge series resonant inverter and a cyclo-converter [35].

When the grid frequency is positive, F_H and F_L switches are turned on. D_H and D_L switches provide sinusoidal shaping of output current with grid frequency. When the grid frequency is negative, D_H and D_L switches are fully turned on and current shaping is provided by F_H and F_L switches. The efficiency of the experimental prototype with 175W output power is reported as 95.9% and it is reported that electrolytic capacitor block of 7.4mF is used for power decoupling [35].

The micro-inverter topology shown in Figure 3.20, consists of three stages. The first stage is a full-bridge voltage source inverter followed by the second stage which is an impedance-admittance conversion circuit made up of inductors and capacitors. The third stage comprised of a cyclo-converter with a center tapped transformer [36].

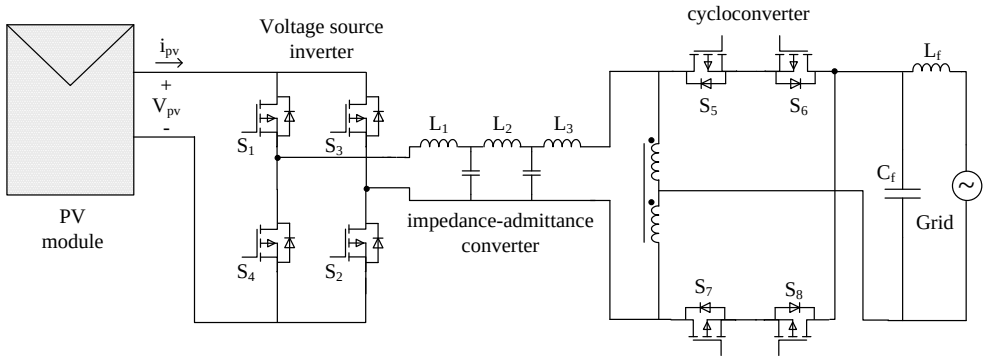

Figure 3.20 Micro-inverter with voltage source inverter, impedance-admittance converter and a cyclo-converter [36].

PMW technique is applied for the control of voltage source inverter. The impedance-admittance unit converts voltage source inverter into current source inverter. Finally, the cyclo-converter provides sinusoidal shaped current at grid frequency to the grid. In order to filter out the high frequency ripples on the output current caused by switching, a low pass filter is utilized. Experimental works are achieved with 30W prototype but no information is given about the efficiency [36].

By means of achieving power transfer from PV module to the grid with two stages, utilization of bidirectional semiconductors, the number of semiconductors used in the circuit is reduced which increases the efficiency. On the other hand, low reliability of bidirectional semiconductors are increased complexity of the control system some of the drawbacks of topologies without DC-link [19]. In Table 3.1, power capacities, semiconductor device counts, decoupling capacitor information, control methods, efficiencies and dimension of the topologies mentioned in this study is given.

Table 3.1 Power capacities, semiconductor device counts, decoupling capacitor information, control methods, efficiencies and dimensions of the topologies

	Ref. No	**power capacity (W)**	**Semicond. count**	**decoupling capacitor**	**control method**	**efficiency**
Micro-inverters with DC-link	[29]	150	9M + 9D	8.2uF film cap.	phase shifted PWM / current control	85.4%
	[30] [31]	210	6M + 2D	electrolytic	repetitive current control	95.6% (160W)
	[32]	100	6M + 4D	-	-	-
Micro-inverters with Pseudo DC-link	[21]	100	4M + 4D	46uF film	DCM	-
	[22]	100	4M + 5D	46uF film	DCM	90.6%
	[23]	200	10M + 2D	40uF film	DCM	-
	[33]	50	6M	electrolytic	BCM	-
	[34]	200	4M + 2D + 4T	electrolytic	DCM / BCM	93.5%
Micro-inverters without DC-link	[35]	175	8M	7.4mF electrolytic	phase shifted PWM / freq. converter phase control	95.9%
	[36]	30	8M	-	PWM	-
M: MOSFET D: Diode T: Thyristor						

3.3 Commercial Micro-inverter Topology Examples

In Figure 3.21, a commercial micro-inverter topology with a pseudo DC-link can be seen which consists of a flyback converter and grid frequency operated unfolding bridge.

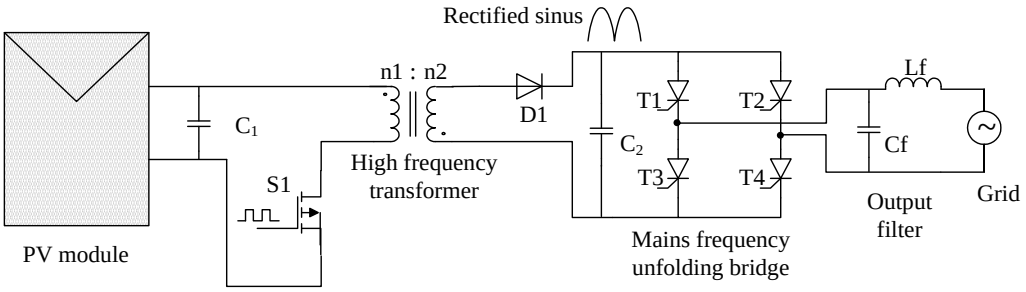

Figure 3.21 A commercial micro-inverter with flyback converter and unfolding bridge (Mastervolt) [18].

By means of primary side current modulation with S_1 switch, the average of the D_1 current has a sinusoidal shape as it is discussed in micro-inverters with pseudo DC-link section. According to the grid voltage polarity, T_1-T_4 or T_2-T_3 thyristors are turned on or off in order to transfer sinusoidal shaped current in phase with the grid.

In an effort to have an efficient micro-inverter system, quasi-resonant interleaved flyback converter is utilized in a commercial micro-inverter topology as it is seen in Figure 3.22. By means of the resonation between an additional capacitor placed in parallel with the main switch or the parasitic capacitance of the switch and the magnetizing inductance of the transformer, quasi-resonant control technique can be achieved decreasing the switching losses and increasing the efficiency. Two-phase interleaved flyback topology provides current sharing reducing the peak current seen by the main switches and the transformers increasing the efficiency.

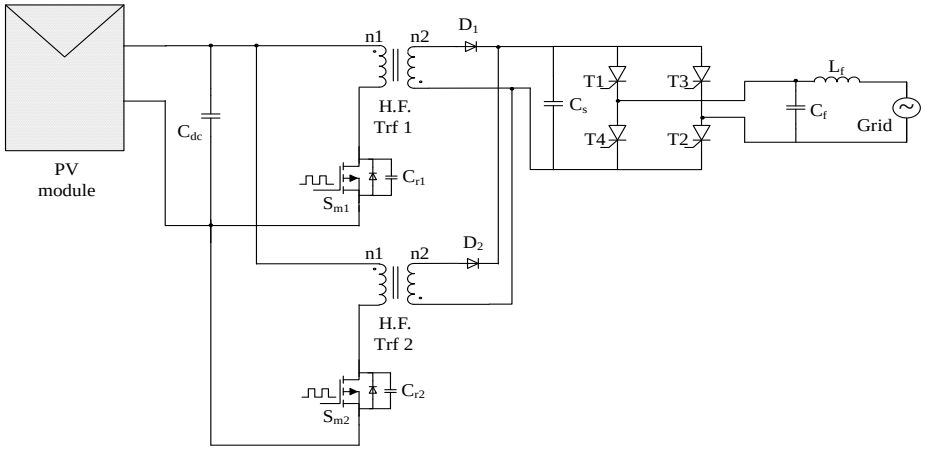

Figure 3.22 A commercial micro-inverter with two-phase interleaved flyback converter and unfolding bridge (Enphase) [44].

In Figure 3.23, a micro-inverter with pseudo DC-link can be seen which arises from a primary side modulated resonant converter and a grid frequency operated unfolding bridge circuit.

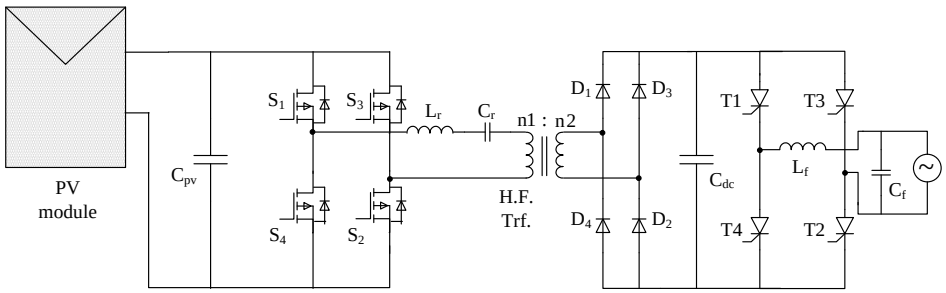

Figure 3.23 A commercial micro-inverter with full-bridge resonant converter and unfolding bridge (OKE 4) [18].

Resonant converters can achieve high efficiencies on the other hand the control complexity of the converter is increased comparing to others [18].

In Figure 3.24, a commercial micro-inverter topology similar to the topology specified in reference [29] can be seen. The topology consists of a resonant converter, a buck converter and unfolding bridge operating at mains frequency.

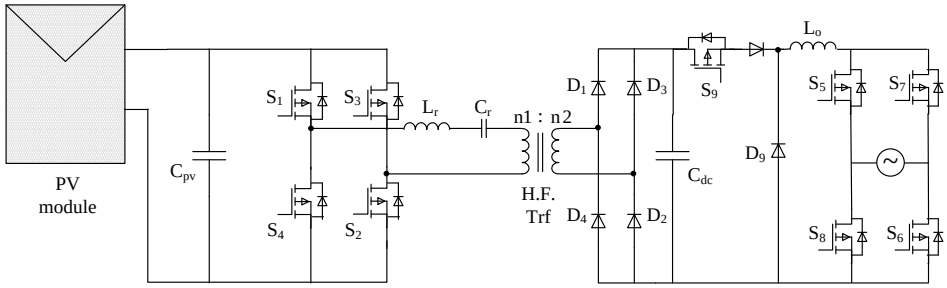

Figure 3.24 A commercial micro-inverter with full-bridge resonant converter, buck converter and unfolding bridge (Enecsys) [45].

Differently from the commercial topologies discussed above, this topology is not primary side modulated. Rectified sinusoidal current is achieved by means of the buck converter switch modulation and with the aid of unfolding bridge, sinusoidal shaped current is transferred to the grid with unity power factor [45].

Another commercial MI topology can be seen in Figure 3.25, including a APDC in order to use film capacitors for decoupling, increasing the lifetime of the MI.

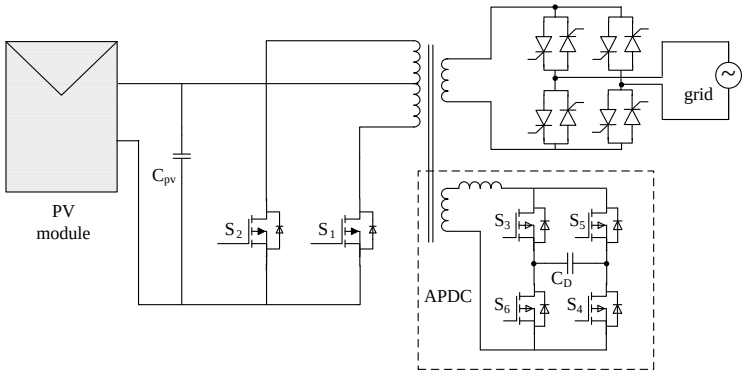

Figure 3.25 A commercial micro-inverter with push-pull converter, APDC and cyclo-converter with anti-parallel thyristors (Solarbridge) [46].

A push-pull converter is used on the PV side which is dc modulated giving the opportunity to use a small film capacitor [18]. Secondary windings of the transformer are connected to APDC including a film decoupling capacitor and a cyclo-converter transferring the energy to the grid including anti-parallel thyristors.

3.4 Summary

In this chapter, three micro-inverter topology categories gaining popularity especially for residential applications classified according to their DC-link configurations. Examples of the commercially used topologies are also given. In Table 3.2, power capacities, semiconductor device counts, decoupling capacitor information, control methods, efficiencies and dimensions of the topologies is given.

As it is seen from the table, the analyzed topologies mostly have power capacities between 100 - 200W and efficiencies between 85 - 95%. Micro-inverters with a large number of semiconductors have lower efficiencies and higher cost. In pseudo DC-link configurations, using APDC, increases the life time but also decreases the system efficiency. Instead of APDC, topologies with soft switching semiconductors and electrolytic capacitors have higher efficiencies but lower life time. In micro-inverters without DC-link, by means of using bidirectional semiconductors the required number of semiconductor is decreased and the efficiency is increased. On the other hand, low reliability of bidirectional semiconductors and the complexity of the controller are some of the disadvantages. In the proposed topologies, in order to increase the efficiency of the system, it is seen that DCM control method is widely used. As it is seen from these topologies, studies growingly continues in order to prolong the lifetime of the micro-inverter and increase the efficiency and reliability by means of film capacitors and soft switching methods. As it is seen from table 3.2, nominal power, peak efficiency, warranty, power density and line communication information of eighteen products from eight different micro-inverter companies are given. Power capacities varies between 190-535W. The efficiencies of the products are between 93-96.3% which is nearly 2-3% less than string inverter efficiencies. There is a great variability of warranties of the products which is from 5 to 25. Power densities are between 0.11 - 0.3.

Table 3.2 Model names, nominal powers, peak efficiencies, warranties, power densities and line communication methods of the commercial micro-inverters

Company name	Model	Nom. power	Peak eff. (%)	Warranty (years)	Power density (W/cm^3)	Line comm.
Enphase	M190	190	95.5	15	0.22	Power line
	M210	210	96	15	0.244	Power line
	M215	215	96.3	25 (Limited)	0.303	Power line
	D380	380	95.5	15	0.237	Power line
Enecsys	SMI-S240W-72-UL	240	94	20	0.164	Zigbee IEEE 802.15.4
	SMI-D360W-72-UL	360	95	20	0.246	Zigbee IEEE 802.15.4
	SMI-D480W-60-UL	480	96	20	0.220	Zigbee IEEE 802.15.4
SolarBridge	Pantheaon	225	95.5	25	0.212	Power line
	Pantheaon II	238	95.7	25	0.245	Power line
SparQ	S190NA3250	190	94.5	25	0.258	Power line
	S215NA3250	215	94.5	25	0.292	Power line
PowerOne	Micro-0.25-I	250	96.5	10	0.110	Wireless
	Micro-0.3-I	300			0.131	
SMA	Sunny Boy 240-US	240	95.9	10	0.136	Sunny Portal
Direct Grid	DGA-S250	238	95	20 (Limited)	0.152	Echelon
	DGA-S400	372	94		0.238	
	DGM-460	430	93		0.275	
Mastervolt	Soladin 600	535	93	5	0.135	NA

CHAPTER 4

OPERATING PRINCIPLES, ANALYSIS AND CONTROL OF FLYBACK-BASED MICRO-INVERTER

In the literature, flyback converter is one of the most popular topologies used for micro-inverter systems [20]. Because of the properties such as ease of implementation, low semiconductor count, easier control structure and providing galvanic isolation, flyback converter topology becomes considerably advantageous. The structure of the micro-inverter system, flyback converter basics, switching strategies, control algorithms such as sinusoidal current reference generation (SCRG), MPPT, PLL and output current control will be explained in this section. In addition, flyback-based two-phase interleaved MI (TPIMI) topology will be discussed and benefits of interleaving will be expressed.

4.1 Flyback-Based Single-Phase Micro-inverter Topology

There are various types of flyback-based micro-inverter topologies developed in order to increase efficiency, reduce switching and conduction losses and cost. flyback-based single-phase MI (SPMI) consisting of decoupling capacitors, flyback converter, unfolding bridge (UB) and LCL filter is shown in Figure 4.1. In order to handle instantaneous power mismatch between input and output power of the MI, decoupling capacitors are placed at the input side as discussed in section 3.1. A PWM flyback converter including an RCD snubber increases the PV panel voltage to the levels compatible with grid voltage, regulates the current, achieves MPPT operation and provides galvanic isolation between PV module and the utility grid. The voltage at the output of the flyback, which is called pseudo DC-link, is a rectified sine wave in phase with the grid voltage. Pseudo DC-link current is controlled to has a rectified sinusoidal waveform via controlling S_1 switch.

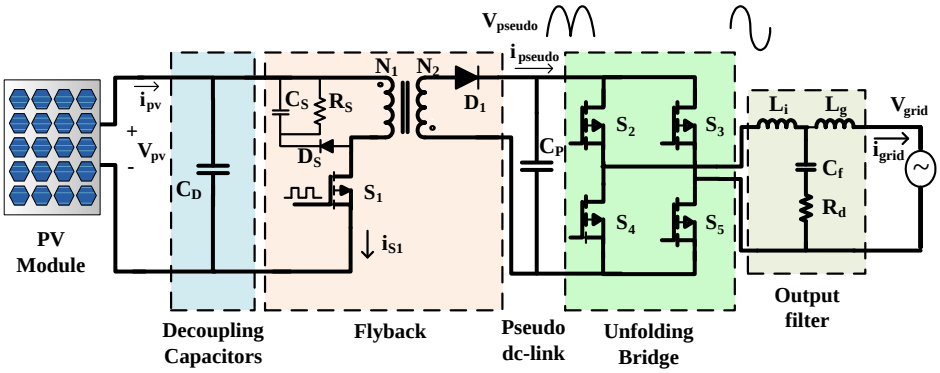

Figure 4.1 Schematic of flyback-based SPMI.

An unfolding bridge (UB) operating at mains frequency unfolds the rectified sinusoidal voltage (current) into sinusoidal form via switching MOSFETs (S_2-S_5) at zero crossings of the grid according to the grid voltage polarity as it is shown in Figure 4.2.

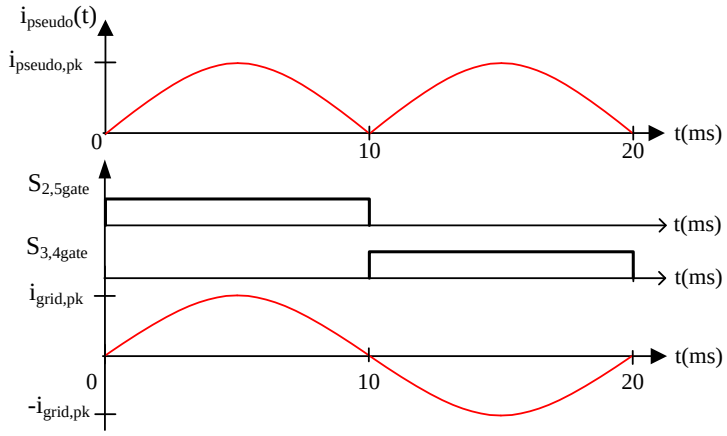

Figure 4.2 SPMI pseudo DC-link current ($i_{pseudo}(t)$), UB MOSFET switching signals ($S_{2\text{-}5\ gate}$) and grid current ($i_{grid}(t)$).

UB is followed by an output filter which filters out current and voltage ripples come into existence because of high frequency switching of the semiconductors and achieves utility grid connection. There are various types of filters used such as L, LC

or LCL filters at the output of an inverter, however for grid-connected systems, LCL filter is rather preferred [53]. A damping resistor R_d is connected in series with the LCL filter capacitor (C_f) in order to prevent oscillations around the corner frequency of the LCL filter.

4.2 Flyback Converter

Basic flyback structure can be seen in Figure 4.3.

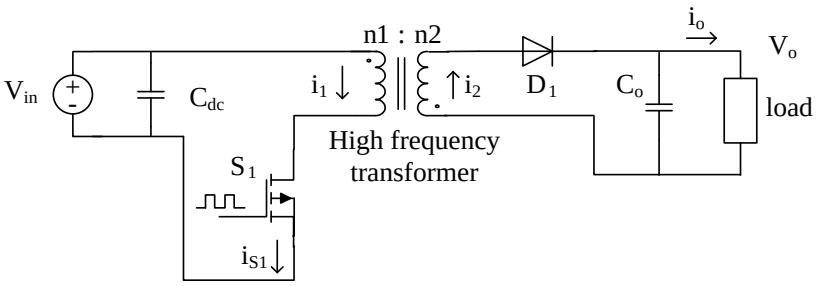

Figure 4.3 Basic flyback converter structure.

Flyback converter is a combination of buck-boost converter and a high frequency (HF) transformer with (n_1/n_2) turns ratio replaced with the inductor causing operating principles of two topologies to be very similar. When S_1 switch turns on, primary current ($i_1 = i_{S1}$) increases linearly storing energy on the magnetizing inductance of the transformer. D_1 prevents energy transfer to the output and C_O feeds the load during this turn-on period (T_{ON}) as it is seen in Figure 4.4.

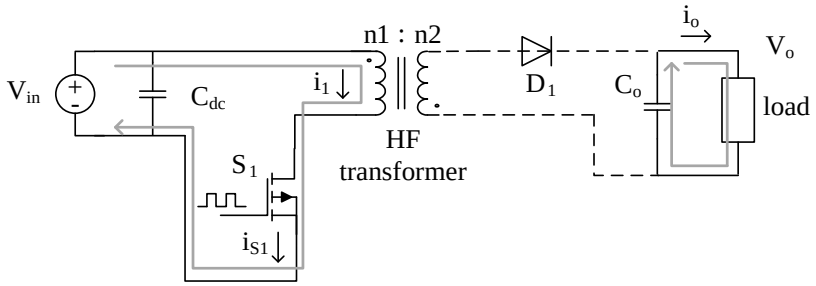

Figure 4.4 Mode of operation when S_1 is on (T_{ON}).

When S_1 turns off, primary current (i_1) goes to zero and by means of forward biased output diode D_1, secondary current (i_2) starts to decrease from a certain value transferring the energy stored on the HF transformer to the output during turn-off period (T_{OFF}) as it is seen from Figure 4.5.

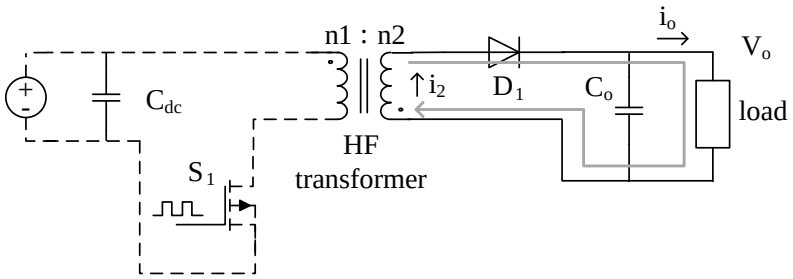

Figure 4.5 Mode of operation when S_1 is off (T_{OFF}).

Having very simple construction and limited number of semiconductors, flyback converter is rather preferred as a micro-inverter topology for grid-connected PV applications. Another advantage of flyback-based micro-inverter is the HF transformer providing galvanic isolation between PV panel and the utility grid providing easier grounding of the PV module.

4.3 Switching Strategy

The switching strategy of a flyback-based micro-inverter is very important in order to design an efficient system. It can be divided into three modes of operation such as;

- Discontinuous conduction mode (DCM)
- Boundary conduction mode (BCM)
- Continuous conduction mode (CCM)

The parameters determining selection of the mode of operation can be written as the transformer size, semiconductor ratings, output filter parameters, THD, power factor and the efficiency of the micro-inverter [37].

Transformer design parameters, RMS and peak transformer currents, switching and conduction losses, switching frequency and power capacity of the circuit are calculated according to the selected mode of operation.

4.3.1 Discontinuous Conduction Mode

DCM operation has three time intervals as it is seen from Figure 4.6. In the first time interval (t_0 - t_1) , the main switch S_1 turns on and the magnetizing current ($i_1 = i_{S1}$) starts to increase from zero to its peak value with a ramp function and energy is stored on the magnetizing inductance of the transformer until the main switch is turned off. During this time interval (T_{ON}), the voltage of the main switch is equal to zero ideally. No energy transfer is achieved during this time interval due to reverse biased D_1 diode.

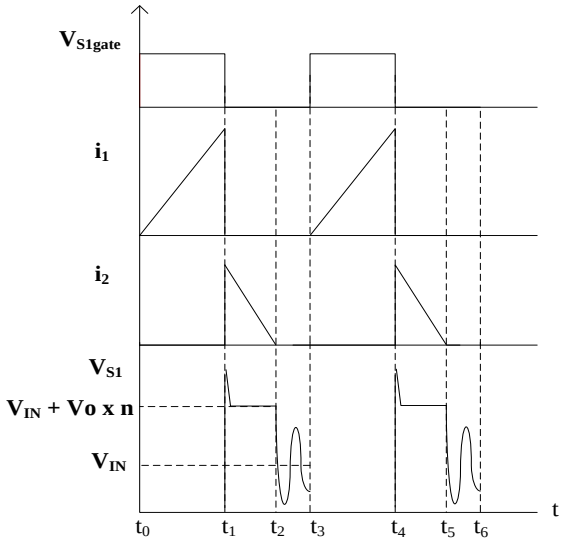

Figure 4.6 Voltage and current waveforms of S_1 and transformer during DCM operation.

In the course of (t_1 - t_2), main switch is turned off and magnetizing current decreases to zero while the secondary current (i_2) starts to flow through forward biased D_1 diode transferring the stored energy to output and i_2 linearly goes to zero at t_2 instant before the switching period is completed (t_0 - t_3) (T_S). At t_1 instant, because of interrupting the current flowing through the leakage inductance of the transformer, there will be a voltage spike on the MOSFET voltage V_{S1}. During (t_1 - t_2), V_{S1} is equal to the sum of input voltage and the reflected output voltage seen by the primary winding. When the secondary current equals to zero at t_2, energy transfer to the output ends and V_{S1} starts to resonate around V_{IN} due to the resonation caused by the parasitic capacitance of S_1 and magnetizing inductance of the transformer during (t_2 - t_3).

4.3.2 Continuous Conduction Mode

For the CCM of operation, either variable switching frequency (VSF) or (mostly) constant switching frequency (CSF) can be achieved. In CCM operation, the magnetizing current starts from a non-zero point causing the name of the operation to be continuous and increases linearly to the peak value as it is seen in Figure 4.7.

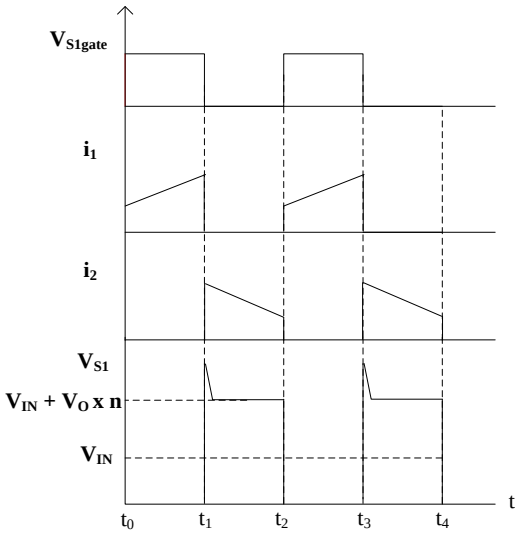

Figure 4.7 Voltage and current waveforms of main switch and transformer during CCM operation.

In the time interval (t_1 - t_2), S_1 switch turns off and D_1 diode starts to conduct due to the energy stored in the transformer. In continuous conduction mode, after t_1 instant, i_2 current decreases linearly. As distinct from other control methods, S_1 turns on before i_2 current goes to zero. In other words, the energy stored in the transformer does not fully transferred to the output.

4.3.3 Boundary Conduction Mode

BCM operation has two time intervals as it is seen from Figure 4.8. The most important difference between BCM operation and the other mode of operations is VSF utilization. This mode of operation operates at the boundary point between DCM and CCM.

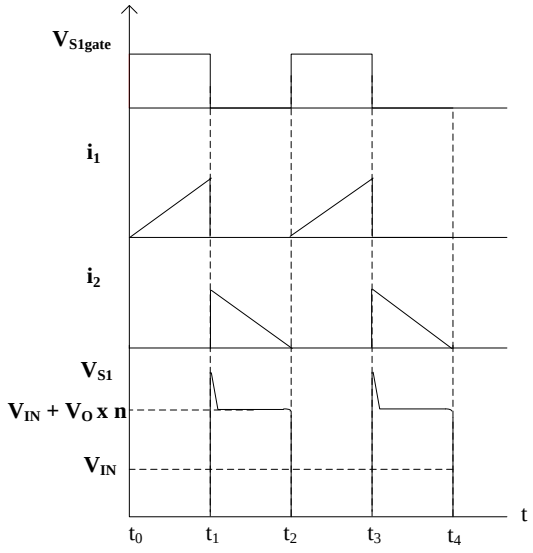

Figure 4.8 Voltage and current waveforms of main switch and transformer during BCM operation.

In this mode of operation, when the main switch is turned on, i_1 starts to increase linearly from zero storing energy on the magnetizing inductance as is the case with DCM operation. At time instant t_1, S_1 is turned off and D_1 diode starts to conduct due to the energy stored in the transformer.

The interruption of current flowing through primary leakage inductance at t_1 causes a voltage spike appearing on V_{S1} as is the case with DCM and CCM operation. During (t_1 - t_2) time interval V_{S1} equals to the sum of input voltage and output voltage divided by the turns ratio ($n = n_1/n_2$) which is the reflected output voltage applied across the secondary winding. At t_2 instant, as soon as there is no energy left in the transformer and i_2 equals to zero, S_1 switch turns on starting T_{ON} again.

4.3.4 Comparison of Conduction Modes

In DCM operation smaller inductance is required which reduces the transformer size. On the other hand, the peak and RMS value of the magnetizing current is very high compared to other conduction modes. Increased current ratings increase winding losses of transformer, enhance switching and conduction losses and switching stresses on the main switch causing to use switches with high current ratings [38]. Increased current ratings also enhance ripple voltage and ripple current on the input and output capacitors. Besides, thicker wires will be needed increasing the transformer size [37]. On the other side, DCM operation provides zero current turn-on of main switch and zero current turn-off of output diode reducing switching losses and cancelling out reverse recovery problem of the output diode. Without reverse recovery condition, EMI radiation will be considerably reduced [39]. DCM operated controller does not present right half plane zero which makes it easy to stabilize the control loop. In addition to these advantages, DCM operation provides valley switching due to the resonation on main switch voltage reducing switching losses. In general, DCM operation is mentioned to be suitable for low power PV applications.

Due to the complete utilization of total switching period, power capacity of a BCM operated inverter can be twice the DCM operated one [37]. As is the case for DCM operation, no right-half-plane zero and reverse recovery takes place in BCM operation. The RMS and peak current ratings are lower causing reduced switching and conduction losses. EMI radiation is also reduced due to zero reverse recovery. On the other hand, variable switching frequency makes it necessary to measure switch current and increases the complexity of the controller. Variable switching

frequency also increases the complexity of the output filter design. CCM operation has lower RMS and peak current ratings than the other methods reducing switching and conduction losses. On the other hand, non-zero current turn-on of the main switch and reverse recovery loss of output diode increases switching losses and EMI radiation due to hard switching condition. A larger inductance is also required which increases the size of the transformer. In addition, CCM operation has a right half plane zero making it difficult to stabilize the control loop for wide input voltage range with bandwidth limitation [39]. Non-zero turn-on causes a higher turn-on current spike on the magnetizing current which can bring on a false turn-off situation [40]. Because of the ease of implementation and other advantages listed above, DCM operation is implemented as switching strategy.

4.4 Flyback-Based Two-Phase Interleaved MI Topology

In Figure 4.9, schematic of flyback-based two-phase interleaved MI (TPIMI) is given. As in SPMI, there is a decoupling capacitor bank placed at the input. On the other hand, TPIMI consists of two flyback converters connected in parallel sharing input current and realizing input voltage amplification, MPPT and galvanic isolation. Current sharing of two-phases is conducted by means of switching the primary semiconductors (S_1, S_2) with 180° phase shift.

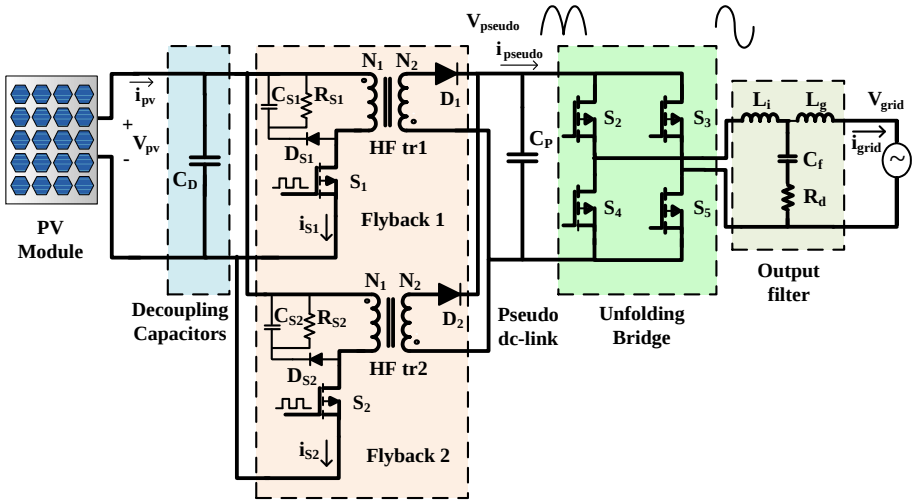

Figure 4.9 Schematic of flyback-based TPIMI.

As in SPMI, UB unfolds rectified sinusoidal pseudo DC-link voltage (current) at fundamental utility grid frequency and an LCL filter carries out noise filtering and grid connection with a damping resistor R_d connected in series with C_f.

4.4.1 DCM Operation of TPIMI

In Figure 4.10, gate signals and current waveforms of DCM controlled TPIMI are shown. As in SPMI, primary currents linearly increase from zero and energy transfer to the output ends before new switching period starts. The only difference is 180° phase shifted turn-on of primary MOSFETs due to two-phase operation providing current sharing between these phases.

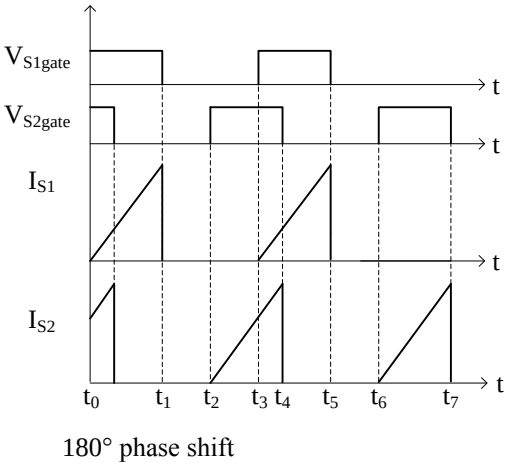

Figure 4.10 180° phase shifted TPIMI MOSFET switching signals (V_{S1gate} - V_{S2gate}) and currents (I_{S1} - I_{S2}).

4.4.2 Benefits of Interleaving

As it is mentioned before, the most important benefit of interleaving operation is current sharing between MI phases [41][42]. Due to current sharing, peak MOSFET and output diode currents will be reduced which reduces switching stresses and EMI especially during turn-off of the MOSFETs. RMS currents of the phases will be also reduced which reduces I^2R losses increasing the efficiency of the MI.

Due to phase shifted operation, there is a ripple cancellation at the input and output current which reduces required filter size and improves transient response of the MI. Reduced input current ripple increases the decoupling capacitor lifetime and MI lifetime as well. Fewer capacitors are required at the input and output which reduce the system cost improving cost production. Moreover, THD of TPIMI is expected to be lower due to ripple cancellation at the output. Smaller output filter also improves the transient response of the MI.

Besides, interleaving technique enables MI to operate at higher power ratings than SPMI providing larger power density.

4.5 Control Strategy of Flyback-Based Micro-inverter

A block diagram consisting of single-stage flyback-based micro-inverter and controller block is shown in Figure 4.11. The control of the current injected to the grid is achieved by means of several operational blocks such as sinusoidal current reference generation (SCRG), MPPT and PLL via measuring input voltage and current, grid voltage, pseudo DC-link current and voltage. TMS320C2000 experimenters kit is used as the controller including a docking station and TMS320F28335 digital signal processor (DSP) with 16 12-bit analog-digital converter (ADC) channels and 18 PWM outputs in order to perform control operations.

Output current of a MI is a sine wave oscillating with grid frequency. As a result, the reference signal must have a rectified sinusoidal shape. SCRG block, provides this signal via using a rectified unity sine wave and calculating peak MOSFET current in terms of input and output currents and voltages which corresponds to the amplitude of the signal. In addition to that, MPPT algorithm allows PV panel to operate at MPP for maximum energy harvest. Under favor of measuring PV panel voltage and panel current and manipulating the reference current step by step according to the sign of the alteration of power, the maximum available power is drawn from the panel.

Via MPPT, the amplitude of reference current is obtained. PLL controller performs unity rectified sine wave generation in phase with the grid in order to achieve grid synchronization of the output current. In addition to that, PLL algorithm controls the unfolding bridge MOSFETs S_2,S_5 and S_3,S_4 in order to provide sinusoidal output current via switching each group at zero crossings of the grid voltage respectively according to the polarity of the grid.

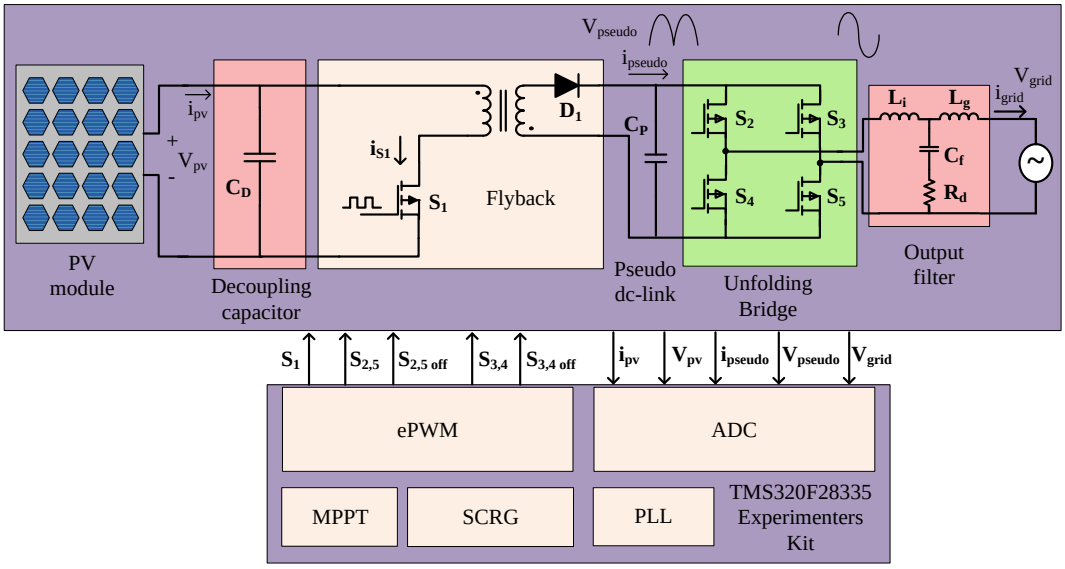

Figure 4.11 Block diagram of flyback-based MI and DSP controller.

The control schematic of the MI is shown in Figure 4.12. As it is seen from the figure, input current and voltage is measured and fed to MPPT block which determines the optimum input power. On the other hand the grid voltage is measured in order to determine the phase angle of the unity rectified sine wave $|sin(\omega t)|$ for grid synchronization.

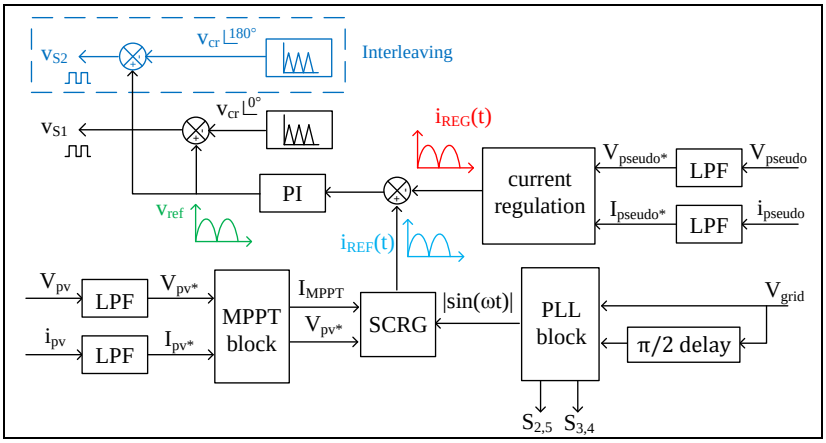

Figure 4.12 Control schematic of SPMI and TPIMI.

Amplitude of the reference current $i_{REF}(t)$ is calculated and multiplied with |sin(ωt)| in SCRG block. Via measuring pseudo DC-link voltage and current, actual output parameters are determined and calculated in terms of $i_{REF}(t)$. These calculated parameters are fed into a PI control block and reference signal v_{ref} is generated.

Only one switching signal (v_{S1}) is created for single-phase (SPMI) operation. On the other hand, 180° phase shifted switching signals (v_{S1}- v_{S2}) are generated by means of 180° phase shifted carrier signals for interleaving (TPIMI). In the next sections, important parts of the control schematic will be presented in detail.

4.5.1 Sinusoidal Current Reference Generation

Simplicity of a design provides ease of implementation as well as cost reduction. In order to meet the requirements of a micro-inverter with minimum cost and complexity, mathematical relation between input and output current is used to generate the reference signal without measuring high frequency primary or secondary current of the flyback transformer [41].

The output current of a conventional flyback DC-DC converter is constant with respect to time. On the other hand, flyback-based micro-inverters have sinusoidal current on the output fluctuating with grid frequency. Because of these circumstances, reference signal created by the controller must be a rectified sine

wave. With the purpose of achieving this requirement, conventional DC/DC flyback converter equations must be modified and output current must be rewritten in terms of reference current. Rectified sinusoidal current reference waveform is created by means of calculating the mathematical relation between peak primary MOSFET current, input current and grid current throughout one grid period which is 20ms for a 50Hz utility grid.

Figure 4.13 represents primary MOSFET current $i_{S1}(t)$, flyback output diode current $i_{D1}(t)$ and the reference current signal $i_{REF}(t)$ of the micro-inverter which is equal to the peak primary MOSFET current throughout one half of the grid period.

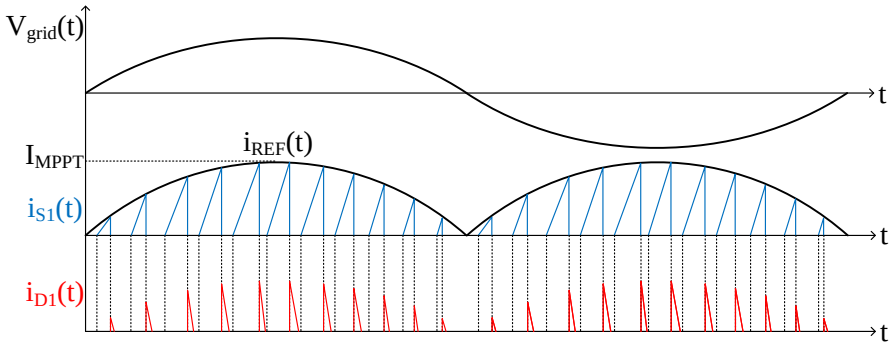

Figure 4.13 Grid voltage V_{grid}, reference current signal $i_{REF}(t)$ with the amplitude I_{MPPT}, primary MOSFET current $i_{S1}(t)$ and output diode current $i_{D1}(t)$ throughout one grid period.

In order to specify the relation between the currents, there is an assumption stating that the average value of $i_{D1}(t)$ is equal to grid current I_{grid} in every switching period [42]. The relation can be determined under favor of the equations (4.1) - (4.13). Based on the magnetizing inductor of the HF transformer, PV panel voltage can be defined as;

$$V_{PV} = L_m \frac{d(i_{PV}(t))}{dt} \tag{4.1}$$

(4.1) represents basic inductor formula where V_{PV} is the input voltage seen by the magnetizing inductance L_m and $i_{PV}(t)$ is the magnetizing current flowing through the inductor which is also equal to the MOSFET current $i_{S1}(t)$. dt represents the conduction time of the main switch which can be written as t_{on}. Because of the DCM operation, the increment of the current is equal to the peak MOSFET current $I_{S1,peak}$. Therefore, peak inductor current can be written as;

$$I_{S1,pk} = \frac{V_{PV}}{L_m} t_{on} \tag{4.2}$$

On the other hand, based on the same statement, secondary side current $I_{D1,pk}$ of the HF transformer can be written as;

$$I_{D1,pk} = \frac{V_{grid}(t)}{L_s} t_{off} \tag{4.3}$$

where L_s is the secondary side inductance of the HF transformer and $V_{grid}(t)$ is the grid voltage which is seen by L_s during primary MOSFET off time t_{off}. While t_{off} is a very short duration in accordance with the utility grid half cycle, $V_{grid}(t)$ can be assumed to be constant and the equation can be written as;

$$I_{D1,pk} = \frac{V_{grid,pk}}{L_s} t_{off} \tag{4.4}$$

where $V_{grid,pk}$ is the peak grid voltage. The relation between primary and secondary currents and inductances can be defined as;

$$I_{D1,pk} = n \times I_{S1,pk} \tag{4.5}$$

$$L_m = L_s \times n^2 \tag{4.6}$$

where n is the turns ratio of the HF transformer (N_1/N_2). On the other hand, the reference current $i_{REF}(t)$ must include a sinusoidal part as it is shown in (4.7).

$$i_{S1}(t) = i_{REF}(t) = I_{S1,pk}\sin(\omega_0 t) \qquad \omega_0 t \in [0, \pi] \tag{4.7}$$

In (4.7), $\omega_0 = 2\pi f_0$ where f_0 is the grid frequency and $I_{S1,pk}$ is the peak MOSFET current value when $\omega_0 t$ is equal to $\pi/2$. From the assumption stating the equality of average value of I_{D1} and I_{grid} in every switching period, I_{grid} can be defined as;

$$I_{grid} = \frac{I_{D1,pk} \times t_{off}}{2T_{sw}} \tag{4.8}$$

where, T_{sw} is the switching period. Just as in V_{grid}, I_{grid} can be stated as constant while t_{off} is a very short duration in accordance with the utility grid half cycle. As a result, (4.8) can be rewritten as;

$$I_{grid,pk} = \frac{I_{D1,pk} \times t_{off}}{2T_{sw}} \tag{4.9}$$

Using (4.3), (4.5) and (4.6), t_{off} can be defined as;

$$t_{off} = \frac{I_{S1,pk} \times L_m}{nV_{grid,pk}} \tag{4.10}$$

From (4.9) and (4.10), peak MOSFET current $I_{S1,pk}$ and reference current $i_{REF}(t)$ can be written in terms of peak grid current $I_{grid,pk}$ and grid power P_{grid} as;

$$I_{S1,pk} = \sqrt{\frac{2 \times I_{grid,pk} \times V_{grid,pk}}{L_m \times f_{sw}}} \tag{4.11}$$

$$i_{REF}(t) = \left|\sin(\omega_0 t)\right| \sqrt{\frac{2 \times I_{grid,pk} \times V_{grid,pk}}{L_m \times f_{sw}}} = 2 \times \left|\sin(\omega_0 t)\right| \sqrt{\frac{P_{grid}}{L_m \times f_{sw}}} \quad (4.12)$$

Since for an ideal system, input power (P_{PV}) is equal to output power (P_{grid}), $i_{REF}(t)$ can be rewritten as;

$$i_{REF}(t) = 2 \times \left|\sin(\omega_0 t)\right| \sqrt{\frac{P_{PV}}{L_m \times f_{sw}}} = 2 \times \left|\sin(\omega_0 t)\right| \sqrt{\frac{I_{PV} \times V_{PV}}{L_m \times f_{sw}}} \quad (4.13)$$

By using the relation between $I_{S1,pk}$ and $I_{grid,pk}$, reference current $i_{REF}(t)$ can be constituted. Via measuring input and output currents and voltages as it is shown in Figure 4.12, output current of the MI can be controlled to be a sine wave in phase with the utility grid via calculated values fed to the PI controller. The amplitude and phase angle of the reference current can be calculated via MPPT and PLL blocks providing maximum energy harvest and high power factor.

4.5.2 Maximum Power Point Tracking

Another important part of the controller system is MPPT block which ensures the effective utilization of the PV module under variable atmospheric conditions. The amplitude of $i_{REF}(t)$, which is $I_{S1,pk}$ in this case, is dependent on PV panel power characteristics as well as PV voltage and current. A mono-crystalline solar panel Sunrise SR-M660230 with 230W rated power is used in this study. In order to realize MPPT operation effectively, P-V and I-V characteristics of the panel are measured at a certain solar irradiation and temperature which is shown in Figure 4.14.

As it is seen from the figure, there is a maximum power point (P_{MPP}) of the PV panel achieved at certain voltage (V_{MPP}) and current (I_{MPP}) values. P-V characteristic of the PV panel is different for both sides of P_{MPP}. On the left hand side of P_{MPP}, there is a directly proportional relation between voltage and power. As the panel voltage increases, power drawn from the panel increases as well. However, as the panel

voltage keeps increasing on the right hand side of P_{MPP}, panel power starts to decrease and goes to zero at open circuit voltage V_{OC}.

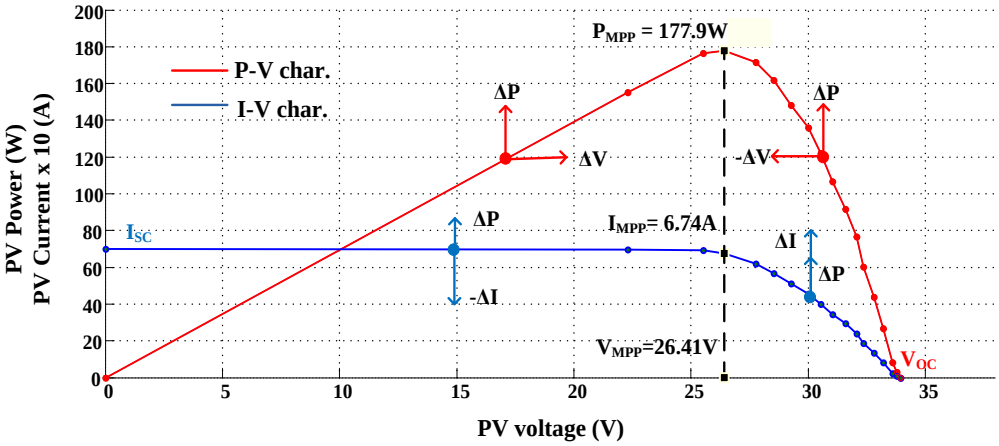

Figure 4.14 Block diagram of MPPT operation.

With the aid of these characteristics, MPP of the panel can be easily found via observing the sign of power alteration with a step change in panel voltage or current (it is the current in this case). As one of the simplest methods of MPPT, perturb and observe (P&O) algorithm is achieved in this study and block diagram is shown in Figure 4.15.

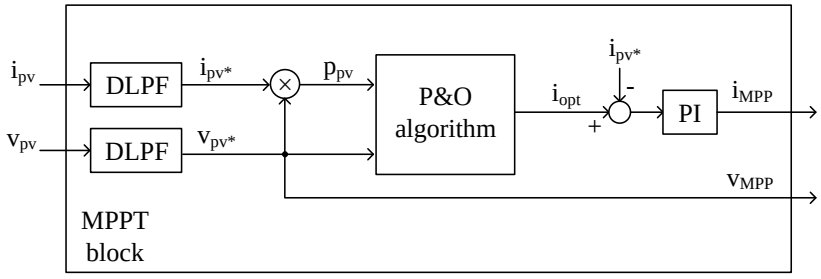

Figure 4.15 Block diagram of MPPT operation.

As it is seen from the figure, measured input voltage and current values are filtered out in order to efficiently calculate the input power (p_{pv}) via digital low pass filters (DLPF). Optimum current (i_{opt}) value is attained by means of calculating the input power and compare input power and input voltages with their previous values for every step as it is mentioned before in Figure 2.6.

According to the algorithm, if both p_{pv} and v_{pv} are increased after a perturbation step on the current, i_{opt} will be decreased since on the right hand side of P_{MPP}, input current and power are inversely proportional. On the other hand, if p_{pv} increases as v_{pv} is decreased, i_{opt} will be increased because of its characteristic on the right hand side of P_{MPP}.

The output of P&O algorithm (current reference, i_{opt}) is compared with the actual PV module current i_{pv}* and the error signal is fed to the PI controller which outputs the MPP current i_{MPP}. v_{MPP} and i_{MPP} values are utilized in order to determine the peak value of the main switch reference signal $i_{REF}(t)$ ($I_{S1,pk} = I_{MPPT}$) which draws maximum energy available from the PV module as given in (4.14).

$$i_{REF}(t) = 2 \times \left|\sin(\omega_0 t)\right| \sqrt{\frac{I_{MPP} \times V_{MPP}}{L_m \times f_{sw}}} = I_{MPPT} \times \left|\sin(\omega_0 t)\right| \tag{4.14}$$

i_{pv} and v_{pv} are read by the ADC channels of the DSP with 10kHz sampling frequency and the DLPF parameters are calculated accordingly. When the system starts up, if grid synchronization is completed, grid voltage specifications are between limits and input voltage is higher than a specified value, system starts from the open circuit condition while i_{MPP} is equal to zero at start-up and no power is drawn from the panel. After checking out grid and input conditions and confirming their conveniences, i_{opt} is increased in order to start MPPT. Once the algorithm detects an alteration on power and voltage, it starts to search for MPP. The algorithm perturbs i_{opt} with 0.04A perturbation step size at every 10ms which is equal to one half of the grid period as it is shown in Figure 4.16. In order to prevent deterioration of the output current, i_{opt} is increased at zero crossings of the grid voltage.

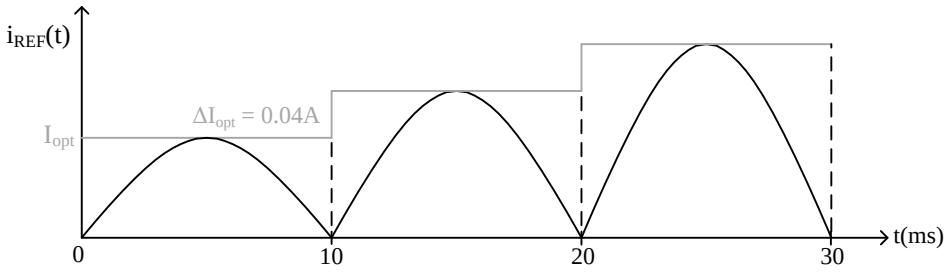

Figure 4.16 Perturbation process of MPPT algorithm.

Since the perturbation never stops and P&O algorithm continuously searches for MPP, when the algorithm reaches the MPP levels of the PV panel, it increases and decreases i_{opt} respectively causing a power fluctuation around MPP. If the perturbation step size is chosen to be very large, the elapsed time to reach MPP will be shortened but at the same time the amplitude of the power fluctuation increases significantly, causing power losses negatively effecting the efficiency of MPPT and MI. The perturbation step size and MPPT period are chosen according to the limitations explained above and the algorithm is exactly the same for both SPMI and TPIMI.

In addition, an algorithm is added up to MPPT block in order to prevent fast hard shading effects such as instant input power drops because of the objects passing through the sun and PV panel. MPPT algorithm has to sense these sudden changes and reduce the reference current accordingly. Otherwise the controller will continue to try to transfer the same amount of power to the grid and will increase the duty cycle causing the controller to enter CCM of operation and PV panel voltage drop. Further voltage drops cause the MI to shut down and loss of available power.

This hard shading algorithm reduces i_{opt} if the voltage drop on v_{pv} is greater than 0.6V with 170kHz sampling frequency, preventing CCM operation and excessive voltage drops. Voltage drop limit is determined via experimental studies.

4.5.3 Phase Locked Loop

Since MIs are designed to be grid-connected, grid synchronization with high power factor is important because of the requirements stated in the standards. As a result, determining amplitude, frequency and phase angle (θ_{grid}) of the grid is necessary. Synchronous reference frame PLL (SRF PLL) generates these information via Park transformation given in (4.15) with fast dynamic response and noise free operation by means of low pass filter characteristic for three-phase and single-phase applications with grid connection [47].

$$\begin{pmatrix} V_q \\ V_d \end{pmatrix} = \begin{pmatrix} \cos\theta_{PLL} & -\sin\theta_{PLL} \\ \sin\theta_{PLL} & \cos\theta_{PLL} \end{pmatrix} \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \tag{4.15}$$

where α-β represent stationary coordinate system (AC quantities), d-q represent rotating coordinate system (DC quantities) and θ_{PLL} represents the phase angle output of the PLL block. SRF PLL operation for three phase systems can be easily implemented since direct and quadrature axis of the d-q transformation block can be produced from the phase voltages as it is shown in Figure 4.17. Sampled stationary reference frame line to line voltages are converted to dc quantities by means of α-β transformation and Park (d-q) transformation respectively. In order to determine frequency and phase information, the DC quantity (V_d) is used in a control loop. V_d is controlled to be zero via a PI controller with a reference signal V_d^* and the controller gives the result as a compensated line frequency in radian ($\Delta\omega$).

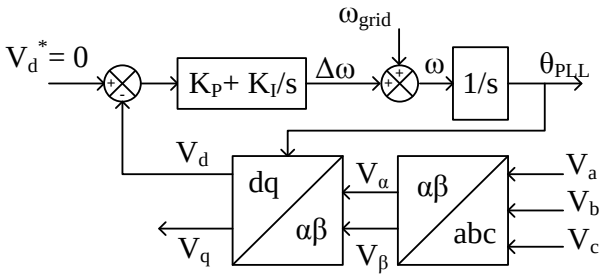

Figure 4.17 PLL structures for three phase grid synchronization.

Grid frequency is added to the result and an integral operator gives the phase angle of the utility grid which is also used as a feedback parameter in Park transformation block. Besides, there is only one phase to generate direct and quadrature axis for single-phase applications. There are various methods used in the literature in order to conduct d-q transformation such as inverse Park-based, Hilbert transform-based and transport delay-based PLL algorithms [48]. Among these SRF PLL methods, transport delay-based PLL method is achieved in this study due to its simplicity and ease of implementation as it is seen in Figure 4.18.

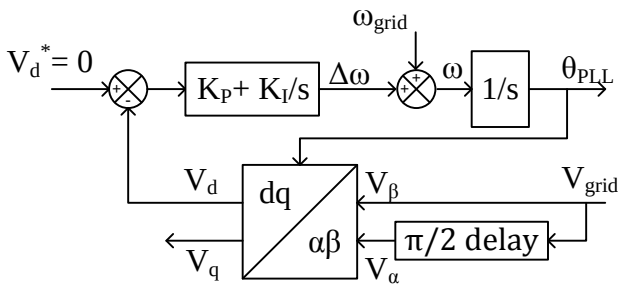

Figure 4.18 PLL structures for single-phase grid synchronization.

In order to generate the quadrature axis of the Park transformer, α and β components are constituted so that there is a 90 degree (*π/2*) phase shift with respect to the fundamental frequency of the grid voltage between V_α and V_β. As it is shown in Figure 4.19, *π/2* delay is realized with the aid of a first in first out (FIFO) buffer storing the fundamental grid data starting from the first one (x[1]) and processing the data in sequence which forms V_β.

While the fundamental grid frequency is 50Hz, 5ms (*π/2*) delay is realized by means of a counter which has a 15kHz sampling frequency. When the counting number (*n*) is equal to 75 (x[75]), the program starts to transfer the stored data to the y stack (x[1] = y[1]) which generates V_α. If "*n*" is equal to 300 which corresponds to one grid period (20ms), *n* is set to zero.

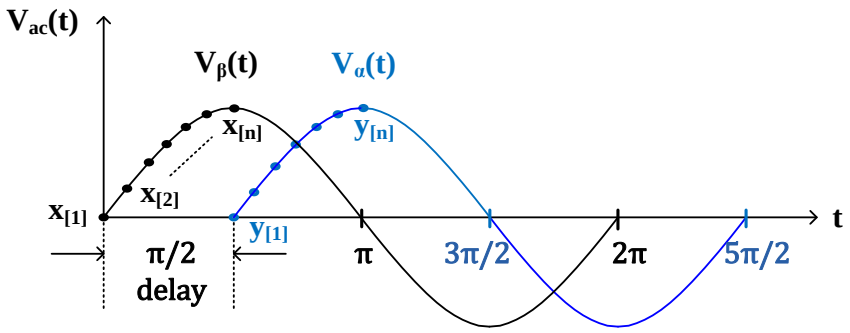

Figure 4.19 V_α and V_β of Park transformation block.

As a result of the delay method, the grid voltage sample V_β and delayed input V_α can be expressed as;

$$V_\beta = V_{grid,pk} \sin(\theta_g) \tag{4.16}$$

$$V_\alpha = -V_{grid,pk} \cos(\theta_g) \tag{4.17}$$

Using (4.15), (4.16) and (4.17), V_d and V_q can be calculated as;

$$V_q = \cos(\theta_{PLL}) \times V_\alpha - \sin(\theta_g) \times V_\beta = -V_{grid,pk} \cos(\theta_g - \theta_{PLL}) \tag{4.18}$$

$$V_d = \sin(\theta_{PLL}) \times V_\alpha + \cos(\theta_g) \times V_\beta = V_{grid,pk} \sin(\theta_g - \theta_{PLL}) \tag{4.19}$$

As can be seen from (4.18) and (4.19), while V_q gives the amplitude of the grid voltage with a negative sign, V_d is equal to zero at steady state condition where the phase angle of the grid (θ_g) is equal to the phase angle output of the PLL block (θ_{PLL}).

V_q can be used as a control parameter since the amplitude of the grid voltage must be checked. If it is not between the specified limits, the MI must stop operating in order to prevent a major malfunction and electrical failure as a safety requirement. On the

other hand in order to generate θ_{PLL}, V_d must be controlled so that the difference between θ_{PLL} and θ_g must be equal to zero at steady state.

In an attempt to set V_d to zero, it is fed to the PI controller with a reference signal V_d^* which is equal to zero as it is shown in Figure 4.15. In order to determine P and I constants of the PI controller, the transfer function of the PLL block must be calculated. Since $sin(\theta_g - \theta_{PLL})$ converges to $(\theta_g - \theta_{PLL})$ when the difference is sufficiently small, the small-signal block diagram of PLL algorithm can be shown as is the case with Figure 4.20.

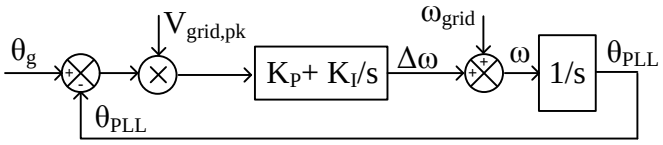

Figure 4.20 Small-signal block diagram of PLL.

From the block diagram given in Figure 4.20, the transfer function of the PLL algorithm, which is a second-order system, can be expressed as;

$$G_{PLL}(s) = \frac{\theta_{PLL}}{\theta_g} = \frac{V_{grid,pk}\left(\frac{K_P}{s} + \frac{K_I}{s^2}\right)}{1 + V_{grid,pk}\frac{K_P}{s} + V_{grid,pk}\frac{K_I}{s^2}} = \frac{V_{grid,pk}K_I + sV_{grid,pk}K_P}{V_{grid,pk}K_I + sV_{grid,pk}K_P + s^2} \qquad (4.20)$$

Since a second-order system can be expressed as $as^2 + bs + c$,using (4.20), damping ratio (ζ) and natural frequency (ω_n) can be calculated as;

$$\zeta = \frac{b}{2\sqrt{a \times c}} = \frac{V_{grid,pk}K_P}{2\sqrt{V_{grid,pk}K_I}} \qquad (4.21)$$

$$\omega_n = \sqrt{\frac{c}{a}} = \sqrt{V_{grid,pk} \times K_I} \tag{4.22}$$

The natural frequency can be written in terms of the rise time for a second order system without zeros as [49];

$$\omega_n \approx \frac{1.8}{t_r} \tag{4.23}$$

From (4.22) and (4.23), ω_n and K_I for a system with 20ms rise time can be calculated as 90 and 26 respectively. According to the analytical relation between normalized rise time ($\omega_n t_r$) and damping ratio given [49], damping ratio is determined as 0,58. Using (4.21), K_P is calculated as 0,33.

While implementing the PLL algorithm with the DSP controller, in order to increase the PLL performance, K_P and K_I constants are manipulated with respect to the experimental studies as 0.1 and 50 respectively.

The output of the PI controller is the compensated line frequency in radian ($\Delta\omega$) which will be zero at steady state. Fundamental grid frequency (ω) is added as a feed-forward controller parameter which is equal to 100π for a 50Hz utility grid. The result is fed to an integral function which generates the ramp function shown in Figure 4.21.

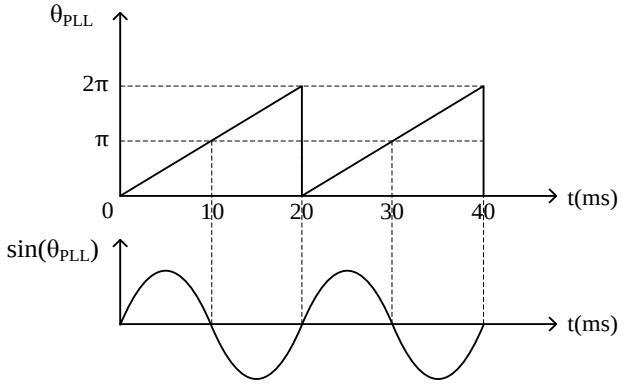

Figure 4.21 The output of PLL block (θ_{PLL}) and resulted $sin(\theta_{PLL})$ function.

The output of integral block of the PLL algorithm is a ramp function increasing continuously. In order to prevent the controller to be saturated, θ_{PLL} must be set to zero when one fundamental grid cycle is completed (i.e. $\theta_{PLL}=2\pi$). The sine and cosine functions of the software is used on the purpose of generating $sin(\theta_{PLL})$ and $cos(\theta_{PLL})$ functions which are used as the inputs of Park transformation block in order to generate V_d and V_q. Generated $sin(\theta_{PLL})$ function is then rectified via software. A dead time is inserted to the reference in order to prevent shoot-through and to ensure the compatibility between rectified unity sinusoidal reference $|sin(\theta_{PLL})|$ and UB MOSFET gate drive signals as it is shown in Figure 4.22.

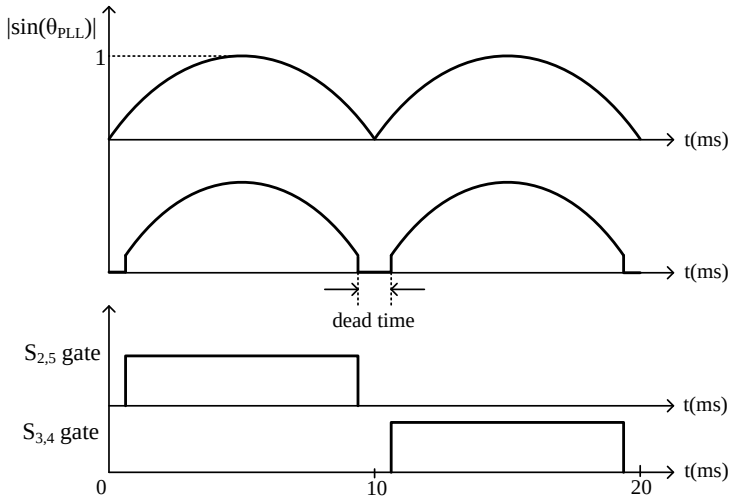

Figure 4.22 Rectified unity sinusoidal reference function with dead time inserted ($|sin(\theta_{PLL})|$) and UB gate drive signals.

The rectified unity sinusoidal reference is then multiplied with the current value determined via MPPT algorithm (I_{MPPT}) thus $i_{REF}(t)$ is generated as it is given in (4.24).

$$i_{REF}(t) = I_{MPPT} \times \left|sin(\theta_{PLL})\right| \tag{4.24}$$

The final status of $i_{REF}(t)$ and rectified grid voltage $|V_{grid}(t)|$ is shown in Figure 4.23.

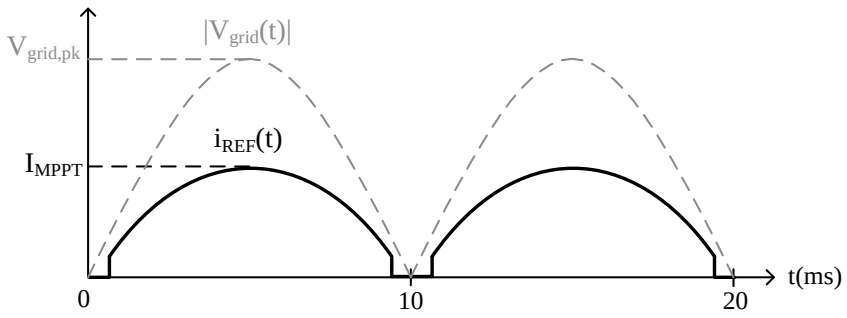

Figure 4.23 $i_{REF}(t)$ generated by the controller and rectified grid voltage $|V_{grid}(t)|$.

As it is seen from the figure, the synchronization between the grid voltage and reference current $i_{REF}(t)$ is achieved. Moreover, via grid synchronization outputs, UB MOSFET gate drive signals are generated and unfolding operation is conducted according to the polarity of the grid voltage. When the grid voltage is positive, S_2 and S_5 MOSFETs are turned on. On the other hand, if the grid voltage is negative, S_3 and S_4 MOSFETs are turned on providing a sinusoidal output current. While V_q output of the Park transformation block is used on the purpose of controlling the grid voltage amplitude if it is convenient for the limitations stated in the standards, the convenient of the grid frequency must also be determined for safety requirements as well.

In order to achieve grid frequency control, the time between the zero crossings of the grid voltage is measured via a counter which has a 170kHz sampling frequency. The frequency limits are implemented such that the MI can operate between 49Hz and 51Hz. In order to achieve frequency limits, counter lower and upper limits are determined as 1666 and 1735 respectively. In case of start-up, the system does not start to operate until the counting number is between the specified limits. If the counting number gets out of the range, MI stops operating and waits for the grid frequency to be convenient for the operation. Grid frequency control is shown in Figure 4.24.

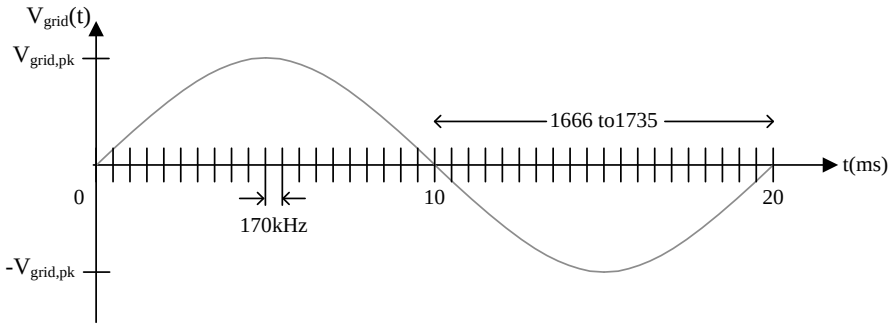

Figure 4.24 Grid frequency control.

4.5.4 Grid Current Control

Primary MOSFET of the flyback MI must be controlled such that the sinusoidal output current is synchronized with the grid and the maximum possible power is transferred. In order to achieve these circumstances, the output voltage and current must be measured and expressed in terms of the reference current as it is given in (4.12). Pseudo DC-link voltage and current (I_{pseudo}, V_{pseudo}) is measured and filtered via LPFs and read by the DSP controller as it is shown in Figure 4.9. These measurements are fed to the current regulation block of the controller in order to calculate the output values in terms of reference current $i_{REF}(t)$ via (4.12) which is called $i_{REG}(t)$ given in (4.25).

$$i_{REG}(t) = \sqrt{\frac{2 \times I_{pseudo} \times V_{pseudo}}{L_m \times f_{sw}}} \tag{4.25}$$

I_{pseudo} is measured via a sense resistor connected in series with D_1 and the signal is fed into the DSP via differential amplifiers. V_{pseudo} is measured via a voltage divider circuit and fed into the controller as well. $i_{REG}(t)$ calculated by the current regulation block and calculated $i_{REF}(t)$ via SCRG block are fed into a PI controller generating the reference signal (v_{ref}) which also has a rectified sinusoidal waveform as it is shown in Figure 4.25.

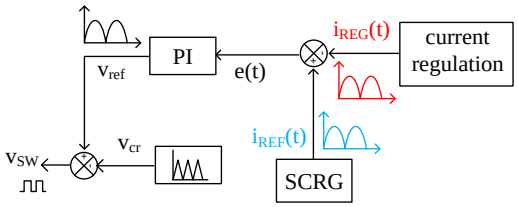

Figure 4.25 Primary MOSFET control signal generation.

Figure 4.26 shows the MOSFET gate signal ($v_{S1gate}(t)$) generation via comparing carrier signal ($v_{cr}(t)$) and the reference signal ($v_{ref}(t)$) which is the PI controller output. The resulting S_1 current can be also seen which has a triangular waveform because of the DCM operation and a rectified sinusoidal peak characteristic with an amplitude of I_{MPPT}.

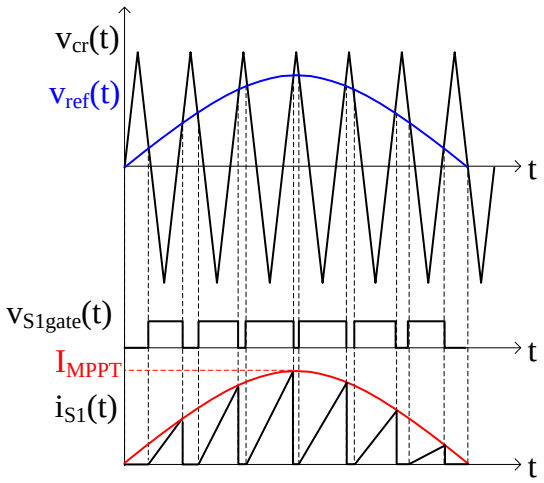

Figure 4.26 S_1 gate signal ($v_{S1gate}(t)$), carrier signal (v_{cr}), reference signal (v_{ref}) and resulting S_1 current.

4.5.5 Interleaved Control Operation

With the intent of controlling TPIMI phases, a very simple control block is implemented as shown in Figure 4.27. The gate drive signal (v_{S2}) of the second phase MOSFET (S_2) is generated by means of comparing the reference signal (v_{ref}) with a carrier signal which is 180° phase shifted due to two-phase operation with

respect to the fundamental carrier signal (v_{cr1}). The resultant switching signal (v_{S2}) is also 180° phase shifted with respect to v_{S1} providing current sharing between two-phases.

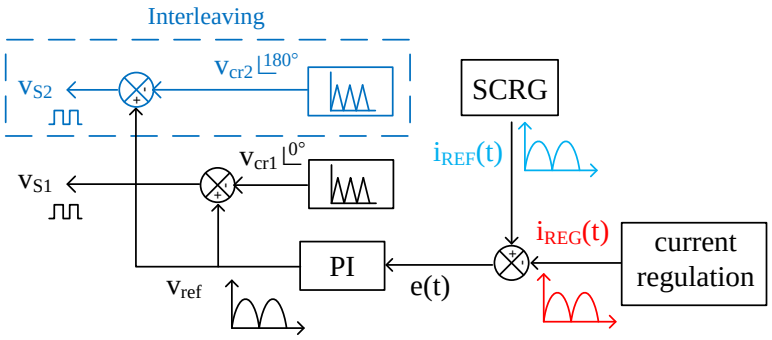

Figure 4.27 Control of TPIMI MOSFETs via interleaving.

4.6 Summary

In this chapter, main structure of the single-phase and two phase interleaved flyback-based MI topologies are clarified. In addition, the basic operating principle of flyback converter is explained and the DCM switching strategy and benefits are represented. Moreover, the interleaving operation and control providing current sharing and switching stress reduction is explained. Additionally, the control strategy including SCRG, MPPT, PLL and grid current control is explained in detail.

CHAPTER 5

DESIGN AND IMPLEMENTATION OF SINGLE-PHASE AND INTERLEAVED FLYBACK-BASED MICRO-INVERTERS

5.1 Introduction

Design parameters of MI topologies show an alteration according to the specifications of PV panel, utility grid and the requirements for a MI such as high efficiency, long lifetime, low THD, high PF, fast transient response, etc. The design parameters of SPMI and TPIMI are calculated in order to fulfill these requirements. Starting from the input, the design steps will be explained in detail in the next sections respectively.

5.2 Decoupling Capacitor Sizing

Starting from the input of the MI, decoupling capacitor sizing is crucial with the intent of achieving an efficient MPPT operation as it is discussed in Section 3.1. While a MI constitutes an interface between the PV module and the utility grid, it has to handle the instantaneous power mismatch via decoupling capacitors.

As it is explained before, on the purpose of an efficient use of PV module energy, the $sin^2(\omega t)$ ripple on the PV module voltage must be lower than 8.5% of the average PV module voltage. Sunrise SR-M660230 PV panel is used as a power supply in the experiments which has 35.92V_{OC} , 29.2V_{MPP} and 7.88A I_{MPP} at 230W rated panel power. The $sin^2(\omega t)$ ripple on the PV module voltage is considered to be 5.5% which is lower than 8.5% limit and corresponds to 1.606V ripple amplitude.

According to the given specifications and using (3.6), in case of a connection to utility grid with 50Hz fundamental frequency, the required decoupling capacitance C_D can be calculated as in (5.1);

$$C_D = \frac{230}{2\pi 50 \times 29.2 \times 1.606} \tag{5.1}$$

which gives the result of 15.6mF decoupling capacitance. In order to fulfill the requirements. In order to reduce the ESRs of the total capacitance, seven 2200μF/50V electrolytic capacitors are connected in parallel at the input of the MIs which makes 15.4mF in total corresponds to 1.63V ripple at 230W input power. In addition, 100nF/100V ceramic capacitors are connected to the electrolytic capacitors in parallel to reduce the total ESR of the capacitor block and filter out the HF noise.

5.3 Flyback Transformer Design

In order to obtain the required magnetizing inductance (L_m) of the flyback transformer, design parameters such as, min. input voltage, max. output voltage, switching frequency, max. duty cycle, turns ratio, input and output currents are vital. According to these specifications, required L_m is calculated using (5.2) - (5.24).

As it is mentioned before DCM operation is selected as a switching method because of its numerous advantages. As a result, while calculating L_m, DCM operation must be ensured at all the operating points which is highly related with the transformer turns ratio n, duty cycle D and turn-off time period t_{off}. In order to transfer sinusoidal current to the grid, as is the case with $I_{S1,pk}$, the duty cycle must include a sinusoidal part as it is given in (5.2).

$$D(t) = D_{pk} \sin(\omega_0 t) \qquad \omega_0 t \in [0, \pi] \tag{5.2}$$

where D_{pk} is the peak duty cycle when $\omega_0 t$ is equal to $\pi/2$. Due to DCM operation, t_{off} is shorter than the difference between peak turn-on time period of MOSFET $t_{on,pk}$ and the switching period T_s as given in (5.3).

$$t_{off} \leq T_s - t_{on,pk} \tag{5.3}$$

where $t_{on,pk}$ is the product of T_s and D_{pk}. In order to define t_{off}, magnetizing inductor equation referred to the secondary side must be considered as shown in (5.4).

$$V_{grid,pk} = L_s \frac{di_s(t)}{dt} \tag{5.4}$$

While T_s is a very short duration, the voltage seen by the secondary side inductance of the transformer L_S is represented by $V_{grid,pk}$ and $i_S(t)$ is the secondary side inductor current. When these parameters are referred to the primary side using (4.5) and (4.6), the equation can be rewritten as;

$$V_{grid,pk} = \frac{L_m}{n^2} \frac{n(di_{PV}(t))}{dt} \tag{5.5}$$

When (5.5) is simplified and rewritten so that dt is the turn-off time period t_{off}, using (4.1) the equation can be expressed as;

$$V_{grid,pk} = \frac{V_{PV}}{n \times t_{off} \times f_{sw}} \times D_{pk} \tag{5.6}$$

According to (5.6), t_{off} can be expressed as;

$$t_{off} = \frac{V_{PV}}{nV_{grid,pk} \times f_{sw}} \times D_{pk} \tag{5.7}$$

Using (5.3) and (5.7), peak duty cycle D_{pk} can be expressed as;

$$D_{pk} \leq \frac{nV_{grid,pk}}{nV_{grid,pk} + V_{PV}} \tag{5.8}$$

(5.8) can be simplified as;

$$D_{pk} \leq \frac{1}{1+\lambda/n} \tag{5.9}$$

where;

$$\lambda = \frac{V_{PV}}{V_{grid,pk}} \tag{5.10}$$

As it is seen from (5.9), the turns ratio of the transformer windings is very important and must be carefully selected in order to ensure DCM operation. While selecting the turns ratio *n*, limitations such as MI power density, switching stress on the semiconductors and the maximum semiconductor current must be considered [43]. According to the flyback converter formula given in (5.11), turns ratios of 0.158 and 0.167 are selected for SPMI and TPIMI topologies respectively.

$$\frac{V_{grid,pk}}{V_{PV,min}} = \frac{\mathrm{D_{pk}}}{(1-\mathrm{D_{pk}})}\frac{1}{\mathrm{n}} \tag{5.11}$$

The input power of the MI is another important parameter effecting the value of the magnetizing inductance. It must be able to transfer the maximum input energy to the secondary side and remain in DCM region. In an ideal inverter, input and output powers are equal to each other and can be written as;

$$P_{PV} = V_{PV} \times I_{PV} = P_{grid} \tag{5.12}$$

I_{PV} is the average input current of MI which can be calculated by means of integrating MOSFET current $i_{S1}(t)$ over a period which is, in this case, equal to half of the grid period because of rectification;

$$I_{PV} = \frac{2}{T_{grid}} \int_{0}^{2/Tgrid} i_{S1}(t).dt \tag{5.13}$$

Since I_{PV} consists of triangular waveforms, (5.13) can be rewritten as;

$$I_{PV} = \frac{2}{T_{grid}} \sum_{i=1}^{\chi} \int_{0}^{t_{on}} i_{S1}(t).dt \tag{5.14}$$

where i = 1,2,3... x; and x is the number of switching cycles per half grid period given as;

$$\chi = \frac{T_{grid}}{2T_{sw}} \tag{5.15}$$

and $t_{on}(t)$ is the turn-on time period throughout one grid period which is expressed as;

$$t_{on}(t) = D_{pk} T_{sw} sin(\omega_0 t) \quad \text{where} \quad sin(\omega_0 t) = sin(2\pi / T_{grid}) = sin(i\,\pi / \chi) \tag{5.16}$$

Using (4.2), (5.14), (5.15) and (5.16), I_{PV} can be rewritten as;

$$I_{PV} = \frac{V_{PV} \times \chi \times D_{pk}^{\ 2} \times T_{sw}^{\ 2}}{T_{grid} \times L_m} \frac{1}{\chi} \sum_{i=1}^{\chi} sin^2(i\,\pi / \chi) \tag{5.17}$$

where;

$$\frac{1}{\chi} \sum_{i=1}^{\chi} sin^2(i\,\pi / \chi) = \frac{1}{2} - \frac{1}{2} cos(i\,2\pi / \chi) \tag{5.18}$$

as a result,

$$\frac{1}{2}-\frac{1}{2}\cos(i\,2\pi/\chi)=\frac{1}{2}-\frac{1}{4\chi}\left[\frac{\sin\left[\left(2\pi+\pi/\chi\right)\right]}{\sin(\pi/\chi)}-1\right]=\frac{1}{2} \tag{5.19}$$

from (5.17) and (5.19) I_{PV} can be rewritten as;

$$I_{PV}=\frac{1}{2}\frac{V_{PV}\times\chi\times D_{pk}{}^{2}\times T_{sw}{}^{2}}{T_{grid}\times L_m} \tag{5.20}$$

Using (5.15) , (5.20) can be simplified as;

$$I_{PV}=\frac{1}{4}\frac{V_{PV}\times D_{pk}{}^{2}}{L_m\times f_{sw}} \tag{5.21}$$

Using (5.12) and (5.21), PV power (P_{PV}) can be rewritten as;

$$P_{PV}=\frac{1}{4}\frac{V_{PV}{}^{2}\times D_{pk}{}^{2}}{L_m\times f_{sw}} \tag{5.22}$$

As it is mentioned before, for an ideal system, input and output powers must be equal. According to this statement, output power (P_{grid}) can be expressed as;

$$P_{grid}=I_{grid,rms}\times V_{grid,rms}=\frac{1}{4}\frac{V_{PV}{}^{2}\times D_{pk}{}^{2}}{L_m\times f_{sw}} \tag{5.23}$$

Using (5.11) and (5.23) P_{grid} can be rewritten as;

$$P_{grid}=\frac{1}{2}\frac{\lambda^{2}\times D_{pk}{}^{2}}{L_m\times f_{sw}}\times V_{grid,rms}{}^{2} \tag{5.24}$$

where, $V_{grid,rms} = V_{grid,pk} / \sqrt{2}$.

Finally if (5.24) is rearranged, L_m can be expressed as;

$$L_m = \frac{1}{2} \frac{\lambda^2 \times D_{pk}^{\ 2}}{P_{grid} \times f_{sw}} \times V_{grid,rms}^{\ 2} \tag{5.25}$$

Design parameters while calculating L_m for both SPMI and TPIMI are given in Table 5.1. While determining the power characteristics of the PV panel with a resistive load and throughout the experimental studies with SPMI and TPIMI connected, the PV panel power never reached 230W rated power. In accordance with these circumstances, rated power of the MI is decided to be 200W.

Table 5.1 Basic design parameters

Rated input power (W)	200
Minimum input voltage ($V_{PV,min}$)	25
Maximum grid voltage ($V_{grid,pk}$)	310
Switching frequency f_{SW} (kHz)	170
Switching period T_{SW} (μs)	5.88
SPMI turns ratio n	0.158
TPIMI turns ratio n	0.167

5.3.1 SPMI Transformer Design

HF transformer of the SPMI is designed according to the parameters given in Table 5.1. λ and the peak duty cycle D_{pk} are calculated using (5.9) and (5.11) as 0.08 and 0.66 respectively. From (5.3) the maximum value of t_{off} is calculated as 2μs where, $t_{on,pk}$ is equal to 3.88μs.

Since the RMS voltage of the utility grid is 220V and rated power is 200W, using (5.25), L_m is calculated as ;

$$L_m = \frac{1}{2} \times \frac{0.08^2 \times 0.66^2}{200 \times 170000} \times 220 = 1.98\,\mu H \tag{5.26}$$

While implementing the designed transformer, the magnetizing inductance of the prototype is measured to be 2μH.

Due to high shielding performance, higher magnetic cross-section allowing higher power ratings and reducing the required primary number of turns, RM-14 type ferrite core without a center hole is used while implementing the designed transformer [50]. The numbers of primary and secondary (N_1,N_2) turns are selected to be 3 and 19 respectively corresponding to turns ratio of 0.158.

5.3.2 TPIMI Transformer Design

HF transformer of the TPIMI is designed according to the parameters given in Table 5.1. The peak duty cycle D_{pk} is calculated using (5.9) as 0.675 while λ is the same with SPMI which is equal to 0.08. From (5.3) the maximum value of t_{off} is calculated as 1.9μs where, $t_{on,pk}$ is equal to 3.98μs. Since the rated power of each phase is equal to 100W, using (5.25), L_m is calculated as ;

$$L_m = \frac{1}{2} \times \frac{0.08^2 \times 0.675^2}{100 \times 170000} \times 220 = 4.15\,\mu H \tag{5.27}$$

While implementing the designed transformer, the magnetizing inductance of the prototype is measured to be 3.93μH. As it is mentioned for SPMI, due to its high performances, RM-12 type ferrite core without a center hole is used while implementing TPIMI HF transformers. The numbers of primary and secondary (N_1,N_2) turns are selected to be 3 and 18 respectively corresponding to 0.167 turns ratio as it is indicated before.

5.4 Snubber Design

In Figure 5.1, flyback converter stage of the MI is shown where L_m is the magnetizing inductance, L_{lk} is the leakage inductance of the HF transformer. C_{oss} represents the parasitic output capacitance of the primary MOSFET S_1.

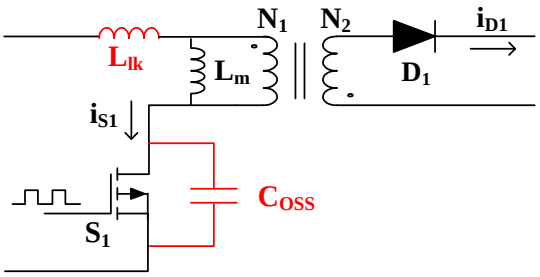

Figure 5.1 Flyback converter stage of the MI.

Primary MOSFET voltage V_{S1} and current I_{S1} , output diode current I_{D1} are shown in Figure 5.2.

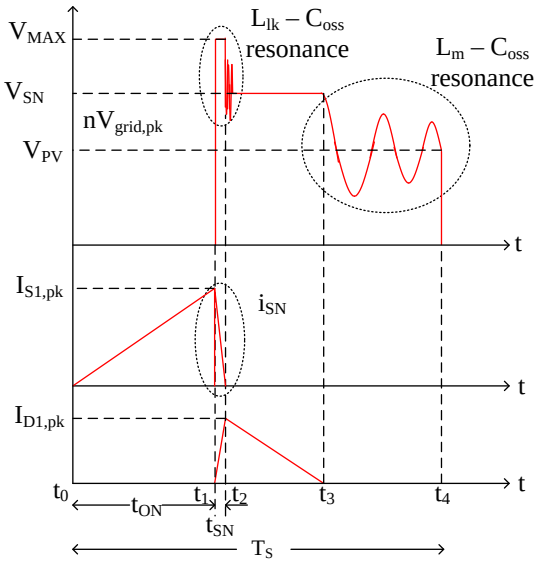

Figure 5.2 S1 voltage and current (V_{S1} - I_{S1}) and D_1 current (I_{D1}) during one switching period T_S.

A shown in the figure, when S_1 is turned off, because of the resonation between L_{lk} and C_{oss}, a voltage spike takes place on V_{S1}, while the primary current flowing through L_{lk} (I_{S1}) goes to zero with a very high *di/dt* ratio which is equal to $I_{S1,pk} / T_{SN}$. Moreover, when I_{D1} equals to zero at t_3 time instant, a resonation between L_m and C_{oss} takes place on the MOSFET voltage until the switching period T_S ends. $nV_{grid,pk}$ is the output voltage reflected to the primary side and V_{MAX} is the maximum value of V_{S1} during turn-off.

In order to protect the primary switch and limit the voltage spike taking place on V_{S1} during T_{SN} time period, an RCD snubber consisting of a diode D_{SN}, capacitor C_{SN} and a resistor R_{SN} is added to the circuit as it is shown in Figure 5.3. When S_1 turns off at t_1 time instant, V_{S1} increases to $V_{PV} + nV_{grid,pk}$.

When V_{S1} exceeds $V_{PV} + nV_{grid,pk}$, the primary current starts to flow through D_{SN} (i_{SN}). At that time, the voltage on the leakage inductance L_{lk} is equal to the difference between C_{SN} voltage and reflected output voltage (V_{SN} - $nV_{grid,pk}$). Therefore the alteration on i_{SN} during TSN can be expressed as;

$$\frac{di_{SN}}{dt} = \frac{i_{S1,pk}}{t_{SN}} = -\frac{(V_{SN} - nV_{grid,pk})}{L_{lk}} \tag{5.28}$$

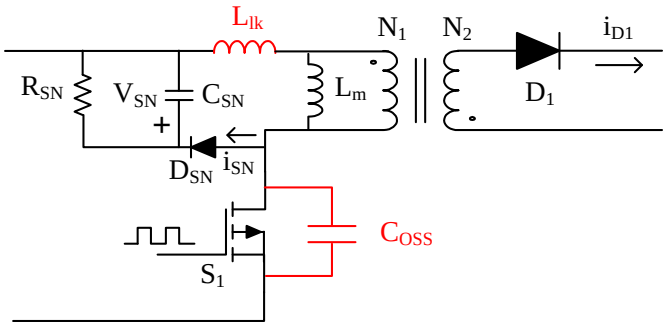

Figure 5.3 Flyback converter stage of the MI with an RCD snubber.

Using (5.28), t_{SN} can be rewritten as;

$$t_{SN} = \frac{L_{lk}}{(V_{SN} - nV_{grid,pk})} \times \mathrm{i}_{S1,pk} \tag{5.29}$$

In order to determine the RCD snubber resistance R_{SN} and capacitance C_{SN} values, snubber voltage V_{SN} and the power dissipated on R_{SN} must be determined at minimum input voltage and rated power. In the literature its indicated that, on the purpose of designing an efficient snubber circuit, V_{SN} must be selected as 2 or 2.5 times $nV_{grid,pk}$ [51]. Moreover, the dissipated power P_{SN} can be calculated as;

$$P_{SN} = V_{SN} \frac{i_{S1,pk} \times t_{SN}}{2} f_{sw} \tag{5.30}$$

Combining (5.29) and (5.30), P_{SN} can be rewritten as;

$$P_{SN} = \frac{1}{2} {i_{S1,pk}}^2 L_{lk} f_{sw} \frac{V_{SN}}{(V_{SN} - nV_{grid,pk})} \tag{5.31}$$

While designing the HF transformer, the leakage inductance generally taken as 3% of L_m and can be reduced down to 1% with a better winding performance. In this study, it will be taken as 3% as well. Moreover, although for a DC-DC flyback converter, maximum MOSFET current is constant with respect to time, for a MI, it has a sinusoidal waveform. According to this statement, P_{SN} can be modified as;

$$P_{SN} = \frac{1}{2} {i_{S1,rms}}^2 L_{lk} f_{sw} \frac{V_{SN}}{(V_{SN} - nV_{grid,pk})} \tag{5.32}$$

where peak MOSFET current is replaced with its RMS value ($i_{S1,rms}$). For a DC-DC flyback converter $i_{S1,rms}$ can be expressed as;

$$i_{S1,rms} = i_{S1,pk}\sqrt{\frac{D}{3}} \tag{5.33}$$

where D is the duty cycle. (5.33) must be recalculated considering sinusoidal waveforms which is given by integrating peak MOSFET current $i_{S1,pk}(t)$ over a utility grid period;

$$I_{S1,rms} = \sqrt{\frac{1}{3T_{grid}}\int_{0}^{1/Tgrid} i_{S1,pk}(t)^2.D.dt.} \tag{5.34}$$

where $I_{S1,pk}(t)$ and D(t) can be expressed using (4.13), (5.2) and (5.22) as;

$$i_{S1,pk}(t) = 4\times sin^2(\omega_0 t)\frac{P_{PV}}{L_m \times f_{sw}} \tag{5.35}$$

$$D(t) = \frac{2\times\sqrt{P_{PV}\times L_m \times f_{sw}}}{V_{PV}} sin(\omega_0 t) \tag{5.36}$$

Using (5.34), (5.35) and (5.36), $I_{S1,rms}$ can be written as;

$$I_{S1,rms} = \frac{4}{3}\sqrt{\frac{2}{\pi}\frac{P_{PV}}{V_{PV}}\sqrt{\frac{P_{PV}}{L_m \times f_{sw}}}} \tag{5.37}$$

Using V_{SN} and P_{SN}, R_{SN} can be calculated as;

$$R_{SN} = \frac{V_{SN}^{\ 2}}{P_{SN}} = \frac{V_{SN}^{\ 2}}{\frac{1}{2} i_{S1,rms}^{\ 2} L_{lk} f_{sw} \frac{V_{SN}}{(V_{SN} - nV_{grid,pk})}} \tag{5.38}$$

On the other hand, the capacitance of the snubber capacitor C_{SN} can be calculated according to the statement that the reasonable voltage ripple on V_{SN} (ΔV_{SN}) is 5-10% of V_{SN} [51]. Using given statement, C_{SN} can be calculated as given in (5.39);

$$C_{SN} = \frac{V_{SN}}{\Delta V_{SN} R_{SN} f_{SW}} \tag{5.39}$$

As it is given in Section 5.3.1 and 5.3.2, implemented magnetizing inductances of SPMI and TPIMI are measured to be 2µH and 3.93µH respectively. The minimum PV panel voltage is accepted as 25V. The output voltage reflected to the primary is calculated as 49V and 52V for SPMI and TPIMI respectively, where $V_{grid,pk}$ is 310V.

The peak MOSFET currents for SPMI and TPIMI are calculated using (4.2) as 48.5A and 25.26A respectively. Using (5.37) RMS currents are calculated as 14.8A and 7.44A as well. Via assuming that the leakage inductances are 3% of magnetizing inductances, they are calculated as 60nH and 117nH.

With the statements given above, the upper limit for V_{S1} which is V_{MAX} is selected to be 150V for both SPMI and TPIMI topologies where V_{SN} will be 125V while $V_{SN} = V_{MAX} - V_{PV}$. Using the calculated values and (5.32), P_{SN} is calculated as 1.84W and 0.94W for SPMI and TPIMI respectively.

If ΔV_{SN} is chosen to be 2% of V_{SN} , from (5.38) and (5.39), snubber resistances are calculated as 8.5kΩ and 16.6kΩ and capacitances are calculated as 35nF and 18nF for SPMI and TPIMI respectively. While implementing the RCD snubber circuits

resistors of 9.1kΩ and 18kΩ and capacitors of 47nF and 22nF are used. The calculated snubber design parameters are given together in Table 5.2.

Table 5.2 Snubber design parameters of SPMI and TPIMI

Topology	**SPMI**	**TPIMI**
Magnetizing inductance, L_m (μH)	2	3.93
Leakage inductance, L_{lk} (nH)	60	117
Reflected output voltage, nV$_{grid,pk}$ (V)	49	52
Peak MOSFET current, $I_{S1,pk}$ (A)	48.5	25.26
MOSFET RMS current, $I_{S1,rms}$ (A)	14.8	7.44
Maximum MOSFET voltage, V_{MAX} (V)	150	150
Snubber voltage, V_{SN} (V)	125	125
Snubber power consumption, P_{SN} (W)	1.84	0.94x2
Snubber resistance, R_{SN} (kΩ)	9.1	18
Snubber capacitance, C_{SN} (nF)	47	22

5.5 Unfolding Bridge Structure

As it is mentioned before, an unfolding bridge shown in Figure 5.4, operating at mains frequency unfolds the rectified sine wave pseudo DC-link voltage (current) into sinusoidal form via switching MOSFETs (S_2-S_5) at zero crossings of the grid voltage in accordance with the polarity.

In order to filter out high frequency triangular pulses on the flyback output current, a pseudo DC-link capacitor C_P is placed between flyback converter output and UB.

Moreover, with the intent of protecting the circuit from instant voltage rises, a varistor is placed in parallel with C_P has a clamping voltage compatible with the utility grid specifications. The same unfolding bridge structure is implemented for both SPMI and TPIMI topologies.

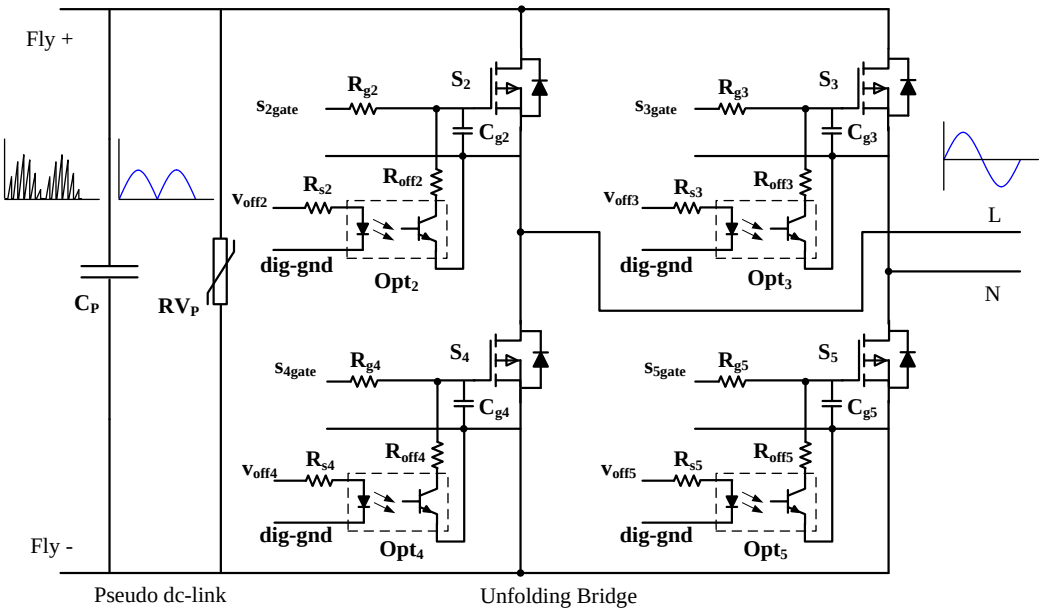

Figure 5.4 Unfolding bridge structure of SPMI and TPIMI.

On the purpose of driving the UB MOSFETs, gate turn-on signals ($s_{gate2\text{-}5}$) are provided by the isolated UB gate drive circuit which will be explained in detail later in this section. In addition to the gate drive signals, turn-off signals are provided by the DSP controller.

When the polarity of the grid voltage is changed from positive to negative, DSP sends a signal with high level (v_{off}) to the opto-couplers of the related MOSFET group ($S_{2,5}$) which turns the opto-couplers on and via R_{off} resistances with small values (1Ω), gate voltages of the MOSFETs are lowered under threshold voltage and turn the MOSFETs off. The procedure is the same when the polarity of the grid voltage changes from negative to positive for MOSFETs $S_{3,4}$.

By means of this process, the turn-on of the contrary MOSFETs and shoot-through situation are prevented. Moreover isolation between DSP controller and the UB MOSFETs is conducted via opto-coupler utilization which is also seen in [50]. The pseudo DC-link and grid voltages, turn-on and turn-off signals of the UB are given in Figure 5.5.

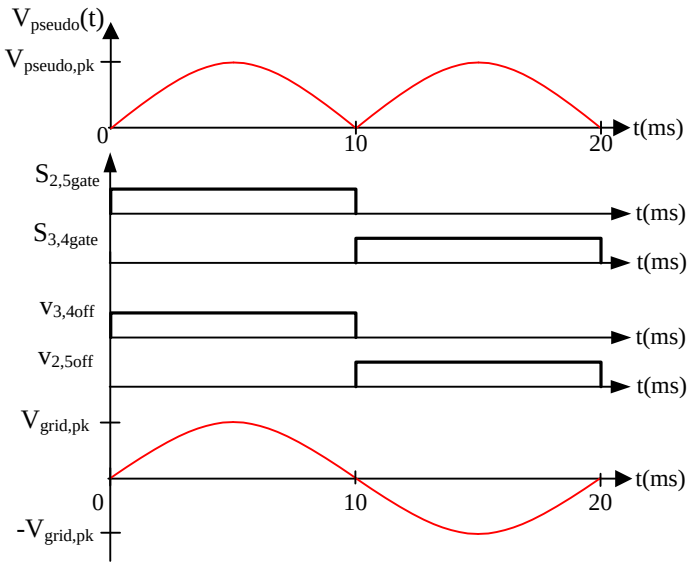

Figure 5.5 Pseudo DC-link voltage $V_{pseudo}(t)$, gate turn-on signals ($S_{gate2\text{-}5}$), gate turn-off signals ($v_{off2\text{-}5}$) and grid voltage $V_{grid}(t)$.

The gate driver circuit of the UB is designed to provide isolation between high side and low side MOSFETs and the DSP controller as it is shown in Figure 5.6. The circuit consists of an IR2113 gate driver, RC filters, pulse transformers with 1:1 turns ratio and diodes. 150kHz gate drive signals with 3.3V amplitude provided by the PLL algorithm of the DSP controller (bridge control+ for $S_{2,5}$ and bridge control- for $S_{3,4}$) are sent to the IR2113 gate driver shown in Figure 5.7.

The gate driver is supplied by 15V which is generated by auxiliary supply circuits increasing the amplitude of the drive signals from 3.3V to 15V. A resistor and a capacitor is connected in series with the high side and low side outputs of the gate driver (HO-LO) in order to filter 150kHz pulses and the DC components on the signals. Output signals of IR2113 with 15V amplitude are fed to the pulse transformers afterwards.

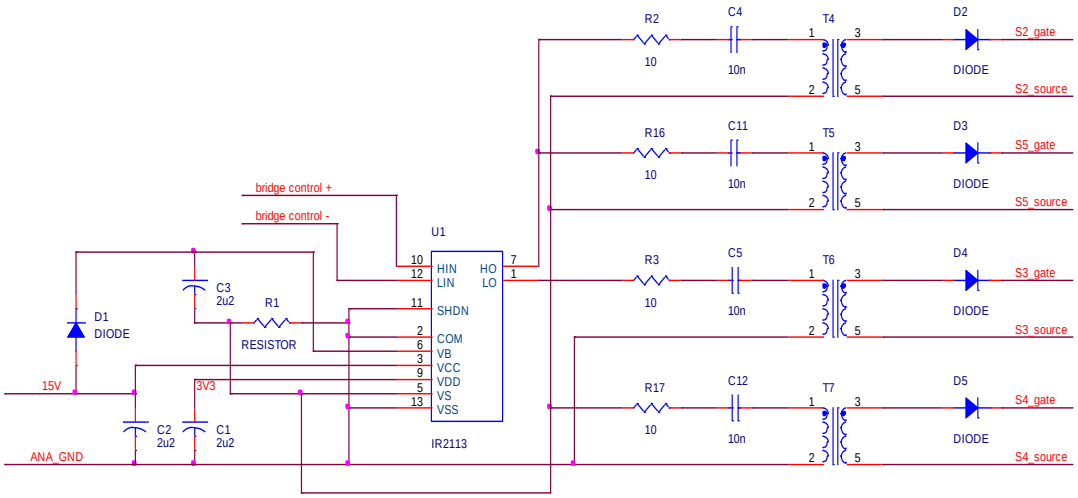

Figure 5.6 Unfolding bridge gate drive circuit.

Diodes connected in series with the pulse transformers rectify the negative parts of the drive signals and 50Hz gate drive signals with 15V amplitude ($s_{gate2\text{-}5}$) are fed to the UB MOSFETs. As it is mentioned before, in order to prevent shoot-through situation, a dead time is inserted between the gate signals.

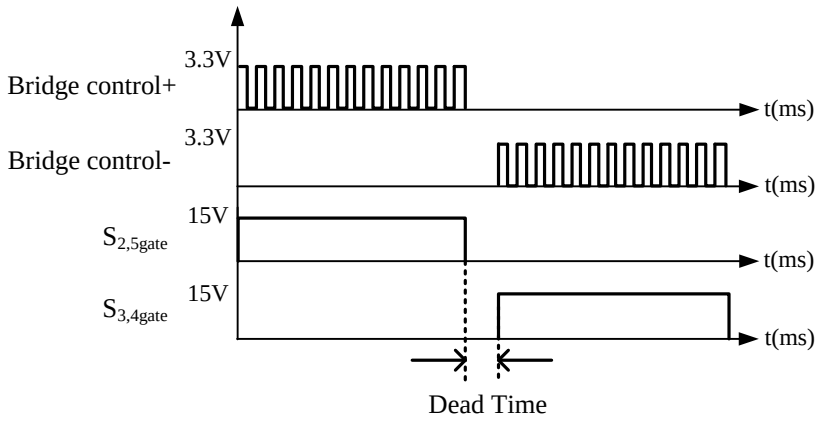

Figure 5.7 High frequency UB drive signals (bridge control+, bridge control) and filtered pulse transformer outputs ($S_{gate2\text{-}5}$).

The unfolding bridge expressed above is followed by an LCL filter which filters out high frequency ripples on the output current and voltage and achieve grid connection which will be explained in detail in the next section.

5.6 Output Filter Design

The optimum design of the output filter of a MI is crucial in order to filter out the high frequency ripples on the output current effectively and achieve grid connection which influences the THD, PF and efficiency performance of the overall system. For a well designed output filter, the attenuation at the switching frequency must be adequate without additional oscillations. There are various filter types to achieve grid connection such as L, LC and LCL filter as it is shown in Figure 5.8. Among these filter types LCL filter seems to be the best choice while it has a good ripple attenuation performance with smaller inductances improving transient response of the MI [52][53].

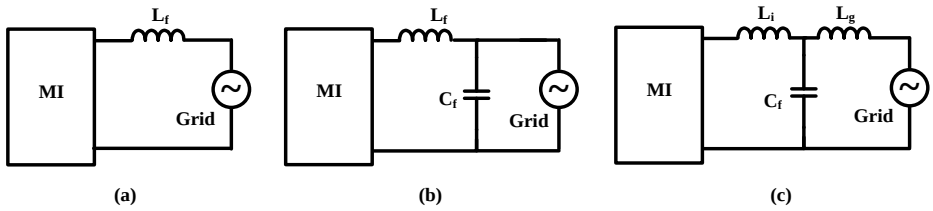

Figure 5.8 Filter types connected between MI and utility grid (a) L filter (b) LC filter and (c) LCL filter.

While the HF damping performance of an L filter is low, LC filter has a better HF damping performance than L filter. However, the oscillations on the utility grid voltage causes excessive currents on the filter capacitor C_f. LCL filter has a good damping performance and the oscillations on the grid voltage does not effects the filter capacitor by means of the inductor connected between the capacitor and the utility grid. LCL filters are sensitive to the oscillations around switching frequency and these oscillations can be amplified by the filter [53]. The simplest way to

prevent further amplification of the oscillations around switching frequency and improve the damping performance is to connect a damping resistor R_d to the filter. While there are various connection configurations as it is shown in Figure 5.9, the damping resistor R_d is connected in series with the filter capacitor C_f in this study.

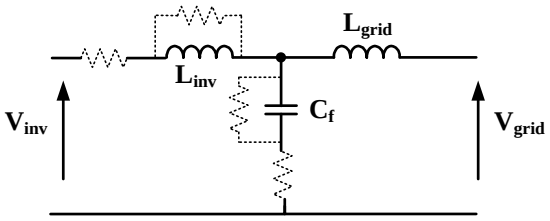

Figure 5.9 Possible connections of damping resistor R_d.

The LCL filter configuration consisting of inverter side inductor (L_{inv}), filter capacitor (C_f), grid side inductor (L_{grid}) and a R_d damping resistor and the small-signal block diagram are given in Figure 5.10(a) and 5.10(b) respectively.

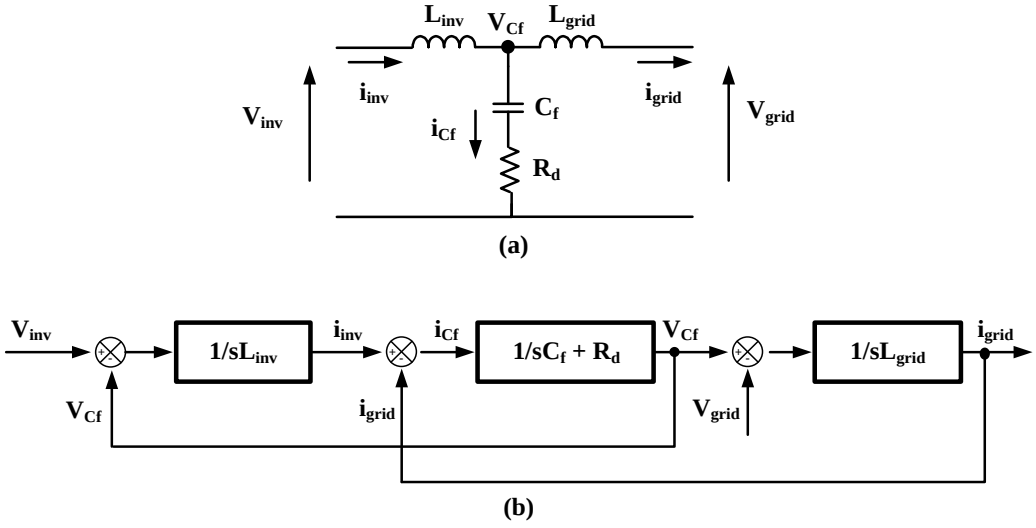

Figure 5.10 The LCL filter (a) configuration with an R_d damping resistor and (b) small-signal block diagram.

On the purpose of designing LCL filter having adequate attenuation around switching frequency, the resonance frequency must be well calculated. In the literature, the high and low limits for the optimum corner frequency is stated to be one half of the switching frequency and at ten times the grid frequency respectively [52]. Resonance frequency of the LCL filter is given in (5.40) as;

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{inv} + L_{grid}}{L_{inv} \times L_{grid} \times C_f}} \tag{5.40}$$

and the equation for specifying the damping resistor value is given as;

$$R_d = \frac{1}{3 \times (2\pi f_{res}) \times C_f} \tag{5.41}$$

According to the specified statements and formulas given in (5.40) and (5.41), the required filter resonance frequencies are chosen to be 20kHz and 40kHz for SPMI and TPIMI topologies respectively. In accordance with the inductors and capacitances used, the resonance frequencies of the implemented LCL filters are 23kHz and 48kHz for SPMI and TPIMI topologies. LCL filter parameters are listed in Table 5.3.

Table 5.3 LCL filter parameters of SPMI and TPIMI topologies

Topology	**SPMI**	**TPIMI**
Inverter side inductance, L_{inv} (μH)	270	100
Grid side inductance, L_{grid} (μH)	180	100
Filter capacitance, C_f (nF)	440	220
Resonance frequency f_{res}*(kHz)*	23	48
Damping resistance, R_d (Ω)	5	5

As it is seen from the table, f_{res} of the LCL filter of TPIMI is twice the f_{res} of SPMI, since 180° phase shifted operation doubles the ripple frequency of the TPIMI. As a

result, the resonance frequency of the TPIMI is selected to be double and filter inductors and capacitor with smaller values are used lowering the cost and improving the transient response of the filter.

5.7 Measurement and Auxiliary Supply Circuits

In order to control the MI effectively, currents and voltages related with the control loop must be measured accurately. On the other hand, measurement devices must be cost effective and simple to implement as well. As a result, the measurement circuits are designed accordingly. Moreover, the auxiliary supply circuits are implemented providing the supply and reference voltages required by the amplifiers, current sensors and MOSFET gate driver ICs.

5.7.1 Voltage and Current Measurement

Accurate and noise free measurement of the input current and voltage is vital for an efficient MPPT operation. LTS 15-NP LEM current transducer is used as a PV current sensor. The number of primary turns is selected as 3, in accordance with the average input current which has a maximum value of 8A. In addition, a voltage divider circuit is implemented in order to measure the PV panel voltage providing ease of implementation. The measured signals are filtered out and fed to the DSP controller as it is seen in Figure 5.11. With the intent of limiting the maximum signal amplitude to 3.3V, a 3V3 zener diode is connected preventing the ADC channel of the DSP controller to burn-out.

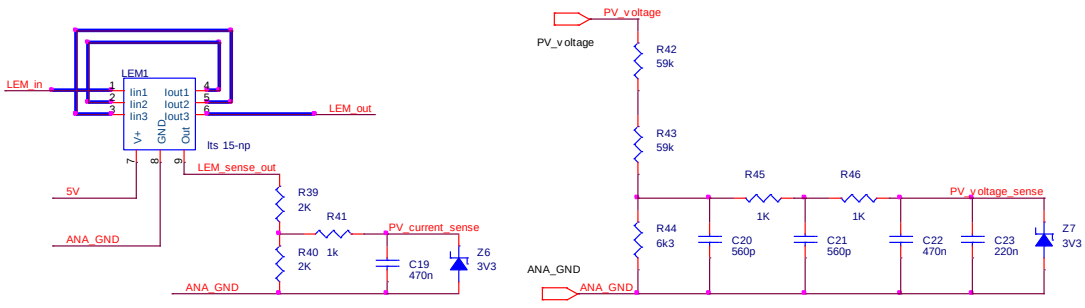

Figure 5.11 PV current and voltage sense circuits.

As in PV voltage measurement, pseudo DC-link voltage is measured via a voltage divider circuit as sown in Figure 5.12(a). Pseudo DC-link current is measured via a 270mΩ sense resistor connected in series with the pseudo DC-link and the measured signal is sent to a differential amplifier and by means of an Op-amp with a low pass filter the current signal is fed to the DSP controller as sown in Figure 5.12(b).

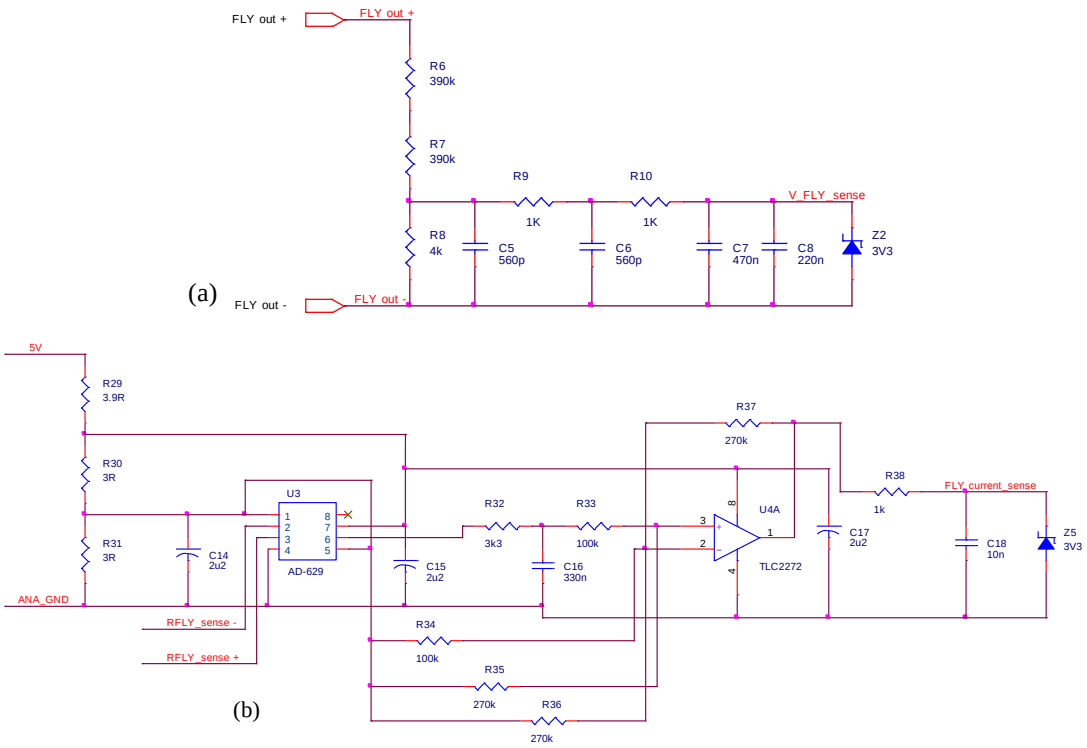

Figure 5.12 Circuit configurations of (a) pseudo DC-link voltage measurement (b) pseudo DC-link current measurement (sense resistor is not shown).

The utility grid voltage is measured via the circuit configuration shown in Figure 5.13. The input side measurements (PV-current-sense, PV-voltage-sense), pseudo DC-link measurements (V-Fly-sense, fly-current-sense), and the grid voltage measurement (grid-sense) are fed to the DSP controllers ADC channels. In order to provide further noise filtering, digital low pass filter (DLPF) is used which is necessary for accurate signal processing.

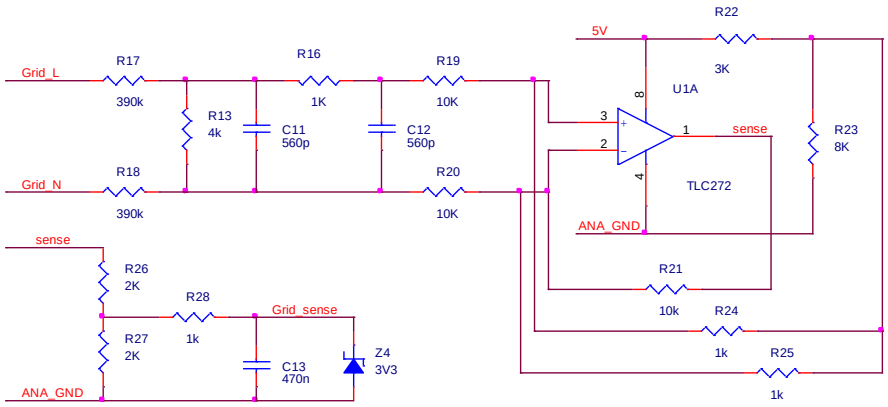

Figure 5.13 Grid voltage measurement circuit.

5.7.2 Auxiliary Supply Circuits

The required supply and reference voltages are provided by means of three LM338 adjustable linear voltage regulators as it is shown in Figure 5.14. Via these circuits required 15V and 5V supply voltages and 3V3 reference voltage are generated.

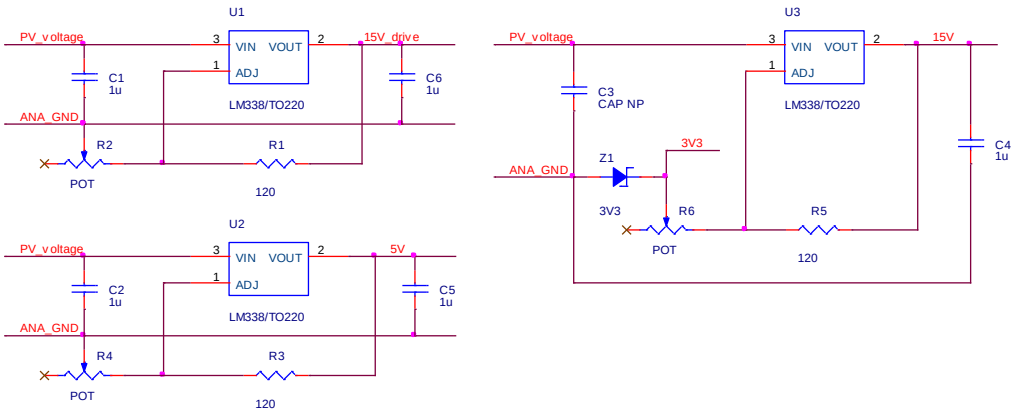

Figure 5.14 Auxiliary supply circuit configurations.

5.8 Power Loss Calculation and Semiconductor Selection

On the purpose of analyzing and comparing the efficiency characteristics of SPMI and TPIMI topologies, power loss calculations are conducted including semiconductor conduction and switching losses, HF transformer losses, snubber and auxiliary circuit losses [54][55][56]. The equations of the loss calculations are given in the following sections.

5.8.1 Semiconductor Conduction Loss Calculation

Semiconductors of the mentioned topologies are consist of primary side MOSFETs, flyback output diodes and unfolding bridge MOSFETs. The relation between the voltage and current of a MOSFET during conduction can be calculated via the equation given below as;

$$V_{DS}(i_D) = R_{DS(on)}(i_D) \times i_D \tag{5.42}$$

where, $V_{DS}(i_D)$ and $R_{DS(on)}(i_D)$ represent the drain-source voltage and on state resistance of the MOSFET at a certain drain current i_D. The value of the $R_{DS(on)}$ can be found in the datasheets as a function of i_D. Using (5.42), the instantaneous conduction loss of the MOSFET ($P_{M,Cond}$) can be expressed as;

$$P_{M,Cond}(t) = V_{DS}(t) \times i_D(t) = R_{DS(on)} \times {i_D}^2(t) \tag{5.43}$$

Via integrating $P_{M,Cond}(t)$ over the switching period, the average conduction loss of a MOSFET can be written;

$$P_{M,Cond}(t) = \frac{1}{T_{SW}} \int_0^{T_{SW}} (R_{DS(on)} \times {i_D}^2(t)).dt = R_{DS(on)} \times {I_{D,RMS}}^2 \tag{5.44}$$

where, $I_{D,RMS}$ is the RMS value of the MOSFET drain current.

The instantaneous conduction loss of a diode can be represented as;

$$P_{D,Cond}(t) = V_F \times i_F(t) + R_D \times i_F{}^2(t) \tag{5.45}$$

V_F represents the forward voltage drop across the diode, R_D is on state resistance and $i_F(t)$ is the current flowing through the diode. In order to calculate the average conduction loss of a diode, as in (5.44), $P_{D,Cond}(t)$ is integrated over one switching period as it is given in (5.46).

$$P_{D,Cond}(t) = \frac{1}{T_{SW}} \int_0^{T_{SW}} ((V_F \times i_F(t)) + (R_D \times i_F{}^2(t)).dt = V_F \times I_{F,AVG} + R_D \times I_{F,RMS}{}^2 \tag{5.46}$$

where $I_{F,AVG}$ and $I_{F,RMS}$ represents the average and RMS diode currents respectively.

The on state resistance of a diode can be obtained using i_F/V_F curve given in the datasheet. For two of the operating points where i_F and V_F are known, R_D can be calculated via (5.47).

$$R_D = \frac{\Delta i_F}{\Delta V_{Drop}} \tag{5.47}$$

5.8.2 Semiconductor Switching Loss Calculation

MOSFET and diode switching losses represent a great part of the total converter loss if the switching frequency is high. In order to calculate switching losses effectively and easily, MOSFET and diode characteristics must be well analyzed with a linear approximation. The representation of a MOSFET model with a free-wheeling diode D_F is shown in Figure 5.15 where V_{gs} is the gate drive voltage provided by the gate driver circuit, i_g is the gate current, R_g represents gate resistance. i_D and i_F are MOSFET drain current and D_F currents respectively. C_{GD}, C_{GS}, C_{DS} are the gate-drain, gate-source and drain-source parasitic capacitances respectively.

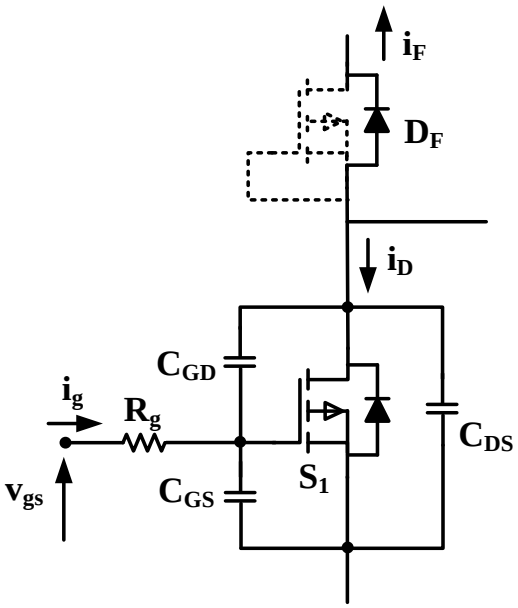

Figure 5.15 MOSFET circuit model including gate resistance R_g and parasitic capacitances (C_{GD}, C_{GS}, C_{DS}).

MOSFET switching losses contains gate drive loss, turn-on - turn-off losses and reverse recovery loss when it is connected in series with a free-wheeling diode. Gate drive loss of a MOSFET can be written as;

$$P_{M,gate} = Q_{g(on)} \times V_{gs} \times f_{SW} \tag{5.48}$$

where, $Q_{g(on)}$ represents the gate charge of the MOSFET which is found in the datasheets. In addition to the gate drive loss of a MOSFET, turn-on and turn-off losses must be calculated according to its characteristics which is shown in Figure 5.16 where i_g is the gate current, V_{drv} is the peak gate drive voltage.

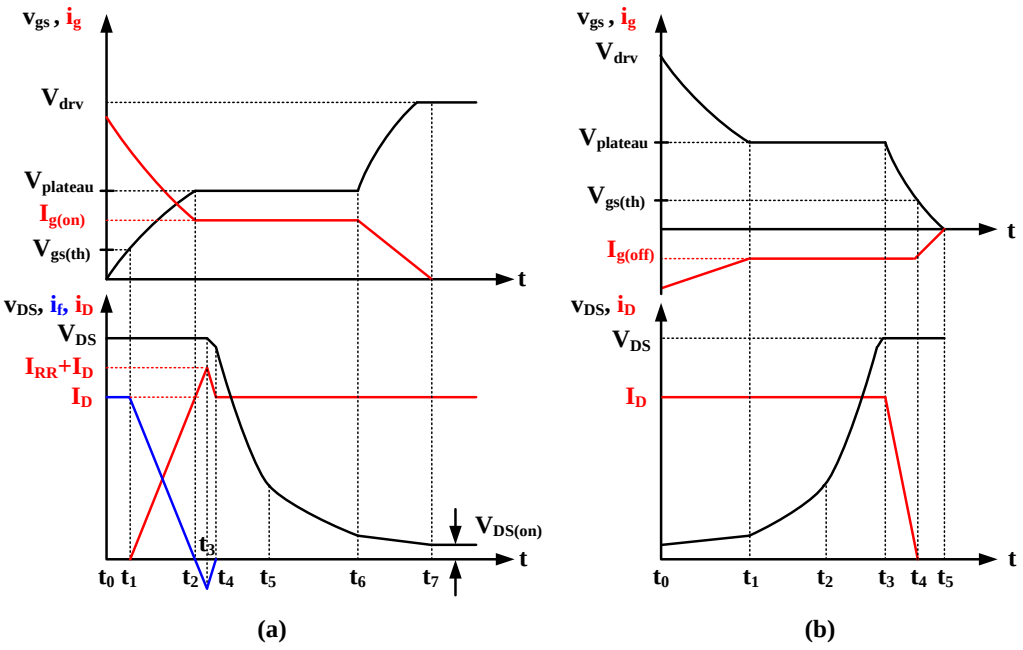

Figure 5.16 MOSFET characteristics at (a) turn-on and (b) turn-off.

In the figure, i_g is the gate current, V_{drv} is the peak gate drive voltage, $V_{gs(th)}$ is the MOSFET threshold voltage, V_{DS} is the MOSFET drain-source voltage and i_D is the drain current. I_D represents the MOSFET drain current at full load condition. i_f is the free-wheeling diode current and I_{RR} defines the reverse recovery current. As it is shown in Figure 5.16(a), during MOSFET turn-on process, when a gate drive voltage V_{drv} is applied to the MOSFET gate, the gate voltage V_{gs} starts to increase from zero as a function of R_g and MOSFET parasitic input capacitance C_{iss} which is C_{GD} + C_{GS}. When it reaches to $V_{gd(th)}$, the drain current starts to increase from zero at t_1 time instant and reaches to I_D full load current at t_2. t_0 - t_1 and the drain current rise time t_0- t_2 can be defined as in (5.49) and (5.50);

$$t_0 - t_1 = R_g \times C_{iss} \times ln\left(\frac{V_{drv}}{V_{plateau}}\right) \tag{5.49}$$

$$t_1 - t_2 = R_g \times C_{iss} \times \left(ln\left(\frac{V_{drv}}{V_{drv} - V_{plateau}} \right) - ln\left(\frac{V_{drv}}{V_{plateau}} \right) \right) \tag{5.50}$$

When the free-wheeling diode passes over conducting to the blocking state, the stored charge in the diode must be discharged and the resulting current flowing in the reverse direction which is called reverse recovery current (I_{RR}) is absorbed by the MOSFET during t_2 - t_4 time period which is also called t_{rr} as a function of reverse recovery charge Q_{rr} which can be determined from the datasheet.

When D_F is switched off (t_4), V_{DS} starts to decrease to the on state voltage $V_{DS(on)}$ which is the product of $R_{DS(on)}$ and I_D. V_{gs} is clamped to the $V_{plateau}$ voltage due to the Miller effect during that time period. Because of the non-linearity of C_{GD}, t_4 - t_6 time period is divided into two parts and linearization is achieved via (5.51), (5.52) and (5.53);

$$t_4 - t_5 = R_g \times C_{GD1} \times \left(\frac{V_{DS} - V_{DS(on)}}{V_{drv} - V_{plateau}} \right) \tag{5.51}$$

$$t_5 - t_6 = R_g \times C_{GD2} \times \left(\frac{V_{DS} - V_{DS(on)}}{V_{drv} - V_{plateau}} \right) \tag{5.52}$$

$$t_4 - t_6 = \frac{(t_4 - t_5) + (t_5 - t_6)}{2} \tag{5.53}$$

where C_{GD1} is the gate-drain capacitance when MOSFET drain-source voltage is equal to $V_{DS(on)}$ and C_{GD2} is the gate-drain capacitance when MOSFET drain-source voltage is equal to V_{DS} . The required values can be obtained via capacitance curve in the datasheet.

The turn-off process has the same steps with the turn-on, taking place on the reverse direction as it is shown in Figure 5.16(b). The turn-off starts when V_{drv} goes to zero

at t_0 instant. While the progress is the same on reverse direction, it is not going to be explained in detail. The equation for the elapsed time for V_{gs} the be equal to $V_{plateau}$ can be written as;

$$t_0 - t_1 = R_g \times C_{\text{iss}} \times \left(\frac{V_{drv}}{V_{plateau}} \right) \tag{5.54}$$

The MOSFET voltage increases from $V_{DS(on)}$ to V_{DS} during t_1 - t_3 time period which can be defined as;

$$t_1 - t_2 = R_g \times C_{GD1} \times \left(\frac{V_{DS} - V_{DS(on)}}{V_{drv} - V_{plateau}} \right) \tag{5.55}$$

$$t_2 - t_3 = R_g \times C_{GD2} \times \left(\frac{V_{DS} - V_{DS(on)}}{V_{drv} - V_{plateau}} \right) \tag{5.56}$$

$$t_1 - t_3 = \frac{(t_1 - t_2) + (t_2 - t_3)}{2} \tag{5.57}$$

Finally, the drain current fall time t3 - t4 can be expressed as;

$$t_3 - t_4 = R_g \times C_{iss} \times \left(\frac{V_{plateau}}{V_{gs(th)}} \right) \tag{5.58}$$

Since the primary side MOSFETs of the MIs mentioned in this thesis are designed to be controlled under DCM operation, the reverse recovery losses on the MOSFETs and output diodes are not explained.

According to the equations given above, the switching loss of a MOSFET during turn-on and turn-off can be represented as;

$$P_{SW(on)} = V_{DS} \times I_D \times \frac{(t_1 - t_6)}{2} \times f_{SW} \tag{5.59}$$

$$P_{SW(off)} = V_{DS} \times I_D \times \frac{(t_1 - t_4)}{2} \times f_{SW} \tag{5.60}$$

and the total switching loss P_{SW} is;

$$P_{SW} = P_{SW(off)} + P_{SW(on)} \tag{5.61}$$

The time periods (t_1 - t_6) and (t_1 - t_4) are the periods calculated from Figure 5.16(a) and 5.16(b) respectively. Full load current I_D corresponds to $I_{S1,RMS}$ when the switching loss is calculated for one half of the grid period. On the other hand, since the MOSFET voltage is limited to 150V via a snubber circuit which is mentioned before, V_{DS} is considered to be 150V during loss calculations.

5.8.3 HF Transformer Loss Calculation

Power loss of a transformer can be collected under two headings such as core loss and low frequency copper loss [56]. The core loss P_{Core} of a transformer with a ferrite core material can be calculated via (5.62) as;

$$P_{Core} = K_{Core} f_{SW}^{\lambda} \Delta B^{\beta} \tag{5.62}$$

where K_{Core} is the proportionality constant which is highly related with the sinusoidal excitation frequency f, ΔB is the peak ac flux density, λ and β are constants related with the core material which are provided by the manufacturers datasheet. The peak flux density can be defined as;

$$\Delta B = \frac{V_{PV,min} t_{on,pk}}{N_1 A_e} \tag{5.63}$$

where $V_{PV,min}$ is the minimum input voltage, $t_{on,pk}$ is the peak MOSFET ON time in μs, N_1 is the primary number of turns and A_e is the effective cross-sectional area of the core.

The total copper loss of the transformer can be given by the equation below.

$$P_{CU,tot} = P_{P,CU} + P_{S,CU} \tag{5.64}$$

where $P_{P,CU}$ and $P_{S,CU}$ are primary side and secondary side cupper losses which can be calculated as;

$$P_{P,CU} = I_{P,AVG}{}^2 \times R_{P,DC} + I_{P,RMS}{}^2 \times R_{P,AC} \tag{5.65}$$

$$P_{S,CU} = I_{S,AVG}{}^2 \times R_{S,DC} + I_{S,RMS}{}^2 \times R_{S,AC} \tag{5.66}$$

In (5.65) and (5.66), I_{AVG} and I_{RMS} represents the average and RMS currents on the primary and secondary sides. R_{DC} and R_{AC} are primary and secondary winding DC and AC resistances. The DC resistances can be expressed as;

$$R_{P,DC} = \rho \frac{N_1 \times MLT}{A_{P,ca}} \tag{5.67}$$

where ρ is the constant representing copper resistivity which is equal to 1.724×10^{-6} Ω-cm at room temperature. MLT is the mean length of one turn of the winding and $A_{P,ca}$ is the wire cross-sectional area and can be calculated as;

$$A_{P,ca} = \frac{I_{P,RMS}}{J_{RMS}} \tag{5.67}$$

where J_{RMS} is the current density (A/cm^2). While a high frequency current flows through the conductor, the skin effect reduces the effective conductor thickness. The skin depth of the copper wire at a given switching frequency (in Hz) can be calculated as;

$$\delta = \frac{7.5}{\sqrt{f_{SW}}} \tag{5.68}$$

The AC resistance of the wire can be calculated as;

$$R_{AC} = \frac{h}{\delta} R_{DC} \tag{5.69}$$

where h is the conductor thickness. By means of using Litz wires which have a thickness equal to the skin depth at a given frequency, the ratio between R_{DC} and R_{AC} can be taken as 1. According to the given statement, P_{CU} can be rewritten as;

$$P_{CU} = R_{P,DC}(I_{P,AVG}{}^2 + I_{P,RMS}{}^2) + R_{S,DC}(I_{S,AVG}{}^2 + I_{S,RMS}{}^2) \tag{5.70}$$

5.8.4 Auxiliary Supply and Snubber Losses

In addition to the semiconductor and transformer losses, the power consumption of the auxiliary power supply and the snubber losses are added to the total loss calculation.

Auxiliary power supply losses are assumed to be 2W and 3W for SPMI and TPIMI topologies respectively. On the other hand, snubber losses are already calculated as 1.84W and 0.94x2W for SPMI and TPIMI in Section 5.4.

5.8.5 SPMI Semiconductor Selection and Loss Calculation

The semiconductors used in SPMI circuit are selected according to the current and voltage ratings given in Table 5.4.

Table 5.4 SPMI current and voltage ratings

Parameter	**magnitude**
Primary MOSFET peak current, $I_{S1,pk}$ (A)	48.5
Primary MOSFET RMS current, $I_{S1,rms}$ (A)	14.8
Primary MOSFET avg. current, $I_{S1,avg}$ (A)	8
Maximum primary MOSFET voltage, $V_{M,MAX}$ (V)	150
Maximum diode voltage, $V_{D,MAX}$(V)	495
Diode peak current, $I_{D,pk}$ (A)	7.66
Diode RMS current, $I_{D,rms}$ (A)	2.34
Diode avg. current, $I_{D,avg}$ (A)	1.26
Maximum UB MOSFET voltage $V_{UB,MAX}$ (V)	620
UB MOSFET peak current, $I_{UB,pk}$ (A)	1.29
UB MOSFET RMS current, $I_{UB,rms}$ (A)	0.91

The parameters of the semiconductors are selected according to the specified current and voltage ratings given below. The conduction and switching loss calculations are conducted temper to the parameters of the semiconductors given in the manufacturer datasheets given in Table 5.5.

Table 5.5 Parameters of the semiconductors given in the manufacturer datasheets

Primary MOSFET (IRFB4127PBF)		**UB MOSFETs (STP21N65M5)**	**Output diode (C3D10065A)**	
V_{DS} (V)	200	650	$V_{rrm\ (max)}$ (V)	650
$I_{D(MAX)}$ (A)	76	17	$I_{f\ (AVG)}$ (A)	10
$R_{DS(on)}$ (mΩ)	17	179	R_D (mΩ)	35
$V_{gs(th)}$ (V)	5	5	$V_{F\ (max)}$ (V)	1.8
C_{iss} (pF)	5380	1950	V_{RSM} (V)	650
C_{oss} (pF)	410	46	V_{DC} (V)	650
C_{rss} (pF)	86	3	I_{FRM} (A)	44
$t_{d(on)}$ (ns)	17	37		
t_r (ns)	18	10		
$t_{d(off)}$ (ns)	56	24		
t_f (ns)	22	12		
$Q_{g(on)}$ (nC)	100	50		

According to the parameters given above and using (5.42) - (5.61), the conduction and switching losses are calculated as given in Table 5.6.

Table 5.6 SPMI semiconductor conduction and switching losses

Power Loss	**magnitude**
Primary MOSFET conduction loss (W)	11
Primary MOSFET switching loss (W)	13.8
Diode conduction loss (W)	2.7
UB MOSFETs conduction loss (W)	0.16x4
UB MOSFETs switching loss (W)	-

Since the UB MOSFETs are turned on and off at zero crossings of the utility grid voltage, the switching losses are ignored. In addition, while primary MOSFET current turns on with zero current, turn-on loss of the primary MOSFET is also ignored. Instead, the loss taking place because of the parasitic capacitance and the

turn on voltage, is considered during the calculation. Transformer core and copper losses are calculated according to the parameters given in Table 5.7.

Table 5.7 SPMI HF transformer parameters

parameter	**magnitude**	**parameter**	**magnitude**
K_{Core}	0.0573	$R_{P,DC}$ $(m\Omega)$	3
α, β	1.66, 2.68	$R_{P,AC}$ $(m\Omega)$	12
ΔB (T)	0.17	$R_{S,DC}$ $(m\Omega)$	28
$A_{P,ca}$ (cm^2)	0.037	$R_{S,AC}$ $(m\Omega)$	140
MLT (cm)	6.5		

According to the parameters given in the table, core loss and copper loss are calculated as 2.5W and 3.63W respectively. According to the results including, semiconductor switching and conduction losses, auxiliary power supply loss, snubber loss, transformer core and copper losses, the total power loss and efficiency of the SPMI is calculated and listed in Table 5.8.

Table 5.8 SPMI loss and efficiency calculation

Parameter	**magnitude**
SPMI rated power (W)	200
Semiconductor total conduction loss (W)	14.34
Semiconductor total switching loss (W)	13.8
Transformer core loss (W)	2.5
Transformer copper loss (W)	3.63
Auxiliary circuit loss (W)	2
Snubber circuit loss (W)	1.84
Total loss of power (W)	38.11
Calculated efficiency (%)	81

5.8.6 TPIMI Semiconductor Selection and Loss Calculation

The semiconductors used in TPIMI circuit are selected according to the current and voltage ratings given in Table 5.9.

Table 5.9 TPIMI current and voltage ratings

Parameter	**magnitude**
Primary MOSFET peak current, $I_{S1,pk}$ (A)	25.26
Primary MOSFET RMS current, $I_{S1,rms}$ (A)	7.44
Primary MOSFET avg. current, $I_{S1,avg}$ (A)	4
Maximum primary MOSFET voltage, $V_{M,MAX}$ (V)	150
Maximum diode voltage, $V_{D,MAX}$(V)	460
Diode peak current, $I_{D,pk}$ (A)	4.21
Diode RMS current, $I_{D,rms}$ (A)	1.24
Diode avg. current, $I_{D,avg}$ (A)	0.67
Maximum UB MOSFET voltage $V_{UB,MAX}$ (V)	620
UB MOSFET peak current, $I_{UB,pk}$ (A)	1.29
UB MOSFET RMS current, $I_{UB,rms}$ (A)	0.91

The parameters of the semiconductors are selected according to the specified current and voltage ratings given below. The conduction and switching loss calculations are conducted temper to the parameters of the same semiconductors given in the manufacturer datasheets given in Table 5.5. According to the parameters given above and using (5.42) - (5.61), the conduction and switching losses are calculated as given in Table 5.10.

Table 5.10 Semiconductor conduction and switching losses of TPIMI

Power Loss	**magnitude**
Primary MOSFET conduction loss (W)	3.3x2
Primary MOSFET switching loss (W)	3.7x2
Diode conduction loss (W)	0.7x2
UB MOSFETs conduction loss (W)	0.16x4
UB MOSFETs switching loss (W)	-

Since the UB MOSFETs are turned on and off at zero crossings of the utility grid voltage, the switching losses are ignored. In addition, while primary MOSFET current turns on with zero current, turn-on loss of the primary MOSFET is also ignored. Instead, the loss taking place because of the parasitic capacitance and the turn on voltage, is considered during the calculation. Transformer core and copper losses are calculated according to the parameters given in Table 5.11.

Table 5.11 TPIMI HF transformer parameters

parameter	**magnitude**	**parameter**	**magnitude**
K_{Core}	0.0573	$R_{P,DC}$ *(mΩ)*	2
α, β	1.66, 2.68	$R_{P,AC}$ *(mΩ)*	10
ΔB *(T)*	0.19	$R_{S,DC}$ *(mΩ)*	50
$A_{P,ca}$ *(cm^2)*	0.018	$R_{S,AC}$ *(mΩ)*	250
MLT (cm)	5		

According to the parameters given in the table, core loss and copper loss are calculated as 3.35W and 1W respectively. According to the results including, semiconductor switching and conduction losses, auxiliary power supply loss, snubber loss, transformer core and copper losses, the total power loss and efficiency of the TPIMI is calculated and listed in Table 5.12.

Table 5.12 TPIMI loss and efficiency calculation

Parameter	**magnitude**
SPMI rated power (W)	200
Semiconductor total conduction loss (W)	8.64
Semiconductor total switching loss (W)	7.4
Transformer core loss (W)	6.7
Transformer copper loss (W)	2
Auxiliary circuit loss (W)	3
Snubber circuit loss (W)	1.88
Total loss of power (W)	29.62
Calculated efficiency (%)	85.2

As it is seen from the calculations, while the efficiency of the SPMI is calculated as 81, the efficiency of the TPIMI is found to be 85.2 providing 4.2% improvement on the efficiency. The calculated results will be compared with the experimental results and the convenience of the results will be verified.

5.9 Summary

In this chapter, the calculations for decoupling capacitor sizing, transformer design, snubber circuit design, unfolding bridge and LCL filter design are listed and the design parameters of both single-phase and two-phase interleaved flyback-based MIs are calculated. At the end of the chapter, the power loss calculations including, switching, conduction, transformer core and copper losses are conducted and the efficiencies of 81% and 85.2% for single-phase and two-phase interleaved MI designs are calculated respectively.

CHAPTER 6

THE PERFORMANCE ANALYSIS OF SINGLE-PHASE AND INTERLEAVED FLYBACK-BASED MICRO-INVERTERS VIA COMPUTER SIMULATIONS

In this chapter, simulation studies of 200W single-phase and 200W two-phase interleaved flyback-based micro-inverters are realized and the compatibility of the results and expected results from chapter 5 is examined. Furthermore, the simulation model of the PV panel is realized and the compatibility with the real panel is verified. In addition, device and controller parameters are modeled in accordance with the implemented circuit models.

Simulation results such as steady state measurements, input and output characteristics, dynamic responses are listed, besides performance analysis of two micro-inverters are realized. Finally, the performance comparison of two topologies are carried out and the compatibility with the calculated results is verified. While conducting the simulation study of the topologies, Simplorer Simulation Center 7.0, simulation program is used [57].

6.1 Modeled PV Panel Characteristics

The PV panel is modeled and power characteristics are simulated according to the parameters of the implemented PV panel as shown in Figure 6.1.

As it is seen in the figure, the maximum power of the PV panel is 200W. In addition, MPP current and voltage are measured to be 7A and 28.8V respectively which is accordant with the PV panel used during the experiments. After the modeling of the panel is accomplished, the simulations of the SPMI and TPIMI topologies are realized.

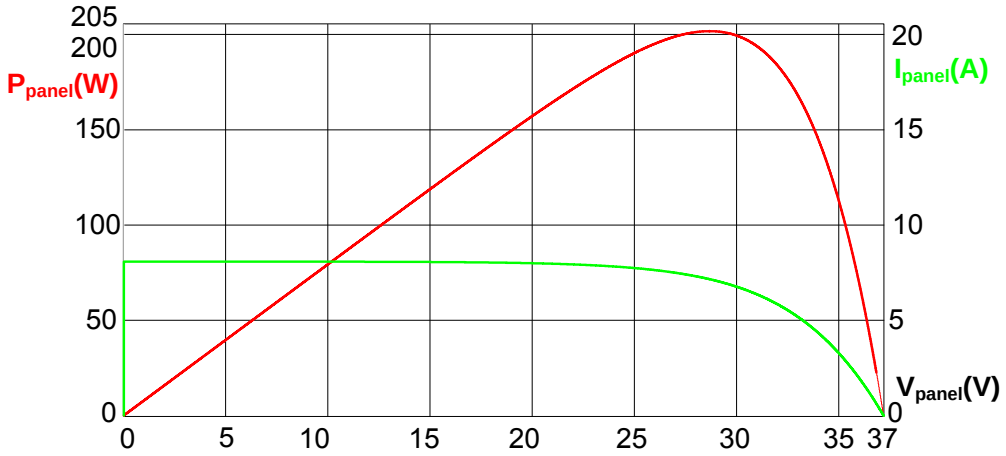

Figure 6.1 Modeled PV Panel P-V (red) and I-V (green) characteristics.

6.2 Simulation Results of SPMI

The circuit parameters are stated in accordance with the calculated values in chapter 5 as it is listed in Table 6.1. Moreover, the circuit model of the simulated SPMI topology is shown in Figure 6.2.

$STEP_1$ step function block is used in order to simulate the solar irradiance alteration. Input current is measured via R_{sense} resistor which models the current sensor of the implemented circuit. Moreover, the input voltage is measured and filtered via an RC filter. C_{oss} and C_2 model the parasitic capacitances of the semiconductors. $EQUBL_2$ and GS_2 equation and s-function blocks achieve the MPPT operation as well as generate the amplitude value of the reference current as it is mentioned before. Furthermore, $EQUBL_1$ and GS_1 blocks conduct the sinusoidal current reference generation and grid synchronization. $SINE_1$ and $TRIANG_1$ blocks provide unity sinusoidal waveform in phase with the grid and the carrier signal with 170kHz respectively. Finally, PWM_1 and PWM_2 blocks provide gate drive signals to the UB MOSFETs.

Table 6.1 SPMI simulation parameters

HF transformer		***Decoupling circuit***	
Magnetizing inductance (μH)	*2*	Decoupling capacitor, (mF)	*15.4*
Pr. leakage inductance (nH)	*60*	***Pseudo DC-link***	
Sec. leakage inductance (nH)	*380*	Pseudo DC-link capacitor,(nF)	*400*
Turns ratio, n (N_1/N_2)	*0.158*	***LCL filter***	
Pr. winding resistance (mΩ)	*15*	Inverter side inductance (μH)	*270*
Sec. winding resistance (mΩ)	*75*	Grid side inductance, (μH)	*180*
Snubber circuit		Filter capacitance, (nF)	*440*
Snubber resistance (kΩ)	*9.1*	Damping resistance, (Ω)	*5*
Snubber capacitance (nF)	*47*	***Utility grid***	
Primary MOSFET		Grid RMS voltage, (V)	*220*
On state resistance (mΩ)	*17*	Grid frequency, (Hz)	*50*
Output capacitance (pF)	*410*	Internal resistance, (mΩ)	*20*
		Equivalent inductance (μH)	*50*

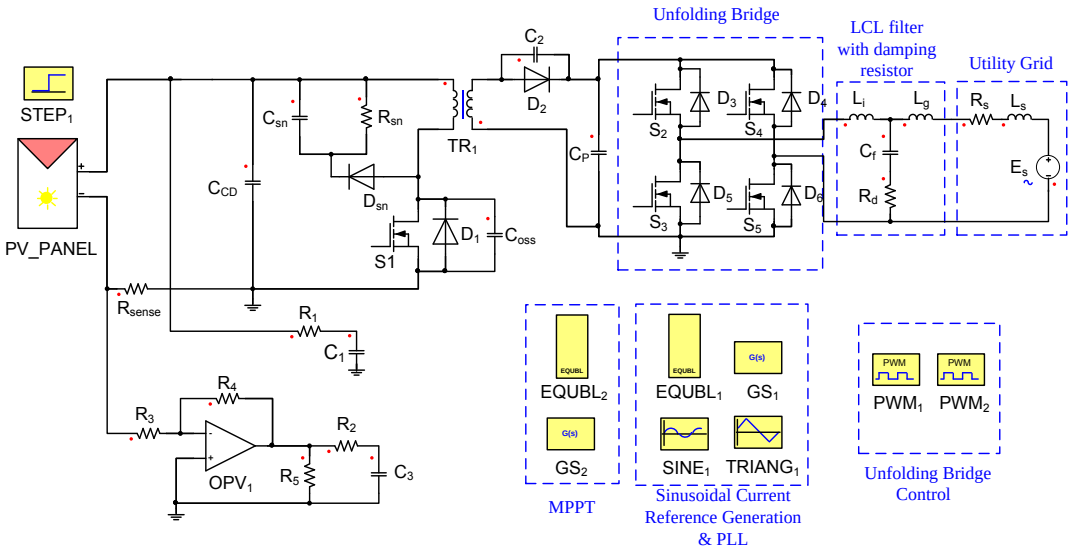

Figure 6.2 The circuit model of the simulated SPMI topology.

6.2.1 Steady State Measurements

The steady state measurements are listed in Table 6.2 at rated power. The efficiency of the SPMI is measured to be 80.5% which is nearly the same with calculated one.

Table 6.2 SPMI steady state measurements at rated power

Input power P_{IN} (W)	200
Grid power P_{GRID} (W)	161
Power loss P_{LOSS} (W)	39
Efficiency η (%)	80.5
Power factor (P.F.)	0.968
Grid current THD_I (%)	4.52
Peak grid current (A)	1.03

Besides, THD of the output current is measured to be 4.52% which is under the 5% limit stated in the IEC standards [24]. On the other hand PF performance is also higher than 0.95 which can be stated as good.

6.2.2 Input Characteristics

In chapter 5, the decoupling capacitors are calculated as 15.4mF in order to limit the input voltage ripple under 8.5%. In accordance with the calculated results, the measured voltage ripple is shown in Figure 6.3 where it is equal to 1.4V at 200W which corresponds to 4.86%.

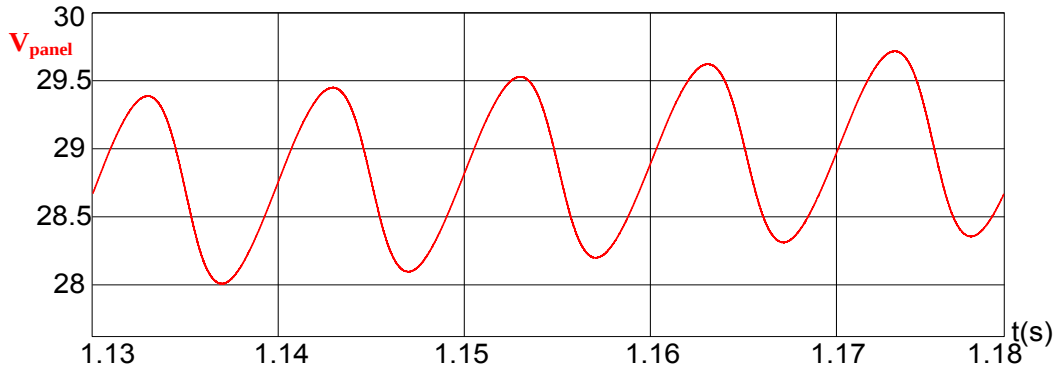

Figure 6.3 Input voltage ripple (V).

6.2.3 Switching Characteristics

Since the output of the MI has a sinusoidal waveform, the HF MOSFET voltage and current has a rectified sinusoidal form throughout two grid period as it is shown in Figure 6.4.

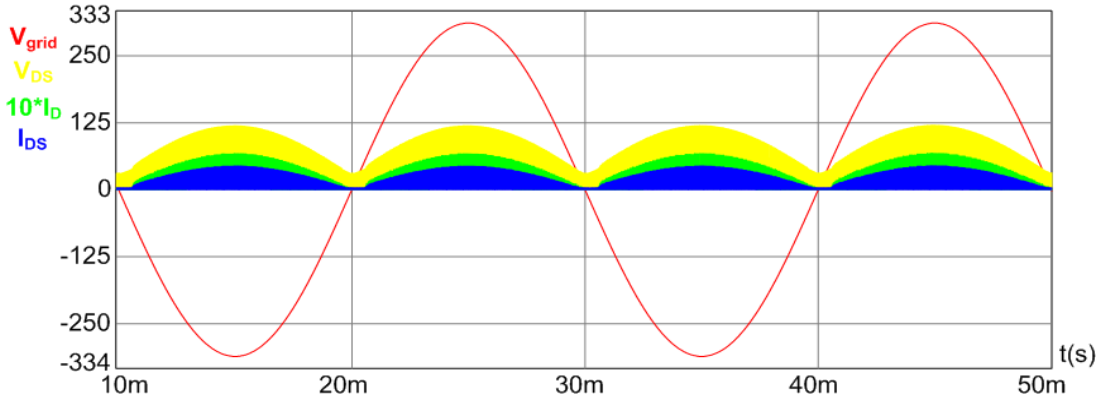

Figure 6.4 Grid voltage(red), MOSFET voltage(yellow) and current(blue), diode current (green)(with multiplication constant of ten).

As it is seen from the figure, MOSFET voltage V_{DS} is under the maximum voltage specified in chapter 5 which is 150V limited via the designed snubber circuit. MOSFET voltage, current and output diode current throughout two switching cycle are shown in Figure 6.5.

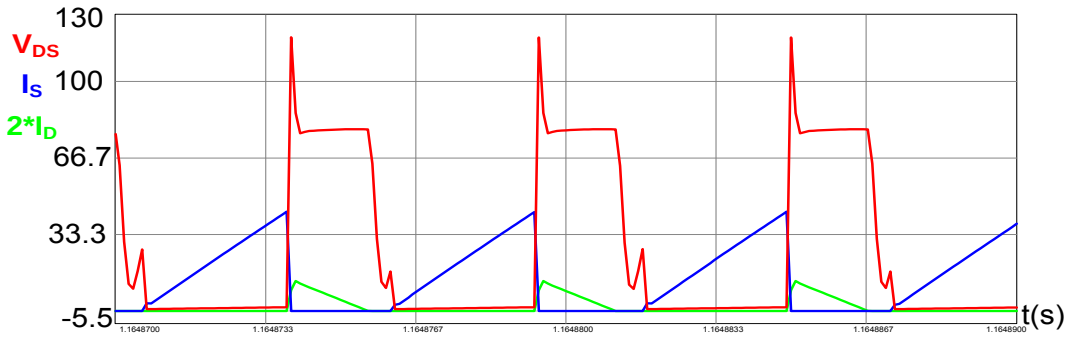

Figure 6.5 MOSFET voltage(red), MOSFET current(blue) and diode current (green)(multiplied by two).

The waveforms given in the figure above represent the peak voltage and current values taking place when $\omega_0 t$ is equal to $\pi/2$. As it is seen from the figure, DCM operation is conducted when the maximum PV power is transferred to the grid. Moreover, The resonation is observed on the MOSFET voltage V_{DS}, because of the magnetizing inductance of the transformer and parasitic capacitance of the MOSFET.

6.2.4 Pseudo DC-link and Output Characteristics

Rectified sinusoidal UB MOSFET (pseudo DC-link) currents and voltage can be seen in Figure 6.6. By means of an UB following the flyback converter, pseudo DC-link waveforms are converted into sinusoidal form.

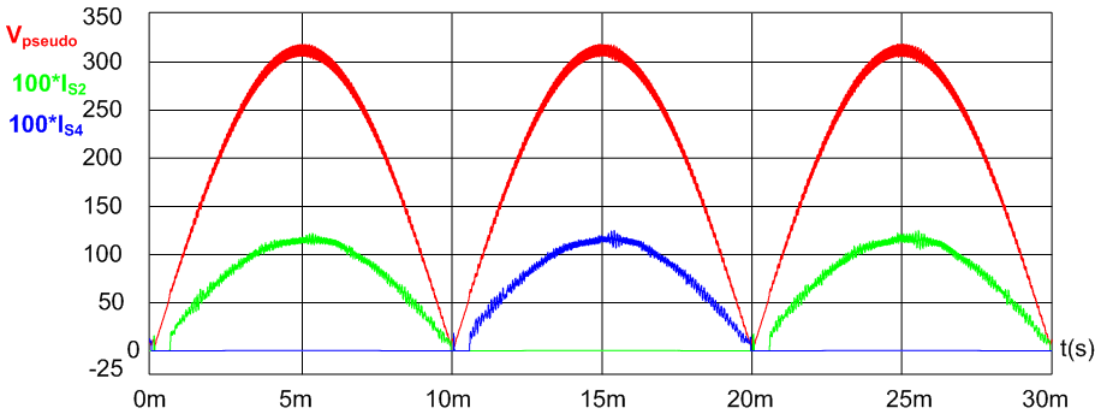

Figure 6.6 Rectified sinusoidal pseudo DC-link voltage (red), UB MOSFET currents I_{S2} and I_{S4} (green - blue) (multiplied by 100).

The pseudo DC-link ripple voltage is measured to be 12V. Moreover, pseudo DC-link voltage and gate signals of Unfolding MOSFETs operating at grid frequency can be seen in Figure 6.7.

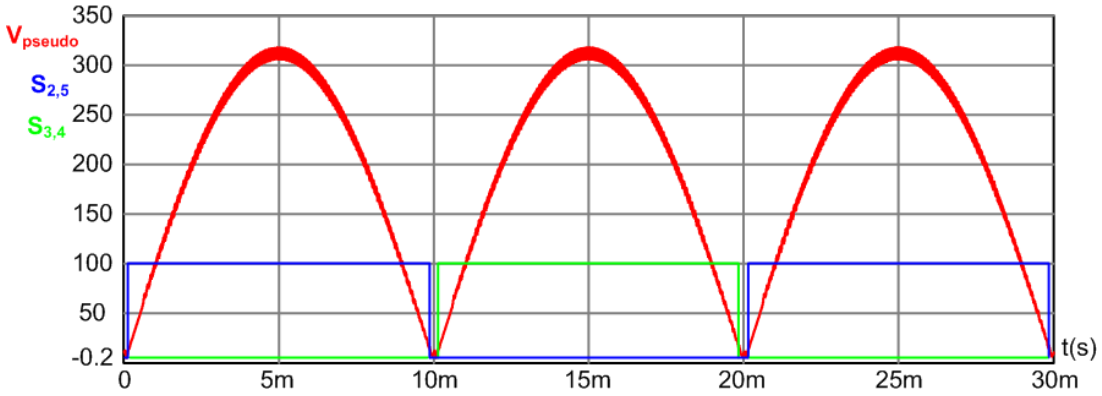

Figure 6.7 Pseudo DC-link voltage (red) and UB MOSFET gate drive signals (blue - green) (multiplied by 100).

Unfolded sinusoidal output current and grid voltage are shown throughout two grid period in Figure 6.8. In order to observe the output current effectively, it is multiplied by a constant of 100.

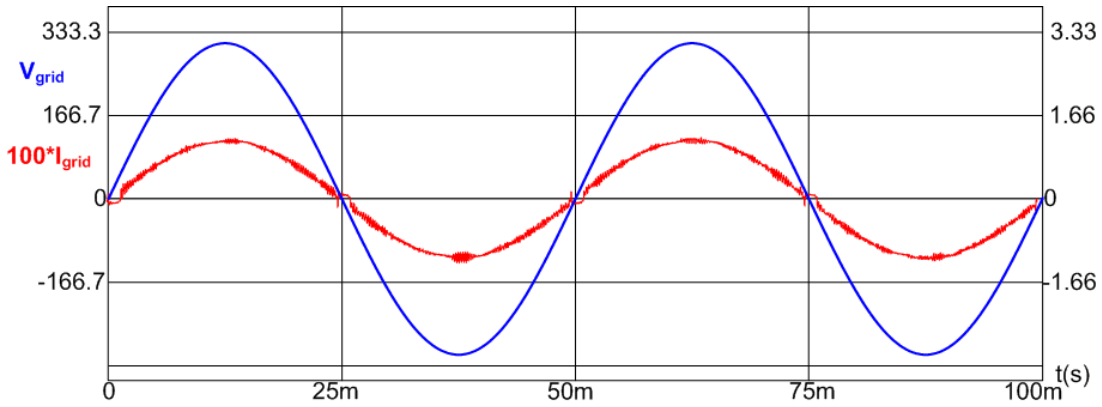

Figure 6.8 Grid voltage (blue) and output current (red) (multiplied by 100).

The grid connection is realized by means of an LCL filter with a damping resistor modeled according to the calculated filter parameters. In addition, an output current THD_I of 4.52% is achieved which is under 5% limit stated in the standards.

6.2.5 Dynamic Response at Start-Up and Under Rapidly Changing Conditions

The energy transfer from PV panel to the utility grid starts from open circuit condition. MPPT algorithm gives rise to an increase on the current drawn from the panel as long as the maximum power is reached. In Figure 6.9, PV panel voltage and current are seen during the MPPT operation. As it is shown in the figure, while the voltage reduces to MPP voltage, the current increases until the MPP current is reached. The green line represents the MPP voltage of the panel. In Figure 6.10, it is shown that, the actual PV panel power reaches to MPP, which is 200W in this case, due to the MPPT operation in 1.08s.

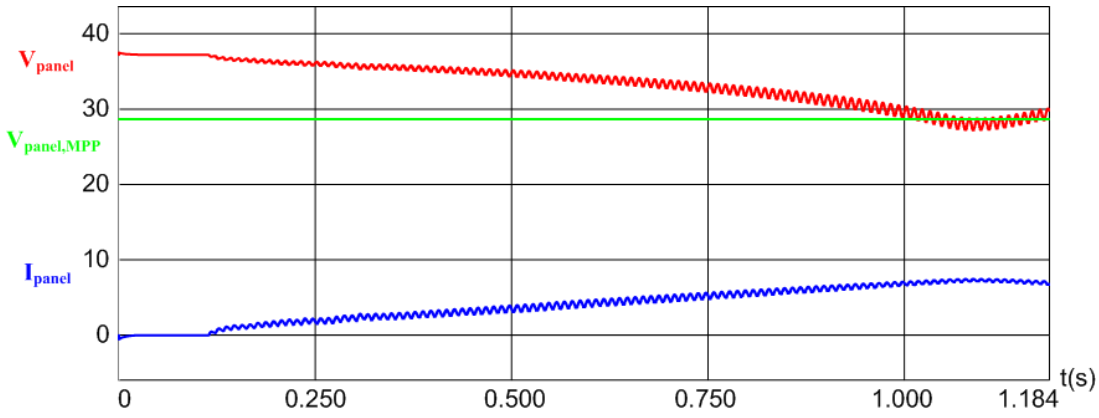

Figure 6.9 Panel voltage (red), panel MPP voltage (green) and current (blue).

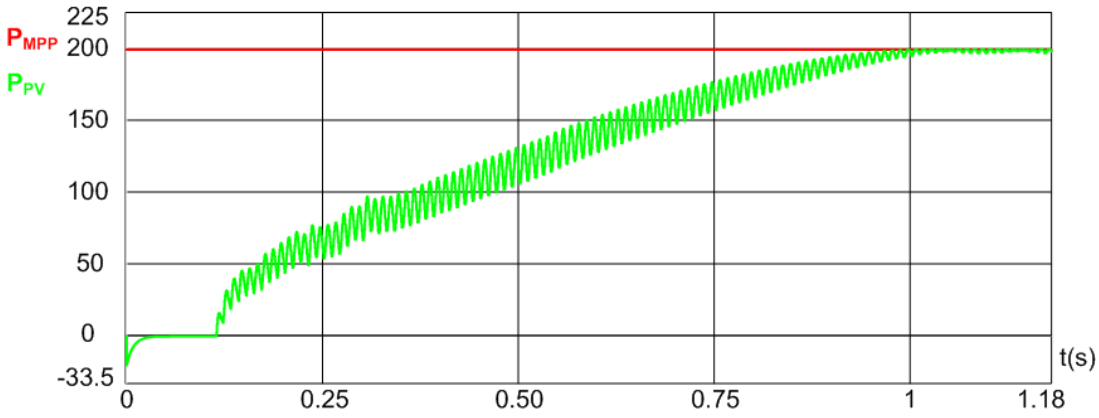

Figure 6.10 PV panel actual power (green), MPP (red).

In addition to the characteristics at start-up, the performance of the MPPT operation under rapidly changing conditions is also measured. For a PV system installed on the roof of a residence, there is a possibility of a sudden shading caused by an object in addition to the shading conditions taking place because of the atmospheric conditions which are slower. The MPPT algorithm must has the ability to track the MPP under rapidly changing conditions.

In Figure 6.11, system starts from open circuit condition and reaches to the maximum power point in 1.08 seconds. 1.5 seconds after start up a sudden power reduction of 40W on input power is realized simulating a sudden shading condition and it is observed that the MPPT algorithm manipulates the actual PV panel power to be equal to the new maximum power operating point where the elapsed time to reach the new MPP is measured to be 0.575 seconds.

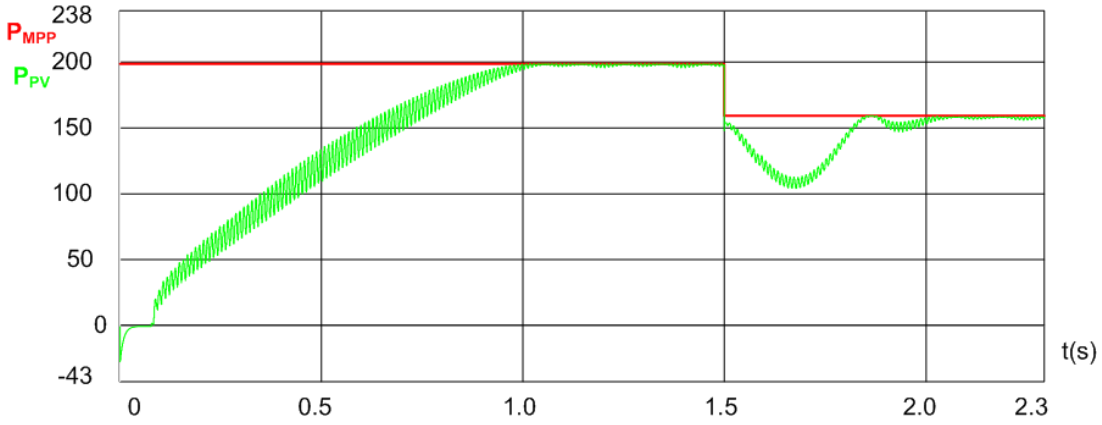

Figure 6.11 PV panel actual power (green), MPP (red).

By means of the simulation results of the SPMI, the compatibility of the calculated and simulated results is verified. Since the calculated efficiency was 81% for SPMI topology, the modeled SPMI has an efficiency of 80.5% which is very close to the calculated one. On the other hand, the THD_I of the SPMI is simulated to be under the specified limits. Moreover, since the PF of the SPMI is measured to be greater

than 0.9 and the elapsed time to reach the MPP is measured to be 1.08s, PF performance and the performance of the MPPT algorithm can be stated as good.

6.3 Simulation Results of TPIMI

The circuit parameters are stated in accordance with the calculated values as it is listed in Table 6.3 and the circuit model of the simulated TPIMI is shown in Figure 6.12.

Table 6.3 TPIMI simulation parameters

HF transformer		***Decoupling circuit***	
Magnetizing inductance (μH)	*3.93*	Decoupling capacitor, (mF)	*15.4*
Pr. leakage inductance (nH)	*118*	***Pseudo DC-link***	
Sec. leakage inductance (nH)	*708*	Pseudo DC-link capacitor,(nF)	*400*
Turns ratio, n (N_1/N_2)	*0.167*	***LCL filter***	
Pr. winding resistance (mΩ)	*20*	Inverter side inductance (μH)	*100*
Sec. winding resistance (mΩ)	*120*	Grid side inductance, (μH)	*100*
Snubber circuit		Filter capacitance, (nF)	*220*
Snubber resistance (kΩ)	*18*	Damping resistance, (Ω)	*5*
Snubber capacitance (nF)	*22*	***Utility grid***	
Primary MOSFET		Grid RMS voltage, (V)	*220*
On state resistance (mΩ)	*17*	Grid frequency, (Hz)	*50*
Output capacitance (pF)	*410*	Internal resistance, (mΩ)	*20*
		Equivalent inductance (μH)	*50*

As it is the case with SPMI simulation model, $STEP_1$ step function block is used in order to simulate the solar irradiance alteration in TPIMI model. R_{sense} resistor and RC filter are used in order to measure input current and voltage respectively. Moreover, C_{oss} and C_2 capacitances are placed in order to model the parasitic capacitances of the semiconductors. The equation and function blocks such as $EQUBL_1$, $EQUBL_2$, GS_1, GS_2, PWM_1 and PWM_2 are used for the same purpose as in SPMI model. In contrast with the SPMI model, there are two function blocks generating triangular signals such as $TRIANG_1$ and $TRIANG_2$ providing 180° phase shifted carrier signals with 170kHz.

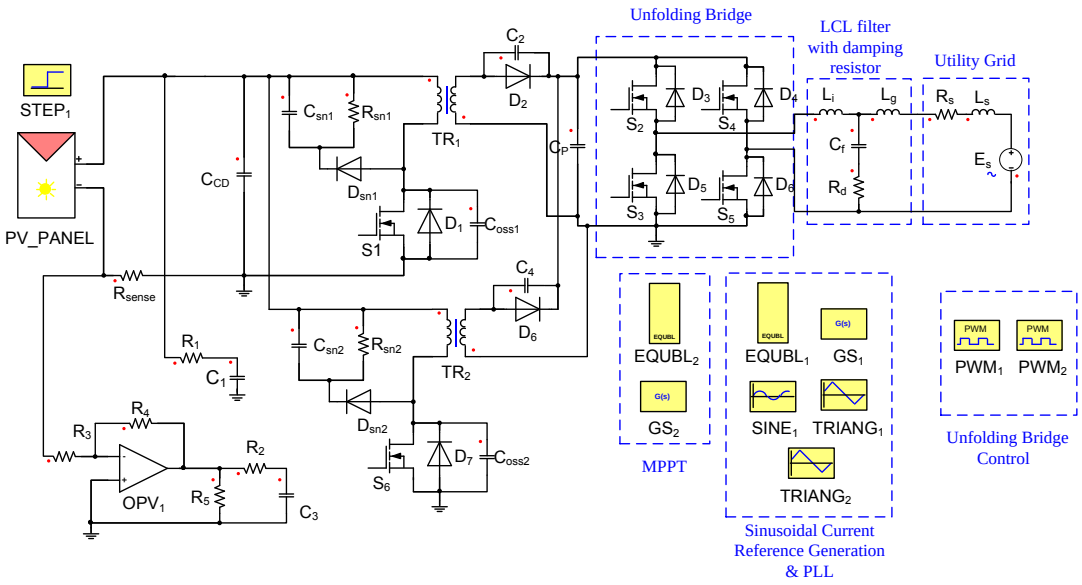

Figure 6.12 The circuit model of the simulated TPIMI topology.

6.3.1 Steady State Measurements

In Table 6.4, the steady state measurements of the TPIMI are listed at rated power. The efficiency of the TPIMI is measured to be 84.2% which is very close to the calculated one in chapter 5.

Table 6.4 TPIMI steady state measurements at rated power

Input power P_{IN} (W)	200
Grid power P_{GRID} (W)	168.4
Power loss P_{LOSS} (W)	31.6
Efficiency η (%)	84.2
Power factor (PF)	0.97
Grid current THD_I (%)	3.61
Peak grid current (A)	1.1

In addition, THD of the output current is measured to be 3.61% which is under the 5% limit stated in the IEC standards as well as the THD performance of SPMI. Moreover, PF performance is also higher than 0.9 and can be stated as a better performance than SPMI as well.

6.3.2 Input Characteristics

The decoupling capacitors are modeled as 15.4mF in order to limit the input voltage ripple under 8.5% as is the case for SPMI. The measured input voltage ripple is 1.2V and shown in Figure 6.13 which corresponds to 4.16%.

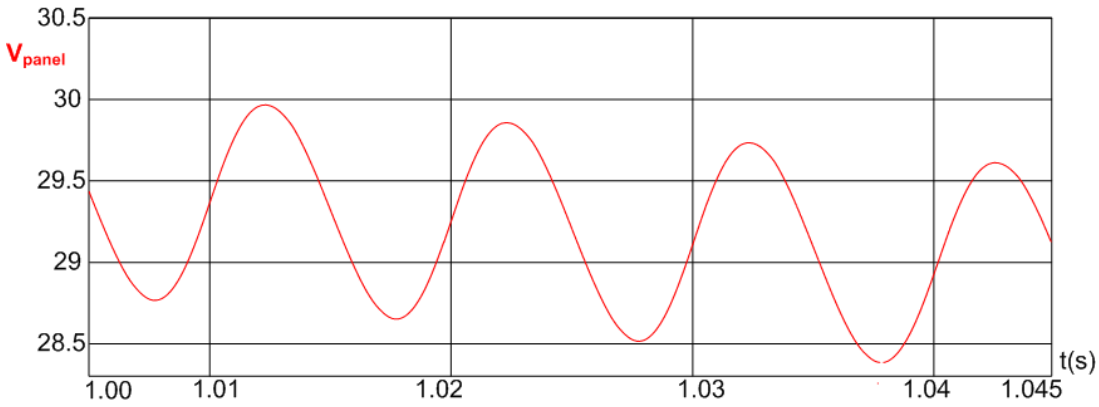

Figure 6.13 Input voltage ripple (V).

6.3.3 Switching Characteristics

The HF MOSFET voltage, current and diode current of one phase of TPIMI and grid voltage is shown in Figure 6.14.

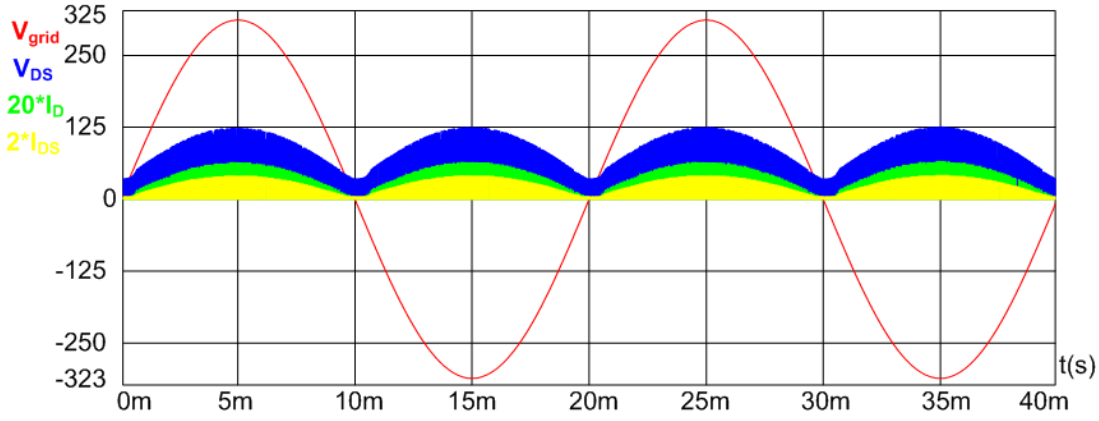

Figure 6.14 Grid voltage (red), MOSFET voltage(blue) and current(yellow)(multiplied with 2) and diode current (green)(multiplied with 20).

As it is seen from the figure, MOSFET voltage V_{DS} is under the 150V maximum voltage limit specified in chapter 5. Moreover, MOSFET voltage current and flyback diode current throughout three switching period is shown in Figure 6.15.

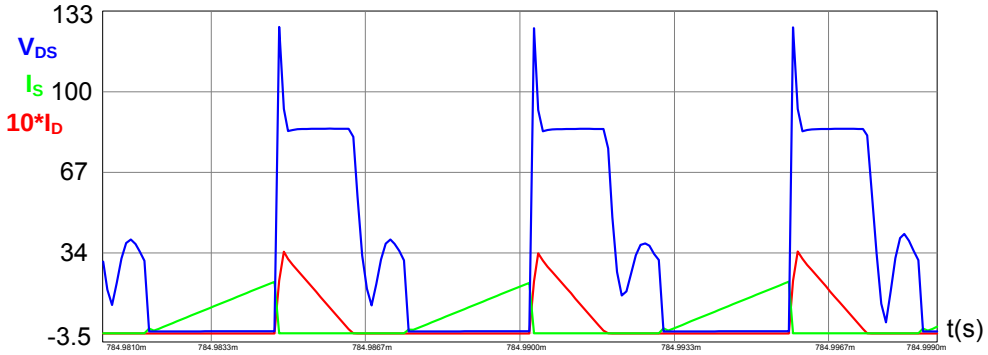

Figure 6.15 MOSFET voltage(blue), MOSFET current(green) and diode current (red) (multiplied with ten).

The waveforms are measured when $\omega_0 t$ is equal to $\pi/2$ for only one phase. Besides, as in SPMI, it is seen that DCM operation is conducted when the maximum PV power is transferred to the grid. In addition, the resonation is observed on the MOSFET voltage V_{DS}, via the magnetizing inductance and parasitic capacitance of the MOSFET. The interleaved operation is shown in Figure 6.16 where a 180° phase shift takes place between phase 1 and phase 2 MOSFET currents I_{S1} and I_{S2}.

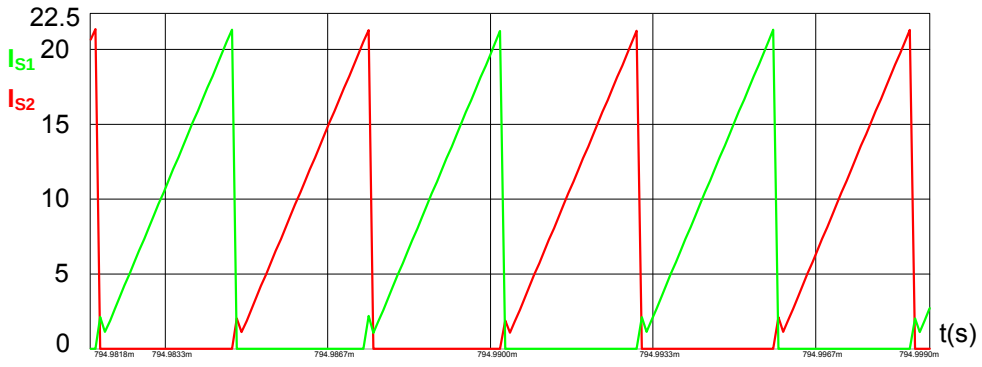

Figure 6.16 Phase 1 and 2 MOSFET currents I_{S1}(green) and I_{S2} (red).

6.3.4 Pseudo DC-link and Output Characteristics

Rectified sinusoidal pseudo DC-link currents and voltage can be seen in Figure 6.17. The same UB structure with the SPMI is modeled in the simulation.

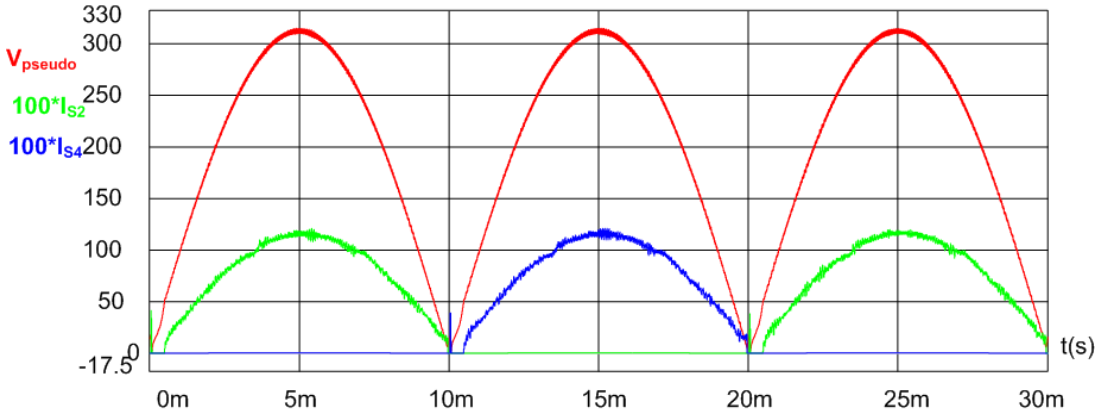

Figure 6.17 Rectified sinusoidal pseudo DC-link voltage (red), UB MOSFET currents I_{S2} and I_{S4} (green - blue) (multiplied by 100).

The pseudo DC-link ripple voltage is measured to be 8V which is lower than the voltage ripple of SPMI topology. Pseudo DC-link voltage and gate signals of unfolding bridge MOSFETs operating at grid frequency can be seen in Figure 6.18.

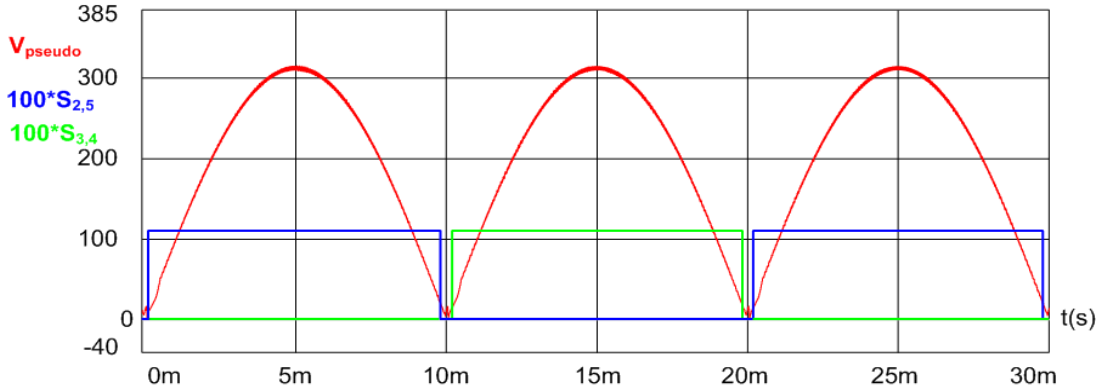

Figure 6.18 Pseudo DC-link voltage (red) and UB MOSFET gate drive signals (blue - green) (multiplied by 100).

Output current and voltage are shown throughout two grid period in Figure 6.19 for TPIMI. The LCL filter with a damping resistor modeled according to the calculated filter parameters. Furthermore, an output current THD_I of 3.61% is achieved which is under 5% limit stated in the standards as well as THD_I of the SPMI.

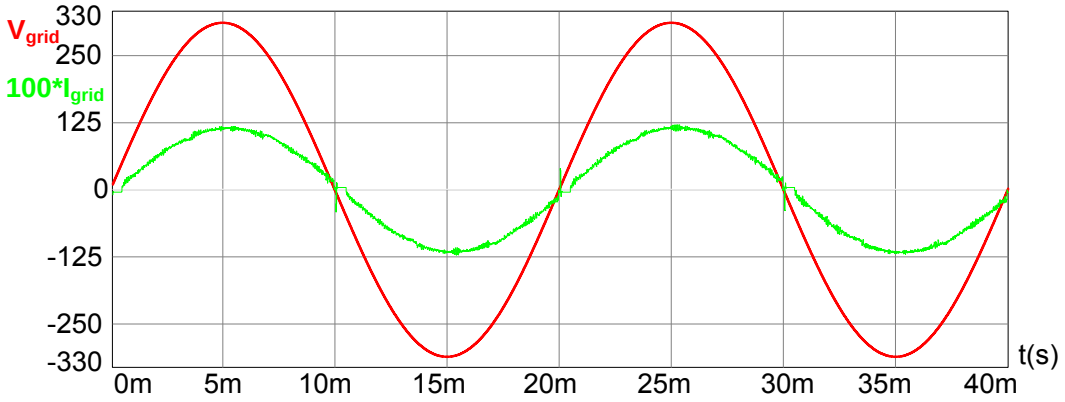

Figure 6.19 Grid voltage (red) and output current (green, multiplied by 100).

6.2.5 Dynamic Response at Start-Up and Under Rapidly Changing Conditions

As in SPMI, the MPPT algorithm starts searching for the MPP of the PV panel from the open circuit condition. The panel voltage goes to V_{MPP} from V_{OC} in 1.04 seconds, in addition, the current goes to I_{MPP} from zero as shown in Figure 6.20.

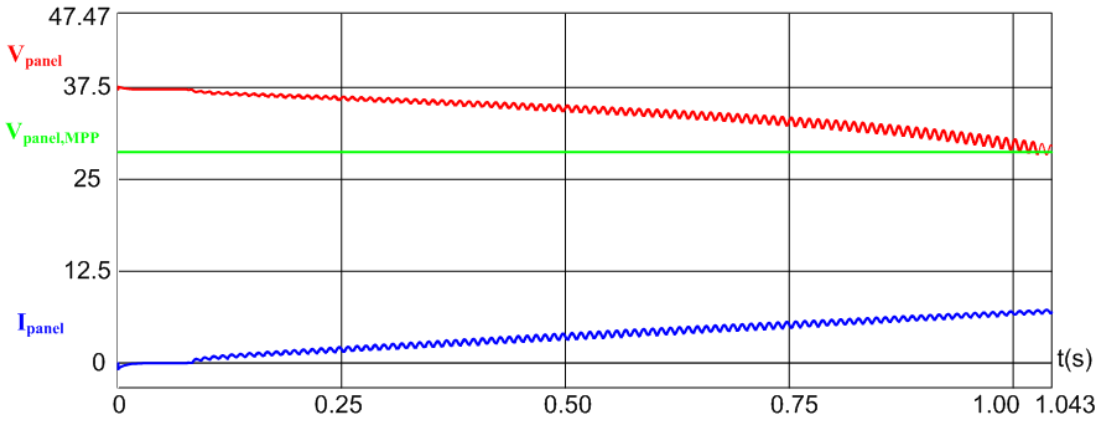

Figure 6.20 Panel voltage (red), panel MPP voltage (green) and current (blue).

In Figure 6.21, the actual PV panel power reaches to MPP of 200W, due to the MPPT operation. Moreover, the effect of the power fluctuation on the grid side on the input power can be observed from the figure as well.

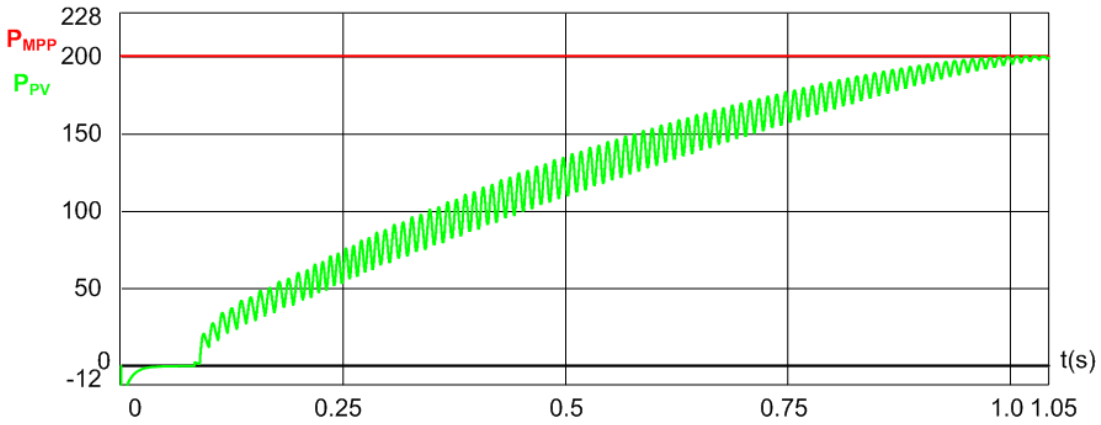

Figure 6.21 PV panel actual power (green), PV panel MPP (red).

While the MPP is reached in 1.04 seconds, the recovery time when a sudden hard shading condition occurs is measured to be 0.565 seconds as it is shown in Figure 6.22 which is nearly equal to the elapsed time for SPMI but better.

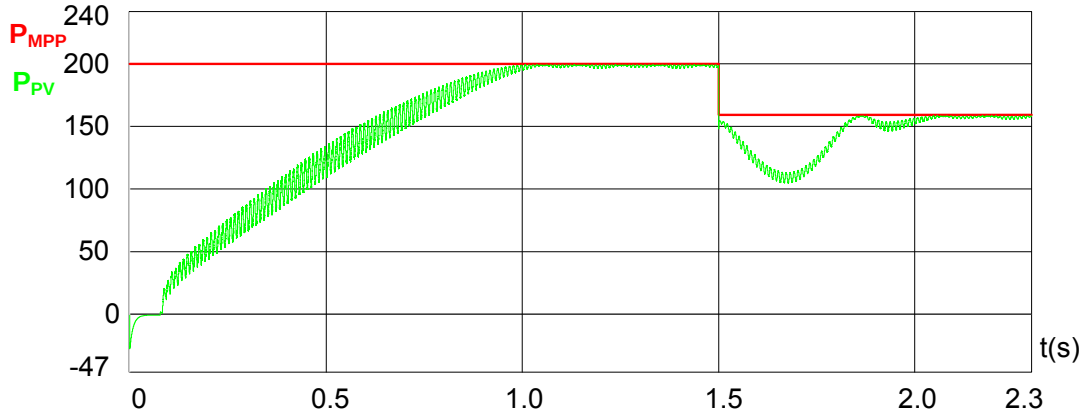

Figure 6.22 PV panel actual power (green), PV panel MPP (red).

6.4 Performance Comparison of SPMI and TPIMI

The simulated results of SPMI and TPIMI topologies are compared according to the steady state and decoupling performances, MPPT performances during start-up and under rapidly changing solar irradiation conditions and switching performances. The performance comparison of two topologies are summarized in Table 6.5.

Table 6.5 Performance comparison of SPMI and TPIMI according to simulation results

Topology	**SPMI**	**TPIMI**
Efficiency at rated power (%)	80.5	84.2
PF at rated power	0.966	0.97
THD_I at rated power (%)	4.52	3.61
Input voltage ripple (%)	4.86	4.16
MPP arrival time (s)	1.08	1.04
MPP recovery time under rapidly changing conditions (s)	0.575	0.565
Peak MOSFET peak voltage (V)	123	125

As it is given in the table, the efficiency of the TPIMI is 3.7% greater than the efficiency of the SPMI at rated power. Moreover, PF and THD_I performances of the TPIMI seems to be better according to the simulation results. In addition, the fluctuation on the input voltage of TPIMI is 0.7% lower due to a better decoupling performance.

On the other hand, MPPT and snubber circuit performances seems to be very similar since the same algorithm is achieved for the topologies. While the reflected output voltage to the input is greater for interleaving operation due to lower turns ratio, the maximum primary MOSFET voltage is slightly higher. On the other hand, snubber circuit performance of both TPIMI and SPMI topologies can be stated as good since the stated limit in Chapter 5 is 150V as well.

CHAPTER 7

THE PERFORMANCE ANALYSIS OF SINGLE-PHASE AND INTERLEAVED FLYBACK-BASED MICRO-INVERTERS VIA EXPERIMENTS

In this chapter, experimental studies of 200W single-phase and 200W two-phase interleaved flyback-based micro-inverters are realized and the compatibility of the experimental results and expected results from Chapter 5 and 6 are examined. At first, system parameters such as PV panel, utility grid and micro-inverter specifications are described. Secondly, experimental setup equipments are identified. Furthermore, experimental results such as steady state measurements, input and output characteristics, dynamic responses are listed and performance analysis of two micro-inverters are realized. Finally the performance comparison of two topologies are carried out.

7.1 System Parameters

The system comes into existence by means of the connection between PV module, micro-inverter and the utility grid. The specifications of these subunits are given in Table 7.1 - 7.4.

During the experiments, PV panel power rarely reached to 180-190W instead of 230W which is the rated power. Observed V_{OC} and V_{MPP} values are lower than the values specified in Table 7.1. As a consequence, measurements are performed at lower power levels than expected. In order to conduct steady state measurements of the MIs at rated power, a GW INSTEK GPC-3060D DC power supply is used as power source.

Table 7.1 Sunrise SR-M660230 PV panel specifications [58]

Electrical characteristics	
Power rating P_{MPP} (W)	230 ± 3
Open circuit voltage V_{OC} (V)	35.92
Short circuit current I_{SC} (A)	8.51
Voltage at maximum power V_{MPP} (V)	29.20
Current at maximum power I_{MPP} (A)	7.88
Panel efficiency η (%)	14.20
Temperature coefficients	
Temperature coefficient of I_{SC}	0.031 %
Temperature coefficient of V_{OC}	-0.37 %
Temperature coefficient of P_{MPP}	-0.53 %
Mechanical characteristics	
Cell type	Mono-crystalline
Number of cells	60 (6 x 10)
Number of bypass diodes	6

Since 18 September 2010, Turkish electricity system is synchronized with the interconnected power systems of Continental Europe [59]. Accordingly, the grid specifications are given in Table 7.2.

Table 7.2 Utility grid specifications

Operation Specifications	
Nominal grid voltage V_{GRID} (V_{RMS})	220
Nominal grid frequency F_{GRID} (Hz)	50

Micro-inverter design parameters are determined due to the calculations in chapter 5. During the implementation of the micro-inverters, some of the parameters are manipulated in order to improve the performance of the system. Design parameters of single-phase and interleaved micro-inverters are listed below.

Table 7.3 Single-phase micro-inverter design parameters

General specifications	
Nominal power (W)	200
Input voltage range V_{IN} (V)	18 - 40
Microcontroller parameters	
Switching frequency F_{SW} (kHz)	170
ADC sampling frequency F_{ADC} (kHz)	170
MPPT sampling frequency F_{MPPT} (kHz)	10
PLL sampling frequency F_{PLL} (kHz)	15
Capacitances	
Input capacitance C_{IN} (μF)	15400 (7 x 2200)
Flyback output capacitance C_{FLY} (nF)	400
Transformer parameters	
Turns ratio N	3 : 19
Primary inductance L_{PR} (μH)	2
Secondary inductance L_{SEC} (μH)	80
Core type	RM-14
LCL filter parameters	
Inverter side inductance L_{INV} (μH)	270
Grid side inductance L_{GRID} (μH)	180
Capacitance (μF)	440
Damping resistor R_d (Ω)	5
Resonance frequency F_{LCL} (kHz)	23

7.2 Experimental Setup

Experimental setup includes the equipments under test (EUT) and measurement equipments such as PV module, micro-inverter, wattmeter, oscilloscope and multi-meter. Control algorithms are implemented with TMS320C2000 Experimenters Kit including a control card with TMS320F28335 Delfino microcontroller and a docking station providing access to all control card signals and on board USB emulation. Code Composer Studio v4 software is used to control the microcontroller. TMS320F28335 runs at 150Mhz and it has 12-bit 16 analog to digital converter (ADC) channels having 80ns conversion rate and 18 PWM outputs. Code Composer Studio gives the opportunity to monitor the program variables from the watch window periodically. Via real time monitoring, accuracy of the signal processing is observed.

Table 7.4 Two-phase interleaved micro-inverter design parameters

General specifications	
Nominal power (W)	200
Input voltage range V_{IN} (V)	18 - 40
Microcontroller parameters	
Switching frequency F_{SW} (kHz)	170
ADC sampling frequency F_{ADC} (kHz)	170
MPPT sampling frequency F_{MPPT} (kHz)	10
PLL sampling frequency F_{PLL} (kHz)	15
Capacitances	
Input capacitance C_{IN} (μF)	15400 (7 x 2200)
Flyback output capacitance C_{FLY} (nF)	400
Transformer parameters	
Turns ratio N	3 : 18
Primary inductances L_{PR} (μH)	3.93
Secondary inductances L_{SEC} (μH)	140.5
Core type	RM-12
LCL filter parameters	
Inverter side inductance L_{INV} (μH)	100
Grid side inductance L_{GRID} (μH)	100
Capacitance (μF)	220
Damping resistor R_d (Ω)	5
Resonance frequency F_{LCL} (kHz)	48

In order to observe the MPPT performance and the steady state performances of the micro-inverters at different power levels, two different computer programs are used. One of the programs lets MPPT algorithm to adjust the current reference according to the power capacity of the PV panel providing maximum energy harvest from the sun. Other program gives the opportunity to the user in order to adjust the current reference externally, providing the user to observe steady state performance of the micro-inverter at different power levels. Steady state measurements of the micro-inverters are performed via the second type of program by means of adjusting PV panel power to certain power levels. Equipments of the system are listed in Table 7.5.

Table 7.5 Experimental setup equipments

Equipment	**Company**	**Model**
PV module	SUNRISE SOLARTECH	SR-M660230
DC power supply	GW INSTEK	GPC-3060D
Wattmeter	HIOKI	3334 AC/DC power HiTESTER
Oscilloscope	TEKTRONIX	TPS2024 digital storage oscilloscope
Current probe	PEM	CWT06 mini Rogowski current transducer
Multi-meter	FLUKE	179 true RMS multi-meter
Microcontroller	TEXAS INSTRUMENTS	TMS320F28335 experimenters kit
Software	TEXAS INSTRUMENTS	Code Composer Studio v4

As it is seen from table 7.1, SUNRISE SOLARTECH SR-M660230 model PV panel and GW INSTEK GPC-3060D DC power supply are used as power source. In order to measure the input and output power, two HIOKI 3334 AC/DC Power Hi-TESTER watt-meters are used. Moreover, in an attempt to verify the accuracy of the wattmeter, Fluke 179 multi-meter with 0,09% accuracy and TPS2024 digital storage oscilloscope with 200Mhz bandwidth, 2GS/s sampling rate and four isolated channels are used. Measurements of these devices are proved to be accurate. With the exception of switching signals, all of the oscilloscope measurements are performed via average mode of the oscilloscope in an effort to filter out the HF noise.

Input and output voltage and current values are also monitored from the watch window of the software. High frequency switching signals such as semiconductor voltages and currents, are measured with the help of CWT06 Mini Rogowski current transducer with 17Mhz bandwidth and 120A current measurement capability. The block diagram of the experimental setup can be seen in Figure 7.1.

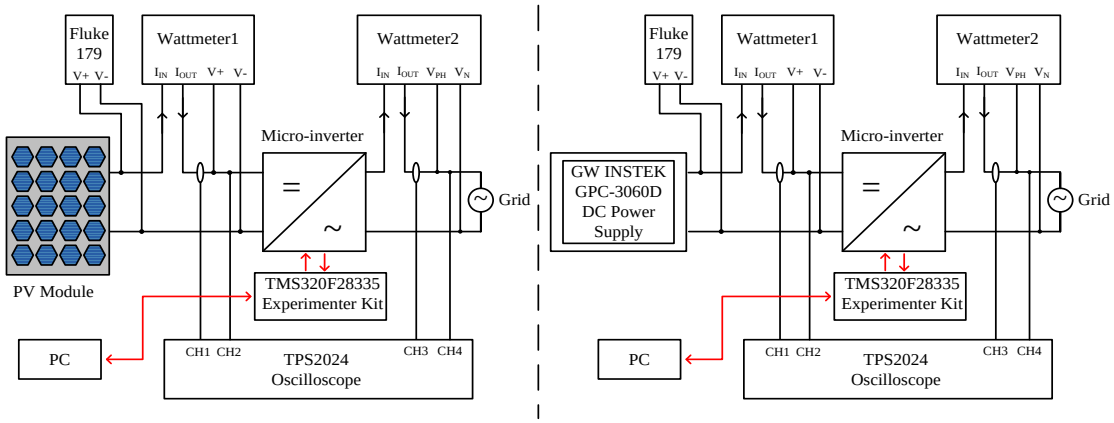

Figure 7.1 Block diagram of the experimental setup with (a) PV panel and (b) DC Power Supply.

In Figure 7.2, the experimental setup including the TPIMI is shown.

Figure 7.2 Experimental setup with TPIMI connected to the grid.

7.3 Experimental Results

In this section, the experimental results of two topologies will be stated. At first, experimental results of single-phase micro-inverter (SPMI) and then the results of two-phase interleaved micro-inverter (TPIMI) will be given.

7.3.1 Experimental Results of SPMI

200W SPMI performance is analyzed in this section. By means of using PV panel as a power source, steady state measurements are conducted to the extent permitted by solar irradiation. In addition to these measurements; input characteristics, switching characteristics, pseudo DC-link and output characteristics are observed and viewed via digital oscilloscope. Moreover, MPPT characteristics at start-up and under rapid hard shading conditions are also determined. With the exception of MPPT characteristics, under favor of DC power supply, all other measurements are conducted at certain power levels including the rated power and the inter-compatibility between the results of PV panel and DC power supply is observed. The implemented SPMI circuit is shown in Figure 7.3.

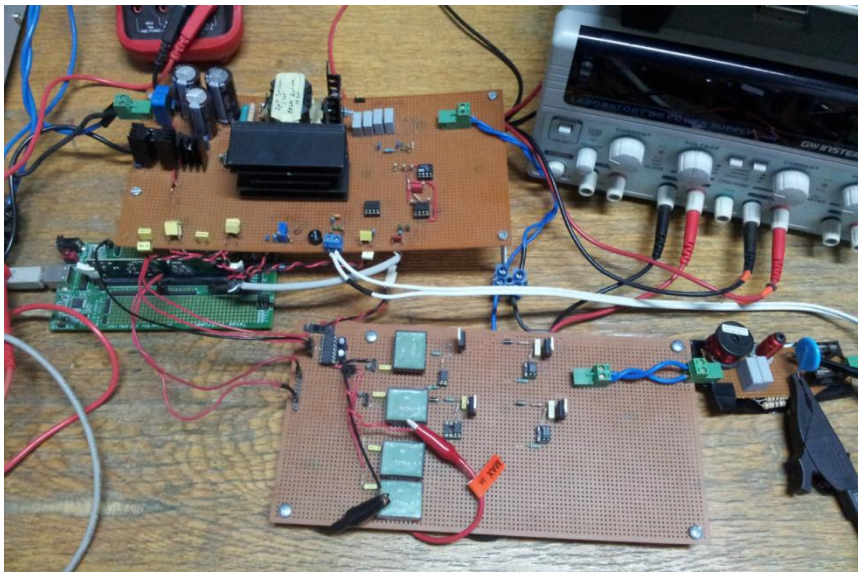

Figure 7.3 SPMI including flyback converter, UB and LCL filter.

7.3.1.1 Steady state measurements

In this section, peak inverter efficiency, euro efficiency, power loss, power factor, grid voltage and grid current total harmonic distortion (THD) of the SPMI are measured.

Steady state measurements of the SPMI at different power levels can be seen in Table 7.6 and Table 7.7. Input and output powers and power factors are measured by watt-meters. Grid voltage and grid current THD values are measured via TPS2024 digital storage oscilloscope. While performing these measurements, power drawn from the sources is adjusted by means of manipulating the current reference value from the software externally. It can be seen from Table 7.6 that the maximum power drawn from the PV panel is 184W during SPMI experiments.

Table 7.6 Steady state measurements of SPMI with PV panel

Input power percentage	**5%**	**10%**	**20%**	**30%**	**50%**	**92%**
Input power P_{IN} (W)	10	20	40	60	100	184
Grid power P_{GRID} (W)	5.3	14.6	31.44	47.58	80	145.36
Power loss P_{LOSS} (W)	4.7	5.4	8.56	12.42	20	38.64
Efficiency η (%)	53	73	78.6	79.3	80	79
Power factor (P.F.)	0.50	0.77	0.923	0.955	0.963	0.97
Grid current THD_I (%)	>100	58	38.2	26	19.4	18.3
Grid voltage THD_V (%)	3.42	3.35	3.35	3.4	3.43	3.36

Table 7.7 Steady state measurements of SPMI with DC power supply

Input power percentage	**5%**	**10%**	**20%**	**30%**	**50%**	**100%**
Input power P_{IN} (W)	10	20	40	60	100	200
Grid power P_{GRID} (W)	5.3	14.7	31.5	47.76	80.13	157.6
Power loss P_{LOSS} (W)	4.7	5.3	8.5	12.24	19.87	42.4
Efficiency η (%)	53	73.5	78.75	79.6	80.13	78.8
Power factor (P.F.)	0.51	0.78	0.93	0.958	0.965	0.972
Grid current THD_I (%)	>100	57.5	37.6	25.3	19.3	17.8
Grid voltage THD_V (%)	3.5	3.33	3.21	3.35	3.4	3.33

It is seen from Table 7.5 and 7.6 that the results are similar with both power supplies. As a result, the measurements at rated power can be accepted as proportionate. The efficiency curve of the SPMI is given in Figure 7.4.

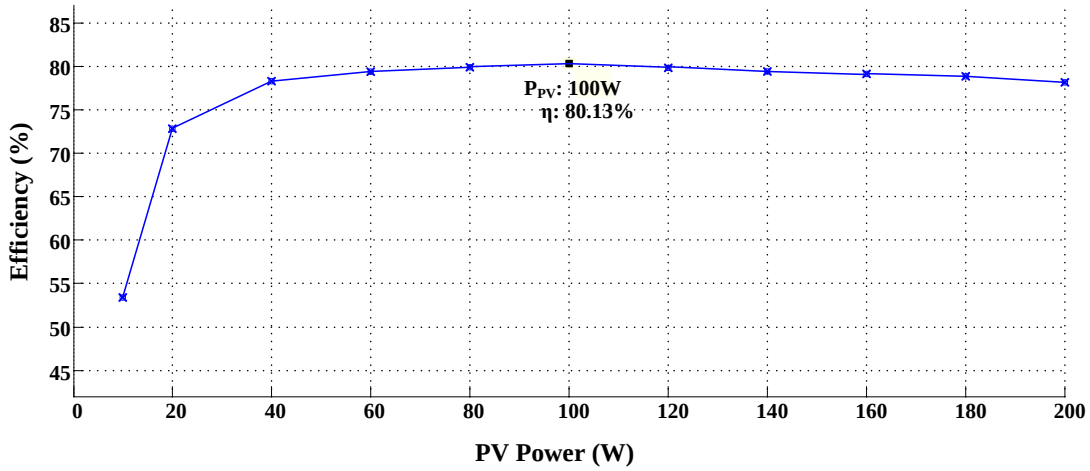

Figure 7.4 Efficiency curve of the SPMI.

An inverter does not always operate at its maximum efficiency over the course of a day. Instead, it has an efficiency profile across the range of the inverters capacity. The value of this weighted efficiency is called European (Euro) Efficiency and is calculated via efficiencies measured at 5%, 10%, 20%, 30%, 50% and 100% of the rated power as in (7.1).

$$\eta euro = 0{,}03\, x\, \eta(5\%) + 0{,}06\, x\, \eta(10\%) + 0{,}13\, x\, \eta(20\%) + 0{,}10\, x\, \eta(30\%) + 0{,}48\, x\, \eta(50\%) + 0{,}20\, x\, \eta(100\%) \quad (7.1)$$

From (7.1), the euro efficiency of the SPMI is calculated as 78.36% which is a low value compared to the commercial micro-inverter efficiencies. From the measurements it is observed that, power consumption for control circuits is 3W and the peak efficiency is 80.13% at 100W input power. Efficiencies are measured including 3W control circuit power consumption. Because of the copper, eddy current losses of flyback transformer and switching, conduction losses of the semiconductors, efficiency is lower than calculated (81%). In addition, THD_I of the inverter is greater than the simulated results specified in chapter 6 which is 4.52%. On the other hand Power Factor performance of the SPMI can be defined as good since at 100W input power, P.F. is greater than 0.95.

7.3.1.2 Input Characteristics

Input voltage and current of SPMI can be seen in Figure 7.5. The peak to peak values are measured as 1.8V and 0.8A at 187W input power. Input capacitor of the SPMI is 15.4mF which corresponds to 1.31Vpk-pk ripple voltage according to (3.6) in case of given circumstances. It can be seen that the measured peak to peak input voltage ripple ($V_{IN\ pk\text{-}pk}$) is 0.49V larger than expected but under the 8.5% design limit which is 6.10% of V_{PV}.

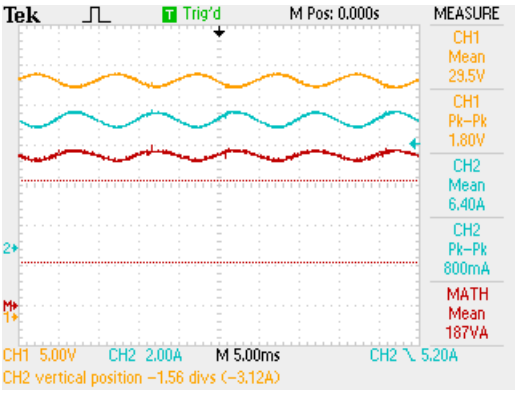

Figure 7.5 Input voltage (CH1-5V/div), current (CH2-2A/div) and power (MATH-50W/div) pk-pk and mean values (5ms/div).

7.3.1.3 Switching Characteristics

Switching characteristics of the SPMI are shown in Figure 7.6 and 7.7. In Figure 7.6, MOSFET current and voltage waveforms are shown. In Figure 7.7, MOSFET voltage and flyback diode current waveforms are shown in order to observe the DCM operation.

As it is mentioned in Chapter 5, when flyback MOSFET turns off, because of the output capacitance of the MOSFET and primary leakage inductance of the flyback transformer, a voltage spike takes place on the MOSFET voltage as it is seen in Figure 7.6. In order to limit this voltage spike, required snubber resistor and capacitor values are calculated in Chapter 5.

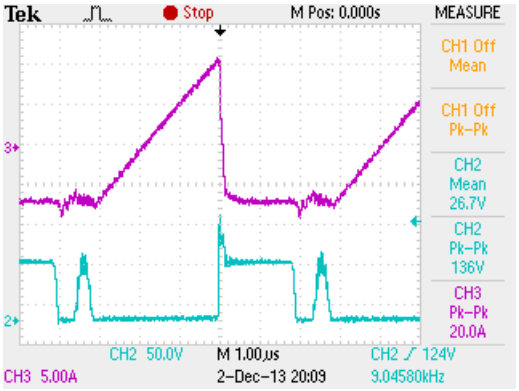

Figure 7.6 MOSFET voltage (CH2-50V/div) and current (CH4-5A/div)(1µs/div).

The peak MOSFET voltage is 136V and the amplitude of the voltage spike is measured to be 57V which is under the calculated 75V voltage spike limit. As a result of DCM operation, diode current goes to zero before MOSFET turns on and the voltage starts to fluctuate because of the resonation between MOSFET output capacitance and flyback transformer magnetizing inductance. MOSFET voltage equals to zero during turn-on period.

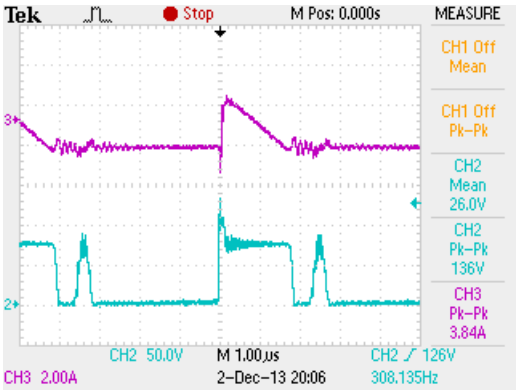

Figure 7.7 MOSFET voltage(CH2-50V/div) and diode current(CH4-5A/div)(1µs).

7.3.1.4 Pseudo DC-link and Output Characteristics

As it is mentioned before, pseudo DC-link current and voltage of the micro-inverter have a rectified sine waveform. By means of an unfolding bridge structure following

the flyback converter, these pseudo DC-link waveforms are converted to sinusoidal form. In this section, pseudo DC-link and output waveforms will be given. From Figure 7.8, pseudo DC-link voltage and current of the micro-inverter can be seen.

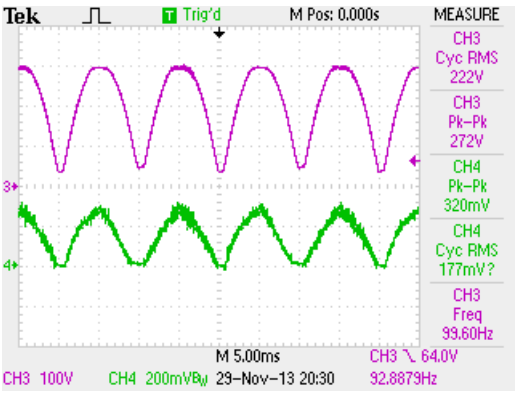

Figure 7.8 Pseudo DC-link voltage (CH3-100V/div) and current (CH4-200mV/div)(5ms/div).

Pseudo DC-link current is measured from the terminals of the sense resistor which is 270mΩ. Moreover, the pseudo DC-link voltage and current waveforms are converted to sinusoidal form via unfolding MOSFETs operating at grid frequency. Pseudo DC-link voltage and gate signals of UB MOSFETs can be seen in Figure 7.9.

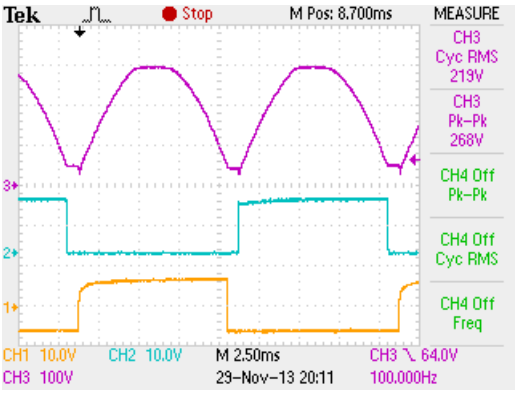

Figure 7.9 Unfolding bridge MOSFET gate drive signals (CH1 - CH2 - 10V/div) and pseudo DC-link voltage (CH3-100V/div)(2.5ms/div).

Pseudo DC-link voltage at system start-up can be seen in Figure 7.10. When input voltage increases to a certain value, PLL determines the grid frequency. If the grid frequency is between specified limits and the synchronization is completed, UB MOSFETs start to conduct according to the polarity of the grid voltage.

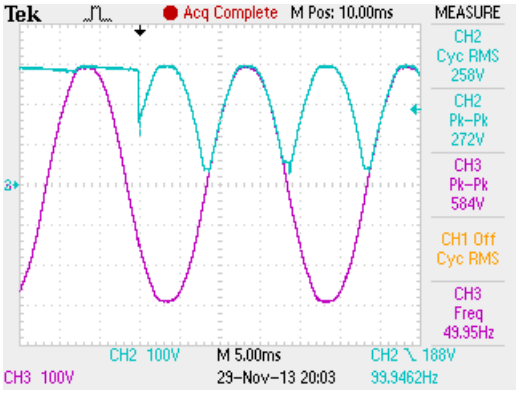

Figure 7.10 Pseudo DC-link voltage (CH2-100V/div) and grid voltage (CH3-100V/div) at start-up (5ms/div).

The output voltage (grid voltage), output current (grid current) and the output power (MATH) of the micro-inverter at half load and full load is shown in Figure 7.11 and Figure 7.12 respectively.

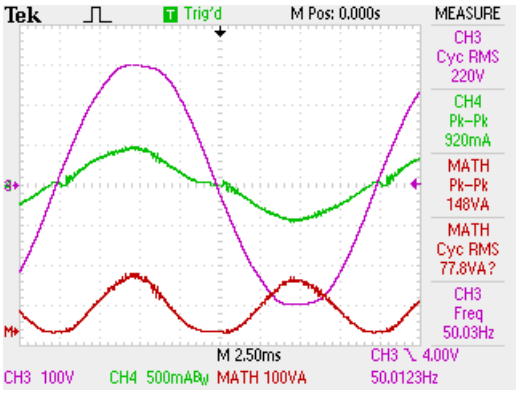

Figure 7.11 Grid voltage (CH3-100V/div) grid current (CH4-500mA/div) and output power (MATH-100VA/div) of the micro-inverter at half load (2.5ms/div).

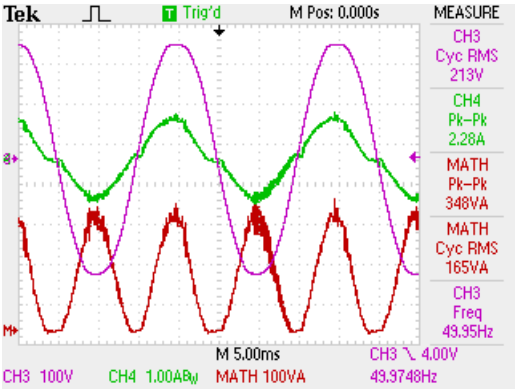

Figure 7.12 Grid voltage (CH3-100V/div) grid current (CH4-1A/div) and output power (MATH-100VA/div) of the micro-inverter at full load (5ms/div).

Zero crossings of the grid current adjusted to be large in order to prevent current spikes which is also effecting the THD performance of the micro-inverter adversely.

7.3.1.5 Dynamic Response at Start-Up and Under Rapidly Changing Conditions

When the system starts up, if grid synchronization is completed, grid voltage specifications are between limits and input voltage is higher than a specified value, MPPT algorithm starts to search for the maximum power point of the PV panel and increases the current reference value in order to increase power drawn from the panel. The MPPT performance of the SPMI can be seen in Figure 7.13.

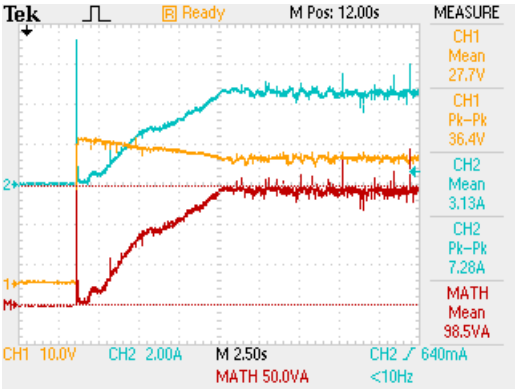

Figure 7.13 SPMI input voltage (CH1-10V/div), input current (CH2-2A/div) and input power (MATH-50VA/div) at system start-up (2.5s/div).

As it can be seen from Figure 7.13, MPP of 160W is reached in 9 seconds. In order to reduce the duration, perturbation period and perturbation step size of the MPPT algorithm can be reduced. The lower limit of the perturbation period is the grid frequency. As it is mentioned in chapter 4, perturbation must take place at zero crossings of the grid voltage which causes the minimum perturbation period to be 10ms for a 50Hz utility grid. On the other hand, the upper limit of the perturbation step size is the input power oscillations around MPP created by the P&O algorithm causing power losses. Optimum perturbation period and step size is determined via experimental studies.

The continuous operation of the micro-inverter is dependent on the PV characteristics varying with atmospheric conditions. As it is mentioned before, the power generated by the PV panel is highly sensitive to solar irradiation and the amount of solar irradiation changes with soft and hard shading effects. Soft shading occurs because of the weather conditions such as cloudy or foggy weather relatively slower than hard shading which occurs because of the objects standing between the sun and PV panel.

Soft shading effects can be tolerated by means of P&O algorithm easily. On the other hand, the effect of hard shading can be instant and influential because of the internal structure of the PV panel and can cause great amount of power loss in a few milliseconds. Controller of the micro-inverter must be able to sense the rapid changes of PV panel power.

If the controller does not act immediately and try to transfer the same amount of energy to the grid, it will increase the duty cycle and will enter CCM region causing the controller to lose its effectiveness. At the same time, increased duty cycle further decreases the PV panel voltage under operating limits because of overloading, causing the micro-inverter to shut down and loss of available energy.

In order to observe the effects of hard shading, a constant resistive load is fed by the PV panel. During energy transfer to the resistive load, one of the PV cells is shaded and the variations of the PV panel voltage, current and power are measured as it is

seen in Figure 7.14. Before hard shading condition, PV panel was transferring 193W at 28V. After one PV cell is shaded, 90W of power loss with 7.6V voltage drop is observed. When four of the PV cells are shaded, 100W of power loss with 8.4V voltage drop is observed as it is seen in Figure 7.15. In order to prevent the effects of rapid hard shading conditions, an algorithm is added to the software which senses PV voltage variation in a short time and decreases duty cycle preventing instant voltage drops and shut down of the micro-inverter.

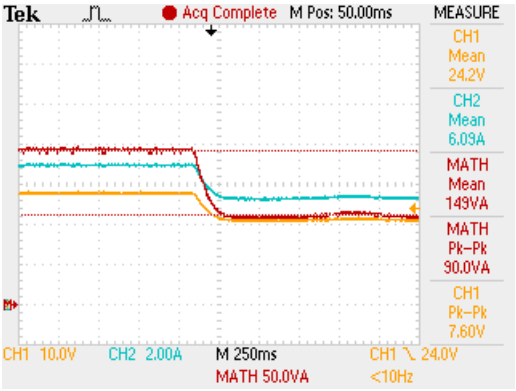

Figure 7.14 SPMI input voltage (CH1-10V/div), input current (CH2-2A/div) and input power (MATH-50VA/div) during hard shading of one PV cell (250ms/div).

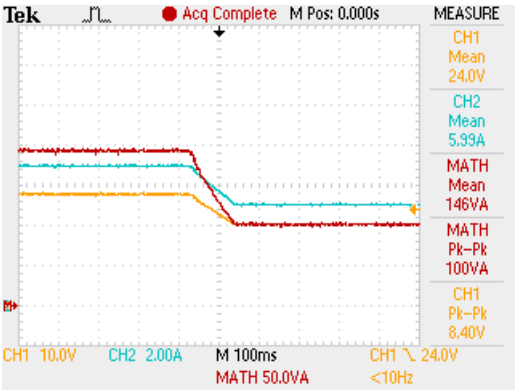

Figure 7.15 SPMI input voltage (CH1-10V/div), input current (CH2-2A/div) and input power (MATH-50VA/div) during hard shading of four PV cells (100ms/div).

In order to observe hard shading performance of the SPMI, one PV cell of the panel is shaded for a short duration. Figure 7.16 shows the effects of hard shading and the reaction of the controller. The amount of power loss and voltage drop can be seen when only one of the PV cells is shaded.

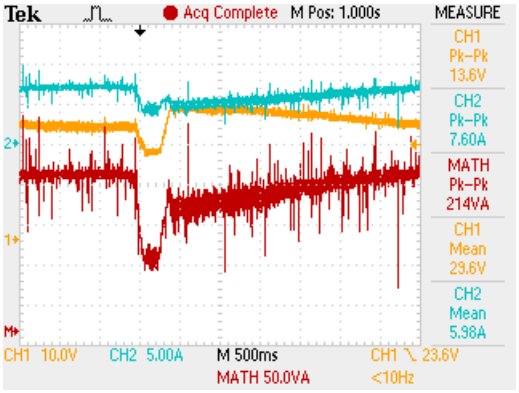

Figure 7.16 Input voltage(CH1-10V/div), current (CH2-5A/div) and power (MATH-50VA/div) variations during hard shading (500ms/div).

When a hard shading condition occurs, PV power starts to decrease immediately and the controller decreases the duty cycle by decreasing current reference preventing the panel current to increase and cause a short circuit condition. If voltage drop of panel voltage is smaller than a certain value, MPPT algorithm starts to search for MPP again and normal operation continues.

7.3.2 Experimental Results of TPIMI

200W TPIMI performance is analyzed in this section. As in section 7.3.1, by means of using PV panel as a power source, steady state measurements are conducted to the extent permitted by solar irradiation. Input characteristics, switching characteristics, pseudo DC-link and output characteristics are observed and viewed via digital oscilloscope. MPPT characteristics at start-up and under rapid hard shading conditions are determined. With the exception of MPPT characteristics, under favor of DC power supply, all other measurements are conducted at certain power levels

including the rated power and the inter-compatibility between the results of PV panel and DC power supply is observed. The implemented TPIMI circuit is shown in Figure 7.17.

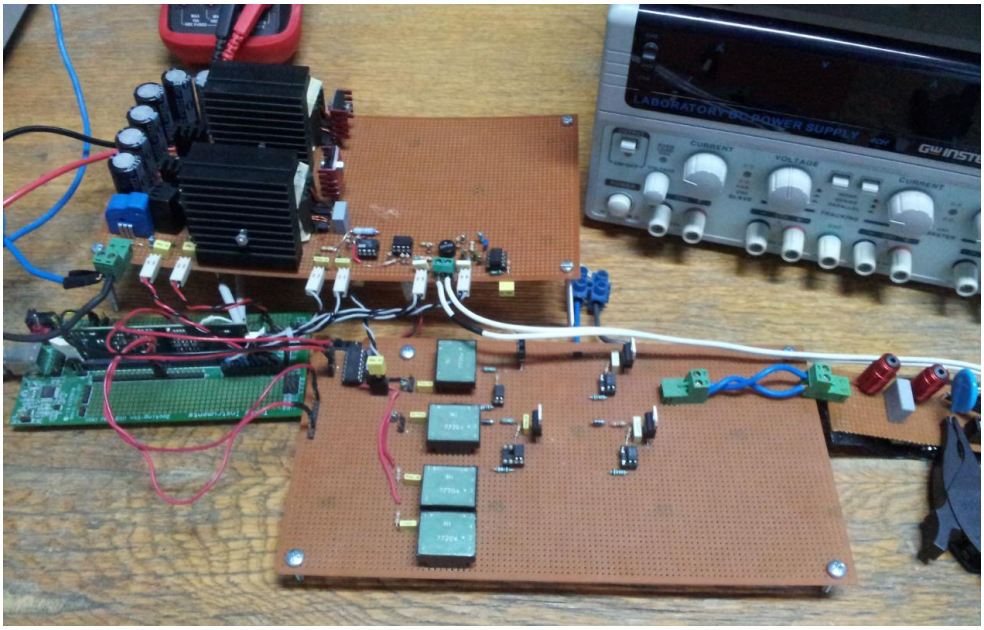

Figure 7.17 TPIMI including flyback converters, UB and LCL filter.

7.3.2.1 Steady state measurements

Just as in 7.3.1.1, peak efficiency and euro efficiency, power factor, power loss, grid voltage and grid current total harmonic distortion (THD) of the micro-inverter are measured in this section. Steady state measurements of the TPIMI at different power levels can be seen in Table 7.8 and Table 7.9.

While performing the measurements, power drawn from the sources is adjusted by means of manipulating the current reference value from the software externally. It can be seen from Table 7.6 that the maximum power drawn from the PV panel is 185W during SPMI experiments.

Table 7.8 Steady state measurements of TPIMI with PV panel

Input Power Percentage	**5%**	**10%**	**20%**	**30%**	**50%**	**92,5%**
Input power P_{IN} (W)	10	20	40	60	100	185
Grid power P_{GRID} (W)	4.7	13.6	30.8	48.85	83.5	155.77
Power loss P_{LOSS} (W)	5.3	6.4	9.2	11.15	16.5	29.23
Efficiency η (%)	47	68	77	81.42	83.5	84.2
Power factor (P.F.)	0.4	0.8	0.896	0.93	0.961	0.97
Grid current THD_I (%)	>100	56	35.8	23.9	17.6	14.6
Grid voltage THD_V (%)	3.18	3.16	3.08	3.43	3.43	3.36

Table 7.9 Steady state measurements of TPIMI with DC power supply

Input Power Percentage	**5%**	**10%**	**20%**	**30%**	**50%**	**100%**
Input power P_{IN} (W)	10	20	40	60	100	200
Grid power P_{GRID} (W)	4.8	13.7	31.1	49.1	83.8	168.1
Power loss P_{LOSS} (W)	5.2	6.3	8.9	10.9	16.2	31.9
Efficiency η (%)	48	68.5	77.75	81.84	83.8	84.05
Power factor (P.F.)	0.40	0.76	0.912	0.945	0.968	0.975
Grid current THD_I (%)	>100	54.2	35.5	23.6	17.5	14.1
Grid voltage THD_V (%)	3.2	3.35	3.25	3.43	3.4	3.25

It can be seen from Table 7.8 and 7.9 that the results are similar with two types of power supplies. As a result, the measurements at rated power can be accepted as proportionate to the measurements with PV panel. The efficiency curve of the TPIMI is given in Figure 7.18.

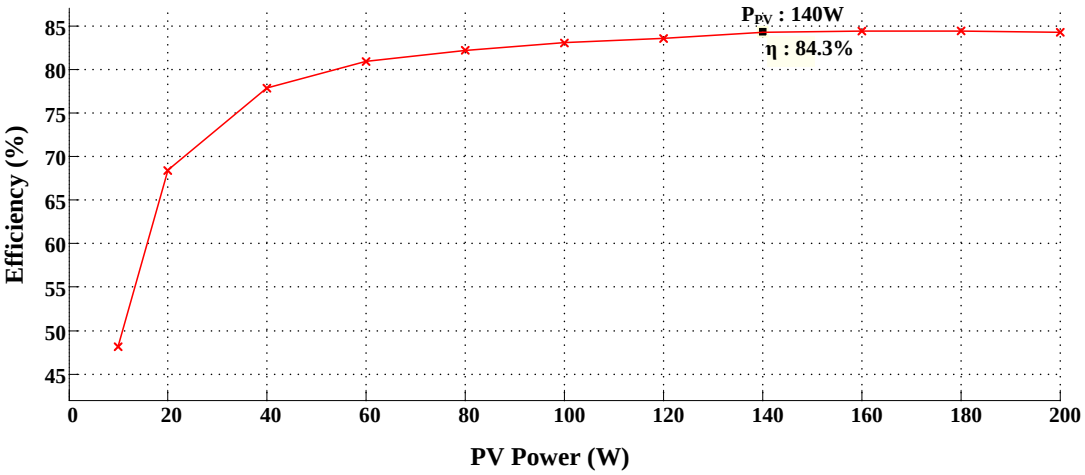

Figure 7.18 Efficiency curve of TPIMI.

The euro efficiency of the TPIMI is calculated from (7.1) as shown blow;

$$\eta euro = 0{,}03\ x\ 48 + 0{,}06\ x\ 68.5 + 0{,}13\ x\ 77{,}75 + 0{,}10\ x\ 81.84 + 0{,}48\ x\ 83{,}8 + 0{,}20\ x\ 84{,}05 \quad (7.2)$$

From (7.2), TPIMI Euro efficiency is calculated as 80.88% which is also a low value compared to the commercial micro-inverter efficiencies but better than SPMI efficiency. From the measurements it is observed that, power consumption for control circuits is 2.5W and the peak efficiency is 84.35% at 140W input power.

Because of the copper and eddy current losses of the flyback transformer and switching, conduction losses of the semiconductors, efficiency is lower than calculated 85.2% efficiency. THD_I performance of TPIMI is higher than the limits stated in standards. On the other hand, PF performance of the TPMI is similar with SPMI performance which also can be stated as good. The efficiency characteristics and efficiency curves of two-phases shown in Table 7.10 and Figure 7.19.

Table 7.10 Efficiency characteristics of TPIMI phase 1 and phase 2 with DC power supply

Input power percentage	**5%**	**10%**	**20%**	**30%**	**50%**	**100%**
Input power P_{IN} (W)	5	10	20	30	50	100
Phase 1 efficiency η (%)	32	62	74	78	80	82.2
Phase 2 efficiency η (%)	28	60	75	81	83.2	85.4

The efficiency difference between two phases can be explained by the additional leakage inductances and the non-idealities between the transformers of the TPIMI.

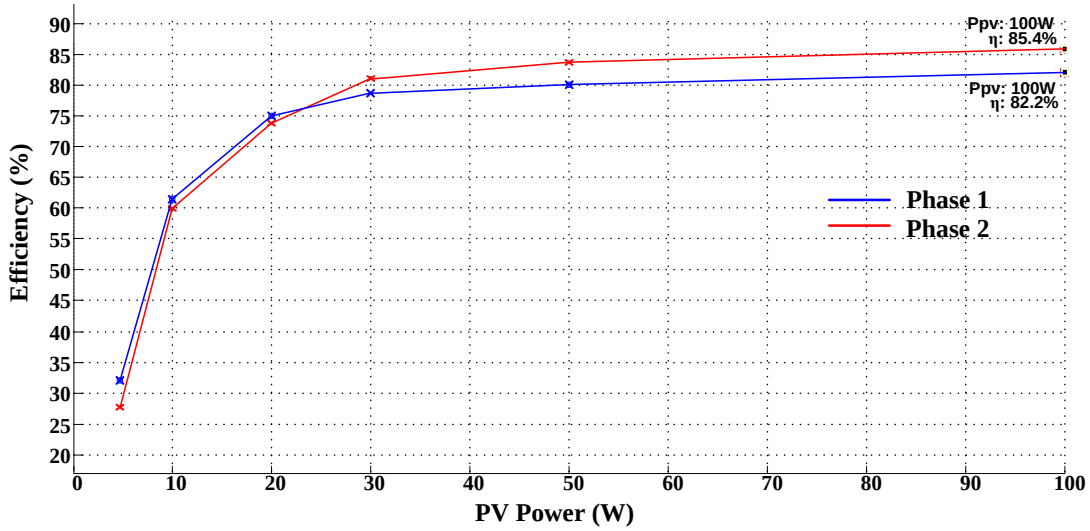

Figure 7.19 Efficiency curves of TPIMI phases: phase 1 (Blue), phase 2 (Red).

7.3.2.2 Input Characteristics

Input voltage and current of micro-inverter can be seen in Figure 7.20. The peak to peak values are measured as 1.6V and 0.96A at 179W input power. Input capacitor of the TPIMI is 15.4mF which correspond to $1.35V_{pk\text{-}pk}$ ripple voltage according to (3.6). It can be seen that the measured peak to peak input voltage ripple ($V_{IN\ pk\text{-}pk}$) is 5.83% of the input voltage and 0.25V larger than expected but still lower than 8.5%.

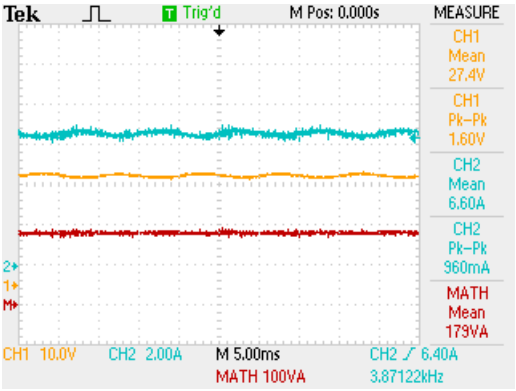

Figure 7.20 Input voltage(CH1-10V/div), current (CH2-2A/div) and power (MATH-100VA/div) pk-pk and mean values (5ms/div).

7.3.2.3 Switching Characteristics

Switching characteristics of TPIMI MOSFETs and diodes are shown in Figure 7.21, 7.22 and 7.23. In Figure 7.21, MOSFET voltage waveforms of two-phases are shown. The 180° phase shift of two voltages can be seen. In Figure 7.22, Phase 1 MOSFET voltage and current waveforms are shown in order to observe the DCM operation of TPIMI.

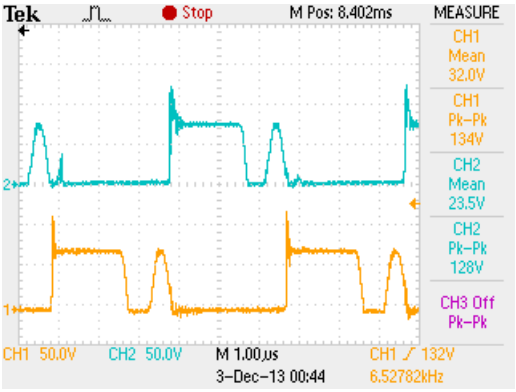

Figure 7.21 Flyback MOSFET voltages of two-phases: Phase 1 (CH1-50V/div) and Phase 2 (CH2-50V/div) (1µs/div).

Such in Section 7.3.1.3, voltage spike takes place on the MOSFET voltage as it is seen in the figures. Required snubber resistor and capacitor values are calculated in chapter 5 for TPIMI. The peak MOSFET voltages are measured as 134V and 128V respectively. The amplitudes of the voltage spikes are measured to be 51V and 47V which are under the 75V voltage spike limit at rated power. As a result of DCM operation, similar characteristics of semiconductor voltages and currents with SPMI are observed in Figure 7.22 and 7.23.

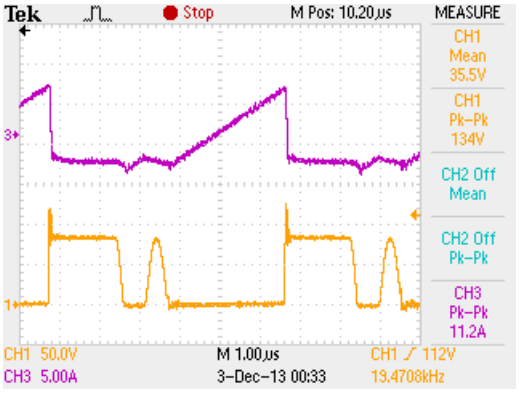

Figure 7.22 Phase 1 MOSFET voltage (CH1-50V/div) and current (CH3-5A/div) (1µs/div).

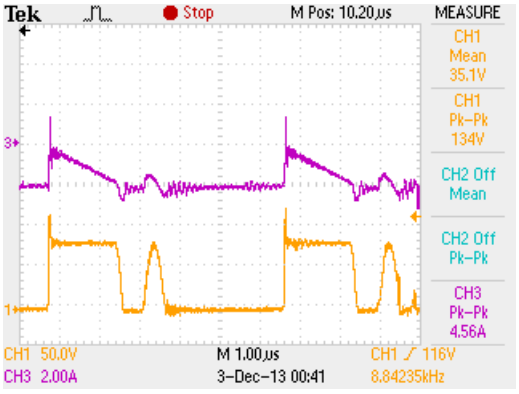

Figure 7.23 Phase 1 MOSFET voltage (CH1-50V/div) and diode current (CH3-2A/div) (1µs/div)

7.3.2.4 Pseudo DC-link and Output Characteristics

In this section, TPIMI pseudo DC-link and output waveforms will be given. As it is shown in Figure 7.24, pseudo DC-link voltage and current of the MI are measured.

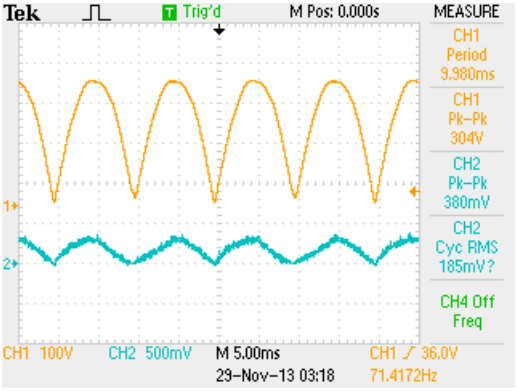

Figure 7.24 Pseudo DC-link voltage (CH1-100V/div), current (CH2-500mV/div).

As is the case with SPMI topology, pseudo DC-link current is measured from the terminals of the sense resistor which is 270mΩ. Furthermore, the pseudo DC-link voltage and current are converted to sinusoidal waveform via unfolding MOSFETs operating at grid frequency. Unfolding bridge gate signals and pseudo DC-link voltage can be seen in Figure 7.25.

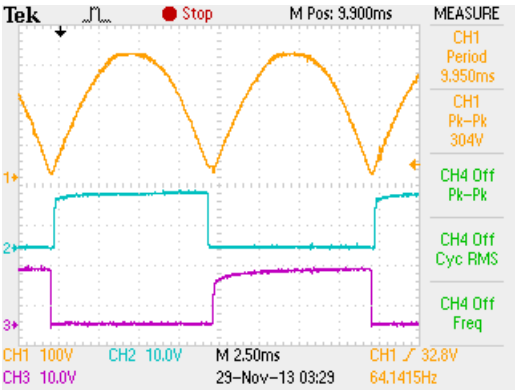

Figure 7.25 Pseudo DC-link voltage (CH1-100V/div) and UB MOSFET gate drive signals (CH2-CH3-10V/div) (2.5ms/div).

Pseudo DC-link voltage at system start-up can be seen in Figure 7.26. Since the same algorithms with SPMI are used, when input voltage increases to a certain value, PLL determines the grid frequency. If the grid frequency is between specified limits and the synchronization is completed, unfolding bridge MOSFETs start to conduct according to the polarity of the grid voltage.

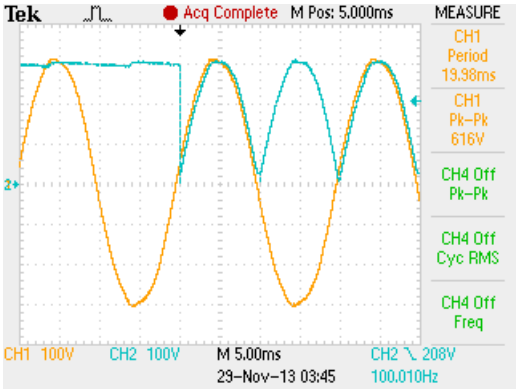

Figure 7.26 Pseudo DC-link voltage (CH2-100V/div) and grid voltage (CH3-100V/div) at start-up (5ms/div).

The output voltage, current and the power (MATH) waveforms of TPIMI at half-load and full-load are shown in Figure 7.27 and Figure 7.28 respectively.

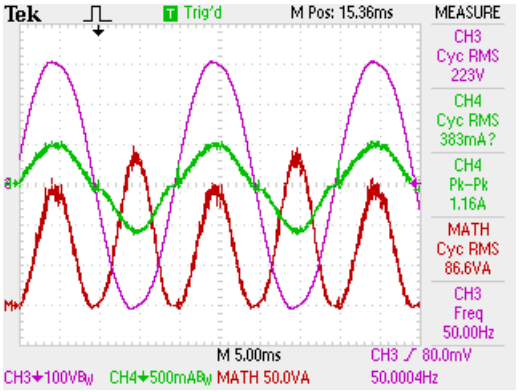

Figure 7.27 Output voltage (CH3-100V/div), current (CH4-500mA/div) and power (MATH-50VA/div) of TPIMI (half-load) (5ms/div).

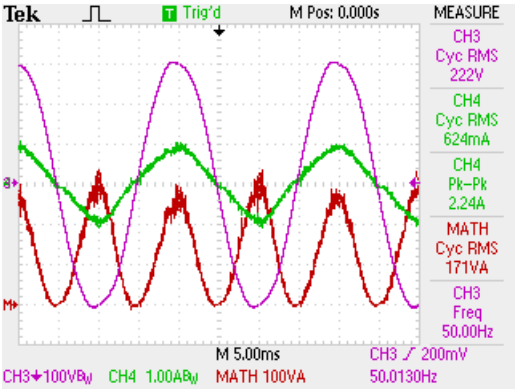

Figure 7.28 Output voltage (CH3-100V/div), current (CH4-1A/div) and power (MATH-100VA/div) of TPIMI (full-load) (5ms/div).

7.3.2.5 Dynamic Response at Start-Up and Under Rapidly Changing Conditions

The MPPT performance of the TPIMI during start-up can be seen in Figure 7.29.

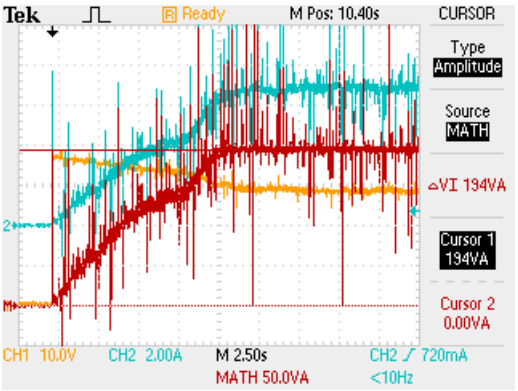

Figure 7.29 TPIMI input voltage (CH1-10V/div), input current (CH2-2A/div) and input power (MATH-50VA/div) at system start-up (2.5s/div).

As it can be seen from Figure 7.29 MPP is reached in 10 seconds. Such in section 7.3.1.5, the optimum perturbation period and step size is determined via experimental studies.

In order to prevent the effects of rapid hard shading conditions, same algorithm is added to the software of TPIMI which senses PV voltage variation in a short time and decreases duty cycle preventing instant voltage drops and shut down of the micro-inverter.

Figure 7.30 shows the effects of hard shading for a short duration and the reaction of the controller. As it is seen from the figure, as for SPMI, when an instant hard shading condition occurs, the power drawn from the panel decreases instantly. When the amount of voltage drop is greater than the specified limit, controller decreases the duty cycle (current reference) preventing the possibility of short circuit condition and micro-inverter continues to operate without shutting down. If voltage drop of panel voltage is lower than a certain value, MPPT algorithm starts again to search for MPP.

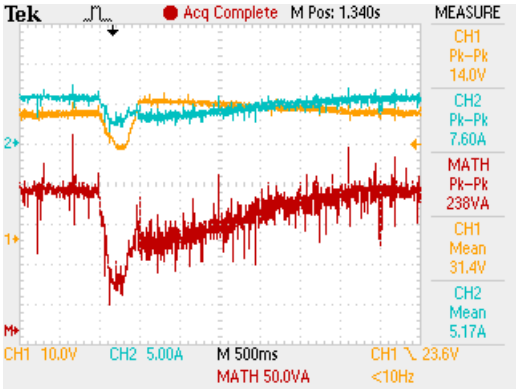

Figure 7.30 Input voltage(CH1-10V/div), current(CH2-5A/div)and power(MATH-50VA/div) variations during hard shading (500ms/div).

7.4 Performance Comparison of SPMI and TPIMI

Steady state performances, decoupling performances and dynamic response of two topologies are compared in this section.

The performance comparison of two topologies are summarized in Table 7.11. It can be seen that, peak, euro and rated power efficiencies of TPIMI are greater than SPMI

efficiencies. In addition, the power loss is reduced from 21.2% to 14.95% and euro efficiency is improved by 2.52% at rated power by means of interleaving which contributes to increase the profit and reduce the payback period of the system. On the other hand both efficiencies can be stated as low compared to the commercial MI products.

Table 7.11 Performance comparison of two topologies

Topology	**SPMI**	**TPIMI**
Peak efficiency (%)	80.13	84.35
Euro efficiency (%)	78.36	80.88
Efficiency at rated power (%)	78.8	84.05
PF at rated power	0.972	0.975
THD_I at rated power (%)	17.8	14.1
THD_V at rated power (%)	3.33	3.25
Input voltage ripple (%)	6.10	5.83
MPPT arrival time (s)	8.5 (160W)	10 (190W)
MPPT recovery time (s)	3	3
Peak MOSFET peak voltage (V)	136	134

Efficiency curves of both topologies can be seen in Figure 7.31. As it is seen from the figure, TPIMI is more efficient when the input power is greater than 44W. Moreover, it is possible to control TPIMI phases such that only one phase of TPIMI operates for power ratings where SPMI efficiency is higher. On the contrary, for the micro-inverters implemented in this study, interception point of efficiencies is very low (44W) and the lowest power produced by the PV panel is nearly 30W at cloudy days. Therefore single-phase control of TPIMI is not conducted.

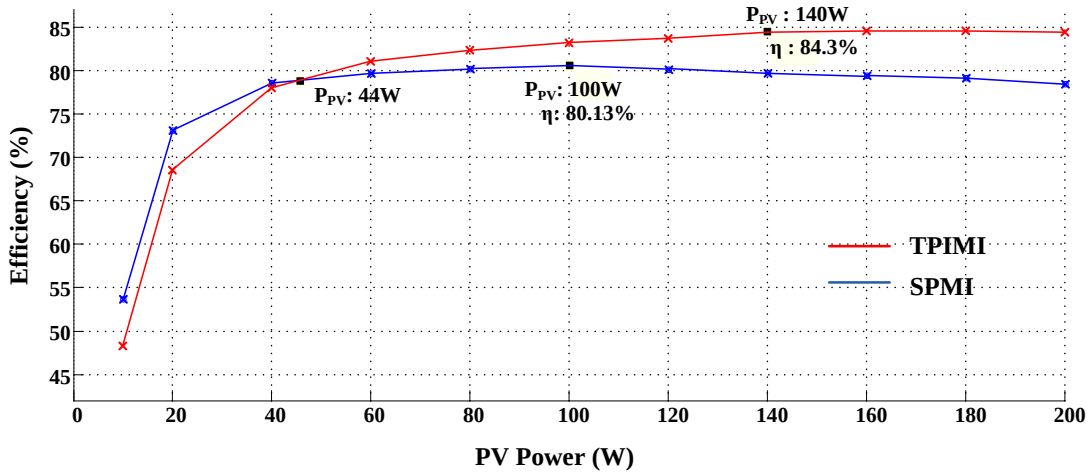

Figure 7.31 Efficiency comparison of TPIMI and SPMI.

Although PF performances of two topologies are very close to each other, PF of TPIMI is slightly greater than PF of SPMI at rated power. On the other hand, both performances can be stated as good since PFs are greater than 0.9 at half load. Furthermore, both PFs are greater than the simulation results. THD_I performance of the TPIMI is also 3.7% better than the performance of SPMI by means of ripple cancellation due to 180° phase shifted switching which also reduces the required filter parameters. On the other hand, THD_I results are greater than simulated THD_I performances and the limits stated in the standards for both topologies.

The effectiveness of the decoupling capacitors for both topologies are very close to each other. In addition to that, input voltage and current ripples of both topologies are more than expected but under the specified limits. As it is mentioned before, the measured input voltage ripple is 1.8V for SPMI. However it is 1.6V for TPIMI. While the percentage of the ripple is 6.10% for SPMI, it is 5.83% for TPIMI which can be stated as a better performance. In addition, it can be seen that the measured ripples are compatible with the simulation results. Moreover, lower input voltage ripple reduces the required number of decoupling capacitors also reducing the system cost.

The dynamic performance of two topologies includes the elapsed time in order to reach MPP of PV panel and performance of MPPT under hard shading condition. Since the same algorithm is used for both of the topologies, elapsed times are very close. As it is mentioned before, SPMI reaches MPP of 160W in 8.5 seconds and TPIMI reaches MPP of 190W in 10 seconds. Same condition is valid for hard shading performances such that the elapsed time to reach MPP of the PV panel after hard shading is nearly 3s for both topologies.

Since additional leakage inductances cause the peak MOSFET voltages to be larger than the simulated results, peak MOSFET voltages are measured to be 136V and 134V for SPMI and TPIMI topologies respectively which are under the design limit of 150V.

CHAPTER 8

CONCLUSION

In recently increasing PV energy applications, as important parts of the system, the DC-AC converters have been drawing significant attention constituting the interface between the PV module and the utility grid transferring the solar energy captured from the sun. New inverter systems have been under development such as central inverters, string inverters, multi-string inverters and micro-inverters. Among these, micro-inverters are typically designed for small-scale residential PV applications having advantages such as PV module level energy generation, plug-N-play operation and module level MPPT with high reliability. Micro-inverters involve various inverter topologies. According to the DC-link configurations, these topologies can be classified into three categories as MI with DC-link, MI with pseudo DC-link and MI without DC-link. Among micro-inverters with pseudo DC-link, also known as single-stage micro-inverters, the flyback MI topology is widely used due to its low semiconductor count, ease of implementation and control, galvanic isolation and low cost.

This thesis investigated a single-phase single-stage flyback-based micro-inverter consisting of a decoupling capacitor bank placed at the input absorbing the instantaneous power mismatch between input and output, a flyback converter including an RCD snubber increasing the PV panel voltage to the levels compatible with grid voltage, providing sinusoidal current control, achieving MPPT and providing galvanic isolation between PV module and the grid, an unfolding bridge operating at mains frequency unfolding the rectified sine wave voltage (current) into sinusoidal form via switching semiconductors at zero crossings of the grid according to the grid voltage polarity, and finally an LCL filter filtering out high frequency

noise and realizing grid connection. Two-phase interleaved flyback-based micro-inverter is also developed and investigated including two flyback converters connected in parallel sharing input current by means of 180° phase shifted operation.

The contribution of this thesis is the controller and hardware design, performance evaluation and comparison of 200W single-phase and two-phase interleaving flyback micro-inverters for grid-connected residential PV systems via mathematical calculations, computer simulations and experimental studies. The verification between calculations, simulations and experiments are conducted and the benefits of interleaving is demonstrated.

The control of the aforementioned micro-inverters are realized via perturb & observe (P&O) based maximum power point tracking (MPPT), transport delay-based phase locked loop (PLL) and sinusoidal current reference generation (SCRG) providing maximum energy harvest from the PV panel, grid synchronization and sinusoidal current injection to the grid. In order to further improve the performance of the MIs, DCM operation, providing soft switching of semiconductors, removing reverse recovery problem, reducing switching losses and EMI radiation, is guaranteed by the design. Besides, DCM operated controller does not present right half plane zero which makes it easy to stabilize the control loop and utilizes constant switching frequency (CSF) increasing the simplicity of the controller.

In order to compare the performances of the mentioned topologies such as efficiencies, output current THDs, MPPT, decoupling and switching performances, the designed models are simulated by means of Ansoft Simplorer Simulation Center 7.0 simulation program. It is observed that the performances of two-phase interleaved micro-inverter (TPIMI) is superior to the performance of the single-phase micro-inverter (SPMI). While the efficiency, PF and THD_I of the SPMI are measured to be 80.5%, 0.966 and 4.52% respectively, they are measured as 84.2%, 0.97 and 3.61% for TPIMI corresponding to a better performance. Moreover, the percentage input voltage ripple of the SPMI and TPIMI are simulated to be 4.86% and 4.16% corresponding for TPIMI to a better decoupling performance. Besides,

the MPPT and switching performances of both topologies can be stated as equal according to the simulation results.

On the purpose of verifying the design and simulation results, the experimental models of the SPMI and TPIMI are implemented in accordance with the design parameters and the simulated models. The euro efficiencies of the SPMI and TPIMI are measured as 78.36% and 80.88% respectively. Moreover, via interleaving operation, the maximum efficiency increases from 80.13% to 84.35%. Although PF performances of two topologies are very close to each other, PF of TPIMI (0.975) is slightly greater than PF of SPMI (0.972) at rated power. On the other hand, both performances can be stated as good since PFs are greater than 0.9 at half load. Moreover, THD_I performance of the TPIMI (14.1%) is also better than the performance of SPMI (17.8%) by means of ripple cancellation due to 180° phase shifted switching which also reduces the required filter parameters. As in simulation results, the MPPT performances are the same since the same algorithms are used. Since, the percentage input voltage ripple of the SPMI is measured to be 6.10%, it is measured as 5.83% for TPIMI which is a better performance.

According to the calculated, simulated and experimental results, the benefits of interleaving are verified while the efficiency, PF, THD and decoupling performances of the SPMI are improved due to current sharing which reduces peak and RMS currents as well as current stresses and losses on the semiconductors providing the MI to operate higher power ratings with lower cost. While the euro efficiency is improved by 2.52%, maximum efficiency is improved by 4.22% which contributes to increase the profit and reduce the payback period of the system.

While two-phase interleaved flyback-based MI is superior to the single-phase MI, for a residential PV system, interleaving technique will be more suitable and the profit will be rather increased. Improving the efficiency and THD_I performances of both topologies can be defined as the most important future works of this study. Moreover, a PCB design will make the inverters more modular and the power density will be improved as well. By means of an active clamp soft switching technique the efficiencies of the topologies can be further improved.

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