F-L-N PARAMETER BASED POWER DENSITY OPTIMIZED DESIGN AND IMPLEMENTATION OF A DIGITALLY CONTROLLED 1-kW INTERLEAVED DC-DC STEP DOWN CONVERTER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

İLKER ŞAHİN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2014

Approval of the thesis:

F-L-N PARAMETER BASED POWER DENSITY OPTIMIZED DESIGN AND IMPLEMENTATION OF A DIGITALLY CONTROLLED 1-kW INTERLEAVED DC-DC STEP DOWN CONVERTER

submitted by **İLKER ŞAHİN** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. Gönül Turhan Sayan _____
Head of Department, **Electrical and Electronics Engineering**

Assoc. Prof. Dr. Ahmet M. Hava _____
Supervisor, **Electrical and Electronics Engineering Dept., METU**

Examining Committee Members:

Prof. Dr. Muammer Ermiş _____
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Ahmet M. Hava _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. A. Nezih Güven _____
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Umut ORGUNER _____
Electrical and Electronics Engineering Dept., METU

Eyyup Demirkutlu M.Sc. _____
GÜÇELSAN Elektrik Elektronik San. Ltd. Şti.

Date: 07/02/2014

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : İlker Şahin

Signature :

ABSTRACT

F-L-N PARAMETER BASED POWER DENSITY OPTIMIZED DESIGN AND IMPLEMENTATION OF A DIGITALLY CONTROLLED 1-kW INTERLEAVED DC-DC STEP DOWN CONVERTER

Şahin, İlker

M.Sc., Department of Electrical and Electronics Engineering

Supervisor : Assoc. Prof. Dr. Ahmet M. Hava

February 2014, 163 Pages

In power electronic conversion, interleaving technique, which can be considered as a special form of paralleling, is a widely utilized method due to the size and performance benefits it introduces. This thesis first compares interleaving to other forms of paralleling techniques and investigates the interleaving technique from both electrical (output voltage ripple, line current distortion, efficiency etc.) and physical (converter size, cost etc.) characteristics points of view. After the detailed description of interleaving, the subject of optimal converter design is stressed: by a careful selection of design parameters such as switching frequency (f), inductance (L) and phase number (N) optimum design points can be found. By means of a MATLAB code which calculates and reports converter efficiency, volume and cost

for various f-L-N values, optimum design points targeting maximum efficiency, minimum volume, and maximum figure of merit which corresponds to smaller volume and higher efficiency together, are suggested for a 1-kW buck converter.

For the physical demonstration of the benefits introduced by interleaving and to test the results of f-L-N based converter optimization, a 1-kW digitally controlled hard switched multi-phase buck converter is designed and implemented. Along the theoretical analyses and computer simulations, detailed laboratory tests are carried out and correlation of analysis, simulation, and implementation results are provided.

Keywords: Interleaving, Multi-Phase Converters, DC-DC Converter Optimization, Efficiency Analysis, Volume Analysis, Inductor Design

ÖZ

YÜKSEK GÜÇ YOĞUNLUĞU İÇİN F-L-N DEĞERLERİ ENİYİLENMİŞ SAYISAL DENETİMLİ 1-kW İNDİRİCİ DC-DC DÖNÜŞTÜRÜCÜ TASARIM VE GERÇEKLENMESİ

Şahin, İlker
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Doç. Dr. Ahmet M. HAVA

Şubat 2014, 163 Sayfa

Güç elektroniğinde, paralelleme yöntemlerinin özel bir çeşidi sayılabilecek olan faz kaydırmalı modül paralelleme tekniği (FKMP), sunmuş olduğu boyut ve başarım getirileri nedeni ile sıkça uygulanmaktadır. Bu tezde, önce FKMP tekniği diğer paralelleme çeşitleriyle karşılaştırılıp elektriksel (çıkış gerilim kıpırtısı, giriş akım bozunumu, verim vb.) ve fiziksel (dönüştürücü büyüklüğü, maliyet vb.) özellikleri bakımından incelenmektedir. FKMP tekniğinin ayrıntılı sunumunun ardından, en iyi dönüştürücü tasarım çalışması üzerinde durulmuştur: anahtarlama frekansı (f), endüktans (L) ve faz sayısı (N) değerlerinin dikkatli seçimiyle en iyi tasarım noktaları bulunabilir. 1-kW'lık indirici tipte bir dönüştürücü için, değişken f-L-N değerlerine göre verim, hacim ve maliyet analizleri yapıp raporlayan bir MATLAB

programı üzerinden, en yüksek verim, en düşük hacim ve yüksek verim ile düşük hacmi beraber değerlendirmek üzere tanımlanmış başarım ölçüsünün ençoklanmasını amaçlayan eniyilenmiş tasarım noktaları sunulmaktadır.

FKMP yönteminin getirilerinin fiziksel gösterimi ve f-L-N temelli dönüştürücü eniyilenmesi çalışmasının sonuçlarının sınanması için 1-kW sayısal denetimli katı anahtarlamalı çok fazlı bir indirici dönüştürücü tasarlanıp gerçeklenmiştir. Kavramsal incelemelerin ve bilgisayar benzetimlerinin yanı sıra ayrıntılı laboratuvar testleri yürütülmüş ve inceleme, benzetim ve laboratuvar çalışmaları arasındaki uyum doğrulanmıştır.

Anahtar Kelimeler: Faz Kaydırmalı Modül Paralelleme, Çok Fazlı Dönüştürücüler, DA-DA Dönüştürücü Optimizasyonu, Verim Analizleri, Hacim Analizleri, Endüktör Tasarımı

To My Family

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Assoc. Prof. Dr. Ahmet M. Hava for his support, encouragement, guidance and critiques on this study throughout my graduate education.

I express my deepest gratitude to my family for their patience and support throughout my life. Without their encouragement, I would not be able to finish this work.

I want to acknowledge thanks to my friends Ziya Özkan and Semih Kavurucu for their help and support. I also would like to thank Eyyup Demirkutlu for his technical and sincere support.

I wish to thank to Middle East Technical University Department of Electrical and Electronics Engineering faculty and staff for their help throughout my graduate studies.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Effective Series Resistance
GaN	Gallium Nitride
GTO	Gate Turn-Off Thyristor
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PFC	Power Factor Correction
PWM	Pulse Width Modulation
RMS	Root Mean Square
SCR	Silicon Controlled Rectifier
SiC	Silicon Carbide
SMPS	Switch-Mode Power Supply
ZVZCS	Zero-Voltage and Zero-Current Switching

CHAPTER 1

INTRODUCTION

1.1 An Introductory Overview of Switch Mode Power Supplies

The inventions in the semiconductor technology such as silicon controlled rectifiers (SCR) in 1957, gate turn-off thyristors (GTO) in 1967 and power bi-polar junction transistors (BJT) in 1970, gave rise to the electronic power conversion. With the development of power metal oxide field effect transistors (MOSFET) and Schottky diodes in late 1970s, the discipline of power electronics matured and recorded a continuous development thus far. In recent years, need for highly efficient power converters rises and the market for power electronics seem to grow.

As a sub-discipline of power electronics, switch mode power supply (SMPS) design mainly deals with AC-DC and DC-DC conversion. Basic power conversion topologies are listed in Figure 1.1.

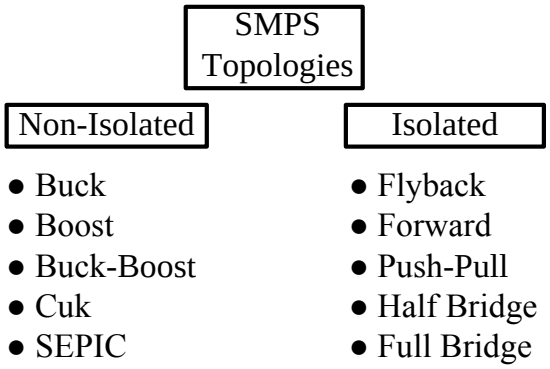


Figure 1.1 A list of basic SMPS topologies.

Although the topologies that are listed in Figure 1.1 form a short list, there are numerous variations of these basic topologies. For example, by employing soft switching, which mainly depends on creating a resonance in the converter that allows zero voltage or zero current situations at the switching instant, to the basic topologies listed in Figure 1.1, a great number of new topologies can be achieved. Similarly, with some small structural changes, new variations of basic topologies can be offered such as two switch forward or synchronous buck converter topologies to name a few. Detailed information on SMPS topologies is provided in [1] and [2]. With different input / output characteristics and performance figures, an SMPS topology is selected considering the application area that it is going to be used at. In this study, buck converter, a simplified illustration of which is depicted in Figure 1.2, is stressed.

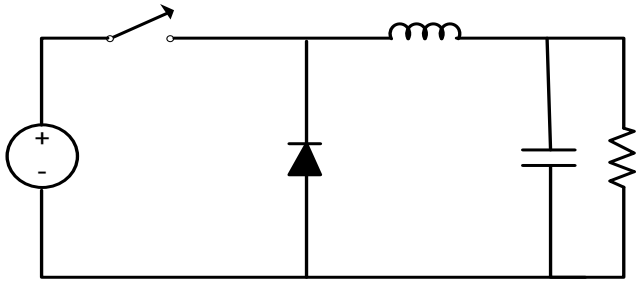


Figure 1.2 A simplified illustration of the buck converter topology.

Today, studies continue for higher performance power converters in several application areas. One of the main research trends in SMPS is the design of high efficiency, small volume voltage regulation modules for new microprocessor generations. Combining the increase in number of transistors per die which is depicted in Figure 1.3 with the supply voltages being decreased, modern microprocessors require low voltage high current DC-DC converters which are also

supposed to meet stringent output voltage ripple and very fast transient response regulations in a very small volume.

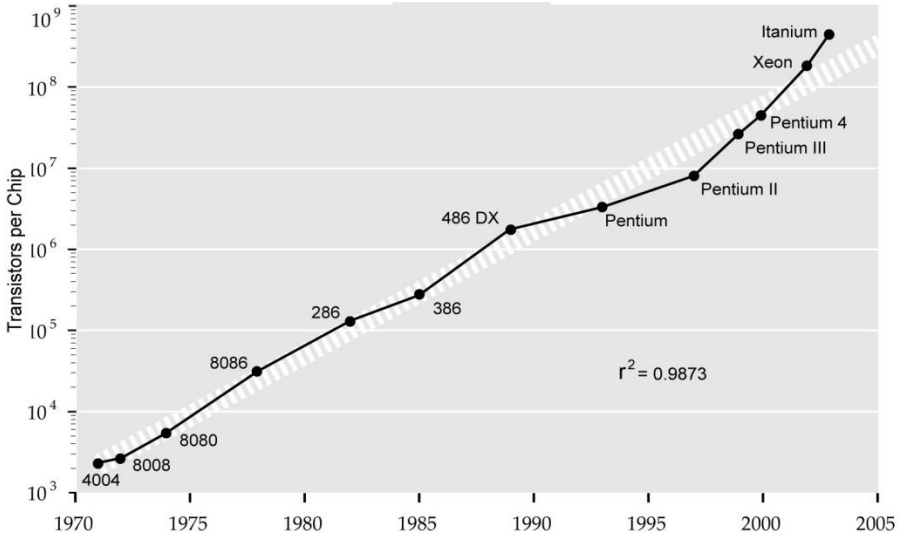


Figure 1.3 Number of transistors in microprocessors [3].

Another main research area in SMPS is the AC-DC conversion by the utilization of PWM rectifiers. Conventional diode bridge rectifiers pollute the grid that they are connected to and are bulky converters due to the low frequency passive components required. Rapid developments in IT technologies and the trend for more-electric aircraft in aerospace applications make the demand for active PFC applications increase. Improving semiconductor technology raises the power limit up to which active PFC is feasible therefore same trend of replacing diode rectifiers is also seen in high power industrial applications.

Depletion of fossil fuels and environmental concerns not only boosts the utilization of clean energy such as solar and wind, but also promotes the use of electric vehicles (EV). EVs require both DC-DC and DC-AC conversion for their operation as depicted in Figure 1.4. As the battery and material technology evolves, EVs are

continuously being developed in key figures of merit such as range and power thus becoming a stronger alternative for internal combustion engine vehicles.

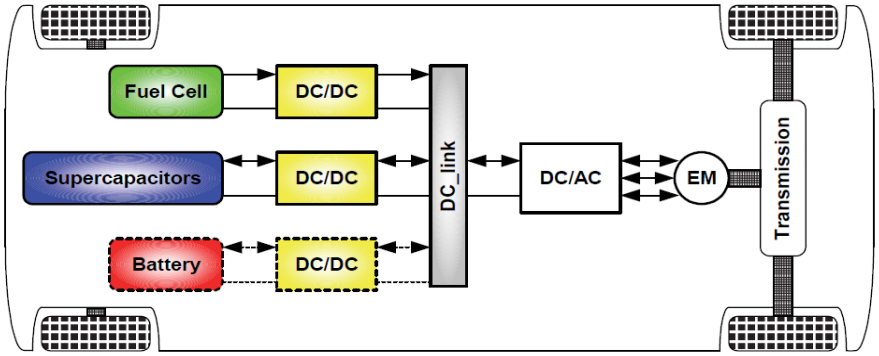


Figure 1.4 Electric vehicle drive system [4].

Regardless of the type of application, all modern power electronic converters are supposed to meet the electrical input/output criteria set for their operation with the minimum volume and cost possible. Efficiency is a major concern for all converters; both rated load efficiency and entire load range efficiency are tried to be set as high as possible due to the economic and environmental interests. These situations altogether constitute a challenge for designers and promote the research on new conversion topologies, superior materials and advanced production techniques (packaging, layout etc.). Table 1.1 is created to summarize important properties of five reference designs and to illustrate the current level of power conversion technology.

Table 1.1 Important parameters of selected high efficiency, high power density, state of the art converters.

	[5]	[6]	[7]	[8]	[9]
Application Area	VRM	Automotive DC-DC	AC-DC-AC	PWM Rectifier	Telecom Supply
Year of Manufacture	2012	2008	2010	2007	2008
Topology	Resonant Converter with GaN Switches	ZVZCS Boost	Vienna Rectifier + 2 level VSI	Vienna Rectifier	Series Parallel Resonant
Cooling Method	Natural Convection	Liquid	Forced Air	Liquid	Natural Convection
Input/Output (V/V)	48/12	150/300	N.A	400/800	400/48..54
Frequency (kHz)	1600	200	70	400	135
Power (kW)	0,36	8,4	10	10	5
Rated Efficiency (%)	95	94	95	96	96
Volume (cm^3)	22	541	3300	1000	263
Power Density (W/cm^3)	16.38	15.50	3.03	10.00	19.10

1.2 Interleaving as a Performance Enhancing Technique and Its Applications

Interleaving technique is simply implementing a power converter such that it is made of paralleled, identical phases with their switching patterns phase shifted in

time. Interleaving is a widespread technique which is not limited to power electronic applications: a conventional internal combustion engine with its cylinders being fired sequentially is a good example of interleaving. In terminology, other expressions for interleaving such as “multi-phase conversion”, “phase shifted parallel” or “phase staggering” exist, yet in this study the technique will be addressed as “interleaving”. A simplified circuit diagram for an interleaved buck converter is depicted in Figure 1.5.

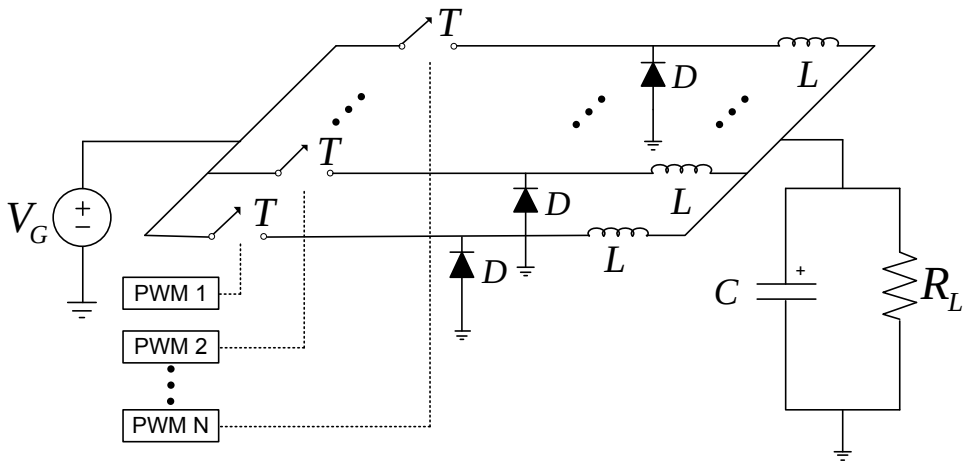


Figure 1.5 “N” phase, interleaved buck converter.

Due to the benefits introduced by interleaving, the technique is intensively applied and thoroughly studied. In the early periods of power electronics, interleaving was applied mainly as a means of obtaining higher power ratings since paralleling is the fundamental solution for higher power. With the evolution of semiconductor switches, interest in interleaving did not decrease. In contrary, interleaving is the favored technique for the areas mentioned in Chapter 1.1, namely voltage regulation modules for microprocessor supplies [10]-[13], PWM PFC [14]-[17] and automotive applications [18]-[21]. Performance enhancements brought by interleaving are investigated in [17] and [22].

1.3 The Need for Converter Optimization

Modern power converters are expected to have high efficiency and high power density while accomplishing stringent criteria set for electrical performance (low ripple, low noise, fast dynamic response etc.). For a commercial converter, robustness, reliability and cost are also very fundamental design aspects that cannot be overlooked. A designer must carefully select proper topology, mode of operation, switching frequency, cost effective electrical components (semiconductor switches, inductors and capacitors) which vary in price, volume and material that they are made of, while maintaining aforementioned indicators of quality. Therefore, converter design is a multi-dimensional problem, every element of which is affected by the change in the other elements.

Once the topology and mode of operation are selected for a specific application, there are several decision points most of which are also dependent on each other. All of converter's subsystems and components should be considered and evaluated in view of the design criteria set for the converter, as depicted conceptually in Figure 1.6. Taking the design process of a buck converter as an example, it is often left to the designer's previous experience or widely accepted norms to decide on the selection of switching frequency (f) and inductance value (L). However, such an approach will most likely yield a result worse than the optimum solution: it is beneficial to consider most, if not all, possible choices of design parameters for an optimized solution. A simplified diagram that shows the efficiency and power density based design process of a buck converter is depicted in Figure 1.7. In Figure 1.7, arrows represent dependence, if there is a direct proportionality in the magnitudes of two variables (for example: magnitude of loss and total volume of heat sink required) arrow is red, if there is an inverse proportionality in the magnitudes of two variables (for example: switching frequency and inductance value) arrow is blue.

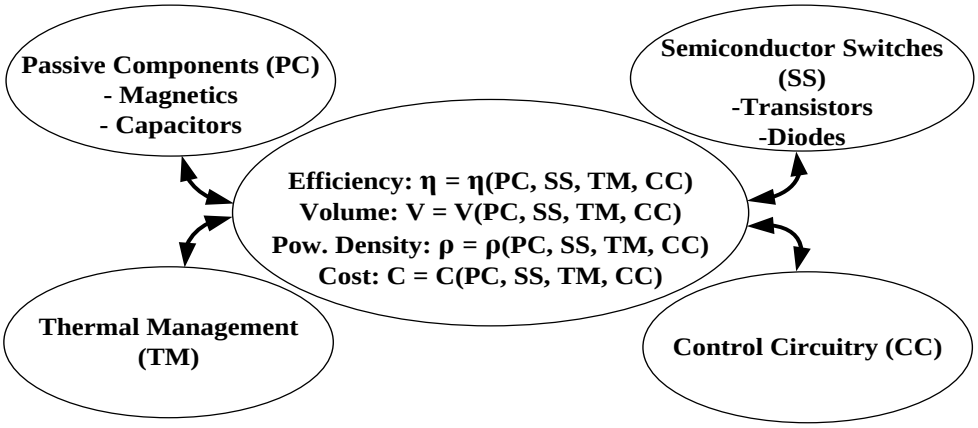


Figure 1.6 Conceptual power electronic converter design diagram showing the interdependency of design parameters.

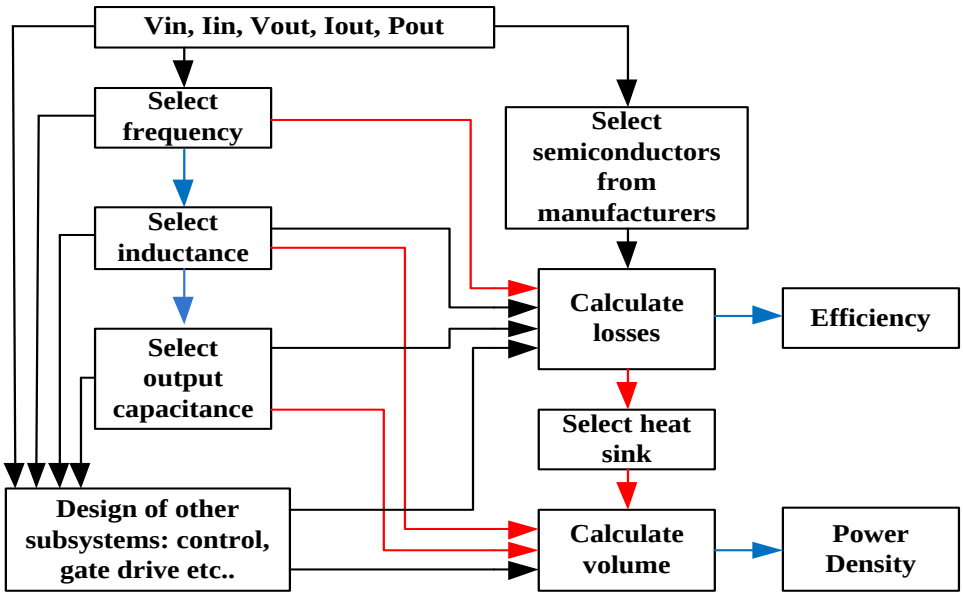


Figure 1.7 A simplified diagram that shows the efficiency and power density based design process of a buck converter.

There has been an intensive study on power converter optimization to obtain higher power density values. In [23] and [24] different optimization techniques and their

effectiveness are discussed. 2 MHz buck and 1.6 MHz ZVZCS inductorless full-bridge converter topologies utilizing GaN switches are designed and optimized for higher power density in [5]. A snubber assisted ZVZCS converter based on boost topology is designed and optimized for automotive applications with high power density and efficiency is presented in [6]. An efficient and low volume solution for AC-DC-AC conversion utilizing SiC devices is studied in [7]. Kolar et al. introduces optimized, highly efficient and high power density converters for unity power rectification [8], telecom [9] and automotive [20] applications. Similar studies exist for flyback converters [25], boost converters for aerospace applications [26] and MHz range on chip buck converters [27].

1.4 Scope of the Thesis

Main objective of this study is to design and implement a digitally controlled 1-kW DC-DC power converter exhibiting high efficiency in small volume. Targeting high efficiency and low volume requires optimization and obtaining an overall picture of converter behavior with respect to parameters such as switching frequency and inductance being changed. Since interleaving is a valuable technique which is widely utilized, special emphasis is put on interleaving thoroughly defining its benefits.

This dissertation consists of five chapters. First chapter introduces a summary of current studies in SMPS and addresses the importance of power converter optimization for the achievement of high efficiency - small volume converter design. A short introduction to interleaving is also provided since it is a major technique which provides superior electrical performance and stands as a candidate in the pursuit of higher power density.

Chapter 2 examines interleaving and compares it to other forms of paralleling such as device or converter paralleling. Detailed mathematical expressions are provided for a thorough examination of the technique.

Chapter 3 deals with the optimization of the target converter. Since converter optimization is a multi-dimensional and application specific process, approach for optimization and models to be used in the process are described first. Then, the MATLAB code written for the analyses on the efficiency and volume of the target converter is presented and its outputs are discussed.

Chapter 4 includes the design and implementation process of a 1-kW, hard switched, multi-phase, CCM buck converter. An additional 500W, two-phase converter is also implemented as a preparatory step and several variations of the optimal design are also provided. Detailed laboratory results and performance analyses of the designed converters are introduced. Comparison of theoretical and practical results is presented. The proposed converter is also compared to other non-optimal designs.

Finally, the dissertation concludes with a summary of information and experience obtained during the study. Developments and future work are also suggested.

CHAPTER 2

INTERLEAVING AND OTHER PARALLELING SCHEMES IN GENERAL

Paralleling of components or modules being common in power electronics, this chapter includes a detailed investigation of paralleling techniques with special emphasis on interleaving. Firstly, a general overview on paralleling schemes is presented. Interleaving technique, a brief definition on and application areas of which have been introduced in Chapter 1, brings many benefits to the converter that it is applied to, such as current and voltage ripple reduction at input and output, passive component scaling to name a few. Interleaving will be described through mathematical expressions and its benefits will be documented. Finally, further applications related to interleaving such as dynamic number of phases and utilization coupled inductors will be discussed.

2.1 An Overview on Paralleling Schemes

2.1.1 Component Paralleling

Component paralleling is mainly applied to satisfy the current rating required if the single component cannot meet the desired current rating. One simple example is the paralleling of inductors for higher current which is depicted in Figure 2.1. In such a case, current capacity of the inductor network is “N” times increased where “N” is the number of paralleled devices yet the effective inductance of the inductor network is reduced to L/N. If the inductance value of the paralleled scheme is desired to be kept as “L”, paralleled inductors should be selected N times higher. Effective series resistances (ESRs) of the inductors are also paralleled yielding a smaller ESR value of Ron/N, which reduces conduction losses.

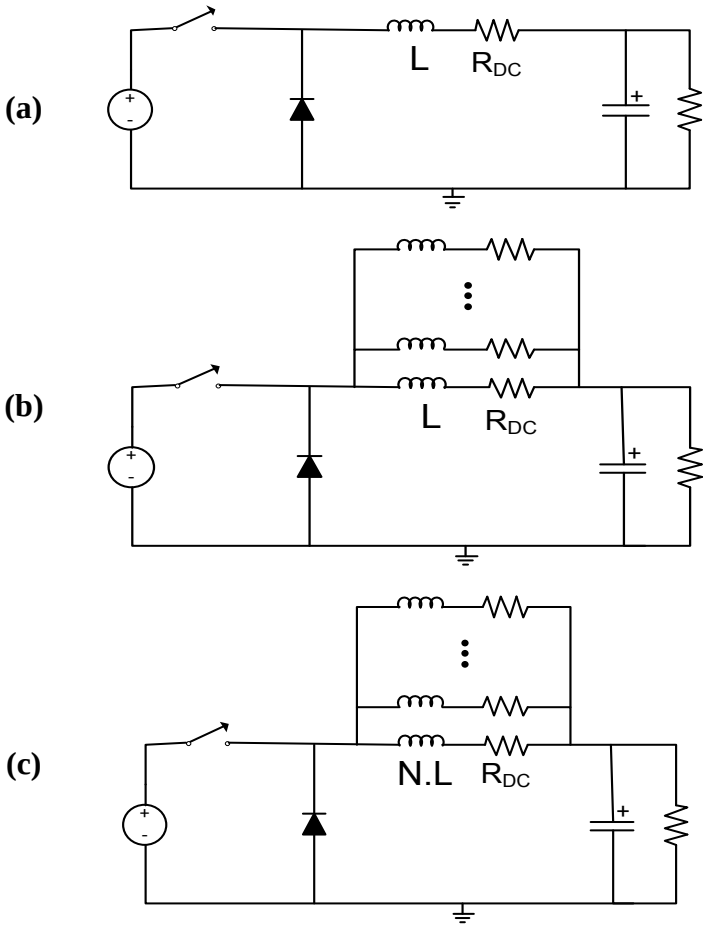


Figure 2.1 Buck converter utilizing single inductor (a) and paralleled inductors with inductance value "L" (b) and "N.L" (c).

Paralleling of capacitors is also widely utilized to reach higher capacitance value with lower ESR. Figure 2.2 illustrates the equivalent circuit diagrams of a non-ideal capacitor. Due to the effective series leakage inductance and effective series resistance, capacitor performance for high frequencies is seriously worsened as depicted in Figure 2.3.

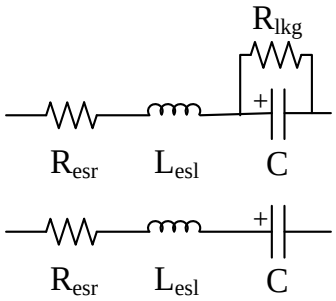


Figure 2.2 Equivalent circuit diagrams of a non-ideal capacitor.

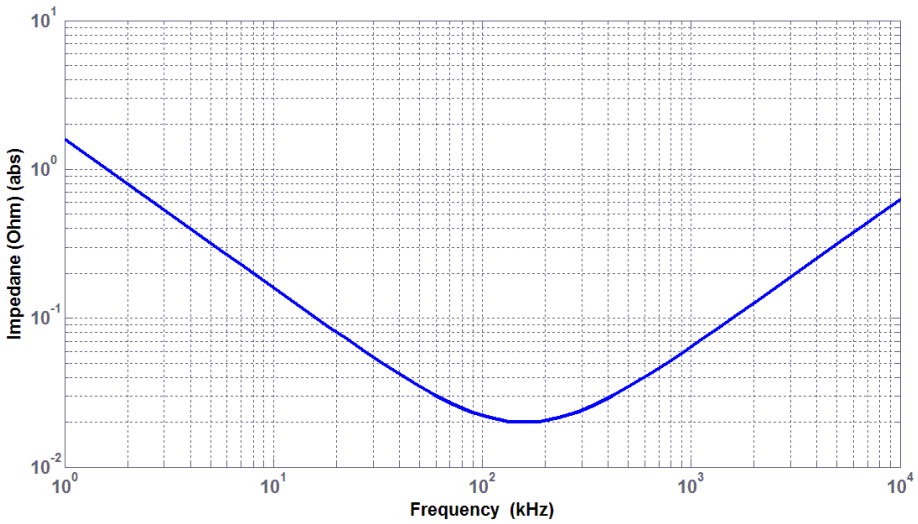


Figure 2.3 Impedance versus frequency graph for a real capacitor which has 100 µF capacitance, 20 mΩ ESR and 10 nH ESL.

For an increased capacitance value with lower ESR and ESL values, it is beneficial to parallel capacitors. An illustration for capacitor paralleling is given in Figure 2.4.

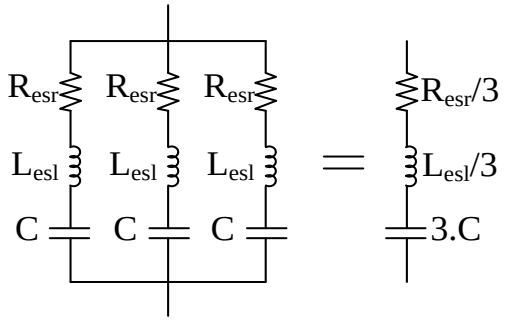


Figure 2.4 Paralleling capacitors for higher capacitance with lower ESR and ESL.

Passive components aside, paralleling of active components such as MOSFETs or IGBTs are also commonly practiced. Being more complex devices, paralleling of active components requires caution.

2.1.1.1 MOSFET Paralleling

MOSFETs can be paralleled if the current rating of the single MOSFET is not enough to meet the current rating dictated by the application. It is also possible to use MOSFETs in parallel to reduce conduction losses by reducing the effective on resistance considering that conduction losses are dominant for most of the applications which utilize MOSFETs, which are known for their fast switching behavior.

MOSFET properties represented in datasheets such as on resistance, trans-conductance and threshold voltage are not strictly precise values; they are best defined within a range. Therefore, for practical semiconductor switches, mismatches in such semiconductor device properties should be expected. These discrepancies can lead to current imbalance during both switching instant and steady state.

Main reason making MOSFETs popular for paralleled use is their positive temperature coefficient property. Being positive temperature coefficient devices, the on-resistance of a MOSFET increases with increasing temperature. Thus, if one device out of many paralleled MOSFETs tends to carry a larger portion of current

which creates temperature rise due to the increasing losses, on resistance of that MOSFET increases which in turn limits the current carried by it. Therefore, thermal runaway is not a big threat for paralleled MOSFETs.

Detailed examination on semiconductor mechanisms describing the causes and results of the device parameter mismatch is beyond the scope of this study. However, some general guidelines and precautions are listed below for a successful parallel operation of MOSFETs. Further explanations and application notes are reported in the literature [28-30]

- Although a higher current rating is obtained with the paralleling of MOSFETs, total current passing thorough the paralleled network should not exceed 70-80% percent of the total current rating. In other words, a safety margin for current should be utilized.
- The resultant paralleled network of MOSFETs should be tested and observed for mismatch and excessive heat spots should be determined if there is any.
- Proper and symmetrical layout of the devices should be utilized. Decreasing the value of stray inductances and MOSFETs having close if not same stray inductance are crucial for successful switching performance.
- Each paralleled MOSFET should have its own gate resistor to avoid parasitic oscillations.
- Utilizing ferrite beads, which act as a frequency dependent resistance, at gate drive circuitry is also advised to eliminate gate ringing.

Illustration of a paralleled MOSFET scheme is depicted in Figure 2.5.

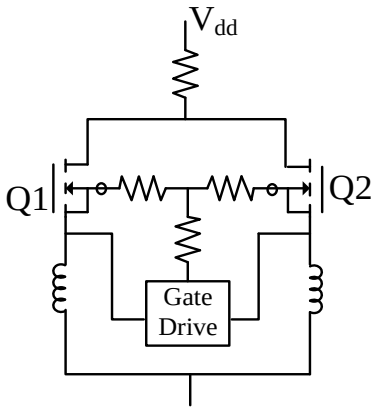


Figure 2.5 Paralleling of MOSFETs with individual gate resistors and ferrite beads.

2.1.1.2 IGBT Paralleling

With power ratings expected from power electronics converters increase, paralleling of IGBTs is also practiced mainly in high power inverter applications. Guidelines for MOSFET paralleling also applies to IGBT paralleling. However, one significant difference between MOSFETs and IGBTs from paralleling point of view is that unlike MOSFETs, IGBTs are negative temperature devices; on resistance drops with increasing temperature therefore the paralleled network of IGBTs is prone to a thermal runaway which can easily cause a permanent damage to the semiconductor devices if the effective counter-measures are not taken. Mounting paralleled semiconductor switches to the same heat sink thus decreasing thermal differences is common in both MOSFET and IGBT paralleling but more crucial for the IGBT case. Further notes and techniques are reported in the literature [31-33]. Reliability issues concerning the parallel operation of power semiconductor switches in general are discussed in [34].

2.1.2 Power Stage Paralleling

Considering a buck converter, it can be said that power stage consists of a transistor (a MOSFET for most of the applications), a diode (another MOSFET if synchronous rectification is applied) and an inductor. This L-T-D (inductor, transistor and diode)

structure can also be paralleled for higher current capability as depicted in Figure 2.6.

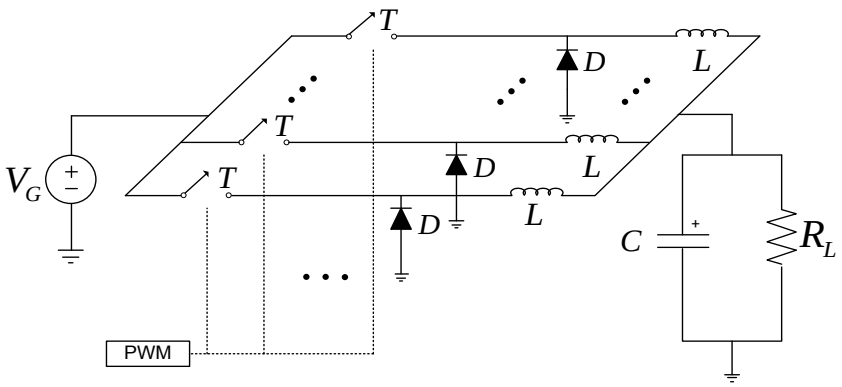


Figure 2.6 Power stage paralleling.

This paralleling scheme has the exact same structure with interleaving with the only difference in the switching pattern of transistors: power stage paralleling pattern utilizes a single PWM source for all of the paralleled stages on the other hand interleaved conversion requires discrete PWM sources for each individual stage which are phase shifted in time. However this single difference creates a serious drawback for power stage paralleling case; current ripples in each phase will add up and result in a much greater current ripple at the output requiring N times more capacitance at the output (where N is the number of paralleled power stages) compared to the single-phase structure as depicted in Figure 2.7. Since this kind of a paralleling approach inherently brings interleaving with only phase shifted PWM signals are to be created, power stage paralleling is not a common technique in power electronic conversion.

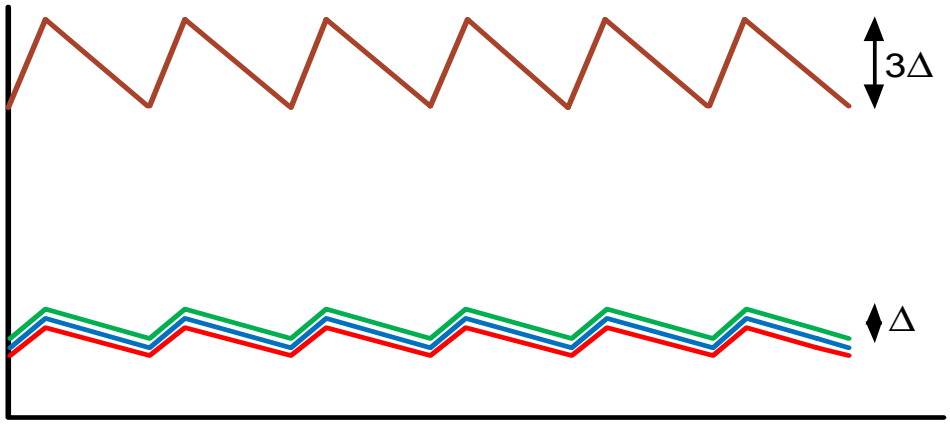


Figure 2.7 Phase currents and their sum for power stage paralleling for the case of three paralleled stages.

2.1.3 Converter Paralleling

Modern commercial power converters are often produced with parallel operation capability. For a converter to have the ability of working in parallel with other converters, a means of communication with other converters and a control scheme utilizing current sharing is a must for reliable operation [35]. An investigation of current control methods for parallel operation of power converters is presented in [36]. If the paralleled converters do not have the ability of active current sharing, a configuration like the one depicted in Figure 2.8 can be applied with additional components such as diodes, fuse or relays. However, overall current capability of paralleled converters should be seriously degraded because overloading of a converter may occur without the presence of active current sharing.

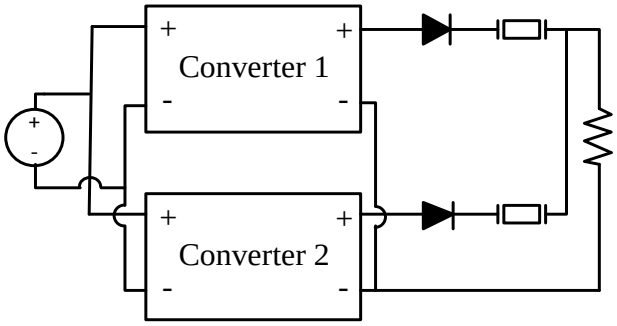


Figure 2.8 Parallel operation of power converters with the utilization of diodes and fuses.

2.2 Interleaving

An interleaved converter consists of paralleled power stages that are driven by phase shifted PWM signals. Phase shift between each consecutive power stage is $2\pi/N$ where N is the number of paralleled power stages. Interleaving offers many advantages to the converter that it is applied to; current and voltage ripple reduction, higher power density due to the reduced volume of passive components to name a few.

2.2.1 Current Ripple Reduction at Input / Output

Considering the inductor currents which add up at the positive terminal of the output capacitor of a buck converter, one can easily understand that phase shifting of the paralleled power stages provides ripple reduction as depicted in Figure 2.9 which illustrates phase currents and their sum for an interleaved, three-phase (N=3) buck converter example that was assumed to operate with a duty cycle of 0.75 (D=0.75). Summation of phase shifted currents (which will be addressed as "total current" to avoid confusion with load current) each of which has peak to peak current ripple of 3Δ results in a current waveform with a peak to peak ripple of Δ.

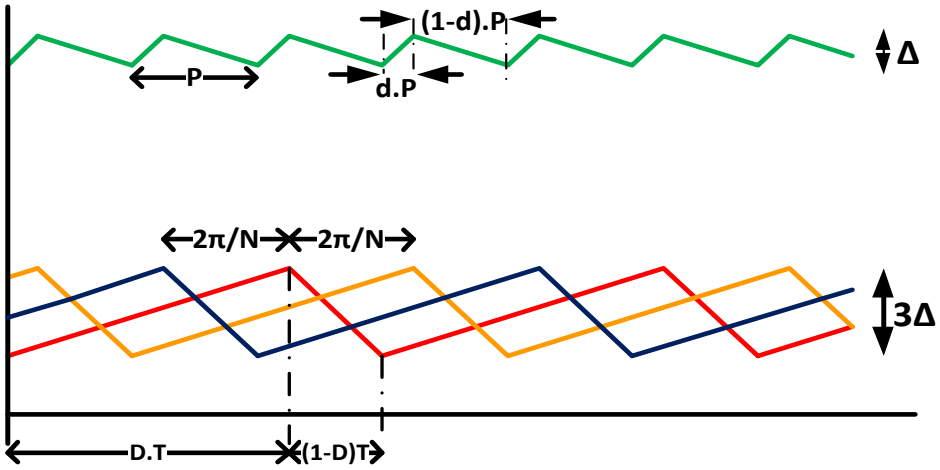


Figure 2.9 Phase currents and their sum for an interleaved buck converter with N=3 and D=0.75.

Another property of interleaving which can be named as “frequency multiplication” can be observed by examining the current waveforms depicted in Figure 2.8. The frequency of the ripple on the total current is N times higher than that of individual phase currents. Denoting the period of the total current waveform with “P” and phase current with “T”, frequency multiplication is expressed in (2.1). Considering that filtering higher frequency ripples is easier, “frequency multiplication” is another benefit introduced by interleaving.

$$P = \frac{T}{N} \tag{2.1}$$

The amount of reduction in the ripple of the total current is a function of N and D. Although reduction in the ripple observed on total current is guaranteed in an interleaved converter, an expression clearly stating current ripple for given N and D is required for a proper interleaved converter design. With further examination of the current waveforms depicted in Figure 2.8 and through mathematical derivations (2.3)-(2.13), an expression for current ripple of interleaved CCM buck converters is formulated.

Similar to a single-phase buck converter inductor current rising in the time interval D.T, and falling in (1-D).T, total current in the interleaved converter rises in d.P and falls in (1-d).P time intervals. Here, a fictitious duty cycle is defined for total current waveform and denoted by "d". Having in mind that the output voltage expressions for both interleaved and single-phase cases are the same (2.2) and a function of D only, it should be stated that the fictitious duty cycle d is not an output voltage describing parameter. In (2.2), V_G and V_O stand for average input and output voltage of a buck converter respectively. As Figure 2.8 shows, d turns out to be 0.25 for the N=3 and D=0.75 case.

$$V_O = D.V_G \tag{2.2}$$

The expression for the peak to peak inductor current ripple of a single-phase buck converter (which also applies for each individual phase of an interleaved buck converter) is given in (2.3). By the division of peak to peak current ripple by the rise and fall times, rising slopes and falling slopes for inductor current (denoted as RS and FS respectively) can be obtained as illustrated in (2.4) and (2.5).

$$\Delta I = \frac{(V_G - V_O)D}{f.L} = \frac{V_G(1-D)D}{f.L} \tag{2.3}$$

$$RS = \frac{V_G(1-D)}{L} \tag{2.4}$$

$$FS = \frac{V_G.D}{L} \tag{2.5}$$

The number of active stages that are the stages their high side switches conducting, during the current rise (d.P) interval will be denoted as "x". Considering that current rise interval starts with the transition of passive stage to active, any arbitrary time instant which the current starts to rise can be defined as t=0 and the power stage which is activated at t=0 can be named as Phase #1. Similarly, current rise interval ends with the transition of an active stage to passive. Having determined Phase #1, current fall interval starts with the transition of the most retarded phase among the

active stages, which turns out to be Phase #x. The time instant which Phase #x turned its high side switch on is:

$$t_x = -\frac{(x-1)T}{N} \tag{2.6}$$

Therefore, current rise interval can be expressed as:

$$(d.P) = D.T - \frac{(x-1)T}{N} \tag{2.7}$$

With the representation of current ripple as the multiplication of current rise time interval and summation of rising and falling slopes present at that interval, (2.8) can be written.

$$\Delta I = (d.P)(\Sigma(RS) - \Sigma(FS)) = (d.P)(x.RS - (N-x).FS) \tag{2.8}$$

Substituting (2.4), (2.5) and (2.7) into (2.8) with the rearrangement of the terms yields:

$$\Delta I = \frac{V_G}{f.L.N}(1 - (x - N.D))(x - N.D) \tag{2.9}$$

Next, an expression for "x" should be developed. If "x" out of N paralleled stages results in the rise of the total current:

$$|x.RS| > |(N-x).FS| \rightarrow x > N.D \tag{2.10}$$

Similarly, if "x-1" out of N paralleled stages being active results in the fall of the total current:

$$|(x-1).RS| < |(N+1-x).FS| \rightarrow x - 1 < N.D \tag{2.11}$$

Then, it can be said that "x" is the integer satisfying (2.12).

$$\frac{x-1}{N} < D < \frac{x}{N} \tag{2.12}$$

Considering the equations (2.9) and (2.12) together, it can be seen that the term (1-(x-N.D)) corresponds to the decimal part of N.D multiplication which is also equal to the fictitious duty cycle value of the total current denoted by "d". Therefore, if the operation of taking a number's decimal part is denoted by the notation $\lfloor k \rfloor$, where k is any number, equation (2.9) simplifies to:

$$d = \lfloor ND \rfloor \quad \rightarrow \quad \Delta I = \frac{V_G}{f.L.N}\, d.(1-d) \tag{2.13}$$

Equation (2.13) provides an elegant way of calculating the ripple in the total current of an interleaved buck converter. By using equation (2.13), current ripple versus duty cycle graph for various numbers of paralleled phases is created and depicted in Figure 2.10. ${}^{V_G}/_{f.L} = 1$ is assumed, therefore y axis of the current ripple graph of Figure 2.10 represents normalized values.

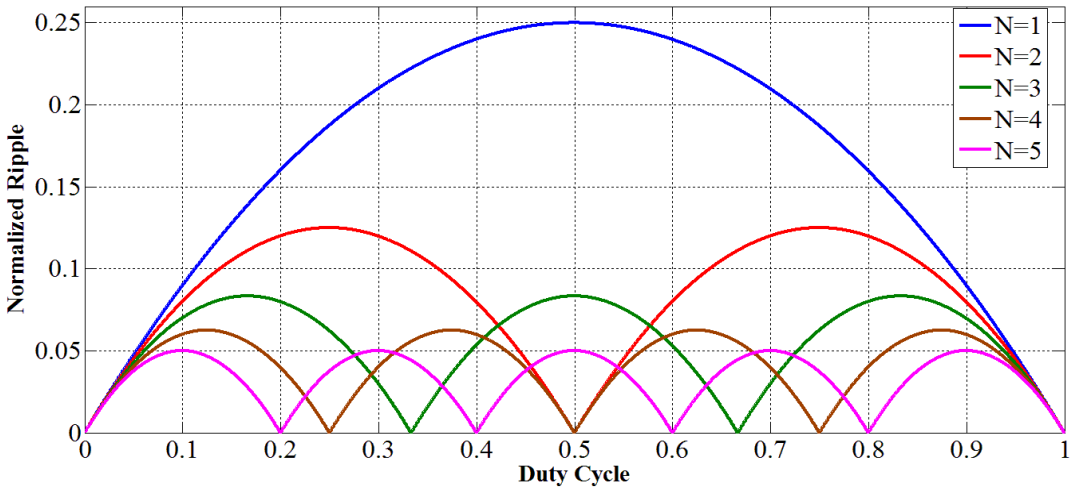


Figure 2.10 Buck converter peak to peak output current ripple versus duty cycle graph for various N values.

Another interesting feature of interleaving that can be observed from Figure 2.10 is that interleaving offers full ripple cancellation if N.D multiplication is an integer. As

an example, if an interleaved buck converter has four paralleled stages and operates with duty cycle D=0.25, total ripple cancellation occurs theoretically eliminating the need for output capacitors. Of course, in practical applications capacitors will be utilized at the output even if the total ripple cancellation is achieved since non-idealities in the converter will yield a small but nonzero ripple or the application may dictate the use of output capacitance due to the total hold up time requirement.

Examining the interleaved current ripple to single-phase current ripple ratio may better reflect the current ripple cancellation benefit which can be observed via Figure 2.11.

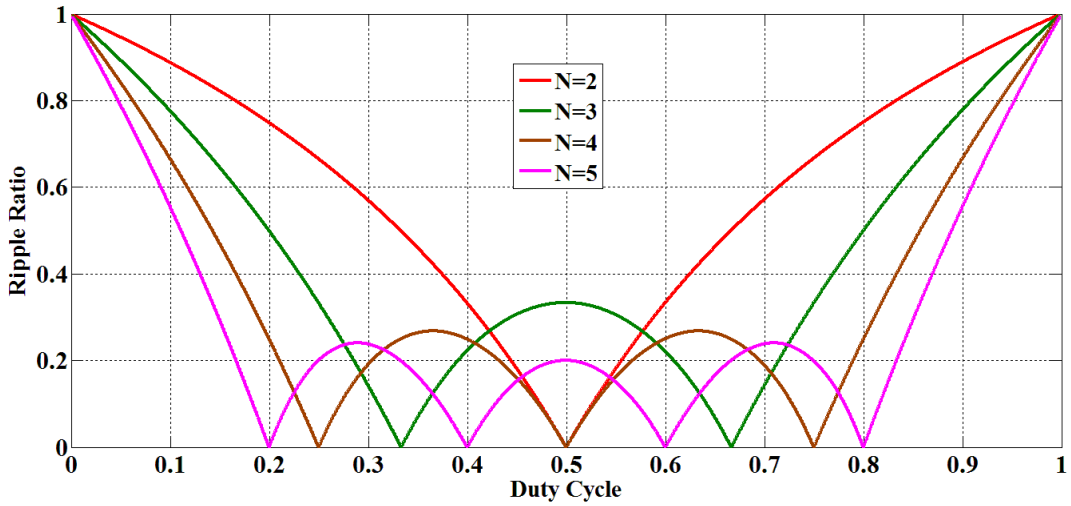


Figure 2.11 Interleaved output current ripple over single-phase structure current ripple ratio versus duty cycle graph for various N values.

Current ripple cancellation also occurs at the input of an interleaved buck converter. Considering the illustration for the input currents of interleaved and single-phase buck converters in Figure 2.12, it is seen that current drawn from the supply by the interleaved converter is of very less pulsating characteristics compared to that of a single-phase converter. Therefore, supply which is the interleaved buck converter is connected to, has been utilized smoothly. Since drawing current with a high peak

value to average value ratio from a practical power supply will result in input voltage fluctuations, this undesirable effect can be said to be lessened for an interleaved converter. Because of the discontinuous, pulsating characteristics of the input current waveforms of buck converters, a formula for input current ripple cancellation will not be provided here.

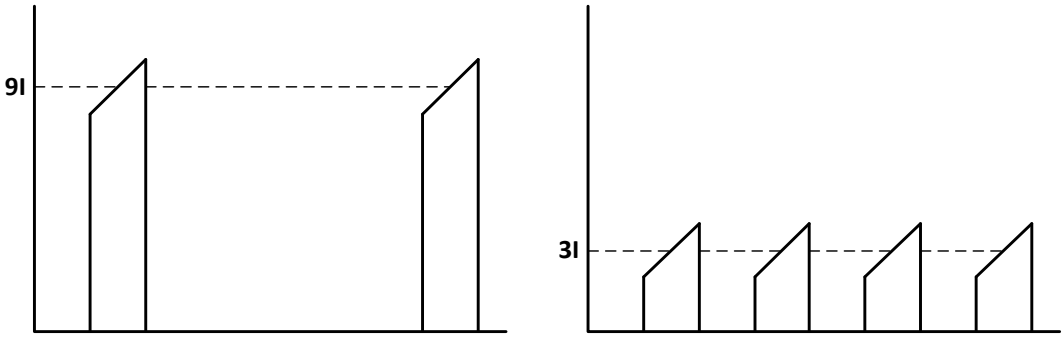


Figure 2.12 Input currents for a single-phase buck converter (left) and three-phase interleaved buck converter (right) with D=1/6.

By utilizing the duality property of buck and boost converters, similar analysis for interleaved current ripple can be carried out for the input current ripple of interleaved boost converters. Equations stated for peak to peak current ripple and rising / falling slopes introduced in (2.3), (2.4) and (2.5) respectively, can be modified for the boost converter as follows.

$$\Delta I = \frac{V_G . D}{f . L} \tag{2.14}$$

$$RS = \frac{V_G}{L} \tag{2.15}$$

$$FS = \frac{V_G . D}{L(1 - D)} \tag{2.16}$$

Definition of “x” and mathematical relation for it (2.12) are also the same for the boost converter case. Leaving the intermediate steps, input current ripple for an interleaved boost converter can be mathematically expressed as (2.17).

$$d = \lfloor ND \rfloor \quad \rightarrow \quad \Delta I = \frac{V_G}{f.L.N} \frac{d(1-d)}{(1-D)} \tag{2.17}$$

Normalized values of input current ripple versus varying duty cycle values drawn for various numbers of paralleled phases for the boost converter case is depicted in Figure 2.13. The interleaved current ripple to single-phase current ripple ratio graph is provided in Figure 2.14.

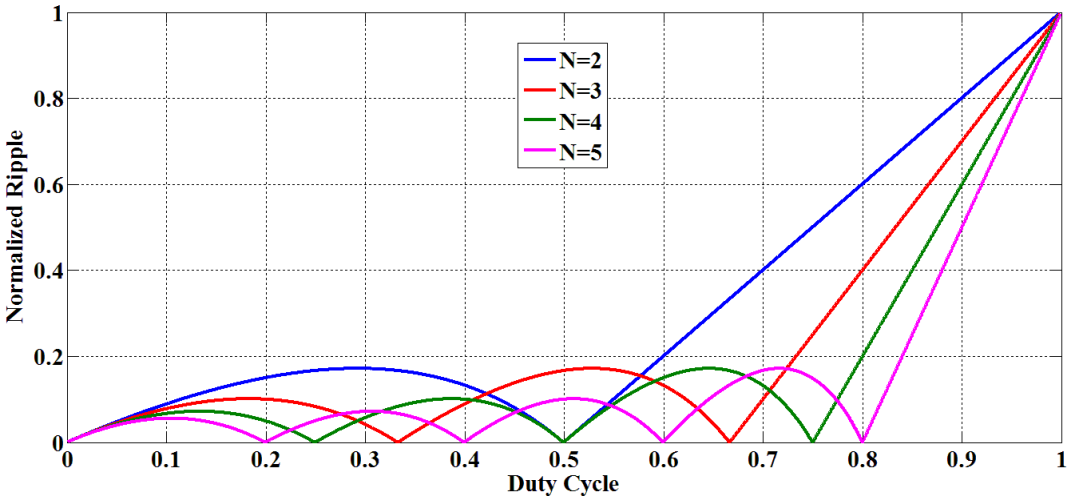


Figure 2.13 Boost converter peak to peak input current ripple versus duty cycle graph for various N values.

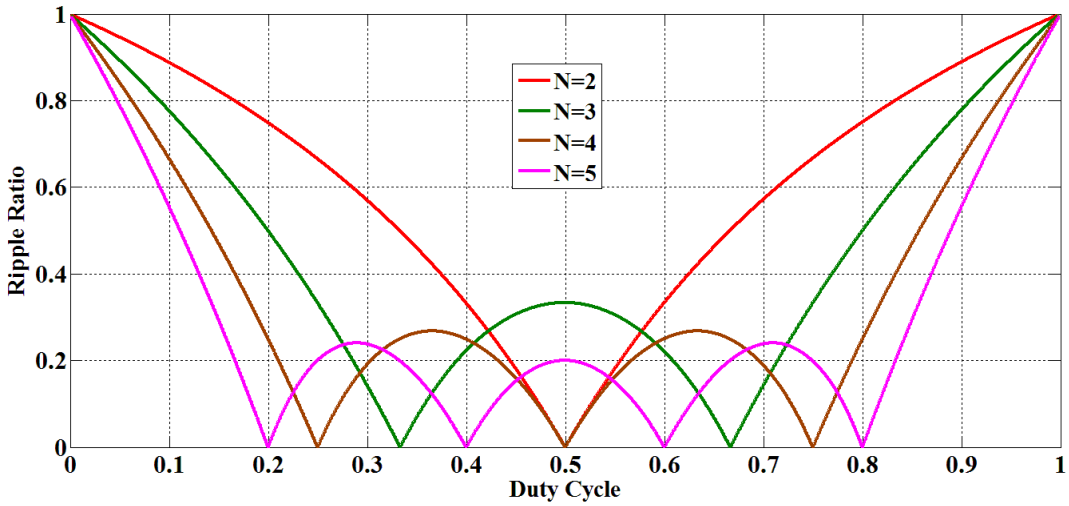


Figure 2.14 Peak to peak input current ripple compared to single-phase structure versus duty cycle graph for various N values.

A time-domain based analysis on current ripple reduction benefit of interleaving has been introduced thus far. Frequency-domain approach can also be adopted to explain the ripple reduction. Since, interleaved boost converters are commonly applied in PFC applications which set strict limitations on THD for the current drawn from supply, effect of interleaving on frequency domain characteristics will be examined on interleaved boost converters. Fourier synthesis and analysis equations are provided in (2.18) and (2.19).

$$x(t) = \sum_{n=-\infty}^{+\infty} a_n e^{jnwt} \tag{2.18}$$

$$a_n = \frac{1}{T}\int_0^T x(t)e^{-jnwt}dt \tag{2.19}$$

Assuming that paralleled phases are represented with "p" such that p ∈ (0, N-1) where p=0 denotes the first phase out of N paralleled phases and i(t) representing phase current for p=0, any phase current can be represented in time-domain as (2.20) depicts.

$$i_p(t) = i(t - \frac{p.T}{N}) \tag{2.20}$$

Similarly, Fourier coefficients for any phase can be found by (2.21) where a_n denotes Fourier coefficients for the first phase (p=0).

$$i_p \ \rightarrow \ a_n e^{-jn2\pi p/N} \tag{2.20}$$

Due to the linearity property, Fourier coefficients (A_n) for input current (denoted by I(t)) can be found by the summation of phase currents.

$$I(t) = \sum_{p=0}^{N-1} i_p(t) \ \rightarrow F\big(I(t)\big) = \sum_{p=0}^{N-1} F(i_p(t)) \tag{2.21}$$

$$I(t) = \sum_{n=-\infty}^{+\infty} A_n e^{jnwt} \tag{2.22}$$

$$A_n = \sum_{p=0}^{N-1} a_n e^{-j2\pi p\frac{n}{N}} \tag{2.23}$$

By the rearrangement of the terms and the utilization of finite sum formula (2.24) is found.

$$\begin{aligned} A_n \ &= \ \sum_{p=0}^{N-1} a_n e^{-j2\pi p\frac{n}{N}} \ = \ Na_n \frac{1 - e^{-jn2\pi}}{1 - e^{-\frac{jn2\pi}{N}}} \\ = \ Na_n &\frac{e^{-jn\pi}(e^{jn\pi} - e^{-jn\pi})}{e^{-\frac{j\pi n}{N}}(e^{\frac{j\pi n}{N}} - e^{-\frac{j\pi n}{N}})} \ = \ Na_n e^{-j\pi n} e^{j\pi n/N} \frac{\sin(n\pi)}{\sin(\frac{n\pi}{N})} \end{aligned} \tag{2.20}$$

Examining the result of (2.20), it can be seen that the equation is equal to zero for all non-integer values of n/N ratio. For the integer values of n/N, after applying l'Hospital's rule equation (2.21) is obtained.

$$A_n = \begin{cases} Na_n & \frac{n}{N} \in Z \\ 0 & \frac{n}{N} \notin Z \end{cases} \tag{2.20}$$

For a single-phase boost converter input current, current harmonics are present at integer multiples of switching frequency. Equation (2.20) states that, for the interleaved case current harmonics will only occur at frequencies Nf, 2Nf, 3Nf etc… The magnitude of the current harmonic at xNf where x any integer is N times the magnitude of the current harmonic of the single-phase structure at xF. This is also the mathematical reasoning of the frequency multiplication property of interleaving which was mentioned before.

2.2.2 Voltage Ripple Reduction

Peak to peak output voltage ripple for a buck converter is given by (2.21). To modify it for obtaining voltage ripple expression for the interleaved case, ΔI terms should be updated as equation (2.13) suggests. Noting that the utilization of interleaving also multiplies the effective frequency with "N", equation for peak to peak output voltage ripple for interleaved converters is obtained as (2.22) suggests.

$$\Delta V = \frac{\Delta I}{8fC} \tag{2.21}$$

$$d = \lfloor ND \rfloor \quad \rightarrow \quad \Delta V = \frac{V_G}{8.f^2.N^2.L.C}\, d(1-d) \tag{2.22}$$

Examining Figure 2.10, it is seen that, ignoring the extreme values of duty cycle (D<0.1 and D>0.9), interleaving brings at least 1/N reduction in current ripple. Therefore, the capacitance required for a single-phase buck converter which corresponds to an acceptable output voltage ripple is lessened by at least N^2 for an interleaved buck converter.

$$C_{INTER} < \frac{C_{SINGLE}}{N^2} \tag{2.23}$$

Note that output voltage ripple magnitude being the most important parameter in the selection of output capacitance in a buck converter, is not the only parameter effecting the selection. A requirement such as total hold up time can be imposed on a buck converter making the drastic reduction of output capacitance impossible although the current ripple is very much decreased. Nonetheless, interleaved converters require less capacitance compared to single-phase structure as (2.23) suggests.

2.2.3 Component Scaling Effect

As already discussed, interleaved converters can be designed with smaller inductors and capacitors due to the current and voltage ripple reduction properties. This ability is named as "component scaling effect" and it is the reason why interleaving is adopted as a means for obtaining higher power density converters.

Even if same amount of inductance that will be denoted by "L" is used in an interleaved and a single-phase converter, the resultant total inductor volume is expected to be smaller for the interleaved case. Considering that inductor volume is directly proportional to the energy stored in inductor (2.24), equations (2.25) and (2.26) describe the total inductor volume reduction property of interleaved converters. Although an energy based approach explains the situation, formulating an exact relation for inductor volume reduction would be impractical since specific parameters such as core size, shape and material and loss mechanisms regarding inductor design should be defined first for such an analysis.

$$V_L \propto E_L = \frac{1}{2} L I^2 \tag{2.24}$$

$$E_{L,SINGLE} = \frac{1}{2} L I^2 \tag{2.25}$$

$$E_{L,INTER} = N.\frac{1}{2} L \left(\frac{I}{N}\right)^2 = \frac{1}{2N} L I^2 \tag{2.26}$$

Interleaving technique also enables the utilization of integrated magnetics. Considering the illustration for the physical implementation of two inductors depicted in Figure 2.15, flux cancellation in the center leg can be achieved which in turn permits the implementation of inductors in a smaller volume [37].

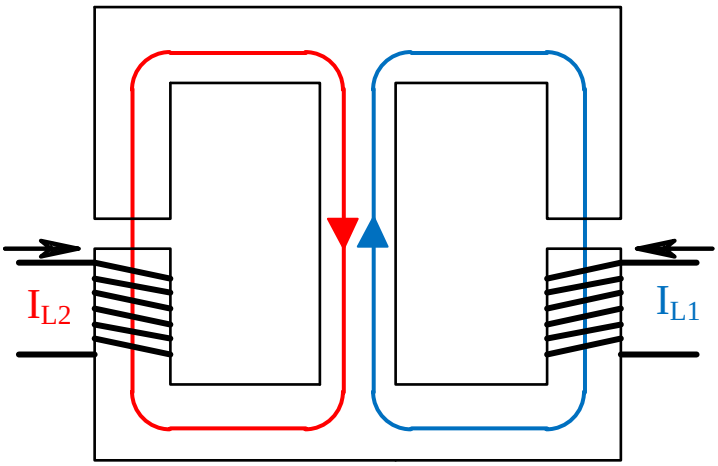


Figure 2.15 Utilization of integrated magnetics for interleaved converters: two decoupled inductors with flux cancellation in center leg.

Note that Figure 2.15 stands for decoupled inductor case. The ungapped center leg provides a low impedance path for the fluxes created by windings positioned at the left and right legs which are gapped. Flux created by each winding tends to flow through the center leg rather than the other gapped leg thus coupling between the two inductors is avoided. With the proper positioning of windings, flux cancellation in the center leg can be provided. The effects of the utilization of coupled inductors on interleaved converter's performance will be examined in a separate section.

Input ripple reduction and frequency multiplication of interleaving also enables the reduction of EMI filter size, which is a critical concern for modern AC-DC front end converters [17, 38].

2.2.4 Faster Dynamic Behavior

Utilization of interleaving enables the design of converters with faster response. Considering that the effective frequency at the output of the converter is multiplied by “N” without a serious penalty on switching losses, gain crossover frequency of the control loop can be tuned to a higher value compared to the non-interleaved case. Moreover, the increase in effective frequency means higher control resolution and smaller time steps for the correcting signals in digitally controlled converters which can further enhance the dynamic behavior. The parallel operation of inductors is also another factor boosting dynamic performance: in the case of an abrupt load current step of ΔI which in turn results in duty cycle saturation for the converter to provide the current amount demanded by the load, (assuming equal inductance values for the interleaved and non-interleaved cases) time required for increasing each inductor current by ΔI/N in the interleaved case is shorter than increasing a single inductor’s current by ΔI, as depicted in Figure 2.16. A comparative study on dynamic response performance of interleaved converters is provided in [39].

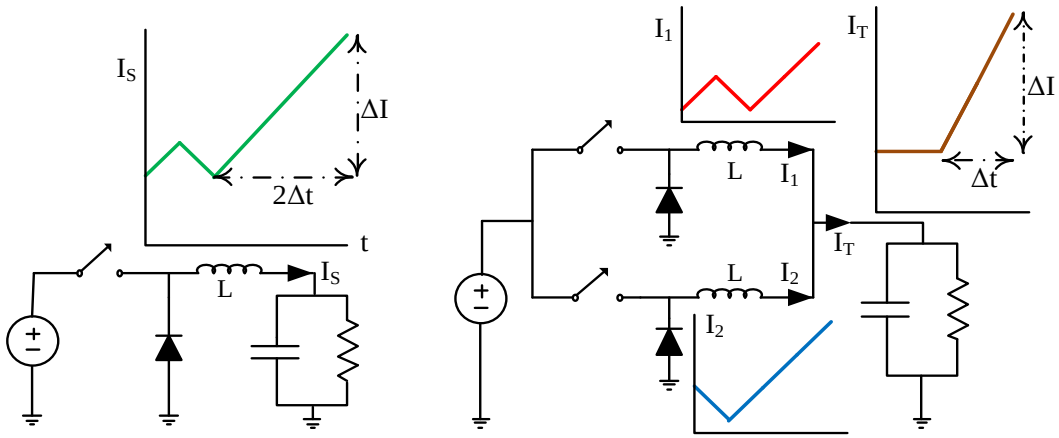


Figure 2.16 Comparison of single-phase and two-phase interleaved buck converters’ output current in the case of duty cycle saturation.

2.2.5 Considerations on the Efficiency of Interleaved Power Conversion

Expressing a general statement such as interleaving enhances or worsens efficiency would be impractical. For a fair comparison of efficiency comparison between two different topologies (interleaved versus traditional single-phase structure), approach for comparison should be defined first and number of semiconductor switches should also be considered. Although an exact statement for superiority or inferiority of interleaved efficiency is not aimed, it is beneficial to consider the effect of interleaving on converter efficiency.

When a converter is implemented in the form of paralleled power stages, which is the case for interleaving, effective series resistance of the power conversion module experiences reduction due to paralleling as illustrated in Figure 2.17. This implies the reduction of conduction losses. Considering that conduction loss is the dominant loss mechanism in many applications, effective series resistance decrease due to paralleling brings efficiency increase. However, noting that total number of components used in the multi-phase converter is N times those of single-phase counterpart, interleaving (or paralleling in general) cannot be stated as a means for efficiency improvement; it is mainly the utilization of higher number of components that brings conduction loss decrease.

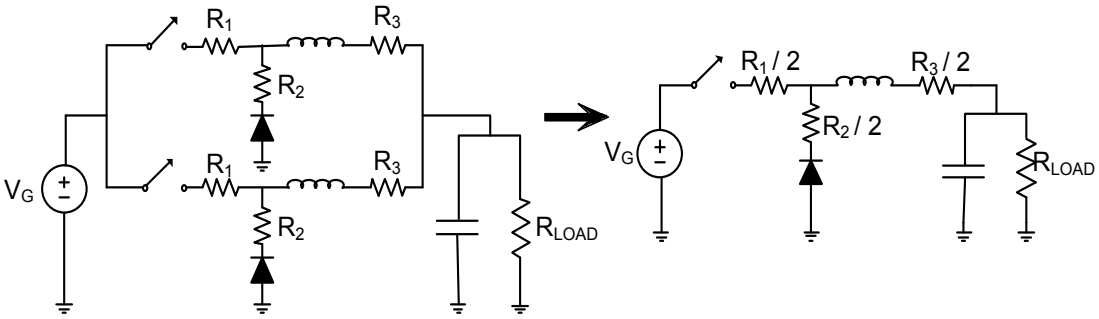


Figure 2.17 Illustration for effective series resistance decrease due to paralleling.

It should also be noted that, in the interleaved power conversion current ripple cancellation occurs at the input and output of a converter. That is, current ripple exists for all paralleled phases as depicted in Figure 2.18. Therefore a conduction loss reduction that is less than 1/N should be expected for the paralleling of N-phases since rms values of phase currents are greater than the average values because of the ripple content.

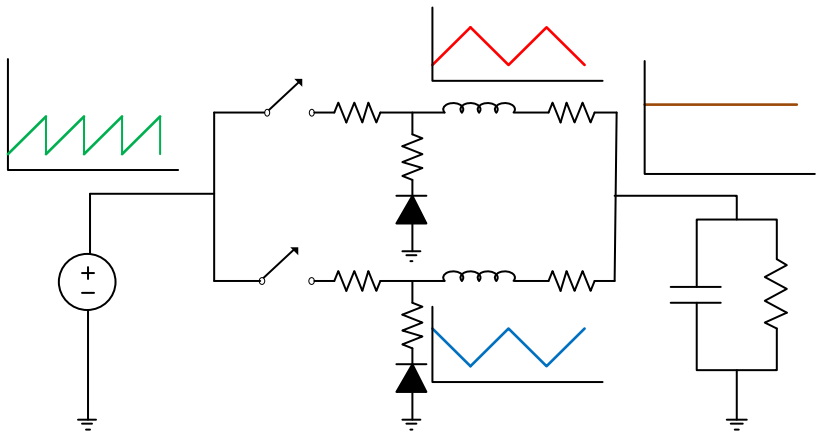


Figure 2.18 Input, output and phase currents for a two-phase, interleaved buck converter with 0.5 duty cycle operation.

The issue of decrease in the reduction of conduction losses in an interleaved converter due to the presence of current ripple at each phase can be further examined by power loss calculations for the simplified scheme depicted in Figure 2.19. A single resistance "R" that carries current with average value I_{avg} with peak ripple ΔI_p and a paralleled scheme of N resistors with the same value resistance value of "R" each of which carrying currents with average value I_{avg}/N with same peak ripple ΔI_p is depicted in Figure 2.18.

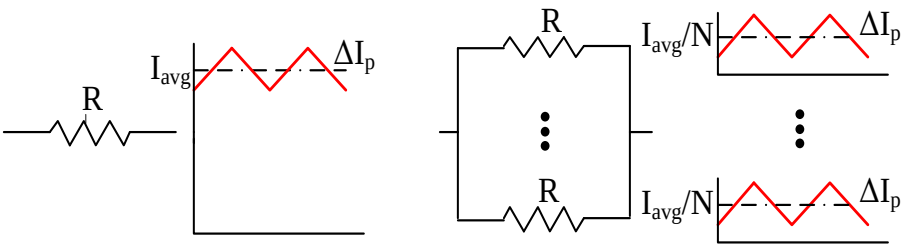


Figure 2.19 Emphasis on the AC content of phase currents.

Rms value of a current with average value I_{avg} and peak ripple ΔI_p is given by (2.27). Power dissipated in the single resistor case and paralleled resistors case is given by (2.28) and (2.29) respectively. Finally, paralleled resistor scheme power dissipation over single resistor power dissipation ratio is obtained as (2.30). Note that, in (2.30) "a" stands for the $\Delta I_p / I_{avg}$ ratio.

$$I_{RMS,S} = \sqrt{I_{avg}^2 + \frac{\Delta I_p^2}{3}} \tag{2.27}$$

$$P_{SINGLE} = R.\left(I_{avg}^2 + \frac{\Delta I_p^2}{3}\right) \tag{2.28}$$

$$P_{PARALLEL} = N.R.\left(\frac{I_{avg}^2}{N^2} + \frac{\Delta I_p^2}{3}\right) \tag{2.29}$$

$$\frac{P_{PARALLEL}}{P_{SINGLE}} = \frac{3 + N^2 a^2}{N(3 + a^2)} \tag{2.30}$$

Using (2.30), paralleled resistor scheme power dissipation over single resistor power dissipation ratio is plotted in MATLAB and depicted in 2.20 for different values of "N" and "a". It can be observed that the effect of current ripple presence at each paralleled component reduces the gain in conduction loss reduction. As an example, paralleled resistor scheme power dissipation over single resistor power dissipation ratio roughly equals to 0.3 for N=4 and a=0.2 case where a ratio of 0.25 would have

been expected if only the average current values were considered for the loss calculations.

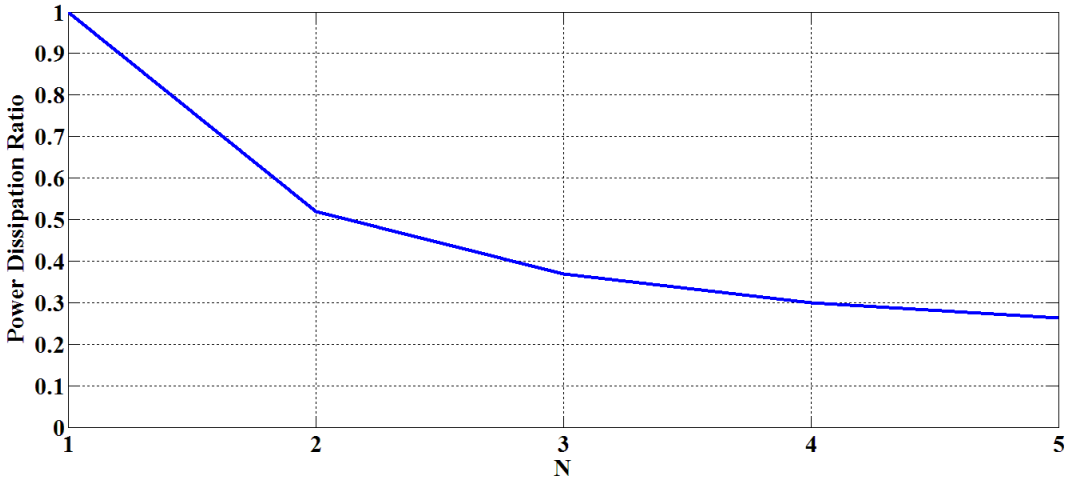


Figure 2.20 Parallel resistors (N number of resistors with resistance R) power dissipation to single resistor (R) power dissipation ratio versus the number of paralleled resistors.

Note that in Figure 2.20, a power dissipation comparison is made between resistance "R" and "N" resistances in parallel each of which equals "R". If the resistances in the paralleled scheme are assumed to be "N.R", equating the effective resistance to that of single resistor case, Figure 2.21 is obtained.

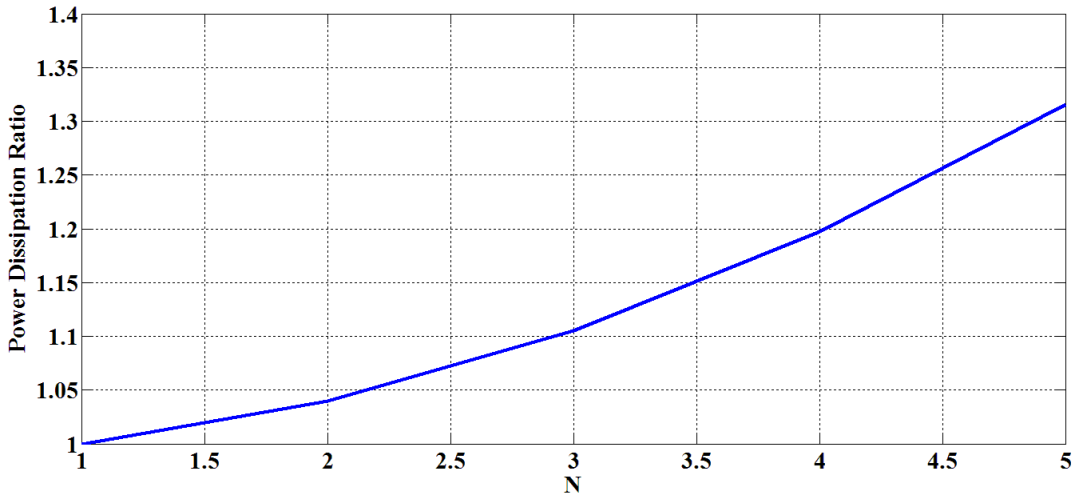


Figure 2.21 Parallel resistors (N number of resistors with resistance N.R) power dissipation to single resistor (R) power dissipation ratio versus the number of paralleled resistors.

Switching loss, which is one of the fundamental loss mechanisms in DC-DC converters, should also be considered for the interleaved case. Assuming small $\Delta I_p / I_{avg}$ ratio and adopting a simplified model (2.31) for switching, it can be seen that interleaving does not seriously affect switching loss performance. However, considering that turn on and off times for semiconductor switches are often determined by EMI/EMC considerations for the practical converter, in an interleaved converter it is possible to turn the switches on and off faster since each switch will be dealing with a reduced magnitude of current due to paralleling. That in turn may yield the reduction of switching losses depending on the rate of shortening the switching instant. It is also worthwhile to mention that the presence of current ripple at each phase may have a boosting effect on switching losses as in the case of conduction losses.

$$P_{SW} = \frac{1}{2} V_{sw,on} I_{sw,on} . f . t_{on} + \frac{1}{2} V_{sw,off} I_{sw,off} . f . t_{off} \tag{2.31}$$

For the inductor losses of an interleaved buck converter example, which can be grouped in two as core and conduction losses, a quick observation shows that

compared to the single-phase structure, interleaving can offer reduced inductor loss since inductors can be designed such that total inductor volume is considerably smaller than that of single-phase case. With the inductor volumes considerably decreased, it is possible to obtain both core and conduction loss reduction. On the other hand, the presence of current ripple at each phase creates individual core losses for each phase inductor, boosting the total inductor losses. Having introduced an overview on inductor losses for the interleaved converter structure, for a concrete analysis on the effect of interleaving on inductor losses, a through definition on the approach for comparison and a detailed inductor design are required which will be presented in Chapter 3.

The only loss type that is directly affected by interleaving is input/output filter loss. Due to the input/output current ripple reduction, losses due to the ESR of output capacitors or input EMI filter losses will be considerably reduced by interleaving. However, these are not among main loss mechanisms heavily effecting the overall efficiency for most of the practical converters therefore reduction in these losses do not offer a serious increase in the overall efficiency.

2.2.6 Further Issues on Interleaving

Benefits of interleaving having already been stated, further techniques on the utilization of interleaving are to be presented. Three important issues, namely current sharing, dynamic number of phases and application of coupled inductors are selected for examination.

An interleaved converter having multiple paralleled power stages may experience serious phase current imbalance and for most of the applications current sharing between parallel power stages is forced. This situation is discussed in 2.2.6.1.

Until now, number of parallel power stages was denoted by “N” and was assumed to be constant over the entire load range. However, it is also common practice to shut down some of the parallel phases in light-load conditions to obtain higher light-load efficiency characteristics as will be described in 2.2.6.2.

In the component scaling effect discussion of 2.2.3, application of integrated magnetics was introduced without an emphasis on the coupled inductor case. Utilization of magnetic coupling betweeN-phase inductors in interleaved DC-DC converters introduces further benefits and complications which are examined in 2.2.6.3.

2.2.6.1 Current Sharing

As already mentioned in MOSFET Paralleling section of 2.1.1.1, even same types of practical power electronic components vary in their effective DC resistance values, creating current imbalance in a paralleled scheme. Even if the resistance values are precisely set by fabrication, aging or drift of the components may also create a difference which in turn can yield a current imbalance. Figure 2.22 depicts a two-phase interleaved buck converter composed of non-ideal components which have different effective DC resistance values from those of their respective counterparts in the other phase.

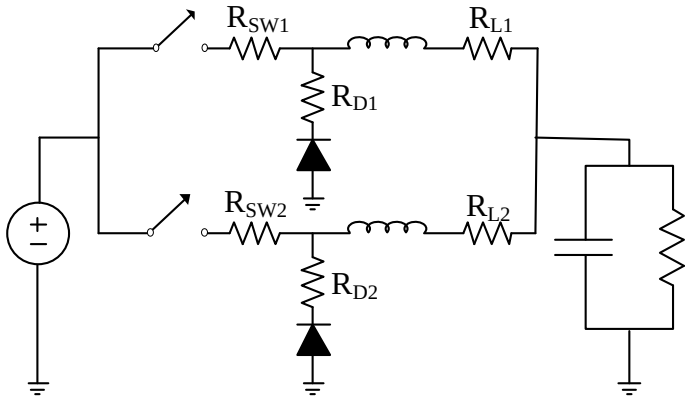


Figure 2.22 A practical two-phase interleaved buck converter diagram with components differing in DC resistance values.

Using the results of state space averaging method applied to the non-ideal case of Figure2.22 in [40], expressions for average inductor currents of each phase are given in (2.32)-(2.35).

$$R_{EQ,1} = R_{L1} + D_1.R_{SW1} + (1 - D_1)R_{D1} \tag{2.32}$$

$$R_{EQ,2} = R_{L2} + D_2.R_{SW2} + (1 - D_2)R_{D2} \tag{2.33}$$

$$I_{L1} = \frac{(D_1 - D_2)V_G}{R_{EQ,1} + R_{EQ,2}} + \frac{R_{EQ,2}}{R_{EQ,1} + R_{EQ,2}} I_O \tag{2.34}$$

$$I_{L2} = \frac{(D_2 - D_1)V_G}{R_{EQ,1} + R_{EQ,2}} + \frac{R_{EQ,1}}{R_{EQ,1} + R_{EQ,2}} I_O \tag{2.35}$$

Several observations can be made on the equations (2.32)-(2.35). Firstly, it can be seen that average phase current distribution is a function of equivalent phase resistance and is not affected by inductance or output capacitance. For a balanced average current distribution between the phases, either equivalent phase resistance matching ($R_{EQ,1}$=$R_{EQ,2}$) should be provided or in the case of mismatch; different duty cycle values should be created for each phase accordingly such that the difference in phase resistances is compensated and balanced phase currents are maintained.

Note that current sharing is inherently provided if a current mode control scheme is utilized since current value for each paralleled power stage is sensed and equated to a common reference signal. In peak current mode control, equal phase current distribution is provided as long as phase inductances are matched; difference in inductance values will result in an average current mismatch. If average current mode control is applied, average values for phase currents will be equal but peak values will differ in the presence of inductance mismatch. Figure 2.23 depicts inductor currents for a two-phase interleaved buck converter with slightly different phase inductances under peak current mode and average current mode cases. However, these variations in phase currents due to inductance mismatch mentioned for peak and average current control techniques do not possess a serious threat for converter operation as long as the mismatch stays within acceptable limits, which is

usually the case. Having in mind that the motivation for current sharing in interleaved converters is to prevent drastic current imbalances which may cause unequal thermal stress and lead to the malfunction of the converter, for most of the time small differences in phase currents can be tolerated. It is also worthwhile to mention that utilization of current mode control requires the use of additional current sensors which increases system complexity and cost.

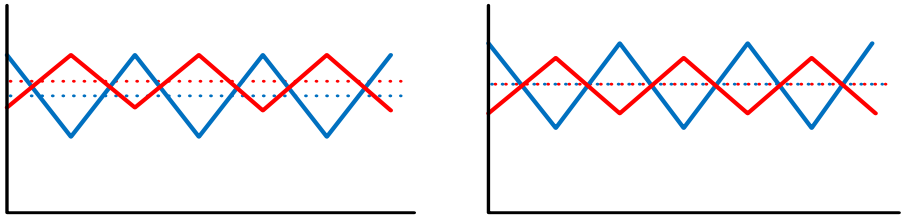


Figure 2.23 Inductor currents of a two-phase interleaved converter with average and peak current imbalance due to inductance mismatch.

In the absence of current mode control, corrective signals for current sharing can be created and individual duty cycle values that yield balanced current distribution can be fed into interleaved stages as (2.34) and (2.35) suggests. Several studies on current sharing for interleaved converters are reported in the literature [40-45]. Theoretical analysis for current sharing and its adoption to current doubler rectifiers are presented in [40]. In [41], a simple and low cost method for current sharing is proposed: with an RC network connected across the low side switch of a buck converter, it is possible to obtain the average DC voltage across it. Then, with the assumption that matched effective series resistances for the inductors are guaranteed, phase currents can be monitored and governed by observing average diode voltage and the output voltage. Decreasing number of current sensors is targeted in [43]; current sharing for a three-phase boost converter is achieved with a single current sensor. A method for achieving current sharing without any type of current sensing is proposed in [42-44] which mainly relies on extracting phase current information

by creating small disturbances in phase duty cycles and observing the corresponding change at the output. Similarly, [45] achieves current sharing without any current sensors by observing input voltage ripple.

2.2.6.2 Dynamic Number of Phases

Another widely utilized technique regarding interleaving is the operation of decreasing active number of paralleled stages as the load current decreases [46-48]. Other expressions for the dynamic number of phases technique exist such as variable number of phases or phase shedding. Main motivation for the utilization of dynamic number of phases for an interleaved converter is to increase light load efficiency.

Considering the efficiency versus load current graph of a converter, it is possible to obtain an increase in efficiency by reducing the number of active phases for a value of load current if the efficiency curve has a positive slope at that point. The operation of a three-phase buck converter utilizing phase shedding technique is presented in Figure 2.24. It can be seen that efficiency curve over the entire load range has become flat and light load efficiency is improved by shutting down some of the parallel phases as load current decreases.

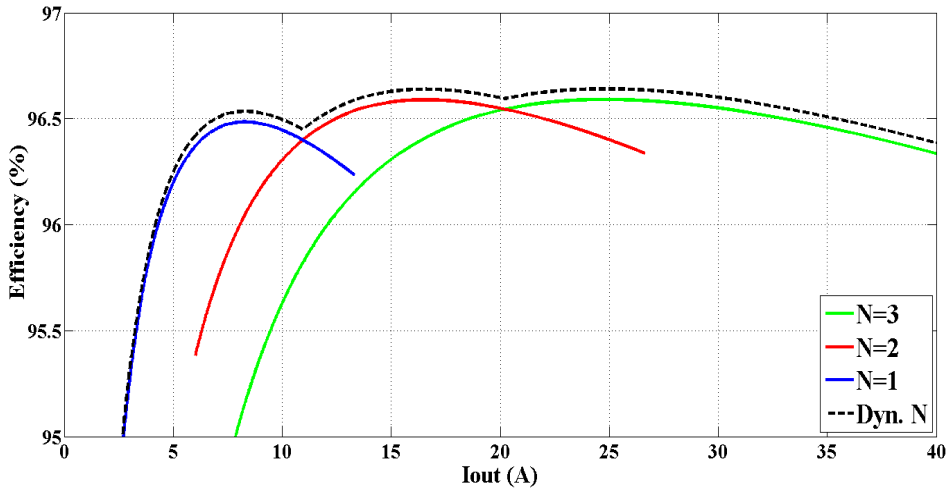


Figure 2.24 Light load efficiency improvement by efficiency curve flattening on a three-phase buck converter example utilizing dynamic number of phases.

Considering the loss mechanisms affecting the efficiency of a converter, it can be concluded that the loss terms resulting in a positive slope of efficiency are the ones which are independent of the load current. For a converter with the conduction loss being the dominant loss term, efficiency is expected to increase as load current decreases. However, load current independent constant loss terms such as inductor core loss, losses due to AC resistances on the power stages, snubber losses and power dissipated to supply active components in the converter such as gate drives or sensors, result in a decrease in efficiency with decreasing load current making the use of dynamic number of phases approach feasible.

2.2.6.3 Application of Coupled Inductance

Integrated magnetics issue was introduced in the Component Scaling Effect section of 2.2.3 yet only the decoupled case with flux cancellation in the center leg was addresses. However, integration of inductances can also be utilized for providing coupling between inductors. Main inductor topologies that can be achieved by the integrated magnetics approach are depicted in Figure 2.24.

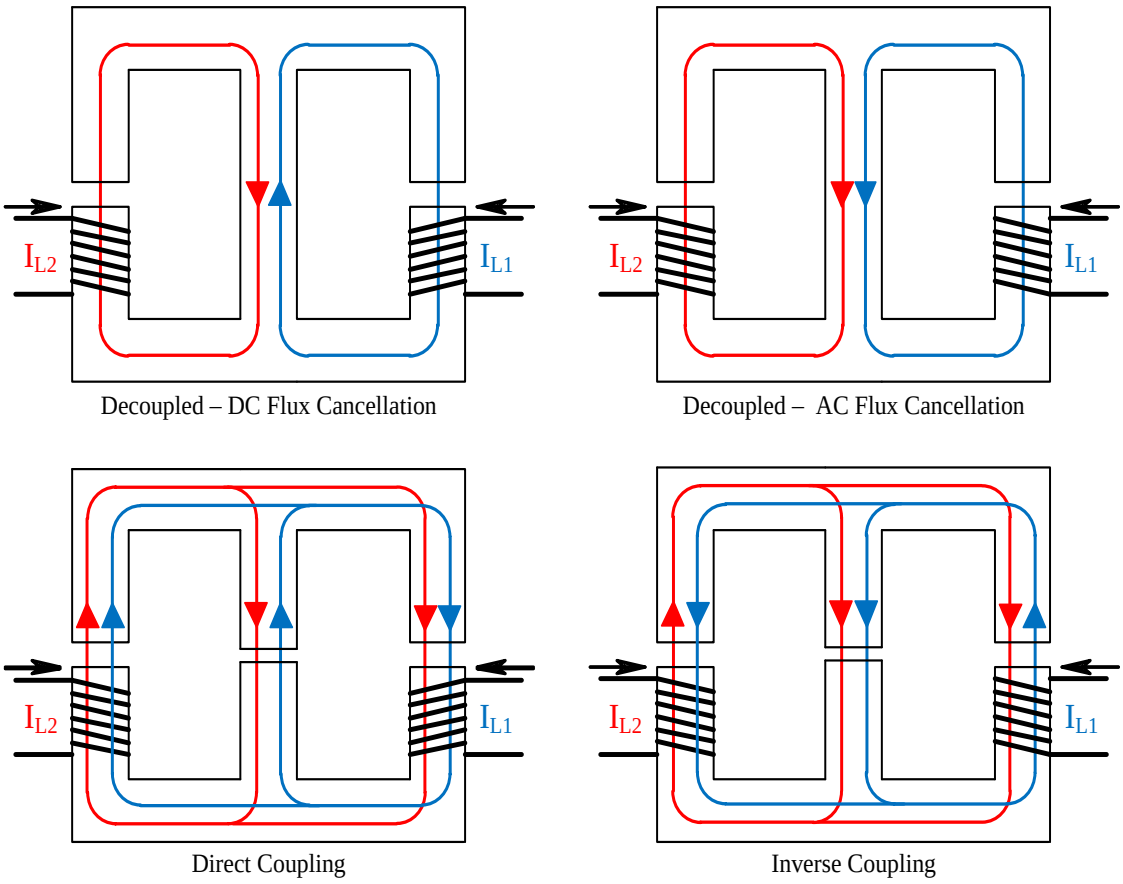


Figure 2.25 A practical two-phase interleaved buck converter diagram with components differing in DC resistance values.

A general examination on the inductor topologies depicted in Figure 2.25 shows that a coupling hence mutual inductance is created between the two inductors by the utilization of a gap in the center leg. Coupling can be in two forms: direct or inverse. In direct coupling, fluxes created by each winding are additive at the counter winding, in the inverse coupling case they are subtractive. Coupling type can be designed by arranging the winding geometry for the desired flow direction of magnetic flux and the amount of coupling can be adjusted by air gap lengths. Note that for the decoupled design, gapless center leg provides a low impedance path for flux therefore fluxes created by each winding do not choose the counter winding's leg as the return path disabling mutual inductance. If flow directions of the two fluxes are opposite in the center leg, DC flux cancellation is provided. Flux

directions being same, DC components are added but AC flux cancellation is possible.

Utilization of coupled inductors for interleaved converters as illustrated in Figure 2.26, offers further benefits such as better steady state operation and faster dynamic response. Several studies are reported for the interleaved converter operation with coupled inductor [13, 37, 49-53].

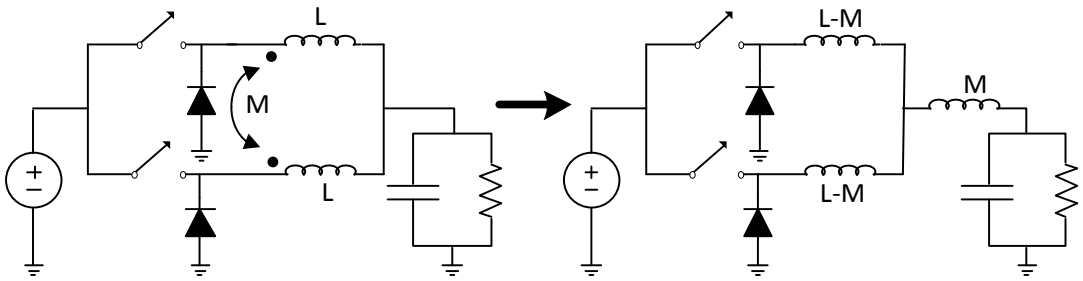


Figure 2.26 A two-phase interleaved buck converter with coupled inductors.

Considering a two-phase interleaved buck converter example, if the inductors in an interleaved converter are magnetically coupled, inductor voltage relation of (2.36) should be revised as (2.37).

$$V_L = L.\frac{di}{dt} \tag{2.21}$$

$$V_{L1} = L_1\frac{di_1}{dt} + M\frac{di_2}{dt}$$

$$V_{L2} = M\frac{di_1}{dt} + L_2\frac{di_2}{dt} \tag{2.22}$$

Theoretical analysis of [13] will be summarized for the explanation on the effect of coupled inductors on converter performance. With the assumption that $L_1 = L_2$ and the definition $\alpha = M / L$, (2.22) can be re-written as:

$$V_{L1} - \alpha V_{L2} = (1 - \alpha^2).L.\frac{di_1}{dt} \tag{2.23}$$

It can be seen that, if the relation between V_{L1} and V_{L2} can be defined, it is possible to simplify the equation of (2.23) and obtain a familiar expression such as (2.21). Narrowing the analysis down to the case of N = 2 and D < 0.5, there are three distinct intervals (phase 1 off, phase 2 off, both off) defining a set of three equations describing V_{L1} - V_{L2} relation. Therefore, three equivalent inductance values can be formulated (2.24)-(2.26) for those three distinct intervals.

$$L_{EQ,1} = \frac{1 - \alpha^2}{1 + \alpha.\frac{D}{1 - D}}.L \tag{2.24}$$

$$L_{EQ,2} = (1 + \alpha).L \tag{2.25}$$

$$L_{EQ,3} = \frac{1 - \alpha^2}{1 + \alpha.\frac{1 - D}{D}}.L \tag{2.26}$$

Equations (2.24) and (2.26) can be used to calculate the peak to peak current ripple of an inductor for D < 0.5 and D > 0.5 respectively. With D < 0.5 assumption, steady state inductor peak to peak current ripple is $L_{EQ,1}$ dependent and formulated in (2.27). Transient response as the ratio of change in current to change in duty cycle is given by (2.28) and it is $L_{EQ,2}$ dependent.

$$\Delta I_{ind} = \frac{V_{ind}.D}{f.L_{EQ,1}} \tag{2.27}$$

$$\frac{\Delta i}{\Delta D} = \frac{V_{in}}{f.L_{EQ,2}} \tag{2.28}$$

A careful examination on the equations presented thus far shows that utilization of inverse (negative) coupling (M < 0) decreases inductor current ripple where direct (positive) coupling (M > 0) increases it. Reduction in inductor current ripple can provide loss reduction considering the reduction of current stress in the

semiconductor switches, core loss and AC losses. However, output current ripple is greater for the inverse coupling case. Another fundamental contribution of coupled inductors is the improved transient response: considering that negative coupling is applied, although phase current ripple is decreased (higher effective inductance seen by phase) the effective output inductance is lessened due to negative coupling, enabling faster current changes thus a superior dynamic performance.

2.3 Summary

With a general examination on paralleling schemes that are commonly applied in power electronics, interleaving technique is discussed in detail and proven to be a very valuable method for achieving superior converter performance. Benefits of interleaving, namely current and voltage ripple reduction at input and output, component scaling and dynamic response are documented. Effect of interleaving on efficiency is evaluated by multiple aspects. Further applications that arise with the utilization of interleaving such as active current sharing, phase shedding and coupled inductors are also described.

CHAPTER 3

CONVERTER OPTIMIZATION

In this chapter, the effect of the selection of switching frequency (f), inductance (L) and number of parallel phases (N) on a converter's efficiency, volume and cost is explored via an optimization program targeting the optimal design of a 1-kW, hard switching, interleaved buck converter. After the detailed descriptions on the approach for optimization, an optimization program is introduced and its outputs are listed to yield optimal (f, L, N) point for the target converter. The optimal design point obtained in this chapter is to be physically implemented.

3.1 f-L-N Based Optimization

The motivation for converter optimization has already been presented in Part 1.3 along several examples. Having in mind that each specific converter has its own characteristics and performance criteria to be met, optimization procedures should also be arranged for the target converter accordingly.

Selection of switching frequency (f) is an important parameter for converter design. Higher switching frequencies enables the use of smaller passive components (capacitors and inductors) which results in a smaller converter volume at the expense of higher switching losses thus a reduced efficiency. Higher switching losses also bring bigger heat sink requirement which may compensate the volume reduction gain. Therefore, for a power converter selection of switching frequency requires efficiency and volume based calculations if an optimal design is aimed.

Considering that the optimal design of a practical buck converter is desired, the importance of inductor selection arises. Inductor volume constitutes a considerable

amount of total volume for a typical buck converter and it is strongly correlated to the selection of switching frequency. In the design of a buck converter, it is common practice to choose an inductance value which results in a current ripple that equals 10 to 30 percent of the average current carried by the inductor. In this study, selection of inductance (L) is another optimization parameter along frequency, which is to be varied and the effects on converter efficiency and volume are to be observed.

Interleaving technique for power electronic converters has been introduced and analyzed as a promising performance enhancer. One may adopt interleaving to reach higher power values or simply due to the superior electrical performance it introduces. Once the utilization of interleaving is decided, number of phases (N) of the interleaved converter is most of the time chosen by experience. In the search of optimum design points, N values ranging from 1 to 5 will be considered in the optimization process. By doing so, analysis on the effect of interleaving on converter efficiency and volume will be carried out. Note that N=1 case corresponds to the single-phase converter structure where interleaving has not been employed: the analysis will also answer the question of whether or not to utilize interleaving technique for a given converter.

In the optimization procedure, a brute force approach is adopted. Efficiency, volume and cost analysis will be done at every (f, L, N) point even if the point does not seem to yield an optimum design. Thus, an overall picture of converter behavior under varying f, L and N will be presented.

3.2 Descriptions on the Approach for Optimization

For a successful modeling of important converter properties such as efficiency and volume under varying f, L and N, several issues such as mathematical representations of loss mechanisms and magnetic component modeling have to be addressed first. In the following chapters, the approach adopted for the optimization study and the computer program prepared are described in detail.

3.2.1 General Converter Specifications

Although the approach for optimization and the expected converter merits would be very much the same, converters designed for different applications may differ in their characteristics and have their own set of performance criteria to be met. As an example, comparing a low power, on-chip DC-DC converter which typically utilizes MHz range switching frequencies to a multi-kW isolated DC-DC converter switching with a frequency of tens of kHz, it can be seen that several design aspects such as modeling for switching losses, magnetics design and thermal management for the reliable operation will seriously differ for these converters. Therefore, it is more appropriate to carry out a converter optimization procedure for a specific, well-defined converter.

This thesis aims the optimal design of a 1-kW, hard switched, non-synchronous buck converter which is supposed to convert 56V to 28V with 36A full load current. Since the highest current rating measurement device available in the laboratory provided for the hardware implementation part of this thesis is Hioki3334 [54] which has a maximum current rating of 30A, to provide a comparison between analytical and experimental results, optimization study is carried out for 800W output power which corresponds to 28A output current.

Considering the converter topology (hard-switched buck converter) and the power capacity, frequency values between 25 kHz and 150 kHz will be considered. Inductance value is also varied at each switching frequency, between a minimum inductance value ($^{1.296}/_{f}$ in Henry) that corresponds to 30% amount of peak to peak current ripple (10.8 A) and a maximum ($^{3.888}/_{f}$ in Henry) that corresponds to 10% peak to peak (3.6 A) current ripple. Finally, effect of interleaved conversion is considered by varying the number of paralleled phases (N) between 1 and 5. A MOSFET is assumed as the main switch which is followed by a schottky rectifier. Further specifications on semiconductor switches will be introduced in 3.3.3. General converter specifications can be seen on Table 3.1.

Table 3.1 General specifications of the target converter.

Input Voltage (V)	56
Output Voltage (V)	28
Nominal Output Current (A)	28
Peak Output Current (A)	36
Nominal Output Power (W)	800
Peak Output Power (W)	1000

3.2.2 Inductor Design

Although inductors can be bought off the shelf for power electronics applications, it is common practice to implement the magnetic element for the application by arranging the geometry and winding a pre-determined number of turns yielding the required inductance value. Different core materials and their sub-families (ferrite, powdered iron etc.) with different core geometries (E core, toroid, planar etc.) along various sizes are present in the market. Since the study of converter efficiency and volume optimization requires examination of various inductors which differ in inductance and current rating value (considering different N yielding different average current for inductors), for a fair comparison it is convenient to determine a fixed core material and geometry such that all the inductors that will be used in efficiency and volume calculations, are made of same core type and material with different sizes and number of turns. Therefore, toroid powder core family introduced by Magnetics® under the name "Kool μ" is chosen for the inductor design process. “Kool μ” is one of several magnetic components generally known as “powder cores” and best suited for power inductors of switch mode power supplies operating at tens to hundreds kHz [55]. Their fundamental advantage over ferrite cores is the decreased core losses. Main drawback for the utilization of Kool μ cores is its relatively higher cost compared to ferrite cores.

For the aim of examining the effects of the change in inductance and operating frequency on the overall converter volume and efficiency, the main optimization

program includes an inductor design sub-module, which designs an optimal inductor at each step as the inductance, frequency and current capacity values are swept by the main optimization program. Necessary inductor related parameters required by the analysis such as inductor core and conduction losses, temperature rise due to these losses and total volume of the designed inductor are also calculated and fed back to the main optimization program. Considering the converter specifications, an inductor core database is created which contains 79 cores of Kool μ family ranging from a minimum volume of 0.9 cm^3 up to a maximum volume of 51.8 cm^3 along necessary physical and electrical properties collected from their respective datasheets required by volume and efficiency analysis.

Expressions for inductance and magnetic flux density for a toroid core are given in (3.1) and (3.2) where N, A, I, l and μ represent number of turns, core cross sectional area, current, magnetic path length and magnetic permeability of the material, respectively.

$$L = {N^2 . A}/{(l/\mu)} \tag{3.1}$$

$$B = {N . I}/{(l/\mu)} \tag{3.2}$$

For the core material of interest, magnetic permeability is seriously degraded with the applied DC bias as depicted in Fig.3.1 which shows inductance per number of turns square value (which is directly related to the effective permeability of the material) versus DC bias (ampere turns) graph for the core number 0077894A7 that has an initial relative permeability value of 60 and core volume 4.15 cm^3.

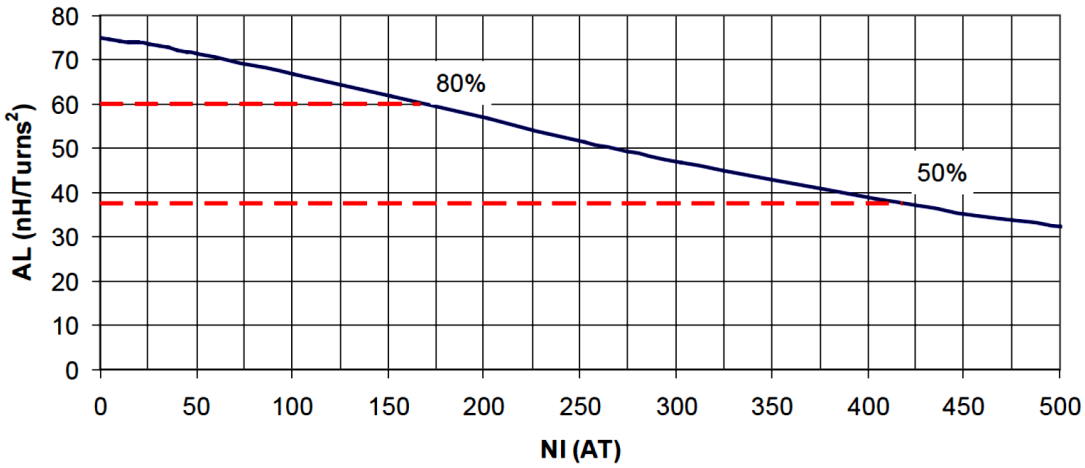


Figure 3.1 Inductance per number of turns square value versus DC bias graph for the core number 0077894A7 [56].

The effect of DC bias dependent permeability can be taken into account in equations (3.1) and (3.2) by considering the expression (3.3) describing permeability-DC bias relationship, provided by the manufacturer [57]. A similar expression giving magnetic flux density is also given in (3.4). In equations (3.3) and (3.4), T and H terms stand for ampere turn and ampere turn per centimeter values, respectively. Note that, form of the expressions for permeability and magnetic flux density remaining same, constants in (3.3) and (3.4) can slightly change depending on the initial permeability of the core yet only the constants for μ=60 case is shown here.

$$\mu\,(p.u) = a + bT + cT^2 + dT^3 + eT^4 \tag{3.3}$$

where;
$a = -8{,}841.10^{-3}$, $b = 5{,}197.10^{-4}$, $c = -7{,}064.10^{-6}$, $d = 1{,}667.10^{-8}$ and $e = 8{,}820.10^{-12}$ for μ=60.

$$B = \sqrt{\frac{a + b.H + c.H^2}{1 + d.H + e.H^2}} \tag{3.4}$$

where;
$a = 1{,}658.10^{-4}$, $b = 2{,}301.10^{-5}$, $c = 7{,}297.10^{-5}$, $d = 5{,}906.10^{-3}$ and $e = 6{,}053.10^{-5}$ for μ=60.

By considering equations (3.1) through (3.4) and the physical properties such as cross sectional area and magnetic path length of a core under examination, the required number of turns value that would yield the desired inductance under predetermined DC bias value can be found. Note that, AC flux swing, frequency and temperature are three other factors that affect permeability but they are not taken into consideration in the analysis since their effects on permeability are negligible (less than 1-2%) for the operating conditions assumed in this analysis.

After the required number of turns to reach target inductance value for the core under examination is calculated, the inductor design program checks whether the resulting N.I value is smaller than that of 50% roll off N.I value. If that is the case, which also guarantees that magnetic saturation is avoided, the next decision point is based upon temperature rise. DC resistance of the inductor is calculated by first finding the length (mean turn length times number of turns) and area (current density of the wire is preset) of the copper wire used then applying the formula for DC resistance (3.5). Although its contribution is small for the frequency range of interest, skin effect is considered throughout the analysis yet proximity effect is omitted. Involving skin effect into calculations yields an effective AC resistance higher than the DC resistance as (3.6) suggests. A simplified equation describing the penetration depth (D_{PEN}) for copper conductors is given in (3.7). Once the DC and AC resistances for the given core and winding properties are obtained, conduction losses of the inductor can be calculated. The other fundamental loss term for an inductor is the core loss. Core loss is calculated by the multiplication of core volume (read by the program from the core database) and core loss density (3.8). Core loss density formula is given in (3.9) and is provided by Magnetics®. Note that B and f stand for magnetic flux density swing and operating frequency respectively and the terms marked as K, α, β are constants depending on the initial permeability of the core.

$$R_{DC} = \rho . \frac{l}{A} \tag{3.5}$$

$$R_{AC} = R_{DC}\frac{r^2}{r^2 - (r - D_{PEN})^2} \tag{3.6}$$

$$D_{PEN} = \sqrt{\frac{0{,}172}{4.\pi^2.f}} \tag{3.7}$$

$$P_{CORE} = P_{CORE,DENS}.Volume \tag{3.8}$$

$$P_{CORE,DENS} = K.B^{\alpha}f^{\beta}\ (mW/cm^3) \tag{3.9}$$

where; K=193, α=2,01 and β=1,29 for μ=60.

Finally, the temperature rise due to the losses occurring on the inductor is calculated via (3.8) and the result is compared to the preset allowable temperature rise value. If thermal criterion is also met, design process is complete and the inductor design program feeds the necessary parameters such as conduction losses, core losses and volume of the inductor back to the main optimization program. If not, inductor design program states that the core under examination is not a proper core for given operating conditions and considers the next core in its database.

$$\Delta T(°\mathrm{C}) = \left(\frac{P_{CORE} + P_{COND.}\ (mW)}{Area\ (cm^2)}\right)^{0.833} \tag{3.10}$$

Flow-chart diagram of the inductor design tool is depicted in Fig.3.2.

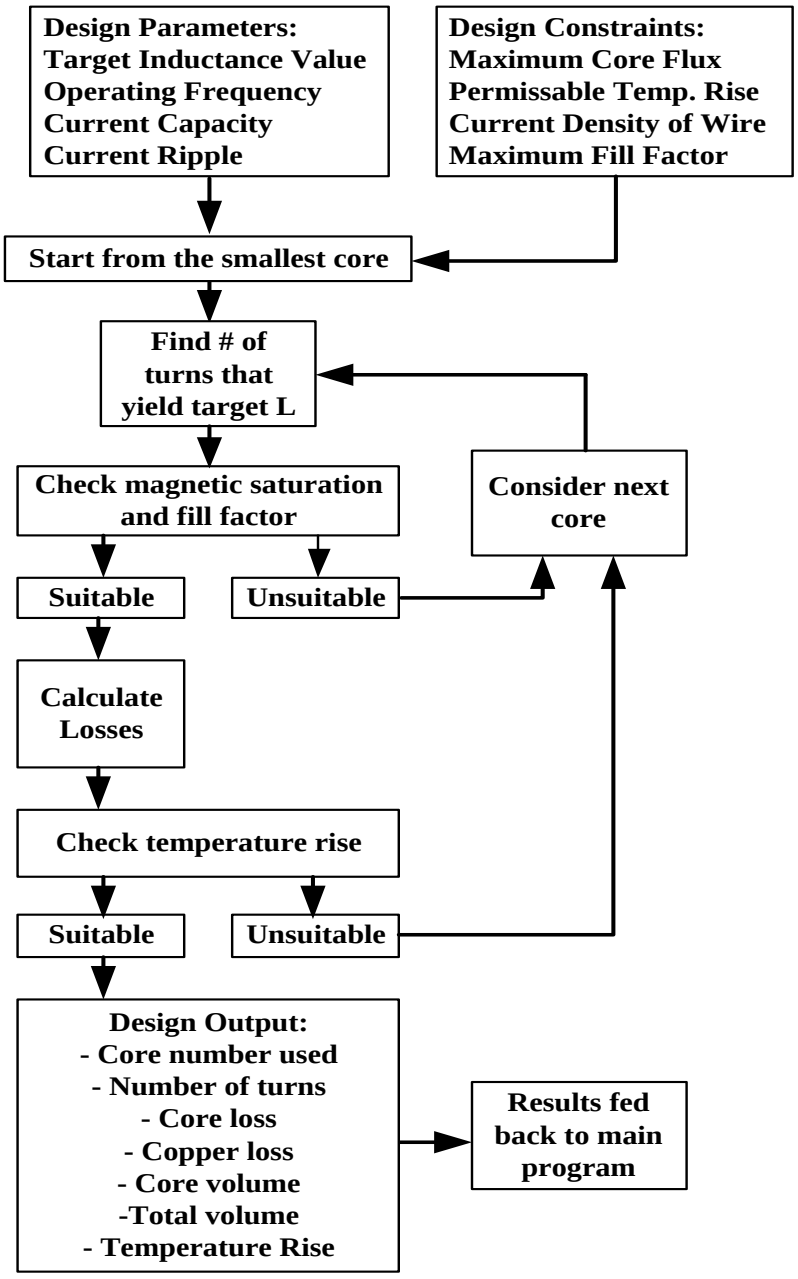


Figure 3.2 Flowchart diagram of the inductor design program.

Inductor design process is a sub-module of the whole optimization program but it can also be used as a stand-alone tool. One design example will be introduced: when user enters the design constraints given in Table 3.2, inductor design program scans its core database, selects the optimum core for the job and produces results which can be seen on Table 3.3. Additional information on the selected core is given

in Table 3.4. Note that, there is no risk of magnetic saturation, maximum N.I value is less than the core's 50% N.I value and temperature rise does not exceed the acceptable limit.

Table 3.2 Inductor design example: constraints set by user.

Full DC Current (A)	25
Peak to peak Current Ripple (A)	10
Frequency (kHz)	25
Wire Current Density (A/cm2)	500
Target Inductance (μH)	50
Allowable Temperature Rise (°C)	50

Table 3.3 Outcomes of inductor design program for the set of constraints listed in Table 3.2.

Suggested Core	0077091A7
Inductance at Full Load (μH)	49.65
Effective u at Full Load	18.95
Number of Turns	41
DC Resistance (mΩ)	8.35
AC Resistance (mΩ)	11.12
Core Loss (mW)	380.3
Copper Loss (mW)	5722.4
Total Loss (mW)	6102.7
Temperature Rise (°C)	45.92
Maximum B (Tesla)	0.3234
Minimum B (Tesla)	0.2249
Maximum N.I (Amp.Turns)	1230
Total Inductor Volume (cm3)	31.6

Table 3.4 Information on the selected core, 0077091A7.

Core Name	0077091A7
Relative Permeability	26
Cross Section (mm2)	134.0
Path Length (mm)	116.3
Volume (mm3)	15580
Surface Area (mm2)	6170
50% NI (Amp.Turns)	2370

Inductor design operation with a limited number of cores in the database results in discrete changes and discontinuity points in the graphs of volume with respect to changing frequency and inductance. Therefore, a second operation option is included in the inductor design program: the program starts with a small core having 2.3 cm^3 volume and relative permeability 60, and increases its physical dimension proportionally by two percent at each step where the current size of the core is not sufficient for target inductor design. This option is used in the analysis since it offers a higher resolution and is better at showing the converter behavior while frequency and inductance are changing. The inductor design program written for the analysis is given in Appendix A.

3.2.3 Converter Loss Modeling

For a buck converter with the specifications introduced, main loss mechanisms can be stated as conduction and switching losses. Relatively small loss mechanisms namely inductor core losses, gate drive losses and losses that stem from MOSFET output capacitance are also included in the analysis. Diode reverse recovery phenomena which is one of the main loss factors in a typical buck converter is not taken into consideration since a schottky type diode is considered. Expressions adopted for loss calculations are given in (3.11) - (3.15). Important parameters regarding MOSFET switching such as gate drive voltage level and gate resistance are selected considering PCB layout, parasitic inductances and EMI problems. For

the analysis, all MOSFETs are assumed to turn on and off with 300 A/μs rate that makes turn on and turn off times depending on the current value they switch.

$$P_{SW} = {}^{1}/_{2} \, . V_{DS} . I_D . (t_{ON} + t_{OFF}) . f \tag{3.11}$$

$$P_{COND} = I_{RMS} . R_{ON} \tag{3.12}$$

$$P_{GATE} = Q_{GATE} . V_{DRIVE} . f \tag{3.13}$$

$$P_{COSS} = {}^{1}/_{2} \, C_{OSS} . V_{DS}^2 . f \tag{3.14}$$

$$P_{ST} = P_{SW} + P_{COND} + P_{GATE} + P_{COSS} \tag{3.15}$$

3.2.4 Approach for Comparison: Equal I – Equal L

Effective series resistance (or $R_{DS,ON}$ for a MOSFET) decreases as the current capacity increases for an electrical component. Therefore, assuming components with same ESR values for both single-phase (N=1) and interleaved cases (N>1) for an efficiency comparison, corresponds to comparing single-phase structure with current rating "I_{RATED}" to interleaved structure with current capacity "$N.I_{RATED}$", favoring interleaving. For a fair comparison between the interleaved and single-phase cases, ESR values for components are assumed to increase proportionally with increasing number of phases. Same inductance values are taken into consideration for different number of phases. This approach developed for the analysis for a fair comparison is named "equal current capacity – equal inductance approach". Parameters for loss calculation in the efficiency analysis such as effective drain-source resistance, output capacitance and gate charge values for MOSFET and forward voltage drop and effective resistance values for the diode are listed in Table 3.5. (Note that MOSFET output capacitance $C_{OUT,}$ and MOSFET gate charge Q_{GATE} increases with increasing current capacity unlike effective series resistance.)

Table 3.5 List of required parameters for semiconductor (switching, conduction, gate drive and parasitic capacitance) loss calculation for efficiency analysis.

	$R_{DS,ON}$ (mΩ)	V_F (V)	R_{DIODE} (mΩ)	C_{OUT} (pF)	Q_{GATE} (nC)
N=1	15	0,6	1.25	800	144
N=2	30	0,6	2.5	400	72
N=3	45	0,6	3.75	266	48
N=4	60	0,6	5	200	36
N=5	75	0,6	6.25	160	28.8

3.2.3 Volume and Cost Considerations

A converter's volume depends not only on the components used but also on the PCB design, spacing between sub-systems and packaging therefore a strict estimation of overall converter volume may be impractical. However, considering that two main volume occupiers in a typical hard switched, natural cooling, near kW DC-DC converter are heat sink and inductor volumes, overall converter volume can be modeled by the addition of these two components. Inductor volume is found via the inductor design program and heat sink volume is assumed such that 6-cm^3 heat sink is required per 1W loss occurring on semiconductors, which corresponds to k=6 for the equation (3.17). Note that, k=6 decision is made by the observations on temperature rise at the heat sink of the implemented converter and considering the volumetric resistance of a typical heat sink as [58,59] suggest. For a similar analysis targeting a different converter or cooling method, the multiplier in (3.17) can be changed depending on the specifications of the application.

$$V_{TOTAL} = V_{H.S} + V_{IND.} \tag{3.16}$$

$$V_{H.S} = k \,.\, P_{S.T} \tag{3.17}$$

Cost per cm^3 values for copper, heat sink and inductor core costs are assumed as 0.03, 0.07 and 0.06 \$/cm^3 respectively. Considering that heat sink volume is

calculated and the inductor design program determines core volume and required copper wire amount, cost values for heat sink and inductor can be calculated by the multiplication of volume and cost density value ($/cm^3). A constant semiconductor cost of 12$ is assumed for all N values since the comparison is made under the assumption of equal current capacity for each N. For more comprehensive cost analysis, components such as sensors, gate drive and control circuitry etc. can also be considered to further extend the accuracy.

3.2.5 Converter Optimization Program

In view of the descriptions and assumptions made thus far, a MATLAB [60] code, flow chart diagram of which is depicted in Fig.3.3, is written to generate efficiency and volume graphs for varying number of paralleled phases, frequency and inductance value used. The program first picks a frequency value starting from 25 kHz, determines inductance values of interest: values between a minimum inductance value that corresponds to 30% peak to peak current ripple (10.8 A) and a maximum inductance value that corresponds to 10% peak to peak current ripple (3.6 A), then calculates efficiency and volume for all frequency and inductance values for all number of phases. The code written for the converter optimization program is given in Appendix B.

For a power converter design, a designer may not aim to obtain the highest efficiency or lowest volume possible (assuming that highest efficiency and lowest volume for a given converter occurs for different set of design parameters); for most of the time, a design point which boosts efficiency and volume reduction together is favorable. Therefore, besides efficiency, volume and cost, a figure of merit (FoM) is defined (3.18) for the converter to represent the optimum design point. $V_{TOT,MAX}$ and $P_{L,MAX}$ expressions stand for the maximum total volume and loss values encountered in the analysis which are 317 cm^3 and 42.6 W respectively. Thus, relative reduction in loss and volume can be expressed in a single form.

$$FoM = {}^{P_{L,MAX}.V_{TOT,MAX}}/_{P_L.V_{TOT}} \tag{3.18}$$

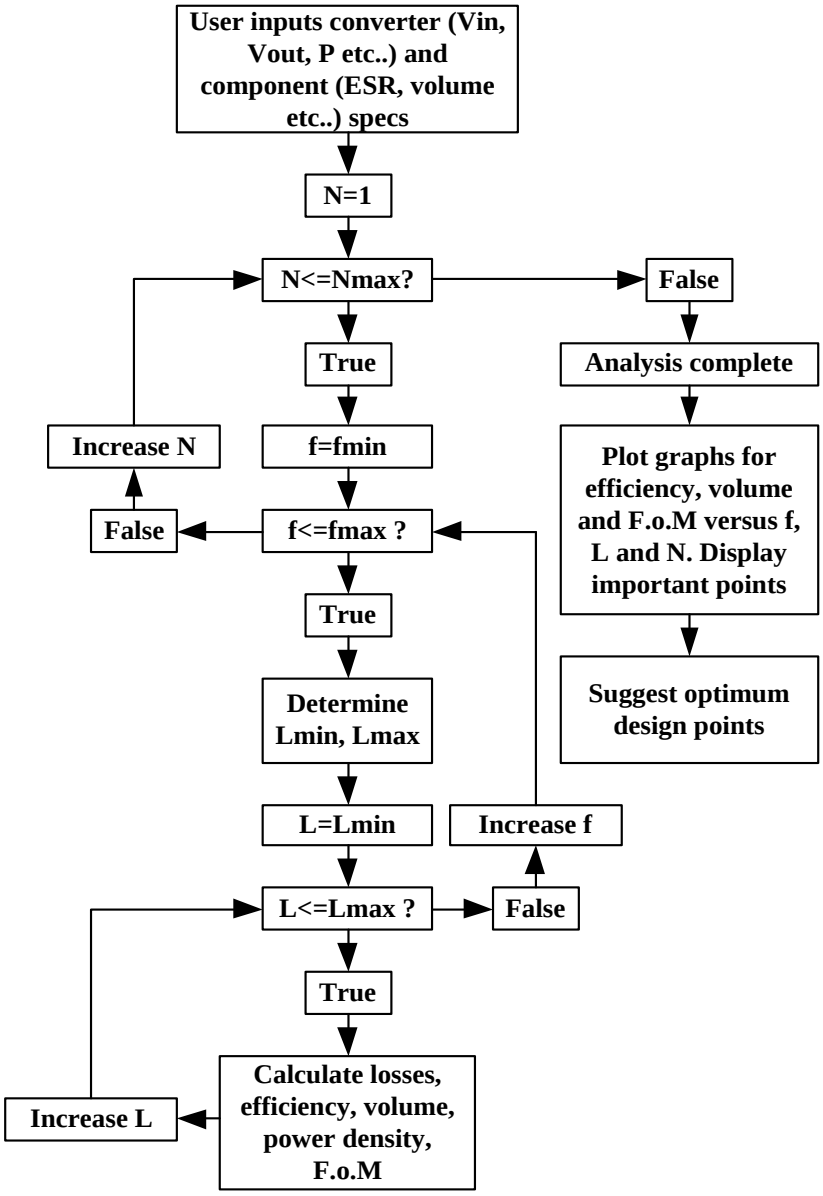


Figure 3.3 Flowchart diagram of the f-L-N based converter optimization program.

3.3 Analysis on the Effect of f, L and N on Converter Efficiency, Volume and Cost

Outputs of the converter optimization program, modeling and comparison approaches of which have been described in detail in the previous parts, will be introduced in this section.

3.3.1 Outputs of the Analysis

Graphs for Efficiency, volume, FoM and cost with respect to frequency (f) and inductance (L) values for various numbers of paralleled phases (N) are depicted in Fig.3.4 – Fig.3.7.

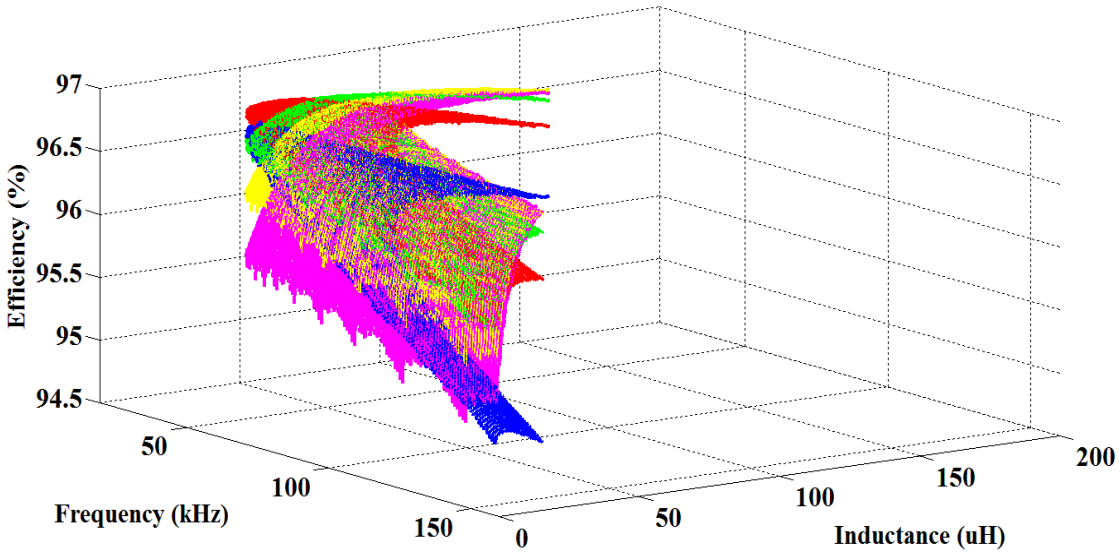


Figure 3.4 Efficiency as a function of f and L with N parameter for single-phase structure (N=1, blue) and the interleaved structures: (N=2; red, N=3; green, N=4; yellow, N=5; magenta).

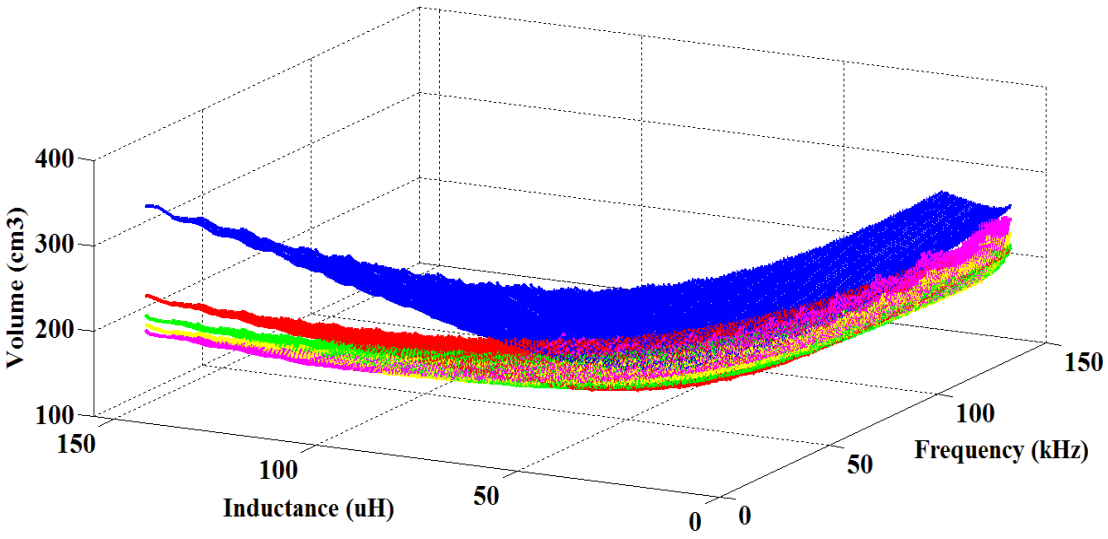


Figure 3.5 Volume as a function of f and L with N parameter for single-phase structure (N=1, blue) and the interleaved structures: (N=2; red, N=3; green, N=4; yellow, N=5; magenta).

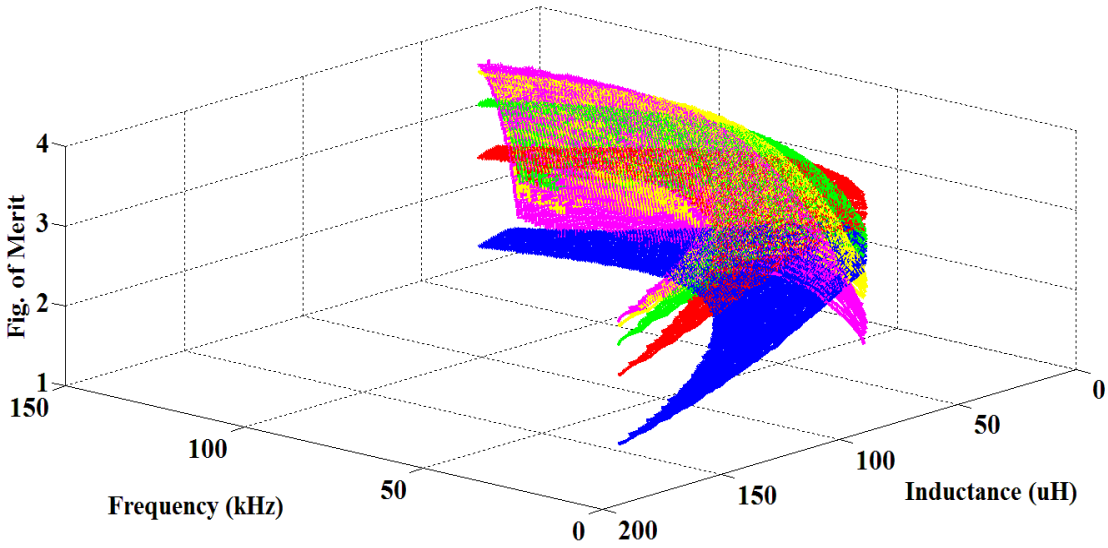


Figure 3.6 FoM as a function of f and L with N parameter for single-phase structure (N=1, blue) and the interleaved structures: (N=2; red, N=3; green, N=4; yellow, N=5; magenta).

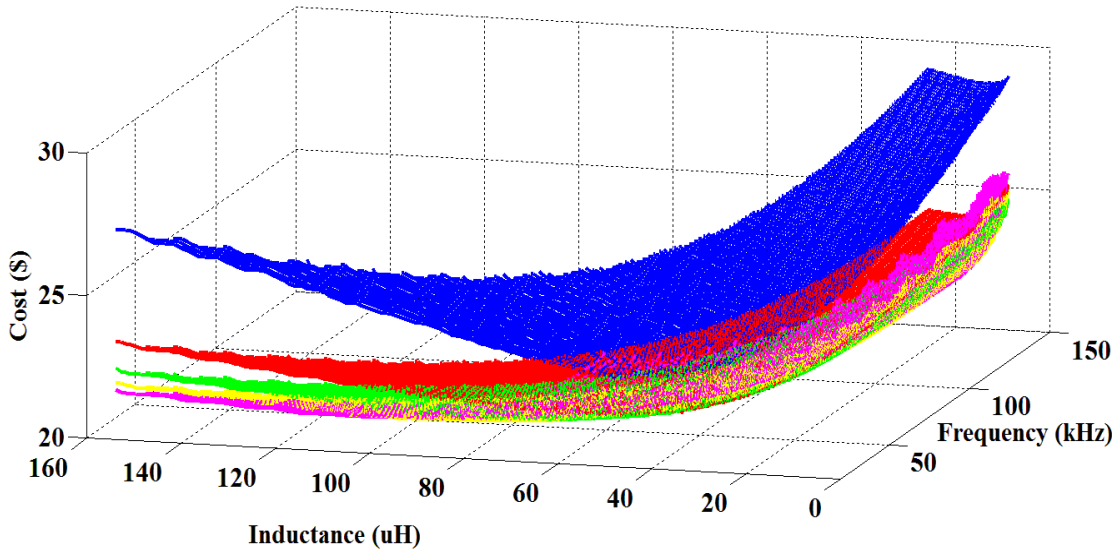


Figure 3.7 Cost as a function of f and L with N parameter for single-phase structure (N=1, blue) and the interleaved structures: (N=2; red, N=3; green, N=4; yellow, N=5; magenta).

Although visualization tools serve the purpose of showing an overall picture of change in the observed quantity with respect to the variables being changed, it may be hard to observe critical design targets such as maximum efficiency or minimum volume points. Therefore Table 3.6 is created to summarize those important points.

Table 3.6 Design extrema and their parameters

N	Quality	Eff. (%)	V_{TOT} (cm^3)	V_L/V_{TOT} (%)	FoM	f (kHz)	L (µH)	Cost ($)
1	Max. Eff.	96,64	187,97	37,58	2,58	31	41,82	22,80
	Min. Eff.	94,94	262,32	18,29	1,21	150	25,92	29,04
	Max. Vol.	95,68	316,55	65,02	1,18	25	152,41	27,14
	Min. Vol.	96,59	179,84	29,19	2,66	42	30,86	22,86
	Max. FoM	96,59	179,84	29,19	2,66	42	30,86	22,86
	Min. Cost	96,61	182,79	34,32	2,64	34	38,12	22,72
2	Max. Eff.	96,84	155,10	28,44	3,34	45	39,28	21,47
	Min. Eff.	95,86	209,35	21,83	1,87	145	8,94	25,02
	Max. Vol.	96,23	211,40	52,70	2,04	25	154,51	23,22
	Min. Vol.	96,82	154,02	25,43	3,34	55	38,33	21,54
	Max. FoM	96,83	154,32	27,25	3,35	48	37,92	21,45
	Min. Cost	96,82	157,21	31,98	3,27	36	46,92	21,38
3	Max. Eff.	96,89	146,84	26,09	3,58	60	46,04	21,07
	Min. Eff.	95,83	208,99	29,12	1,86	141	9,19	24,41
	Max. Vol.	95,95	213,89	30,20	1,87	144	9,00	24,61
	Min. Vol.	96,88	144,66	24,95	3,63	58	41,76	20,99
	Max. FoM	96,88	144,66	24,95	3,63	58	41,76	20,99
	Min. Cost	96,86	146,74	29,04	3,55	44	54,45	20,93
4	Max. Eff.	96,94	143,51	24,62	3,72	70	48,61	20,94
	Min. Eff.	95,52	226,03	35,91	1,59	139	9,32	24,83
	Max. Vol.	95,70	231,70	37,17	1,62	141	9,19	25,03
	Min. Vol.	96,89	139,89	22,42	3,77	76	39,80	20,81
	Max. FoM	96,91	140,44	23,71	3,78	71	43,71	20,78
	Min. Cost	96,85	142,06	28,01	3,66	48	57,01	20,69
5	Max. Eff.	96,93	139,53	23,51	3,79	84	46,29	20,73
	Min. Eff.	95,07	249,67	40,63	1,29	149	9,32	25,71
	Max. Vol.	95,32	250,69	40,47	1,36	142	9,13	25,77
	Min. Vol.	96,87	137,58	22,47	3,78	80	43,37	20,66
	Max. FoM	96,91	138,95	23,61	3,80	81	48,11	20,70
	Min. Cost	96,81	139,32	26,52	3,68	55	56,89	20,59

3.3.2 Examining the Overall Converter Behavior and Target Design Points under Varying f, L and N

Results of the analysis clearly demonstrate the importance of an efficiency and volume based analysis before the implementation of a converter: there exist different values of f and L which correspond to basic design goals like minimization of losses and volume or both (FoM maximization). General rules of thumb such as increase in switching frequency decreasing the passives' hence converter's overall volume and interleaving technique's volume reduction effect can be observed throughout the analysis. On the other hand: following aforementioned rules of thumb without any calculation of loss and volume with respect to varying parameters can lead the designer unexpected design outcomes such as a higher frequency converter which results in a bigger volume.

3.3.2.1 Examining the Results in View of Efficiency

While varying f, L, and N in the 1-kW hard switched buck converter example, efficiency changes between a maximum of 96.94% (which occurs for the maximum efficiency point for N=4 case) and a minimum of 94.94% (which occurs for the minimum efficiency point for N=1 case). Corresponding change in loss is 25.2 and 42.6 W respectively. If the maximum efficiency points are considered, an efficiency increase from 96.64% to 96.94% is possible with N is changed from N=1 to N=4. Since "equal current rating-equal inductance" approach is adopted and conduction losses are dominant for the converter of interest, a wide difference in the efficiency values is not observed. The factors creating difference in efficiency analysis can be stated as switching losses (which increases with the frequency), inductor losses (smaller inductors can offer decreased conduction losses and core loss is prone to current ripple and frequency) and the effect of current ripple in each phase. It was assumed that switches turn on and off with 300 A/μs. Under that assumption, interleaving results in lowered switching losses but rate of reduction in losses decrease with increasing number of phases. For interleaved converters, it should also be noted that every single-phase of the converter experiences the same current ripple of the non-interleaved converter as discussed in 2.2.5, “Considerations on the

Efficiency of Interleaved Power Conversion". This yields additional conduction and inductor losses and is the main reason why the efficiency increase obtained for the interleaved cases of the analysis saturates at N=4.

3.3.2.2 Examining the Results in View of Volume

From the converter optimization program's outputs, it can be observed that increase in f has volume reduction effect up to 60-80 kHz band (depending on number of phases), above that band, there is no gain in volume with increasing frequency due to the fact that little or no volume reduction is accomplished in inductors compared to the increase in heat sink volume because of the increased switching losses. This situation can be better observed by looking at the simplified volume versus inductance graph drawn for 25, 85 and 150 kHz frequency values for N=1 which is depicted in Figure 3.8.

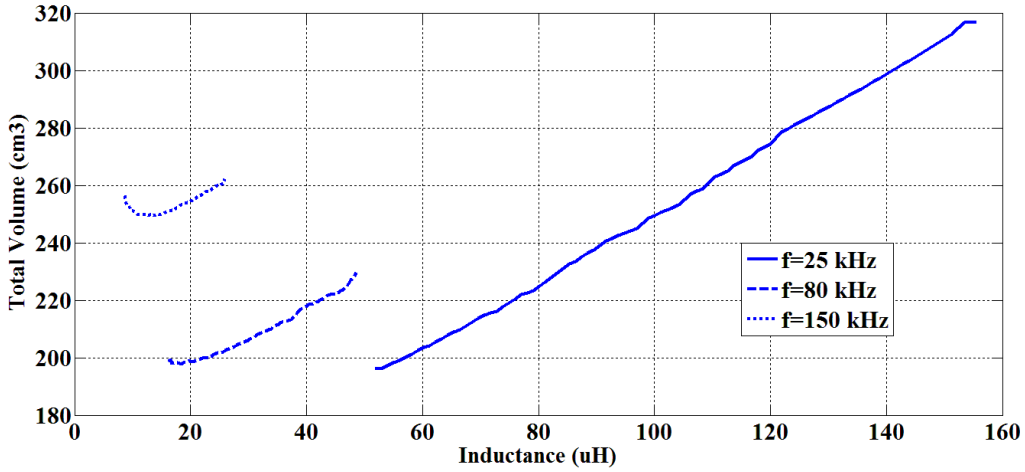


Figure 3.8 Total volume versus inductance at three different frequency values for N=1.

From the results of the optimization program listed Table 3.6 and Figure 3.5, it can be seen that interleaving boosts volume but the boosting effect quickly saturates for the converter example under consideration. Fig. 7.a-b show total volume versus f

when ripple is kept constant at 3.6 A (a) and 10.8 A (b) respectively. From Fig. 7.a, volume reduction benefit of interleaving and the decrease in rate of reduction can be observed. Fig. 7.b corresponds to minimum inductance - maximum current ripple hence maximum core loss case and explains why the maximum volume points for N>2 occur at high frequencies. This is due to the fact that all phases experiencing large amount of current ripple under high frequency yields serious core losses, which requires larger cores since all the inductors are designed to satisfy same thermal limit.

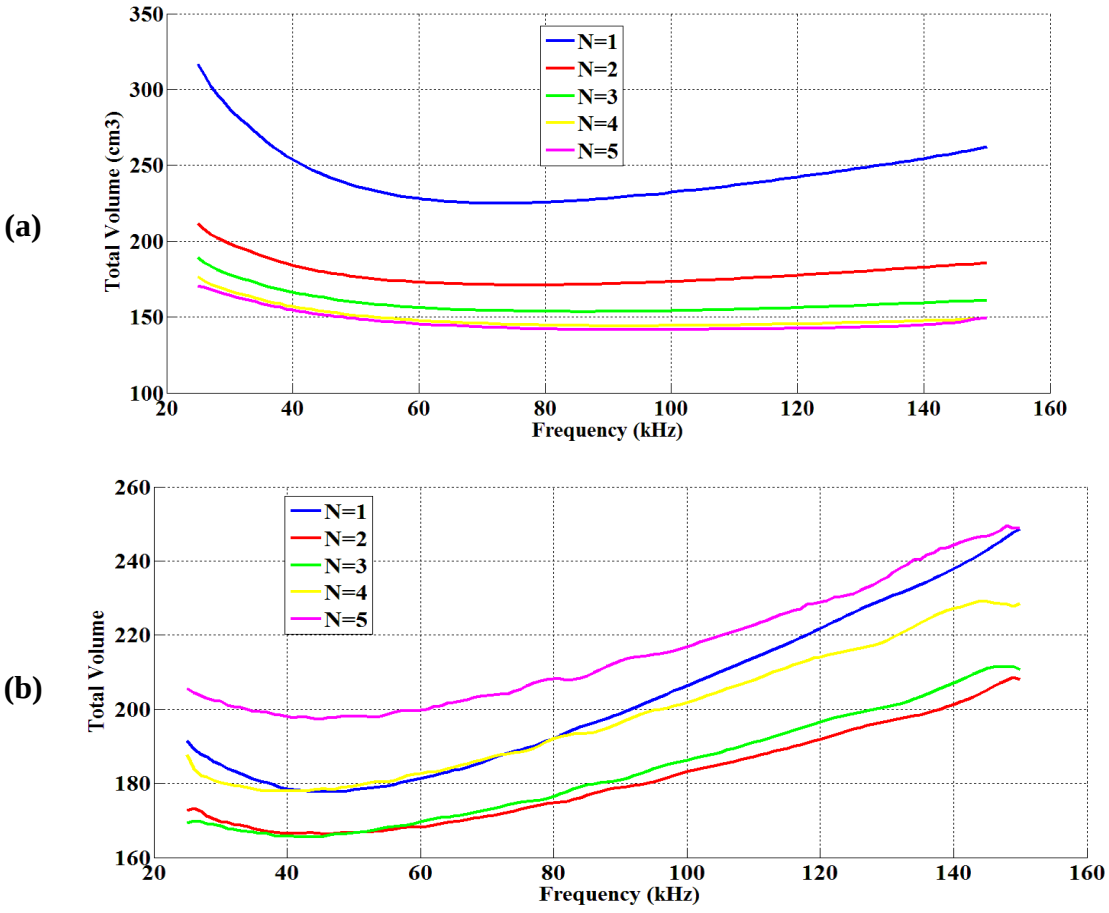
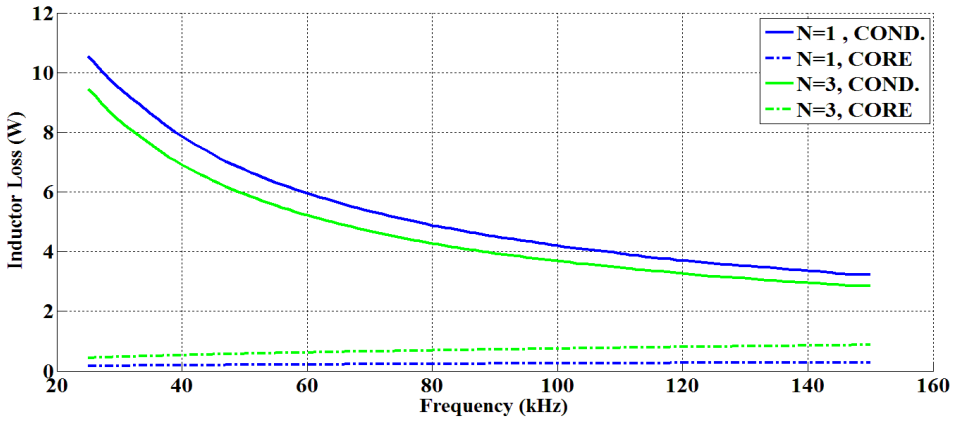


Figure 3.9 Volume versus frequency graph for minimum current ripple, ΔI=3.6 A (a) and maximum current ripple, ΔI=10.8 A (b) cases.

Examining inductor core and winding losses separately further explains results of Table 3.6 and Figure 3.9.a-b. In Figure 3.10.a-b, total core and winding losses are given for N=1 and N=3 cases for minimum and maximum current ripple situations respectively. As the frequency is increased and a large ripple in current hence core magnetic field is allowed, core losses have profound effect. Combining that with N, total inductor losses for multi-phase converter can exceed single-phase converter inductor losses. Although it seems reasonable to drastically decrease the inductance in a multi-phase buck converter, relying on the ripple cancellation property of interleaving, the resulting multi-phase converter may lack its single-phase counterpart in terms of both efficiency and volume while the designer expects just the opposite situation.

(a)



(b)

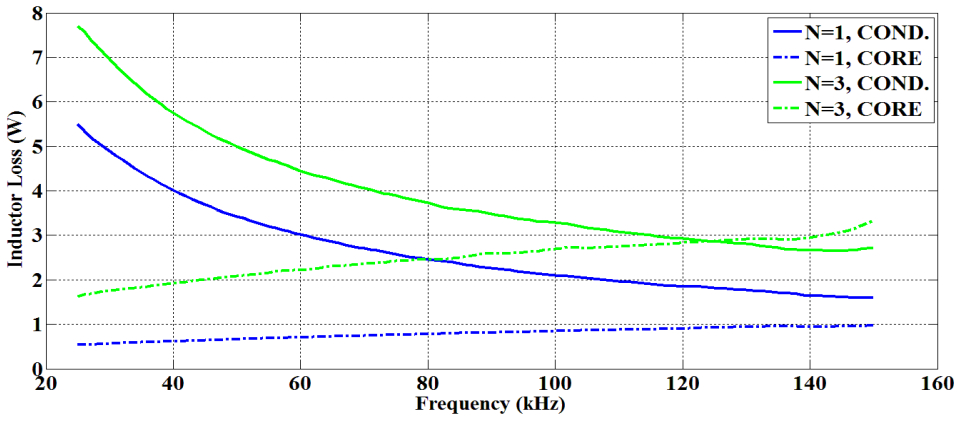


Figure 3.10 Core and conduction losses versus frequency for ΔI= 3.6 A (a) and ΔI=10.8 A (b) cases for N=1 and N=3.

3.3.2.3 Examining the Results in View of Cost

Examining the results listed in Table 3.6 and the cost graph of Figure 3.7, it is seen that cost varies between a minimum of 20.59$ and a maximum of 29.04$. Note that 12$ semiconductor cost is constant for all (f, L, N) points since equal current capacity approach is adopted for the analysis. It is also important to note the relation between maximum FoM and minimum cost points: they seem to lay very close if not the same for all values of N. This is due to the fact that when the extreme design points such as maximum volume and minimum efficiency are omitted, which is also the case for FoM maximization, cost values tend to minimize since it has a volume based calculation.

3.3.3 Optimum Design Point with FoM Comparison

Rather than efficiency and volume alone, a figure of merit was defined as the multiplication of relative gains in both volume and efficiency, to represent the optimal design point. Examining the (f, L) points where FoM maximization occurs for different N shows that a meaningful trade-off between volume and efficiency is obtained by avoiding extreme values.

Since both of the volume components namely heat sink and the inductors are designed with temperature rise limitations, there is a correlation between efficiency increase and volume reduction. It can be best observed with maximum efficiency, minimum volume and maximum FoM points occurring for close values of (f, L) sets.

Contributions of interleaving on converter volume and efficiency can be observed by the increase in FoM values. However, as N increases, increase in FoM values saturates. Considering that the main mechanism behind volume reduction benefit of interleaving is the total magnetics volume being reduced, further decreasing already reduced magnetics volume does not offer a serious volume advantage after N=3. Also, the presence of current ripple at each individual phase is a limiting factor.

In the analysis, highest FoM value is 3.80 and obtained for (f, L, N) = (81, 48.11, 5). Similarly, maximum FoM point for N=4 is nearly same with 3.78 and occurs at (f, L) = (71, 43.71). Depending on the characteristics of the application, a designer may promote some properties of the converter above others but from a general point of view, FoM maximization can be considered as the optimum design point. Since maximum FoM values for N=4 and N=5 are nearly identical, it is reasonable to adopt any of these (f, L, N) sets as the optimum design points. However, considering the input-output characteristics (56V input, 28V output) of the converter that is going to be implemented, N=4 case offers full ripple cancellation at the output due to the operating condition yielding a duty cycle of D=0.5. Furthermore, examining the maximum efficiency, minimum volume and maximum FoM points for N=4 show that these three design points occur for close values of frequency and inductance which also shows that there is not a considerable sensitivity in FoM values for that particular region of (f, L) set. Therefore, in view of the converter optimization study introduced thus far, the optimal (f, L, N) point chosen for the DC-DC converter that is going to be implemented is (f, L, N) = (75 kHz, 45 μH, 4 phases).

3.4 Summary

In this chapter, an optimization study aiming high power density for a DC-DC converter performing 56V to 28V conversion has been introduced. Frequency, inductance and number of paralleled phases as optimization parameters, an optimal (f, L, N) point is suggested for the converter of interest. The converter, whose implementation procedure and experimental results will be provided in Chapter 4, is designed according to that optimal (f, L, N) point suggested by the optimization study which is (f, L, N) = (75 kHz, 45 μH, 4 phases).

Rather than pointing an optimal design point alone, converter behavior in terms of efficiency, volume and cost under varying frequency, inductance and phase number has been described and necessary explanations provided.

The need for converter optimization is also highlighted: considering the change in crucial performance merits for a practical converter such as efficiency and volume with respect to the variables such as frequency, inductance and phase number, it can be seen that considerable gains can be made with a careful selection of these design parameters. Similarly, it is shown that an arbitrary selection of design parameters can yield a very low profile design outcome.

The boosting effect of interleaving on converter efficiency and volume is also examined with phase number varying between N=1 and N=5. Note that the optimization procedure also contains the study of phase number optimization of interleaved converters, which is most of the time decided according to the designer's former experience or just maximization input/output ripple cancellation of interleaving.

Although this study mainly focuses on the optimum design of an 800W interleaved buck converter, approach for optimization can be modified for different types of power converters with their own set of criteria.

CHAPTER 4

DESIGN AND IMPLEMENTATION OF A DIGITALLY CONTROLLED 1-kW INTERLEAVED DC-DC STEP DOWN CONVERTER

In this chapter, hardware implementation part of the thesis study will be documented. A 4-phase interleaved, digitally controlled, hard switching, 1-kW buck converter performing 56V to 28V DC-DC conversion has been implemented in view of the optimal (f, L, N) design point suggested by the optimization study described in the previous chapter. Various oscilloscope recordings will be provided for the presentation of the electrical power conversion performance. Efficiency and volume values are measured for comparison with analytical results. The implemented converter is also tested with different switching frequencies, inductors and switching speeds (smaller/larger gate resistances) to see these parameters' effect on converter performance. In addition to the 1-kW, 4-phase converter, a 2-phase 500W converter is implemented as a preparatory step for the actual converter. Electrical performance and efficiency measures for the 2-phase converter will also be presented. Furthermore, several variations of the optimal design are provided to test non-optimal design points.

4.1 Auxiliary Hardware Implemented

For the operation of the actual 1-kW converter, an auxiliary supply for gate driving and a resistive load bank which is capable of sinking 36A DC current are implemented. Before presenting the implemented converters, a brief description on these auxiliary components is to be introduced.

4.1.1 Auxiliary Gate Drive Supply

MOSFETs, being voltage controlled devices, are known for their ease of switching: simply applying a proper potential difference (10-15V) between the gate and source legs of a MOSFET with the source pin at ground potential (low-side MOSFET) results in the transition from blocking to conducting state. However, the source leg of a MOSFET being connected to a point with varying potential (high-side MOSFET), as in the case of a buck converter, complicates the gate driving process. For high side MOSFETs, three main gate drive techniques can be mentioned:

- Bootstrapping
- Transformer coupled gate driving
- Utilization of floating voltage supplies

A bootstrap gate drive circuitry is depicted in Figure 4.1. Main logic behind bootstrapping is to charge a bootstrap capacitor (C_{BOOT} in the figure) while the high side MOSFET is in the blocking state and applying the potential built up on that bootstrap capacitor between gate and source to turn the high side MOSFET into conduction state.

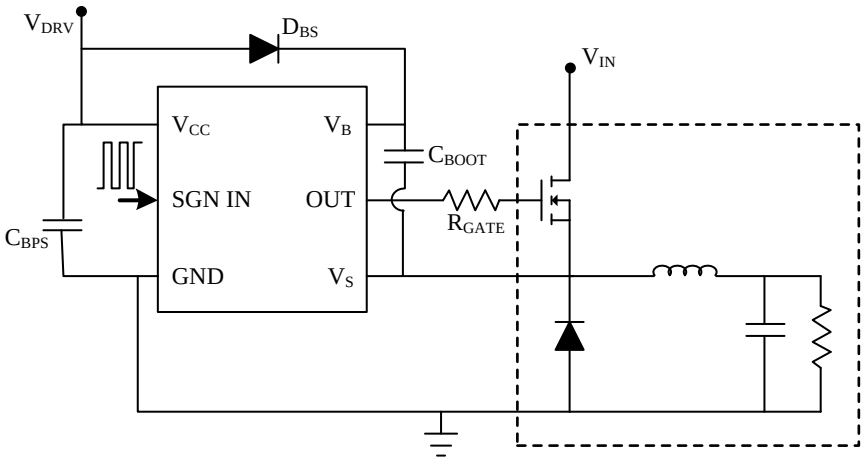


Figure 4.1 A simplified bootstrapping scheme for high side MOSFET driving.

Considering the fast switching speeds that MOSFETs exhibit and the impulsive nature of the currents that stems from fast switching, gate driving require careful placement of components and proper PCB design. The presence of stray inductances at MOSFET and diode legs may result in MOSFET source voltage going well below ground voltage at switching off instant which is a widely encountered problem. To overcome this problem, some slight yet effective countermeasures can be taken to protect gate drive circuitry and related components as depicted in Figure 4.2. A low forward voltage drop, fast schottky diode (D_S) is placed between V_S terminal and ground and gate resistor is placed at the return end to limit the added schottky diode's current.

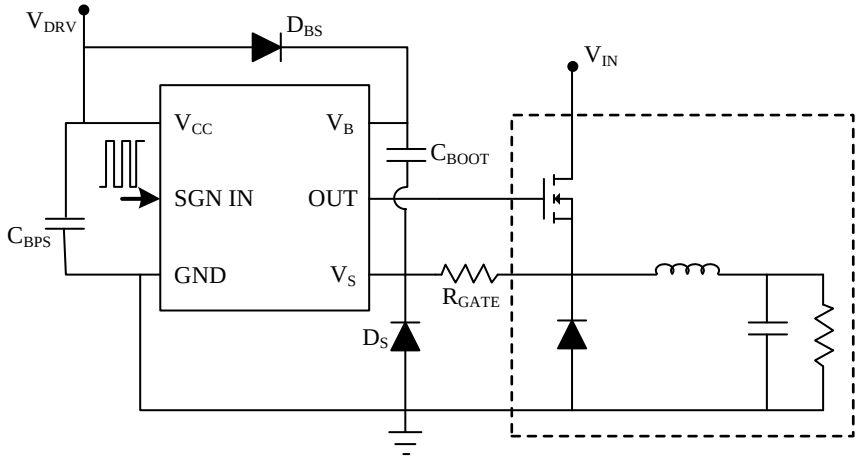


Figure 4.2 A simplified bootstrapping scheme for high side MOSFET driving with noise counter-measures.

Selection of bootstrap capacitor is important. It should be selected large enough such that the potential built up on the capacitor does not quickly fade away while maintaining current for the switching action. The relation (4.1) can be used for bootstrap capacitor selection. In equation (4.1), Q_{GATE} stands for gate charge for the MOSFET and Q_{OTHER} represents the addition of other charge components such as reverse recovery charge and the level shift charge that stems from the driver. The

terms V_F, V_{LS} and V_{UVLO} stand for forward voltage drop of the bootstrap diode (D_{BS}), forward voltage drop at the low side switch and the under voltage lock out value of the gate driver IC, respectively.

$$C \gg \frac{2.Q_{GATE} + Q_{OTHER}}{V_{CC} - V_F - V_{LS} - V_{UVLO}} \tag{4.1}$$

Basic countermeasures against noise for power electronic circuitry should also be taken at bootstrap gate drive design: components must be placed as close as possible and loop areas for impulsive currents must be minimized. Some additional components for start-up of the bootstrap gate drive are also common for applications such as battery charging however such details will not be covered here.

Transformer coupled gate driving is another common technique for high side gate driving. A simplified transformer coupled gate drive is depicted in Figure 4.3. Basic operation principle is to transfer the square wave pulses produced by PWM controller via a high frequency transformer which provides galvanic isolation and creates the necessary gate to source potential.

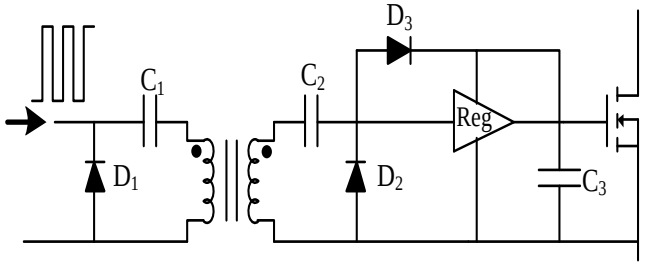


Figure 4.3 A simplified transformer coupled gate drive scheme for high side MOSFET driving.

For a comprehensive overview on MOSFET driving [61] can be referred. In this study, independent, floating voltage supplies are used for gate drive purposes.

Adjustable, 10 to 15V floating voltages are obtained via linear regulators which follow the rectification of low frequency transformers' (220V primary, 15V secondary) outputs as depicted in Figure 4.4. Although, the utilization of low frequency transformers for gate drive purposes is not an elegant way, this method is chosen for its simplicity since the focus of the converter implementation process is to attest the analytical results and provide a converter with superior input/output characteristics due to interleaving.

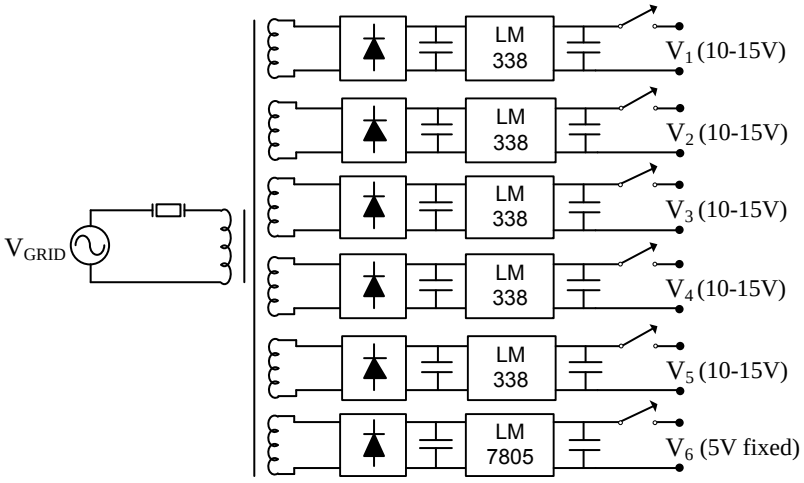


Figure 4.4 Circuit diagram of the auxiliary supply designed for gate driving.

A photo of the implemented auxiliary supply is given in Figure 4.5.

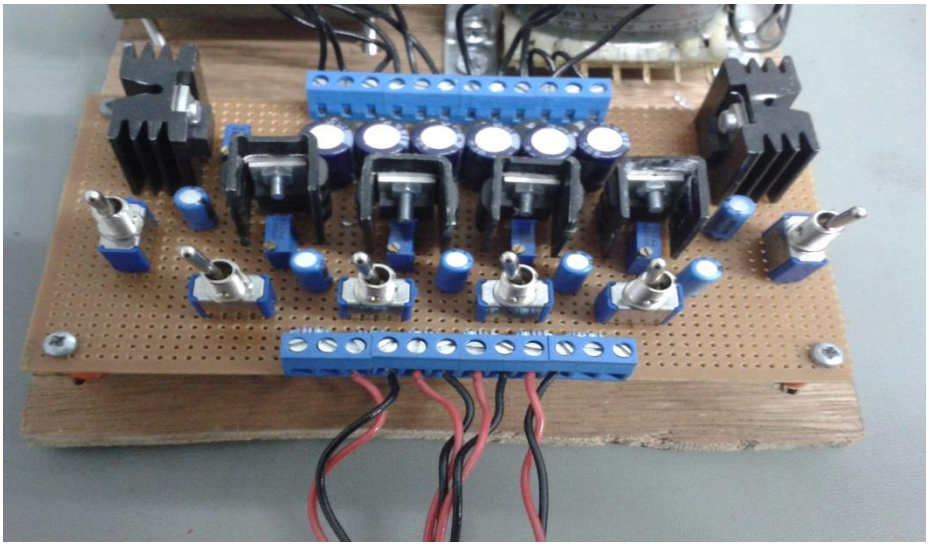


Figure 4.5 Photo of the auxiliary supply designed for gate driving.

4.1.2 1-kW Resistive Load Bank

To test the implemented converter with different loading levels, a resistive load bank that can be set to several resistance values is designed. Considering the output power (1-kW), resistors are mounted on heat sinks which are forced air cooled. Circuit diagram of the load bank is depicted in Figure 4.6.

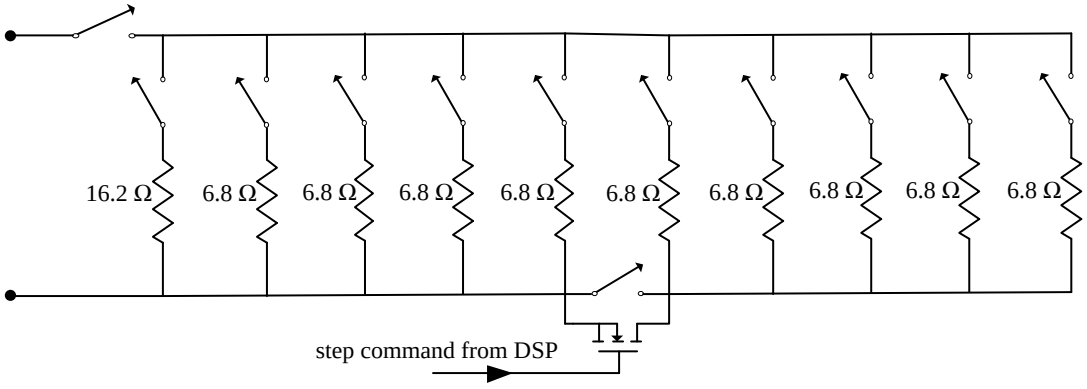


Figure 4.6 Circuit diagram for 1-kW, resistive load bank.

Each resistor has a metallic switch allowing the utilization of different loading levels. Two other metallic switches are included for 100% and 50% on-off switching. Note that, to test the transient performance of a converter for sudden changes at the load current, metallic switches exhibit poor performance. Therefore, a MOSFET is also provided to enable sudden loading / load removal tests. Turn on/off command is fed from the digital signal processor. A photo of the implemented resistive load bank is provided in Figure 4.7.

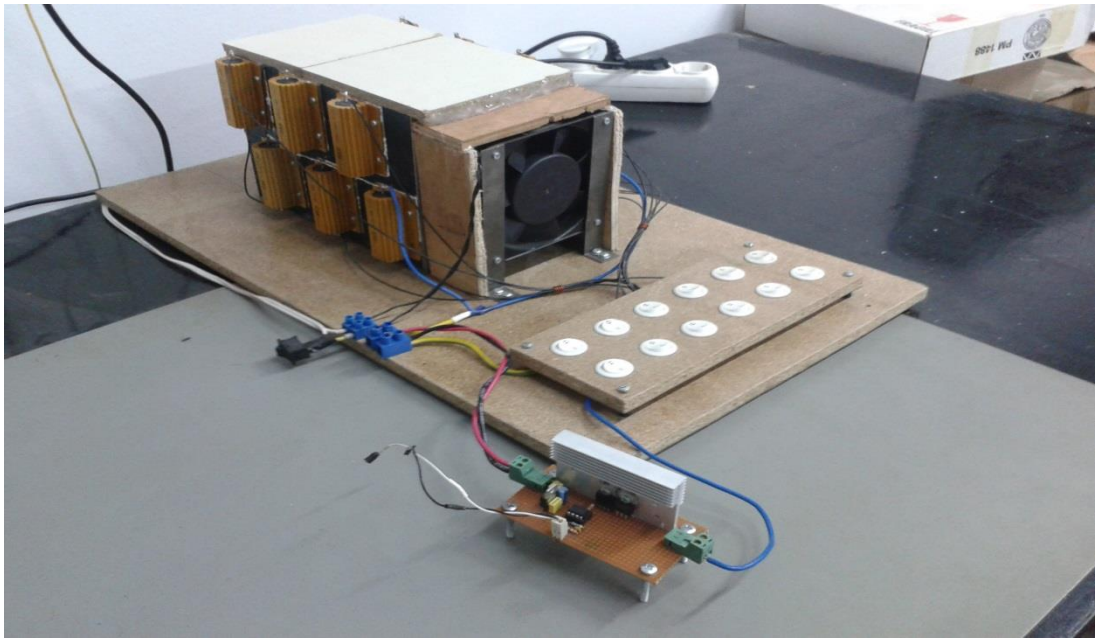


Figure 4.7 Photo of the 1-kW resistive load bank.

4.2 Laboratory Equipment Used for Hardware Implementation

Considering the voltage and power level of the target converter to be implemented, it can be seen that a high performance DC supply is required. Therefore, a programmable DC power supply with the model name 62012P-80-60 produced by Chroma is utilized for the testing of the implemented converter. The device has maximum voltage and current limits of 80V and 60A respectively and can provide

up to 1.2kW. Further information on the device can be found on the datasheet provided by its manufacturer [62].

An oscilloscope with model number TPS2024 produced by Tektronix is used to observe important waveforms during the testing of the implemented converter. TPS2024 has four isolated channels each having 2 GS/s sampling rate and 200 MHz bandwidth [63]. For the observation of current waveforms, current clamps produced by Fluke under the name i30s are utilized which have 20 A maximum current rating and 100 mV/A reading sensitivity [64].

Converting 56V at the input to 28V at the output yields 18A input and 36A output current for 1-kW operation. For a reliable efficiency analysis, a careful measurement of input and output voltage and currents values is a must. However, the output current level severely exceeds the maximum rating of the current clamps utilized with the oscilloscope, posing a threat for the current clamp devices. Therefore, two wattmeters under the brand name Hioki 3334 are used for the efficiency tests. These wattmeters can measure current up to 30A and are the highest current rating devices available for the thesis study. In addition to their higher current rating compared to Fluke i30s current clamps, it was seen that Hioki3334 wattmeters offer higher precision measurements as the TPS2024 oscilloscopes having ±3% DC voltage reading accuracy. Noting that the current rating required for the measurement of the output current under full load operation (36A) still not satisfied, efficiency analyses are carried out at 800W operation which corresponds to 28A output current. Further information on the wattmeters can be found on the datasheet provided by the manufacturer [54].

In this study, the implemented converters are controlled via a digital signal processor (DSP). The chosen DSP is TMS320F28335 of Delfino family microprocessors produced by Texas Instruments. Having 150 MHz clock frequency, 16 ADC and 18 PWM channels [65], the selected DSP is more than enough to meet the requirements that the target converter possesses. An experimenter kit, which houses the DSP "TMS320F28335" along necessary connections and utilities [66] is used as the controller unit for the implemented converters.

4.3 Design and Implementation of a Two-Phase, 500W Step-Down Converter

Before the implementation and testing of the target converter with optimized (f, L, N) values suggested by the study documented in Chapter 3, a two-phase 500W version is implemented as a preparatory step for the actual converter to gain insight in both hardware implementation and digital control. Note that, the two-phase converter is not designed according to an optimization study: frequency, inductance and phase number parameters are selected intuitively. Electrical input/output characteristics are the same: 56V DC input is to be converted into 28V DC at the output corresponding to 18A maximum output current for 500W operation.

The two-phase converter utilizes DCR current sensing method. After a brief description on DCR current sensing, the simulation study and its outputs will be presented. Finally, the implemented converter will be introduced: important oscilloscope waveforms regarding the converter performance will be provided along efficiency and volume analyses.

4.3.1 DCR Current Sense Method

Current mode control is a widely utilized control technique for practical power converters and as the name implies, obtaining current information and feeding it into the control system is required. Current monitoring is even more important for interleaved power conversion: equal current distribution between phases currents should be maintained to prevent unequal thermal stresses that may yield converter failure.

Using a dedicated current sensor being the most straightforward solution, one common way for current sensing is to put high-precision resistors across current paths and measure the voltage drop on the resistor. Note that this kind of an approach yields in a decreased efficiency and is not suitable especially for high current applications. MOSFET $R_{DS,ON}$ can also be used as a sense resistor to provide current information, preventing the extra loss that would occur for the utilization of current sense resistors. Decreased accuracy is the main drawback for this technique

since $R_{DS,ON}$ values can significantly differ between MOSFETs of the same brand and they are temperature dependent.

One elegant way of lossless current sense is to connect an RC network in parallel to a practical inductor having an effective resistance R_L as depicted in Figure 4.8.

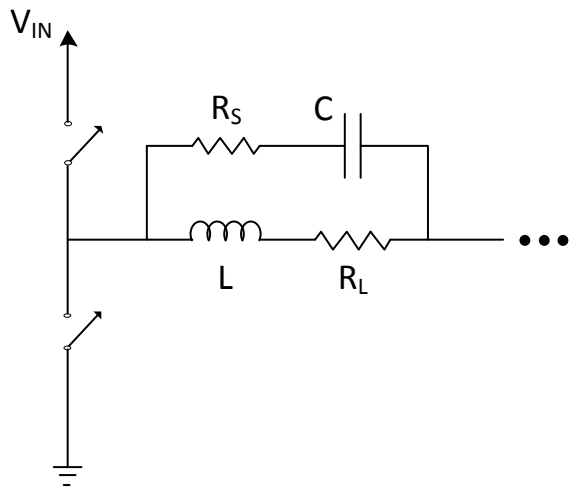


Figure 4.8 A simplified scheme for DCR current sense technique.

Once the equation (4.2) is satisfied, that is the time constants of RL and RC networks are equal, the voltage on the capacitor mimics the voltage across R_L, the effective DC resistance of the inductor. Once the effective resistance of the inductor is known, accurate current information can be obtained by the observation of capacitor voltage.

$$R_S.C = \frac{L}{R_L} \tag{4.2}$$

Factors such as the dependence of L and R_L values on frequency and temperature, component tolerances affect the accuracy of DCR current sensing. On the other hand, R_S and C values do not influence the DC level observed; only the AC part of the inductor current deviates at the presence of a time constant mismatch. Further

analyses on DCR current sense technique are provided in [67,68]. It is also important to note that, the voltage across the sense-capacitor which bears the inductor current information is a high side voltage and cannot be fed into a controller as it is. The capacitor voltage must be transformed into a current signal which has the same voltage value but referenced to signal ground, via a differential amplifier.

A DCR current sensing example is provided in Figure 4.9. An RC network of 470 nF capacitance and 10k pot is connected across a 320 µH inductor and the resistive pot is adjusted such that time constants are matched. As Figure 4.9 shows, voltage developed across the capacitor (Channel 1) is a scaled down version of the actual inductor current (Channel 2).

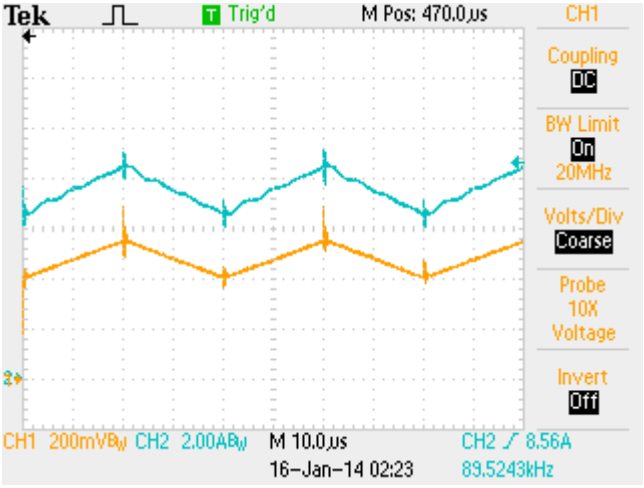


Figure 4.9 A DCR current sensing example: sense-capacitor voltage (CH1: 200mV/div) and inductor current (CH2: 2A/div, 10µs/div).

Note that, for the implementation of two-phase converter, values adopted for current sense-capacitor and resistor are larger than equation (4.2) suggests: since average current mode control is targeted and average phase currents should be monitored for equal phase current distribution, careful matching of the R_L-L and C_S-R_S time constants to precisely sense the AC component of the inductor current is not

required. By the significant increase in RC time constant, only the DC current value of the inductor currents are sensed and fed back to the controller. AD629 difference amplifiers [69] are utilized to convert sense-capacitor voltage reference to signal ground.

4.3.2 Computer Simulations for the Two-Phase 500W Converter

Computer simulations are carried out to guide the implementation step. SIMPLORER, which is a simulation program designed especially for power electronics applications [70], has been used. The converter scheme for the simulation procedure is depicted in Figure 4.10.

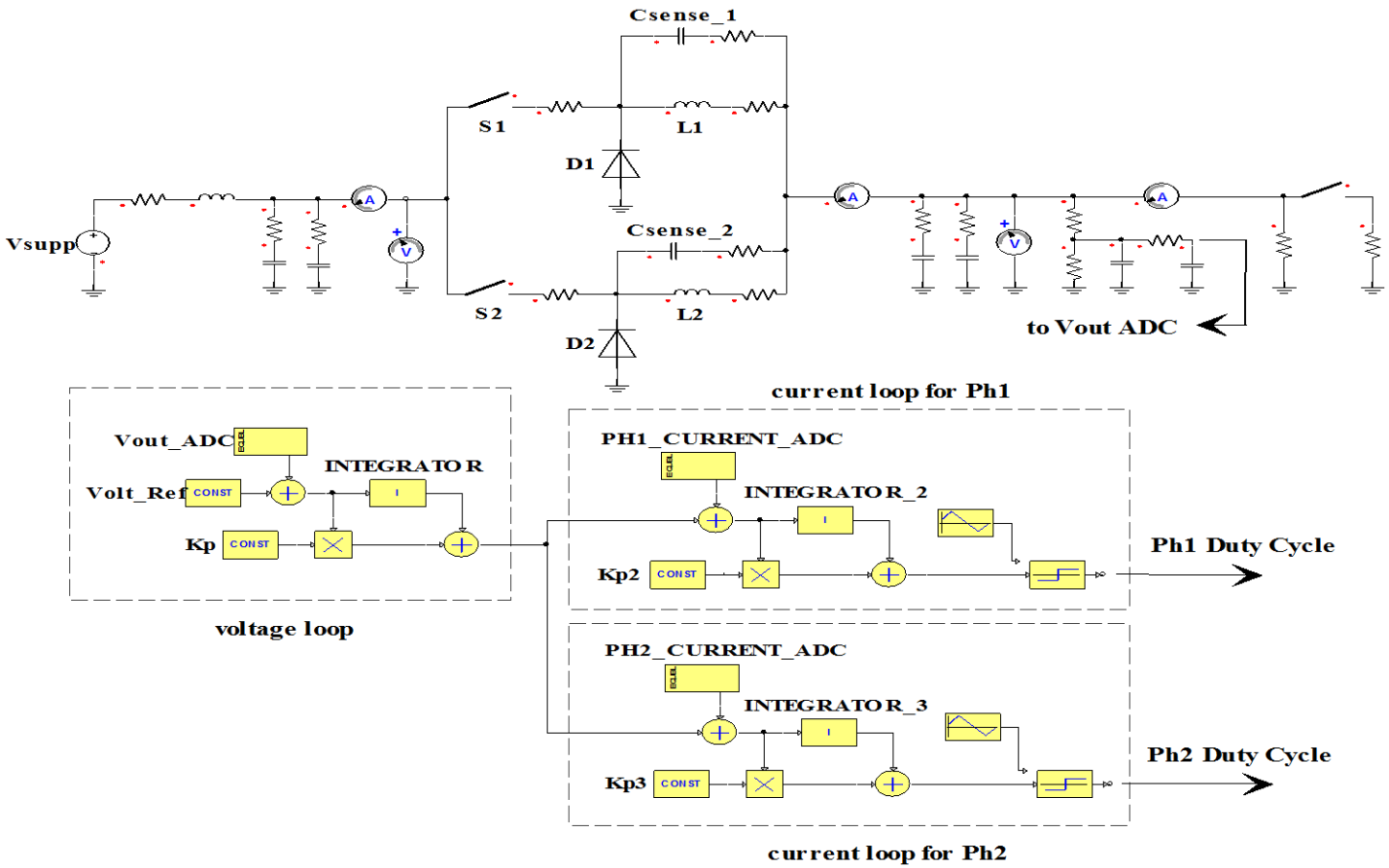


Figure 4.10 Simulation screen for two-phase 500W converter.

The converter scheme depicted in Figure 4.10 had been updated along the implementation study: ESR values of components such as power switches, electrolytic capacitors and inductors are measured with an LCR meter and taken into account at the simulation step for a more successful modeling of the actual converter. Even the parasitic components at the connection between the converter and the supply are tried to be modeled since a considerable voltage drop at the input was observed at the implemented converter due to the non-ideal power supply that it is connected to and the connection between. Important parameters related to the simulation are listed in Table 4.1.

Table 4.1 List of important simulation parameters for the two-phase, 500W converter.

Supply Voltage	56V
Output Voltage	28V
Maximum Output Current	18A
Frequency	25kHz
Inductance (at each phase)	320μH
Phase Number	2
Input Capacitance	21.4μF
Output Capacitance	42.5μF
MOSFET $R_{DS,ON}$	40mΩ
Diode V_F and r_T	0.6V and 10mΩ
DC resistance of inductor	50 mΩ

The control blocks utilized at the simulation represents the related sub-modules of the DSP: by placing equation blocks which read the output voltage and phase currents at 40 ms time intervals and converting the incoming data into a number

between 0 and 4095 (0 for 0V and 4095 for 3.3V), the ADC operation of the DSP is imitated. Then, PI controllers process the error signals and two 180˚ phase-shifted PWM signals for the parallel phases are created in accordance to the operating principles of the DSP's PWM module.

Important waveforms obtained by the computer simulation are given in Figure 4.11-4.16. In Figure 4.11, supply voltage and the output voltage of the converter are depicted to illustrate the steady state conversion performance.

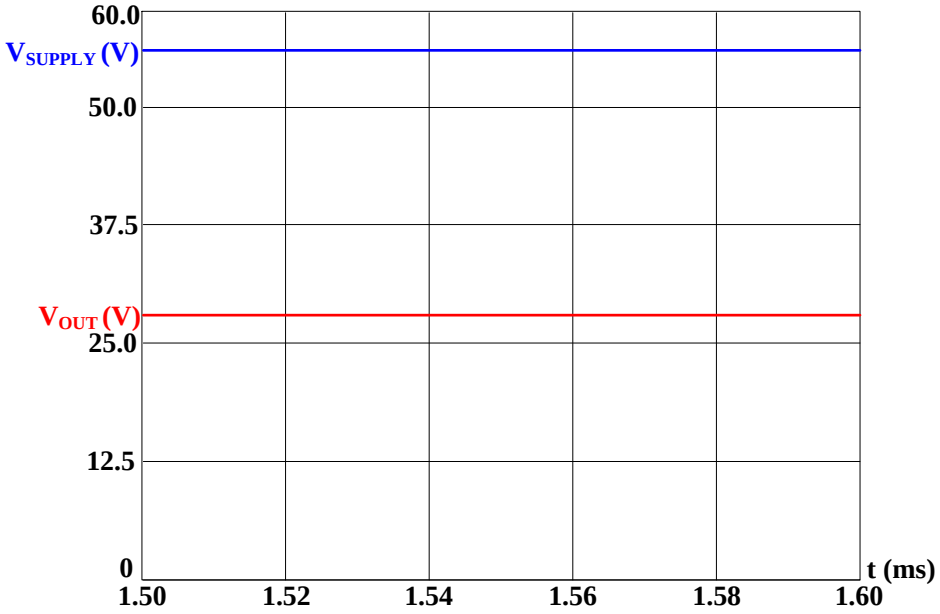


Figure 4.11 Supply voltage and the output voltage of the simulated two-phase converter at steady state.

Input and output current waveforms are provided in Figure 4.12. Note that a continuous input current is achieved due to the interleaving.

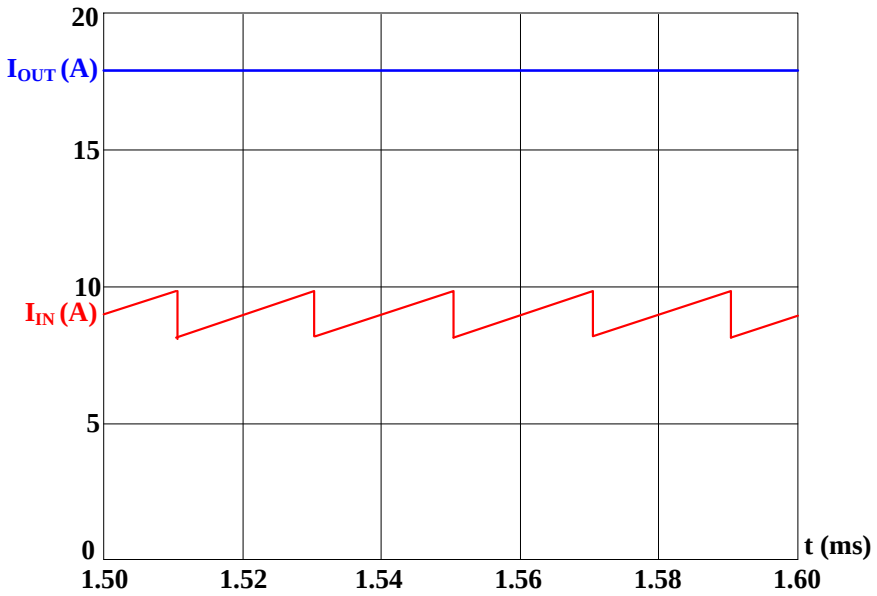


Figure 4.12 Input and output current waveforms of the simulated two-phase converter at steady state.

Voltage ripples at the input and output are given in Figure 4.13 and 4.14 respectively. Note that, under ideal conditions interleaving results full ripple cancellation for D=0.5 and N=2 case, however non-ideal components having effective resistances yields a duty cycle greater than 0.5 for 56V to 28V conversion. Therefore, a small output voltage ripple can be expected. Similarly, a voltage ripple at the input is not expected under ideal conditions, however since the power supply used at the implementation step and the connections between supply and the converter are not ideal, which is also represented at the simulation, a small but non-zero voltage ripple can be observed at the input.

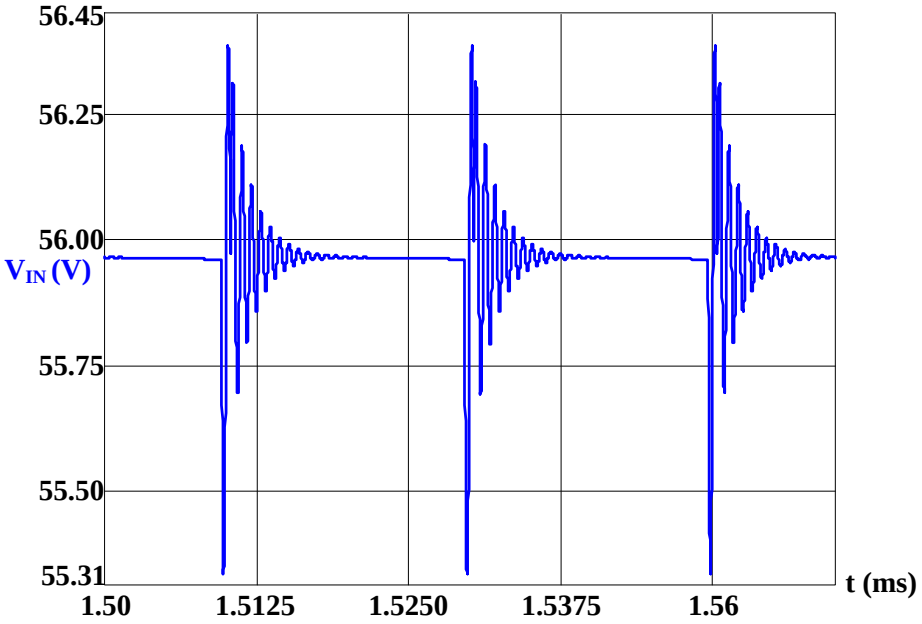


Figure 4.13 Input voltage ripple for the two-phase 500W converter.

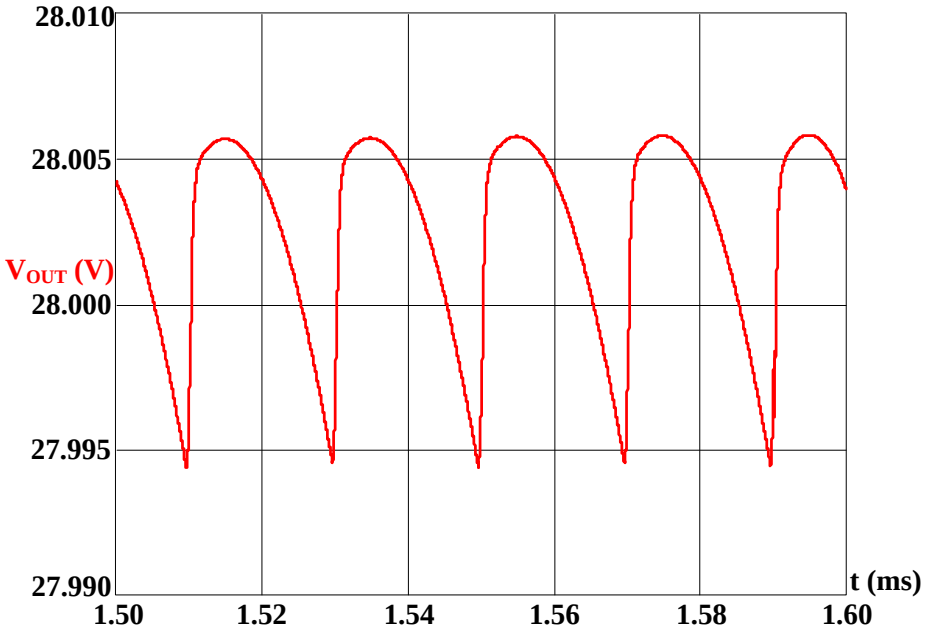


Figure 4.14 Output voltage ripple for the two-phase 500W converter.

Frequency multiplication property of interleaving technique can be observed from the input and output ripple waveforms given in Figures 4.13 and 4.14. Although the switching frequency is set to 25 kHz which corresponds to a 40 µs period, period for the input and output ripple is 20 µs which corresponds to 50 kHz. Considering that a higher frequency waveform is easier to filter compared to a lower frequency one, increasing the effective frequency without the cost of increased switching losses is another benefit of interleaving.

Current waveforms for phase inductors are depicted in Figure 4.15 which is also very explanatory for interleaved operation: current ripples for 180˚ phase shifted waveforms cancel each other at the output which yields a near-pure DC current.

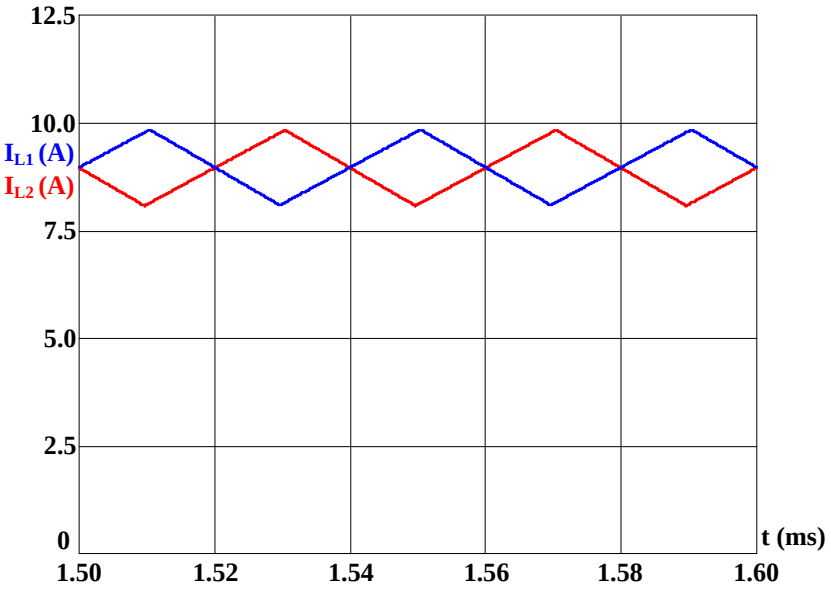


Figure 4.15 Inductor current waveforms of the simulated two-phase converter at steady state for the two-phase 500W converter.

4.3.3 Performance Analysis on the Implemented Two-Phase, 500W, Digital Controlled Step-Down Converter with Non-Optimized f-L-N Parameters

In view of the explanations introduced thus far, a two-phase interleaved, 500W, digitally controlled DC-DC step down converter, photo of which is depicted in Figure 4.16, has been implemented.

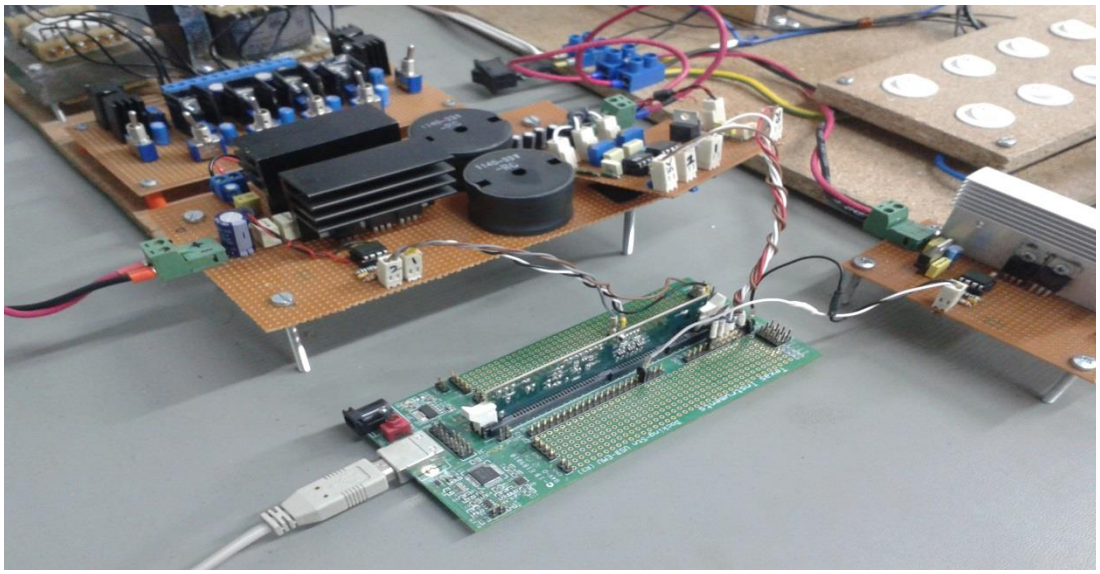


Figure 4.16 Photo of the two-phase interleaved, 500W, digitally controlled DC-DC step down converter.

At each phase, 100V 44A MOSFETs with product name IXTP44N10T [71] are utilized as the main switches. For diodes, 100V 10A schottky diodes with product name MBR10100CT [72] are used. Although it is not very effective practice to parallel diodes for higher current rating, two diodes are used in parallel at each phase since the current rating of a single device has nearly no safety margin considering that the full load phase current will be 9A. 320µH 11.4A inductors with product name 1140-331-RC [73] are utilized.

During the implementation process, both voltage mode and current mode control methods are applied and with voltage mode control, where phase current information

is not used, it is seen that there is no considerable phase current imbalance which requires forced current sharing. PI controllers are adopted for the control loops and coefficients are determined by a trial and error approach in both simulation and experimental studies. Since the focus of this study is to pursue high power density with an emphasis on interleaving, optimization of control methods or frequency domain stability analysis will not be provided here.

Oscilloscope waveforms that show important voltages and currents will be provided to document the power conversion performance of the implemented converter. Figure 4.17 shows the input and output voltages at steady state. Note that the output is precisely set to 28V and controlled via a multimeter and the power supply feeding the implemented converter provides smooth 56V. It is the DC error of the oscilloscope that yields the input and output recordings of 28.3 and 57.2 respectively.

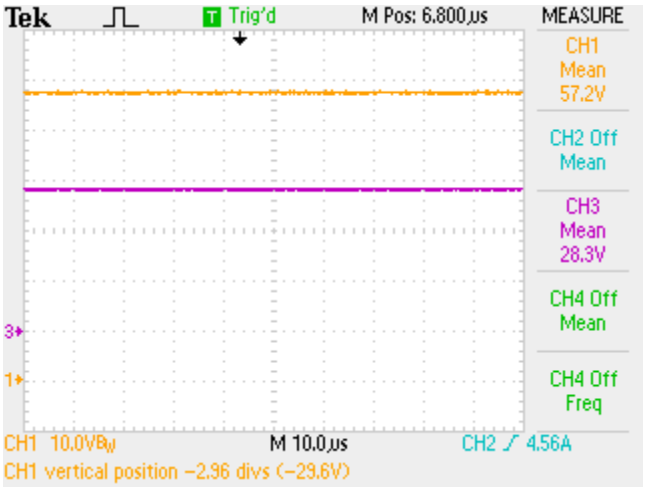
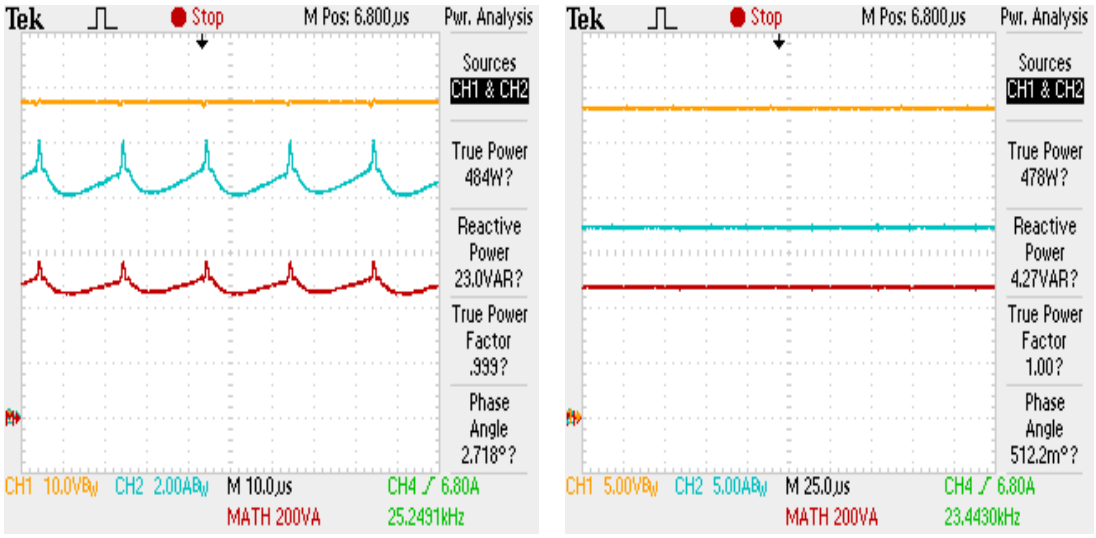


Figure 4.17 Input (CH1: 10V/div) and output (CH3: 10V/div, 10µs/div) voltages for the non-optimal converter.

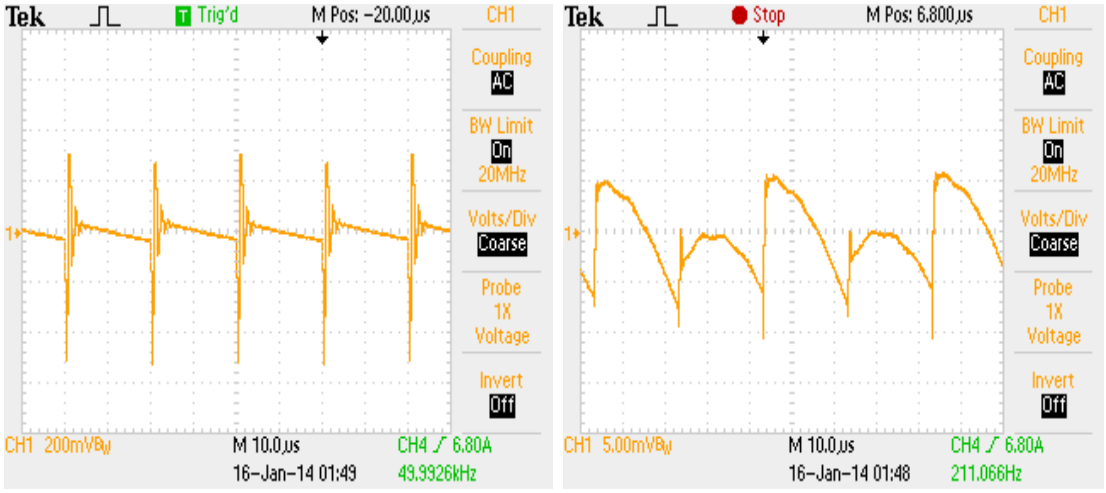
Input voltage, input current and their multiplication which gives input power are shown in Figure 4.18-(a). Waveform recording that contains output voltage, current and power is provided in Figure 4.18-(b). Note that the input current does not have a pulsating waveform which would occur for a single-phase converter.



(a) **(b)**

Figure 4.18 Input (a) (CH1: 10V/div, CH2: 2A/div, MATH: 200VA/div, 10µs/div) and output (b) (CH1: 5V/div, CH2: 5A/div, MATH: 200VA/div, 25µs/div) voltages, currents and powers for the non-optimal converter.

Voltage ripples at the input and output are depicted in Figure 4.19 (a) and (b) respectively which also clearly show the ripple cancellation property introduced by interleaving. Neglecting spikes, input voltage ripple is roughly 500mV and the output voltage ripple is 13mV. As already explained in the simulation results, zero ripple would be expected for the ideal case. However, very small yet non-zero ripples at the input and output occur due to the non-idealities of the supply and the components used in the implementation. Nonetheless, 10mV voltage ripple, which corresponds to 0.046% for 28V output, is a very good performance figure for a practical DC-DC converter.



(a) **(b)**

Figure 4.19 Input (a) (CH1: 200mV/div) and output (b) (CH1: 5mV/div, 10µs/div) voltage ripples for the non-optimal converter.

As a further exemplification on interleaving technique, Figure 4.20 can be referred where phase currents and their sum are depicted. It can be seen that due to the near-total cancellation of the inductor current ripples, a DC output current is obtained which does not require a considerable filtering by the output capacitor stage.

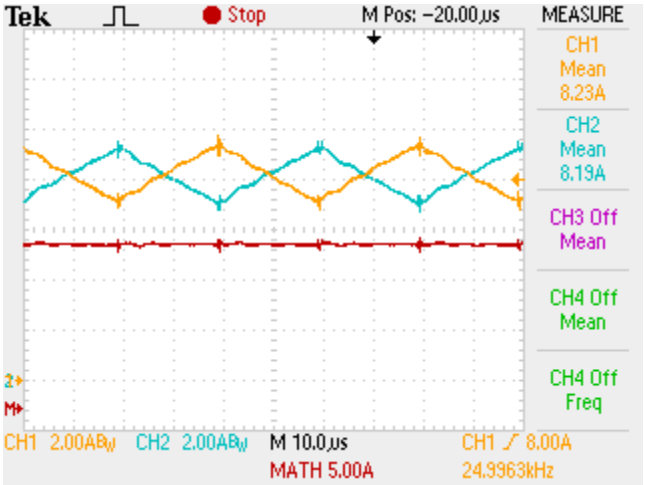
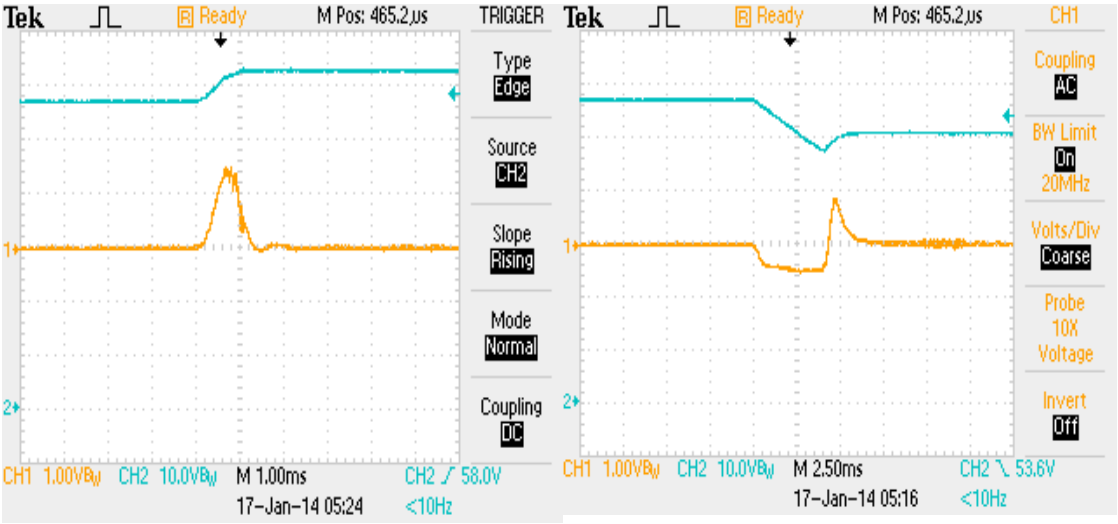


Figure 4.20 Phase currents (CH1-CH2: 2A/div) and their sum (MATH: 5A/div, 10µs/div) for the non-optimal converter.

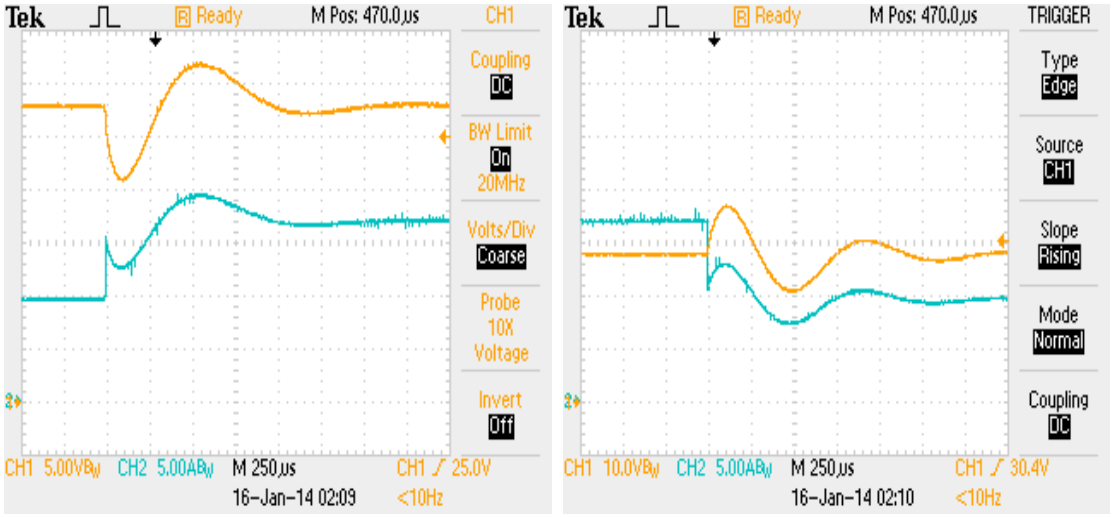
The implemented converter has been tested for line regulation: using the programmability property of the power supply, input voltage has been changed ±5V while the converter was supplying its rated power at the rated voltage (56V). As the input goes up and down by 5V, corresponding change at the output is depicted in Figure 4.21. Although the rate of change that the power supply can provide is far from being "sudden", it is important to see that the implemented converter can tolerate the change.



(a) **(b)**

Figure 4.21 Output voltage (CH1: 1V/div) waveform as the input (CH2: 10V/div) goes up (a) (1ms/div) or down (b) (2.5ms/div) by 5V from the rated voltage (56V) for the non-optimal converter.

Similarly, response of the implemented converter for a sudden change in the resistance of the load is depicted in Figure 4.22.



(a) **(b)**

Figure 4.22 Output voltage (CH1: 5V/div) and current (CH2: 5A/div, 250µs/div) waveforms for the sudden decrease (a) and increase (b) of the load resistance for the non-optimal converter.

Utilization of TMS320F28335, which is a powerful DSP, as the controller of the converter, brings additional abilities. Considering that the processor is not overloaded with the execution of controller operations and main mechanisms required for the control of a power converter such as PWM generation or signal reading by ADC are hardly a burden for the DSP, the implemented converter is equipped with some crucial abilities that a commercial power converter should have. As an example, the implemented converter has under voltage lock-out (UVLO) property: it does not try to convert power if the input voltage is below 48V. Similarly, over voltage protection (OVP) inhibits the converter operation for input voltages greater than 63V. Phase current measurements are used for over current protection (OCP): when an overcurrent is detected in any of the phases, converter stops all its operations and requires a reset to continue. Finally, the converter starts with increasing its voltage reference from zero to the actual value slowly, enabling soft-start operation (SS) which is depicted in Figure 4.23.

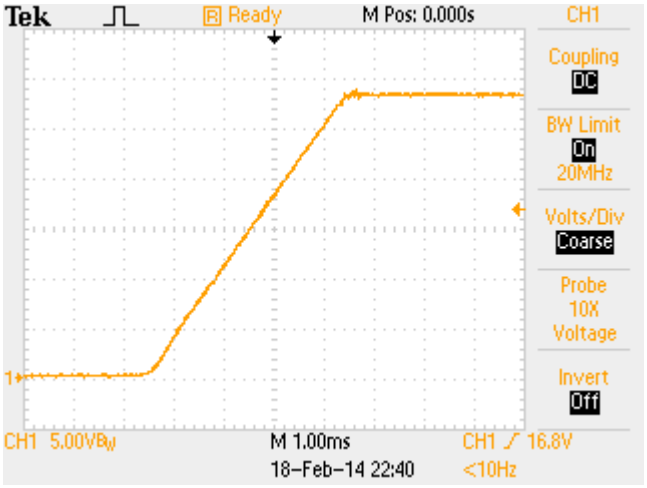


Figure 4.23 Soft-start operation for the non-optimal converter (CH1: 5V/div, 1ms/div).

By the utilization of different loading levels and measuring input and output powers with Hioki3334 wattmeters, efficiency versus load characteristics of the converter was obtained and depicted in Figure 4.24. Looking at the figures, it can be said that satisfactory efficiency values are obtained for a hard switching converter implemented with ordinary power switches.

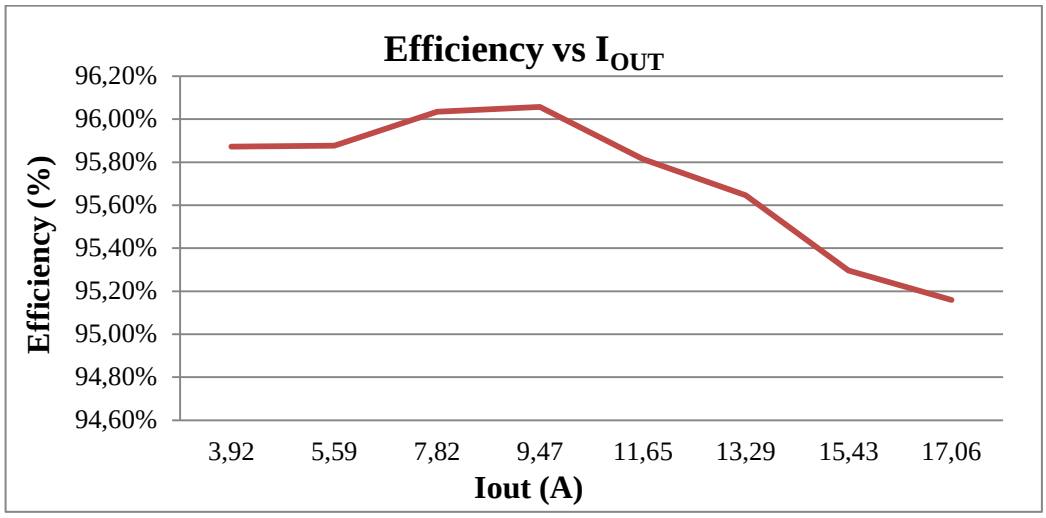


Figure 4.24 Efficiency versus load current graph for the non-optimal converter.

To conclude the examinations on the two-phase 500W step-down converter, Table 4.2 is created to summarize important converter characteristics. Note that in Table 4.2, the term "volume" corresponds to heat sink and magnetics volumes combined. Being a preparatory step for the implementation of the actual 1-kW converter with optimized f-L-N values, valuable knowledge on practical converter design, basic noise counter-measures and DSP programming is obtained.

Table 4.2 List of important performance figures for the two-phase, 500W converter.

V_{IN} Ripple (V)	0.5
V_{IN} Ripple (%)	0.89
V_{OUT} Ripple (mV)	13
V_{OUT} Ripple (%)	0.046
Full Load Efficiency (%)	95.16
Average Efficiency (%)	95.72
Total Inductor Volume (cm^3)	60
Total Heat Sink Volume (cm^3)	73
Total Volume (cm^3)	133
Power Density (W/cm^3)	3.75
Under Voltage Lock-Out	✓
Over Voltage Protection	✓
Over Current Protection	✓
Soft Start	✓

4.4 Design and Implementation of the Optimal Converter

According to the optimum (f, L, N) design point that the study introduced in Chapter 3 suggests, a four-phase, hard switched 1-kW DC-DC step down converter has been implemented with the aid of hardware experience gained through the design of two-

phase converter described in the previous part. Important converter properties are listed in Table 4.3. Interleaved buck converter topology is depicted in Figure 4.25.

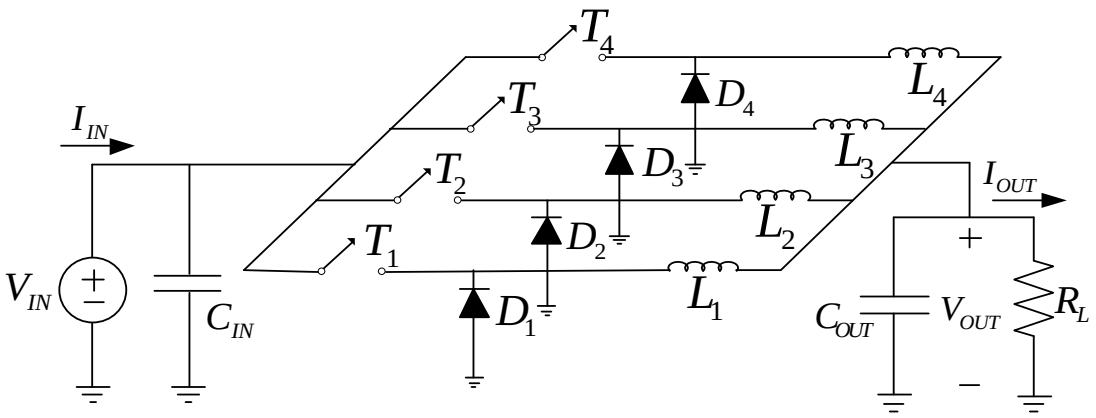


Figure 4.25 Four-phase interleaved buck converter topology.

Table 4.3 List of important parameters for the optimal converter.

Supply Voltage	56V
Output Voltage	28V
Maximum Output Current	36A
Rated Output Power	800W
Maximum Output Power	1000W
Frequency	75kHz
Inductance (at each phase)	45µH
Phase Number	4

Before continuing with the descriptions on simulation and implementation phases of the converter design, first a brief explanation on the handcrafted inductors which utilize Kool µ powder cores will be provided.

4.4.1 Inductor Design

Two sets of inductors (each contains four identical inductors for the four phase operation) are prepared by the utilization of the inductor design program introduced in Chapter 3 and some iterations. Maximum output current for the converter is 36A which corresponds to the maximum inductor current of 9A with four phase operation. Considering the degradation of permeability with respect to the applied DC bias explained in "Inductor Design" part of Chapter 3, inductors are prepared such that overall permeability degradation does not exceed 50% under 10A inductor current (1A being the safety margin). A maximum temperature rise of 40 ˚C is assumed. Inductor design program, which has been revised many times during this study, suggests the utilization of a core pretty much the same as the "Kool μ" powder core with part number 77894A7. Therefore, four inductors with 9A DC current rating having 45μH inductance under full current are produced. Additionally, another set of four inductors are implemented which corresponds to an overdesign case: cores with part number 77259A7 , that have 10.5 cm^3 core volume which is considerably more than enough for the application of interest, are utilized for the realization of 50μH under 9A DC current. Important core properties and figures for the inductors that are implemented with these core types are listed in Table 4.4 and Table 4.5 respectively.

Table 4.4 List of important core properties for 77894A7 and 77259A7.

Core Part Number	**77894A7**	**77259A7**
Initial Permeability	60	75
Cross Sectional Area (mm^2)	65.4	107.2
Magnetic Path Length (mm)	63.5	98.4
50% Roll-Over NI Value (A.turns)	415	525
Volume (cm^3)	4.15	10.5
Weight (gr)	24	62.3
MTL for 40% Winding Factor (mm)	41	54

Table 4.5 List of important figures for the inductors that are implemented with cores 77894A7 and 77259A7.

	With 77894A7	**With 77259A7**
Number of Turns	30	25
Inductance at No-Load (μH)	67.5	63.1
Inductance at 9A Loading (μH)	45	50
Effective DC Resistance (mΩ)	17	19
Core Loss (for I=7A, ΔI=3.8A, f=75kHz) (W)	0.71	0.68
Conduction Loss (for I=7A) (W)	0.83	0.93
Overall Inductor Volume (cm^3)	11	22

A photo of the implemented inductors is depicted in Figure 4.26.

Figure 4.26 Implemented inductors with cores 77259A7 (left) and 77894A7 (right).

For the two-phase converter introduced in the previous chapter, unshielded ferrite inductors with part number 1140-331-RC produced by Bourns were utilized. To compare the ferrite inductor 1140-331-RC of Bourns to the manually implemented inductor with the Kool μ core part number 77894A7, Table 4.6 is created.

Table 4.6 Comparison between 1140-331-RC and the inductor made using 77894A7.

	77894A7	**1140-331-RC**
Inductance (μH)	45	320
Energy Stored for Full Rated Current (mJ)	1.8	20.8
Volume (cm^3)	11	30
Energy Density (mJ/cm^3)	0.18	0.69
Effective DC Resistance (mΩ)	17	50

Examining the results of Table 4.6, it can be seen that the ferrite inductor of 1140-331-RC enables higher energy in smaller volume whereas the inductor utilizing the powder core 77894A7 exhibits lower losses. Note that core loss data for the ferrite inductor has not been provided by its manufacturer. Another fundamental difference between the inductors is the EMI issue; 1140-331-RC exhibits poor performance since it is made of a ferrite rod with a coil wound around, it pumps the magnetic flux all around itself. On the other hand, magnetic flux is very much trapped inside the toroidal core for the 77894A7 case. Figure 4.27 shows the voltage induced across the terminals of a 20 turn search coil placed in the vicinity of the ferrite inductor. For the inductor made of Kool μ toroidal core, there occurs no perceivable voltage waveform.

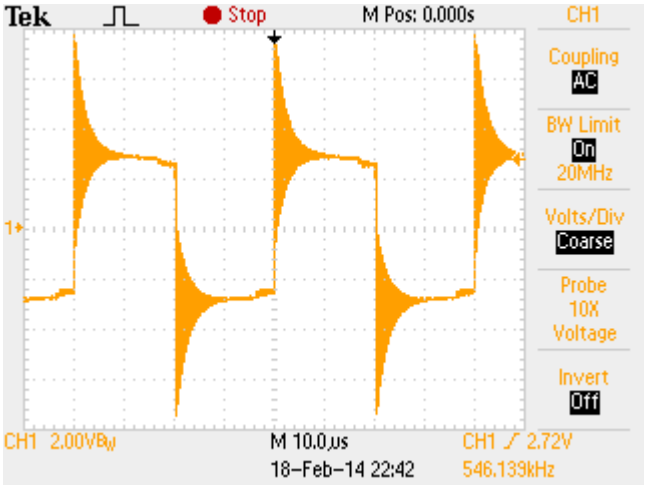


Figure 4.27 Voltage developed across the terminals of a 20-turn search coil placed in the vicinity of the inductor, 1140-331-RC (CH1: 2V/div, 10µs/div).

4.4.2 Computer Simulations for the Implementation of the Optimal Converter

As in the case of two-phase converter, a simulation study has been carried out to aid the implementation step. Having acquired the (f, L, N) parameters as (75 kHz, 45µH, 4 phases) from the optimization study of Chapter 3, only the control block is to be designed and converter performance should be checked for proper operation. Note that since there is no input or output voltage ripple expected for the ideal conditions, the amount of capacitance at input and output is found by experimental iterations rather than using ripple formulas and the resultant capacitance values are updated at the simulation. Again, the converter simulation is tried to reflect the actual converter operation by a careful modeling of component non-idealities and DSP structure. In this case however, only the voltage mode control is considered. Important simulation parameters for the optimal converter are depicted in Table 4.7.

Table 4.7 List of important simulation parameters for the four-phase, 1-kW converter.

Supply Voltage	56V
Output Voltage	28V
Rated Output Current	28A
Maximum Output Current	36A
Frequency	75kHz
Inductance (at each phase)	45μH
Phase Number	4
Input Capacitance	34μF
Output Capacitance	7.87μF
MOSFET $R_{DS,ON}$	50mΩ
Diode V_F and r_T	0.6V and 10mΩ
DC resistance of inductor	17mΩ

The converter scheme prepared for simulation via SIMPLORER is depicted in Figure 4.28.

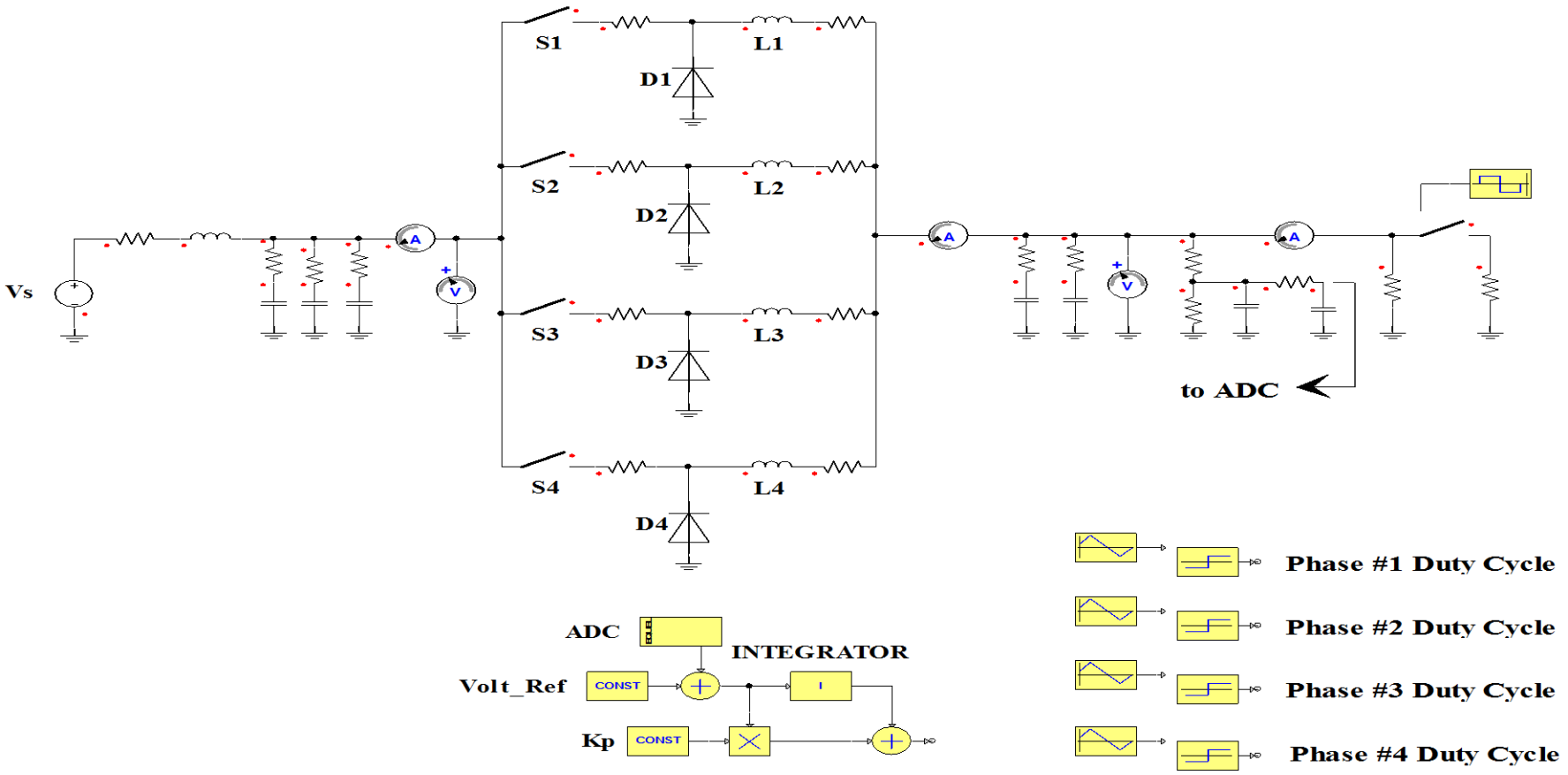


Figure 4.28 Simulation screen for the optimal converter design.

Important waveforms obtained by the computer simulation are given in Figure 4.29-4.35. In Figure 4.28, supply voltage and the output voltage of the converter are depicted to illustrate the steady state conversion performance.

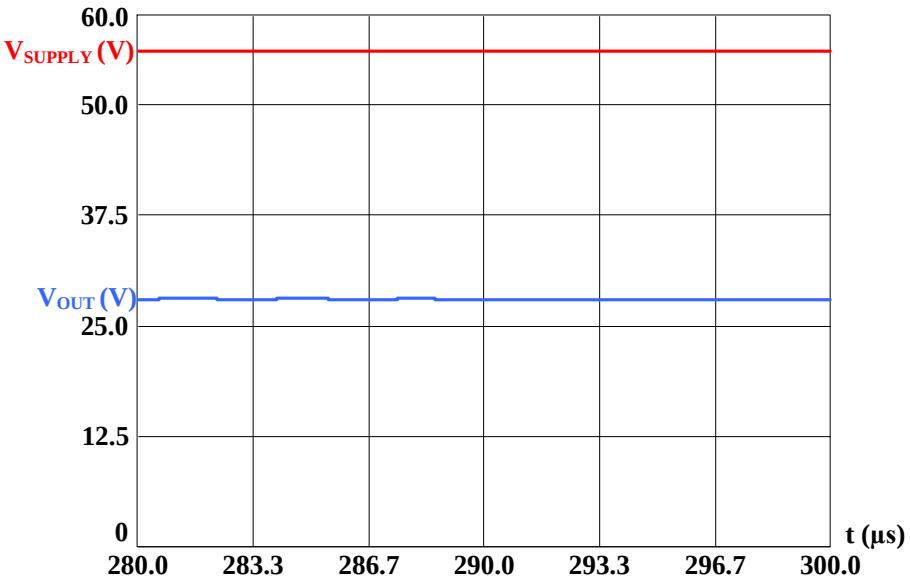


Figure 4.29 Supply and output voltage of the simulation for optimal converter.

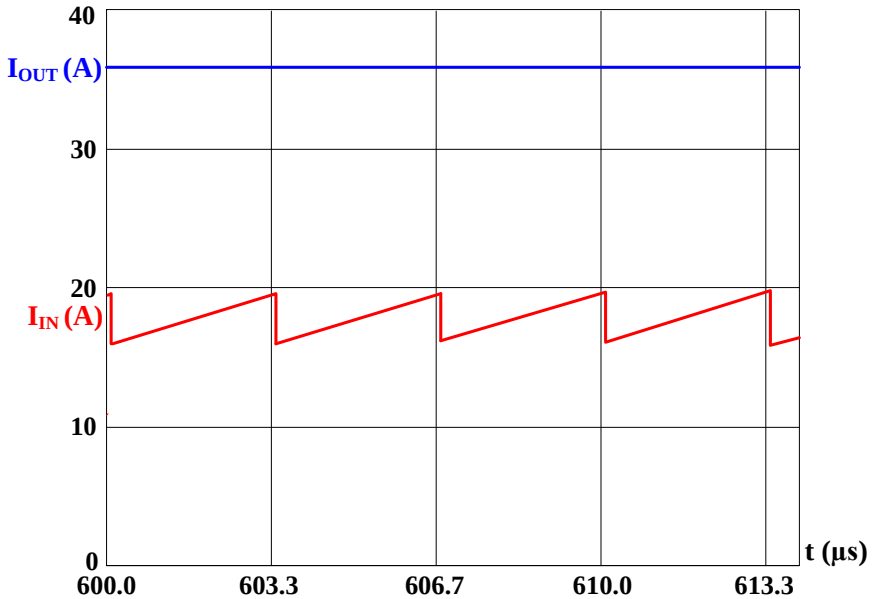


Figure 4.30 Input and output currents of the simulation for the optimal converter.

Input and output current waveforms are also provided in Figure 4.30. Note that a continuous input current is achieved due to the interleaving. Input and output voltage ripples are depicted in Figure 31 and 32 respectively.

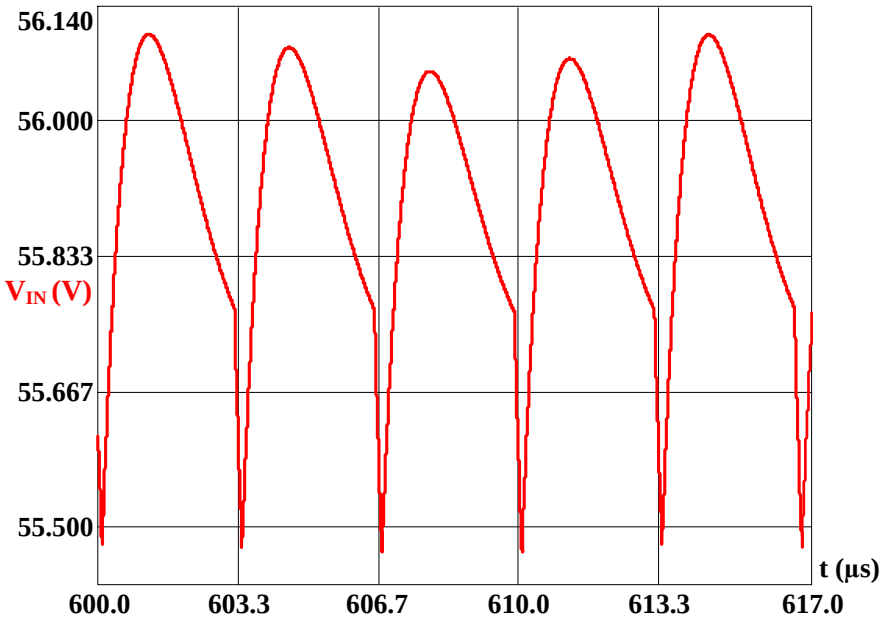


Figure 4.31 Input voltage ripple of the simulation for the optimal converter.

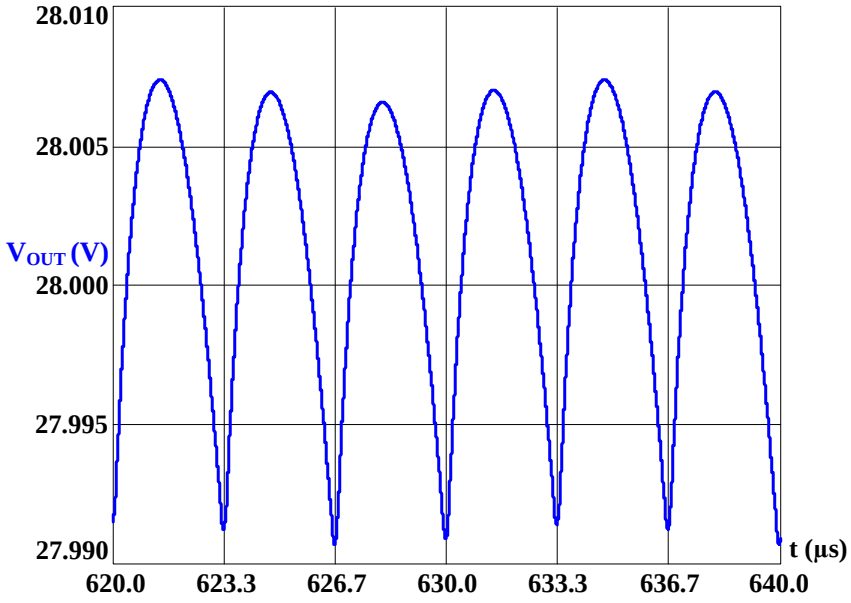


Figure 4.32 Output voltage ripple of the simulation for the optimal converter.

As in the case of two-phase converter simulation waveforms, frequency multiplication property of interleaving technique can be observed from the input and output ripple waveforms given in Figures 4.31 and 4.32. Although the switching frequency is set to 75 kHz which corresponds to a 13.33 µs period, period for the input and output ripple is 3.33 µs which corresponds to 300 kHz. Considering that a higher frequency waveform is easier to filter compared to a lower frequency one, increasing the effective frequency without the cost of increased switching losses is another benefit of interleaving.

Current waveforms for phase inductors are depicted in Figure 4.33 which is also very explanatory for interleaved operation: current ripples for 90˚ phase shifted waveforms cancel each other at the output which yields a near-pure DC current.

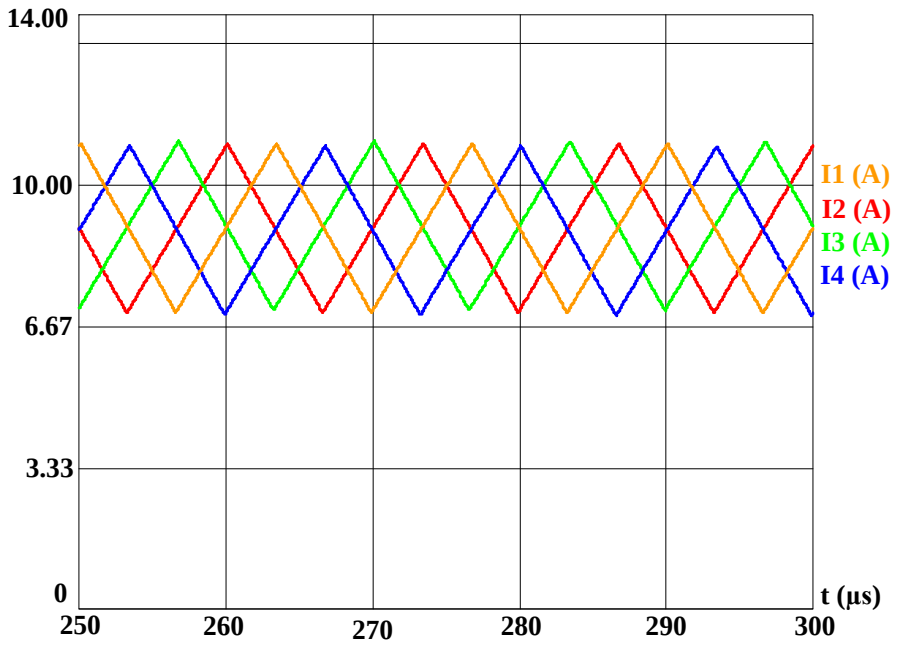


Figure 4.33 Phase current waveforms of the simulation for optimal converter.

Output voltage and current waveforms for an instant change in load step-up are depicted in Figure 4.34. Similarly, Figure 4.35 depicts the same waveforms for load step-down.

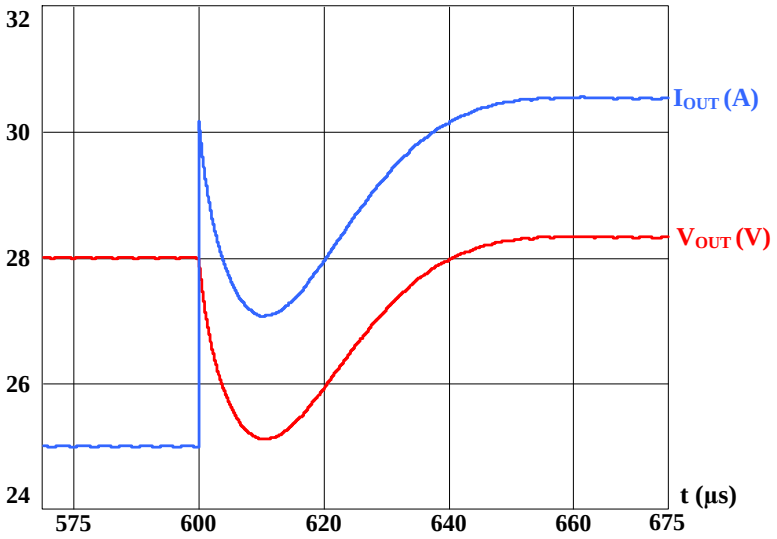


Figure 4.34 Output voltage and currents waveforms for an instant drop at the load resistance for the optimal converter.

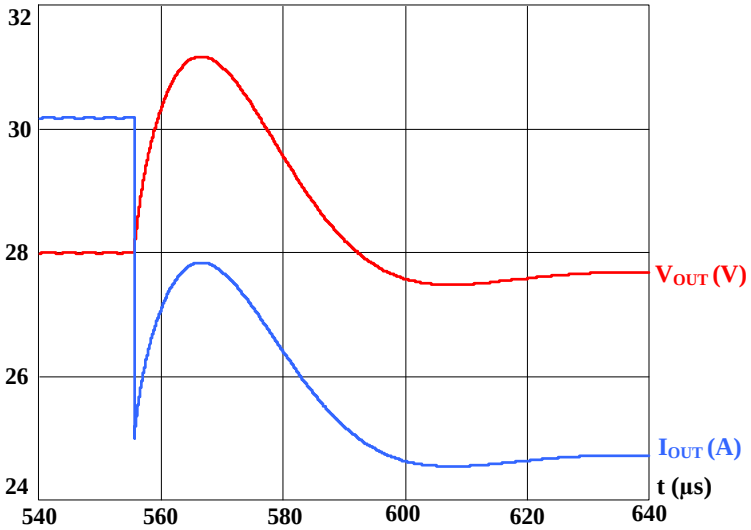


Figure 4.35 Output voltage and currents waveforms for an instant increase at the load resistance for the optimal converter.

4.4.3 Performance Analysis on the Implemented Four-Phase, 1-kW, Digital Controlled Step-Down Converter with Optimized f-L-N Parameters

The converter, (f, L, N) parameters of which have been determined by an optimization study as (75kHz, 45µH, 4phases), has been implemented in view of the previously introduced computer simulations. 100V 33A IRF540 [74] MOSFETs have been utilized as main switches for the buck topology and a paralleled scheme of two 100 V 10 A schottky diodes DSA10I100PM [75] has been utilized as the low-side switch. Inductors that exhibit 45µH inductance under 9A have been manually prepared as discussed in Part 4.4.1. Photo of the implemented converter can be seen on Figure 4.36. This time, only the voltage mode control is adopted for the implemented converter since there is no serious current imbalance between phases.

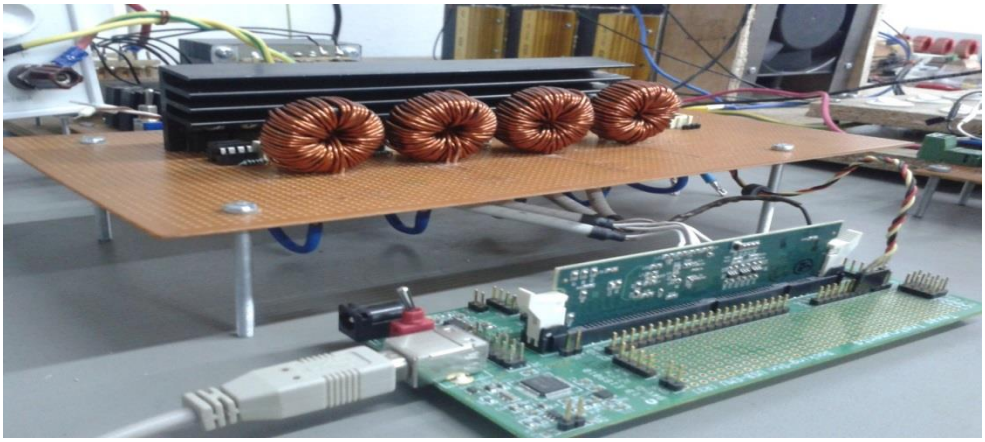


Figure 4.36 Photo of the four-phase interleaved, 1-kW, digitally controlled DC-DC step down converter with optimized (f, L, N) parameters.

Detailed oscilloscope waveforms will be provided for a complete analysis on the electrical conversion performance of the implemented converter. Figure 4.37 depicts

the input and output voltage waveforms. Note that the average values for input and output voltages which are 56.7V and 28.8V respectively stems from the DC reading error of the oscilloscope: output voltage is precisely set to 28V by a multimeter and the input is slightly below 56V that the power supply precisely provides.

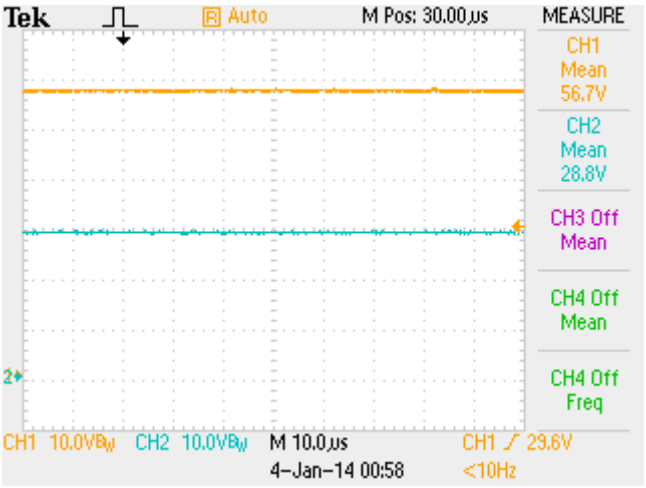
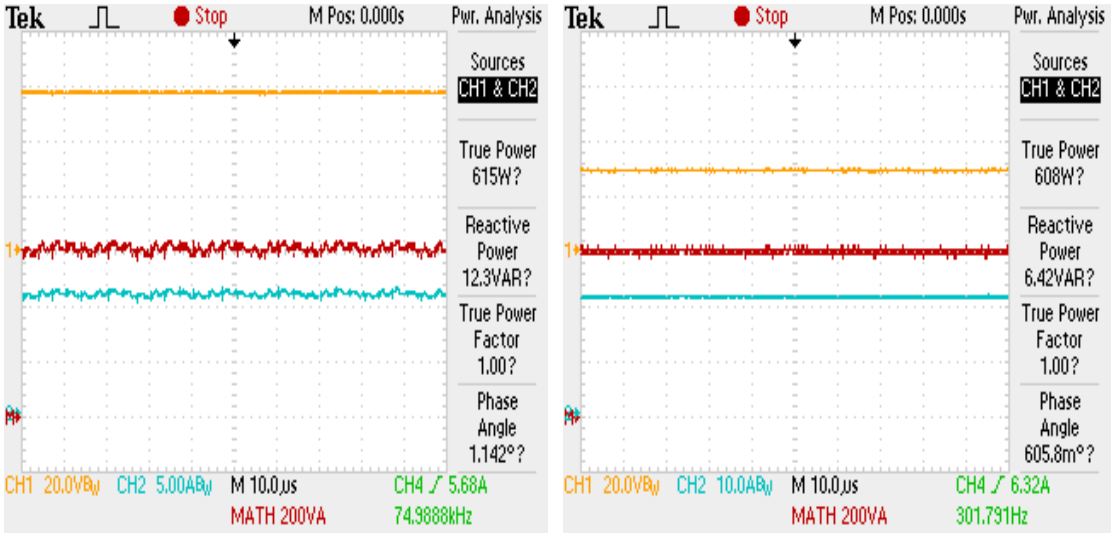


Figure 4.37 Input (CH1: 10V/div) and output (CH2: 10V/div, 10µs/div) voltages for the converter with optimized (f, L, N) parameters.

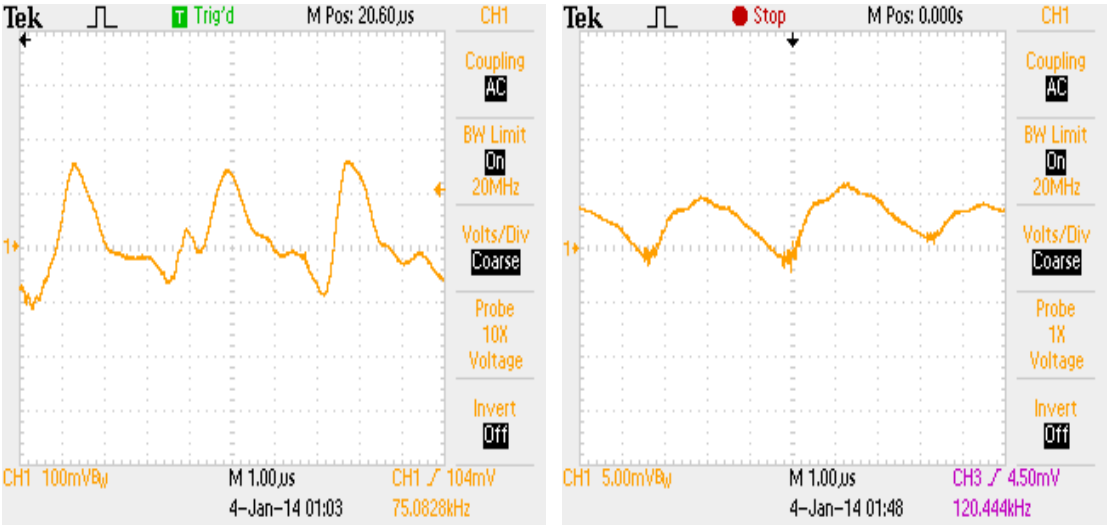
Input voltage, input current and their multiplication which gives input power are shown in Figure 4.38-(a). Waveform recording that contains output voltage, current and power is provided in Figure 4.38-(b). Note that the input current has a near DC characteristics with little ripple on it due to interleaving.



(a) **(b)**

Figure 4.38 Input (a) (CH1: 20V/div, CH2: 5A/div, MATH: 200VA/div) and output (b) (CH1: 20V/div, CH2: 10A/div, MATH: 200VA/div, 10µs/div) voltages, currents and powers for the converter with optimized (f, L, N) parameters.

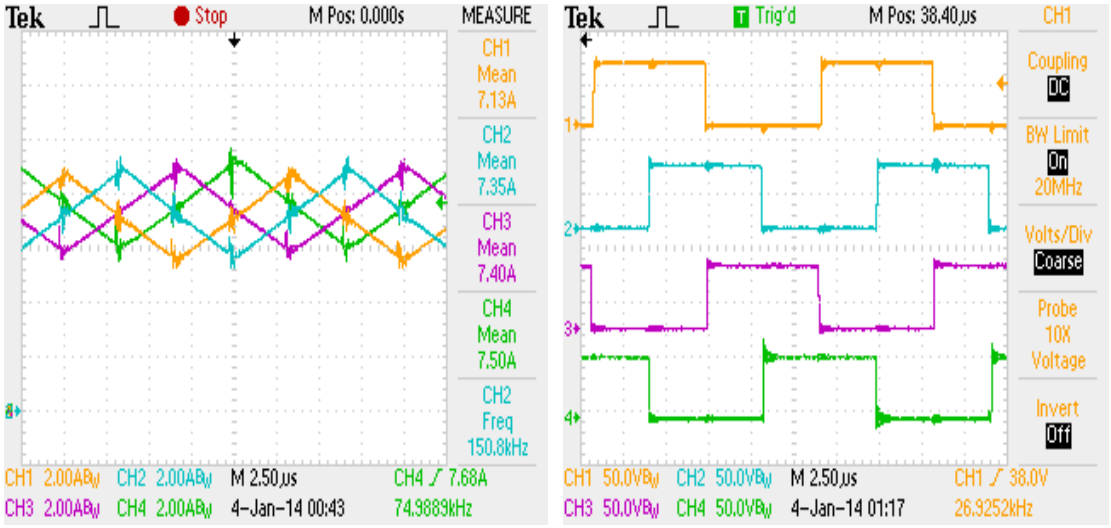
Input and output voltage ripples are depicted in Figure 4.39 (a) and (b) respectively. As can be seen from the related waveforms, input voltage ripple is 250 mV (which corresponds to 0.45% for 56V input) and the output ripple is around 8 mV (which corresponds to 0.03% for 28V output). Note that these figures can be considered as quite demanding ripple values for a practical buck converter.



(a) **(b)**

Figure 4.39 Input (a) (CH1: 100mV/div) and output (b) (CH1: 5mV/div, 1µs/div) voltage ripples for the converter with optimized (f, L, N) parameters.

Inductor currents and MOSFET drain to source (V_{DS}) for all four parallel phases are depicted in Figure 4.40 (a) and (b) respectively, to exemplify the interleaved operation. Inductor currents given in Figure 4.40 show a balanced current distribution without forced current sharing.



(a) **(b)**

Figure 4.40 Inductor currents (a) (CH1-CH4: 2A/div) and V_{DS} voltages (b) (CH1-CH4: 50V/div, 2.5µs/div) for all phases of the converter with optimized (f, L, N) parameters.

The unfiltered sum of phase currents is given in Figure 4.41. It can be seen that ripple cancellation results in a pure DC current without any serious need for filtering. Sum of phase currents is recorded at 20A not to exceed the rating of the current clamps.

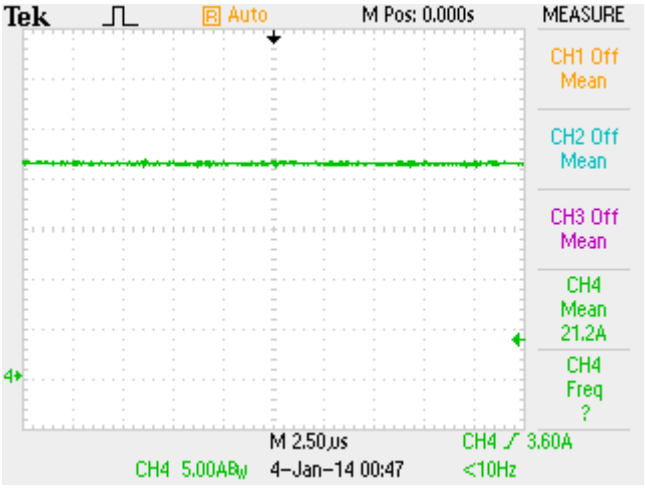


Figure 4.41 Sum of phase currents (CH4: 5A/div, 2.5µs/div) for the converter with optimized (f, L, N) parameters.

MOSFET V_{DS} voltage waveform is a clear indicator for switching performance: situations like voltage spikes during turn-off of the MOSFET or source voltage going negative during turn-on indicate a poor design. From the V_{DS} waveform depicted in Figure 4.42, it can be observed that the switching performance of the implemented converter is satisfactory.

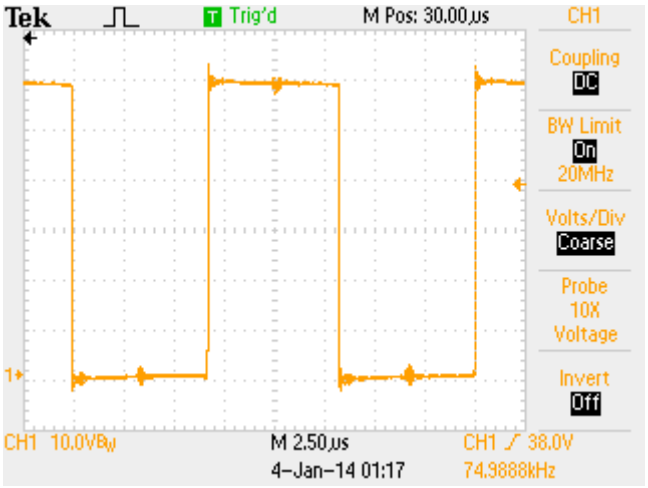
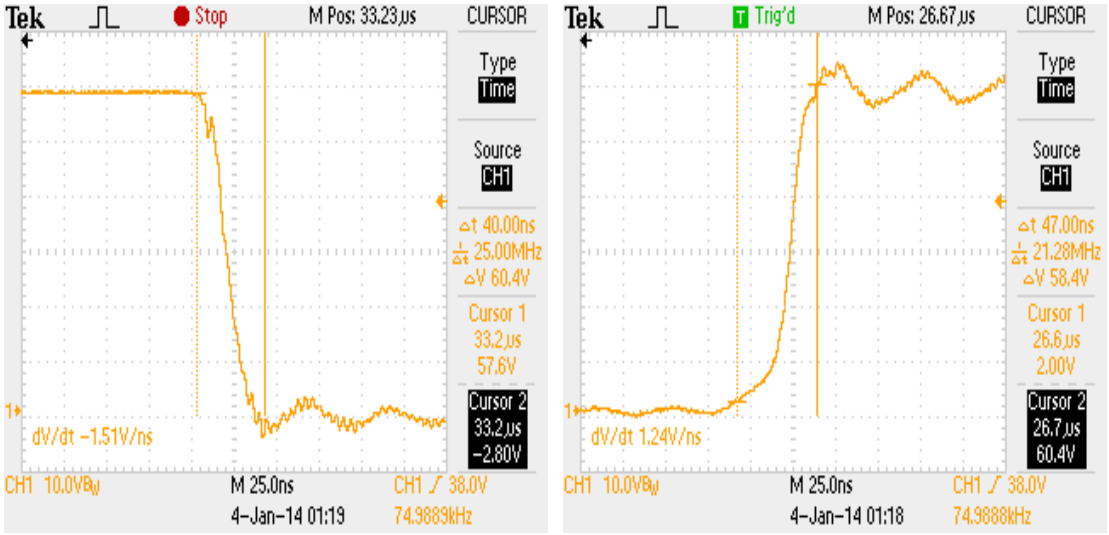


Figure 4.42 MOSFET V_{DS} waveform (CH1: 10V/div, 2.5µs/div) for the converter with optimized (f, L, N) parameters.

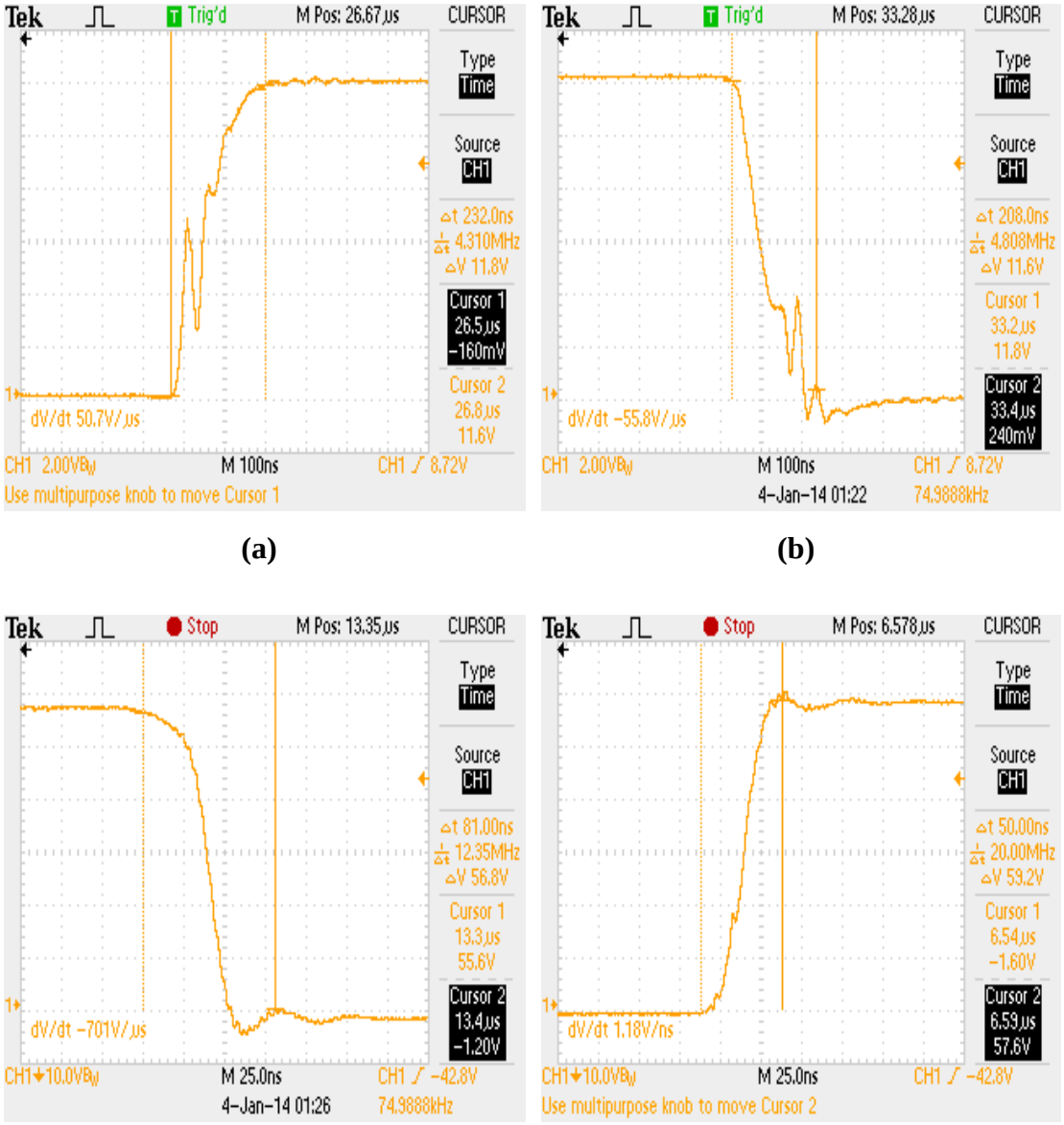
By zooming in the V_{DS} waveform given in Figure 4.42, Figure 4.43 is created to provide better images for V_{DS} during MOSFET turn on (a) and off (b). From the figure, it can be seen that time required for MOSFET switching is less than 50 ns. Parasitic oscillations can also be observed from the related figure.



(a) **(b)**

Figure 4.43 MOSFET V_{DS} waveform during turn-on (a) and turn-off (b) instants (CH1: 10V/div, 25ns/div) for the converter with optimized (f, L, N) parameters.

Other switching related voltage waveforms are depicted in Figure 4.44 such as MOSFET gate to source voltage (V_{GS}) during turn-on (a) and off (b) and diode anode to cathode voltage (V_D) during turn-on (c) and off (d). Figure 4.43 shows that gate to source potential fully building up requires more time than transition for drain to source voltage. Switching characteristic for the diode is pretty much the same as that of MOSFET's.



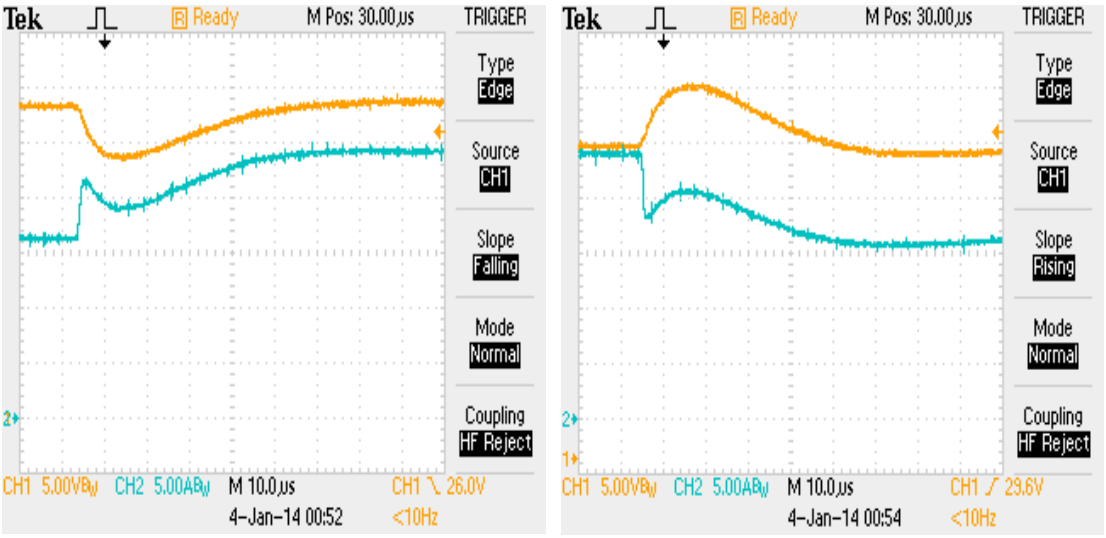
(a) **(b)**

(c) **(d)**

Figure 4.44 MOSFET V_{GS} waveform during turn-on (a) and turn-off (b) (CH1: 2V/div, 100ns/div) and diode V_D during turn-on (c) and off (d) (CH1: 10V/div, 25ns/div) instants for the converter with optimized (f, L, N) parameters.

Converter response for an abrupt change in load resistance can be observed from Figure 4.45 which contains output voltage and current waveforms for load step-up (a) and step-down (b) situations. Figure 4.44 shows that the converter can tolerate

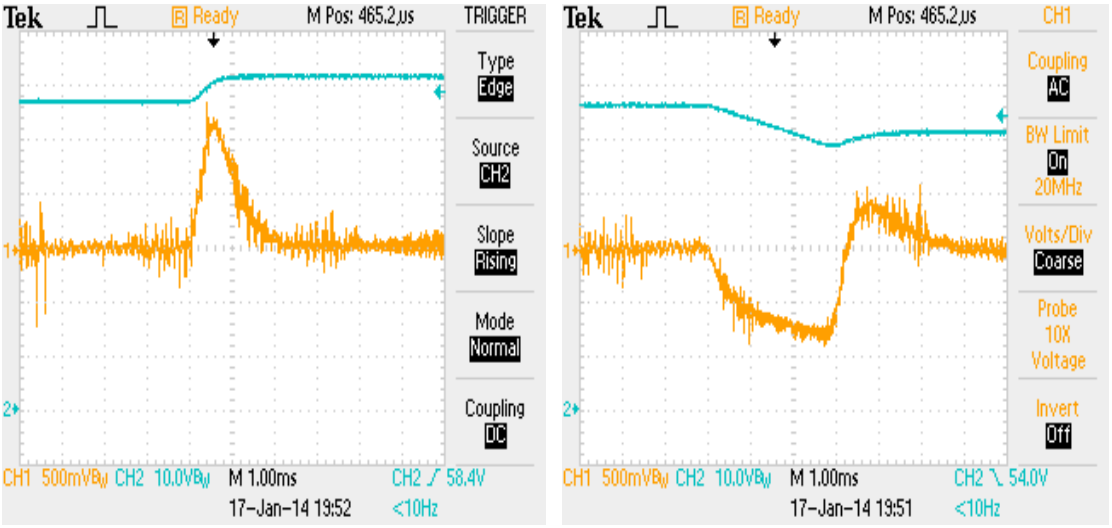
the change with little fluctuations at the output, recovering to steady state within approximately five switching cycle time.



(a) **(b)**

Figure 4.45 Output voltage (CH1: 5V/div) and current (CH2: 5A/div, 10µs/div) waveforms during an instantaneous load step-up (a) and down (b) for the converter with optimized (f, L, N) parameters.

Load regulation being documented, a similar test has also been applied at the input side where supply voltage goes up or down by 5V. Although the change in the input voltage is far from being instant, it is the best rate of change that the power supply used for the experimentation can provide. Change in the output voltage with respect to the input is depicted in Figure 4.46 during input voltage rise (a) and fall (b) by 5V.



(a) **(b)**

Figure 4.46 Input (CH2: 10V/div) and output (CH1: 500mV/div, 1ms/div) voltage waveforms during supply voltage rise (a) and fall (b) by 5V for the converter with optimized (f, L, N) parameters.

The implemented converter possesses important properties such as under-voltage lock out, over voltage protection and soft start as does the two-phase converter introduced before. Soft start operation, being suitable for an oscilloscope display, has been depicted in Figure 4.47. The implemented converter slowly increases its voltage reference for its control loop thereby avoids an instant loading of the supply that it is connected to.

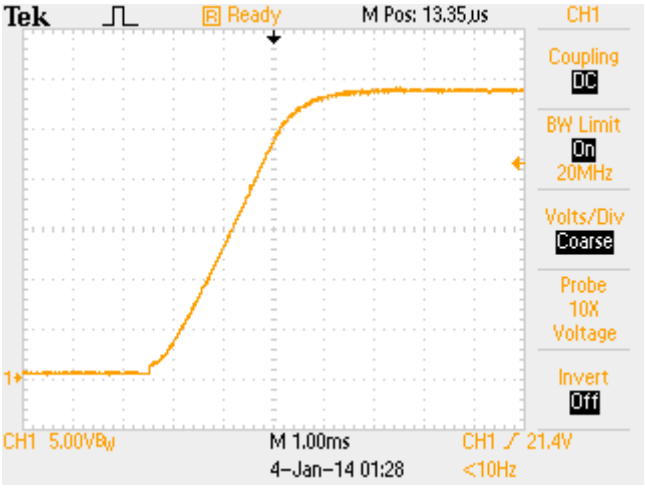


Figure 4.47 Soft start operation (CH1: 5V/div, 1ms/div) for the converter with optimized (f, L, N) parameters.

Power conversion performance of the implemented converter has been documented by several oscilloscope waveforms which indicate low ripple, low noise and satisfactory dynamic performance. Efficiency analysis follows next. In Figure 4.48, efficiency values with respect to output current are plotted. Similarly, total loss versus load current graph is also provided in Figure 4.49. Efficiency and loss versus load current graphs include both analytical and experimental efficiency values which are pretty close to each other. For the analytical calculation of the efficiency, equations for loss mechanisms introduced in Chapter 3 are used, which will not be repeated here. Analytical and experimental efficiency measurements turning out pretty close indicates that the equations adopted for the analysis are good approximations of the actual loss mechanisms. This partly stems from the fact that, the dominant loss terms being conduction losses for the implemented converter, it is relatively easy to successfully predict the efficiency outcome once the accurate ESR values are adopted for the analysis. As already discussed at the beginning of this chapter, Hioki3334 wattmeters are utilized for efficiency measurements for their accuracy.

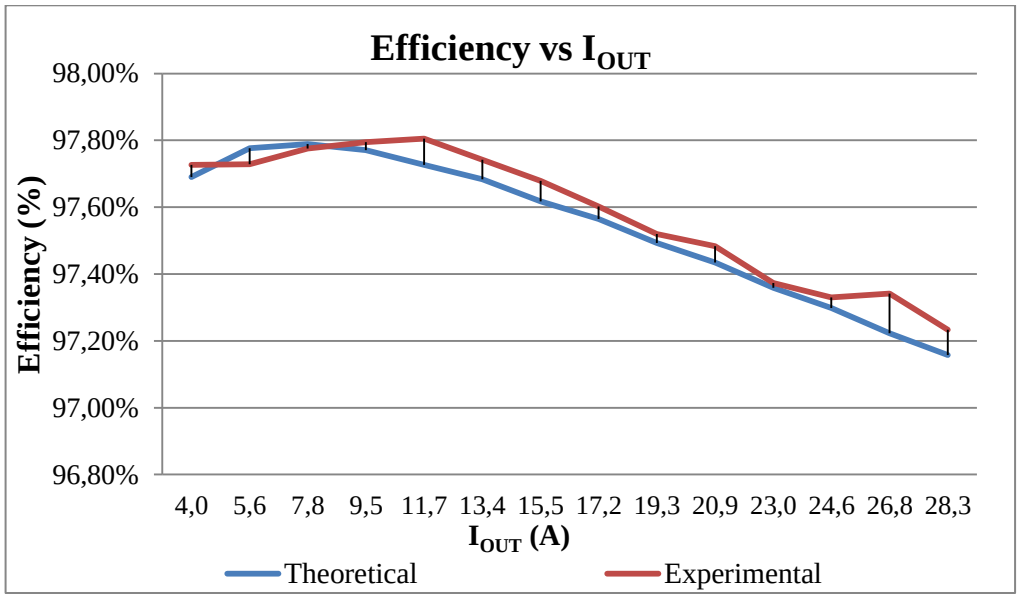


Figure 4.48 Efficiency versus load current graph for the converter with optimized (f, L, N) parameters.

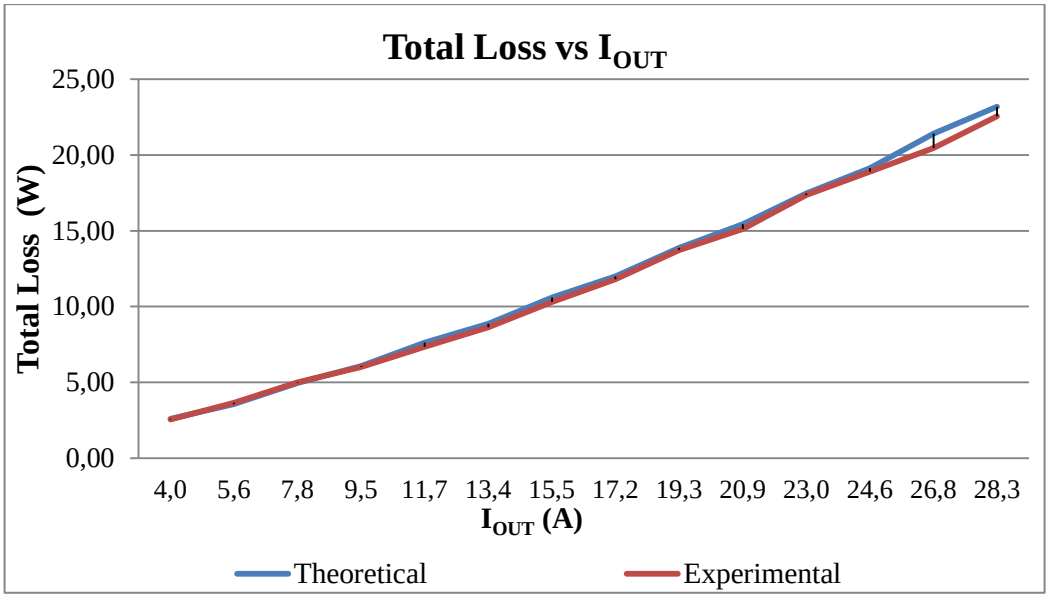


Figure 4.49 Total loss versus load current graph for the converter with optimized (f, L, N) parameters.

Loss distribution of the implemented converter under full rated current (28 A) is depicted in Figure 4.50.

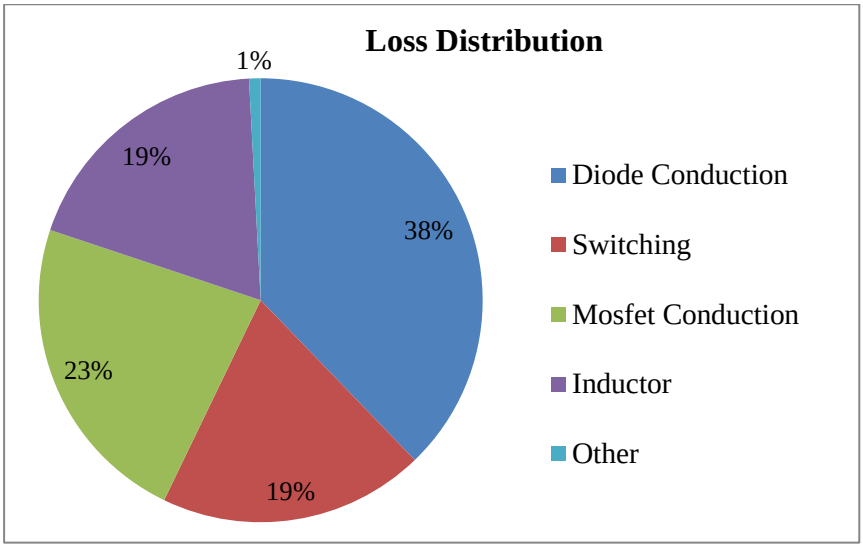


Figure 4.50 Loss distribution for the converter with optimized (f, L, N) parameters.

By shutting down some of the parallel phases, one, two and three-phase parallel operation of the implemented converter is tested and the efficiency values for those operating conditions are plotted in Figure 4.51 along the nominal four-phase structure. Note that the amount of phase shift between the parallel phases are modified as the active number of phases (N) being changed according to the formula $\theta = {}^{2\pi}/_{N}$. As already discussed in "2.2.6.2 -Dynamic Number of Phases" section of Chapter 2, shutting down some of the parallel phases as the load current decreases is a common technique for interleaved power conversion to obtain better light-load efficiency characteristic, however the application of this technique to the implemented converter is not feasible as the efficiency figures decrease with the decreasing N. This is because of the fact that the effective resistance that the

converter exhibits increases with decreasing N which results in a net efficiency decrease for a converter whose loss terms are conduction loss dominated.

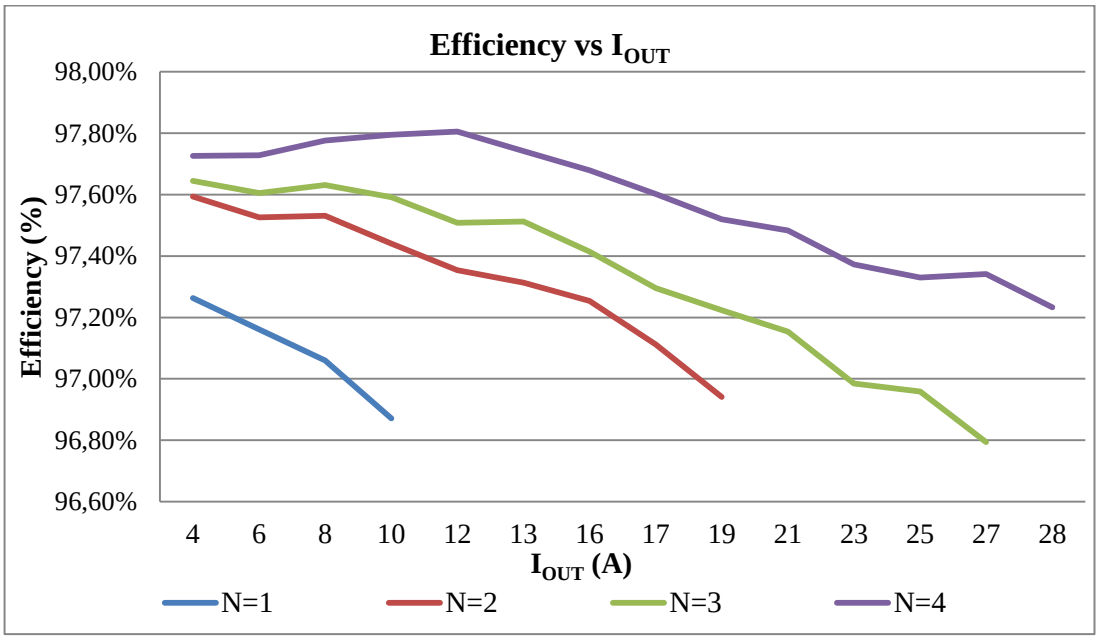


Figure 4.51 Efficiency versus load current graph under varying N for the converter with optimized (f, L, N) parameters.

Detailed oscilloscope recordings and efficiency analyses introduced thus far show that the converter with optimized (f, L, N) values suggested by the study given in Chapter 3, exhibits superior power conversion characteristics thanks to interleaving and also performs power conversion efficiently. To summarize the important properties of the converter, Table 4.8 is provided. Again, the volume term corresponds to heat sink and total inductor volume combined. Considering that the converter has been implemented with low cost materials and actually being a prototype converter with many features that can be improved, the efficiency and power density figures obtained for it are quite demanding.

Table 4.8 List of important performance figures for the converter with optimized (f, L, N) parameters.

V_{IN} Ripple (mV)	250
V_{IN} Ripple (%)	0.45
V_{OUT} Ripple (mV)	8
V_{OUT} Ripple (%)	0.03
Full Load Efficiency (%)	97.23
Average Efficiency (%)	97.58
Total Inductor Volume (cm^3)	44
Total Inductor Volume (cm^3)	110
Total Volume (cm^3)	154
Power Density (W/cm^3) (for rated power assumption)	5.2
Power Density (W/cm^3) (for peak power assumption)	6.5
Under Voltage Lock-Out	✓
Over Voltage Protection	✓
Soft Start	✓

4.5 Other Variations Tested for the Optimized Converter

Implementation and test results of the optimal converter having been introduced, variations of the optimal design are also provided. First, the non-optimal inductor described in "4.4.1 Inductor Design" section will be utilized then different R_{GATE} and frequency values are tested for efficiency. Then, a four-phase parallel operation is tested for comparison with the interleaved operation, to exemplify the benefits of interleaving.

4.5.1 Testing the Converter with Different R_{GATE} and Frequency Values

Same converter is also implemented with the non-optimal inductors made of core 77259A7, details of which have been addressed in "4.4.1 Inductor Design" section. While the overall inductor volume has been increased from 44 cm^3 to 88 cm^3, efficiency figures stay very much the same since losses under same operating conditions are nearly same for both inductors. A photo of the converter implemented with the non-optimal inductors is given in Figure 4.52.

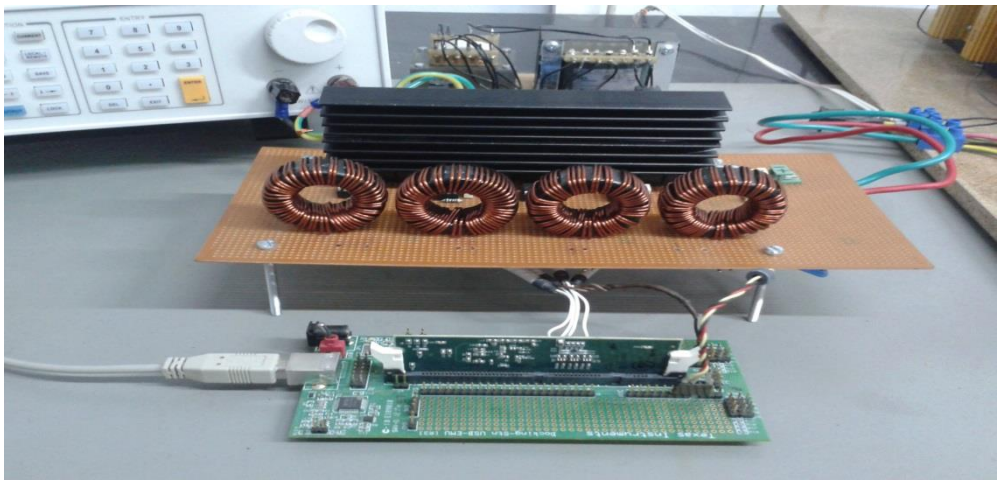


Figure 4.52 Photo of the converter implemented with non-optimal inductors.

Note that, in Figure 4.52 heat sink volume has also been increased. With this variation, the nominal power rating of the converter increases to 1-kW, in other words the converter can supply a power of 1-kW indefinitely without a dangerous temperature rise at the semiconductor switches.

On the converter illustrated in Figure 4.52, two main parameters; namely different switching speeds and frequencies are tested. Gate resistance which is utilized between the gate driver's output and the gate leg of the MOSFET to be driven is one of the key parameters for MOSFET switching; higher gate resistance values increases the time constant hence delays MOSFET turn-on and off. On the other

hand, lower limit for gate resistance is usually determined by noise considerations: higher switching speeds result in voltage spikes and other noise related phenomena that can affect the overall converter. In our case, the main problem caused by noise is the DSP malfunction. For the implemented converter, 10 and 22Ω gate resistances are utilized at the gate drivers and their effect on converter efficiency.

The nominal frequency being 75 kHz which is suggested by the optimization study, 50 kHz switching frequency has also been tested for its effect on efficiency. Inductors being kept the same, the selection of a lower frequency results in lower switching loss. On the other hand ripples for phase currents are increased which will increase conduction losses due to current waveforms having higher rms value for the same average current.

Efficiency and total loss versus load current graphs for all variations (R_{GATE}=10 and 22Ω, f=50 and 75 kHz) are depicted in Figure 4.53 and Figure 4.54 respectively. Loss distribution graphs for all variations are given in Figure 4.55.

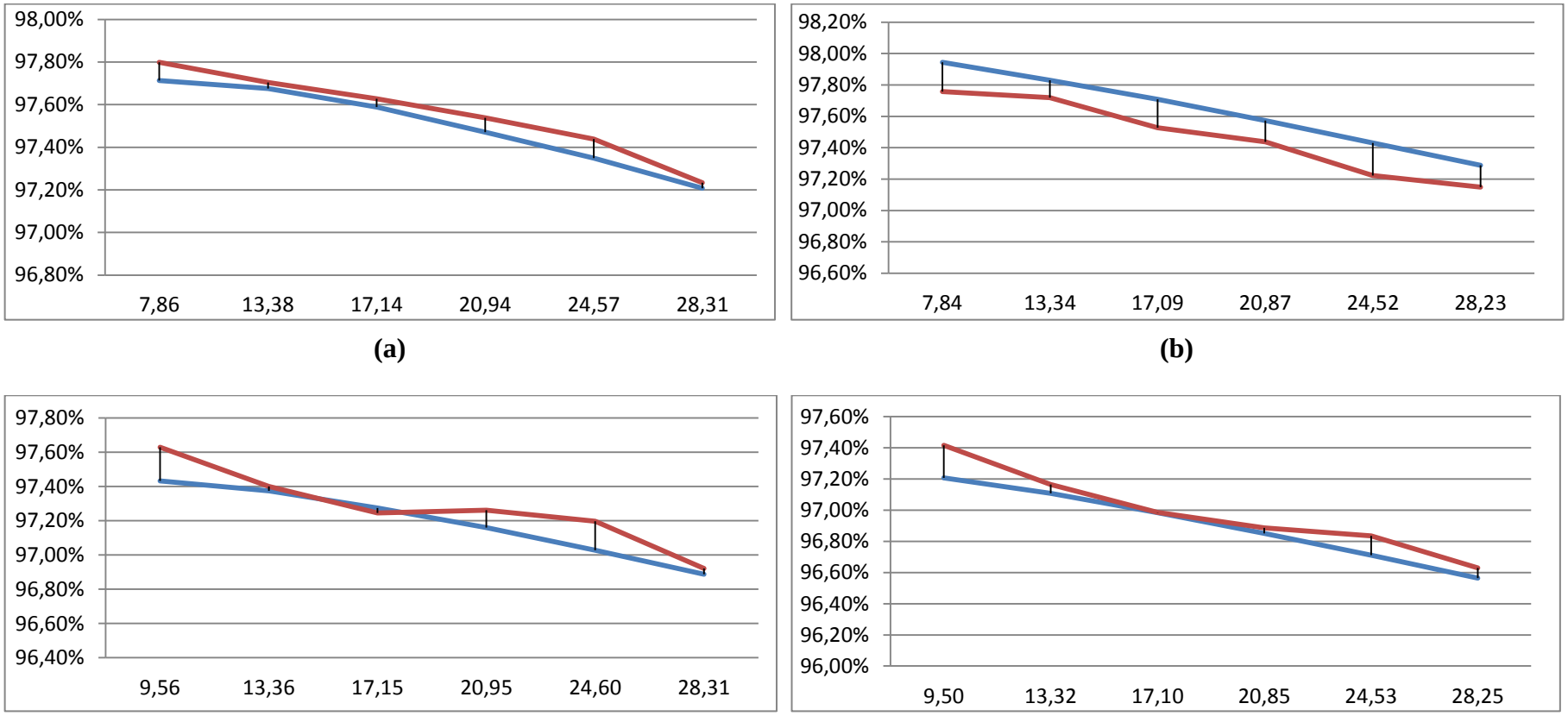
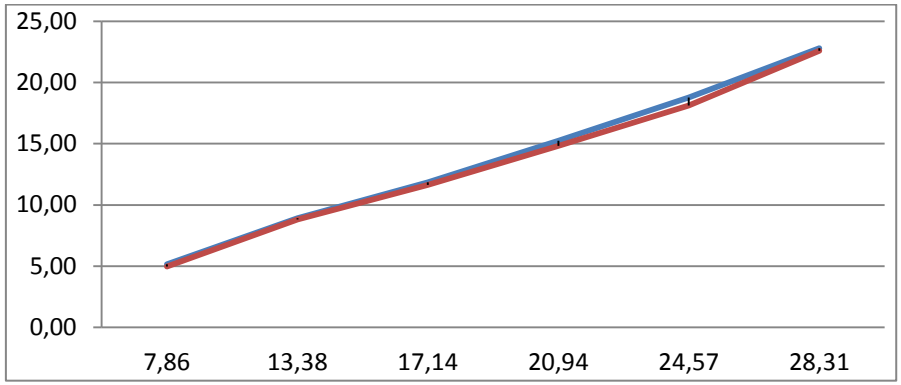
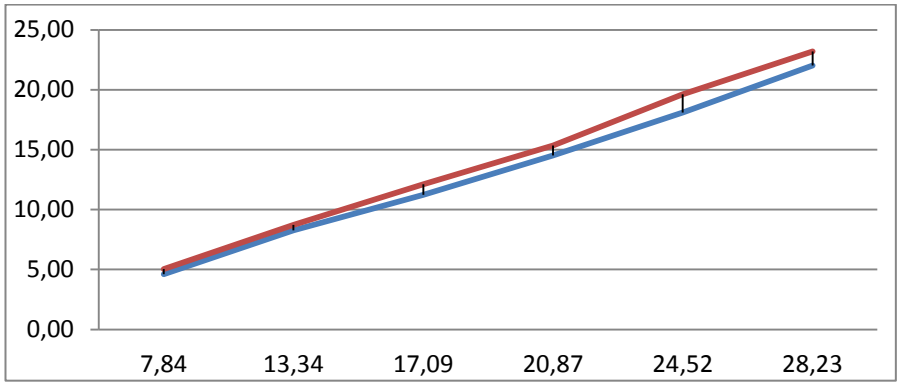


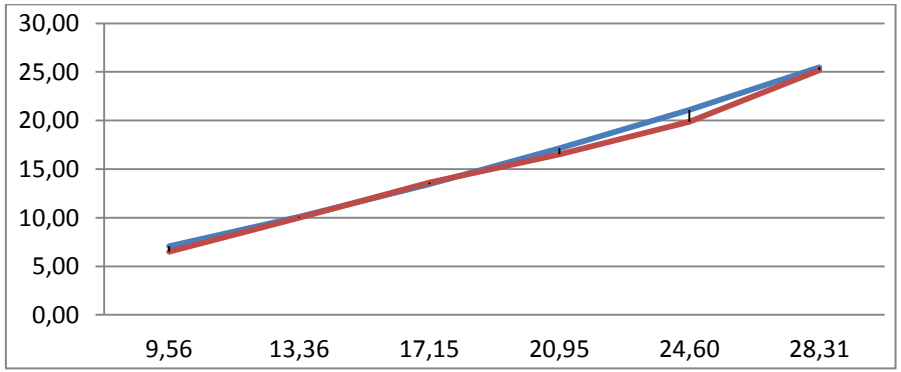
Figure 4.53 Efficiency (%) versus load current (in A) graphs for R_{GATE}=10Ω and f=50kHz (a), R_{GATE}=10Ω and f=75kHz (b), R_{GATE}=22Ω and f=50kHz (c), R_{GATE}=22Ω and f=75kHz (d). Blue indicates analytical, red indicates experimental figures.



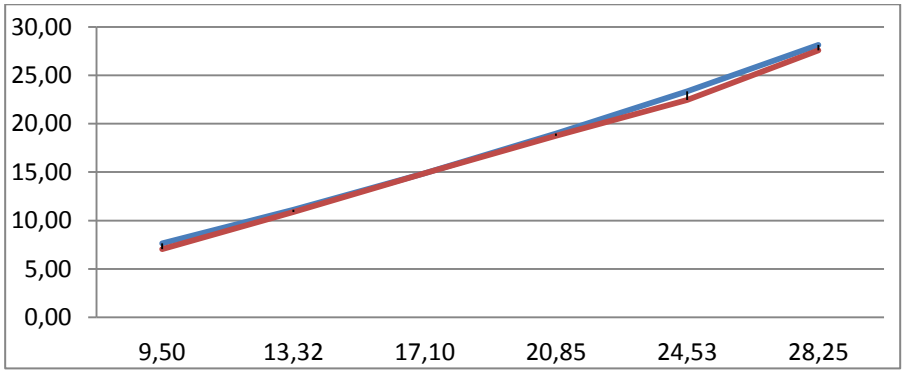
(a)



(b)



(c)



(d)

Figure 4.54 Total loss (in W) versus load current (in A) graphs for R_{GATE}=10Ω and f=50kHz (a), R_{GATE}=10Ω and f=75kHz (b), R_{GATE}=22Ω and f=50kHz (c), R_{GATE}=22Ω and f=75kHz (d). Blue indicates analytical, red indicates experimental figures.

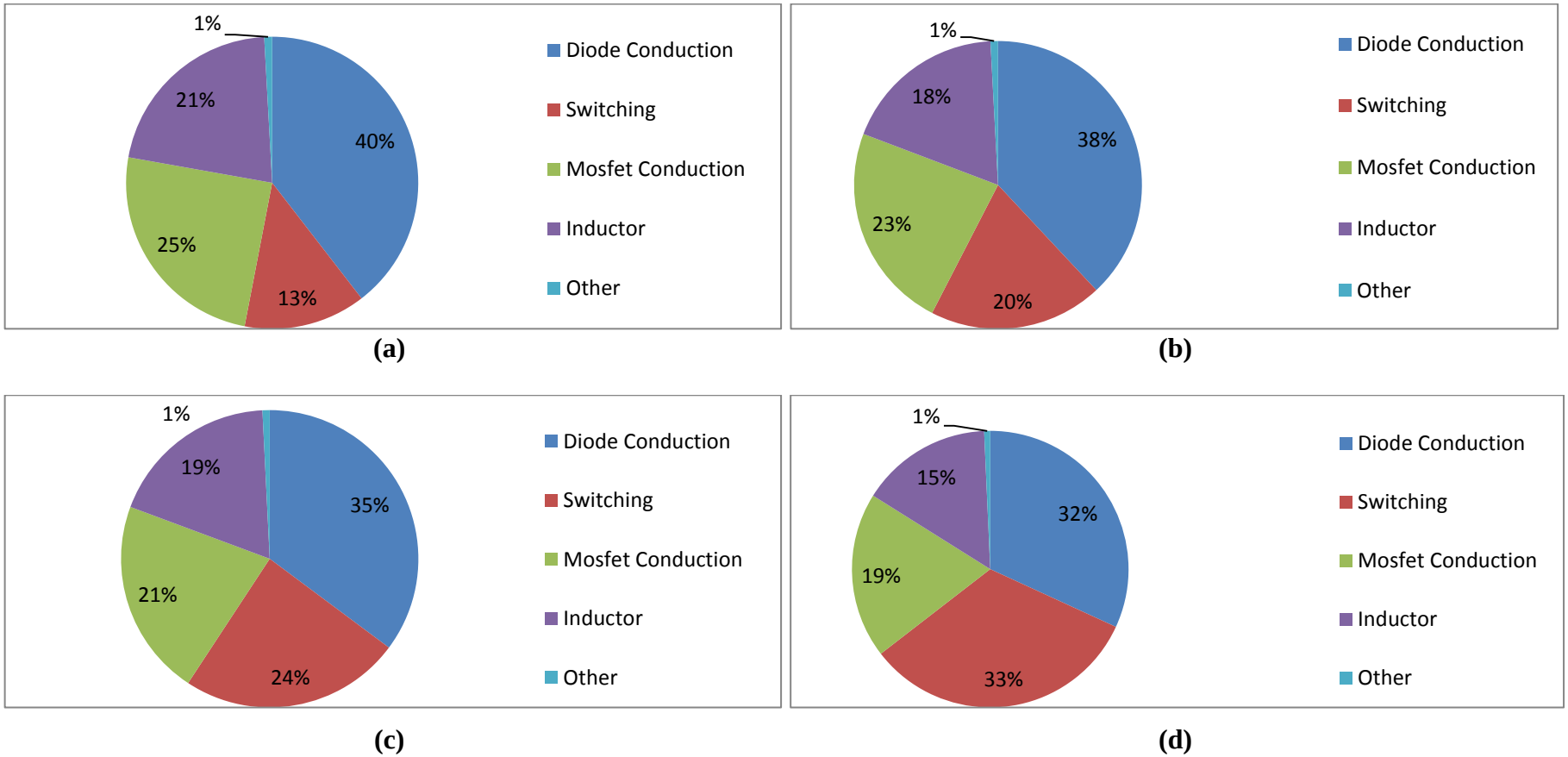
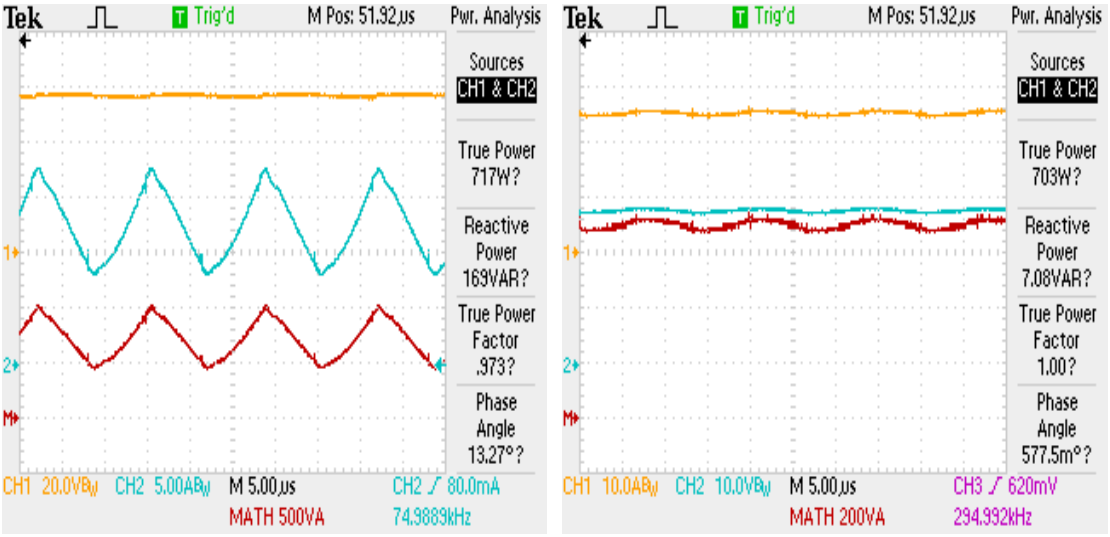


Figure 4.55 Loss distribution graphs for R_{GATE}=10Ω and f=50kHz (a), R_{GATE}=10Ω and f=75kHz (b), R_{GATE}=22Ω and f=50kHz (c), R_{GATE}=22Ω and f=75kHz (d).

As the efficiency and loss graphs depicted in Figure 4.53-4.55 summarize, faster switching operation enables switching loss reduction. On the other hand, switching frequency decrease from 75 to 50 kHz offers no serious increase in efficiency: decrease in switching losses cannot compensate the increase in conduction loss due to the increased current ripple on the parallel phases. In other words, under given operating conditions and component selection, frequency increase from 50 to 75 kHz comes free.

4.5.2 Four-Phase Parallel Operation without Phase Shifting

By the elimination of phase angles between PWM signals for each parallel phase, a four-phase parallel operation without the benefits of interleaving has been tested. With this configuration, the converter imitates the single-phase operation. Note that, without the phase shifting that enables ripple cancellation at the input and output, additional capacitors are required since the interleaved version utilizes very small capacitive filters because of the reduced need for filtering due to the ripple cancellation property. Therefore, additional capacitances of 91 and 63 μF are added to the input and output respectively. Switching frequency is kept same at 75 kHz and 22Ω gate resistors are utilized. Power conversion performance under these conditions can be examined through the oscilloscope waveforms provided. In Figure 4.56 voltage, current and power waveforms are depicted.



(a) **(b)**

Figure 4.56 Input (a) (CH1: 20V/div, CH2: 5A/div, MATH: 500VA/div) and output (b) (CH1: 10V/div, CH2: 10A/div, MATH: 200VA/div, 5µs/div) voltages, currents and powers for parallel operation without phase shifting.

Figure 4.56 alone indicates the superiority of interleaved power conversion: although the capacitances at the input and output are drastically increased for the parallel operation greater ripple magnitudes are observed. The input current, which would have a pulsating characteristic, has been filtered to some extent by the input capacitance however the input current waveform for the interleaved operation is far better than the one depicted in Figure 4.56. Voltage ripples at the input and output turn out to be 1.5 and 1 V respectively and are given in Figure 4.57.

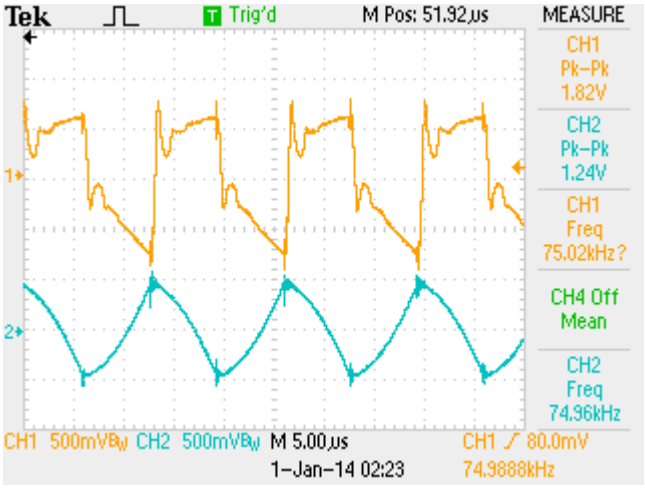


Figure 4.57 Input (CH1: 500mV/div) and output (CH2: 500mV/div, 5µs/div) voltage ripples for the parallel operation without phase shifting.

The parallel operation of the converter is illustrated in Figure 4.58 where current waveforms for parallel phases are depicted.

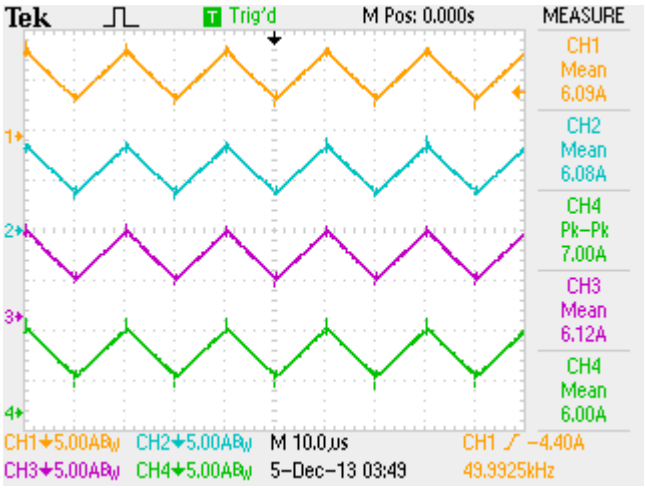


Figure 4.58 Phase currents (CH1-4: 5A/div, 10µs/div) for the parallel operation without phase shifting.

Contrary to interleaved operation, current ripples on the phase currents add up at the input and output of the converter, magnifying the ripple amount. Sum of phase currents at the output side before and after the output capacitance is depicted in Figure 4.59. As the figure shows, summation of phase currents has a great ripple component and a considerably large output capacitance (71 µF) is required to satisfactorily filter it.

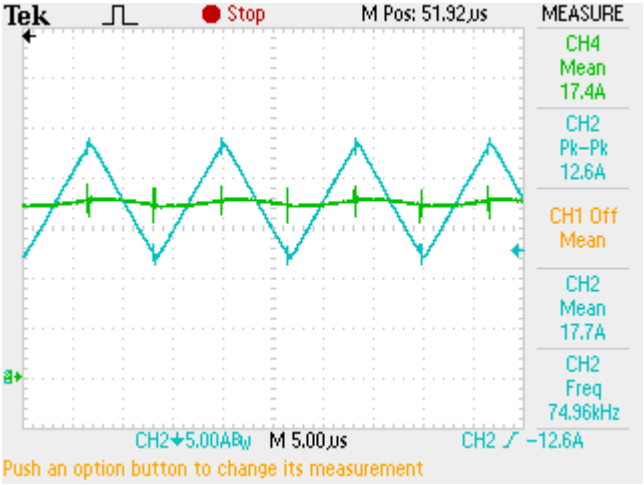


Figure 4.59 Sum of phase currents (CH2: 5A/div) and load current (CH3: 5A/div, 5µs/div) for the parallel operation without phase shifting.

The analyses for the parallel operation will be concluded with the introduction of efficiency versus load current graph which can be seen in Figure 4.60.

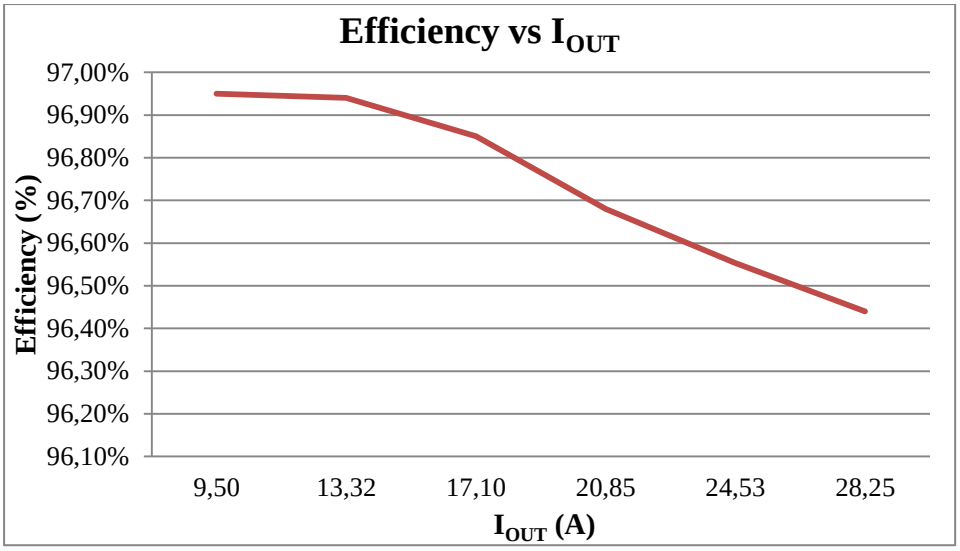


Figure 4.60 Efficiency versus load current graph for the parallel operation without phase shifting.

Comparing the efficiency graph for the parallel operation case to its counterpart (f=75 kHz, R_{GATE}=22Ω efficiency graph depicted in Figure 4.52), it can be seen that efficiency values for the parallel operation is slightly smaller than those of interleaved case. This can be explained with the additional capacitor losses both at the input and output.

To provide a comparison between the interleaved and parallel operation cases, Table 4.9 has been prepared. It is seen that the parallel operation of the converter exhibits higher voltage ripple in spite of the extra capacitance (91 µF to input, 63 µF to output) added. In terms of efficiency, parallel operation case slightly lacks its interleaved counterpart. Note that the efficiency value given for the interleaved case in Table 4.9 corresponds to the f=75 kHz, R_{GATE}=22Ω case of Figure 4.50.

Table 4.9 Comparison between interleaved and parallel operation cases.

	SINGLE-PHASE	INTERLEAVED
C_{IN} (μF)	125	34
C_{OUT} (μF)	71	7.87
V_{IN} Ripple (mV)	1500	250
V_{OUT} Ripple (mV)	1000	8
V_{IN} Ripple (%)	<2.7	<0.45
V_{OUT} Ripple (%)	<3.5	<0.03
Efficiency (%)	96,44	96,60

4.6 Comparison between Analytical and Experimental Results

In this part, the correlation of analytical and experimental results will be examined. Referring back to the optimization study carried out in Chapter 3, three important design points for N=4 case is given in Table 4.10.

Table 4.10 Three important design points for N=4 suggested by the optimization study.

	Eff. (%)	**V_{TOT} (cm^3)**	**V_L/V_{TOT} (%)**	**FoM**	**f (kHz)**	**L (μH)**	**Cost ($)**
Max. Eff.	96,94	143,51	24,62	3,72	70	48,61	20,94
Min. Vol.	96,89	139,89	22,42	3,77	76	39,80	20,81
Max. FoM	96,91	140,44	23,71	3,78	71	43,71	20,78

Considering these three design points listed in Table 4.10, it can be seen that the maximum efficiency and minimum volume (and maximum FoM which is a hybrid of these two) converge and target design outcomes such as efficiency and volume

vary little within the area defined by these points, a design point of (f, L, N) = (75 kHz, 45 μH, 4 phases) is selected for the converter implementation. The optimization program foresees an efficiency value close to 96.90% and volume value roughly equals to 140 cm^3. Efficiency and volume values of the implemented converter turn out to be 97.20% and 154 cm^3 respectively. It can be said that a good match has been provided between the analytical and experimental results considering that the anticipation of efficiency and volume values for a practical power converter is not an easy task.

Efficiency turned higher than expected by 0.3% which corresponds to losses occurring 2.4 W less than the analytical model. On the other hand, volume is higher than expected by 10%. This stems from the fact that the core suggested by the inductor design sub-module of the optimization program, was not available during the implementation study therefore the core 0077894A7 was utilized for inductors which is a little larger than the ideal. Also, the winding utilized for the inductors exhibit lower A/cm^2 value than the 500 A/cm^2 assumption adopted for the analysis. Same situation applies to the heat sink utilized: the available heat sink for converter implementation, which is slightly larger than the expected, has not been trimmed to fit the expectations. These issues related to the inductor and heat sink add up and created the 14 cm^3 difference in the outcomes. To sum up, having stated the reasons for the discrepancies, the implemented converter well reflects the analytical approach with excusable discrepancies.

Note that analytical efficiency curves are also provided along the experimental efficiency curves for the optimal converter and its variations and they are nearly identical. With the same loss calculation methodology described in Chapter 3, important figures related to loss calculations such as inductor ESR have been updated with the converter implementation and such close values could be obtained. Considering any of the loss distribution graphs introduced thus far, it can be seen that the dominant loss mechanism is the conduction loss and within the conduction loss terms the diode losses take the biggest share. This situation eases the way for accurate loss and efficiency calculations since these types of losses are easy to

model: once the correct loss parameters (such as $R_{DS,ON}$ for a MOSFET or V_T for a diode) are adopted, analytical outcomes lay very close to the experimental ones.

4.7 Summary

This chapter involves the hardware design and implementation part of the thesis study. Two power converters namely a two-phase, 500 W buck converter and an optimized four-phase 1-kW buck converter with several variations have been implemented and tested for their power conversion performance. Computer simulations are also carried out to aid the implementation step.

With the design and implementation of the two-phase, 500 W buck converter, insight for practical converter design and experience on DSP utilization for power conversion have been acquired.

According to the optimum design point suggested by the optimization study of Chapter 3, a four-phase, hard switched, digital controlled step down converter having 800W nominal 1kW peak power has been implemented. The power conversion performance of the converter is very satisfactory: it has 97.2% full load efficiency and exhibit 5.2W/cm^3 power density. Electrical input/output characteristics are also very rewarding due to the interleaved structure.

Variations of the 1-kW converter have been provided: different switching speeds and frequency values are tested for their effect on efficiency. With the elimination of phase shifting between phases, the parallel mode of operation is also tested for comparison with the interleaved operation.

CHAPTER 5

CONCLUSION AND FUTURE WORK

This thesis involves the design and implementation of an interleaved, hard switched, digital controlled 1kW step down converter with optimized f-L-N values for higher power density. Theoretical analyses on the subject include mathematical expressions and computer simulations. The hardware implementation part of the study is documented with various oscilloscope recordings and measurements.

With a brief introduction on the current level of SMPS technology, main design challenges have been addressed. The importance of converter optimization to obtain higher efficiency values in lower volume has been highlighted.

With an overall examination on paralleling schemes, interleaving technique, which is a widely utilized technique in high-level converters due to the benefits it introduces, has been thoroughly analyzed. The effects of interleaving on power conversion performance of a converter have been described in detail with a comprehensive mathematical approach. Important issues related to the interleaving technique, such as dynamic number of phases, coupled inductors and current imbalance have also been addressed.

The importance of power converter optimization to design higher performance converters being emphasized, an exhaustive search method based optimization scheme is presented. Important properties for the converter under examination such as efficiency, volume and cost have been calculated for various values of f, L and N. It was shown that it is possible to find an optimal solution which promotes both efficiency and power density by a careful selection of (f, L, N) parameters. The

optimum design point suggested by the analyses is (f, L, N) = (75kHz, 45 μH, 4 phases).

According to the optimum design point determined by the optimization study, a four-phase, hard switched, digital controlled step down converter having 800W nominal and 1kW peak power has been implemented which exhibits 97.2% full load efficiency and has 5.2W/cm^3 power density while maintaining superior electrical input/output characteristics. Along the optimized converter, an additional two-phase 500W non-optimized converter has also been implemented as a preparatory step. The two-phase, 500W converter exhibits 95.16% full load efficiency and 3.75 W/cm^3 power density. Several variations of the optimal converter, which employ different switching speeds, inductors and switching frequencies, have been provided for comparison. The implementation procedure, which involves computer simulations and inductor design, has been clearly described.

As future work, the optimization study can be evolved into a higher-level form which utilizes effective optimization techniques rather than exhaustive search, considers more parameters and covers several power converter topologies in addition to the buck converter. Besides, the consideration of emerging power semiconductors such as SiC or GaN and/or different materials for converter implementation (different core types and geometries, cooling methods etc.) would be beneficial. Spatial optimization of the components that the converter is made of should also be included for a better modeling of the total volume of a practical power converter.

REFERENCES

[1] N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications, and Design." 3rd Edition, John Wiley & Sons, Inc., 2002.

[2] R. W. Erickson, D. Maksimovic, "Fundamentals of Power Electronics." 2nd Edition, Kluwer Academic Publishers, 2001.

[3] Intel Transistors on Microprocessors: Microprocessor Quick Reference Guide, Intel Research, "http://www.intel.com/pressroom/kits/quickrefyr.htm" last accessed on [15.02.2014].

[4] M. Sakka, J. V. Mierlo, H. Gualous, "DC-DC Converters for Electric Vehicles." http://www.intechopen.com/download/get/type/pdfs/id/19583., last accessed on [15.02.2014].

[5] D. C. Reusch, "High Frequency, High Power Density Integrated Point of Load and Bus Converters," Ph.D. Thesis, Virginia Polytechnic and State University, Blacksburg-Virginia, 2012.

[6] M. Pavlovsky, Y. Tsuruta, A. Kawamura, "Pursuing high power-density and high efficiency in DC-DC converters for automotive application", in IEEE-PESC Conf., pp.4142-4148, 2008.

[7] R. L. Wang, P. Ning, D. Zhang, D. Jiang, R. Burgos, D. Boroyevich, K. J. Karimi, V. D. Immanuel, "A high power density converter", in IEEE-Industrial Electronics Magazine., pp.4-12, 2010.

[8] S. D. Round, P. Karutz, M. L. Heldwein, J. W. Kolar,"Towards a 30kW/liter, three-phase unity power factor rectifier", IEEE-PCC Conf., pp. 1251-1259, 2007.

[9] U. Badstuebner, J. Biela, J. W. Kolar, "Power density and efficiency optimization of resonant and phase-shift telecom DC-DC converters" in IEEE-APEC Conf., pp. 311-317, 2008.

[10] X. Zhou, P. L. Wong, X. Peng, F. C. Lee, A. Q. Huang "Investigation of candidate VRM topologies for future microprocessors", IEEE Transactions on Power Electronics, pp. 1172-1182, 2000.

[11] P. L. Wong, P. Xu, B. Yang, F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors", IEEE Transactions on Power Electronics, pp.499-507, 2001.

[12] Y. Panov, M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50A voltage regulator modules", IEEE Transactions on Power Electronics, pp.776-783, 2001.

[13] P. L. Wong, "Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors," Ph.D. Thesis, Virginia Polytechnic and State University, Blacksburg-Virginia, 2001.

[14] Y. Gang, A. Chen, X. He, "Soft switching circuit for interleaved boost converters", IEEE Transactions on Power Electronics, pp.80-86, 2007.

[15] C. A. Gallo, F. L. Tofoli, J. A. C. Pinto, “Two stage isolated switch-mode power supply with high efficiency and high input power factor”, IEEE Transactions on Industrial Electronics, pp.3754-3766, 2010.

[16] P. Zumel, O. Garcia, J. A. Cobos, J. Uceda, “Exploring interleaved converters as an EMI reduction technique in power converters”, IEEE-IECON Conf., pp.1219-1224, 2002.

[17] C. Wang, “Investigation on Interleaved Boost Converters and Applications” Ph.D. Thesis, Virginia Polytechnic and State University, Blacksburg-Virginia, 2009.

[18] A. Consoli, M. Cacciato, G. Scarcely, A. Testa, “Compact, reliable efficiency; a multi-phase dc/dc converter for automotive dual-voltage power systems”, IEEE-Industry Applications Magazine, pp.35-42, 2004.

[19] O. Garcia, P. Zumel, A. Castro, J. A. Cobos, “Automotive DC-DC bidirectional converter made with many interleaved buck stages”, IEEE Transactions on Power Electronics, pp.578-586, 2006.

[20] S. Waffler, M. Preindl, J. W. Kolar, “Multi-objective optimization and comparative evaluation of Si soft-switched and SiC hard-switched automotive DC-DC converters”, IEEE-IECON Conf., pp.3814-3821, 2009.

[21] J. Czogalla, L. Jieli, C. R. Sullivan, “Automotive application of multi-phase coupled inductor DC-DC converter”, Industry Applications Conf., pp.1524-1529, 2003.

[22] B. A. Miwa, “Interleaved Conversion Techniques for High Density Power Supplies” Ph.D. Thesis, Massachusetts Institute of Technology, 1992.

[23] S. Balachandran, F. C. Y. Lee, “Algorithms for power converter design optimization”, in IEEE Transactions on Aerospace and Electronic Systems, vol. AES-17, no. 3, pp. 422-432, 1981..

[24] T. C. Neugebauer, D. J. Perreault, “Computer aided optimization of DC-DC converters for automotive applications”, IEEE Transactions on Power Electronics, pp.775-783, 2003.

[25] S. H. Kang, D. Maksimovic, I. Cohen, “Efficiency optimization in digitally controlled flyback DC-DC converters over wide ranges of operating conditions”, IEEE Transactions on Power Electronics, pp.3734-3748, 2012.

[26] Y. Louvrier, P. Barrade, A. Rufer, “Weight and efficiency optimization strategy of an interleaved DC-DC converter for a solar aircraft”, in IEEE-EPE Conf., pp. 1-10, 2010.

[27] G. Sizikov, A. Kolodny, E. G. Fridman, M. Zelikson, “Efficiency optimization of integrated DC-DC buck converters”, in IEEE-ICECS Conf., pp. 1208-1211, 2010.

[28] J. B. Forsythe, “Paralleling of power MOSFETs for higher power output” International Rectifier Application Note, www.irf.com/technical-info/appnotes/para.pdf, last accessed on [15.02.2014].

[29] “Paralleling HEXFET power MOSFETs” International Rectifier Application Note,http://www.eetasia.com/ARTICLES/2003JUN/A/2003JUN27_AMD_POW_AN6.PDF?SOURCES=DOWNLOAD, last accessed on [15.02.2014].

[30] “Power MOSFET application precautions” Toshiba Application Note, http://www.semicon.toshiba.co.jp/shared/doc_pdf/com_pw-MOSFET_04_e.pdf, last accessed on [15.02.2014].

[31] “Paralleling of IGBT modules” ABB Application Note, http://www05.abb.com/global/scot/scot256.nsf/veritydisplay/565fbed2beb9eba8c1257a6b004c3932/$file/5SYA%20209800%20Aug.12%20(Paralleling%20of%20IGBT%20modules)_RSn.pdf, last accessed on [15.02.2014].

[32] “Paralleling of IGBTs” ON Semi Application Note, http://www.onsemi.com/pub_link/Collateral/AND9100-D.PDF, last accessed on [15.02.2014].

[33] “Connecting IGBTs in parallel (Fundamentals)” Infineon Application Note, https://www.infineon.com/dgdl/Infineon+-+Application+Note+-+IGBT+-+Connecting+IGBTs+in+Parallel+-+Fundamentals.pdf?folderId=db3a30433a047ba0013a69f8f64c0705&fileId=db3a30433f565836013f5cbaba342d37, last accessed on [15.02.2014].

[34] B. Abdi, A. H. Ranjbar, G. B. Gharehpetian, J. Milimonfared, “Reliability considerations for parallel performance of semiconductor switches in high-power switching power supplies”, IEEE Transactions on Industrial Electronics, pp.2133-2139, 2009.

[35] “Parallel operation of DC power modules” Wall Industries Application Note, https://www.wallindustries.com/docs/appnotes/Parallel_Operation_Of_DC_Power_Modules_AN.pdf, last accessed on [15.02.2014].

[36] K. Siri, C. Q. Lee, “Current distribution control of converters connected in parallel”, Industry Applications Society Conf., pp.1274-1280, 1990.

[37] P. Zumel, O. Garcia, J. A. Cobos, J. Uceda, “Magnetic integration for interleaved converters”, IEEE-APEC Conf., pp.1143-1149, 2003.

[38] J. A. Oliver, P. Zumel, O. Garcia, J. A. Cobos, J. Uceda, “Passive component analysis in interleaved buck converters”, IEEE-APEC Conf., pp.623-628, 2004.

[39] Y. Y. Law, J. H. Kong, J. C. P. Liu, N. K. Poon, “Comparison of three topologies for VRM fast transient application”, IEEE-APEC Conf., pp.210-215, 2002.

[40] H. Mao, L. Yao, C. Wang, I. Batarseh, “Analysis of inductor current sharing in nonisolated and isolated multi-phase DC-DC converters," IEEE Transactions on Industrial Electronics, pp. 3379-3388, 2007.

[41] X. Zhou, P. Xu, F. C. Lee, “A novel current sharing control technique for low-voltage high-current voltage regulator module applications", IEEE Transactions on Power Electronics, pp. 1153-1162, 2000.

[42] R. Foley, R. C. Kavanagh, M. G. Egan, “Sensorless current estimation and sharing in multi-phase buck converters”, IEEE Transactions on Power Electronics, pp.2936-2946, 2012.

[43] J. C. Schroeder, M. Petersen, F. W. Fuchs, “One sensor current sharing in multi-phase interleaved DC-DC converters with coupled inductors”, IEEE-EPE/PEMC Conf., pp.DS3c.1-1-DS3c.1-7, 2012

[44] X. Zhang, L. Corradini, D. Maksimovic, “Sensorless current sharing in digitally controlled two-phase buck DC-DC converters”, IEEE-APEC Conf., pp.70-76, 2009.

[45] S. Chae, Y. Song, H. Jeong, "Digital current sharing method for parallel interleaved DC-DC converters using input ripple voltage", IEEE Transactions on Industrial Informatics, pp.536-544, 2012.

[46] P. Zumel, C. Fernandez, A. Castro, O. Garcia, “Efficiency improvement in multi-phase converter by changing dynamically the number of phases”, IEEE-PESC Conf., pp.1-6, 2006.

[47] W. Qiu, C. Cheung, S. Xiao, G. Miller, “Power loss analyses for dynamic phase number control in multi-phase voltage regulators”, IEEE-APEC Conf., pp.102-108, 2009.

[48] A. Costabeber, P. Mattavelli, S. Saggini, “Digital time-optimal phase shedding in multi-phase buck converters”, IEEE Transactions on Power Electronics, pp.2242-2247, 2010.

[49] P. L. Wong, P. Xu, B. Yang, F. C. Lee, “Performance improvements of interleaving VRMs with coupling inductors”, IEEE Transactions on Power Electronics, pp.499-507, 2001.

[50] P. A. Dahono, S. Riyadi, A. Mudawari, Y. Haroen, “Output ripple analysis of multi-phase DC-DC converters”, IEEE-PEDS Conf., pp.626-631, 1999.

[51] J. Li, C. R. Sullivan, A. Schultz, “Coupled inductor design optimization for fast response low voltage DC-DC converters”, IEEE-APEC Conf., pp.817-823, 2002.

[52] H. B. Shin, J. G. Park, S. K. Chung, H. W. Lee, T. A. Lipo, “Generalized steady-state analysis of multi-phase interleaved boost converter with coupled inductors”, IEEE Proceedings Electric Power Applications, pp.584-594, 2005.

[53] P. W. Lee, Y. S. Lee, D. K. W. Cheng, X. C. Liu, “Steady state analysis of an interleaved boost converter with coupling inductors”, IEEE Transactions on Industrial Electronics, pp.787-795, 2000.

[54] Hioki3334 wattmeter product datasheet, Hioki Inc., http://www.hioki.com/file.php?t=catalog&iid=1_659, last accessed on [15.02.2014].

[55] “Kool μ powder cores application note”, Magnetics Inc., http://www.mag-inc.com/design/technical-documents, last accessed on [15.02.2014].

[56] Kool μ 77894 product datasheet, Magnetics Inc., http://www.mag-inc.com/products/powder-cores/kool-mu, last accessed on [15.02.2014].

[57] Kool μ material curves, Magnetics Inc., http://www.mag-inc.com/products/powder-cores/kool-mu/kool-mu-material-curves, last accessed on [15.02.2014].

[58] S. Lee, “How to select a heat sink”, Aavid Thermalloy Application Note, https://www.aavid.com/sites/default/files/technical/papers/how-to-select-heatsink.pdf, last accessed on [15.02.2014].

[59] N. Seshasayee, “Understanding thermal dissipation and design of a heat sink”, Texas Instruments Application Note, http://www.ti.com/lit/an/slva462/slva462.pdf, last accessed on [15.02.2014].

[60] Matlab R2008a, Mathworks Corporation, 2008.

[61] L. Balogh, “Design and application guide for high speed MOSFET gate drive circuits”, Texas Instruments Application Note, http://www.ti.com/lit/ml/slup169/slup169.pdf, last accessed on [15.02.2014].

[62] 62024P-80-60 Power supply product datasheet, Chroma Inc., http://www.chromausa.com/pdf/62000P.pdf, last accessed on [15.02.2014].

[63] TPS2024 Oscilloscope product datasheet, Tektronix Inc., http://www.tek.com/datasheet/tps2000b-series, last accessed on [15.02.2014].

[64] i30s AC/DC current clamp product datasheet, Fluke Inc., http://www.farnell.com/datasheets/1520312.pdf, last accessed on [15.02.2014].

[65] TMS320F28335 Digital signal processor product datasheet, Texas Instruments., http://www.ti.com/product/tms320f28335, last accessed on [15.02.2014].

[66] TMS320F28335 Digital signal processor docking station product datasheet, Texas Instruments., http://www.ti.com/tool/tmdsdock28335, last accessed on [15.02.2014].

[67] E. Dallago, M. Passoni, G. Sassone, "Lossless current sensing in low-voltage high-current DC-DC modular supplies", IEEE Transactions on Industrial Electronics, pp.1249-1252, 2000.

[68] H. P. Forghanizadeh, G. A. Rincon-Mora, "Current sensing techniques for DC-DC converters", IEEE-MWSCAS Conf., pp.577-580, 2002.

[69] AD629 Difference amplifier product datasheet, Texas Instruments., http://www.analog.com/static/imported-files/data_sheets/AD629.pdf, last accessed on [15.02.2014].

[70] Ansoft Simplorer, V7.0, Ansoft Corporation, Pittsburgh, PA, 2004.

[71] IXTP44N10T MOSFET datasheet, IXYS, http://ixapps.ixys.com/DataSheet/DS99646A(IXTY-TP44N10T).pdf, last accessed on [15.02.2014].

[72] MBR10100CT Schottky diode datasheet, Vishay, http://www.vishay.com/docs/89125/mbr1090c.pdf, last accessed on [15.02.2014].

[73] 1140-331-RC Inductor datasheet, Bourns Inc., http://www.bourns.com/pdfs/bourns_jwmiller_magnetics.pdf, last accessed on [15.02.2014].

[74] IRF540N MOSFET datasheet, International Rectifier, http://www.irf.com/product-info/datasheets/data/irf540n.pdf, last accessed on [15.02.2014].

[75] DSA10I100PM Schottky diode datasheet, IXYS, http://ixdev.ixys.com/DataSheet/DSA10I100PM.pdf, last accessed on [15.02.2014].

APPENDIX A

Inductor Design Program

```
%Inductor design program is a sub-module of the main optimization
%program. It can also be used as a stand-alone tool for inductor design
%if "I", "Ltarget" and "ripple"  parameters are manually set. The inductor
%program designs the optimal inductor and feeds the important inductor
%properties such as core and conduction losses, inductor volume etc. to
%the main optimization program.

flag=1; %program runs for flag=1
counter=1; %counter is initiated
curdens=600; %current density for inductor winding in A/cm2
tempriseallowed=40; %the allowable temperature rise


%Program runs until a suitable inductor is created (flag becomes zero).
%Counter<500 condition is placed to avoid an infinite loop in the case of a
%possible coding error
while( flag && (counter<500))


% Important properties of the smallest core that the program starts with
% are given below.
A=44.01*1.02^(2*(counter-1)); %Core cross sectional area in mm2
l=52.09*1.02^(counter-1); %Core length in mm
a=60; %Relative permitivity
b=340.44*1.02^((counter-1)); %NI value that corresponds to 50% permitivity
volume=2.29*1.02^(3*(counter-1)); %Core volume in cm3
MTL=4.31*1.02^(counter-1); %Mean length of a turn in cm
coreweight=13.25*1.02^(3*(counter-1)); %Core weight in gr
surfarea=1663*1.02^(2*(counter-1)); %Core surface area in mm2
windowarea=105.05*1.02^(2*(counter-1)); %Window area in mm2
realvolume=4.33*1.02^(3*(counter-1));%Total volume occupied by inductor cm3


%Necessary parameters such as average current, target inductance and
%current ripple is given by the main optimization program. For the use as a
%stand-alone inductor design program, the user can manually enter the three
%values below
I=Iuserwants;
Ltarget=Luserwants;
```

```
ripple=rippleuser;

%Constants used for equation 3.4, provided by core manufacturer
aa=1.658e-4;
bb=2.301e-5;
cc=7.297e-5;
dd=5.906e-3;
ee=6.053e-5;

%PROGRAM START

%First, a rough estimation on the required number of turns is made by
%solving equation 3.1 under the assumption that core degradation due to DC
%bias is linear
kkk=((A*I*a*pi*4e-4)/(2*b*l)); %intermediate calculation step
m=[kkk,-A*a*4e-4*pi/l,0,Ltarget];
% one root of the above equation gives correct number of turns
n=roots(m);
i=1;
N=0; %Number of turns value is denoted with "N" and it is set to zero at
%the beginning

%The roots of equation "m" will be tested. Imaginary or negative roots are
%discarded since they make no sense for number of turns value.
while(i<4)
   if((imag(n(i))==0)&& (n(i)>0))
      N=n(i); %The proper root has been reserved under variable "N".
   else
   end
   i=i+1;
end

%H value under the determined N in Amp.Turns/cm is found
AmpT=N*(I+ripple);
%Wirearea, wire diameter and the space that will be filled with the winding
%are calculated
wirearea=I/curdens;
wirediam=20*sqrt(wirearea/pi);
wirespace=wirediam*wirediam*N;


%Program checks if the winding can fit to the window area
```

```
if (wirespace < (0.9*windowarea))
   wirefit=1;
else
   wirefit=0;
end

%Program checks if the resultant ampere.turns is smaller than 50% NI value
if ( AmpT < b)
   Hfit=1;
else
   Hfit=0;
end



if((N==0)|| (wirefit==0) || (Hfit==0)) %If any of these expressions are
%true, then the core under examination is not a possible solution. Program
%considers the next core.
   counter=counter+1;
else

N=round(N); %N value is rounded to the nearest integer

%Fine tuning step: this time equation 3.3 will be used for the
%determination of permitivity rather than the linear approximation.
%Required constants for equation 3.3 is given in x,y,z, and w.
x=-4.445e-3;
y=-8.763e-5;
z=9.446e-7;
w=-2.616e-9;

diff=10000;
%Temporary variable indicating the difference between target inductance and
%the inductance obtained by the current configuration.

%Now several number of turns value in the vicinity of N are checked. The N
%value which gives the closest inductance to target inductance will be
%found.
i=round(N/2);
while (i<N+6)
   T=(i*I)/(l/10);
   u=a*(1+x*T+y*T^2+z*T^3+w*T^4);%Precise calculation of permitivity
   Ltunedtemp=i*i*A*pi*4e-4*u/l;
```

```
    if (abs(Ltarget-Ltunedtemp)<diff)
        diff=abs(Ltarget-Ltunedtemp);
        Ltuned1=Ltunedtemp;
        Ntuned1=i;
        Tpeak=(i*(I+ripple))/(l/10);
        uatfull=a*(1+x*Tpeak+y*Tpeak^2+z*Tpeak^3+w*Tpeak^4);
        %Full load permitivity is also noted.
    else
    end
    i=i+1;
end

%No load inductance is also calculated.
Lnoload=Ntuned1*Ntuned1*A*pi*4e-4*a/l;

%Next, inductor losses will be calculated. But first, magnetic swing under
%given conditions should be found.

H1=(Ntuned1*(I-ripple))/(l/10); %minimum Amp.Turns/cm value
H2=(Ntuned1*(ripple+I))/(l/10); %maximum Amp.Turns/cm value
B1=sqrt((aa+bb*H1+cc*H1^2)/(1+dd*H1+ee*H1^2));%min. flux density in Tesla
B2=sqrt((aa+bb*H2+cc*H2^2)/(1+dd*H2+ee*H2^2));%max. flux density in Tesla
deltB=0.5*(B2-B1);%Flux swing

%Core loss density is found by equation 3.9 provided by the manufacturer.
corelossdens=193*deltB^2.01*f^1.29;
%Core loss is found by multiplying core loss density with volume.
coreloss=corelossdens*volume;

%DC resistance is found as equation 3.5 suggests.
wirearea=I/curdens; %cm2
wirelength=MTL*Ntuned1; %cm
Rdc=((172e-5)*wirelength)/wirearea; %in mOhm

%For AC resistance, skin effect is considered. Double winding is assumed.
r=sqrt(wirearea/(2*pi))*0.01; %in meter
Dpen=sqrt(0.172/(4*pi^2*f*1000)); %penetration depth
Rac=Rdc*((pi*r^2)/((pi*r^2)-pi*(r-Dpen)^2)); %AC resistance

%Inductor loss calculation:
Pcond=Rdc*I^2 + Rac*((2*ripple)/sqrt(3))^2;
Ptotal=(Pcond+coreloss)/1000; %in mW
```

```
%Next decision point is temperature rise: reject core if high.
temprise=(100*(Pcond+coreloss)/surfarea)^0.833;

if(temprise<tempriseallowed)%thermal limit is also safe
    flag=0;%inductor design complete and the necessary parameters are fed
            %back to main optimization program
    totalindweight=wireweight+coreweight;
    Rinddc=Rdc;
    Rindac=Rac;
    Indcoreloss=coreloss;
    totalcorevolume=volume;
    totalrealvolume=realvolume;
else
   counter=counter+1; %proceed to the next core and continue searching
end
end
end
```

APPENDIX B

Main Optimization Program

```
%Main optimization program spans frequencies between 25 and 150 kHz
%and inductors that correspond to 10 to 30% current ripple at each
%frequency value for number of phases varying between 1 and 5 to find
%optimal design points. It can plot graphs of efficiency, volume, cost and
%FoM  for (f, L, N) parameters. Additionally, a written report is generated
%to summarize the design extrema.


clc

hscostdg=0.07;  %Here, the $/cm3 values are declared for heatsink,
indcost=0.06;     %inductor core and copper.
copcost=0.03;

PhaseNum=1;     %Calculations start with phase number equals to one.

while(PhaseNum<6) %Phase numbers between 1 and 5 will be considered.
disp('N=')
disp(PhaseNum)%Phase number is displayed as the calculations progress.

f=25; %Frequency starts with 25 kHz, then all values between 25 and 150
        %will be spanned

create_variables %This script creates the variables used in calculations
                 %such as efficiency, volume etc. in the form of 1x100
                 %matrices with all elements equal to zero.
while(f<151)

   %For the current frequency value, corresponding L values which yield
   %10 to 30 percent current ripple, are determined.
   %Formula for buck converter inductor current ripple is:
   %ripple=(Vin*D*(1-D))/(f*L)

   Lmin=14000/(f*10.8); %Minimum L corresponds to 10.8A ripple
   Lmax=14000/(f*3.6);  %Maximum L corresponds to 3.6A ripple
```

```
%Having determined maximum and minimum values for L, an L matrix is
%created by dividing these extrema by 100.
L=linspace(Lmin,Lmax,100);

k=1; %counter for spanning L
 while(k<101)

   curripple=14000/(f*L(k)); %Calculates the cuurent ripple for
                             %current f and L values.

   %f, L and N is known, next step is to feed the necessary
   %information to inductor design module so that an optimal inductor
   %is created by it

   Iuserwants=36/PhaseNum; %Declearing the average DC value for the
                           %inductor
   Luserwants=L(k);       %Declearing the target inductance value
   rippleuser=curripple/2; %Declearing the current ripple value.

   ind_program %Inductor design program has been run. Now, we have an
               %inductor designed for the conditions determined, core
               %and conduction losses are known along physical
               % properties of the inductor.

   Iindavg=28/PhaseNum; %800W operation corresponds to 28A output,
                        %average inductor current can be found by
                        %dividing 28 by phase number

   %Average value and ripple known, rms value of the inductor current
   %is found
   Iindrms=sqrt((Iindavg+curripple/2)*(Iindavg-curripple/2)+(curripple^2)/3);
   Iswavg=Iindavg/2; %average value of MOSFET current is found.
   Iswrms=Iindrms*sqrt(0.5);%rms value of MOSFET current is found.
   Idiodeavg=Iindavg/2;%average value of diode current is found.
   Idioderms=Iindrms*sqrt(0.5);%rms value of diode current is found.

   %Having acquired current values, losses are calculated next.
   %Equations adopted for loss analyses are described in "3.2.3
   %Converter Loss Modelling"
   %Note that, due to "equal current capacity" approach, effective DC
   %values are increasing proportionally with increasing phase number,
   %maintaining equal overall resistance.
   swcond=Iswrms^2*0.015*PhaseNum; %conduction loss for MOSFET
```

```
        %Switching loss for MOSFET is calculated
        swswloss=(28*f)*((Iindavg-currripple/2)^2+(Iindavg+currripple/2)^2)/300000;
        %Conduction loss for diode is calculated
        diodeloss=Idiodeavg*0.6+Idioderms^2*0.00125*PhaseNum;
        %Inductor conduction loss has been retrieved from inductor program.
        indcondloss(k)=Pcond/1000;
        %Inductor core loss has been retrieved from inductor program.
        Pcore(k)=Indcoreloss/1000;

        %Losses being calculated, the resultant volume will be found.
        %With 6 cm3 heat sink assumption per 1W loss heat sink volume is
        %found
        %Inductor volume is provided by inductor design program, overall
        %inductor volume is found by multiplying it by total number of
        %inductors
        totvol(k)=(swcond+swswloss+diodeloss)*6*PhaseNum+totalrealvolume*PhaseNum;

        %Cost is found by the multiplication of volume and predetermined
        %cost density values

cost(k)=(swcond+swswloss+diodeloss)*6*hscostdg*PhaseNum+totalcorevolume*indcost*P
haseNum+wirearea*wirelength*copcost*PhaseNum+12;

        %As additional information, inductor volume to total volume and
        %heat sink volume to inductor volume ratios are determined.
        ratio(k)=(totalrealvolume*PhaseNum)/totvol(k);
        hsinktoindratio(k)=((swcond+swswloss+diodeloss)*6)/totalrealvolume;

        %Loss terms have been added to yield the overall loss
        totalindloss(k)=indcondloss(k)+Pcore(k);
        loss(k)=(swcond+swswloss+diodeloss+indcondloss(k)+Pcore(k))*PhaseNum+(10e-
5*f);

        %Finally, efficiency, power density and FoM values are found
        eff(k)=80000/(800+loss(k));
        powdens(k)=1000/totvol(k); %W/cm^3
        merit(k)=(317*42.6)/(totvol(k)*loss(k));

        %Calculations continue with the consideration of the next L value
        k=k+1;
    end

   %With the span from the minimum to maximum L values is complete, this
   %array of 100 elements is evaluated. Important points such as maximum
```

```
    %efficiency, minimum volume etc. are recorded and the f,L,N point where
    %it occurs is noted.
    important_point_select_script_app

    %Obtained results are plotted. Each plot operation is for values
    %between Lmin and Lmax for a specific f and N. Later, by the complete
    %sweping of f and N, the overall picture will be completed. User can
    %arrange any parameter (efficiency, volume etc.) that s/he wants to    observe.
    %Note that different colors are adopted to imply different phase
    %number values.
    if(PhaseNum==1)
    plot3((f*ones(1,100)),L,eff,'LineWidth',3)
    hold on
    else if(PhaseNum==2)
    plot3((f*ones(1,100)),L,eff,'r','LineWidth',3)
    hold on
    else if(PhaseNum==3)
    plot3((f*ones(1,100)),L,eff,'g','LineWidth',3)
    hold on
    else if(PhaseNum==4)
    plot3((f*ones(1,100)),L,eff,'y','LineWidth',3)
    hold on
    else if(PhaseNum==5)
    plot3((f*ones(1,100)),L,eff,'m','LineWidth',3)
    hold on
    else
    end
    end
    end
    end
    end
    %When the plotting operations is finished, frequency is increased by
    %one and the whole procedure is repeated again.
    f=f+1;
end

%With all of the inductance values between Lmin and Lmax for all
%frequency values between 25 and 150kHz are spanned, the analysis for N=1
%condition is complete.
%Now, important points such as maximum efficiency, minimum volume etc. and
%the points where they occur recorded by the important point select script,
%is shown to user with the code below which simply displays those recorded
%points.
result_display_scriptwithcost
```

```
%The analysis continues with the consideration of the next value of N.
PhaseNum=PhaseNum+1;
end
%With all N between 1 and 5 being considered, the analysis is complete.
%The resultant graph is now displayed along the written report which
%informs the user with important points.
 grid on
```