ELIMINATION OF TRANSFORMER CORE SATURATION IN CASCADED MULTILEVEL CONVERTER BASED T-STATCOM SYSTEMS

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ABSTRACT

ELIMINATION OF TRANSFORMER CORE SATURATION IN CASCADED MULTILEVEL CONVERTER BASED T-STATCOM SYSTEMS

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This research work is devoted to the description of coupling transformer core saturation phenomenon and its elimination by modulated firing algorithms in Cascaded Multilevel Converter (CMC) based T-STATCOM systems. Transmission-type Static Synchronous Compensator (T-STATCOM) is connected to the transmission voltage level (≥110kV) via a coupling transformer. The coupling transformer may be an existing Medium Voltage (MV) to High Voltage (HV) or Extra High Voltage (EHV), or a specially designed transformer. This thesis work deals with coupling transformer core saturation problem in Cascaded Multilevel Converter (CMC) based T-STATCOM systems. The effects of nonlinear characteristics of the coupling transformer and CMCs on the core saturation phenomenon are investigated, and the associated mechanisms are described. Imbalance in positive and negative cycles of the converter output voltage waveform, 2^{nd} harmonic voltage at the ac primary side, and low operation flux density of the

transformer may lead to asymmetric saturation of the coupling transformer core. Transformer core saturation results in significant increase in not only in dc current but also in the 2nd harmonic current and hence voltage component at the ac side of the converter. Furthermore, the 2nd harmonic voltage component will be reflected to the dc side of the converter in the form of ac voltage component at supply frequency. Dc current components in the coupling transformer secondary lines are eliminated by modulating one or more than one voltage steps of staircase CMC voltage waveforms via the electronic gating circuitry. The proposed dc current elimination method is implemented on a 154-kV, ±50-MVAr CMC based T-STATCOM system, which is operating either in inter-area oscillation damping or terminal voltage regulation modes at any time in a 400/154-kV transformer substation since March 2010. The effectiveness of recommended dc current elimination method is verified in the field.

Keywords: Cascaded Multilevel Converter (CMC), dc current elimination, transformer core saturation, Transmission-type Static Synchronous Compensator (T-STATCOM)

ÖZ

KASKAT BAĞLI ÇOK SEVİYELİ ÇEVİRGEÇ TEMELLİ İLETİM STATKOM'U SİSTEMLERİNDE TRAFO ÇEKİRDEK SATÜRASYONUNUN GİDERİLMESİ

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Bu araştırma çalışması, kaskat bağlı çok seviyeli iletim STATCOMu sistemlerindeki kuplaj trafosu çekirdek satürasyonu olgusunun açıklanmasına ve değiştirilmiş ateşleme algoritmaları ile giderilmesine adanmıştır. İletim-tipi Statik Senkron Kompanzatör (T-STATCOM) iletim seviyesine (≥110kV) kuplaj trafosu aracılığı ile bağlanmaktadır. Kuplaj trafosu, halihazırda bulunan bir Orta Gerilim (OG), Yüksek Gerilim (YG) ya da Çok Yüksek Gerilim (ÇYG) trafosu veya özel tasarlanmış bir trafo olabilir. Bu tez çalışması, Çok Seviyeli Kaskat Çevirgeç (CMC) tabanlı T-STATCOM sistemlerindeki kuplaj trafosu çekirdek satürasyonu problemi ile ilgilidir. Kuplaj trafosu ve CMClerin doğrusal olmayan karakteristiklerinin çekirdek satürasyonu olgusu üzerine etkileri araştırılmış ve ilişkili mekanizmalar açıklanmıştır. Çevirgeç çıkışı gerilim dalga şeklindeki pozitif ve negatif çevrimler arasında bulunan dengesizlik, primer aa taraftaki 2. harmonik gerilim ve trafonun düşük tasarlanmış akı yoğunluğu, kuplaj trafosu çekirdeğinin asimetrik satürasyonuna yol açabilir. Trafo çekirdek satürasyonu, çevirgecin aa tarafında sadece da akımda değil aynı zamanda 2. harmonik akım ve dolayısıyla gerilimde

büyük miktarda yükselişe sebep olur. Ayrıca 2. harmonik gerilim, çevirgecin da tarafına şebeke frekansında bir gerilim bileşeni olarak yansımaktadır. Trafo sekonderindeki da akım bileşenleri, merdiven şeklinde gerilim dalga şekillerine sahip olan CMClerin bir veya birden fazla gerilim adımının, elektronik anahtarlama devresi kullanılıp değiştirilmesi ile elenmektedir. Önerilen da akım eleme yöntemi, 400/154 kV bir trafo merkezinde Mart 2010 dan beri faaliyette bulunan 154-kV, ±50-MVAr gücünde CMC tabanlı bir T-STATCOM sistemine uygulanmıştır. Bu sistem bölgeler-arası salınım bastırma veya bara gerilimi regülasyonu modunda çalışmaktadır. Önerilen da akım eleme yönteminin etkinliği sahada kanıtlanmıştır.

Anahtar Kelimeler: Çok Seviyeli Kaskat Çevirgeç (CMC), da akım elemesi, trafo çekirdek satürasyonu, İletim-tipi Statik Senkron Kompanzatör (T-STATKOM)

To My Family

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

NOMENCLATURE

E_s': Internal source voltage referred to CMC side

I_c: Fundamental component of the CMC line current

L_r Series filtering reactor inductance value

PCC: Point of Common Coupling

P_c, Q_c: Active and reactive power inputs to CMC

P_s, Q_s: Active and reactive power inputs to T-STATCOM at PCC

R: Total series resistance including internal resistance of the coupling transformer referred to CMC side and internal resistance of the input filter reactors

X: Total series reactance including leakage reactance of the coupling transformer referred to CMC side and reactance of input filter reactors

X_s': Internal source reactance referred to CMC side

V_c: Fundamental component of the CMC ac voltage

V_s': Fundamental voltage component at Point of Common Coupling (PCC) referred to CMC side

Z: Impedance angle, $\tan^{-1}(X/R)$

θ: Phase angle between $\vec{V}_c$ and $\vec{I}_c$

δ: Power angle between $\overrightarrow{V'}_s$and $\vec{V}_c$.

ABBREVIATIONS

CMC	Cascaded Multilevel Converters
CSS	Conventional Selective Swapping
DCMC	Diode Clamped Multilevel Converters
D-STATCOM	Distribution type STATCOM
FACTS	Flexible Alternative Current Transmission Systems
FCMC	Flying Capacitor Multilevel Converters
GTO	Gate Turn-off thyristors
HB	H-Bridge
HECS	Hall Effect Current Sensor
IGBT	Insulated Gate Bipolar Transistors
IGCT	Integrated Gate Commutated Thyristors
MC	Multilevel Converter
MV	Medium Voltage
MSS	Modified Selective Swapping
PCC	Point of Common Coupling
RCVT	Resistive-Capacitive Voltage Transformer
SHEM	Selective Harmonic Elimination Method
STATCOM	Static Synchronous Compensators
SVC	Static VAr Compensators
T-STATCOM	Transmission type STATCOM
TCR	Thyristor Controlled Reactor
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TSC	Thyristor Switched Capacitor

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

There existed only dc sources composed of chemical batteries when electricity first started to be used. The increase in demand of electricity brought out the necessity of electricity being transferred through distances. As the distances between the place of generation and consumption grew, the power transfer started to be infeasible due to the large amount of power loss and voltage drop. These would be decreased significantly by the use of higher voltage levels, but it's always been a problem for dc voltage to be boosted for transmission and then reduced at distribution level. On the other hand, ac voltage had the advantage of being transformed into high values from low values or vice versa by use of transformers. The use of ac and transformers make it possible to transfer huge amounts of energy through long distances.

The use of ac results in the inevitable need for reactive energy, which is stored in magnetic and/or electric fields created by transformers, lines and most of the loads. In parallel with the need of reactive power, the stability of ac power system and voltage regulation are other issues that should be taken into account.

The reactive power need not be produced where the active power is generated. It can be produced where and when it is needed by use of special equipment. In order not only to supply the reactive power need (mostly capacitive), but also to control the active power flow, and hence enhance voltage regulation and stability in ac power

transmission systems, Flexible Alternative Current Transmission Systems (FACTS) devices are being increasingly used. These devices include power semiconductors that can be switched on and off in order to control active and reactive power flow at the point where it is needed. FACTS devices can be divided into three categories [1]:

- Series devices,
- Shunt devices
- Combined series-shunt devices.

The shunt devices are the most used ones due to the fact that using appropriate amount of compensated reactive power, the transmitted power carrying capacity can be increased and the voltage profile of the transmission line can be controlled. Furthermore, they can be used for load balancing, flicker mitigation and power factor correction, especially at distribution level.

Static Synchronous Compensators (STATCOM) and Static VAr Compensators are the two shunt FACTS devices. SVCs consist of power semiconductor switched inductor and/or capacitors. They can produce or absorb reactive power at desired magnitude. However, the reactive power value is directly proportional to the square of voltage magnitude. On the other hand, STATCOMs can produce rated reactive power regardless of the voltage magnitude, as long as the current limits for STATCOM equipment like power semiconductors, capacitors and inductors are not violated, i.e., the limiting factor for the output reactive power for STATCOMs is the current rating.

In Thyristor Switched Capacitor (TSC) based SVC systems, one or more than one stage of capacitor banks or harmonic filter banks are switched in and out by use of line commutated thyristors. Most of the time, there exists a microcontroller that measures the reactive power needed and decides on which stages to take into or out of conduction. A simple single line diagram of a TSC based SVC system is given in Figure 1.1. It is seen in this figure that the stages consist of harmonic filters instead

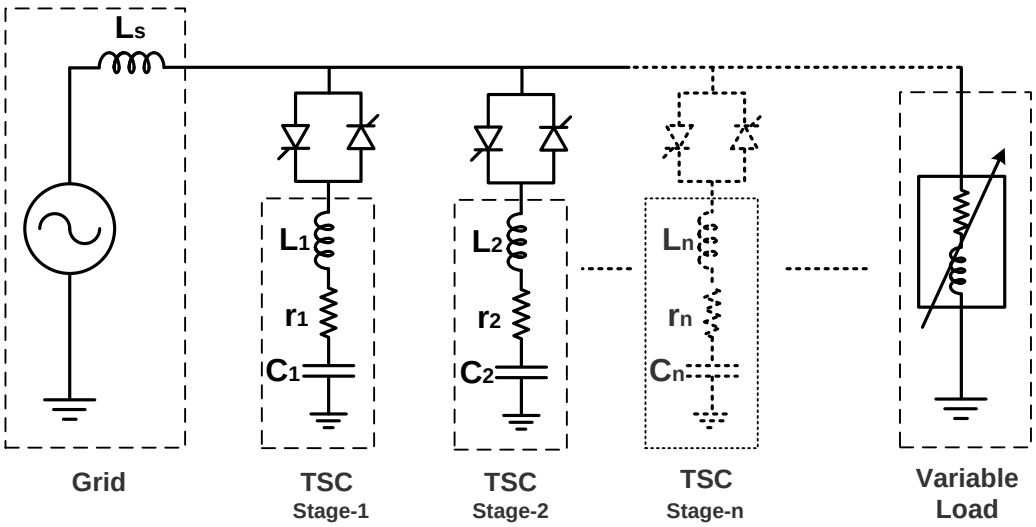


Figure 1.1 Single line diagram of a TSC based SVC system

of plain capacitor banks. This configuration is chosen when there are harmonics to be filtered (tuned harmonic filters are used), or when there is a risk of parallel harmonic resonance (de-tuned harmonic filters are used).

Another SVC configuration is built up using Thyristor Controlled Reactor (TCR) and Harmonic Filters (HF). The triggering angles of thyristors are changed according to the need of load. When reactors are fully in conduction, no reactive power is produced by the TCR+HF combination, whereas maximum reactive power is produced when the reactors are taken out of conduction by turning the thyristors off. A simple single line diagram of a TCR based SVC system is given in Figure 1.2.

Different from SVCs, STATCOMs employ power semiconductors with turn-off capability. The idea of STATCOM comes from synchronous condenser. A synchronous condenser is an unloaded (no active power except the losses of the machine itself) synchronous machine connected to and running in synchronism (same frequency and phase angle) with the grid. When the field current of the machine is increased so that its output voltage is greater than the grid voltage, the machine produces reactive power (capacitive mode of operation). On the other hand,

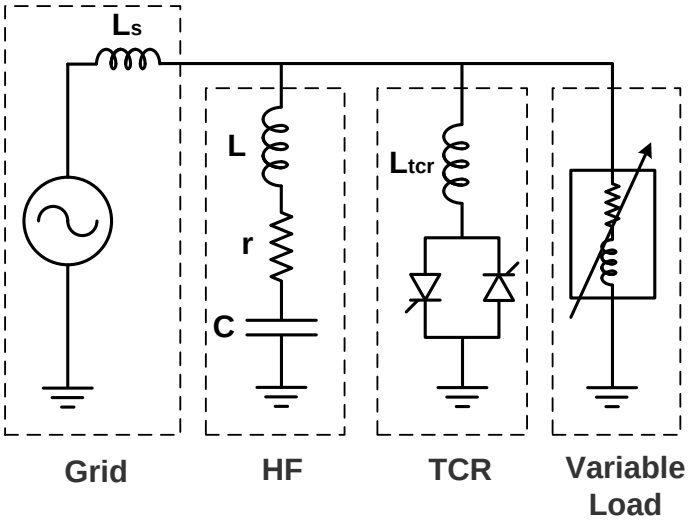


Figure 1.2 Single line diagram of a TCR based SVC system

when the field current of the machine is decreased so that its output voltage is less than the grid voltage, it absorbs reactive power (inductive mode of operation).

The magnitude of the reactive power generated/absorbed depends directly on the output voltage of the machine and also the value of coupling inductance between the machine and the grid. However, the response time of the machine depends on its electrical and mechanical time constants, which undermines the transient response of synchronous compensator.

As an accelerated alternative of synchronous compensator, STATCOM can respond to changes of reactive power demand very quickly (only in a few cycles). It uses Voltage Source Converter (VSC) or Current Source Converter (CSC) based topologies in order to produce the desired voltage magnitude at its output. Although CSC based STATCOMs exist, most of the STATCOMs employ voltage source converters.

STATCOM is connected to the grid via a coupling reactor, which is used for both limiting the reactive power transfer and also filtering of any current harmonics that may be produced by STATCOM converter. A simple single line diagram of a STATCOM system is shown in Figure 1.3.

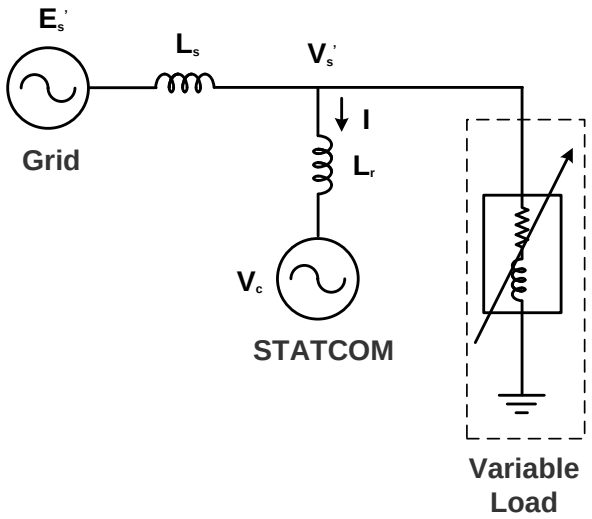


Figure 1.3 Single line diagram of a STATCOM system

For Figure 1.1, Figure 1.2, and Figure 1.3, the coupling transformers between the grid and reactive power compensation systems are not shown.

The STATCOM converters used in transmission system applications should control a few tens or hundreds of MVArs, operate at medium voltage levels and are connected to EHV or HV transmission system buses via specially designed coupling transformers. These are called Transmission-type STATCOMs (T-STATCOM) in the literature [2]. The STATCOMs connected to MV level either directly or via a specially designed coupling transformer are called Distribution-type STATCOMs (D-STATCOM). Following functions are performed by T- and D-STATCOMs [3]:

1) terminal voltage regulation [4], [5],
2) control of reactive power flow in overhead (O/H) [2], or load lines [6]–[9],
3) suppression of light flicker [10]–[14], or
4) power system stability improvement [15],[16] including inter-area oscillation damping [17].

These are achieved by varying the reactive power generated by the STATCOM rapidly and steplessly in both capacitive and inductive regions.

Various Multilevel Converter (MC) topologies operating at switching frequencies at or near the supply frequency fit best to the needs of T-STATCOMs. In T-STATCOM systems, the use of 6-pulse converters is not feasible owing to the need for series connected power semiconductor switches, and much higher switching frequencies for waveform synthesizing. Multilevel Converters for T-STATCOM applications are classified in three groups [18]:

a) Diode Clamped (or Neutral Point Clamped) Multilevel Converters (DCMC),
b) Flying Capacitor Multilevel Converters (FCMC),
c) Cascaded Multilevel Converters (CMC).

The use of three-level neutral point clamped converters employing series connected power semiconductor stages [19] or two-level, six-pulse bridge converters [6]–[9] with relatively high switching frequencies and relatively low installed capacities is the characteristic of distribution-type STATCOM (D-STATCOM) systems. These are connected to the MV distribution or load bus either directly [20], [21] or via a step-up, semi-custom coupling transformer [22]. In a D-STATCOM, either a voltage-source converter (VSC) having a capacitor in the dc link and series reactors on the ac side, or a current-source converter (CSC) having a reactor in the dc link and shunt-connected capacitors on the ac side can be employed. However, transmission-type STATCOM (T-STATCOM) systems have much higher installed capacities, and therefore the power semiconductors in their converter system/s should be switched at lower frequencies [23]. Various multilevel converter (MC) topologies, e.g., cascaded multilevel converter (CMC), operating at switching frequencies at or near the supply frequency fit best to the needs of T-STATCOMs.

For much higher MVAr ratings, more than one, i.e., "*m*" number of CMCs should be operated in parallel in a T-STATCOM system. Since VSCs are usually the characteristic of MC of T-STATCOM, each converter should have its own series-connected input filter reactor. MCs are usually designed for operation at MV level and connected to EHV or HV bus via a semi-custom coupling transformer.

Sometimes they may be connected to the MV side of an existing power transformer [24].

The circuit configuration of a CMC is shown in Figure 1.4. As seen from the figure, each phase of the CMC consists of "*n*" number of H-Bridges (HB) connected in series, whereas an HB consist of four IGBTs together with their inverse-parallel connected diodes, a dc link capacitor, a discharge resistor and a discharge IGBT.

Equalization problem of the dc link capacitor voltages is the common drawback of MC topologies. Among these, CMC topology has the advantage of modularity, flexibility and lower component count in comparison with the others. Commercial CMC based T-STATCOMs employ either GTO or GCT/IGCT devices with inverse-parallel connected power diodes. To limit di/dt overvoltages on GTOs during turn-off operation, bulky snubber circuits were used. To equalize individual capacitor voltages, high frequency IGBT based auxiliary circuits supplied from low voltage side were employed. Specially designed isolating transformers were used to isolate auxiliary circuits from the power stage of CMC.

An important contribution to the solution of voltage equalization problem of dc link capacitors is known as the Selective Swapping Algorithm [25] which can be embedded in the control algorithm of CMC, thus eliminating the need for bulky auxiliary circuits. Although the effectiveness of voltage equalization algorithm decreases as the number of HBs connected in series and/or peak-to-peak ripple content of the capacitor voltage increase/s, it provides the lowest switching frequency for the power semiconductors.

The most common connection types of STATCOM systems are summarized in Figure 1.5, in which grey-colored parts are the existing power system components and black-colored parts are the new installations. STATCOM systems are subject to voltage regulation problem on the ac side when the reactive power is varied from full

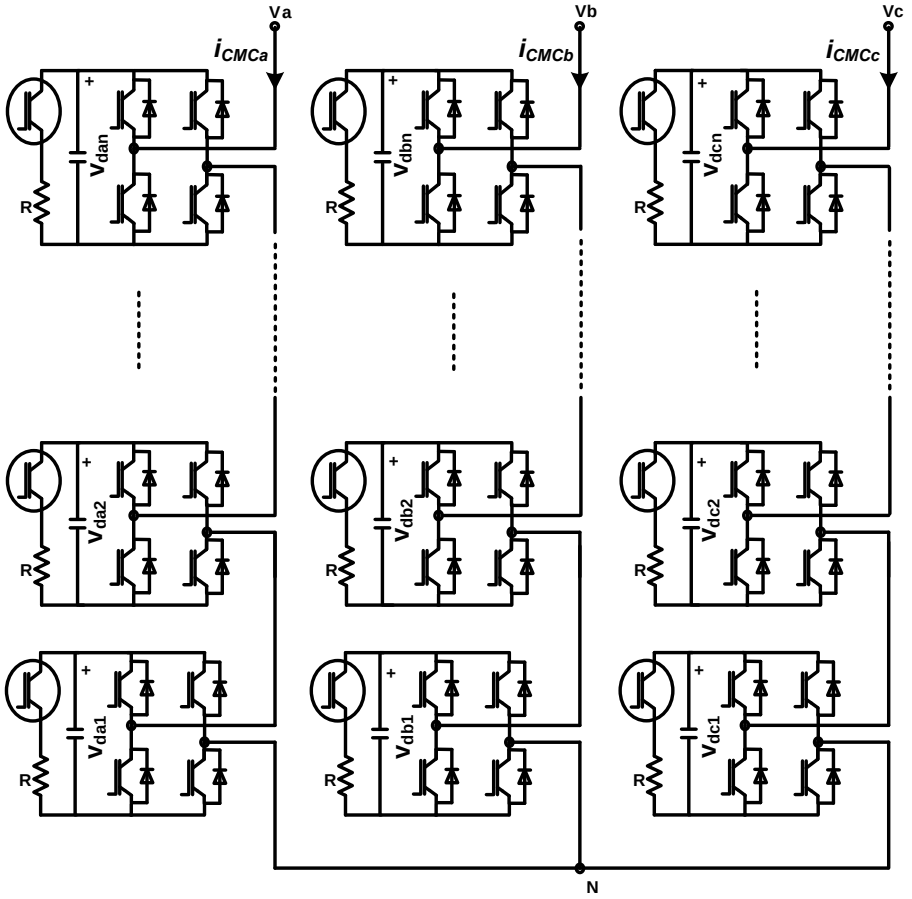


Figure 1.4 Circuit configuration of a CMC

inductive to full capacitive. This will affect the voltage rating of the power semiconductors as well as the design of input filter, and may lead to saturation of coupling transformer core. Coupling transformer core saturation may also result from dc current component injected by the converter.

Transformer core saturation problem in high power applications has been reported first for high voltage direct current (HVDC) transmission systems [26]. This problem in line-commutated converter based HVDC transmission systems has been investigated in [27]–[35] and different countermeasures such as installation of harmonic filters [28], [29] or dc blocking capacitors [36], firing angle modulation [37], and etc. have been proposed. Transformer core saturation instability, harmonic

instability and possible precautions for HVDC systems have been explained in [38] and [39].

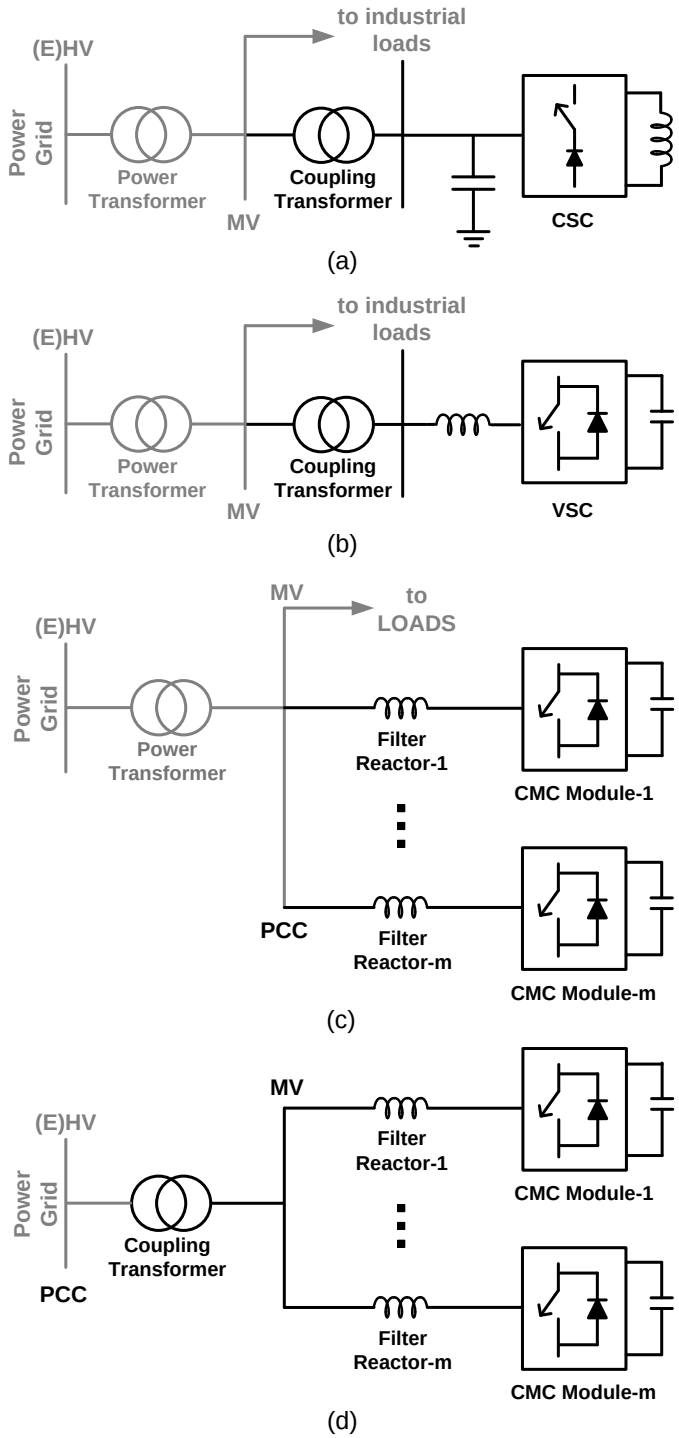


Figure 1.5 Connection of STATCOM system to the grid / grey: existing grid components; black: newly installed STATCOM components

Modeling of a STATCOM which is connected to the grid via a transformer has been achieved in time domain in [40], and the interaction of harmonics generated by the converter transformer and the voltage source of the STATCOM is examined by neglecting dc flux component in the coupling transformer core. In [41], harmonics arising from coupling transformer asymmetrical core saturation have been attributed to the difference between the forward and backward thyristor stacks of thyristor switched or controlled reactor systems. A phasor solution method has been recommended in [42] for calculating transformer generated harmonics in electromagnetic transients program simulation studies by considering a symmetrical magnetization characteristic. Effects of design value of transformer core flux under presence of a dc flux component on transformer magnetizing current harmonics have been investigated in [43].

A new control method preventing transformer dc magnetization for two-level, multipulse voltage source GTO converters with inter-magnetics has been proposed in [24]. This method is based on the control of pulse widths to reduce rapidly the dc voltage in the system to zero. The major sources of transformer dc magnetization are stated to be high inrush currents of neighboring large transformers and power system faults.

Direct current injected by a transformerless cascaded multilevel converter based STATCOM laboratory prototype (±100-kVAr, 1-kV line-to-line, delta-connected, 12 HBs in each phase) is investigated in [44]. Generation of dc is attributed to nonideal current sensing and high gain of the controller in the output current feedback loop at very low frequency. Dc current injected by this system is eliminated by controlling pulse widths of all HBs simultaneously and results are verified experimentally in the laboratory. Dc offset in the magnetization characteristic of a single-phase high frequency transformer is reported in [45] for low power phase-shift full-bridge converters. This problem has been solved by the addition of a compensation duty cycle, when the offset arises in the positive direction.

In existing D-STATCOM systems, coupling transformer core saturation problem has not been reported yet. Furthermore, for D-STATCOMs presented in [6]–[9], this problem has not been observed because their coupling transformers in Figure 1.5-b were designed at flux densities (around 1.4T), lower than those of conventional distribution transformers.

This is the first research work reporting the transformer core saturation problem in an actual CMC based T-STATCOM system, which is connected to a 154-kV transmission bus via a dedicated coupling transformer. Transformer core saturation is shown to be triggered by the nonlinear operating characteristics of the coupling transformer and CMC/s, and explained by the cross-modulation phenomenon across the ac-ac-dc link of the T-STATCOM. Various countermeasures against this problem are discussed and among these, a fully-electronic method is recommended in this thesis to prevent the coupling transformer core from being saturated. Dc current elimination in the lines of the coupling transformer secondary is shown to be based on narrowing/widening output voltage positive and/or negative half-cycle/s of one HB in each phase of the CMC, or all HBs simultaneously. Their performances are calculated theoretically, and then compared in view of digital control range, precision of digital pulse-width control, distortion of line-to-neutral voltage waveforms, and THD of CMC line-to-line output voltage. Among these, narrowing the pulse width of one of the HBs symmetrically, has been chosen for implementation due to its best precision figure. In this work, the transformer core saturation phenomenon is illustrated and the effectiveness of recommended dc current elimination technique is verified by extensive field test results.

1.2 SCOPE OF THE THESIS

This research work reports transformer core saturation problem in a ±50-MVAr CMC based T-STATCOM system connected to the 154-kV transmission bus via a coupling transformer (Figure 1.5-d). Transformer core saturation is shown to be triggered by the nonlinear operating characteristics of coupling transformer and

CMC/s. Various countermeasures against this problem are discussed and a fully-electronic method is recommended in this thesis to prevent the coupling transformer core from being saturated. The effectiveness of recommended dc current elimination technique is verified in the field.

The 154-kV, ±50-MVAr, 21-level T-STATCOM system by the parallel use of five CMCs built in scope of this work has been implemented in the field primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. Since the operating voltage of CMC is chosen to be 10.5-kV (max.12-kV) line-to-line, it is connected to 154-kV line-to-line transmission bus through a specially designed 50/62.5-MVA Y-Y connected coupling transformer and each CMC module is connected to the secondary side of the coupling transformer via a series filter reactor bank.

This is the first application of CMC based T-STATCOM with wire-bond HV IGBTs and Modified Selective Swapping (MSS) Algorithm in the world. The use of bulky auxiliary circuits for equalization of the dc link voltages has been eliminated and a compact HB unit has been designed and implemented. The Conventional Selective Swapping (CSS) Method has been modified in order to enhance the voltage equalization of HB dc links.

The outline of the thesis is given below:

In Chapter 2, system description, operating principles and field performance for the 154-kV, ±50-MVAr, 21-level CMC based T-STATCOM system have been given. Active and reactive power control with waveform synthesizing used for STATCOM systems are presented. The Modified Selective Swapping Algorithm proposed in order to solve the equalization problem of dc link capacitors is described. Field performance of the T-STATCOM system is discussed.

Chapter 3 defines the transformer core saturation problem for the sample T-STATCOM system. The mechanism of transformer core saturation and interaction between harmonics and nonlinear B-H characteristic of coupling transformer core are described. The field observations for the sample T-STATCOM regarding the transformer core saturation are also discussed.

In Chapter 4, elimination of transformer core saturation is presented. The proposed dc current elimination method is explained in detail. Then the simulation results for the sample system implementing the elimination method are given. Verification of the effectiveness of the proposed method is made via field tests and results are included in this chapter.

Conclusions and recommendations for the future work are given in Chapter 5.

CHAPTER 2

SYSTEM DESCRIPTION, OPERATING PRINCIPLES AND FIELD PERFORMANCE

2.1 GENERAL INFORMATION AND SYSTEM COMPONENTS

The first T-STATCOM in Turkey was designed and implemented by Power Electronics Department of TÜBİTAK UZAY (now known as Electrical Power Technologies Department of TÜBİTAK MAM Energy Institute), and has been in service in Sincan (Ankara, Turkey) Transformer Substation since March 2010. Its ratings are 154-kV and ±50-MVAr. It is composed of five 10.5-kV, ±12-MVAr CMC modules which are connected in parallel via air-core reactors. 11-level line-to-neutral voltage and hence 21-level line-to-line voltage waveforms are created by using five series connected HBs in each phase of the Y-connected CMC modules. This system can be classified in the class of Single-Star Bridge-Cells within the Modular Multilevel Cascade Converter family according to [46].

This T-STATCOM has been designed and implemented primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. It is equipped with a digital control system, except some analog interface and protection circuits. Figure 2.1 shows the schematic diagram of the T-STATCOM system. Interior views of the T-STATCOM are given in Figure 2.2, Figure 2.3, Figure 2.4 and Figure 2.5. Transformer core saturation is investigated

and eliminated for this system, therefore the basic information about the system is given in this chapter.

2.1.1 Coupling Transformer

The combination of five STATCOM modules is connected to 154-kV bus via a 154/10.5-kV, 50/62.5-MVA, Y-Y connected coupling transformer. The neutral point of the primary is solidly grounded while that of the secondary is grounded via a 6.93Ω grounding resistor to limit line-to-ground fault current to 1-kA. The transformer primary has 25 on-load taps. By using these taps, the secondary voltage can be adjusted in 0.1-kV steps while the primary voltage is 154-kV. The tap is left at 23rd for the sample system, so that the secondary voltage is 10.1-kV when the primary voltage is 154-kV. The short circuit impedance, u_k of the coupling transformer is 17%.

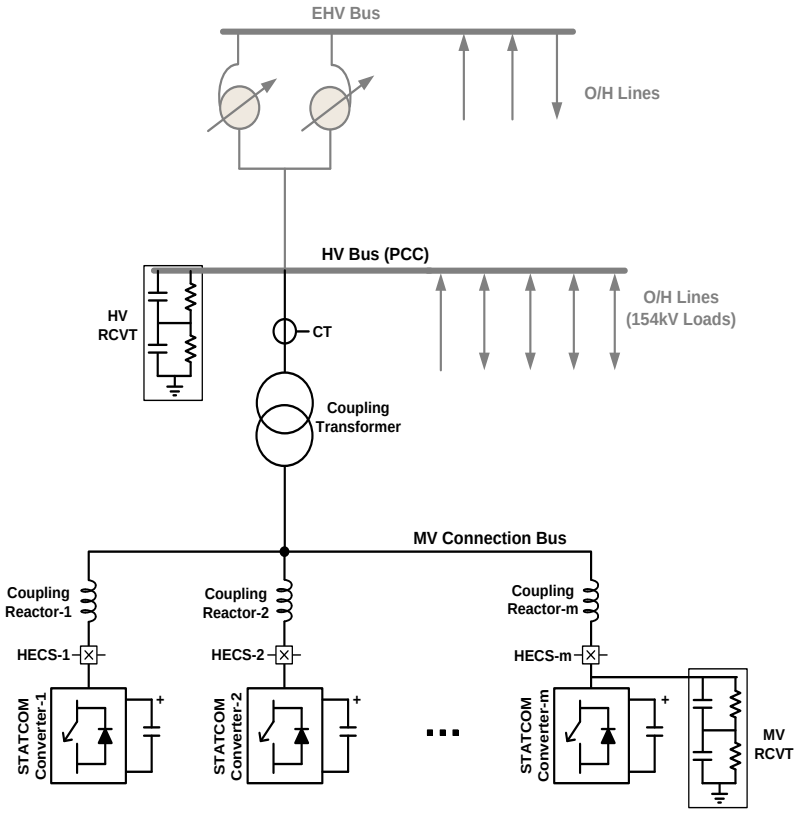


Figure 2.1 Schematic diagram of the sample T-STATCOM which is subject to transformer core saturation problem / RCVT: Resistive-capacitive voltage transformer; HECS: Hall effect current sensor, m: Number of parallel CMCs

In Figure 2.1, HV RCVTs are connected to the PCC in order to get precise measurements for transformer primary voltage harmonics, whereas MV RCVTs are connected to the CMC output in order to measure both the voltage harmonics and any dc component of converter output voltages.

2.1.2 Air-Core Coupling Reactors

Each CMC has an optimized series filter reactor on its ac side as shown in Figure 2.1. Its optimum value has been determined by considering the total demand distortion (TDD) limit for weak supply according to IEEE Std. 519-1992, and also the voltage regulation at the ac side of the CMC from full capacitive to full inductive operation mode. Optimum value of filter reactor is marked on Figure 2.6 for the physical T-STATCOM mentioned above. In this figure, it is seen that the THD created by the STATCOM decreases as the series inductance gets larger, however this causes a higher CMC output voltage change between maximum inductive and maximum capacitive regions. Percentage voltage regulation, *PVR* of each CMC is defined as given in eqn. (2.1).

$$PVR = \frac{V_{rc} - V_{ri}}{V_{nl}} 100 \qquad (2.1)$$

where, V_{rc} is CMC line-to-line voltage for full capacitive operation mode, V_{ri} for full inductive operation mode, and V_{nl} no-load (Q=0) voltage of the CMC and these are the rms values of fundamental components of the associated distorted CMC voltage waveforms.

Series filter reactor value is of importance also for putting the limits of reactive power delivered/absorbed when converter output maximum and minimum voltage are pre-defined. As in the case of CMC, where specified harmonics like 5^{th}, 7^{th}, 11th, 13^{th}, etc are to be eliminated using Selective Harmonic Elimination (SHEM), corresponding triggering angles of HBs can be found for a defined interval of modulation index, *M*. Therefore the fundamental component of the produced CMC

output voltage will have a maximum and minimum value dictated by the solution of nonlinear equations that equate the defined harmonic components to zero.

Figure 2.2 Interior view of T-STATCOM power stage room

Figure 2.3 T-STATCOM control cabinets

Figure 2.4 T-STATCOM trailer on road

In Figure 2.5, ①: Air-core series filter reactor banks, ②: 154/10.5-kV coupling transformer and its HV switchgear equipment, ③: MV switchgear, ④: Control room, ⑤: Power stage, ⑥: De-ionized water cooling pump station, ⑦: Water-to-air heat exchanger.

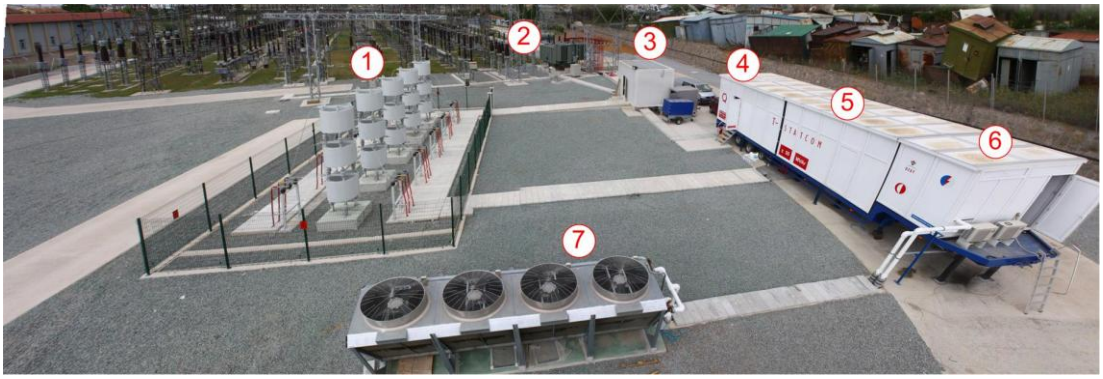


Figure 2.5 General view of T-STATCOM System

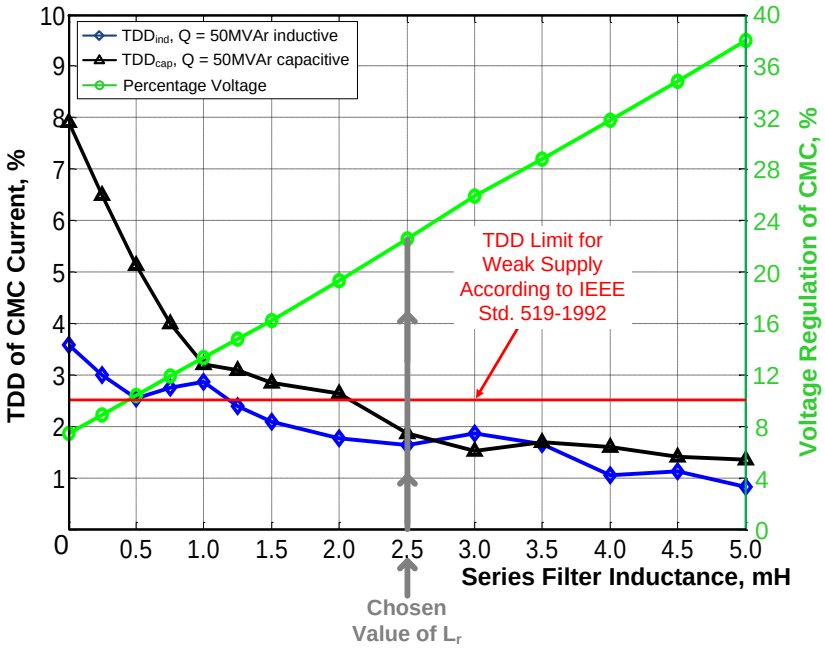


Figure 2.6 Effects of series filter inductance on TDD of CMC line current waveform and *PVR* of CMC as defined in eqn. (1)

The choice of a filter reactor lower than the optimum value leads to undesirably high harmonic content, and higher values result in a more expensive series filter reactor bank, higher CMC voltages, and hence higher power semiconductor voltage ratings and *PVR* values for the CMC. It is worth to note that transformer secondary voltage and hence the exciting branch voltage are independent of the design value of L_r.

They depend only upon the amount of reactive power delivered by T-STATCOM, grid voltage, and coupling transformer parameters.

2.1.3 Dc Link Capacitors

The dc link of each HB is formed by connecting two 4.6-mF MKP capacitors in parallel. In constructing 11 levels in line-to-neutral and 21 levels in line-to-line voltage waveforms, *K* of the dc links are connected in series while the remaining 5-*K* dc links are bypassed by properly chosen power semiconductor switching patterns in each phase of the CMC module. Therefore the equivalent dc link capacitance, C_{eqv} of each CMC module is given by (2.2).

$$C_{eqv} = 9.2/K \text{ mF} \quad (2.2)$$

where, *K*=1,2,...,5 is the number of dc link capacitors connected in series out of five.

2.1.4 Power Semiconductors

The power semiconductors in a CMC should have turn-off capability. Therefore GTOs, IGCTs or IGBTs can be used. Regarding factors such as conduction losses, switching losses, need for snubber, availability and price in this T-STATCOM system, IGBTs were chosen among these choices. The chosen IGBTs have their inverse-parallel diodes in the package. Their voltage and current ratings are 3300V, 1200A.

2.1.5 Other HB Components

Other HB components include IGBT driver cards, HV isolated power supply to feed the IGBT driver cards, capacitor voltage measurement card, capacitor overvoltage protection card, laminated ac and dc busbars, copper water-cooled heatsink to cool the IGBTs, and finally the main frame to hold the HB equipment together. As a summary, ±12-MVAr, 10.5-kV 21-level CMC module consists of 15 pieces of ±840-kVAr HB units. Table 2.1 summarizes the technical specifications of each HB, CMC module and the resulting T-STATCOM system.

The photograph of the CMC prototype in MV laboratory is given in Figure 2.7. In this figure the HB is also shown at the right-top of the figure, where

1) L-shape laminated buses, L_{stray}=70nH
2) Two pairs of HV IGBTs (3300V, 1200A)
3) Front panel with optical connectors
4) Fiber reinforced composite based chassis
5) Two parallel dc link capacitors
6) Water pipe pairs with quick coupling
7) Glass-fiber reinforced polyester based structure of Power Stage (3x5 matrix)

Table 2.1 T-STATCOM, CMC and HB specifications

T-STATCOM	
Rated Power	±50 MVAr
Rated Voltage	154 kV
Coupling Transformer	Y-Y, 154/11.1 kV, 50/62.5 MVA, 17% u_k
Number of CMC Modules in Parallel	5
Cascaded Multilevel Converters (CMC)	
Rated Power	±12 MVAr
Rated Voltage	10.5 kV
Number of H-Bridges per phase	5
Number of Levels in Voltages	11 Levels Line-to-Neutral, 21 Levels Line-to-Line
Harmonics Eliminated by SHEM	5^{th}, 7^{th}, 11^{th}, 13^{th}
Coupling Reactors	2.5mH, air core
Cooling System	De-ionized water cooling
H-Bridges (HB)	
Rated Power	±840 kVAr
Rated Voltage	1.8 kV rms
Power Semiconductor	3300V, 1200A HV IGBT with parallel inverse diode
Effective Switching Frequency	500Hz
Design Value of DC Link Voltage	1900Vdc
DC Link Capacitor* **Metallized Polypropylene (MKP)*	9.2mF (4.6mF//4.6mF) ±10%
	260A rms, 2000Vdc
	250V peak-to-peak ripple

Figure 2.7 The view of CMC lab prototype and HB

The coupling transformer, HV and MV switchgear equipment, series filter reactors and the water-to-air heat exchanger of this system are installed outdoor. The power stage, the control system and part of the de-ionized water cooling system excluding water-to-air heat exchanger are placed into a non-magnetic container mounted on the trailer. The aspects of HB and CMC design and implementation are discussed in detail in [47].

2.2 OPERATING PRINCIPLES

2.2.1 Active and Reactive Power Flow

Single-phase Y-equivalent circuit model of the T-STATCOM and its phasor diagram are given in respectively in Figure 2.8 and Figure 2.9 where,

E_s': Internal source voltage referred to VSC side

X_s': Internal source reactance referred to VSC side

PCC: Point of Common Coupling

V_s': Fundamental voltage component at PCC referred to VSC side

R: Total series resistance including internal resistance of the coupling transformer referred to VSC side and internal resistance of the input filter reactors

V_c: Fundamental component of the VSC ac voltage

I_c: Fundamental component of the VSC line current

θ: Phase angle between $\overrightarrow{V_c}$ and $\overrightarrow{I_c}$

δ: Power angle between $\overrightarrow{V_s'}$ and $\overrightarrow{V_c}$

ϕ: Impedance angle, $\tan^{-1}(X/R)$

P_s, Q_s: Active and reactive power inputs to T-STATCOM at PCC

P_c, Q_c: Active and reactive power inputs to VSC

X: Total series reactance including leakage reactance of the coupling transformer referred to VSC side and reactance of input filter reactors

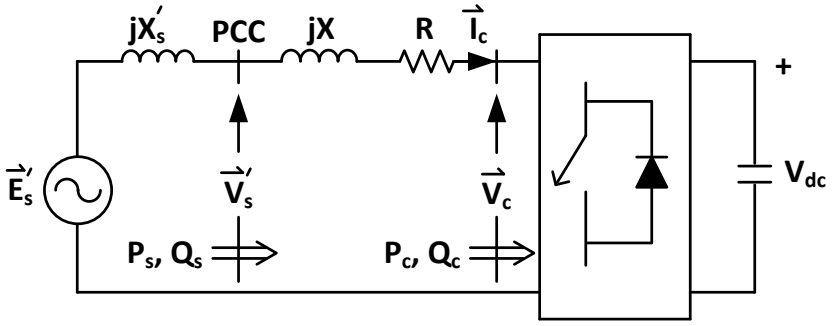


Figure 2.8 Simplified single line diagram of T-STATCOM

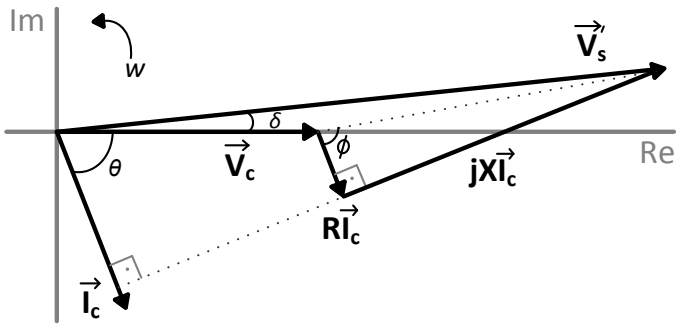


Figure 2.9 Phasor diagram for lossy system (exaggerated)

In Figure 2.8, all voltages and currents are rms values and active and reactive powers are per phase values. P_s, P_c, Q_s and Q_c in Figure 2.8 can be expressed respectively as in (2.3), (2.4), (2.5) and (2.6), in terms of terminal quantities V_s' and V_c and angles θ and δ.

$$P_s = V_s' I_c Cos(\theta + \delta) \tag{2.3}$$

$$P_c = V_c I_c Cos\theta \tag{2.4}$$

$$Q_s = V_s' I_c Sin(\theta + \delta) \tag{2.5}$$

$$Q_c = V_c I_c Sin\theta \tag{2.6}$$

I_c and θ in (2.3)–(2.6) can be eliminated as given in Appendix. The operations given yield the power expressions in (2.7)–(2.10).

$$P_s = V_s' \left[V_c X Sin\delta - V_c R Cos\delta + V_s' R \right] / Z^2 \tag{2.7}$$

$$P_c = V_c \left[V_s' X Sin\delta + V_s' R Cos\delta - V_c R \right] / Z^2 \tag{2.8}$$

$$Q_s = V_s' \left[V_s' X - V_c X Cos\delta - V_c R Sin\delta \right] / Z^2 \tag{2.9}$$

$$Q_c = V_c \left[V_s' X Cos\delta - V_c X - V_s' R Sin\delta \right] / Z^2 \tag{2.10}$$

where, $Z = \sqrt{(R^2 + X^2)}$

P_c can be related to P_s in terms of power dissipation on R as in (2.11). In a similar way, Q_c can be related to Q_s in terms of the reactive power absorbed by X.

$$P_c = P_s - I_c^2 R \tag{2.11}$$

$$Q_c = Q_s - I_c^2 X \tag{2.12}$$

Since $I_c^2 R$ plays no basic part in the control of reactive power and since R is small in comparison with X, R in Figure 2.8 and in (2.7)–(2.11) will be neglected. According to this assumption, active power, P transferred between $\overrightarrow{V_s'}$ and $\overrightarrow{V_c}$ can be expressed as in (2.13).

$$P = P_s = P_c = \left(V_s^{'} V_c / X\right) Sin\delta \qquad (2.13)$$

P is very small during the operation of the VSC in the steady state, to supply only the VSC losses and hence δ takes a very small value (δ is around 0.017 rad ≡ 1 degree). For such small values of δ, $Sin\delta \approx \delta$ holds, and hence P can be approximated by (2.14):

$$P = \left(V_s^{'} V_c / X\right) \delta \qquad (2.14)$$

By substituting R=0, (2.9) and (2.10) will reduce respectively to (2.15) and (2.16).

$$Q_s = V_s^{'} \left[\left(V_s^{'} - V_c Cos\delta\right) / X\right] \qquad (2.15)$$

$$Q_c = V_c \left[\left(V_s^{'} Cos\delta - V_c\right) / X\right] \qquad (2.16)$$

Since δ is very small, $Cos\delta \approx 1$ holds. Hence (2.15) and (2.16) can be approximated to (2.17) and (2.18), respectively.

$$Q_s = V_s^{'} \left[\left(V_s^{'} - V_c\right) / X\right] \qquad (2.17)$$

$$Q_c = V_c \left[\left(V_s^{'} - V_c\right) / X\right] \qquad (2.18)$$

Complex power input, $\vec{S} = P + jQ_s$ to the T-STATCOM is defined according to power sink convention. P is always positive in the steady-state to compensate for coupling transformer, series filter reactor and VSC losses. However, the sign of Q_s depends upon the operation mode of the T-STATCOM, i.e. positive for inductive mode of operation and negative for capacitive mode. θ is positive ($\approx +\pi/2$) for inductive mode of operation in the steady state while it is negative ($\approx -\pi/2$) for capacitive mode. The transition between capacitive and inductive mode of operations occurs when $Q_c = I_c^2 X_c = 0$, which corresponds to unity power factor (*pf*) operation of the T-STATCOM at PCC.

Active power into the T-STATCOM is controlled by varying δ in order to keep the dc link capacitor voltages constant at a pre-specified value over the entire operating range in both transient-state and steady-state. δ is always positive in the steady-state under the assumption of R=0. However, δ may have negative values for inductive

operation mode of the T-STATCOM ($V_s' > V_c$) when R is not neglected. This occurs for very small values of δ and even for a practical X/R ratio. This phenomenon is apparent from (2.7) and (2.8). This small negative value for δ does not reverse the direction of real power flow for the operation of the system given in Figure 2.8 in the steady-state. For capacitive operation mode however, since $V_s' < V_c$; δ is always positive as can be understood from (2.7) and (2.8).

Q_s and Q_c are controlled by varying V_c by PWM technique. If V_c is made smaller than V_s', T-STATCOM operates in inductive operation mode as can be understood from (2.17). On the other hand, if V_c is made sufficiently higher than V_s', it starts to operate in capacitive operation mode and delivers reactive power to the supply. In practice, the situation is more complex, because the supply is not an infinite bus. That is, the capacitive operation mode causes a rise in the supply voltage, V_s', while the inductive operation causes a drop.

2.2.2 Waveform Synthesizing

The input voltage waveform of VSC, $v_c(t)$ will be approximated to a pure sinusoidal voltage at supply frequency by using the CMC topology and SHEM. It is well known that the number of voltage levels, s, in the staircase voltage waveform in Figure 2.10 produced by CMC is defined by (2.19) and (2.20):

$s=2n+1$ in the line-to-neutral voltage (2.19)

$s=4n+1$ in the line-to-line voltage (2.20)

where, n is the number of HBs in one phase. For the T-STATCOM described in this work, CMC yields 11 voltage levels in the line-to-neutral voltage waveform and 21 voltage levels in the line-to-line voltage waveform.

As illustrated in Figure 2.10, five pulses with different widths and the same magnitudes (V_d) are to be superimposed in order to create a half-cycle of an 11-level line-to-neutral voltage waveform. This makes necessary assigning five different angles $\theta_1, \theta_2, \ldots, \theta_5$ in such a way that the harmonic distortion of line-to-neutral

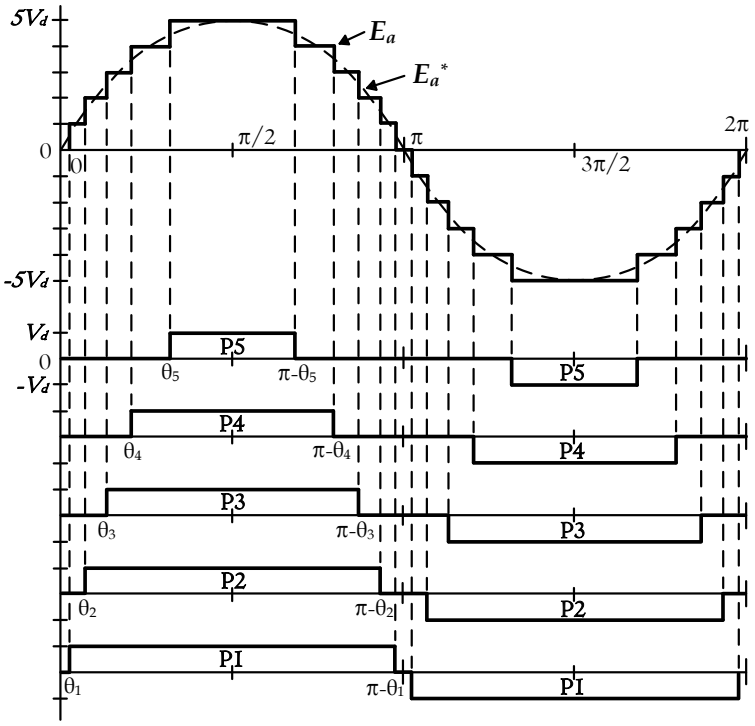


Figure 2.10 11-level line-to-neutral voltage waveform of CMC

voltage waveform will be minimum. 3rd harmonic and its integer multiples will not appear in the line-to-line voltage waveform for balanced operation. There remains only the elimination of dominant voltage harmonics which are the 5th, 7th, 11th and 13th. In a staircase waveform with odd-quarter symmetry, these are eliminated by using SHEM. If a lower harmonic content were allowed in line-to-line voltage waveform, a larger series filter reactor would be needed at the expense of voltage regulation problem.

The expressions which are used in the calculation of optimum values of θ_1, θ_2, ..., θ_5 using a hybrid algorithm are given in Appendix. The hybrid algorithm is a combination of the genetic algorithm [48], [49] and the gradient based method. First, the genetic algorithm is used for determination of proper initial conditions. Then, these initial conditions are applied to the gradient based method to reach the global minima much faster than the use of genetic algorithm only.

The magnitude of the CMC fundamental output voltage can be controlled by adjusting modulation index, *M*, as given in (2.21):

$M=(V_c^*/V_{cmax})$ (2.21)

where, $V_{c\max}=(\sqrt{3/2})(4/\pi)V_{dc}$, V_c* is the set value of fundamental line-to-line output voltage of CMC, and V_{cmax} denotes the maximum value of fundamental line-to-line rms voltage that can be produced by one HB in any CMC, and V_{dc} is the total mean dc link voltages of each phase of CMC.

Optimum values of θ_1, θ_2, ..., θ_5 are obtained for different modulation index values so that -50-MVAr to +50-MVAr reactive power control range is divided into approximately 200 steps and corresponding results are arranged as a 200x6 offline look-up table.

Maximum and minimum values of *M* are dictated by rated *Q*, V_s' and *X* in (2.15)−(2.18) for the design value of V_{dc}. It is worth to note that maximum value of *M* corresponds to rated *Q* in capacitive mode while minimum value of *M* to rated *Q* in inductive mode. The resolution of *Q* control depends on the number of steps between maximum and minimum values of *M*. As can be understood from (2.15)−(2.18), the number of steps in the stepwise adjustment of *M* is directly proportional to *X* for a pre-specified resolution in *Q* control.

When one or more than one CMC/s is/are disconnected from the FACTS device having *m* parallel CMCs, maximum and minimum values of *M* will be changed. This is because; equivalent series reactance *X* in Figure 2.8 depends upon the number of parallel CMCs in service. This will also affect the optimum values of PI controllers' parameters for the Reactive Power Compensation and the Terminal Voltage Regulation modes.

For the T-STATCOM system with *n*=5 and *m*=5, minimum and maximum values of *M*, together with PI controller parameters (K_p and K_i) for Reactive Power

Compensation mode as a function of the number of active CMCs, m' (out of m number of parallel CMCs) are as given in Table 2.2.

2.2.3 Equalization of Dc Link Capacitor Voltages

The major drawback of multilevel converters is the voltage balancing problem of dc link capacitors. The mean value of total dc link voltage of each CMC, V_{dc} is given by (2.22) in terms of supply voltage at PCC referred to the CMC side.

$$V_{dc} = (\pi/2\sqrt{3})V_s' \qquad (2.22)$$

where, V_s' is the rms line-to-line voltage at PCC.

Since each CMC is composed of n number of HBs in each phase, mean dc link voltage of each HB, V_d is given by (2.23).

$$V_d = V_{dc}/n \qquad (2.23)$$

V_{dc} is kept constant by P control as given in (2.13) at its design value, however V_d is to be kept nearly constant at the value given by (2.23) by a proper voltage equalization method. An important contribution to the solution of voltage equalization problem of dc link capacitors is known as the Selective Swapping Algorithm which can be embedded in the control algorithm of CMC.

Table 2.2 Maximum and minimum values of *M*, and PI parameters

Number of active CMCs, m'	min. M	max. M	K_p	K_i
1	3.10	3.80	16×10^{-6}	100×10^{-9}
2	2.95	3.90	11×10^{-6}	80×10^{-9}
3	2.80	4.00	9×10^{-6}	60×10^{-9}
4	2.65	4.08	8×10^{-6}	50×10^{-9}
5	2.50	4.13	6×10^{-6}	35×10^{-9}

The method is called the swapping algorithm because at each level change (θ_1 to θ_5 in Figure 2.10), the previous set of HB/s which are in operation is going to be interchanged with a new set in each phase of each CMC module, according to the values of dc link capacitor voltages.

If the current and the voltage are both positive or negative, the input power to the HB converter is positive and hence the associated dc link capacitor is going to be charged. On the other hand, if one of these quantities is positive while the other is negative, the input power to HB is negative and hence the associated dc link capacitor is going to be discharged. Charging, discharging and by-pass states of a typical dc link capacitor are as illustrated in Figure 2.11.

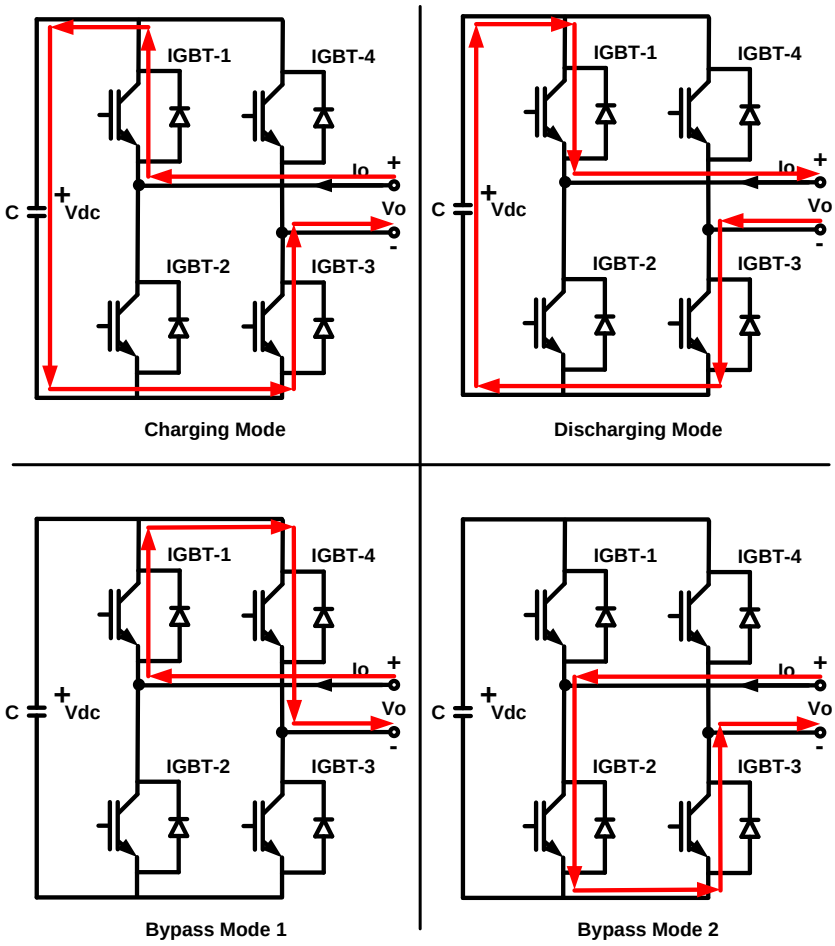


Figure 2.11 Some operation modes of an H-bridge

In order to determine which HB/s are going to be operated at each level change, the values of individual dc link capacitor voltages, polarity of the voltage and direction of the current should be measured.

The polarity of the input voltage to HBs is determined indirectly by using a PLL circuit which is locked to line-to-neutral voltage at PCC. The digital signal produced by PLL is phase advanced or delayed by power (load) angle, δ in Figure 2.8 to determine the zero crossing point of the CMC modules' fundamental line-to-neutral voltage. After determining the new status of dc link capacitors (charging or discharging) by this way, HBs having the lowest dc link voltages will be put into operation for charging and HBs having the highest dc link voltages, for discharging mode of operations. This method is called the Conventional Selective Swapping (CSS). The CSS gives minimum switching frequency for the power semiconductors.

The major drawback of the CSS is the higher variations observed in the dc link capacitor voltages as the number of HBs in each CMC is reduced. In order to eliminate this drawback, the CSS is modified and then applied to the T-STATCOM. In the Modified Selective Swapping (MSS) algorithm, selective swappings are applied not only at level changes but continuously at a pre-specified frequency during the operation of the CMC. Figure 2.12 illustrates the application of the MSS method proposed in comparison with the CSS.

It is seen in Figure 2.12 that, the swappings are made only at voltage level changes for CSS, whereas they are also made at defined time periods for MSS In the field tests of the T-STATCOM, the MSS has been applied at a pre-specified period of Δt_s=400μs and also of Δt_s=200μs, at the expense of higher switching frequency and hence switching losses. The effects of MSS on voltage balancing problem and switching frequency are discussed in [1] and [2], in comparison with those of CSS.

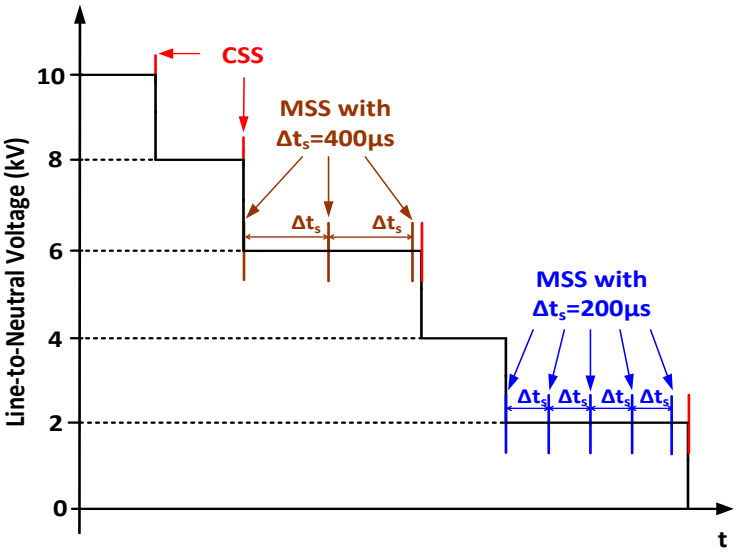


Figure 2.12 The illustration of CSS and MSS

2.2.4 Controls

Simplified block diagram of the T-STATCOM control system is given in Figure 2.13. The T-STATCOM can be operated in reactive power compensation mode (Q-mode) or terminal voltage regulation mode (V-mode) by using a selector switch. Operation at the set value of the bus voltage at PCC is achieved by closed loop control which employs the digital implementation of a simple PI controller. The operation in Q-mode tends to reduce the reactive power flow in between 154-kV bus and autotransformers in Figure 2.1 to zero.

Active power delivered by the 154-kV bus to the T-STATCOM supplies the losses of the coupling transformer, series filtering reactors and CMCs in order to keep dc link capacitor voltages at their rated values ($1900V_{dc,mean}$). This is achieved by employing a digitally implemented closed loop power (load) angle (δ in Figure 2.13) control. Furthermore, each dc link capacitor is equipped with a parallel connected, chopper controlled discharge resistor in order to protect the dc link from dangerous overvoltages. When the T-STATCOM is turned off, the chopper controlled discharge resistors are automatically activated to discharge the capacitors for safety purposes.

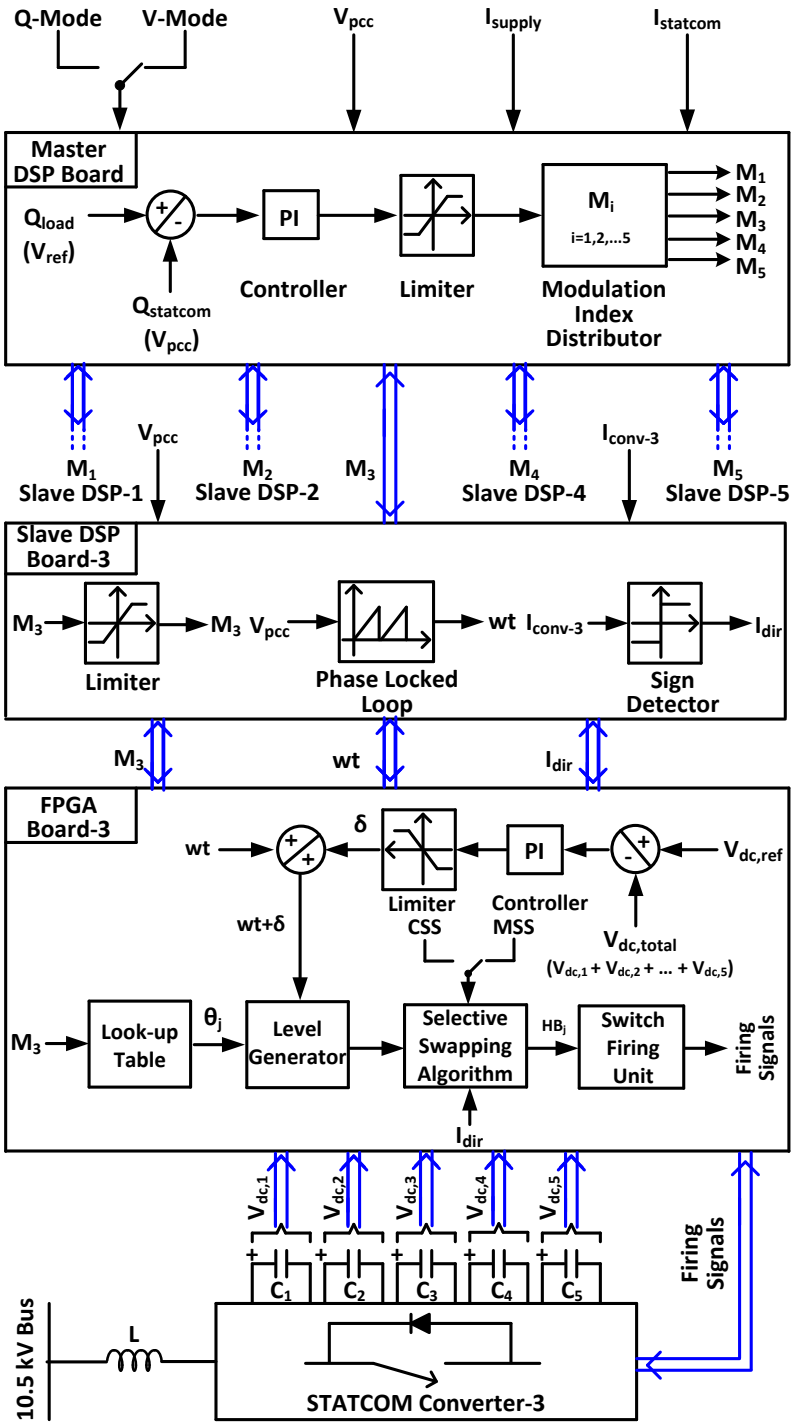


Figure 2.13 Simplified block diagram of T-STATCOM control system

The T-STATCOM is also equipped with an automatic pre-charge circuit at 10.5-kV side for cold start. The dc link capacitor voltages are increased to their set values via a pre-charge resistor.

Technical specifications and the type numbers of integrated circuit (IC) boards which are used in the sample system are given in Table 2.3. If the number of series HBs in each phase of a CMC was greater than six (n>6), either a more advanced version of FPGA board in Table 2.3 or three of the same FPGA, one for each phase of each CMC, were to be used. On the other hand, if more than five CMCs (m>5) are going to be operated in parallel in the same FACTS device, a Master DSP Expansion Board can be used between the Master DSP and Slave DSPs and also the Communication Interface Board is to be improved.

Digital communication rate is largely determined by the needs of the application. In the sample system, all necessary calculations are completed within 40μs time period. These 17 word data including modulation indices, phase angles, line current directions, dc link capacitor reference voltage, PI coefficients and check-sum words should be sent to FPGA Boards by the Slave DSP Boards as quickly as possible such as in 20μs time period. This leads to a time delay of 40μs+20μs=60μs in control action. However, the communication speed between Slave DSP Board and FPGA Board is limited by the baud rate of the chosen DSP Board which is 10 Mbits/s.

Table 2.3 Technical specifications of IC boards

Name of the IC board	Number of the boards	Number of Controller ICs on each board	Type number	Technical specifications
Master DSP Board	1	2	Texas Instruments TMS320F28335	150 MHz, 32 bit, Floating Point DSP
Slave DSP Board	m	2	Texas Instruments TMS320F28335	150 MHz, 32 bit, Floating Point DSP
FPGA Board	m	1	Xilinx Spartan 3 XCS1500	
μController in DC_VM	3×n×m	1	Cypress PSoC CY8C27443	
PLC	1	-	Siemens S7226	3 MHz CPU, 24 kB RAM
Communication Interface Unit	1	-	Custom Design	
Digital Interface Unit	1	-	Custom Design	
Industrial Computer	1	-	Advantech Uno 3072	Celeron M 1GHz CPU, 1GB RAM

To be on the safe side, the baud rate is chosen to be 9.375 Mbit/s which is 1/16 of the DSP clock frequency (150MHz). This choice is consistent with the communication limit of the chosen fiber optic receiver (HFBR-2528) and the transmitter (HFBR-1528). This choice gives 29μs + 40μs time delay in control action which is found to be quite satisfactory in the field tests.

The communication need between Master DSP and PLC is much slower than the one between Slave DSP and FPGA Boards. Synchronous Serial Data Link, which is named SPI (Serial Peripheral Interface) has been chosen wherever a high-speed, full-duplex communication is needed between the two devices. However, 210 ns maximum propagation delay in the fiber optic links of the sample application causes communication error at the input of the slave device. To compensate for this error, SPI communication has been applied in two half-duplex links between the Slave DSP and FPGA pairs. Since, the amount of data that will be transmitted from 3x*n* HBs (DC link capacitor voltages, heatsink temperatures, pressure valve status of dc link capacitors, and operation status of discharge circuits) to the associated FPGA Board in each CMC is low and hence the required communication speed is relatively slow, half-duplex asynchronous type Serial Communication Interface (SCI) has been used between DC_VM Boards and the associated FPGA Board.

A smooth transition between different Q or V settings is aimed at the design of the control system. This will minimize the oscillations in current, voltage and reactive power in transition periods and hence reduce the settling time. The extreme operating condition is the transition from full capacitive to full inductive operation mode, or vice versa. For this purpose, the changes in the modulation index have been applied only at zero crossing points of the CMC line current.

The detailed functions, specifications and units for control of the T-STATCOM system are discussed in [50].

2.3 FIELD PERFORMANCE

2.3.1 Voltage and Current Harmonics at PCC

Harmonic contents of the line-to-neutral voltages at PCC with and without T-STATCOM are as given in Table 2.4. These values are deduced from the measurements of Resistive-Capacitive Voltage Transformers (RCVT of Trench). The RCVT has a frequency bandwidth of 1-MHz and can measure low order harmonic components with unity gain. It is seen from Table 2.4 that the operation of T-STATCOM at its rated capacity in both capacitive and inductive operation modes does not affect the harmonic content of the PCC voltage. On the other hand, harmonic contents of the coupling transformer line current waveforms on the HV side (154-kV) are as given in Table 2.5. Both individual voltage and current harmonic values, and THD and TDD values comply with IEEE Std. 519-1992.

There were only two HV RCVT columns installed in Sincan transformer substation, that is why phase-a measurement results are absent in Table 2.4.

Table 2.4 PCC voltage line-to-ground harmonics

Harmonic Number	No Operation		Capacitive Mode		Inductive Mode		IEEE Std.519-1992 (%)
	$V_{b,g}$ (%)	$V_{c,g}$ (%)	$V_{b,g}$ (%)	$V_{c,g}$ (%)	$V_{b,g}$ (%)	$V_{c,g}$ (%)	
1	100	100	100	100	100	100	**100**
3	0.6	0.5	0.6	0.5	0.6	0.5	**1.0**
5	0.5	0.4	0.5	0.4	0.4	0.2	**1.0**
7	0.4	0.3	0.4	0.3	0.3	0.2	**1.0**
11	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
13	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
17	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
19	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
21	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
THD	**0.9**		**0.9**		**0.9**		**1.5**

Table 2.5 154-kV side current harmonics at rated power (I_L=188A, I_{sc}=20kA)

Harmonic Number	Capacitive Mode			Inductive Mode			IEEE Std.519-1992 (%)
	I_a (%)	I_b (%)	I_c (%)	I_a (%)	I_b (%)	I_c (%)	
1	100	100	100	100	100	100	**100**
3	0.2	0.2	0.2	0.2	0.2	0.2	**3.0**
5	0.4	0.4	0.4	0.4	0.4	0.4	**3.0**
7	0.2	0.2	0.2	0.2	0.2	0.2	**3.0**
11	0.1	0.1	0.1	0.1	0.1	0.1	**3.0**
13	0.1	0.1	0.1	0.1	0.1	0.1	**1.5**
17	0.5	0.5	0.5	0.5	0.5	0.5	**1.15**
19	0.3	0.3	0.3	0.3	0.3	0.3	**1.15**
21	0.1	0.1	0.1	0.1	0.1	0.1	**1.15**
TDD	**0.77**			**0.77**			**3.75**

2.3.2 CMC Output Voltage Waveforms

CMC output line-to-neutral voltage waveforms of three phases when the T-STATCOM is producing and absorbing rated MVAr are given in Figure 2.14 and Figure 2.15, respectively during use of MSS method with Δt_s=400µs.

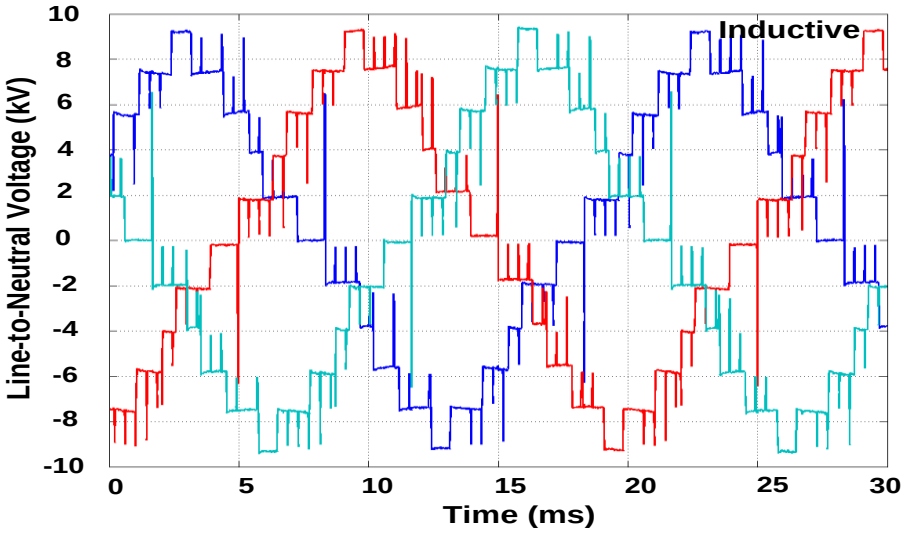


Figure 2.14 CMC output line-to-neutral voltage waveform for full inductive mode

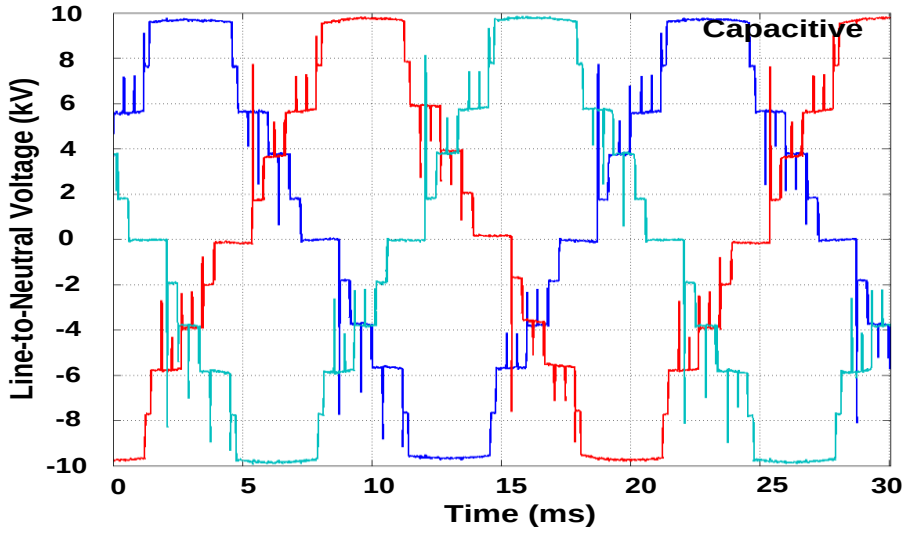


Figure 2.15 CMC output line-to-neutral voltage waveform for full capacitive mode

Harmonic contents of the line-to-neutral and the line-to-line voltage waveforms at the output of the CMC are given in Table 2.6 and Table 2.7 for rated inductive and capacitive operation modes, respectively. Following conclusions can be drawn from these results:

- The SHEM applied in this research work successfully minimizes 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics in the line-to-neutral voltage waveforms.
- Although the 3^{rd} harmonic component is significant in the line-to-neutral voltage waveforms, it becomes vanishingly small in line-to-line voltage waveforms.

Table 2.6 CMC output voltage harmonics for full-inductive mode

Harmonic Number	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	V_{ab}(%)	V_{bc}(%)	V_{ca}(%)
1	100	100	100	100	100	100
3	12.6	12.2	12.0	0.1	0.1	0.2
5	0.5	0.4	0.5	0.4	0.4	0.5
7	0.3	0.2	0.3	0.2	0.2	0.3
11	0.1	0.2	0.1	0.2	0.2	0.1
13	0.5	0.6	0.6	0.5	0.6	0.5
17	3.0	3.0	3.0	3.0	3.0	3.0
19	2.8	2.8	2.8	2.8	2.8	2.8
21	2.0	2.1	2.1	0.1	0.1	0.1

Table 2.7 CMC output voltage harmonics for full-capacitive mode

Harmonic Number	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	V_{ab}(%)	V_{bc}(%)	V_{ca}(%)
1	100	100	100	100	100	100
3	10.7	10.4	10.4	0.1	0.1	0.1
5	0.7	0.5	0.5	0.6	0.5	0.6
7	0.2	0.1	0.2	0.2	0.2	0.1
11	0.1	0.1	0.2	0.1	0.1	0.1
13	0.4	0.4	0.5	0.4	0.5	0.4
17	3.3	3.3	3.3	3.3	3.3	3.3
19	3.1	3.1	3.1	3.1	3.1	3.1
21	0.1	0.1	0.1	0.1	0.1	0.1

2.3.3 Harmonic Content at Coupling Transformer Secondary

Harmonic contents of the line-to-ground and line-to-line voltage waveforms on the medium voltage side of the coupling transformer (after series connected input filter reactor) at rated reactive power are as given in Table 2.8. These results show that voltage harmonics are filtered out by the input filter reactor to a certain extent. Harmonic contents of the line current on the medium voltage side of the coupling transformer are given in Table 2.9. Their magnitudes are relatively low, as expected.

2.3.4 Effectiveness of MSS Method

The performance of MSS method in balancing the dc link voltages is investigated by using field test results. Voltage peak-to-peak ripple, δV_{dc}, peak-to-peak mean dc link voltage ripple, ΔV_{dc}, of dc link capacitor voltage and effective switching frequency,

Table 2.8 Transformer MV side voltage harmonics at rated reactive power

Harmonic Number	Capacitive Mode			Inductive Mode		
	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)
1	100	100	100	100	100	100
3	0.3	0.2	0.2	0.3	0.1	0.2
5	0.2	0.1	0.1	0.4	0.3	0.5
7	0.1	0.1	0.2	0.1	0.1	0.1
11	0.1	0.1	0.2	0.1	0.1	0.1
13	0.1	0.1	0.1	0.1	0.1	0.1
17	2.0	2.0	2.1	1.7	1.7	1.7
19	2.3	2.2	2.2	2.0	1.9	1.9
21	0.1	0.1	0.1	0.1	0.1	0.1

Table 2.9 Transformer MV side current harmonics at rated reactive power

Harmonic Number	Capacitive Mode			Inductive Mode		
	I_a(%)	I_b(%)	I_c(%)	I_a(%)	I_b(%)	I_c(%)
1	100	100	100	100	100	100
3	1.2	1.2	1.2	2.0	2.0	2.0
5	0.5	0.5	0.5	0.4	0.4	0.4
7	0.6	0.6	0.6	0.2	0.2	0.2
11	0.3	0.3	0.3	0.1	0.1	0.1
13	0.2	0.2	0.2	0.1	0.1	0.1
17	0.8	0.8	0.8	0.5	0.5	0.5
19	0.9	0.9	0.9	0.2	0.2	0.2
21	0.1	0.1	0.1	0.1	0.1	0.1

$f_{sw(eff)}$ (number of turn-ons in one second per switch) are of concern.

Figure 2.16 and Figure 2.17 show the variations in instantaneous values of dc link capacitor voltage against time for MSS method (sampling rate=1-MHz) for full inductive and full capacitive modes of operation, respectively. The variation in mean dc voltage ($V_{dc,mean}$) is also marked on the same waveform (20ms averaged data). The results of CSS and MSS method with different Δt_s are summarized in Table 2.10. MSS algorithm reduces considerably both the instantaneous dc link voltage ripple and mean dc link voltage ripple at the expense of higher switching losses for power

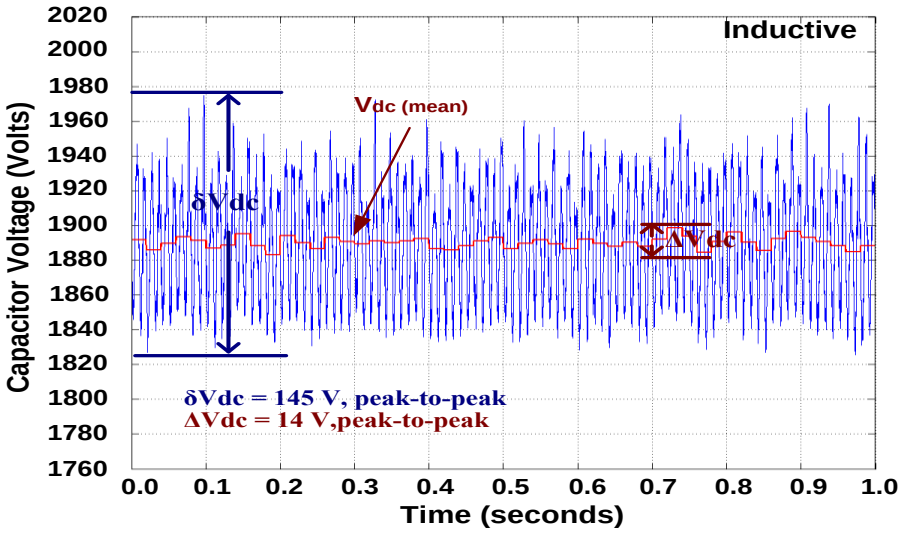


Figure 2.16 Variations in the dc link voltage of an HB under MSS method with Δt_s=400µs during full inductive mode

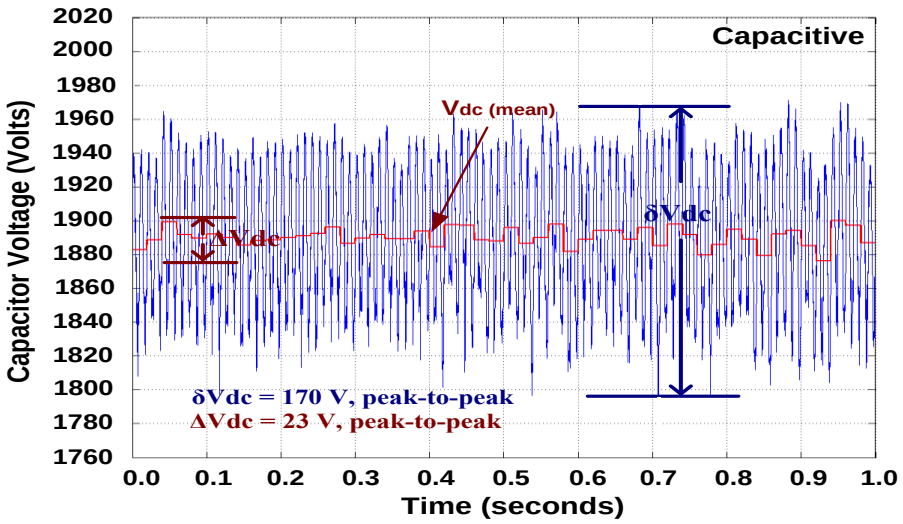


Figure 2.17 Variations in the dc link voltage of an HB under MSS method with Δt_s=400µs during full capacitive mode

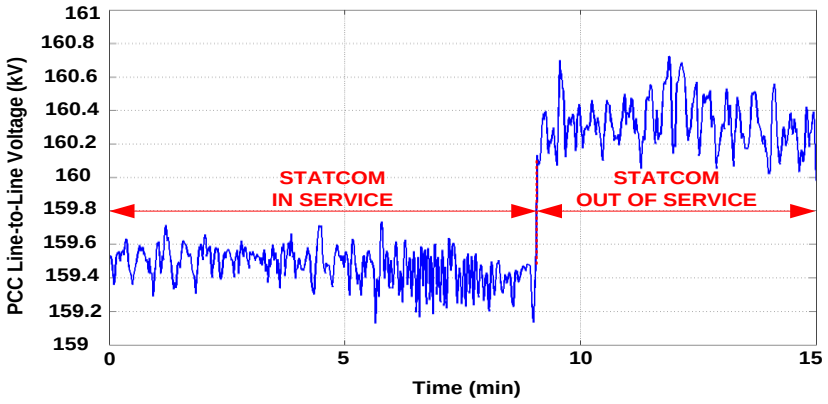
semiconductors. It is not beneficial to reduce swapping period, Δt_s, considerably, i.e. below 400µs according to field test results given in Table 2.10. These results show that the modified selective swapping algorithm and its digital implementation balance the dc link capacitor voltages perfectly.

2.3.5 Terminal Voltage Regulation Mode (V-mode)

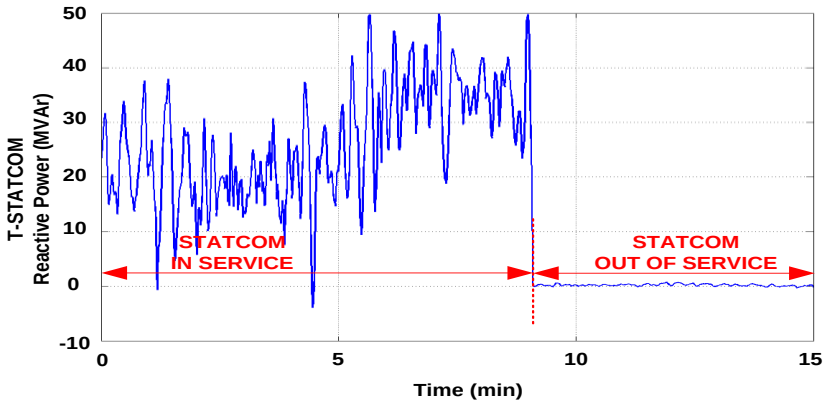
The 154-kV bus-bar to which the T-STATCOM is connected is a strong bus (5300 $MVA_{,SC}$). Therefore, the effect of T-STATCOM on bus-bar voltage in V-mode does not exceed ±1% depending upon the power demand of the loads supplied from the same bus. The performance of the T-STATCOM in V-mode is illustrated in Figure 2.18. These waveforms are constructed from 20ms averaged data. Line-to-line rms voltage at PCC in Figure 2.18-a when T- STATCOM is in service is not a pure level voltage variation (0.5-kV peak-to-peak max). These fluctuations are attributed to the facts that 1) Analog to digital converter introduces an error of ±0.5%, and 2) Sometimes the installed capacity of the T-STATCOM becomes insufficient to keep the terminal voltage precisely constant at the set value (159.5-kV) as can be understood from Figure 2.18-a and Figure 2.18-b. Figure 2.18-c shows that reactive power at PCC is fluctuating since it is not controlled in V-mode.

Table 2.10 Performance of selective swapping algorithms

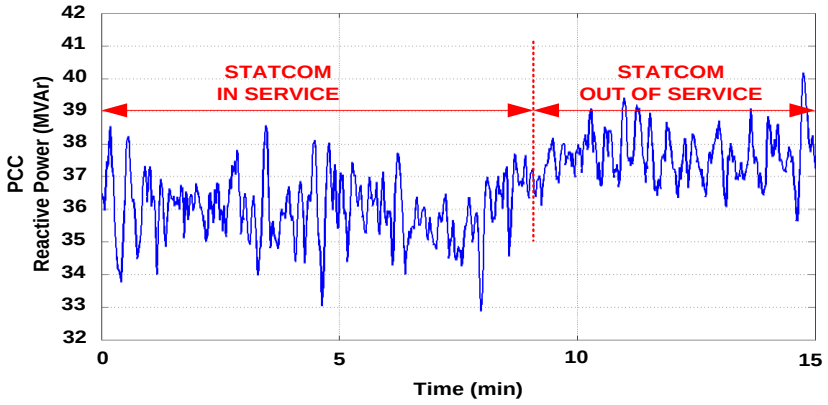
Applied Method	Full inductive			Full capacitive		
	CSS	MSS with 400µs	MSS with 200µs	CSS	MSS with 400µs	MSS with 200µs
Instantaneous Voltage Ripple (peak-to-peak)	190V	145V	130V	205V	170V	190V
Mean Voltage Ripple (peak-to-peak)	30V	14V	16V	50V	23V	27V
Effective Switching Frequency	250Hz	500Hz	650Hz	200Hz	500Hz	700Hz



(a)



(b)

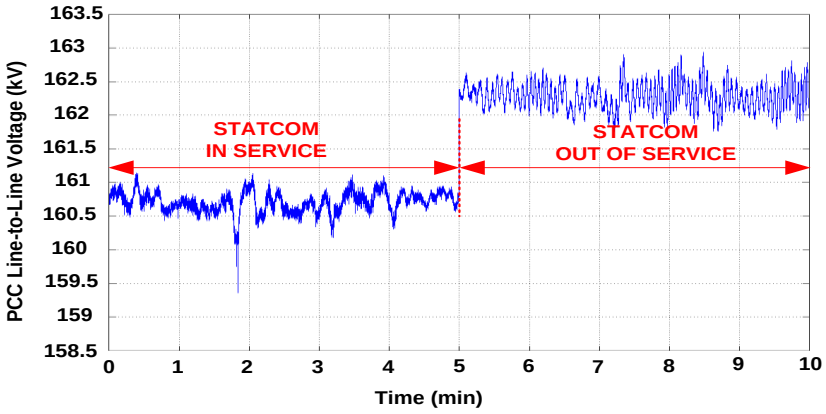


(c)

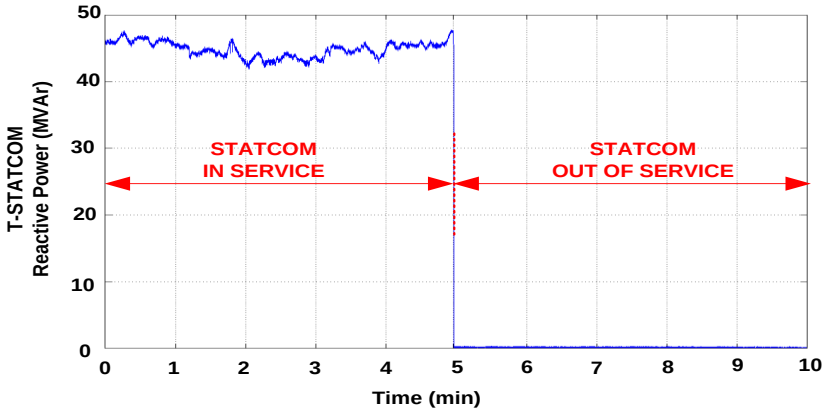
Figure 2.18 The performance of T-STATCOM in V-mode (Field data)

2.3.6 Reactive Power Compensation Mode (Q-mode)

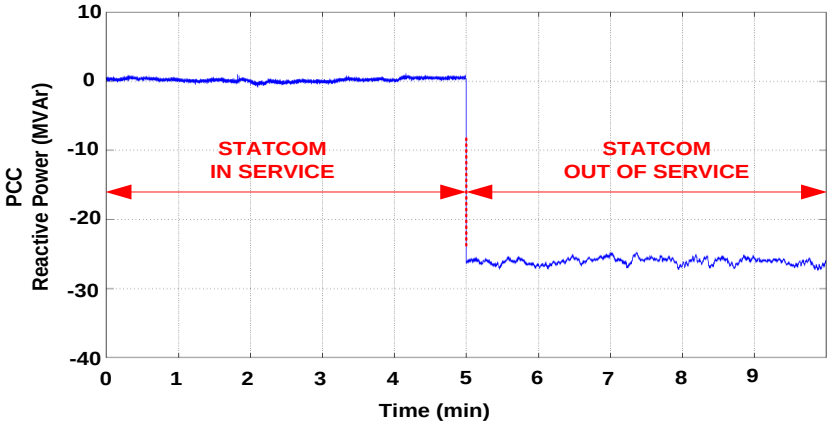
The records in Figure 2.19 (20ms averaged data) show the performance of the T-STATCOM in Q-mode. In the first 5-minute part of the record, the T-STATCOM brings the power factor to unity as viewed from the 154-kV side of the



(a)



(b)



(c)

Figure 2.19 The performance of T-STATCOM in Q-mode (Field data)

autotransformers (Figure 2.19-c). For this purpose, T-STATCOM produces nearly 45-MVAr inductive (Figure 2.19-b). When T-STATCOM is operated in standby mode (Figure 2.19-b) to produce 0-MVAr, nearly 27-MVAr capacitive reactive power starts to flow to PCC via the autotransformers (Figure 2.19-c). This reactive power flow is not equal to the 45-MVAr inductive reactive power previously generated by T-STATCOM. This is attributed to the fact that the bus voltage at PCC increases nearly 2-kV (Figure 2.19-a), owing to the non-linear characteristics of power plants and loads connected to the same bus when T-STATCOM is operating in standby mode.

2.3.7 Transient Performance

The reactive power variations on the 154-kV side and 10.5-kV side of the coupling transformer are given when Q_{set} of T-STATCOM is varied from +50-MVAR (inductive) to -50-MVAr (capacitive) in Figure 2.20 and Figure 2.21, respectively.

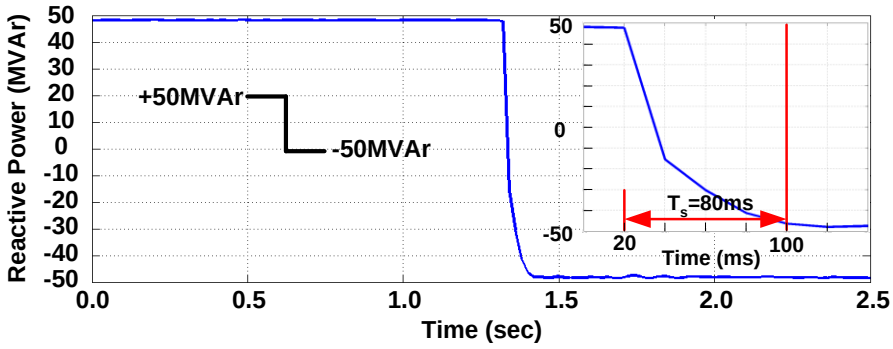


Figure 2.20 Transition from full inductive to full capacitive, 154-kV side

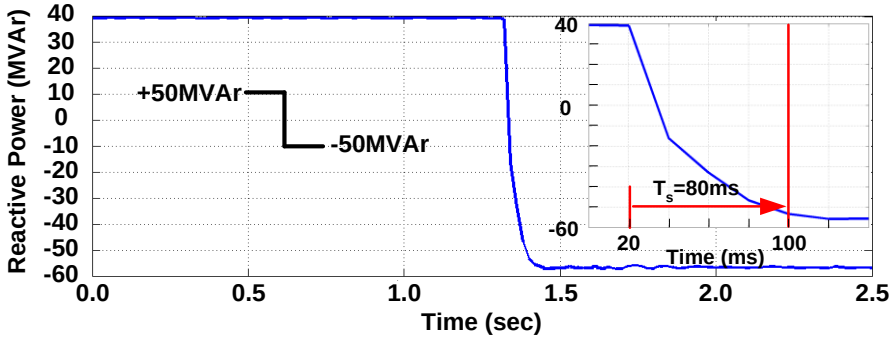


Figure 2.21 Transition from full inductive to full capacitive, 10.5-kV side

There is a 10-MVAr (inductive) difference between the reactive power values of 154-kV and 10.5-kV sides. This is the reactive power consumption of the coupling transformer. As can be seen from the waveforms in Figure 2.20 and Figure 2.21, the settling time of the closed loop control system is only 80ms. On the other hand, when Q_{set} is varied from -50-MVAr (capacitive) to +50-MVAr (inductive), the response of the closed loop control system will be as in Figure 2.22 and Figure 2.23. For this case, the settling time is measured to be 100ms. It is worth to note that if the T-STATCOM were operated in open loop control mode, the settling time would not exceed 45ms.

The line-to-neutral voltage waveform and the associated line current waveform on the 10.5-kV side of the coupling transformer during transition from Q_{set} = +50-MVAr to -50-MVAr with the closed loop control system are given in Figure 2.24. The associated waveforms from Q_{set}=-50-MVAr to +50-MVAR are shown in Figure 2.25. The responses in Figure 2.24 and Figure 2.25 show the smooth and fast

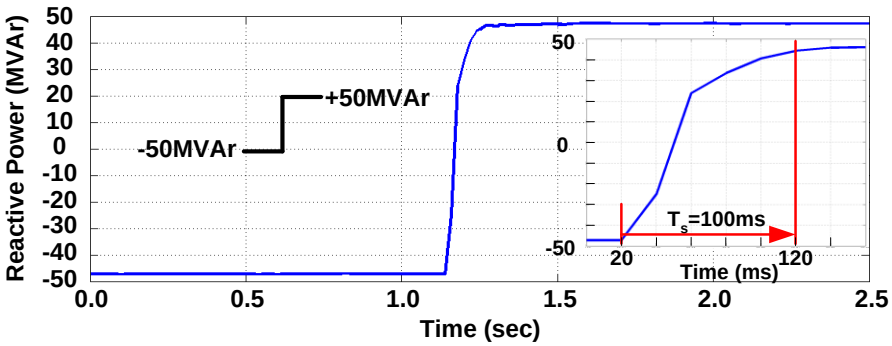


Figure 2.22 Transition from full capacitive to full inductive, 154-kV side

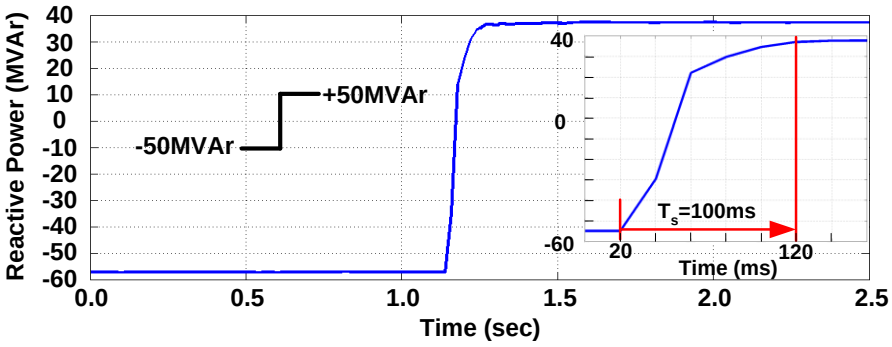


Figure 2.23 Transition from full capacitive to full inductive, 10.5-kV side

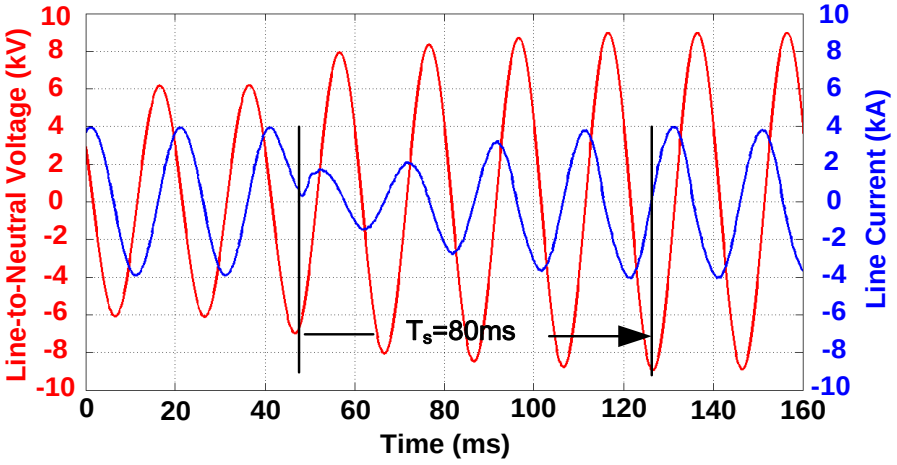


Figure 2.24 Variations in line-to-ground voltage and current during the transition from full inductive to full capacitive, 10.5-kV side

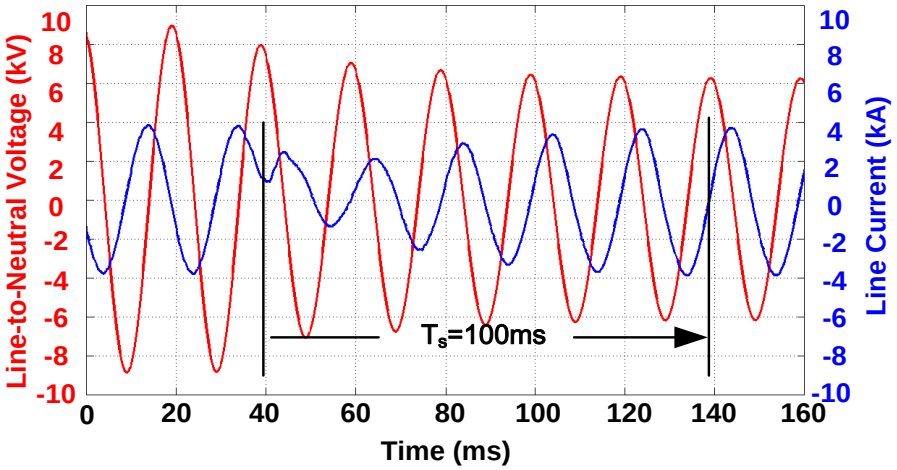


Figure 2.25 Variations in line-to-ground voltage and current during the transition from full capacitive to full inductive, 10.5-kV side

response of the control system against changes in Q_{set} from full inductive to full capacitive, or vice versa.

CHAPTER 3

TRANSFORMER CORE SATURATION PROBLEM

3.1 DEFINITION, CAUSES AND COUNTERMEASURES

3.1.1 Definition

Transformer core saturation problem can be defined as an asymmetrical core saturation whose asymmetry worsens in time. High dc and low order current harmonics with growing magnitudes flow in the lines of the transformer secondary and low order current harmonics flow in the primary. These may be harmful for system components.

A T-STATCOM system may be connected to the MV side of a dedicated coupling transformer, or secondary or tertiary winding of an existing power transformer as shown in Figure 1.5. Since the existing power transformer is transferring huge amounts of active power, it is not common to have core saturation problem in such applications because of high electrical damping and operating voltage levels lower than or near the rated transformer voltage. Only the very high dc and second harmonic current components in the inrush current waveform of a large power transformer during its energization might be the cause of transformer core saturation [24].

3.1.2 Causes

The possible causes of core saturation problem for a CMC based T-STATCOM system having a dedicated separate coupling transformer are listed as follows:

- Imbalance in the gating signals of the converter power semiconductors,
- Presence of second harmonic voltage on the transformer primary,
- Transformer inrush currents generated by neighboring large power transformers,
- Supply side imbalance in line impedances,
- Imbalance of supply voltage,
- Geomagnetically-induced currents (GIC) [36].

GIC is known to create dc currents in the magnetizing branch of transformers in the grid for decades, and some countermeasures are given in the literature.

3.1.3 Countermeasures

Coupling transformer core saturation problem should be eliminated by applying one of the following countermeasures:

- A significantly over-designed transformer having a rated flux density around 1.2T peak may be used. This approach cannot guarantee the elimination of the problem and results in an unnecessarily bulky and hence costly coupling transformer.
- The use of second harmonic filter bank on the supply side of the coupling transformer and/or 50-Hz filters in the dc links of the CMC HBs. It is also a bulky and expensive solution.
- Preventing core saturation by electronic control such as modifying gate signal patterns. This is an effective and cheapest solution for the elimination of core saturation problem.

3.2 MECHANISM OF TRANSFORMER CORE SATURATION

3.2.1 No Perturbation (Normal Operation)

The mechanism of transformer core saturation is as illustrated in Figure 3.1. Coupling transformer and CMC/s are the two nonlinear components of the T-STATCOM system. It is meant by the normal operation of the T-STATCOM system that magnetic operating point of the transformer is on the linear portion of the *B-H* characteristic, CMC/s perform/s balanced operation without dc current injection, and the grid voltage is a purely sinusoidal wave at power frequency (50-Hz). If both harmonic components in the supply voltage and odd harmonic components in the magnetizing current have very small magnitudes, then the operation mode is classified as normal operation by neglecting them. Cross modulation phenomenon across ac-ac-dc link of the T-STATCOM performing normal operation is as shown in Figure 3.1-a. 50-Hz grid voltage produces 100-Hz voltage and current components in addition to the dc voltage and current in the dc links of CMC HBs. These are reflected back to grid side in the form of 50-Hz current component.

3.2.2 Even Harmonics as the Origin of Perturbation

Figure 3.1-b illustrates the effects of dominant even harmonic voltage components, such as 100-Hz in the grid voltage waveform, on the cross modulation phenomenon. For this case, 50-Hz voltage and current components will be produced in the dc links of CMC HBs, in addition to normally obtained dc and 100-Hz components. 50-Hz in dc link will be reflected to the transformer secondary in the form of a dc and a 100-Hz current component. 100-Hz current on the transformer secondary may increase the 100-Hz voltage component of the grid voltage and dc current component on the secondary may cause asymmetric saturation of transformer core.

Dc offset in the magnetization characteristic magnifies the magnitudes of even harmonic voltage components, which results in a positive feedback effect if the overall system has not sufficient electrical damping. In summary, the presence of

second harmonic voltage component in supply lines causes flow of dc component in the lines of transformer secondary, thus producing an asymmetrical magnetizing current waveform in the transformer core, and hence transformer core saturation may occur as will be discussed in Section 3.3

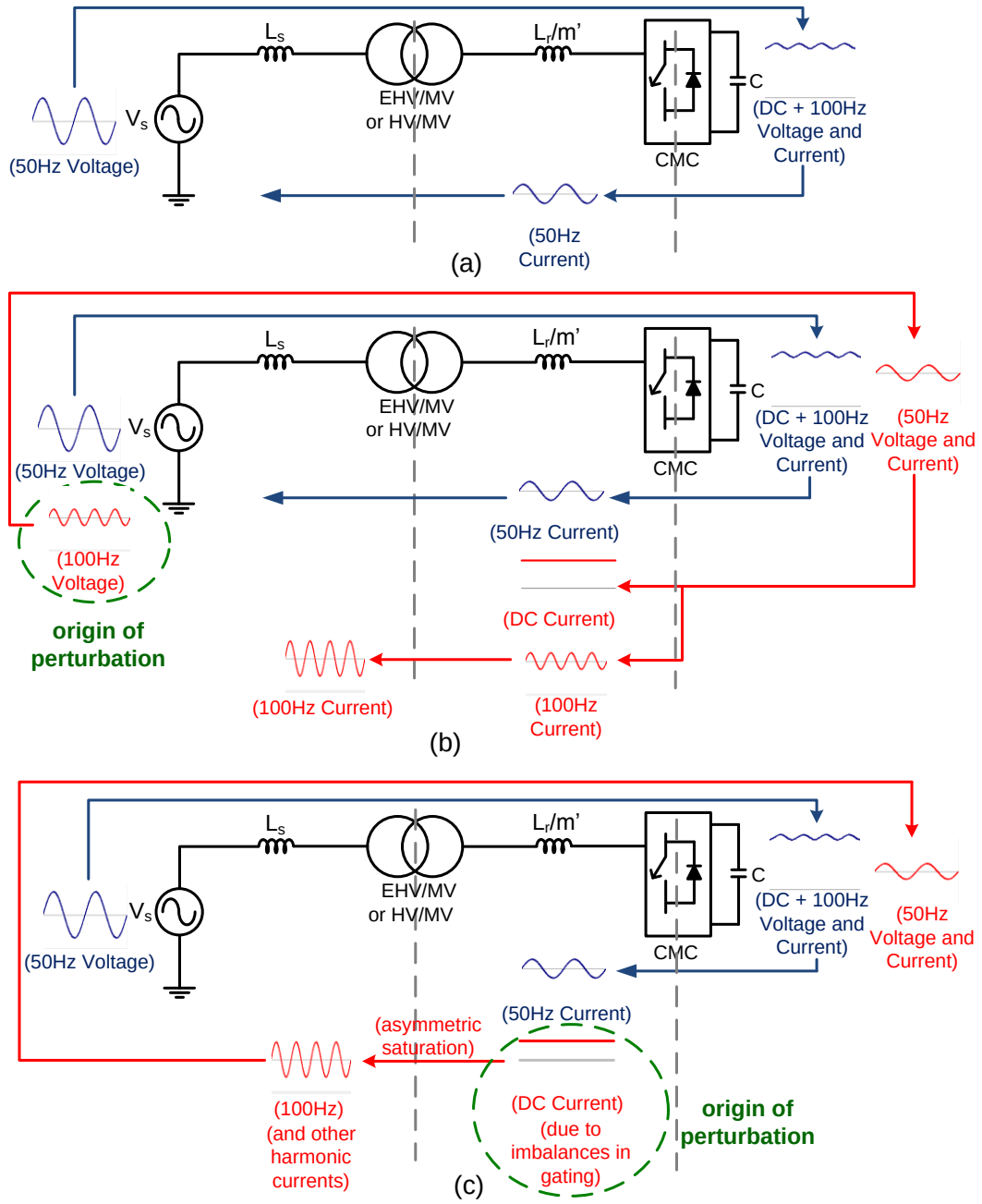


Figure 3.1 Cross modulation phenomenon across ac-ac-dc link of a CMC based T-STATCOM a) Normal operation b) Presence of even harmonics in the supply voltage c) Dc current injected by CMC/s

3.2.3 Dc Current as the Origin of Perturbation

Figure 3.1-c illustrates the effects of dc current injected by the CMC/s owing to imbalances in their gating signals, on cross modulation phenomenon. Dc currents in the lines of transformer secondary cause generation of 100-Hz and other even and odd harmonic current components in the lines of transformer primary owing to the asymmetric saturation of the transformer core. These harmonics will appear as voltage harmonics on the primary side impedances.

In summary, dc current injected by the CMC to the secondary of the coupling transformer leads to an asymmetrical magnetizing current, and hence generation of second harmonic voltage and current components as will be discussed in Section 3.3 This may result in transformer core saturation problem.

3.3 INTERACTION BETWEEN HARMONICS AND NONLINEAR B-H CHARACTERISTIC OF COUPLING TRANSFORMER CORE

Effects of dc and harmonic components in Figure 3.1-b and -c on the operation of the coupling transformer core are examined by considering the *B-H* characteristic of a high-quality transformer core material (C130-30 / ThyssenKrupp [51]). The *B-H* characteristics of this core material is given in the Appendix. This core material is used in order to see the general trend of the saturation, it does not correspond to the real material of the T-STATCOM system's coupling transformer. Core type and core shape of the transformer are not considered.

The *B-H* data that will be given in the next subsections and tables are all created from the polynomial approximated mathematical model of this core material characteristics. The magnetic field intensity (*H*) values given in the tables are assumed to be directly related and proportional to the magnetizing current magnitudes.

3.3.1 Normal Operation Case

In the case of normal operation of the T-STATCOM on the linear portion of *B-H* characteristic of the transformer core, magnetizing current contains only the fundamental component as illustrated by Case 1 in Table 3.1. The choice of operating peak flux density (B_{1p}) in the saturated portion of the *B-H* characteristic causes generation of odd harmonic components as expected (Case 3 in Table 3.1). Further increase of B_{1p} yields higher magnitude odd harmonic components in magnetic field intensity (H_{np}), where n is the harmonic number.

3.3.2 Dc Component in Magnetizing Flux Density

The effects of dc component in magnetizing flux density on the harmonic content of magnetic field intensity waveform, and hence magnetizing current waveform are exercised by assuming 0.1T dc bias, which results in asymmetrical flux density and hence magnetizing current waveforms. Corresponding results are given in Table 3.2 and the associated plots of *B(t)*, *H(t)* and virgin *B-H* characteristic in Figure 3.2 for Case 3 (B_0=0.1T and B_{1p}=1.6T). As can be seen from Table 3.2 and Figure 3.2, asymmetrical flux density waveform causes generation of dc and even order harmonics with significant magnitude in the magnetizing current waveform. Furthermore, it causes flow of higher fundamental and odd harmonic components in the magnetizing branch as compared to the base case (Case 3 in Table 3.1).

Table 3.1 Normal operation (magnetizing flux density has only the fundamental component)

Case No	B, T	H_{np}, % [40.2A/m ≡ 100%]									
	B_{1p}	H_{0p}	H_{1p}	H_{2p}	H_{3p}	H_{4p}	H_{5p}	H_{6p}	H_{7p}	H_{8p}	H_{9p}
1	1.20	0.0	53.2	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
2	1.40	0.0	64.8	0.0	2.5	0.0	2.0	0.0	1.5	0.0	1.0
3	1.60	0.0	100.0	0.0	22.8	0.0	13.4	0.0	5.1	0.0	0.4
4	1.80	0.0	430.5	0.0	296.1	0.0	213.0	0.0	133.1	0.0	74.1

Table 3.2 Magnetizing flux density is distorted by a dc component

Case No	B, T		H_{np}, % [40.2A/m ≡ 100%]									
	B_0	B_{1p}	H_{0p}	H_{1p}	H_{2p}	H_{3p}	H_{4p}	H_{5p}	H_{6p}	H_{7p}	H_{8p}	H_{9p}
1	0.10	1.20	4.4	53.2	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
2	0.10	1.40	7.6	68.4	5.8	5.2	4.4	3.5	2.5	1.7	0.9	0.4
3	0.10	1.60	24.8	122.4	36.4	41.4	25.7	27.0	14.8	14.5	7.8	7.2
4	0.10	1.80	309.6	763.1	559.4	572.3	430.7	401.7	278.1	235.6	148.2	113.5

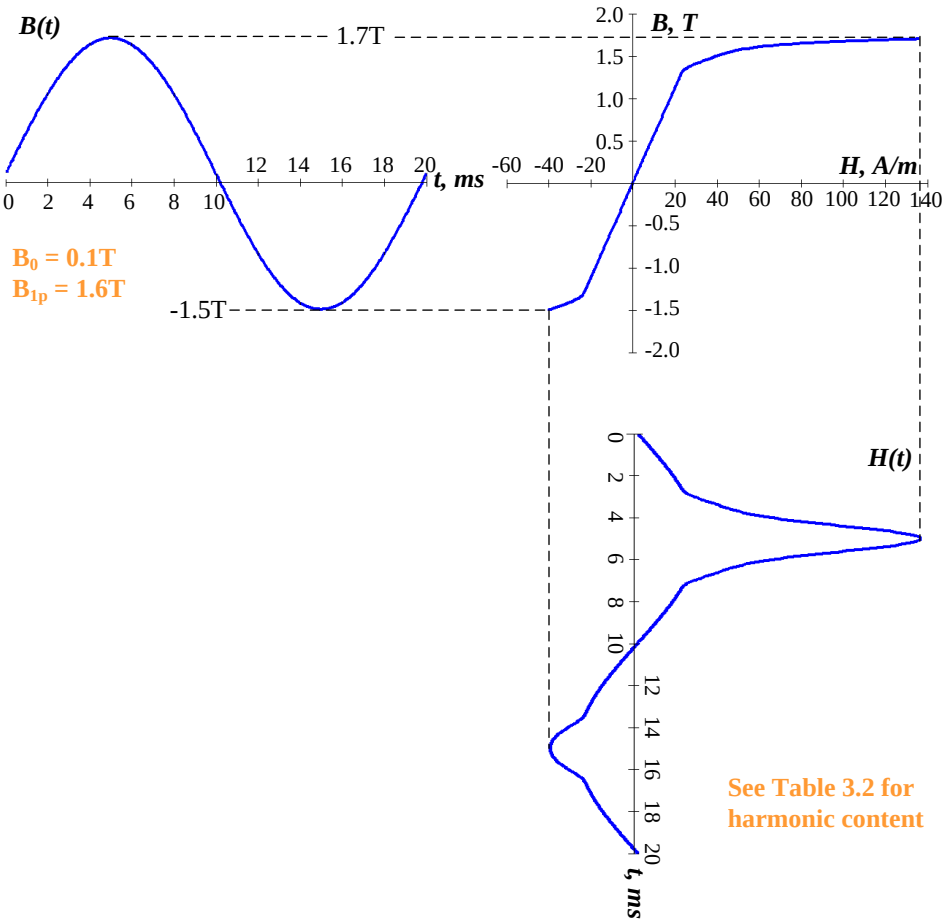


Figure 3.2 Graphical construction of *H(t)* waveform for Case 3 in Table 3.2

When the dc component of magnetic flux density is doubled whereas the fundamental component stays the same, the harmonic content of magnetic field

intensity is as given in Table 3.3. The associated plots of *B(t)*, *H(t)* and virgin *B-H* characteristic for Case 3 of Table 3.3 is shown in Figure 3.3 (B_0=0.2T and B_{1p}=1.6T).

Table 3.3 Magnetizing flux density is distorted by a larger dc component

Case No	B, T		H_{np}, % [40.2A/m ≡ 100%]									
	B_0	B_{1p}	H_{0p}	H_{1p}	H_{2p}	H_{3p}	H_{4p}	H_{5p}	H_{6p}	H_{7p}	H_{8p}	H_{9p}
1	0.20	1.20	9.6	54.7	1.4	1.3	1.2	1.0	0.9	0.7	0.6	0.4
2	0.20	1.40	16.9	77.6	14.0	11.7	9.0	6.3	3.9	1.9	0.6	0.1
3	0.20	1.60	103.3	257.8	171.5	154.6	129.1	107.0	82.1	63.6	45.5	33.3
4	0.20	1.80	996.0	2033.3	1788.6	1601.4	1324.8	1067.4	791.3	564.4	366.4	221.0

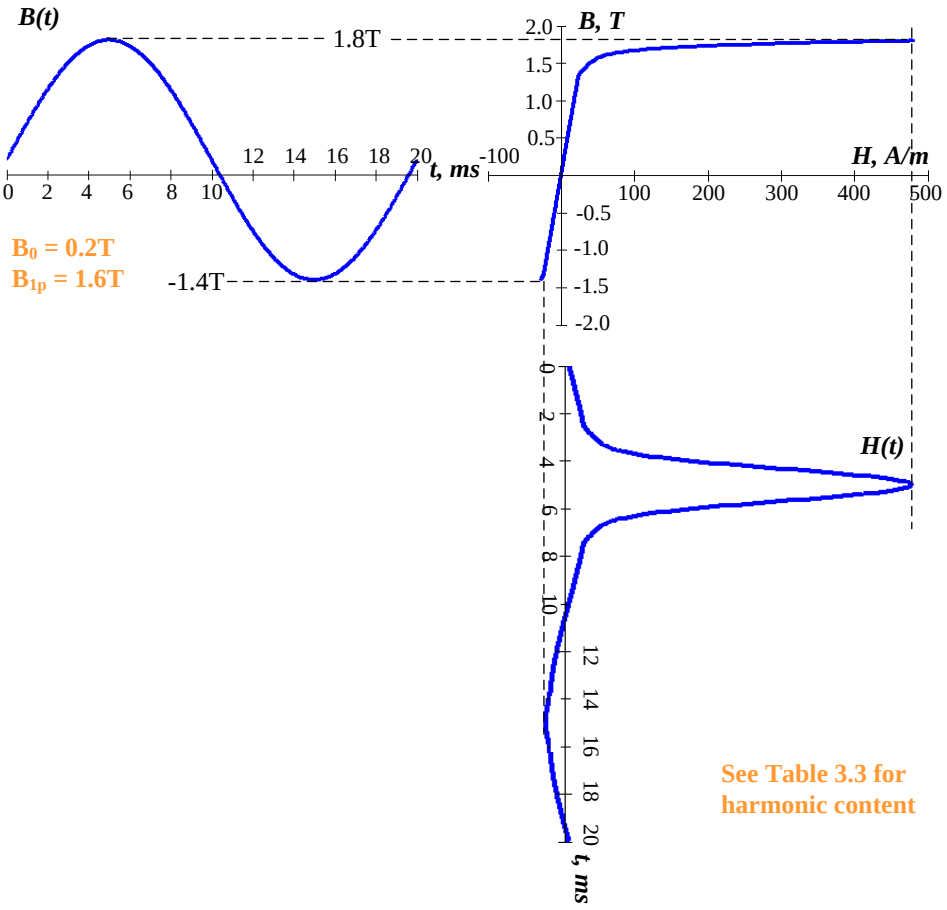


Figure 3.3 Graphical construction of *H(t)* waveform for Case 3 in Table 3.3

3.3.3 2nd Harmonic Component in Magnetizing Flux Density

B_{2p}=0.05T second harmonic is considered in the magnetizing flux density waveform in addition to B_{1p}. The worst case occurs when the positive peaks of the fundamental and second harmonic flux density components are coincident as given in Table 3.4. As can be understood from Table 3.4, presence of the second harmonic component in the worst case causes generation not only of all even and odd harmonics, but also a dc component in the magnetic field intensity waveform, and hence in the magnetizing current waveform. It is obvious that existence of the second harmonic voltage component corresponds to a grid voltage distorted by second harmonic component in magnetizing flux, since n^{th} harmonic component of induced emf across the magnetizing branch, E_n is directly proportional to the time maximum value of n^{th} harmonic magnetizing flux density, B_{np}, as given in (3.1).

$$E_n = 4.44NAf_nB_{np} \tag{3.1}$$

where, N is the number of series turns of the primary or secondary, A is the effective cross-sectional area of core leg, and f_n is the frequency of n^{th} harmonic component.

It can be concluded from the results given in Table 3.2, Table 3.3, and Table 3.4 that the presence of dc or second harmonic component in the magnetizing flux density wave leads to a magnetizing current waveform distorted by dc, and all odd and even harmonic components provided that magnetic operating point periodically moves into the highly-saturated region of the *B*-*H* characteristic.

Table 3.4 Magnetizing flux density is distorted by 2nd harmonic component

Case No	B, T		H_{np}, % [40.2A/m ≡ 100%]									
	B_{2p}	B_{1p}	H_{0p}	H_{1p}	H_{2p}	H_{3p}	H_{4p}	H_{5p}	H_{6p}	H_{7p}	H_{8p}	H_{9p}
1	0.05	1.20	0.0	53.2	2.2	0.0	0.0	0.0	0.0	0.0	0.0	0.0
2	0.05	1.40	1.4	65.6	5.0	3.1	2.2	2.5	1.6	1.7	0.9	0.9
3	0.05	1.60	6.7	103.9	14.3	26.3	8.9	16.4	5.4	7.4	3.0	2.0
4	0.05	1.80	119.4	497.7	225.4	355.0	182.0	258.0	129.0	162.7	78.5	90.2

Table 3.5 Magnetizing flux density is distorted by a larger 2nd harmonic component

Case No	B, T		H_{np}, % [40.2A/m ≡ 100%]									
	B_{2p}	B_{1p}	H_{0p}	H_{1p}	H_{2p}	H_{3p}	H_{4p}	H_{5p}	H_{6p}	H_{7p}	H_{8p}	H_{9p}
1	0.20	1.20	0.6	54.4	10.0	1.1	1.0	0.9	0.8	0.8	0.7	0.6
2	0.20	1.40	6.4	74.6	20.6	10.5	9.0	7.2	5.5	3.8	2.4	1.3
3	0.20	1.60	76.9	225.7	153.0	136.1	119.1	105.7	87.5	73.4	58.1	46.3
4	0.20	1.80	819.7	1727.1	1540.8	1431.6	1247.8	1077.9	880.0	698.1	528.9	381.4

When the 2nd harmonic component of magnetic flux density is quadrupled whereas the fundamental component stays the same, the harmonic content of magnetic field intensity is as given in Table 3.5.

3.3.4 Dc Component in Magnetic Field Intensity

Magnetic field intensity waveform (and hence the associated magnetizing current) in the magnetizing branch is assumed to be composed only of a fundamental component H_{1p} and a fixed dc component of H_0=4A/m. The results in Table 3.6 are obtained for different values of H_{1p}. H_{1p} of Case 3 (H_0=4A/m and H_{1p}=40A/m) corresponds to percentage H_{1p} value of Case 3 in Table 3.1. As can be seen from Table 3.6, flux density waveform in the magnetizing branch still contains all odd and even harmonics superimposed on a dc component. In this analysis, all even and odd harmonics in H are ignored. When the dc component of magnetic field intensity is quadrupled, the harmonic content of magnetic flux density is as given in Table 3.7.

Table 3.6 Magnetic field intensity is distorted by a dc component

Case No	H, A/m		B_{np}, % [1.6T ≡ 100%]									
	H_0	H_{1p}	B_{0p}	B_{1p}	B_{2p}	B_{3p}	B_{4p}	B_{5p}	B_{6p}	B_{7p}	B_{8p}	B_{9p}
1	4.0	21.4	13.3	69.8	0.4	0.1	0.2	0.4	0.4	0.4	0.2	0.0
2	4.0	26.0	11.8	83.0	2.3	1.2	2.0	0.7	0.8	0.2	0.2	0.4
3	4.0	40.0	7.2	106.0	6.8	11.9	0.5	1.0	1.7	1.4	0.9	0.1
4	4.0	175.0	1.6	133.7	2.9	39.2	2.5	20.3	2.2	12.2	1.8	7.7

Table 3.7 Magnetic field intensity is distorted by a larger dc component

Case No	H, A/m		B_{np}, % [1.6T ≡ 100%]									
	H_0	H_{1p}	B_{0p}	B_{1p}	B_{2p}	B_{3p}	B_{4p}	B_{5p}	B_{6p}	B_{7p}	B_{8p}	B_{9p}
1	16.0	21.4	45.9	58.5	7.8	3.9	0.6	1.1	0.9	0.1	0.5	0.2
2	16.0	26.0	42.4	67.4	11.1	4.7	0.0	0.2	0.7	0.5	0.7	0.0
3	16.0	40.0	30.0	93.5	22.0	5.9	1.6	2.8	0.0	1.3	0.3	0.4
4	16.0	175.0	6.5	133.2	11.4	37.7	9.9	18.3	8.2	9.9	6.6	5.3

3.3.5 A More Realistic Case for Magnetic Field Intensity

For better approximation to the actual case, the same *B-H* characteristic is used, and fundamental component and all odd harmonics of Case 3 in Table 3.1 are superimposed on the dc component of H_0=4A/m.

Dc and all harmonic components of the corresponding flux density waveform are given in Table 3.8. The associated plots of *B(t)*, *H(t)* and virgin *B-H* characteristic are as given in Figure 3.4.

Table 3.8 Practical case (Magnetic field intensity is distorted by dc and all odd harmonics)

		Applied Harmonics of H(t) Waveform									
		H_0	H_{1p}	H_{3p}	H_{5p}	H_{7p}	H_{9p}	H_{11p}	H_{13p}	H_{15p}	H_{17p}
H_{np}	A/m	4.0	40.2	9.17	5.40	2.04	0.15	0.27	0.05	0.35	0.31
	%	10.0	100.0	22.8	13.4	5.1	0.4	0.7	0.1	0.9	0.8
		Calculated Harmonics of B(t) Waveform									
		B_{0p}	B_{1p}	B_{2p}	B_{3p}	B_{4p}	B_{5p}	B_{6p}	B_{7p}	B_{8p}	B_{9p}
B_{np}	T	0.145	1.550	0.105	0.050	0.053	0.013	0.004	0.009	0.025	0.019
	%	9.4	100.0	6.8	3.2	3.4	0.8	0.3	0.6	1.6	1.2

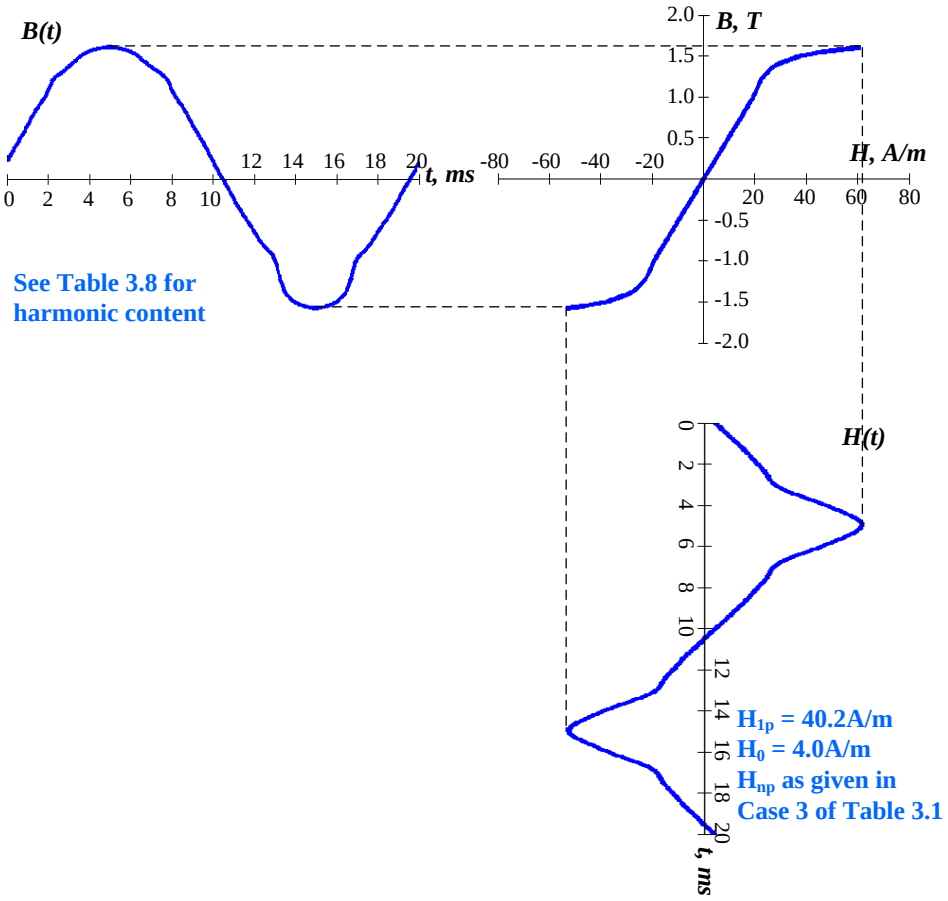


Figure 3.4 Graphical construction of *B(t)* waveform for Table 3.8

In conclusion, dc current component in the lines of transformer secondary and hence in the magnetizing current waveform causes distortion of magnetizing flux density by a dc component and all even and odd harmonics. These harmonics in the flux density wave will appear as voltage harmonics on the primary side of the coupling transformer except the dc component, because the magnetizing branch provides a short-circuit return path to the dc current component in the transformer secondary lines. Operation at low values of B_0 and very low values of B_{1p} is an exception.

3.4 FIELD OBSERVATIONS FOR THE SAMPLE T-STATCOM SYSTEM REGARDING TRANSFORMER CORE SATURATION

In the capacitive operating region of the T-STATCOM, CMC ac voltage and hence transformer secondary voltage will increase significantly above their rated values as given in Figure 3.5, which means that operating value of the fundamental flux

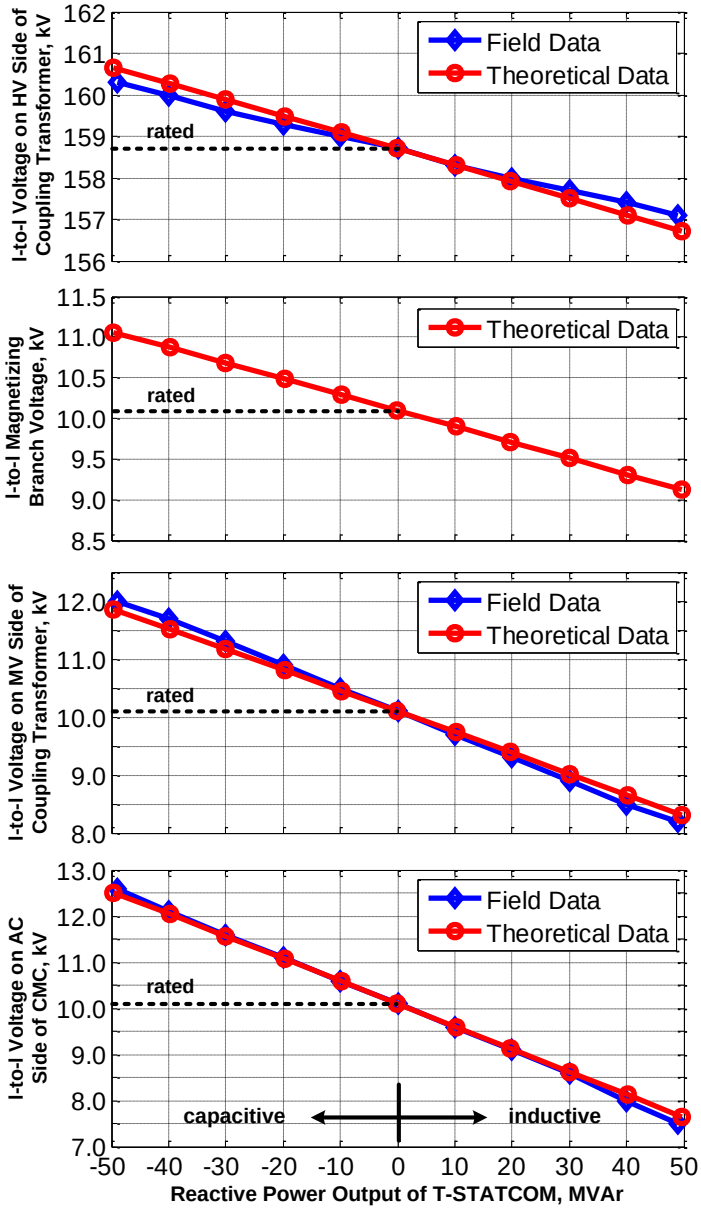


Figure 3.5 Variations in fundamental voltage components at different points of the T-STATCOM system against reactive power

density component in the transformer core is higher than the rated value. However in the inductive operating region, the coupling transformer secondary voltage and fundamental flux density component are lower than their rated values, and hence transformer core saturation problem is never observed in the field. The values in Figure 3.5 are found using the simplified single line model of the T-STATCOM system given in Figure 3.6. In the analysis and calculations of Figure 3.5, the magnetizing branch is neglected (R_c and L_m are ignored), and transformer primary and secondary resistances & reactances are assumed to be equal. This model perfectly represents the total T-STATCOM system since it takes into account all the system parameters at fundamental frequency. For the results given in Figure 3.5, *m'* value given in Figure 3.6 is taken as five, meaning that the T-STATCOM reactive power rating is ±50-MVAr.

3.4.1 Inductive Mode of Operation

Transformer core saturation problem owing to presence of second harmonic voltage component in the supply lines and/or dc current component in the lines of the transformer secondary is not observed during the operation of T-STATCOM system in inductive mode in the field. In order to illustrate it, a sample record is given in Figure 3.7. During this record, T-STATCOM absorbs 45-MVAr inductive from the supply, which corresponds to nearly 38-MVAr inductive reactive power flow on the secondary side of the coupling transformer (Figure 3.7 last record).

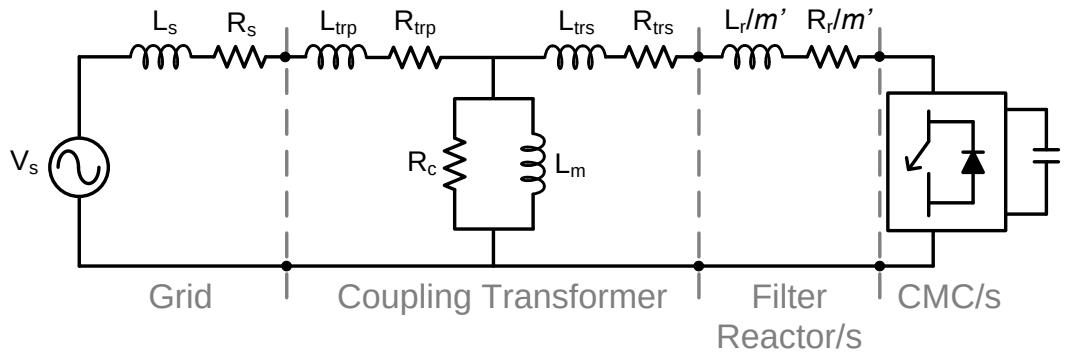


Figure 3.6 Simplified single line model of the T-STATCOM system

In Figure 3.7, the values shown are 10-cycle averaged rms quantities, there exists no dc current elimination control, the dc current is injected in two steps. During this record reactive power absorbed by T-STATCOM and CMC fundamental current are +45-MVAr and 495A, respectively.

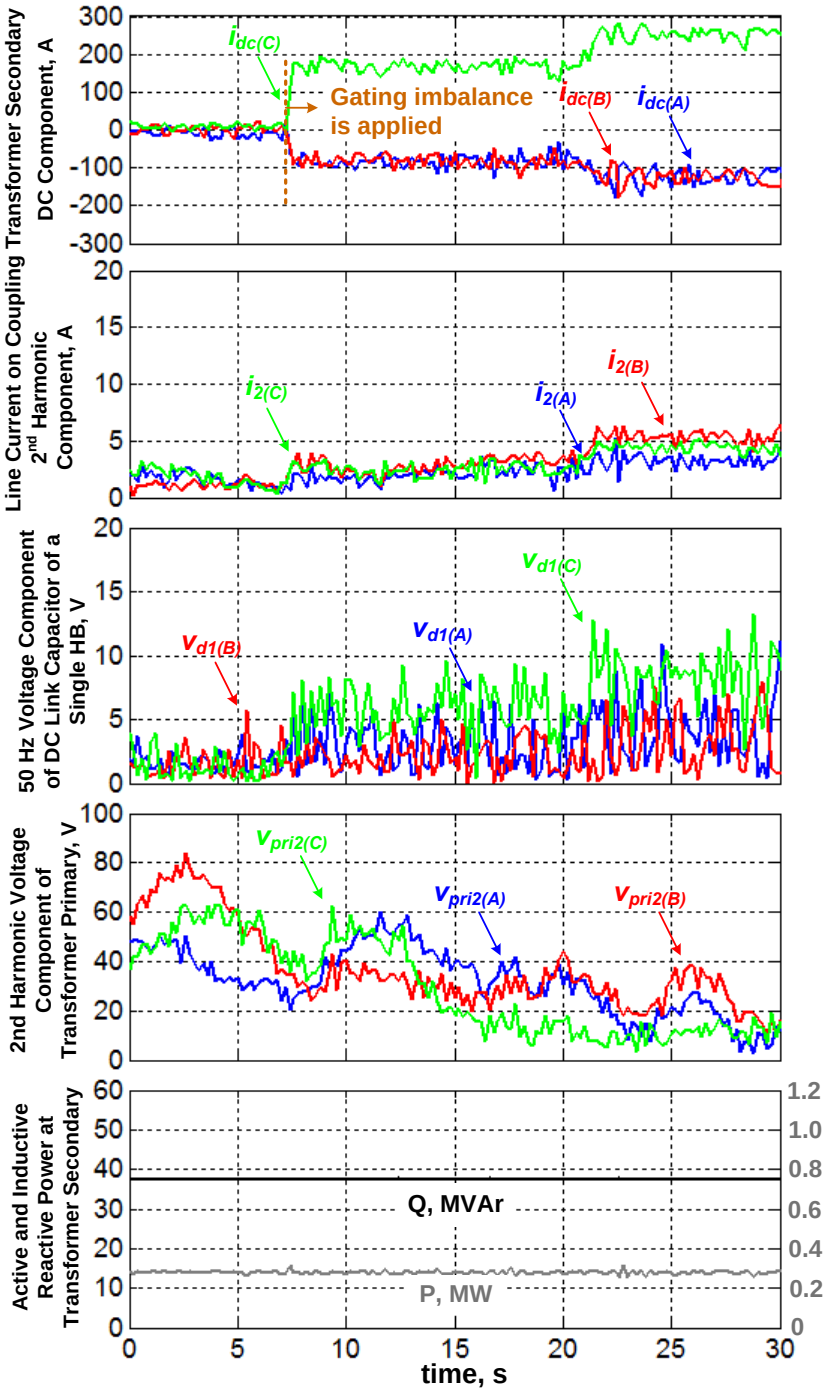


Figure 3.7 Field record illustrating the fact that dc current injected by CMCs cannot trigger transformer core saturation in inductive mode

In order to be able to detect whether transformer core saturation occurs or not, the digital gating circuit for phase-C of the CMCs is reprogrammed to inject dc current components to the transformer secondary which are increased in steps as a result of gating imbalance (Figure 3.7 first record). Since T-STATCOM is operating at nearly full inductive load, CMC ac voltage, transformer secondary voltage, magnetizing voltage (and hence time-maximum value of magnetizing flux density), and transformer primary voltage are nearly at their minimum values (Figure 3.5).

As can be seen from Figure 3.7, neither second harmonic voltage nor injected dc current grows up for the operating condition defined above.

It is worth to note that regardless of the operation mode (capacitive or inductive) of the T-STATCOM, the coupling transformer and series filter reactors consume reactive power, e.g., the reactive power consumption of coupling transformer in the above test (Figure 3.7) is nearly 7-MVAr. It means that the CMCs should generate reactive power higher than the desired MVAr output of the T-STATCOM in capacitive mode, while in inductive mode, less by the reactive power consumptions of the coupling transformer and filter reactors.

3.4.2 Capacitive Mode of Operation

Since the transformer secondary voltage and magnetizing flux density are higher than their rated values (Figure 3.5), capacitive operating region of T-STATCOM is the most critical operating region from the viewpoint of transformer core saturation problem. The transformer rated primary and secondary voltages with the tap adjusted to 23 of 25 are 154kV and 10kV, respectively. The capacitive operating region given in Figure 3.5 shows that the transformer secondary voltage is higher than the rated value of 10-kV. The transformer excitation current data given in Appendix also verifies that the core is saturated when the rated voltage is exceeded because it is seen from Appendix that the rms value of the magnetizing currents (4.948A on 3-phase average) for 10% percent higher voltage (12.22-kV) are 2.5 times larger than

the magnetizing currents (1.934A on 3-phase average) for rated voltage (11.09-kV) applied to the secondary of the transformer.

A perturbation such as second harmonic component in the grid voltage and/or a dc current injected by CMC/s may trigger transformer core saturation because the conversion loop of 100-Hz → 50-Hz → dc+100-Hz → 100-Hz in Figure 3.1-b and -c strengthens dc bias in the transformer core, and hence the magnetic operating point may be moved gradually into heavily saturated region either in the first or third quadrant of the *B*-*H* plane. Field observations on the sample T-STATCOM system have shown that initiation of transformer core saturation depends on how many of the five CMCs are active (m') and total capacitive VAr generated by the T-STATCOM, e.g., if capacitive Q exceeds 31.5-MVAr, transformer core saturation occurs when all CMCs are active (m'=5). The reasoning behind this fact will be explained in Subsection 3.4.3.

Variations in various voltage and current components recorded in the field during transformer core saturation process on the sample T-STATCOM system given in Figure 3.8 verify the core saturation phenomenon presented in this thesis. During this record, the method proposed in this work which eliminates transformer core saturation is disabled. As described in [50], when the setting of any digital protection relay is exceeded, protection system first blocks all gating pulses and then sends a signal to PLC to open the associated circuit-breaker/s, if necessary. In this figure, the values shown are 10-cycle averaged rms quantities; there exists no dc current elimination control; total dc current of five CMCs is 740A at tripping instant; the reactive power delivered by T-STATCOM and CMC fundamental current are -45-MVAr and 495A, respectively.

Although the CMC output voltage waveforms do not contain dc components due to any firing imbalance, the core saturation instability is triggered. This is attributed to the existence of 2nd harmonic voltage at PCC, and the rms voltage at the transformer secondary being higher than the rated value. This implies that mechanism (b) in

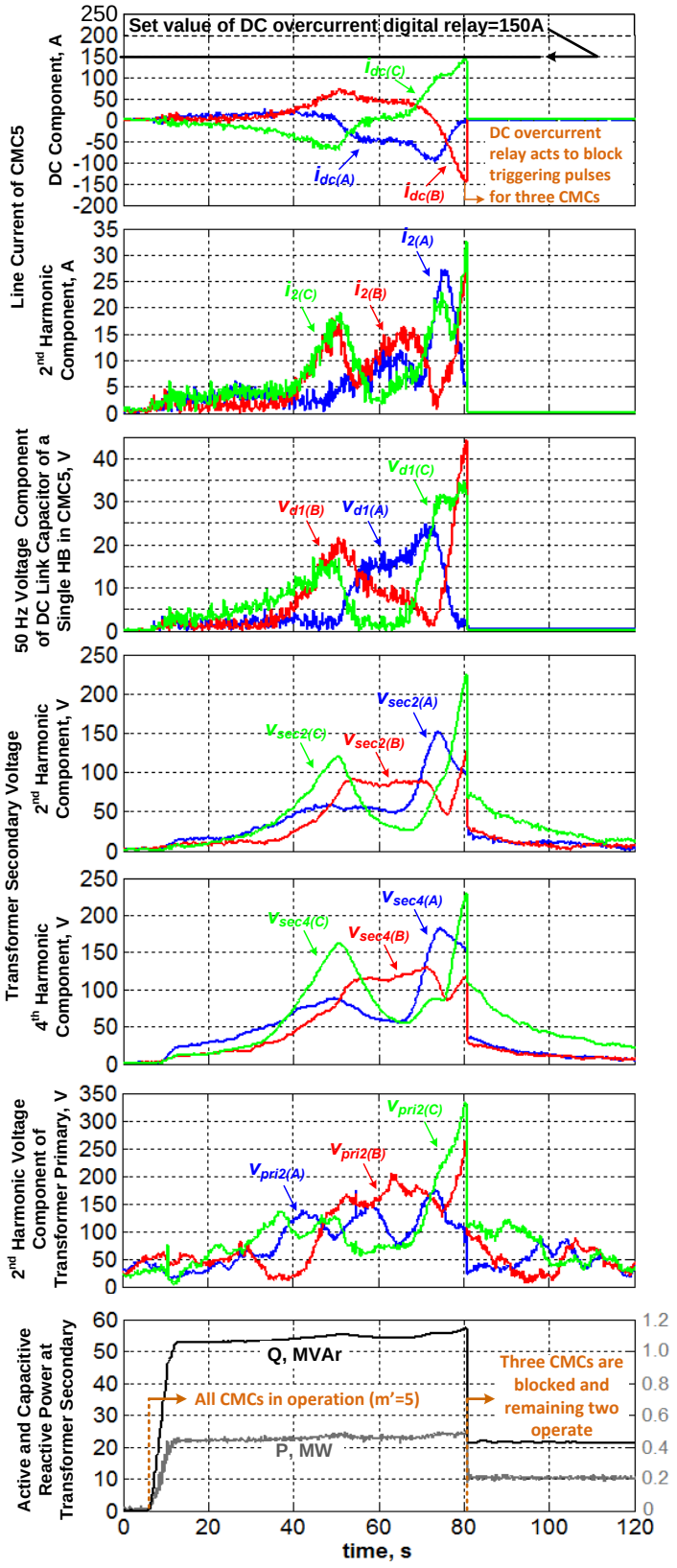


Figure 3.8 Line-to-neutral voltage and line current harmonics recorded at different points of the T-STATCOM during core saturation in capacitive mode

Figure 3.1 is valid. In other words, with STATCOM being out of service, the PCC voltage is at rated value so that the transformer is not saturated, but PCC voltage includes 2nd harmonic component although its value is very low.

In the field test in Figure 3.8, trip level of each dc overcurrent digital relay was set to 150A in order to prevent IGBTs from overcurrents. At t=5s, a transition occurs from inductive operation to highly capacitive operation, and then nearly in 10s time, transformer core saturation process is initiated.

It is observed in the field during the process in Figure 3.8 that dc, 100-Hz and all even and odd harmonic current components on the secondary side of the transformer, 50-Hz and odd harmonic voltage components on the dc links of CMC HBs, and 100-Hz and all harmonic voltage components on the primary side of the transformer grow slowly in magnitude. Dc current component in phase-C of CMC3, 4, and 5 (only that of CMC5 is shown in the first record of Figure 3.8) tends to exceed 150A in nearly 75s time, resulting in trip of only three CMCs. The remaining two CMCs continue to operate in capacitive region.

3.4.3 Initiation of Core Saturation Process for Different Numbers of Parallel CMCs in Operation (m')

The initiation of transformer core saturation process for the T-STATCOM system should be related to the transformer secondary fundamental voltage magnitude (and hence magnetizing branch fundamental voltage magnitude), or magnitude of injected dc or harmonic current components, if any. Field tests have shown that the point where the transformer core saturation process starts is not directly related to the transformer secondary fundamental voltage magnitude. It is observed that the capacitive reactive power measured at the transformer primary and transformer secondary fundamental voltage magnitude for different number of parallel CMCs in operation at the instant where the core saturation first starts are as given in Table 3.9.

Table 3.9 Reactive power and transformer secondary voltage for core saturation initiation with different m'

m'	Q (MVAr)	Vsec (kV)
1	Not observed	
2	-18	10.7
3	-23	10.9
4	-27	11.1
5	-31.5	11.2

The reasoning behind the reactive power values given in Table 3.9 are explained using Figure 3.9. First of all the fundamental current magnitude flowing from the source (I) can be directly found using the reactive power values and assuming that 1) V_s does not change with respect to the current drawn, 2) X_s is negligibly small. Then, current into every CMC can be found directly by dividing into m' branches equally.

The current flowing into every CMC is known to be responsible for the voltage ripple across the CMC HB dc links. Therefore a voltage harmonic, possibly an even order, is reflected from the dc link to the ac terminals of CMC. This harmonic voltage is supposed to be responsible for the core saturation initiation. Since *Vs* is composed of fundamental voltage only, during the analysis of the harmonic voltage division it is considered to be short-circuited. If the harmonic voltage magnitude on the transformer magnetizing branch, V_{mh} can be shown to be the same for different m', then the reasoning behind the values in Table 3.9 will be proven.

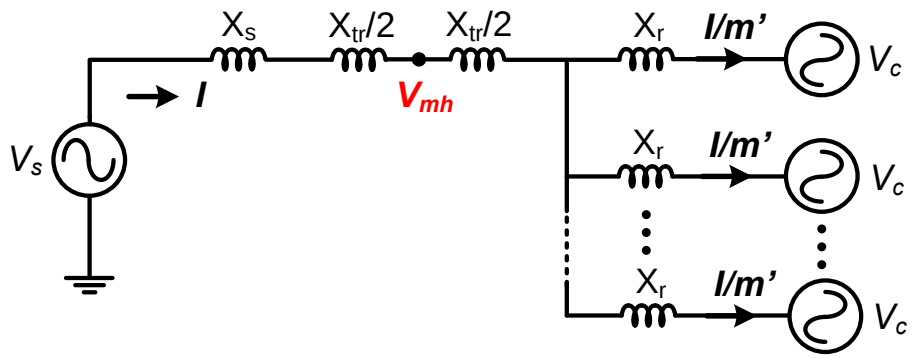


Figure 3.9 T-STATCOM system simplified single line diagram for core saturation initiation analysis

Since the short-circuit MVA value at 154-kV bus is 5300-MVA, X_s reflected to the transformer secondary can be found as follows:

$$X_s = \frac{(10.1kV)^2}{5300MVA} = 0.019\Omega$$

where

$$X_{tr}/2 = \frac{(10.1kV)^2}{50MVA} x 0.17/2 = 0.173\Omega$$

and

$$X_r = (1.6mH)(2\pi 50) = 0.503\Omega$$

therefore, X_s can be neglected. On the other hand, the change in V_s for reactive power change between -18-MVAr and -31.5-MVAr is seen to be negligible from Figure 3.5. Hence, the current can be taken as directly proportional to reactive power.

m'=2:

Let the current drawn from the source (I_2) be *I*. Then, each CMC current will be *I/2*. This current is assumed to create a harmonic voltage of magnitude $V_{ch}/2$ at the ac terminals of CMC. Since there are two sources with same magnitude ($V_{ch}/2$), and an equal coupling inductor of L_r=1.6mH in series with them, the Thevenin equivalent will be a single source with the same magnitude in series with an inductor of $L_r/2$=0.8mH. Hence, the harmonic voltage drop among the magnetizing branch can be found as follows:

$$V_{mh} = \left(\frac{\frac{X_{tr}}{2}}{X_{tr}+\frac{X_r}{2}}\right)\left(\frac{V_{ch}}{2}\right) = 0.145V_{ch} \qquad (3.2)$$

m'=3:

Similar to the case above, the current drawn from the source (I_3) will be in proportion with the change in reactive power, i.e.:

$I_3 = I_2\left(\frac{23}{18}\right)$ and each CMC current will be third of this, therefore the harmonic voltage at the ac terminals of CMC will be $\left(\frac{23}{18}\right)\left(\frac{V_{ch}}{3}\right)$. Hence, the harmonic voltage drop among the magnetizing branch can be found as follows:

$$V_{mh} = \left(\frac{\frac{X_{tr}}{2}}{X_{tr}+\frac{X_r}{3}}\right)\left(\frac{23}{18}\right)\left(\frac{V_{ch}}{3}\right) = 0.143V_{ch} \qquad (3.3)$$

m′=4:

Similar to *m′*=3 case, this time the harmonic voltage at the ac terminals of CMC will be $\left(\frac{27}{18}\right)\left(\frac{V_{ch}}{4}\right)$. Hence, the harmonic voltage drop among the magnetizing branch can be found as follows:

$$V_{mh} = \left(\frac{\frac{X_{tr}}{2}}{X_{tr}+\frac{X_r}{4}}\right)\left(\frac{27}{18}\right)\left(\frac{V_{ch}}{4}\right) = 0.138V_{ch} \quad (3.4)$$

m′=5:

Similar to *m′*=3 case, this time the harmonic voltage at the ac terminals of CMC will be $\left(\frac{31.5}{18}\right)\left(\frac{V_{ch}}{5}\right)$. Hence, the harmonic voltage drop among the magnetizing branch can be found as follows:

$$V_{mh} = \left(\frac{\frac{X_{tr}}{2}}{X_{tr}+\frac{X_r}{5}}\right)\left(\frac{31.5}{18}\right)\left(\frac{V_{ch}}{5}\right) = 0.136V_{ch} \quad (3.5)$$

As seen from equations (3.2)−(3.5), the harmonic voltage drop among the magnetizing branch is nearly the same. This concludes the proof of reasoning behind the values given in Table 3.9.

CHAPTER 4

ELIMINATION OF TRANSFORMER CORE SATURATION

4.1 PROPOSED DC CURRENT ELIMINATION METHOD

In the proposed method, dc current component in the line current waveforms of the transformer secondary is eliminated by modulating one or more than one step voltage in the CMC staircase voltage waveforms. This is achieved electronically via the digital control system of the sample T-STATCOM. Details of multi-DSP and -FPGA-based fully digital control system for CMC based T-STATCOM are given in [50]. Figure 4.1 shows the block diagram representation of the digital control system. In this figure, the newly added dc current elimination controller is shown by yellow-colored block.

As seen in Figure 4.1, the dc current elimination controller mainly consists of two PI controllers implemented for phase-A and phase-B for every CMC. These controllers output an angle which is used to narrow or widen the HB output voltage waveform's either half-cycle in order to create a dc voltage which can be used to oppose the dc current flowing in the CMC lines. By this means, the dc currents are brought to setting value (in our case this setting value is zero). There is no PI controller on phase-C because the current passing through phase-C is a dependent value, i.e., it is the negative of summation of currents passing through phase-A and phase-B, since

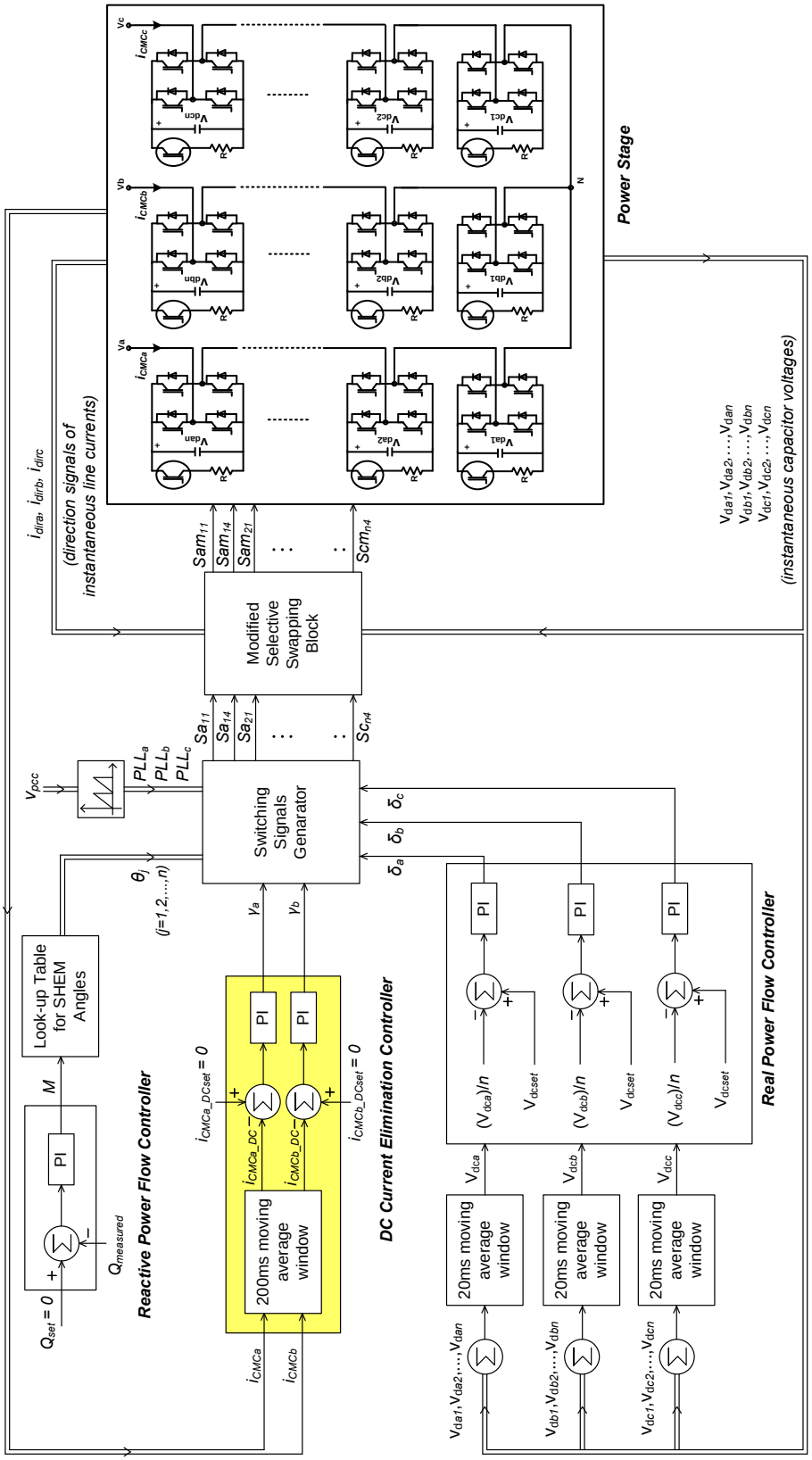


Figure 4.1 Integration of dc current elimination controller to the fully digital control system described in [50]

the neutral is isolated from ground, so that the total current in three phases cannot be different than zero.

One of the objectives in this research work is to use a single dc current elimination controller for each CMC for simplicity and reliability in the implementation. This approach needs only the division of variable γ (to find the widening and/or narrowing angle of each HB, named $\Delta\theta$) by an integer such as 2, 4, 10, and 20 for the sample T-STATCOM system before the application of control signal to one or more than one HB evenly in each CMC. γ is defined as the total widening or narrowing which is directly proportional to the dc voltage produced. Uneven application method requires more than one dc current elimination controller, usually one for each HB, which results in an unnecessary complexity in the control software.

The other controllers seen in Figure 4.1 are also designed and implemented by the author, but since they are not in scope of this thesis work, they are not discussed in detail here.

Each CMC may inject a dc current component owing to internal (gating imbalance) or external (second harmonic voltage component at the coupling transformer primary) causes. According to power sink convention, positive dc current component is flowing from the transformer secondary to the CMC, and negative dc current is flowing in the opposite direction. The control system in Figure 4.1 brings this current to zero by the use of two PI controllers, one in phase-A, the other in phase-B, since the sum of dc currents in phase-A, -B, and -C is zero.

4.1.1 Application of the Proposed Method to Only One HB or to All HBs

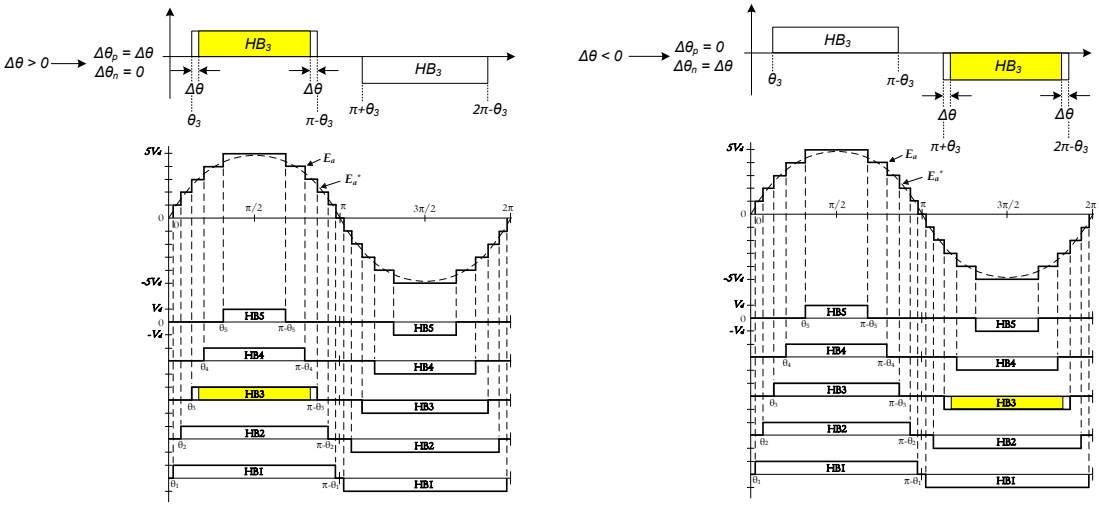
In order to bring a negative dc current component in transformer secondary lines rapidly to zero either of the following two methods can be applied:

Method-1) The area under the positive half-cycle of the CMC line-to-neutral voltage waveform should be reduced as illustrated in Figure 4.2a.

Method-2) Both of the areas under the positive and negative half-cycles can be controlled simultaneously, i.e., the area under the negative half-cycle can be increased while reducing the area under the positive half-cycle by an equal amount, as illustrated in Figure 4.3-a.

Elimination of positive dc current component needs the application of one of the methods described above (method-1 or -2) in the opposite manner, as shown in Figure 4.2-b and Figure 4.3-b, respectively.

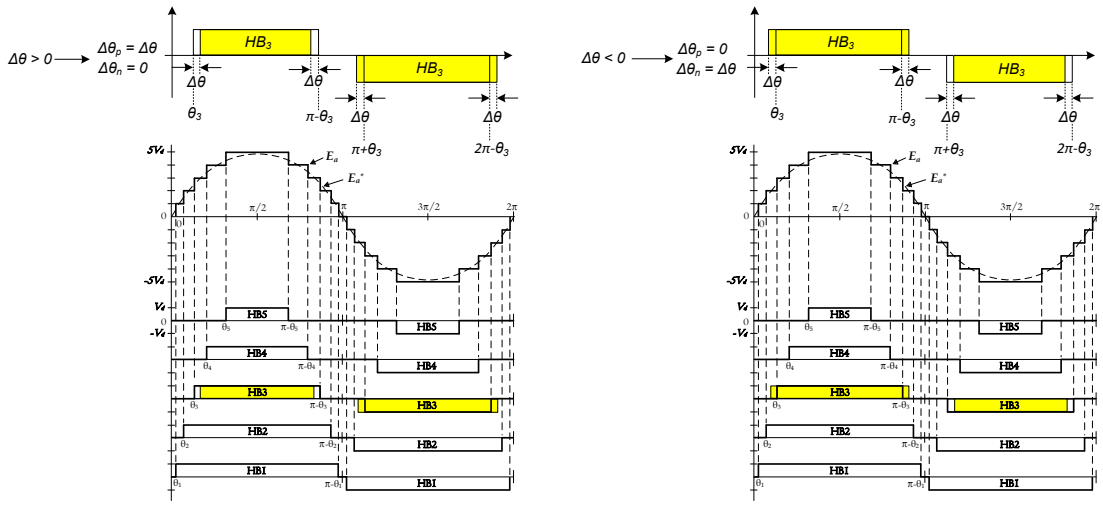
The effective (total) change in pulse width over a full cycle of the CMC line-to-neutral voltage waveform obtained by narrowing and/or widening HBs' voltage pulses will be denoted by angle γ. On the other hand, method-1 and -2 can be applied to either a) only one HB (Figure 4.2 and Figure 4.3), or b) more than one or every HB simultaneously. Each half-cycle of any HB output voltage is narrowed or widened symmetrically by angle $\Delta\theta$.



(a) Dc current component injected by CMC flows from coupling transformer to CMC

b) Dc current component injected by CMC flows from CMC to coupling transformer

Figure 4.2 Application of method-1a to HB3 of 21-level CMC-based T-STATCOM system



(a) Dc current component injected by CMC flows from coupling transformer to CMC

b) Dc current component injected by CMC flows from CMC to coupling transformer

Figure 4.3 Application of method-2a to HB3 of 21-level CMC-based T-STATCOM system

4.1.2 Selection of the HB to Which the Proposed Method will be Applied

In Figure 4.2, pulse width control is assumed to be applied to either positive or negative half-cycle of output voltage of only one HB (HB3 among five HBs). Since narrowing or widening the pulse width of the associated voltage pulse is applied symmetrically according to the philosophy of SHEM, $\Delta\theta = \gamma/2$ in Figure 4.2. However in Figure 4.3, one half-cycle is narrowed, while the next half-cycle of the HB output voltage is widened. This control strategy needs a pulse width adjustment of $\Delta\theta = \gamma/4$. On the other hand, the pulse width control method illustrated in Figure 4.2 or the one in Figure 4.3 can be applied simultaneously to all HBs of the CMC, which yield $\Delta\theta = \gamma/(2n)$ for the method in Figure 4.2 and $\Delta\theta = \gamma/(4n)$ for the method in Figure 4.3, where n is the number of HBs in each phase of the CMC. Asymmetrical narrowing or widening control is not recommended, because this approach increases the distortion of the CMC line-to-neutral voltage, and THD of CMC line-to-line voltage waveforms significantly.

The four pulse width control techniques (method-1 a and b, method-2 a and b) for dc current elimination as described above are compared in view of digital control range,

precision of $\Delta\theta$ control, distortion of line-to-neutral voltage waveforms, and THD of CMC line-to-line output voltage.

Gating instants of IGBTs in five HBs are determined according to SHEM and denoted by $\theta_1, \theta_2,..., \theta_5$ in Figure 4.2 and Figure 4.3. Differences between gating angles of all five HBs are calculated as a function of modulation index, M over the entire operating range of the T-STATCOM system from full inductive to full capacitive, and are given in Table 4.1. It is noted that the variation range of M in transient state, e.g., rapid changes in reactive power produced by each CMC, activation of the dc current elimination controller, unbalances in supply voltage, occurrence of single line-to-ground faults, etc., is wider than that of the steady state operation. Although the digital control system of the sample T-STATCOM is equipped with a 24-MHz clock, FPGA board of each CMC module updates gating pulses of IGBTs at a rate of 1-MHz. It corresponds to a time step of 1-μs and hence 0.018° precision in adjusting gating angles. The hard limiter circuit in the dc current elimination controller is designed to limit the control range between $+\gamma_{max}$ and $-\gamma_{max}$. γ_{max} is dictated by the maximum permissible value of $\Delta\theta$, $\Delta\theta_{max}$ for each method in order not to ruin the shape of the 11-level line-to-neutral voltage waveform. These are marked as blue colored boxes in Table 4.1, and associated γ_{max} and $\Delta\theta_{max}$ values are listed in Table 4.2. It is worth to note that $\Delta\theta_{max}$ values may be different in narrowing and widening of any HB output voltage pulse, e.g., for HB3, $\Delta\theta_{max}$ is 6.70° in narrowing, whereas it is 4.98° in widening control.

As can be understood from the results given in Table 4.2, method-1 gives a high precision in $\Delta\theta$ control. Among method-1a and method-1b, method-1a is the most precise one. On the other hand, method-2b gives the highest control range, γ_{max}. Since the amount of dc current that can be injected by each CMC is directly proportional to γ_{max}, method-2b is the best one from the view point of dc current injection/absorption capability. However the field experience has shown that such a high control range is never needed for a carefully designed T-STATCOM system.

Table 4.1 Differences between SHEM angles of sample T-STATCOM system over the entire operating range in transient state

Differences Between SHEM Angles, °	Modulation Index, M						
	2.50	**2.90**	**3.25**	**3.69**	**3.74**	**4.00**	**4.23**
$\theta_2 - \theta_1$	9.97	16.06	12.40	13.52	7.69	12.37	2.42
$\theta_3 - \theta_2$	11.71	4.98[2]	16.55	20.80	15.24	8.24	12.60
$\theta_4 - \theta_3$	12.00	13.22	21.43	6.70[1]	22.00	17.95	11.45
$\theta_5 - \theta_4$	15.72	9.77	29.90	40.34	1.75[3]	17.10	21.73

Table 4.2 Comparison of four pulse width control techniques in view of control range and precision of Δθ control

Method	$\Delta\theta_{max}$ per HB, °	γ_{max}, °	Precision of Δθ control	
			Actual, °	Percent of $\Delta\theta_{max}$, %
Method-1a	6.70[1]	13.40	0.018	0.27
Method-1b	4.98[2]	19.92*	0.018	0.36
Method-2a	1.75[3]	17.50[#]	0.018	1.03
Method-2b	1.75[3]	35.00[†]	0.018	1.03

* 19.92 = ($\Delta\theta_{max}$ per HB) x (number of half-cycles) x (2 due to symmetrical application to each half-cycle)= 4.98 x 2 x 2

[#] 17.50 = ($\Delta\theta_{max}$ per HB) x (n) x (2 due to symmetrical application to each half-cycle)= 1.75 x 5 x 2

† 35.00 = ($\Delta\theta_{max}$ per HB) x (n) x (number of half-cycles) x (2 due to symmetrical application to each half-cycle) = 1.75 x 5 x 2 x 2

[1, 2, 3]: See Table 4.1

The effects of four possible pulse width control methods described above on the distortion of line-to-neutral and THD of line-to-line voltages of CMC are calculated by using Matlab, and then given in Table 4.3 over the steady state operating range. From full inductive to full capacitive operation, modulation index, *M* of any CMC is

varying from 3.00 to 4.20 at rated busbar voltage in the steady state. THD values of line-to-line CMC voltage in Table 4.3 show that all pulse width control techniques have minor effect on THD (not more than 10% increase in the worst case for method-1 a, in full inductive operation mode) in comparison with THD value of the reference case (ideal operation, no dc current component in line current waveforms). Also for harmonic content of line-to-neutral CMC voltage waveforms, similar conclusions can be drawn. Field experience has shown that the dc current elimination controller varies γ in the range between -1.0° and +1.0° for vast majority of T-STATCOM operation time. It means that wider variation ranges for γ occur rarely for short time periods. In view of these harmonic results and field observations, all methods are equally applicable to sample T-STATCOM system.

In the sample T-STATCOM system, method-1a (narrowing either positive or negative half-cycle pulses of HB3 in phase-A and -B of each CMC by $\Delta\theta_{max}$=6.7°) is preferred in the implementation by taking into consideration its best precision figure of 0.27%, over the other methods. The precision has a crucial importance in the digital implementation, because a poor precision in the adjustment of $\Delta\theta$ may cause a dc current ripple in the lines of every CMC. This phenomenon can be improved further by updating the gating pulses of IGBTs at a higher rate than 1-MHz. The field performance of the chosen method will be given later.

4.2 SIMULATION RESULTS

The T-STATCOM system, including the power system components, power electronic equipment and control functions are modeled in a computer aided power system simulation tool, namely EMTDC PSCAD v4.4. Due to some limitations in number of signals and nodes, only one CMC is implemented in the simulations.

The reactive power control, active power control and MSS method mentioned earlier are all implemented into the simulation by using either default blocks or user created Fortran codes.

Table 4.3 Effects of four possible dc current elimination methods on harmonic components of line-to-neutral voltage and THD of line-to-line voltage of CMC

Change in pulse width/s		Method Applied to	Modulation Index	Harmonic Components of CMC L-to-N Voltage, V																	THD of L-to-L CMC Voltage
γ , °	Δθ , °																				
Total	Per HB		M	Dc	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	...	(%)
0.0	0.0	-	3.00	1	5130	0	1815	1	1	0	0	0	90	0	0	0	0	1	233		7.2
			4.20	1	7181	1	348	0	0	0	3	0	205	0	2	0	2	0	187		5.3
1.0	0.5	HB3	3.00	-5	5107	1	1828	6	7	5	1	5	83	7	3	1	6	7	234		7.3
			4.20	-5	7180	4	343	1	6	6	3	7	200	4	9	2	5	7	186		5.2
	+0.25 / -0.25	HB3	3.00	-5	5114	1	1825	6	1	5	1	5	76	7	0	2	0	7	240		7.3
			4.20	-5	7183	4	351	1	1	6	1	7	204	4	2	2	1	7	187		5.3
	0.1	All HBs	3.00	-5	5107	1	1827	3	2	1	1	1	75	0	0	1	2	2	240		7.3
			4.20	-5	7180	3	345	0	2	0	4	1	206	1	2	1	3	1	187		5.2
	+0.05 / -0.05	All HBs	3.00	-5	5114	1	1825	3	1	1	0	1	76	0	1	1	0	2	240		7.3
			4.20	-5	7183	3	351	0	1	0	1	1	204	1	2	1	1	1	187		5.3
6.0	3.0	HB3	3.00	-31	5097	12	1830	37	45	33	8	20	130	44	31	5	22	40	191		7.4
			4.20	-31	7164	28	307	8	36	39	5	42	172	15	46	23	24	44	199		5.1
	+1.5 / -1.5	HB3	3.00	-31	5114	10	1823	40	0	28	5	28	74	40	5	10	5	44	235		7.4
			4.20	-31	7182	30	350	3	2	35	3	44	200	25	3	10	5	39	195		5.2
	0.6	All HBs	3.00	-32	5097	9	1827	19	15	7	5	7	84	1	1	3	11	12	231		7.3
			4.20	-32	7162	21	322	2	12	2	17	7	212	7	2	4	13	10	188		5.1
	+0.3 / -0.3	All HBs	3.00	-32	5114	9	1825	19	1	7	0	6	75	1	1	4	0	11	239		7.3
			4.20	-32	7183	21	351	1	1	2	1	6	204	7	2	4	1	9	186		5.3
12.0	6.0	HB3	3.00	-63	5059	29	1840	70	89	75	32	21	156	86	74	35	15	59	153		7.9
			4.20	-63	7142	53	262	25	65	84	8	74	130	6	81	64	20	81	237		5.5
	+3.0 / -3.0	HB3	3.00	-63	5112	19	1817	80	2	55	17	55	71	77	22	19	18	81	219		7.7
			4.20	-63	7181	60	348	6	6	69	14	86	187	48	6	18	18	71	220		5.3
	1.2	All HBs	3.00	-65	5061	20	1839	39	29	15	11	14	78	3	2	6	22	26	225		7.4
			4.20	-65	7140	42	294	4	24	3	33	15	219	14	2	6	26	22	187		5.1
	+0.6 / -0.6	All HBs	3.00	-63	5114	18	1824	39	1	14	0	13	75	3	1	8	0	23	237		7.4
			4.20	-63	7183	41	350	2	1	5	1	12	204	13	2	8	1	18	154		5.3

4.2.1 General View of the Simulation

The simulation consists of separate pages (blocks) as seen in Figure 4.4. The Power System blocks consist of 154-kV three phase balanced voltage source with short-circuit MVA=5300, and a 154/10.5-kV transformer with 50-MVA and u_k=17% ratings. PLL is also implemented here. Q Measurement and Control block is responsible for adjusting the modulation index to satisfy the reactive power demand.

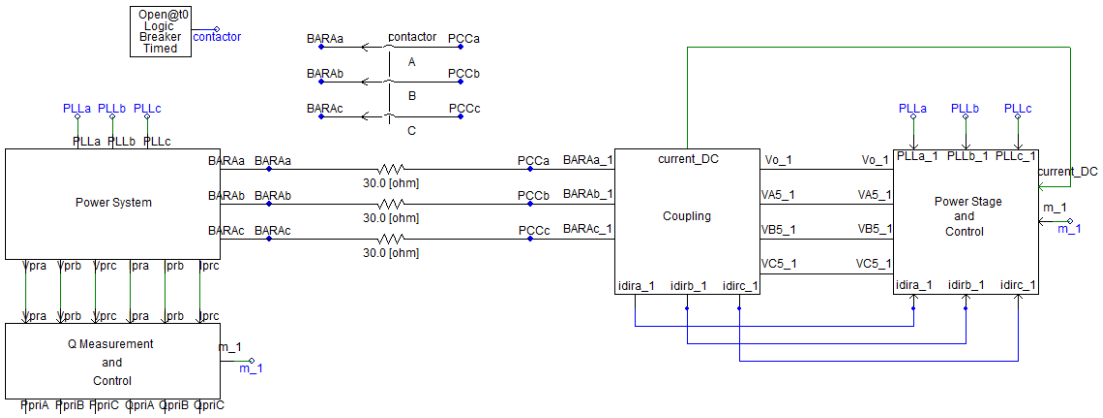


Figure 4.4 Main simulation page view

The pre-charge of the CMC HB dc link capacitors are made via 30Ω resistors (much more rapidly than the real case). When the pre-charge is complete, a by-pass contactor short-circuits the pre-charge resistors.

Coupling block consist of the series filter reactors (2.5mH) and their equivalent series resistances. Currents into CMC are measured here, and their average (dc) values are also calculated, then they are sent to the Power Stage and Control block.

The latter block is the heart of the simulation. It includes the HBs, dc link voltage control loops, MSS algorithm, offline look-up table for triggering angles, triggering signals and the dc current elimination controller.

The simulation time step is 66.67µs, plotting time step is 4ms, and the simulation duration is 40s. It was not possible to model transformer core saturation phenomenon in PSCAD, therefore the dc current elimination controller could not be tested for a growing dc current resulting from the core saturation. However, there are other reasons for dc current to flow, such as gating imbalance, 100-Hz voltage component in the transformer primary and 50-Hz voltage component in the dc links as mentioned earlier. These are all implemented in the simulation and the effectiveness of the dc current elimination control has been tested.

The Power System block seen in Figure 4.4 is given in detail in Figure 4.5.

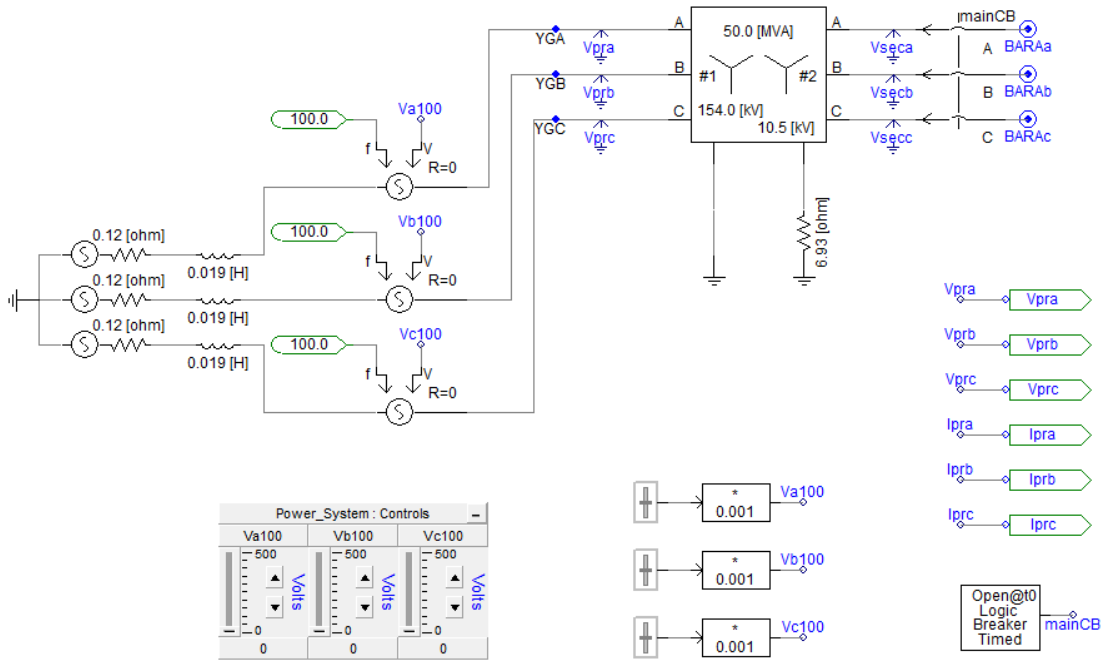


Figure 4.5 Power system simulation block

In Figure 4.5, 50-MVA, 154/10.5-kV coupling transformer is seen. The grid is modeled with a Thevenin equivalent circuit having 154-kV source and 3000-MVA short circuit power and X/R≈50. A 100-Hz voltage harmonic disturbance at PCC is controlled manually in order to test the dc current elimination controller.

The Coupling block is seen in Figure 4.6 in detail. The coupling reactors' inductance and resistance values are seen to be 2.5mH and 15mΩ, respectively with the ratio X/R≈50. Dc currents in the lines are measured by double averaging the current values by two windows with lengths 20 ms and 200 ms. The 3-phase average calculator block is user defined and Fortran code belongs to the author himself. The current directions are also sensed to be used for the selective swapping algorithm.

Q Measurement and Control block includes a PI controller which inputs the difference of 3-phase reactive power measured and reactive power set value. It outputs the modulation index value, *M*. The power stage view and the other blocks inside the Power Stage and Control block are seen in Figure 4.7 and Figure 4.8, respectively.

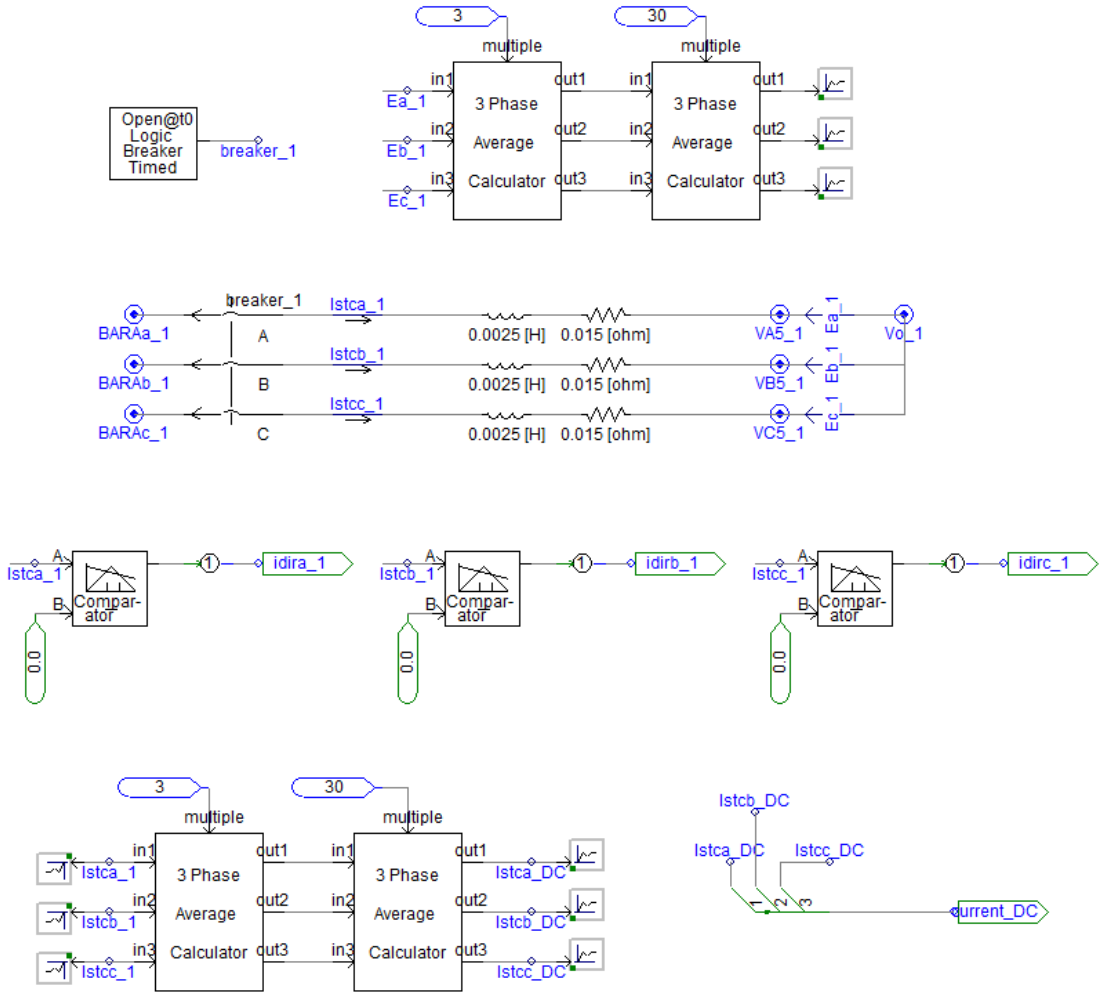


Figure 4.6 Coupling simulation block

In Figure 4.7, 15 HBs are seen in detail with their IGBTs, inverse parallel diodes, dc capacitors and their series resistances, laminated busbar stray inductances, etc. A manually controlled 50-Hz harmonic voltage source is connected in series to the dc link capacitor of phase-A HB1 in order to test the dc elimination controller.

In Figure 4.8, Dc Voltages and Control block and Triggering Signals block are seen. Dc Voltages and Control block takes the instantaneous voltage measurements from every HB dc link capacitor and averages every of them with a window of 20 ms long. For each phase, 5 HB dc link average voltages are summed up, the difference of this value from the set value (1900V) is passed through a PI controller and the delay angle, δ is found for each phase.

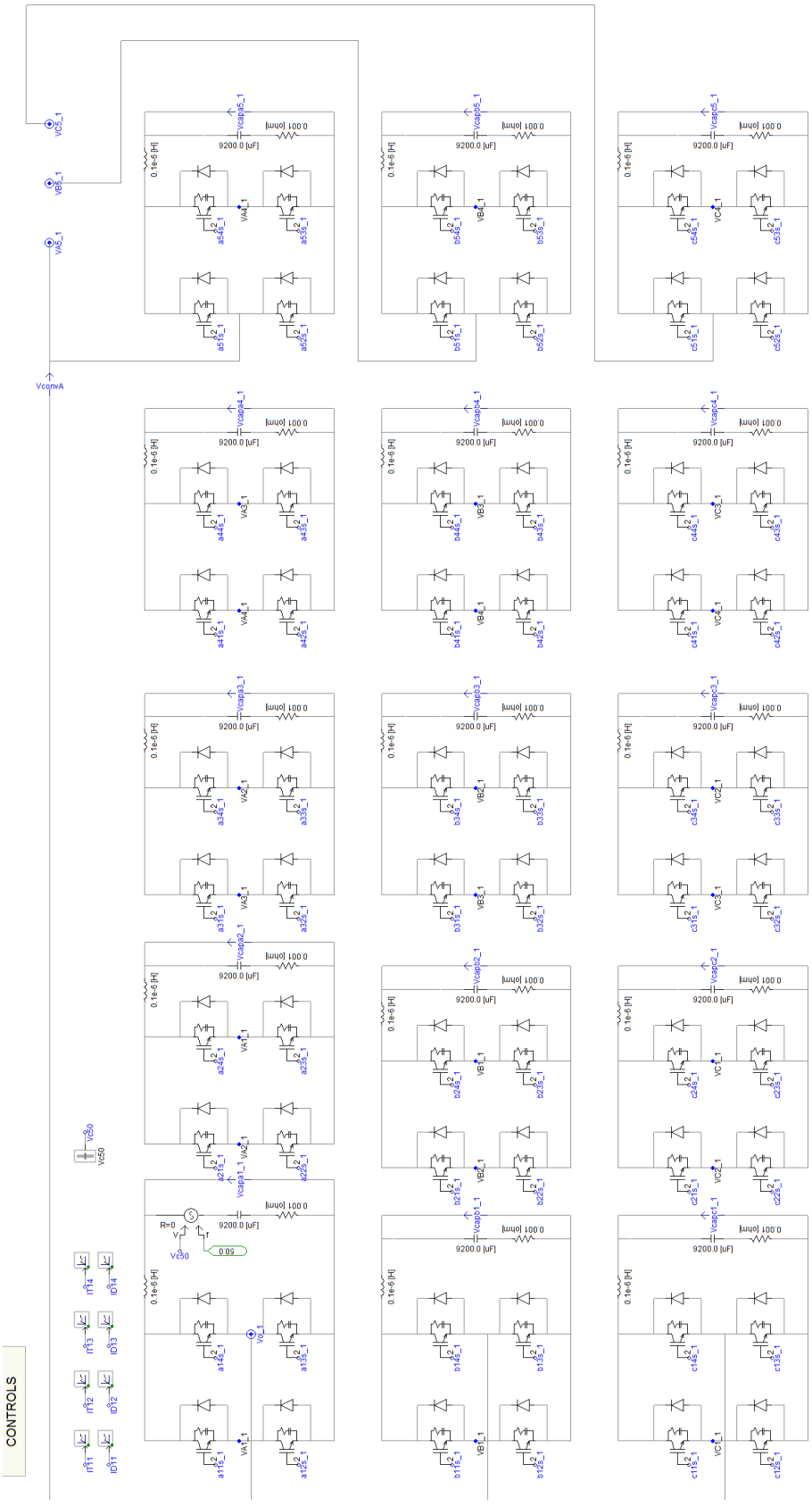


Figure 4.7 Power stage view in the simulation

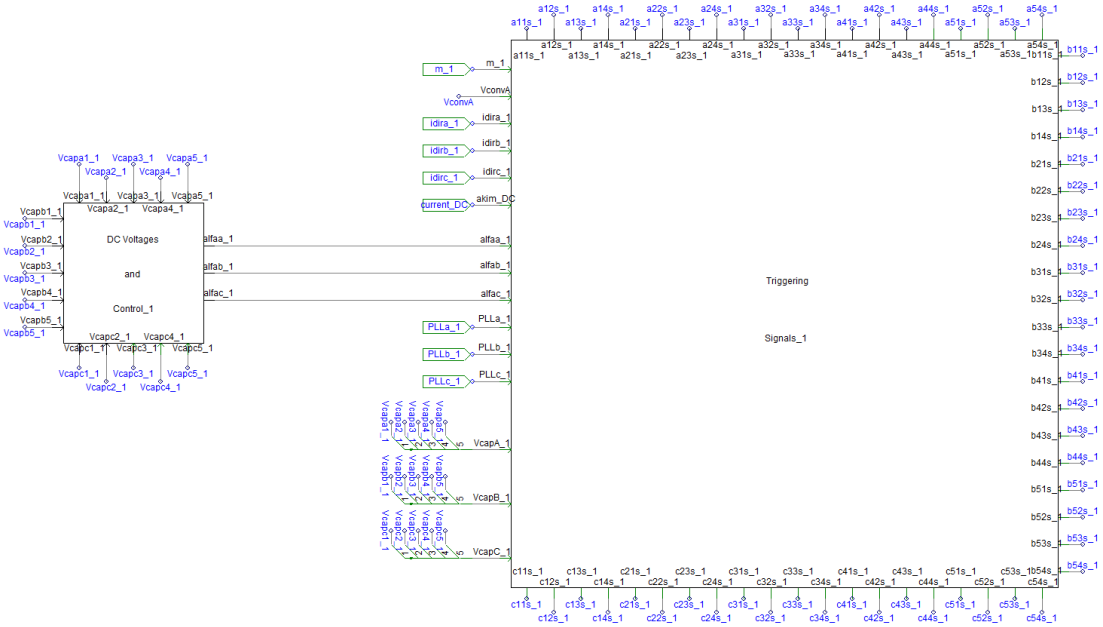


Figure 4.8 The other blocks inside the power stage and control simulation block

Triggering Signals block is the most complicated part of the simulation. It creates the switching signals for 60 IGBTs. It uses *M* value to find the θ values from the offline look-up table. It calculates the critical angle values determined as π-θ, π+θ, 2π-θ, and then adds δ value on all of these. It uses the output of phase locked loop (PLL) block together with these values to decide on the switching instants of the IGBTs. Selective swapping algorithm is also run here in a code block written in Fortran by the author. Interpolated firing pulse compatible blocks are used in order to maintain precise switching instants rather than a big time precision of 66.67µs, which is the simulation time step.

The following simulations are all conducted at rated capacitive reactive power (-10-MVAr at transformer primary), where CMC line current is 550A.

4.2.2 Gating Imbalance

Since the dc current elimination controller is implemented on phases A and B, the remaining phase can be used to create gating imbalance, and hence dc current. In Figure 4.9, the gating imbalance is changed by changing $\Delta\theta$ value of phase-C. The

set values for the dc current in phases A and B are zero. Therefore, $\Delta\theta$ values for phases A and B are changed by the PI controllers in such a way to bring the dc current in phases A and B, and hence all phases to zero. It is inferred from Figure 4.9 that $\Delta\theta$ values for phase A and B ($\Delta\theta_A$ and $\Delta\theta_B$) turn out to be same with $\Delta\theta_C$. This makes sense, since when all the phases have the same dc voltage, there will not be a dc unbalance and no dc current will flow in CMC lines, provided that the neutral is isolated from the ground.

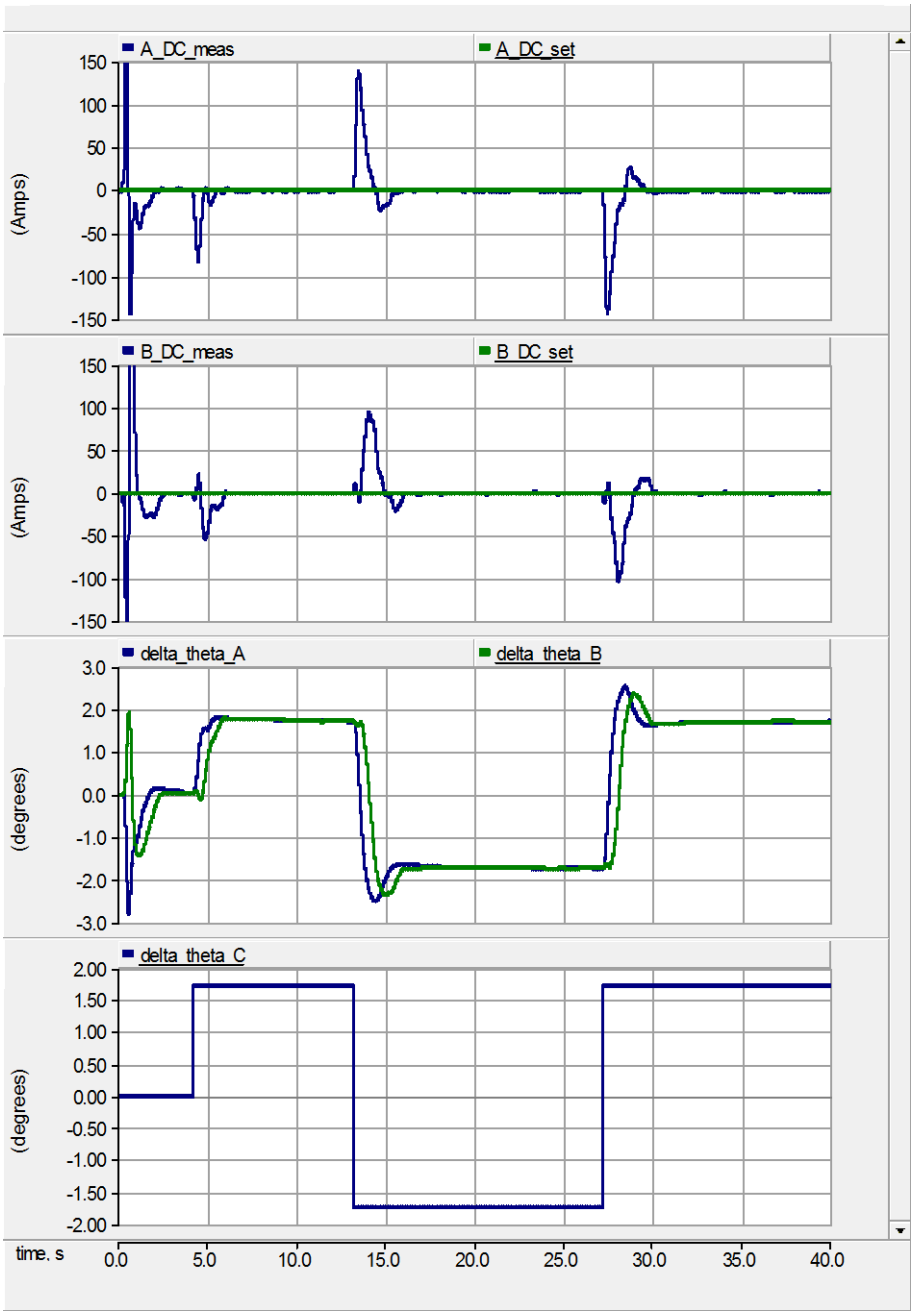


Figure 4.9 Response of dc current elimination control for gating imbalance

4.2.3 Second Harmonic Voltage on the Transformer Primary

This time, dc current elimination controller was off at the beginning of the simulation. At t=10s, a positive sequence second harmonic voltage with 0.5-kV peak magnitude is added to the 154-kV source. It is seen from Figure 4.10 that this results in a dc current flow into the CMC from t=10s to t=20s. At t=20s, dc current

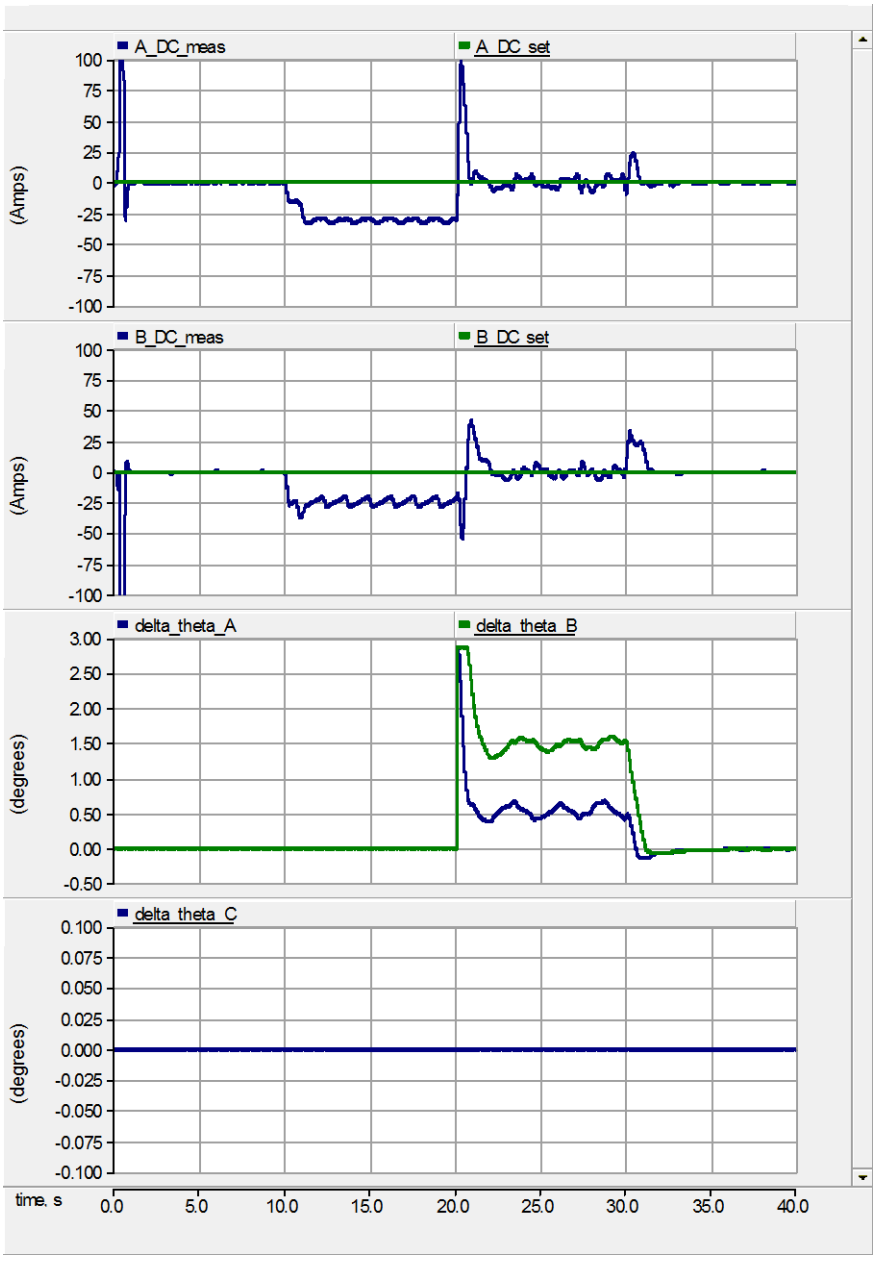


Figure 4.10 Response of dc current elimination control for second harmonic voltage at transformer primary

elimination controller is turned on. In less than two seconds, dc current components are diminished in both phases A and B. At t=30s, the second harmonic voltage on the source side is reduced to zero. Afterwards, it is seen that $\Delta\theta_A$ and $\Delta\theta_B$ also go to zero.

4.2.4 Fundamental Voltage Component on the HB Dc Link

Similar to the case above, dc current elimination controller was off at the beginning of the simulation. At t=10s, a 50-Hz voltage with 100-V peak magnitude is added to HB1 of phase-A. It is seen from Figure 4.11 that this results in a dc current flow into the CMC from t=10s to t=20s. At t=20s, dc current elimination controller is turned on. In less than two seconds, dc current components are diminished in both phases A and B. At t=30s, the 50-Hz voltage component on dc link of HB1 in phase-A is reduced to zero. Afterwards, it is seen that $\Delta\theta_A$ and $\Delta\theta_B$ also go to zero.

4.2.5 Different Dc Current Set Values

Normally, the set values for phases A and B dc currents are zero in the dc current elimination controller. However, these can be adjusted freely. In Figure 4.12, the response of $\Delta\theta_A$ and $\Delta\theta_B$, and hence dc currents in phases A and B are seen. It can be concluded that the set values are followed satisfactorily and the dc current elimination controller operates effectively.

4.3 MEASUREMENT SETUP

For the field measurements conducted in this research work, the Power Quality Analyzers (PQA) that have been designed and implemented by TÜBİTAK MAM Energy Institute, Electrical Power Technologies Department in scope of National Power Quality Project of Turkey, were used together with 36-kV and 420-kV Resistive Capacitive Voltage Transformers (RCVT), high voltage probes, Rogowski coils, and Hall Effect Current Sensors (HECS).

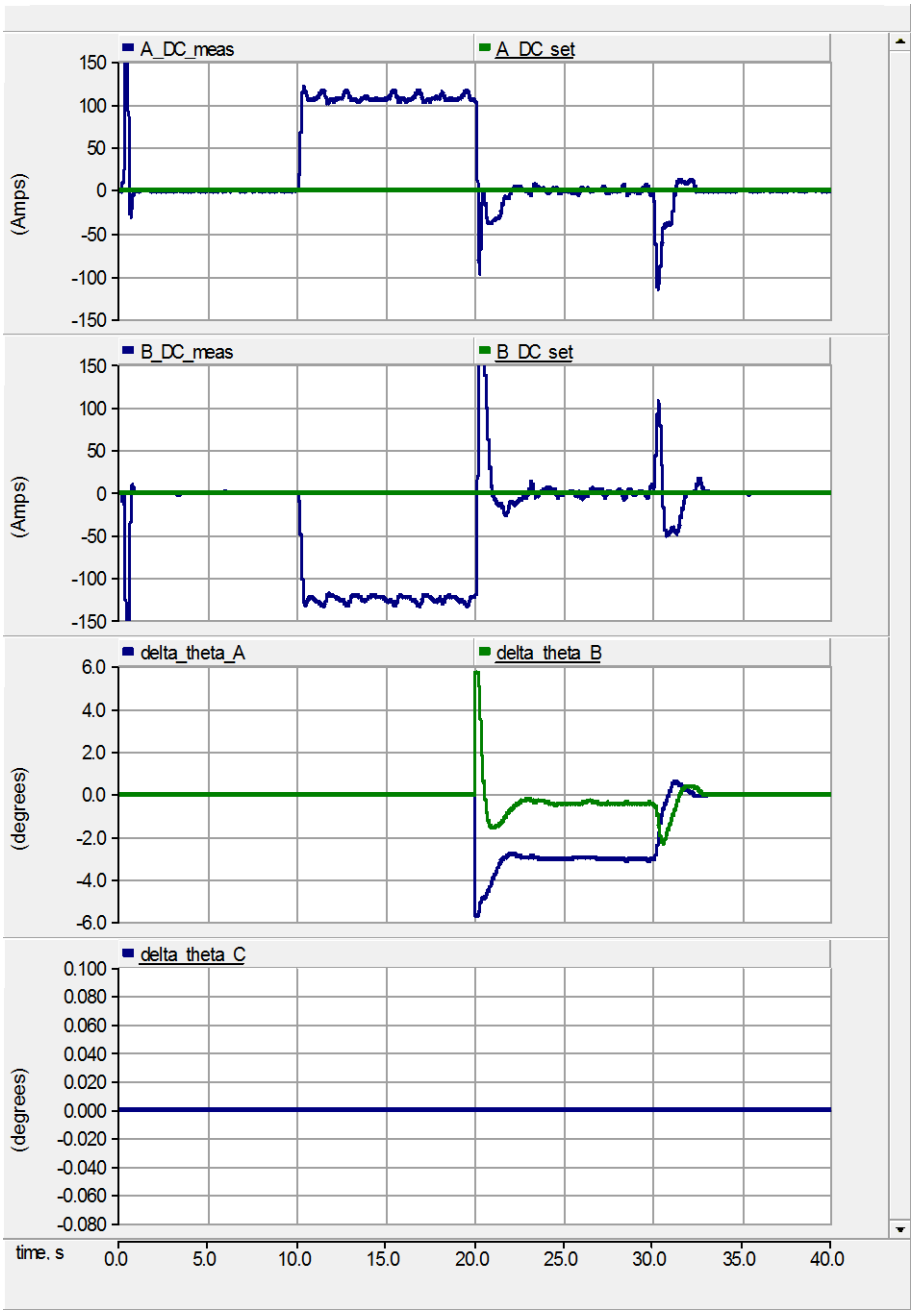


Figure 4.11 Response of dc current elimination control for fundamental voltage component on HB dc link

Four PQAs (see Figure 4.13) were used in order to measure

1) 3-phase HECS currents for all CMCs
2) Coupling transformer primary line currents by 0.2S class CTs
3) Coupling transformer primary line-to-earth voltages by 420-kV RCVTs
4) Coupling transformer secondary line-to-earth voltages by 0.5 class VTs

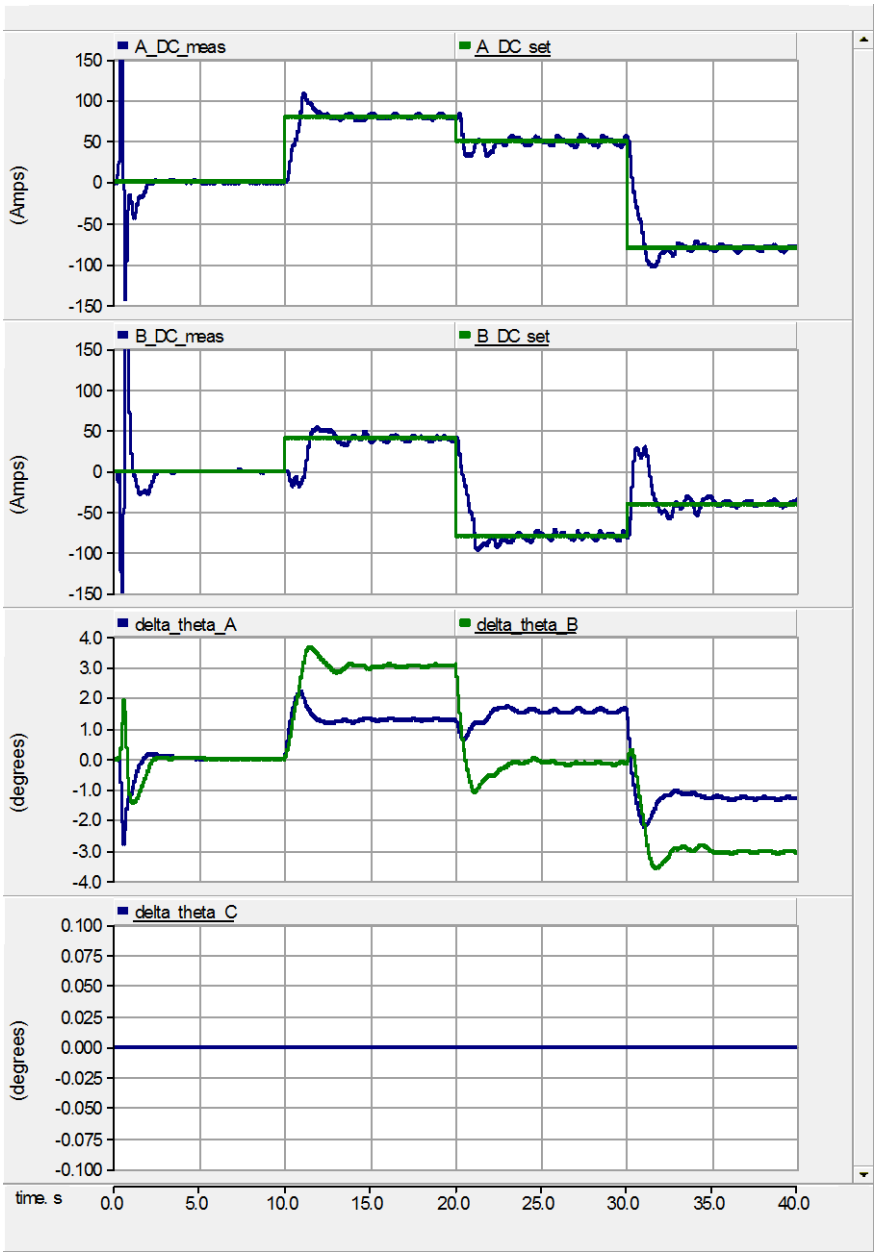


Figure 4.12 Response of dc current elimination control to difference set values of dc current

5) CMC5 output line-to-neutral voltages by 36-kV RCVTs
6) CMC5 3-phase HB1 capacitor voltages by high voltage probes
7) CMC5 phase-A and phase-B HB1 capacitor currents by Rogowski coils

The PQAs measure the voltage and current signals with a sampling frequency of 25.6-kS/s/ch. The HECSs are able to measure pure dc and the maximum amplitude

they can measure is ±1500-A. HECSs are mounted at the head of MV XLPE cables that connect the CMCs to coupling transformer secondary as seen in Figure 4.14 and Figure 4.15.

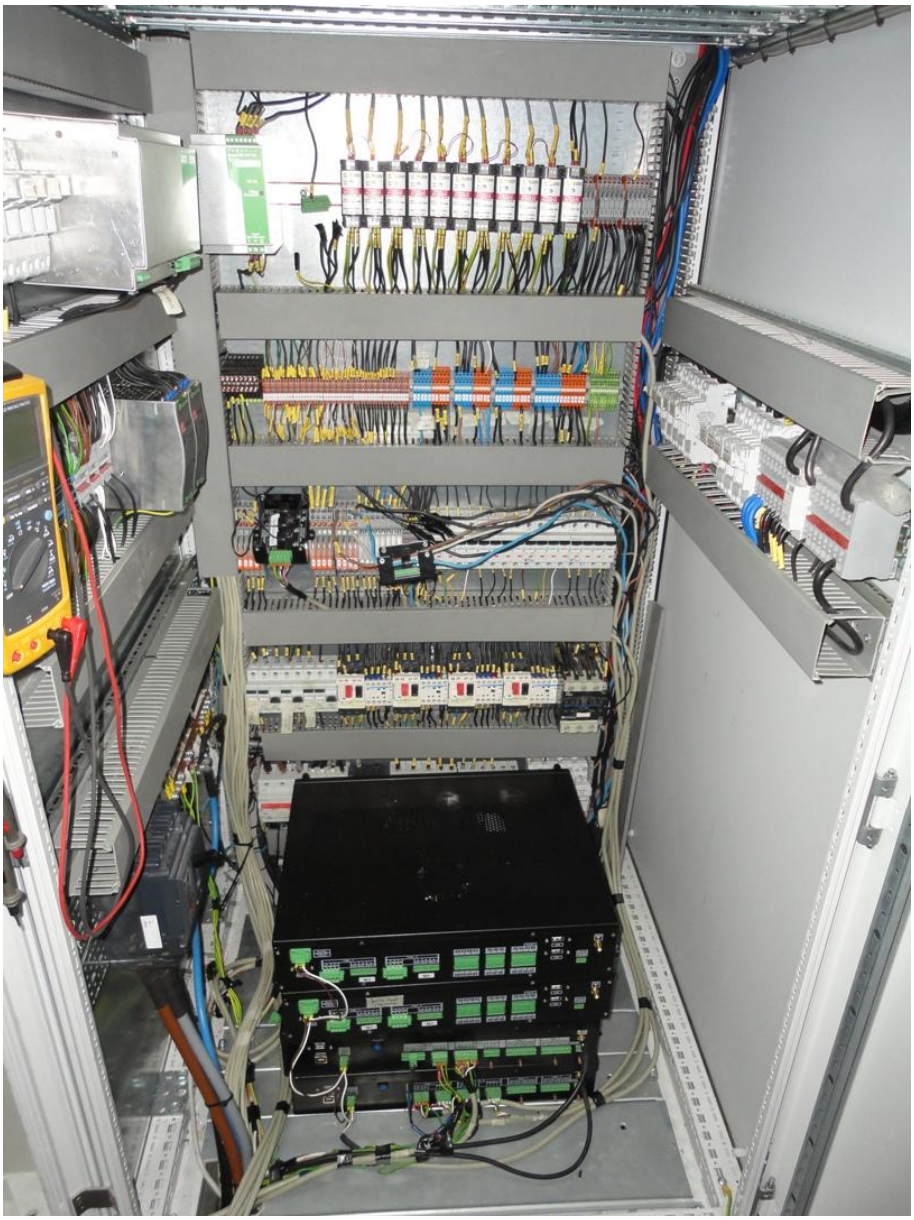


Figure 4.13 The power quality analyzers used for measurements in scope of the thesis

Figure 4.14 View of HECS sensors on the heads of MV XLPE cables

HB capacitor voltages and currents were measured with high voltage probes and Rogowski coils seen in Figure 4.16.

A single column of 36-kV RCVT that has been used for measuring line-to-earth output voltages of CMC5 is seen in Figure 4.17.

Figure 4.15 The HECS used in this thesis work for measuring CMC currents

4.4 FIELD TEST RESULTS

Following observations are made on the performance of sample T-STATCOM system during its operation in the field:

- Even harmonic components in the coupling transformer primary voltage waveform, especially 2^{nd} and 4^{th}, usually cause transformer core saturation when the fundamental component of transformer primary voltage is above the rated value.
- Transformer core saturation is never observed when only one CMC among five is active ($m'=1$).
- Proposed method is not necessarily to be applied simultaneously to all active CMCs, e.g., application to any three CMCs among five is quite enough.
- Transformer core saturation process may initiate at different values of reactive power delivered by the T-STATCOM in capacitive operation mode depending upon the strength of electrical damping.
- In the inductive operation region of the T-STATCOM, transformer core saturation never occurs even one makes the output ac voltage unbalanced manually.

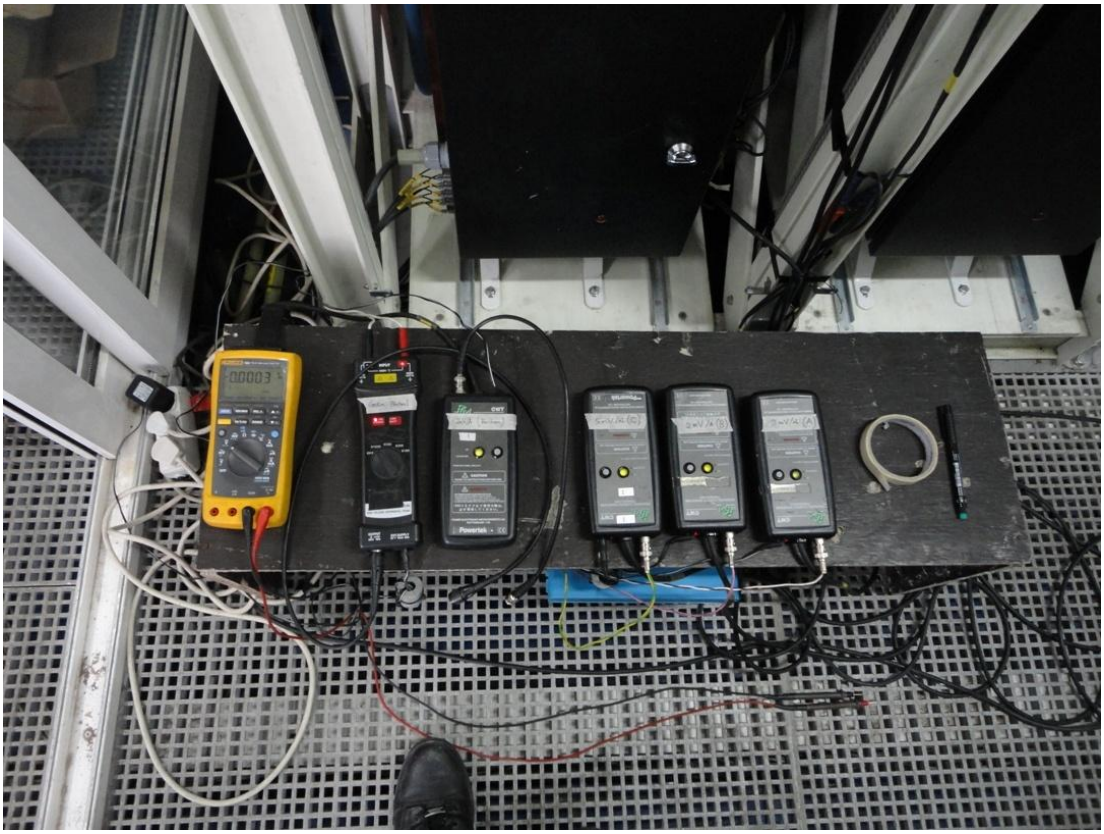


Figure 4.16 High voltage probes and Rogowski coils used for HB capacitor voltage and currents

Figure 4.17 36-kV RCVT column

- After equipping the T-STATCOM with the dc current elimination controller recommended in this thesis, coupling transformer has not come up with core saturation problem.

4.4.1 Prevention of Transformer Core Saturation

In order to illustrate the success of the dc current elimination method, a sample record in Figure 4.18 is taken from the T-STATCOM system during operation in the field (Q=-40-MVAr, m'=5). Normally, the trip value of the dc current elimination controller is adjusted to 150A per CMC, while its set value is always zero as shown in Figure 4.1. However in this test, the controller is enabled and disabled manually, i.e., whenever the total dc current in the lines of the transformer secondary tends to approach 600A (detected by visual inspection), the controller is enabled. This experiment is repeated rapidly and several times without permitting the decay of second harmonic flux entirely to zero. That is the main reason why the dc current component in Figure 4.18 grows up more rapidly than that of Figure 3.8.

During the record of waveforms in Figure 4.18, not only the fundamental component of transformer secondary voltage is considerably higher than its rated value (11.7-kV line-to-line), but also the primary voltage (160-kV line-to-line) is above the rated value. Furthermore, 2^{nd} and 4^{th} harmonic components continuously exist in the primary voltage waveform and their magnitudes are nearly the same (85V line-to-line). Persistent initiation of transformer core saturation process is attributed to these facts.

Figure 4.18 shows that the proposed method eliminates the dc current component in the lines of transformer secondary rapidly and prevents the transformer core from being saturated in CMC based T-STATCOM systems. In Figure 4.18, 10-cycle averaged rms quantities are plotted; Enb means enabled; Dsb means disabled; T-STATCOM delivers Q=40-MVAr to supply; m'=5; dc elimination controller is enabled and disabled manually. The dc current reaching 600A may be seen in the first graph of Figure 4.18. At this instant, the dc current elimination controller is enabled. It is seen that dc current, 50-Hz voltage on dc link, 2^{nd} harmonic current and voltage are all seen to cease rapidly. After a few seconds, the dc current elimination controller is disabled again. As can be understood from zoomed in records in Figure 4.19, dc current components and second harmonic current components decay to zero

nearly in 2-s time after enabling the dc current elimination controller at t=33.6s. In summary, the response in Figure 4.18 and Figure 4.19 shows that the proposed method eliminates the dc current component in the lines of transformer secondary

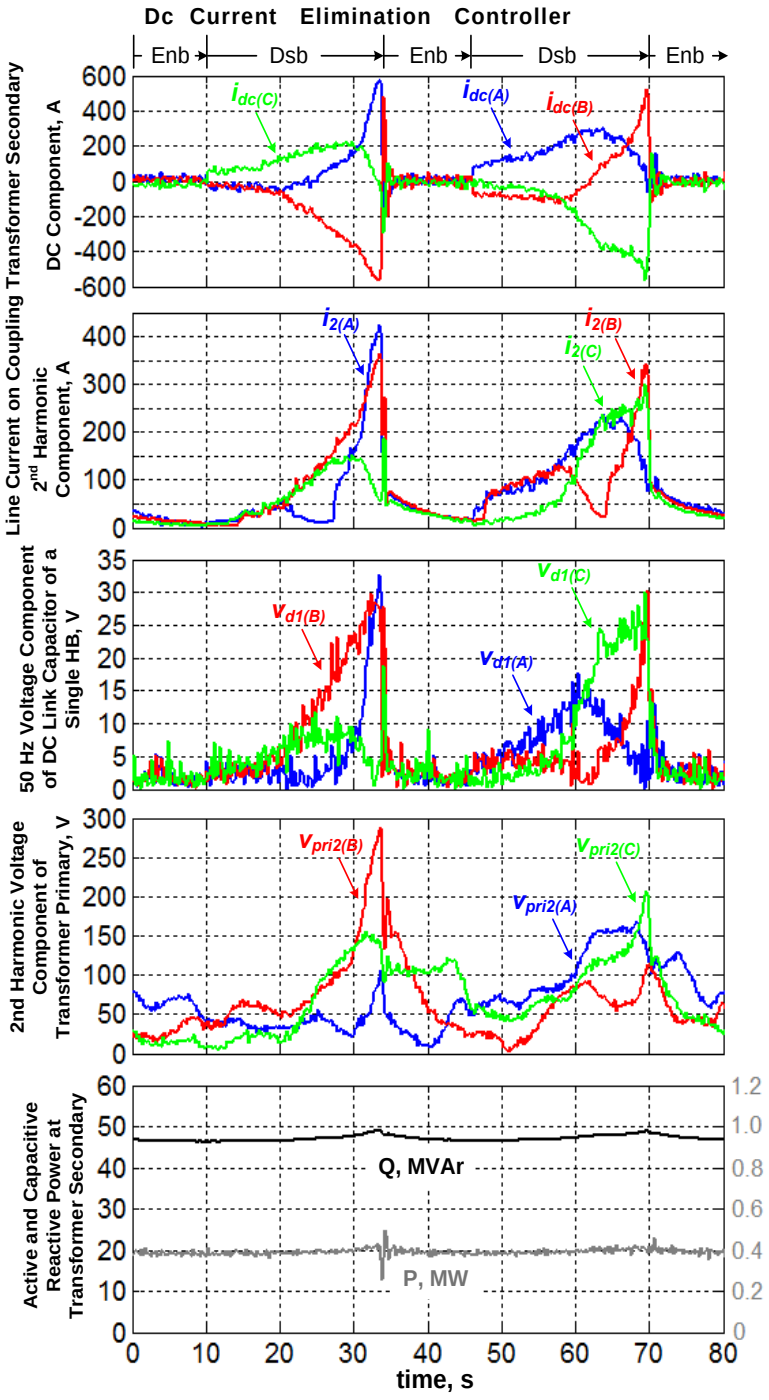


Figure 4.18 Field performance of the proposed dc current elimination method (80-s record)

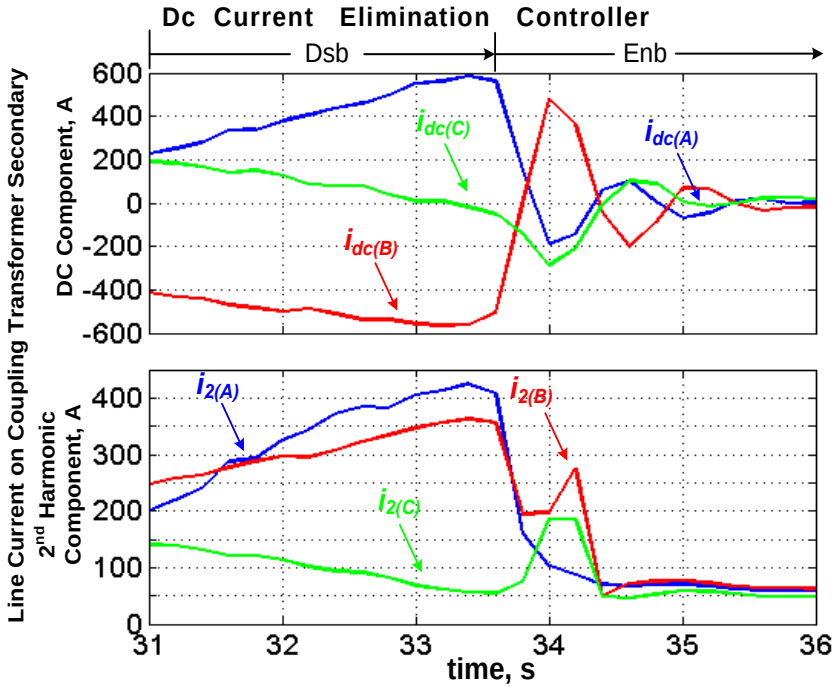


Figure 4.19 Field performance of the proposed dc current elimination method (Zoomed in record from 31st s to 36th s)

rapidly and prevents the transformer core from being saturated in CMC based T-STATCOM systems.

4.4.2 Nonzero Dc Current Set Values

Apart from preventing the transformer core from going into saturation by fixing the dc currents in CMC lines A and B at zero, the dc current elimination controller is also able to hold the dc currents at any desired value for a prolonged time. This is illustrated by Figure 4.20 (Q=+30-MVAr, m'=5).

In Figure 4.20, the set values of I_{Adc} and I_{Bdc} in each CMC for the first 70 seconds are zero. Between t=70s and t=225s, the set values of I_{Adc} and I_{Bdc} in each CMC are -70A and 60A, respectively. After t=225s, the set values are changed as I_{Adc}=80A, I_{Bdc}=0. As can be clearly seen from Figure 4.20, the dc current elimination controller can hold the dc currents in phases A and B at desired values.

The effect of dc current in CMC lines on HB dc link 50-Hz voltages, transformer secondary line current 100-Hz component and transformer primary voltage 100-Hz voltage is also seen in Figure 4.20. Together with the results given in Subsection 4.4.1, these results verify that the dc current elimination controller is able to hold the dc currents in CMC lines at any desired value including zero, and hence can prevent transformer core from going into saturation.

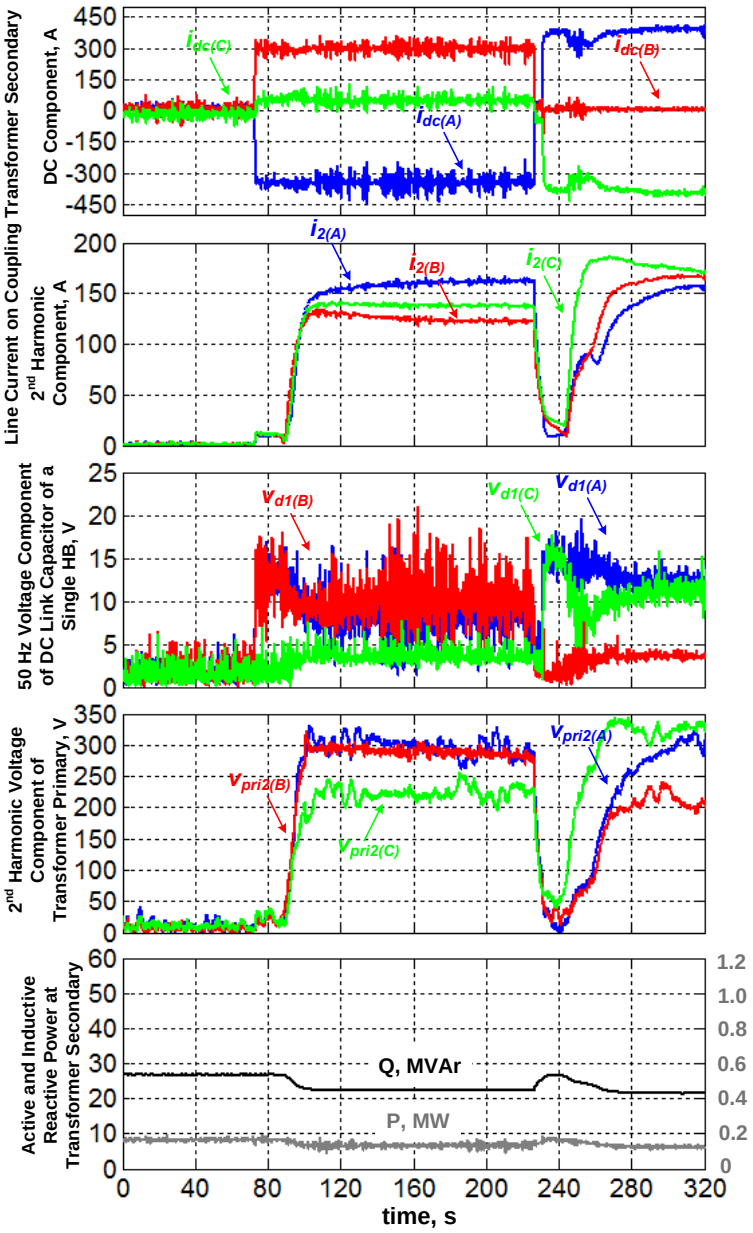


Figure 4.20 Nonzero dc currents at desired values set by the dc current elimination controller

CHAPTER 5

CONCLUSIONS

FACTS devices are being widely used in power systems, in order to enhance the system utilization and power transfer capacity as well as the stability, security, reliability and power quality of ac system interconnections. As a shunt FACTS device, Static Synchronous Compensator (STATCOM) systems are being installed at transmission and distribution levels.

This research work deals with coupling transformer core saturation problem in cascaded multilevel converter (CMC) based transmission-type static synchronous compensator (T-STATCOM) systems. The effects of nonlinear characteristics of the coupling transformer and CMCs on the core saturation phenomenon are investigated, and the associated mechanisms are described. In order to prevent the transformer core from being saturated, dc current components in the coupling transformer secondary lines are eliminated by modulating one or more than one voltage steps of staircase CMC voltage waveforms via the electronic gating circuitry. The proposed dc current elimination method is implemented on a 154-kV, ±50-MVAr CMC based T-STATCOM system, which is operating either in inter-area oscillation damping or terminal voltage regulation modes at any time in a 400/154-kV transformer substation since March 2010.

The implemented T-STATCOM consists of five 10.5-kV, ±12-MVAr CMC modules operating in parallel. The power stage of each CMC is composed of five series connected H-Bridges (HB) in each phase, thus resulting in 21-level line-to-line voltages. Dc link capacitor voltages of HBs are perfectly balanced by means of the

Modified Selective Swapping Algorithm proposed. The field tests carried out have shown that the steady-state and transient responses of the system are quite satisfactory.

At the present time, the T-STATCOM system is operating in terminal voltage regulation mode, but whenever an inter-area oscillation at ~0.15-Hz in weak ties is detected between the Turkish power system and European network of electricity transmission, it starts to operate in inter-area oscillation damping mode.

The major drawback of VSCs operating as a T-STATCOM is the significant rise in the secondary terminal voltage of the coupling transformer from full inductive mode to full capacitive mode. That is the main reason why peak flux density in the core of the coupling transformer may be moved to the saturation region for operation at high capacitive MVArs. For such operating conditions, the presence of even harmonic voltage components in the supply, particularly 2^{nd} harmonic, and/or dc current components in the transformer secondary lines injected by CMC/s may trigger the transformer core saturation process as a result of strengthening effect of ac-ac-dc cross modulation phenomenon. Therefore in the design of the coupling transformer, maximum possible transformer secondary voltage should be taken into account. Unfortunately, this may not be a solution to the transformer core saturation problem for perturbations with significant magnitudes. In addition to this, as recommended in this thesis, the electronic control circuit should be equipped with a dc current elimination controller in order to prevent the transformer core from being saturated even for perturbations with significant magnitudes.

Dc currents in transformer secondary lines are eliminated by modulating (narrowing and/or widening) positive and/or negative half-cycle voltages produced by one or more than one HB symmetrically, in each CMC. All control techniques described in this work are shown to have minor effect on distortion of line-to-neutral, and THD of line-to-line CMC output voltage waveforms, and hence they are equally applicable to the sample T-STATCOM system. However, the method which can be summarized as narrowing either the positive or negative half-cycle of the output voltage in the 3^{rd}

HB among five HBs, has been chosen for implementation because of its higher precision in the digital adjustment of pulse width. The effectiveness of recommended dc current elimination technique is verified by extensive field test results.

Future Work

In this research work, the core saturation problem of CMC based T-STATCOM system was solved, which enabled the system to operate at capacitive reactive power values higher than 30-MVAr. Another problem that reduces the reliability of the system is the overload currents observed during single line-to-ground faults. Therefore, operation under unbalanced voltages via modification in control algorithms is an important topic for the future.

The implemented system is designed to operate with balanced line currents. A future work can be the modification of control system into *dq0* domain positive and negative sequences in order to compensate unbalanced loads.

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APPENDIX-A

DERIVATIONS OF (2.3)–(2.6) IN CHAPTER-2

$$\vec{V}_c = V_c\angle 0, \vec{I}_c = I_c\angle -\theta, \vec{V}_s' = V_s'\angle\delta \tag{A1.1}$$

$$\text{T-STATCOM current: } \overrightarrow{I_c} = \frac{\overrightarrow{V_s'} - \overrightarrow{V_c}}{R + jX} \tag{A1.2}$$

Complex power input to T-STATCOM:

$$\begin{aligned}
&\overrightarrow{S_s} = P_s + jQ_s = \overrightarrow{V_s'}\overrightarrow{I_c}^* \\
&\overrightarrow{S_s} = \overrightarrow{V_s'}\left(\frac{\overrightarrow{V_s'} - \overrightarrow{V_c}}{R + jX}\right)^* = \overrightarrow{V_s'}\left(\frac{\overrightarrow{V_s'}^* - \overrightarrow{V_c}^*}{R - jX}\right) \\
&\overrightarrow{S_s} = \frac{V_s'^2 - V_s'V_c\angle\delta}{R - jX} = \frac{V_s'^2 - V_s'V_c\left(Cos\delta + jSin\delta\right)}{R - jX}
\end{aligned} \tag{A1.3}$$

Multiplying numerator and denominator by *(R+jX)*:

$$\overrightarrow{S_s} = \frac{V_s'^2R + jV_s'^2X - V_s'V_c\left[RCos\delta - XSin\delta + j\left(RSin\delta + XCos\delta\right)\right]}{Z^2} \tag{A1.4}$$

where, $Z = \sqrt{(R^2+X^2)}$

Real power input to T-STATCOM:

$$\begin{aligned}
&P_s = \mathrm{Re}\left\{\overrightarrow{S_s}\right\} = \frac{V_s'^2R - V_s'V_c\left[RCos\delta - XSin\delta\right]}{Z^2} \\
&P_s = \frac{V_s'\left[V_cXSin\delta - V_cRCos\delta + V_s'R\right]}{Z^2}
\end{aligned} \tag{A1.5}$$

Reactive power input to T-STATCOM:

$$Q_s = \mathrm{Im}\left\{\overrightarrow{S_s}\right\} = \frac{V_s^{'2}X - V_s^{'}V_c\left[\left(RSin\delta + XCos\delta\right)\right]}{Z^2}$$

$$Q_s = \frac{V_s^{'}\left[V_s^{'}X - V_cXCos\delta - V_cRSin\delta\right]}{Z^2} \qquad \text{(A1.6)}$$

Complex power input to VSC:

$$\overrightarrow{S_c} = P_c + jQ_c = \overrightarrow{V_c}\overrightarrow{I_c}^*$$

$$\overrightarrow{S_c} = \overrightarrow{V_c}\left(\frac{\overrightarrow{V_s^{'}} - \overrightarrow{V_c}}{R + jX}\right)^* = \overrightarrow{V_c}\left(\frac{\overrightarrow{V_s^{'}}^* - \overrightarrow{V_c}^*}{R - jX}\right) \qquad \text{(A1.7)}$$

$$\overrightarrow{S_c} = \frac{V_s^{'}V_c\angle\left(-\delta\right) - V_c^{\,2}}{R - jX} = \frac{V_s^{'}V_c\left(Cos\delta - jSin\delta\right) - V_c^{\,2}}{R - jX}$$

Multiplying numerator and denominator by *(R+jX)*:

$$\overrightarrow{S_c} = \frac{V_s^{'}V_c\left[RCos\delta + XSin\delta + j\left(XCos\delta - RSin\delta\right)\right] - V_c^{\,2}R - jV_c^{\,2}X}{Z^2} \qquad \text{(A1.8)}$$

Real power input to VSC:

$$P_c = \mathrm{Re}\left\{\overrightarrow{S_c}\right\} = \frac{V_s^{'}V_c\left[XSin\delta + RCos\delta\right] - V_c^{\,2}R}{Z^2}$$

$$P_c = \frac{V_c\left[V_s^{'}XSin\delta + V_s^{'}RCos\delta - V_cR\right]}{Z^2} \qquad \text{(A1.9)}$$

Reactive power input to VSC:

$$Q_c = \mathrm{Im}\left\{\overrightarrow{S_c}\right\} = \frac{V_s^{'}V_c\left[\left(XCos\delta - RSin\delta\right)\right] - V_c^{\,2}X}{Z^2}$$

$$Q_c = \frac{V_c\left[V_s^{'}XCos\delta - V_s^{'}RSin\delta - V_cX\right]}{Z^2} \qquad \text{(A1.10)}$$

APPENDIX-B

SHEM EQUATIONS

The line-to-neutral waveform for 11-level CMC shown in Figure 2.10 of Chapter-2 can be expressed as:

$$f(t) = F_0 + \sum_{n=1}^{\infty}(a_n \cos(\text{hwt}) + b_n \sin(\text{hwt})) \quad \text{(B1.1)}$$

Since the output voltage is odd-quarter wave;

$$a_h = 0 \quad \text{(B1.2)}$$

and

$$b_h = \begin{cases} \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\theta)\sin(h\theta)\ d\theta & for\ h = 1,3,5\ldots \\ 0\ for\ h = 2,4,6,\ldots \end{cases} \quad \text{(B1.3)}$$

Assuming dc link capacitor voltages are all balanced and equal to V_d;

$$b_h = \frac{4V_d}{\pi}[\cos(h\theta_1) + \cos(h\theta_2) + \cdots + \cos(h\theta_n)] \quad \text{(B1.4)}$$

The fundamental component is

$$b_1 = \frac{4V_d}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_n)] \quad \text{(B1.5)}$$

To eliminate low order harmonics of 5^{th}, 7^{th}, 11^{th} and 13^{th} in the line-to-neutral voltages of CMC by the switching angles of θ_1, θ_2,...., θ_5, the following equations are used:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = M \quad \text{(B1.6)}$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \quad \text{(B1.7)}$$

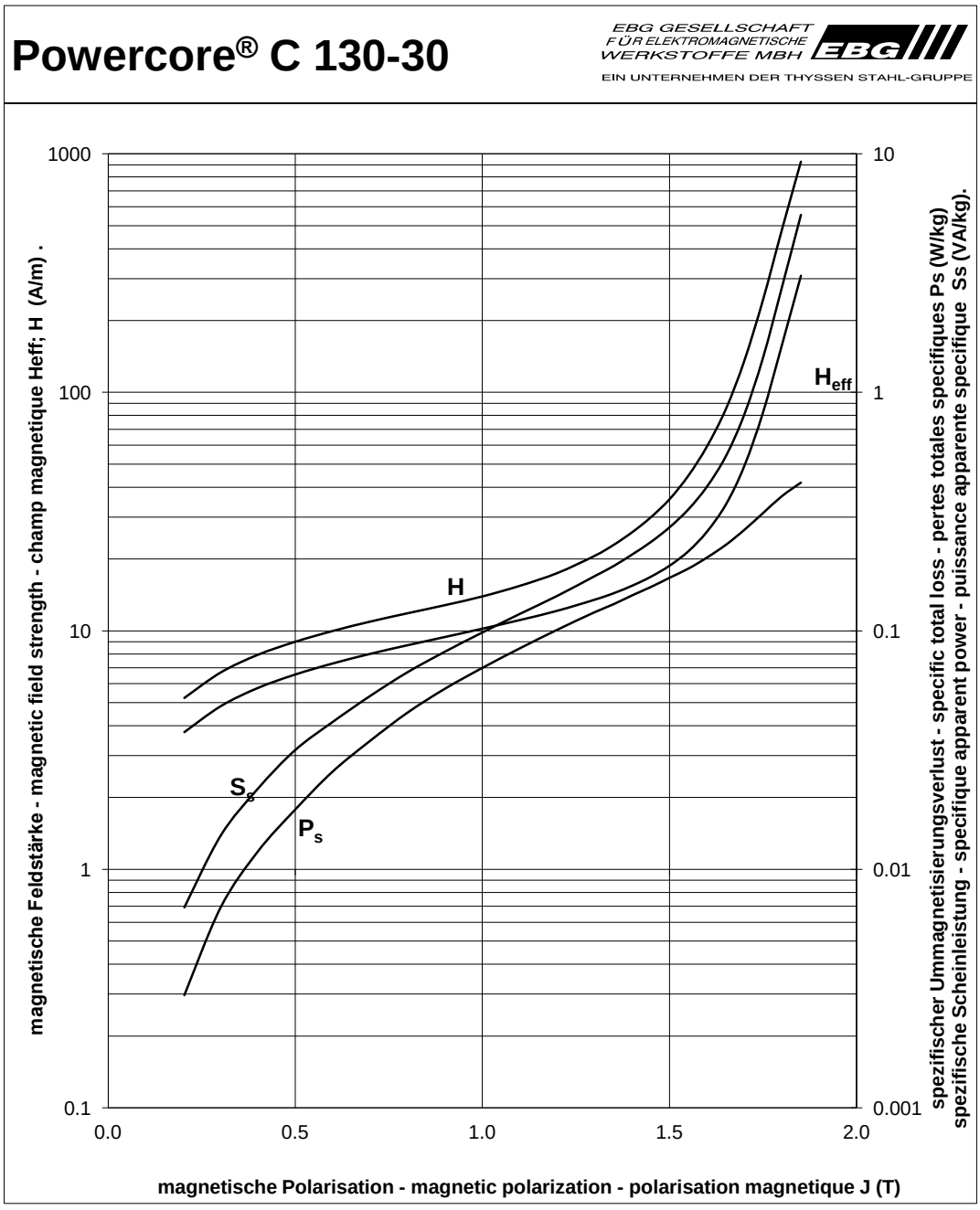
$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \quad \text{(B1.8)}$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \quad \text{(B1.9)}$$

$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \quad \text{(B1.10)}$$

APPENDIX-C

B-H CHARACTERISTICS OF C130-30 TRANSFORMER CORE MATERIAL



APPENDIX-D

COUPLING TRANSFORMER
EXCITATION CURRENT DATA

BEST

3 Fazlı Yağlı Tip Transformatör
Boşta Kayıp ve Boşta Çalışma
Akımının Ölçümü **Deney Raporu**

Müşteri:	TEİAŞ				
Seri No.:	54078	Rapor No.:		Sayfa No.:	
Anma Gücü(kVA):	50000 / 62500	Bağlantı Gr.:	YNyn0	Standart:	IEC 60076
Anma Gerilimi(kV):	154 / 11,1	Soğutma Tipi:	ONAN/ONAF		

	Gerilim	Akım	Güç	Açıklamalar
Ölçü Aletinden Okunan	11086	2,242	12,526	
	11086	1,389	7,244	
	11086	2,17	8,859	
Sonuç	11086 V.	Ort. A. 1,934	Top. kW. 28,629	I_0 % = 0,0595
Ölçü Aletinden Okunan	12227	5,587	20,308	
	12227	3,691	10,25	
	12227	5,565	9,176	
Sonuç	12227 V.	Ort. A. 4,948	Top. kW. 39,734	I_0 % 0,152

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FOREIGN LANGUAGES

English

PUBLICATIONS

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3. T. Atalik, M. Deniz, E. Koc, C.O. Gercek, B. Gultekin, M. Ermis, I. Cadirci, “Multi-DSP and -FPGA-Based Fully Digital Control System for Cascaded Multilevel Converters Used in FACTS Applications”, *IEEE Trans. Ind. Info.*, vol. 8 , no. 3, pp. 511–527, 2012.
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5. M. Deniz, B. Gultekin, C.O. Gercek, T. Atalik, I. Cadirci, M. Ermis “A new DC voltage balancing method for cascaded multilevel inverter based STATCOM”, *IEEE International Aegean Conference on Electrical Machines and Power Electronics*, pp.532-535, 2007.