

K BAND SUBSTRATE INTEGRATED WAVEGUIDE POWER DIVIDERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

ORÇUN KİRİŞ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2014

Approval of the thesis:

K BAND SUBSTRATE INTEGRATED WAVEGUIDE POWER DIVIDERS

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ABSTRACT

K BAND SUBSTRATE INTEGRATED WAVEGUIDE POWER DIVIDERS

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September 2014, 108 pages

In this thesis, various K band power divider structures are developed using the substrate integrated waveguide (SIW) technology. In the design and production of the 1 x 2 Y and T - Junction power dividers known as the conventional power divider types, good agreements are observed between measured and simulated S_{11} results. Also, the differences between simulated and measured S_{21} results are approximately $0.4 - 0.8$ dB at the operating frequency. In addition to these, 1 x 4 dividers obtained by successive addition of the conventional structures are designed and produced. The designed and fabricated Y & Y and T & Y - Junction SIW power dividers have approximately 0.6 dB and 0.4 dB insertion loss differences between the measurement and simulation results respectively. Moreover, there are good agreements between the S_{11} simulation and measurement results.

Furthermore, a novel 1 x 8 power divider is proposed for unequal power division operation. The proposed divider is designed and fabricated to provide almost equal phases and -20 dB SLL Taylor ($n=3$) amplitude distribution at output ports.

8x1 and 8x4 slotted SIW arrays, fed through this power divider, are designed, fabricated and measured. Measurement results are compared with the simulations to verify the designs and measured far fields agree very well with the simulated ones.

Keywords: Substrate Integrated Waveguide (SIW), Power Dividers, Beam Forming Networks (BFN), Slot Array Antenna

ÖZ

K BAND SUBSTRAT TÜMLEŞİK DALGA KILAVUZU GÜÇ BÖLÜCÜLER

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Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Prof. Dr. Özlem Aydın Çivi

Eylül 2014, 108 sayfa

Bu tez çalışmasında Substrat Tümlleşik Dalga Kılavuzu (STDK) teknolojisi kullanılarak çeşitli güç bölücü yapıları incelenmiştir. Geleneksel ikiye bölen güç bölücü yapıları olarak bilinen 1 x 2 Y ve T-Bağlantı güç bölücülerinin tasarımı ve üretiminde, S_{11} ölçüm ve benzetim sonuçlarının uyumlu olduğu gözlenmiştir. Ayrıca, S_{21} ölçüm ve benzetim sonuçları arasındaki farklar çalışma frekansında $0.4 - 0.8$ dB civarındadır. Bunlara ek olarak, geleneksel yapıların art arda kullanılması ile elde edilen 1 x 4 güç bölücü yapıları tasarlanmış ve üretilmiştir. Tasarlanan ve üretilen Y & Y ve T & Y - Bağlantı STDK güç bölücülerini, araya girme kaybı ölçüm ve benzetim sonuçları arasında sırasıyla yaklaşık 0.6 dB ve 0.4 dB farklılığa sahiptir. S_{11} benzetim ve ölçüm sonuçları da birbiriyle uyumludur.

Bu çalışmada ayrıca, eşit olmayan güç bölme işlemi için yeni bir sekize bölen güç bölücü yapısı önerilmiştir. Önerilen yapı, çıkış terminallerinde neredeyse eş fazlara sahip olacak ve -20 dB SLL Taylor ($n=3$) genlik dağılımını sağlayacak şekilde tasarlanmış ve üretilmiştir.

Tasarlanan güç bölücü ile beslenen 8x1 ve 8x4 yarıkli STDK dizi antenleri tasarlanmış, üretilmiş ve ölçülmüştür. Tasarımı doğrulamak amacıyla ölçüm sonuçları benzetimler ile karşılaştırılmış; ölçülen ve benzetimden elde edilen ışım örüntüleri arasında iyi bir uyum gözlenmiştir.

Anahtar Kelimeler: Substrat Tümlşik Dalga Kılavuzu (STDK), Güç Bölücüler, Hüzme Biçimlendirme Ağı, Yarık Dizi Anteni

Dedicated to my family...

ACKNOWLEDGEMENTS

I would like to express my gratitude to everyone who has helped me in completing this thesis, even if their names are not mentioned here. First and foremost, I would like to present my sincere thanks to my advisor Prof. Dr. Özlem Aydın Çivi, not only for her guidance, advice, criticism and encouragement during the course of this thesis, but also for the trust and opportunity she bestowed upon me to pursue my research in Microwave Research Group. I would like to thank Prof. Dr. Sencer Koç and Prof. Dr. Şimşek Demir for sharing their invaluable experience and suggestions. I also would like to thank Prof. Dr. M. Tuncay Birand, Prof. Dr. Nevzat Yildirim, Prof. Dr. Altunkal Hızal, Prof. Dr. Gülbin Dural and Assoc Prof. Dr. Lale Alatan for their unsurpassed lecture hours, from which I learned much.

I would like to express my acknowledgements to Ömer Bayraktar not only for his guidance, support and encouragement, but also for being my elder brother with whom I can consult about anything in my life without hesitation.

I would like to express my thanks to ASELSAN and in particular to Şebnem Saygıner, Zeynep Eymür and Didem Cansu İlhan for their help in producing some of the devices.

I would like to thank Alper Yalım, Nuri Kapucu and Mehmet Bilim for their support, contributions and friendship throughout research. I am also thankful to Özgehan Kılıç, Çağrı Çetintepe, İlker Comart, Yaşar Barış Yetkil, Savaş Karadağ, Yusuf Sevinç, Ahmet Kuzubaşlı, Enis Kobal, Ufuk Tamer and Amin Ronaghzadeh for their help and providing such a friendly research environment.

I offer my deepest thanks to my childhood friend Halil Dođan for his genuine support, understanding, and constant encouragement in all circumstances.

Last but certainly not least, my heartfelt thanks go to my mother Raziye Kiriř, my father Fikrettin Kiriř and my brother Onur Kiriř for their steadfastness, toleration, everlasting love, support and trust in me. This work would have never been completed without them.

This work is partially supported by the Scientific and Technical Research Council of Turkey (TÜBİTAK) within the scope of the 111R001 and the 109A008 projects.

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CHAPTER 1

INTRODUCTION

Recently, several antennas, arrays and microwave components are presented by Substrate Integrated Waveguide (SIW) technology. SIW technology is a mixture of the conventional waveguides and the microstrip technology.

Conventional waveguide technology has various disadvantages such as the high cost, large size, high precision machining requirement, inflexibility, difficulty of mass production and trouble of post fabrication tuning. However, it is commonly utilized to realize the high power handling capacities, high-Q with low insertion losses in the microwave and the millimeter wave systems. Moreover, the integration of waveguides with planar structures necessitates complicated, bulky and lossy transitions. These transitions commonly require a mechanical assembling which is too pricy to be actualized in millimeter-wave frequencies. Additionally, it is not suitable for the trial purposes production used in research and development, because of these trade-offs.

Microstrip structures, however, have completely opposite characteristics. While these structures have high ohmic losses and high insertion losses at higher frequencies, their low size, flexibility and ease of manufacturing make them common in many printed circuit board (PCB) designs. In addition, the production of these structures is relatively fast and inexpensive.

Recently, a novel convenient scheme of high-frequency applications has been presented that is called “Substrate Integrated Waveguide (SIW)” [1]. SIW is an artificial channel that guides waves with the help of two parallel rows of plated-through (metalized) via holes in a planar substrate which have metal-coated top and bottom surfaces. A typical SIW structure is shown in Figure 1.1.

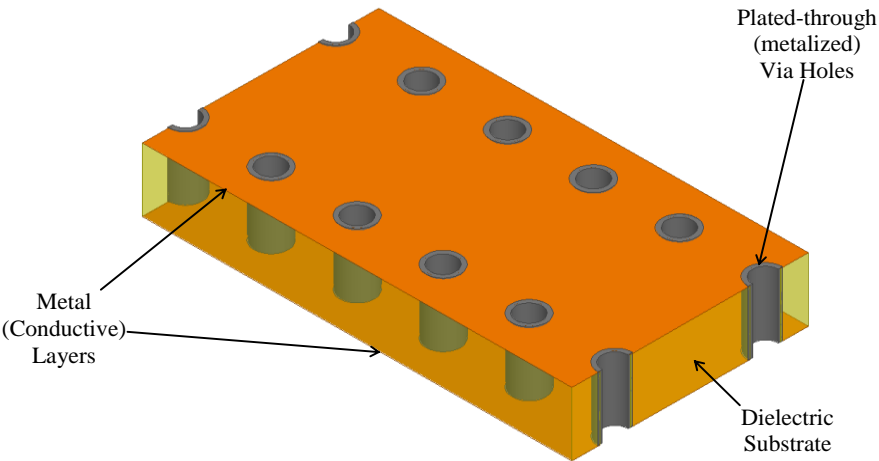


Figure 1.1: Substrate Integrated Waveguide

SIW has a remarkable role in low profile, low weight millimeter-wave and microwave systems with low return loss, low cost, relatively high Q-factor and power handling capacity [2]-[4]. Moreover, the SIW structure can be easily manufactured by PCB technology. Therefore, the SIW based components are easy to be integrated in the other types of the planar circuits which can be produced as PCB. Also, interconnection losses of waveguides integrated to planar microwave circuits are largely eliminated by designing the transitions on the same substrate.

Power dividers are utilized to design various subsystems such as antenna feeding networks, multiplexers, couplers. Several power divider structures realized by waveguide technology as well as microstrip technology can be found in the literature and are also available commercially in the market.

SIW power dividers are developed in order to eliminate the negative features of the waveguide and microstrip technology mentioned above. SIW power dividers can easily be integrated with planar antennas and other microwave components on the same substrate.

The conventional power divider designs in waveguide technology are separated in two main categories as T-Junction and Y-Junction. The experience gained from the traditional design methods is also used in SIW based power divider designs [4], [40].

A 1 x 2 T-Junction SIW power divider is designed in the 82-99 GHz frequency range [41]. The results achieved from this study show that -15 dB return loss (S_{11}) and about -3 dB insertion loss (S_{21} , S_{31}) have been obtained at each output port. Use of SIW decreases the dimensions of the similar functional structure that is designed with conventional waveguide structure approximately by fifty percent. A further optimization of 1 x 16 T-Junction power divider with bending structures is proposed in [22]. In another study, a Y-Junction power divider operating at 22-26 GHz frequency band is used with SIW hybrid 3 dB coupler [42]. The results obtained from this study, S_{11} ve S_{22} are below -20 dB at the center of the frequency band and also less than -15 dB during the mentioned frequency band. A good isolation between the terminals is understood from the results of this design. For example, $S_{53} = -37$ dB and the other required parameters are consistent with the theoretical values. The two conventional methods have been studied in another study [43]. A T-Junction power divider operating at 25.7-33 GHz frequency range and a Y-Junction power divider operating at 23.8-32 GHz frequency range are designed in this study. In both designs, S_{21} and S_{31} of these designs are about -3 dB and S_{11} values are obtained below -20 dB in the specified frequency ranges. A further optimized structure, Y-junction four-way power divider, is proposed by integrating the 90° Y-junction SIW power divider and the half-mode substrate integrated waveguide (HMSIW) power divider [44]. Use of the half-mode HMSIW reduces the size of SIW by almost 50%. The return loss of

this design is below -15 dB over 8.6 to 12.2 GHz and transmissions are about $27.6\text{ dB} \pm 0.2\text{ dB}$ in the passband.

In addition to all mentioned before, the SIW power dividers that are designed by combining T and Y-Junction design types are available in the literature. One of these is a 1×8 SIW power divider operating in the range of $8\text{-}12\text{ GHz}$ [45]. The most remarkable feature of this design is that it has less than $\pm 0.9\text{ dB}$ and $\pm 4^\circ$ amplitude and phase imbalance over a bandwidth of 4 GHz centered at 10 GHz . An application of this power divider structure is used as the feeding network of a Vivaldi antenna array operating at 10 GHz [26]. A 1×16 SIW power divider operating at $10.25\text{ - }12\text{ GHz}$ frequency range is presented with less than -15 dB return loss value [46]. Also, S_{i1} ($i=2, \dots, 17$) values of this divider have been measured as about $-14.5\text{ dB} \pm 0.5\text{ dB}$.

Another important advantage of using SIW technology is that; it allows multi-layer design and manufacturing due to its low volume and planarity. In this method, the power divider utilizes coupling slot transition between SIW guides with the conventional power divider such that the size is nearly reduced by half [47]-[49].

Another power divider design in literature is based on the Multimode Interference Imaging (MMI). The insertion loss from the input waveguide to each divided output is -9 dB at 25 GHz . The isolation between each output port is better than 10 dB [50].

Radial cavity power divider is presented in [51]. It consists of a SIW radial cavity that is synthesized in a planar substrate with arrays of metallic via in order to achieve peripheral walls, a central probe, and equally located identical peripheral probes. A probe-to-waveguide transition is realized with the help of a metallic via designated by a current probe by which power dividing is achieved. In another study, a 1×4 radial half-mode SIW with improved center feeding is proposed [52].

1.1. Thesis Objectives and Organisation

The main objective of this thesis is to investigate, design and implement Substrate Integrated Waveguide (SIW) Power Dividers. The goals can be summarized as follows,

- ❖ Characterization of SIW
 - Determination of diameter and period values for metalized vias of SIW in order to minimize the leakage.
 - Analyzing the amount of leakage of SIW design with determined diameter and period values.
- ❖ Efficient transition structure design
 - Designing a transition for efficient power transfer from microstrip feeding line to SIW or vice versa.
- ❖ Development and Characterization of 1 x 2 SIW Power Dividers
 - Design, fabrication and characterization of Y and T-Junction SIW power dividers.
- ❖ Characterization of 1 x 4 SIW Power Dividers
 - Design, fabrication and characterization of 1 x 4 Y & Y and T & Y-Junction SIW power dividers.
- ❖ Design and Characterization of a novel 1 x 8 SIW unequal power divider
 - Design of 1 x 8 Multimode based unequal SIW power divider.
 - Design of slotted SIW array antennas fed by 1 x 8 SIW Power Divider
 - Fabrication and measurements of the arrays and power divider

After this introduction chapter, Chapter 2 introduces the fundamental SIW technology, the feeding types of SIW and determination of diameter and period of vias. The design of the microstrip to SIW transition is also included in this chapter.

Chapter 3 explains the design methodology for different kinds of SIW power dividers. This chapter presents a comparison of the alternative power divider designs. A novel 1 x 8 unequal power divider and two slotted SIW arrays fed by this 1 x 8 unequal power divider are also presented in this chapter.

Chapter 4 includes the conclusion of the thesis and suggests future work demanding further research.

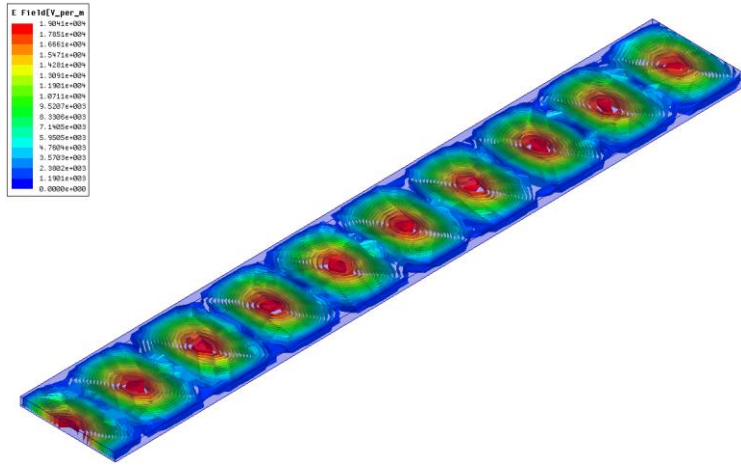
CHAPTER 2

SUBSTRATE INTEGRATED WAVEGUIDES

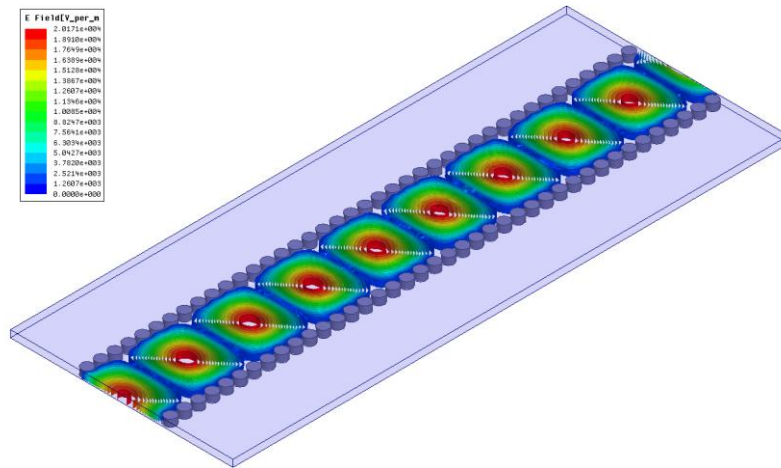
2.1. SIW Design Parameters

SIW can be considered as a combination of the best features of microstrip technology and dielectric-filled rectangular waveguide (DFW). Functionally, SIW is similar to a low-height DFW. However, SIW is more compatible with microstrips due to its planarity and same types of production technology. A typical DFW structure is shown in Figure 2.1 (a), where all conductor walls are completely metal and also the height of the waveguide and the operation frequency are identically same with SIW in Figure 2.1 (b).

SIW has entirely metal-coated top and bottom surfaces. However, its lateral walls are established two parallel rows of plated-through (metalized) via holes in a planar substrate. In spite of not having completely closed side walls, the SIW structures do not have any remarkable leakage loss arising from this structural feature. This is achieved by adjusting the diameter and the period of constituent vias of holes that form the side walls. Because of the quasi-rectangular waveguide form of SIW, with the help of periodic metalized via-hole connections between upper and bottom layers, the dominant mode is the TE_{10} mode. Moreover, since the height of the structure is much less than the guided wavelength in the SIW, electromagnetic field is constant along the height of substrate.



(a)



(b)

Figure 2.1: (a) DFW and (b) SIW propagation characteristics

Since SIW devices can be thought as a special form of DFW, the starting point to calculate propagation constant, cut-off frequencies and most critical design parameters of the SIW, is DFW equations. These design parameters are the equivalent SIW width “ a_{SIW} ”, the diameter of vias “ d ” and the period of vias “ p ”.

Generally, width and height of a rectangular waveguide are denoted with “ a ” and “ b ” respectively as shown in Figure 2.2.

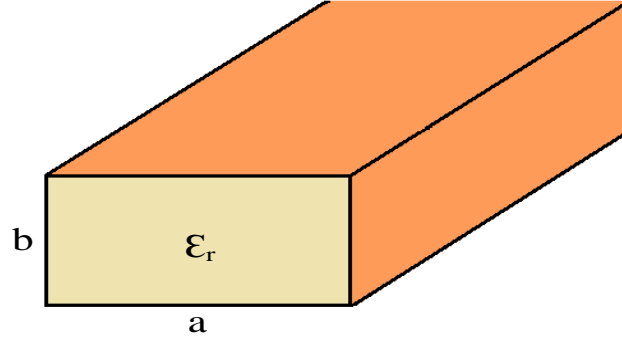


Figure 2.2: Schematic structure and dimensions definition of DFW

In order to identify cut-off frequencies of the DFW for TE_{mn} modes ($m = 0, 1, 2 \dots$ and $n = 0, 1, 2 \dots$) “a” and “b” parameters are utilized. Because of the dominant mode of the SIW (TE_{10}), determination of the SIW cut-off frequency can be simplified [5] as expressed in Equation (2.1):

$$f_{c_{mn}} = \frac{k_c}{2\pi} = \frac{1}{2\pi\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \rightarrow f_{10} = \frac{1}{2a\sqrt{\mu\epsilon}} \quad (2.1)$$

where, “b” is the height of the DFW that is equal to substrate height of SIW. “a” is the width of the DFW that is used for conversion of the equivalent SIW width. In addition, “ k_c ” is cut-off constant, “ ϵ ” and “ μ ” are permittivity and permeability of the planar substrate, respectively.

For TE_{10} mode, since the dimension “b” does not affect the calculation of the waveguide cut-off frequency, the thickness of substrate (“b” or “h”) can have any value. Since the thickness is proportional to the dielectric loss, efficiency decreases with increasing thickness. However, the cost and the precision machining requirement increase in the fabrication of the low thickness substrates.

Another important point, after having determined the dimension “a” of the DFW (is called “ a_{RWG} ”), is determination of the equivalent SIW width (a_{SIW}). In Figure 2.3, “ a_{SIW} ” is the equivalent width of the SIW and “ a_{RWG} ” is the width of the conventional rectangular waveguide, “d” is the diameter and “p” is the period of the identical plated-through (metallized) via holes. Also, the height of substrate is symbolized by “h”.

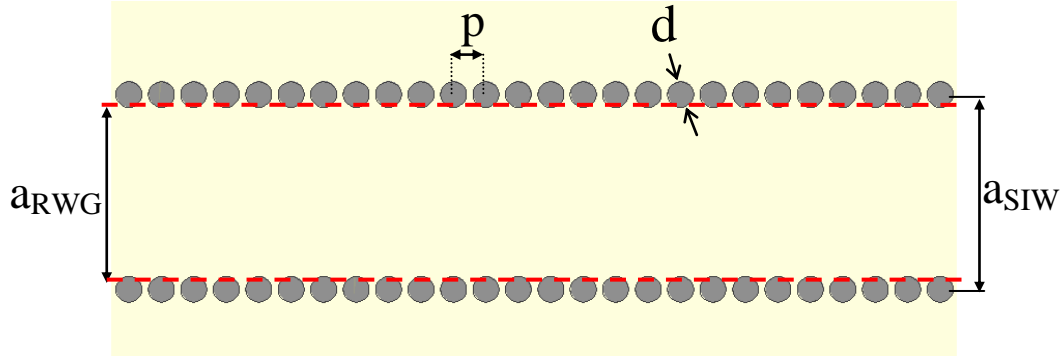


Figure 2.3: Configuration of the SIW synthesized using metallized via-hole arrays

In literature, a number of articles are presented on the definition of design parameters and the modeling of SIW [2], [6]-[13]. Yan et al. published an experimental formula for the normalized width of the equivalent waveguide [6], such that:

$$a_{\text{RWG}} = a_{\text{SIW}} \cdot \bar{a} \quad (2.2)$$

where

$$\bar{a} = \xi_1 + \frac{\xi_2}{\frac{p}{d} + \frac{(\xi_1 + \xi_2 - \xi_3)}{(\xi_3 - \xi_1)}} \quad (2.3)$$

$$\xi_1 = 1.0198 + \frac{0.3465}{\frac{a_{\text{SIW}}}{p} - 1.0684} \quad (2.4)$$

$$\xi_2 = -0.1183 - \frac{1.2729}{\frac{a_{\text{SIW}}}{p} - 1.2010} \quad (2.5)$$

$$\xi_3 = 1.0082 - \frac{0.9163}{\frac{a_{\text{SIW}}}{p} + 0.2152} \quad (2.6)$$

Substantially, Equations (2.2) - (2.6) enable a ratio to be obtained between “ a_{SIW} ” and “ a_{RWG} ”. According to the design requirements, equivalent width of RWG or SIW can be calculated with less than 1% estimated relative error [6].

Another important step of the SIW design is the determination of the via diameter “ d ” and the arrangement period of vias “ p ” parameters. These parameters are crucial for leakage that may occur on the walls. Che et al. [14] published an article containing a brief discussion on leakage and ohmic loss. This study shows that, when period and diameter values of the SIW walls are properly adjusted, the leakage from an SIW is quite less. Leakage loss values of SIW as a function of “ p ” and “ d ” normalized to the cut-off wavelength are given in Figure 2.4 [15].

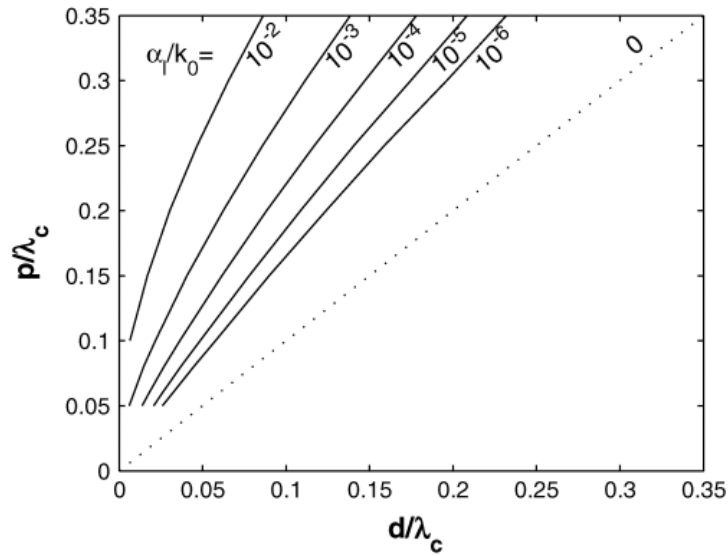


Figure 2.4: Leakage losses varying from 10^{-6} to 10^{-2} Np/rad as functions of the post diameter and period length normalized to the cutoff wavelength [15]

In addition, a plot showing the region of the interest is provided for the design purpose in [15] as shown in Figure 2.5. The effect of the design parameters "d" and "p" values according to the operating frequency can be observed roughly with the help of this graph. Also, the operating frequency band limits that are determined by cut-off frequencies of the propagation modes can change with values of period and diameter. The lower and/or upper frequencies of the frequency band can shift to the leakage, bandgap, over-perforated or unrealizable regions with varying "d" and "p" values. On the other hand, "d" and "p" values are usually constrained parameters. These values are dependent on the manufacturing capabilities. The optimum design parameters can be determined with the help of the graph shown in Figure 2.5 by taking into consideration the available manufacturing tolerances.

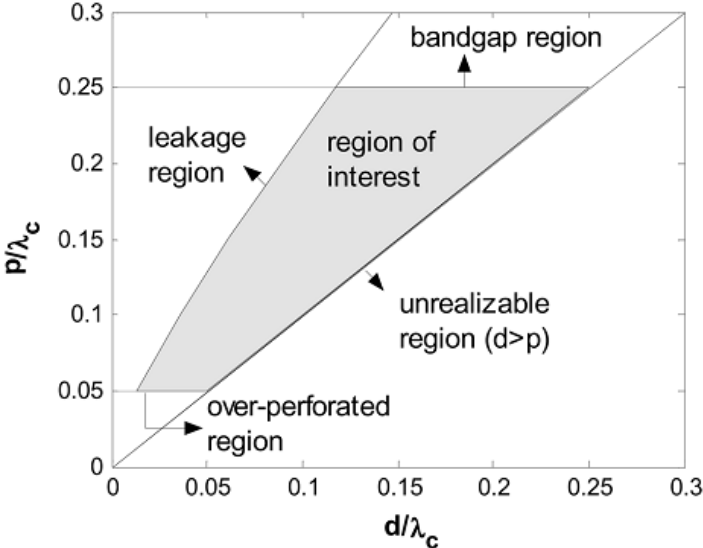


Figure 2.5: Region of interest for the SIW in the plane of d/λ_c and p/λ_c [15]

In this thesis work, the Equations (2.2) - (2.6) have been utilized because of the low relative error and the high accuracy rate obtained from production datas. The design parameters "d" and "p" at 25 GHz operation frequency are determined using this set of equation and by considering the production capability. These parameters are tabulated in Table 2.1.

Table 2.1. The determined SIW design parameters utilized in this thesis

a_{SIW}	a_{RWG}	p	d	f_{c10}	f_{c20}
6 mm	5.3435 mm	1 mm	0.8 mm	16.2 GHz	32.4 GHz

Another one of the most important issues in the design of the SIW is the amount of the losses in structure. Although hollow metallic waveguides are very low loss structures, SIW suffers from dielectric losses as well as leakage through vias. Therefore, careful design is required to reduce the losses.

In SIW, the amount of loss varies with material, design quality and production factors. These factors are regulated according to the acceptance criteria of the design that is determined so as not to impair the function of the structure. The total loss in the structure is defined as the sum of the conductor loss, the dielectric loss and the leakage loss of structure:

$$\alpha_{total} = \alpha_c + \alpha_d + \alpha_l \quad (2.7)$$

Dielectric substrate with low tangent loss ($\tan\delta$) at the operating frequency should be chosen to reduce dielectric losses. Conductor coatings on the dielectric should be thick enough to reduce conductor losses. Besides, substrate choice can be dependent upon physical factors such as; flexibility needs, type and adaptation properties of the structure to be fed, available space, ease of production and testing etc.

In this thesis, the 0.5 mm thick Rogers 3003 ($\epsilon_r = 3$, $\tan\delta = 0.0013 @ 10 \text{ GHz}$) is chosen as a substrate of all the SIW designs. Some of the power dividers designed in this thesis are used to feed a slotted SIW array conformed on a cylinder. So, Rogers 3003 is chosen since it is relatively soft material that can be conformed on nonplanar structures easily. This choice makes a compromise between dielectric losses and flexibility needs in project which partially supports the work carried out in this thesis.

2 Port SIW is designed using Rogers 3003 substrate of thickness 0.5 mm and parameters given in Table 2.1. Ansoft HFSS is used for full EM simulations. The designed structure is shown in Figure 2.6.

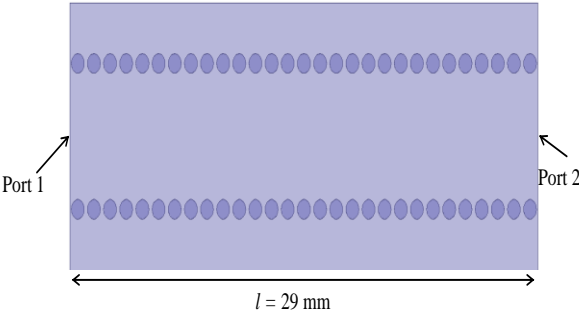


Figure 2.6: The designed 2 Port SIW with determined parameter values

The length of the structure is chosen as approximately equal to double of the guided wavelength at 20 GHz . This frequency is the lower frequency limit (= longest wavelength) of the examined frequency range. The simulation results of insertion loss (S_{21}) and return loss (S_{11}) of the designed 2 Port SIW are shown as in Figure 2.7.

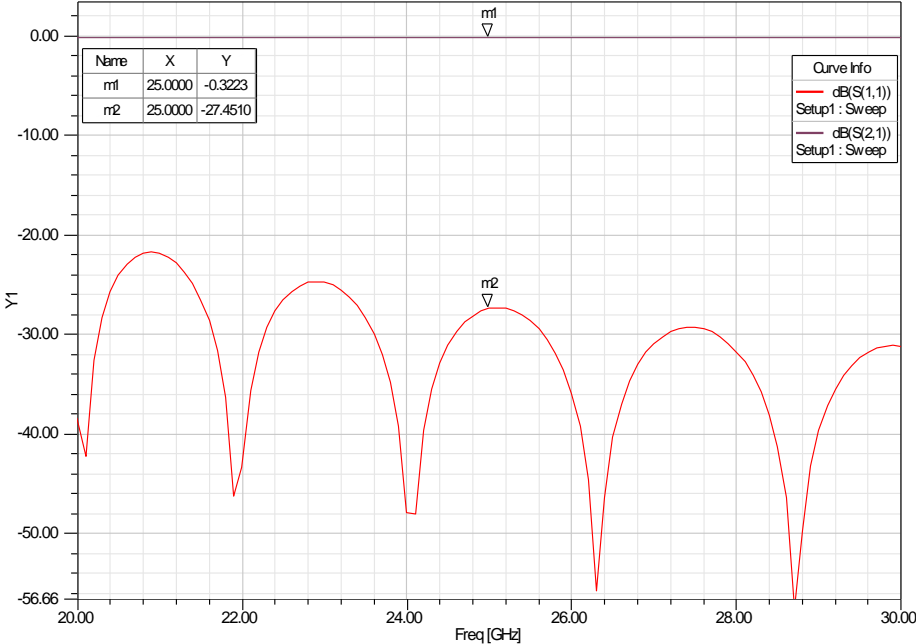


Figure 2.7: The simulation results (S_{21} and S_{11}) of the designed 2 Port SIW

It is seen from Figure 2.7 that considering the dielectric and conductor losses, the insertion loss (S_{21}) is very low (-0.32 dB) between 20 GHz and 30 GHz with determined “p” and “d” values. Also, return loss value (-27 dB) is satisfactory.

2.2. SIW Leakage Analysis

A four port SIW structure is designed with the help of Ansoft HFSS design software to examine the amount of leakage loss on the side walls. The designed structure is illustrated in Figure 2.8.

The leakage loss that occurs due to discontinuous side walls is examined with this structure. The structure is fed from Port 1 and S_{21} , S_{31} ve S_{41} values are obtained between 20 to 30 GHz.

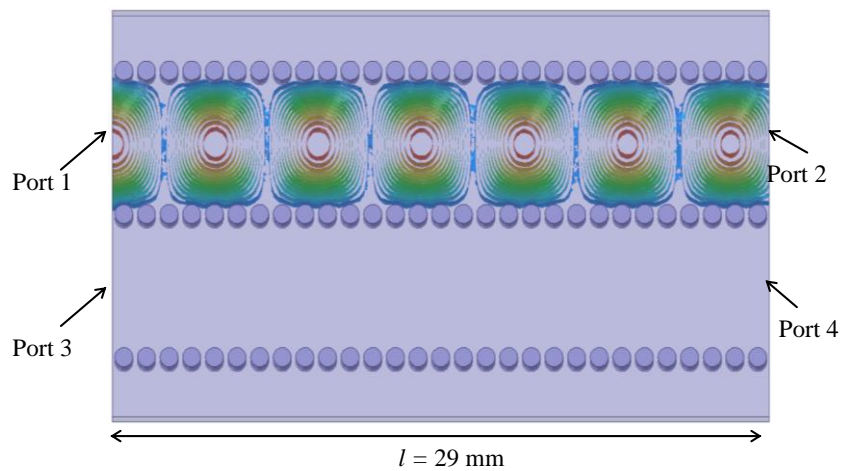


Figure 2.8: 4 Port SIW structure designed for Leakage Analyze

The results of insertion loss (S_{21}) and leakage loss (S_{41}) are shown in Figure 2.9, where as isolation (S_{31}) is plotted in Figure 2.10.

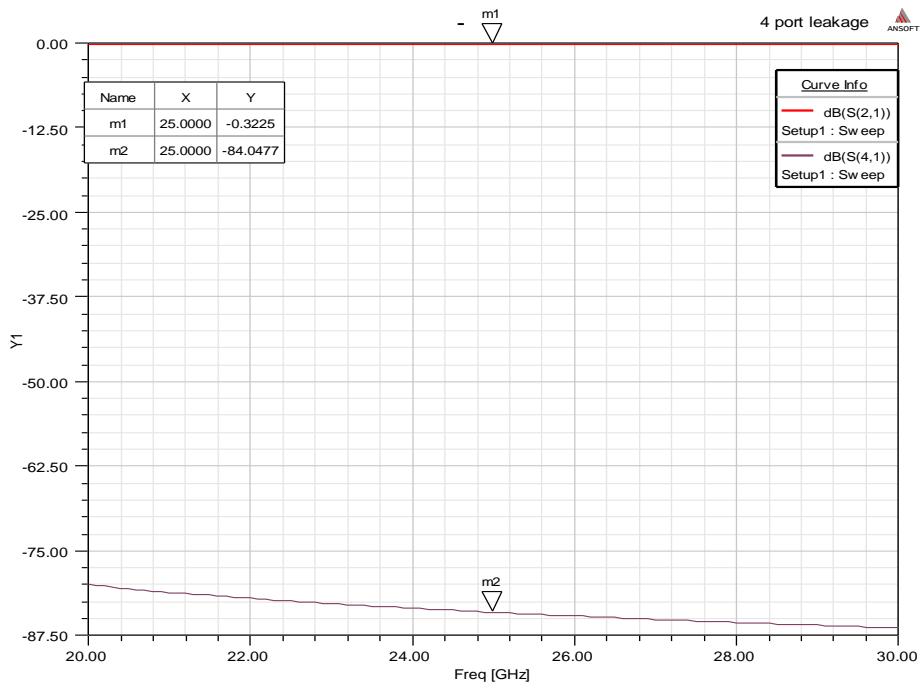


Figure 2.9: The results of insertion loss (S_{21}) and leakage loss (S_{41}) of the 4 Port SIW structure

As it is seen from Figure 2.9, the insertion loss (S_{21}) of the 4 Port SIW structure is very low (-0.32 dB) considering the dielectric and conductor losses with determined “p” and “d” at 25 GHz . Also, almost no leakage loss (S_{41}) is observed in this frequency band.

As can be seen from Figure 2.10, the amount of interaction between the adjacent ports (S_{31}) is extremely low between 20 GHz and 30 GHz . It can be said that Port 1 and Port 2 are almost completely isolated from each other.

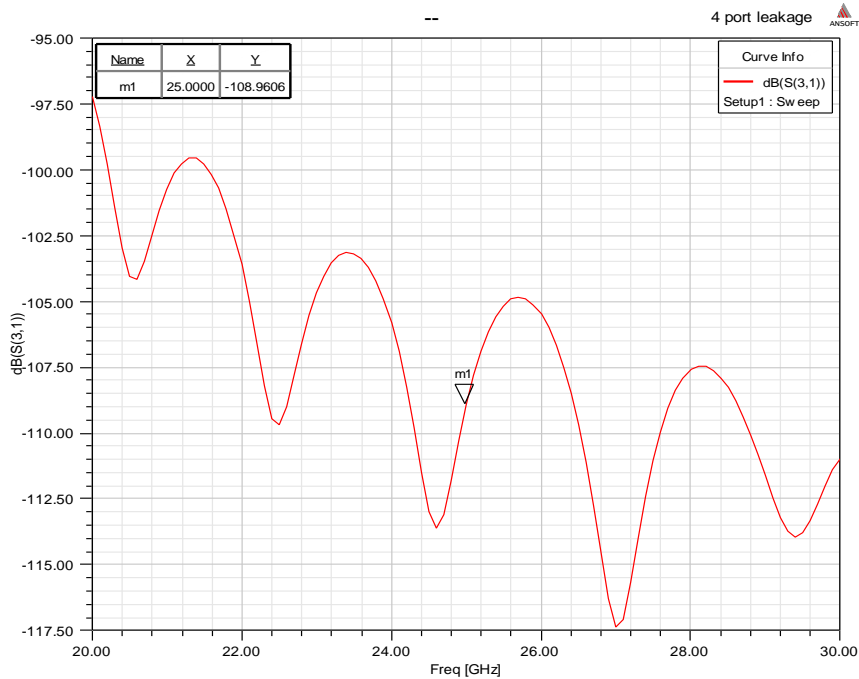


Figure 2.10: The quality of the isolation between adjacent ports (S_{31}) of the 4 Port SIW structure

2.3. SIW Feeding Types

One of the most important considerations in the design of SIW is the feeding section of the structure. Many methods and topologies on feeding types of SIW structures are investigated in the literature. These methods can be classified as; Microstrip, Coplanar Waveguide (CPWG), Probe and Rectangular Waveguide (RWG) feeding structures.

Microstrip transition structures are the most commonly used structures in the SIW feeding systems. These structures are very handy in terms of design and production and providing wide frequency band. One of the most important factors in the choice of the microstrip line for feeding is that SIW and microstrip transition structure can be entirely combined on the same substrate without requiring any mechanical assembly. Microstrip feeding structures are commonly and effectively used in SIW

structures which have low thickness. The characteristic impedances of SIW and microstrip transition have more coherence for substrates with small thickness. The basic view of microstrip feeding structure is shown in Figure 2.11. There are many examples that are designed with microstrip transition feeding in the literature [6], [16]-[23].

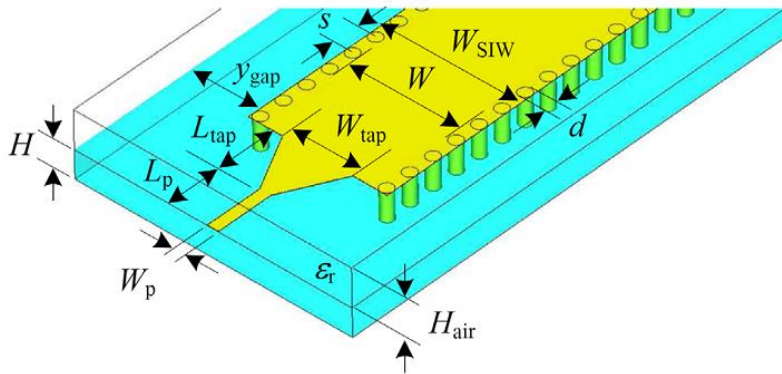


Figure 2.11: Microstrip feeding structure [23]

Another type of feeding structure which is implemented in SIW feeding operation is CPWG. In general, both in microstrip and CPWG, E-field and H-field coupling depend on the substrate thickness of SIW. However, CPWG feedings are more convenient for the SIW structures that are designed with a thick substrate. This is because the characteristic impedance of CPWG is almost independent of substrate thickness. CPW-SIW conformance is better than microstrip feeding for the SIW which is designed with a thick substrate. Tapered coupling slot structures are utilized in CPWG feeding structures to exactly match the port impedance of CPWG with the characteristic impedance of SIW. Because of all these advantages and ease of manufacture, CPWG feeding structures are used in the feeding of SIW structure frequently [24]-[29]. The schematic representation of CPWG feeding structure is shown in Figure 2.12.

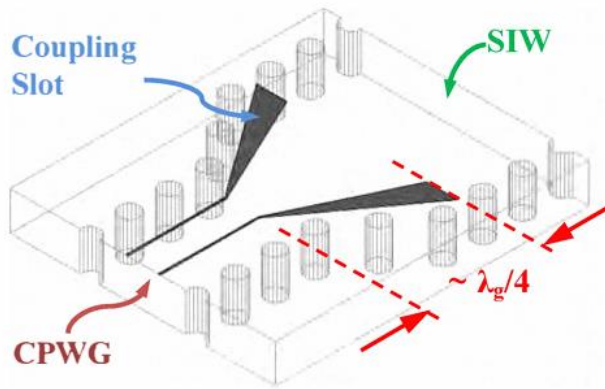
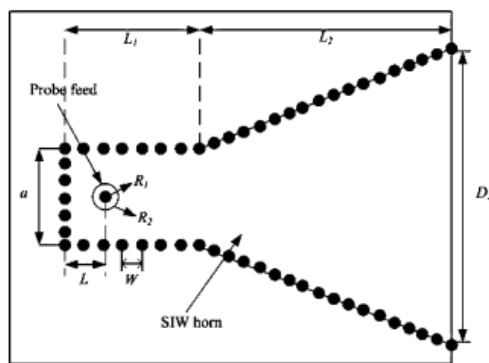


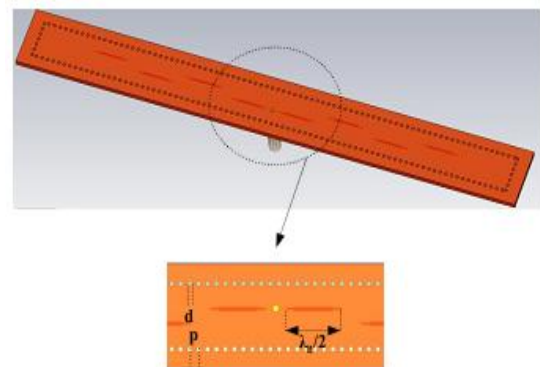
Figure 2.12: CPWG feeding structure [24]

Another type of feeding structures used in literature is probe feeding [30]-[33]. SIW structures can also be fed from underneath via a probe. The ground conductor of connector is connected to the bottom surface of the SIW and the center conductor of connector is extended up to top layer. According to the requirement of the design, location of probe feeding can be altered as shown in Figure 2.13.



(a)

Aside located probe feeding structure
[31]



(b)

Centrally located probe feeding structure
[32]

Figure 2.13: Probe feeding structure and different location types

RWG is also used to feed SIW structures [34], [35]. These structures are bulky in terms of design and production. They are generally used in narrow frequency band applications. RWG feeding structures can feed SIW structures by means of a slot which is etched on the surface of SIW. This slot couples the energy between SIW and RWG. The schematic representation of RWG feeding structure is seen in Figure 2.14.

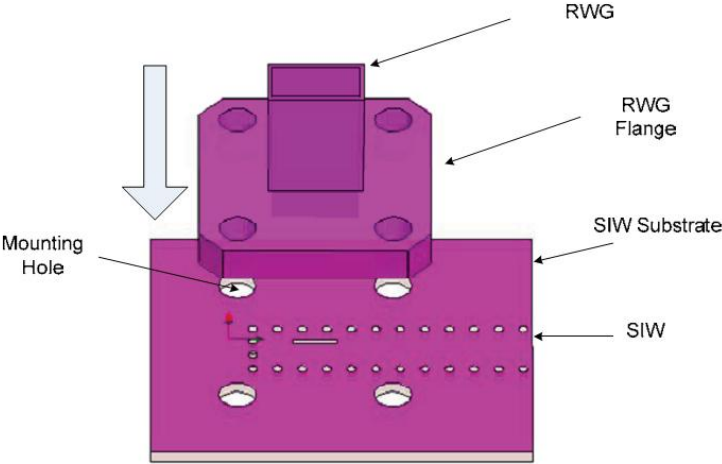


Figure 2.14: RWG feeding structure [34]

Additionally, the slot that etched on the surface of SIW can also be used to transfer the power between two SIW structures with the help of bilateral located slots on each side. First, SIW structure can be fed by any feeding type and the power is transmitted to etched slot. The other SIW part that has identically same slot is attached to with first SIW part as slots completely overlap to couple the energy between them [36].

2.4. Microstrip to SIW Transitions

Microstrip to SIW transitions are very critical structures for complete integration of the SIW components with off-board devices. SIW structures must be interconnected with planar structures in order to perform the measurement of S-parameters via

mounting SMA connectors. Likewise, in case of combined usage of the SIW with off-board devices, microstrip transitions and SMA connectors assume the role of the interface between them. Besides, port impedance of the structure can be adjusted to the 50Ω with the help of a low reflection tapered transition section between the 50Ω microstrip transmission line and the SIW. By the way, port impedance of the device can be set to a desired value regardless of the impedance of the SIW section. The tapered microstrip transitions have been widely used for several reasons. One of them is that the transitions are usable for almost the entire bandwidth of the SIW. Furthermore, the transition losses are quite low due to the fact that electromagnetic field characteristics in the microstrip and SIW match very well.

Since the microstrip transmission line consists of a thin conducting strip separated from a ground plane by a dielectric layer, the electric field propagates through not only the substrate but also the air section that is above the substrate as seen in Figure 2.15 (b).

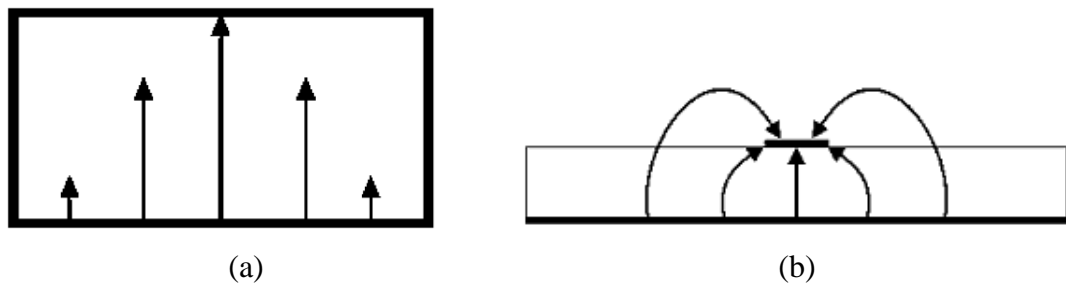


Figure 2.15: Dominant mode electrical field distributions in
 (a) Rectangular Waveguide (b) Microstrip Transmission Line [3]

Under these structural conditions, the microstrip transmission line can be said to propagate a quasi-TEM mod compared to a pure transverse electromagnetic (TEM) line, such as a stripline. Therefore, an electromagnetic mode conversion is required to provide transmission of signals from the planar TEM, or quasi-TEM transmission line to the guided waveguide mode (or vice versa) in order to interconnect waveguides to planar transmission lines. Furthermore, in order to provide a low-

reflection transition between these structures, the wave impedance that varies with changes in frequency must be simultaneously matched to the characteristic impedance of the planar transmission lines. The wave impedance of an electromagnetic wave is described as the ratio of the transverse components of the electric and magnetic fields of the waveguide for TE_n modes [37].

A single layer transition from microstrip line to a SIW with a tapered microstrip line section has been proposed in [3]. The authors report a measured return loss between $10\text{-}50\text{ dB}$ over a 6 GHz bandwidth and insertion losses as low as 0.1 dB in both simulation and measurement. The width of the narrow transmission line is gradually increased from W_m to W_t as shown in Figure 2.16 and this structure is named as “tapered microstrip line section”. The principal tasks of the tapered microstrip line section are mode and impedance matching between $50\ \Omega$ transmission line and the SIW. The quasi-TEM mode of the microstrip line is transformed into the TE_{10} mode in the waveguide and the wave impedance that varies with changes in frequency is simultaneously matched with the characteristic impedance of the planar transmission lines regardless of the changes in frequency and the port impedance of the SIW section. As can be seen in Figure 2.16, SIW and a transition structure are entirely combined on the same substrate without requiring any mechanical assembly.

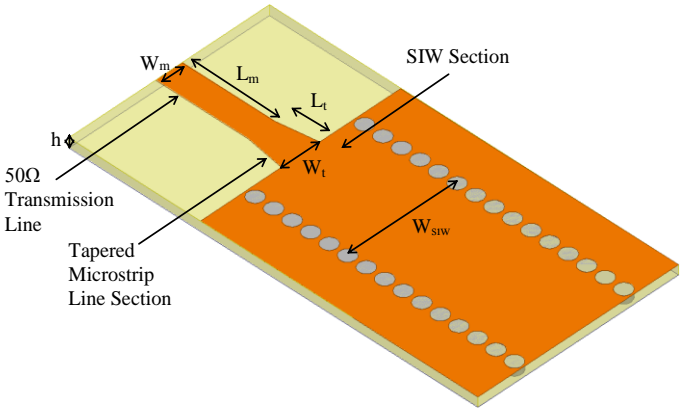


Figure 2.16: Configuration of Microstrip to SIW transition

Design steps of the structure seen in Figure 2.16 are not laborious and do not require too complex calculations. Also, a great number of commercial or free calculation software and website dedicated to facilitate many of these steps can be found effortlessly. Firstly, a $50\ \Omega$ microstrip transmission line is designed by considering the dielectric properties of substrate which is used in the process and RWG dimensions are determined by waveguide theory. In this manner, “ W_m ”, “ L_m ” and W_{RWG} are determined. Then, length “ L_t ” and width “ W_t ” of the tapered microstrip line section should be determined. To accomplish this, the most widely used method is modeling and optimization in any relevant commercial software over the required frequency range and bandwidth. However, this way may not be an efficient way at all time. Because of the rising number of plated-through (metalized) via holes can be complicated meshing-solving process and increase the time consumed. In such an unlikely situation, analytical equation can be used and parameter determination process would be accelerated. The analytical design equations for a low reflection tapered transition section have been reported by Deslandes in [38]. In this study, the microstrip transmission line is modeled by an equivalent transverse electromagnetic (TEM) waveguide as shown in Figure 2.17.

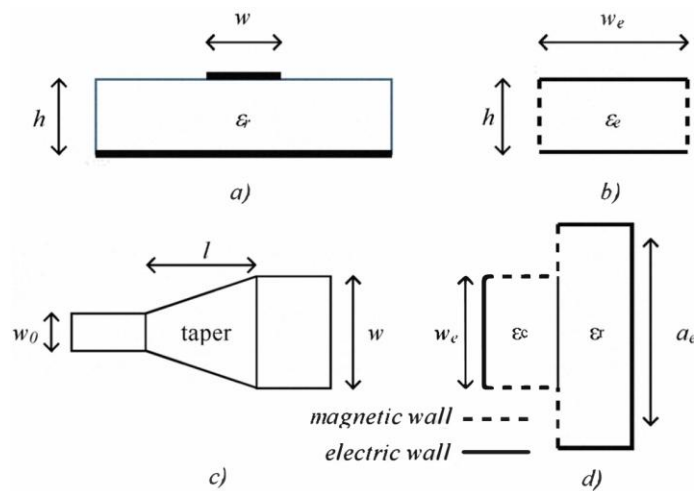


Figure 2.17: Equivalent topology for the microstrip-to-SIW transition: (a) microstrip line, (b) waveguide model of a microstrip line, (c) top view of the microstrip taper, (d) microstrip-to-SIW step [38].

By using a curve fitting technique, an equation that relates optimum microstrip width to the SIW width is derived. Wherefore magnetic walls are used as walls of the SIW, the capacitance effects at the end of the SIW in the transition plane are ignored. In order to reduce the return loss as much as possible, tapered transition section length “ L ” must be chosen as a multiple of a quarter of a wavelength. According to this study, these set of equations provide a return loss superior to -20 dB between 18 GHz and 75 GHz frequency bands and cover the complete single-mode SIW bandwidth.

As shown in Figure 2.18, the transition structure used in thesis work is assessed by a structure consisting of three parts which are $50\ \Omega$ microstrip transmission line section, tapered microstrip line section and SIW section as mentioned in the design steps. All sections are designed and fabricated on same substrate with mentioned design parameters in Table 2.1.

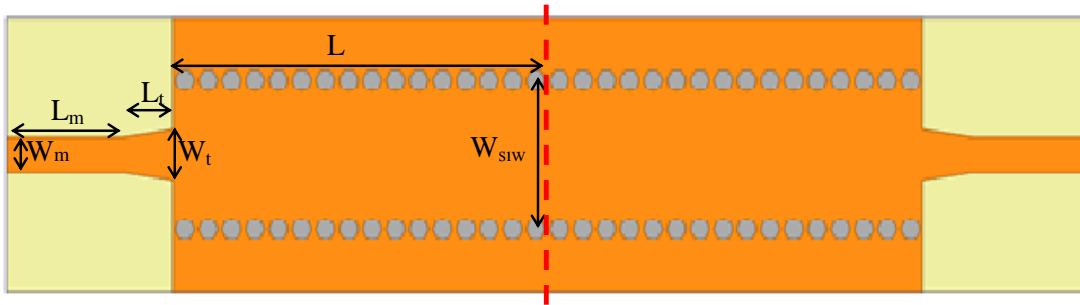


Figure 2.18: Top view of designed Microstrip to SIW transition structure

$50\ \Omega$ microstrip transmission line sections are designed to work properly at the operating frequency (25 GHz) by taking into consideration the microstrip line theory. Its dimensions are determined as width $W_m = 1.25\text{ mm}$ and length $L_m = 7.5\text{ mm}$. The tapered microstrip line section has equal width with microstrip line section at the connection point of them. However, the width of tapered section gradually increased from W_m to $W_t = 2.1\text{ mm}$ until the connection point with SIW. The length of tapered section and the SIW section are set to be $L_t = 2.1\text{ mm}$ and $L = 10\text{ mm}$ respectively.

To characterize the transition, two microstrip to SIW transitions are connected back to back as shown in Figure 2.18. However, the additive components that are not taken into account in the design like connectors can affect the results at rate that cannot be fully estimated. Therefore, connectors are added to designed structure in Figure 2.18 and simulation is repeated in order to figure out the behavior of the structure as close to reality as possible. By this means, the practical effects of the connectors can also be seen in the studied frequency band. The transition structure with depicted connectors is designed as shown in Figure 2.19. The connectors used in the measurements are the product of Southwest Microwave, Inc.

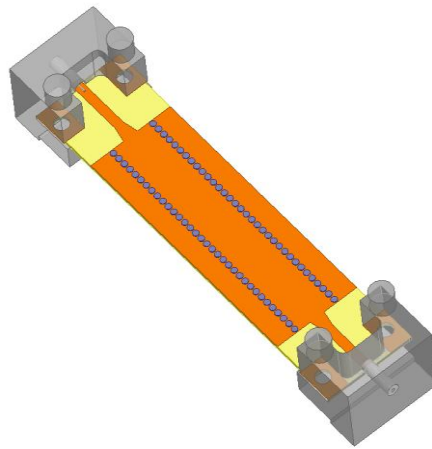


Figure 2.19: Designed Microstrip to SIW transition structure with depicted connectors

The all structures produced in this thesis except 1 x 8 power divider, 8 x 1 and 8 x 4 slotted SIW antennas are fabricated using electroplating and PCB manufacturing tools in the Microwave and Millimeter Wave Research Laboratory of METU Electrical and Electronics Engineering Department.

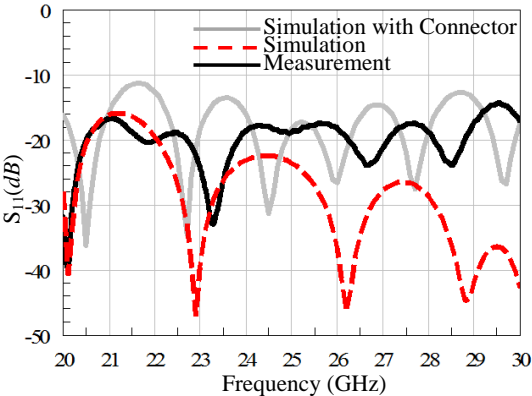
Firstly, the substrate that has copper cladding on both sides is drilled as designed. Then, the substrate is electroplated and the internal walls of the drilled via holes are

coated with copper. Finally, milling of the microstrip lines and cutting of the devices outlines are carried out by using PCB process.

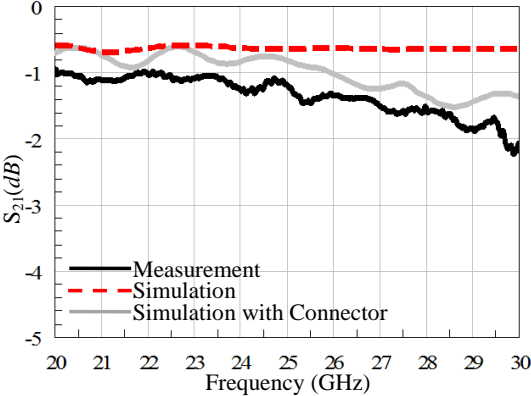
A photograph of manufactured transition structure is given in Figure 2.20 (a). Measured S-parameters are shown in Figure 2.20: (b) and Figure 2.20 (c). There is a reasonable agreement between results of the simulations and the measurements. Additionally, the measurement results show that the manufactured microstrip to SIW transition is very suitable for using between 20 GHz and 30 GHz frequency band.



(a)



(b)



(c)

Figure 2.20: Microstrip to SIW transition

(a) Photograph of the production

(b) Return Loss (S_{11}) measurement and simulations comparison

(c) Insertion Loss (S_{21}) measurement and simulations comparison

Particularly, when the results of simulation with connector are taken into consideration, measured return loss (S_{11}) is lower than -10 dB and measured insertion

loss (S_{21}) is higher than -1.5 dB in this frequency range. At 25 GHz that is the design and the operating frequency of the structure, measurement and simulation with connector results are very close. The simulation with connector insertion loss (S_{21}) result is about 0.8 dB while the measured insertion loss is about 1.2 dB and the difference between the measured and simulated results is just about 0.4 dB.

This difference may stem from the calculation of the copper and tangent losses that cannot be expected as accurate as reality by the simulation program.

In the scope of this production, Thru-Reflect-Line (TRL) calibration work has been tried to remove the effect of the transitions and connectors on the SIW. However, it could not be carried out due to the problems experienced in fabrication and measurement at 25 GHz about repeatability and standardization of devices.

CHAPTER 3

SUBSTRATE INTEGRATED WAVEGUIDE POWER DIVIDERS

3.1. Introduction to Power Dividers

Power dividers are passive devices used to divide the power that is applied at the input port, equally or unequally. The number of output ports of the divider can be two or more in accordance with the number of the structures that is needed to be fed by the power divider. The schematic diagram of 1 x N power divider is shown in Figure 3.1.

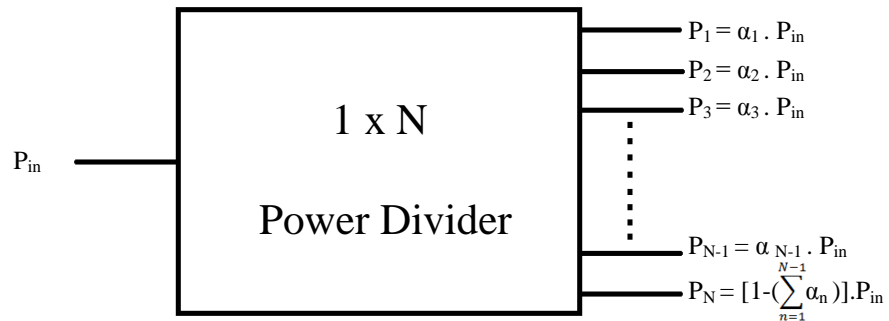


Figure 3.1: Schematic diagram of the lossless 1 x N power divider

As seen in Figure 3.1, the input power is divided into N part according to “ α ” values. The sum of the power at the output ports is equal to the input power in the lossless structure. 1 x N power dividers are N+1 port devices and the scattering matrix of an arbitrary N+1 port network is given in Equation (3.1).

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \bullet & S_{1N+1} \\ S_{21} & S_{22} & S_{23} & \bullet & S_{2N+1} \\ S_{31} & S_{32} & S_{33} & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet \\ S_{N+1\ 1} & S_{N+1\ 2} & \bullet & \bullet & S_{N+1\ N+1} \end{bmatrix} \quad (3.1)$$

The scattering matrix which is also known as S matrix is utilized to obtain voltage waves ratio between incident (V^+) and reflected (V^-) voltage waves considering both of magnitude and phase terms. This relation can be written as;

$$[V^-] = [S] [V^+] \quad (3.2)$$

By means of these equations, each element of the scattering matrix can be described as a function of reflected and incident voltage. The general form of this description can be expressed when the structure is solely excited from the j'th port and reflected voltage measured at i'th port. It can be written as;

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ = 0, k \neq j} \quad (3.3)$$

When structure fed from j'th port of device, incident voltages at the other ports are set to zero and all output ports are terminated with match load except port i. Thus, the amount of reflection of the i'th port can be obtained without the influence of the other terminals.

As long as the device does not contain any anisotropic materials, its scattering matrix must be reciprocal and symmetric ($S_{ij}=S_{ji}$). Generally, a three-port lossless reciprocal network cannot be matched at all ports ($S_{ii} = 0$).

The scattering matrix of a lossless junction is a unitary matrix. The unitary property can be expressed in Equation (3.4) and (3.5) [39].

$$\sum_{i=1}^{N+1} |S_{ij}|^2 = 1 \quad (3.4)$$

$$\sum_{i=1}^{N+1} S_{ki} S_{kj}^* = 0 \quad i \neq j \quad (3.5)$$

The basic power dividers are 1 x 2 power dividers (three-port structures) that are used to divide the power in equal ratios. The half of the input power (-3 dB) is delivered to each of the two output ports by means of these structures. In the opposite manner, if structure is fed from two ports, it works as a combiner due to the reciprocal nature of the structure. The power division and combining representation of three-port structures is shown in Figure 3.2.

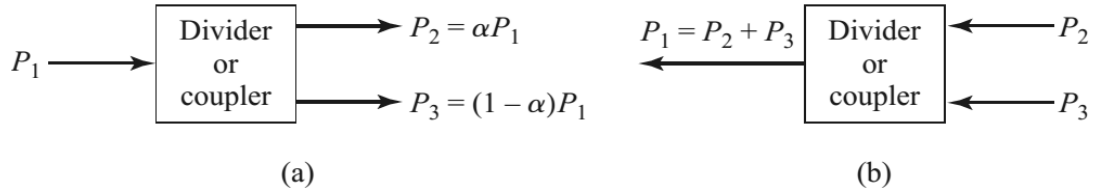


Figure 3.2: Power division and combining
(a) Power division, (b) Power combining [37]

As mentioned before, if the device is passive, reciprocal and all ports are matched, its scattering matrix must satisfy $S_{ij} = S_{ji}$ and $S_{ii} = 0$ properties [37].

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & 0 \end{bmatrix} \quad (3.6)$$

If the network is also lossless, then energy conservation requires that the scattering matrix satisfy the following conditions [37];

$$|S_{12}|^2 + |S_{13}|^2 = 1 \quad (3.7)$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \quad (3.8)$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \quad (3.9)$$

$$S_{13}^* S_{23} = 0 \quad (3.10)$$

$$S_{23}^* S_{12} = 0 \quad (3.11)$$

$$S_{12}^* S_{13} = 0 \quad (3.12)$$

According to Equations (3.10) - (3.12), it is indicated that minimum two of the three parameters (S_{12} , S_{13} , S_{23}) must be zero. But this condition is inconsistent with one of Equations (3.7) - (3.9) in any case, implying that a three-port network cannot be lossless, reciprocal and matched all ports. The realizable devices can be possible, when any one of these three conditions is released [37]. A three-port junction is depicted in Figure 3.3.

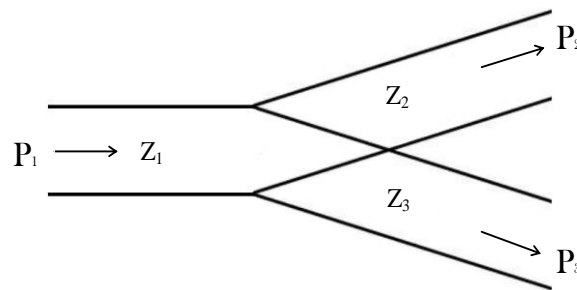


Figure 3.3: A lossless three-port junction used as a power divider [39]

To achieve a lossless three-port junction to divide the input power P_1 into two, the conditions below must be satisfied;

- $\alpha P_1 = P_2$
- $(1 - \alpha) P_1 = P_3$

for Ports 2 and 3, this is readily accomplished [39]. If the input port is matched, the input power is described as;

$$P_1 = \frac{1}{2} Y_1 |V_1^+|^2 \quad (3.13)$$

Due to the parallel connection of all three lines, it can be said that;

$$V_2^- = V_3^- = V_1^+ \quad (3.14)$$

and Equation (3.13) can be updated as;

$$P_1 = \frac{1}{2} Y_2 |V_1^+|^2 + \frac{1}{2} Y_3 |V_1^+|^2 \quad (3.15)$$

For impedance matching, it requires $Y_1 = Y_2 + Y_3$ and in order to obtain the arbitrary power division, it must satisfy;

$$\frac{Y_2}{Y_3} = \frac{\alpha}{1 - \alpha} \quad (3.16)$$

The output ports of this lossless type power divider cannot be matched. Since S_{23} will not be equal to zero, full isolation between the output ports is not possible. However, it can be achieved by locating shunt susceptance at the junction, which will result in excitation of evanescent mode in a waveguide T or Y junction. The input port can also be matched by locating a proper shunt-compensating susceptance at the suitable position in the input line. Thus, S_{23} can be equal to zero and neither reflected power at Port 2 couple into Port 3 nor reflected power at Port 3 couple into Port 2 [39].

3.2. The Comparison of SIW and Other Power Divider Types

The behavior of the power dividers can vary with respect to design conditions even though the basic power divider theory is the same for all power divider types. The design conditions can be dependent upon factors such as; operating frequency, flexibility needs, type and adaptation properties of the structure to be fed, available space, ease of production and testing etc. These conditions may impose restrictions and can influence the selection process of the power divider type to be used. The most commonly used type of power divider structures in microwave and millimeter-wave systems are waveguide, microstrip and SIW power dividers.

To compare the performance of the SIW power divider with the other power divider types, the mentioned three types of power divider structures have been designed, simulated using the T-Junction configuration with the help of the Ansoft HFSS desing program. Their performances are compared at the operating frequency (25 GHz) in this section.

Waveguide power dividers are commonly used to perform low insertion losses, high power handling capacities, high-Q devices that are designed for use in especially the microwave and millimeter wave bands. However, they have a large size, high cost and require high precision machining. Waveguide power dividers are not suitable for trial purposes production for research and development. This type of power dividers are difficult to be produced by mass production techniques and to apply post fabrication tuning. The waveguide power dividers are inflexible. The integration of waveguide components with planar circuits require bulky and lossy transitions. These transitions commonly require a mechanical integration which is very sophisticated and expensive to perform at millimeter-wave frequencies.

As shown in Figure 3.4, 1 x 2 air-filled rectangular waveguide power divider that has T-Junction configuration is designed in order to observe the behavior of the

waveguide power dividers at 25 GHz . The walls of air-filled rectangular waveguide power divider are chosen as copper. The recess that is seen in the waveguide power divider structure shown in Figure 3.4 is referred to as “iris”. Iris has inductive effect in the system during the operation. The location of iris acts on the power transfer rate of the arms. When it is placed at the middle of the structure symmetrically, the input power is divided in half and transmitted to each of the output arms. The shifting in the iris location rightwardly or leftwardly results in unequal power division.

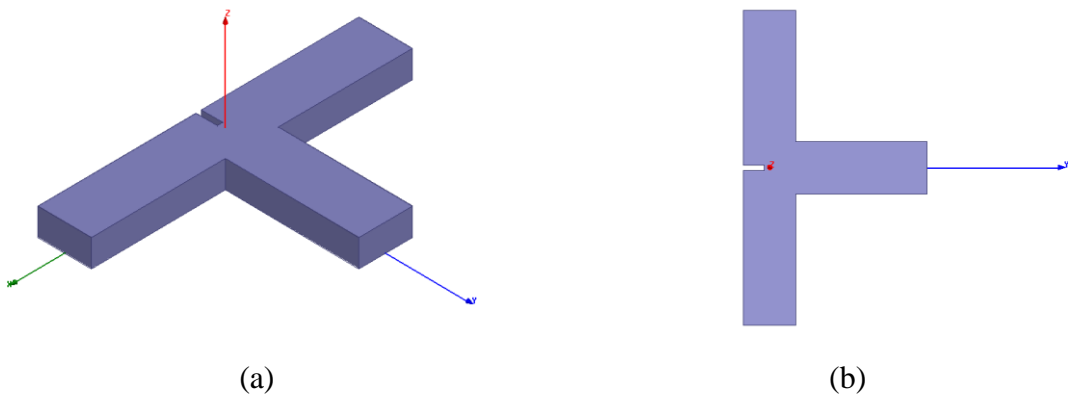


Figure 3.4: 1 x 2 Air-filled rectangular waveguide power divider
(a) Crosswise view (b) Top view

Insertion loss (S_{21} and S_{31}) and return loss (S_{11}) of the designed rectangular waveguide divider are shown in Figure 3.5.

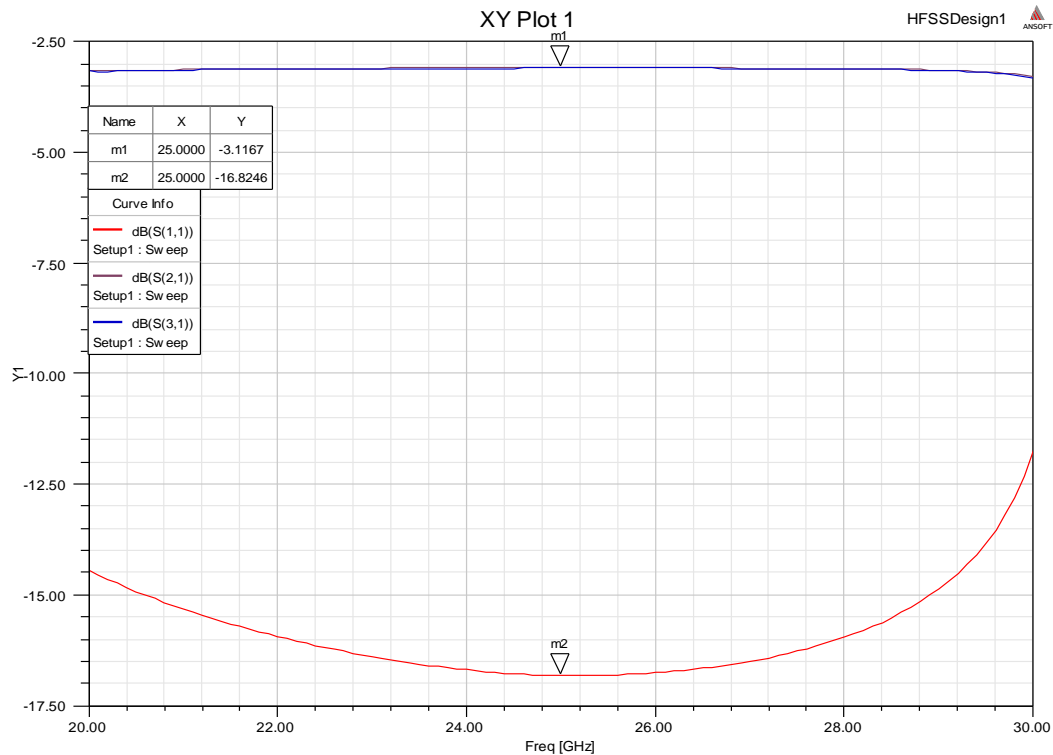


Figure 3.5: 1 x 2 Air-filled rectangular waveguide power divider results

As can be seen from Figure 3.5, insertion loss values (S_{21} and S_{31}) almost completely overlap in 20 - 30 GHz frequency band. The S_{21} and S_{31} values approximately equal to -3.12 dB. The insertion loss values are very close to the theoretical quotient value (-3 dB) despite the copper losses at 25 GHz. Furthermore, the return loss value is very suitable for use at the operating frequency.

Microstrip dividers are built on planar substrates and have quite different characteristics from waveguide power dividers. Microstrip power dividers have high ohmic, insertion and return losses at higher frequencies. Unlike the other two types of power divider, microstrip power dividers have mutual coupling problem between microstrip lines. On the other hand, their low cost, low size, flexibility and ease of manufacturing make them common in many printed circuit board (PCB) designs such as the feeding of microstrip antenna array. Also, the microstrip power dividers do not need any transition structures to unite with other planar structures. In addition,

production of these structures is relatively fast and inexpensive and hence, it is suitable for trial purposes production for research and development.

An 1 x 2 T-Junction microstrip power divider is designed to examine the behavior at 25 GHz as seen in Figure 3.6.

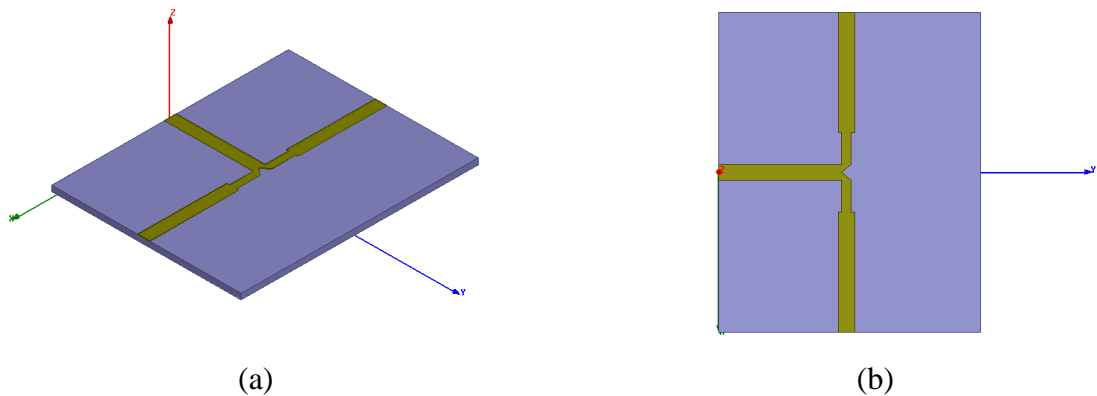


Figure 3.6: 1 x 2 T-Junction microstrip power divider

(a) Crosswise view (b) Top view

Impedances of the lines extending to the divider ports seen in Figure 3.6 are designed with equal port impedance as $50\ \Omega$ to minimize the return loss. In the standard design of a 1 x 2 T-junction microstrip power divider, $50\ \Omega$ input line is connected to two parallel output lines that have $100\ \Omega$ impedance value to provide the impedance compliance and the full bisection. To change the impedance $\lambda/4$ ($70.7\ \Omega$) transition lines are used. Also, 45° bending structures are utilized in order to divide the input power into branches with minimal power loss as an iris.

Insertion loss (S_{21} and S_{31}) and return loss (S_{11}) of the designed microstrip power divider are plotted on Figure 3.7.

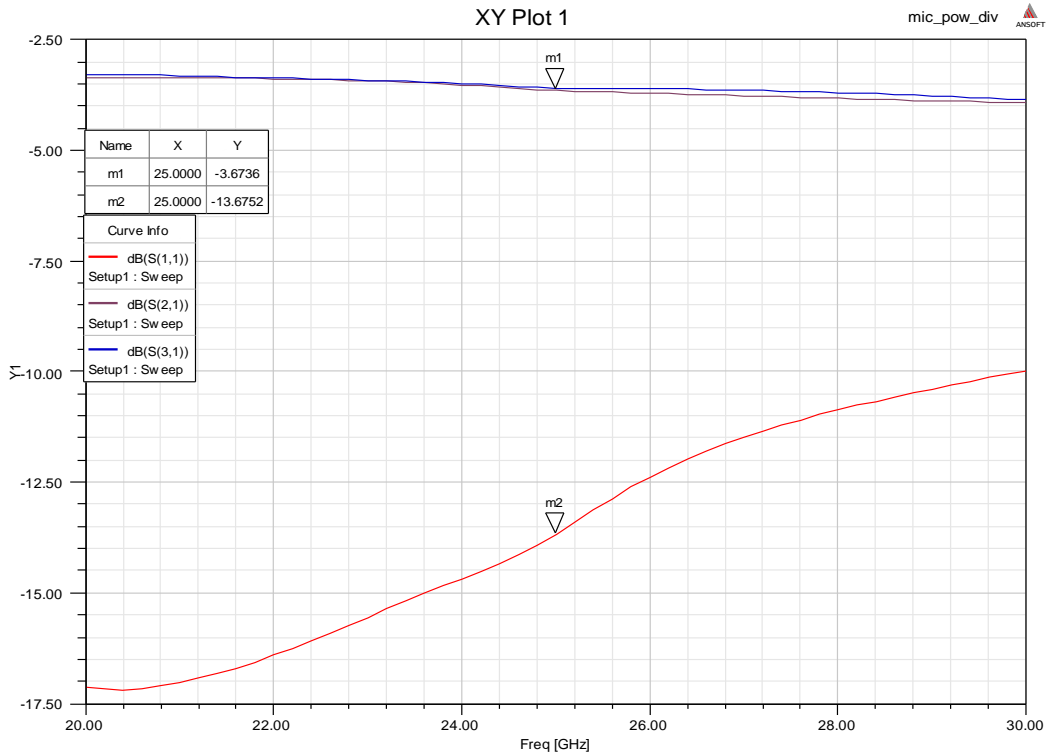


Figure 3.7: 1 x 2 Microstrip power divider results

As can be seen in Figure 3.7, S_{21} and S_{31} are close to each other. The S_{21} and S_{31} values approximately equals to -3.67 dB at 25 GHz . The return loss (S_{11}) approximately equals to -13.67 dB . When comparing the results of the first two power divider types, it can be said that the insertion and return loss levels of microstrip power divider are worse than rectangular waveguide power divider loss levels. This results are reasonable due to the fact that microstrip power divider has dielectric, copper and radiation losses different from rectangular waveguide power divider.

The SIW power dividers come to the fore with low insertion and return loss as well as low cost, high Q-factor and reduced size. Also, transitions are designed on the same substrate with power divider like microstrip power divider, thus transition loss is eliminated considerably. In this way, power divider can be integrated to planar circuits even in a substrate and hence, reduces size, weight and greatly improves

producing repeatability. Moreover, the SIW power dividers can be fabricated as a printed circuit board assembly without the coupling effect.

The designed SIW power divider is shown in Figure 3.8. The mission of the center via that is located at middle of the power divider as seen in Figure 3.8 (a) is similar to iris structure of RWG power divider that is seen in Figure 3.4 (a). So, the design of SIW power dividers is similar to RWG power dividers. However, the physical conditions and the manufacturing process of SIW are like the microstrip waveguide power divider. SIW power dividers are constituted to benefit from the advantages of both RWG and microstrip power dividers but, have received its fair share of their disadvantages even a small amount.

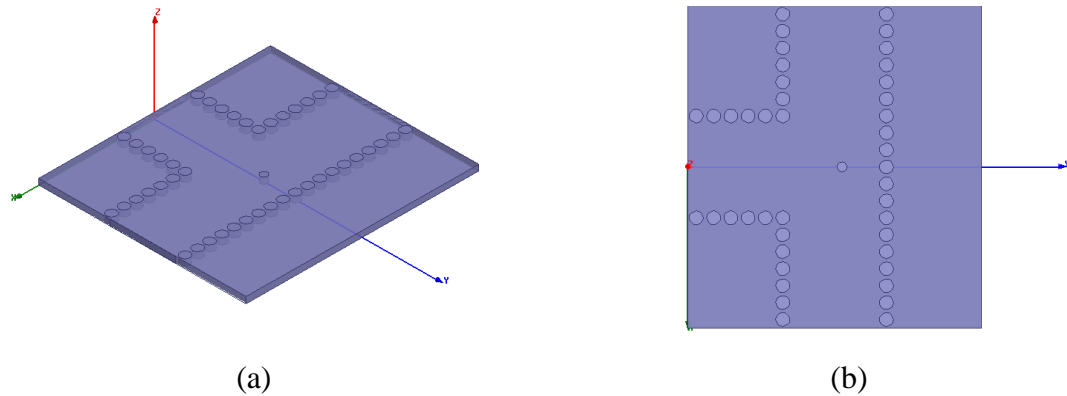


Figure 3.8: 1 x 2 T-Junction SIW power divider

(a) Crosswise view (b) Top view

The period and diameter of the metalized via hole in outer walls are 1 mm and 0.8 mm respectively. The diameter of the center via approximately equals to 0.6 mm . It is placed symmetrically to the “x axis” and its distance from Port 1 is approximately equal to 0.9 mm . The metalized via holes, top and bottom surfaces of substrate are taken as copper. The graph that contains insertion losses (S_{21} and S_{31}) and return loss (S_{11}) of the designed SIW power divider is shown in Figure 3.9.

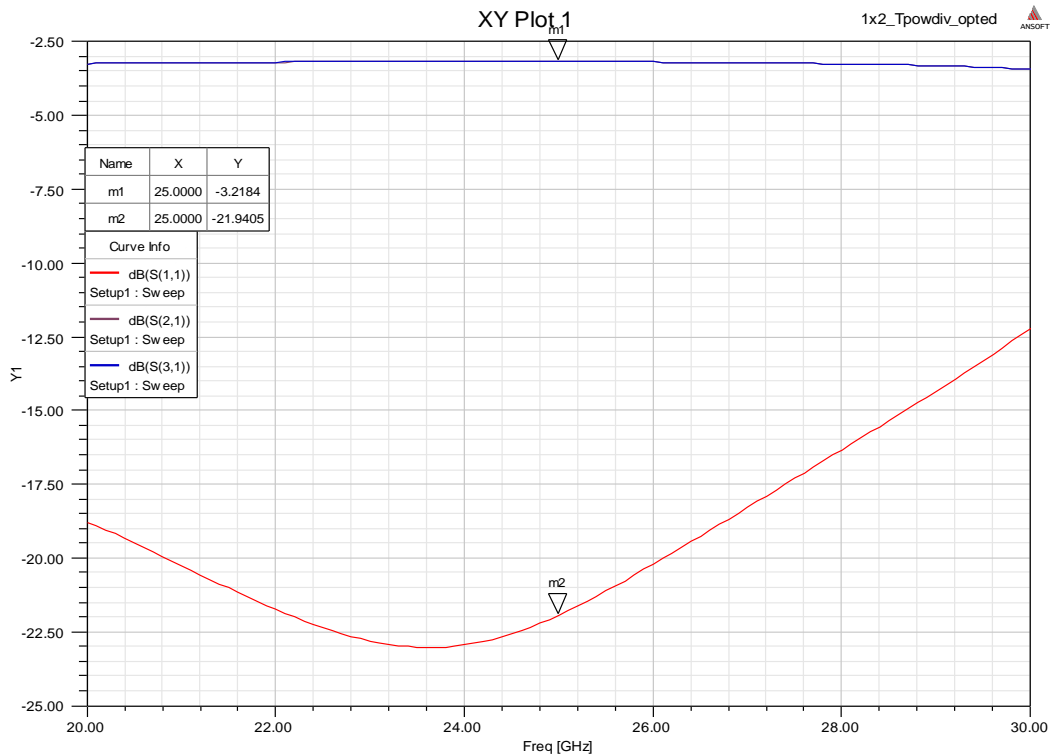


Figure 3.9: 1 x 2 SIW power divider results

As can be seen from Figure 3.9, S_{21} and S_{31} are almost completely overlap in 20-30 GHz frequency band like RWG power dividers. The S_{21} and S_{31} values approximately equal to -3.21 dB. The insertion loss level of the designed SIW power divider is very close to the designed RWG insertion loss level despite the dielectric losses. Moreover, it is better than the designed microstrip power divider loss level at 25 GHz. Furthermore, the return loss value seems to be better than the other two type dividers and very suitable for use at the operating frequency.

As a conclusion, it can be said that the SIW power dividers are the best in terms of the return losses levels at 25 GHz. On the other hand, they are worse than the RWG power dividers and better than the microstrip power dividers in terms of insertion loss.

3.3. 1 x 2 SIW Power Dividers

3.3.1. 1 x 2 Y-Junction SIW Power Divider

3.3.1.1. Design of 1 x 2 Y-Junction SIW Power Divider

The 1 x 2 Y-Junction SIW power divider is one of the basic SIW power divider types that can be also used in more complex dividers. These type power dividers have comparatively wide bandwidth, low insertion loss and high quality factor. Also, the design technique of the 1 x 2 Y-Junction SIW power dividers is simple and has a very little variable quantity.

Mostly, the 1 x 2 Y-Junction SIW power dividers provide uniform feeding to the antennas, such as the same phase and power level at both of the ports. Since the distance between its output ports is very small, adjacent structures can be fed by Y-Junction SIW power dividers easily.

The 1 x 2 Y-Junction SIW power dividers have an inductive post as a metallic via that short circuited top and bottom walls of the SIW. This metallic via is located in the middle of the structure and adjusted to improve power reflection. The diameter and position of the inductive matching via are optimized to set the ratio of the power in the output branches by keeping the return loss as low as possible at the operation frequency band.

The conventional waveguide approaches could be used in the design of the SIW and the inductive post can be considered as equivalent to a parallel susceptance according to the conventional waveguide theory. Based on this knowledge, the circuit-equivalent of the straight Y-Junction is proposed in [4] thanks to rectangular waveguide equivalent models approaches in [53]. The equivalent circuit representation of the each discontinuity in 1 x 2 Y-Junction power divider is as seen in Figure 3.10.

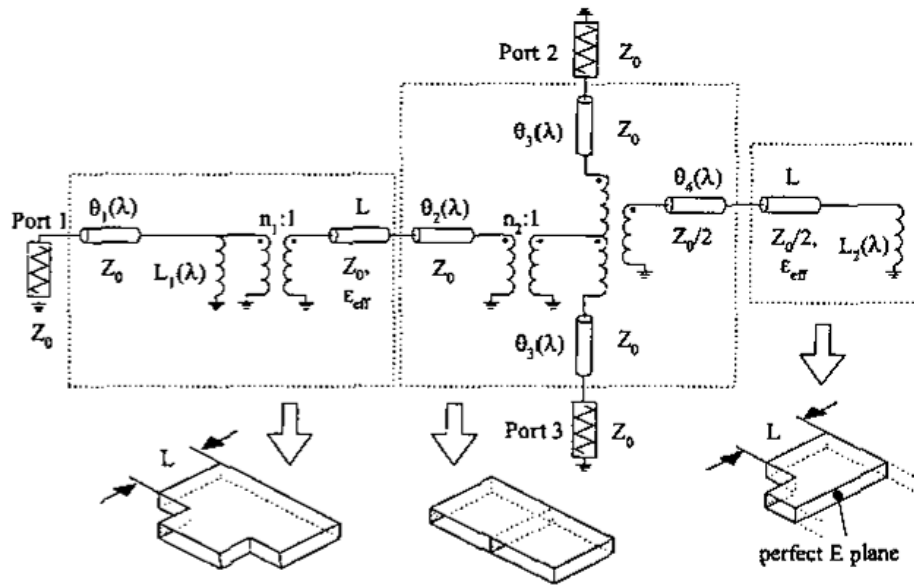


Figure 3.10: The circuit-equivalent model of the straight Y-Junction [4]

A 1 x 2 Y-Junction SIW power divider is designed within the scope of this thesis work by using the design models that are presented in [4] and [46]. In this power divider design, the input power is transmitted to each of output ports by equally dividing into two. The designed power divider is shown in Figure 3.11.

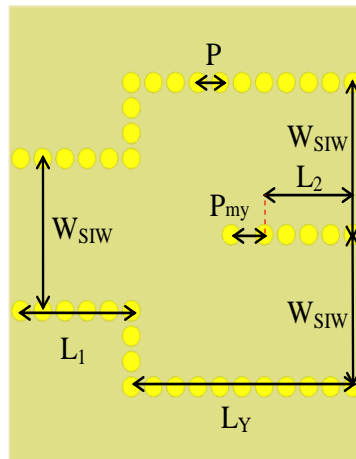


Figure 3.11: Designed 1 x 2 Y-Junction SIW power divider

All dimensions shown in Figure 3.11 are measured between the centers of vias. The diameters and the period of vias are the same as specified previously in Table 2.1. The period changes only at the center located via position and its value is $P_{my} = 1.5$ mm. The dimensions are presented in Table 3.1.

Table 3.1. Design parameters of 1 x 2 Y-Junction SIW power divider

L1	L_Y	L2
5 mm	10 mm	4 mm

The operation frequency of the designed power divider is 25 GHz. E-field distribution of this divider at the operation frequency is presented in Figure 3.12.

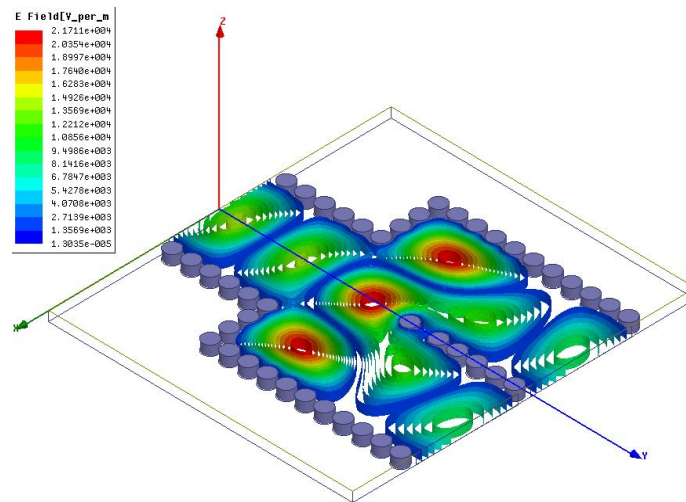


Figure 3.12: E-field distribution of 1 x 2 Y-Junction SIW power divider at 25 GHz

The designed 1 x 2 Y-Junction SIW power divider is completely symmetrical about the y-axis. Therefore, the divider provides the same phase and amplitude on each of the output ports ($S_{21} = S_{31}$). The metallic via which is located in the middle of the structure is optimized only in the direction of the y-axis to minimize the return loss (S_{11}). The simulation results of this divider are given in Figure 3.13.

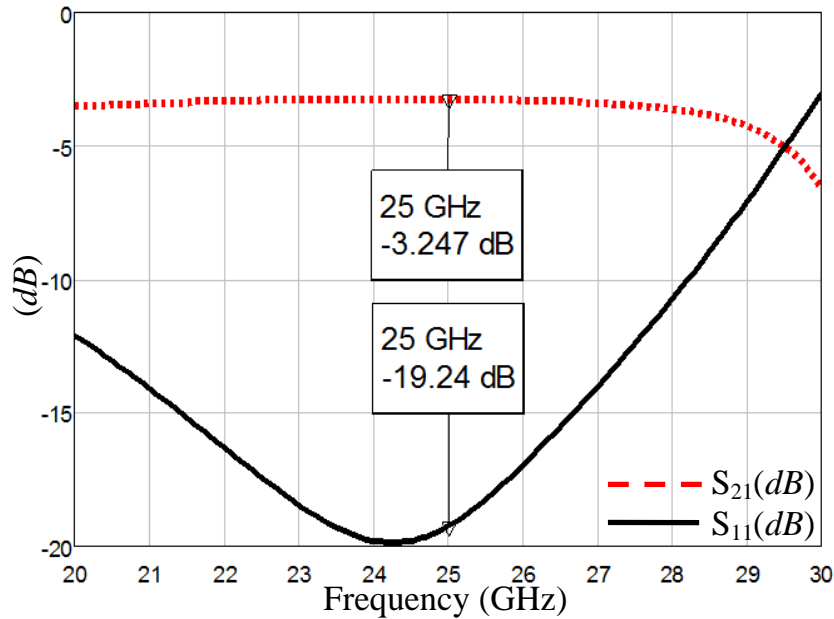


Figure 3.13: Simulation results of 1 x 2 Y-Junction SIW power divider

As seen in Figure 3.13, the designed power divider has a large frequency bandwidth. Especially, S_{21} and S_{31} values are very close to the ideal value (-3 dB) of them. Also, the return loss (S_{11}) values are considerably low particularly between 20 to 28 GHz . Moreover, the insertion loss values are almost unchanged in the mentioned frequency range.

3.3.1.2. Production of 1 x 2 Y-Junction SIW Power Divider

Transitions to microstrip line are added to the ports of the power divider designed in the previous section for the measurement as shown in Figure 3.14.

Considering the high operating frequency, a special type of the SMA connectors called “super SMA connectors” must be used in production for an accurate measurement. Super SMA type connectors can work properly up to 26.5 GHz .

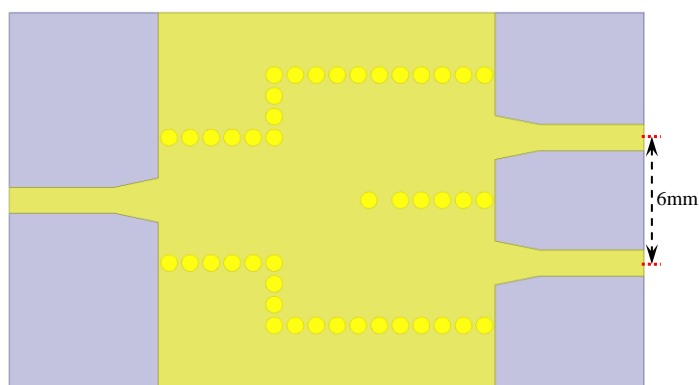


Figure 3.14: Designed 1 x 2 Y-Junction SIW power divider with microstrip transitions

However, the microstrip lines of the designed structure seen in Figure 3.14 are too close to connect two connector side by side. To overcome this problem, microstrip lines are bended. The most important criterion for selection of the bending type is the amount of impact on the insertion and return loss. Bending structure should have no effect in ideal case, but in reality it is desirable to minimize its effect on losses.

The main requirement for the production of the designed 1 x 2 Y-Junction SIW power divider is 90° bending of each microstrips located at the output ports in opposite directions. Thus, the ends of the output ports are located at the two opposite side of the structure and so the area which is necessary for soldering and placement of the connectors is provided. For 90° bending, the most commonly used bend types are circular and L-type with various angle (the most frequently used 45°) bending structures. In order to select bending type intended to be used in design, these bending types are sampled and compared with straight microstrip line with the same length. The designed $50\ \Omega$ comparison samples are shown in Figure 3.15.

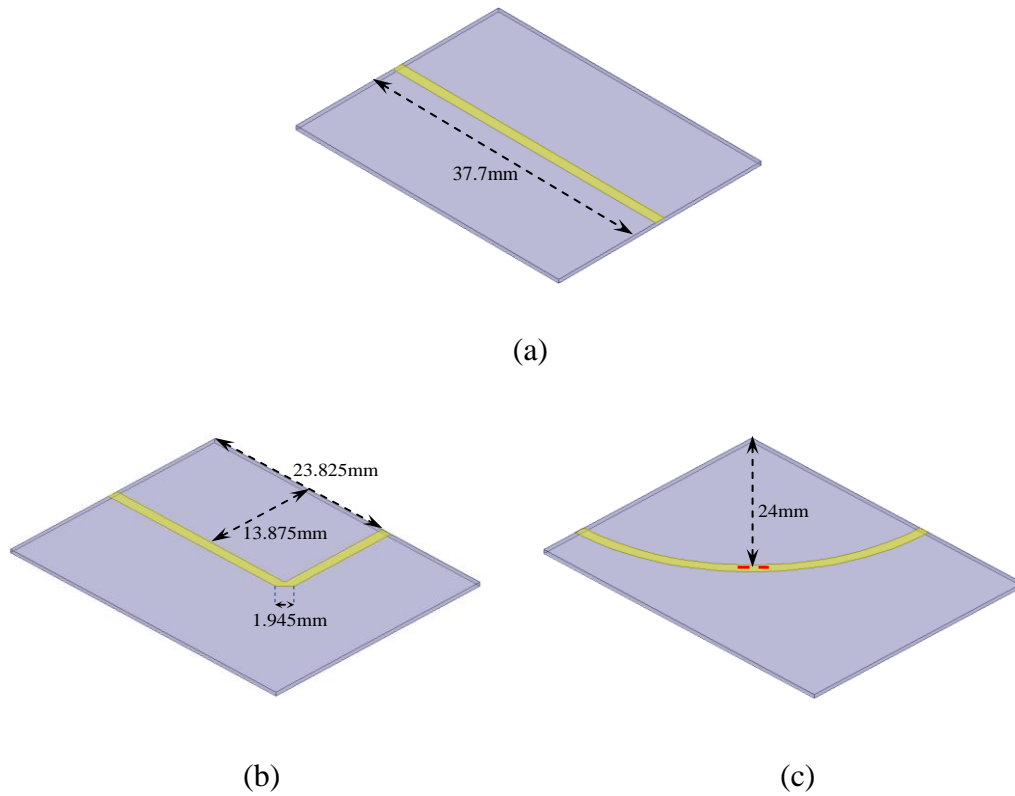
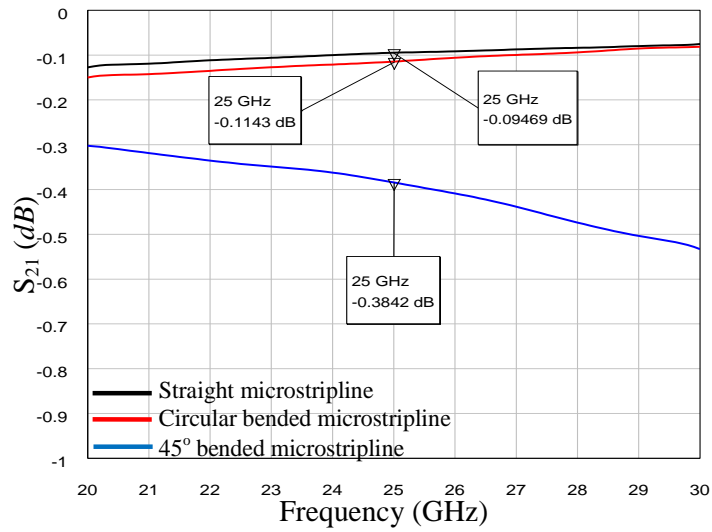


Figure 3.15: Designed comparison structures (50 Ω)

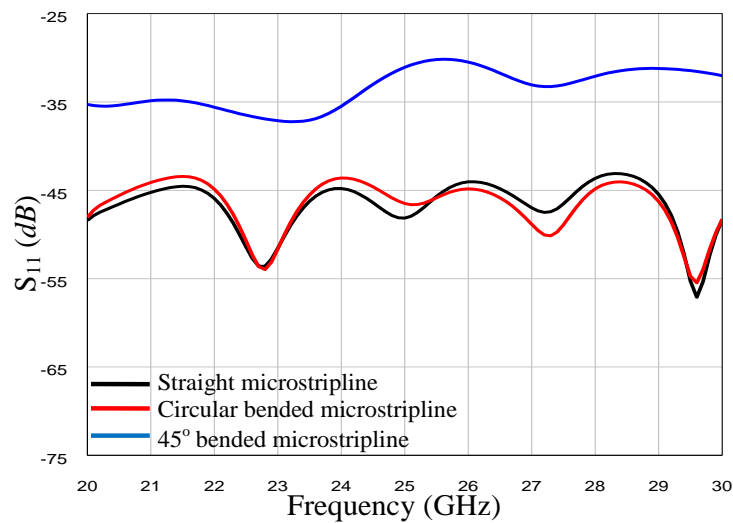
(a) Straight microstrip line, (b) 45⁰ L-Type bending and (c) Circular Type bending

The structures seen in Figure 3.15, designed with perfect electric conductor (PEC) microstrip lines on a substrate that has not any dielectric loss in order to understand exactly loss characteristics of the devices without the effect of the dielectric and conductor losses. Also, the lengths of microstrip lines are selected such that the distance between ports can be greater than twice the maximum wavelength in the operation frequency band in order to minimize interaction between the ports. The red dashed line on the quarter-circle microstrip line seen in Figure 3.15 (c) indicates the middle of microstrip line and widths of all microstrip lines are equal to 1.25 mm in all other designs. On the other hand, 45⁰ bending section of the L-Type bending structure is optimized with the help of Ansoft HFSS and the dimensions shown in Figure 3.15 (b) are the best ones after the optimization. These three structures are

simulated with the help of Ansoft HFSS and S parameters are plotted in Figure 3.16 (a) and (b).



(a)



(b)

Figure 3.16: Results of designed 50 Ω comparison structures

(a) Insertion losses, (b) Return losses

As seen in Figure 3.16, the results of the circular bending structure are more close to straight microstrip line results than the results of the 45° L-Type bending structure. According to the information obtained from the results, circular bending structure is selected for the production of the 1 x 2 Y-Junction SIW power divider.

3.3.1.2.1. Production of 1 x 2 Y-Junction SIW Power Divider Using Circular Bended Microstrip Lines

Output ports of the power divider are combined with circular bended microstrip lines as shown in Figure 3.17.

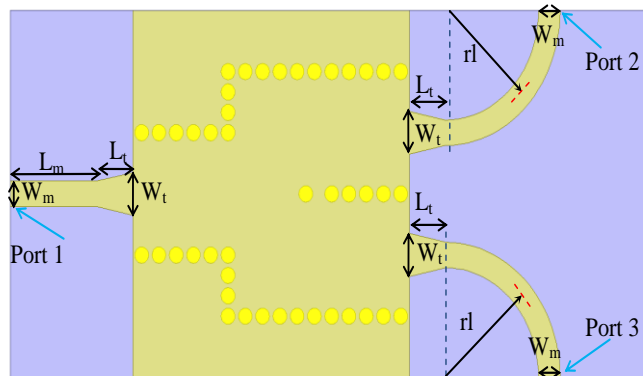


Figure 3.17: Design of the 1 x 2 Y-Junction SIW power divider using circular bended microstrip lines

The output 50Ω circular microstrip lines curvature radius is equal to $rl = 6mm$ when measured from the middle of the microstrip and all the other parameters are equal to previously determined values. The photograph of the produced 1 x 2 Y-Junction SIW power divider using circular bended microstrip lines is shown in Figure 3.18.

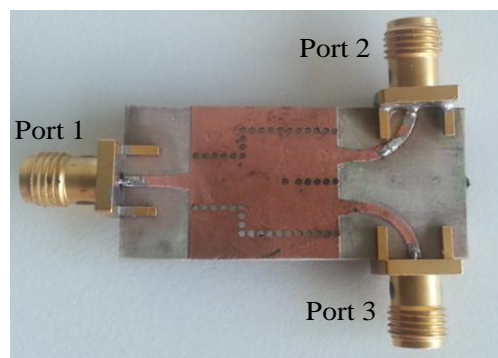
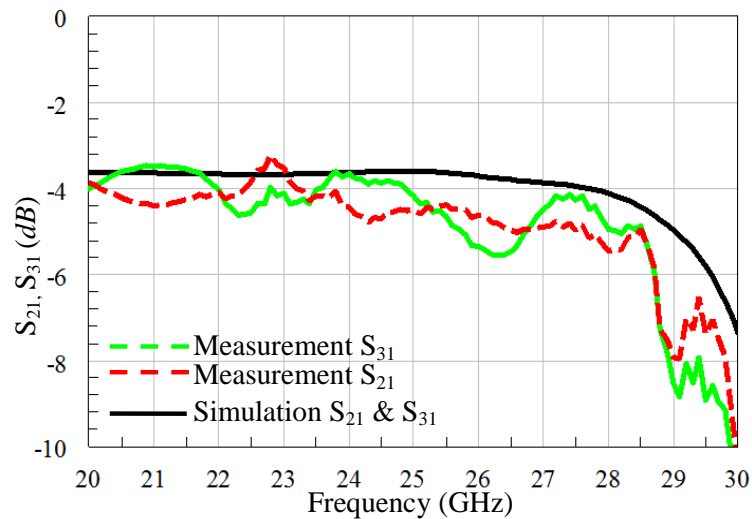
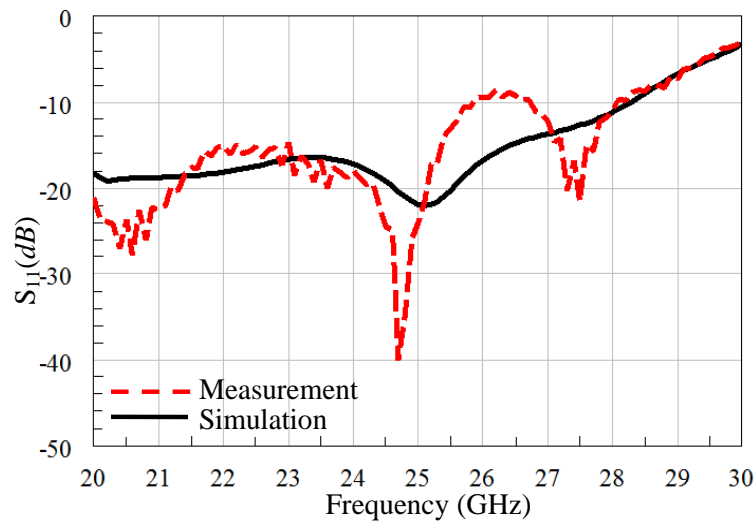


Figure 3.18: The photograph of the produced 1 x 2 Y-Junction SIW power divider using circular bended microstrip lines

The S parameters of the power divider are measured and compared with simulations in Figure 3.19 (a) and (b). When Figure 3.19 is observed, there is a good agreement between the simulations and the measurement results. Small disagreements may arise from the influence of the connectors that are added at the production but not considered in the simulation of the 1 x 2 Y-Junction SIW power divider.



(a)



(b)

Figure 3.19: Comparison results of produced 1 x 2 Y-Junction SIW power divider using circular bended microstrip lines with simulation results

(a) Insertion losses, (b) Return losses

3.3.1.2.2. Production of 1 x 2 Y-Junction SIW Power Divider Using Back-to-Back Configuration

For the characterization of the power divider, two power dividers are placed back-to-back as shown in Figure 3.20 and fabricated.

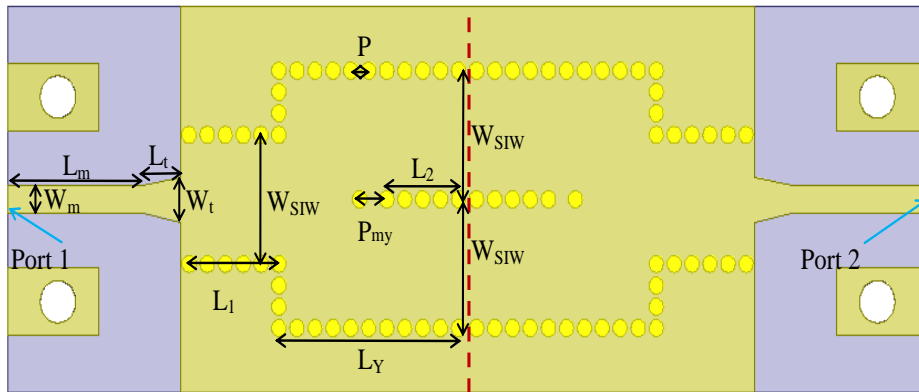


Figure 3.20: Design of the 1 x 2 Y-Junction SIW power divider using back-to-back configuration

The structure is mirror-image symmetric with respect to the red dash-line which is in the middle of Figure 3.20. The connectors are also included in the simulation as shown in Figure 3.21.

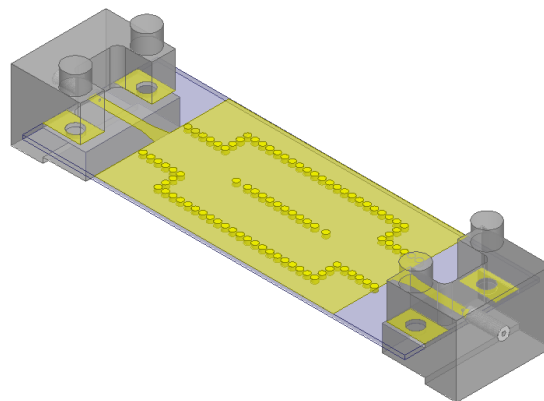


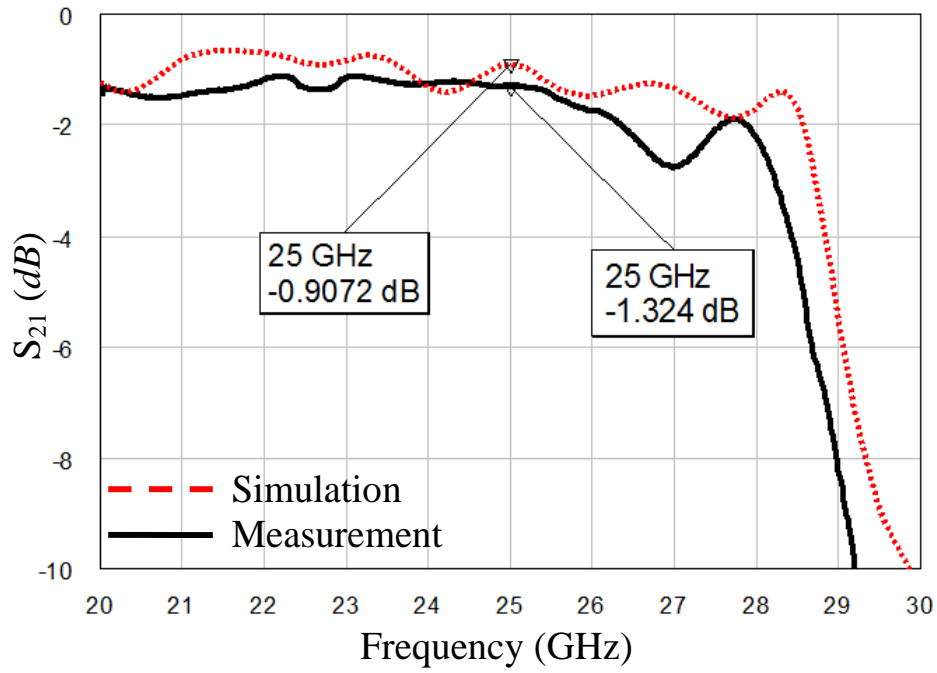
Figure 3.21: 1 x 2 Y-Junction SIW power divider using back-to-back configuration with depicted connectors

The photograph of the produced 1 x 2 Y-Junction SIW power divider using back-to-back configuration is shown in Figure 3.22.

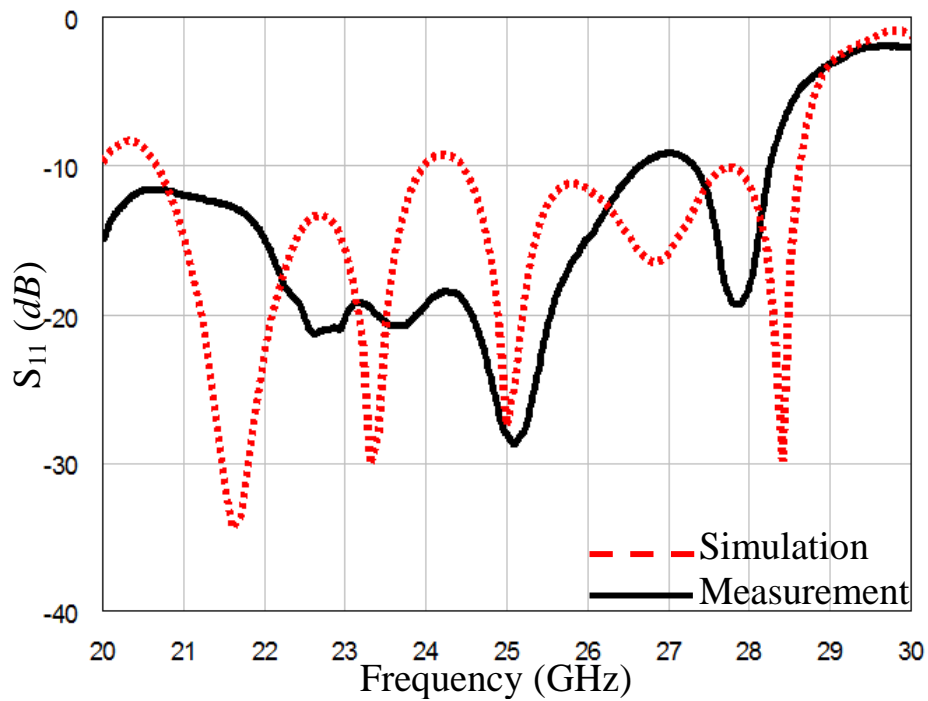


Figure 3.22: The photograph of the produced 1 x 2 Y-Junction SIW power divider using back-to-back configuration

Measurement results are compared with the simulation in Figure 3.23 (a) and (b). As seen in Figure 3.23, there is a better agreement between the simulations and the measurement results. Insertion losses in simulation and measurement are equal to -0.9 dB and -1.32 dB respectively at 25 GHz . In addition, discrepancies are very slight and just around -0.4 dB at the operating frequency.



(a)



(b)

Figure 3.23: Comparison results of produced 1 x 2 Y-Junction SIW power divider using back-to-back configuration with depicted connectors added simulation results

(a) Insertion losses, (b) Return losses

3.3.2. 1 x 2 T-Junction SIW Power Divider

3.3.2.1. Design of 1 x 2 T-Junction SIW Power Divider

The 1 x 2 T-Junction SIW power divider is also a basic SIW power divider structure. These type power dividers have wide bandwidth, low insertion loss, high quality factor and high power capability like 1 × 2 Y-Junction SIW power dividers.

Generally, the 1 x 2 T-Junction SIW power dividers provide uniform feeding to the antennas, such as the same phase and power level on all their ports but of course phase and power level ratio of output ports can be adjusted by using some design techniques. Unlike 1 x 2 Y-Junction SIW power dividers, 1 x 2 T-Junction SIW power dividers have an adjustable gap between output ports.

The 1 x 2 T-Junction SIW power dividers have three inductive posts realized as metallic vias that are short circuited top and bottom walls of the SIW. One of these metallic vias is located in the middle of the structure and the others are located at the left and the right side of the dividing section. The diameters and positions of these vias are optimized to set the ratio of the power in the output ports by keeping the return loss as low as possible at the operation frequency band.

A 1 x 2 T-Junction SIW power divider is designed by using the design models that are presented in [4] and [46]. In this power divider design, the input power is evenly divided into two and transmitted to each of the output ports. The designed power divider is as seen in Figure 3.24.

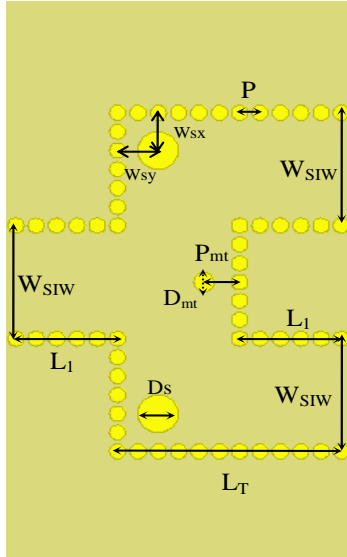


Figure 3.24: Designed 1 x 2 T-Junction SIW power divider

All given dimensions shown in Figure 3.24 are indicated between the centers of the corresponding vias. The distance of the center located via from the nearest outer wall is $P_{mt} = 1.75 \text{ mm}$ and its diameter is $D_{mt} = 1 \text{ mm}$. The position of the identical vias which are located at the left and the right side of dividing section are equal to $W_{sx} = W_{sy} = 2 \text{ mm}$ with respect to the nearest walls and their diameters are $D_s = 2 \text{ mm}$. The lengths are $L_1 = 5 \text{ mm}$ and $L_T = 11 \text{ mm}$. The operation frequency of the designed power divider is 25 GHz and E-field distribution of this divider at the operation frequency is given in Figure 3.25.

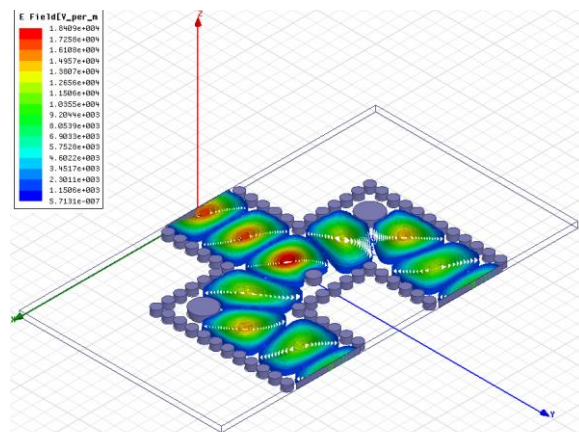


Figure 3.25: E-field distribution of 1 x 2 T-Junction SIW power divider at 25 GHz

The designed 1 x 2 T-Junction SIW power divider is entirely symmetrical about the y-axis. Therefore, the divider provides the same phase and the amplitude on each of the output ports ($S_{21} = S_{31}$). The simulation results of this divider are given in Figure 3.26.

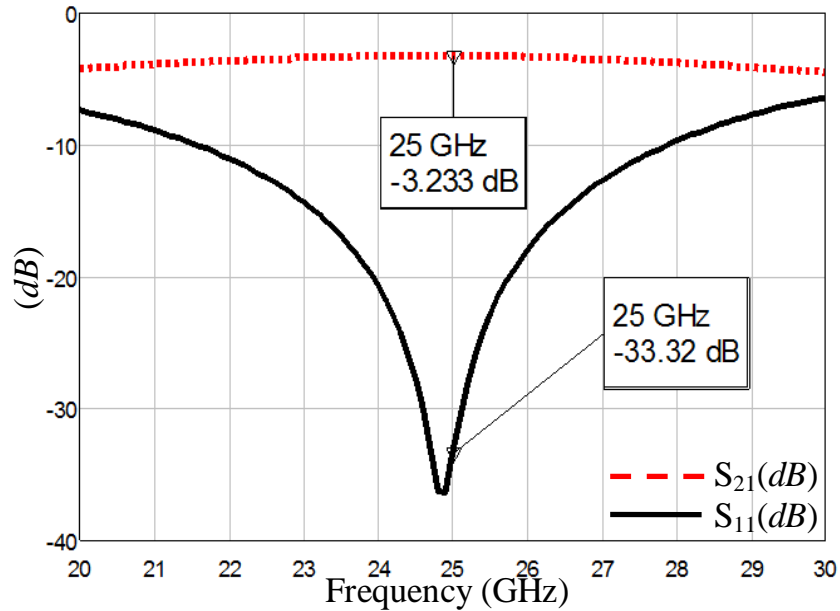
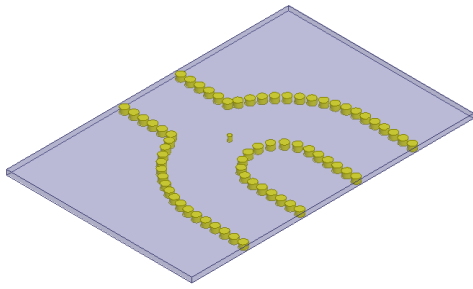


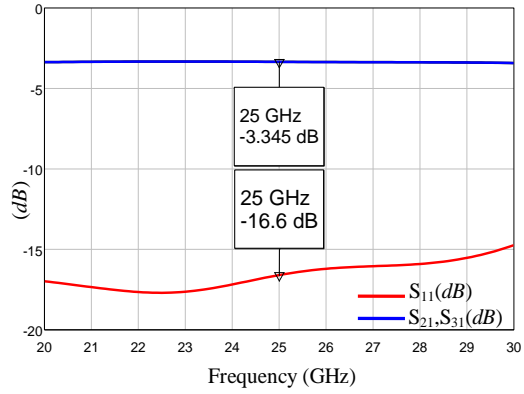
Figure 3.26: Simulation result of 1 x 2 T-Junction SIW power divider

As seen in Figure 3.26, the designed power divider has a large frequency bandwidth and very good matching condition at 25 GHz. S_{21} and S_{31} values are very close to the ideal values (-3 dB). In particular, the return loss (S_{11}) values are considerably low particularly between 21 to 28 GHz and equal to -33.32 dB at 25 GHz.

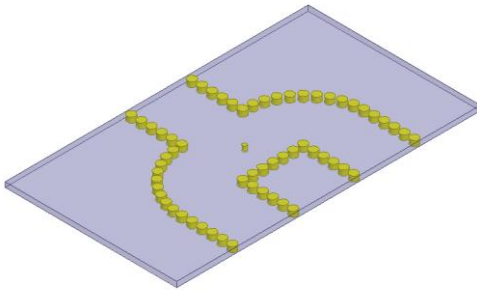
Apart from this design that is also used in the production, many 2-way SIW power dividers have been designed similar to T-Junction. Some of these designs having satisfactory results are shown in Figure 3.27 (a) - (f).



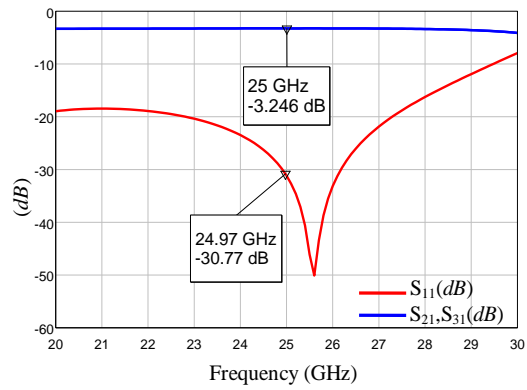
(a)



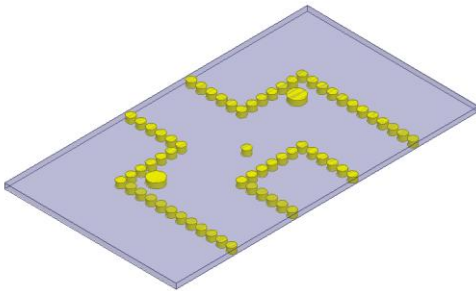
(b)



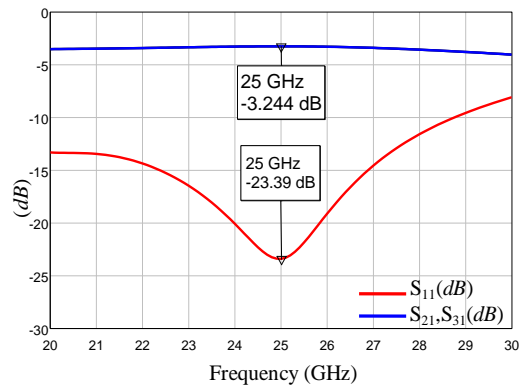
(c)



(d)



(e)



(f)

Figure 3.27: The other designed 1 x 2 SIW power dividers

(a) Design type 1, (b) Design type 1 Results, (c) Design type 2, (d) Design type 2 Results, (e) Design type 3, (f) Design type 3 Results

These 1 x 2 T-Junction SIW power dividers shown in Figure 3.27 have large bandwidth, good insertion and return loss levels in simulation. However, the productions of these devices can be problematic with the existing production facilities. “Design type 1” and “Design type 2” have very small center located metalized via. Based on the experience in production, it can be said; drilling and electroplating process in smaller via dimeters are not as efficient as the via diameters that are larger than 0.8 mm . On the other hand, “Design type 3” seen in Figure 3.27 (e), have via dimeters larger than 0.8 mm diameter but, inner side vias are too close to the external walls of the SIW. During the drilling process, the copper surfaces lie between the inner side vias and the external walls of the SIW are peeled off. Because of all these reasons, the structures seen in Figure 3.27 have not been produced.

3.3.2.2. Production of 1 x 2 T-Junction SIW Power Divider

For the characterization of the designed power divider, two dividers are placed back-to-back as shown in Figure 3.28. The structure has a mirror-image symmetry with respect to red dash-line.

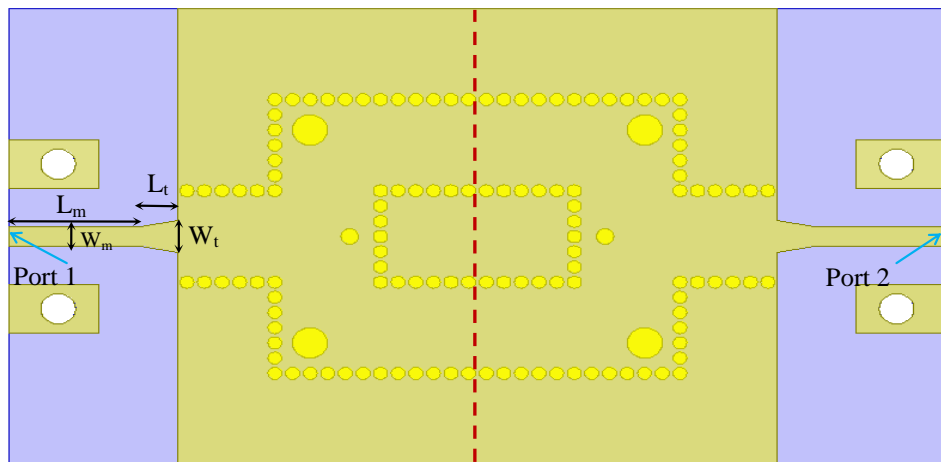


Figure 3.28: Designed 1 x 2 T-Junction SIW power divider for the production

The depicted connectors are also included in the simulations as shown in Figure 3.29.

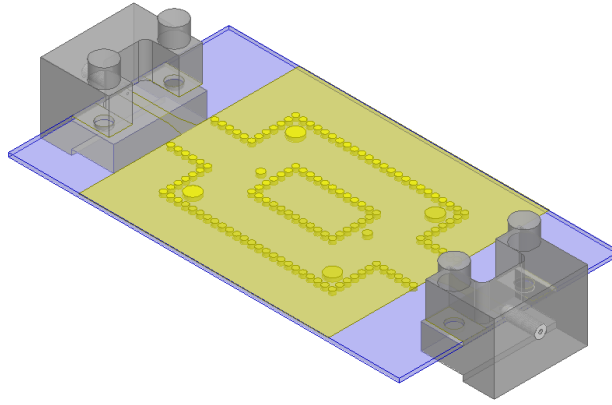


Figure 3.29: Designed 1 x 2 T-Junction SIW power divider for production with depicted connectors

The photograph of the produced 1 x 2 T-Junction SIW power divider is provided in Figure 3.30.

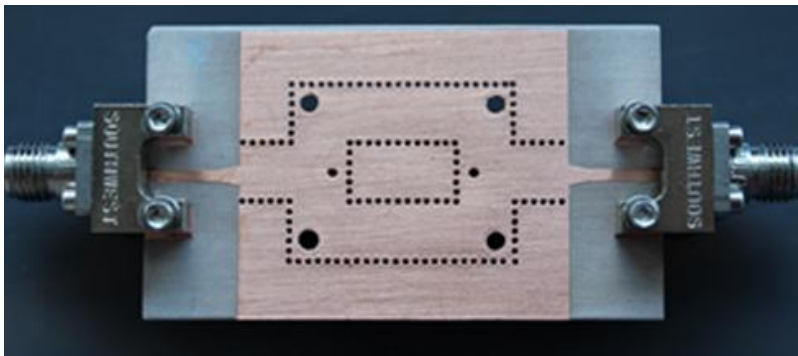
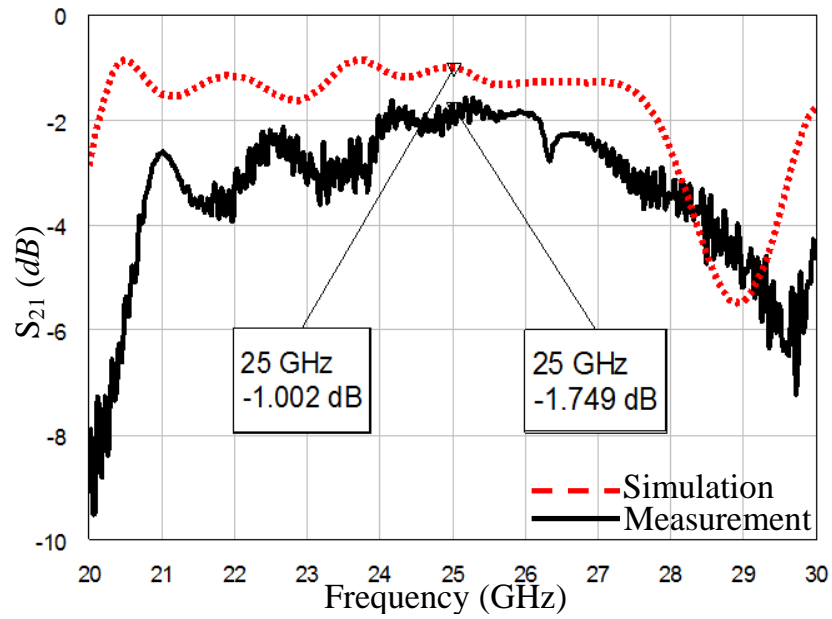
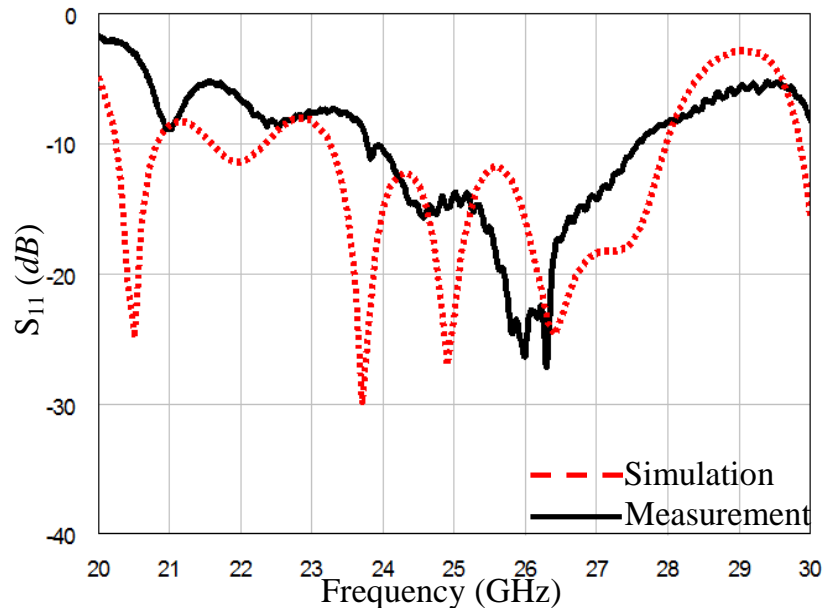


Figure 3.30: The photograph of the produced 1 x 2 T-Junction SIW power divider

Measurement results are compared with simulation in Figure 3.31 (a) and (b).



(a)



(b)

Figure 3.31: Comparison results of produced 1 x 2 T-Junction SIW power divider with depicted connectors added simulation results

(a) Insertion losses, (b) Return losses

Agreement between measured and simulated S_{11} values are good. However, there is approximately $0.5 - 1$ dB difference between S_{21} measurements and simulations.

3.4. 1 x 4 SIW Power Dividers

3.4.1. 1 x 4 Y & Y-Junction SIW Power Divider

3.4.1.1. Design of 1 x 4 Y & Y-Junction SIW Power Divider

1 x 4 Y & Y-Junction SIW power divider is obtained by concatenating two 1 x 2 Y-Junction SIW power dividers. However, the 1 x 2 Y-Junction SIW power dividers need modification. As mentioned before, 1 x 2 Y-Junction SIW power dividers have adjacent output ports. Due to this feature, it is not possible to add a divider to the each output port of the 1 x 2 Y-Junction SIW power divider without any modification on it. In order to accomplish this modification, an additional piece that increases the distance between output ports is designed. The new modified divider including additional expanding structure is shown in Figure 3.32.

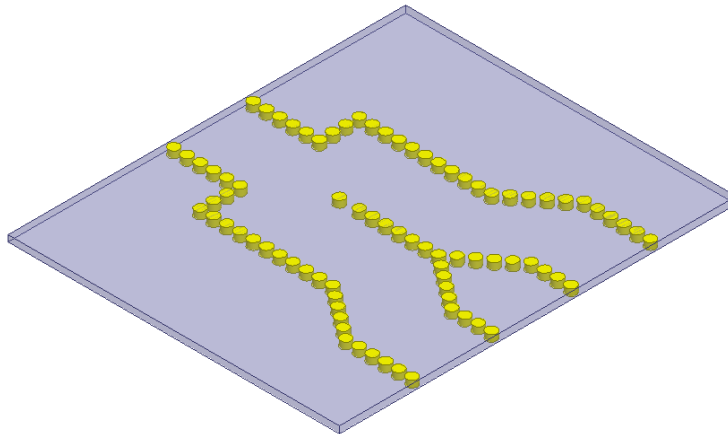


Figure 3.32: 1 x 2 Y-Junction SIW power divider including additional expanding structure

The effects of the additional structure to 1 x 2 Y-Junction SIW power divider are examined in the simulation environment. The insertion and return losses of the power divider are shown Figure 3.33.

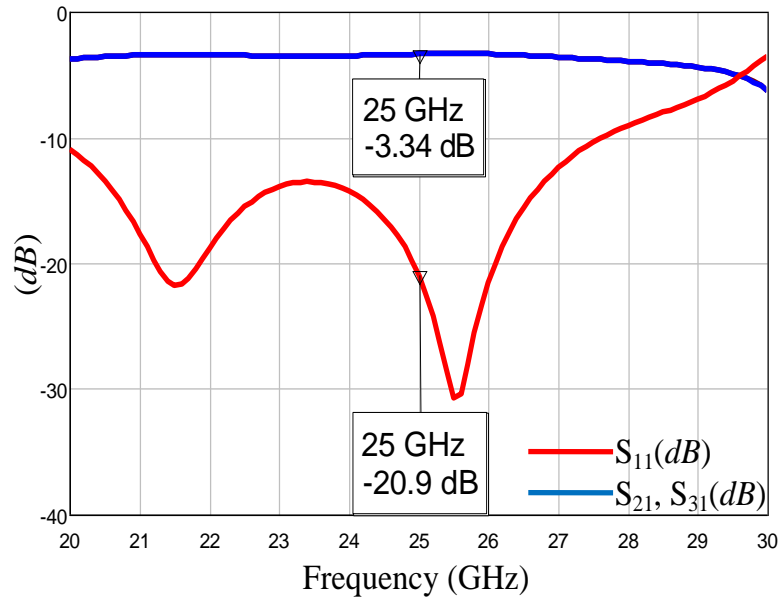


Figure 3.33: Results of the 1 x 2 Y-Junction SIW power divider having expanding structure

As seen in Figure 3.33 the amount of the expected deterioration on insertion and return loss resulting from discontinuities is very small and highly suitable for use in the operating frequency band. Also, two adjacent 1 x 2 Y-Junction SIW power divider are designed as having a side wall in common for adding to the output ports of the input divider. The designed output dividers are shown in Figure 3.34. By dint of these output dividers, halved power that came from their input port is divided into two again.

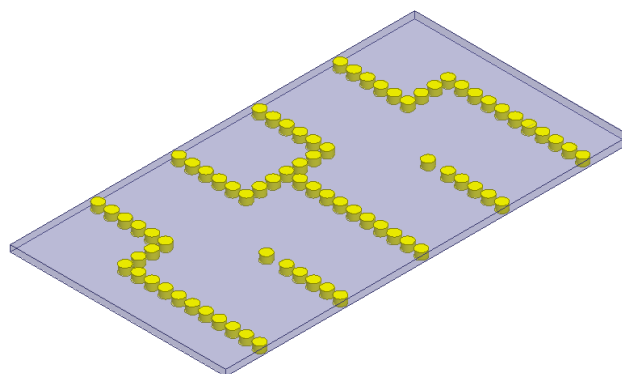


Figure 3.34: The designed output dividers

Finally, design of the 1 x 4 Y & Y-Junction SIW power divider is obtained as seen in Figure 3.35 by combining the all designed parts.

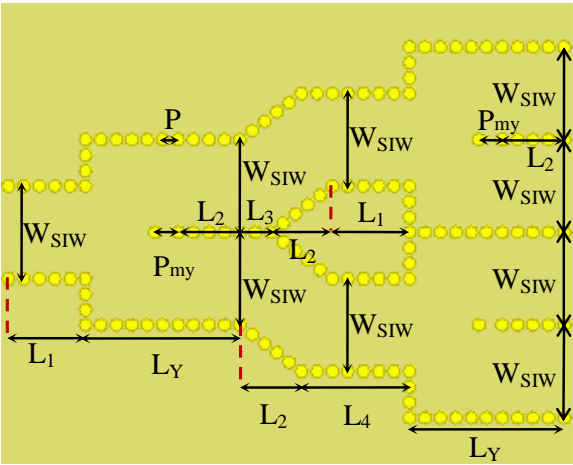


Figure 3.35: Design of the 1 x 4 Y & Y-Junction SIW power divider

The dimensions of the parameters of the designed 1 x 4 Y & Y-Junction SIW power divider are the same as the designed 1 x 2 Y-Junction SIW power divider except than $L3 = 2\text{ mm}$, $L4 = 7\text{ mm}$. E-field distribution of this divider at the operation frequency can be seen in Figure 3.36.

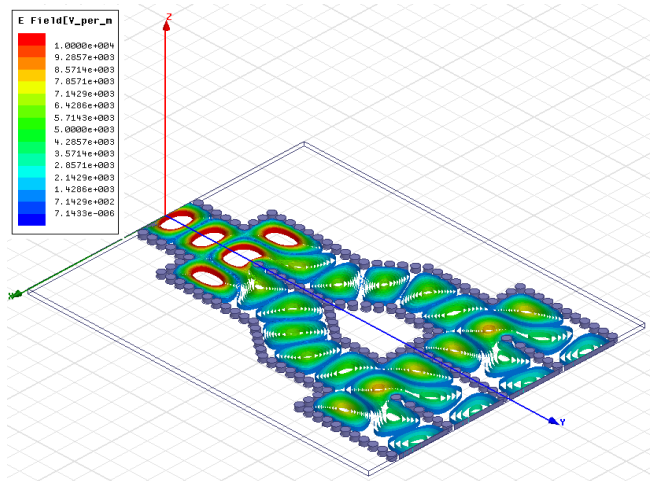


Figure 3.36: E-field distribution of the designed 1 x 4 Y & Y-Junction SIW power divider

The designed 1 x 4 Y & Y-Junction SIW power divider seen in Figure 3.36 is completely symmetrical about the y-axis. Therefore, the divider provides the same phase and amplitude on each of the output ports ($S_{21} = S_{31} = S_{41} = S_{51}$).

The simulation results of designed 1 x 4 Y & Y-Junction SIW power divider are given in Figure 3.37.

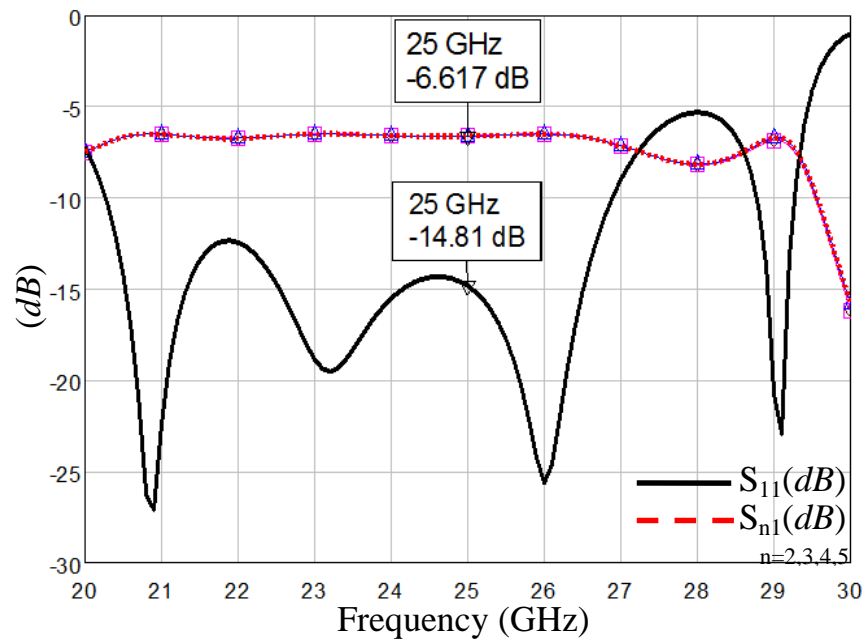


Figure 3.37: Simulation result of 1 x 4 Y & Y-Junction SIW power divider

As seen in Figure 3.37, the designed power divider is very suitable for use in the operating frequency band and has a large frequency bandwidth. Also, S_{21} , S_{31} , S_{41} , S_{51} lines are completely overlap each other and are equal to -6.6 dB at operating frequency. There is 0.6 dB loss due to the power divider structure.

3.4.1.2. Production of 1 x 4 Y & Y-Junction SIW Power Divider

Back-to-back configuration of the designed 1 x 4 Y & Y-Junction SIW power divider shown in Figure 3.38 is fabricated.

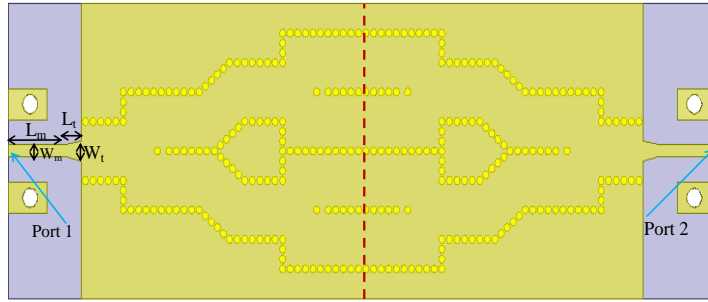


Figure 3.38: Designed 1 x 4 Y & Y-Junction SIW power divider for the production

The back-to-back configuration of 1 x 4 Y & Y-Junction SIW power divider with depicted connectors is simulated as shown in Figure 3.39.

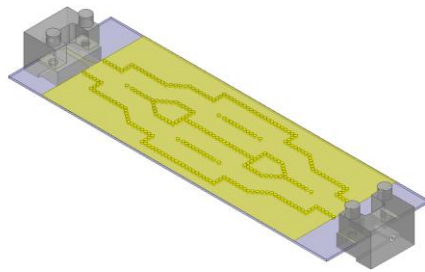


Figure 3.39: 1 x 4 Y & Y-Junction SIW power divider using back-to-back configuration with depicted connectors

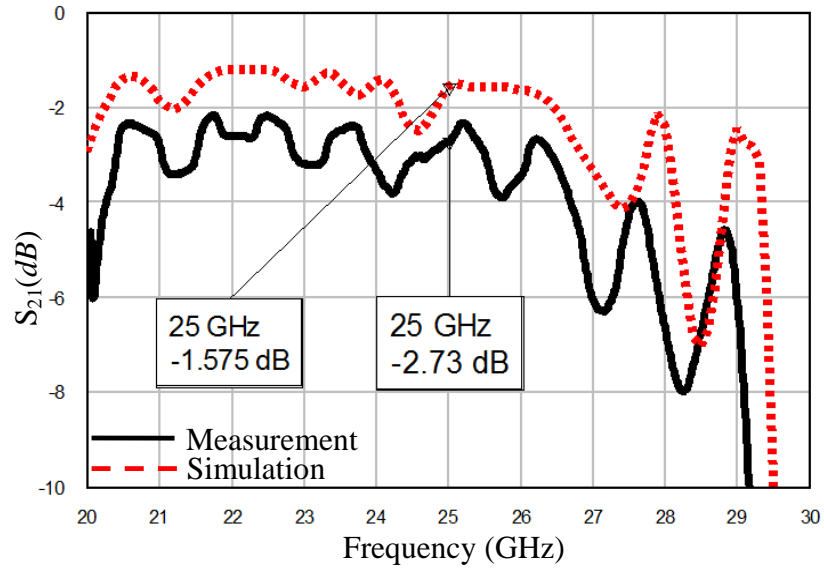
The photograph of the produced 1 x 4 Y & Y-Junction SIW power divider using back-to-back configuration is shown in Figure 3.40.



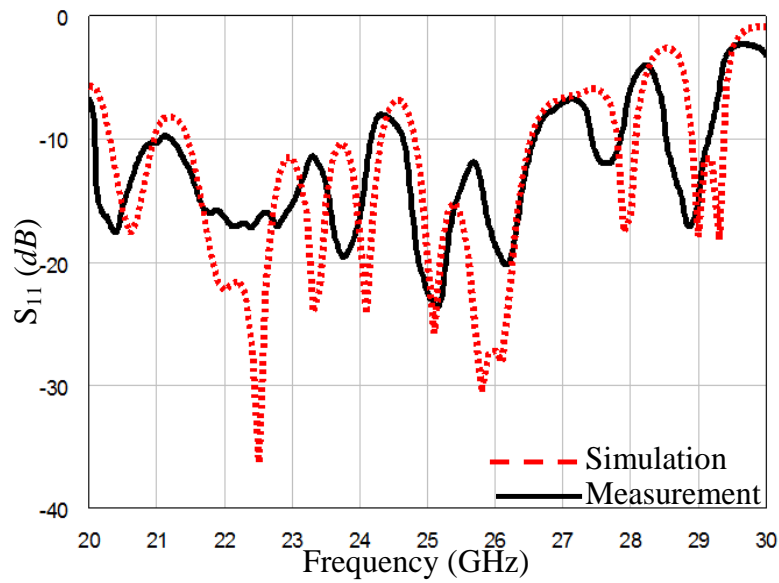
Figure 3.40: The photograph of the produced 1 x 4 Y & Y-Junction SIW power divider using back-to-back configuration

The comparison of measurement and simulation results of the produced 1 x 4 Y & Y-Junction SIW power divider are shown in Figure 3.41 (a) and (b).

As seen in Figure 3.41, there is a good agreement between the S_{11} simulations and the measurement results. In S_{21} , there is approximately 1 dB difference between measurement and simulation results.



(a)



(b)

Figure 3.41: Comparison results of produced 1×4 Y & Y-Junction SIW power divider using back-to-back configuration with depicted connectors added simulation results (a) Insertion losses, (b) Return losses.

3.4.2. 1 x 4 T & Y-Junction SIW Power Divider

3.4.2.1. Design of 1 x 4 T & Y-Junction SIW Power Divider

The 1 x 4 T & Y-Junction SIW power divider design is obtained by direct addition of the aforementioned 1 x 2 T-Junction SIW power divider and two adjacent 1 x 2 Y-Junction SIW power divider having a side wall in common (seen in Figure 3.34).

The main advantage of the 1 x 4 T & Y-Junction SIW power divider is that there is no need to modify the output dividers. Thus, the length of divider becomes shorter and insertion loss decreases. The view of the the 1 x 4 T & Y-Junction SIW power divider design is shown in Figure 3.42.

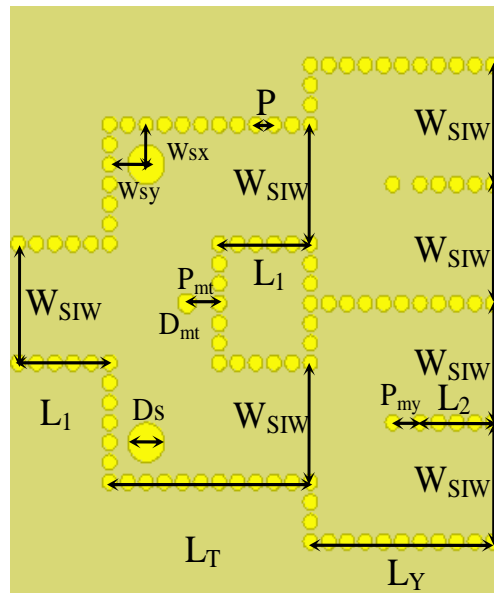


Figure 3.42: Design of the 1 x 4 T & Y-Junction SIW power divider

The dimensions are the same as the designed 1 x 2 Y-Junction and 1 x 2 T-Junction SIW power dividers.

The E-field distribution of this divider at the operation frequency is shown in Figure 3.43.

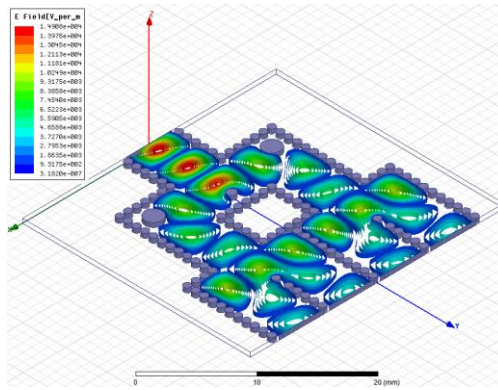


Figure 3.43: E-field distribution of 1 x 4 T & Y-Junction SIW power divider at 25 GHz

The designed 1 x 4 T & Y-Junction SIW power divider seen in Figure 3.43 is completely symmetrical about the y axis. Therefore, the divider provides the same phase and amplitude on each of the output ports ($S_{21} = S_{31} = S_{41} = S_{51}$). The simulation results of the designed 1 x 4 T & Y-Junction SIW power divider are shown in Figure 3.44. As can be seen, the designed power divider is very suitable for use in the operating frequency band and has a large frequency bandwidth. Also, $S_{21}, S_{31}, S_{41}, S_{51}$ completely overlap each other and are equal to -6.4 dB at operating frequency. There is 0.4 dB loss due to power divider structure. This amount of loss is 0.2 dB less than the loss of 1 x 4 Y & Y-Junction SIW power divider.

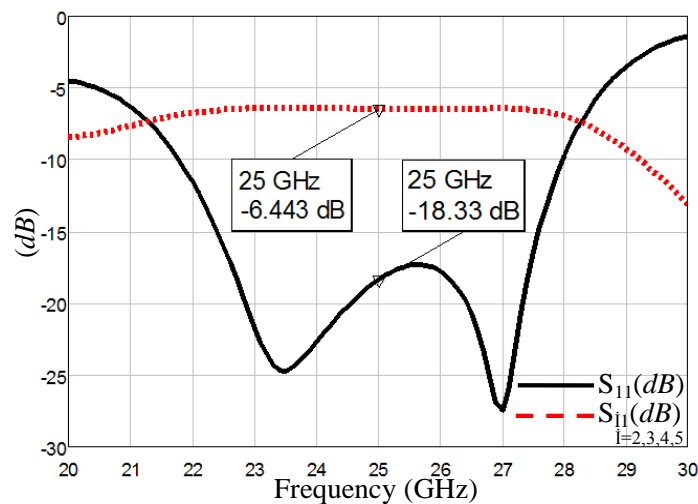


Figure 3.44: Simulation result of 1 x 4 T & Y-Junction SIW power divider

3.4.2.2. Production of 1 x 4 T & Y-Junction SIW Power Divider

Back-to-back configuration of the designed 1 x 4 T & Y-Junction SIW power divider is shown in Figure 3.45.

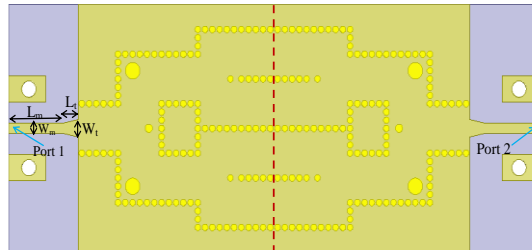


Figure 3.45: Designed 1 x 4 T & Y-Junction SIW power divider for the production

The back-to-back configuration of 1 x 4 T & Y-Junction SIW power divider with depicted connectors is simulated as shown in Figure 3.46.

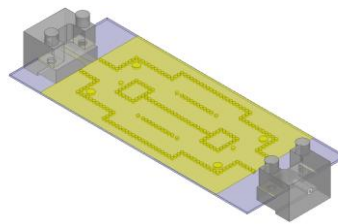


Figure 3.46: 1 x 4 T & Y-Junction SIW power divider using back-to-back configuration with depicted connectors

The photograph of the produced 1 x 4 T & Y-Junction SIW power divider using back-to-back configuration is shown in Figure 3.47.

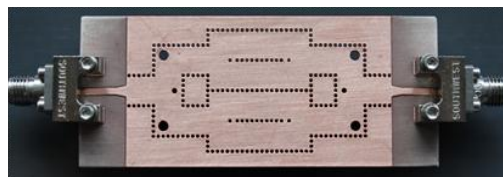
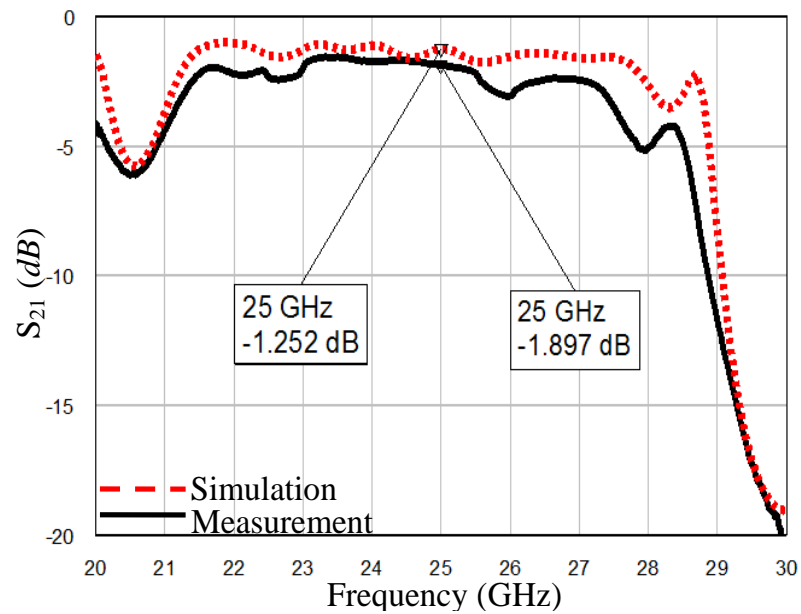
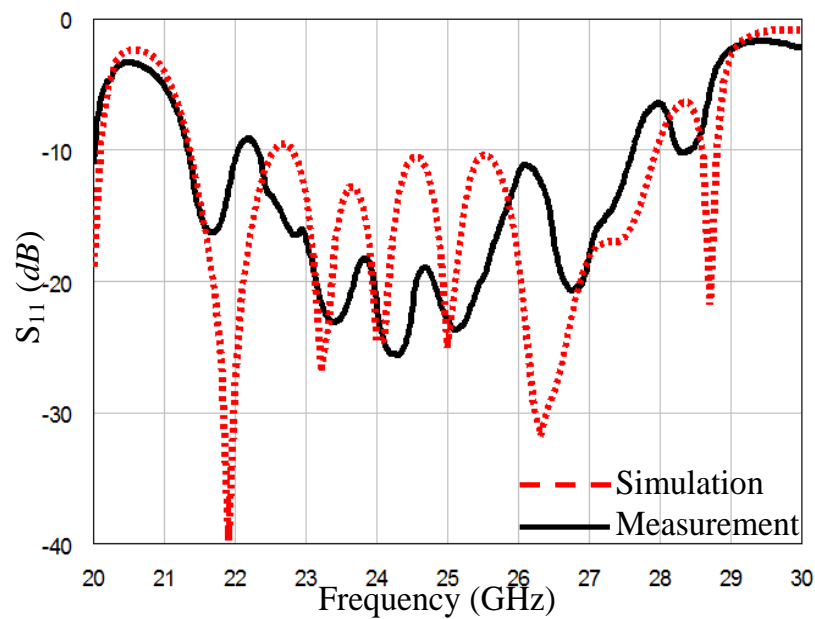


Figure 3.47: The photograph of the produced 1 x 4 T & Y-Junction SIW power divider using back-to-back configuration

The comparisons of measurement and simulation results are provided in Figure 3.48 (a) and (b).



(a)



(b)

Figure 3.48: Comparison results of produced 1 x 4 T & Y-Junction SIW power divider using back-to-back configuration with depicted connectors added simulation results (a) Insertion losses, (b) Return losses

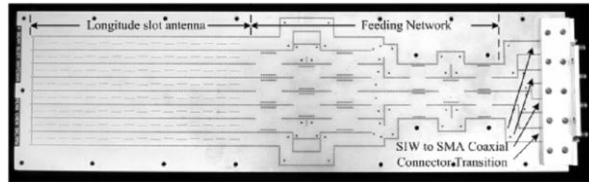
As seen in Figure 3.48, there is a good agreement between the S_{11} simulations and the measurement results. In S_{21} , there is approximately 0.6 dB difference between measurement and simulation. This means that; there is a better agreement between the simulations and the measurement results than the 1 x 4 Y & Y-Junction SIW power divider. The reason of the decrease in loss is substantially related to the reduction in length of the structure. The 1 x 4 T & Y-Junction SIW power divider is 10 mm shorter than 1 x 4 Y & Y-Junction SIW power divider.

3.5. 1 x 8 SIW Power Divider

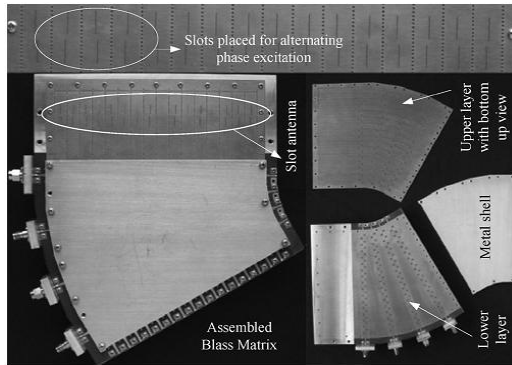
3.5.1. Design of 1 x 8 SIW Power Divider

One of the most widely used areas of the SIW power dividers is the feeding of antenna arrays. Antenna arrays are used to obtain high gain, electronic beam steering, to provide diversity reception, to maximize the Signal to Interference Plus Noise Ratio (SINR), help to determine the direction of arrival of the incoming signals (target tracking) and many signal processing functions such as spatial filtering, interference suppression. Unlike a single antenna which has a constant radiation pattern for a given antenna type and shape, pattern of antenna arrays can be adjusted by changing the excitation weights of the array elements. Thus, the design of amplitude and phase distributions of the antenna elements are necessary to achieve required far-field patterns which bring the design of power dividers with unequal power division into prominence.

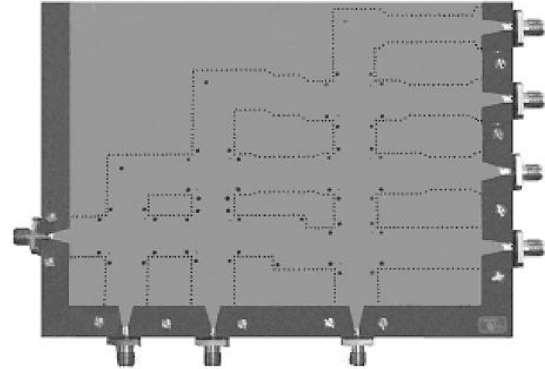
In the literature, there are several beamforming structures by using SIW technology [54]-[65]. Some of them are called as circuit-based beamforming networks that are separated into two main classes: Butler [54]-[60] and Blass [61]-[63] matrices. In addition to these classes, the Nolen [64]-[65] matrix which is a generalization of them is utilized in the beamforming network designs. Some examples of the different circuit based beamforming network types in literature are shown in Figure 3.49.



a)



(b)

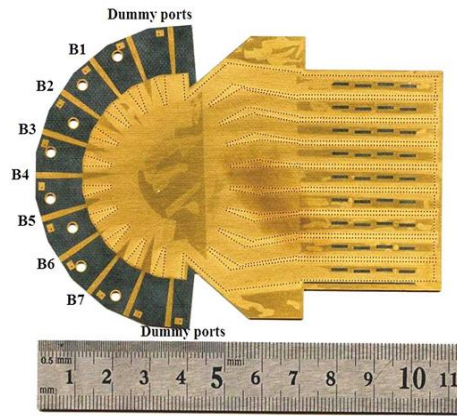


(c)

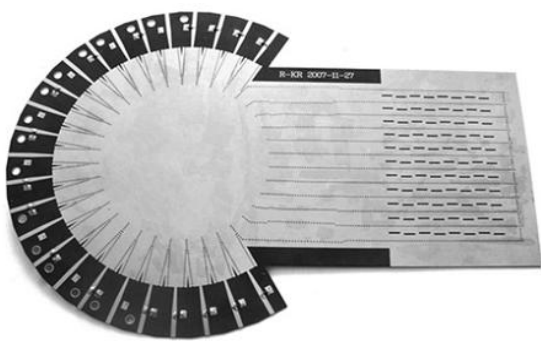
Figure 3.49: Photos of some manufactured circuit-based beamforming networks in literature (a) Butler Matrix based [59], (b) Blass Matrix based [63], (c) Nolen Matrix based [65]

Generally in circuit-based structures, beamwidths and beam angle depend on frequency but, beam crossover levels are independent from frequency [75].

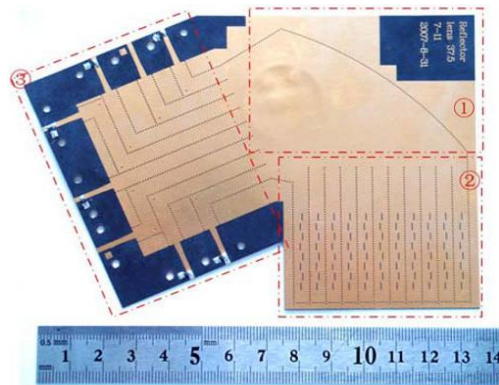
Besides there are SIW beamforming networks based on lenses such as; Rotman [66]-[71], R-KR [72], Reflector Lenses [73], [74]. Some examples of the different lens based beamforming network types in literature are shown in Figure 3.50. Design of lens based structures is much easier and more efficient compared to circuit-beamforming network counterparts. However, lens based structures do not have the same efficiency level in terms of occupied area and generally spread to larger areas [80].



a)



(b)



(c)

Figure 3.50: Photos of some manufactured lens-based beamforming networks in literature (a) Rotman Lens based [67], (b) R-KR Lens based [72], (c) Reflector Lens based [74].

In this thesis, a novel 1 x 8 SIW unequal power divider is developed. This structure has the advantages of the lens-based structures as well as occupies a relatively small area. The designed power divider is shown in Figure 3.51.

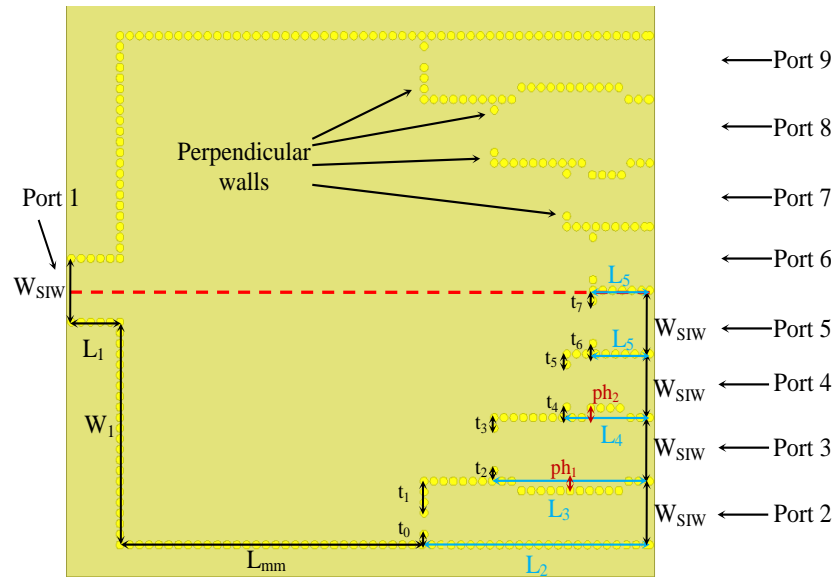


Figure 3.51: Designed 1 x 8 SIW power divider

The most of the design parameters of the 1 x 8 SIW power divider are determined with the help of the Sequential Nonlinear Programming (SNP) optimizer of Ansoft HFSS. The structure has mirror-image symmetry with respect to the red dash-line and the lengths that measured from the center to center are presented in Table 3.2.

Table 3.2. Design parameters of 1 x 8 SIW power divider (mm)

L_1	L_2	L_3	L_4	L_5	W_1	W_{SIW}	ph_1	ph_2
5	23.17	15.97	8.53	6.23	21	6	0.7	0.08
L_{mm}	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7
31.23	0.51	2	0.33	0.18	0.6	0.67	0.3	0.25

The power divider is excited from Port 1 and the optimizations are carried out to have same phases and 20 dB SLL Taylor ($\tilde{n}=3$) amplitude distribution at output ports in operating frequency. The sudden expansion of the SIW width encountered just after the input SIW part generates the higher-order modes. These modes excite the fundamental mode in the relatively narrow SIW structures which are placed at the output ports of the divider. These narrow SIW structures are designed with different

lengths (like Rotman or R-KR Lenses) in order to reduce the phase differences at the output ports. The remaining small phase differences are almost eliminated by narrowing the walls using the parameters $ph1$ and $ph2$. Also, the vias which are perpendicularly located at the entrance of these narrow SIW structures are utilized to adjust the desired amplitude distribution.

E-field distribution of this divider at the operation frequency is presented in Figure 3.52.

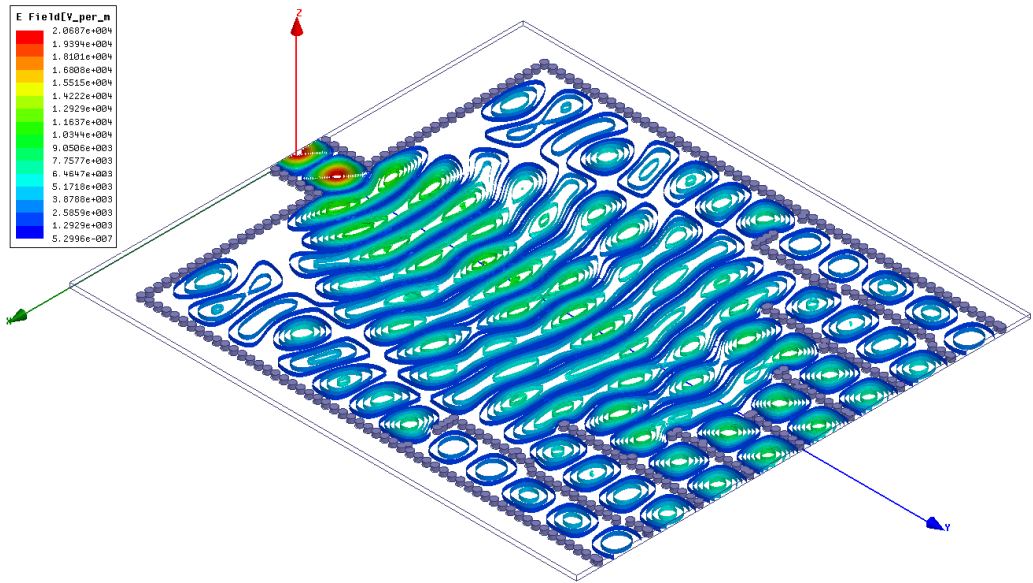


Figure 3.52: E-field distribution of 1 x 8 SIW power divider at 25 GHz

One of the most critical steps of this design is the determination of initial L_{mm} value for optimization. This value is determined according to the guided wavelength of the mode that has highest cut-off frequency smaller than the operating frequency. To determine this parameter, RGW equivalent of the width of enlarged SIW section is calculated with the help of Equations (2.2) - (2.6). Then, cut-off frequencies are calculated using Equation (2.1).

The enlarged SIW section width of the designed 1 x 8 power divider is equal to 48 mm and its RWG equivalent width is equal to 47.5931 mm. The calculated cut-off frequencies using $a = 47.5931$ mm and $b=0.5$ mm are presented in Table 3.3.

Table 3.3. Cut-off frequencies for a= 47.5931 mm

m	n	$f_{c_{mn}}$ (GHz)
1	0	1.82
2	0	3.64
3	0	5.46
4	0	7.27
5	0	9.09
6	0	10.91
7	0	12.73
8	0	14.55
9	0	16.37
10	0	18.19
11	0	20
12	0	21.83
13	0	23.64

The mode that has highest cut-off frequency smaller than 25 GHz is $TE_{13 0}$. The guided wavelength of this mode is equal to 21.4139 mm. The initial value of L_{mm} can be chosen to provide the following criteria;

$$2 \times \lambda_{g_{13 0}} > L_{mm} > \lambda_{g_{13 0}}$$

The normalized amplitudes at the output ports and S_{11} results of the designed 1 x 8 SIW power divider are obtained by simulations as shown in Figure 3.53.

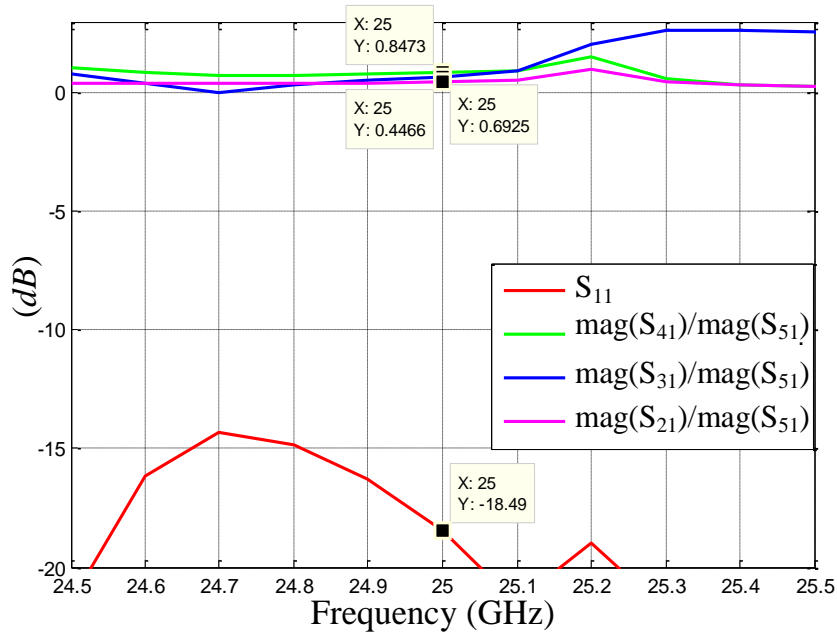


Figure 3.53: The normalized amplitudes and S_{11} results of designed 1 x 8 SIW power divider simulation

The normalized amplitudes of the 20 dB SLL Taylor ($\tilde{n}=3$) are calculated using the equations in [76] and compared with simulation results as seen in Table 3.4.

Table 3.4. The normalized amplitudes comparisons of the 20 dB SLL Taylor ($\tilde{n}=3$) and designed 1x8 power divider

	$\frac{\text{Port 2}}{\text{Port 5}}$	$\frac{\text{Port 3}}{\text{Port 5}}$	$\frac{\text{Port 4}}{\text{Port 5}}$	$\frac{\text{Port 5}}{\text{Port 5}}$	$\frac{\text{Port 6}}{\text{Port 5}}$	$\frac{\text{Port 7}}{\text{Port 5}}$	$\frac{\text{Port 8}}{\text{Port 5}}$	$\frac{\text{Port 9}}{\text{Port 5}}$
20 dB Taylor($\tilde{n}=3$)	0.5532	0.6793	0.8644	1	1	0.8644	0.6793	0.5532
Simulation Results	0.4466	0.6925	0.8473	1	1	0.8473	0.6925	0.4466

Also, the phase difference between ports must be close to zero in order to obtain in phase contribution of each port in the array. The phase differences result of the designed 1 x 8 power divider with reference to the Port 5 is shown in Figure 3.54.

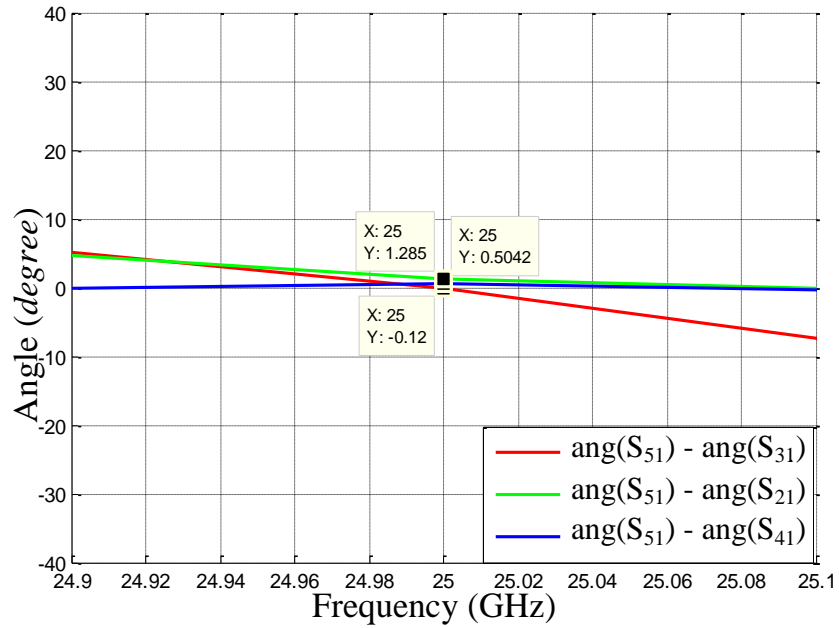


Figure 3.54: The phase result of designed 1 x 8 SIW power divider simulation

The phase results are very close to each other and maximum phase difference is approximately 1 degree. Since the structure is mirror-image symmetric with respect to the red dash-line shown in Figure 3.51, the results of symmetrical ports are equal to each other.

The array factors are calculated using the amplitude excitation coefficients obtained by standard -20 dB SLL Taylor ($\tilde{n}=3$) distribution and by simulations that are shown in Figure 3.53 and Figure 3.54. The comparison of the array factors of the designed structure is given in Figure 3.55. As can be seen in Figure 3.55, SLL values calculated the excitation coefficients obtained from the simulation results of the 1 x 8 SIW power divider agree well with the ones obtained by using ideal 20 dB Taylor distribution.

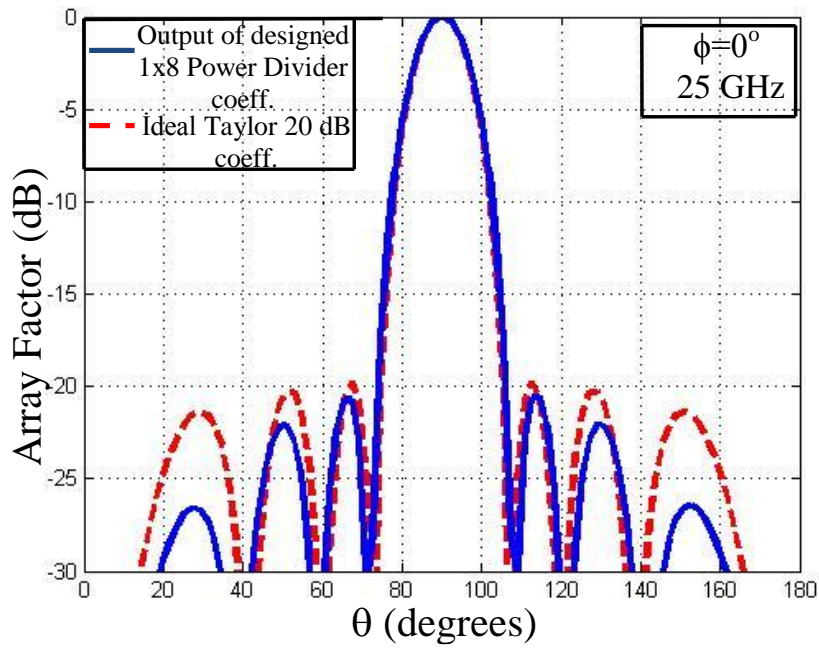


Figure 3.55: The comparison of the designed 1 x 8 SIW power divider and calculated 20 dB SLL Taylor ($\tilde{n}=3$) array factor results

The array factors for different frequencies around 25 GHz are plotted in Figure 3.56.

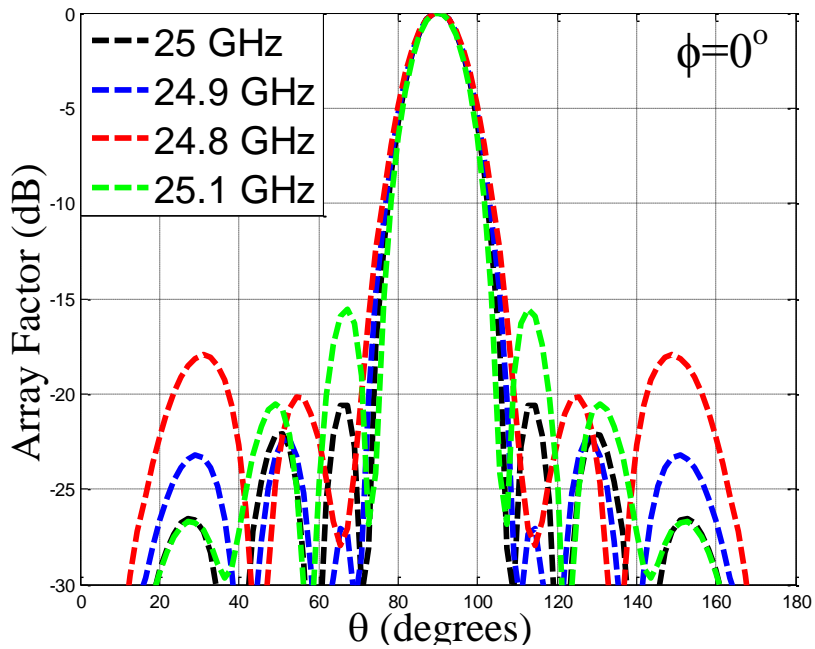


Figure 3.56: The array factors for -15 dB reference level

It is observed that side lobe levels of the power divider are below -20 dB between 24.9 - 25 GHz and below -15 dB between 24.8 - 25.1 GHz frequency bands. It can be concluded that this power divider is a narrowband structure considering SLL less than -15 dB pattern bandwidth definition (approximately %2 bandwidth).

3.5.2. Production of 1 x 8 SIW Power Divider

Microstrip line to SIW transitions are added to the ports for the measurements as shown in Figure 3.57.

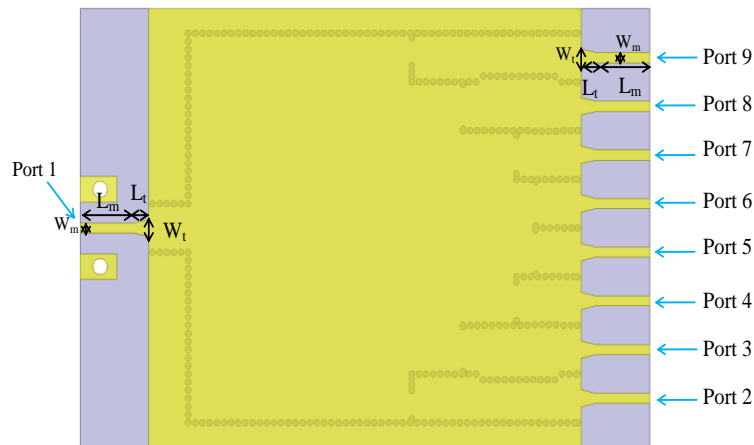


Figure 3.57: Designed 1 x 8 power divider for the production

Since the output ports are too close to connect two connectors side by side, chip terminations are utilized in some of the output ports. Through the use of chip terminators, even numbered output ports can be terminated by 50Ω chip terminations while super SMA connectors are added to odd numbered output ports (or vice versa). Thus, the distance restriction is overcome and one of the super SMA connectors at the output ports is selected to take measurement while the others are terminated by 50Ω SMA terminations.

The photograph of the produced 1 x 8 SIW power divider is shown in Figure 3.58.

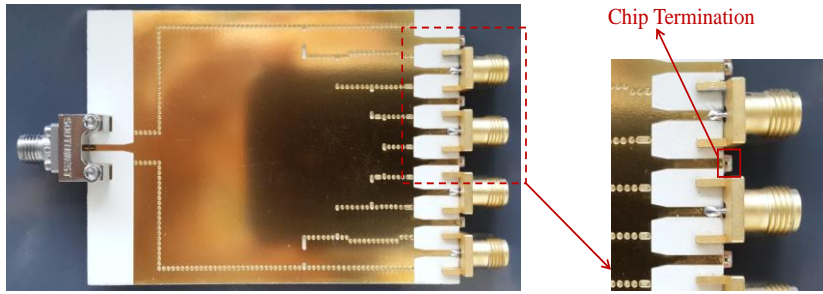


Figure 3.58: The photograph of the produced 1 x 8 SIW power divider at 25 GHz

The comparison of the simulated and measured S_{11} results of the designed 1 x 8 SIW power divider is shown in Figure 3.59. It is seen that there is a good agreement between measured and simulated S_{11} results.

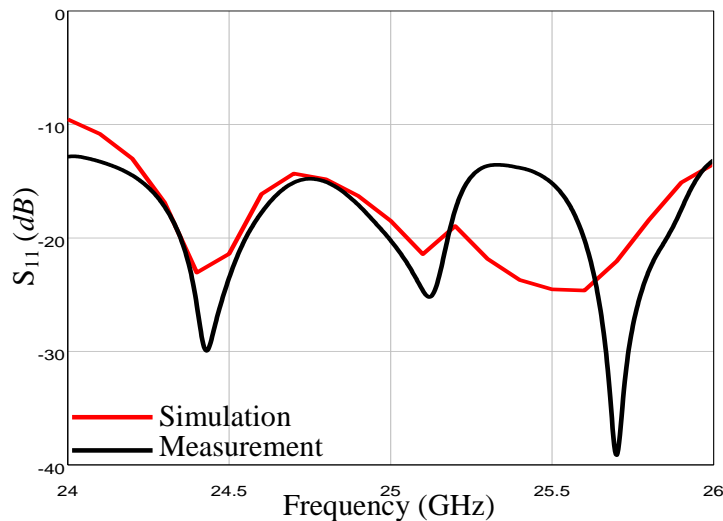


Figure 3.59: The comparison of the simulated and measured S_{11} results of the 1 x 8 SIW power divider

The measurements are performed by terminating all the output ports by a matched load except the port under measurement. The insertion loss results of all output ports are compared with simulation results as shown in Figure 3.60. As can be seen in Figure 3.60, the measurement results agree well with the simulation results of the designed 1 x 8 SIW power divider. There is approximately 1 - 2 dB difference between the measured and simulated results.

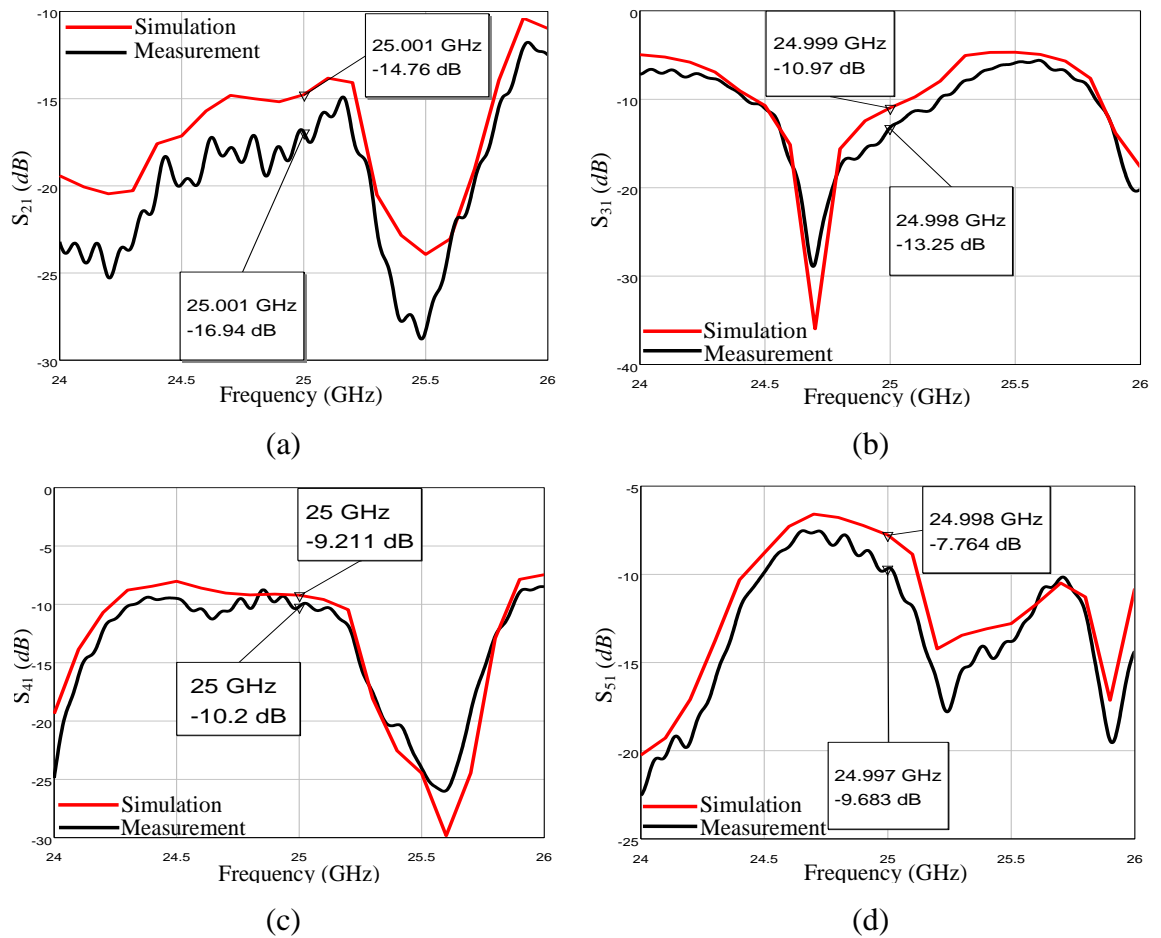


Figure 3.60: The comparison of the simulated and measured insertion loss results of the 1 x 8 SIW power divider.

In the simulations, permittivity and loss tangent value given in the data sheet of the substrate provided by the vendor are used, which are $\epsilon_r = 3$, $\tan\delta = 0.0013$ at 10 GHz. However these values may differ for 25 GHz. So, it is anticipated that differences between the measured and simulated results may stem from using incorrect loss tangent ($\tan\delta$) value in the simulations. To characterize the material at 25 GHz, thru line is simulated for different tangent loss values and results obtained are compared with the measurements in Figure 3.61.

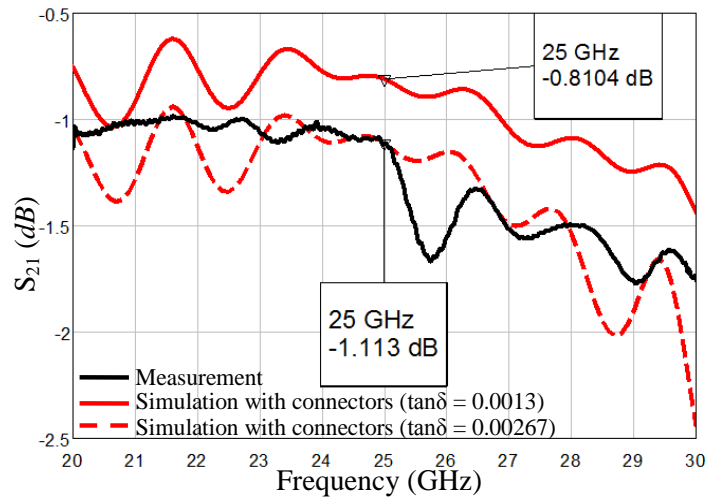


Figure 3.61: The comparison of the thru line results obtained simulation and measurement for different tangent loss values

It is seen that the differences between simulation and measurement results can be reduced when the loss tangent value is taken to be 0.00267 .

Since the differences seen in Figure 3.60 do not significantly change the normalized excitation coefficients of the output ports, these discrepancies are not crucial for the amplitude distribution ratios at the output ports. The comparison of the normalized excitation coefficients obtained from Taylor -20 dB distribution, HFSS simulation and measurement are plotted in Figure 3.62.

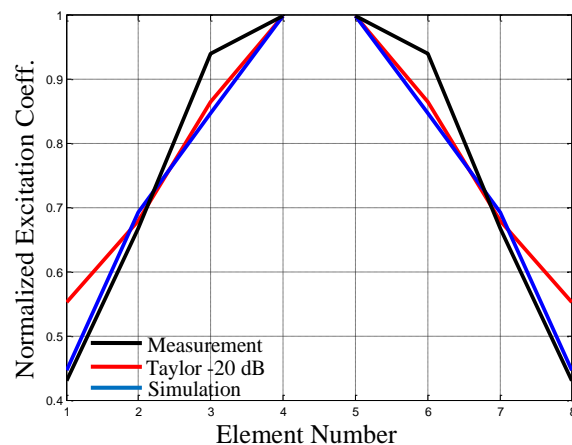


Figure 3.62: The comparison of the normalized excitation coefficients

The array factors obtained by using -20 dB SLL Taylor ($\tilde{n}=3$) distribution, simulation and measurement coefficients of 1×8 SIW power divider are compared in Figure 3.63.

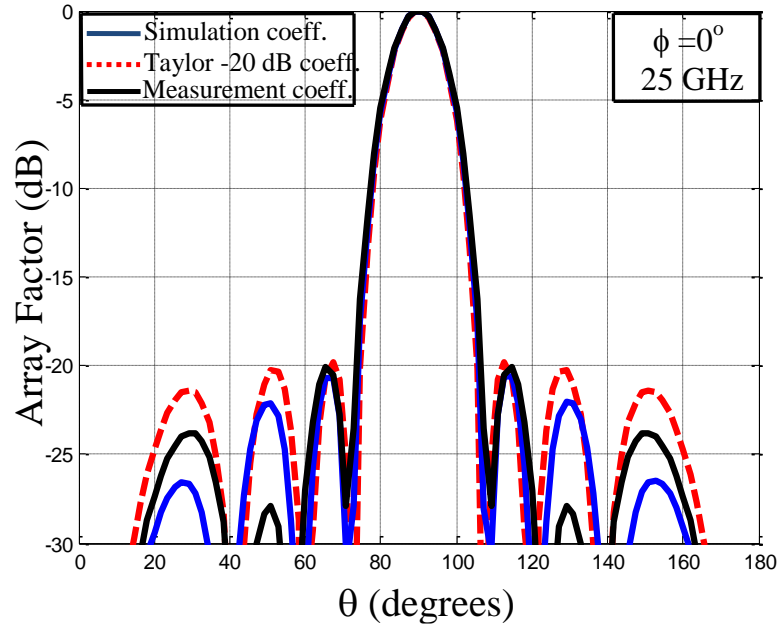


Figure 3.63: The comparison of the array factors obtained by using Taylor distribution, simulation and measurement coefficients of designed 1×8 SIW power divider

As can be seen in Figure 3.63, there is a good agreement between the SLL values of the patterns.

3.6. Slotted SIW Array Antennas

In this thesis, two different standing wave slotted SIW array antennas are designed and fed by the designed 1×8 SIW power divider. These antennas are resonant structures having narrow bandwidth and they are suitable to be used in combination with SIW power dividers.

3.6.1. 8 x 1 Slotted SIW Array Antenna

3.6.1.1. Design of 8 x 1 Slotted SIW Array Antenna

The designed 8 x 1 slotted SIW array antenna is composed of single longitudinal slot SIW antennas. Longitudinal slot antenna on shorted SIW is shown in Figure 3.64.

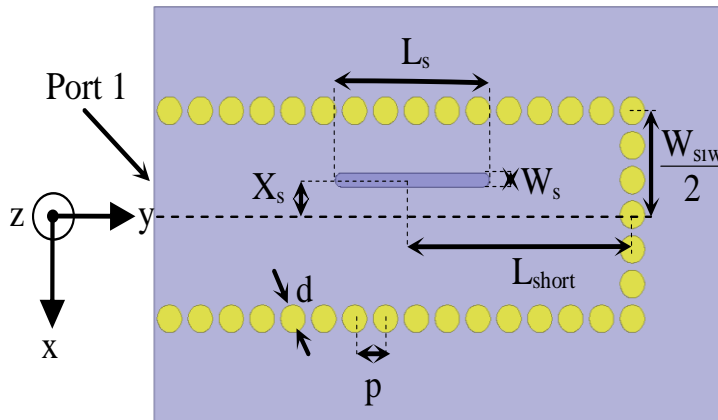


Figure 3.64: The radiating slot element designed for 8 x 1 slotted SIW array antenna

The same SIW diameter and period values in the earlier designs are used in the design of the 8 x 1 slotted SIW array antenna. The design parameters of the slot shown in Figure 3.64 are the distance between the short-circuited end of the SIW and the center of the slot L_{short} , the length of slot L_s , the width of slot W_s and the slot offset X_s . All 8 SIW structures have the same slot parameters in the design. The W_s value is selected to be 0.25 mm to apply narrow slot assumption which assumes only x-directed electrical field in the slot region shown in Figure 3.64, and hence, a longitudinal slot can be modeled as shunt admittance [78]. The value of these shunt admittances depends on X_s and L_s values and total admittance seen by the center of the slot toward the short circuited part of the SIW must be real for a good matching. For this reason, the short circuit at the end of the SIW must be converted to open circuit and proper X_s and L_s values should be determined to have purely real shunt admittance representing the slot.

The initial values of X_s and L_s are determined using characterization polynomials for different X_s and L_s values with the help of self-slot admittance characterization of single longitudinal slot [77]. The final values are obtained by optimization. To achieve open-circuit transformed to the terminals of the real admittance stem from slot, initial value of L_{short} must be selected as the quarter guided wavelength at the operating frequency ($\lambda_g = 9.099 \text{ mm}$). However, the initial value of L_{short} is selected to be $3\lambda_g/4$ to obtain the same termination effect because $\lambda_g/2$ is smaller than the half initial length of the slot. L_{short} is optimized according to the simulation results by starting from $3\lambda_g/4$ initial value. The optimizations are carried out in Ansoft HFSS using the initial values determined by the self-slot admittance characterization. The slot offsets and lengths are determined as shown in Table 3.5.

Table 3.5. Design parameters of the single radiating element (mm)

L_{short}	X_s	L_s	W_s
7.13	0.5	4.4	0.25

The simulation result (S_{11}) of the designed single radiating element is shown in Figure 3.65.

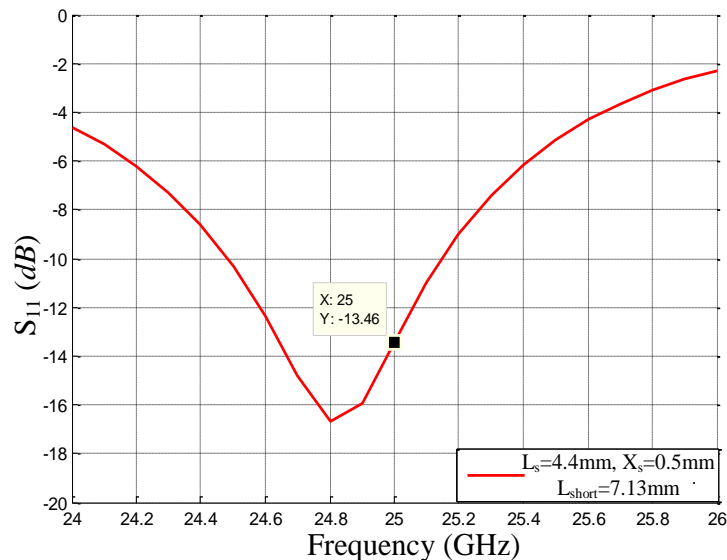


Figure 3.65: The simulation result (S_{11}) of designed single radiating element

As seen in Figure 3.65, the return loss is equal to -13.45 dB at 25 GHz and this means that the only $\% 4.52$ of the input power returns back to the input port. So, the designed radiating element is suitable to be used in the operating frequency.

An 8 element SIW antenna array is constructed by using the designed radiating element as shown in Figure 3.66.

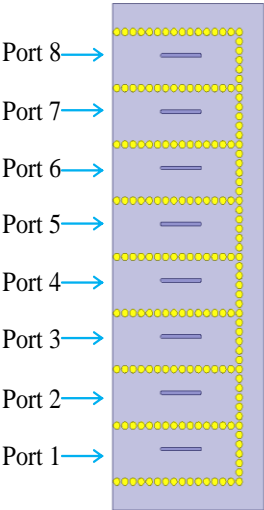


Figure 3.66: The designed 8 x 1 slotted SIW array antenna

To observe and eliminate the mutual coupling effect on the results, the designed 8 x 1 slotted SIW array antenna is fed simultaneously from all of the ports in the simulations. The ports are fed with the amplitude and phase values obtained from output ports of the designed 1 x 8 SIW power divider shown in Figure 3.53 and Figure 3.54. The active S parameters of the designed 8 x 1 slotted SIW antenna array are shown in Figure 3.67.

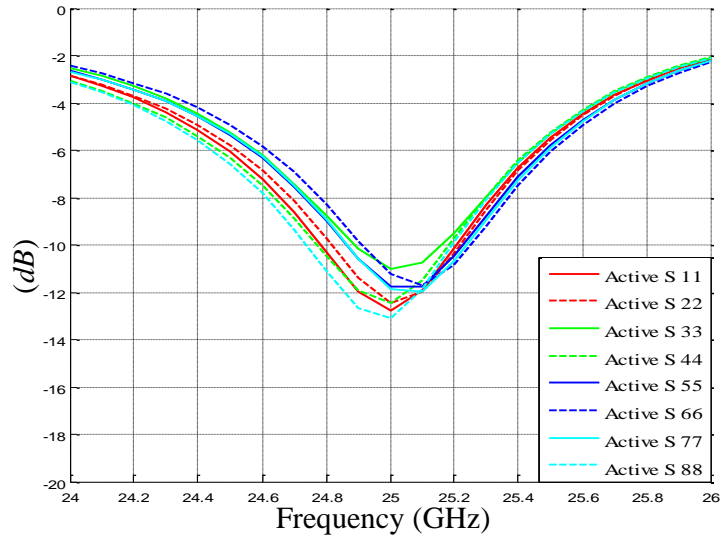


Figure 3.67: The active S parameters of the designed 8 x 1 slotted SIW antenna array

As can be seen in Figure 3.67, the active S parameters are below -10 dB , and hence, mutual couplings do not deteriorate the performance of the structure. The designed 8 x 1 slotted SIW antenna array is combined with the designed 1 x 8 SIW power divider. The combined structure is shown in Figure 3.68.

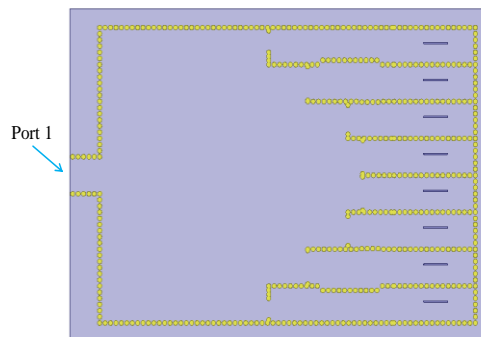


Figure 3.68: The combination of the designed 8 x 1 slotted SIW antenna array and 1 x 8 SIW power divider

The structure shown in Figure 3.68 is simulated with the determined parameter values. In order to improve input matching, the design parameters are adjusted and the exact values of the design parameters are determined from the optimization of the full structure. The exact values of the design parameters are presented in Table 3.6.

Table 3.6. The exact design parameters of the full structure (mm)

L_{short}	X_s	L_s
7.35	0.5	4.5

The simulation results of 8 x 1 slot array integrated with power divider structure using parameters presented in Table 3.6 are shown in Figure 3.69 (a) and (b).

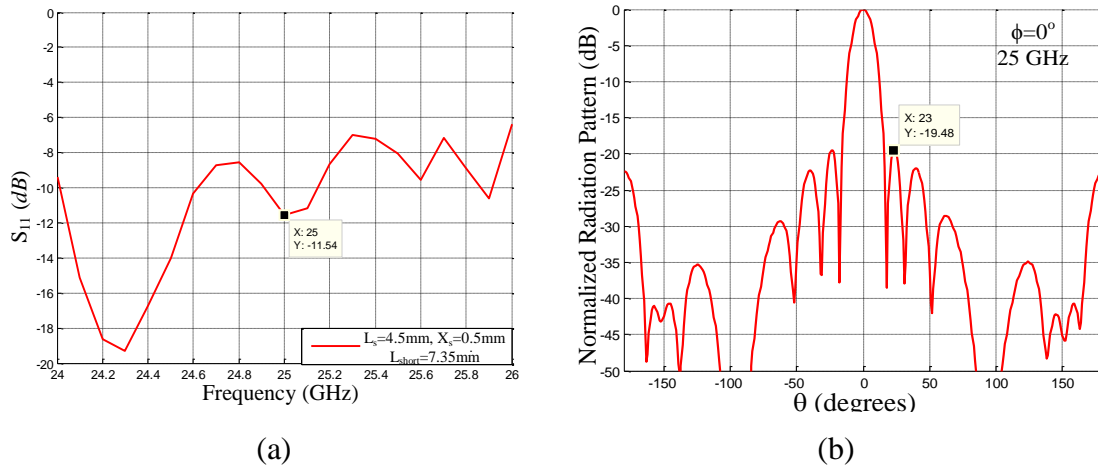


Figure 3.69: The simulation results of the designed full structure
(a) S_{11} , (b) Normalized radiation pattern

As seen in Figure 3.69 (a) and (b), the return loss is equal to -11.54 dB and the first SLL is equal to -19.48 dB . According to these results, it can be concluded that the structure has a good matching and the SLL is very close to the desired -20 dB level.

3.6.1.2. Production of 8 x 1 Slotted SIW Array Antenna

The designed microstrip line to SIW transition structure is added to the input of the designed 8x1 slotted SIW array structure shown in Figure 3.68 and the array is fabricated. The photograph of the fabricated structure is shown in Figure 3.70.

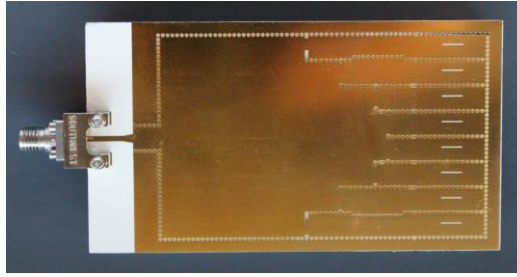


Figure 3.70: The photograph of the produced 8x1 slot array

The comparison of measurement and simulation S_{11} results of the fabricated structure is shown in Figure 3.71.

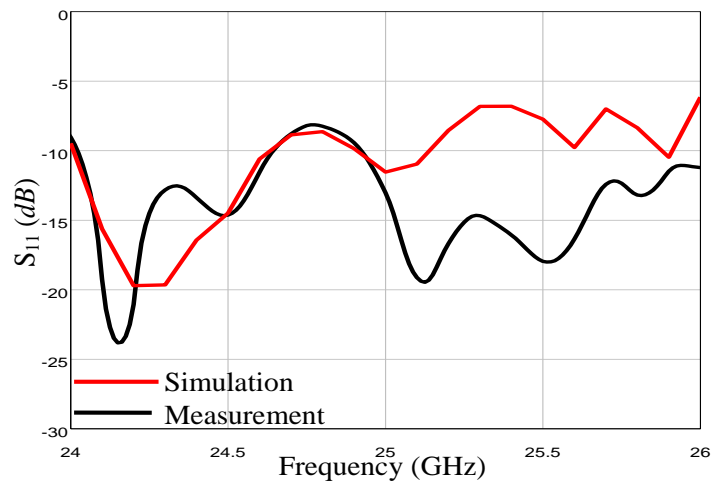


Figure 3.71: The comparison of the simulation and measurement results of the produced structure

As can be seen in Figure 3.71, the measured S_{11} results agree well with the simulated S_{11} results of the structure. Also, the radiation patterns of the fabricated array are measured using the measurement setup shown in Figure 3.72.



Figure 3.72: The measurement setup of the 8x1 slot array

The comparison of the simulated and measured normalized radiation patterns of the 8 x 1 slot array in two principal planes are shown in Figure 3.73.

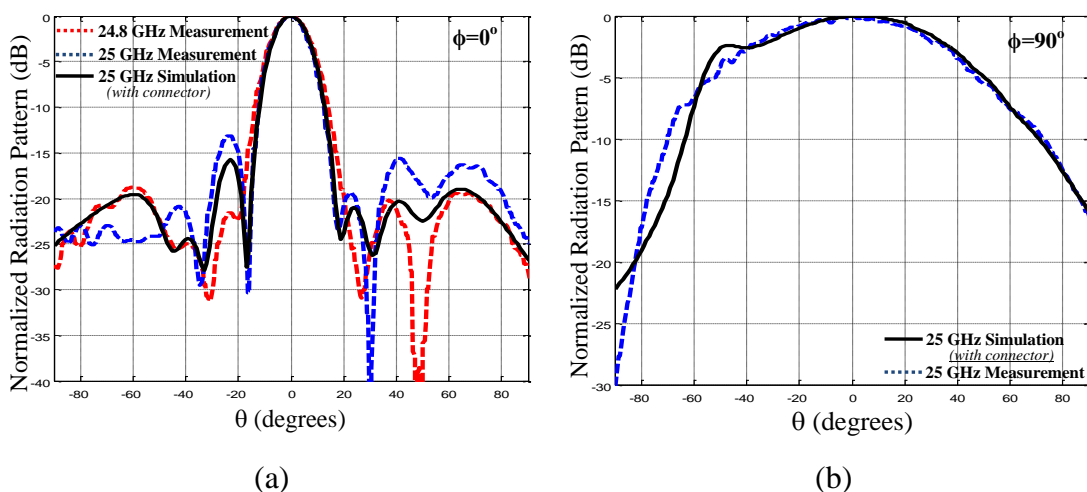


Figure 3.73: The comparison of the simulated and measured radiation pattern results of the 8 x 1 SIW power divider (a) E-plane, (b) H-plane

As seen in Figure 3.73, there are quite good agreements between the simulated and measured patterns at 25 GHz. It is observed that the pattern measured at 24.8 GHz has lower SLL than the others.

Diameter and period values of the SIW are the same as the previous designs that operate at the same frequency (25 GHz). Also, “ L_{short} ” and “ W_s ” values are selected as the values found in Table 3.5 in the 8 x 1 slotted SIW array antenna design. “ L_s ” and “ X_s ” values of the slots are determined with the help of design procedure of Elliot for small arrays of shunt slots [78] [79]. Determined design parameter values of the single antenna element of 8 x 4 slotted SIW array antenna are presented in Table 3.7.

Table 3.7. Design parameters of the single antenna element of 8 x 4 slotted SIW array antenna (mm)

L_{short}	X_s	L_s
7.13	0.223	4.002

The simulation result of the designed single antenna element is shown in Figure 3.75.

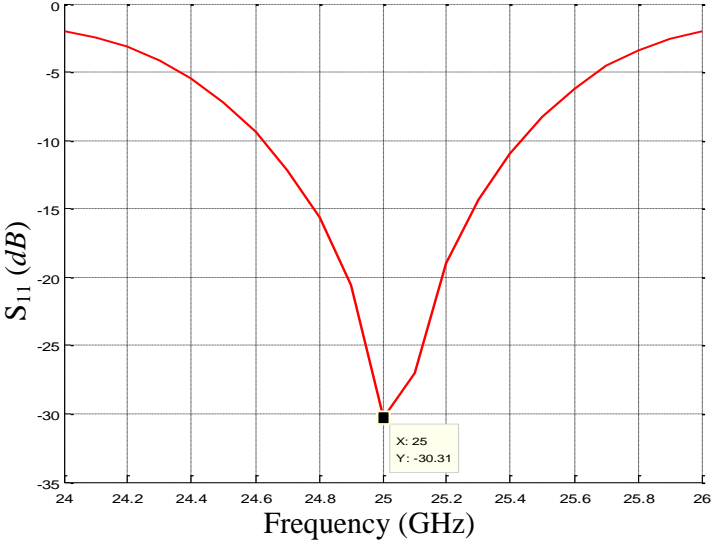


Figure 3.75: The simulation result (S_{11}) of designed single antenna element

As seen in Figure 3.75, the return loss is equal to -30.31 dB at 25 GHz . So, the designed radiating element is suitable for use in the operating frequency. The 8 x 4 SIW antenna array constructed using the parameters listed in Table 3.7 is shown in Figure 3.76.

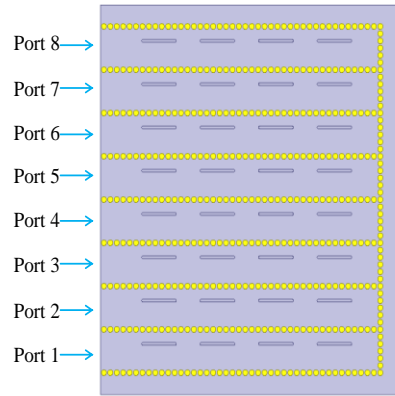


Figure 3.76: The designed 8 x 4 slotted SIW array antenna

To observe the mutual coupling effects, the designed 8 x 4 slotted SIW array antenna shown in Figure 3.76 is fed simultaneously from all of the ports with the amplitude and phase values obtained from the output ports of the designed 1 x 8 SIW power divider shown in Figure 3.53 and Figure 3.54. The active S parameters of the designed 8 x 4 slotted SIW antenna array is shown in Figure 3.77.

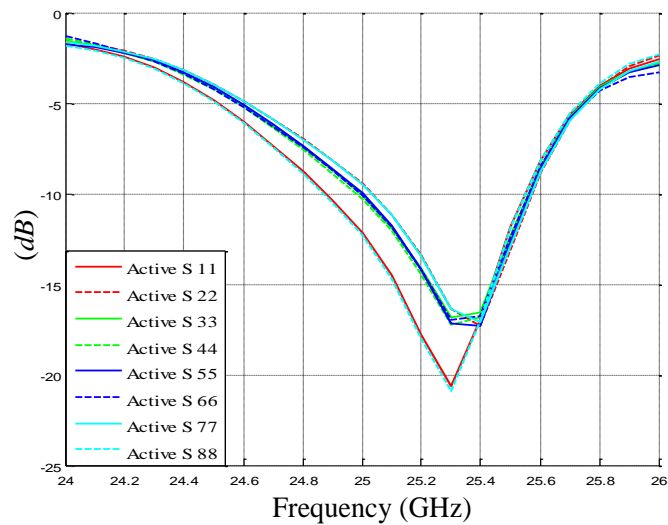


Figure 3.77: The active S parameters of the designed 8 x 4 slotted SIW antenna array

As seen in Figure 3.77, the active S parameters results are around 10 dB at 25 GHz . The designed 8 x 4 slotted SIW antenna array is combined with the designed 1 x 8 SIW power divider. The combined structure is shown in Figure 3.78.

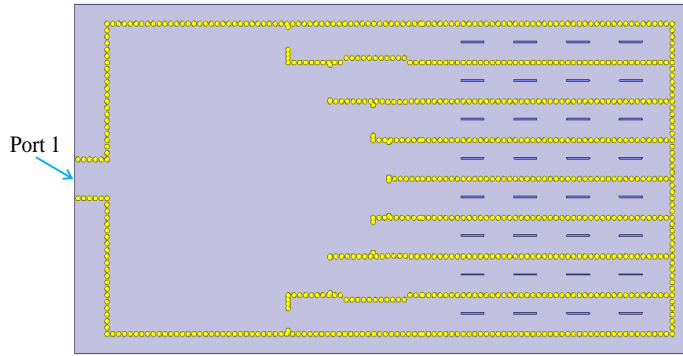


Figure 3.78: The combination of the designed 8 x 4 slotted SIW antenna array and 1 x 8 SIW power divider

The simulation results of designed full structure are shown in Figure 3.79.

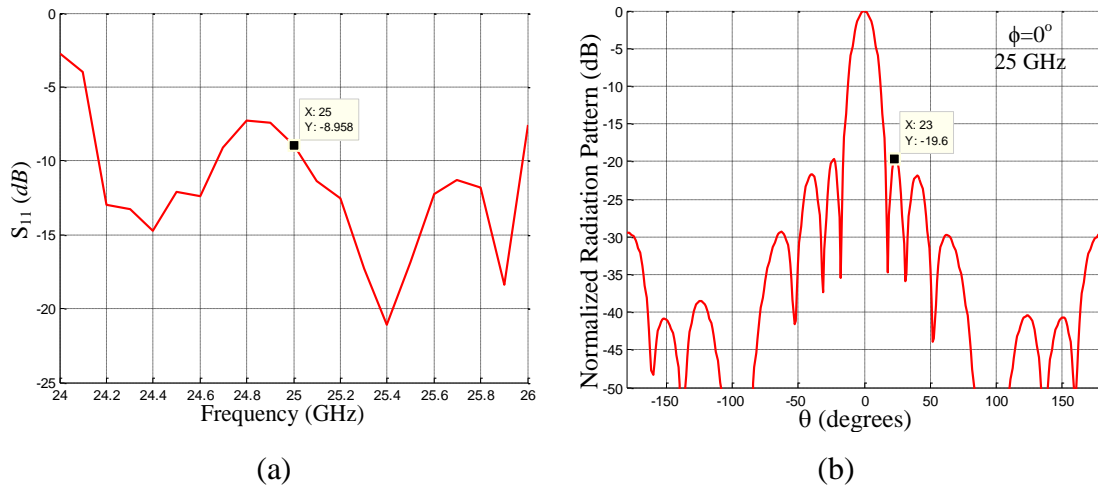


Figure 3.79: The simulation results of the designed 8 x 4 slotted SIW antenna array
(a) S_{11} , (b) Normalized radiation pattern

As can be seen in Figure 3.79 (a) and (b), the return loss is equal to -8.93 dB and SLL is equal to -19.6 dB . According to these results, the structure has a good matching and the SLL is very close to the desired -20 dB level as expected from the radiation pattern (shown in Figure 3.55) obtained by using the excitation coefficients at the output ports of the 1 x 8 power divider to excite the array elements.

3.6.2.2. Production of 8 x 4 Slotted SIW Array Antenna

The designed 8x4 slot array shown in Figure 3.78 is fabricated together with the designed microstrip line to SIW transition structure at the input port. The photograph of the fabricated structure is shown in Figure 3.80.

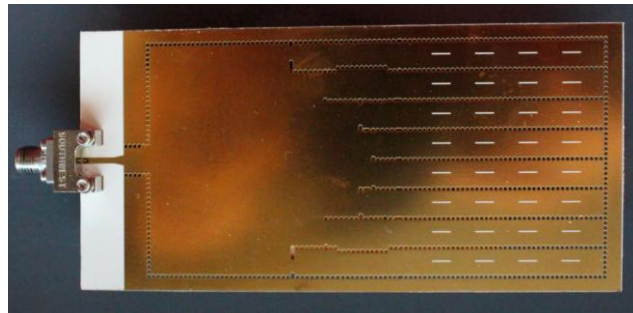


Figure 3.80: The photograph of the produced 8x4 slot array structure

The comparison of measured and simulated S_{11} results of the fabricated structure is shown in Figure 3.81.

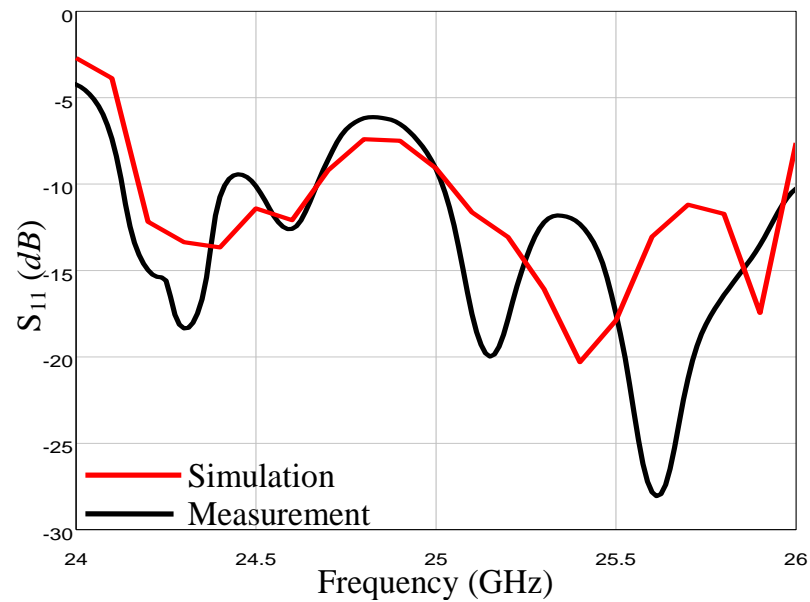


Figure 3.81: The comparison of measured and simulated results of produced 8 x 4 slot array structure

As can be seen in Figure 3.81, the measured S_{11} results agree well with the simulated ones. The normalized radiation patterns in two principal planes of the 8 x 4 slot array obtained from the simulations and measurements are compared in Figure 3.82.

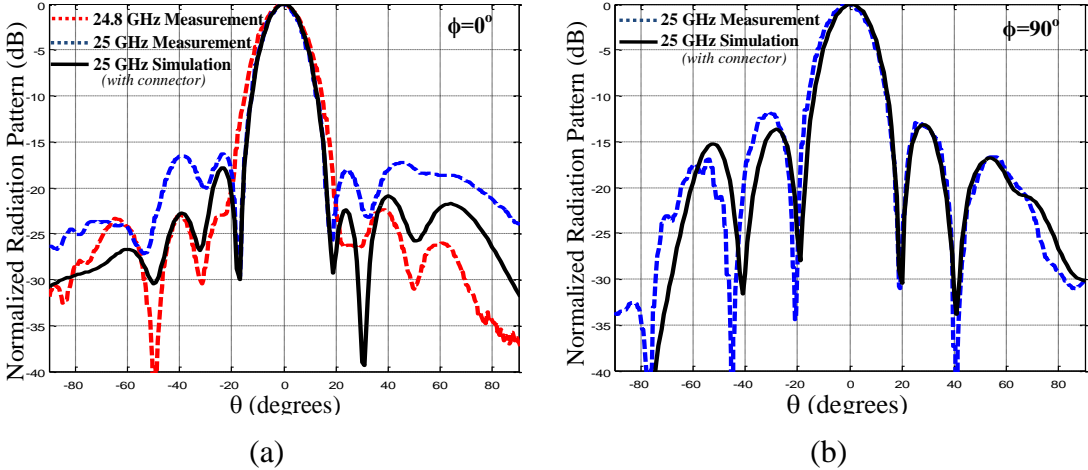


Figure 3.82: The comparison of the simulated and measured radiation pattern results of the 8 x 4 slot array

As seen in Figure 3.82, there is a good agreement between the simulated and measured results. The discrepancies may stem from the fabrication tolerances and the tangent loss prediction errors. It is observed that pattern measured at 24.8 GHz has lower SLL than the others.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

This thesis presents several power divider structures based on Substrate Integrated Waveguide (SIW) technology. Conducted research is three-fold in its scope. The first group of the established structures encompasses analysis, design and implementation of the 1 x 2 Y and T-Junction SIW power dividers, known as the conventional power divider types. These conventional divider types are designed, produced and measured successfully using SIW technology at 25 GHz . In the design and production of the 1 x 2 T SIW power divider, there is a good agreement between measured and simulated S_{11} and the difference between S_{21} is approximately $0.5 - 1\text{ dB}$. Likewise, there is a better agreement between the simulated and the measured S_{11} results of the 1 x 2 Y SIW power divider and insertion loss discrepancies in simulation and measurement are very slight and just around -0.4 dB at the operating frequency.

The second group of power divider studies is the analysis, design and implementation of the 1 x 4 SIW power dividers that are obtained by successive addition of the designed 1 x 2 SIW power dividers. These 1 x 4 power divider types are named as Y & Y and T & Y - Junction SIW power dividers. There is a good agreement between the S_{11} simulation and measurement results. The designed Y & Y and T & Y - Junction SIW power dividers have approximately 0.6 dB and 0.4 dB insertion loss differences between the measurement and simulation results respectively.

Development of a novel 1 x 8 unequal power divider is the main original contribution of this thesis study. This 8-way power divider designed and fabricated to have nearly the same phases and 20 dB SLL Taylor ($\tilde{n}=3$) amplitude distribution at the output ports in the operating frequency. The power divider is characterized by the measurements. It is shown that required amplitude distribution is obtained at the output ports. However, as expected it is a narrowband power divider. Also, two different standing wave slotted SIW array antennas have been designed as combined with the divider. These array antennas are fabricated and measured. The discrepancies between simulation and measurement results may stem from production imperfections and use of inaccurate tangent loss value at 25 GHz in the simulations.

Presented results can be improved or extended further with the following future works:

- The new SIW power divider designs can be performed that have different number of output ports.
- The operating frequency band of unequal SIW power divider can be enlarged with the help of new design techniques.
- Novel SIW dividers can be designed to further reduce the dimensions by using single and multilayer topologies.
- The losses of SIW dividers can be reduced with the help of the new low-loss substrate material investigations and improved production process.

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