SELECTION OF SUITABLE PWM SWITCHING AND CONTROL METHODS FOR MODULAR MULTILEVEL CONVERTER DRIVES

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ABSTRACT

SELECTION OF SUITABLE PWM SWITCHING AND CONTROL METHODS FOR MODULAR MULTILEVEL CONVERTER DRIVES

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The thesis focuses on the determination of suitable carrier based PWM switching and control method for modular multilevel converter drives. Characterization of various level-shifted and phase-shifted carrier based PWM methods are provided in terms of switching pulse patterns and resultant voltage waveforms both for N+1 and 2N+1 level output phase voltages. Modular multilevel converter PWM based control approaches are evaluated. Performances of different control methods are given for output harmonics distortion, submodule capacitor voltage ripple, circulating current ac component, efficiency and other criteria under equal switching count principle, for the dc/ac conversion step of a 10MW HVDC transmission system. Moreover, a 9.1MW induction motor drive application is studied from standstill to full speed range, giving attention to low frequency region operation. The study is conducted by means of mathematical analysis of the converter, topological and controller design, and detailed computer simulations.

Keywords: Modular multilevel converter, carrier based PWM, control, harmonics, submodule capacitor voltage, circulating current, efficiency, grid-interface, motor drive, simulation

ÖZ

MODÜLER ÇOK SEVİYELİ DÖNÜŞTÜRÜCÜ SÜRÜCÜLERİ İÇİN UYGUN DGM ANAHTARLAMA VE KONTROL YÖNTEMİNİN SEÇİMİ

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Bu tez modüler çok seviyeli dönüştürücü sürücüleri için uygun taşıyıcı tabanlı DGM anahtarlama ve kontrol yönteminin belirlenmesi üzerinde durmaktadır. N+1 ve 2N+1 seviyeli dönüştürücü çıkış faz gerilimleri için, çeşitli seviye kaydırmalı ve faz kaydırmalı taşıyıcı tabanlı DGM yöntemlerinin anahtarlama şablonları ve sonuç olarak meydana gelen gerilim dalga şekillerinin karakterizasyonu sağlanmaktadır. Modüler çok seviyeli dönüştürücülerin DGM tabanlı kontrol yaklaşımları değerlendirilmektedir. Farklı kontrol yöntemlerinin çıkış harmonik bozunma, altmodül kondansatörü gerilim kıpırtısı, dolaşım akımı ac bileşeni, verim ve diğer kıstaslar bakımından başarımları, 10MW'lık bir HVDC iletim sisteminin da/aa dönüşüm aşaması üzerinden karşılaştırılmıştır. Ayrıca düşük hız bölgesinde çalışmaya dikkat çekilerek, durma durumundan tam hızda çalışmaya kadar 9.1MW'lık bir endüksiyon motoru sürücüsü çalışılmıştır. Çalışma, dönüştürücünün matematiksel analizi, topolojik tasarımı, kontrolcü tasarımı ve ayrıntılı bilgisayar benzetimleri aracılığıyla gerçeklenmiştir.

Anahtar Kelimeler: Modüler çok seviyeli dönüştürücü, taşıyıcı temelli DGM, kontrol, harmonikler, altmodül kondansatör gerilimi, dolaşım akımı, verim, şebeke ara yüzü, motor sürücüsü, benzetim

To Göksu

and

My Parents

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LIST OF ABBREVIATIONS

APOD	Alternative Phase Opposition Disposition
CR	Carrier Rotation
HVDC	High-Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
MMC	Modular Multilevel Converter
PD	Phase Disposition
POD	Phase Opposition Disposition
PSC	Phase-shifted Carriers
PWM	Pulse-width Modulation
RMS	Root Mean Square
S&S	Sort and Select
S&S-RS	Sort and Select with Reduced Count of Switching
SM	Submodule
STATCOM	Static Synchronous Compensator
SVC	Space Vector Control
SVPWM	Space Vector Pulse-width Modulation
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

CHAPTER 1

INTRODUCTION

1.1. Background and Motivation

Energy is the most valuable and indispensable asset of countries from the very beginning of the human history. In the 20th century, electricity has become the dominant form of energy due to its ease of conversion to other forms. Today, the modern civilization based its operation on an increasing energy demand, substituting human activities with complex and sophisticated machines mainly run by electric power. Indeed, the world energy consumption is expected to increase by more than 54% every ten years [1]. Electricity will be more dominant than ever while supplying this energy demand since the countries try to bypass especially fossil fuels in the supply chain of energy. Therefore, it is obvious that the need of electricity will increase tremendously day after day. In order to meet the increasing demand, electric power generation, transmission, distribution and conversion become more and more important.

The recent attention in environmental protection and preservation has lead countries to shift to sustainable and renewable energy sources. Electric power generation from solar and wind energy is wide spread today. These resources will diffuse and occupy an increasingly important role in energy production in coming years. Therefore, the need of high quality electric power conversion systems to be used in this area is greater than ever.

From the beginning of the 21st century, many countries have chosen to deregulate their electricity market. The situation resulted in a mix of energy sources while pursuing higher efficiency, particularly with the introduction of private investments in the energy market.

In the light of above mentioned events, in order to accomplish all requirements both from users and legal regulations, and to reduce the environmental impact, power conversion and control is needed to be reliable, safe, efficient, and available.

Voltage Source Converter (VSC) technology has been becoming common in many of modern demanding electric power systems, such as high-voltage direct current (HVDC) transmission systems (especially in offshore wind power transmission), medium-voltage motor drives, STATCOM applications, electric traction/propulsion systems or grid connected energy storage systems. Today, the majority of the applications of these electric power systems are driven by conventional two- or three-level VSC's. However, these conventional VSC's are not able to respond properly to emerging requirements such as high power, high efficiency, reliability of the system, and environmental compatibility. The solution to these problems has been evolved through the use of combinable, standardized, distributed, and simpler converter structures with lower voltage steps. Indeed, standardized and distributed systems have become the recommended solution to achieve modern projects requirements in all engineering areas. These configurations provide a more reliable operation, facilitates fault diagnosis, maintenance, and reconfigurations of control system. Especially in fail safe situations, distributed configuration allows control system to isolate the problem, drive the process in safe state easily, and in many cases allows continuing almost normal operation in faulty conditions.

Multilevel converters have been progressed as significant competitors to the conventional VSCs in order to overcome the abovementioned limitations. At present, modular multilevel converter (MMC, MMLC, M2LC, M2C) (Figure 1.1) is at the heart of research and development studies in power electronics area, both for

academic and industrial scope. Its unique chopper cell based topological structure was firstly proposed by Lesnicar and Marquardt in 2003 [2]. The initial target was very high-voltage applications, especially network interties in power generation and transmission. Since then, the topology had a great attraction due to its promising features. Compared to conventional VSC technology, MMC offers advantages such as higher voltage and power levels, modular and redundant construction, longer maintenance intervals, improved reliability, and higher efficiency.

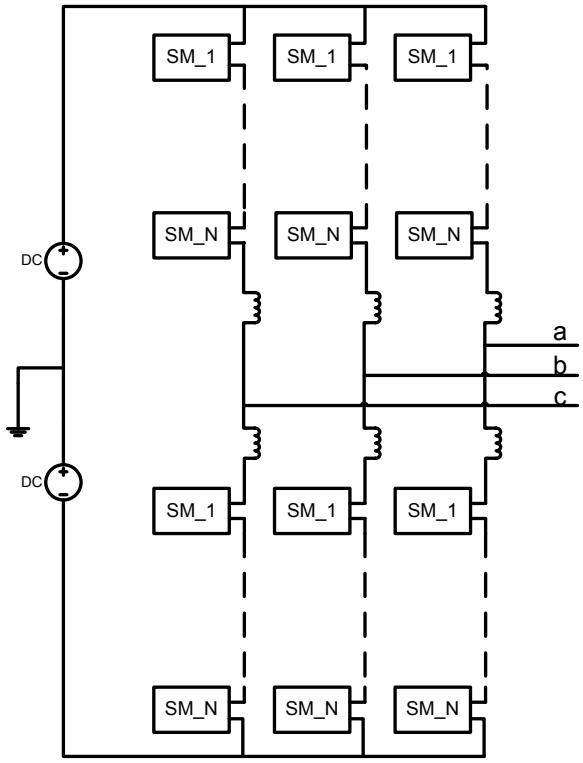


Figure 1.1 Modular multilevel converter

Synthesis of output voltage waveform in conventional two- or three-level VSCs is done by reflecting half of the dc-link voltage to the output, which results in high harmonic content and requirement for output harmonic filters which increase both the cost and footprint of the system. On the other hand, that of the MMC topology is based on the sum of small voltage steps reducing harmonic content, and removing

the need of harmonic filter at the output. Output voltage synthesis concepts of two, three and multilevel converters are illustrated in Figure 1.2.

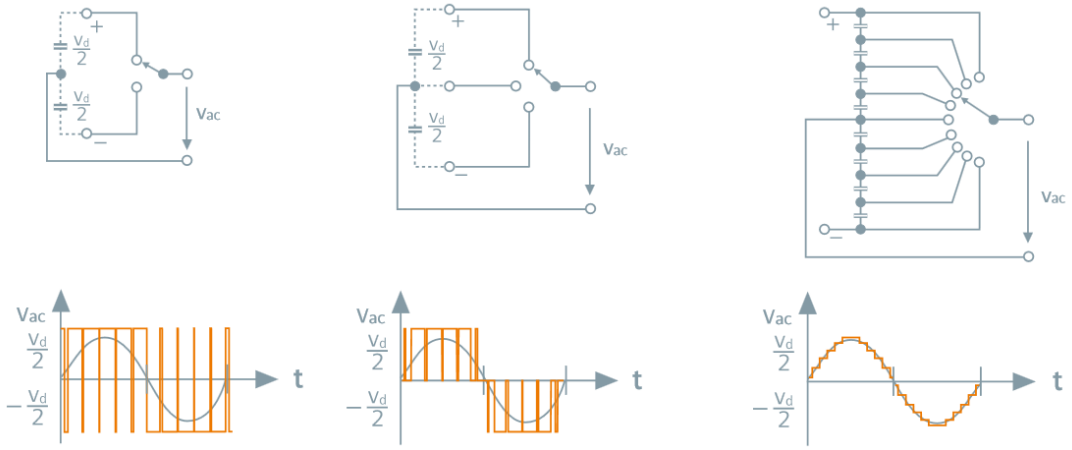


Figure 1.2 Output voltage synthesis concepts of two, three and multilevel converters [4]

1.1.1. Typical Application Areas of MMC

HVDC transmission is an important and efficient alternative to three-phase ac transmission of electric power over long distances. Advantages for choosing HVDC transmission instead of three-phase ac transmission can be numerous and should be considered in individual situation apart. However, the mostly acknowledged advantages could be summarized as follows: lower transmission losses, the capacity to transfer more power over the same right of way, the ability to interconnect systems that are not synchronized or using different frequencies, short-circuit currents limitation, long distance water crossing capability. One of the most important advantages of HVDC transmission on ac transmission is the ability of controlling active power transmission accurately, while ac lines power flow cannot be controlled in the same direct way. Moreover, in [3] it is shown that the cost of HVDC transmission is less than ac transmission above a distance of 800km overhead line or 50km underground or submarine cables. This is due to the fact that the higher cost of HVDC converters is overcome by the cost of reduced number of

transmission line conductors. Figure 1.3 shows the cost estimations for ac and HVDC transmission by distance via overhead line and submarine or underground cable.

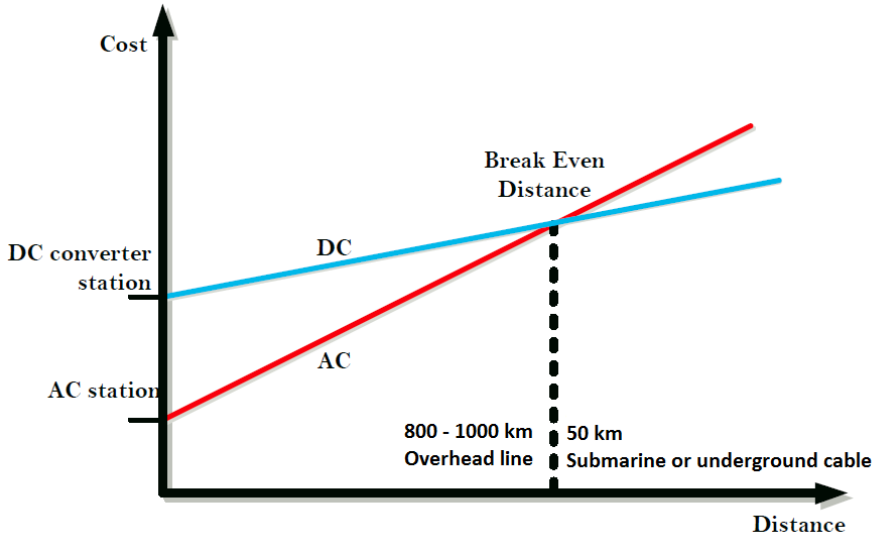


Figure 1.3 Cost estimations for ac and HVDC transmission by distance [3]

Today, HVDC technology has evolved from current source converters to voltage source converters, and even more to modular multilevel converters. Its smaller footprint due to smaller filter size or even no filter at the output, made the topology especially suitable for offshore wind farm HVDC transmission systems to the mainland. There are various commercial products with brand names "HVDC Plus" (Siemens) [4], "HVDC MaxSine" (H-bridge based, Alstom) [5] and "HVDC Light" (ABB) [6]. In Table 1.1, several HVDC projects based on MMC concept are shown. An offshore wind power station HVDC platform is shown in Figure 1.4 and a submodule and the MMC structure of MaxSine (Alstom) are shown in Figure 1.5.

Table 1.1 Several HVDC projects based on MMC concept [70], [71]

Project	**Installed year**	**Manufacturer**	**Dc-link voltage (kV)**	**Power (MW)**	**Location**
Trans Bay Cable	2010	Siemens	±200	400	USA
Caprivi Link	2010	ABB	350	300	Namibia-Zambia
Valhall	2011	ABB	150	78	Norway
BorWin2	2013	Siemens	300	800	Germany
HelWin1	2013	Siemens	259	576	Germany
DolWin1	2013	ABB	±320	800	Germany
East West Interconnector	2013	ABB	±200	500	UK-Ireland
SylWin1	2014	Siemens	±320	864	Germany
South-West Link	2014	Alstom	N/A	1440	Sweden
Mackinac	2014	ABB	±71	200	USA
Skagerrak 4	2014	ABB	500	700	Norway-Denmark
BorWin1	2015	ABB	±150	400	Germany
HelWin2	2015	Siemens	±320	690	Germany
DolWin2	2015	ABB	±320	900	Germany
INELFE	2015	Siemens	±320	2x1000	France-Spain
Aland	2015	ABB	±80	100	Finland
Troll A 3-4	2015	ABB	±60	2x50	Norway
Nordbalt	2015	ABB	±300	700	Sweden-Lithuania
Tres Amigas Superstation VSC	2016	Alstom	345	750	USA
BorWin3	2019	Siemens	±320	900	Germany

Figure 1.4 HelWin2 offshore HVDC platform by Siemens [8]

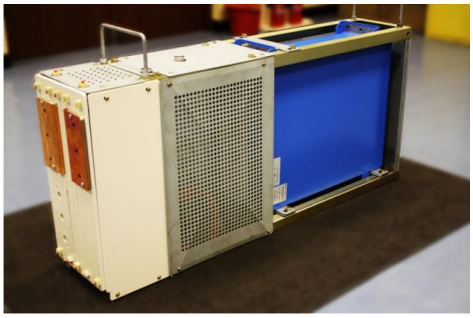


Figure 1.5 Submodule (up) and MMC (down) structure of MaxSine (Alstom) [7]

Medium-voltage motor drives are another application area of MMC. Many researchers and manufacturers are working on the issue. The medium-voltage drives cover power ratings from 250kW to more than 100MW at the medium-voltage (MV) level of 2.3 to 13.8kV. In this way, the majority of the installed MV drives are in the 1 to 4 MW range with voltage ratings from 3.3kV to 6.6kV [9]. One of the major markets for the MV drive is retrofit applications intended to improve the efficiency and achieve energy saving. It is reported that 97% of the currently installed MV motors operate at a fixed speed; only 3% of them being driven by variable speed drives [9]. For pump/blower like motors, fixed speed operation results in a substantial amount of energy loss because of mechanical methods used for control of fluid. It is reported in [10] that an MMC based motor drive for a converter-fed synchronous machine for pumped hydro storage plant with a power rating of 100MVA has been installed in Switzerland in 2013 by ABB (Figure 1.6). Currently, commercialization of MMC based motor drives is not as wide spread as in HVDC case. However, there is a big opportunity for MMC to penetrate into the variable frequency motor drive applications, since the need of efficiency improvement in this field, as explained above.

Figure 1.6 MMC based motor drive for a converter-fed synchronous machine by ABB and Oberhasli Hydroelectric Power Company in Switzerland [11]

As mentioned, STATCOM applications are one of the fields for MMC to penetrate in. In order to improve dynamic stability and power quality of power systems which have been deregulated and liberalized especially from the beginning of the 21st century, STATCOM applications are widely used. The MMC topology provides improved dynamic stability of transmission systems, increased power quality, flexibility to adapt to different power ratings, compact design with low footprint as well as redundancy and minimized engineering costs to STATCOM systems. Different manufacturers have MMC based STATCOM systems, some of which are SVC Plus (full-bridge based, Siemens) [72] and SVC Light (full-bridge based, ABB) [73]. In Table 1.2, several STATCOM projects based on MMC topology and in Figure 1.7 an example of projects are shown.

Table 1.2 Several STATCOM projects based on MMC concept [74], [75]

Project	**Installed year**	**Manufacturer**	**System voltage (ac)(kV)**	**Power (MVAr)**	**Location**
Kikiwa	2009	Siemens	220	2x(±50)	New Zealand
The Thanet offshore wind farm	2009	Siemens	11	N/A	UK
Mocuba	2010	Siemens	33	N/A	Mozambique
Cerro Navia	2011	ABB	220	+65/ -140	Chile
The Greater Gabbard offshore wind farm	2011	Siemens	13.9	N/A	UK

Figure 1.7 Kikiwa STATCOM project based on MMC by Siemens [12]

1.2. Scope of the Thesis

As explained in section 1.1, MMC was firstly proposed in 2003 and it is still in the development progress. Thus, it is a topical subject in academic and industrial research studies at present. From the advent of the topology, many studies have been carried out for the modulation, control, modeling, design and protection of the converter.

The framework of the thesis is selection of suitable carrier based PWM method and control technique for MMC topology used for used for grid-interface and electrical motor drives. The procedure also involves devising the optimal circuit parameters. Then, the design is verified by means of detailed computer simulations and

computer based mathematical tool outputs with different PWM and control techniques. Several power ratings are considered to provide a thorough performance evaluation of the designed system.

The main objectives of this thesis are:

i. Evaluation and discussion of MMC among other VSCs and multilevel converter topologies
ii. Studying the basic operation principle of MMC topology
iii. Evaluation and comparison of different carrier based PWM techniques of MMC
iv. Analysis and comparison of different control strategies of MMC
v. Design, simulation, and performance analysis of a grid connected MMC system
vi. Design, simulation and performance analysis of an MMC based motor drive

Carrier based PWM techniques for MMC are widely studied [13]-[15]. There are several studies that consider carrier based PWM methods for MMC switching. One of the earliest studies [15], introduces LS PWM methods and compares their performances. Carrier based PWM methods comparisons for specific m_a (amplitude modulation index) and m_f (carrier to fundamental frequency ratio) values are given in [16] and [17]. Another work [13], also rates sinusoidal PWM methods, for specific m_a and m_f values in terms of harmonics performances. Variations in the output voltage levels are studied in [18]. However, still there is a need for a systematic analysis and comparison of different carrier based PWM methods. Switching pulse patterns, and output harmonics of methods should be analyzed with equal switching count per leg. In high power systems, which are the main application area for MMC, minimum switching losses are aimed. The energy cost lost for the switching or cooling system cost for the converter sums up to big amounts, because of the high power rating of the converter. Therefore, it is

important to evaluate the methods with equal switching count principle, keeping the switching losses low and similar to each other. The first main contribution of this thesis is to provide the fundamental characteristics of different carrier based PWM methods, level-shifted and phase-shifted carriers, used for MMC switching. Pulse pattern, switching manner and output harmonic content of PD, POD, APOD and phase-shift methods are investigated under equal total count of switching in a phase leg principle, throughout broad m_a and m_f ranges. Also, principles of switching methods for N+1 and 2N+1 phase-to-neutral output voltage levels are explained.

Control of MMC with different control approaches are studied in [19]-[24]. Output power control, circulating current control and submodule capacitor voltage balancing techniques are explained. However, there is no general agreement about the suitability of the characteristics and comparison of different control strategies. Systematizing the analysis and evaluation of control and modulation strategies for MMCs are still need to be studied. The second main contribution of the thesis is to provide the performance comparisons of different MMC control techniques with N+1 and 2N+1 phase voltage levels, in terms of output harmonic content, submodule capacitor voltage ripple and circulating current ac component for a grid connected system under different loading conditions.

Motor drive with MMC is intensively studied at present. Being relatively a developing area compared to HVDC and STATCOM, motor drives, especially the low frequency region where MMC is problematic, are the topical subject for MMC studies [10], [25]-[31]. In this thesis, a motor drive application with MMC is considered. Low frequency operation of the converter is covered with a multi MW electrical machine. From the start-up, low frequency operation of the machine as well as steady state high frequency operation with a fan/blower like load is presented and characteristics of the converter such as submodule capacitor voltages, circulating current and arm currents under these circumstances are given.

This thesis consists of nine chapters.

Chapter 2 gives the classification of multilevel converters. Diode-clamped, capacitor clamped and submodule based (cascaded H-bridge and MMC) multilevel converters are considered. Submodule structures, specifically full-bridge and chopper cell, are detailed. Characteristics, topological features, and switching of these converters are covered. Advantages and disadvantages of different topologies are listed. Additionally, the power semiconductors used in multilevel converters are explained. Thyristor, IGBT and IGCTs are considered and their characteristics are provided.

Chapter 3 gives the mathematical model and circuit analysis of MMC. Topological structure of the converter is provided in detail. Upper/lower arm and phase leg quantities, current and voltage loops, energy and power equations of the converter are analyzed. State variables for the control of the converter are detected.

Chapter 4 provides a comprehensive explanation of switching methods for MMC. Low frequency and high frequency switching methods are classified. Application and characteristics of these methods are provided and carrier based PWM methods analyzed deeply. Level-shift and phase-shift methods are detailed. Switching pulse patterns, resultant output voltage waveforms and their harmonic contents are analyzed, throughout broad m_a and m_f values. Moreover, the branching in the application of carrier based PWM methods to the converter which results in N+1 or 2N+1 phase-to-neutral voltage levels at the output is shown.

Chapter 5 discusses the component rating determination of MMC. Number of submodules per arm, submodule capacitor and arm inductor values are the fundamental design issues of MMC. Right choice of these values is critically important in the waveform quality, efficiency and initial cost of the converter. The determination processes are covered mathematically.

In chapter 6, control of MMC with carrier based PWM methods is considered. The fundamental control targets of the converter, output power control, submodule capacitor voltage balancing control, and circulating current ac component

suppression control, are introduced. The mostly acknowledged control approaches in the literature, direct modulation and phase-shifted carrier based control, are detailed. Application of the control methods and determination of control parameters are given.

Chapter 7 merges the content studied in the previous chapters and uses them as background and input to the analyses conducted herein. In this chapter, a grid connected MMC is designed and simulated. For the dc/ac conversion step of a 10MW HVDC system, MMC component ratings are determined and the converter is run by different control and carrier based PWM methods for different loading conditions. Comparisons of different control and modulation methods are done in terms of output harmonics performance, submodule capacitor voltage ripple, circulating current ac component, and efficiency with equal switching count per phase leg principle. By this way, the suitable control and modulation method for the mentioned criteria are discovered.

In chapter 8, motor drive application of MMC is explained. The problems of the topology in motor drive applications are clarified. The solution methods to these problems found in the literature are provided and one of them is verified via a 9.1MW induction machine simulation from the start up to the full speed range.

Finally, the thesis concludes with a summary of information and experience gained throughout the study. Developments and future work are also addressed.

CHAPTER 2

MULTILEVEL CONVERTER TOPOLOGIES

2.1. Introduction

The concept of multilevel converters goes back to the mid 1970s. Baker and Bannister gave the very first examples of the multilevel topology [34]. The topology was achieved by connecting single-phase inverters in series. Separate dc sources were used to build up multilevel voltage at the output.

In conventional two-level voltage source converters, the converter simply connects the positive or negative dc-link voltage to the output; and in three-level converters, an additional neutral voltage is seen at the output. Therefore the signal created on the ac side of two- or three-level converters is a series of pulses containing the required fundamental frequency and higher harmonic signals, which can be removed by appropriate filters. Multilevel converters, on the other hand, synthesize smaller voltage steps in a sinusoidal manner at the ac output terminals which are obtained either from capacitors or separate dc sources. As the number of voltage levels increase at the ac side, generated voltage waveform is much like a sinusoid. Therefore, output voltage harmonic distortion of the multilevel converters is much less than two- or three-level converters, which is the principal advantage of multilevel converters over two- or three-level converters. Other advantages of multilevel converters can be listed as below:

- Multilevel converters, especially submodule based ones, are easily expandable to broad power and voltage levels, by simply increasing the series connected submodule number.

- Due to stepped output waveform, voltage change speed, namely dv/dt rate, is reduced, also reducing electromagnetic compatibility problems.

- Multilevel converters can be switched at lower frequencies (even at fundamental frequency). Thus, switching losses per switching device decrease and semiconductor thermal management can be handled easier.

- Input current distortion and output common-mode voltage of multilevel converters are lower compared two-level converters.

- Multilevel converters are relatively independent from the fast changing state of the art of semiconductor devices. They can be made up using standard and proven semiconductor devices.

- In conventional two-level converters, a number of semiconductors should be serially connected and operated simultaneously. A delay of operation among one of them results in a failure. However, in multilevel converters, the voltage ratings of semiconductors are limited by the voltage level step size, enabling single semiconductor usage. Therefore, failure rates of multilevel converters are lower.

On the other hand, the two basic disadvantages of multilevel converters are listed as below:

- Multilevel converters consist of a greater number of semiconductors and circuit elements, increasing their initial cost.

- Switching and control of multilevel converters are more difficult than two-level converters because of their complex topological structures.

2.2. Classification of Conventional Multilevel Converter Topologies

2.2.1. Diode-Clamped (Neutral-point-clamped) Multilevel Converter

Diode-clamped multilevel converter was proposed by Nabae, Takahashi, and Akagi in 1981 [35]. Several papers had been published in the 1990s covering four-, five- or six-level diode-clamped multilevel converters for static VAR compensation, variable speed motor drives, and high-voltage system interconnections. A phase leg of five level diode-clamped converter and its output voltage waveform are shown in Figure 2.1. Each of the phases shares a common dc-link, which is subdivided into five levels, $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$ and $V_{dc}/2$, by four capacitors. All the capacitors are charged to $V_{dc}/4$ and the voltage stress across the switching devices is limited to $V_{dc}/4$ through the clamping diodes. However, the clamping diodes need to block different voltage levels; D1 and D3' being $V_{dc}/4$, D1' and D3 being $3V_{dc}/4$, D2 and D2' being $V_{dc}/2$. Table 2.1 shows the required switch states for the desired output voltage of the five-level converter, "1" corresponding to the switch is "ON" and "0" to "OFF".

The diode-clamped multilevel converter has 2N-1 voltage levels line-to-line if used as three-phase converter, where N being the number of per phase-to-neutral voltage levels. Therefore, a single-phase five-level converter as in Figure 2.1 has nine voltage levels line-to-line when used as three-phase.

The diode-clamped multilevel converter was initially built up in order to expand the power ratings of converters to megawatt ranges other than paralleling or series connecting the power semiconductors. Today, the converter is utilized in many few kilowatts to megawatt applications, including general purpose adjustable speed drives. However, the converter has the drawback of increasing complexity of control and capacitor voltage balancing problems as the number of voltage levels increase.

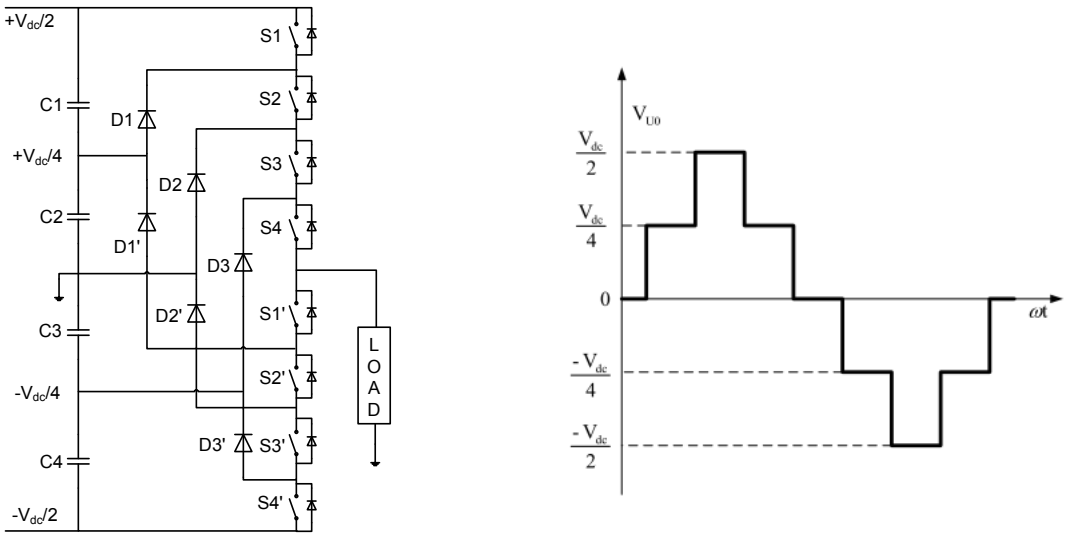


Figure 2.1 Single-phase five-level diode-clamped converter at left and output voltage waveform at right

Table 2.1 Switch states for the desired output voltage of the five level converter

Output Voltage	S1	S2	S3	S4	S1’	S2’	S3’	S4’
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/2$	0	0	0	1	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

2.2.2. Flying Capacitor (Capacitor-Clamped) Multilevel Converter

Flying capacitor multilevel converter was proposed by Meynard and Foch in 1992 [36]. The topology is similar to diode-clamped converter except for clamping diodes, whereas in flying capacitor topology, capacitors are used for clamping purpose. A phase leg of five level flying capacitor converter and its output voltage waveform are shown in Figure 2.2. Each of the phases shares a common dc-link, which is subdivided into five levels, $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$ and $V_{dc}/2$, by four capacitors. The required number of dc-link capacitors for N level converter is N-1 and auxiliary capacitors is (N-1) x (N-2) / 2. Table 2.2 shows the required switch

states for the desired output voltage of the five-level converter, again "1" corresponding to the switch is "ON" and "0" to "OFF".

The topology has the advantage of phase redundancy for inner voltage levels; in other words, a desired output voltage may be obtained by two or more switching combinations. This feature can be exploited appropriately for capacitor voltage balancing issue. However, as the number of voltage levels increase, again control of the converter and capacitor voltage balancing become highly complicated. Also the number of required capacitors increases dramatically, resulting in increase of cost, and also packaging and dimension problems of the converter. The topology is mainly employed for utility power electronics applications [93]-[94].

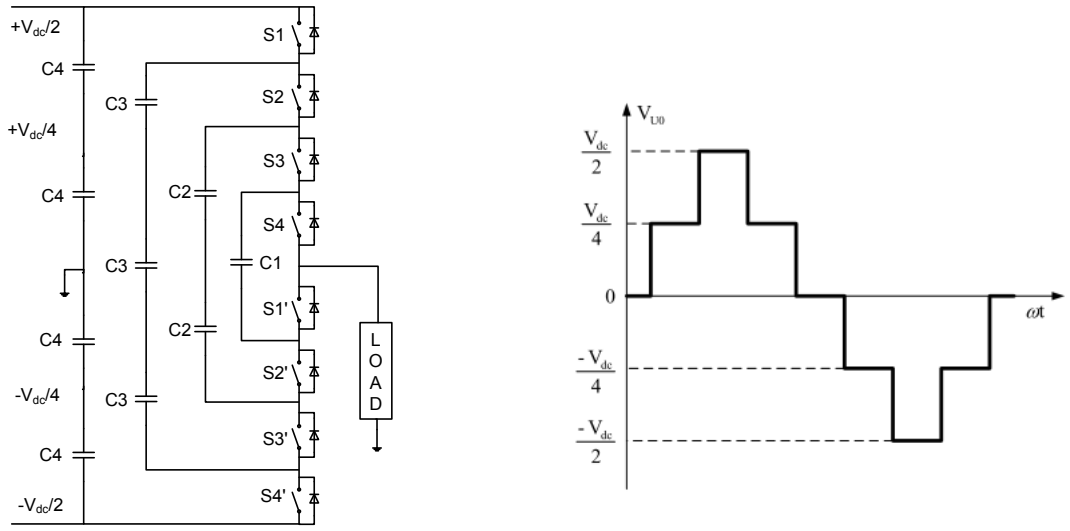


Figure 2.2 Single-phase five level flying capacitor converter at left and output voltage waveform at right

Table 2.2 Switch states for the desired output voltage of the five-level converter

Output Voltage	S1	S2	S3	S4	S1’	S2’	S3’	S4’
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$- V_{dc}/2$	1	0	0	0	1	1	1	0
$- V_{dc}/4$	0	0	0	0	1	1	1	1

2.3. Submodule Based Multilevel Converters (Modular Multilevel Cascade Converters)

Apart from conventional multilevel converter topologies explained in the previous chapter, the most attractive topology for the researchers have been the submodule based multilevel converters which are also called as modular multilevel cascade converters.

Submodule based multilevel converters have three degrees of freedom in their circuit topology: one is connection of submodules to each other, being either star or delta connection. The second is the circuit topology of the submodules, being half-bridge (chopper cell) or full-bridge (H-bridge). Moreover, from the point of usage of delta connected or star connected clusters (serially connected submodules) as a single cluster or dual clusters, the third degree of freedom is obtained in terms of converter topology. As a result, theoretically 2^3=8 different converter topologies are present for submodule based multilevel converters. However, not all of them are practically implementable. Table 2.3 shows all the possible variations by a tick corresponding to an implementable topology or by a cross corresponding to an irrelevant topology [37].

Table 2.3 Submodule based multilevel converter topology variations

	Star		Delta	
	Single	Double	Single	Double
Chopper	x	✓	x	x
Full-bridge	✓	✓	✓	x

The four practically implementable submodule based multilevel converter topologies are listed as below and illustrated in Figure 2.3 and Figure 2.4 [38]:

i. Single-Star Bridge-Cells (SSBC)
ii. Single-Delta Bridge-Cells (SDBC)
iii. Double-Star Chopper-Cells (DSCC)
iv. Double-Star Bridge-Cells (DSBC)

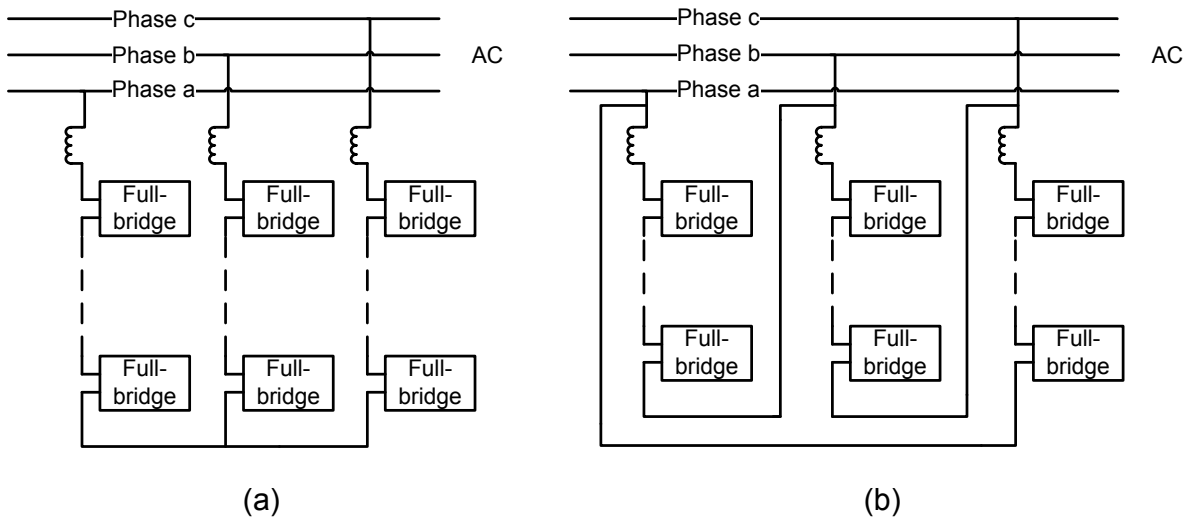


Figure 2.3 (a) SSBC (b) SDBC

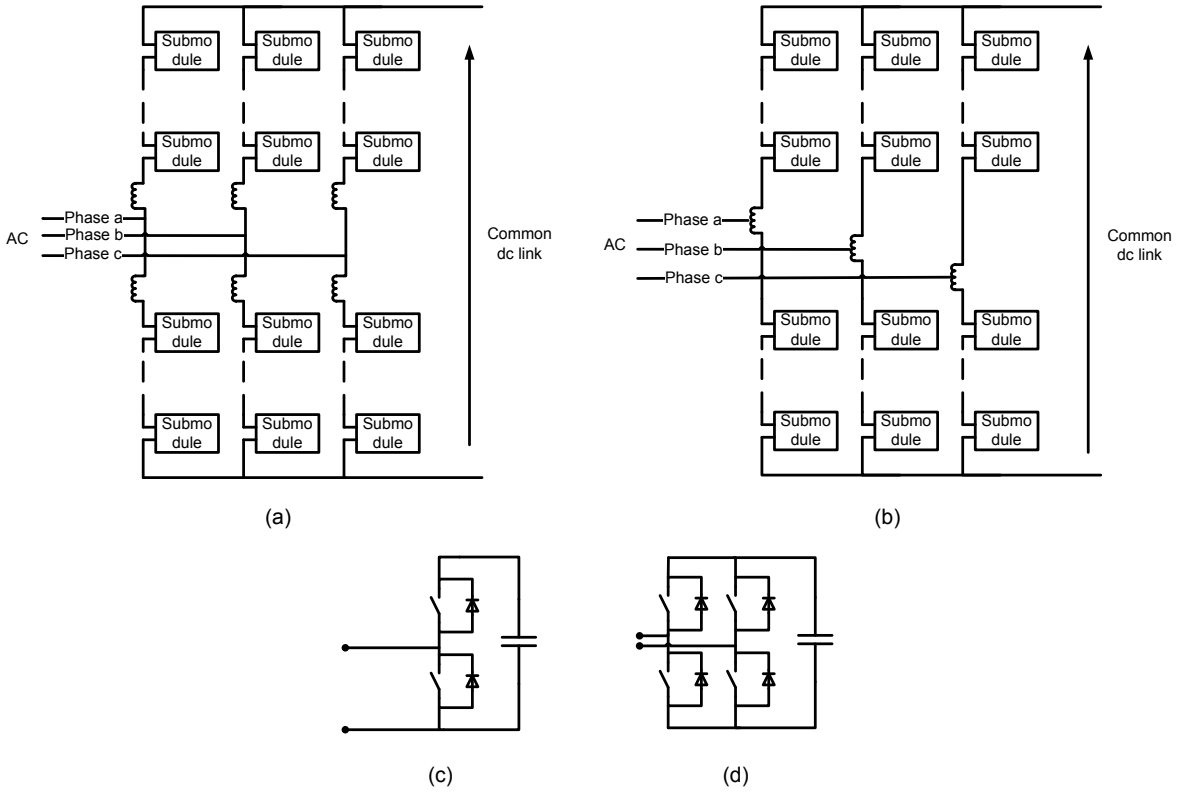


Figure 2.4 Possible circuit configurations of DSCC and DSBC (a) Power circuit using coupled arm inductors (b) Power circuit using non-coupled arm inductors (c) Chopper cell (DSCC) (d) Bridge cell (DSBC)

Irrelevance of the other four topologies could be explained as follows: As Figure 2.3 (b), SDBC topology, is investigated, it is realized that "double-delta" structure is irrelevant since in delta connection, there is no common neutral point as in star connection. Therefore, a double-delta structure is actually equivalent to two separate parallel connected single-delta structure. In case of single-star or single-delta structures, in order to generate ac voltage at the output, bridge cell usage is a must. With chopper cells, it is not possible to generate ac voltage at the output. As a result, "single-star chopper cells" or "single-delta chopper cells" could not be used practically. Consequently, four of submodule based multilevel topologies among eight theoretical combinations are practically not implementable.

In the literature, above mentioned four practical topologies are termed as "modular multilevel cascade converter" in general [38]. More specifically, these topologies can be classified as either being "cascaded H-bridges" or "modular multilevel converter". Some researchers give the name "modular multilevel converter" to both chopper cell and bridge-cell based double-star configured multilevel converters, while some others refer only the chopper cell based DSCC structure. In this thesis hereafter, bridge-cell based topologies, namely SSBC, SDBC and DSBC, will be referred as cascaded H-bridges; while chopper cell based structure, DSCC, will be referred as modular multilevel converter (MMC). The common features of all these four topologies are the serial connection of submodules, either being chopper cell or bridge cell, and the serially connected inductor (arm inductor) to these submodules. For the double-star case, the arm inductor may be a single coupled inductor for both of the phase arms or two separate inductors for each of the arms. In the former case, the size and weight of the inductor is less than the total of two uncoupled inductors. Topological characteristics of cascaded H-bridges and modular multilevel converters are explained in the next sections.

2.3.1. Cascaded H-Bridges

Cascaded H-bridges topology can be implemented with three different structures as explained in previous chapter, SSBC, SDBC and DSBC. SSBC and SDBC topologies do not have a common dc-link as in the case of DSBC. Thus, in case there exists a single dc-link (energy source) in the system, it is not possible to use SSBC and SDBC structures for applications in which active power transfer should be done from dc-link to the output, or in inverse direction such as motor drives. In these cases, separate isolated dc sources connected parallel to the bridge capacitors are required to use the SSBC and SDBC topologies. However, providing separate isolated dc sources for each submodule requires heavy and bulky transformers which also increase the cost of the converter. DSBC structure, on the other hand, can be connected to a single dc-link from the neutral points of the star connection. It can be used in motor drive and HVDC applications practically.

The full-bridge circuit, seen in Figure 2.5, can generate three different output voltages, $+V_c$, 0 and $-V_c$, where V_c is the submodule capacitor voltage. Switch states corresponding to these output voltages are listed in Table 2.4. The ac outputs of each of the different full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of full-bridges' outputs. Serial addition of one full-bridge results in an increase of two in the number of output voltage levels.

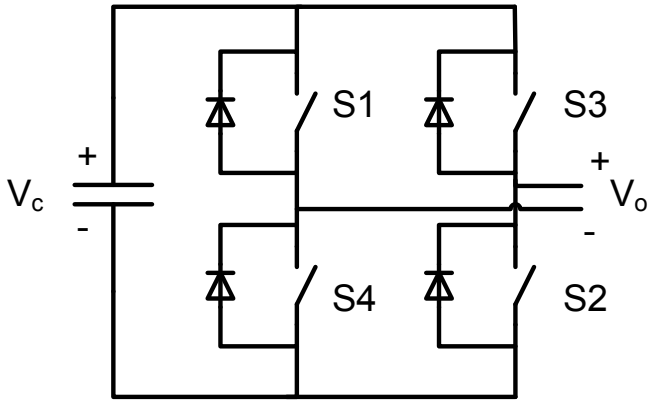


Figure 2.5 The full-bridge circuit topology

Table 2.4 Full-bridge circuit switching states

S_1	S_2	S_3	S_4	V_o
1	1	0	0	V_c
0	0	1	1	$-V_c$
1	0	1	0	0
0	1	0	1	0

SSBC and SDBC topologies are mainly considered for STATCOM and battery energy storage systems. DSBC topology can be used as motor drive for fans/blowers. Also, since it is able to tolerate a broad range of variations in the dc-link voltage due to its buck and boost functions, it is applicable to wind/solar power systems where dc-link voltage varies with wind and weather conditions [38].

The cascaded H-bridge topology is attractive in terms of doubling output voltage level for the same number of submodules per phase, compared to the counterpart with chopper cells. Also, in case separate dc sources are used in submodules, there is no need for submodule capacitor voltage balancing, resulting in easier of control of the converter. However, separate dc source requirement of the topology itself is the major drawback in terms of size, weight, and cost, since each separate dc sources are obtained generally by a transformer and active front end combination.

2.3.2. Modular Multilevel Converter

Modular multilevel converter (MMC) topology was firstly proposed by Lesnicar and Marquardt in 2003 [2]. Since then many researchers have investigated this topology and it has become the most attractive topology among the multilevel converters especially for high power applications. Voltage source converter high-voltage direct current (VSC-HVDC) transmission systems, medium-voltage motor drives, STATCOM applications, and renewable energy interconnection systems to the grid are the typical application areas of MMC. An example "submodule", "arm" and typical converter arrangement of MMC are illustrated in Figure 2.6, while the terms are detailed in the next paragraph.

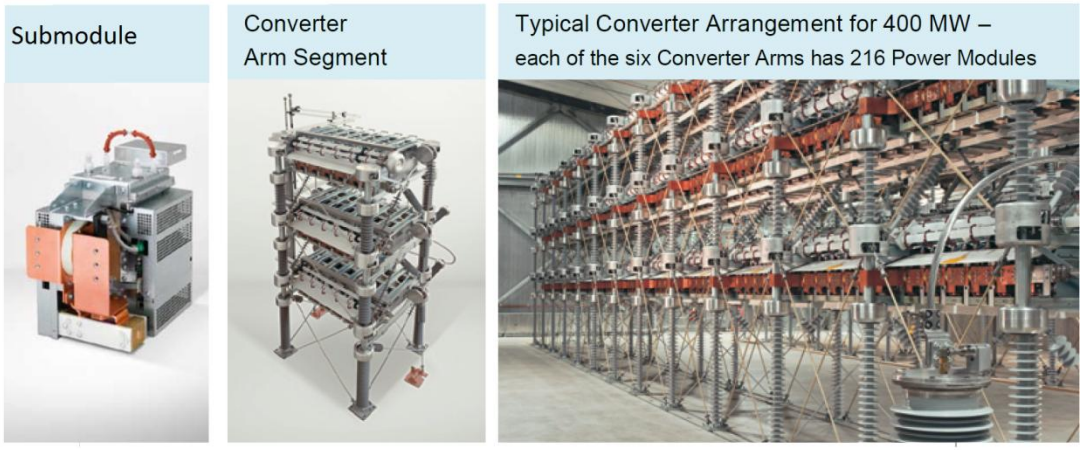


Figure 2.6 Submodule, arm and typical converter arrangement illustrations of MMC by Siemens [39]

Among submodule based multilevel converters, DSCC topology is acknowledged as MMC in this thesis, as explained in section 2.3. Circuit topology of a three-phase MMC is shown in Figure 2.7. All the phases share the common dc-link. The converter is comprised of three "phase legs", while each phase leg is comprised of "upper phase arm" and "lower phase arm". Each phase arm contains N (nominally) identical, cascade connected submodules and an arm inductor, L_{arm}. The arm inductor filters the high frequency component in arm current, limits the fault current and controls the circulating current as will be explained in chapter 4. The submodules produce the required ac phase voltage. Ac side terminals of the converter branch out between the two inductors of upper and lower arms. The submodule topology, being half-bridge circuit as shown in Figure 2.8, is composed of only two switches in cascade and a submodule capacitor paralleled to the switches. This simple and efficient structure allows the half-bridge circuit to dominate the others as the common submodule structure.

At any time, only one of the switches of half-bridge circuit should be ON. If S1 is ON and S2 is OFF, then the half-bridge circuit is “switched on” or “inserted to the current path”. Else if S2 is OFF and S2 is ON, then the half-bridge circuit is “switched off” or “bypassed”. The terminal voltage of half-bridge circuit is equal to

the voltage across the submodule capacitor, V_c, if switched on/inserted; or zero, if switched off/bypassed. If both of the switches are ON, then the submodule capacitor is short-circuited. If both of the switches are OFF, terminal voltage of the submodule is undetermined and according to the direction of the current, different voltages may occur at the terminals. Depending on the states of half-bridge circuit and the direction of submodule current, submodule capacitor is either charged or discharged. All above mentioned switching combinations, terminal voltage of the half-bridge and capacitor charge/discharge conditions are illustrated in Figure 2.9 and Table 2.5.

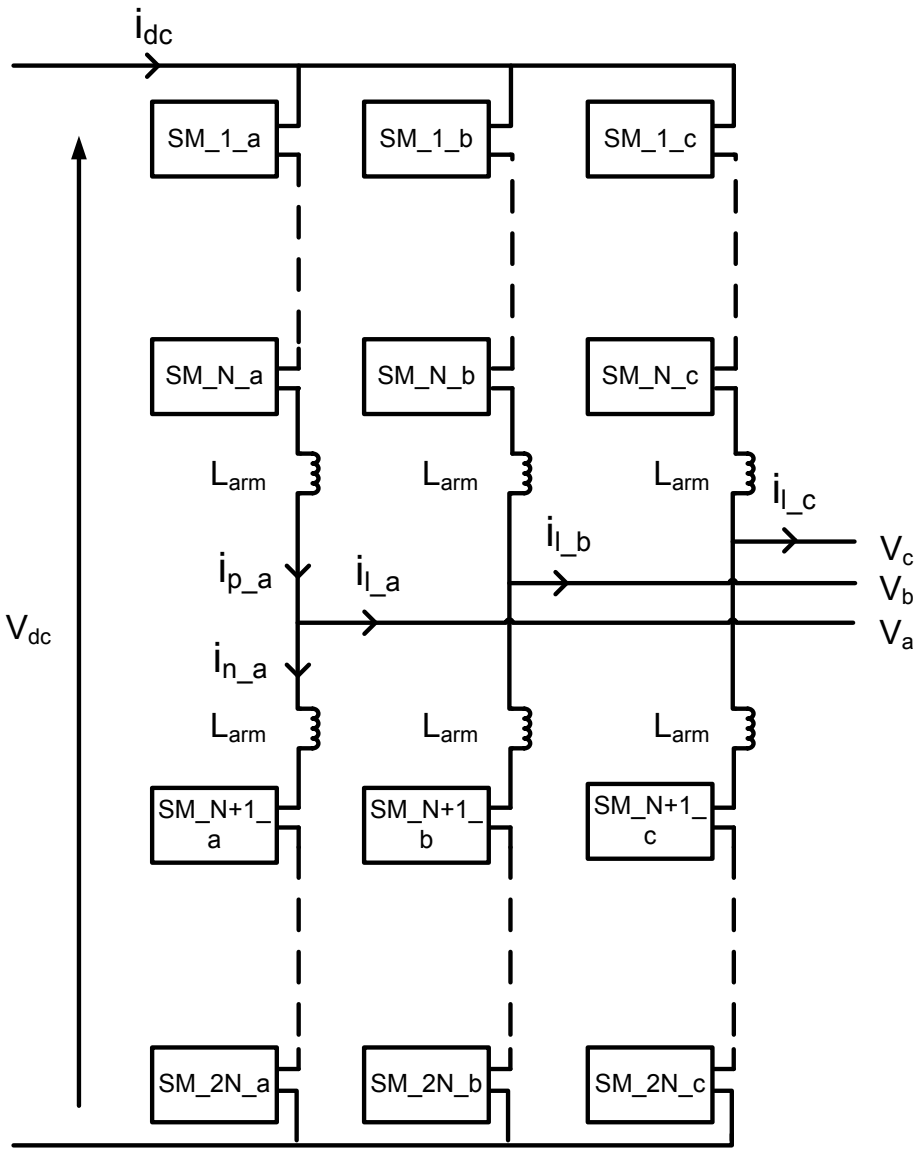


Figure 2.7 Circuit topology of modular multilevel converter

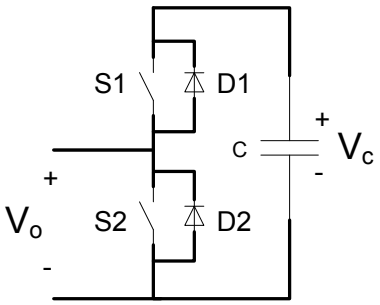


Figure 2.8 Half-bridge (chopper) circuit

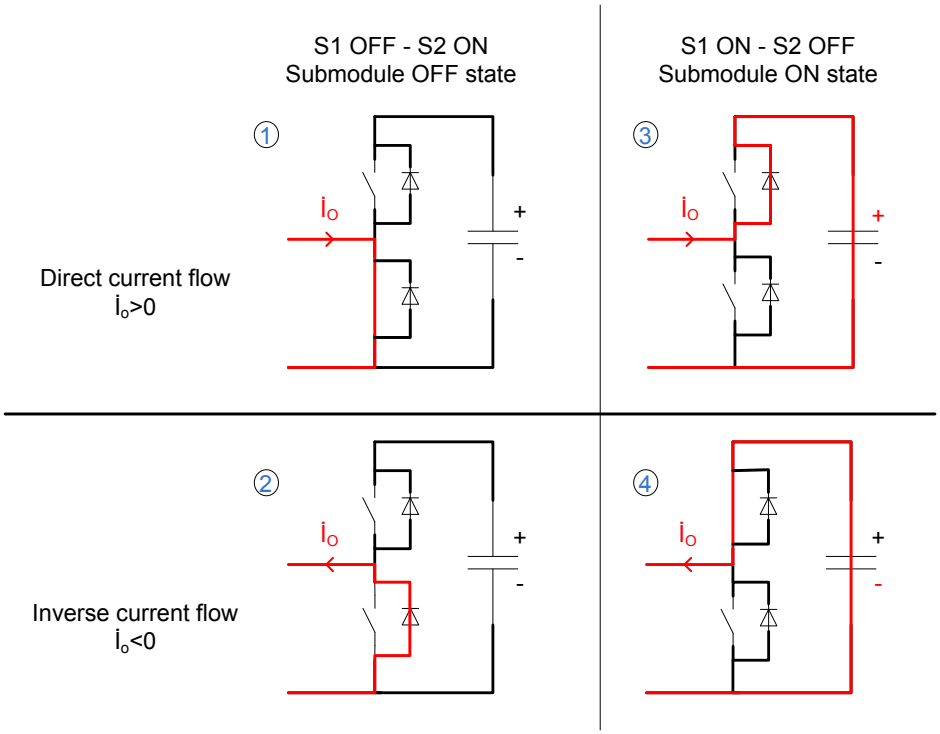


Figure 2.9 States of half-bridge (chopper) circuit and current paths

Table 2.5 Half-bridge circuit switching states

State number in Figure 2.9	**S_2**	**S_1**	**V_o**	**Current direction**	**Current path**	**Capacitor charge**
1	1	0	0	$i_o>0$	S_2	-
2	1	0	0	$i_o<0$	D_2	-
3	0	1	V_c	$i_o>0$	D_1	Charge
4	0	1	V_c	$i_o<0$	S_1	Discharge

In an MMC, the energy of the dc-link is not stored in a single large capacitor, as in the case of conventional VSCs, but it is distributed among the submodule capacitors. There are 6N capacitors in the converter and energy values of these capacitors should be kept as equal as possible, in order to prevent generation of extra currents inside the converter which result from the voltage imbalance. Submodule capacitor voltage balancing methods are presented in chapter 4. For now, it is assumed that all the capacitors are equally charged. In steady state open loop operation of the converter, among 2N submodules in a phase leg, N of them are inserted to the current path. Therefore, the natural average voltage of submodule capacitors, V_c, is expressed as in Equation (2.1):

$$V_c = \frac{V_{dc}}{N} \tag{2.1}$$

Change of number of inserted submodules in the leg causes an imbalance between the phase leg and the dc source, creating internal circulating currents to charge/discharge the submodules capacitors. However, it is important to note that this condition is valid for the open loop operation of the converter and it is a natural balance point. As will be explained in chapter 4, with some specific closed loop control methods, the number of submodules inserted in a phase leg may be increased or decreased from N, intentionally and temporarily.

Compared to other multilevel converter topologies, MMC is advantageous as a result of the features listed below:

i. Ease of flexibility for scaling to different power and voltage levels
ii. Independence from the state of the art of fast developing power devices owing to highly modular and identical submodule structure
iii. Low harmonic distortion, decreased filter size and cost
iv. Higher efficiency
v. High redundancy due to modular structure (a faulty submodule can be bypassed and the converter is able to continue its operation normally;

moreover, if a spare module is present, it could be replaced with the faulty one)

vi. Independence from a centralized circuit element, such as dc-link capacitor or separate dc sources as in the case of cascaded H-bridges
vii. High "apparent" switching frequency of the converter, although low switching frequency of the submodules
viii. Low voltage rating requirements of semiconductors, limited to the submodule capacitor voltage (V_{dc}/N)
ix. Limitation of ac side current in case of a dc-link short-circuit due to arm inductors

On the other hand, disadvantages of MMC's compared to other multilevel converter topologies are listed as below:

i. The number of devices required is usually higher compared to other topologies
ii. Control of submodule capacitor voltage balance brings important computational and measurement requirements, depending on the method used
iii. For high current applications, voltage drop across arm inductors may be significant and may cause reactive power losses

2.3.3. Other Submodule Topologies

In the literature, some other submodule based multilevel converters are proposed. Apart from half-bridge and full-bridge circuits, alternative circuits forming submodules are listed below and illustrated in Figure 2.10:

i. The clamp double circuit
ii. The three-level converter circuits, either capacitor-clamped or diode-clamped
iii. The five level cross connected circuit

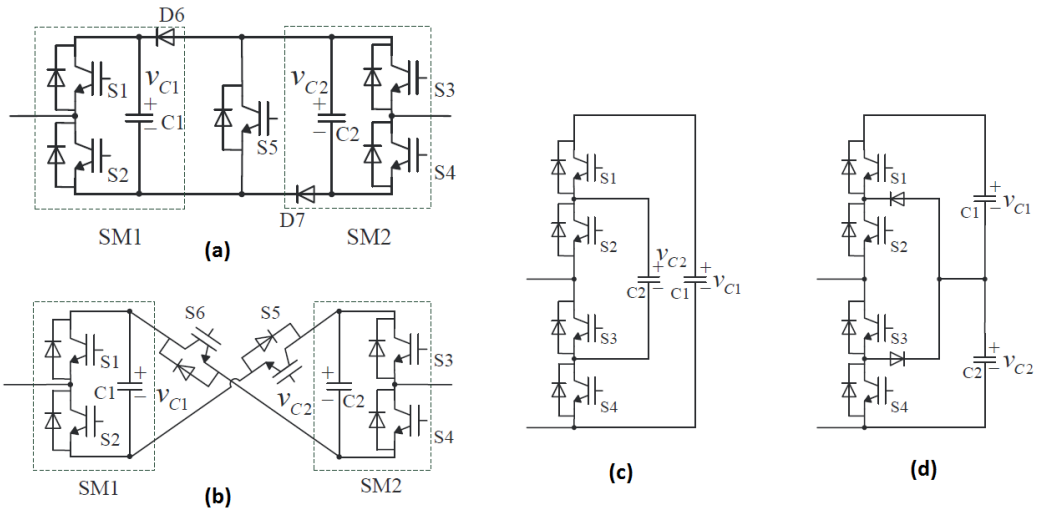


Figure 2.10 (a) The clamp double circuit (b) The five level cross connected circuit (c, d) capacitor-clamped and diode-clamped three-level converters [69]

2.4. Semiconductor Devices for Multilevel Converters

One of the most important advantages of MMCs over other VSCs and multilevel converters is the independence of the topology from fast changing state of the art of power semiconductor devices as explained earlier. The submodules can be constructed by using standard and well-proven semiconductors. Nonetheless, the power rating of a single submodule is dependent on the semiconductors used as half-bridge. Therefore, it is convenient to specify the semiconductors used in MMC.

In the semiconductor market, devices for medium and high power applications cover only a much reduced part of total portion as shown in Figure 2.11. Several high power semiconductors in the market are shown on Figure 2.12 with their manufacturers, current and voltage ratings.

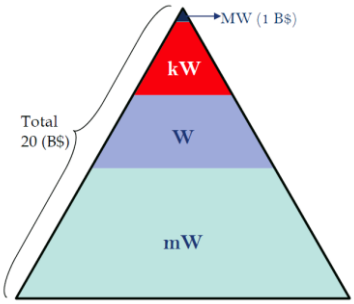


Figure 2.11 Semiconductor market according to power ratings [3]

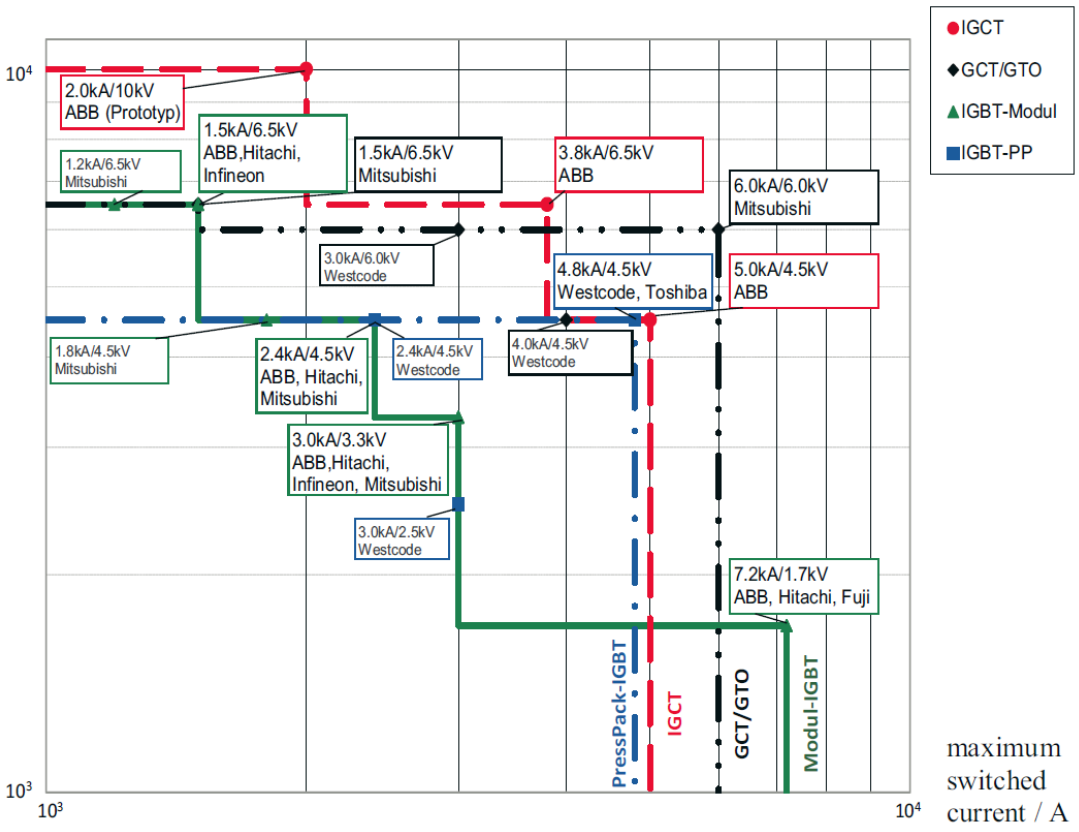


Figure 2.12 Power semiconductors by July 2011 [40]

Further properties of the revealed semiconductor types according to power level are summarized in Table 2.6.

Table 2.6 Power semiconductors overview [76]

Base Technology			Special Features	Short Cct. Lim.	Switching Losses	Conduction Losses
Transistor	Voltage driven turn on/off technology, low control energy, high switching frequency	Low-voltage Insulated Gate Bipolar Transistor (LV-IGBT)	Cost effective, module size	Yes	Low	High
		High-voltage Insulated Gate Bipolar Transistor (HV-IGBT)	Module size, mainstream	Yes	Low	High
		Press Pack IGBT (PPI)	Press packed (single source)	Yes	Low	High
		Injection Enhanced IGBT (IEGT)	High ratings (single source)	No	Medium	Medium
Thyristor	Current driven turn-on/-off technology, high ratings, low conducting losses	Gate turn off thyristor (GTO)	Need of large snubber	No	High	Low
		Integrated gate commutated thyristor (IGCT)	High ratings, mainstream	No	Medium	Low
		Symmetrical gate commutated thyristor (SGCT)	Reverse blocking for CSI	No	Medium	Low
	Only turn on, very high ratings	Silicon controlled rectifier (SCR=thyristor)	Need of commutation	No	Low	Low

2.4.1. Thyristor

Thyristors for use in converters were already in commercial applications since the early 1960s. The performance of the thyristors has since made enormous progress as seen in Table 2.7. Currently, these devices that can sustain voltages in the range of 10kV are matched for very high power applications [3]. On the market, devices which can conduct current levels up to 5kA can be found. Thyristors can reach very high voltage levels, they are very fast during turn-on and they don't show overvoltage problems in series connection. Nevertheless, the thyristor is not a fully controllable switch. The lower and medium power range is covered by turn-off

components. At higher power ratings, the thyristor is used in a special version: the IGCT, which is detailed in section 2.4.3. In the highest power range, thyristor still remains unbeaten for performance, reliability, and low equipment costs.

Table 2.7 Development of the main thyristor characteristic values [41]

Year	Si Ø (inches)	Current (A)	Voltage (V)
1965	0.5	40	1350
1970	2	400	3600
1980	3	1400	4200
1990	4	2600	5200
2000	5	3000	8000

2.4.2. IGBT (HVIGBT)

The Insulate Gate Bipolar Transistor (IGBT) was introduced in 1981 combining a MOS gate with a bipolar transistor for high-voltage sustaining and simple gate driving. IGBTs are widely used for multilevel converters. On the market there are IGBTs which can sustain a voltage up to 6.5kV and switch a peak current up to 1.5kA, as seen in Figure 2.12. Indeed, some of the manufacturers (e.g., Mitsubishi, Hitachi) name this group of IGBTs with high voltage and current rating as High-voltage IGBT, HVIGBT. Different manufacturers produce standardized voltage level IGBTs. This voltage levels can be sorted as 1.7kV, 2.5kV, 3.3kV, 4.5kV and 6.5kV. As the voltage rating of devices increases, current rating decreases. Substantially, different manufacturers offer the same voltage and current ratings. Differentiation occurs in switching times, switching losses and on state voltage drops. The main advantages of IGBTs, especially for small and medium power ratings, are the controllability of the switching behavior due to the MOS gate as well as the short-circuit current blocking capability of the components. This makes it possible to operate the IGBTs without a snubber, enabling a simple, low-cost, lighter and more efficient converter structure. The high-voltage IGBTs are based on multichip substrates and packaged as modules. The bi-directionality in current is

guaranteed by the reverse diode which is included in the structure. Table 2.8 shows fundamental characteristics for some of the HVIGBTs of different manufacturers.

Table 2.8 Fundamental characteristics for the HVIGBTs of different manufacturers [77] -[92]

Volt. Rating	Manufacturer	Part Number	I_c (A) (nom. curr.)	I_{CRM} (A) (peak rpt.)	Switching time (µs) (@25°C)		Switching loss (J) (@25°C)		V_{CE} sat (V) (@25°C)
					t_{on}	t_{off}	E_{on}	E_{off}	
6.5kV	Infineon	FZ750R65KE3	750	1500	1.03	7.7	4.2	3.6	3.0
	ABB	5SNA 0750G650300	750	1500	1.32	5.56	4.7	4.2	2.9
	Mitsubishi	CM750HG-130R	750	1500	1.4	7.66	3.85	3.6	3.9
	Hitachi	MBN750H65E2	750	1500	4.9	6.7	5.5	4.2	3.6
4.5kV	Infineon	FZ1200R45KL3_B5	1200	2400	1.05	6.95	4.6	4.2	2.5
	ABB	5SNA 1200G450350	1200	2400	0.95	2.88	3.08	4.96	2.6
	Mitsubishi	CM1200HG-90R	1200	2400	1.28	3.95	4.6	3.2	3.5
	Hitachi	MBN1200H45E2-H	1200	2400	2.3	3.6	3.2	3.2	3.7
3.3kV	Infineon	FZ1500R33HE3	1500	3000	1.15	3.30	1.9	1.6	2.55
	ABB	5SNA 1500E330305	1500	3000	0.89	1.99	1.6	2.1	2.5
	Mitsubishi	CM1000E4C-66R	1500	3000	1.28	3	1.5	1.5	2.45
	Hitachi	MBN1500E33E3	1500	3000	3.7	3.9	3.5	2.65	2.45
1.7kV	Infineon	FZ3600R17HE4	3600	7200	0.94	1.78	0.65	1.1	1.95
	ABB	5SNA 3600E170300	3600	7200	0.77	1.43	0.8	1.33	2.5
	Mitsubishi	CM2400HC-34H	2400	4800	2.9	3.5	0.81	0.87	2.6
	Hitachi	MBN3600E17F	3600	7200	2.8	3.85	0.95	2.6	2.3

2.4.3. IGCT

The Integrated Gate-Commutated Thyristor (IGCT) is a further development of the gate turn-off (GTO) thyristor. It was jointly developed by Mitsubishi and ABB [42]. Like the GTO thyristor, the IGCT is a fully controllable power switch, meaning that it can be turned both on and off by its control terminal, the gate. It is exclusively used for very high power/current transmission applications. These devices can turn-off up to 6 kA under 4.5 kV. In Table 2.9 a comparison for the characteristics of IGBTs and IGCTs is given. IGCTs offer smaller on state voltage drops, but their switching times and switching losses are higher.

Table 2.9 Characteristics overview between IGCTs and IGBT modules [40]

	IGCT	**IGBT**
Application	Medium-voltage	Low and medium-voltage
Scalability	Parallel and series (with snubber)	Parallel and series
Losses	Low	Medium
Cost	Low	Low
Type of failure	Short-circuit	Open (plasma)
Chip design	Monolithic	Single chips, internal parallel connection
Gate control	No active gate control	Active di/dt and dv/dt control
External clamp	Needed	Possible
On state voltage	Lower than IGBT	Higher than IGCT

For high power, high current transmission systems the IGCT is an important alternative compared to IGBT modules. The better efficiency up to 4% for high current ratings and also the higher possible converter power are significant advantages of IGCTs [40]. Figure 2.13 shows semiconductor loss comparison for MMCs with IGBT and IGCTs for rectifier and inverter operation.

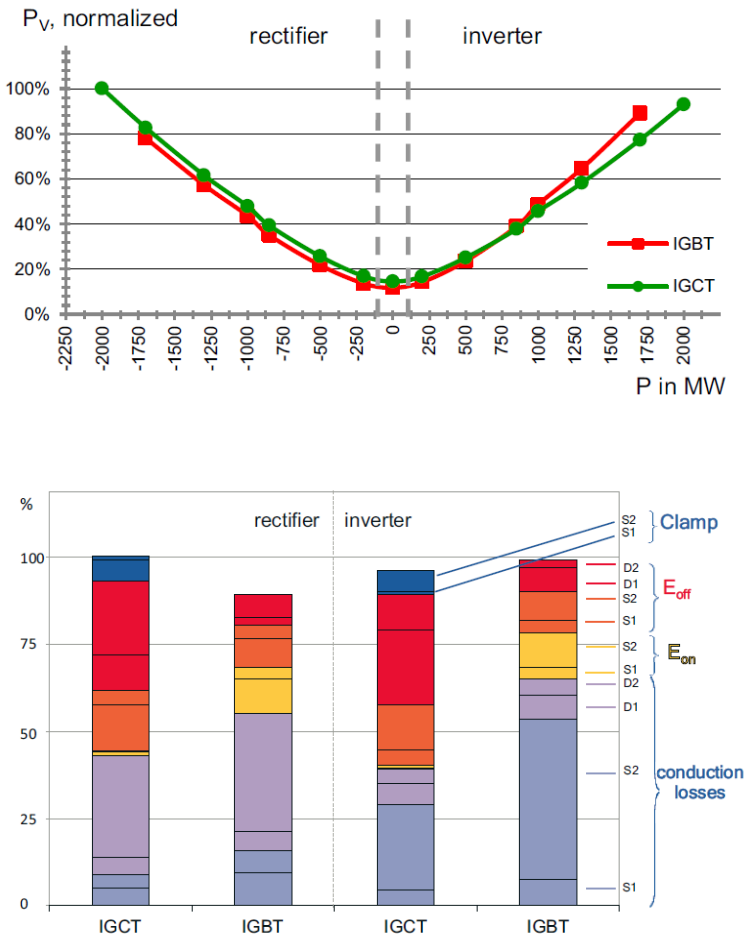


Figure 2.13 Normalized semiconductor losses at the top and semiconductor losses of a MMC submodule splitted in its components for P=850MW, Q=350MVar, f_{switch}=150Hz, V_{dc} = 600kV at the bottom [40]

In the future, the IGCT could be the best candidate for HVDC systems based on VSCs. Already, many applications including MMC based motor drives are powered by IGCTs [10].

CHAPTER 3

CIRCUIT ANALYSIS OF MODULAR MULTILEVEL CONVERTER

3.1. Mathematical Model of Modular Multilevel Converter

Circuit structure of MMC is shown in Figure 3.1. In this model, compared to Figure 2.7, an additional arm resistor can be noticed that models the power loss in each arm.

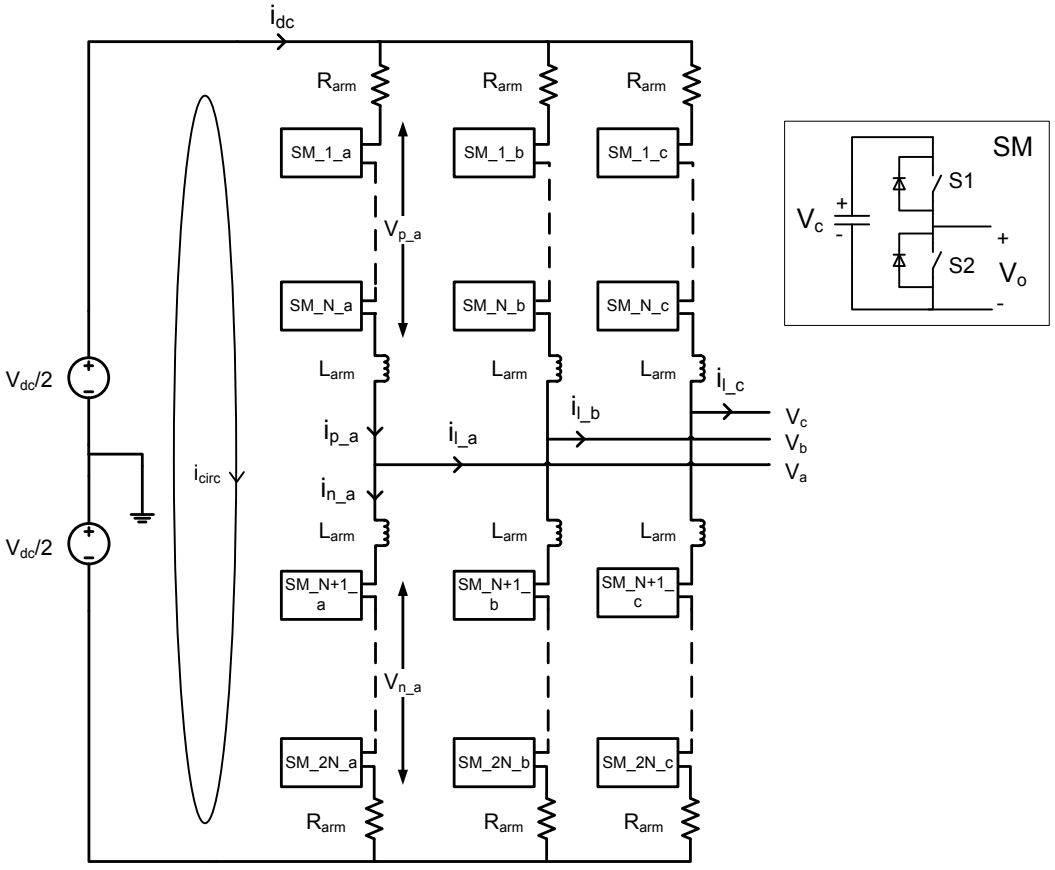


Figure 3.1 Circuit structure of MMC

There are N submodules per arm of the MMC. Let N_{on} be the number of inserted submodules to the current path. Then, let $n(t)$ be the insertion index that sets the number of submodules inserted to the current path. $n(t)$ is expressed as in Equation (3.1). $n(t) = 0$ means all the submodules of the arm are bypassed and $n(t) = 1$ means all the submodules are inserted to the current path.

$$n(t) = \frac{N_{on}}{N} \tag{3.1}$$

If the capacitance of each submodule is C, the capacitance of series connection of N submodules per arm, C^{arm}, is expressed as in Equation (3.2):

$$C^{arm} = \frac{C}{N} \tag{3.2}$$

Then, the applicable capacitance of the inserted submodules per arm becomes as in Equation (3.3):

$$C^{m} = \frac{C^{arm}}{n(t)} \tag{3.3}$$

Assuming that all the capacitors are equally charged to V_{dc}/N, and sum of all capacitor voltages of an arm being $\sum v_C$, the voltage inserted by an arm is expressed as in Equation (3.4), for each phase:

$$v_{p/n} = n_{p/n}(t) \sum v_{Cp/n} \tag{3.4}$$

The current flowing through each arm charges the inserted capacitors of the arm, having effective capacitance of C^m, according to Equation (3.5):

$$i_{p/n} = C^{m}_{p/n} \frac{d\left(\sum v_{Cp/n}\right)}{dt} \tag{3.5}$$

Equation (3.5) can be rewritten as in Equations (3.6) and (3.7) where, n_p and n_n stand for the upper and lower arm insertion indices:

$$i_p = \frac{C^{arm}}{n_p}\frac{d\left(\sum v_{Cp}\right)}{dt} \tag{3.6}$$

$$i_n = \frac{C^{arm}}{n_n}\frac{d(\sum v_{Cn})}{dt} \tag{3.7}$$

The upper, i_p, and lower, i_n, arm currents, are expressed as the sum of half of output (ac side) current, i_l, and circulating current, i_{circ}, as in Equations (3.8) and (3.9):

$$i_p = i_{circ} + \frac{i_l}{2} \tag{3.8}$$

$$i_n = i_{circ} - \frac{i_l}{2} \tag{3.9}$$

Note that i_p, i_n and i_l are branch currents, whereas i_{circ} is a loop current that is impossible to measure directly. i_{circ} circulates between each phase leg and the dc-link (and/or to another phase leg). Under balanced load conditions, the dc-link current, i_{dc}, is shared equally between three phase legs. The circulating current is composed of this dc-link current and an ac component emanating from the capacitors voltage ripple in the phase leg and voltage difference between different phase legs. Based on Equations (3.8) and (3.9), the circulating current and output current are expressed in terms of upper and lower arm currents as in Equations (3.10) and (3.11):

$$i_{circ} = I_{circ,dc} + i_{circ,ac} = \frac{i_{dc}}{3} + i_{circ,ac} = \frac{i_p + i_n}{2} \tag{3.10}$$

$$i_l = i_p - i_n \tag{3.11}$$

The mathematical models of upper and lower arms are expressed as in Equations (3.12) and (3.13):

$$\frac{V_{dc}}{2} - v_p = L_{arm}\frac{di_p}{dt} + R_{arm}i_p + v_l \tag{3.12}$$

$$\frac{V_{dc}}{2} - v_n = L_{arm}\frac{di_n}{dt} + R_{arm}i_n - v_l \tag{3.13}$$

where v_p and v_n represent the upper and lower arm voltages of phase as expressed in Equation (3.4) and v_l represents the output voltage. Based on Equations (3.12) and (3.13), output voltage is expressed as in Equation (3.14):

$$v_l = \frac{v_n - v_p}{2} - \frac{R_{arm}}{2}i_l - \frac{L_{arm}}{2}\frac{di_l}{dt} \tag{3.14}$$

Using Equation (3.10), differential equation of i_{circ} can be found as in Equation (3.15):

$$\frac{di_{circ}}{dt} = \frac{1}{2}\left(\frac{di_p}{dt} + \frac{di_n}{dt}\right) \tag{3.15}$$

Substituting di_p/dt and di_n/dt from Equations (3.12) and (3.13), Equation (3.15) can be reordered as in Equation (3.16):

$$\begin{aligned}\frac{di_{circ}}{dt} &= \frac{V_{dc}}{2L_{arm}} - \frac{R_{arm}}{L_{arm}}i_{circ} - \frac{v_p}{2L_{arm}} - \frac{v_n}{2L_{arm}} \\ &= \frac{V_{dc}}{2L_{arm}} - \frac{R_{arm}}{L_{arm}}i_{circ} - \frac{n_p}{2L_{arm}}\left(\sum v_{Cp}\right) - \frac{n_n}{2L_{arm}}\left(\sum v_{Cn}\right)\end{aligned} \tag{3.16}$$

Equations (3.6) and (3.7) can be reordered as in Equations (3.17) and (3.18) by using i_p and i_n from Equations (3.7) and (3.8):

$$\frac{d(\sum v_{Cp})}{dt} = \frac{n_p}{C^{arm}} i_{circ} + \frac{n_p}{2C^{arm}} i_l \tag{3.17}$$

$$\frac{d(\sum v_{Cn})}{dt} = \frac{n_n}{C^{arm}} i_{circ} - \frac{n_n}{2C^{arm}} i_l \tag{3.18}$$

Equations (3.15) and (3.16) reveal that in case of i_{circ} is equal to zero; the output current distorts the voltage balance of upper and lower arm voltages. As the steady state waveform of i_l is ac and changes its value between a positive top and negative bottom value, time derivative of upper and lower arm voltages oscillate around a mean value. A continuous model of a phase leg is obtained as in Equation (3.19) by using Equations (3.16), (3.17) and (3.18):

$$\frac{d}{dt}\begin{bmatrix} i_{circ} \\ \sum v_{Cp} \\ \sum v_{Cn} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & -\frac{n_p}{2L_{arm}} & -\frac{n_n}{2L_{arm}} \\ \frac{n_p}{C^{arm}} & 0 & 0 \\ \frac{n_n}{C^{arm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{circ} \\ \sum v_{Cp} \\ \sum v_{Cn} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_{arm}} \\ \frac{n_p}{2C^{arm}} i_l \\ \frac{n_n}{2C^{arm}} i_l \end{bmatrix} \tag{3.19}$$

Modulation signal for an ideal sinusoidal output voltage is given as in Equation (3.20). In this equation, ω_N is the output frequency and $\hat{m}$ is modulation index.

$$m(t) = \hat{m}\cos(\omega_N t) \tag{3.20}$$

The output voltage is then given by Equation (3.21):

$$v_l(t) = \frac{V_{dc}}{2} m(t) \tag{3.21}$$

The output current is assumed as given in Equation (3.22). Here, φ is the load angle and it can be chosen arbitrarily to model different kind of loads.

$$i_l(t) = \hat{\imath_l}\cos(\omega_N t + \varphi) \tag{3.22}$$

The modulator converts the modulation signal into insertion indices as in Equations (3.23) and (3.24).

$$n_p(t) = \frac{1 - m(t)}{2} \tag{3.23}$$

$$n_n(t) = \frac{1 + m(t)}{2} \tag{3.24}$$

It is obvious from Equations (3.23) and (3.24) that the sum of upper and lower arm insertion indices is one, which means at any time sum of the number of inserted submodules in upper and lower arms is N. Ideally, the sum of voltages of inserted submodules capacitors is equal to V_{dc}. However, the submodule capacitor voltages are not constant at the reference value and oscillate around that. As a result, a difference current (named as circulating current, i_{circ}, above) flowing between the phase leg and dc-link is forced by the difference between the sum of inserted submodule capacitor voltages and dc-link voltage. The circulating current contains a high second harmonic component which increases the losses in converter phase legs, ratings of the elements in the current path. Also, if left uncontrolled, circulating current may lead an unbalanced situation and disturbances in the system, and these may cause instability of the system.

3.2. Energy Dynamics and General Circuit Analysis of MMC

From Equation (3.16), voltage loop equation for the circulating current can be found as in Equation (3.25):

$$L_{arm}\frac{di_{circ}}{dt} + R_{arm}i_{circ} = \frac{V_{dc}}{2} - \frac{v_p + v_n}{2} \tag{3.25}$$

From Equations (3.14) and (3.25), the following conclusions are derived:

- The output voltage v_l depends on the output current and the difference between the upper and lower arm voltages v_p and v_n.
- The arm voltage difference works like an inner alternating voltage, and R_{arm} and L_{arm} like an impedance for alternating current.
- i_{circ} depends only on the dc-link voltage and the sum of arm voltages. Thus, adding the same quantity to both of the arm voltages does not affect the ac side voltage, while it shapes the circulating current.

Starting from Equation (3.12), in order to control the circulating current, it is convenient to define a circulating voltage component, with substituting the upper arm current i_p as in Equation (3.8):

$$\frac{V_{dc}}{2} - v_p = L_{arm}\frac{d(i_{circ} + \frac{i_l}{2})}{dt} + R_{arm}(i_{circ} + \frac{i_l}{2}) + v_l \tag{3.26}$$

Equation (3.26) can be rewritten as in Equation (3.27) below:

$$v_p = \frac{V_{dc}}{2} - v_l - \frac{R_{arm}}{2}i_l - \frac{L_{arm}}{2}\frac{di_l}{dt} - R_{arm}i_{circ} - L_{arm}\frac{di_{circ}}{dt} \tag{3.27}$$

From Equation (3.12),

$$v_l + \frac{R_{arm}}{2}i_l + \frac{L_{arm}}{2}\frac{di_l}{dt} = \frac{v_n - v_p}{2} = e_v \tag{3.28}$$

Then, Equation (3.27) can be rearranged as in Equation (3.29):

$$v_p = \frac{V_{dc}}{2} - e_v - v_{circ} \tag{3.29}$$

For the lower arm, the same approach can be carried out as in Equation (3.30):

$$v_n = \frac{V_{dc}}{2} + e_v - v_{circ} \tag{3.30}$$

where v_{circ} is defined as in Equation (3.31):

$$v_{circ} = R_{arm} i_{circ} + L_{arm} \frac{di_{circ}}{dt} \tag{3.31}$$

Assuming the voltage of submodule capacitors are equal in upper and lower arms, the total energy stored in the upper and lower arms are given by Equations (3.32) and (3.33):

$$\sum W_{cp} = N\left[\frac{C}{2}\left(\frac{\sum v_p}{N}\right)^2\right] = \frac{C}{2N}\left(\sum v_p\right)^2 = \frac{C_{arm}}{2}\left(\sum v_p\right)^2 \tag{3.32}$$

$$\sum W_{cn} = N\left[\frac{C}{2}\left(\frac{\sum v_n}{N}\right)^2\right] = \frac{C}{2N}(\sum v_n)^2 = \frac{C_{arm}}{2}(\sum v_n)^2 \tag{3.33}$$

Derivatives of the stored energy in the upper and lower arm capacitors are the arm powers as in Equations (3.34) and (3.35) below:

$$\frac{d\left(\sum W_{cp}\right)}{dt} = i_p v_p = \left(i_{circ} + \frac{i_l}{2}\right)\left(\frac{V_{dc}}{2} - e_v - v_{circ}\right) \tag{3.34}$$

$$\frac{d(\sum W_{cn})}{dt} = i_n v_n = \left(i_{circ} - \frac{i_l}{2}\right)\left(\frac{V_{dc}}{2} + e_v - v_{circ}\right) \tag{3.35}$$

Total energy in the phase leg and the energy difference between the upper and lower arms are calculated as below in Equations (3.36) and (3.37):

$$\sum W_c = \sum W_{cp} + \sum W_{cn} \tag{3.36}$$

$$\Delta W_c = \sum W_{cp} - \sum W_{cn} \tag{3.37}$$

Derivative of Equations (3.36) and (3.37) with respect to time yields:

$$\frac{d(\sum W_c)}{dt} = (V_{dc} - 2v_{circ})i_{circ} - e_v i_l \tag{3.38}$$

$$\frac{d(\Delta W_c)}{dt} = \left(\frac{V_{dc}}{2} - v_{circ}\right) i_l - 2e_v i_{circ} \tag{3.39}$$

The Equations (3.38) and (3.39) reveal the fact that the circulating current is the key component in controlling the total energy stored in the capacitors in the phase legs. In (3.38), the product of $V_{dc} i_{circ}$ covers the power delivered to the output and the losses created by the circulating current itself. $v_{circ} i_{circ}$ product represents the losses in the arm resistance and the magnetic energy variation of arm inductance. $e_v i_l$ product is the output power. Therefore, dc component of i_{circ} can be used to control the total energy in the phase leg, which in turn the voltages of submodule capacitors. From Equation (3.39), it is inferred that the dc component of i_{circ} has no impact on the difference of arms energy since e_v does not contain dc component. However, an ac component of i_{circ} having the same fundamental frequency as the output voltage e_v, can be used to control the capacitor energy difference of upper and lower arms.

CHAPTER 4

MODULAR MULTILEVEL CONVERTER SWITCHING METHODS

4.1. Introduction

Switching of modular multilevel converters can mainly be divided into two categories: low frequency switching and high frequency switching. In low frequency switching, a pre-calculated pulse pattern is used to drive the converter. Harmonic elimination methods can be used to improve the performance of the converter. These methods have low switching count and therefore high efficiency. However, their weakness is the dynamic response. In high frequency switching, a reference output voltage waveform (a modulation signal, sinusoid based) is compared in magnitude with a high frequency carrier waveform and switching logic signal is generated. Generally these methods yield low output voltage and current waveform harmonic distortion, enabling the converter to require smaller and lower cost passive filters and to have fast dynamic response to the source/load changes. Although high frequency switching methods tend to have higher switching count (which means higher switching loss) than low frequency switching; with suitable design, losses can be decreased and the major disadvantage of high frequency switching can be overcome. Additionally the third category of switching method, namely mixed switching, can be added to take the advantages of the two methods above. As the name refers, this method has characteristics of both low frequency and high frequency switching. The switching methods for modular multilevel converters are illustrated in Figure 4.1.

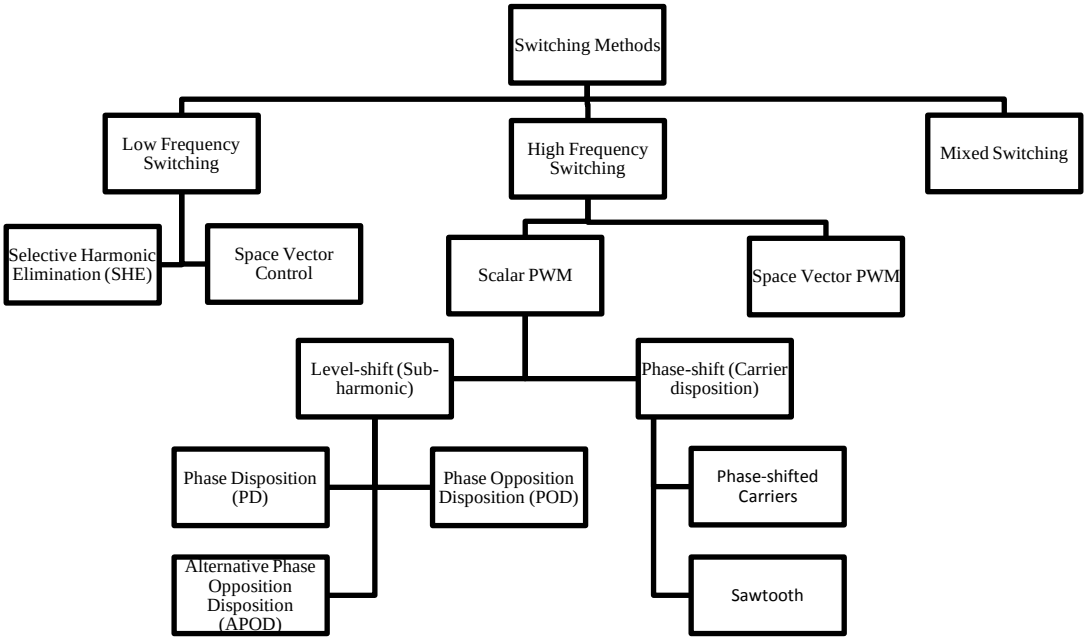


Figure 4.1 Switching methods for modular multilevel converters

4.2. High Frequency (Carrier based) Switching

High frequency switching methods are widely considered for modular multilevel converter due to satisfactory performance and ease of implementation. In high frequency switching, the carrier frequency is constant and in each switching period, reference and output voltage mean values are made equal. For this aim, scalar method or space vector method can be used. Scalar method uses a reference (modulation) waveform having the desired output voltage magnitude and frequency, and a high frequency carrier waveform. Magnitudes of reference and carrier are compared and at the crossover points, switching occurs. The space vector method, on the other hand, creates a vector diagram in space for each switching condition of the converter and the output reference is represented by a vector. In order to get the desired output voltage, the converter is driven by the relevant switching pulse

pattern generated according to the reference vector and the switching condition vectors. Although both methods may produce similar switching pulse pattern, implementation of scalar method is much easier.

4.2.1. Scalar PWM [68]

4.2.1.1. Level-shift (LS) (Sub-Harmonic) Methods

These methods require N identical triangular carriers being displaced contiguously in the whole dc-link voltage; V_{dc}. In order to provide a balanced exploitation of circuit elements that create different voltage levels, peak-to-peak amplitudes of the carriers are set equal to each other, V_{dc}/N, which is a necessary but not a sufficient condition. They have frequency of f_c. Carriers do not cross. Depending on the phase-shift of carriers with respect to each other, level-shift methods branch into three different sub-methods: phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD).

4.2.1.1.1. Phase Disposition (PD) Method

In phase disposition method, all the carriers are in phase. For an MMC having 4 submodules per phase arm (N=4), carriers of PD method are displaced in the V_{dc} band as illustrated in Figure 4.2. In the Figure 4.2 to Figure 4.6, 1 p.u. in vertical axis corresponds to V_{dc}.

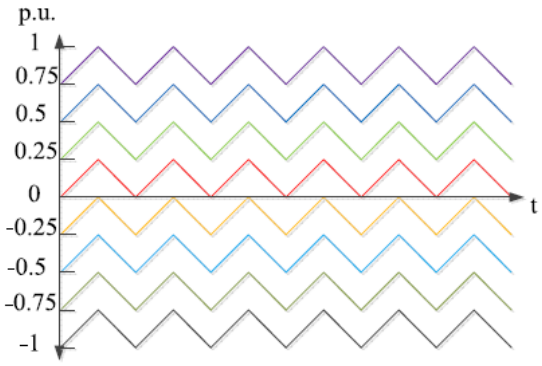


Figure 4.2 Phase disposition (PD) method

4.2.1.1.2. Phase Opposition Disposition (POD) Method

In phase opposition disposition method, carriers above the zero axis and below the zero axis are 180° out of phase. For an MMC having 4 submodules per phase arm (N=4), carriers of POD method are displaced in the V_{dc} band as illustrated in Figure 4.3.

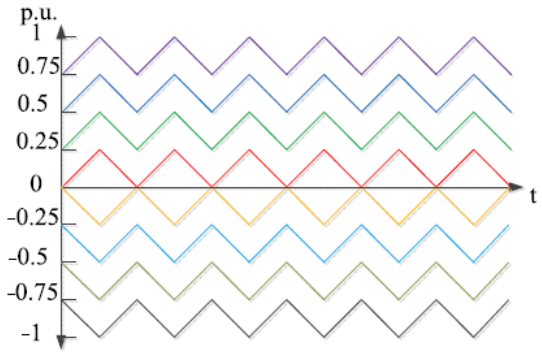


Figure 4.3 Phase opposition disposition (POD) method

4.2.1.1.3. Alternative Phase Opposition Disposition (APOD) Method

In alternative phase opposition disposition method, contiguous carriers are 180° out of phase. For an MMC having 4 submodules per phase arm (N=4), carriers of APOD method are displaced in the V_{dc} band as illustrated in Figure 4.4.

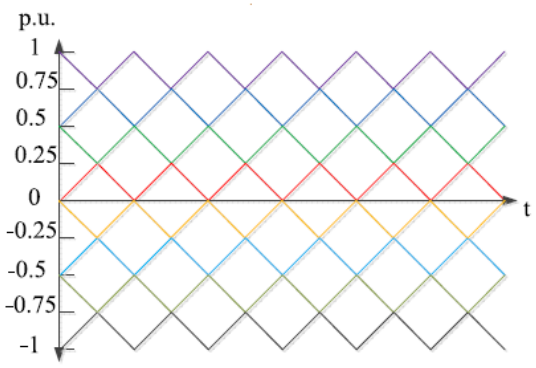


Figure 4.4 Alternative phase opposition disposition (APOD) method

4.2.1.2. Phase-shift (PS) (Carrier Disposition) Method

This method again require N identical triangular carriers being displaced with a phase-shift of 360°/N between each other in the whole dc-link voltage; V_{dc}. Carriers have peak-to-peak amplitude of V_{dc} and frequency of f_c. Carriers cross each other. For an MMC having 4 submodules per phase arm (N=4), carriers of phase-shift method are displaced in the V_{dc} band as illustrated in Figure 4.5.

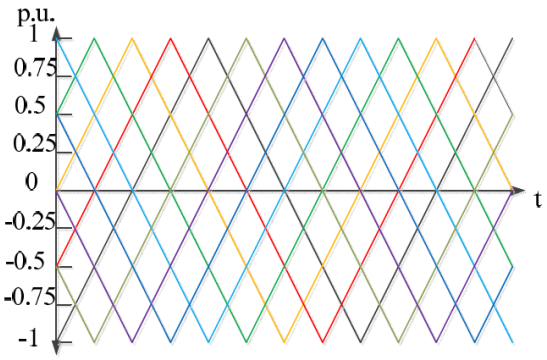


Figure 4.5 Phase-shifted carriers method

In the literature, there exists another phase-shift method in which the carriers are very much like in those in Figure 4.5; however, they are sawtooth waveforms rather than triangular. This method is called "sawtooth rotation", but it is out of the scope of the thesis. For convenience, carriers of sawtooth rotation method for an MMC having 4 submodules per phase arm (N=4) are illustrated in Figure 4.6.

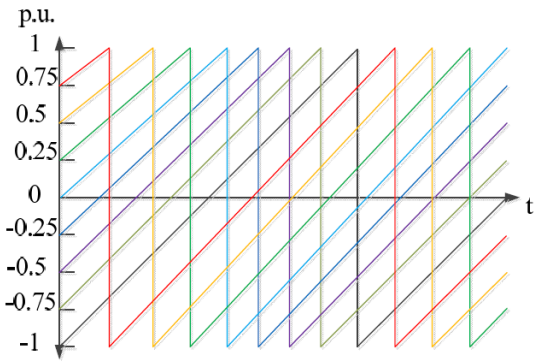


Figure 4.6 Sawtooth rotation method

In this thesis hereafter, the term "phase-shift" (PS) refers to the method with triangular carriers, i.e. Figure 4.5.

4.2.2. Space Vector PWM

Space vector PWM is another high frequency switching method for modular multilevel converters. Although scalar PWM methods can be used both for single and three-phase systems, space vector PWM method can be used in three-phase systems. In space vector modulation, three reference modulation signals are transformed into a reference vector and this vector is positioned in a space vector diagram. In Figure 4.7 sample space vector diagrams are illustrated for two- and five-level converters. In these hexagon formed diagrams, each corner of the triangles correspond to a switching state of the converter. According to the magnitude and angle of the reference vector, which are directly dependent on the three reference modulation signals, the nearest three triangle corners (in other words switching states of the converter) are identified. The modulation period of each of these switching states are calculated and the converter is switched according to these switching states with the calculated switching periods. The reference vector is synthesized by the three adjacent vectors as given in Equation (4.1), where T is the total switching period, T_j, T_{j+1} and T_{j+2} are the calculated switching periods of adjacent vectors and $T = T_j + T_{j+1} + T_{j+2}$.

$$V_{ref} = \frac{(T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2})}{T} \tag{4.1}$$

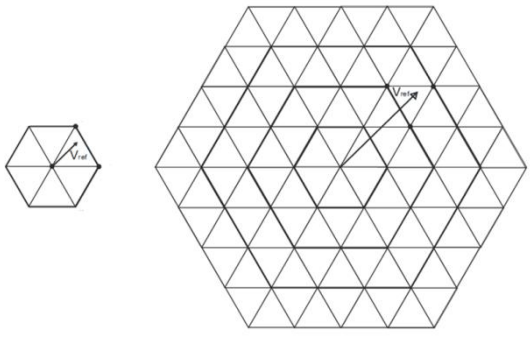


Figure 4.7 Space vector diagrams for two-level converter at left and five-level converter at right

Space vector diagram is universal and it can be used with any type of multilevel converters. The method generally creates low current ripple, has good utilization of dc-link voltage and easy hardware implementation by a digital signal processor. However, as the number of voltage levels increases, redundancy of switching states increase and so does the complexity of choosing states.

4.3. Low Frequency Switching

4.3.1. Selective Harmonic Elimination

Selective harmonic elimination (SHE) method is based on the harmonic elimination theory [43], [44]. The switching angles are pre-calculated so as to set the desired amplitude of fundamental component and cancel the predominant low frequency harmonics in the output voltage [45]. In Figure 4.8, output voltage waveform for a five-level converter whose switching angles are determined by selective harmonic elimination method is shown.

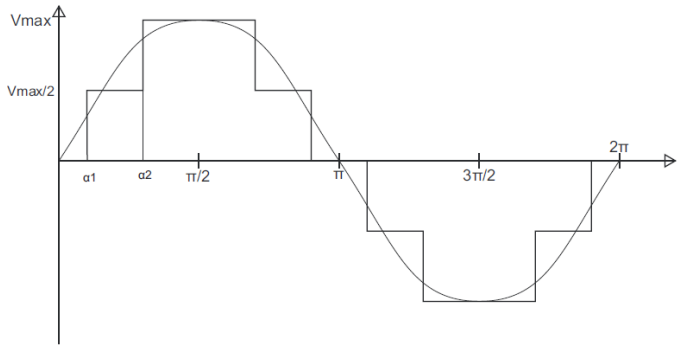


Figure 4.8 Output voltage waveform for a five-level converter, switching angles determined by selective harmonic elimination method

4.3.2. Space Vector Control

Space vector control (SVC) is another low frequency modulation method. Converse to space vector pulse-width modulation method, space vector control does not generate the wanted mean output voltage in every switching period. The main idea in space vector control is to generate an output voltage with smallest error (distance) to the reference vector. As the number of voltage levels increase, density of switching states in the space vector diagram (Figure 4.7) increases, and the errors of each individual switching state to the reference vector are decreased. Therefore, it is unnecessary to use three switching states adjacent to the reference vector. A single switching state with greatest proximity to the reference vector is used to switch the converter accordingly [46].

4.4. Switching Pulse Patterns and Generated Output Voltage Characteristics of Scalar PWM Methods

Scalar PWM methods are dominantly used for MMC switching due to satisfactory performance and ease of implementation. These methods have various forms and implementation process as described in previous sections. Therefore, characteristics of generated switching pulse patterns and resultant output voltages are different for various methods. In order to make a proper MMC design, it is important to understand these characteristics defined by the switching pulse patterns of different scalar PWM methods and match the suitable method with the given requirements. Thus, it is required to analyze the switching pulse patterns generated by these methods and the generated output voltages. In this study, the analysis of all level-shift methods and phase-shift method are conducted. Analysis is based on the fundamental pulse pattern generations which only result from the comparison of triangular carrier and sinusoidal reference signals. By doing so, it is intended to have a fundamental data and guiding principles about the scalar PWM methods with their purest form, before going into more complex control mechanisms of MMC.

4.4.1. Discussion on Carrier Sets and Number of Output Voltage Levels

The numbers of output voltage levels for conventional two/three level converters are fixed as the names of the topologies refer. For MMC, on the other side, it is not correct to call a converter with N submodules per arm as "*N+1 level converter*". It is possible to obtain N+1 or 2N+1 output phase-to-neutral voltage levels from an MMC with the same number of submodules per arm. Indeed, the situation is dependent on the "carrier sets" used for switching of upper phase arm and lower phase arm.

The two fundamental scalar PWM methods, level-shift and phase-shift, require N carriers as details are given in section 4.2.1. For both of the methods, N carriers corresponding to one arm of MMC form "a set of carriers". Switching of upper and lower arms of MMC can be done either by using *the same set of carriers*, or by *two different sets of carriers*, provided that there is a predefined phase difference between them. The switching manner, using only a set of carriers or two different sets of carriers for upper and lower arms, results in N+1 or 2N+1 phase-to-neutral voltage levels at the output of the converter. MMC performance variations in the results of N+1 or 2N+1 level phase voltages will be explained in chapter 7. Here, principles of switching for N+1 and 2N+1 level of phase-to-neutral voltages will be given. It is essential to note that, in all the explanations in this section, the sinusoidal reference signals for upper and lower arms of a phase leg are assumed to be π radians out of phase which is justified in chapter 6.

4.4.1.1. N+1 Level Phase Voltages

4.4.1.1.1. Level-shift Methods

4.4.1.1.1.1. PD

PD method should be implemented with *two different carrier sets* for upper and lower arms in order to construct the phase voltage in N+1 level. First set of carriers is arranged in the same way as expressed in section 4.2.1.1.1. The other carrier set has again N identical carriers with amplitude of V_{dc}/N and displaced contiguously in the V_{dc} band, ranging from 0 to V_{dc}; however, this set has a phase difference of π radians relative to the first set. Submodules in upper and lower arms are switched with the first and second carrier sets. In this case, output phase voltage is N+1 level. Figure 4.9 illustrates the case with PD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the frequency of the level-shifted carriers, as expressed in Equation (4.2).

$$f_{c\_eq} = f_c \tag{4.2}$$

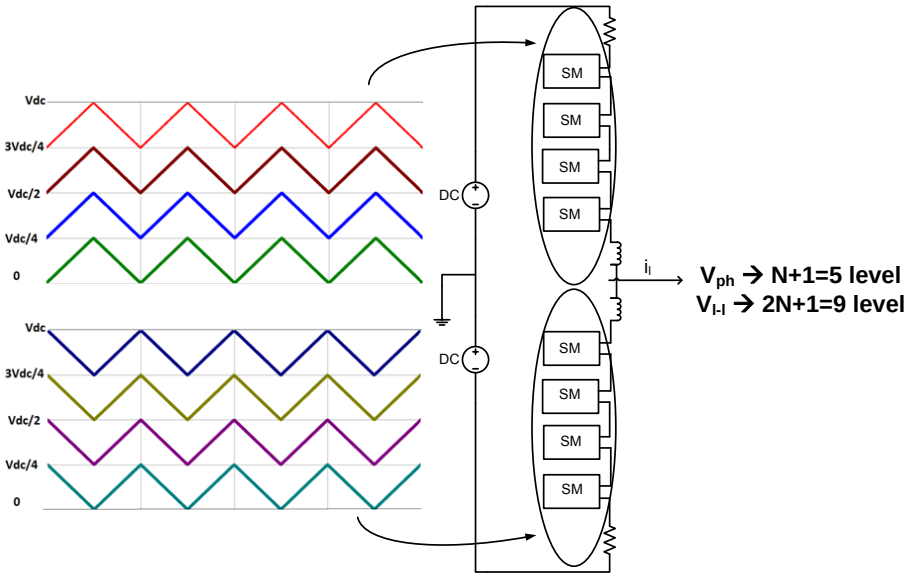


Figure 4.9 Carrier sets for N+1 level phase voltage of PD method

4.4.1.1.1.2. POD

POD method should be implemented with *a single carrier set* for both upper and lower arms in order to construct the phase voltage in N+1 level. The single set is arranged in the same way as expressed in section 4.2.1.1.2. Submodules in upper and lower arms are switched with this carrier set. In this case, output phase voltage is N+1 level. Figure 4.10 illustrates the case with POD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the frequency of the level-shifted carriers, as expressed in Equation (4.3).

$$f_{c\_eq} = f_c \tag{4.3}$$

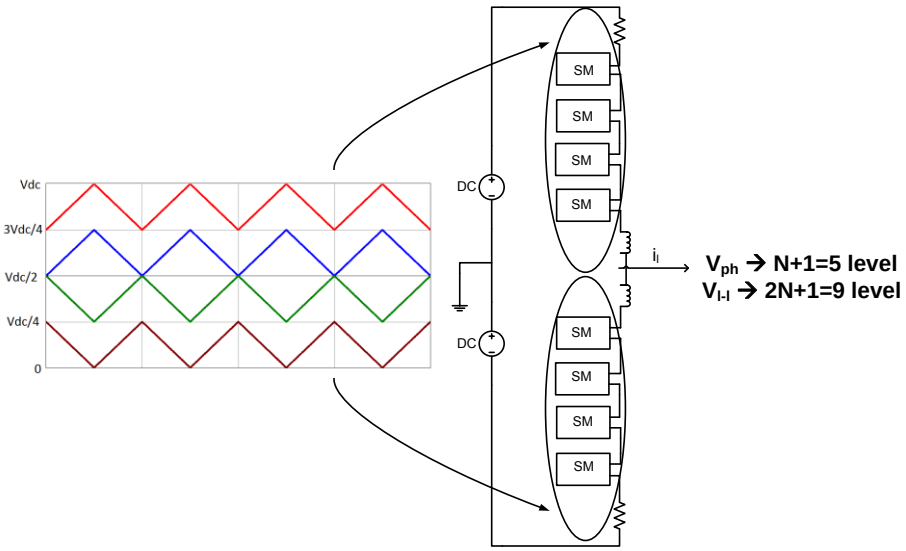


Figure 4.10 Carrier set for N+1 level phase voltage of POD method

4.4.1.1.1.3. APOD

In order to construct the phase voltage in N+1 level, APOD method should be implemented with *a single carrier set* for both upper and lower arms. The single set is arranged in the same way as expressed in section 4.2.1.1.3. Submodules in upper and lower arms are switched with this carrier set. In this case, output phase voltage

is N+1 level. Figure 4.11 illustrates the case with APOD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the frequency of the level-shifted carriers, as expressed in Equation (4.4).

$$f_{c\_eq} = f_c \tag{4.4}$$

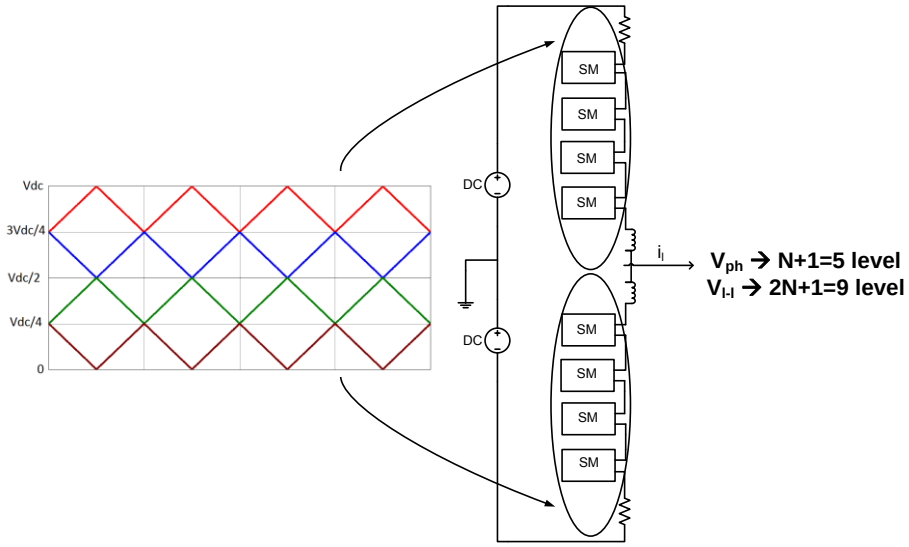


Figure 4.11 Carrier set for N+1 level phase voltage of APOD method

4.4.1.1.2. Phase-shift Method

For phase-shift method, carrier sets are arranged according to N being odd or even.

In case N is odd, two different carrier sets are used for upper and lower arms. First set of carriers is arranged in the same way as expressed in section 4.2.1.2. The second set has again the same waveform, but with π/N radians phase difference relative to the first set. Submodules in upper and lower arms are switched with these first and second carrier sets. In this case, output phase voltage is N+1 level. Figure 4.12 illustrates the case with phase-shift method on a phase leg with N=3.

In case N is even, a single carrier set is used for both upper and lower arms. The only carrier set is the same as explained in section 4.2.1.2. Submodules in upper and lower arms are switched with this carrier set. In this case, output phase voltage is N+1 level. Figure 4.13 illustrates the case with phase-shift method on a phase leg with N=4.

For these cases, converter equivalent switching frequency, f_{c_eq}, is equal to number of carriers times the frequency of phase-shifted carriers, as in Equation (4.5).

$$f_{c\_eq} = N * f_c \tag{4.5}$$

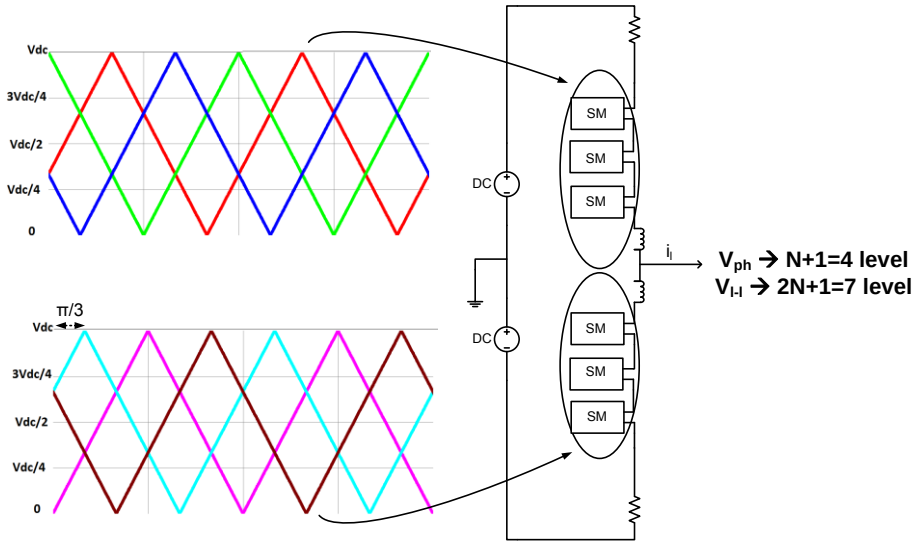


Figure 4.12 Carrier sets for N+1 level phase voltage of phase-shift method with odd number of submodules

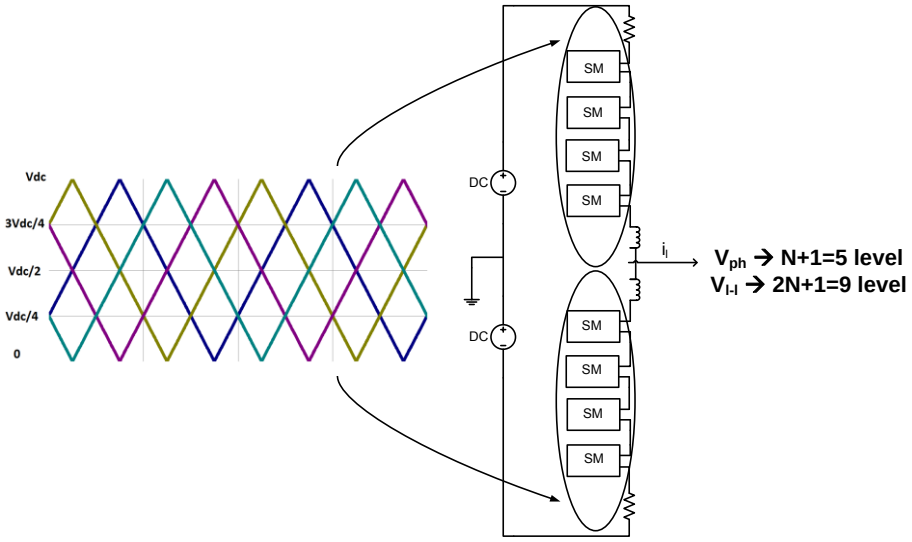


Figure 4.13 Carrier set for N+1 level phase voltage of phase-shift method with even number of submodules

4.4.1.2. 2N+1 Level Phase Voltages

4.4.1.2.1. Level-shift Methods

4.4.1.2.1.1. PD

In order to construct the phase voltage in 2N+1 level, PD method should be implemented with *a single carrier set* for both upper and lower arms. The single set is arranged in the same way as expressed in section 4.2.1.1.1. Submodules in upper and lower arms are switched with this carrier set. In this case, output phase voltage is 2N+1 level. Figure 4.14 illustrates the case with PD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the two times the frequency of the level-shifted carriers, as expressed in Equation (4.6).

$$f_{c\_eq} = 2 * f_c \tag{4.6}$$

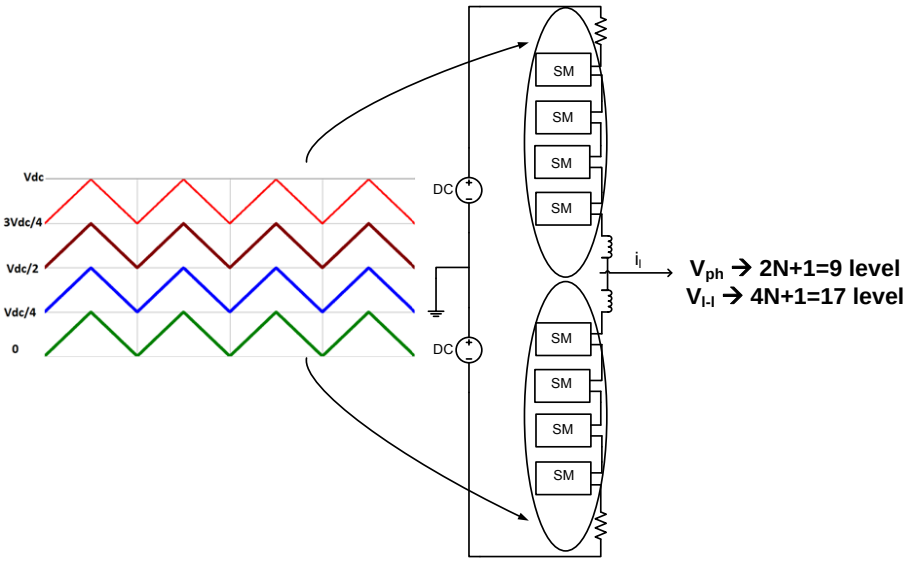


Figure 4.14 Carrier set for 2N+1 level phase voltage of PD method

4.4.1.2.1.2. POD

In order to construct the phase voltage in 2N+1 level, POD method should be implemented with *two different carrier sets* for upper and lower arms. First set of carriers is arranged in the same way as expressed in section 4.2.1.1.2. The second carrier set has again N identical carriers with amplitude of V_{dc}/N and displaced contiguously in the V_{dc} band, ranging from 0 to V_{dc}; however, this set also has a phase difference of π radians relative to the first set. Submodules in upper and lower arms are switched with the first and second carrier sets. In this case, output phase voltage is 2N+1 level. Figure 4.15 illustrates the case with POD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the two times the frequency of the level-shifted carriers, as expressed in Equation (4.7).

$$f_{c\_eq} = 2 * f_c \tag{4.7}$$

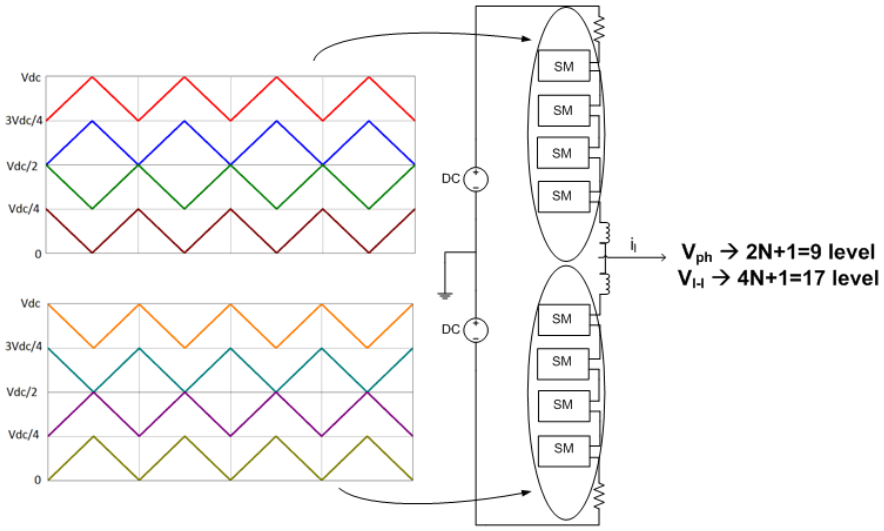


Figure 4.15 Carrier sets for 2N+1 level phase voltage of POD method

4.4.1.2.1.3. APOD

In order to construct the phase voltage in 2N+1 level, APOD method should be implemented with *two different carrier sets* for upper and lower arms. First set of carriers is arranged in the same way as expressed in section 4.2.1.1.3. The second carrier set has again N identical carriers with amplitude of V_{dc}/N and displaced contiguously in the V_{dc} band, ranging from 0 to V_{dc}; however, this set also has a phase difference of π radians relative to the first set. Submodules in upper and lower arms are switched with the first and second carrier sets. In this case, output phase voltage is 2N+1 level. Figure 4.16 illustrates the case with APOD method on a phase leg with N=4. In this case, converter equivalent switching frequency, f_{c_eq}, is equal to the two times the frequency of the level-shifted carriers, as expressed in Equation (4.8).

$$f_{c\_eq} = 2 * f_c \tag{4.8}$$

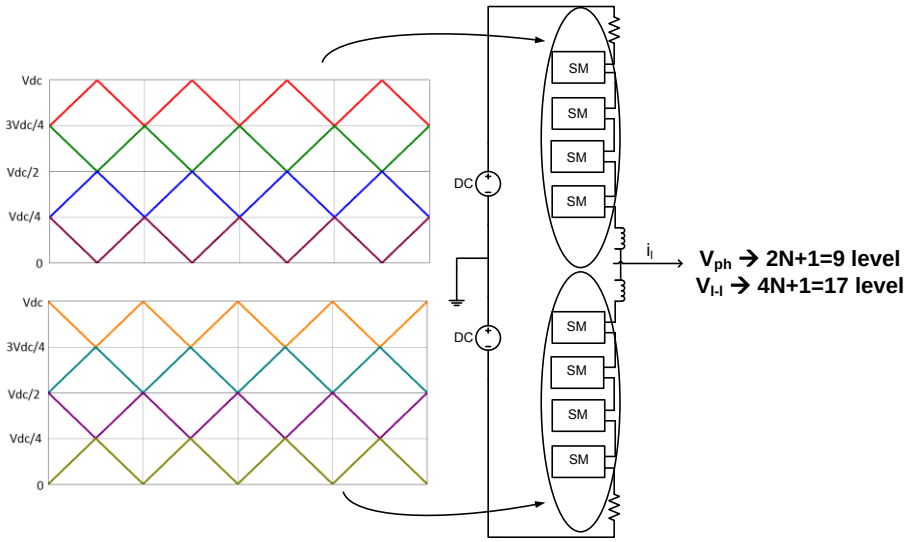


Figure 4.16 Carrier set for 2N+1 level phase voltage of APOD method

4.4.1.2.2. Phase-shift Method

For phase-shift method, carrier sets are arranged according to N being odd or even.

In case N is odd, a single carrier set is used for both upper and lower arms. The only carrier set is arranged in the same way as expressed in section 4.2.1.2. Submodules in upper and lower arms are switched with this carrier set. In this case, output phase voltage is 2N+1 level. Figure 4.17 illustrates the case with phase-shift method on a phase leg with N=3.

In case N is even, two different carrier sets are used for upper and lower arm. First set of carriers is arranged in the same way as expressed in section 4.2.1.2. The second set has again the same waveform, but with π/N radians phase difference with the first set. Submodules in upper and lower arms are switched with these first and second carrier sets. In this case, output phase voltage is 2N+1 level. Figure 4.18 illustrates the case with phase-shift method on a phase leg with N=4.

For these cases, converter equivalent switching frequency, f_{c_eq}, is equal to twice the number of carriers times the frequency of phase-shifted carriers, as expressed in Equation (4.9).

$$f_{c\_eq} = 2N * f_c \tag{4.9}$$

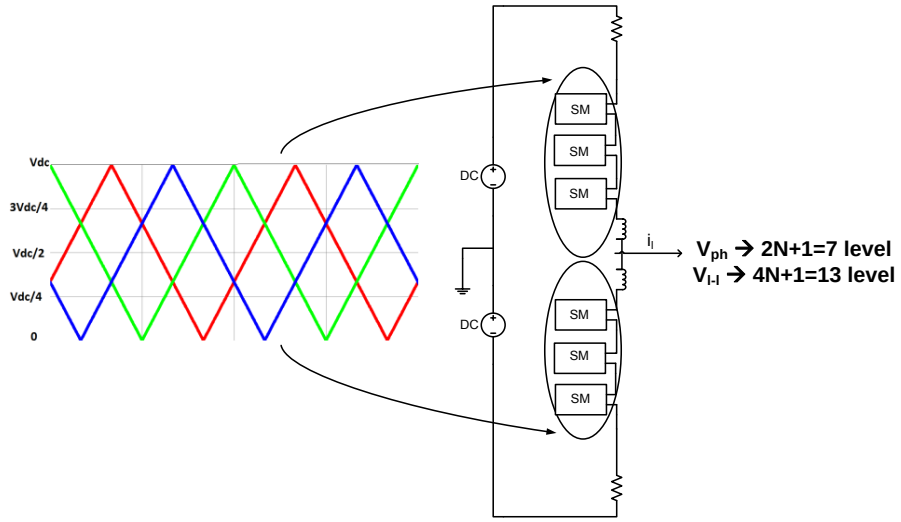


Figure 4.17 Carrier sets for 2N+1 level phase voltage of phase-shift method with odd number of submodules

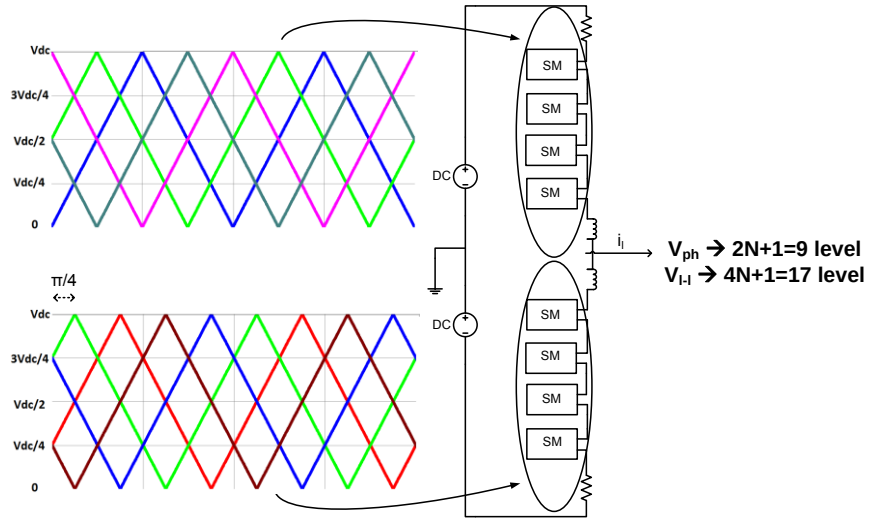


Figure 4.18 Carrier sets for 2N+1 level phase voltage of phase-shift method with even number of submodules

4.4.2. Analysis of Switching Pulse Patterns

Output voltage waveform of a converter takes on a shape starting from the switching pulse patterns generated by PWM signals. In order to get a fundamental insight on the output voltage characteristics of MMC, switching pulse patterns and respective output voltage waveforms shall be analyzed. For this aim, studies on all the scalar PWM methods were conducted using an MMC with N=4 as shown on Figure 4.19. Firstly, switching pulse patterns were obtained resulting from the carrier and reference signal comparison. Then, the resultant output voltage waveforms are analyzed, and their harmonic spectra are calculated. Performances of the methods were investigated using different amplitude modulation (m_a) and frequency modulation (m_f) indices. For MMC, calculations of m_a and m_f for different methods are shown on Table 4.1.

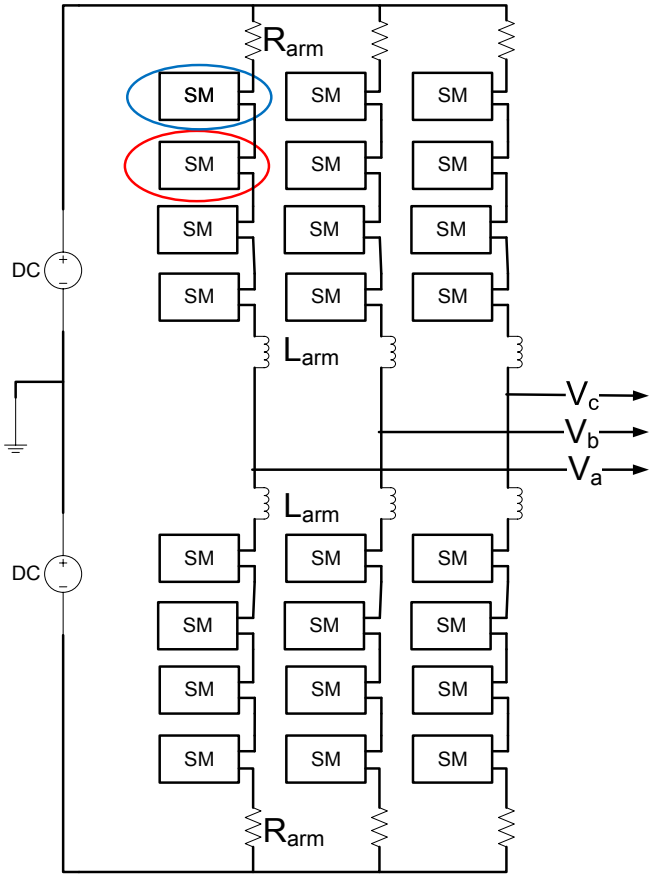


Figure 4.19 MMC with four submodules per arm

Table 4.1 m_a and m_f calculation for scalar PWM methods [13]

	Level-shift methods	Phase-shift method
m_a	$\frac{A_m}{\frac{n-1}{2} * A_c}$	$\frac{A_m}{A_c}$
m_f	$\frac{f_c}{f_m}$	

n : number of output phase-to-neutral voltage levels

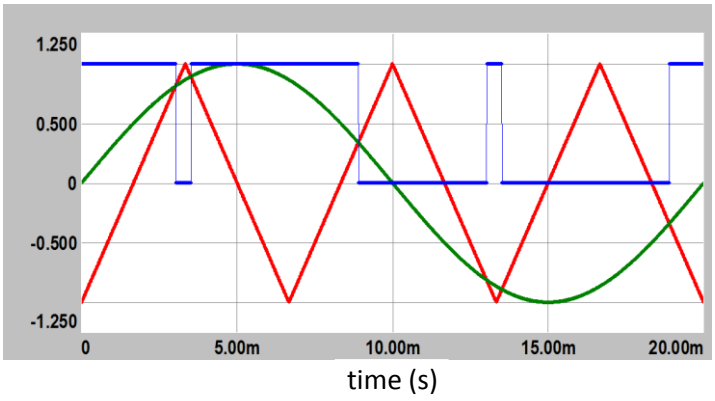
A_m : amplitude of modulation signal

A_c : amplitude of carrier signal

f_m : frequency of modulation signal

f_c : frequency of carrier signal

Exploring the carrier and reference waveforms of different scalar PWM methods, it is inferred that for the same m_a and m_f values, the PS method has much more total count of carrier and reference crossings (thus switching) than LS methods. Total count of switching in a phase leg for all the LS and PS PWM methods are computed for different systems with different number of carriers. It is observed that, irrespective of how many carriers are used, the PS method has a total count of switching which is approximately *number of carriers* times that of LS methods. As an example, one carrier (red) and reference (green) signal waveforms for PS and PD methods and the resultant switching pulse signal (blue) for a four carrier system (N=4) are illustrated in Figure 4.20, for m_a=1 and m_f=3 (f_c=50Hz).



(a)

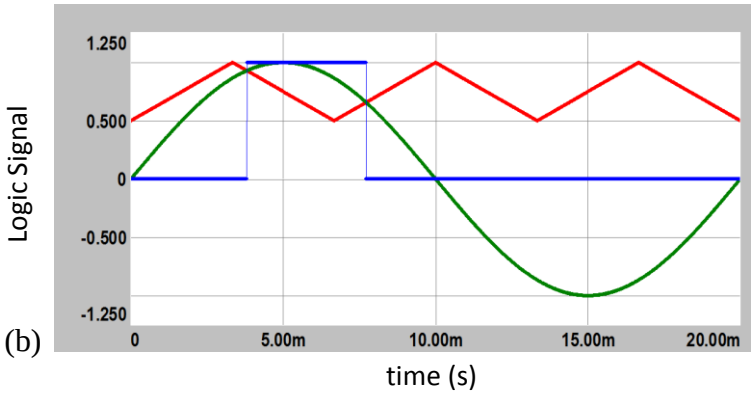


Figure 4.20 Carrier, reference and switching pulse signals for (a) PS and (b) PD methods for m_a=1 and m_f=3

As can be seen in Figure 4.20, for a four carrier system, for the same m_a and m_f values, PD method resulted in a single switching pulse, while PS method resulted in four (*number of carriers* times *number of switching pulses for PD method*) switching pulses for a period of reference signal. Indeed, rather than PD method, all LS methods have the same characteristics. In Figure 4.21 to Figure 4.24, similar switching pulse signals for PS and LS methods for different m_a and m_f values are illustrated again for four-carrier system in one period of reference signal (1/50Hz=20ms). Again an MMC with N=4, as shown in Figure 4.19, is used for PWM pulse pattern generation, via Matlab [32]. For simplicity and readability, two of the generated pulse patterns (corresponding to red and blue circled submodules in Figure 4.19) out of four for the whole phase arm, are shown. The red pulse pattern is scaled by two in order to distinguish among each other.

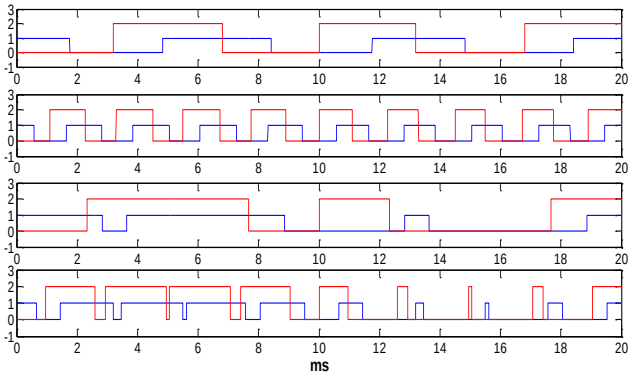


Figure 4.21 Switching pulse patterns of PS for (ma=0.1, mf=3), (ma=0.1, mf=9), (ma=0.9, mf=3) and (ma=0.9, mf=9) from the top to the bottom

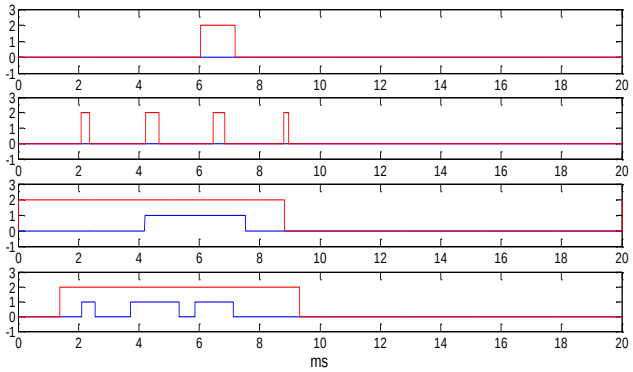


Figure 4.22 Switching pulse patterns of PD for (ma=0.1, mf=3), (ma=0.1, mf=9), (ma=0.9, mf=3) and (ma=0.9, mf=9) from the top to the bottom

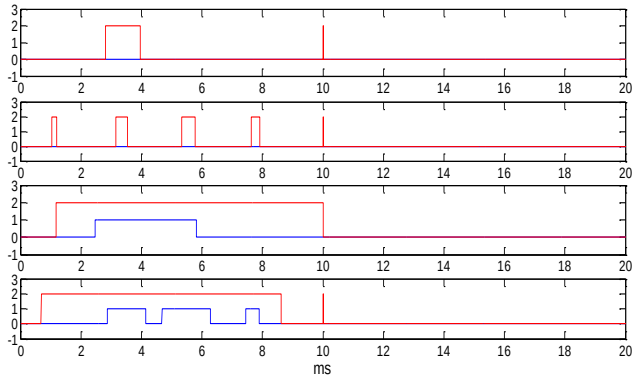


Figure 4.23 Switching pulse patterns of POD for (ma=0.1, mf=3), (ma=0.1, mf=9), (ma=0.9, mf=3) and (ma=0.9, mf=9) from the top to the bottom

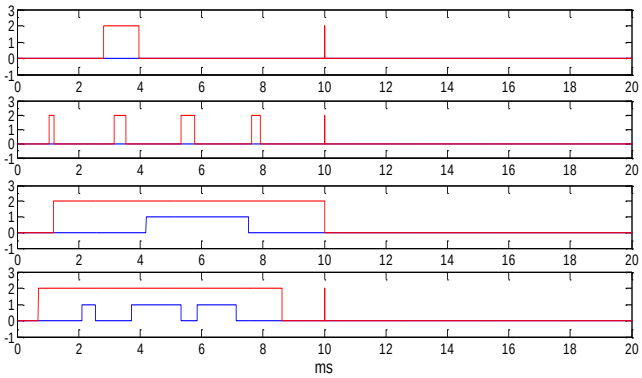


Figure 4.24 Switching pulse patterns of APOD for (ma=0.1, mf=3), (ma=0.1, mf=9), (ma=0.9, mf=3) and (ma=0.9, mf=9) from the top to the bottom

It is a well-known fact for a power converter, higher switching count implies higher output voltage waveform quality, but at the cost of increasing switching loss, thus reduced converter efficiency. In particular, for MMC whose target applications are at multi MW power rating, energy efficiency is an important characteristic. In this power range, the cost of energy lost in the switching and the thermal management costs of the converter sum up to noteworthy amounts. Therefore, a fair switching pulse pattern and output waveform characteristics comparison of scalar PWM methods for MMC should be based on "*equal total count of semiconductor switching per leg in a period of output voltage*" principle. In the light of above mentioned information, in order to obtain equal switching count, LS methods should be implemented with an m_f value which is *number of carriers times that of PS method*.

Switching pulses generated by PS and LS methods in one period of reference signal (1/50Hz=20ms) while keeping the above mentioned "equal switching count principle" are shown in Figure 4.25 to Figure 4.28.

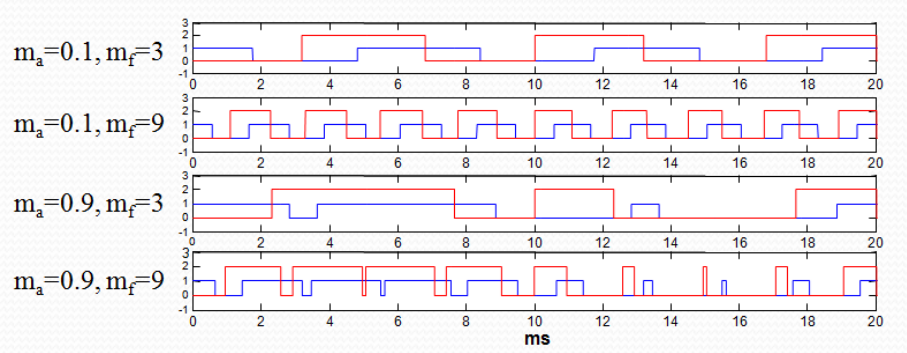


Figure 4.25 Switching pulse patterns of PS

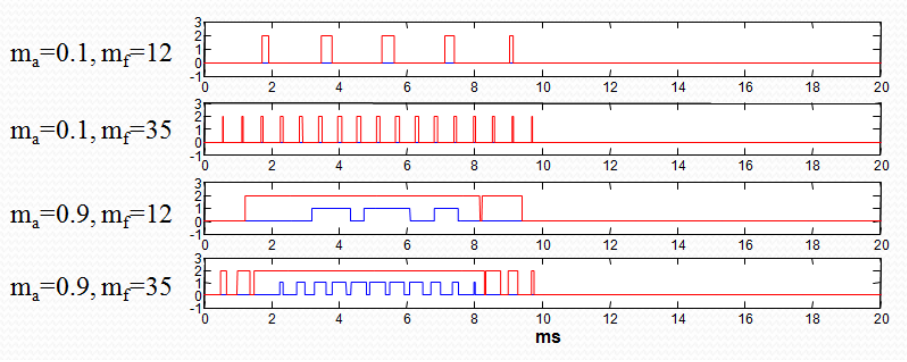


Figure 4.26 Switching pulse patterns of PD

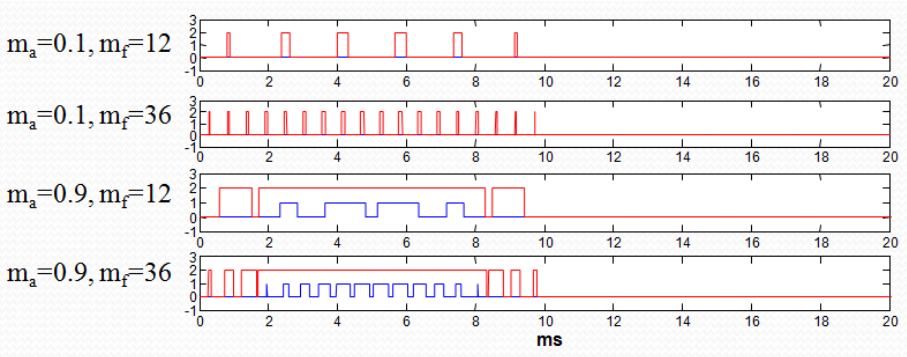


Figure 4.27 Switching pulse patterns of POD

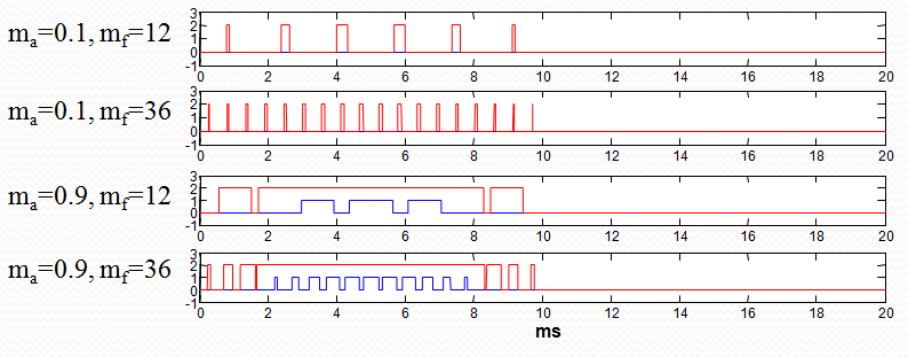


Figure 4.28 Switching pulse patterns of APOD

In the light of Figure 4.25, the pulse patterns generated by the PS method reveal that:

- Number of switching and switching manner resulting from different carriers in a system are highly similar to each other. This method generates much more homogeneous and balanced switching functions than that of the LS methods.
- Number of switching for each carrier and also total number of switching for all the carriers of a phase are dependent just on the m_f.
- All the carriers generate switching functions.
- Switching occurs in both of the half periods, since the carriers cover full dc band and so the carrier and reference signals cross in both half periods.

In the light of Figure 4.26, Figure 4.27 and Figure 4.28, the pulse patterns generated by the LS methods reveal that:

- Switching functions resulting from PD, POD and APOD are similar in terms of number of switching and switching instants.
- Number of switching and switching manner resulting from different carriers in a system are not equal to each other. These methods generate highly heterogeneous switching functions which could lead to unbalanced usage of semiconductors, high stress in terms of thermal conditions, unequal charge/discharge of submodule capacitors and therefore high circulating currents [47].

- Number of switching for each carrier is dependent both on m_a and m_f.
- Total number of switching for all the carriers of a phase is dependent on m_f.
- Depending on the sign of the carriers (being negative or positive), switching occurs in one of the half periods (for our case, in the first half cycle). In the other half period, switching function is constant, since the reference and carrier signals do not cross in that half period.
- Depending on m_a (for low m_a values), starting from the uppermost and lowermost carriers and going through to the zero crossing, some carrier pairs may not generate switching functions, having constant value [48].

4.4.3. Analysis of Generated Output Voltage Characteristics

4.4.3.1. N+1 Level Output Phase Voltage

Using the N+1 level output phase voltage generating method explained in section 4.4.1.1 and the switching pulse patterns illustrated at the bottom of Figure 4.25 to Figure 4.28 (those with m_a=0.9 and m_f=9 for PS, m_a=0.9 and m_f=36 for LS methods), normalized (1 unit of voltage for each level) output line voltages of a 5-level (9-level line-to-line) MMC system are generated for PS, PD, POD and APOD methods. It is important to remind that, these voltage waveforms are the outcome of only the scalar PWM pulse patterns generated by carriers and reference signal, and they are independent from any external control method as detailed in chapter 6. Each switching pulse in Figure 4.25 to Figure 4.28 corresponds to voltage level of unity. Output line voltage waveforms are shown in Figure 4.29 to Figure 4.32.

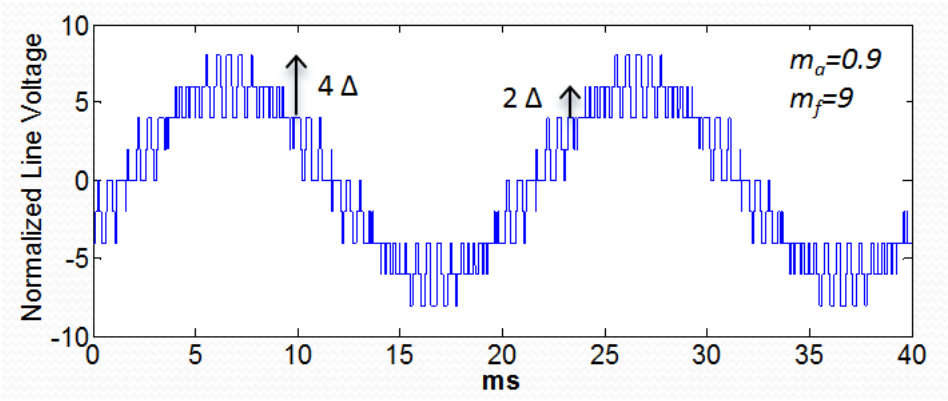


Figure 4.29 Normalized line voltage of PS for N+1 level V_{ph}

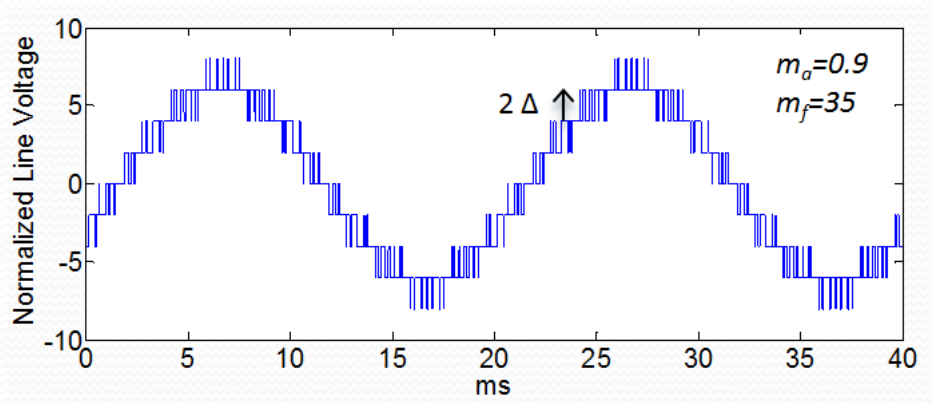


Figure 4.30 Normalized line voltage of PD for N+1 level V_{ph}

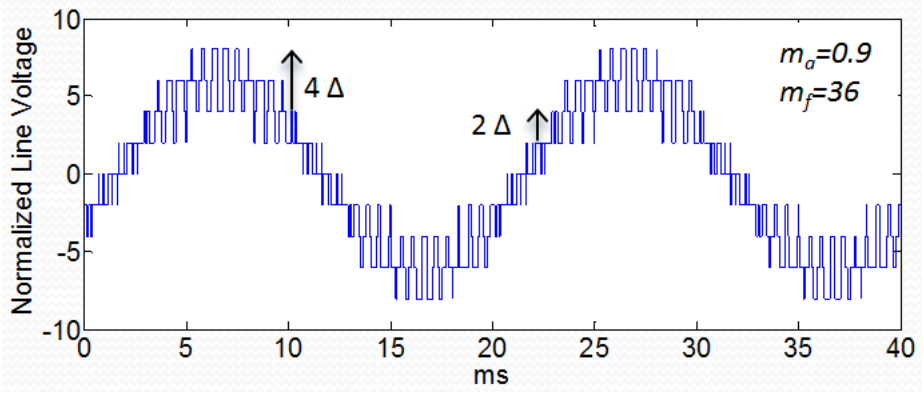


Figure 4.31 Normalized line voltage of POD for N+1 level V_{ph}

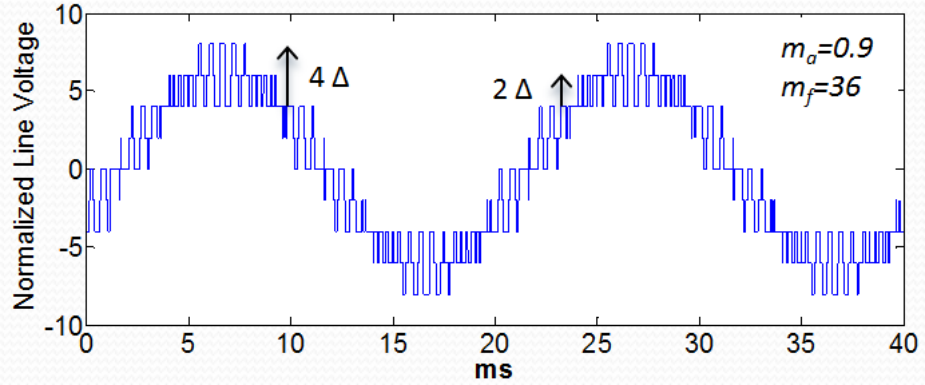


Figure 4.32 Normalized line voltage of APOD for N+1 level V_{ph}

The output line voltages, seen in Figure 4.29 to Figure 4.32, are all well-balanced and quarter wave symmetrical; but there exist differences in terms of transitions in voltage steps and voltage harmonics. Investigating Figure 4.29, for PS method, transitions from a voltage level to another may occur as four units (e.g. from level 8 to level 4) as well as two units (e.g. from level 6 to level 4). Actually, this phenomenon is the same for POD and APOD methods, also. On the other hand, for PD method, as seen in Figure 4.30, the transitions always occur as two units. These arguments are validated also by voltage waveforms of methods with different m_a values. Therefore, it is inferred that PD method gives a modulation function like unipolar switched PWM; whereas PS, POD and APOD methods give functions like bipolar switched PWM. This difference revealed its effects on the line voltage harmonics.

Current harmonics are the source of various power quality problems such as heating in the equipment, torque pulsations in motor drives, and heating and waveform distortion problems in grid connected inverters. Current harmonics are directly dependent on voltage harmonics divided by the output impedance. Therefore, for inductive loaded systems, which are the case for most ac motor drive and utility interface applications, low order harmonics are much more problematic, since high order ones are filtered greatly by the output inductance. In the light of this fact, line voltage harmonics of waveforms in Figure 4.29 to Figure 4.32 are weighted, based

on their orders and V_n/n terms are calculated. Weighted output line voltage harmonic spectrums can be seen in Figure 4.33, to Figure 4.36.

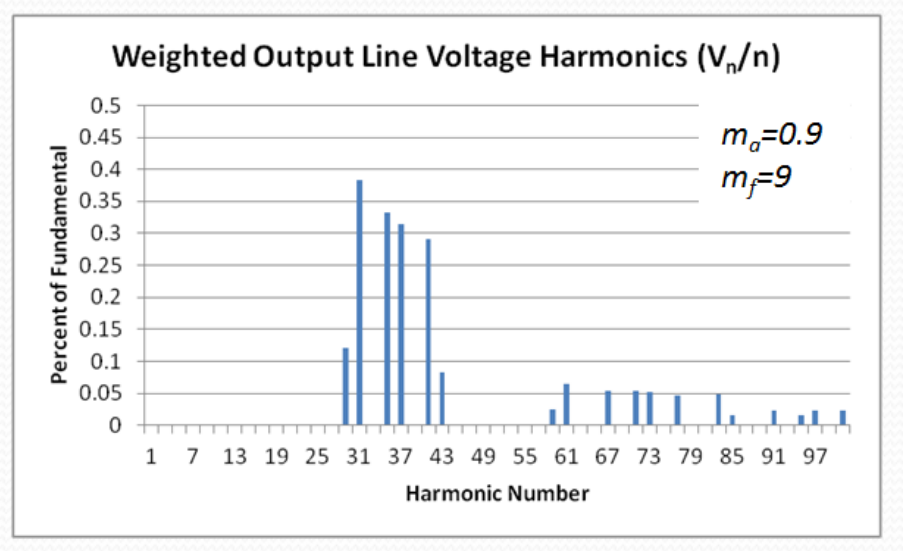


Figure 4.33 Weighted line voltage harmonics of PS for N+1 level V_{ph}

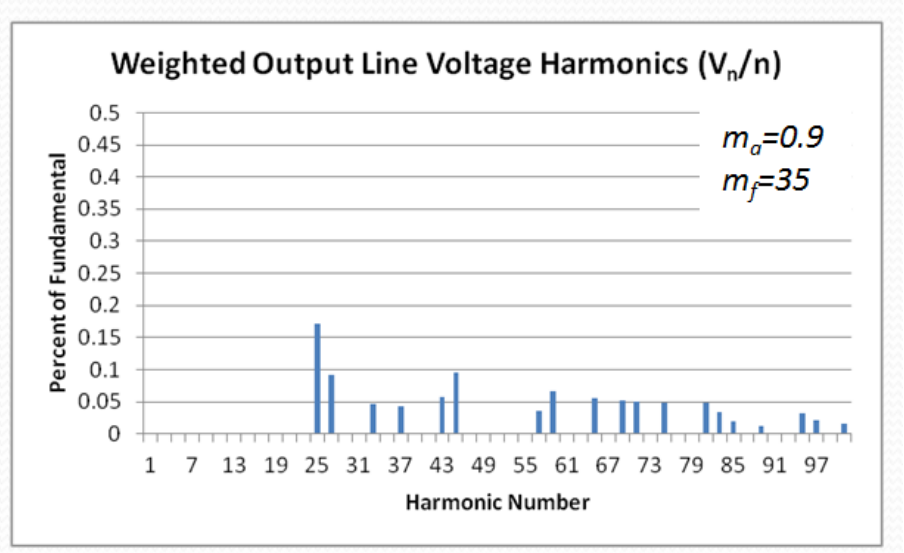


Figure 4.34 Weighted line voltage harmonics of PD for N+1 level V_{ph}

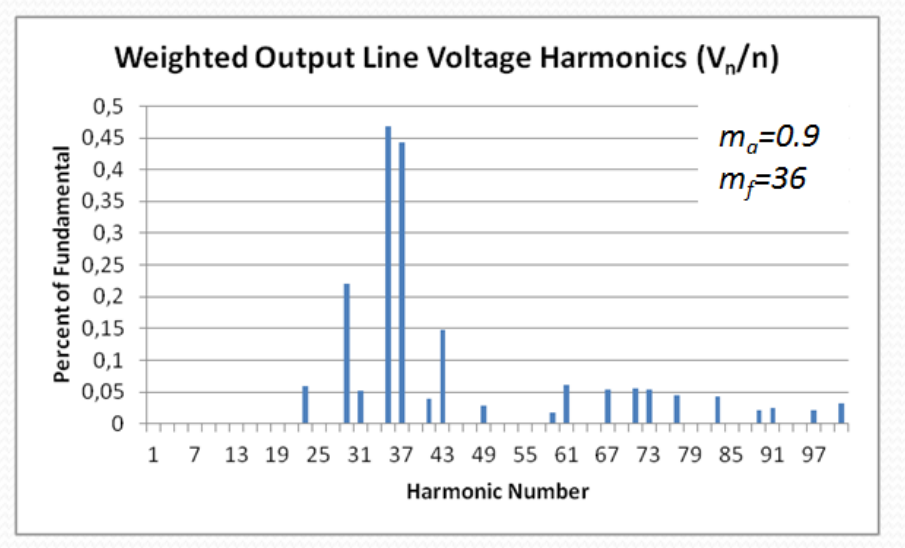


Figure 4.35 Weighted line voltage harmonics of POD for N+1 level V_{ph}

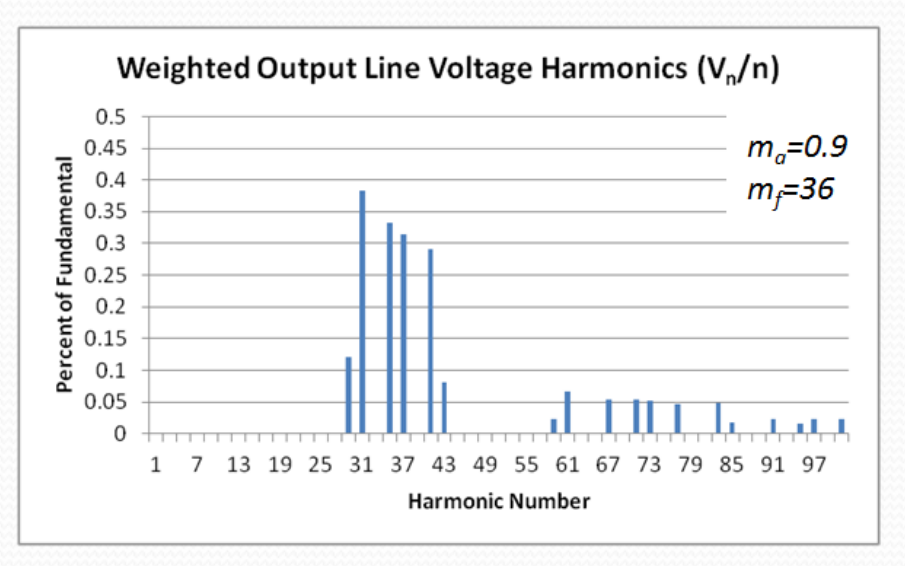


Figure 4.36 Weighted line voltage harmonics of APOD for N+1 level V_{ph}

Investigating Figure 4.33 to Figure 4.36, it is inferred that dominant harmonics of LS methods are centered about their carrier frequency, while that of PS method is centered about *number of carriers times its own carrier frequency*, which is indeed the converter apparent switching frequency as explained in section 4.2.1.2. Thus, the

dominant voltage harmonics locations of different methods are approximately equal as well as the converter apparent switching frequency. It is important to note that although PS method has the frequency multiplication feature in terms of converter switching frequency; this is not a distinct advantage since the total count of switching in a phase leg is the same for both PS and LS methods. Nevertheless, PD method, as a result of its unipolar characterized switching function, has much smaller harmonics magnitude compared to other methods. This advantage makes the PD method favorable, in terms of output harmonics distortion performance among the other LS and PS methods. Figure 4.37 and Figure 4.38 show weighted line voltage harmonic spectrum of PD method also for m_a=0.2 and m_a=0.6. For m_a=0.2, again the harmonics centered about carrier frequency are the dominant ones; while for m_a=0.6, harmonics about two times the carrier frequency as well as carrier frequency, are dominant.

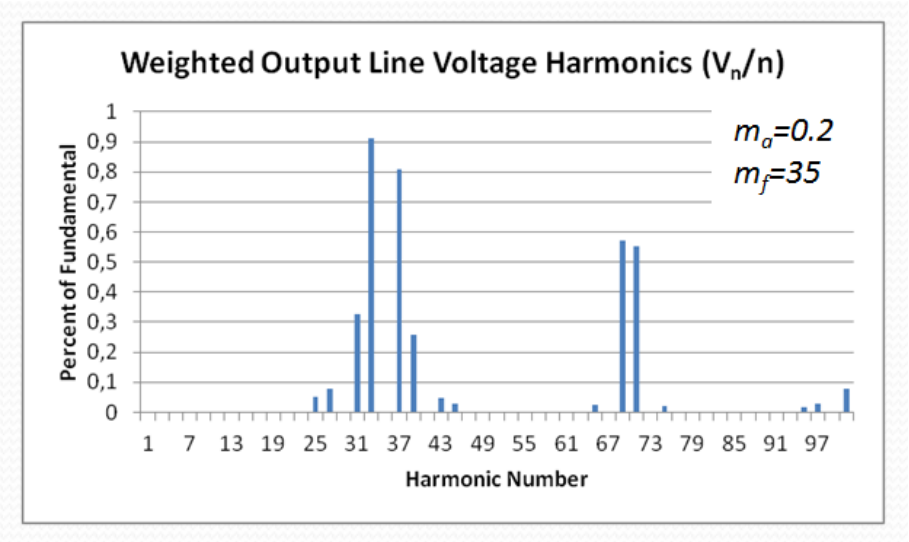


Figure 4.37 Weighted line voltage harmonics of PD for N+1 level V_{ph}

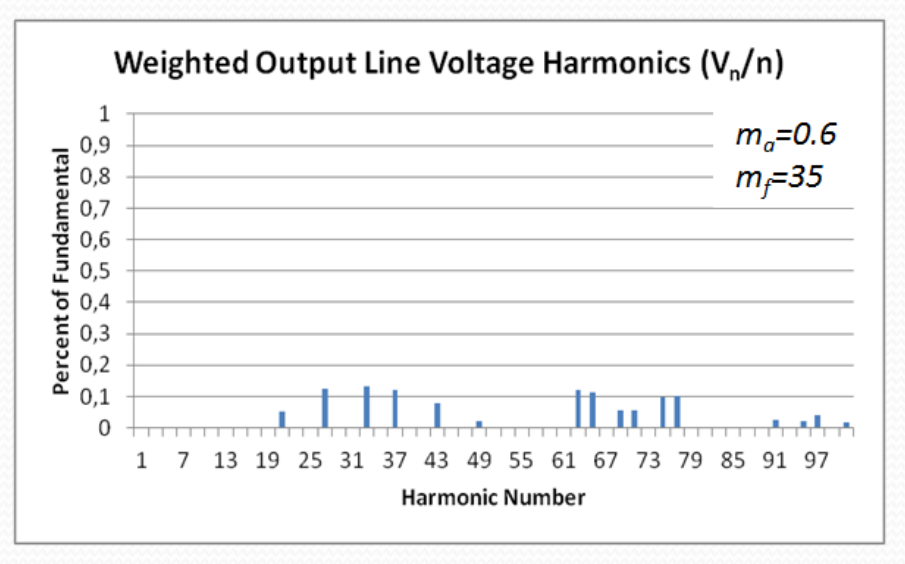


Figure 4.38 Weighted line voltage harmonics of PD for N+1 level V_{ph}

The analysis of weighted harmonic spectrums of line voltages for scalar PWM methods can be digitized and broadened to different amplitude modulation and frequency modulation indices by calculating "*weighted total harmonic distortion (WTHD)*" values of line voltage waveforms. Different from classical THD calculation, output line voltage WTHD calculation involves the effect of orders of harmonics. Therefore it is much like current harmonics of the converter. It is defined in percent as in Equation (4.10):

$$WTHD = \frac{\sqrt{\sum_{i=2}^{n}\left(\frac{V_{LLi}}{i}\right)^2}}{V_{LLi}} * 100 \tag{4.10}$$

where i is the harmonic order and V_{LLi} is the amplitude of the i^{th} line-to-line harmonic voltage. WTHD values are irrespective from the parameters of the topology used, giving a universal result. WTHD values of the four scalar PWM methods are calculated for varying m_a and varying m_f values separately. Figure 4.39 shows WTHD values for fixed m_f and varying m_a. Figure 4.40, on the other hand, shows WTHD values for fixed m_a and varying m_f. Again, total count of switching

throughout varying m_a or m_f ranges in Figure 4.39 and Figure 4.40 are the same for different PWM methods. It is important to note that, for Figure 4.39 and Figure 4.40, m_f values on the chart are valid for PS method, whereas that of LS methods are number of carriers (namely four) times shown m_f values.

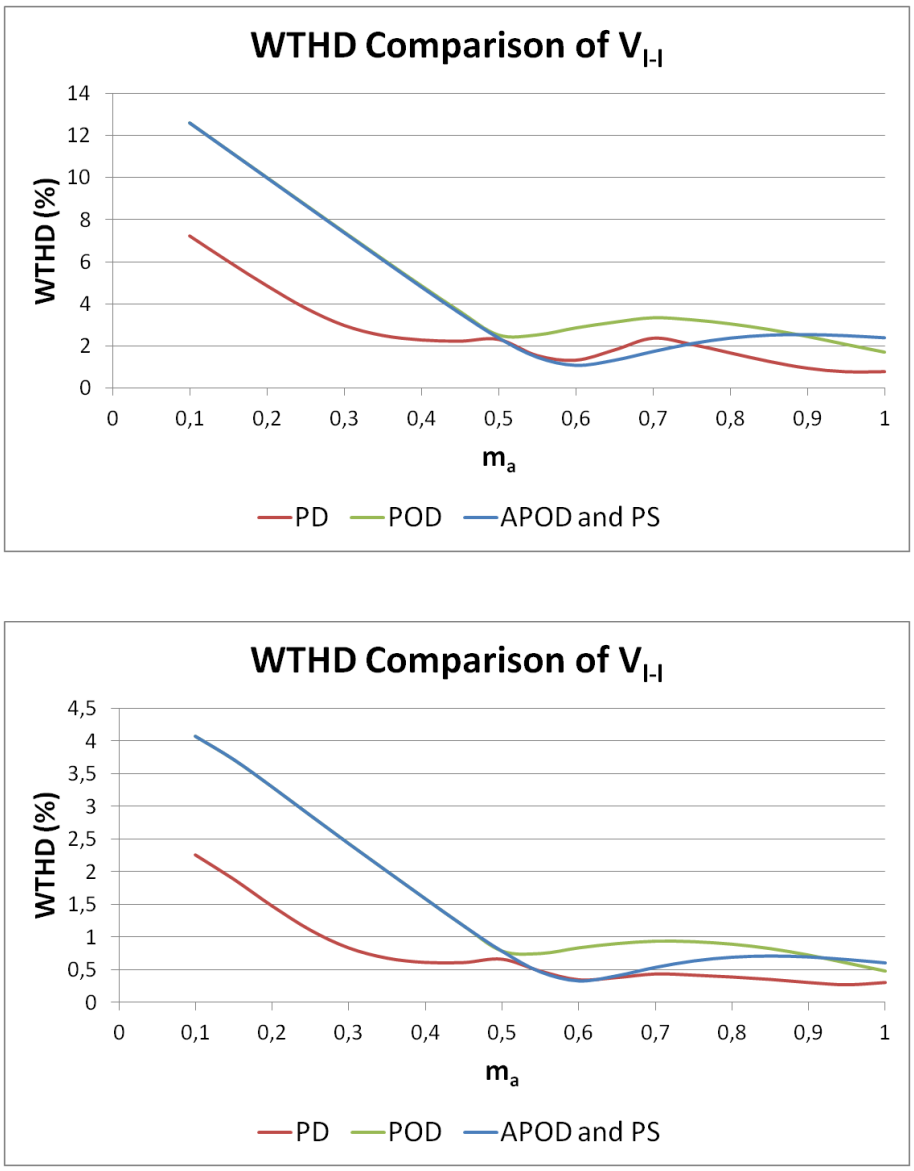
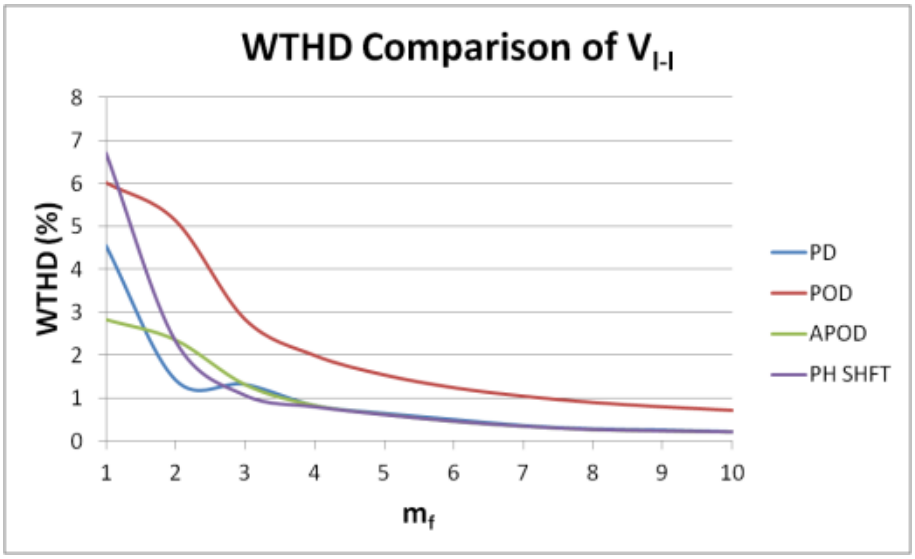


Figure 4.39 WTHD values for changing m_a and fixed m_f=3 and m_f=9 at the top and at the bottom, for N+1 level V_{ph}



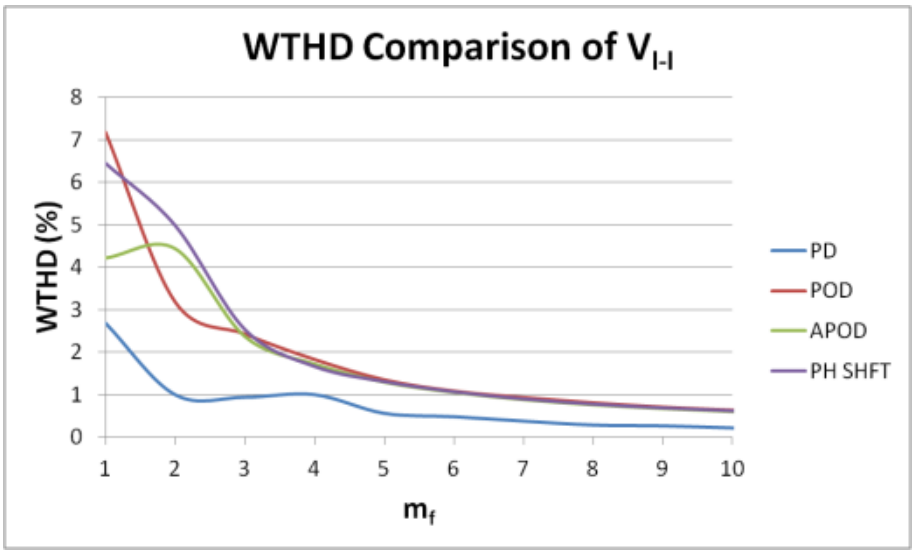


Figure 4.40 WTHD values for changing m_f and fixed m_a=0.6 and m_a=0.9 at the top and at the bottom, for N+1 level V_{ph}

Analyzing Figure 4.39, performances of POD, APOD and PS methods are similar especially at low modulation indices. PD method, on the other hand, has a significant superiority on WTHD performance at low modulation indices. At higher modulation indices, from m_a=0.5 and up, methods have more diverse WTHD performances, but PD method has generally the best performance again. It is clear that as m_f value (which also implies total count of switching) increases, WTHD

value decreases for the same m_a value, since the dominant voltage harmonics go to higher frequency range. Nonetheless, operating at higher m_f values, performances of different methods become close to each other, also verified by Figure 4.40, which shows that the methods' performances differ especially at low m_f values, specifically up to five. Therefore, it is important for an MMC being operated with the right scalar PWM method when keeping m_f value, and so switching loss, is lower. PD method again has, except for a few operation points, better characteristics throughout the m_f range. Consequently, both of the WTHD graphs highlight PD that it would be the right method for the converter with N+1 level V_{ph}, considering output voltage harmonics, with equal switching count provision [49].

4.4.3.2. 2N+1 Level Output Phase Voltage

Using the 2N+1 level output phase voltage generating method explained in section 4.4.1.2 and the switching pulse patterns illustrated at the bottom of Figure 4.25 to Figure 4.28 (those with m_a=0.9 and m_f=9 for PS, m_a=0.9 and m_f=36 for LS methods), normalized (1 unit of voltage for each level) output line voltages of a 9-level (17-level line-to-line) MMC system are generated for PS, PD, POD and APOD methods. Output line voltage waveforms are shown in Figure 4.41 to Figure 4.44.

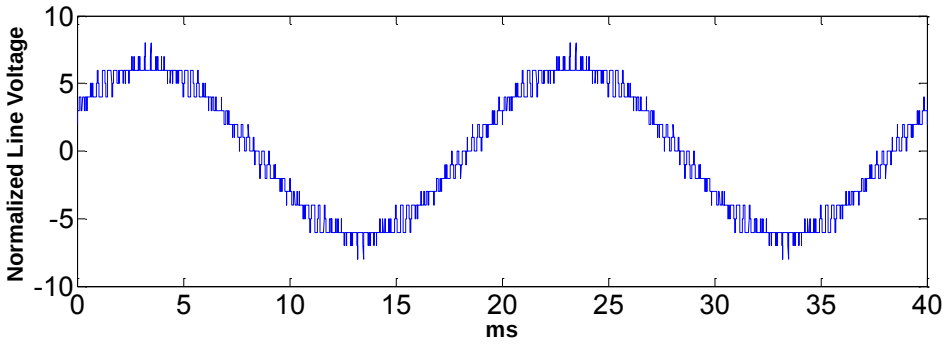


Figure 4.41 Normalized line voltage of PS for 2N+1 level V_{ph}

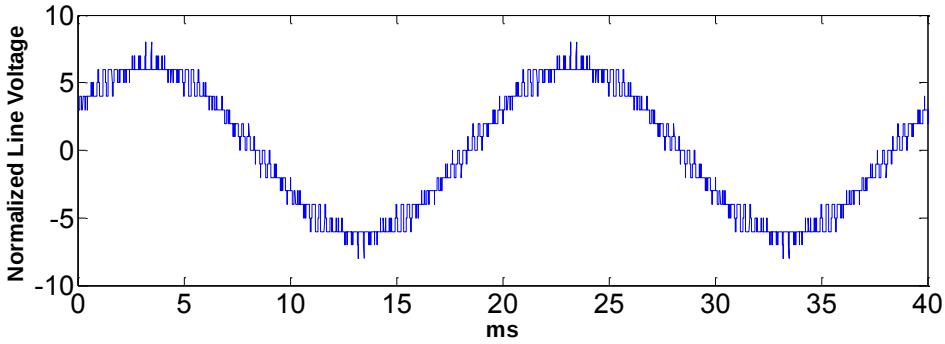


Figure 4.42 Normalized line voltage of PD for 2N+1 level V_{ph}

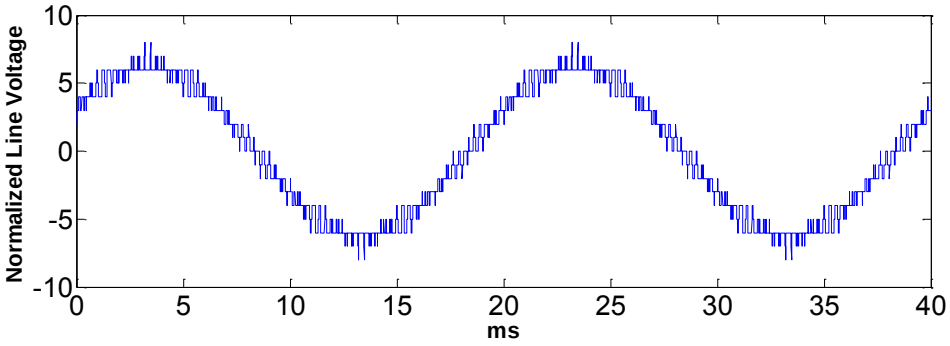


Figure 4.43 Normalized line voltage of POD for 2N+1 level V_{ph}

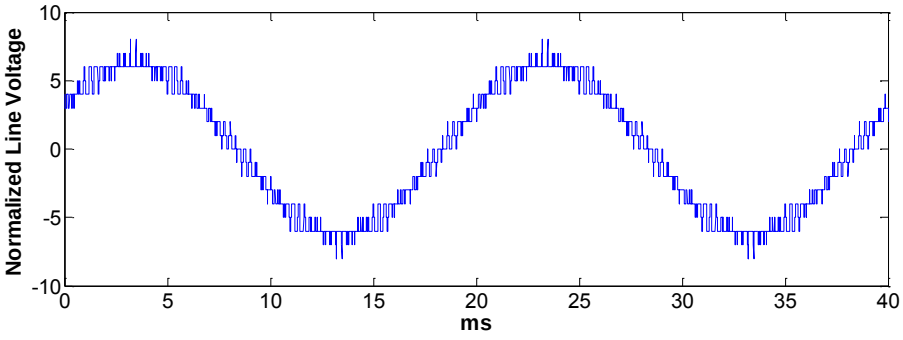


Figure 4.44 Normalized line voltage of APOD for 2N+1 level V_{ph}

The output line voltages, seen in Figure 4.41 to Figure 4.44, are all well-balanced and quarter wave symmetrical. The voltage transitions in the figures are all similar to each other and occurred as single or double units. There is no difference in the transitions as in the case of N+1 level phase voltage. All the LS and PS methods give a modulation function like bipolar switched PWM for 2N+1 level output phase voltage. The similarity between output voltage waveforms revealed its effects on the line voltage harmonics. Weighted line voltage harmonics of LS and PS methods are given in figures from Figure 4.45 to Figure 4.48.

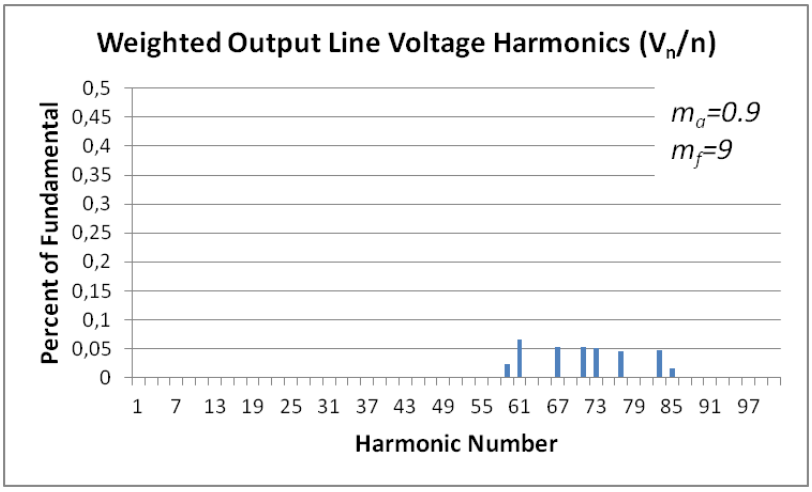


Figure 4.45 Weighted line voltage harmonics of PS for 2N+1 level V_{ph}

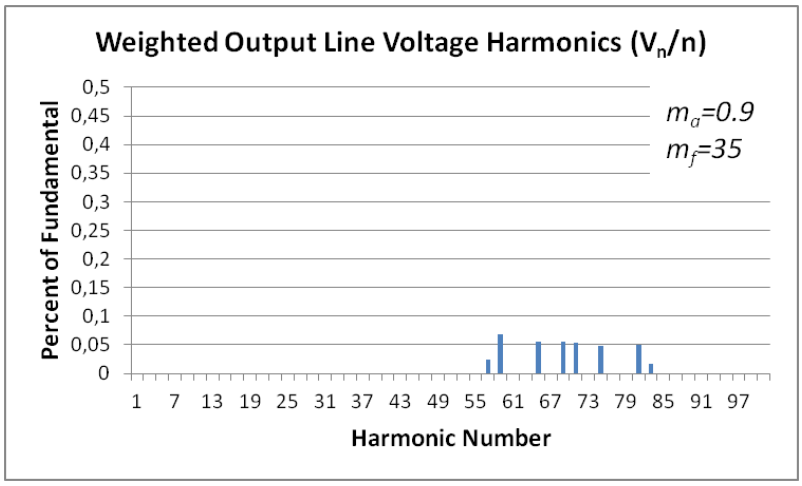


Figure 4.46 Weighted line voltage harmonics of PD for 2N+1 level V_{ph}

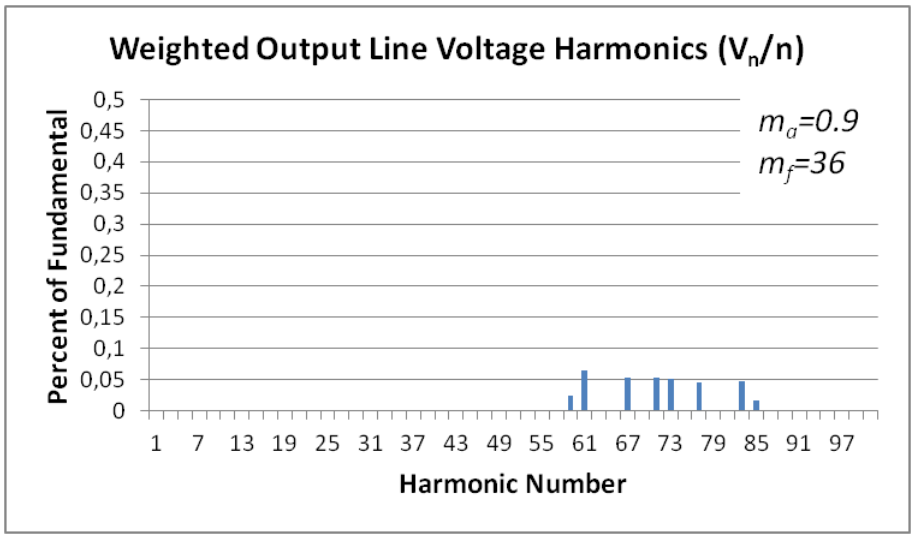


Figure 4.47 Weighted line voltage harmonics of POD for 2N+1 level V_{ph}

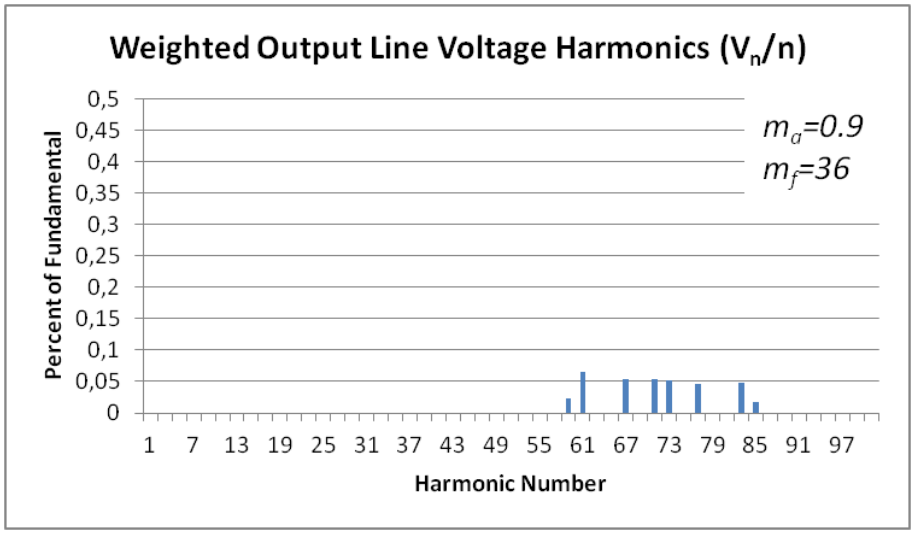
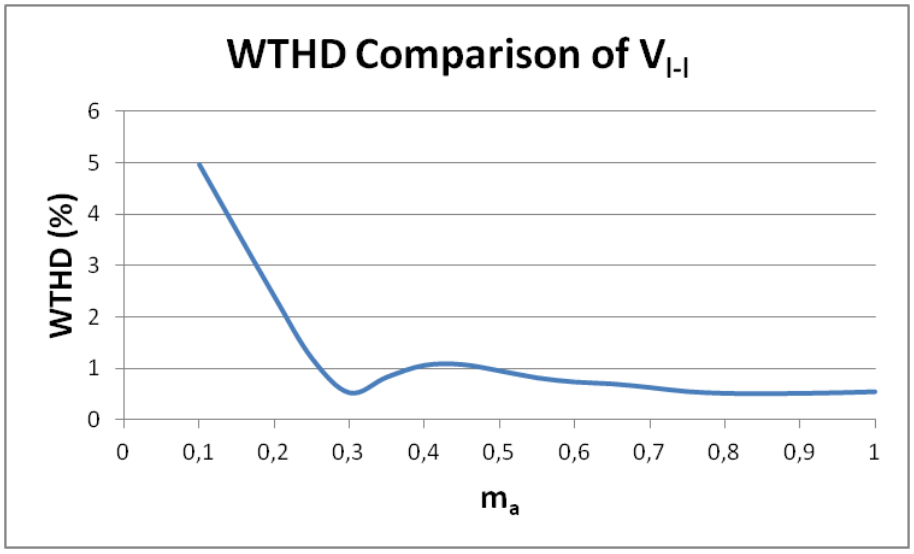


Figure 4.48 Weighted line voltage harmonics of APOD for 2N+1 level V_{ph}

Investigating Figure 4.45 to Figure 4.48, the similarity of different scalar PWM methods in terms of output voltage waveform can be argued. The locations of dominant harmonics are the same for LS and PS methods. As expected from section 4.4.1, they are at the sidebands of *twice of the carrier frequency* for LS methods and at the sidebands of *twice of the number of carriers times the carrier frequency* for PS

method. Therefore, the locations of dominant harmonics are again similar for LS and PS methods. Moreover, for this case, the amplitudes of weighted harmonics are similar to each other. The weighted line voltage harmonics for all the methods are about 0.05 percent of the fundamental harmonic. No method has a distinct advantage over others as in the case of N+1 level V_{ph}.

The analysis of weighted harmonic spectrums of line voltages for scalar PWM methods are again digitized and broadened to different amplitude modulation and frequency modulation indices by calculating WTHD values of line voltage waveforms. WTHD values of the four scalar PWM methods are calculated for varying m_a and varying m_f values separately. Figure 4.49 shows WTHD values for fixed m_f and varying m_a and Figure 4.50 shows WTHD values for fixed m_a and varying m_f. Again for these figures, m_f values on the chart are valid for PS method, whereas that of LS methods are number of carriers (namely four) times shown m_f values. The graphs shown on the figures are all valid for the whole LS and PS methods.



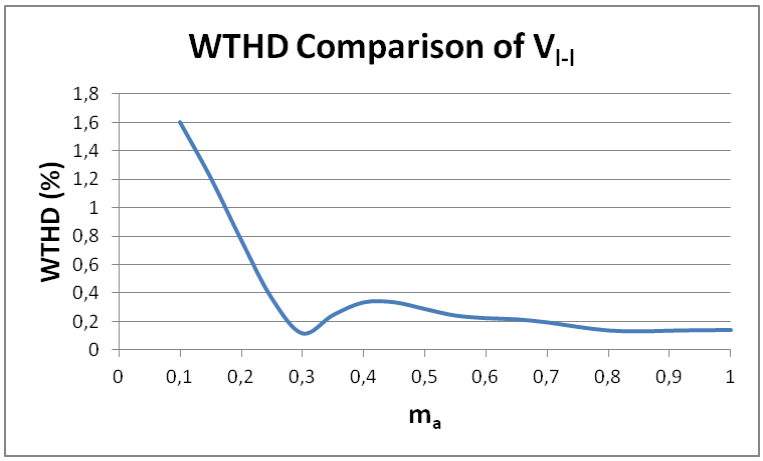


Figure 4.49 WTHD values for changing m_a and fixed m_f=3 and m_f=9 at the top and at the bottom, valid for all the LS and PS methods for 2N+1 level V_{ph}

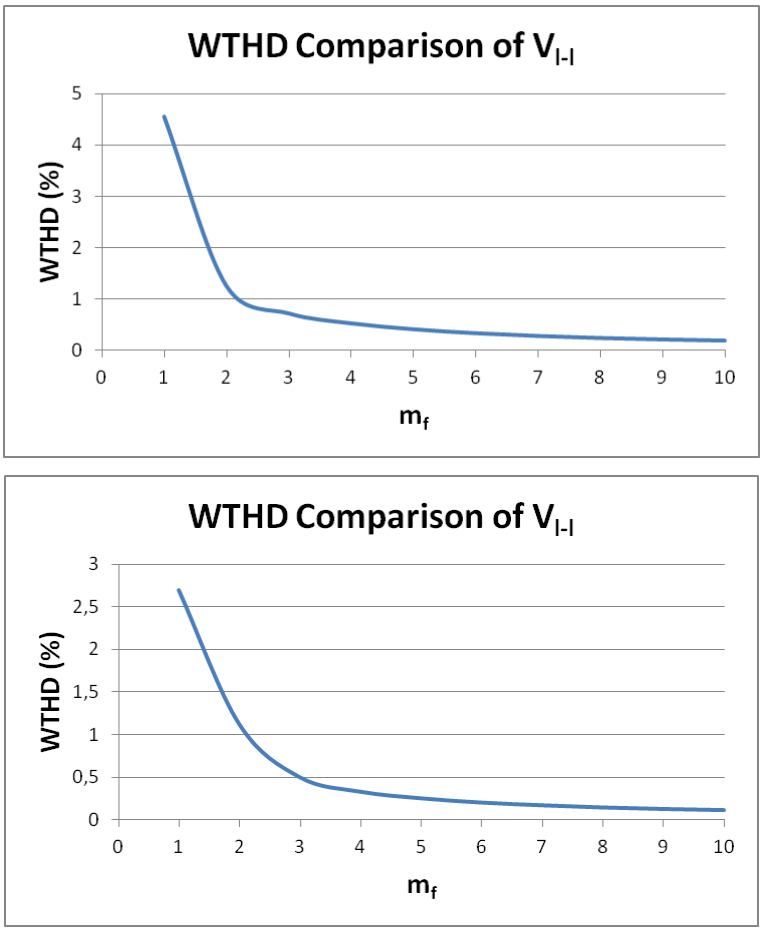


Figure 4.50 WTHD values for changing m_f and fixed m_a=0.6 and m_a=0.9 at the top and at the bottom, valid for all the LS and PS methods for 2N+1 level V_{ph}

Analyzing Figure 4.49 and Figure 4.50, the similarity of weighted harmonics in Figure 4.45 to Figure 4.48 are reflected to the WTHD values. All the scalar PWM methods have the same output line voltage WTHD values for changing m_a and changing m_f ranges. No method has an advantage for 2N+1 level V_{ph}.

4.5. Conclusion

In this chapter MMC switching methods, specifically carrier based PWM methods, are analyzed in detail. Implementation of carrier based PWM methods on the converter resulting in N+1 and 2N+1 level output voltage waveforms are explained. Their fundamental switching patterns, without any external control loop, are obtained. Resultant output voltage waveforms and their harmonic spectrum are analyzed with equal switching count per phase principle for each PWM method. The characteristics and performances of carrier based PWM methods are compared. The following results are obtained:

- PS method provides balanced and homogeneous pulse patterns for different carriers in the set, whereas LS methods yield unbalanced and heterogeneous patterns. Therefore, LS methods require additional precautions before being used for the switching of the converter, in order to prevent unbalanced exploitation of submodules.
- The locations of output voltage harmonics are similar to each other for LS and PS methods both for N+1 and 2N+1 level V_{ph}, as long as equal switching count principle is followed. It is important to note that, in order to maintain this principle, carrier frequency of LS methods shall be *N times that of PS method*. The locations are summarized in Table 4.2.

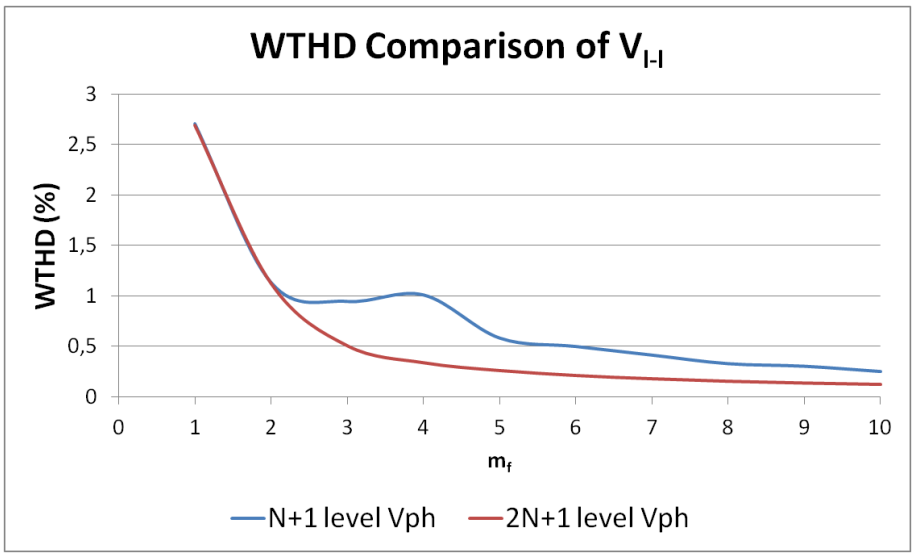
Table 4.2 Locations of output line voltage harmonics for scalar PWM methods

	N+1 level V_{ph}	**2N+1 level V_{ph}**
LS (all PD, POD and APOD)	f_c	2 x f_c
PS	N x f_c	2N x f_c

- In case N+1 level V_{ph} is generated, PD of LS methods has lower output voltage harmonics in magnitude than the other methods due to its unipolar switched PWM function. Therefore it is favorable to use PD method for N+1 level V_{ph}.

- In case 2N+1 level V_{ph} is generated, all the LS and PS methods give similar performances to each other in terms of the magnitude of output voltage harmonics. Not any method has an advantage. Therefore it is not consequential to use any method for 2N+1 level V_{ph}.

- For 2N+1 level V_{ph} case, since the output voltage level is doubled relative to N+1 level V_{ph} case, the locations of dominant harmonics are doubled also, getting smaller when weighted by their harmonic orders. WTHD comparison of N+1 and 2N+1 level V_{ph} generating methods are done in Figure 4.51. Since PD method gives the best performance for N+1 level case, in these figures the comparison is based on PD method. According to Figure 4.51, it is favorable to use 2N+1 level V_{ph} generating method for MMC switching, when only the output harmonics are of interest, with the purest form of carrier based PWM methods. The other effects of N+1 or 2N+1 level V_{ph} generating methods are detailed in chapter 7.



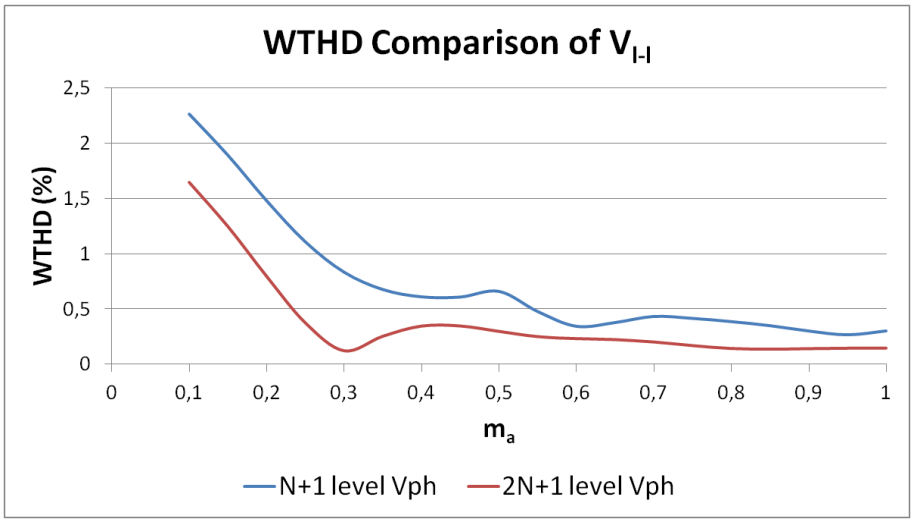


Figure 4.51 WTHD values for changing m_f and fixed m_a=0.9 at the top and changing m_a and fixed m_f=9 at the bottom, for N+1 and 2N+1 level V_{ph}

CHAPTER 5

MODULAR MULTILEVEL CONVERTER COMPONENT RATING DETERMINATION

5.1. Introduction

Converter circuit design and component rating determination of MMC is a multi task operation. In an MMC the ultimate circuit properties to be determined are the number of submodules per arm, the arm inductor and submodule capacitor value, as well as the semiconductor ratings. For sure, determination of all these values is highly dependent on each other, the MMC system to be implemented, load and waveform quality requirements and of course cost. In this section, the mathematical relations and limitations on number of submodules, arm inductor and submodule capacitor values will be provided for a proper MMC design.

5.2. Discussion on Number of Submodules per Arm

The number of submodules per arm, N, is among fundamental parameters of the MMC topology to be determined. As expressed in chapter 2, the ease of scalability to different voltage and power levels is one of the advantages of MMC topology to conventional two/three-level and other multilevel converter topologies. Indeed, this phenomenon is realized as a result of the submodule based structure of MMC. As N increased, higher output voltage and power ratings can be achieved. Therefore, determination of N is directly related with the dc-link voltage, output power and voltage characteristics. Moreover, since the increase in N results in the output waveform quality improvement, another constraint can be proposed by the desired

output harmonic content and THD value, while keeping the arm inductors the same. Actually, increase in N allows decreasing the arm inductor and output harmonic filter size. In practice, however, as long as the commercial submodules have fixed submodule capacitor value (or have alternatives with different capacitor values to be selected), there exists some constraints on N. First of all, the submodule voltage ratings should be respected. Given a dc-link voltage, Equation (5.1) sets a limit on the minimum value of N as below:

$$N \geq \frac{V_{dc}}{V_{sm,max}} \tag{5.1}$$

where, $V_{sm,max}$ stands for the maximum allowable voltage on individual submodule which is dependent on the submodule capacitor as well as semiconductor rating. Moreover, given the output power, Equation (5.2) sets another constraint on maximum value of N, based on energy storage requirement of converter and given a value for allowed submodule voltage ripple [50]:

$$N \leq \frac{C * \Delta V_c}{\frac{S}{3 * m_a * \omega_0 * V_{dc}^2}\left[1 - \left(\frac{m_a * cos\varphi}{2}\right)^2\right]^{3/2}} \tag{5.2}$$

where, ΔV_c is submodule capacitor voltage ripple, S is apparent power of the converter and ω_0 is fundamental frequency. Indeed, the equation emanates from the dimensioning of the submodule capacitor value assuming constant circulating current and negligible voltage unbalance between the submodules of the same arm. The proper number of N can be determined in the light of Equations (5.1) and (5.2), and with the output voltage harmonic content requirements. If the two equations do not meet up in a common interval, submodule capacitor should be changed accordingly.

5.3. Arm Inductor Value

Arm (buffer) inductor is one of the distinguishing components of MMC among other multilevel converters. Connected in series with the submodules, arm inductors filter the output current as well as the circulating current between the dc-link and phase leg. Therefore, arm current ripple, output current quality and semiconductor ratings are directly affected by the arm inductor. As explained in chapter 2, the voltage difference between the dc-link and phase leg causes a circulating current. Equation (3.25) is rewritten in Equation (5.3) for convenience.

$$L_{arm}\frac{di_{circ}}{dt} + R_{arm}i_{circ} = \frac{V_{dc}}{2} - \frac{v_p + v_n}{2} \tag{5.3}$$

The magnitude of the circulating current is shaped by the arm inductor and arm resistance. In [51] it is found that the circulating current is composed of even harmonics of output current and especially the second harmonic is dominant. In [52] circulating current second harmonic is found as in Equation (5.4):

$$I_{2f} = \frac{I_{dc}}{3\cos(\varphi)}\frac{N}{8\omega_0^2 L_{arm}C - N} \tag{5.4}$$

Then, arm inductor value can be found as in Equation (5.5):

$$L_{arm} = \frac{N}{8V_{dc}\omega_0^2 C}\left(\frac{S}{3I_{2f}} + V_{dc}\right) \tag{5.5}$$

where, S is apparent power of the converter. By this equation, given a maximum circulating current second harmonic ripple, it is possible to select the arm inductor value.

Moreover, in [47], another approach is tracked in terms of resonance frequency of the converter. The arm capacitance and arm inductance forms a resonance frequency of the

converter, giving a boost to the circulating current. Equation (5.6) gives the values of resonance frequencies:

$$\omega_r = \sqrt{\frac{N}{L_{arm}C}}\sqrt{\frac{2(n^2-1)+m_a^2n^2}{4n^2(n^2-1)}} \tag{5.6}$$

where, n=3k±1. If the converter is operated at the resonant frequency, then the n^{th} harmonic is only limited by the arm resistance, which is intentionally kept small for efficiency purposes. Therefore, it is suitable to operate the converter above the highest resonant frequency, which is obtained by n=2 and m_a=1. Then, the following constraint in Equation (5.7) is obtained for the multiplication of arm inductor and submodule capacitor:

$$L_{arm}C > \frac{5N}{24\omega_0^2} \tag{5.7}$$

In order to satisfy the Equation (5.7), the fundamental frequency of the converter should be above the highest resonant frequency, which results in big values of L_{arm} and/or C values. Therefore, neither the fundamental frequency nor the harmonics coincide with the resonant frequency.

In systems for which the output of the converter is connected to a voltage source, such as HVDC systems, in case of a short-circuit, the arm inductor limits the fault current. Therefore, apart from circulating current second harmonic elimination process, the second factor to take into account for arm inductor selection is the maximum rate of change of fault current. A short-circuit in dc side represents the worst case. Assuming the transient is short enough to keep the capacitor voltages unchanged and ignoring the arm resistance, Equation (5.8) gives the current through a phase leg of the converter:

$$L_{arm}\frac{di_p}{dt} + L_{arm}\frac{di_n}{dt} = V_{dc} \tag{5.8}$$

Since the fault current would be significantly larger than the nominal arm currents, upper and lower arm fault currents can be assumed equal. Then Equation (4.8) can be rewritten as in Equation (5.9):

$$2L_{arm}\frac{di_{p/n}}{dt} = V_{dc} \tag{5.9}$$

$$L_{arm} = \frac{V_{dc}}{2\frac{di_{p/n}}{dt}}$$

Equation (5.9) gives another constraint on the value of arm inductor, provided allowable fault current slope is available.

5.4. Submodule Capacitor Value

Selection of submodule capacitor value requires considering on the acceptable capacitor voltage ripple and the sizing, thus cost. As shown in Equations (3.17) and (3.18), submodule capacitors are charged/discharged by arm currents which are composed of half of the output current and circulating current. Thus, submodule capacitors voltage ripple is shaped according to magnitude and direction of these currents. Voltage ripple cannot be totally eliminated, but its magnitude can be lowered as the capacitance of submodule capacitors is increased and as the circulating current is controlled. The output current itself creates a voltage ripple in the capacitors at output current frequency and indeed it is inescapable. The circulating current, on the other hand, is composed of a dc and ac component in which the second harmonic is dominant. The ac component of circulating current causes extra voltage ripple on the submodule capacitors apart from the output current. Therefore, control of this ac component, especially the second harmonic, is

favorable in terms of suppressing submodule capacitor voltage ripple. The required capacitor value for a fixed voltage ripple can be decreased with proper control of circulating current ac component.

Submodule capacitors selection is based on maximum total energy stored in the converter and converter rated power. Energy-power ratio, which is given in Equation (5.10), should be kept in a range of 10J/kVA to 50J/kVA, depending on the application and converter [53].

$$EP = \frac{E_{Cmax}}{S_n} \tag{5.10}$$

where, E_{Cmax} is the maximum energy stored in capacitors and S_n is rated converter power. Lower energy-power ratio means reduction of capacitor size and cost, but in return for higher capacitor voltage ripple and vice versa. Maximum stored energy in submodule capacitors of three-phase converter is given by Equation (5.11):

$$E_{Cmax} = 6N * \frac{1}{2} C V_c^2 = 3NC \left(\frac{V_{dc}}{N}\right)^2 = \frac{3CV_{dc}^2}{N} \tag{5.11}$$

Then, using Equation (5.10) and (5.11), submodule capacitor value can be determined as in Equation (5.12):

$$C = \frac{EP * N * S_n}{3V_{dc}^2} \tag{5.12}$$

Apart from stored energy approach as given above, another predefined voltage ripple magnitude based approach is proposed in [97]. Assuming the circulating current contains no ac component, the submodule capacitor value is calculated as in Equation (5.13), with a predefined peak-to-peak capacitor voltage ripple magnitude.

$$C = \frac{P}{3 * N * m_a * V_c * \Delta V_c * \omega_0 * \cos\varphi}\left(1 - \left(\frac{m_a * \cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} \quad (5.13)$$

In the literature, approximately 10% peak voltage ripple of submodule capacitors is taken as acceptable [54], [95]-[96]. Higher capacitor values increase the volume of the system and the cost of the converter. Moreover, high capacitor values cause to slow down the response of the system to dynamic changes in dc-link. Therefore, submodule capacitors are chosen as small as possible, keeping the voltage ripple in acceptable range.

In section 7.2, the simulated converter circuit parameters are determined in the light of information given in this chapter.

CHAPTER 6

MODULAR MULTILEVEL CONVERTER SWITCHING AND CONTROL

6.1. Introduction

Switching and control methods and issues of modular multilevel converters are basically similar to other conventional two-level VSCs up to a point. For sure, as the topology differs from conventional VSCs, there exist some extra control loops and variations. First of all, the output active and reactive power control of the MMC, which can be called as basic VSC control, is fundamentally the same as conventional converters. As the submodule based structure of MMC distributes the energy stored in the converter to all the submodule capacitors, instead of a single dc side capacitor as in conventional two-level converters, an extra control requirement is emerged for MMC topology. That is equating the energy in all the submodules as much as possible, which also means equating the capacitor voltages of all submodules. If this voltage balance is not achieved, the stability of the converter cannot be guaranteed. In such cases, high internal currents may build up between the submodules and phases, and the output waveforms may distort. Additionally, the presence of circulating currents in the converter results in another control mechanism, suppression/control of the circulating current ac component as explained in chapter 2. This current component does not take part in the power transfer to the output and should be suppressed for high converter efficiency and low circuit component ratings.

It is important to note that, switching and modulation of MMC are much more integrated to each other than conventional VSCs. As explained in chapter 3, there exists a wide range of switching methods for MMC. As the switching methods branch, integration of control with these different switching methods has to be shaped accordingly. In this work, the carrier based PWM switching methods are used in the control loops of the MMC. Apart from output power control, which can be considered as common among all VSCs, for capacitor voltage balancing and circulating current suppression goals, in the literature there exist two fundamental control approaches, one is proposed in [2] by Lesnicar and Marquardt and the other is proposed in [22] by Hagiwara and Akagi. Both of the approaches will be detailed in next sections; but firstly, the common control loop, output power control, will be explained.

6.2. Output Power Control

Output power control of MMC is similar to conventional two- or three-level converters' synchronous frame dq current control where the VSC output voltage is adjusted to a calculated value in order to track the actual active and reactive power references [55]. In this method, after the transformation of output currents from abc stationary reference frame to dq rotating reference frame such that the d axis is aligned on the grid voltage vector, i_d current is controlled to track active power and i_q current is controlled to track reactive power. Thus, to have the output current vector in phase with the output voltage vector (i.e. for unity power factor), i_q should be zero. The active and reactive powers produced by the converter are given by Equations (6.1) and (6.2), which are based on instantaneous power theory [101]:

$$P = \frac{3}{2}\left(v_{l\_d} i_{l\_d} + v_{l\_q} i_{l\_q}\right) \tag{6.1}$$

$$Q = \frac{3}{2}\left(v_{l\_q} i_{l\_d} - v_{l\_d} i_{l\_q}\right) \tag{6.2}$$

Assuming that the d axis is completely aligned with the converter output voltage such that $v_{l\_q} = 0$, the Equations (6.1) and (6.2) reduces to Equations (6.3) and (6.4):

$$P = \frac{3}{2} v_{l\_d} i_{l\_d} \tag{6.3}$$

$$Q = -\frac{3}{2} v_{l\_d} i_{l\_q} \tag{6.4}$$

The reference i_d and i_q output currents can be calculated by Equations (6.3) and (6.4) for a fixed output voltage and power. Figure 6.1 shows the block diagram of active and reactive power control for MMC.

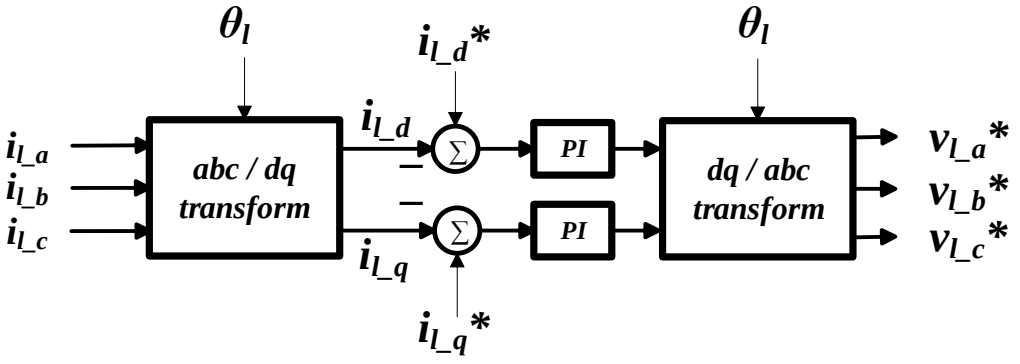


Figure 6.1 Block diagram of active and reactive power control for MMC

In Figure 6.1, i_{l_a}, i_{l_b} and i_{l_c} stand for the output phase a, b and c currents, θ_l stands for output displacement angle in rad/s for abc/dq transformation. abc/dq transformation is detailed in Appendix A. i_{l_d} and i_{l_q} are transformed output currents in dq reference frame. $i^*_{l\_d}$ and $i^*_{l\_q}$ are the reference currents in dq frame. θ_l can be obtained by phase locked loop (PLL) configuration for grid connected systems or by field oriented control for motor drives. In order to track the reference values of $i^*_{l\_d}$ and $i^*_{l\_q}$ currents, PI controllers are utilized owing to their superiority in reference tracking with zero steady-state error. The design of the PI controller

relies on the pole-zero placement methodology. The aim of this method is to consider the total closed loop, from the error calculation until the current output of the converter, as a first order system. The controller is parameterized according to the controlled system and the bandwidth of the closed loop. In this way, the calculation of the PI gains is simplified. In Figure 6.2 the overview of the output current controller and the physical system is illustrated.

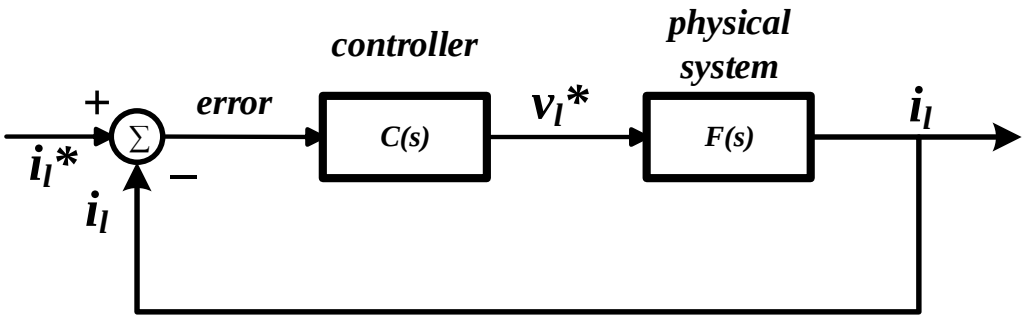


Figure 6.2 Overview of the output current PI controller and physical system

Based on Equation (3.28), equivalent circuit of MMC in terms of output currents is illustrated in Figure 6.3, and (3.28) is reordered as in Equation (6.5) taking the output resistance and inductance into account.

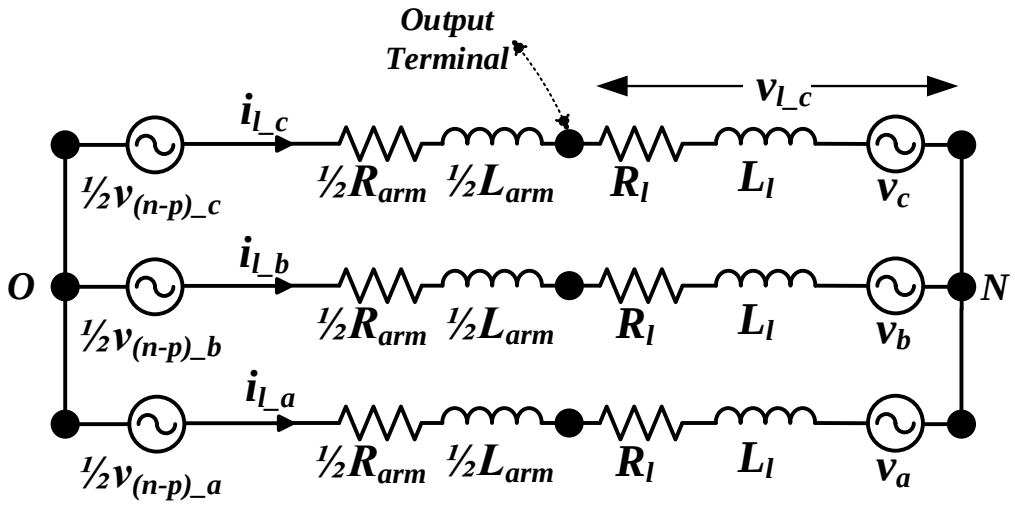


Figure 6.3 Equivalent circuit of MMC in terms of output currents

$$v_o + \left(\frac{R_{\text{arm}}}{2} + R_l\right) i_l + \left(\frac{L_{\text{arm}}}{2} + L_l\right) \frac{di_l}{dt} = \frac{v_n - v_p}{2} = e_v \tag{6.5}$$

Equation (6.5) can be arranged to dq coordinates as in Equation (6.6):

$$e_{v\_dq} = v_{o\_dq} + \left(\frac{R_{\text{arm}}}{2} + R_l\right) i_{l\_dq} + \left(\frac{L_{\text{arm}}}{2} + L_l\right) \frac{di_{l\_dq}}{dt} + j\omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) i_{l\_dq} \tag{6.6}$$

$$e_{v\_d} = v_{o\_d} + \left(\frac{R_{\text{arm}}}{2} + R_l\right) i_{l\_d} + \left(\frac{L_{\text{arm}}}{2} + L_l\right) \frac{di_{l\_d}}{dt} - \omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) i_{l\_d} \tag{6.7}$$

$$e_{v\_q} = v_{o\_q} + \left(\frac{R_{\text{arm}}}{2} + R_l\right) i_{l\_q} + \left(\frac{L_{\text{arm}}}{2} + L_l\right) \frac{di_{l\_q}}{dt} + \omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) i_{l\_q} \tag{6.8}$$

As seen in Equations (6.7) and (6.8) there is an interaction among the quantities of d axis and q axis currents through coupling terms as $\omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) i_{l\_q}$ and $\omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) i_{l\_d}$. Solving Equation (6.6) for $\frac{di_{l\_dq}}{dt}$ and applying Laplace transformation gives:

$$i_{l\_dq} = \frac{e_{v\_dq} - v_{o\_dq}}{\left(\frac{R_{\text{arm}}}{2} + R_l\right) + j\omega \left(\frac{L_{\text{arm}}}{2} + L_l\right) + \left(\frac{L_{\text{arm}}}{2} + L_l\right) \text{s}} \tag{6.9}$$

The Laplace transformation of PI controller, C(s), is defined as in Equation (6.10):

$$C(s) = K_p + \frac{K_i}{\text{s}} \tag{6.10}$$

Then, the block diagram in Figure 6.2 is rearranged as in Figure 6.4.

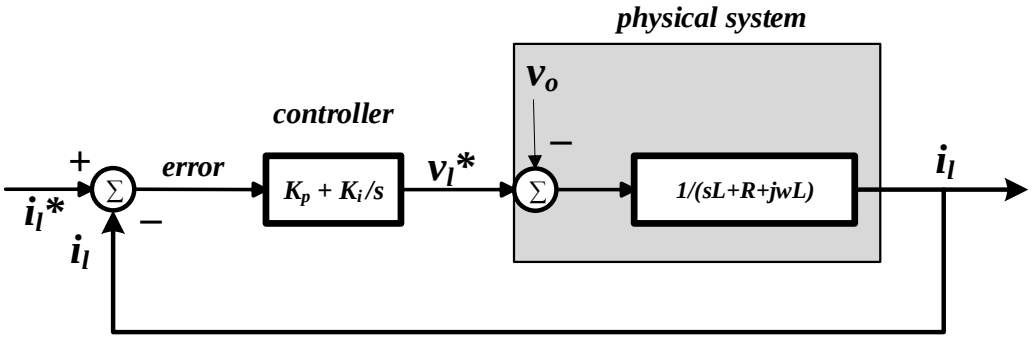


Figure 6.4 Overview of the output current PI controller and physical system with output voltage

The coupling terms and output voltage are temporarily ignored to ease the design of the current controller. Then, the physical system seen by the controller is reduced to Equation (6.11):

$$i_{l\_dq} = \frac{e_{v\_dq}}{\left(\frac{R_{\text{arm}}}{2} + R_l\right) + \left(\frac{L_{\text{arm}}}{2} + L_l\right)\text{s}} \tag{6.11}$$

The closed loop transfer function of Figure 6.2 is given in Equation (6.12):

$$G(s) = \frac{C(s)F(s)}{1 + C(s)F(s)} = \frac{i_{l\_dq}}{i^*_{l\_dq}} \tag{6.12}$$

As expressed previously, the closed loop system is to be a first order system whose transfer function can be written as in Equation (6.13):

$$G(s) = \frac{a_c}{s + a_c} \tag{6.13}$$

where, a_c is the bandwidth of the controller. Setting Equation (6.12) and (6.13) equal to each other results in Equation (6.14):

$$G(s) = \frac{C(s)F(s)}{1 + C(s)F(s)} = \frac{a_c}{s + a_c} = \frac{{a_c}/{s}}{1 + {a_c}/{s}} \tag{6.14}$$

Then, $C(s)F(s)$ is equal to ${a_c}/{s}$ and $C(s)$ can be defined as in Equation (6.15):

$$\begin{aligned} C(s) = F^{-1}(s)\frac{a_c}{s} &= \left(s\left(\frac{L_{\text{arm}}}{2} + L_l\right) + \left(\frac{R_{\text{arm}}}{2} + R_l\right)\right)\frac{a_c}{s} \\ &= a_c\left(\frac{L_{\text{arm}}}{2} + L_l\right) + \frac{a_c}{s}\left(\frac{R_{\text{arm}}}{2} + R_l\right) = K_p + \frac{K_i}{\text{s}} \end{aligned} \tag{6.15}$$

As given in Equation (6.15), controller gains are expressed in terms of circuit parameters and bandwidth of the controller. Bandwidth of the controller is chosen as one tenth of the equal switching frequency of the converter in rad/s. It is important to remind the different values of switching frequency of the converter from chapter 4 for different scalar PWM methods. Bandwidth of the converter, K_p and K_i are expressed in Equations (6.16), (6.17) and (6.18), respectively.

$$a_c = 2\pi\frac{f_{c\_eq}}{10} \tag{6.16}$$

$$K_p = a_c\left(\frac{L_{\text{arm}}}{2} + L_{\text{l}}\right) = 2\pi\frac{f_{c\_eq}}{10}\left(\frac{L_{\text{arm}}}{2} + L_{\text{l}}\right) \tag{6.17}$$

$$K_i = a_c\left(\frac{R_{\text{arm}}}{2} + R_{\text{l}}\right) = 2\pi\frac{f_{c\_eq}}{10}\left(\frac{R_{\text{arm}}}{2} + R_{\text{l}}\right) \tag{6.18}$$

In this way, the PI controller sees the converter as a first order system. As the ignored terms, coupling term and output voltage, are included, Figure 6.5 shows the whole block diagram of the converter.

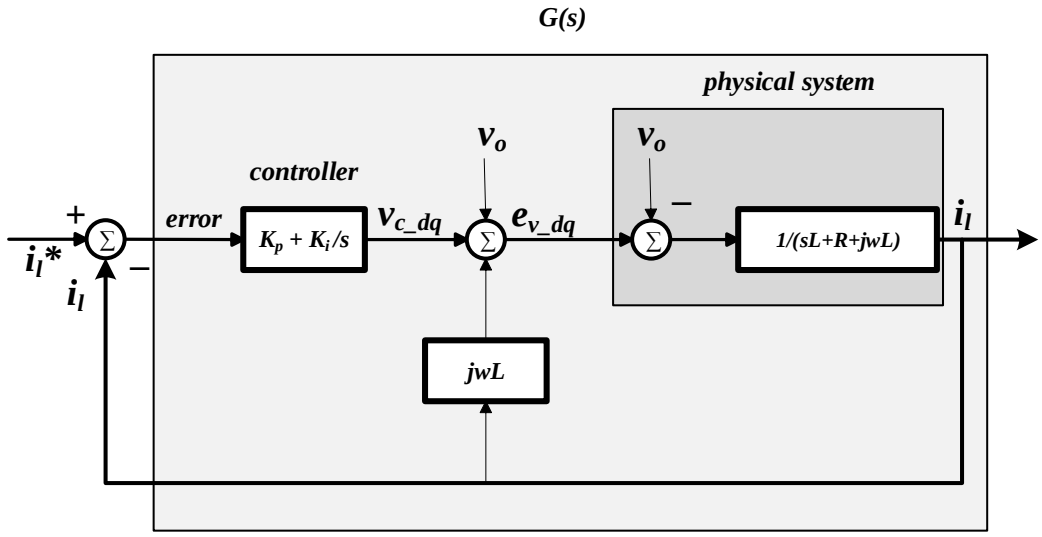


Figure 6.5 Feed forward of output dq current coupling term and output voltage of the converter

According to Equation (6.6), output of the MMC can be written as in Equation (6.19):

$$e_{v\_dq} = v_{o\_dq} + i_{l\_dq}\left(\left(\frac{R_{\text{arm}}}{2} + R_l\right) + \left(\frac{L_{\text{arm}}}{2} + L_l\right)s + j\omega\left(\frac{L_{\text{arm}}}{2} + L_l\right)\right) \tag{6.19}$$

Also, from Figure 6.4, output of the MMC can be written as in Equation (6.20):

$$e_{v\_dq} = v_{o\_dq} + v_{c\_dq} + j\omega\left(\frac{L_{\text{arm}}}{2} + L_l\right)i_{l\_dq} \tag{6.20}$$

Equating (6.19) and (6.20), Equation (6.21) is obtained as below:

$$v_{c\_dq} = \left(\left(\frac{R_{\text{arm}}}{2} + R_l\right) + \left(\frac{L_{\text{arm}}}{2} + L_l\right)s\right)i_{l\_dq} \tag{6.21}$$

Therefore, as long as the circuit parameters R_{arm}, R_l, L_{arm}, L_l and output voltage displacement angle θ_l are determined precisely, the PI controller can treat the MMC as a first order system.

6.3. Direct Modulation

As explained in section 6.1, apart from basic VSC control, there exist specific variables in MMC topology being controlled: submodule capacitor voltages and circulating current. For these MMC specific control aims, there are two fundamental approaches acknowledged in the literature. One is being proposed by Lesnicar and Marquardt [2] and it is referred hereafter as direct modulation [19]. In this method, for all the submodules in a phase leg, a single reference signal is used for modulation. It treats all the submodules in the phase leg for modulation simultaneously. As for the carrier signal, both LS and PS carriers may be used. Nonetheless, for this control approach, it is shown that PD method of LS gives the best result in terms of output harmonic distortion [18], [49]. Two separate control algorithms are implemented for submodule capacitor voltage balancing and circulating current control. The block diagram of the controllers is shown on Figure 6.6.

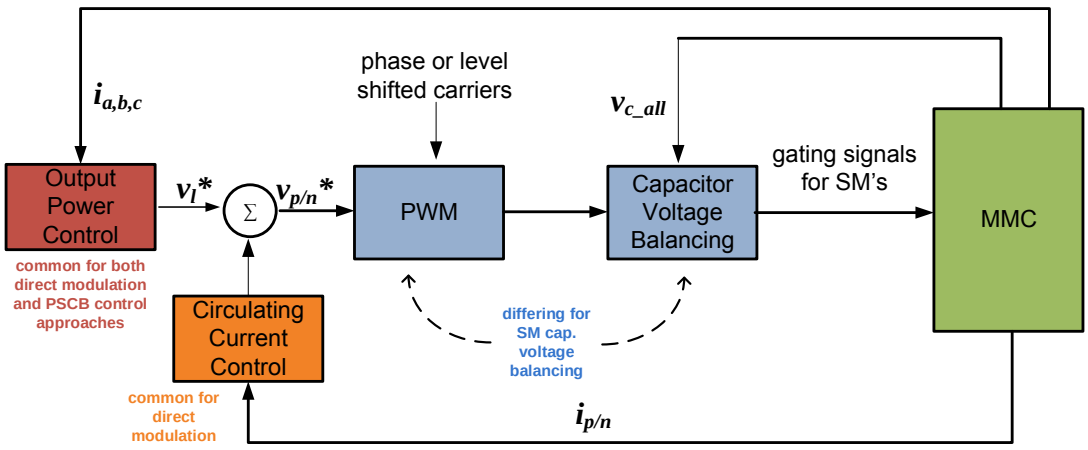


Figure 6.6 Block diagram of direct modulation method

6.3.1. Submodule Capacitor Voltage Balancing

As explained in chapter 2, submodule capacitors are charged and discharged during steady state operation of the converter. Indeed, this process of charge/discharge at the output current frequency is inevitable. Only its ripple magnitude may be decreased by increasing the capacitor value. Moreover, if the circulating current contains ac component, then the capacitor voltages are also charging/discharging at these circulating current frequencies. The charge/discharge amount of different capacitors in an arm should be kept equal to each other as much as possible. If this balance is not maintained, the output voltage and current distort, internal currents of the converter boost and damage the circuit equipments as well as the voltage ratings of submodule capacitors can be exceeded resulting in capacitor failures.

The charge/discharge states of submodule capacitors are given in Figure 2.9 and Table 2.5. The states basically depend on either the submodule is inserted or bypassed and if inserted, the direction of the submodule current. Briefly, if the submodule is bypassed, capacitor voltage does not change. If it is inserted to the current path and the current is positive, then the submodule capacitor is charged and else if the current is negative, then the submodule capacitor is discharged. Therefore, in order to maintain the voltage balance of submodules, these states should be used accordingly for each submodule during the operation of the converter.

6.3.1.1. Sort and Select (S&S) Method

Most commonly, direct modulation approach uses a "sort and select" method in order to maintain voltage balance of submodule capacitors [2]. This method, first of all, requires the measurement of capacitor voltages of all the submodules and polarity data of the arm current. Implementation of the method is explained in steps below:

1. The "required" number of submodules, N_{on}, to be inserted to the current path of the arm (upper and lower) should be determined. N_{on} is found out by the modulation waveforms, that is the reference and carrier signals. As explained in chapter 3, there are N carriers for N submodules in an arm. Reference and carrier signals are compared in amplitude, if the reference is greater than a carrier, one submodule for this carrier should be inserted to the current path, corresponding to increase of N_{on} by one; if not, one submodule should be bypassed, not changing the value of N_{on}. By this way, all the N carriers are compared with the reference and N_{on} is determined. The procedure is illustrated in Figure 6.7.

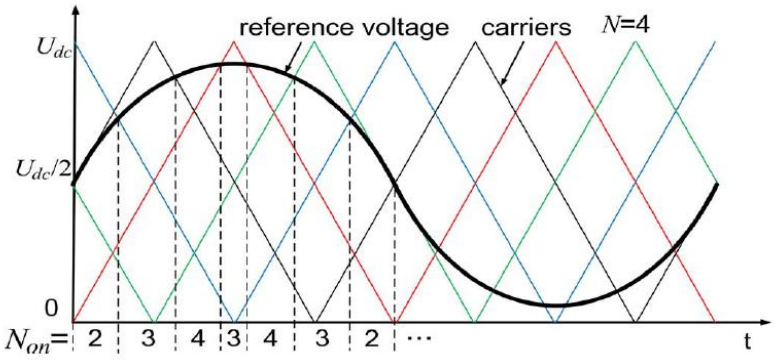


Figure 6.7 Determination of N_{on} [58]

2. All the capacitor voltages in an arm are measured and sorted from the highest to the lowest.
3. If N_{on} does not change from previous step time N_{on} value, inserted and bypassed submodules do not change in an arm. But as N_{on} changes, inserted number of submodules should be changed. The submodules to be inserted and bypassed are determined according to the following algorithm:
    a. If the arm current is positive (as in Figure 2.7), N_{on} submodules with lowest capacitor voltage are inserted (so as to charge them), and the rest (N - N_{on}) is bypassed (so as not to overcharge them).

b. Else if the arm current is negative, N_{on} submodules with highest capacitor voltage are inserted (so as to discharge them), and the rest ($N - N_{on}$) is bypassed (so as not to over discharge them). The procedure is illustrated in Figure 6.8.

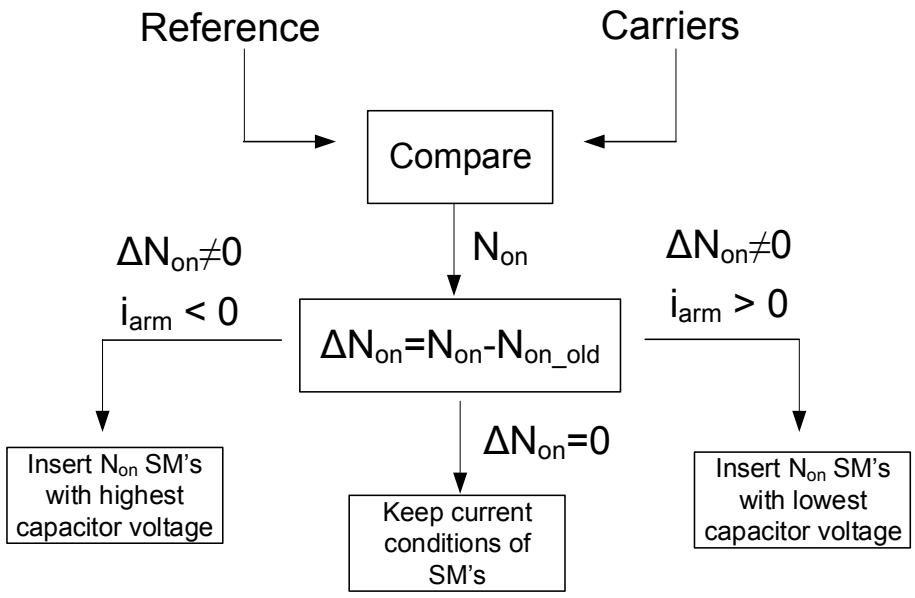


Figure 6.8 Determination of inserted submodules to the current path for sort and select method

By this way, all the submodule capacitors mean voltages converge to the average value of V_{dc}/N, with some ac ripple.

6.3.1.2. Sort and Select Method with Reduced Switching Count (S&S-RS) Method

A modified version of sort and select method for capacitor voltage balancing is sort and select method with reduced switching count [58]. It is basically the same as sort and select method; however, implementation of the method differs at the stage of determination of inserted or bypassed submodules. Step number 3 of sort and select

method is rearranged as below so as the method is tailored as sort and select method with reduced switching count:

1. Step 1 is the same as sort and select method.
2. Step 2 is the same as sort and select method.
3. As N_{on} changes, $\Delta N_{on} = N_{on} - N_{on\_old}$ is determined; where, N_{on_old} is the value of N_{on} at the previous step time. The submodules to be inserted and bypassed are determined according to the following algorithm:
    a. If ΔN_{on} is zero, inserted and bypassed submodules do not change in the arm.
    b. If ΔN_{on} is positive, additional submodules to the existing ones should be inserted to the current path. Selection of these additional submodules is executed again considering the arm current polarity and capacitor voltage levels of submodules as in sort and select method. However, the selection is made among only the currently bypassed submodules, while sort and select method makes the selection among the whole submodules, both inserted and bypassed.
    c. If ΔN_{on} is negative, some submodules should be bypassed from the current path. Selection of these excess submodules is executed again considering the arm current polarity and capacitor voltage levels of submodules as in sort and select method. However, the selection is made among only the currently inserted submodules to the current path, while sort and select method makes the selection among the whole submodules in the arm, both inserted and bypassed. Figure 6.9 illustrates the procedure.

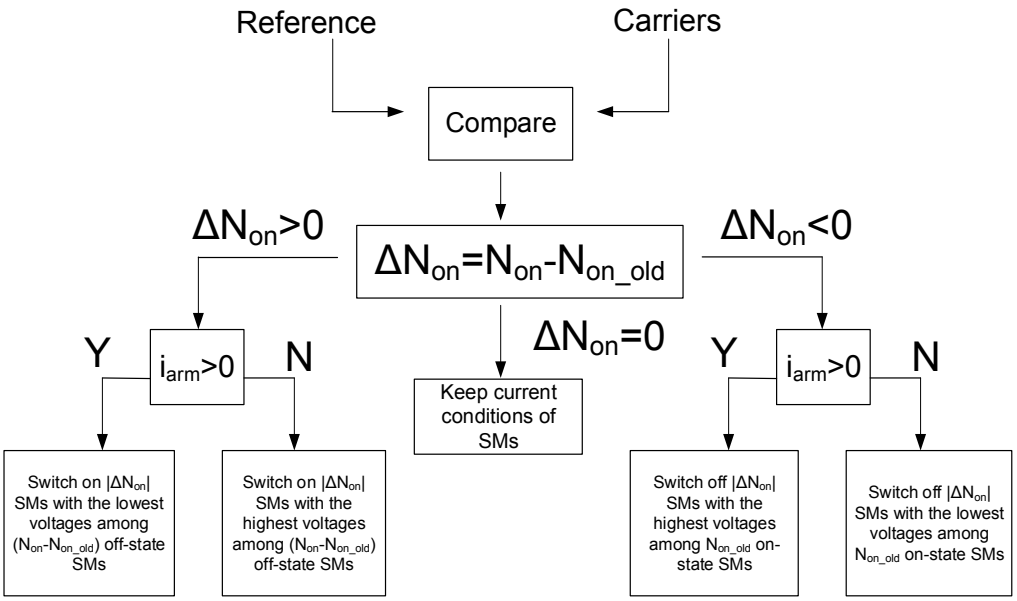


Figure 6.9 Determination of inserted or bypassed submodules for sort and select method with reduced number of switching

By this way, total switching count of submodules can be reduced significantly in return for some increase in the submodule capacitor voltage ripple due to restricted dynamic control of capacitor voltage balancing.

6.3.1.3. Voltage Balancing with Carrier Rotation

For submodule capacitor voltage balancing, there exists another method to be used with direct modulation control approach, without the need for submodule capacitor voltage measurement and arm current polarity data [56]. This method is especially evolved for LS PWM. It is based on assigning each carrier signal to a submodule and switching the submodule with the common reference signal and assigned carrier signal. However, if each carrier signal is permanently assigned to one submodule, then insert/bypass durations of these submodules will diverge from each other, because of the reasons as explained in section 4.4.2. In this condition, charge/discharge rates of capacitors will also diverge from each other, resulting in an unbalance between capacitor voltages. In order to equate these insert/bypass times of

different submodules, each carrier signal should be assigned for each submodule on the arm for a period of time, and the assignment of carriers should be changed periodically. By this way, insert/bypass durations of submodules are equated to each other so as the charge/discharge amounts. Therefore, a balance of submodule capacitors voltage could be achieved. The rotation period of carriers is equal to fundamental period of output voltage. At each fundamental period, carrier is assigned to the next submodule, until the N^{th} submodule. Then, the carrier is assigned to the very first submodule and the process continues. It is important to note that, as N increases, the balancing capability of the method degrades, due to the increase in rotation period. In Figure 6.10, rotated carriers for N=4 is illustrated. In the figure, each submodule is colored differently, and switching of these is done by the same colored carrier parts. As seen, each carrier part with different colors is placed in different modulation regions, providing the insert/bypass time durations of the submodules to be equal.

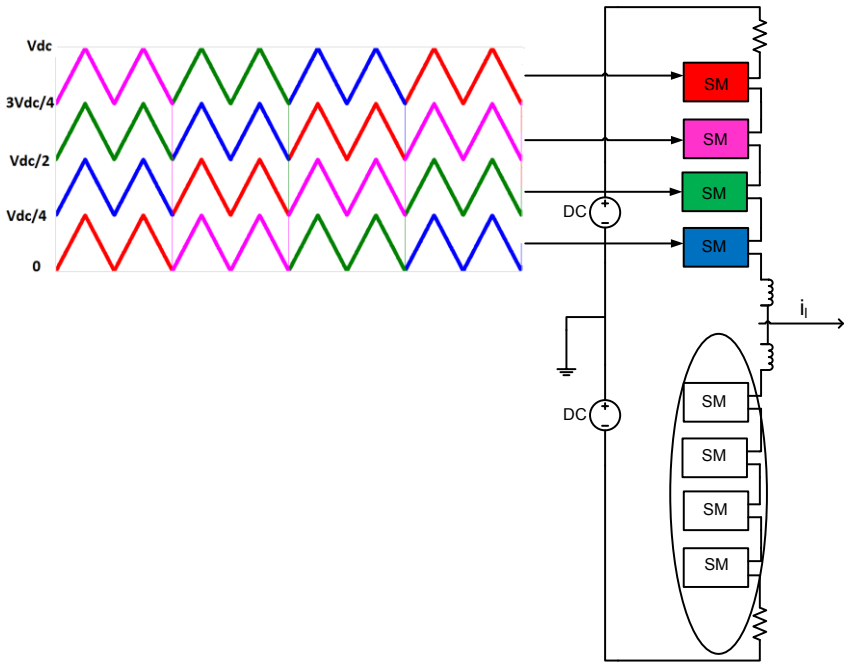


Figure 6.10 Carrier rotation method for submodule capacitor voltage balancing

6.3.2. Circulating Current Control

Circulating current is one of the characteristics of the MMC. As defined in Equation (3.10), it consists of a dc component responsible for power transfer to the output and an ac component. Ac component of circulating current causes extra conduction loss and requires the circuit elements to be rated higher. Therefore, it is convenient to mitigate this ac component unless it is intentionally generated for specific purposes such as in case of low frequency operation of the converter, which is detailed in chapter 8. The ac component of circulating current emanates from variations in the total submodule capacitor voltages between the upper and lower arms of a phase leg and between different phase legs. Although the voltage variations between upper and lower arms could be minimized by suitable voltage balancing mechanisms as explained above; voltage imbalance between different legs is inevitable since in a three-phase system there should be a phase difference between different phases. Therefore, submodule capacitors voltages of different phase legs fluctuate out of phase, causing circulating currents. Indeed, in [57] it is shown that the sum of capacitor voltages in an arm contains an ac component consisting of a dominant fundamental frequency component and a second harmonic component, apart from the nominal dc voltage, V_{dc}. For the other arm, fundamental component is π radians out of phase because of the modulation scheme and the second harmonic is in phase with the former arm voltage sum. As a result, the sum of all capacitor voltages in the phase leg contains a dominant second harmonic and the fundamental component is eliminated. Thus, a second harmonic voltage ripple is added to the phase leg voltage sum, resulting in second harmonic circulating current. This circulating current is proportional with output current and inversely proportional with submodule capacitor value [55]. Equation (3.16) related with circulating current is rearranged here as in Equation (6.22):

$$2L_{arm}\frac{di_{circ}}{dt} + 2R_{arm}i_{circ} = V_{dc} - (v_p + v_n) \tag{6.22}$$

Equation (6.18) models the circulating current flowing between a phase leg and the dc-link. Moreover, a similar voltage loop equation could be written for the circulating current flowing between different phase legs as in Equation (6.23):

$$4L_{arm}\frac{di_{circ}}{dt} + 4R_{arm}i_{circ} = (v_p + v_n)_a - (v_p + v_n)_b \tag{6.23}$$

where, $(v_p + v_n)_a$ stands for phase a leg voltage and $(v_p + v_n)_b$stands for phase b leg voltage. Figure 6.11 illustrates the circulating current equivalent circuit of MMC.

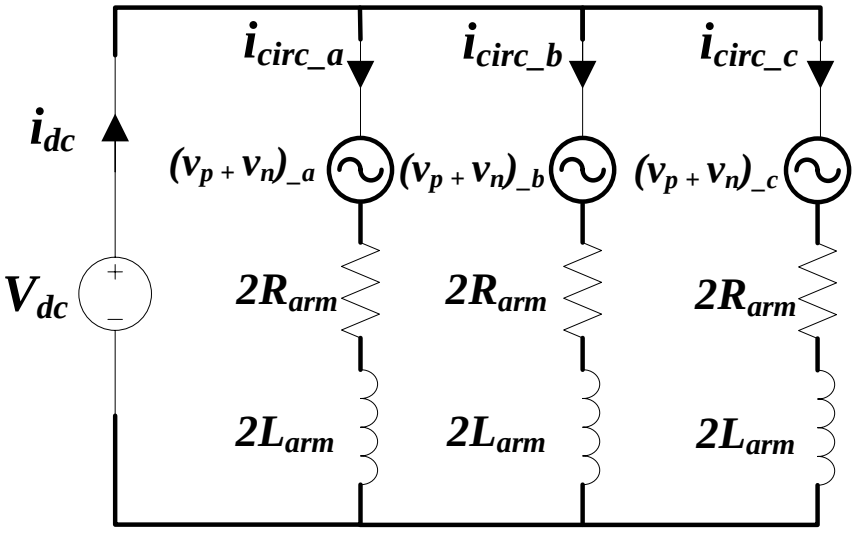


Figure 6.11 Circulating current equivalent circuit of MMC

According to Equations (6.22) and (6.23)(6.19) circulating current is limited by the leg impedance, mainly the arm inductor. However, an active control strategy could be implemented without affecting the output voltage, by increasing both the upper and lower arm voltages, so that right sides of the Equations (6.22) and (6.23) are zero. The control algorithm basically tries to keep the voltage balance between dc-link and phase legs or between different phase legs by inserting or bypassing extra submodules both from upper and lower arm so as not to distort the output voltage.

Supposing, at a given time, the sum of capacitor voltages in phase a has higher average value than the ones in phases b and c. The difference between the phases can be reduced by inserting more than N submodules in phase legs of b and c, where the submodule voltages are lower. Therefore, at specific instant, phase leg a may have N-2 submodules inserted to the current path and phases b and c may have N+1 submodules, resulting in a balance between phase leg voltages. This technique allows for regulation of the amplitude of the total inserted submodules capacitor voltage, reducing the temporary imbalances between the phases and consequently eliminating the circulating current ac components.

The dominant ac component is second harmonic, thus it is appropriate to suppress this component from circulating current. In order to implement the abovementioned technique, vector control approach could be exploited as in the case of output power control [58]. Circulating current second harmonic component is transformed from abc stationary reference frame to rotating dq reference frame. It is important to note that, the dominant ac component, second harmonic is in the form of negative sequence and during abc/dq transformation this condition should be taken into account. Then PI controllers are used to track the reference second harmonic components (which are essentially set to zero). PI parameters could be determined with the same algorithm explained in section 6.2 and using the circulating current equivalent circuit in Figure 6.11. Bandwidth of the controller is the same as in Equation (6.16). K_p and K_i parameters are given for the sake of convenience in Equations (6.24) and (6.25) below:

$$K_3 = a_c(2L_{\text{arm}}) = \frac{2\pi * f_{c\_eq} * L_{\text{arm}}}{5} \tag{6.24}$$

$$K_4 = a_c(2R_{\text{arm}}) = \frac{2\pi * f_{c\_eq} * \text{R}_{\text{arm}}}{5} \tag{6.25}$$

The outputs of PI controllers are the reference circulating current suppression voltages in dq frame. They are summed up with the cross coupling compensation terms and the final reference voltages are back transformed to the abc reference

frame. Block diagram of the controller is given in Figure 6.12. Back transformed voltage components are used in the modulation block as explained in the next section.

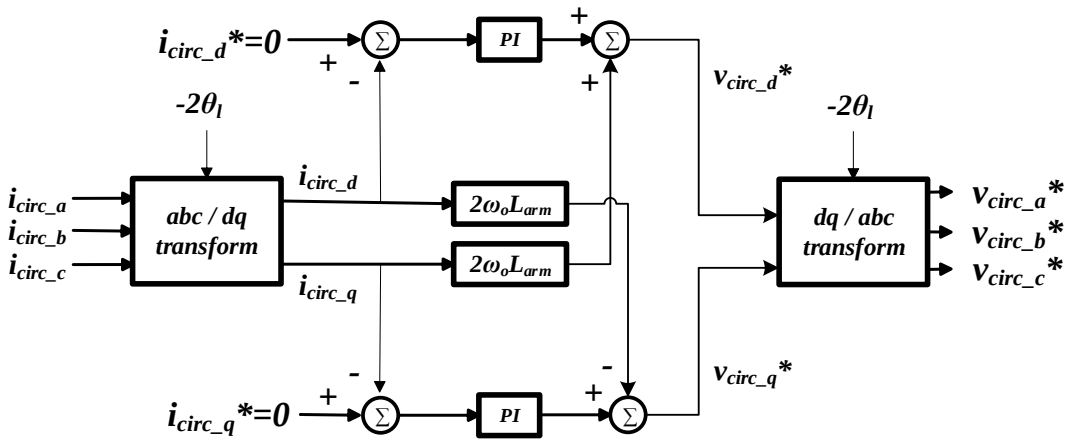


Figure 6.12 Circulating current second harmonic controller block diagram

6.3.3. Reference Signal Generation and Modulation

The reference signal which should be the input of the modulation block is generated by summing up the resulting signals of output power control as in Figure 6.1, circulating current control as in Figure 6.12 and half of the dc-link voltage. Reference signals of upper and lower arms of a phase are given in Equations (6.26) and (6.27).

$$v_{p\_u}^* = \frac{V_{dc}}{2} - v_{l\_u}^* - v_{circ\_u}^* \tag{6.26}$$

$$v_{n\_u}^* = \frac{V_{dc}}{2} + v_{l\_u}^* - v_{circ\_u}^* \tag{6.27}$$

As given in Equations (6.26) and (6.27), output control signal is summed for lower arm and subtracted for upper arm. Circulating current control component is subtracted for both upper and lower arms. Unless carrier rotation technique is used

for submodule capacitor voltage balancing, reference signal is then compared with the carriers in order to determine N_{on}. This value is fed to submodule capacitor voltage balancing algorithm as explained in sections 6.3.1.1 and 6.3.1.2. The outputs of this algorithm are the gate signals going to the semiconductors of the submodules. Block diagram for generation of reference signals and the remaining process for obtaining gate signals of submodules are illustrated in Figure 6.13.

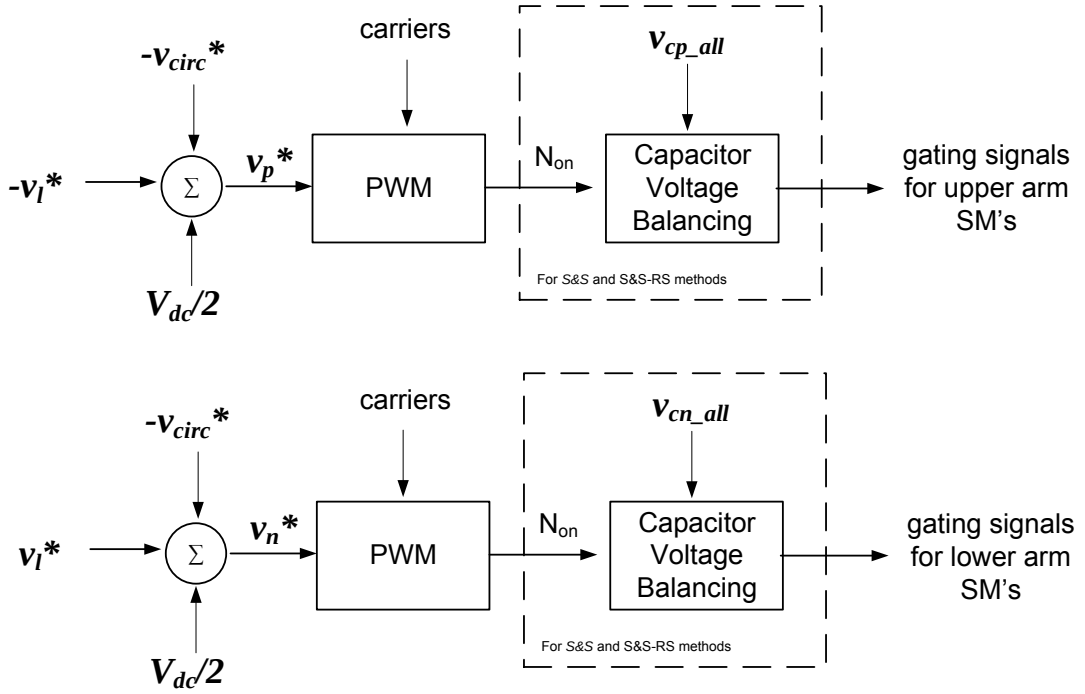


Figure 6.13 Block diagram for generation of reference signals and the remaining process for obtaining gate signals of submodules

6.4. Phase-shifted Carrier Based Control

The second control approach for MMC submodule capacitor voltage balance and circulating current is proposed by Hagiwara and Akagi in [22]. It is phase-shifted carrier based control and referred hereafter as PSCB control. Different from direct modulation, separate reference signals are generated for each submodule in a phase leg. Switching is treated individually for each submodule, rather than the whole

phase arm as in the case of direct modulation. In this method, only PS carriers are proposed for PWM block. The block diagram of this control approach is shown in Figure 6.14.

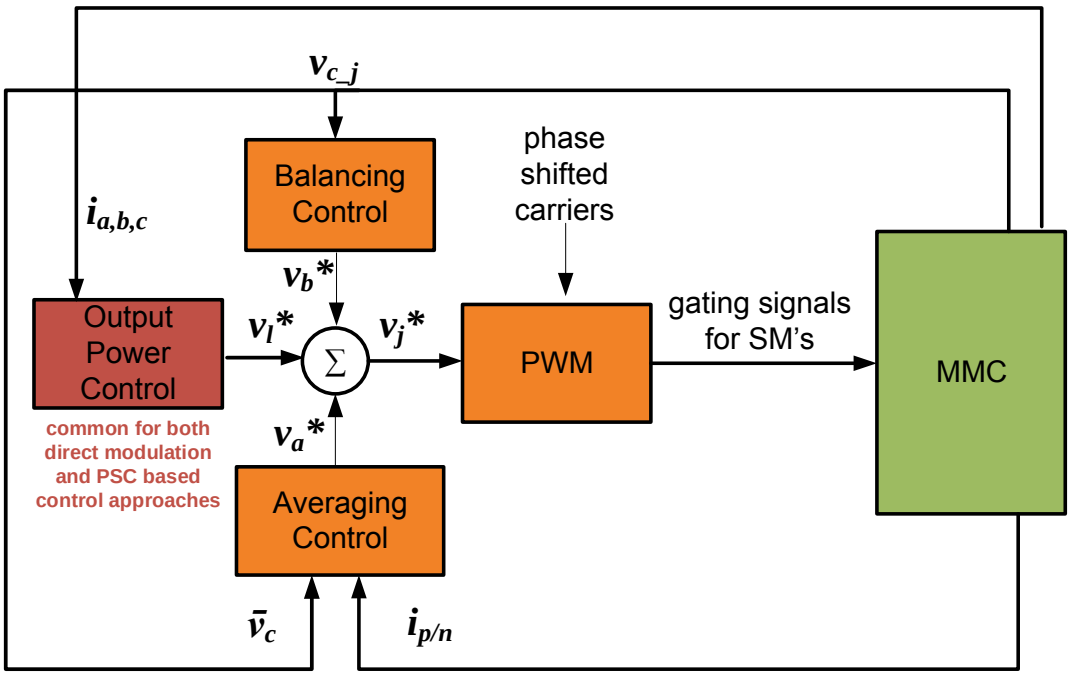


Figure 6.14 Block diagram of phase-shifted carrier based control

Submodule capacitor voltage balancing and circulating current control are integrated in phase-shifted carrier based control approach. For these aims, "averaging control" and "balancing control" methods are implemented. The averaging control ensures that the voltage of each submodule capacitor in a leg is close to the reference capacitor voltage. Actual average capacitor voltage of a leg is calculated by summing up all the capacitor voltages and dividing it by the number of submodules in the leg, 2N. Error between the reference voltage value and actual average voltage value is found. Then, the error is fed into a PI controller, in order to generate a reference for the circulating current controller. The actual circulating current is calculated as in Equation (3.10) and again the error between the reference and the actual circulating currents is calculated. This current error is fed into another PI

controller, giving the average controller output as reference averaging voltage component. It is important to note that, averaging controller is separate for each phase leg of the MMC. The block diagram of average controller is shown in Figure 6.15 below.

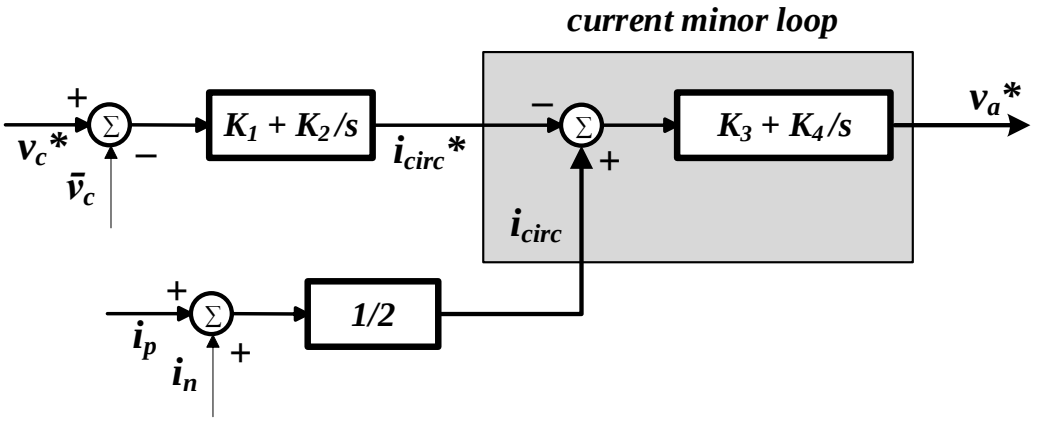


Figure 6.15 Averaging control of PSCB control

The current minor loop is similar to the circulating current control in direct modulation control approach. Equivalent circuit model seen by the current minor loop is again as in Figure 6.11. Therefore, K_p and K_i parameters for the PI controller of the current minor loop can be calculated as in Equations (6.21) and (6.22).

The outer control loop in Figure 6.15 is the voltage control loop and should have a slower bandwidth than the current minor loop. Considering the current minor loop as an ideal controller, the open loop transfer function of the outer voltage control loop is given in Equation (6.28) below [50]:

$$G_{out\_op}(s) = \left(K_1 + \frac{K_2}{s}\right)\frac{1}{sC_{arm}} \tag{6.28}$$

The bandwidth of the voltage control loop is roughly estimated by equating K_2 to zero as in Equation (6.29):

$$BW_{out} \approx \frac{K_1}{C_{arm}} \tag{6.29}$$

Then, K_1 is found as in Equation (6.30):

$$K_1 \approx BW_{out} C_{arm} \tag{6.30}$$

The close loop transfer function of voltage control loop could be formed as in Equation (6.31):

$$G_{out\_clsd}(s) = \frac{\frac{1}{C_{arm}}(sK_1 + K_2)}{s^2 + s\frac{K_1}{C_{arm}} + \frac{K_2}{C_{arm}}} \tag{6.31}$$

Then, K_2 could be estimated as in Equation (6.32):

$$K_2 = \frac{K_1^2}{4\xi^2 C_{arm}} \tag{6.32}$$

where, ξ is the damping ratio and is generally chosen to be one, in order not to have overshoot.

The second controller is individual "balancing control". It is responsible for setting each submodule capacitor voltage to its reference value. The balancing controller is separate for each submodule in MMC. The error between the actual submodule capacitor voltage and the reference voltage is found and this is fed into a proportional (P) controller. The output is negated if the arm current is negative. The block diagram of balancing controller is shown in Figure 6.16 below.

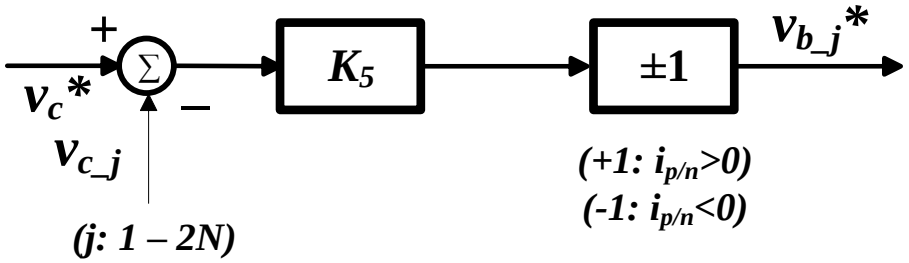


Figure 6.16 Balancing control of PSCB control

As explained in the very first paragraph of the section, separate reference signals are generated for each submodule of the converter, since the balancing controller is separate for each submodule. Equations (6.33) and (6.34) give the reference signals for upper and lower arm submodules of a phase, respectively.

$$v_{j\_u}^{*} = v_{a\_u} + v_{b\_j} - \frac{v_{l\_u}^{*}}{N} + \frac{V_{dc}}{2N} \qquad (j: 1 - N) \tag{6.33}$$

$$v_{j\_u}^{*} = v_{a\_u} + v_{b\_j} + \frac{v_{l\_u}^{*}}{N} + \frac{V_{dc}}{2N} \qquad (j: N - 2N) \tag{6.34}$$

where, v_{a_u} is the output of the averaging controller for u-phase, v_{b_j} is the output of the balancing controller for submodule-j and $v_{l\_u}^{*}$ is the output of the output power control block for u-phase. Figure 6.17 shows the reference signal generation for upper and lower arm submodules separately.

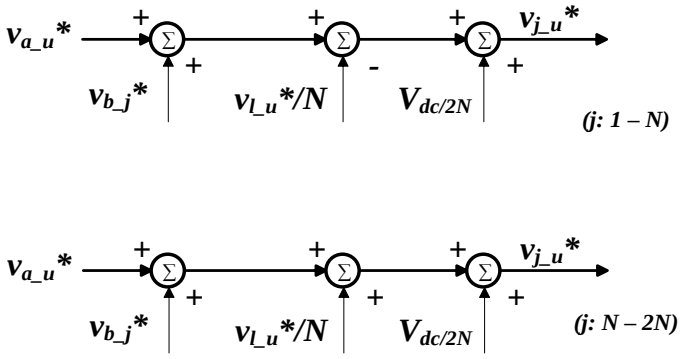


Figure 6.17 Reference signal generation for upper and lower arm submodules

The reference voltage signal $v_{j\_u}^{*}$ is normalized by corresponding submodule capacitor voltage, v_{Cj_u}, and this normalized reference signal is compared with phase-shifted carrier signal having a maximal value of unity and a minimal value of zero. By this way, gating signals for each submodule are generated separately.

6.5. Other Control Approaches: Closed-loop Control and Open-loop Control

In the literature, two more control approaches are proposed for MMC: closed-loop control [20] and open-loop control [59]. Closed-loop control is principally based on direct modulation approach. Different from direct modulation, the total stored energy in the leg and the energy balance between each arm is controlled by two voltage contribution terms v_{reg}^{Σ} and v_{reg}^{diff}, which are subtracted from the output voltage reference. Total leg energy and arm energy are calculated by measuring the voltage of each submodule capacitor. Modulation of submodules is again sort and select based. Reference modulation signals of closed-loop control method are shown in Equations (6.35) and (6.36).

$$v_{p\_u}^{*} = \frac{V_{dc}}{2} - v_{l\_u}^{*} - v_{reg}^{\Sigma} - v_{reg}^{diff} \tag{6.35}$$

$$v_{n\_u}^{*} = \frac{V_{dc}}{2} + v_{l\_u}^{*} - v_{reg}^{\Sigma} - v_{reg}^{diff} \tag{6.36}$$

Open-loop control is a modification of closed-loop control. While in closed-loop control all submodule capacitor voltages are measured for arm and leg energy calculations, in open-loop control, leg and arm energy are estimated from output current and dc-link voltage measurements. The reason behind that is the complication of measurement, communication and huge data to be processed for MMC's with high number of submodules per arm. By using these estimated values, an energy balancing contribution, v_{diff}, is generated to be subtracted from the output voltage reference, v_{l}^{*}. Reference signals of open-loop control method are shown in Equations (6.37) and (6.38).

$$v_{p\_u}^{*} = \frac{V_{dc}}{2} - v_{l\_u}^{*} - v_{diff} \tag{6.37}$$

$$v_{n\_u}^{*} = \frac{V_{dc}}{2} + v_{l\_u}^{*} - v_{diff} \tag{6.38}$$

CHAPTER 7

SIMULATION STUDY AND CONTROL METHODS PERFORMANCE COMPARISON

7.1. Introduction

Carrier based PWM methods characterization, MMC components rating determination and control methods of the converter are analyzed in previous chapters. As seen, switching and control of MMC may be ramified and get complicated because of the combination of different carrier based PWM methods, cases of N+1 or 2N+1 output voltage levels and different control approaches. Therefore an important design issue arises, which control method among plenty of combinations should be implemented on the MMC. For sure, the correct answer may depend on the specific conditions of the system to be worked on. Nonetheless, in this chapter, a set of simulations are carried out by Ansoft Simplorer® 7.0 [33] computer simulation program, to investigate the characteristics and performances of different control methods. In this way, advantages and disadvantages of different methods are discovered and in terms of specific criteria, such as output harmonics distortion, submodule capacitor voltage ripple magnitude, circulating current ac component magnitude or efficiency, the best method is proposed.

In all the simulations, *equal total count of semiconductor switching per leg* principle is respected as its importance being explained in chapter 4. Consequently, switching losses of the converter for different simulations are made close to each other, with similar switched amounts of current. Conduction losses, on the other hand, depend on the arm currents. As explained in Equations (3.8) and (3.9), arm currents are the

sum of half of the output current and circulating current which is comprised in ac and dc components. For the same amount of output power; output current and circulating current dc component are approximately the same for different simulation sets. Therefore, ac component of circulating current is the major component which differentiates the conduction losses of different simulation sets. Loss and efficiency calculations of the simulations are detailed in Appendix B.

7.2. Simulated System

Dc/ac conversion step of an HVDC system is considered for the simulated system. Circuit structure of the simulated system in Simplorer is shown in Figure 7.1. The first and the second submodules from the top of the upper arm of phase a are circled in blue and red, whose switching pulse patterns, as in chapter 4, are given in the following simulation results sections. Dc-link is assumed to be 14.4kV and ac side line-to-line (grid) voltage of the system is assumed to be 8.66kV_{rms} at 50Hz. Rated power of the converter is 10MVA with 667A_{rms} output current. Base impedance of the system is calculated in Equation (7.1) below:

$$Z_{base} = \frac{V_{base}^2}{S_{base}} = \frac{(8.66 * 10^3)^2}{10 * 10^6} = 7.5\Omega \quad (7.1)$$

Ac side grid inductance is assumed to be 0.05pu, corresponding to 1.2mH and grid resistance is assumed to be 0.003 pu, corresponding to 25mΩ. Also, arm resistance of the converter is assumed to be 50mΩ (0.007pu). The rest of the converter parameters are determined in the next sections in the light of information given in chapter 5.

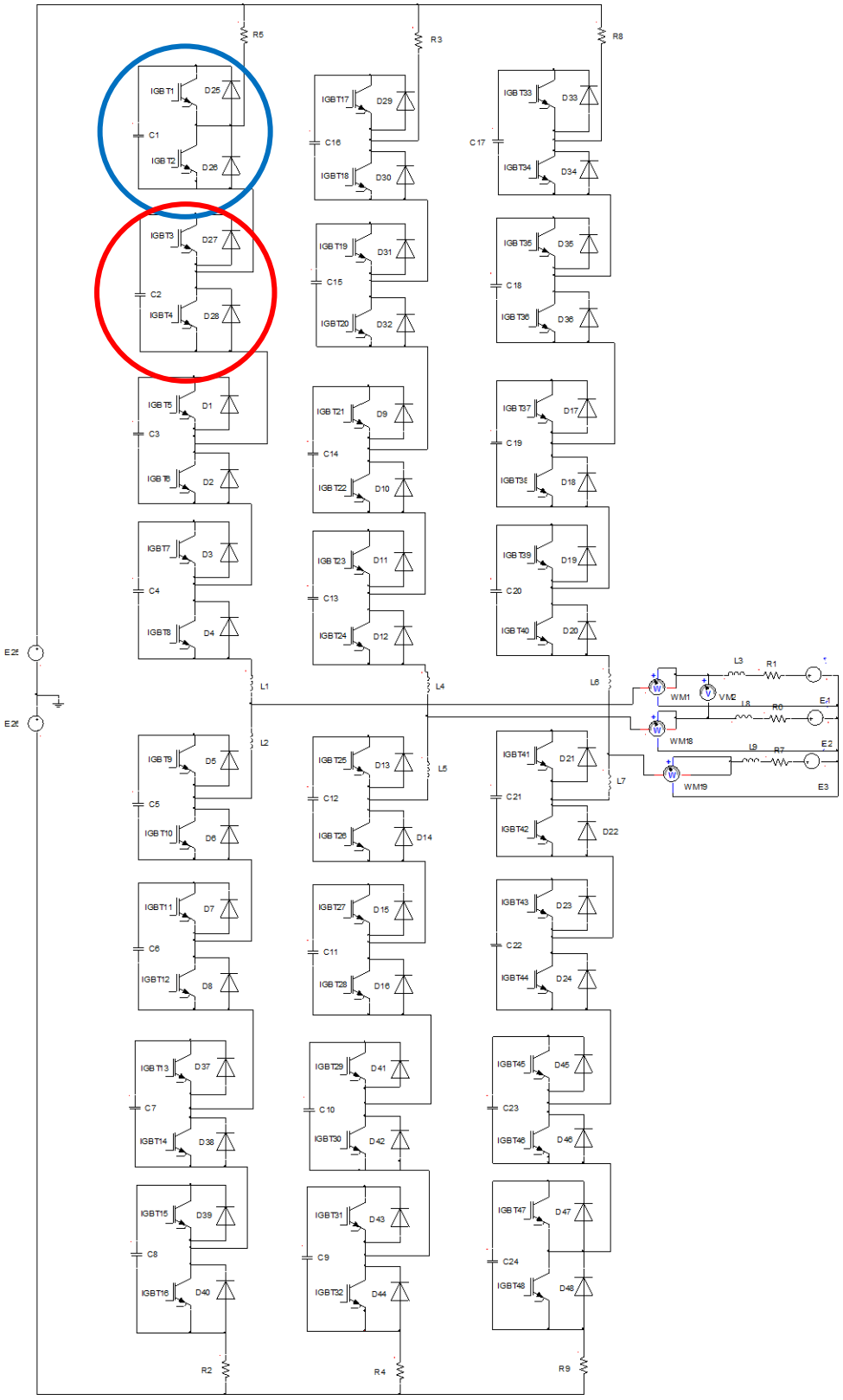


Figure 7.1 Circuit structure of the simulated dc/ac conversion step of an HVDC system in Simplorer

7.2.1. Number of Submodules per Arm

Number of submodules per arm, N, is fixed as four keeping into account the available semiconductors in the market, implementation effort for the simulation and reasonable harmonic content with this number. As expressed in Equation (2.1), natural balance voltage of submodule capacitors with N=4 is given in Equation (7.2) below:

$$V_c = \frac{V_{dc}}{N} = \frac{14400}{4} = 3600V \tag{7.2}$$

Ideal arm current magnitude, which is calculated as in Equation (7.3), is half of the output current and circulating current dc component, which is ideally one third of the dc source current.

$$\begin{aligned} i_{p/n} = i_{circ,dc} \pm \frac{i_l}{2} = \frac{S}{3 * V_{dc}} \pm \frac{i_l}{2} = \frac{10 * 10^6}{3 * 14400} A_{dc} \pm \frac{667}{2} A_{rms} \\ = 231.48 A_{dc} \pm 333.5 A_{rms} \end{aligned} \tag{7.3}$$

Then, ideal peak arm current is calculated in Equation (7.4):

$$i_{p/n,peak} = 231.48 + 333.5\sqrt{2} = 703.12A \tag{7.4}$$

As seen in Figure 2.12, three manufacturers have 1.5kA/6500V IGBT modules. These modules can be used as the switching devices of the submodules.

7.2.2. Submodule Capacitor Value

Submodule capacitor value is fixed as 3mF for the simulated system, which gives approximately 10% peak-to-peak voltage ripple for the submodules as will be seen

in the simulation results section. The energy-power ratio in this case is calculated as in Equation (7.5):

$$EP = \frac{3V_{dc}^2 * C}{N * S_n} = \frac{3 * 14400^2 * 3 * 10^{-3}}{4 * 10 * 10^3} = 46.6\, J/kVA \tag{7.5}$$

7.2.3. Arm Inductor Value

Equation (5.5) gives the arm inductor value for passively damping the circulating current second harmonic component. However, this method leads to big values of arm inductors, which is not desirable in terms of cost and size of the converter. For example, in our case, with 10% circulating ac current second harmonic content with respect to dc component, the required inductor value is calculated as in Equation (7.6). Ideal dc component of circulating current is 231.48A as calculated in Equation (7.3).

$$L_{arm} = \frac{N}{8V_{dc}\omega_0^2 C}\left(\frac{P_A}{3I_{2f}} + V_{dc}\right) \tag{7.6}$$

$$= \frac{4}{8 * 14400 * (2\pi * 50)^2 * 3 * 10^{-3}}\left(\frac{10 * 10^6}{3 * 0.1 * 231.48} + 14400\right)$$

$$= 18.5 * 10^{-3}$$

This amount of arm inductor is approximately 0.775pu for our case, which out of the range of applicable limits 0.15-0.20pu. Therefore, as proposed in chapter 6, active circulating current second harmonic suppression methods are implemented in the simulations which resulted in much less arm inductor values. The limit for the arm inductor value is calculated in the light of Equation (5.7) as in Equation (7.7) below:

$$L_{arm}C > \frac{5N}{24\omega_0^2} \Rightarrow L_{arm} > \frac{5N}{24\omega_0^2 C} = \frac{5 * 4}{24 * (2\pi * 50)^2 * 3 * 10^{-3}} \tag{7.7}$$

$$= 2.81 * 10^{-3}$$

Then, arm inductor value is fixed as 4.7mH, which corresponds to 0.2pu approximately.

The whole circuit parameters are listed in Table 7.1 below.

Table 7.1 MMC simulation circuit parameters

Symbol	Meaning	Value	Comments
V_{dc}	Dc-link voltage	14.4kV	
V_l	Ac side line-to-line voltage	8.66kV_{rms}	
f_l	Fundamental frequency	50Hz	
N	Number of submodules per arm	4	
L_l	Grid side inductance	1.2mH	0.05pu
R_l	Grid side resistance	25mΩ	0.003pu
L_{arm}	Arm inductance	4.7mH	0.2pu
R_{arm}	Arm resistance	50mΩ	0.007pu
C	Sub module capacitance	3mF	46.6 J/kVA

7.2.4. Simulation Sets and Limitations

The two fundamental control approaches, *direct modulation* and *phase-shifted carrier based control* as explained in sections 6.3 and 6.4 are considered in the simulations. Carrier sets with N+1 and 2N+1 phase-to-neutral output voltages are analyzed separately. In direct modulation case, for the submodule capacitor voltage balancing mechanism, all the methods mentioned in section 6.3 are considered, i.e. *sort and select method*, *sort and select method with reduced count of switching* and *carrier rotation method*. Consequently, all the simulation combinations are listed in Table 7.2.

In section 4.4 it is shown that for N+1 level output voltage, PD method of LS PWM methods has the lowest output harmonics content among all carrier based PWM methods. For 2N+1 level output voltage, on the other hand, all the LS and PS PWM methods have the same harmonics distortion performance. Therefore, for direct modulation control approach, PD method is used as carriers. For phase-shifted carrier based control approach, PS PWM method is used, as the name of the control

approach refers. As for reference output signal, sinusoidal PWM method is used for all the simulation sets.

Table 7.2 Simulation sets

	N+1 phase-to-neutral voltage levels				**2N+1 phase-to-neutral voltage levels**			
	Direct modulation				Direct modulation			
Control method	Sort and select (S&S)	Sort and select with reduced count of switching (S&S-RS)	Carrier rotation (CR)	Phase-shifted carrier based control (PSCB)	Sort and select (S&S)	Sort and select with reduced count of switching (S&S-RS)	Carrier rotation (CR)	Phase-shifted carrier based control (PSCB)
Scalar PWM method	Level-shift, phase disposition (LS-PD, Figure 4.2)			Phase-shift (PS, Figure 4.5)	Level-shift, phase disposition (LS-PD, Figure 4.2)			Phase-shift (PS, Figure 4.5)

Frequency of the carriers are set as 1800Hz for PD PWM, corresponding to individual switching frequency of the submodules as $f_c/N=1800/4=450Hz$, approximately. Accordingly, carrier frequency of PS method should be $f_{c\_PD}/N= 1800/4=450Hz$, in order to equate the total count of switching per leg, as explained in section 4.4.1. However, this principle of "equal count of switching per leg" is valid for ideal waveforms of carrier based PWM methods as in chapter 4; in other words, without any control method being implemented. In case there are control loops in the system, it is seen that the total count of switching per leg may differentiate from the target value. For example, S&S and S&S-RS methods lead to different total count of switching per leg, as expected. This condition of unbalanced switching count may lead to unfair comparisons of different methods. Therefore, total count of switching per leg for all the methods are converged to 450Hz±5% by tuning the carrier frequency of the related simulation set, if required. Moreover, it is shown in [65] that, for the PS method, the carrier frequencies which are integer multiples of fundamental frequency should be avoided as they can cause the submodule capacitor voltages to diverge. Hence, the PS method carrier frequencies

are adjusted to non-integer multiples of fundamental frequency, as details are given in simulation results.

In the next sections, K_p and K_i values of output power control and circulating current second harmonic suppression control loops are given and simulation results of different output power conditions are illustrated by switching pulse patterns, voltage and current waveforms with their harmonics spectrums and numerical data. In the harmonics spectrum graphics, only the harmonics that are greater than one per cent of the fundamental component are shown.

7.3. Simulation Results

7.3.1. Rated Power (10MVA) with Unity Load Angle (cos(φ)=1)

7.3.1.1. Case 1: N+1 Output Voltage Levels

i. Direct Modulation, Sort and Select Method

In this simulation case, carrier frequency is tuned as 1350Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.3 K_p and K_i values of S&S method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=6	K_i=84.8	K_p=15.9	K_i=170

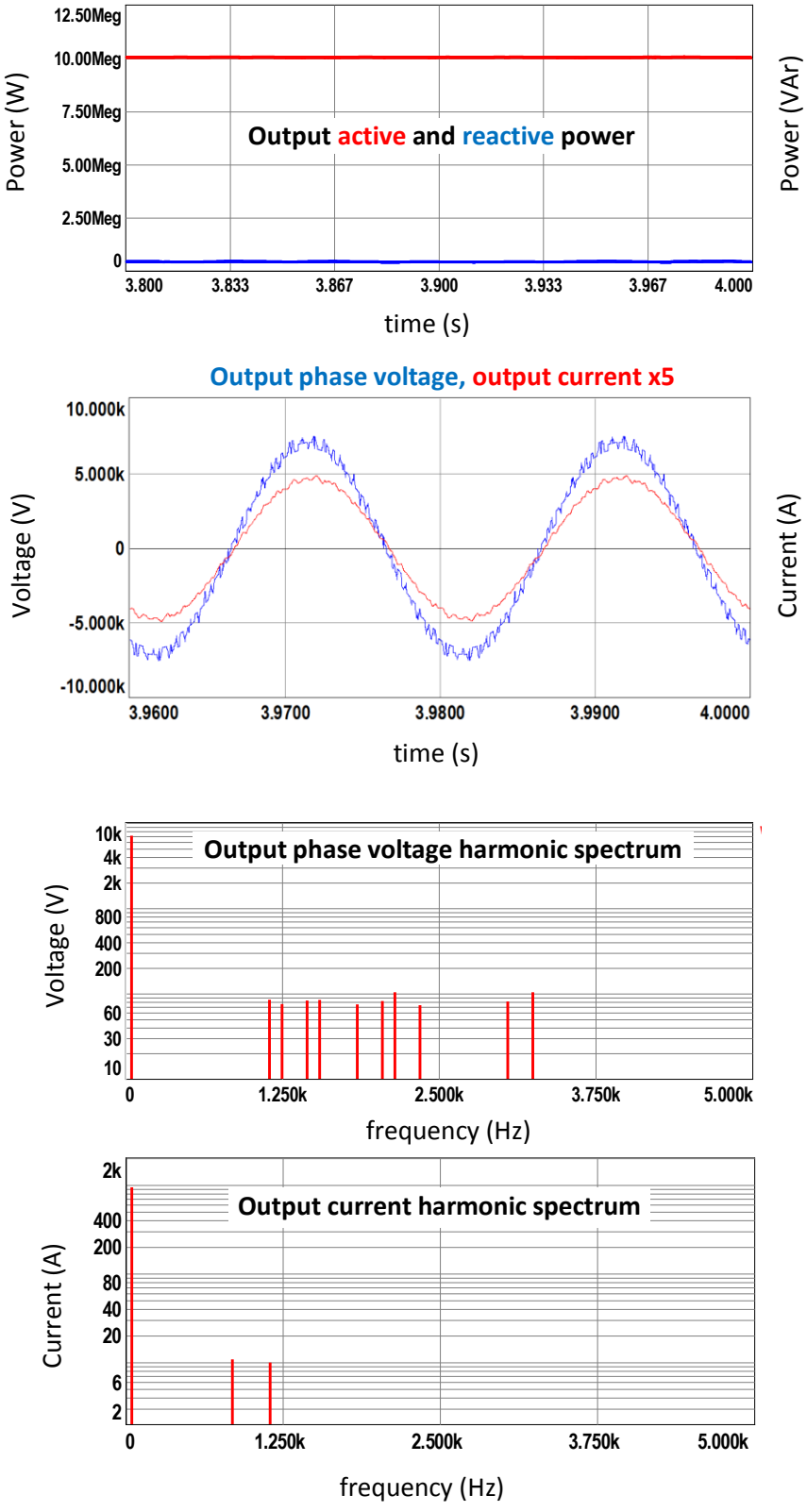


Figure 7.2 Simulation results for S&S method with N+1 level V_{ph}, full load

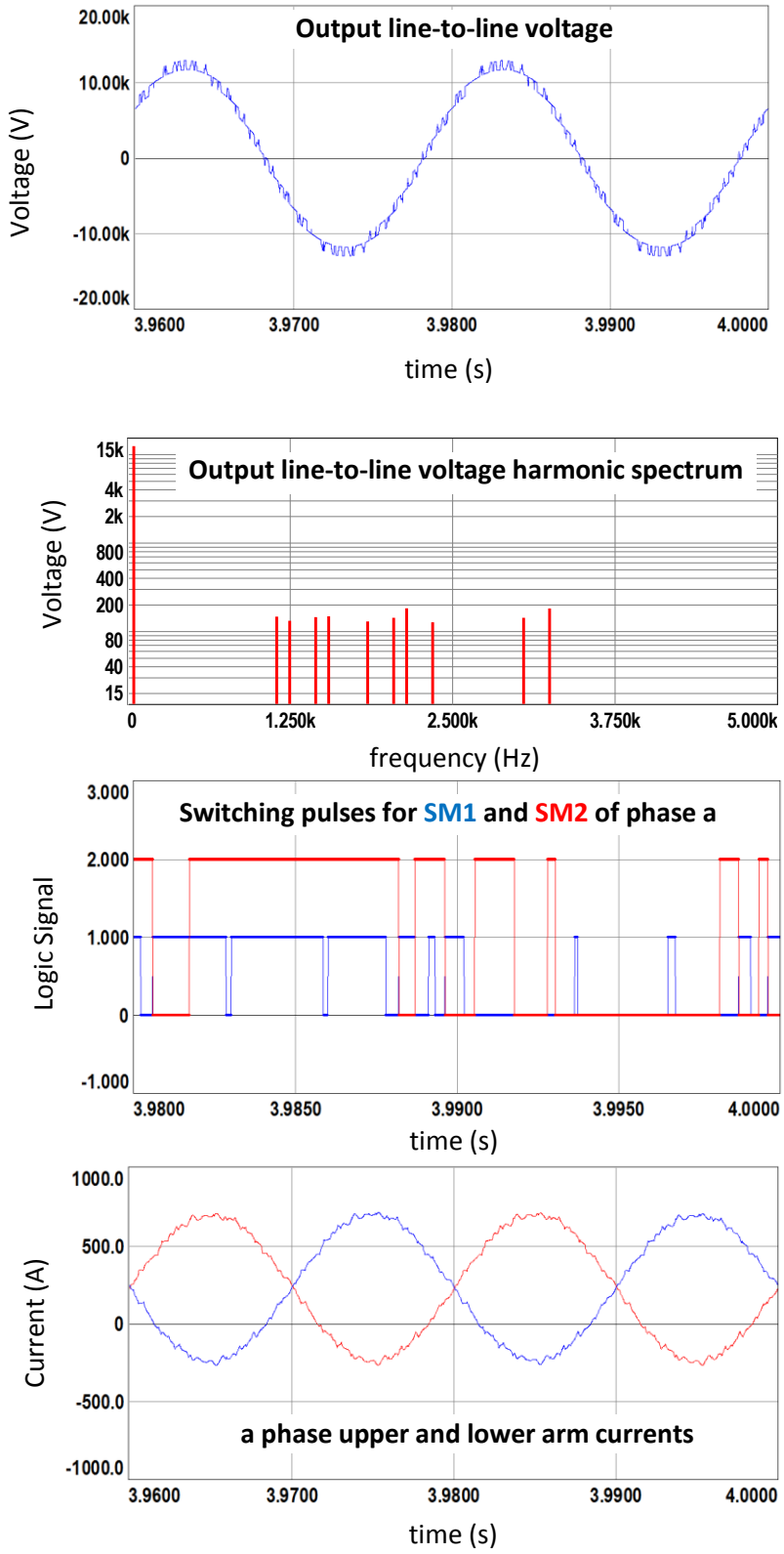


Figure 7.2 (continued) Simulation results for S&S method with N+1 level V_{ph}, full load

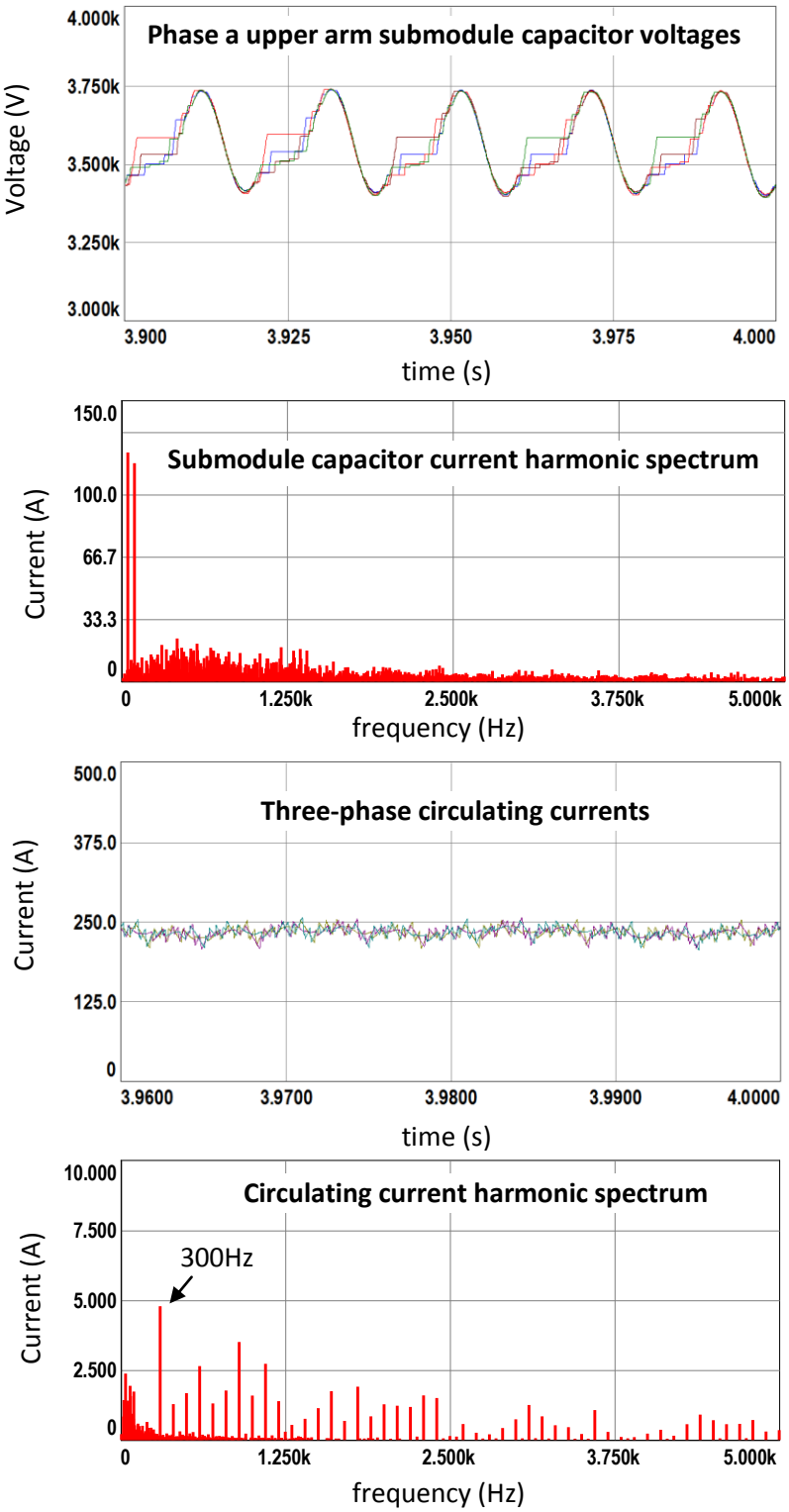


Figure 7.2 (continued) Simulation results for S&S method with N+1 level V_{ph}, full load

In Figure 7.2, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics at the sidebands of f_c and $2f_c$, as expected from Figure 4.34. Output current is close to pure fundamental frequency ac; but there are small harmonics at the sidebands of f_c, which are the seventeenth and twenty-third harmonics. Switching pulse patterns of submodules are differentiated from the original PD method shown in Figure 4.26. In order to keep the submodule capacitor voltage balance, the two submodules are switched in both of the half periods of the fundamental frequency and similar pulses with unequal durations are seen for both of the submodules. Thus, the switching pattern rather resembled to that of PS method as in Figure 4.25. Upper and lower arm currents are balanced in magnitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental and second harmonics. In the low frequency range, there are many consecutive small harmonic components. Three-phase circulating currents are close to dc, the second harmonic is suppressed successively. The remaining ac component is formed mainly by the sixth harmonic. Numerical results of the simulation are listed in Table 7.7.

ii. Direct Modulation, Sort and Select with Reduced Count of Switching Method

Table 7.4 K_p and K_i values of S&S-RS method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

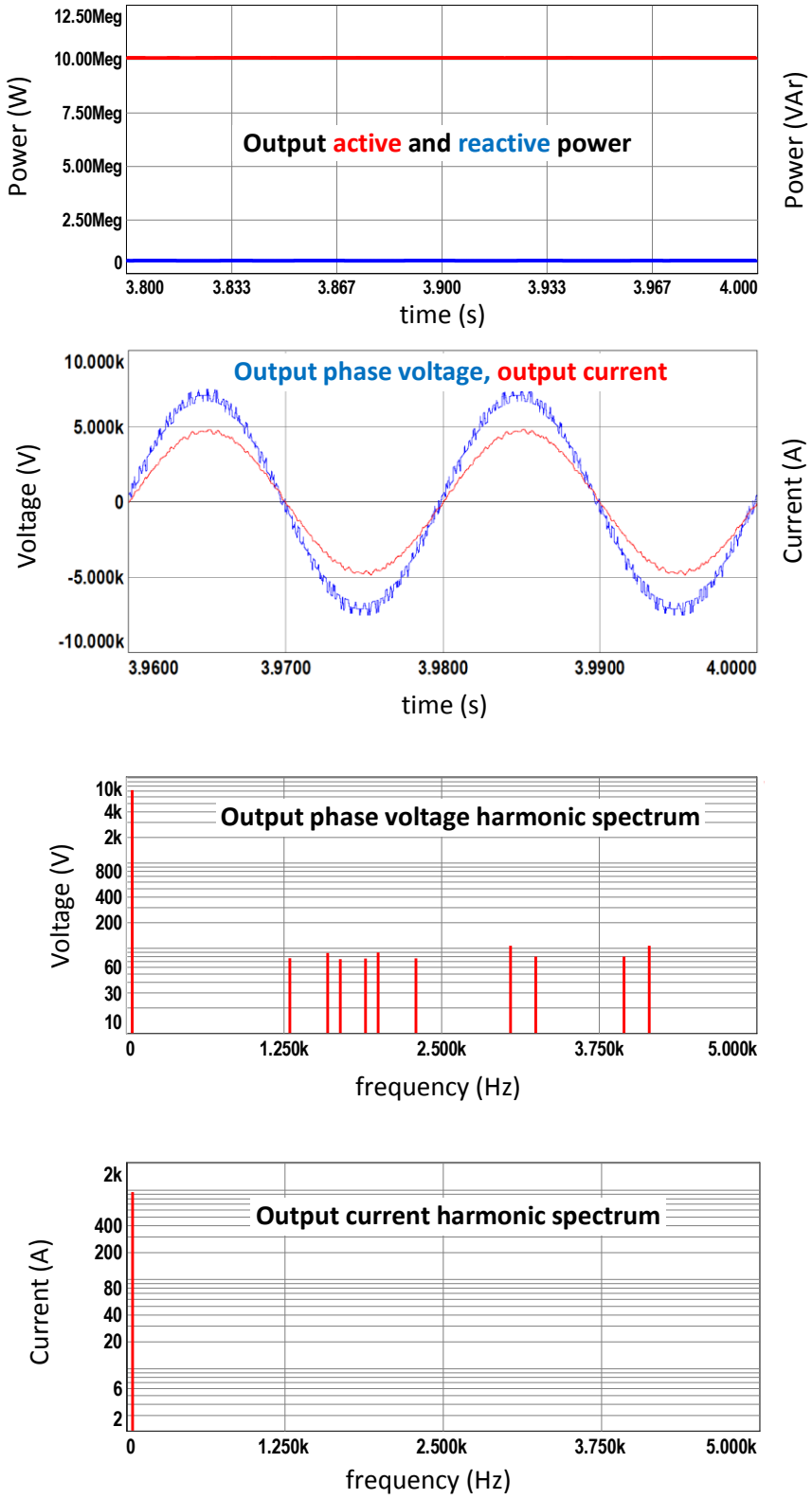


Figure 7.3 Simulation results for S&S-RS method with N+1 level V_{ph}, full load

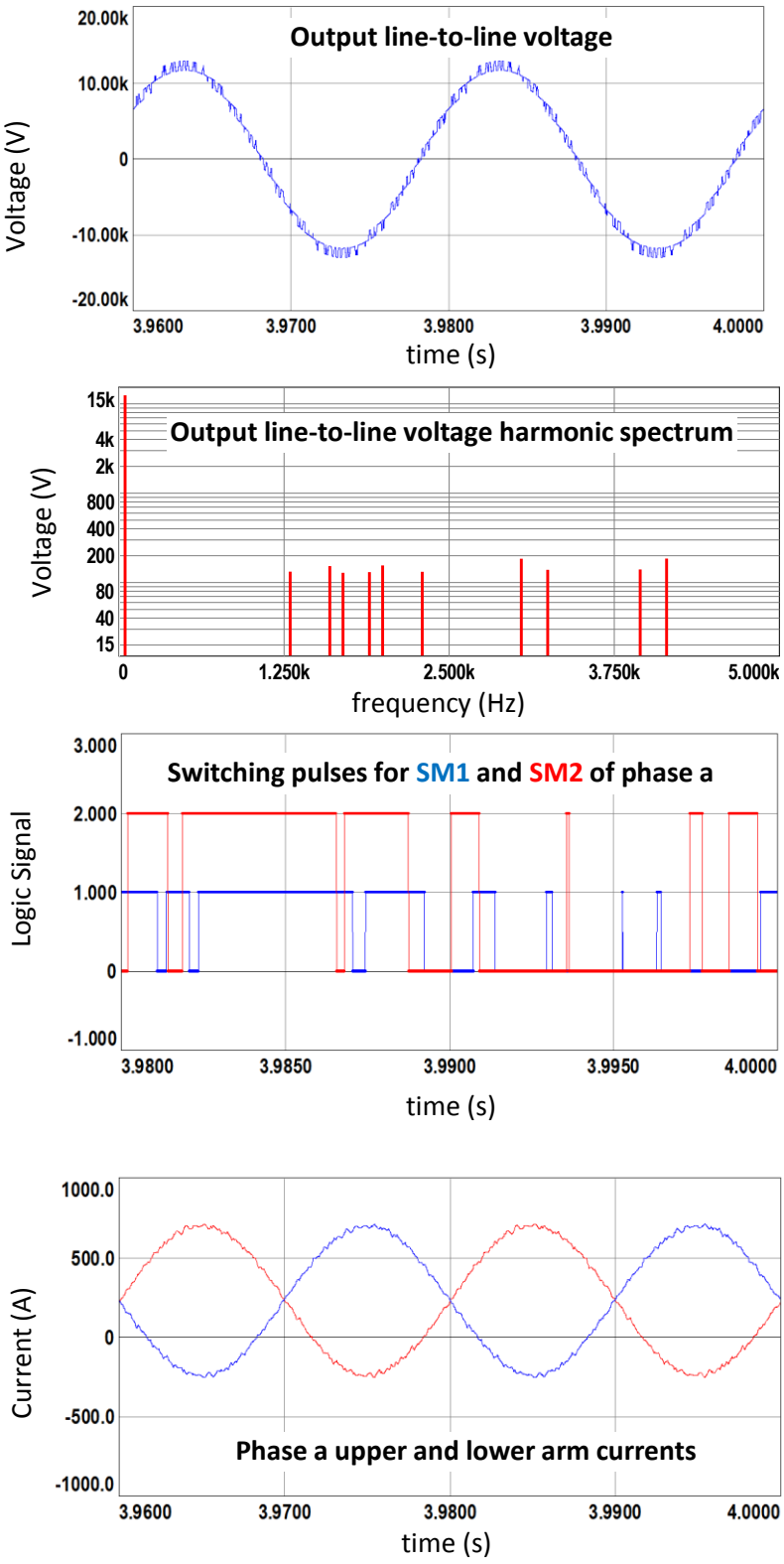


Figure 7.3 (continued) Simulation results for S&S-RS method with N+1 level V_{ph}, full load

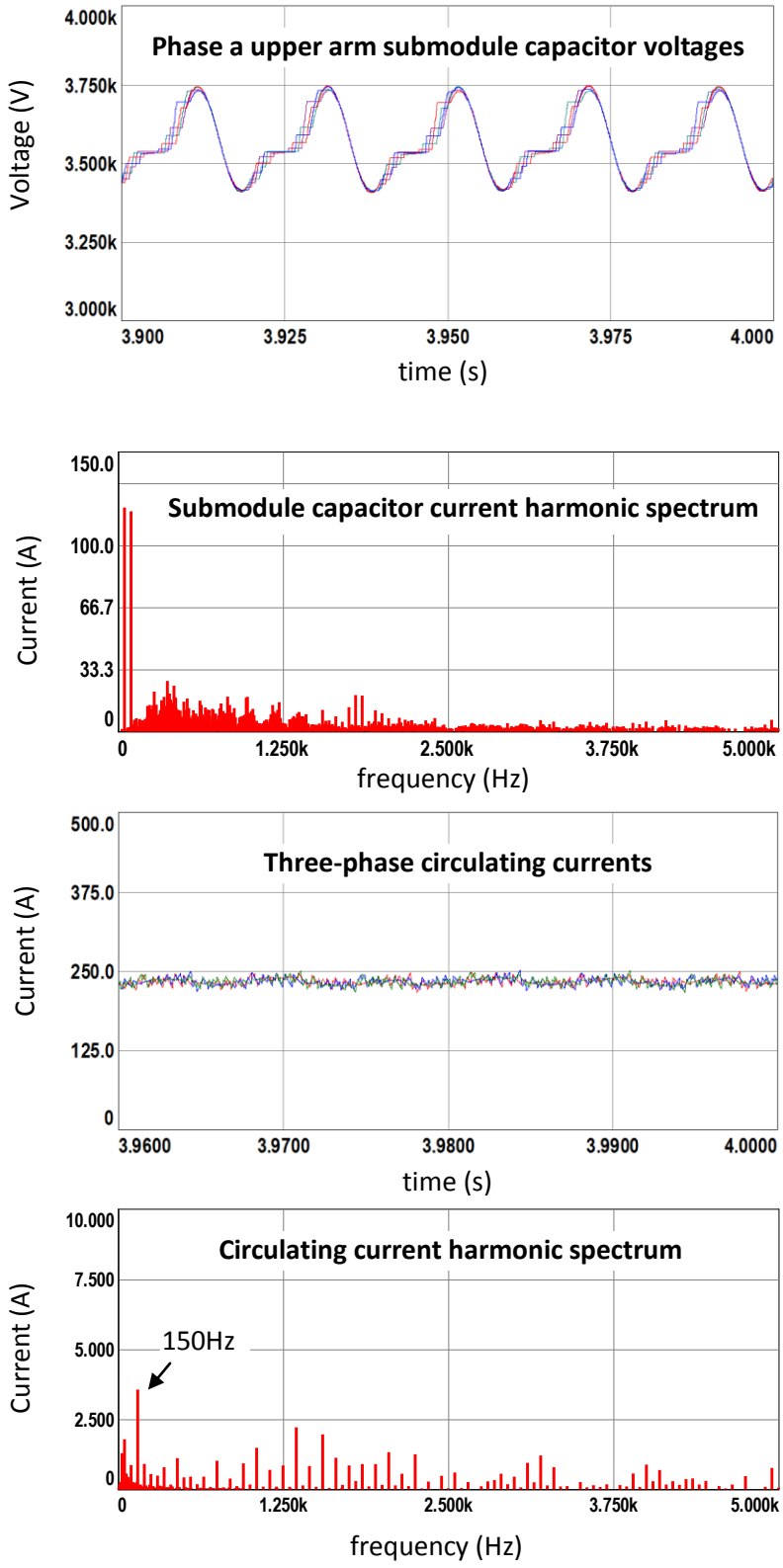


Figure 7.3 (continued) Simulation results for S&S-RS method with N+1 level V_{ph}, full load

In Figure 7.3, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics at the sidebands of f_c and $2f_c$, as expected from Figure 4.34. Output current is close to pure fundamental frequency ac. It has no harmonic which is greater than one per cent of the fundamental. Switching pulse patterns of submodules are differentiated from the original PD method as shown in Figure 4.26. In order to keep the submodule capacitor voltage balance, the two submodules are switched in both of the half periods of the fundamental frequency and similar pulses with unequal durations are seen for both of the submodules. Thus, the switching pulse pattern rather resembled to that of PS method as in Figure 4.25. Upper and lower arm currents are balanced in magnitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental and second harmonics. In low frequency range, there are many consecutive small harmonic components. Three-phase circulating currents are close to dc, the second harmonic is suppressed successively. The remaining ac component is formed mainly by the third harmonic. Numerical results of the simulation are listed in Table 7.7.

iii. Direct Modulation, Carrier Rotation Method

In this simulation case, carrier frequency is tuned as 1950Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.5 K_p and K_i values of CR method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

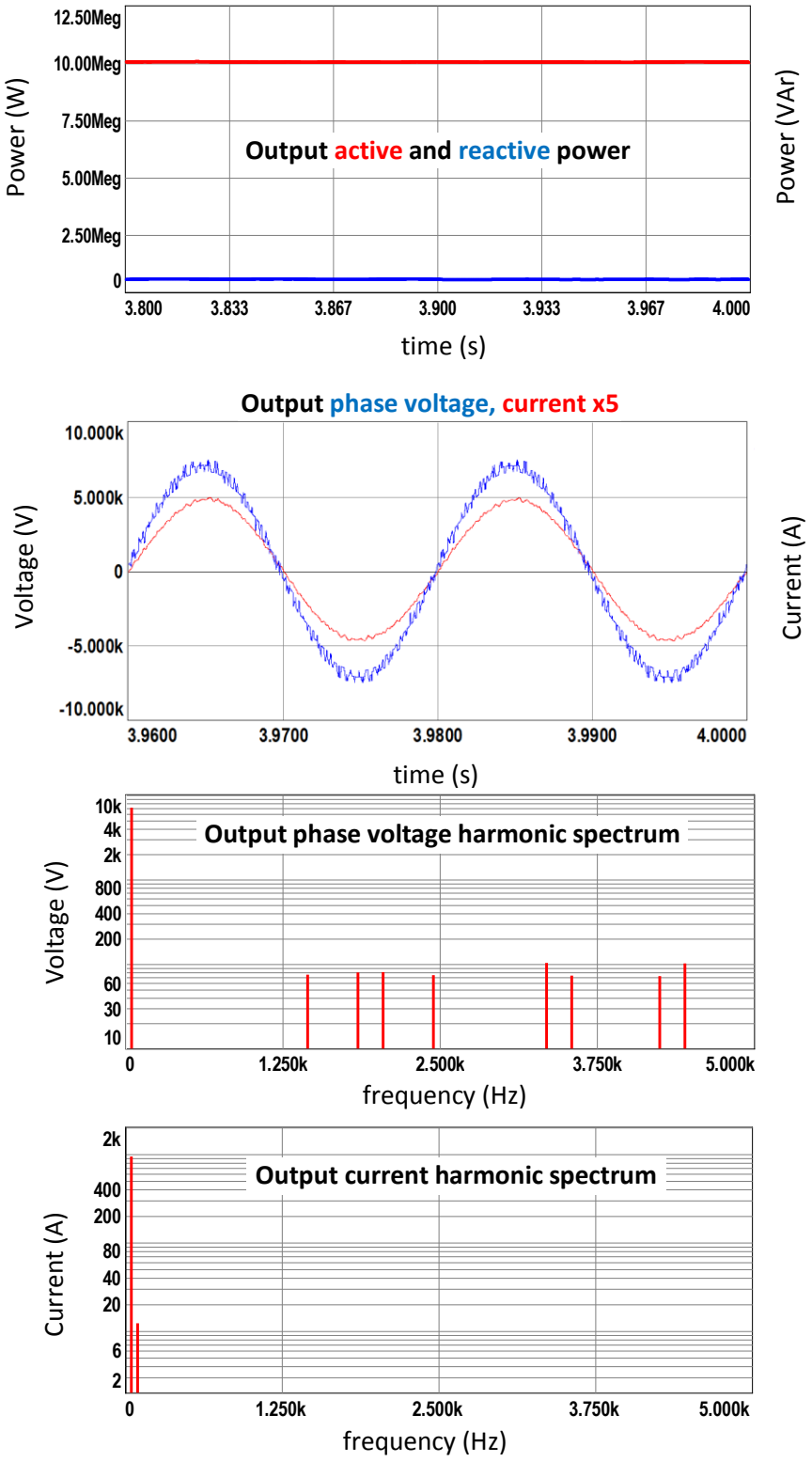


Figure 7.4 Simulation results for CR method with N+1 level V_{ph}, full load

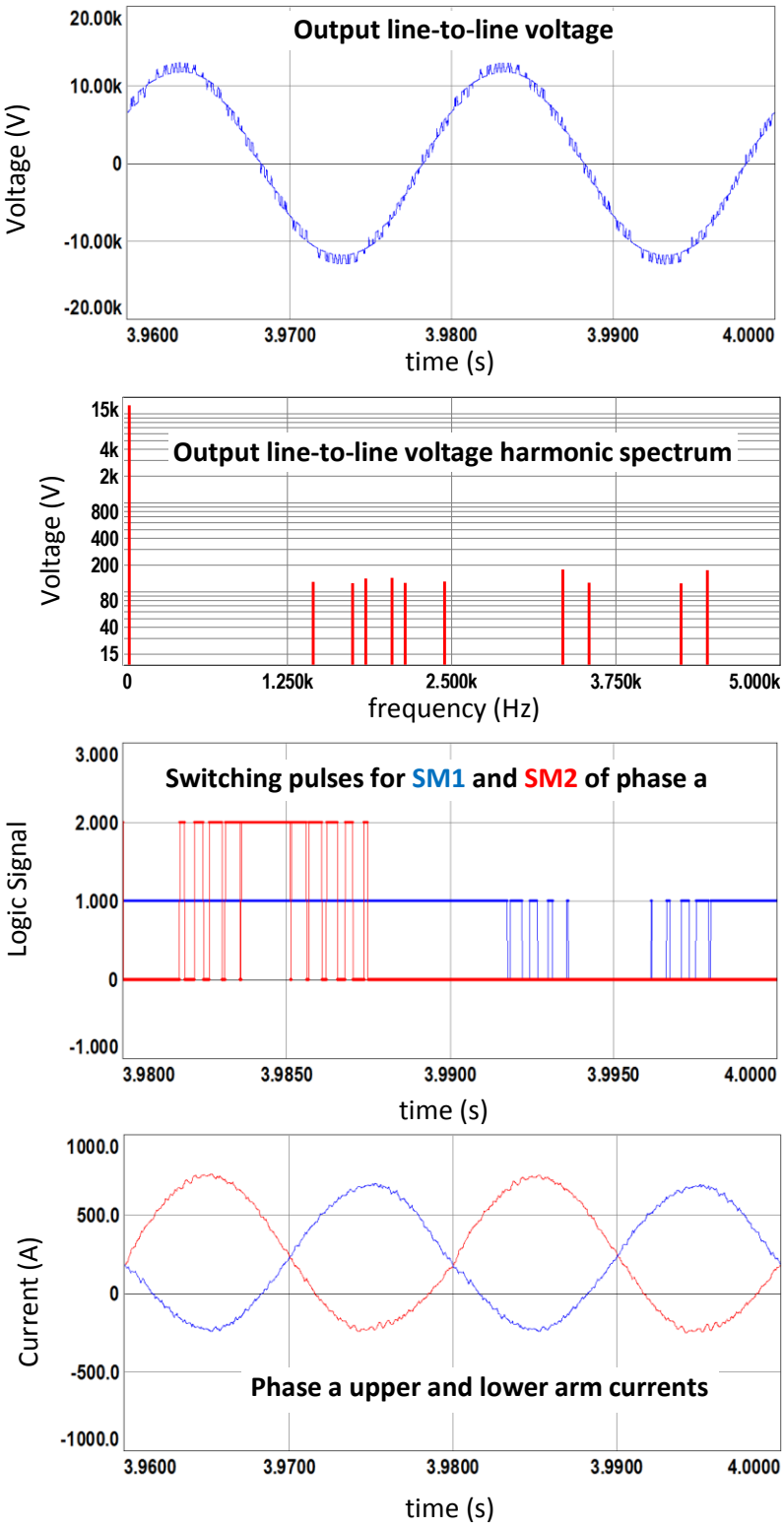


Figure 7.4 (continued) Simulation results for CR method with N+1 level V_{ph}, full load

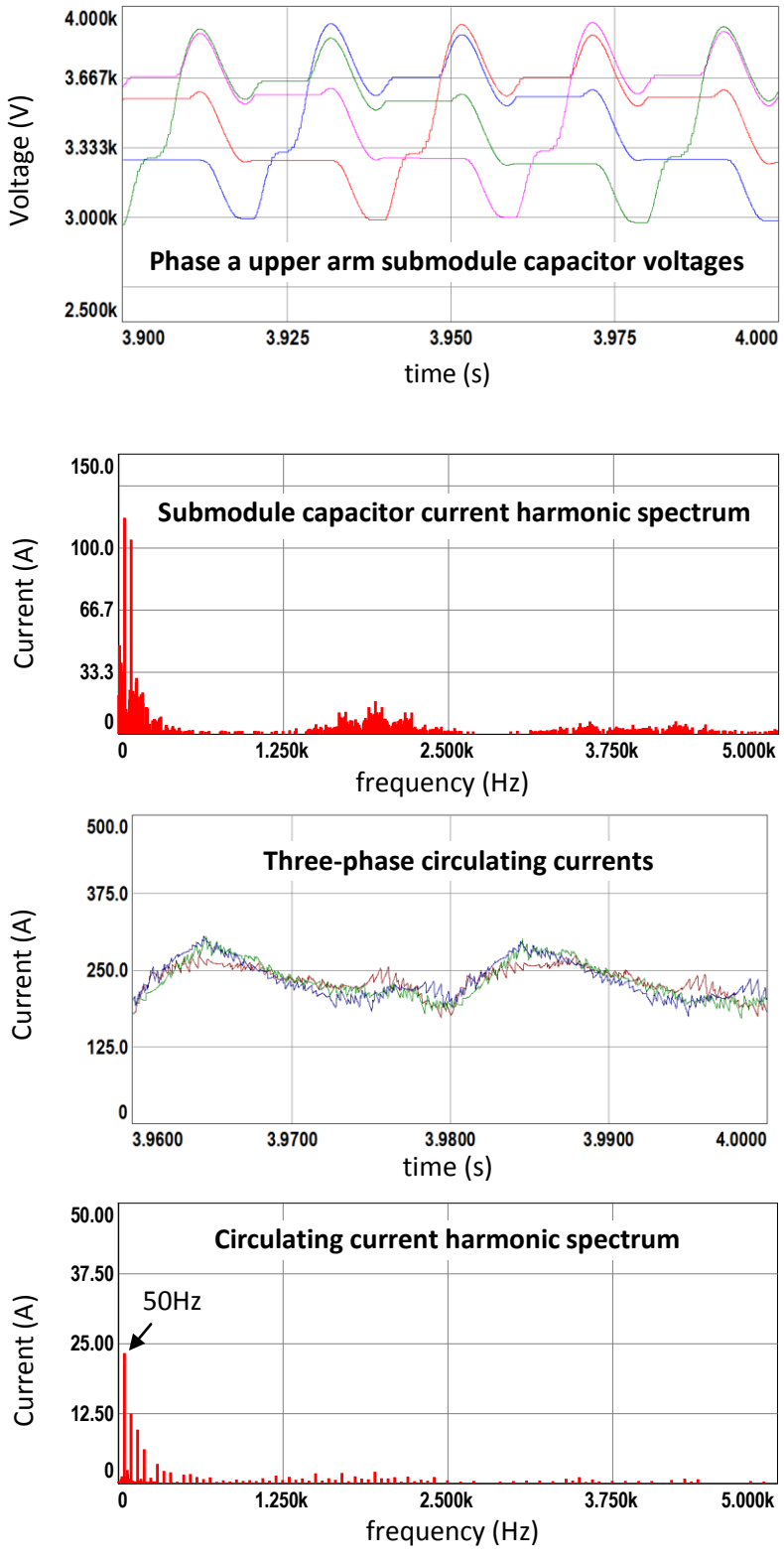


Figure 7.4 (continued) Simulation results for CR method with N+1 level V_{ph}, full load

In Figure 7.4, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics at the sidebands of f_c and $2f_c$, as expected from Figure 4.34. Output current is close to fundamental frequency ac; however, there exists an unexpected small second harmonic component. Actually, this is because of the unbalance between the upper and lower arm currents in amplitude. Switching pulse patterns of submodules are still similar to that of original PD method as shown in Figure 4.26. The switching pulses are present only in one half period of fundamental frequency and they are highly heterogeneous. Therefore the submodule capacitor voltages are greatly differed and the voltage balance is obtained just at the end of carrier rotation period, 80ms for this case. Submodule capacitor current is composed of mainly the fundamental and second harmonics. In low frequency range, there are many consecutive small harmonic components. Three-phase circulating currents are greatly distorted due to the capacitor voltage unbalance. It has a fundamental frequency component as well as the second harmonic. Numerical results of the simulation are listed in Table 7.7.

iv. Phase-shifted Carrier Based Control

In this simulation case, carrier frequency is tuned as 470Hz in order not to have an integer multiple of fundamental frequency [65] and to converge the total count of switching per leg to 450Hz±5%.

Table 7.6 K_p and K_i values of PSCB method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=8	K_i=113	K_p=5.3	K_i=56.5

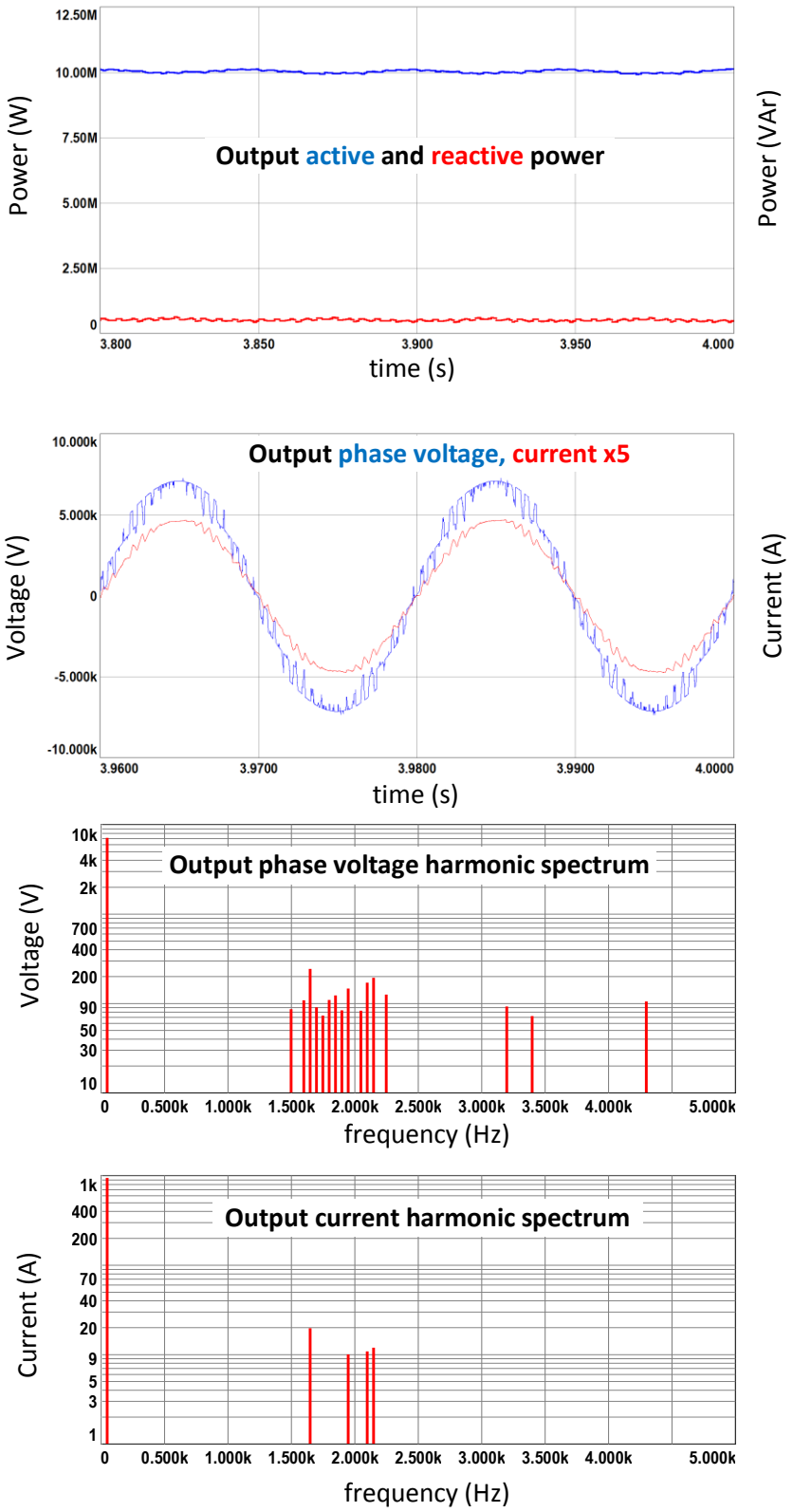


Figure 7.5 Simulation results for PSCB method with N+1 level V_{ph}, full load

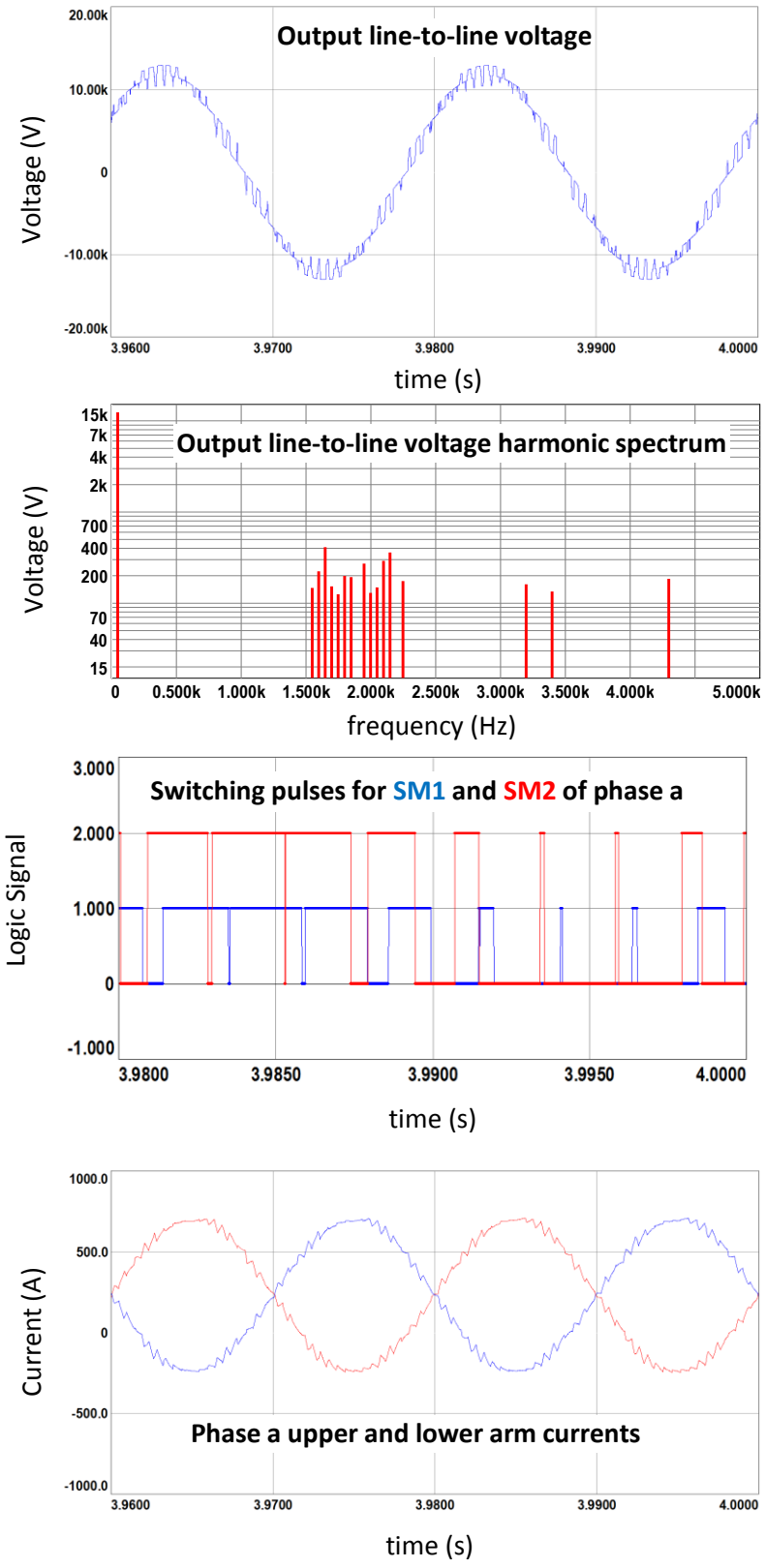


Figure 7.5 (continued) Simulation results for PSCB method with N+1 level V_{ph}, full load

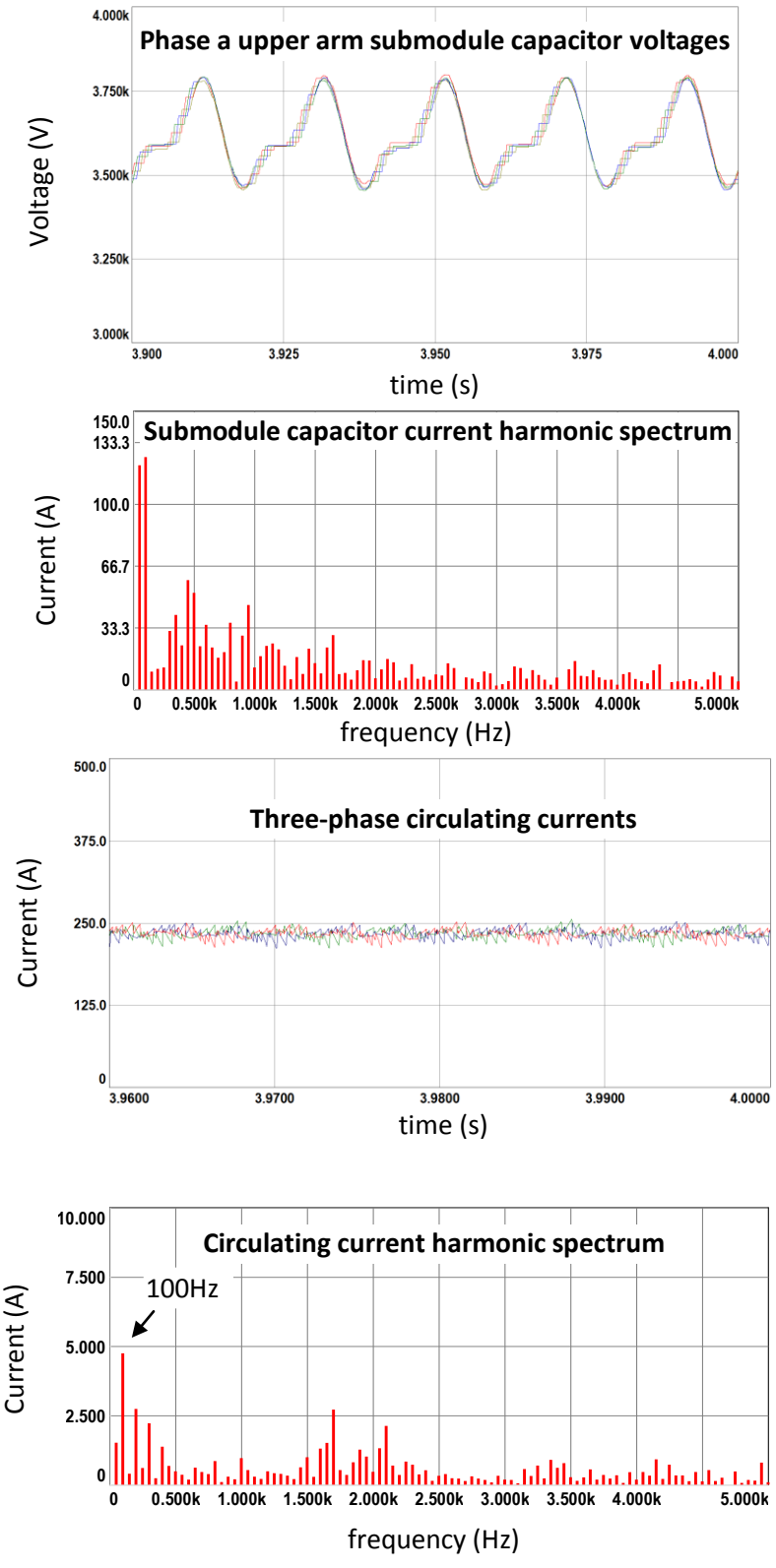


Figure 7.5 (continued) Simulation results for PSCB method with N+1 level V_{ph}, full load

In Figure 7.5, output active and reactive power references are tracked successively; nonetheless the ripple in output power is more than direct modulation case, especially for reactive power output. Output phase and line voltages have harmonics at the sidebands of converter switching frequency (N x f_c) and twice the converter switching frequency (N x $2f_c$), as expected from Figure 4.33. Output current has the highest harmonic distortion among all compared control methods with N+1 level output voltage; it has some odd harmonics at the sidebands of the converter switching frequency. Switching pulse patterns of submodules are similar to that of original PS method as shown in Figure 4.25. Upper and lower arm currents are balanced in amplitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value and they are in close proximity. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental component and second harmonic. Also, there are significant harmonics close to the carrier frequency. In low frequency range, there are many consecutive small harmonic components; however, these are much less in count and greater in amplitude than that of direct modulation methods, S&S and S&S-RS. Three-phase circulating currents are close to dc, but there still exists a dominant second harmonic as well as some other even harmonics such as the fourth, sixth, eighth and tenth, in the frequency spectrum. Numerical results of the simulation are listed in Table 7.7.

Table 7.7 reveals important performance results about the simulated control methods. The average switching frequency of an arm is close to the range of 450±5% Hz, for all the methods. Actually, for S&S method, it is slightly out of the range, but decreasing the m_f value resulted in a worse case, going more out of the range in the lower band, so the former condition is kept. Although it gives the best output voltage harmonics performance, CR method on its own is not suitable for MMC control since it has the largest submodule capacitor voltage ripple (roughly three times compared to others) and circulating current ac component (six times compared to S&S-RS). Also the unbalance of arm currents for CR method resulted

in a second harmonic component in output current and fundamental harmonic in the circulating current, which are both abnormal. Moreover, since the method does not sense the capacitor voltages, in case of a fault or an unbalanced condition in capacitor voltages, the method is not able to respond the occasion rapidly. Therefore the circuit is very likely to go an unsteady situation. The all other methods are able to keep the circuit in steady state. They provided a balanced exploitation for the submodules of an arm. They have similar switching counts, which eases thermal control of semiconductors. The performance of S&S-RS method is superior to others in terms of output current harmonic distortion (3/4 times that of the next better method, S&S), circulating current ac component magnitude and efficiency. Indeed, efficiency values of the methods are close to each other and the largest difference is in the range of three in ten thousand. Although the values are close to each other except CR method, PSCB method has the lowest submodule capacitor voltage ripple. However, its output harmonic distortion for voltage is more than one and a half times and current is twice higher than direct modulation methods. Hence, S&S-RS method seems to be the suitable method, for N+1 level output voltage case for a grid connected MMC drive.

Table 7.7 Simulation results numerical data for N+1 level output voltage

		Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		5.03	5.01	4.80	8.25
Line-to-line voltage THD (%)		5.02	5.01	4.78	8.23
Current (i_l) THD (%)		2.76	2.00	2.34	4.04
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		9.56	9.39	26.35	9.06
Circulating current ($i_{circ,dc}$) (A)		234.21	234.50	233.95	234.22
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		3.73	2.31	13.01	2.73
Arm current (i_p) (A_{rms})		407.73	408.17	425	409.07
Average switching frequency of phase a upper arm submodules (Hz)	SM1	480	428	434	448
	SM2	476	438	432	439
	SM3	472	445	433	448
	SM4	490	450	433	449
	Average of arm	480	440	433	446
Efficiency (%)		98.88	98.91	98.88	98.89

7.3.1.2. Case 2: 2N+1 Output Voltage Levels

i. Direct Modulation, Sort and Select Method

In this simulation case, carrier frequency is tuned as 1350Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.8 K_p and K_i values of S&S method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=12	K_i=84.8	K_p=15.9	K_i=170

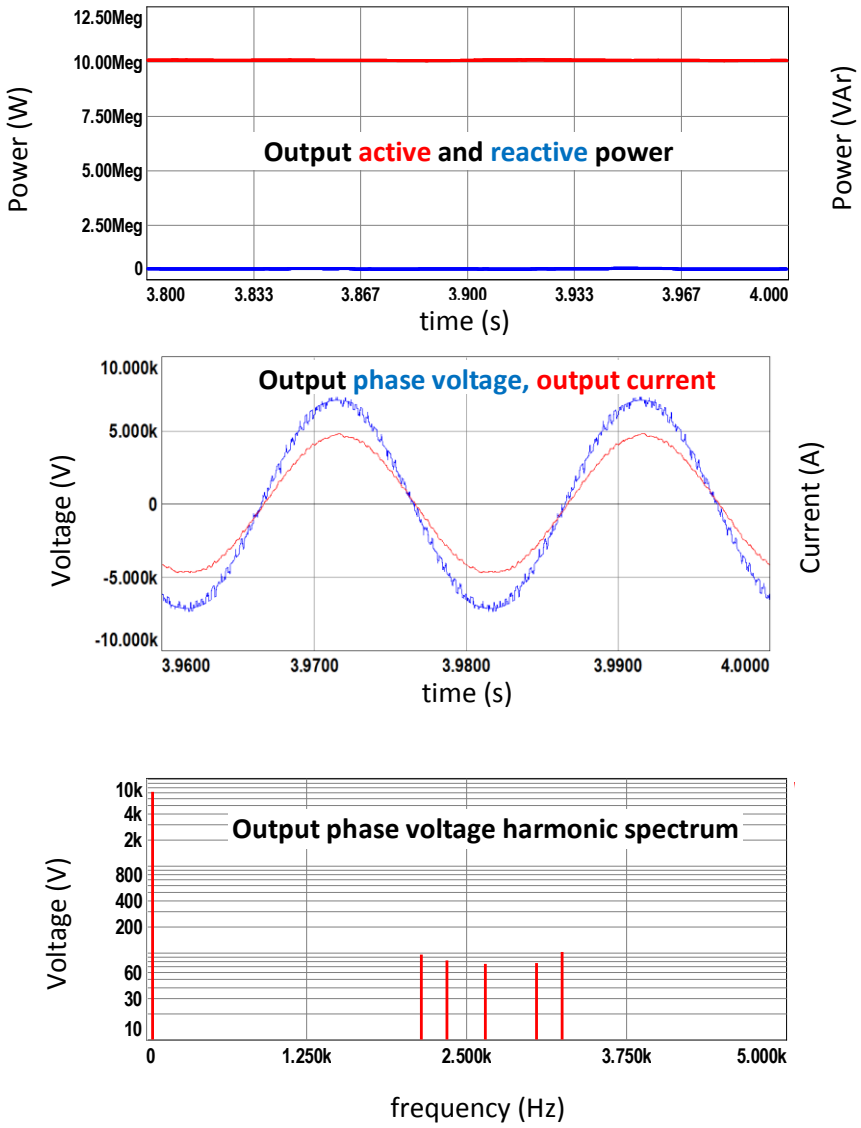


Figure 7.6 Simulation results for S&S method with 2N+1 level V_{ph}, full load

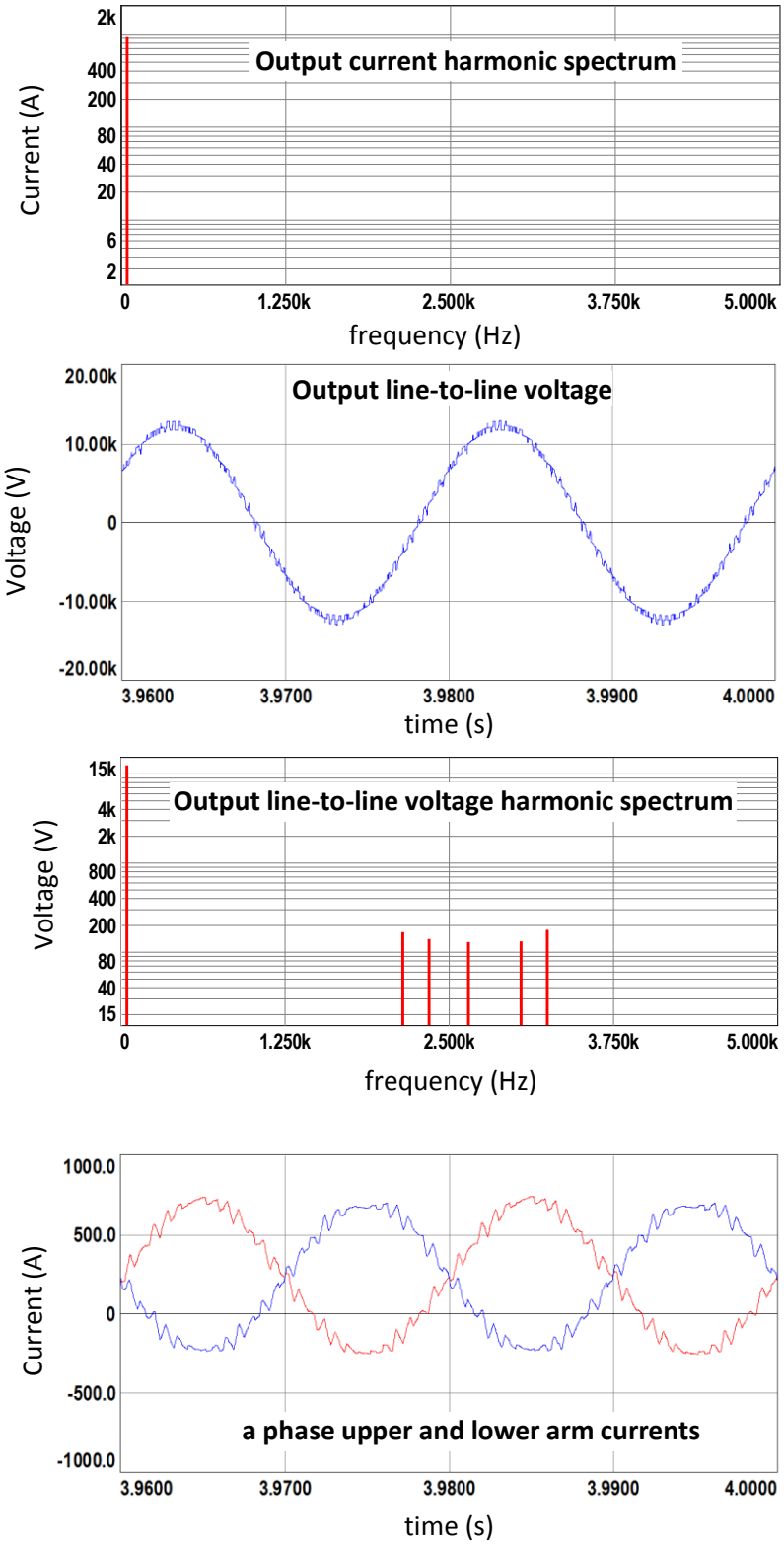


Figure 7.6 (continued) Simulation results for S&S method with 2N+1 level V_{ph}, full load

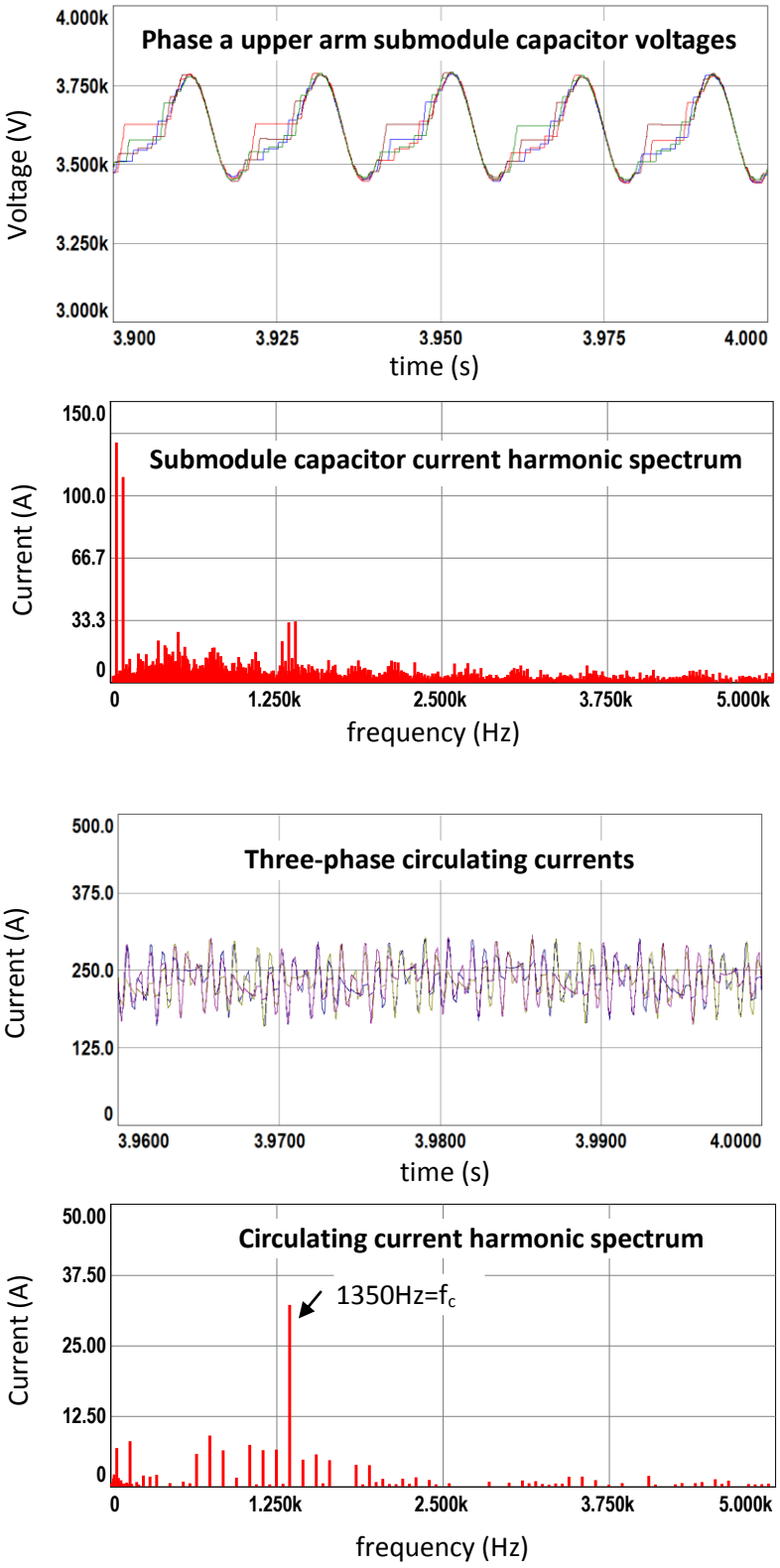


Figure 7.6 (continued) Simulation results for S&S method with 2N+1 level V_{ph}, full load

In Figure 7.6, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics at the sidebands of $2f_c$, as expected from Figure 4.46. Output current is closer to pure fundamental frequency ac than that of N+1 case, since the output voltage level, so does the converter switching frequency, is doubled. There is no current harmonic greater than one per cent of fundamental component. Upper and lower arm currents are balanced in magnitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental and second harmonics. Furthermore, there are significant harmonics at the sidebands of carrier frequency. In low frequency range there are many consecutive small harmonic components. Three-phase circulating currents have much more ac component than N+1 case. Although the second harmonic is suppressed successively, different from N+1 case, a significant carrier frequency component emerged which distorts the waveform distinctly. Numerical results of the simulation are listed in Table 7.12.

ii. Direct Modulation, Sort and Select with Reduced Count of Switching Method

Table 7.9 K_p and K_i values of S&S-RS method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

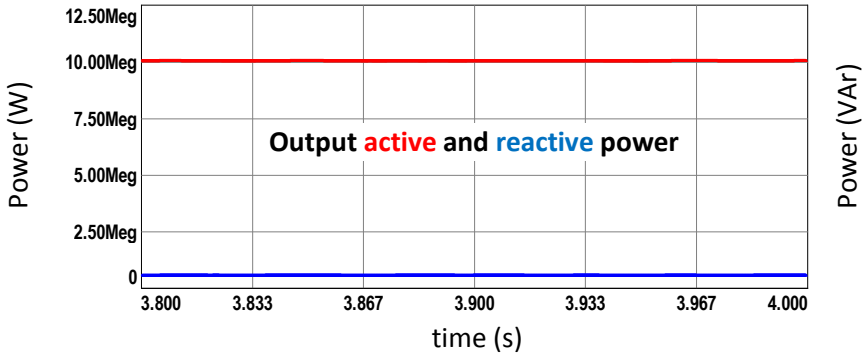


Figure 7.7 Simulation results for S&S-RS method with 2N+1 level V_{ph}, full load

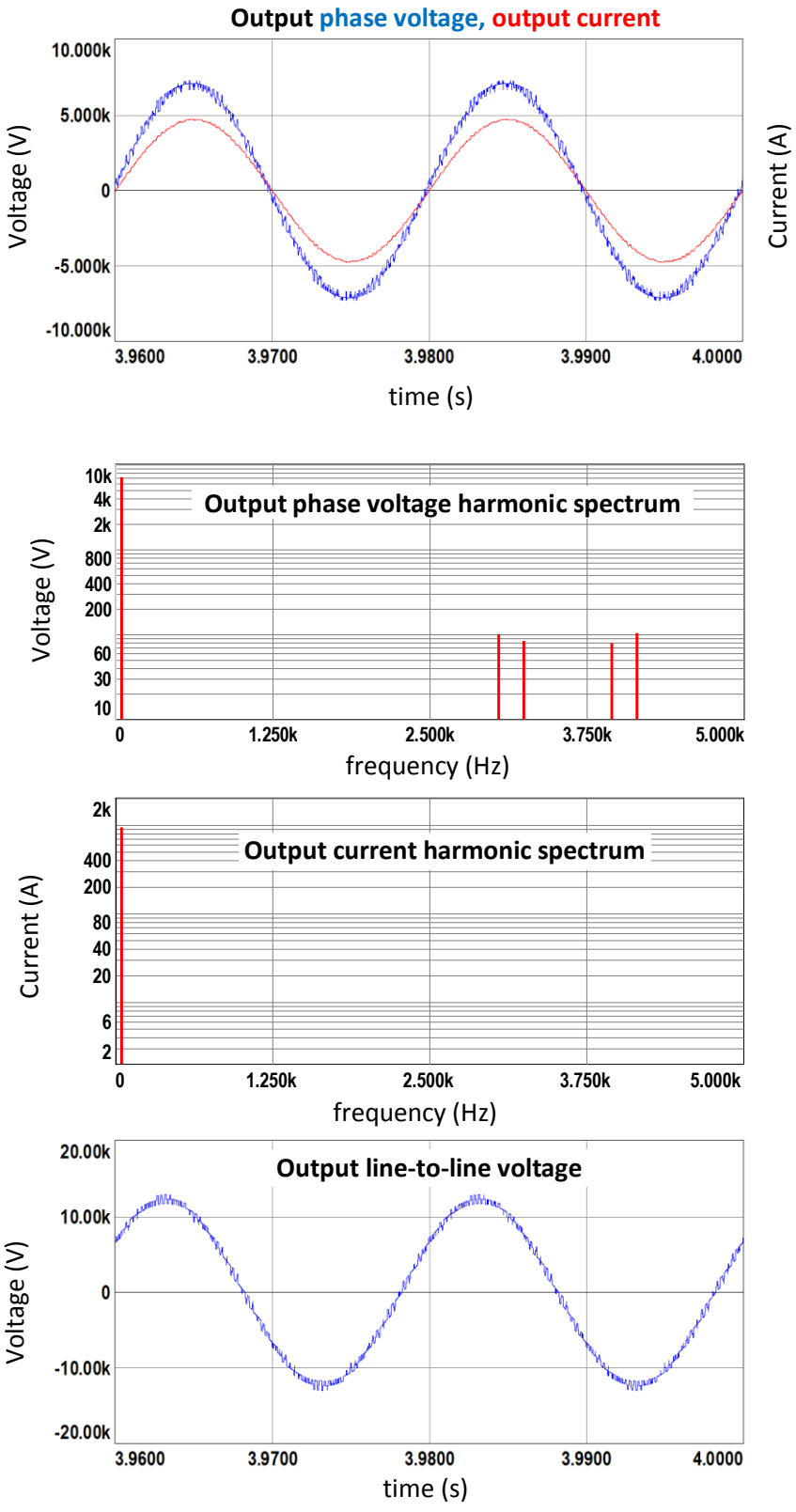


Figure 7.7 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, full load

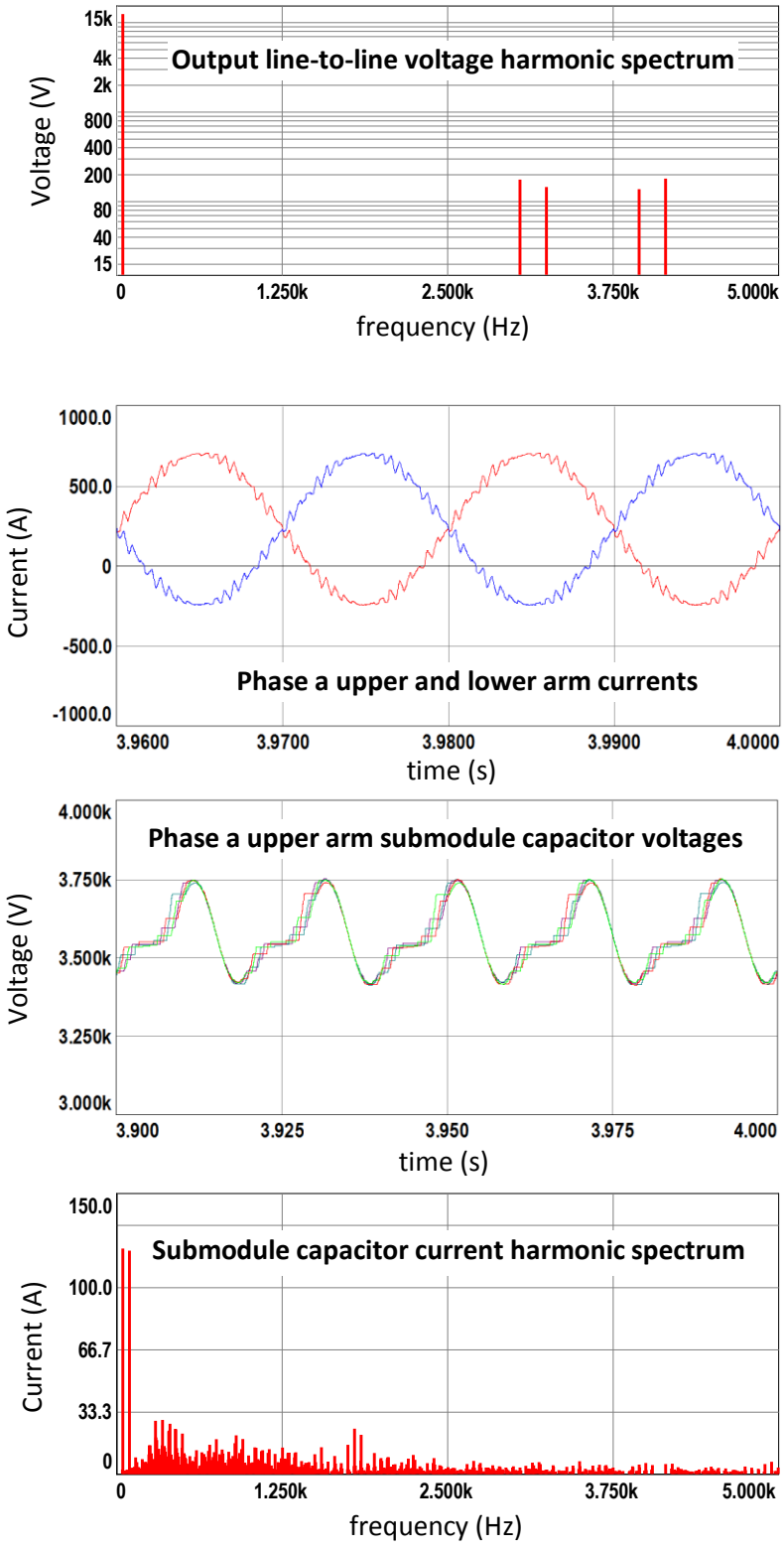


Figure 7.7 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, full load

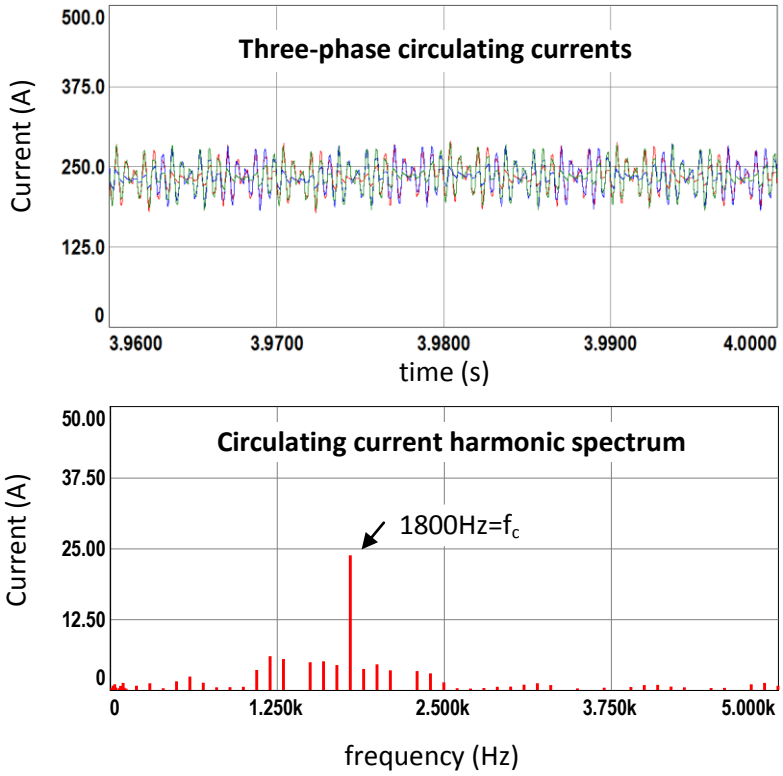


Figure 7.7 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, full load

In Figure 7.7, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics around $2f_c$, as expected from Figure 4.46. Output current is closer to fundamental frequency ac than that of N+1 case, since the output voltage level, so does the converter switching frequency, is doubled. There is no current harmonic greater than one per cent of fundamental component. Upper and lower arm currents are balanced in magnitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental and second harmonics. Also, there are significant harmonics at the sidebands of carrier frequency and in low frequency range there are many consecutive small harmonic components. Three-phase

circulating currents have much more ac component than N+1 case. Although the second harmonic is suppressed successively, different from N+1 case, a significant carrier frequency component emerged which distorts the waveform distinctly. Numerical results of the simulation are listed in Table 7.12.

iii. Direct Modulation, Carrier Rotation Method

In this simulation case, carrier frequency is tuned as 1950Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.10 K_p and K_i values of CR method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

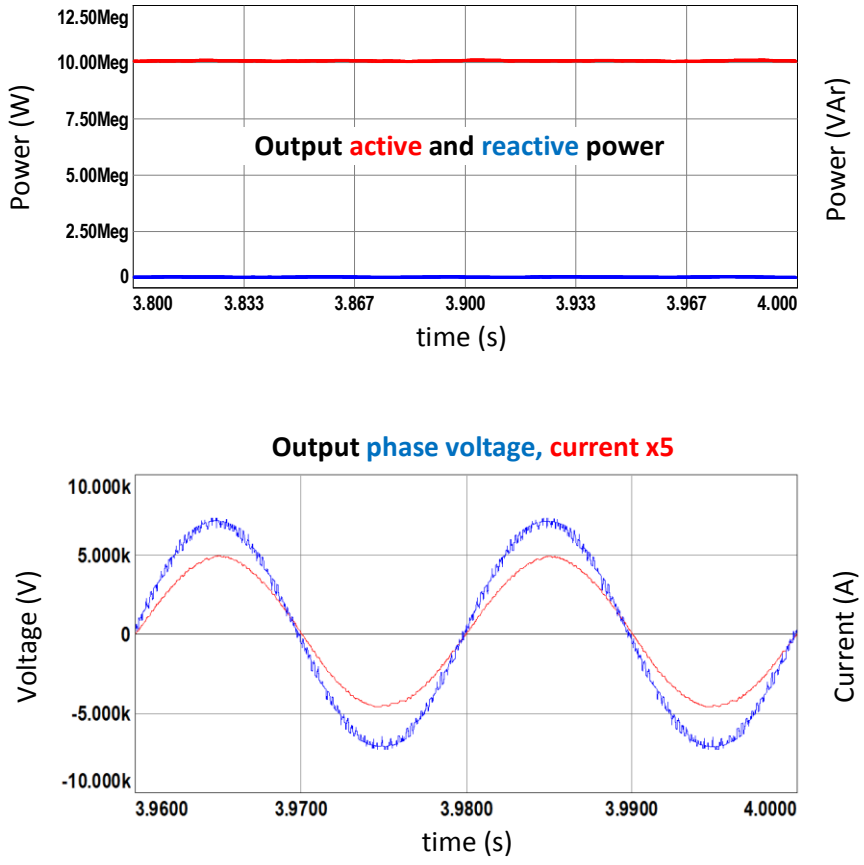


Figure 7.8 Simulation results for CR method with 2N+1 level V_{ph}, full load

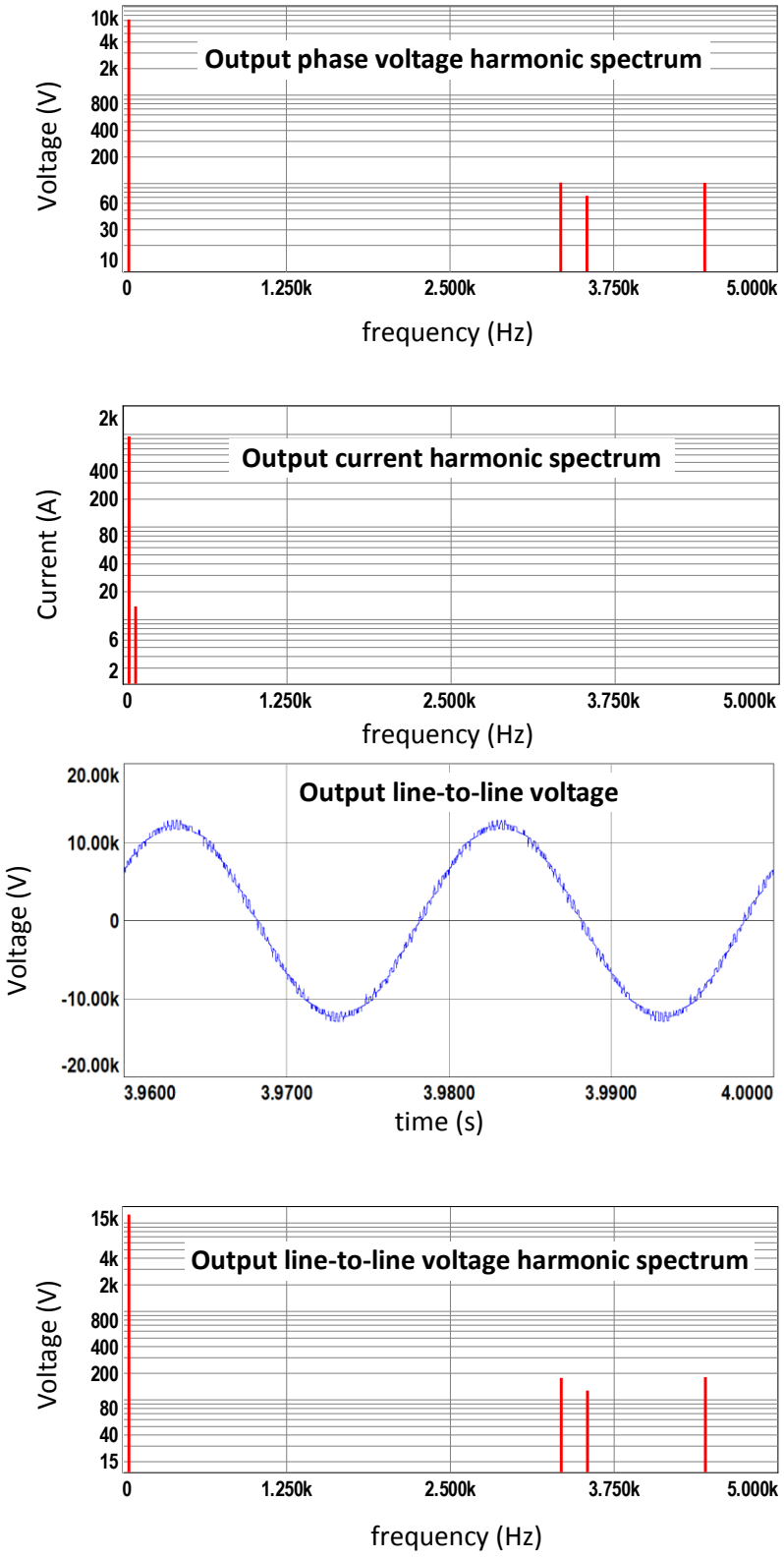


Figure 7.8 (continued) Simulation results for CR method with 2N+1 level V_{ph}, full load

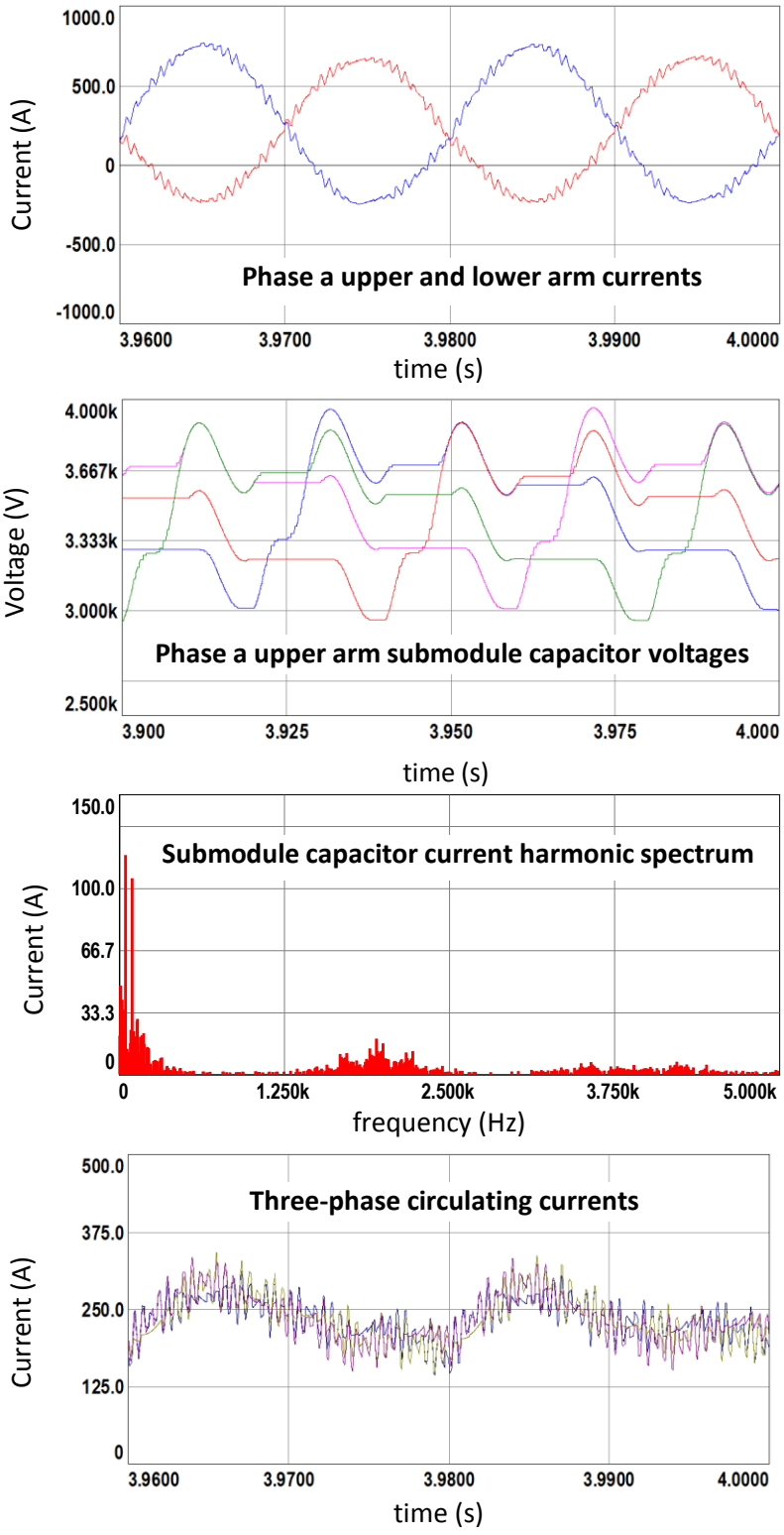


Figure 7.8 (continued) Simulation results for CR method with 2N+1 level V_{ph}, full load

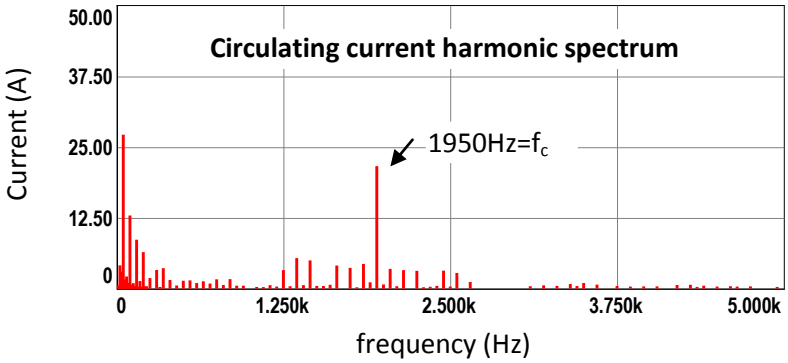


Figure 7.8 (continued) Simulation results for CR method with 2N+1 level V_{ph}, full load

In Figure 7.8, output active and reactive power references are tracked successively. Output phase and line voltages have harmonics at the sidebands of $2f_c$, as expected from Figure 4.46. Output current is closer to fundamental frequency ac than that of N+1 case, since the output voltage level, so does the converter switching frequency, is doubled. However, it again contains second harmonic as in N+1 case, because of the unbalance between the upper and lower arm currents in amplitude. The submodule capacitor voltages are greatly differed and the voltage balance is obtained just at the end of carrier rotation period, 80ms for this case. Submodule capacitor current is composed of mainly the fundamental and second harmonics. In low frequency range, there are many consecutive small harmonic components. Three-phase circulating currents are greatly distorted due to the capacitor voltage unbalance. They have a fundamental frequency component as well as other even harmonics. Moreover, a significant carrier frequency component emerged which distorts the waveform distinctly. Numerical results of the simulation are listed in Table 7.12.

iv. Phase-shifted Carrier Based Control

In this simulation case, carrier frequency is tuned as 430Hz in order not to have an integer multiple of fundamental frequency [65] and to converge the total count of switching per leg to 450Hz±5%.

Table 7.11 K_p and K_i values of PSCB method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=12	K_i=169.62	K_p=5.3	K_i=56.5

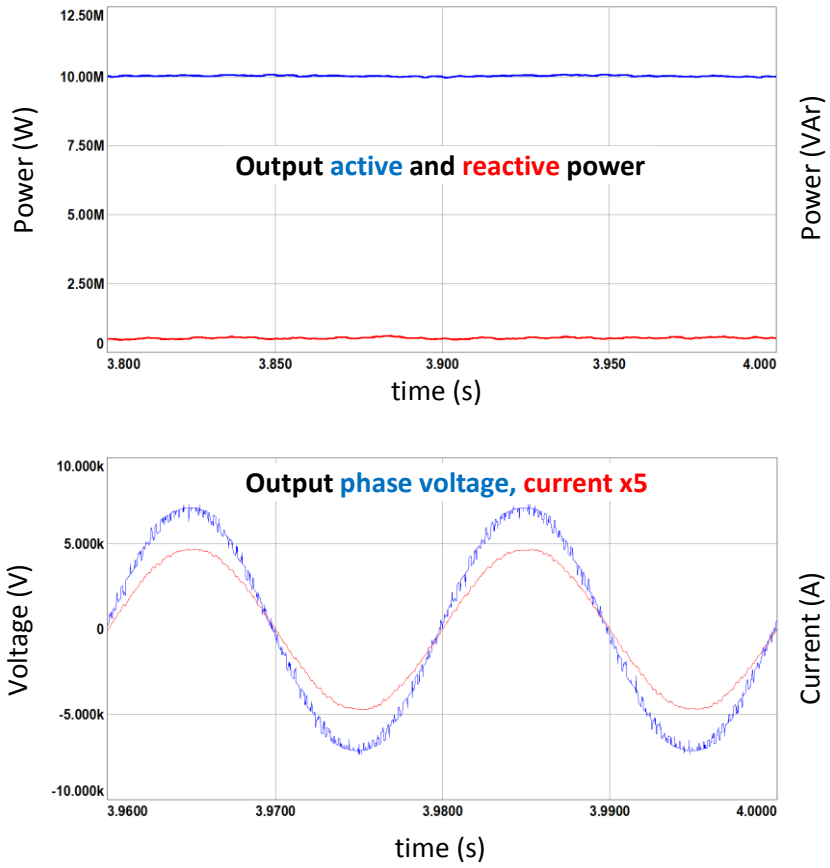


Figure 7.9 Simulation results for PSCB method with 2N+1 level V_{ph}, full load

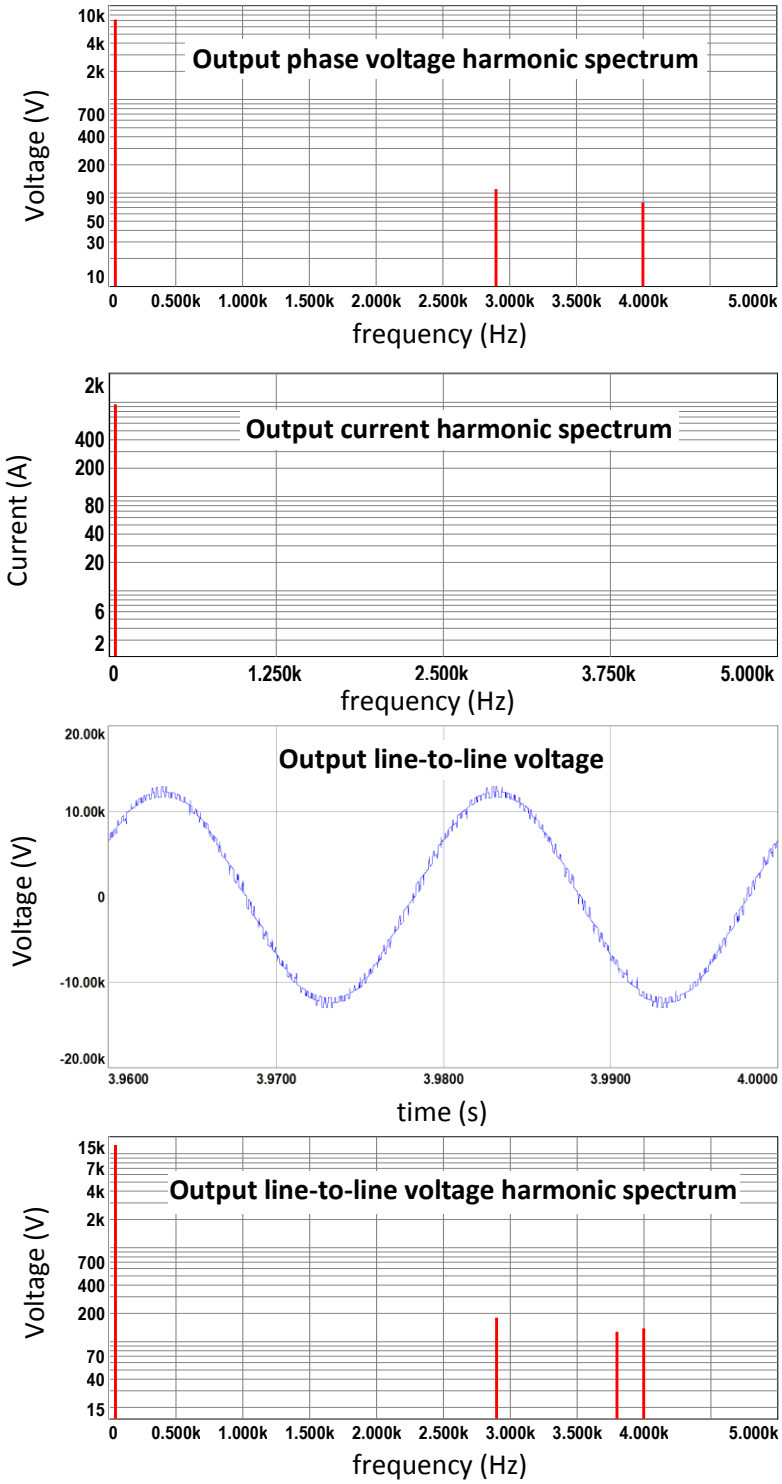


Figure 7.9 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, full load

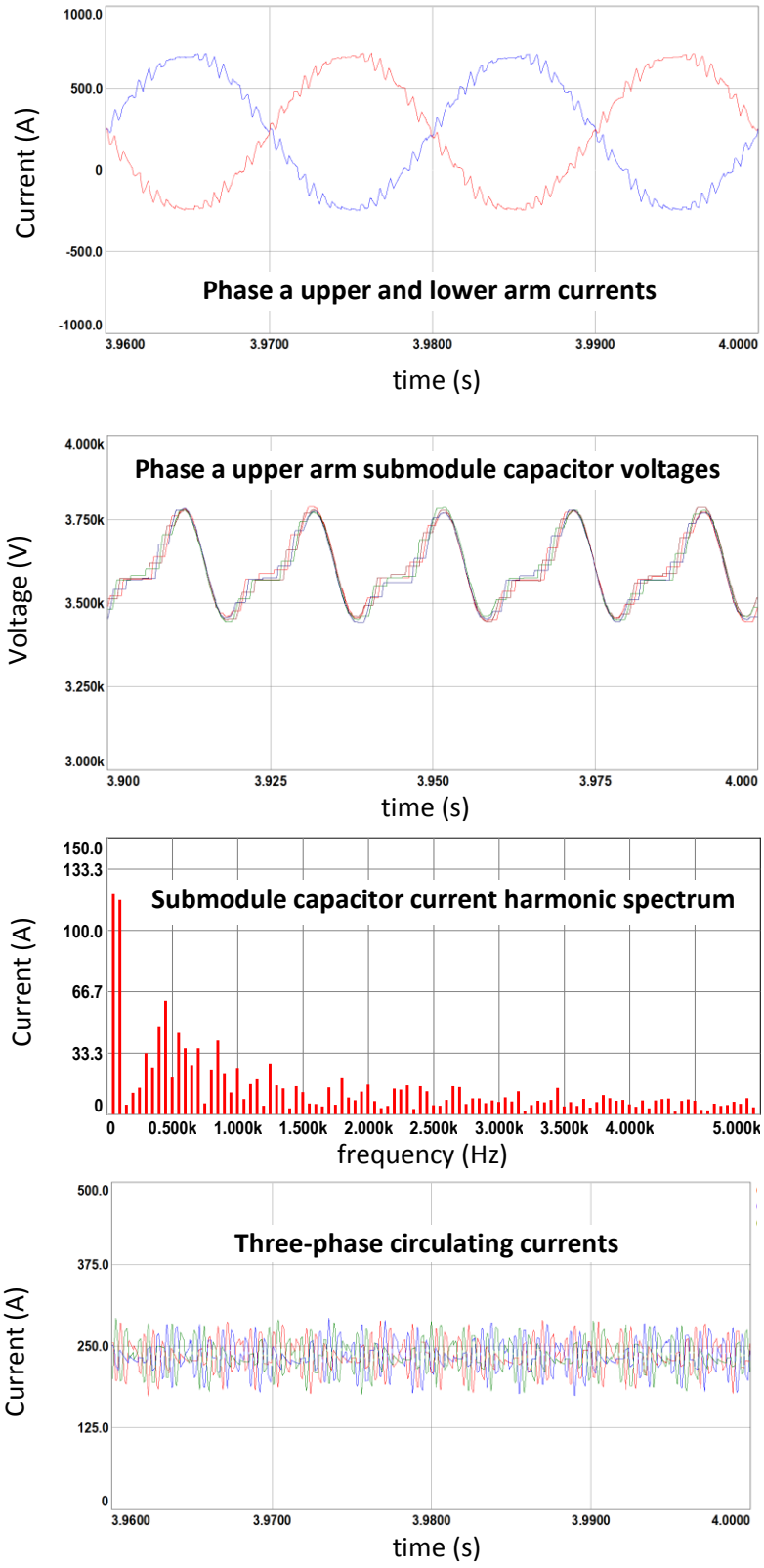


Figure 7.9 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, full load

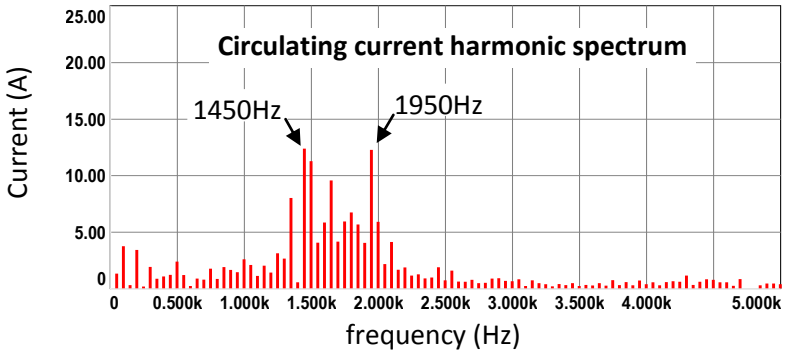


Figure 7.9 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, full load

In Figure 7.9, output active and reactive power references are tracked successively. The ripple in output active and reactive power decreased significantly compared to N+1 level V_{ph} case. Output phase and line voltages have harmonics at the sidebands of converter switching frequency (2N x f_c), as expected from Figure 4.45. Output current is closer to fundamental frequency ac than that of N+1 case, since the output voltage level, so does the converter switching frequency, is doubled. There is no harmonic greater than one per cent of fundamental component. Upper and lower arm currents are balanced in magnitude and π radians out of phase as expected. Submodule capacitor voltages are balanced around 3.6kV nominal value and they are in close proximity. They have a dominant fundamental frequency and significant second harmonic component, validated by submodule capacitor current harmonic spectrum. It is composed of mainly the fundamental and second harmonics. Also, there is a significant harmonic close to the carrier frequency. In low frequency range, there are many consecutive small harmonic components; however, these are much less in count and greater in magnitude than that of direct modulation methods. Three-phase circulating currents have much more ac component than N+1 case. Although the second harmonic is suppressed successively, different from N+1 case, there exist significant components at the sidebands of (N x f_c) which distort the waveform distinctly. Numerical results of the simulation are listed in Table 7.12.

Table 7.12 Simulation results numerical data for 2N+1 level output voltage

		Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		3.97	3.93	3.84	4.15
Line-to-line voltage THD (%)		3.98	3.92	3.81	4.19
Current (i_l) THD (%)		1.69	1.06	2.11	1.49
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		9.67	9.40	26.72	9.16
Circulating current ($i_{circ,dc}$) (A)		234.43	234.46	234.93	234.31
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		12.16	8.64	15.86	9.39
Arm current (i_p) (A_{rms})		412.8	408.34	429.70	407.31
Average switching frequency of phase a upper arm submodules (Hz)	SM1	458	435	431	465
	SM2	440	443	432	443
	SM3	446	437	430	464
	SM4	461	451	429	463
	Average of arm	451	442	431	459
Efficiency (%)		98.85	98.92	98.79	98.83

Table 7.12 gives similar results to the Table 7.7 for the different control methods. Again S&S-RS method gives the best performance in terms of output current harmonic distortion, circulating current ac component magnitude and efficiency. Output current THD of S&S-RS method is about 0.7 times that of PSCB method and 0.63 times that of S&S method. Voltage THD is close to each other for direct modulation methods and that of S&S-RS method is 0.9 times of PSCB. Circulating current is significantly lower for S&S-RS and PSCB methods, compared to S&S and CR methods, and S&S-RS has 0.9 times that of PSCB method. Efficiency values are again close to each other but this time efficiency of S&S-RS is more distinctly higher compared to N+1 case; about 0.07% compared to the next efficient method, S&S. PSCB gives lowest submodule capacitor voltage ripple as in N+1 case, but the difference between S&S-RS and PSCB is 0.24%. As a result, taking all the criteria into account, S&S-RS method stands out among all, highlighting that it would be the suitable method for 2N+1 level output voltage case, as well as N+1 level case [66].

Table 7.13 gives the differences of characteristics for N+1 and 2N+1 level output voltage cases: in 2N+1 level case, since the converter switching frequency is doubled, as explained in section 4.4.1.2, the dominant output voltage and current

harmonics are shifted to higher frequency range and decreased in magnitude, giving lower THD values for output voltages and current. S&S-RS method with 2N+1 level output voltage gives the lowest current THD value among all and it is about the half of the best method of N+1 case, which is indeed S&S-RS again. Voltage THD values of direct modulation methods for 2N+1 level case are about 0.8 times that of N+1 level case and CR method with 2N+1 level output voltage gives the lowest voltage THD value among all. For N+1 level PSCB method, current THD value is twice and voltage THD value is three times that of 2N+1 level case. On the other hand, since the circulating current contained noteworthy components on/around carrier frequency for 2N+1 level case, the ac component of circulating currents are higher significantly. This has leaded to an increase in total arm currents, so does the conduction losses of the converter. Consequently, a decrease in the efficiencies is seen, except for S&S-RS method. For the S&S-RS method, the conduction loss decreased for the 2N+1 case because of the reduction of the dc component, resulting in a minor increase in the efficiency. S&S-RS method with N+1 level output voltage gives the lowest circulating current ac component. It is about one fourth of the best method in 2N+1 level case, which is S&S-RS again. For PSCB method, it is 3.5 times higher for 2N+1 level case, compared to N+1 level case. The submodule capacitor voltage ripple is a little bit higher for 2N+1 case, as a result of the increasing ac component of the circulating current. PSCB method with N+1 level output voltage gives the lowest submodule capacitor voltage ripple; but except CR method, all the values of methods are in the range of 9.06% and 9.67%. S&S-RS method with 2N+1 level output voltage gives the highest efficiency among all, but the efficiency range for all the methods is not broad, the difference is 0.13% for the least efficient and the most efficient methods.

Table 7.13 Simulation results numerical data for both N+1 and 2N+1 level output voltage, full load

		N+1 Level Output Voltage				2N+1 Level Output Voltage			
		Direct Modulation			Phase-shifted carrier based control	Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		5.03	5.01	4.80	8.25	3.97	3.93	3.84	4.15
Line-to-line voltage THD (%)		5.02	5.01	4.78	8.23	3.98	3.92	3.81	4.19
Current (i_l) THD (%)		2.76	2.00	2.34	4.04	1.69	1.06	2.11	1.49
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		9.56	9.39	26.35	9.06	9.67	9.40	26.72	9.16
Circulating current ($i_{circ,dc}$) (A)		234.21	234.50	233.95	234.22	234.43	234.46	234.93	234.31
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		3.73	2.31	13.01	2.73	12.16	8.64	15.86	9.39
Arm current (i_p) (A_{rms})		407.73	408.17	425	409.07	412.8	408.34	429.70	407.31
Average switching frequency of phase a upper arm submodules (Hz)	SM1	480	428	434	448	458	435	431	465
	SM2	476	438	432	439	440	443	432	443
	SM3	472	445	433	448	446	437	430	464
	SM4	490	450	433	449	461	451	429	463
	Average of arm	480	440	433	446	451	442	431	459
Efficiency (%)		98.88	98.91	98.88	98.89	98.85	98.92	98.79	98.83

7.3.1.3. Half Rated Power (5MVA) with Unity Load Angle (cos (φ) =1)

7.3.1.4. Case 1: N+1 Output Voltage Levels

i. Direct Modulation, Sort and Select Method

In this simulation case, carrier frequency is tuned as 1350Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.14 K_p and K_i values of S&S method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=6	K_i=84.8	K_p=15.9	K_i=170

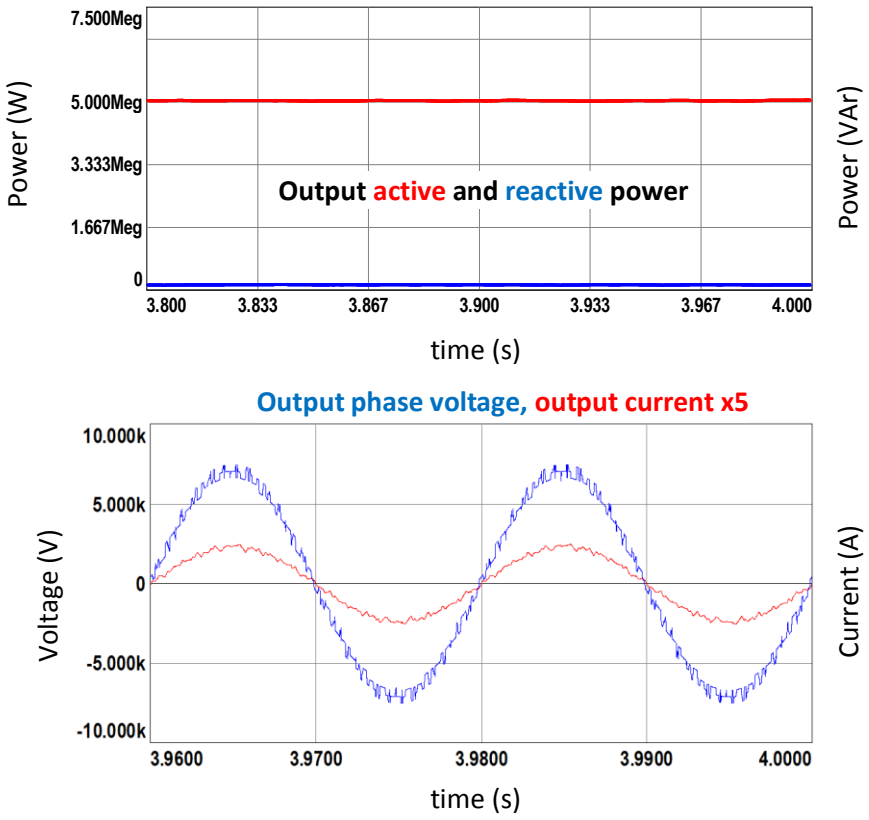


Figure 7.10 Simulation results for S&S method with N+1 level V_{ph}, half load

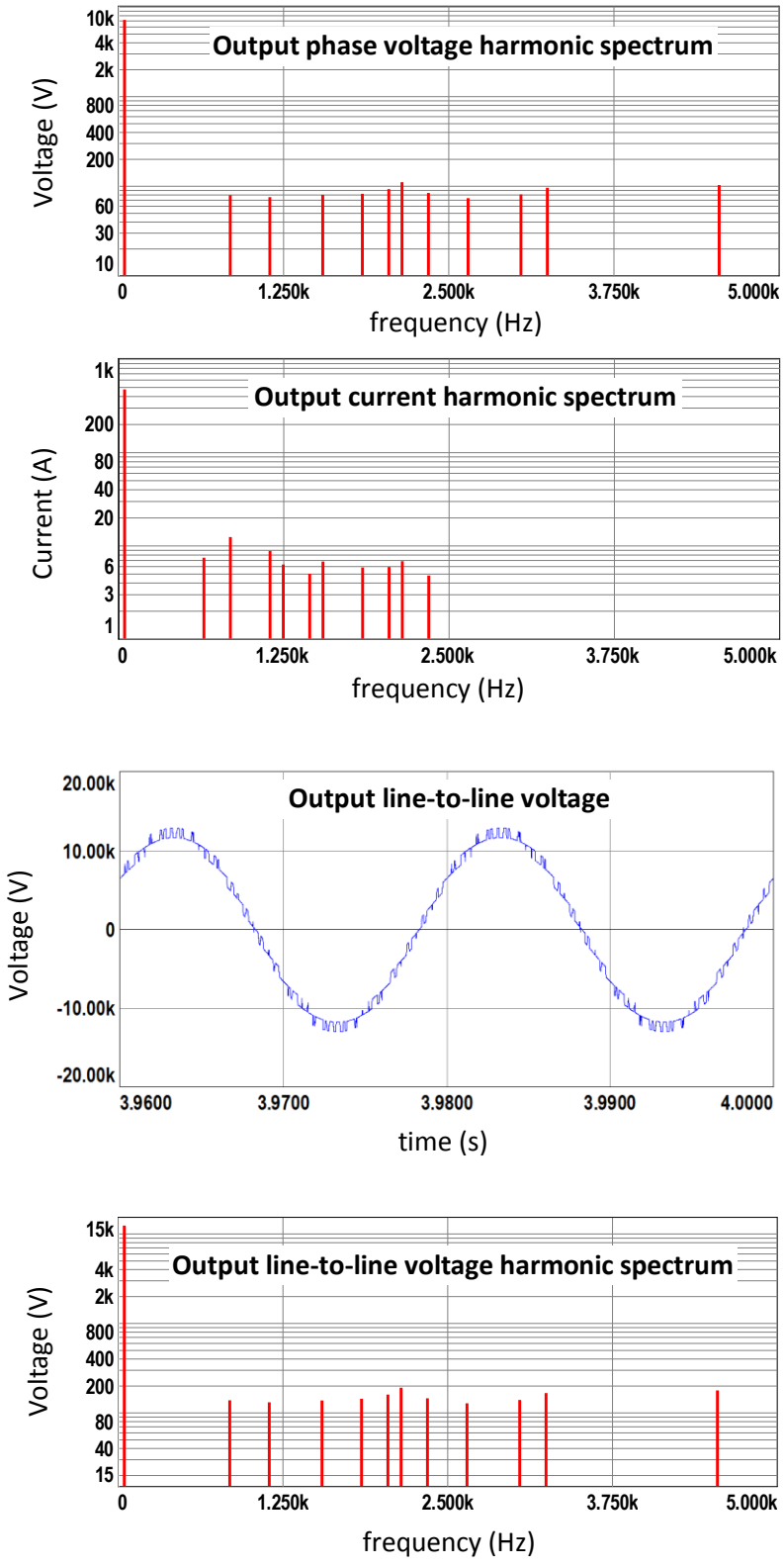


Figure 7.10 (continued) Simulation results for S&S method with N+1 level V_{ph}, half load

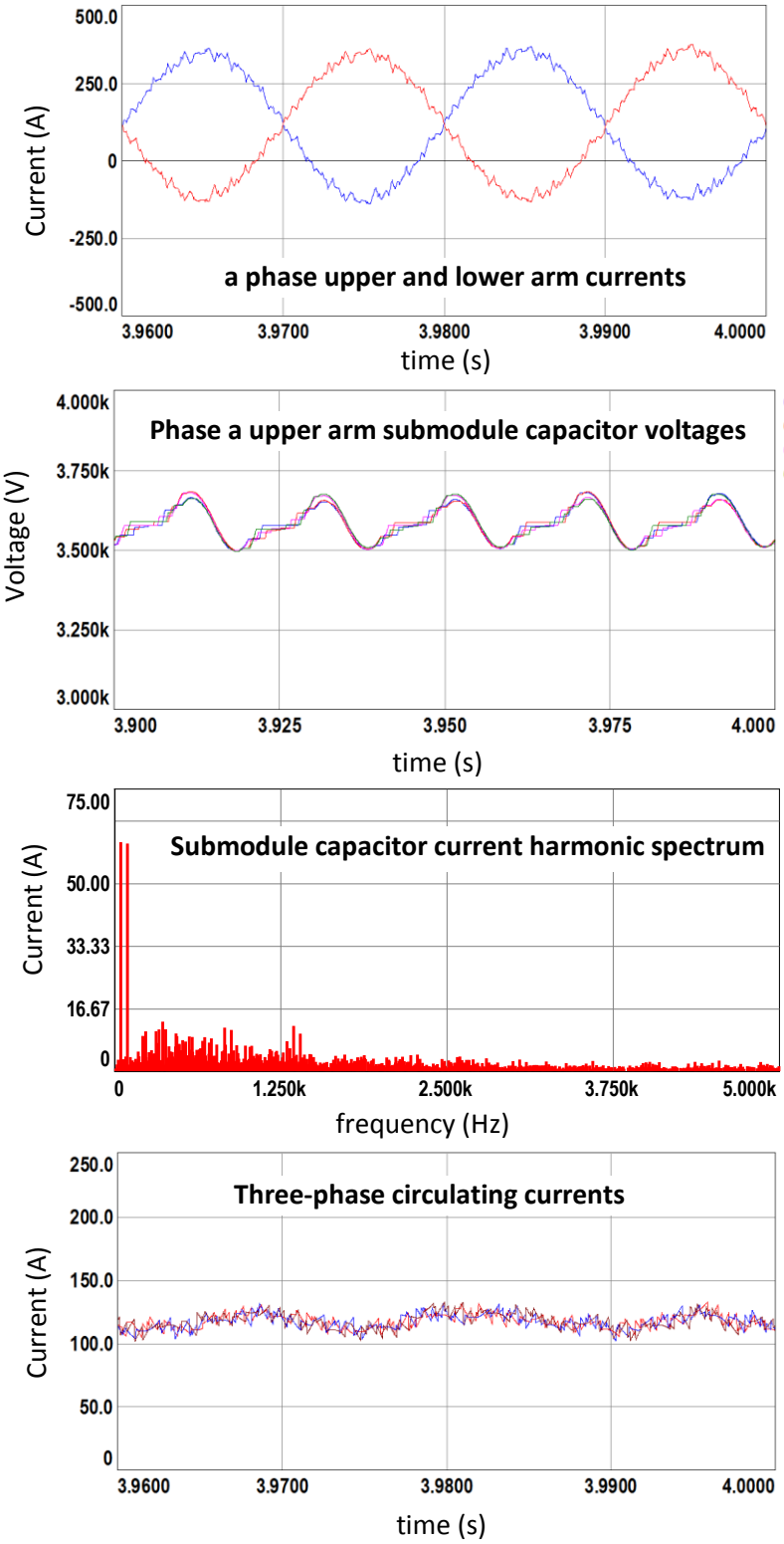


Figure 7.10 (continued) Simulation results for S&S method with N+1 level V_{ph}, half load

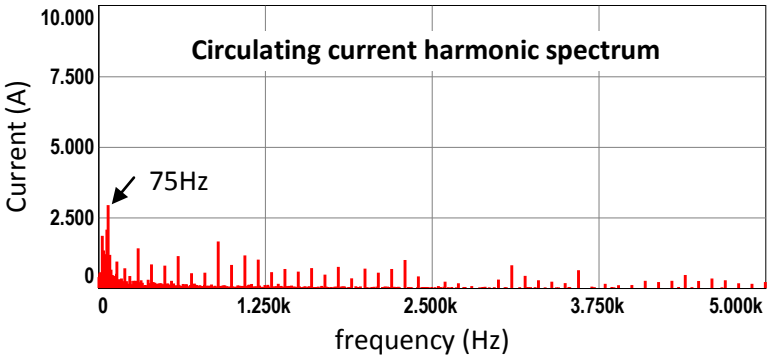


Figure 7.10 (continued) Simulation results for S&S method with N+1 level V_{ph}, half load

In Figure 7.10, the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so does the arm current is halved. The harmonic distortion of output voltage and especially current waveforms increased compared to full load case. Also, a dominant sub-harmonic at 75Hz emerged in circulating current for this case, while the dominant circulating current harmonic is the sixth harmonic for full load case. Numerical results of the simulation are listed in Table 7.18.

ii. Direct Modulation, Sort and Select with Reduced Count of Switching Method

Table 7.15 K_p and K_i values of S&S-RS method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

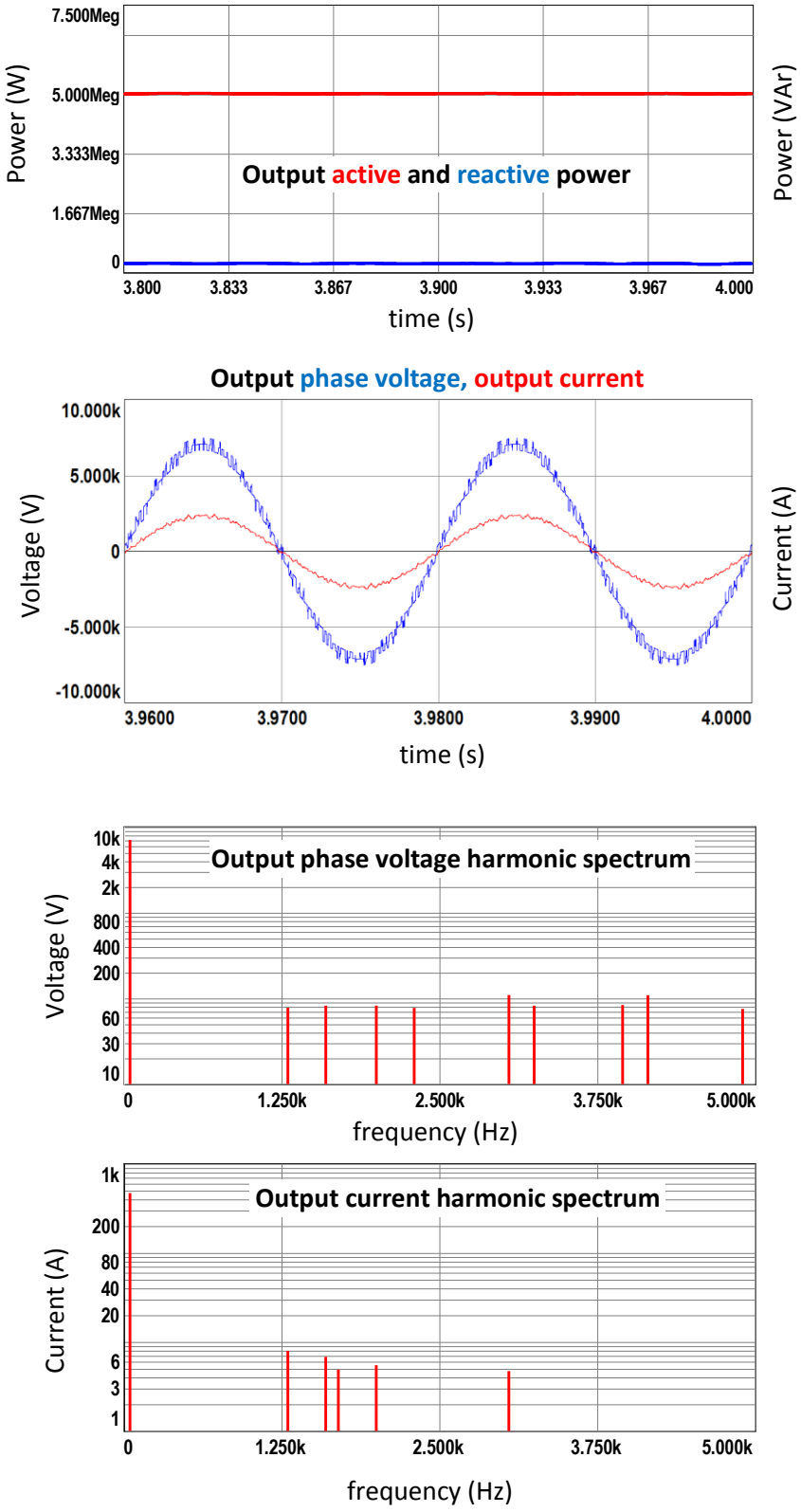


Figure 7.11 Simulation results for S&S-RS method with N+1 level V_{ph}, half load

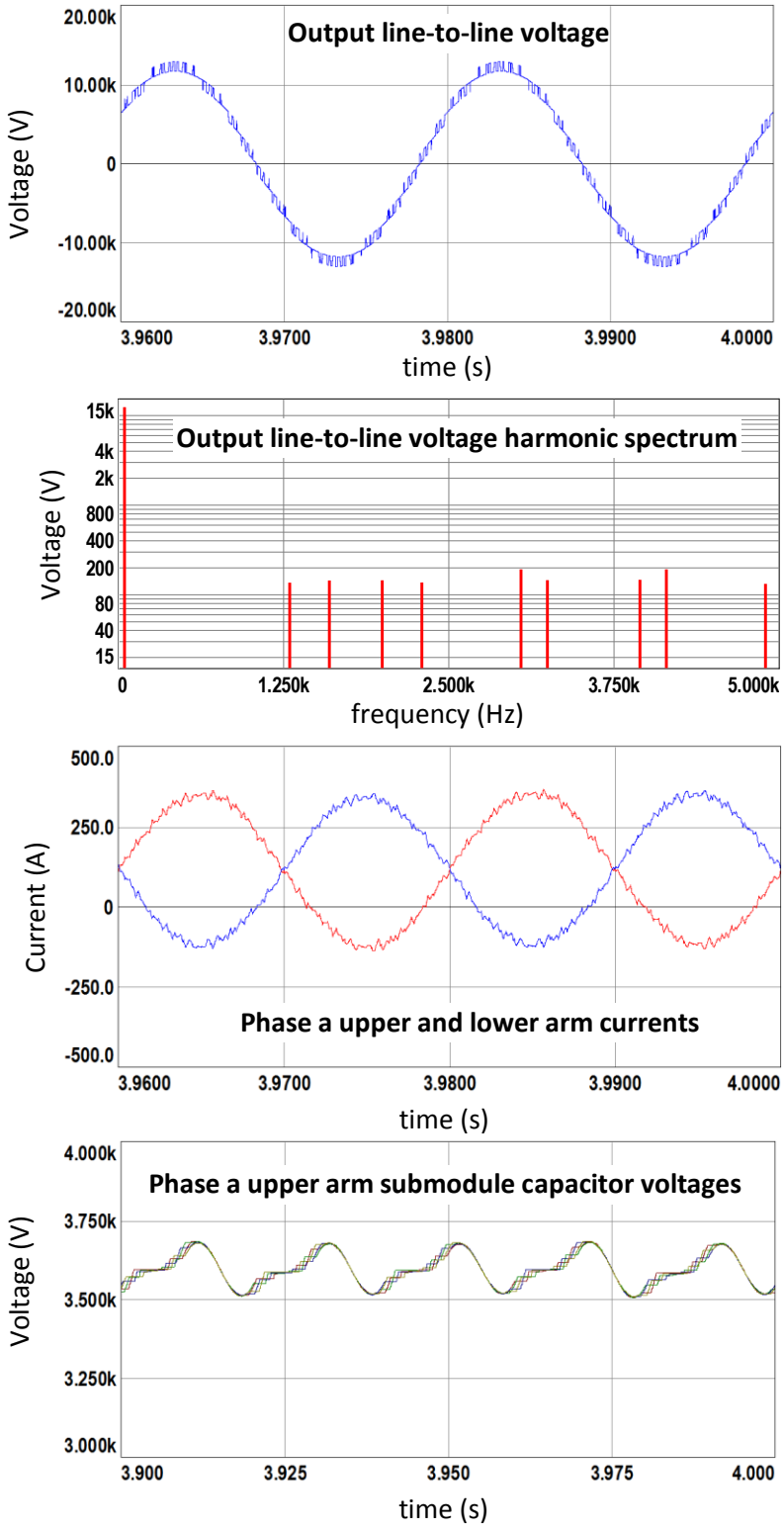


Figure 7.11 (continued) Simulation results for S&S-RS method with N+1 level V_{ph}, half load

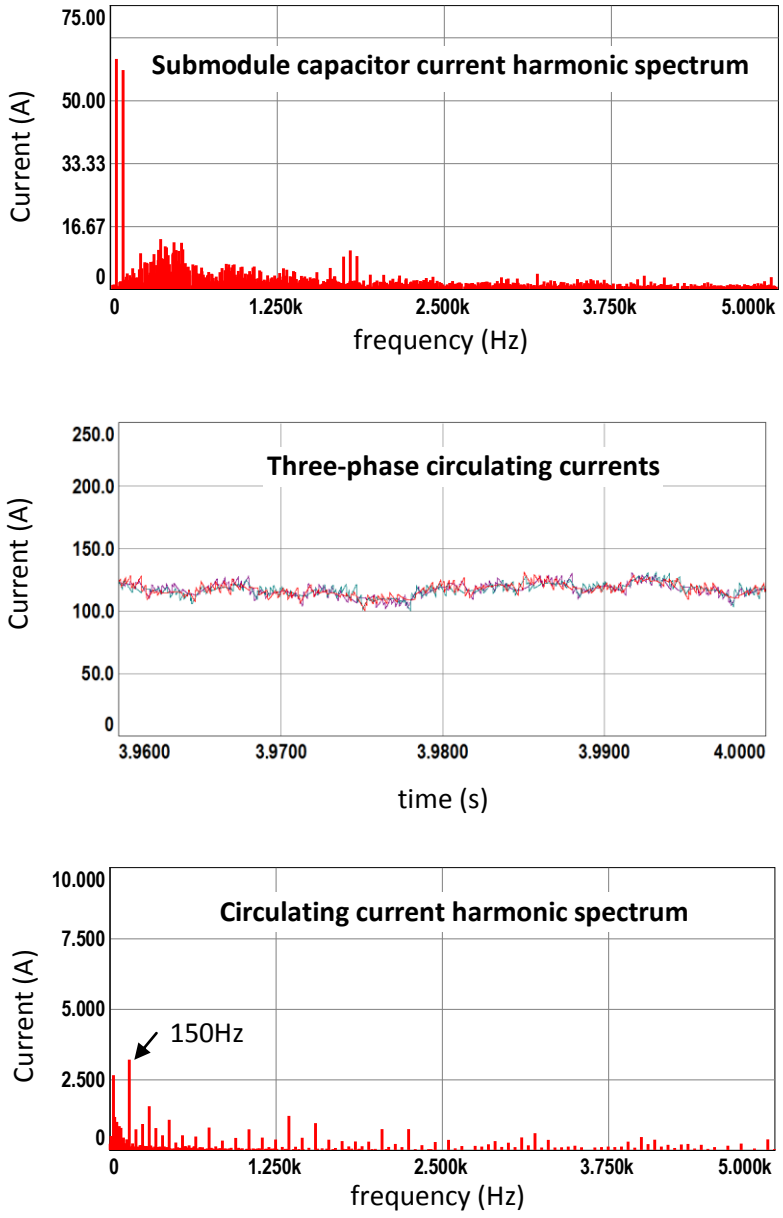


Figure 7.11 (continued) Simulation results for S&S-RS method with N+1 level V_{ph}, half load

In Figure 7.11, the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so does the arm current is halved. The harmonic distortion of output voltage and especially

current waveforms increased compared to full load case. Numerical results of the simulation are listed in Table 7.18.

iii. Direct Modulation, Carrier Rotation Method

In this simulation case, carrier frequency is tuned as 1950Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.16 K_p and K_i values of CR method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

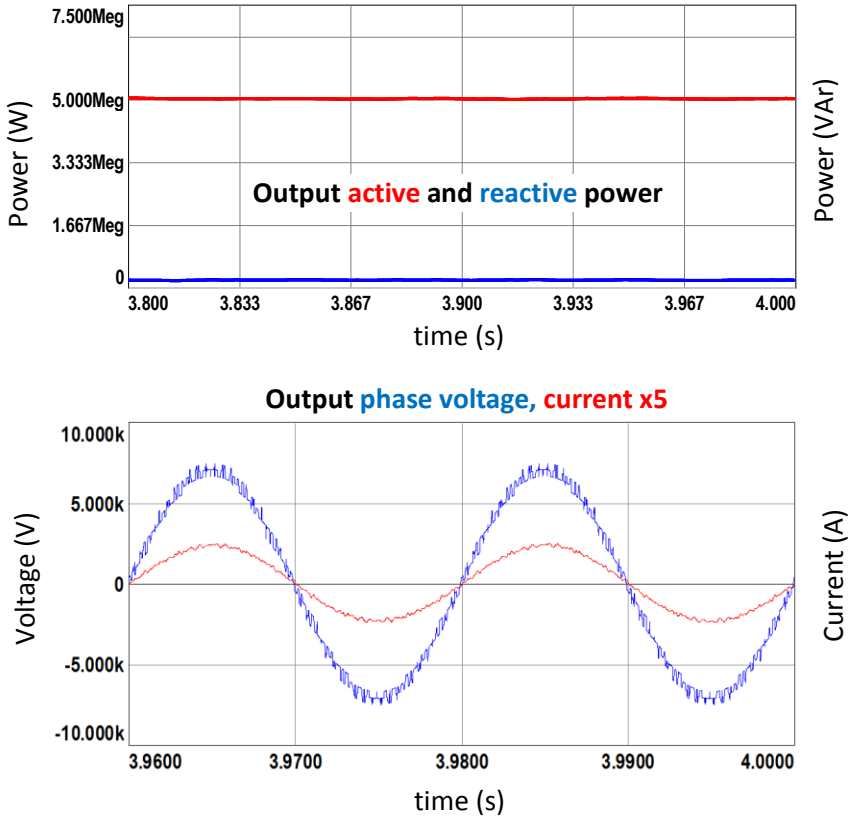


Figure 7.12 Simulation results for CR method with N+1 level V_{ph}, half load

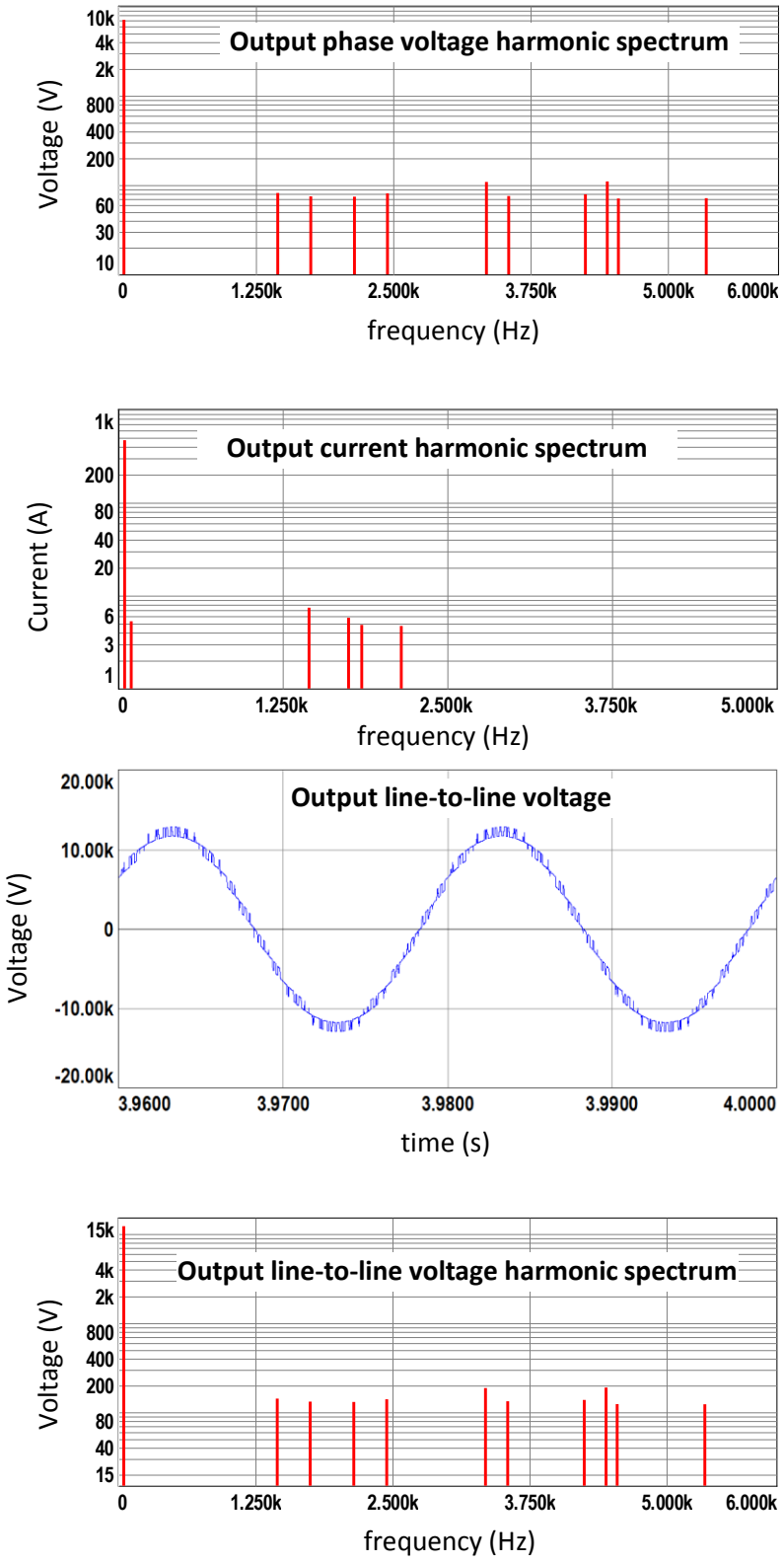


Figure 7.12 (continued) Simulation results for CR method with N+1 level V_{ph}, half load

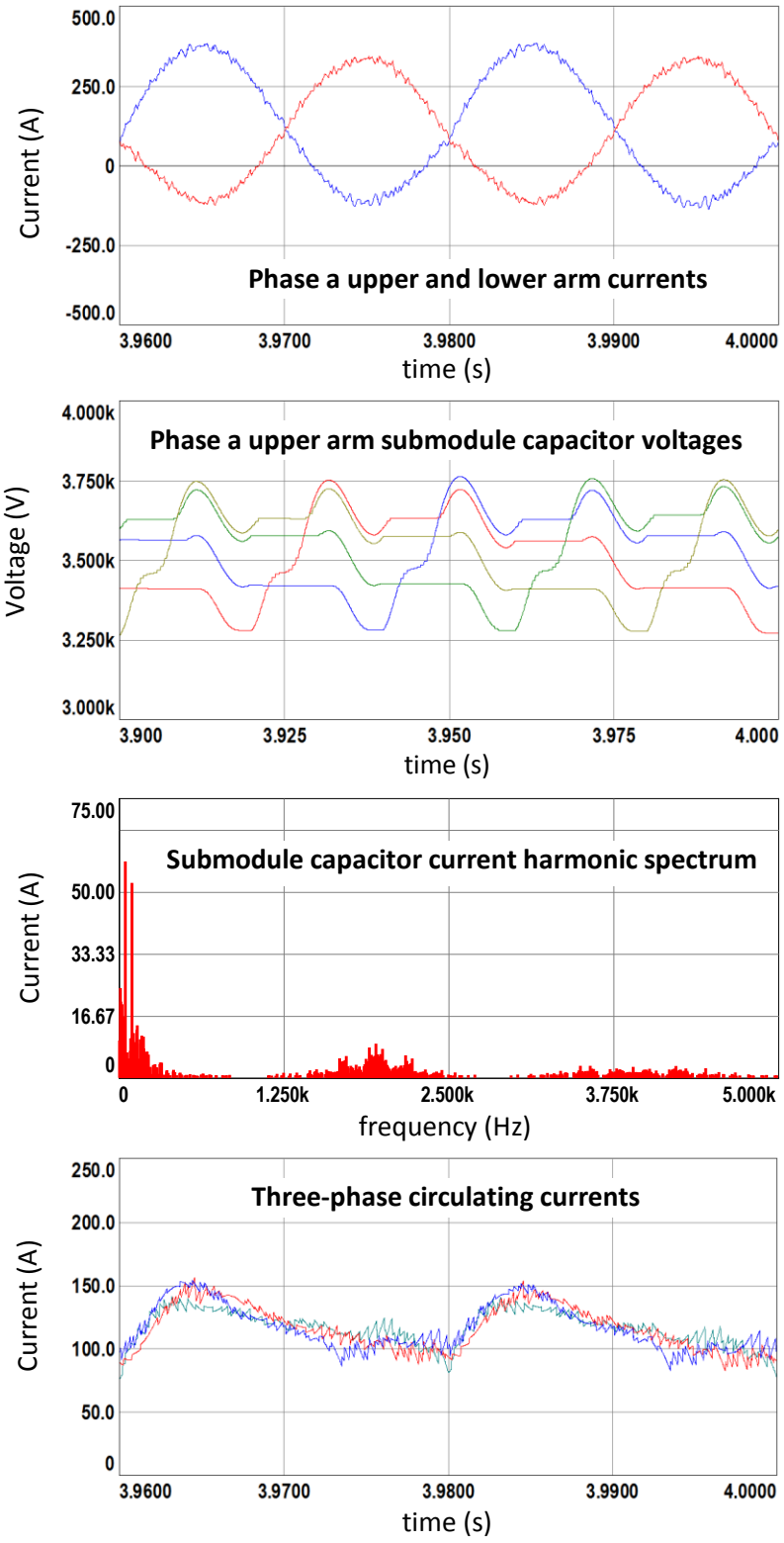


Figure 7.12 (continued) Simulation results for CR method with N+1 level V_{ph}, half load

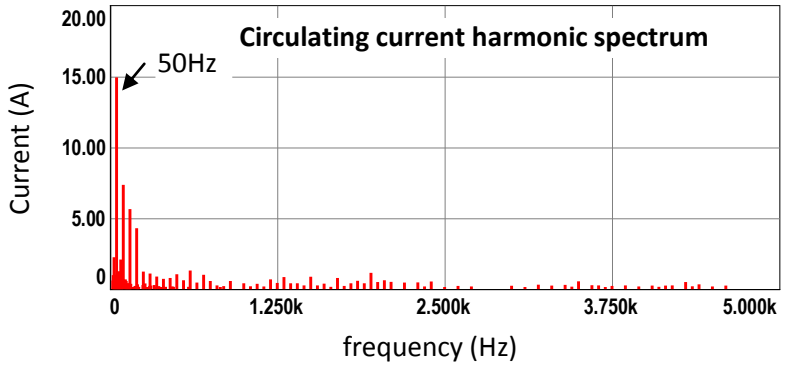


Figure 7.12 (continued) Simulation results for CR method with N+1 level V_{ph}, half load

In Figure 7.12, the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so as the arm current is halved. The harmonic distortion of output voltage and especially current waveforms increased compared to full load case. Numerical results of the simulation are listed in Table 7.18.

iv. Phase-shifted Carrier Based Control

In this simulation case, carrier frequency is tuned as 470Hz in order not to have an integer multiple of fundamental frequency [65] and to converge the total count of switching per leg to 450Hz±5%.

Table 7.17 K_p and K_i values of PSCB method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=8	K_i=113	K_p=5.3	K_i=56.5

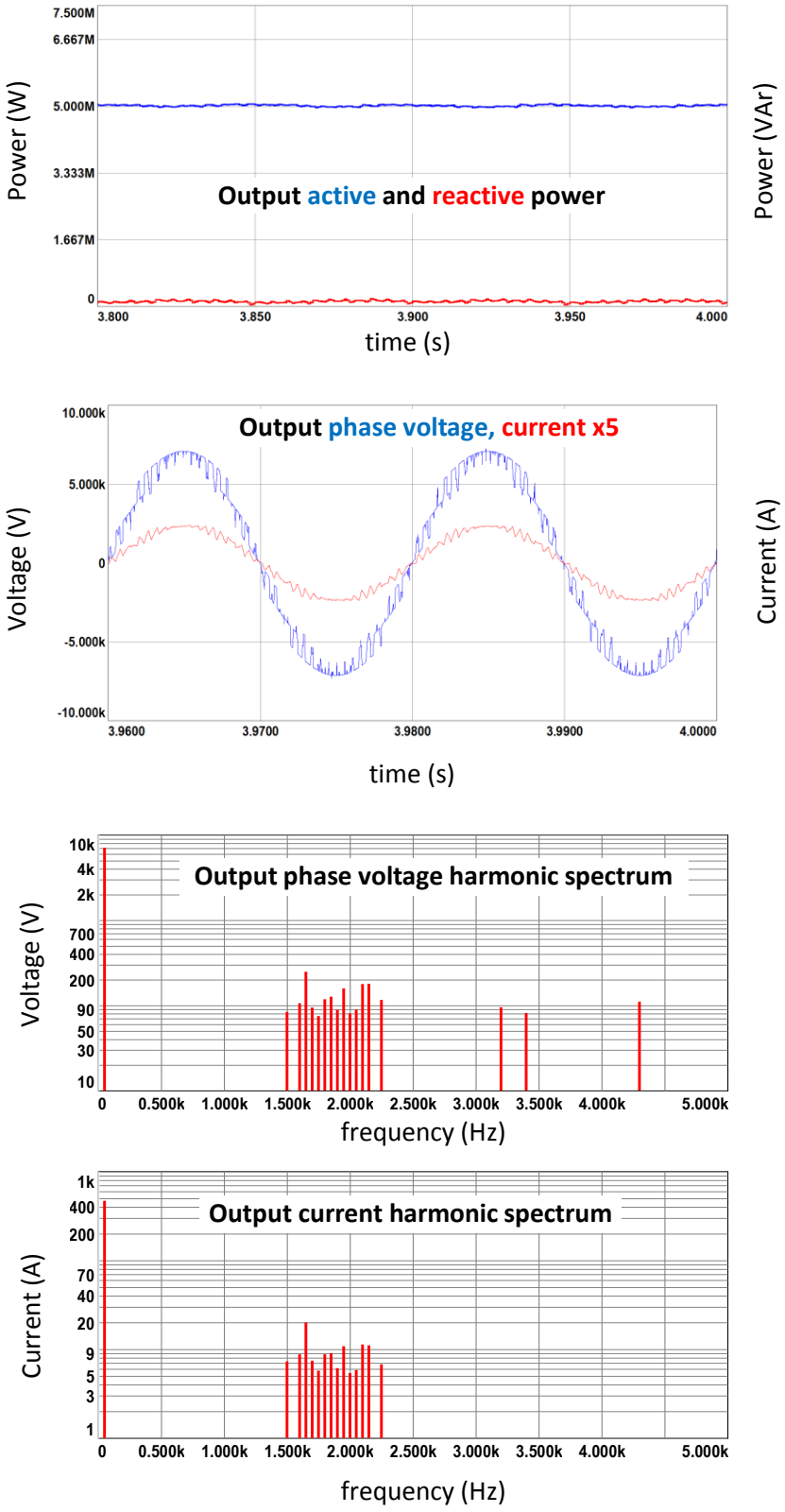


Figure 7.13 Simulation results for PSCB method with N+1 level V_{ph}, half load

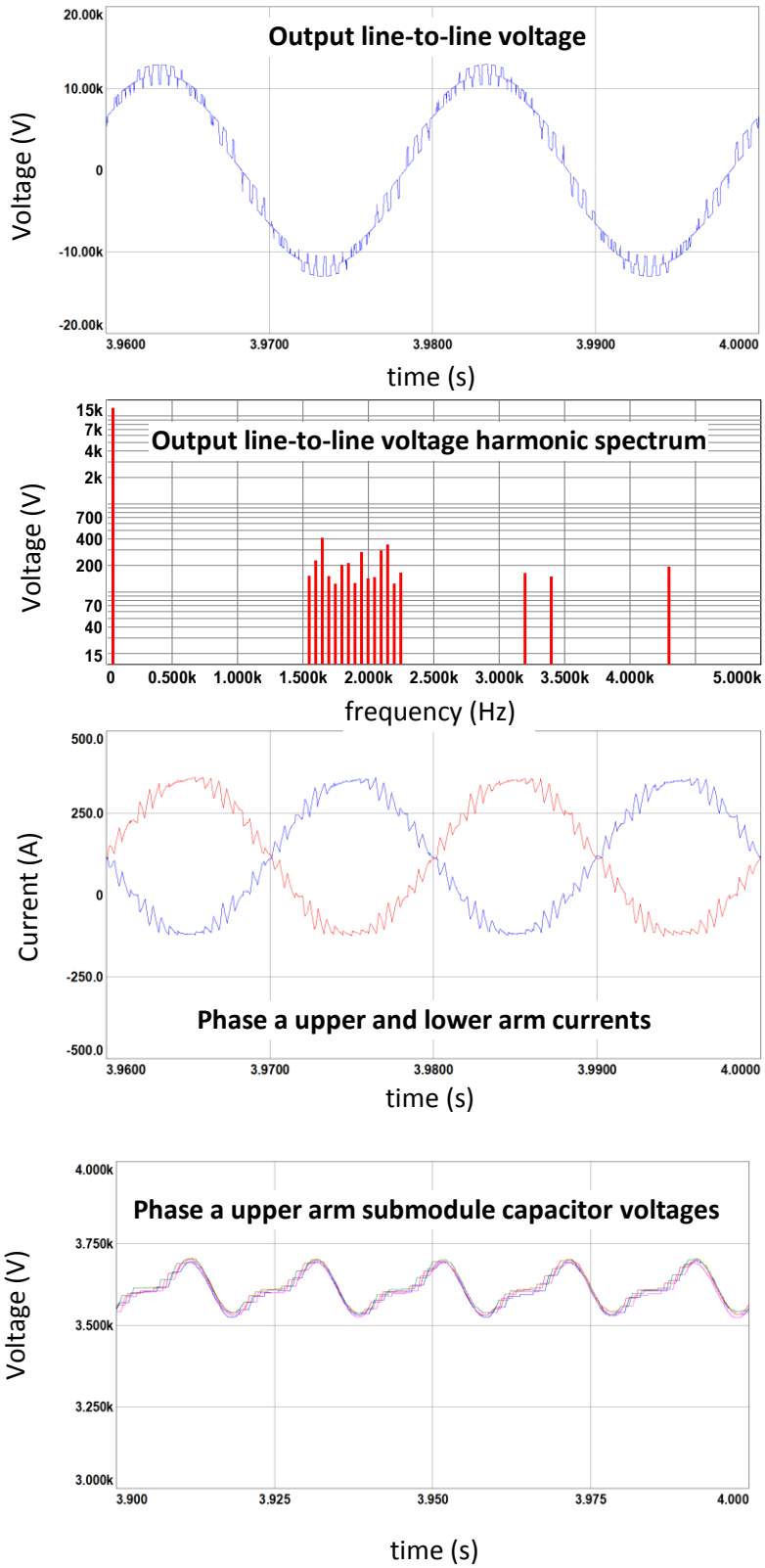


Figure 7.13 (continued) Simulation results for PSCB method with N+1 level V_{ph}, half load

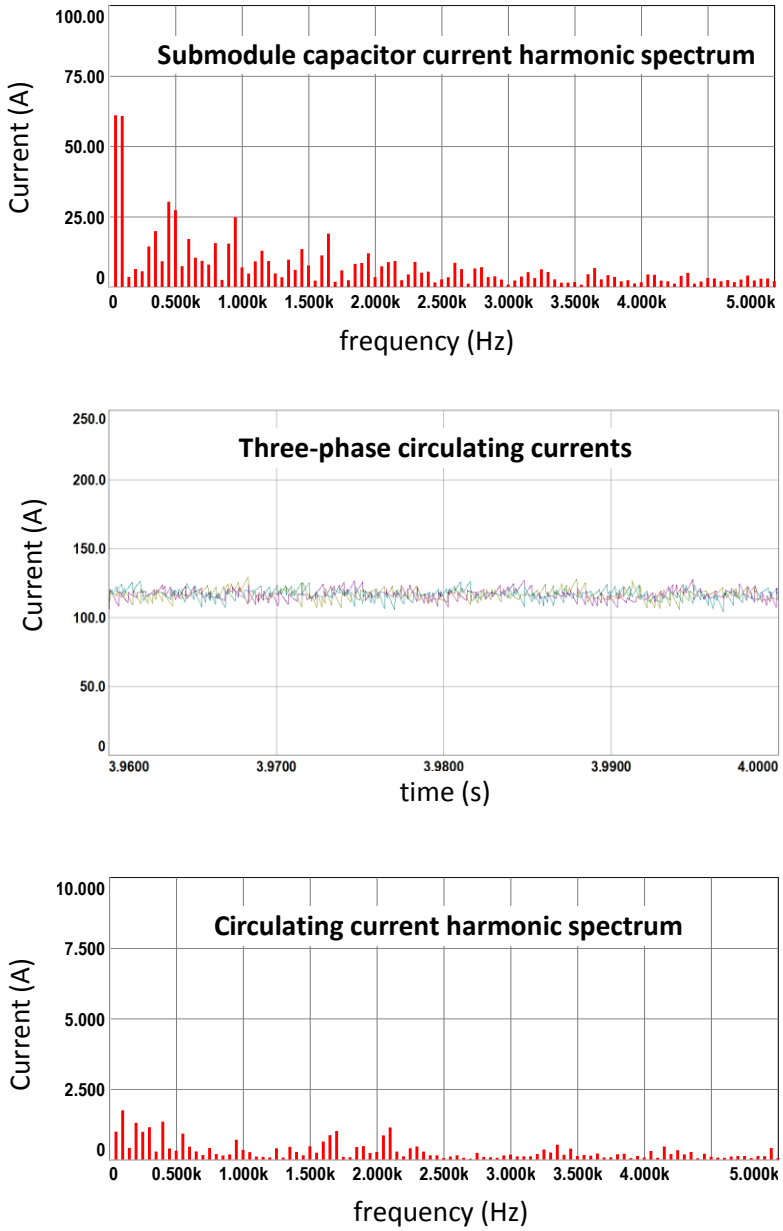


Figure 7.13 (continued) Simulation results for PSCB method with N+1 level V_{ph}, half load

In Figure 7.13, the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so does the arm current is halved. The harmonic distortion of output voltage and chiefly current waveforms increased. Numerical results of the simulation are listed in Table 7.18.

Table 7.18 Simulation results numerical data for N+1 level output voltage

		Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		5.23	5.38	5.13	8.58
Line-to-line voltage THD (%)		5.22	5.38	5.13	8.55
Current (i_l) THD (%)		5.31	3.88	3.90	8.16
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		5.26	4.88	13.62	4.53
Circulating current ($i_{circ,dc}$) (A)		117.04	116.87	116.69	116.57
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		4.43	3.88	11.73	2.89
Arm current (i_p) (A_{rms})		203.93	203.89	214.67	204.38
Average switching frequency of phase a upper arm submodules (Hz)	SM1	490	450	459	473
	SM2	485	463	460	470
	SM3	477	457	459	474
	SM4	465	445	458	479
	Average of arm	479	454	459	474
Efficiency (%)		98.79	98.99	98.80	98.88

The results shown by Table 7.18 are similar to full load case, Table 7.7. CR method has the lowest output voltage harmonic distortion, but it still has the unbalance problem in the capacitor voltages and arm currents. Voltage THD values of direct modulation methods are roughly 0.6 times that of PSCB method. S&S-RS method is superior to other methods in terms of output current harmonic distortion and efficiency. Current THD of PSCB method is about twice of S&S-RS. PSCB method has lower submodule capacitor voltage ripple (about 0.35% lower than S&S-RS method) and circulating current ac component (about 3/4 of S&S-RS). The efficiencies of all the methods decreased compared to full load case, except S&S-RS method. The conduction loss of S&S-RS method for half load case has decreased to one third of full load conduction loss, while for the other methods the conduction losses are halved approximately. As a result, S&S-RS method has the highest efficiency for half load case.

7.3.1.5. Case 2: 2N+1 Output Voltage Levels

i. Direct Modulation, Sort and Select Method

In this simulation case, carrier frequency is tuned as 1350Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.19 K_p and K_i values of S&S method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=6	K_i=84.8	K_p=15.9	K_i=170

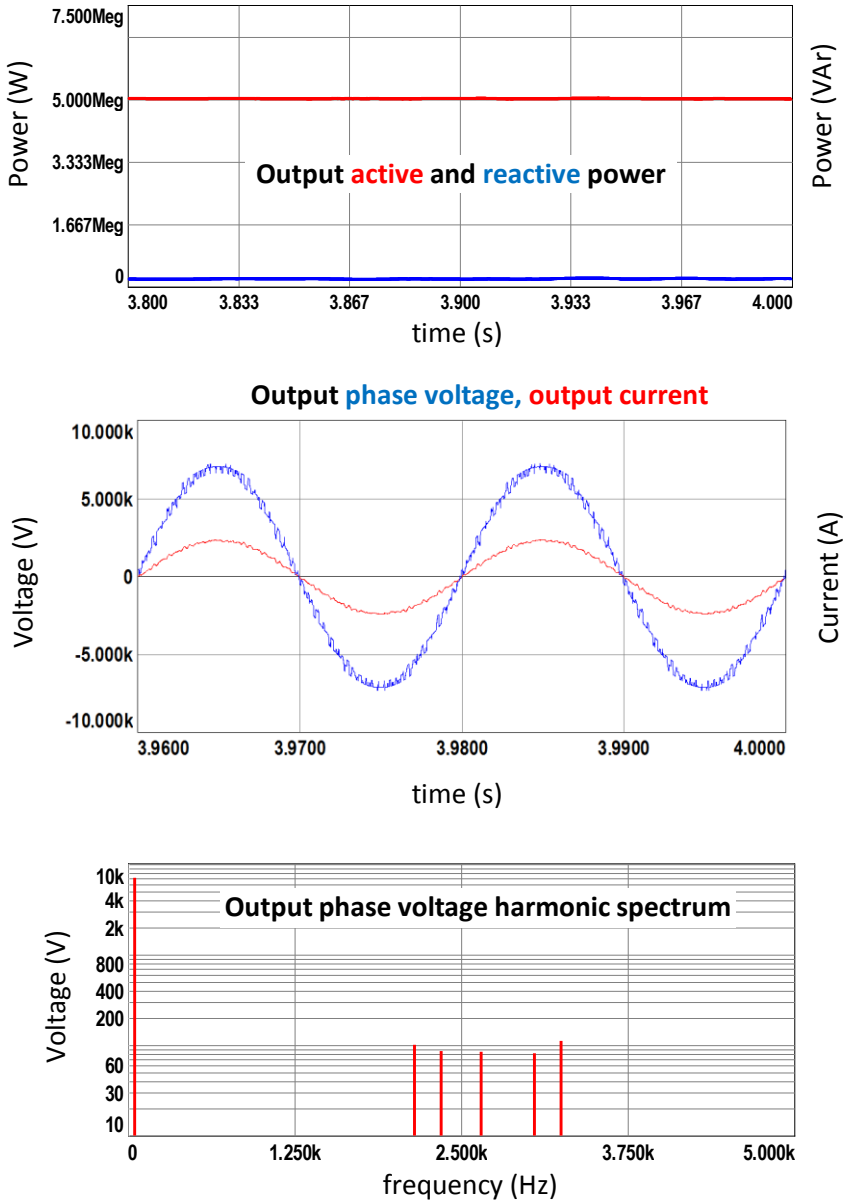


Figure 7.14 Simulation results for S&S method with 2N+1 level V_{ph}, half load

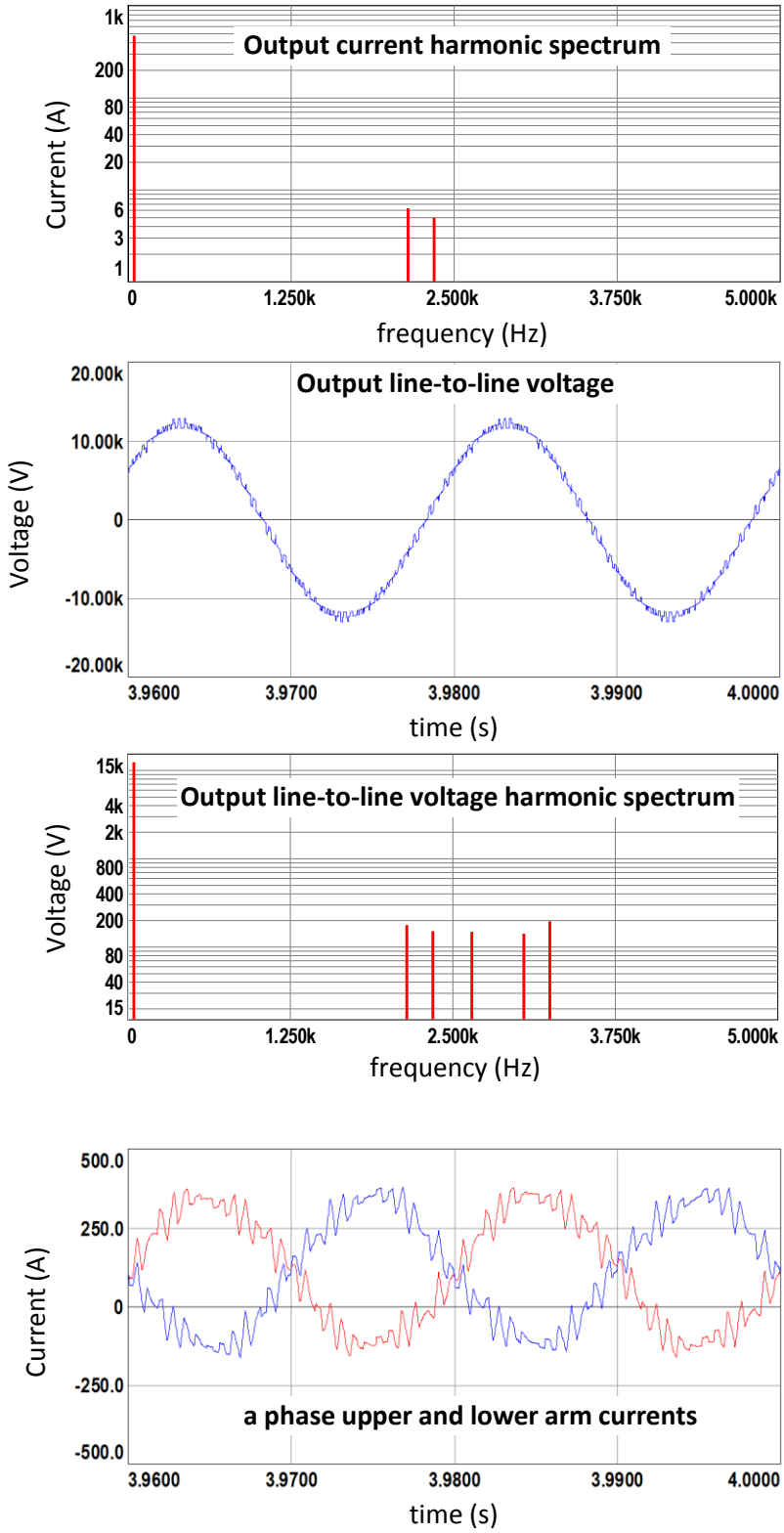


Figure 7.14 (continued) Simulation results for S&S method with 2N+1 level V_{ph}, half load

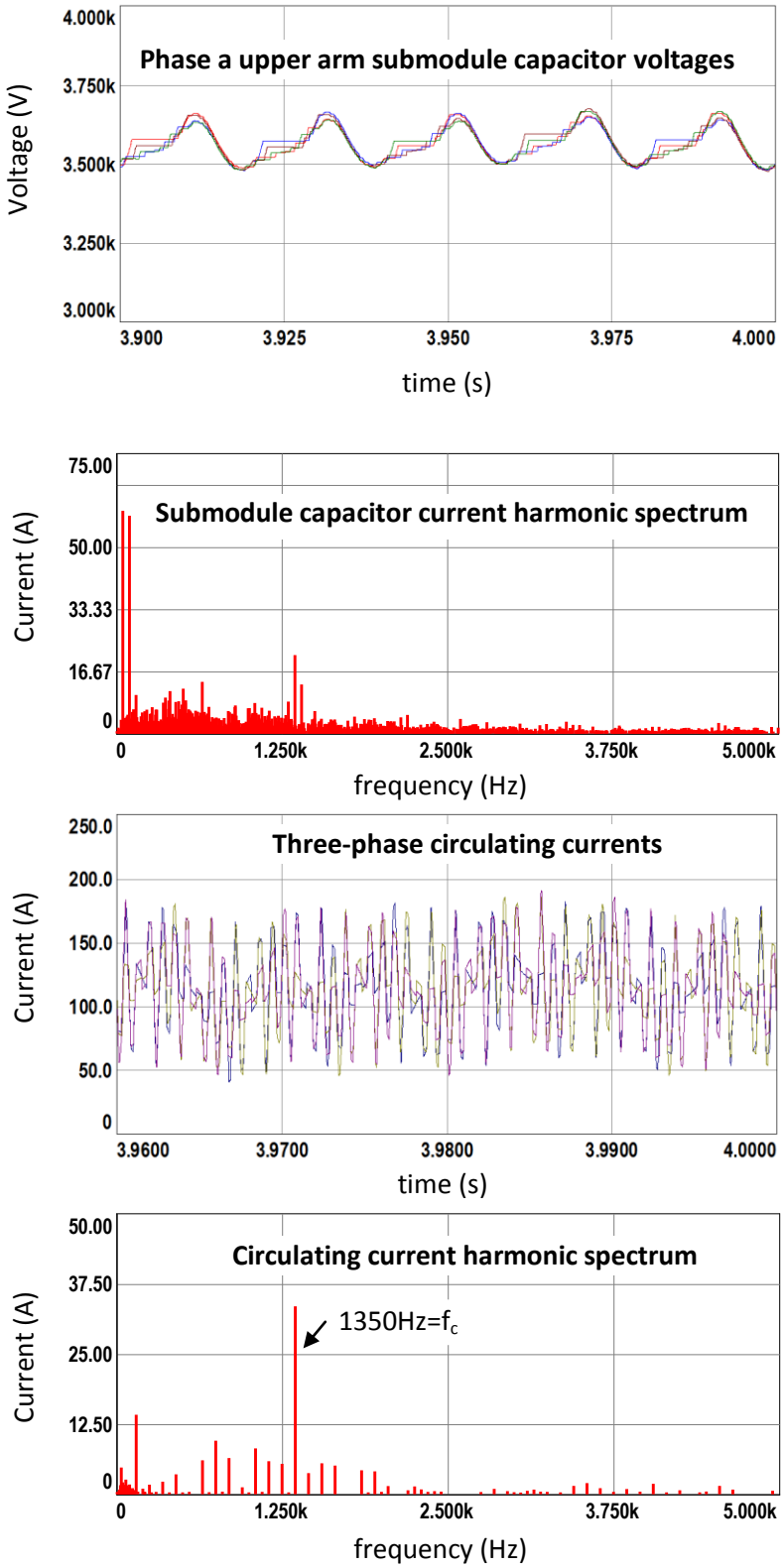


Figure 7.14 (continued) Simulation results for S&S method with 2N+1 level V_{ph}, half load

In Figure 7.14 the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so as the arm current is halved. The harmonic distortion of output voltage and especially current waveforms increased compared to full load case. Numerical results of the simulation are listed in Table 7.23.

ii. Direct Modulation, Sort and Select with Reduced Count of Switching Method

Table 7.20 K_p and K_i values of S&S-RS method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

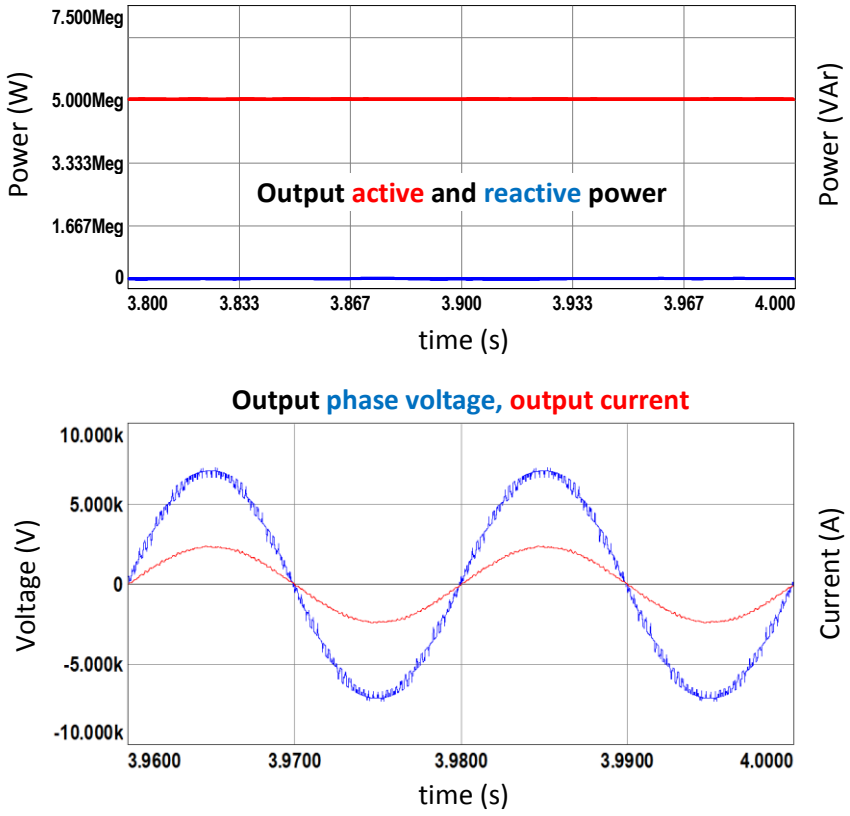


Figure 7.15 Simulation results for S&S-RS method with 2N+1 level V_{ph}, half load

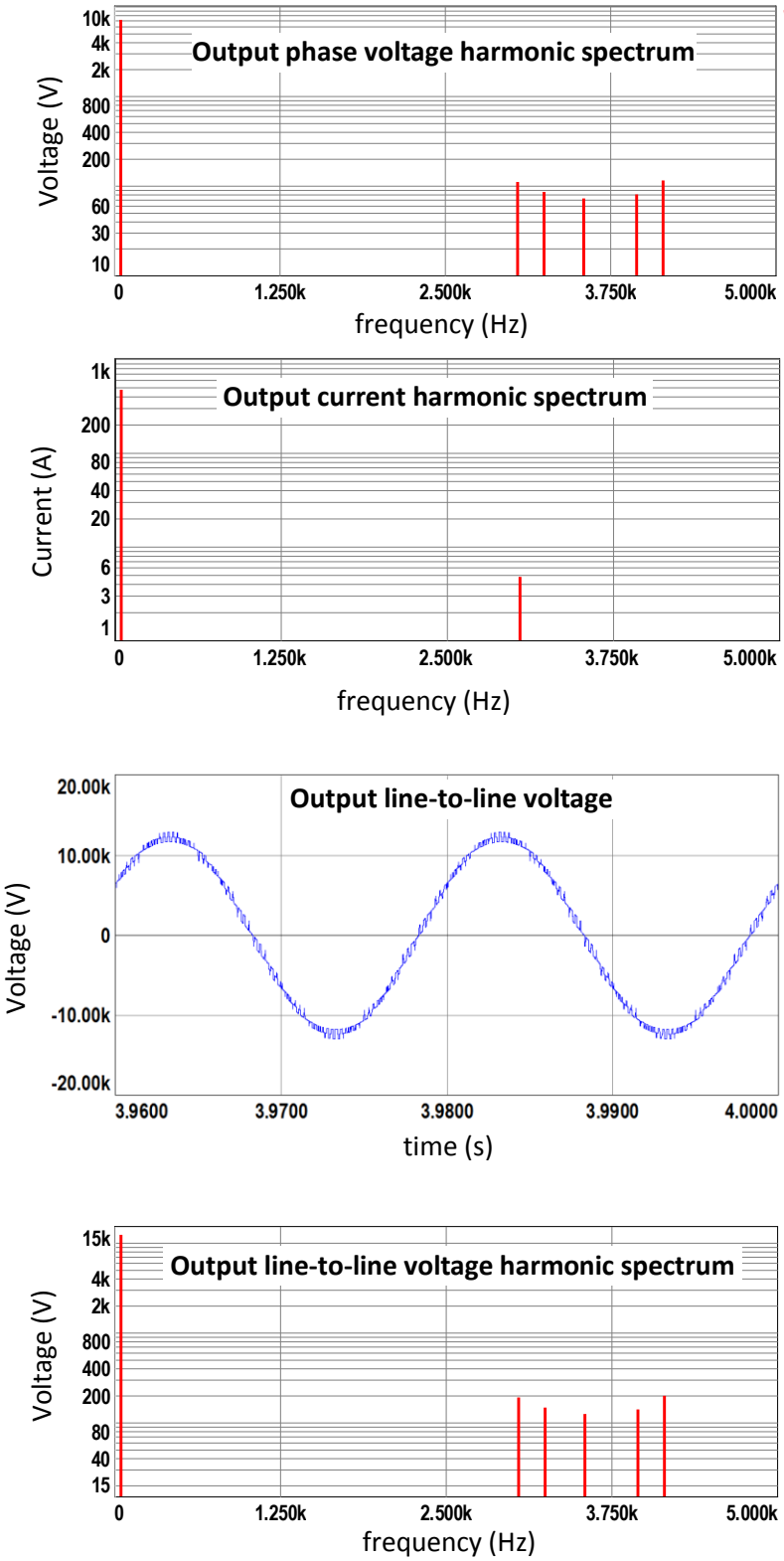


Figure 7.15 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, half load

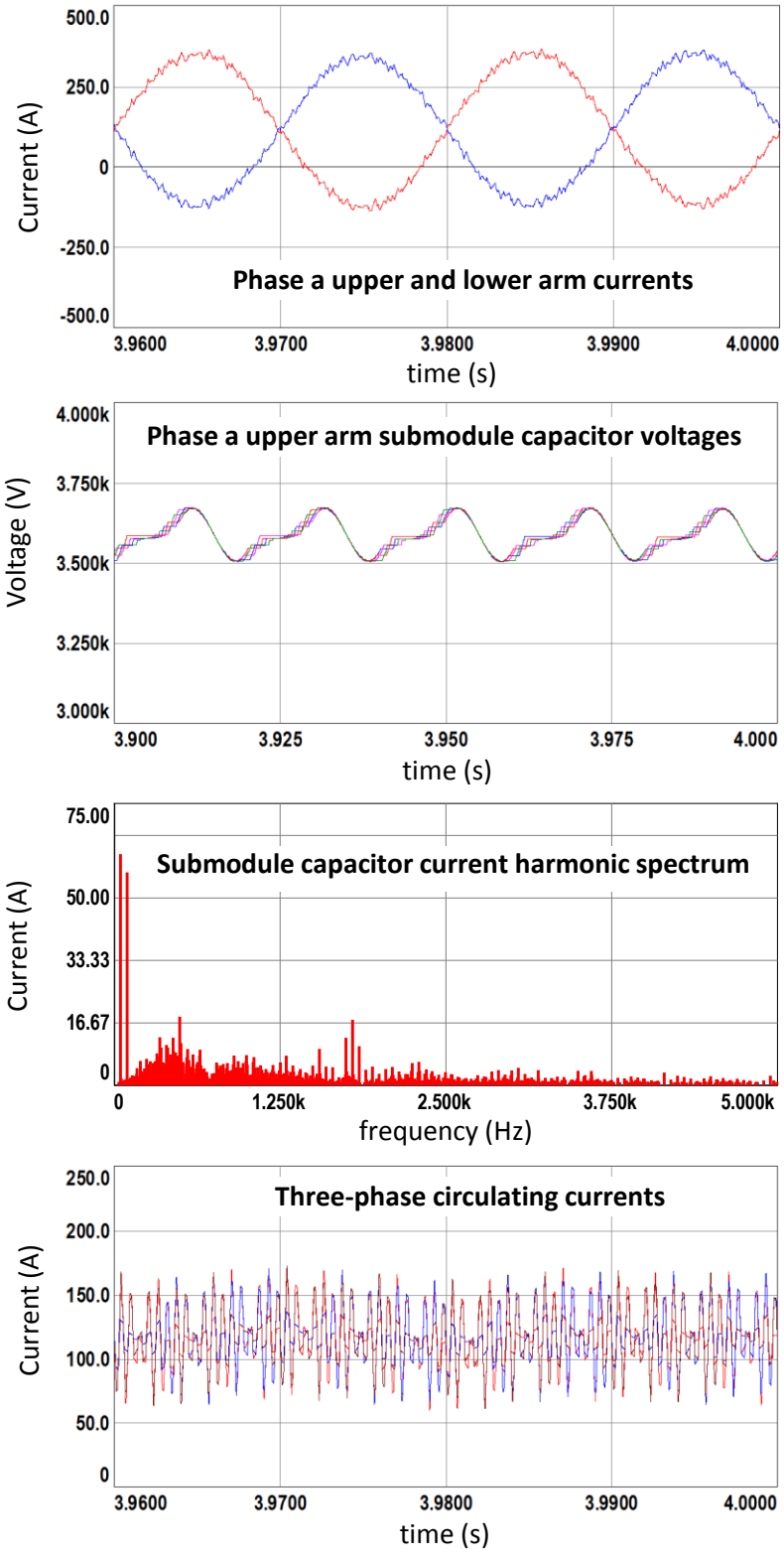


Figure 7.15 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, half load

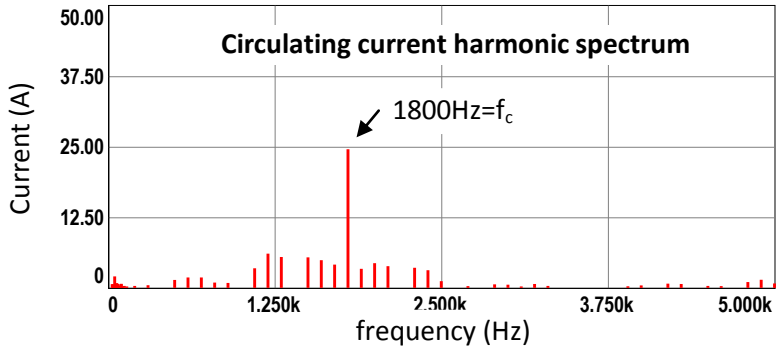


Figure 7.15 (continued) Simulation results for S&S-RS method with 2N+1 level V_{ph}, half load

In Figure 7.15, the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so as the arm current is halved. The harmonic distortion of output voltage and especially current waveforms increased compared to full load case. Numerical results of the simulation are listed in Table 7.23.

iii. Direct Modulation, Carrier Rotation Method

In this simulation case, carrier frequency is tuned as 1950Hz in order to converge the total count of switching per leg to 450Hz±5%.

Table 7.21 K_p and K_i values of CR method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=4	K_i=56.54	K_p=10.63	K_i=565

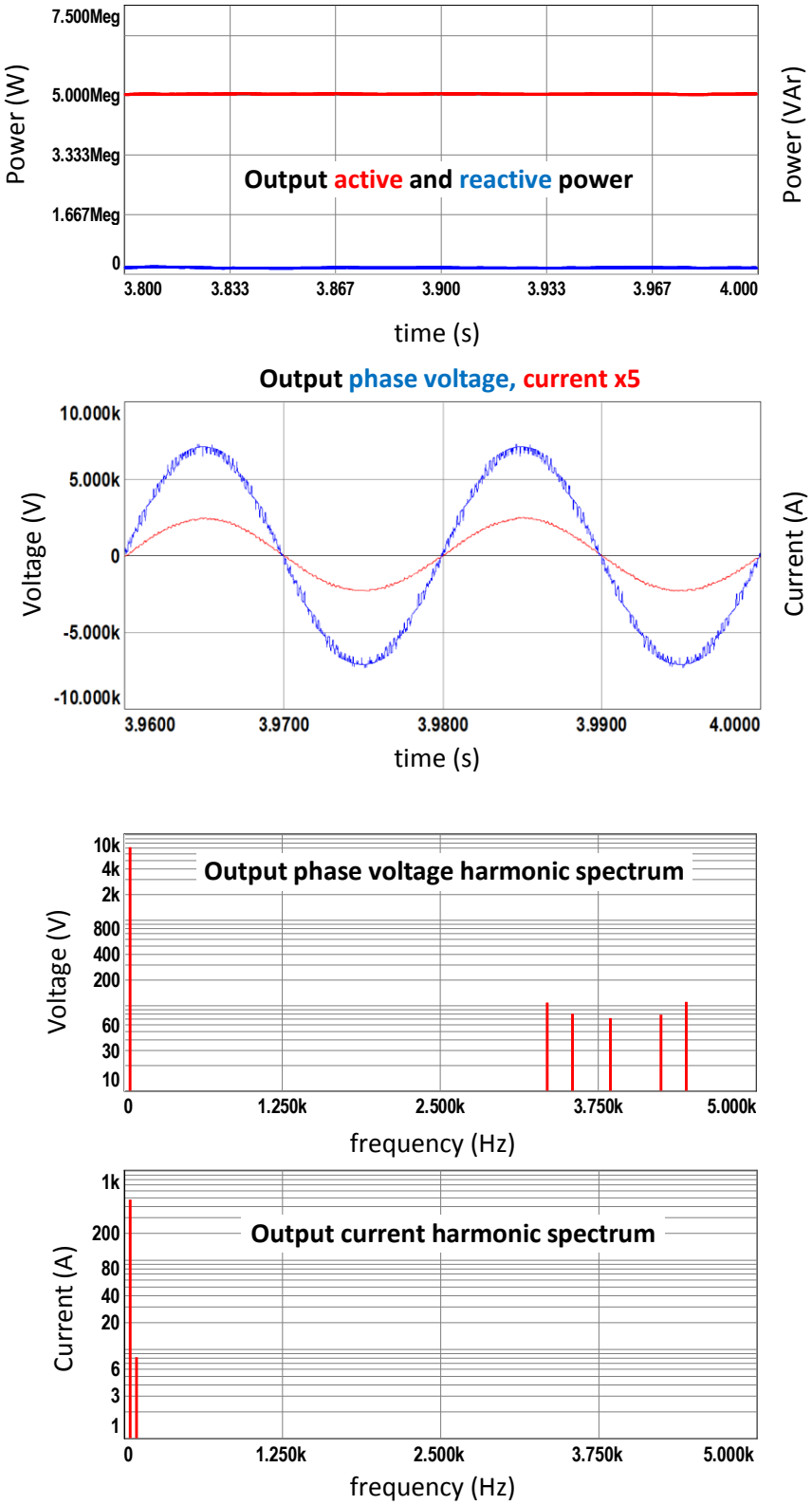


Figure 7.16 Simulation results for CR method with 2N+1 level V_{ph}, half load

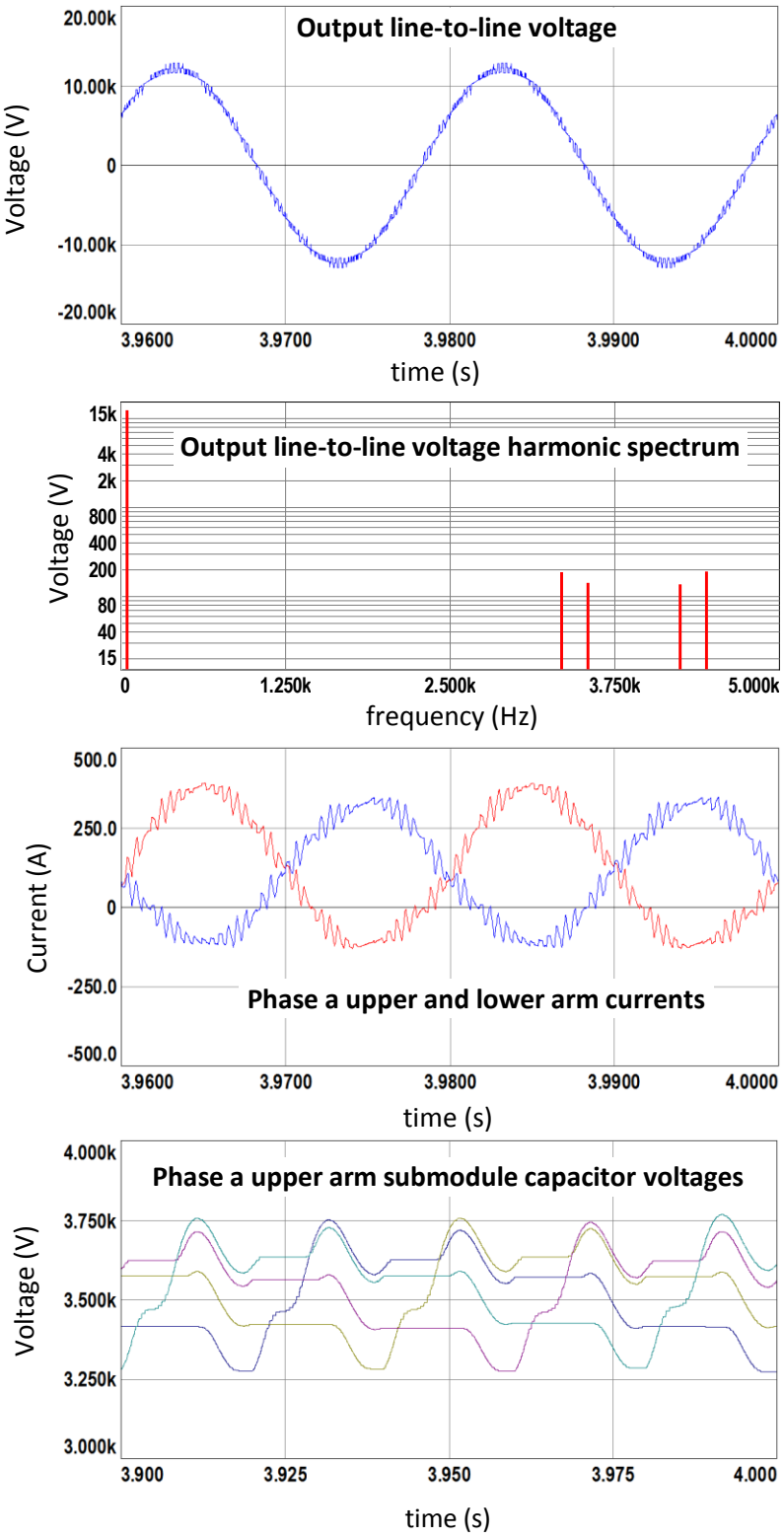


Figure 7.16 (continued) Simulation results for CR method with 2N+1 level V_{ph}, half load

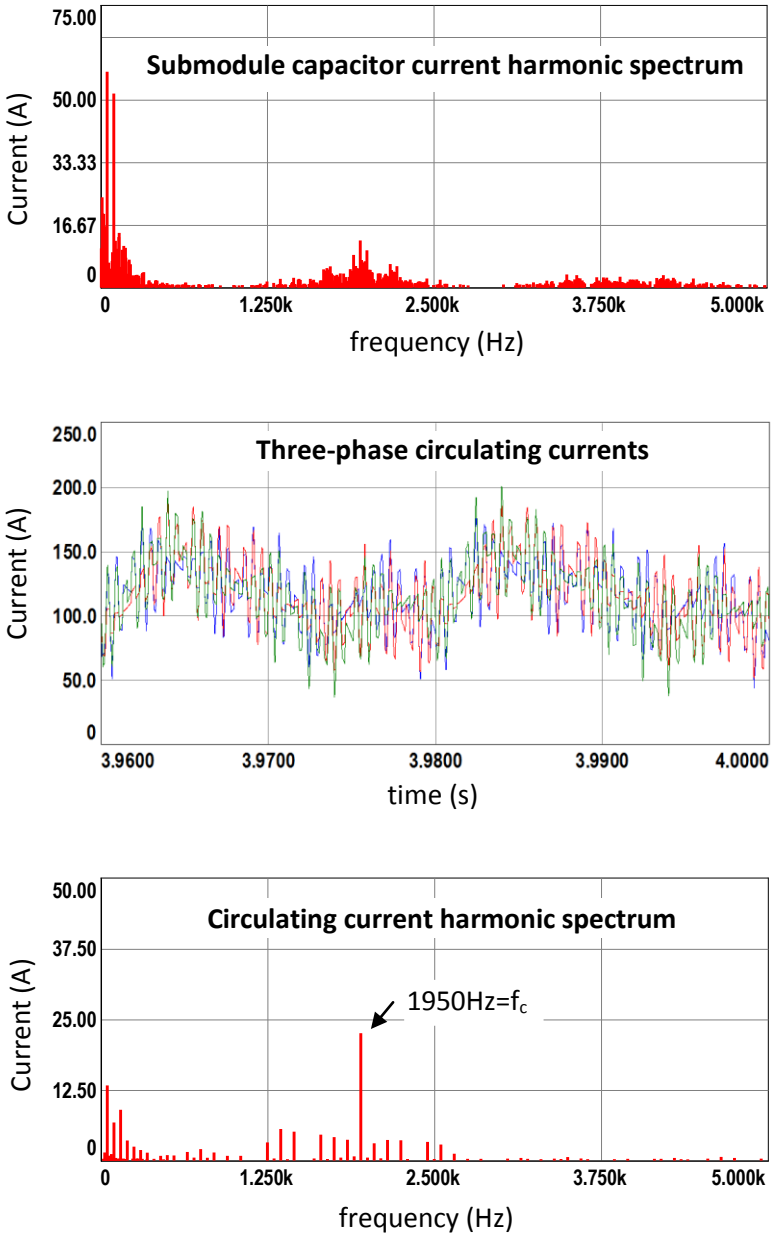


Figure 7.16 (continued) Simulation results for CR method with 2N+1 level V_{ph}, half load

In Figure 7.16 the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so as the arm current is halved. The harmonic distortion of output voltage and especially current waveforms

increased compared to full load case. Numerical results of the simulation are listed in Table 7.23.

iv. Phase-shifted Carrier Based Control

In this simulation case, carrier frequency is tuned as 430Hz in order not to have an integer multiple of fundamental frequency [65] and to converge the total count of switching per leg to 450Hz±5%.

Table 7.22 K_p and K_i values of PSCB method

Output Power Control		Circulating current 2nd Harmonic Supp.	
K_p=8	K_i=113	K_p=5.3	K_i=56.5

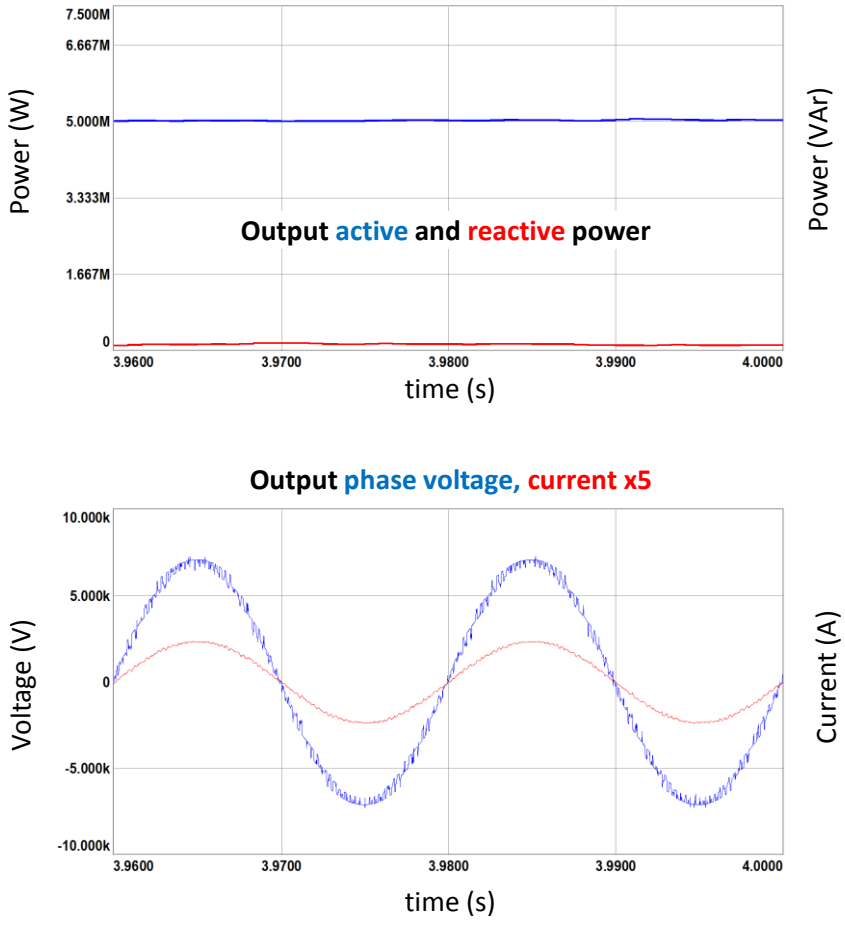


Figure 7.17 Simulation results for PSCB method with 2N+1 level V_{ph}, half load

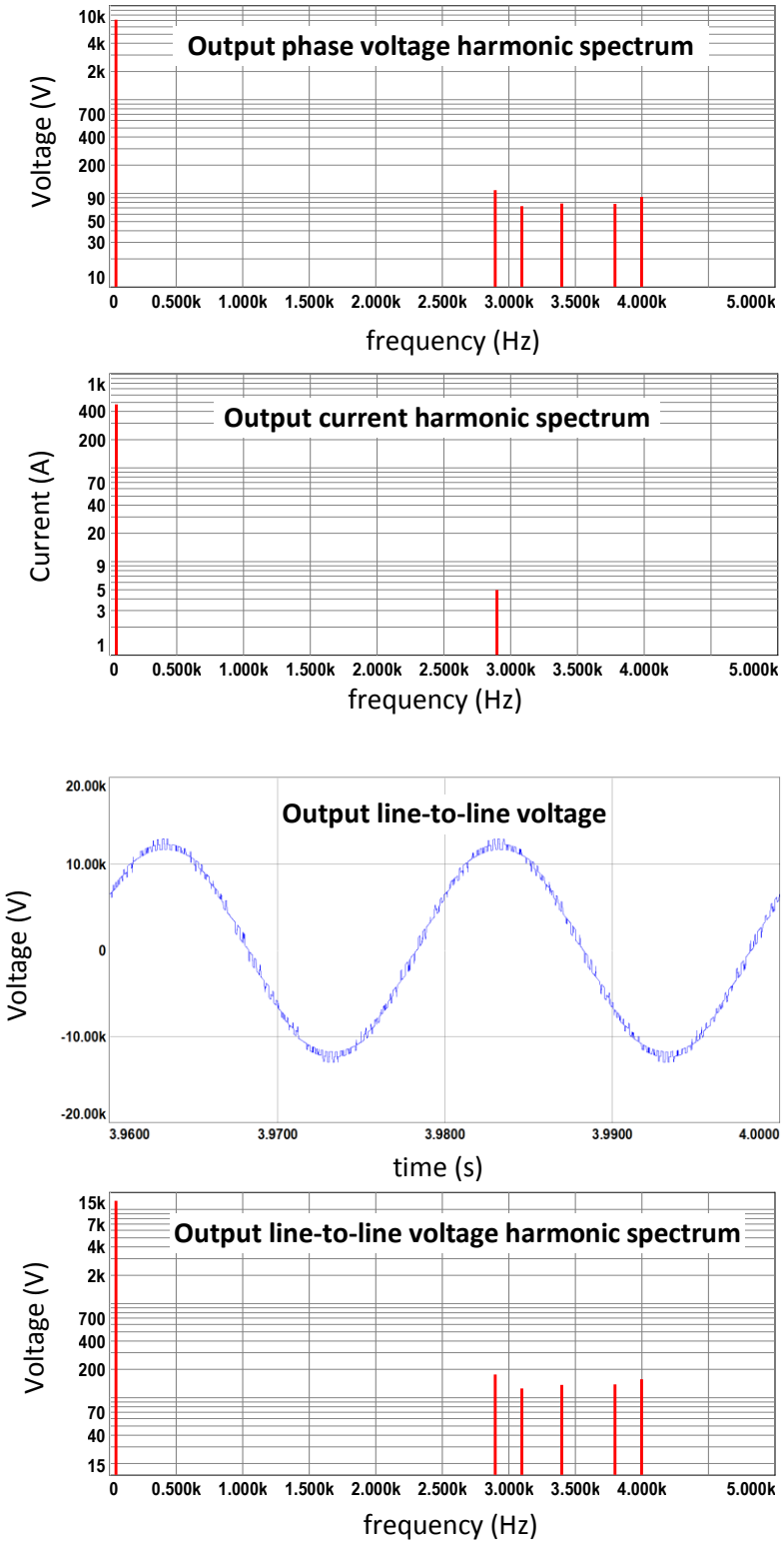


Figure 7.17 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, half load

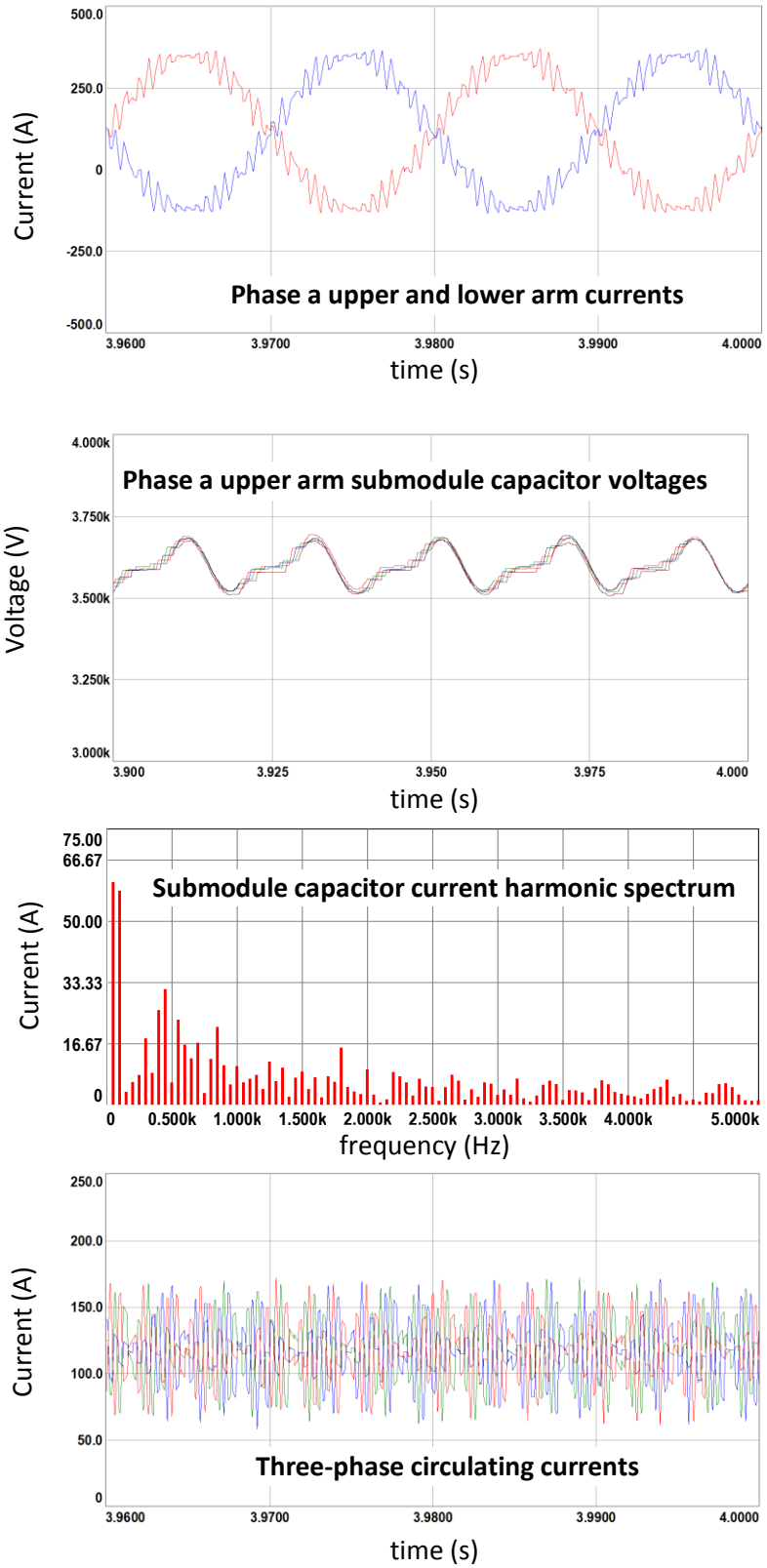


Figure 7.17 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, half load

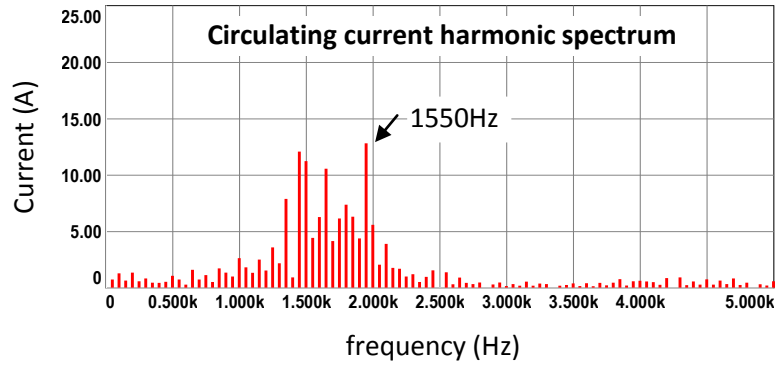


Figure 7.17 (continued) Simulation results for PSCB method with 2N+1 level V_{ph}, half load

In Figure 7.17 the results are similar to the full load case. Differently, the submodule capacitors voltage ripple decreased, since the output power, so as the arm current is halved. The harmonic distortion of output voltage and especially current waveforms increased compared to full load case. Numerical results of the simulation are listed in Table 7.23.

Table 7.23 Simulation results numerical data for 2N+1 level output voltage

		Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		4.11	4.08	4.00	4.19
Line-to-line voltage THD (%)		4.13	4.07	3.97	4.18
Current (i_l) THD (%)		2.89	2.09	2.75	2.37
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		5.01	4.71	13.34	4.65
Circulating current ($i_{circ,dc}$) (A)		116.78	116.80	116.97	116.92
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		26.12	17.76	22.70	18.90
Arm current (i_p) (A_{rms})		206.81	204.97	215.41	204.73
Average switching frequency of phase a upper arm submodules (Hz)	SM1	470	456	451	470
	SM2	450	424	448	484
	SM3	463	462	452	487
	SM4	458	472	449	480
	Average of arm	460	454	450	480
Efficiency (%)		98.44	98.91	98.75	98.74

The results shown by Table 7.23 are similar to full load case, Table 7.12. CR method has the lowest output voltage harmonic distortion, but it still has the unbalance problem in the capacitor voltages and arm currents. The difference in voltage THDs between direct modulation methods and PSCB method diminished. S&S-RS method is superior to other methods in terms of output current harmonic distortion, circulating current ac component magnitude, and efficiency. The current THD of S&S-RS method is 0.9 times that of PSCB method, and 0.7 times that of S&S method. Circulating currents are close to each other for S&S-RS and PSCB methods, while S&S-RS has a small advantage. However, they are about 3/4 of S&S and CR methods. Except CR method, the three other methods have contiguous submodule capacitor voltage ripple. Meanwhile, PSCB method has the lowest submodule capacitor voltage ripple which is 0.06% less than S&S-RS. The arm currents are nearly the same for S&S-RS and PSCB methods. The efficiencies of all the methods decreased compared to full load case, but S&S-RS method has the highest efficiency, again. It is 0.17% higher than PSCB method.

Table 7.24 gives the differences of characteristics for N+1 and 2N+1 level output voltage cases for half load. The results are similar to full load case as in Table 7.13. In 2N+1 level case, since the converter switching frequency is doubled, as explained in section 4.4.1.2, the dominant output voltage and current harmonics are shifted to higher frequency range and decreased in magnitude, giving lower THD values for output voltages and current. S&S-RS method with 2N+1 level output voltage gives the lowest current THD value and it is about half of the best case in N+1 level case, which is indeed S&S-RS again. For direct modulation methods, the voltage THDs of 2N+1 case are about 3/4 of N+1 case. CR method with 2N+1 level output voltage gives the lowest voltage THD value among all. The THD differences between the N+1 and 2N+1 level cases for PSCB are higher compared to direct modulation case. For PSCB method, the current THD in N+1 level case is 3.5 times and voltage THDs are about twice for that of 2N+1 level case values. On the other hand, since the circulating current contained noteworthy components on/around carrier frequency for 2N+1 level case, the ac component of circulating currents are

increased significantly. This has leaded to an increase in total arm currents, so does the conduction losses of the converter. Consequently, decrease in the efficiencies is seen. PSCB method with N+1 level output phase voltage gives the lowest circulating current ac component, and it is about 3/4 times of S&S-RS method. For 2N+1 level case, circulating currents are greatly higher; for PSCB method it is 6.5 times and for S&S-RS method it is 4.5 times higher. S&S-RS method with N+1 level output phase voltage gives the lowest arm current and the highest efficiency. The arm currents are increasing roughly 0.5% for 2N+1 level case for direct modulation methods and 0.2% for PSCB method. The efficiency of S&S-RS method is 0.09% higher for N+1 level case than 2N+1 level, and the difference is 0.14% for PSCB method. The submodule capacitor voltage ripple, which is dependent on the output and circulating current, is a little bit lower for 2N+1 level case for direct modulation methods, although the circulating currents ac component and consequently arm currents increased. It seems that the increasing circulating current resulted in a decrease in the submodule capacitor voltage ripple. However for PSCB method, the ripple is lower for N+1 level case, and it is the lowest among all, although they are in fact close to each other, except CR method.

Table 7.24 Simulation results numerical data for both N+1 and 2N+1 level output voltage, half load

		N+1 Level Output Voltage				2N+1 Level Output Voltage			
		Direct Modulation			Phase-shifted carrier based control	Direct Modulation			Phase-shifted carrier based control
		S&S	S&S-RS	CR		S&S	S&S-RS	CR	
Phase voltage (V_l) THD (%)		5.23	5.38	5.13	8.58	4.11	4.08	4.00	4.19
Line-to-line voltage THD (%)		5.22	5.38	5.13	8.55	4.13	4.07	3.97	4.18
Current (i_l) THD (%)		5.31	3.88	3.90	8.16	2.89	2.09	2.75	2.37
Peak-to-peak submodule capacitor voltage (V_c) ripple (% of V_{dc}/N)		5.26	4.88	13.62	4.53	5.01	4.71	13.34	4.65
Circulating current ($i_{circ,dc}$) (A)		117.04	116.87	116.69	116.57	116.78	116.80	116.97	116.92
Circulating current ($i_{circ,ac}$) (A_{rms}) (% of dc)		4.43	3.88	11.73	2.89	26.12	17.76	22.70	18.90
Arm current (i_p) (A_{rms})		203.93	203.89	214.67	204.38	206.81	204.97	215.41	204.73
Average switching frequency of phase a upper arm submodules (Hz)	SM1	490	450	459	473	470	456	451	470
	SM2	485	463	460	470	450	424	448	484
	SM3	477	457	459	474	463	462	452	487
	SM4	465	445	458	479	458	472	449	480
	Average of arm	479	454	459	474	460	454	450	480
Efficiency (%)		98.79	98.99	98.80	98.88	98.44	98.91	98.75	98.74

In conclusion, the all simulation results revealed some important outcomes about the control methods of a grid connected MMC. Generally, the performances of S&S-RS and PSCB methods are superior to S&S and CR methods. In fact, S&S-RS method is the best in terms of output current harmonics distortion, circulating current ac component and efficiency, for most of the simulation cases. Since the switching counts are made close to each other for different control methods, the efficiencies are also close to each other and the major difference occurred in the output harmonic performances. The current THD of S&S-RS method is about half of and about 3/4 of the PSCB method for N+1 level and 2N+1 level case, respectively. Similarly, S&S-RS method voltage THDs are about 0.6 times of PSCB method for N+1 level case. Comparing the N+1 level and 2N+1 level case for the same control method, 2N+1 level case provides roughly half of the current THD value of N+1 level case for direct modulation and one fourth for the PSCB method. Submodule capacitor voltage ripple is close to each other for all the methods, except CR method; although PSCB method gives the lowest value for N+1 and 2N+1 level case. Circulating current ac component of S&S-RS method is close to PSCB with a small advantage of about 0.8 times. However the difference between N+1 level and 2N+1 level case are significant for both S&S-RS and PSCB methods; which is at least four times. All in all, S&S-RS method with 2N+1 level output voltage stands out among all methods with its lowest current THD, reasonable circulating current ac component and submodule capacitor voltage ripple, and highest efficiency for a grid connected MMC drive.

CHAPTER 8

MMC BASED MOTOR DRIVE

8.1. Introduction

Medium-voltage variable-speed motor drives are one of the application areas of MMC's as discussed in chapter 1. Especially fan, blower, compressor and pump applications are widely considered with MMC [60], [61]. Low-voltage step in the inverter output significantly reduces motor current ripple and the resultant motor torque ripple, as well as it mitigates undesirable effects of common-mode voltage on ground leakage current and/or bearing current. Application of the MMC to medium-voltage variable-speed drives has been shown to be advantageous over other multilevel converters such as neutral-point-clamped converter and cascaded H-bridge converter, with respect to the installed silicon area and dc-link energy [60]. However, this application has its own unique control challenges. As discussed in Equations (3.17) and (3.18), and seen in chapter 7, the submodule capacitors has an ac voltage ripple with a dominant output voltage frequency component. Indeed, in [62] the voltage ripple magnitude of submodule capacitors is derived as in Equation (8.1):

$$\Delta V_c = \frac{\sqrt{2} i_l}{4\pi f C} \tag{8.1}$$

The ripple magnitude is proportional with the output current and inversely proportional with the output voltage frequency. Thus, the main challenge of MMC

as a variable-speed motor drive is the large ripple magnitude of the submodule capacitor voltages at low frequencies. Large voltage ripple of submodule capacitors may distort the stable operation of the converter and output voltage waveforms as well as exceeding the voltage ratings of semiconductors and capacitors. Therefore, MMC based motor drives would not be suitable for constant torque motors that requires the rated torque at low-speed region. Fan/blower like loads, in which the load torque is proportional to the square or cube of the speed of the motor (in other words output voltage frequency) are more suitable for MMC based motor drives. However, the ac voltage ripple at low speed region operation of the converter is still a problem that needs taking a measure.

8.2. Submodule Capacitor Voltage Ripple Reduction for Low-Speed Region Operation

Low-speed operation of the converter as a variable-speed drive has been recognized as one of the research challenges of MMCs. The ac-voltage ripple shown by Equation (8.1) should be suppressed to an acceptable level. Being a topical subject, the first ripple reduction method was proposed in the literature by Korn, Winkelnkemper and Steimer, in 2010 [25]. This method basically involves the injection of a sinusoidal-wave common-mode voltage and an ac circulating current, $i_{circ,ac}$, into each phase leg. The ac voltage ripple in submodule capacitors is attenuated by an instantaneous power resulting from the common-mode voltage and the ac circulating current. The principals of the method are explained below.

The peak-to-peak ac voltage ripple of the submodule capacitors is proportional to the variation of the stored energy in the submodules. The peak-to-peak energy variation of the capacitor, E_{c_pp}, is expressed in Equation (8.2), with V_{c_avg} being the average capacitor voltage and V_{c_pp} the peak-to-peak voltage ripple:

$$E_{c\_pp} = CV_{c\_avg}V_{c\_pp} \tag{8.2}$$

The energy variation of an arm with N submodules is proportional to the all N submodule capacitor voltage ripple magnitudes. Energy variation of an arm is expressed as in Equation (8.3):

$$E_{\sum c\_pp} = C_{arm} V_{\sum c\_avg} V_{\sum c\_pp} \tag{8.3}$$

As the stored energy in a submodule is the integral of the submodule power, stored energy in the arm is the integral of the arm power likewise. Then, the power spectrum of the arm is deterministic in the submodule capacitors voltage ripple. The arm power is calculated as in Equations (8.4) and (8.5), with the assumption that the circulating current is purely dc, i.e. no ac component exists:

$$p_p = v_p i_p = \left(\frac{V_{dc}}{2} - v_l\right)\left(\frac{i_{dc}}{3} + \frac{i_l}{2}\right) = \frac{V_{dc}}{2}\frac{i_{dc}}{3} + \frac{V_{dc}}{2}\frac{i_l}{2} - v_l\frac{i_{dc}}{3} - v_l\frac{i_l}{2} \tag{8.4}$$

$$p_n = v_n i_n = \left(\frac{V_{dc}}{2} + v_l\right)\left(\frac{i_{dc}}{3} - \frac{i_l}{2}\right) = \frac{V_{dc}}{2}\frac{i_{dc}}{3} - \frac{V_{dc}}{2}\frac{i_l}{2} + v_l\frac{i_{dc}}{3} - v_l\frac{i_l}{2} \tag{8.5}$$

The arm powers contain all frequency components of phase voltage and current, v_l and i_l. The term $\left(\frac{V_{dc}}{2}\frac{i_l}{2}\right)$ leads to arm energy as in Equation (8.6):

$$\frac{V_{dc}}{4}\int i_l\, dt = \frac{V_{dc} I_l}{2\omega}\sin(\omega t) \tag{8.6}$$

This energy term leads to a voltage ripple as in Equation (8.1), being proportional to the output current and inversely proportional to the fundamental frequency. This ripple can be reduced using a special low frequency operation mode. In this mode of operation, common mode phase voltage, v_{cm}, and the circulating current are the circuit parameters to be used as the degrees of freedom. As explained in chapter 3, these parameters do not affect the output or input currents. Adding a common mode voltage term to the arm voltage and circulating current term to the arm current, arm powers are recalculated as in Equation (8.7) and (8.8):

$$p_p = v_p i_p = \left(\frac{V_{dc}}{2} - v_l - v_{cm}\right)\left(\frac{i_{dc}}{3} + \frac{i_l}{2} + i_{circ}\right) \tag{8.7}$$
$$= \frac{V_{dc}}{2}\frac{i_{dc}}{3} + \frac{V_{dc}}{2} i_{circ} - v_l \frac{i_l}{2} - v_{cm}\frac{i_l}{2} + \frac{V_{dc}}{2}\frac{i_l}{2} - v_l \frac{i_{dc}}{3} - v_l i_{circ}$$
$$- v_{cm}\frac{i_{dc}}{3} - v_{cm} i_{circ}$$

$$p_n = v_n i_n = \left(\frac{V_{dc}}{2} + v_l + v_{cm}\right)\left(\frac{i_{dc}}{3} - \frac{i_l}{2} + i_{circ}\right) \tag{8.8}$$
$$= \frac{V_{dc}}{2}\frac{i_{dc}}{3} + \frac{V_{dc}}{2} i_{circ} - v_l \frac{i_l}{2} - v_{cm}\frac{i_l}{2} - \frac{V_{dc}}{2}\frac{i_l}{2} + v_l \frac{i_{dc}}{3} + v_l i_{circ}$$
$$+ v_{cm}\frac{i_{dc}}{3} + v_{cm} i_{circ}$$

Equations (8.7) and (8.8) can be grouped as a common mode term and a differential mode term, defining them in Equations (8.9) and (8.10):

$$p_{cm} = \frac{V_{dc}}{2}\frac{i_{dc}}{3} + \frac{V_{dc}}{2} i_{circ} - v_l \frac{i_l}{2} - v_{cm}\frac{i_l}{2} \tag{8.9}$$

$$p_{dm} = \frac{V_{dc}}{2}\frac{i_l}{2} - v_l \frac{i_{dc}}{3} - v_l i_{circ} - v_{cm}\frac{i_{dc}}{3} - v_{cm} i_{circ} \tag{8.10}$$

Then, p_p and p_n can be grouped as in Equations (8.11) and (8.12):

$$p_p = p_{cm} + p_{dm} \tag{8.11}$$

$$p_n = p_{cm} - p_{dm} \tag{8.12}$$

The load harmonic terms of the common mode power can be compensated with a common mode circulating current component as in Equation (8.13) and that of the differential mode power can be compensated with a differential mode circulating current component as in Equation (8.14):

$$i_{circ\_cm} = \frac{v_l i_l}{V_{dc}} - \frac{i_{dc}}{3} \tag{8.13}$$

$$i_{circ\_dm} = i_l \frac{\frac{v_l^2}{\frac{V_{dc}}{2}} - \frac{V_{dc}}{2}}{2v_{cm}} \tag{8.14}$$

Then, the overall circulating current is the sum of common mode and differential mode components. Also, the terms of the remaining power is rewritten as in Equation (8.15):

$$p_p = v_{cm}\frac{i_l}{2} + \left(\frac{V_{dc}}{2} - v_l\right) i_{circ\_dm} - v_{cm}\left(\frac{i_{dc}}{3} + i_{circ\_cm}\right) \tag{8.15}$$

In this case, the remaining power terms are all factors of either v_{cm} or i_{circ_dm}. Thus, submodule capacitor voltage ripple will be around the frequency of v_{cm} and the magnitude of it will depend on the frequency of v_{cm} as expressed in Equation (8.1), if all its frequency components are at higher frequencies than the output voltage.

Differential mode circulating current, as expressed in Equation (8.14) may become infinite as v_{cm} crosses zero, thus making the remaining arm power infinite also. However, in order to be spectrally separated from the output current and not to give rise to undesired power terms with nonzero mean, v_{cm} has to be zero mean and thus, cross zero. The division by zero in Equation (8.14) can be prevented by forming v_{cm} as a square wave, or a sinusoidal wave. This two alternatives form the fundamentals of choosing v_{cm} and i_{circ}.

8.2.1. Selection of Waveforms for v_{cm} and i_{circ}

Selection of waveforms for v_{cm} and i_{circ_dm} is based on the fact that the common mode voltage term v_{cm} should be zero mean. For this aim, two fundamental methods are presented in the literature: sinusoidal wave method and square wave method [25], [26], [28], [63].

i. Sinusoidal Wave Method

The sinusoidal wave method gives v_{cm} and i_{circ_dm} as in Equations (8.16) and (8.17):

$$v_{cm} = \sqrt{2}V_{cm}sin(\omega_{cm}t) \tag{8.16}$$

$$i_{circ} = i_{circ\_cm} + i_{circ\_dm} = \frac{v_l i_l}{V_{dc}} - \frac{i_{dc}}{3} + \frac{1}{\sqrt{2}V_{cm}}\left(\frac{2v_l^2}{V_{dc}} - \frac{V_{dc}}{2}\right) i_l sin(\omega_{cm}t) \tag{8.17}$$

At low speed operation of fan-/blower like load, the common mode terms of circulating current is negligible compared to differential mode term [26].

ii. Square Wave Method

The square wave method gives v_{cm} and i_{circ_dm} as in Equations (8.18) and (8.19):

$$v_{cm} = \begin{cases} -V_{cm} & \left(0 < t < \frac{1}{2f_{cm}}\right) \\ V_{cm} & \left(\frac{1}{2f_{cm}} < t < \frac{1}{f_{cm}}\right) \end{cases} \tag{8.18}$$

$$\begin{aligned} i_{circ} &= i_{circ\_cm} + i_{circ\_dm} \\ &= \begin{cases} \frac{v_l i_l}{V_{dc}} - \frac{i_{dc}}{3} + \frac{1}{2V_{cm}}\left(\frac{2v_l^2}{V_{dc}} - \frac{V_{dc}}{2}\right) i_l & \left(0 < t < \frac{1}{2f_{cm}}\right) \\ \frac{v_l i_l}{V_{dc}} - \frac{i_{dc}}{3} - \frac{1}{2V_{cm}}\left(\frac{2v_l^2}{V_{dc}} - \frac{V_{dc}}{2}\right) i_l & \left(\frac{1}{2f_{cm}} < t < \frac{1}{f_{cm}}\right) \end{cases} \end{aligned} \tag{8.19}$$

The square wave method is superior to the sinusoidal wave method in terms of the reduced peak circulating current.

8.2.2. Control Method with Low Frequency Region Operation

Control methods of MMC with low frequency operation are again based on direct modulation approach and phase-shifted carrier based control as explained in chapter 6. In this thesis, phase-shifted carrier based control will be investigated [26].

The fundamentals of the control algorithm are the same as expressed in section 6.4. Figure 8.1 shows the block diagrams for the averaging control, circulating current control and balancing control. Equations (8.20) and (8.21) show the positive and negative arm voltage commands for submodules:

$$v_{j\_u}^{*} = v_{A\_u} + v_{B\_j} - \frac{v_{l\_u}^{*} + v_{cm}}{N} + \frac{V_{dc}}{2N} \qquad (j: 1 - N) \tag{8.20}$$

$$v_{j\_u}^{*} = v_{A\_u} + v_{B\_j} + \frac{v_{l\_u}^{*} + v_{cm}}{N} + \frac{V_{dc}}{2N} \qquad (j: N - 2N) \tag{8.21}$$

Here, $v_{l\_u}^{*}$ is the positive-sequence component calculated from "field-oriented control" [64].

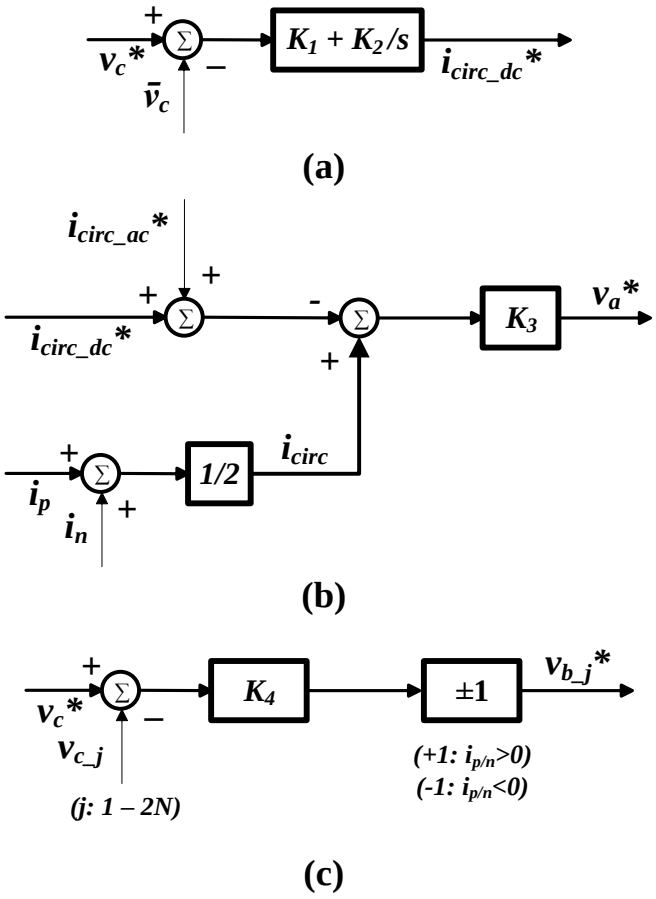


Figure 8.1 Block diagrams for (a) averaging control, (b) circulating current control and (c) balancing control while low frequency operation of MMC

Since i_{circ} is a circulating current as explained in chapter 3, the peak value of i_{circ} should be mitigated to reduce the arm inductor size and decrease the conduction loss. Considering Equation (8.14), in order to mitigate i_{circ} as much as possible, v_{cm} should be increased. However, v_{cm} on the other hand is limited by the modulation index of each chopper cell. Neglecting the first and second terms in Equation (8.20), which are small compared to the others, the following equation should be satisfied to avoid over modulation of each chopper cell:

$$m = \frac{1}{V_c}\left(-\frac{v_{l\_u}^* + v_{cm}}{N} + \frac{V_{dc}}{2N}\right)_{max} \leq 1 \tag{8.22}$$

Equation (8.22) implies that the low frequency operation region should be fixed in the frequency range, since near the nominal frequency of the motor, $v_{l\_u}^*$ is generally high. Indeed, in this region, it is not necessary to inject common mode voltage, since the output current itself is at high frequency, not boosting the ac voltage ripple of submodule capacitors. Therefore low frequency operation region may be limited to the frequency region of, for example, $0<f<f_{nom}/4$.

The frequency of common mode voltage should be more than three times of output current frequency in order to satisfactorily suppress the ac voltage ripple of submodule capacitors. Also, it should be less than one-tenth of the carrier frequency, f_c, in order to achieve good controllability of current.

8.3. Operation of a 9.1MW Induction Machine with MMC and Simulation Results

In order to verify the above mentioned low frequency operation of MMC based motor drive, a simulation study is conducted via Simplorer. A 9.1MW induction machine is operated from standstill to the full speed, by field oriented control [64]. Sinusoidal wave method is implemented for low frequency region operation up to 20Hz output frequency. In between 10Hz and 20Hz output frequency, the injected

common-mode voltage gradually decreased, as can be noticed from Figure 8.8. MMC simulation parameters are given in Table 8.1 and rated parameters of the induction machine is given in Table 8.2.

Torque reference and output of the machine are given in Figure 8.2. The reference is tracked successively. The magnetizing current reference and magnetizing current of the machine can be seen in Figure 8.3. The magnetizing current has high frequency ac component especially in low frequency operation. The speed reference and speed of the machine are given in Figure 8.4. The machine is able to track the speed reference successively. In Figure 8.5, three-phase stator currents can be seen. It is possible to observe the operation of the machine from standstill to the full speed. Figure 8.6 shows the upper and lower arm currents of phase a. In low frequency operation region, the arm currents are high because of the circulating currents; however, they are still not higher than their magnitude in full speed region. Therefore, the low frequency region operation does not make the circuit elements exceed their nominal ratings. The success of the method in suppressing the submodule capacitor voltage ripple in low frequency region operation can be noticed by Figure 8.7. Indeed, without the low frequency operation control, the submodule capacitors voltages would increase to multiples of nominal voltage. Three-phase circulating currents are seen in Figure 8.8. As expected, they are high in magnitude in low frequency region operation. However, when the low frequency operation is ended, the circulating currents are close to dc. It is suitable to end up the low frequency operation at a proper frequency in order not to increase the conduction losses via circulating currents and decrease the efficiency of the converter.

Table 8.1 Simulation parameters for MMC motor drive

Symbol	**Meaning**	**Value**	**Comments**
V_{dc}	Dc-link voltage	16.4kV	
N	Number of submodules per arm	4	
L_{arm}	Arm inductance	4.7mH	0.133pu
R	Arm resistance	50mΩ	
C	Sub module capacitance	3mF	66.5J/kVA
f_c	Carrier frequency	2kHz	Phase-shifted

Table 8.2 Rated parameters of the induction machine*

Symbol	Meaning	Value
S	Power	9.1MW
F	Frequency	50Hz
V	Line-to-line rms voltage	10kV
N_{rm}	Rotating speed	2990rpm
I_1	Stator rms current	590A
I_0	Magnetizing current	194A
P	Pole-pair number	1
J_m	Moment of motor inertia**	1.79kgm^2
T_L	Load torque	$0.2 * w_m^2$

* Motor parameters are derived from Siemens H-compact PLUS 1RP6 716-2HJ■0 [67].

** The original moment of motor inertia is divided by 100 in order to quicken the simulation and not to overload the RAM of the computer on which the simulation runs.

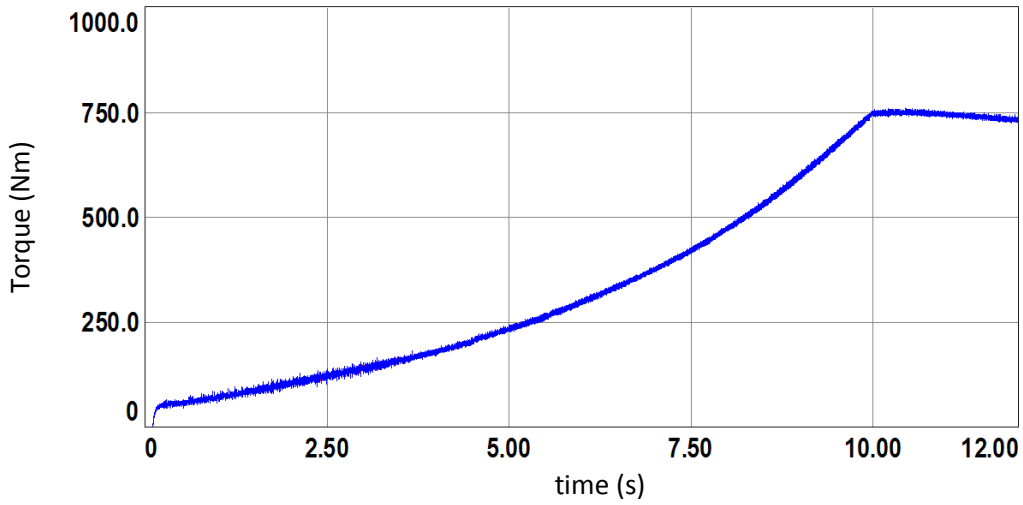


Figure 8.2 Torque reference and output of the induction machine

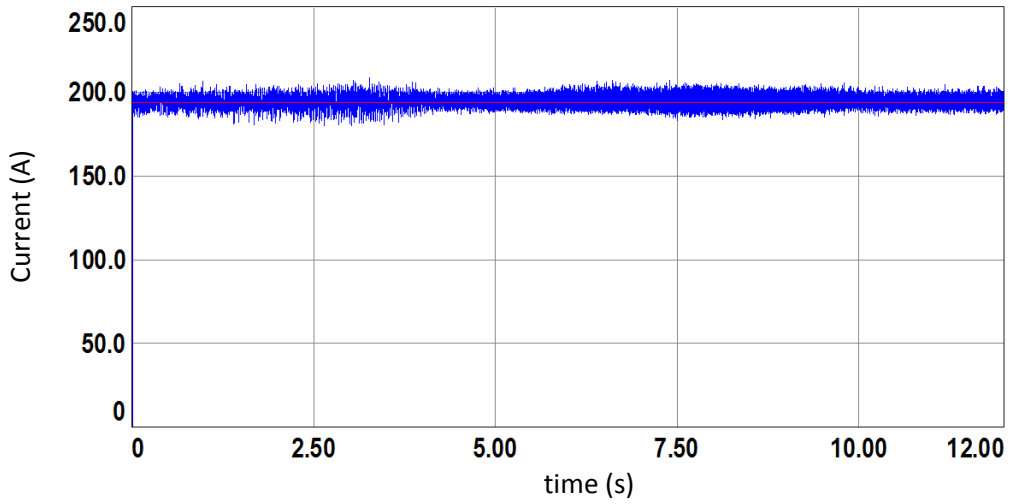


Figure 8.3 Magnetizing current reference and field current of the induction machine

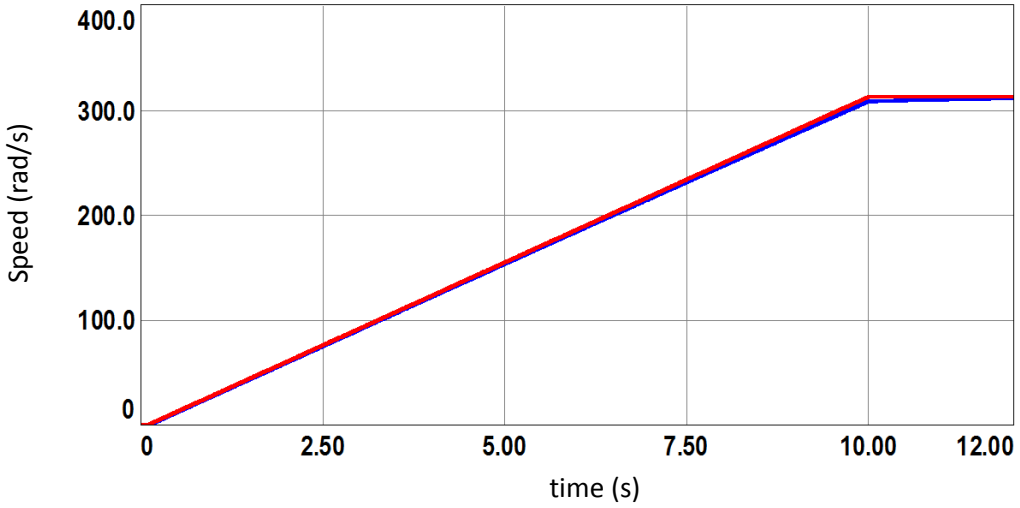


Figure 8.4 Speed reference and speed of the induction machine

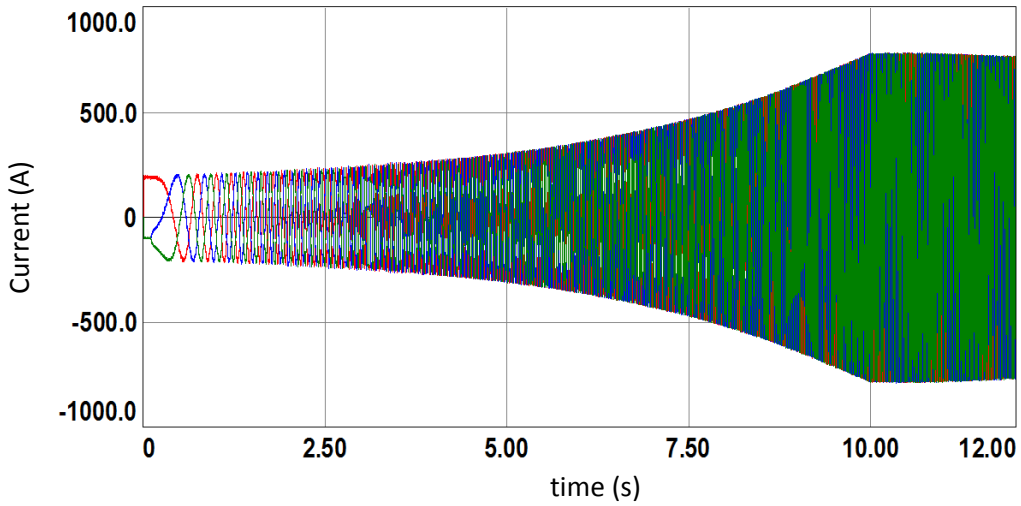


Figure 8.5 Three-phase stator currents of the induction machine

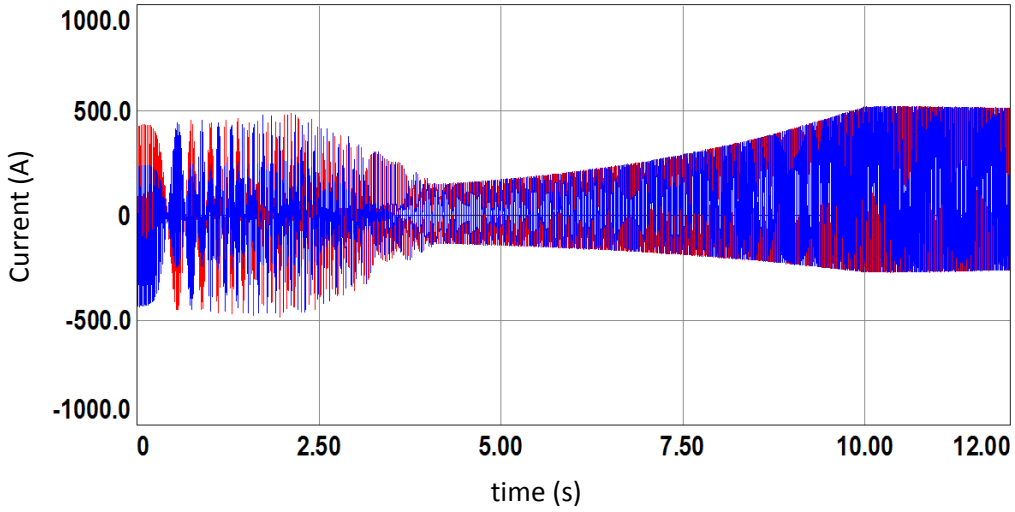


Figure 8.6 Phase a upper and lower arm currents of MMC motor drive

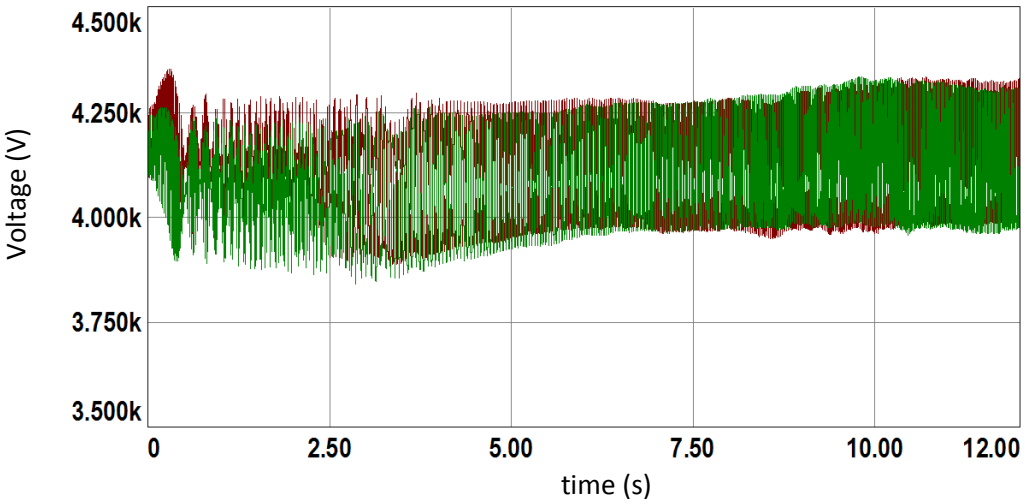


Figure 8.7 Phase a upper and lower arm capacitor voltages of MMC motor drive

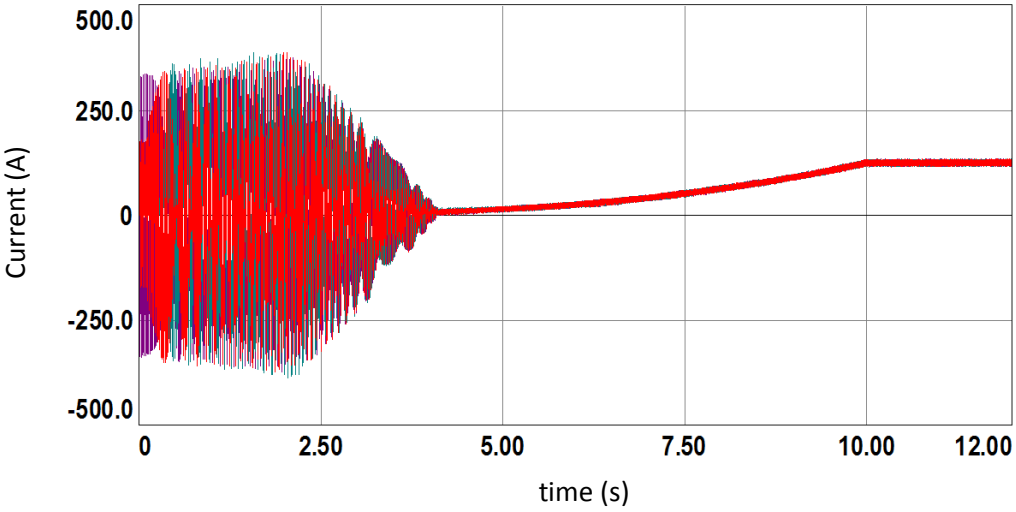


Figure 8.8 Three-phase circulating currents of MMC motor drive

CHAPTER 9

CONCLUSION

Energy is the most valuable and indispensable asset of countries. The energy demand of mankind is increasing day by day. As the machines are replacing manpower since the industrial revolution, modern civilizations have based their survival on energy, anymore. The electrical energy is obviously the dominant form among others due to its flexibility of conversion to other forms, ease of transmission to the consumption site, low environmental effect and its sustainable character. It is obvious that the demand of electrical energy will increase tremendously, not only because of the population increase, but also the faster increasing automation in every aspect of life. Moreover, apart from supplying this increasing demand, renovation of conventional depletable electrical energy sources to sustainable and environmental friendly ones, brings extra workload to electrical power engineering industry. Thus, the electrical energy systems are required to respond properly to this continuously increasing demand. Moreover, they need to be reliable and supply the electrical energy with high quality, meeting the national and international relevant standards. High efficiency, low cost and infrequent maintenance need as well as environmental friendliness are being expected from the electrical energy systems of today. The conventional two/three-level voltage source converters are not able to respond all these requirements accurately. They have limitations in terms of power capacity, energy quality, semiconductor ratings, reliability, robustness, efficiency, cost, size and footprint and so on. Modular multilevel converter is proposed to overcome these high end requirements. Their modular submodule structure provides many favorable features such as adaptability to broad power and voltage ranges, advanced redundancy, independence from the fast developing state-of-the-art of

semiconductor devices, resilience, and ability to continue to operation in case of a fault. Moreover, their stepped output voltage waveform provides low harmonic content compared to conventional VSCs, which eliminates the usage of big, lossy, and costly output harmonic filters. They do not need a centralized energy storage element or separate dc sources. The switching frequency of the semiconductors may even be decreased to fundamental frequency, enabling low switching loss and easing thermal management of semiconductors. Also, the input current distortion and output common-mode voltage of MMC are less than conventional VSCs. Owing to these features, MMCs are mainly appealing in multi megawatt systems, such as HVDC transmission (especially in the connection of offshore wind energy power stations to the mainland, energy transfer to the islands and between asynchronous electricity grids, international and intercontinental energy transfer), medium-voltage motor drives, STATCOM applications and energy storage applications.

This thesis is focused on the selection of suitable PWM switching and control methods for MMC drives.

The first main objective of the thesis is to provide the fundamental characteristics of different carrier based PWM methods used for MMC switching: level-shifted and phase-shifted carriers with their purest forms, i.e. without any external control loop. Pulse pattern, switching manner and resultant output harmonic content of PD, POD, APOD and phase-shifted carriers methods are investigated under equal total count of switching in a phase leg principle, throughout broad m_a and m_f ranges. Also, principles of switching methods for N+1 and 2N+1 phase-to-neutral output voltage levels are explained. It is shown that PS method provides balanced and homogeneous pulse patterns for different submodules in a phase arm, whereas LS methods yield unbalanced and heterogeneous switching pulses. As a result, PS method can provide equal exploitation and aging for different submodules, also enabling common maintenance and thermal management. The LS methods cause unequal aging and voltage unbalance in different submodules; the methods should be implemented with suitable measures to eliminate these problems. The locations of

resultant output voltage harmonics are similar to each other for LS and PS methods both for N+1 and 2N+1 level V_{ph}, as long as LS methods' switching frequency is N times that of PS method, which enables equal switching count per leg. For N+1 level case, the dominant harmonics are at the sidebands of the equivalent converter switching frequency (f_c for LS and Nx f_c for PS); for 2N+1 level case, they are at the sidebands of twice the converter switching frequency. Moreover, the magnitudes of harmonics generated by all LS and PS methods are similar to each other for 2N+1 level V_{ph} generating cases. It does not make sense which method is used for modulation. However, the differentiation occurs in magnitudes of the harmonics for N+1 level V_{ph} generating cases. PD method of LS carriers generally has the smallest output harmonics throughout broad m_a and m_f ranges, for the case with N+1 level V_{ph}. Thus, it gives the lowest weighted total harmonic distortion among all methods. Figure 4.39 and Figure 4.40 give the exact values, but roughly PD has half of the WTHD values of other methods. Consequently, PD would be the right method to be used for N+1 level V_{ph} modulation. Comparing the N+1 level and the 2N+1 level V_{ph} generating methods, the latter provides a doubling in the converter switching frequency, so does in the locations of dominant voltage harmonics. Therefore, the magnitudes of these harmonics weighted by their locations get smaller, which improves the quality of the output voltage waveforms. Figure 4.51 gives the exact values, but roughly 2N+1 level method gives half of the WTHD value of N+1 level method.

The second main objective of the thesis is to provide the performance comparisons of different MMC control techniques with N+1 and 2N+1 level V_{ph} voltages, in terms of output voltage/current harmonic content, submodule capacitor voltage ripple, circulating current ac component and efficiency for a grid connected system under different loading conditions. Direct modulation and phase-shifted carrier based (PSCB) control are considered. Moreover, the branching in direct modulation in terms of submodule capacitor voltage balancing mechanisms is explained, comprising in sort and select (S&S) method, sort and select method with reduced count of switching (S&S-RS) and carrier rotation (CR) method. The methods are

evaluated on a dc/ac conversion step of an HVDC transmission system. It is shown that the CR method on its own is not suitable for MMC control because of its problematic submodule capacitor voltage ripple and circulating current ac component characteristics. Generally, S&S-RS is superior to S&S method in terms of applicable performance criteria. Therefore, the suitable control method selection shall be made among the direct modulation S&S-RS method and PSCB method. It is found that in general S&S-RS method has superiority over all other mentioned control methods in terms of output current harmonics distortion, magnitude of circulating current ac component, and efficiency. Current THD of S&S-RS method is roughly at the range of 1/2 to 3/4 of PSCB method and voltage THD of S&S-RS method is roughly at the range of 0.6 to full of PSCB method. Circulating current ac component of S&S-RS method is roughly 0.8 times that of PSCB method. PSCB method, on the other hand, is better than the others in terms of submodule capacitor voltage ripple. However, the ripple values are close to each other except CR method. Moreover, the results revealed that the methods with N+1 and 2N+1 level output phase voltages have different characteristics. In 2N+1 level case, since the converter switching frequency is doubled, the dominant output voltage and current harmonics are shifted to higher frequency range and decreased in magnitude, giving lower THD values. The current THD values for direct modulation methods are halved and for PSCB method it is decreased to one fourth. Nonetheless, since the circulating current contained noteworthy components on/around converter switching frequency for 2N+1 case, the ac component of circulating currents is higher significantly. This has leaded to an increase in total arm currents, so does the conduction losses and a decrease in the efficiency of the converter. The circulating current ac component in 2N+1 level case is at least four times that of N+1 level case, both for direct modulation and PSCB methods. All in all, S&S-RS method with 2N+1 level output voltage stands out among all methods with its lowest current THD, reasonable circulating current ac component, submodule capacitor voltage ripple, and efficiency for a grid connected MMC drive. General characteristics and the suggested control methods for specific performance criteria for N+1 and 2N+1 level output voltage generating methods are summarized in Table 9.1.

Table 9.1 Suggested control methods for N+1 and 2N+1 level output voltage generating methods

		N+1	**2N+1**
General characteristics		- Higher output harmonic distortion - Lower circulating current ac component - Higher efficiency	- Lower output harmonic distortion - Higher circulating current ac component - Lower efficiency
Suggested control method for	Minimum output harmonics distortion	S&S-RS with PD	S&S-RS
	Minimum submodule capacitor voltage ripple	PSCB	PSCB
	Minimum circulating current ac component	S&S-RS with PD	S&S-RS
	Maximum efficiency	S&S-RS with PD	S&S-RS

The third main objective of the thesis is to provide an MMC based motor drive and operate it from standstill to full speed operation, solving the low frequency problem of MMC based motor drives. Boosting in the submodule capacitor voltage ripple in the low frequency region of the drive is solved by a special control method in low frequency, depending on injection of common mode voltage to the phase arms. The method is verified on a 9.1MW induction machine. The machine is operated from standstill to full speed range with a fan/blower-like load, successively.

As future work, MMC based motor drive might be controlled with direct modulation control approach and a similar comparison as in this thesis might be given for the control methods for motor drives with special attention to low frequency operation. Besides, the performance comparisons can be broadened to more realistic efficiency criteria with polynomial based calculation of conduction and switching losses. Moreover, the submodule capacitor voltage ripple suppression by circulating current shaping might be studied [25], [98].

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APPENDIX A

CLARK AND PARK TRANSFORMATIONS

A.1 Clark Transformation

Clark transformation (also known as alpha-beta, αβγ, transformation) is a mathematical transformation employed to simplify the analysis of three-phase circuits. For the transformation, the first step is to define the variable (voltage, current, flux linkage, etc.) in a three-phase system. Here, transformation will be carried out for voltage. For a positive sequence system the voltage of every phase can be written as in Equations (9.1), (9.2) and (9.3) below:

$$v_a = \hat{V}\cos(\omega t) \tag{9.1}$$

$$v_b = \hat{V}\cos\left(\omega t - \frac{2\pi}{3}\right) \tag{9.2}$$

$$v_c = \hat{V}\cos\left(\omega t - \frac{4\pi}{3}\right) \tag{9.3}$$

Every three-phase system can be uniquely represented by a rotating vector called space vector. The same vector can be described in the complex plane as a function of two components α (real) and β (imaginary). This description of real and imaginary components is Clarke transformation as given in Equation (9.4):

$$v^s(t) = v_\alpha(t) + jv_\beta(t) = \frac{2}{3}K\left(v_a(t) + v_b(t)e^{j\frac{2\pi}{3}} + v_c(t)e^{j\frac{4\pi}{3}}\right) \tag{9.4}$$

where, the superscript s is for the αβ stationary reference frame, in which the quantities rotate with electrical speed w and K is the scaling constant.

In matrix form, Clark transformation is given in Equation (9.5):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = K \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{9.5}$$

The inverse Clark transformation is given in Equation (9.6):

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = K \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{9.6}$$

The value of K is given in Table A.1 for different types of Clark transformation.

Table A.1 Types of Clark transformation

Amplitude invariant	K=1
RMS-value invariant	K=$\frac{1}{\sqrt{2}}$
Power invariant	K=$\sqrt{\frac{3}{2}}$

A.2 Park Transformation

Park transformation (also known as direct-quadrature-zero, dq0 or dqo) is a mathematical transformation that reduces the three ac quantities to two dc quantities, on which simplified calculations can be carried out. For the dqo transformation, Clark transformed variables in the stationary reference frame are transformed to the rotating dqo frame. The angular frequency that the rotating frame is rotating can be

arbitrarily selected, such as output voltage fundamental frequency for output power control as in section 6.2 or twice of the output voltage fundamental frequency for circulating current control as in section 6.3.2. A vector in the dq reference frame is written as in Equation (9.7):

$$\begin{aligned} v_{dq} = v_d + jv_q = e^{-j\theta}v^s = \big(\cos(\theta) - jsin(\theta)\big)\big(v_\alpha + jv_\beta\big) \\ = v_\alpha \cos(\theta) + v_\beta\, sin(\theta) + j\big(-v_\alpha \sin(\theta) + v_\beta \cos(\theta)\big) \end{aligned} \tag{9.7}$$

In matrix form, Park transformation is given in Equation (9.8):

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{9.8}$$

The inverse Park transformation is given in Equation (9.9):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{9.9}$$

The combination of Clark and Park transformations gives dq reference frame variables directly from abc stationary reference frame as in Equation (9.10):

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{9.10}$$

The inverse Clark-Park transformation is given in Equation (9.11):

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{9.11}$$

APPENDIX B

SIMULATION LOSS CALCULATIONS

In section 7.3, efficiencies of simulated systems are calculated separately by taking switching and conduction losses of the MMC into account. The switching losses are calculated manually with a linear approximation of the devices' switching characteristics, with the average switching count of the submodules data as given in Table 7.7, Table 7.12, Table 7.18 and Table 7.23 in section 7.3 [99]-[100]. The conduction losses are calculated by the simulation software automatically while switching semiconductors and diodes are modeled linearly in the software. In the calculations, FZ750R65KE3 model numbered Infineon IGBT module is taken as the switching semiconductor, and its datasheet values for 125°C junction temperature are used [77].

B.1 Switching Losses

The switching loss of an IGBT in this thesis is calculated as the sum of all turn-on and turn-off energy at the switching instants per second as in Equation (10.1):

$$P_{sw,IGBT} = \sum_{n} E_{sw,IGBT}\,(i_n) = \sum_{n} \left(E_{on} + E_{off}\right) \frac{i}{I_{nom}} \frac{V_{dc}}{V_{nom}} \tag{10.1}$$

where, n is average switching count of the submodules per second as given in Table 7.7, Table 7.12, Table 7.18 and Table 7.23, E_{on} and E_{off} are the nominal turn on and turn off switching losses of the IGBT as given in the datasheet. i is the rms current of the IGBT under investigation (the upper and lower IGBTs in a chopper cell have different rms current values) and V_{dc} is nominal capacitor voltage for our case.

Therefore, two separate calculations are done for the upper and lower IGBT of the submodules. The result of Equation (10.1) is multiplied by the total number of IGBTs in the converter, which is 24 for each of the upper and lower IGBTs in our case.

The switching loss of a diode in this thesis is calculated as the sum of all turn-off energy at the switching instants per second as in Equation (10.2), while turn-on losses are neglected:

$$P_{sw,diode} = \sum_{n} E_{sw,diode}\,(i_n) = \sum_{n} E_{off}\,\frac{i}{I_{nom}}\frac{V_{dc}}{V_{nom}} \tag{10.2}$$

where, E_{off} is the nominal turn off switching loss of the diode as given in the datasheet. i is the rms current of the diode under investigation. Again, for the upper diode and lower diode of the submodules, two separate calculations are done. The result of Equation (10.2) is multiplied by the total number of diodes in the converter, which is 24 for each of the upper and lower diodes in our case.

B.2 Conduction Losses

Conduction losses in this thesis are calculated by the simulation software. The steady state forward voltage and bulk resistance of IGBTs and diodes are implemented with a linear approximation of nominal datasheet values. Linearization of these values is shown in Figure A.1. The forward voltage is taken as the zero crossing point of the red line and bulk resistance is assumed as the cotangent of the red line. The arm resistances are removed from the simulation circuit and the conduction loss is calculated as the difference of input and output power, as in Equation (10.3). Note that the simulation software does not include the switching losses in the calculations; therefore, the power difference corresponds purely to conduction loss.

$$P_{cond} = P_{in} - P_{out} \tag{10.3}$$

The efficiency of the simulated circuit is calculated as in Equation (10.4):

$$\eta = \frac{P_{out} - P_{sw}}{P_{in}} = \frac{P_{out} - \left(P_{sw,IGBT} + P_{sw,diode}\right)}{P_{in}} \tag{10.4}$$

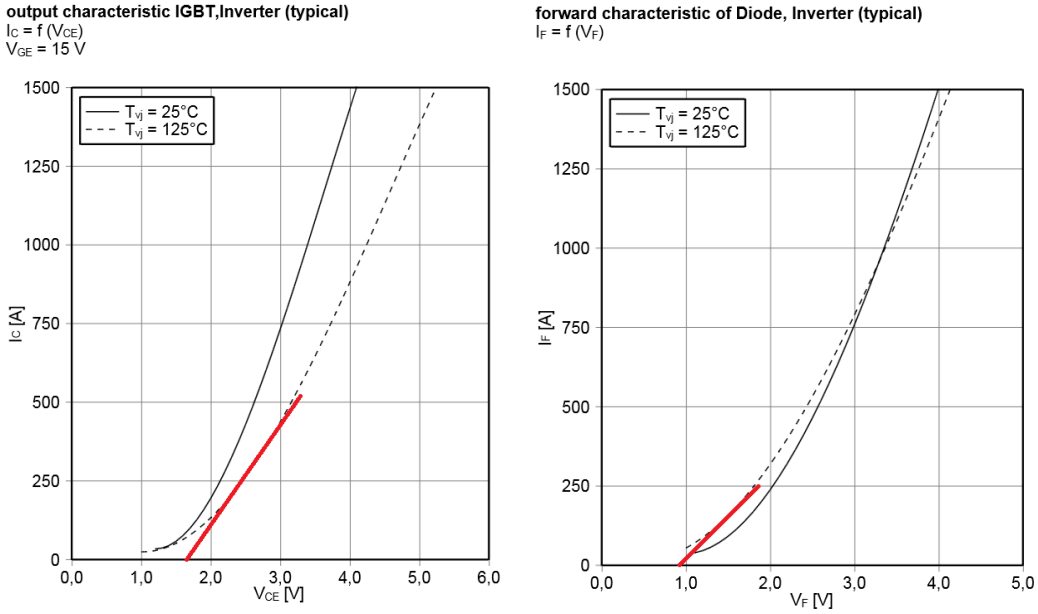

Figure A.1 Linearization of forward voltage and bulk resistance of IGBT at left and diode at right