HIGH SPEED LVDS DIGITAL INPUT/OUTPUT INTERFACE CIRCUITRIES FOR HIGH RESOLUTION IMAGING SENSORS

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ABSTRACT

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This thesis presents the design and implementation of high speed low voltage differential signaling (LVDS) digital input/output interface circuitries for high resolution imaging applications. Designed input/output interface includes high speed LVDS transmitter and receiver circuitry. The circuitries are designed for high speed, low noise, wide common mode range and low power consumption. The designed LVDS transmitter circuitry has a feedback structure used to stabilize the differential common mode voltage to comply with the LVDS standard. In addition, pre-charge and pre-emphasis circuitries are integrated in the transmitter in order to increase the speed and enhance the output signal quality which results in reducing inter-symbol interference in the transmission line. Besides, high current drive mode is added to be able to drive long cables without distorting the LVDS data. The designed LVDS receiver improves the conventional LVDS receiver by supporting the full variation of the common mode voltage as described in LVDS standards. The LVDS test chip is implemented using 0.35 μm CMOS process. The test chip includes two LVDS transmitters, an LVDS receiver, a serializer, a serial programming interface and a bias generator. Test chip provides a programmable serial programming interface (SPI) which allows control over the bias blocks of the LVDS transmitter and LVDS receiver. SPI can also be used to program different modes of operation of the LVDS input/output interfaces. Test chip receives 16-bit parallel data and converts them to a high speed serial data utilizing a serializer for testing the LVDS transmitter. LVDS transmitter design supports 1.5 Gb/s data rate. Differential output swing and the common mode voltage of the transmitter is 350 mV and 1.2V, respectively. The power consumption of the transmitter is designed to be 45 mW at 1.5 Gb/s with 2.5V supply voltage for the driver and 3.3V supply voltage for the other blocks. LVDS receiver design supports 2 Gb/s data rate with full variation of the common mode voltage. The receiver can convert differential input signals with amplitudes larger than 100mV peak-to-peak to 3.3V CMOS signals. The power consumption of the receiver at 2 Gb/s is designed to be less than 6mW with a 3.3V supply voltage. The LVDS transmitter and receiver in the fabricated test chip have been successfully tested at data rates up to 400 Mb/s using an FPGA based test setup developed as part of this thesis.

Keywords: LVDS, differential signal, input/output, transmitter, receiver, serializer, serial programming interface, image sensors, high speed design, low power design.

ÖZ

YÜKSEK ÇÖZÜNÜRLÜKLÜ GÖRÜNTÜ SENSÖRLERİ İÇİN
YÜKSEK HIZLI LVDS GİRİŞ/ÇIKIŞ
ARAYÜZÜ DEVRESİ

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Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
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Bu tez yüksek çözünürlüklü görüntü sensörleri için yüksek hızlı düşük sinyal seviyeli giriş çıkış devresi arayüz devre şeması sunmaktadır. Tasarlanan giriş çıkış devresi LVDS verici ve alıcı devrelerini içerir. Devreler yüksek hızlı, düşük güç tüketimli, düşük gürültü seviyeli ve geniş bir ortak mod aralığına sahip olması için tasarlandı. Tasarlanan LVDS vericisi difereansiyel çıkışın ortak mod voltajının dengede kalmasını sağlamak için geri bildirim yapısına sahiptir. Ek olarak, çıkış sinyalinin kalitesini ve hızını arttırmak için önşarj ve önvurgulama teknikleri uygulandı. Bu teknikler aynı zamanda verici hattındaki simgeler arası karışmayı da azaltır. Bunun yanısıra uzun kabloların sinyal kalitesi bozulmadan sürülebilmesi için yüksek akım modu eklendi. Tasarlanan LVDS alıcısı LVDS standartlarında tanımlanan ortak mod voltajının tamamını destekleyecek şekilde geliştirildi. LVDS test çipi 0.35 µm CMOS teknolojisiyle üretildi. Çipin içinde iki tane verici, bir tane alıcı bir tane serileştirici, bir tane seri programlama arayüzü ve akım üreteci yer almaktadır. Test çipinin içindeki seri programlama arayüzü alıcı ve vericiler için gerekli akımların üretilmesini sağlayan blokların programlanmasına olanak tanır. Seri programlama arayüzü giriş çıkış devresinin çeşitli modlarının kullanılabilmesine de olanak sağlar. Test çipi 16 tane parallel veri alır, serileştirici sayesinde seri hale çevirir ve vericinin testi için kullanılmasını sağlar. Verici saniyede 1.5 Gb verinin transferini destekleyecek şekilde tasarlanmıştır. Vericinin diferansiyel çıkış salınımı 350 mV ve ortak mod voltajı 1.2V olarak tasarlanmıştır. Saniyede 1.5 Gb veri aktarırken 45 mW enerji tüketir. Sürücü devresi 2.5 V güç çekerken diğer bloklar 3.3 V güç çeker. Alıcı saniyede 2 Gb veri alımına olanak sağlar ve ortak mod voltajının tüm aralığında çalışabilecek şekilde tasarlanmıştır. 100 mV'tan büyük LVDS verilerini CMOS verisine çevirebilir. Alıcının 3.3V'luk güç kaynağı kullanarak saniyede 2 Gb veri alırken harcadığı energy tüketimi 6 mW'tan azdır. Üretilen test çipindeki alıcı ve verici devreleri 400 Mb/s veri hızlarına kadar başarıyla test edilmiştir.

Anahtar kelimeler: LVDS, diferansiyel sinyal, giriş/çıkış, verici, alıcı, sıralandırıcı, seri programlama arayüzü, görüntü sensörleri, yüksek hızlı dizayn, düşük güç tüketimli dizayn.

To my family and my love

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CHAPTER 1

INTRODUCTION

Imaging industry is one of the fastest growing industries, with imaging system manufacturers striving for higher number of megapixels each year. As imaging and display formats grow, the systems need higher and higher transmission rates, and conventional CMOS transmitters and receivers become unable to satisfy these rates, while other faster alternatives either consume too much power to be feasible in contemporary compact systems, or are incompatible with standard CMOS process. To understand where and why such transmitters and receivers are needed, one first needs to understand what an imaging system is and which components of an imaging system needs to communicate fast in order to achieve highest frame rates.

1.1 Imaging Systems

An imaging system has optical, electrical and mechanical parts to convert incoming light rays into an electrical stream of data to be displayed or processed in a following system. Optical equipment conveys scene to sensor, electrical equipment converts this optical information to analog and digital signals and mechanical part connects optical and electrical parts and brings camera into use.

Electrical part of the system includes image sensor and readout electronics. Readout electronics processes electrical data from the sensor, amplify and send to output circuitry. Readout circuitry includes digital controller, pixel array, bias generator, analog-to-digital converter (ADC), and I/O interfaces. MT6415CA imaging sensor can be shown as example with its external electronics designed by Mikro-Tasarım. Figure 1-1 shows the stack consists of a 640x512 imaging sensor coupled with an FPGA card and an ADC card [1].

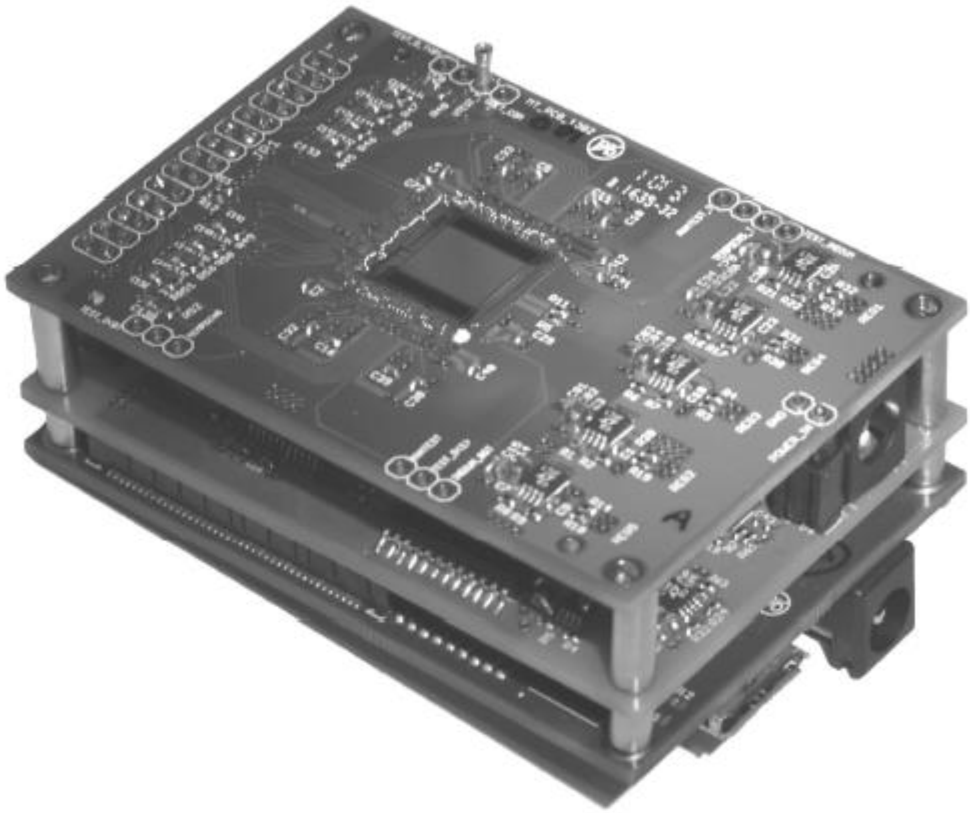

Figure 1-1: MT6415CA imaging sensor coupled with an FPGA card and ADC card [1]

1.1.1 Sensor

There is a huge variety of different sensors used for imaging, ranging from integrated CMOS sensors to hybrid photon detectors bonded to the readout circuits after the chip is produced, covering any desired part of the electromagnetic spectrum. Due to the different behavior of materials in different parts of the electromagnetic spectrum, it is not feasible to generalize sensor structures for each imaging system. Therefore, let us consider the visible image sensors. Visible image sensors are divided into two main categories in terms of usage in industry, namely charge-coupled device (CCD) and complementary metal-oxide semiconductor (CMOS) imagers. Both sensors use metal-oxide semiconductors. The difference between the sensors is the way of processing image after capturing light.

CCD sensor captures photons as electrical charges in each photosite which is a light-sensitive area representing a pixel and the charges on its pixels are read after the exposure. After exposure, the charge packet of each pixel swept into a common output structure sequentially and charge is converted to voltage in there. Then output signals are fed to an ADC.

CMOS sensor contains a solid-state circuitry at each pixel, therefore it can conduct the data in the sensor. Charge is converted to voltage in the pixel and most processes are integrated in the chip which leads to imager functions less flexible but more reliable [2].

CCD sensor is less noisy and more sensitive to light than CMOS sensors; however, with the help of the development of the CMOS process technology, sensitivity of the CMOS sensors has been significantly increased and noise has been decreased. Furthermore, CMOS sensors have lower power dissipation and lower cost. On the other hand, It is possible to make smaller pixels with CCD sensor which leads to make smaller cameras than CMOS technology. Despite their differences, both sensors give very good results and soon there will be little differentiation by these improvements in both areas [3].

1.1.2 Supporting Electronics

1.1.2.1 Analog to Digital Converter (ADC)

Image sensors convert incoming photons to electrical signals. These electrical signals are analog and need to be converted to digital in order to get an image. At this point, Analog-to-Digital Converters (ADC) take place and convert voltage to a digital word. Although there are variety of ADCs in the industry, they are chosen according to some important parameters namely, power dissipation, speed, signal-to-noise ratio, and stated resolution [4].

CMOS image sensors are more preferable than CCDs for high-speed applications particularly. There are three main ADC architectures for high-speed CMOS image sensors namely, single-channel ADC, pixel-level ADC and column-parallel ADC. The single–channel must have significantly high speeds because it uses a single ADC for the whole pixel array. On the other hand, pixel-level ADC takes place in each pixel and converts voltage to digital signals right in the pixel. Above those, the column-parallel ADC uses an ADC for each column and provides better tradeoff for power dissipation, silicon area and frame rate. Hence, the column-parallel ADC is the most preferred one in order to achieve high speed while keeping the performance of imager high [5].

1.1.2.2 Field Programmable Gate Array (FPGA)

Field Programmable Gate Array (FPGA) is an integration circuit which has programmable logic blocks. Complex functions can be implemented and used for communication with peripheral interfaces. The world’s first FPGA, XC2064, is introduced by Xilinx in 1985. There are approximately 1000 logic gates in XC2064 [6]. Today FPGAs have more than one million logic gates.

Image systems use FPGA for processing digital image converted by ADC. High speed I/O interfaces are needed for transferring the digital data to the FPGA for high resolution image sensors. In the following section high speed transceivers are explained.

1.2 Evolution of High Speed Transceivers

Since the advent of the transistor, data transfer always become an important issue. Digital data transmission occurs in two main modes: serial or parallel transmission. In serial communication a serial bit is sent at a time. Bits are sent sequentially on the same channel. However, in parallel communication several bits are send as a whole at a time on buses. Multiple bits are sent simultaneously on the different channels. Data can be transferred perfectly inside a system as parallel. Nevertheless, transferring the parallel data out of the system can cause some problems like complex cabling and crosstalk which causes undesired effect in close channels and distortion. Serial transmission can be the solution for these problems for the communication between the systems.

With the decreasing in the transistor sizes, the speed of the circuits and the demand for the high speed transmission increased. Increases in the bandwidth of the data have led the vendors to develop new transmission technologies. In 1962, RS-232 was introduced with the industry standard by Electronic Industries Alliance [7]. First introduced RS-232 standard was based around single ended transmissions and operates from ±12V power supply. Then new standards and differential I/O interfaces are developed rather than single ended transmission

1.2.1 Transistor to Transistor Logic (TTL)

Transistor to transistor logic was invented in 1961 and composed of bipolar transistors and resistors [8]. In this class of digital circuit, digital and analog functions are performed by the transistors. Before the complementary metal oxide semiconductor (CMOS) transistors becomes popular, TTL was used widely in many applications. TTL can transmit data up to 100 MHz and is needed +5V power supply for operation. One of the drawbacks of TTL is slower switching speed, because transistors are required to be either in saturation mode or cut off to operate. For high speed transceivers TTL logic is not appropriate

1.2.2 Emitter Coupled Logic (ECL)

Emitter coupled logic is another digital circuit family developed for high-speed applications. Emitter coupled logic sometimes called current mode logic (CML) because of the fact that the current steers between the two terminal of the emitter-couple pair [9]. ECL transistors are always in the active region and never goes to saturation mode so that the switching speed is faster than TTL family. The state changing speed is increased with placing small DC bias on the base of the transistor. Although ECL has very fast switching speed, there are two major drawbacks exist. First, ECL operates with negative power which causes interfacing problems with other systems. Secondly, ECL requires higher power consumption than TTL because of the working principle [10].

1.2.3 Complementary Metal Oxide Semiconductor (CMOS)

Before the invention of the bipolar transistors, metal-oxide-silicon-field-effect transistor (MOSFET) idea was patented in 1930’s [11]. However, in 1963 the complementary metal oxide semiconductor (CMOS) devices is introduced. CMOS devices have very low static power consumption and high noise immunity. CMOS technology allows high speed circuits up to 40 Gb/s [12].

1.3 Differential High Speed Systems

High speed systems can be transmitted as single ended or differential ended. Differential ended transmission has some advantages over single ended transmission. Differential ended transmission provides lower noise and faster transition rates than single ended transmission for providing the same amount of power dissipation and the voltage swing. In this section, differential ended topologies are explained in detail.

There are plenty of high speed differential signaling technology varying in terms of performance, power consumption and target application. The most common differential signaling technologies are Low Voltage Positive Emitter Coupled Logic (LVPECL), Current Mode Logic (CML), and Low Voltage Differential Signaling (LVDS). Table 1-1 shows the various attributes of the most common differential signaling technology [13]

Table 1-1: Various attributes of the most common differential signaling technology

	Maximum Data Rate	**Output Swing**	**Power Consumption**
LVPECL	10+ Gb/s	800 mV	High
CML	10+ Gb/s	800 mV	Medium
LVDS	3.125 Gb/s	350 mV	Low

In today's Field Programmable Gates Arrays (FPGAs) support most of them. For example, Altera Stratix device family supports LVDS, LVPECL, HyperTransport, and PCML [14].

In Section 1.3.1, 1.3.2, and 1.3.3 LVPECL, CML and LVDS which are the most common differential signaling technologies are explained respectively. They are also compared in terms of power, performance, and some important parameters.

Figure 1-2 shows the application targets for LVPECL, CML and LVDS [13].

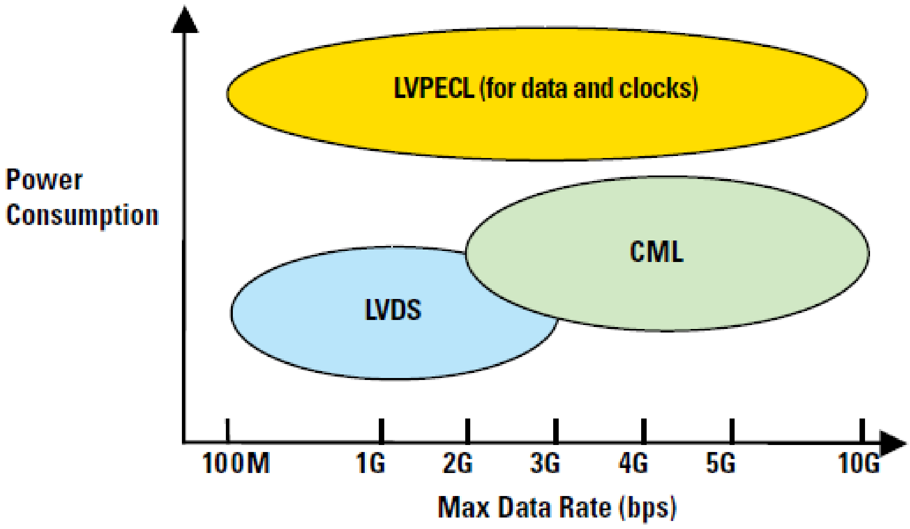

Figure 1-2: Application targets for LVPECL, CML, and LVDS [13]

1.3.1 Low Voltage Positive Emitter Coupled Logic (LVPECL)

Low Voltage Positive Emitter Coupled Logic (LVPECL) is offshoot of Emitter Coupled Logic (ECL). ECL needs -5.2V power supply for operation. This situation causes incompatibility with other logic families. Positive Emitter Coupled Logic (PECL) is introduced firstly to provide compatibility. PECL needs 5V power supply. Then LVPECL is introduced to decrease the power rail from 5V to 3.3V. The output swing of all emitter coupled logic families is 800mV. LVPECL can transmit data up to 10 Gb/s. Very fast data rates can be achieved at the expense of the high power consumption due to the fact that the output stage of the LVPECL always remains in the active region. Figure 1-3 shows typical LVPECL implementation [13].

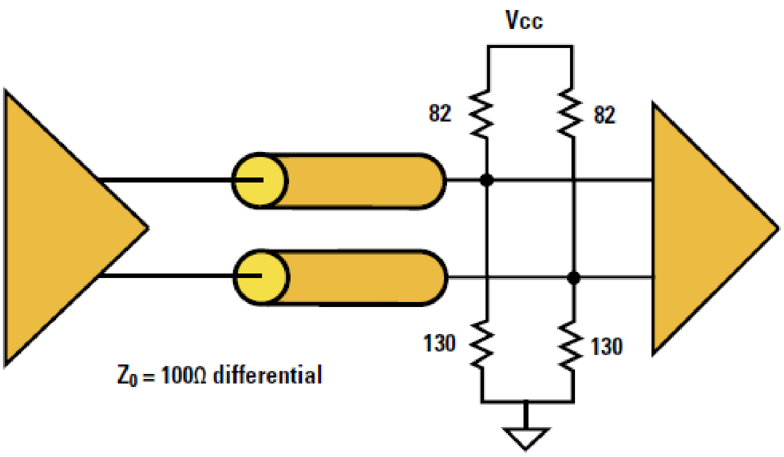

Figure 1-3: Typical LVPECL implementation [13]

1.3.2 Current Mode Logic (CML)

Current Mode Logic (CML) is one of most commonly used high speed differential digital I/O interfaces. CML supports data rates above 10 Gb/s. CML is usually used for fiber optic transmission lines. In addition, well-known video links like HDMI and DVI are implemented with CML.

CML does not require any extra termination resistor between the driver and receiver for termination. Figure 1-4 shows the typical CML implementation [13].

Power consumption of CML is lower than LVPECL but higher than the LVDS.

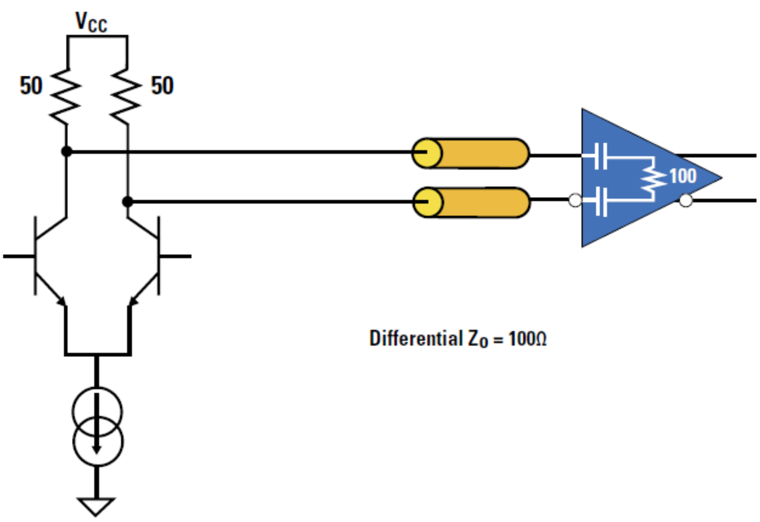

Figure 1-4: Typical CML implementation [13]

1.3.3 Low Voltage Differential Signaling (LVDS)

Low Voltage Differential Signaling (LVDS) is a high speed, low power and low noise I/O interface which is implemented with CMOS transistors. LVDS is not as fast as LVPECL or CML but has some important advantages over them. For example, LVDS is standardized as an electrical layer standard by the TIA. The LVDS standard is published as ANSI/TIA/EIA-644. In addition, some signal-conditioning techniques such as pre-emphasis can be applied to LVDS interface to increase SNR and drive long cables. LVDS has ability to be integrated into chips which is very important for integrity.

With the development of the process technology in CMOS, design of high speed LVDS becomes one of the hottest topic in research. The higher data rates is achieved with the development of the CMOS process. With 0.5 μm CMOS process, 800 Mb/s data rate for transmitter is achieved [15]. The transmitter designed with 0.35 μm CMOS process can reach 1 Gb/s data rate [16], [17]. According to [18], 2.5 Gb/s and 1.3 Gb/s data rate is achieved for the transmitter and receiver respectively with 0.25 μm CMOS process technology. In [19] 5 Gb/s data rate of the transmitter is asserted with 0.18 μm CMOS process.

1.4 The Motivation of the Thesis

Up to know, imaging systems and high speed I/O interfaces are explained in general. As mentioned above, the high resolution imaging sensors need ADC, high speed I/O interface and FPGA for creating the complete camera system. The main purpose of this thesis is to design an optimal high speed I/O interface for high resolution imaging sensors.

LVDS is chosen as the optimal I/O interface for image sensors in terms of power, noise and reliability. LVDS is a low noise and low power differential I/O interface and has ability to integrate in the system level IC design. The output circuitry of the image sensor should have very low noise and consume low power and LVDS I/O circuitry can handle this problem. The LVDS transmitter can be used in the high resolution image sensor chips for transmitting the digital data to the FPGA to process. In addition, LVDS receiver receives high speed LVDS data from the external chips to communicate with the image sensor chip.

This thesis explains the design of the LVDS transmitter and receiver in 0.35 μm CMOS process. In addition, the test chip is implemented for testing the I/O interfaces. The test chip implementation and test steps are explained in detail for testing the whole system.

CHAPTER 2

LVDS TRANSMITTER

Low Voltage Differential Signaling (LVDS) also known as TIA/EIA-644 is a differential signaling technology for high speed serial communication applications [20]. LVDS standard[21] is mainly designed for low power, high speed, and low noise applications mainly. LVDS has low output voltage swing resulting in lower power and faster switching speed utilizing differential structure for transmission and termination [22].

Table 2-1 shows the ANSI/TIA/EIA-644 (LVDS) standards for transmitter

Table 2-1: ANSI/TIA/EIA-644 (LVDS) standards for transmitter [21]

Parameter	Description	Min	Max
V_{OH} (mV)	Output voltage high		1475
V_{OL} (mV)	Output voltage low	925	
$\|V_{OD}\|$ (mV)	Output Differential Voltage	250	400
V_{OS} (mV)	Output offset voltage	1125	1275
R_o (Ω)	Output impedance, single ended	40	140
I_{SA}, I_{SB} (mA)	Short circuit output current		40

In this chapter design and implementation of the LVDS transmitter is explained in detail. LVDS transmitter is designed and implemented using 0.35 µm CMOS technology. Circuit level simulations are performed using spice circuit level simulator.

LVDS transmitter consists of three main parts: (1) Driver block (2) Opamp circuitry for common mode feedback, and (3) Predriver block. Section 2.1, 2.2 and 2.3 will explain the design of these parts respectively. Figure 2-1 shows the overview of the LVDS transmitter with these three blocks.

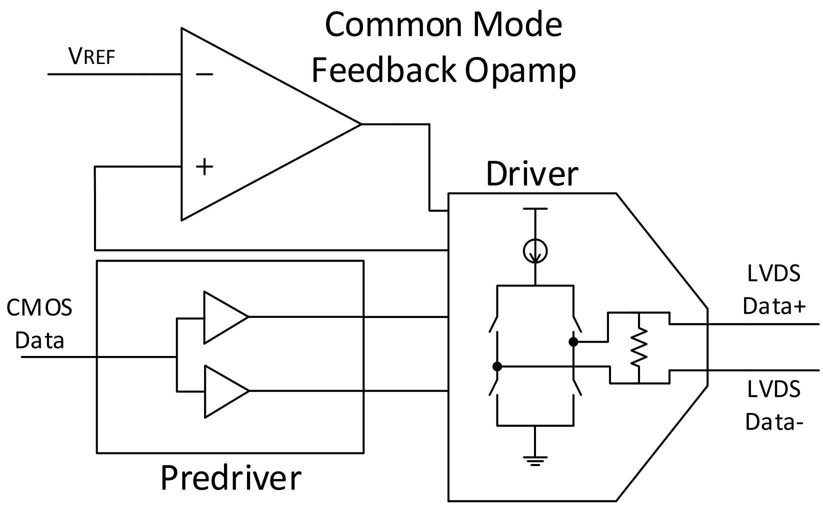

Figure 2-1: Overview of the LVDS Transmitter

2.1 Driver

Driver circuit is the main part of the LVDS transmitter. Driver block mainly converts the differential CMOS data into LVDS data at the termination. Driver is designed as current source with a switched polarity [23]. This nominal current source supplies 3.5 mA in conventional LVDS driver. Figure 2-2 shows the schematic diagram of the conventional driver circuit. Four MOS transistors (M1-M4) are used in bridge configuration for changing the polarity of the flowing current through the load resistor.

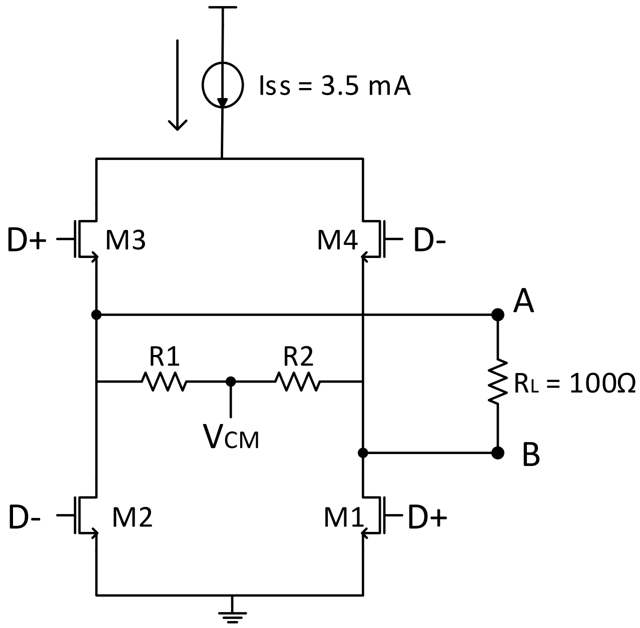

Figure 2-2: Schematic diagram of the conventional driver circuit

The polarity of the current flowing into the load resistor (100Ω) is controlled by the signals generated by the predriver block output signals, D^+ and D^-. When M1 & M3 are on and M2, M4 are off (state 1), the current flows into the termination resistor. When M1, M3 are off and M2, M4 are on (state 2 - i.e. complementary case), the current flows into the reverse direction. The voltage difference between node A and node B for state 1 and state 2 can be written respectively as follows;

$$V_A - V_B = I_{SS}R_L \quad (2.1.1)$$

$$V_A - V_B = -I_{SS}R_L \quad (2.1.2)$$

Between nodes A and B, a high resistance voltage divider (R_1 and R_2) is placed in order to sense the common-mode output voltage (V_{cm}). This common mode voltage is compared with the reference voltage by means of the common mode feedback differential amplifier. The common mode feedback block will be explained in detail later.

In this thesis pre-charge and pre-emphasis techniques are applied to this conventional driver in order to increase the speed and enhance the output signal quality reducing inter-symbol interference (ISI) in the transmission line. Additionally, a high current mode is added in order to drive long cables without distorting the LVDS data. Pre-charge and pre-emphasis techniques and high current mode is explained in Section 2.1, 2.2 and 2.3 respectively. In addition, termination of the driver is explained in Section 2.3 with high current mode.

2.1.1 Pre-charge Technique

While the output current is changing its direction in the switching period, overshoot occurs at the edge [23], since a very large current is induced within a very short time interval. This situation causes distortion and pre-charge technique is proposed in order to handle this problem. Figure 2-3 shows the schematic diagram of the LVDS driver with pre-charge capacitor.

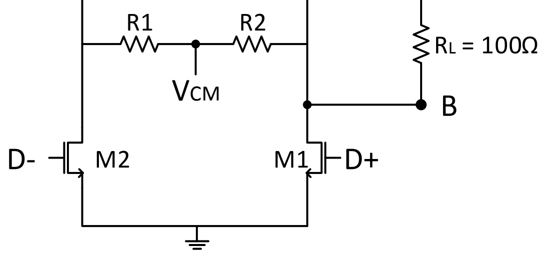

Figure 2-3: Schematic diagram of LVDS Driver with pre-charge capacitor

The pre-charge capacitor is placed into the bridged-switch configuration. Figure 2-4 shows the working principle of this pre-charge technique [23]. When D^+ turns

M1 and M3 on and D^- turns M2 and M4 off defined as state 1 above, pre-charge capacitor C_p is charged parallel with load capacitor, C_L as shown in the Figure 2-4(a) and creates a voltage swing of $I_{SS}R_L$. On the contrary When D^+ turns M1 and M3 off, D^- turns M2 and M4 on, defined as state 2 above, C_L and C_p have different polarity and C_L is neutralized with C_p instantly [23]. This causes the voltage difference between node A and node B (V_A - V_B) to change rapidly as follows due to the charge conservation principle;

$$V_A - V_B = \frac{C_P - C_L}{C_P + C_L} I_{SS}R_L \qquad (2.1.1.1)$$

For example in this design C_p is selected as 4 times larger than C_L and in this case the voltage difference will be changed from $I_{SS}R_L$ to $-0.6I_{SS}R_L$ rapidly. If higher C_p is selected than layout area will be very large. This design does not consume additional power, because C_p is an energy storage element. This pre-charge technique increases layout area due to the large C_p capacitance but reduces the transition time greatly.

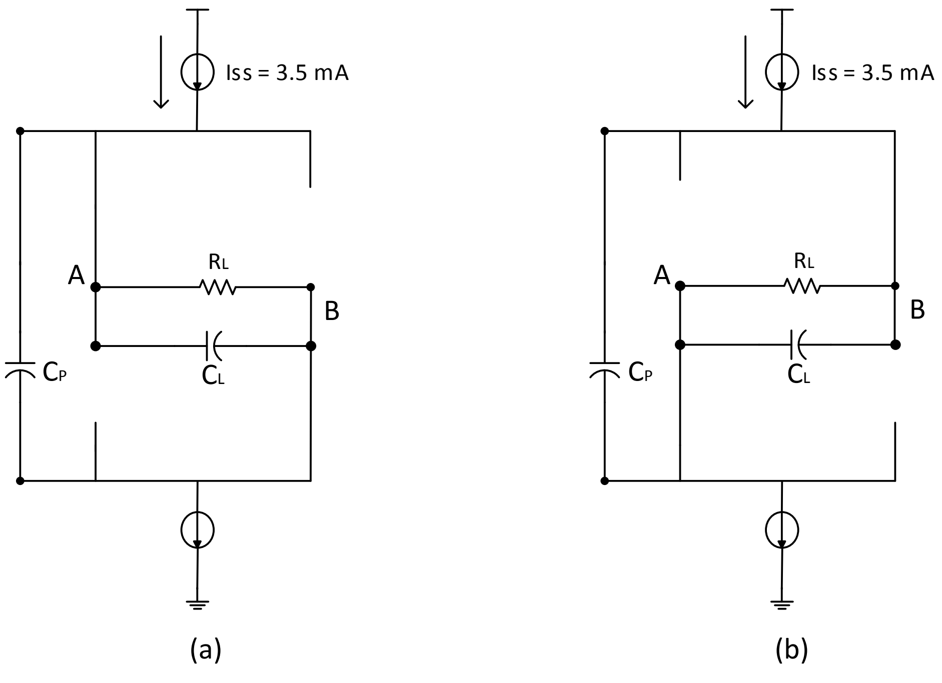

Figure 2-4: Working principle of the pre-charge technique

2.1.2 Pre-Emphasis Technique

While transmitting a stream, if the data is changed after a series of same logic level, the voltage level of the signal increases due to the capacitance in the transmission medium. The data recover becomes very hard. This situation also causes inter-symbol interference (ISI) [24]. ISI is interference of the transmitted symbol with the subsequent symbol because of distortion at high data rates and complicates high data rate communications [25]. Pre-emphasis is implemented to solve these problems. Pre-emphasis technique mainly focus on increasing the energy of the high-frequency component of the data while keeping the high-frequency noise component stable. Thus, higher signal-to-noise ratio (SNR) can be maintained on the receiver end.

LVDS Transmitter output is generated by the tail current flowing through the termination resistors. The tail current limits the operation speed of the LVDS transmitter. In order to increase the LVDS transmitter switching speed, tail current can be increased but this causes higher power consumption and increasing in the output voltage swing. Pre-emphasis circuit injects extra current to the termination resistor while output is changing from low-to-high and high-to-low [26]. This extra current helps increase the high frequency component relative to low-frequency component. This results in a more open eye diagram at the receiver end.

The proposed driver circuit with pre-emphasis includes an extra current supplier and the control circuit to generate pre-emphasis control signals. Extra current supplier circuit is composed of four MOS transistors in bridge configuration. Figure 2-5 shows the schematic diagram of the driver circuit with pre-emphasis. The proposed driver operates like a two tapped finite response filter (FIR). At every transition of the data the current is boosted.

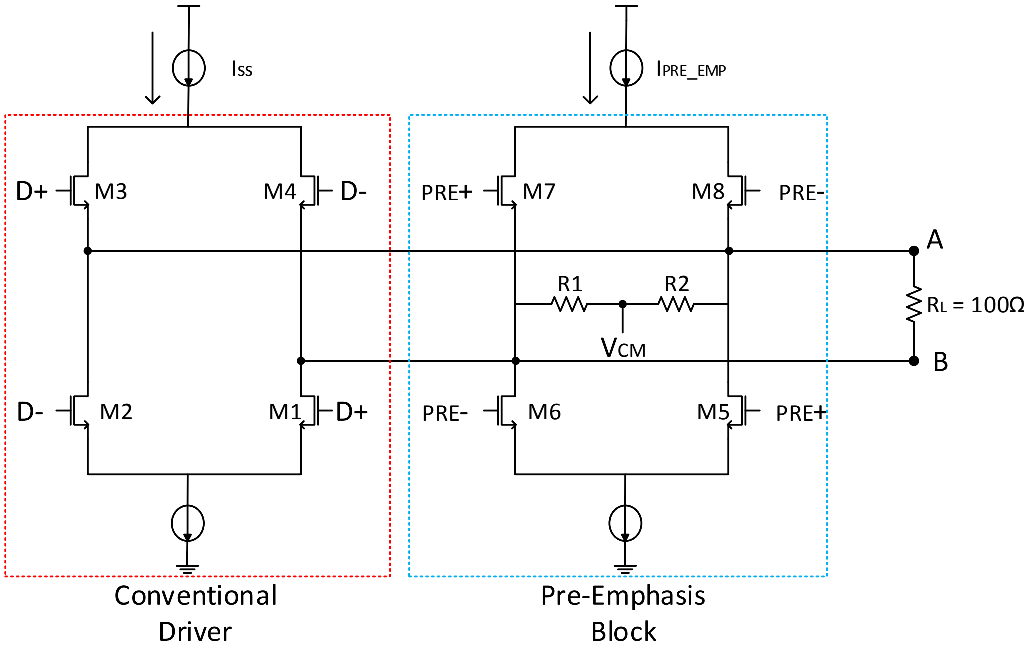

Figure 2-5: Schematic diagram of the driver circuit with pre-emphasis

The control circuit generates pre+ and pre- signals for the pre-emphasis part of the driver circuit. An XOR gate is used to compare the original data signal with the delayed version and an AND gate is used to generate the control signals from the original signal. Figure 2-6 shows the schematic diagram of the pre-emphasis control circuit and its signal waveform. The control circuit is implemented in the predriver circuit.

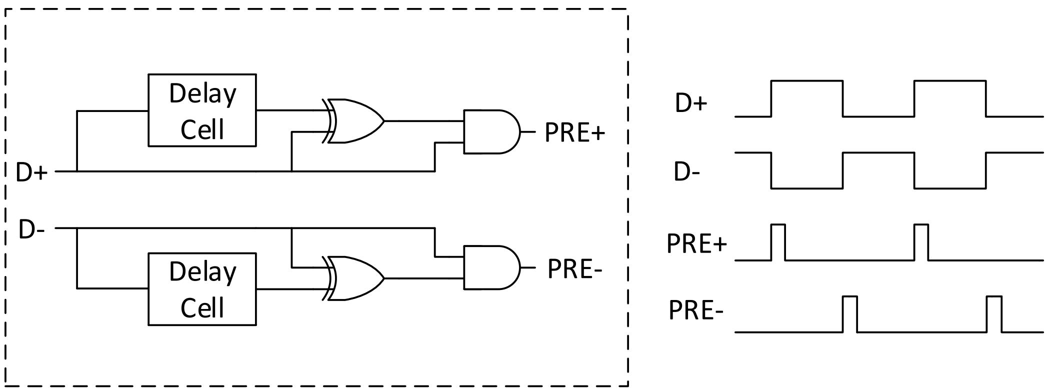

Figure 2-6: Schematic diagram of the pre-emphasis control circuit and its signal waveform

2.1.3 Termination and High Current Mode

LVDS driver and receiver pair are typically used as a point-to-point configuration. Figure 2-7 shows the point-to-point configuration of the LVDS transmitter and receiver. The termination resistor (100Ω) should be placed as close as the receiver end and the impedance of the differential line should be 100Ω. Improper terminations or impedance within the physical media anomalies due to signal reflections causes ISI [13].

In this chip only one transmitter will be connected to one receiver with point-to-point configuration.

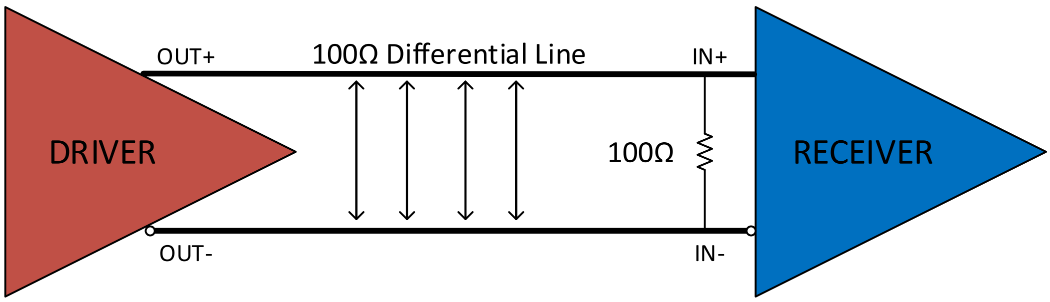

Figure 2-7: Point-to-point configuration of the LVDS driver and receiver. LVDS single termination at the load diagram

Driver and receiver sides can be connected in either single or double termination configuration. If the termination resistor is placed only near the receiver side this configuration is named as single termination as shown in Figure 2-7. In double termination configuration, termination resistor is placed both driver and receiver side. Single termination configuration can be sufficient for most applications. Despite the fact that LVDS is capable of transmitting high-speed signals over substantial lengths of cable, when the cable length is too long, double termination configuration should be used to decrease the reflection coefficient. Figure 2-8 shows the double termination configuration.

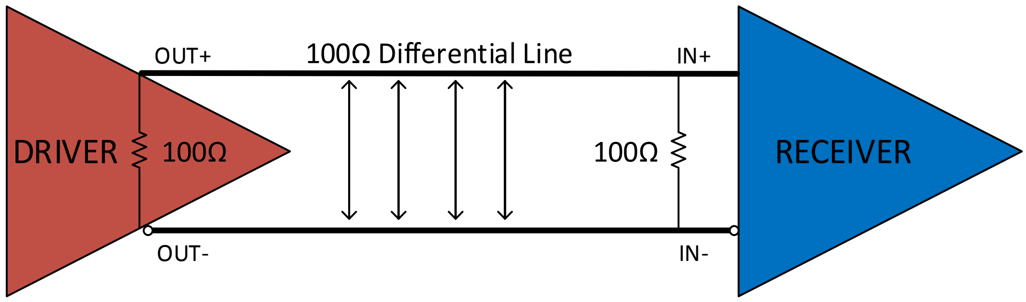

Figure 2-8: LVDS double termination diagram

When the load reflection coefficient is relatively high, double termination configuration can be used. In this configuration the load resistor is effectively reduced to 50Ω. The voltage difference between the inputs of the receiver is equal to 175mV which is the half of the single termination configuration output voltage with the same amount of current supply. In order to increase the output voltage swing, driver should provide 7 mA output current. This configuration decreases the reflection coefficients significantly.

When the high current mode is activated, a termination resistor (100Ω) should be placed between the driver outputs. On-chip termination resistor is implemented in this thesis, with selection option so that without doing any change on the proximity card, double or single termination configuration can be applied even without changing the output voltage swing.

2.2 Predriver

Predriver is designed for receiving the digital data and preparing the digital data for the driver block. This block is mainly composed of a single-to-differential signal generator and a buffer chain circuitry. The single-to-differential signal generator block generates equally delayed differential signals from the serial data coming from the serializer. Generated differential signal should have %50 duty cycle to ensure exact timing and a clearer eye diagram. The buffer chain is implemented to minimize the rise and fall times of the generated signals, since they are the inputs of the LVDS driver. Buffer chain is designed as programmable with

3-bits in order to meet desired rise and fall time constraints for different speed requirements. For slow speed (data rate slower than 500Mb/s) the last step of the buffer can be turned off for power efficiency. Predriver also includes a pre-emphasis signal generator as mentioned in Section 2.1.2. Figure 2-9 shows the schematic diagram of the predriver.

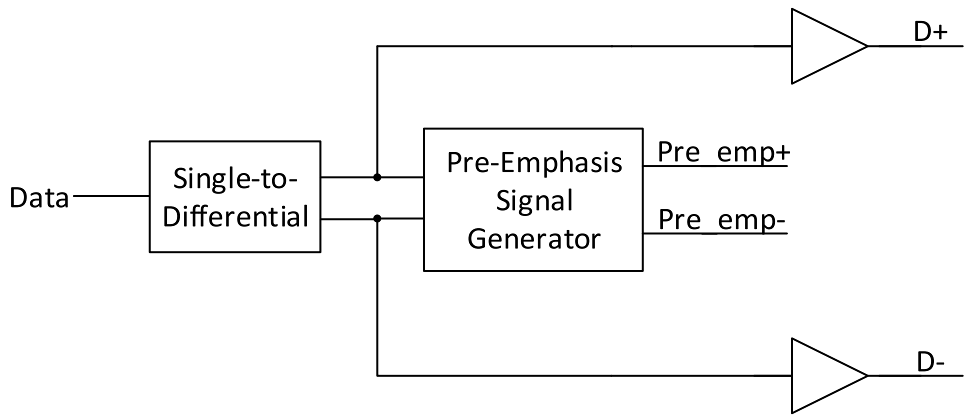

Figure 2-9: Schematic diagram of the predriver

2.3 Common Mode Differential Amplifier

The LVDS transmitter differential output signals change around the common mode voltage. The common mode voltage should be between 1.125V and 1.375V according to LVDS standard specifications (TIA/EIA-644) [21]. In this thesis, common mode voltage is selected as 1.2V. Common mode voltage should not vary anytime during transmission. A feedback loop is needed for a stable common mode voltage. Common mode differential amplifier is designed for this purpose. The common mode voltage is sensed by the resistors R_1 and R_2 in Figure 2-2 , which are very high with respect to the load resistor, and then compared with the reference voltage. In order to adjust the desired output common mode voltage level, a reference voltage is generated in the chip.

Common mode differential amplifier should respond to the switching of the output signal as fast as possible and the stability of the amplifier should be designed to prevent large signal changes at the common mode voltage. The phase-margin of the amplifier is calculated as 82º. . The opamp provides large stability margin with pole-zero compensation network. Figure 2-10 shows the schematic diagram of the common mode feedback amplifier.

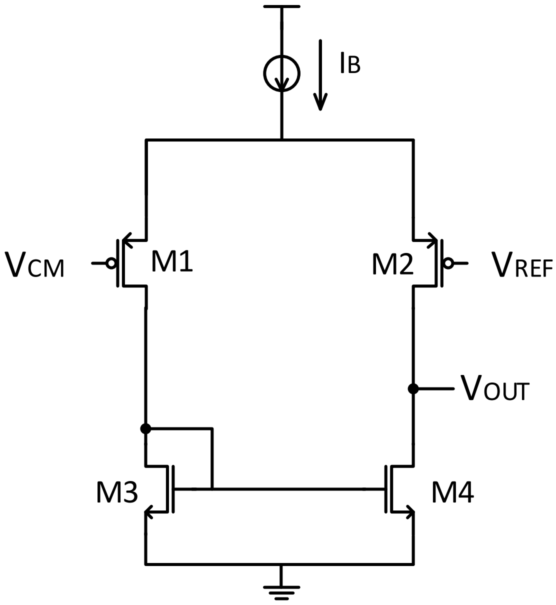

Figure 2-10: Schematic diagram of the common mode differential amplifier

In differential amplifiers, output common mode voltage is highly susceptible to mismatches. Therefore input transistors M1 and M2 are drawn in a common centroid topology. Common centroid layout design provides better matching and the transistors become less sensitive to process variations. If the common centroid layout is drawn more compact then non-linear gradients will be less effective [27].

Figure 2-11 shows the top level of the LVDS transmitter. The driver is placed at the top of the layout. The outputs of the driver are connected to pads and selectable termination resistor is placed between the outputs. The predriver is placed the bottom of the top layout. The layout is implemented considerably dense. Layout of the cell without pad circuitry is 0.052 mm^2.

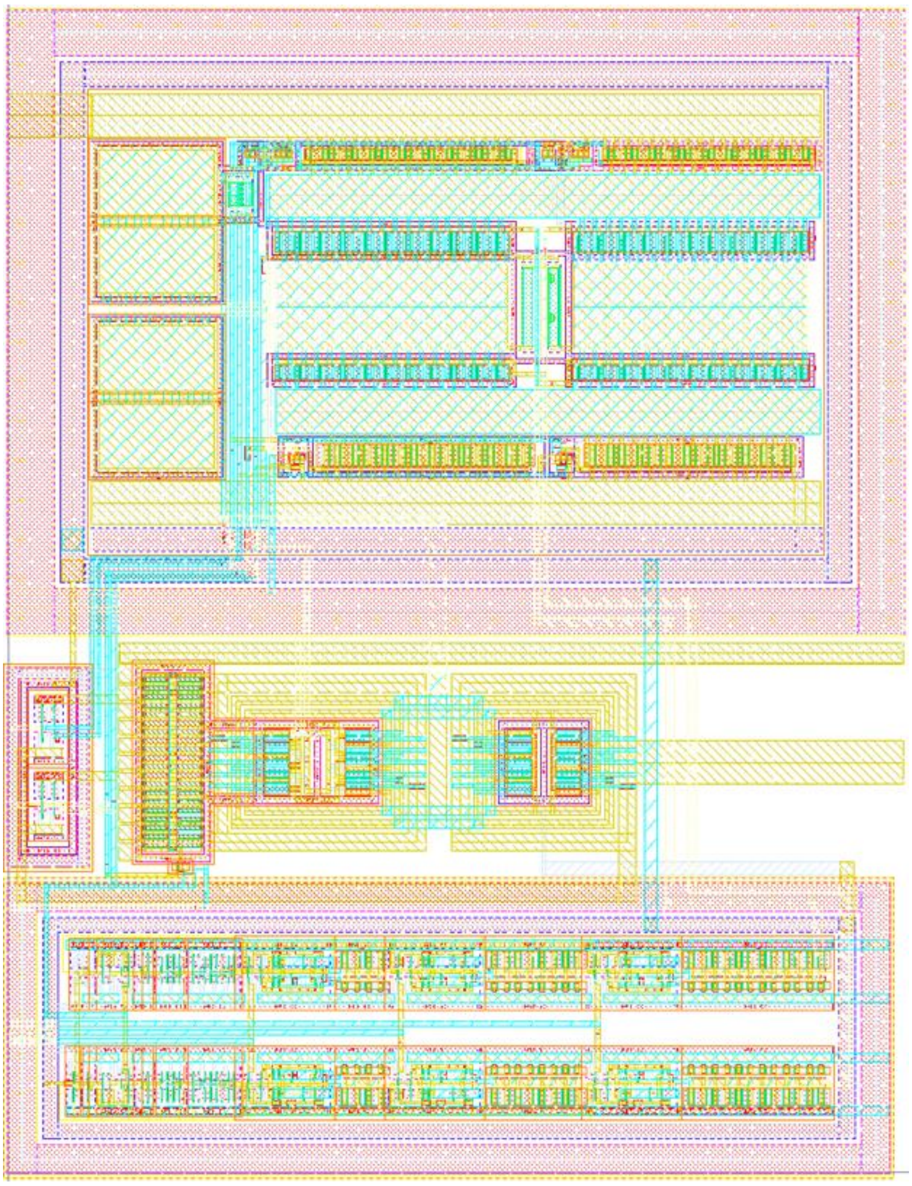

Figure 2-11: Top level layout of the LVDS transmitter. It measures 260 μm in height and 200 μm in width in a 0.35 μm CMOS technology.

The maximum transmission speed of the LVDS transmitter is 1.5 Gb/s. Total DC power consumption is 10 mA at 1Gb/s. Total power consumption is 30 mW at 1 Gb/s transmission rate. The simulation results are shown in the Simulation Results and Test Setup chapter. The designed transmitter fully complies with the requirements of TIA/EIA-644.

Table 2-2 shows the LVDS transmitter performance comparison with other works.

Table 2-2: LVDS transmitter performance comparison

	[28] 1997	[16] 2001	[29] 2002	This Work
Process (µm)	0.35	0.35	0.35	0.35
Power Consumption(mW)	-	43 @ 3.3V	12 @ 1.8V	45 @ 3.3V-2.5V
Maximum Data Rate (Gbps)	0.7	1	1	1.5
Unit Power (mW/Gbps)	-	43	12	30

CHAPTER 3

LVDS RECEIVER

LVDS Receiver is a high-speed differential line receiver that implements the electrical characteristics of Low-Voltage Differential Signaling (LVDS). In this chapter, design and implementation of the LVDS receiver will be explained in detail. Proposed LVDS receiver is designed and implemented using 0.35 μm CMOS technology. Circuit level simulations are performed using spice circuit level simulator.

Table 3-1shows the ANSI/TIA/EIA-644 (LVDS) standards for transmitter

Table 3-1: ANSI/TIA/EIA-644 (LVDS) standards for receiver [21]

Parameter	Description	Min	Max
V_{ICM} (mV)	Input common mode voltage	0	2400
V_{IDTH} (mV)	Input differential threshold	-100	100
$\lvert V_{OD} \rvert$ (mV)	Input differential hysteresis	25	
R_{IN} (Ω)	Differential input impedance	90	110

LVDS Receiver is composed of three main blocks: (1) Preamplifier stage (2) Schmitt Trigger and (3) Buffer stage. Overview of the LVDS receiver with these three blocks is shown in Figure 3-1.

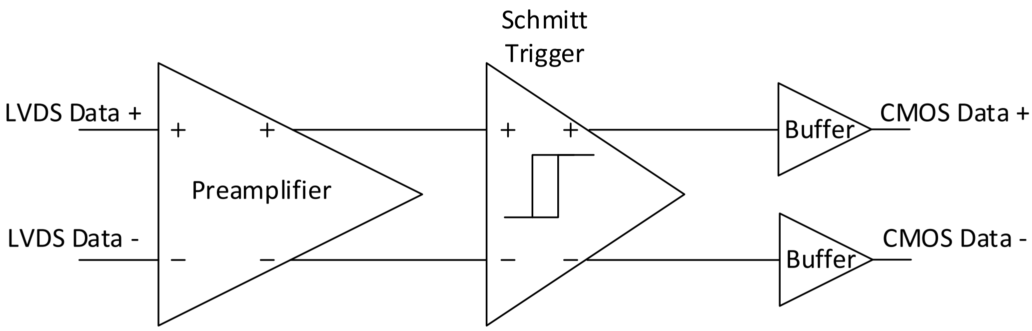

Figure 3-1: Overview of the LVDS Receiver

3.1 Preamplifier

Preamplifier block is the first block of the LVDS Receiver. This block receives the LVDS signals. Preamplifier is very sensitive to substrate crosstalk noise which affects the performance of the receiver negatively especially when input signal levels are low [18]. In order to minimize the common mode noise, a differential structure is used. The preamplifier receives differential signals larger than 100mV peak-to-peak. Common mode voltage range of the differential input signal should be as follows according to LVDS specifications [21].

$$0V \leq Vcm \leq 2.4V \quad (3.1)$$

Preamplifier block is designed in order to support full variation of the common mode voltage.

Figure 3-2 shows the typical LVDS receiver which cannot support full range variation [30]. When input common-mode voltage approaches to 100mV, M1 and M2 can enter the triode region if low-threshold transistors are not available in the process [16]. The preamplifier block is designed as the folded-cascode amplifier with resistive load providing high gain-bandwidth product. Figure 3-3 shows the schematic diagram of the designed preamplifier.

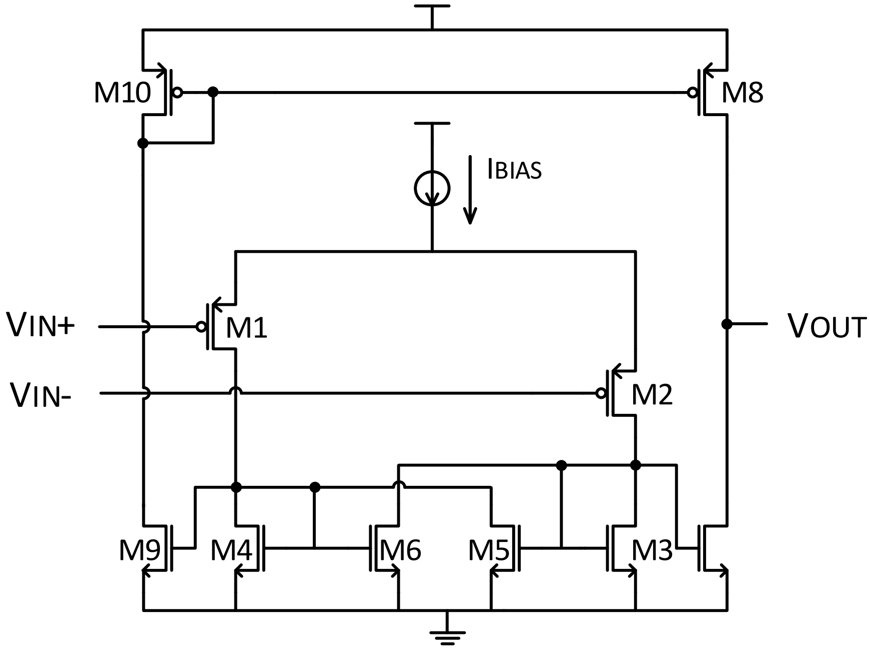

Figure 3-2: Schematic diagram of the typical LVDS receiver

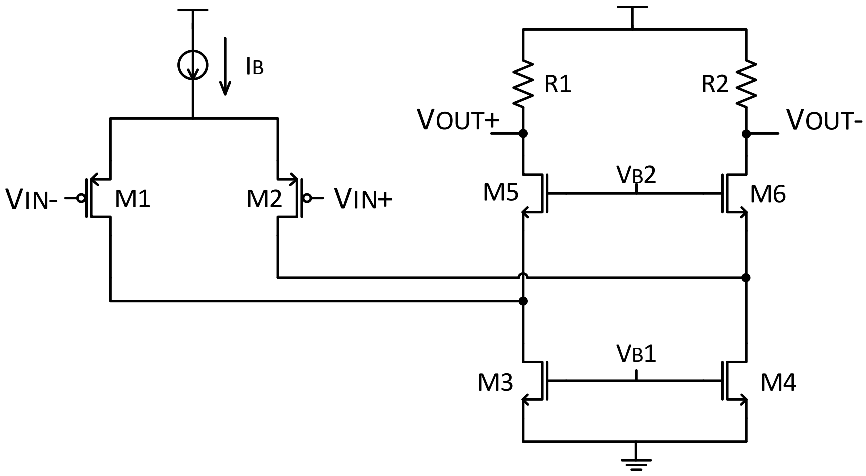

Figure 3-3: Schematic diagram of the preamplifier

M1 and M2 are the input transistors and they are designed with a high W/L ratio for larger transconductance and therefore higher overall gain. This gain should be independent of the input common-mode voltage whose range is defined in the LVDS specification. For this purpose, drain of the input transistors should be set to a low DC voltage with the help of the M3-M6 cascode transistors. Cascode configuration also provides low impedance at the drain node of the input transistors, in order to meet the required bandwidth. The gate voltages of the M3-M6 transistors are generated inside the chip. The values of the load resistors R1 and R2 should be chosen for the correct common-mode voltage for the schmitt trigger input transistors. The common-mode voltage of the differential output is set to 1.65V. The output of the preamplifier is detected by the Schmitt trigger. Schmitt trigger will be explained in detail in the next section.

3.2 Schmitt Trigger

The second block of the receiver is the Schmitt trigger stage. Schmitt Trigger is designed as a typical hysteresis comparator. The differential inputs of the Schmitt trigger are the preamplifier differential outputs whose common-mode voltage is set to 1.65V. Figure 3-4 shows the schematic diagram of the Schmitt trigger with 50mV hysteresis.

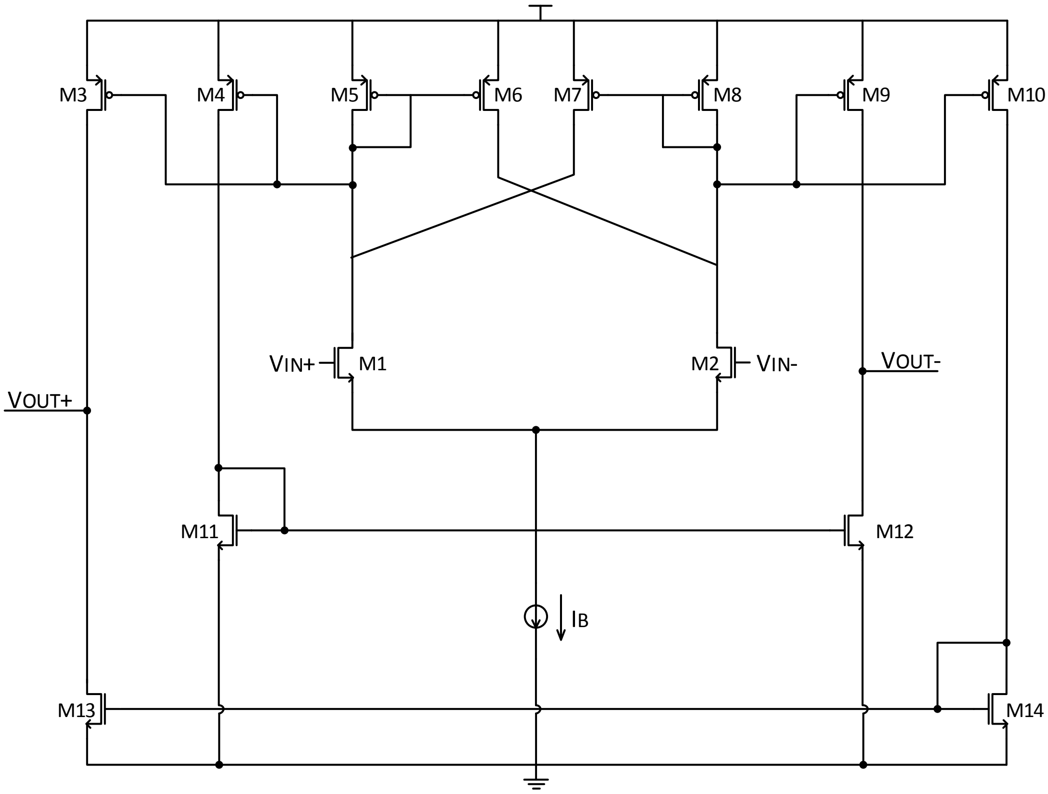

Figure 3-4: Schematic diagram of the Schmitt trigger

The Schmitt trigger is implemented as a hysteresis comparator [23] in order to convert an analog differential signal whose common-mode voltage is 1.65V to a digital differential signal. When the input signal is higher than the threshold voltage, the output voltage for this signal will be 3.3V, which is the logic 1 in this process. On the contrary, when the input signal is lower than the threshold voltage, the output is 0V which is logic 0. The output of the Schmitt trigger will not be affected of small glitches in the input. Figure 3-5 shows the simulation result of the Schmitt trigger. 50mV hysteresis can be observed.

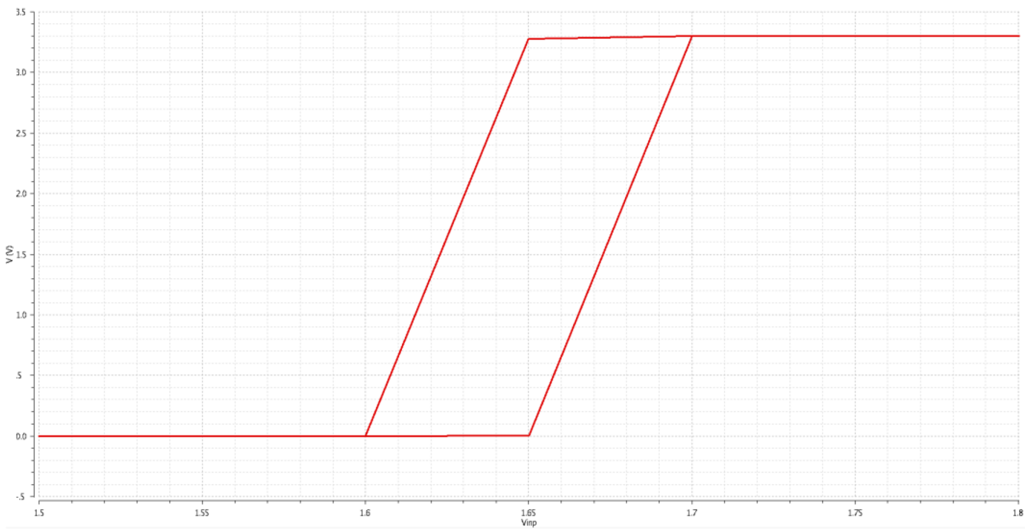

Figure 3-5: Simulation result of the Schmitt Trigger

3.3 Buffer Stage

Buffer stage is the last stage of the proposed LVDS receiver. In this stage the differential signals are buffered by the inverter chain. Figure 3-6 shows the buffer stage of the receiver. Drive strength of the buffers can be controlled by 3 bits generated by the memory unit. Drive strength can be weakened for slower operations in order to decrease power dissipation.

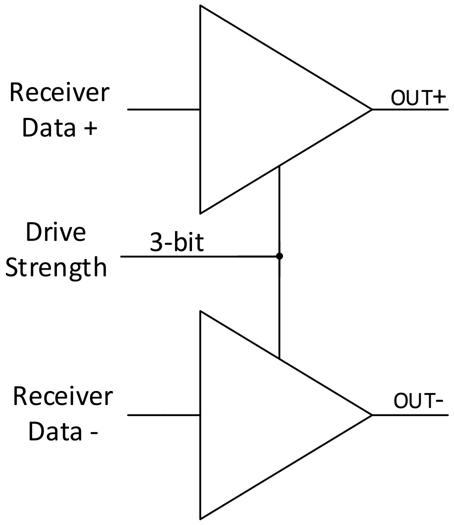

Figure 3-6: Buffer stage of the receiver

3.4 Input Termination Resistor

Differential termination resistor should be connected across the input of the receiver. If this termination resistor is placed on the PCB, it should be placed near the receiver as close as possible. In this receiver design, termination resistor is implemented between the input pads of the receiver in the chip. If 100Ω termination resistor is not placed on the PCB this termination resistor can be used. This resistor can be activated by configuring the related bit in the memory. When the enable signal is active, a total 100Ω is connected between the inputs of the receiver. Figure 3-7 shows the termination resistor across the receiver inputs.

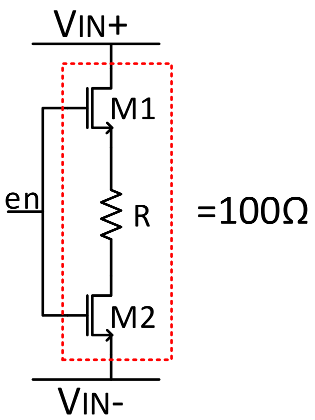

Figure 3-7: Termination resistor across the receiver inputs

In the normal operation of the receiver, 3.5 mA current passes through this resistor and its layout should be drawn accordingly.

Figure 3-8 shows the top level schematic diagram of the receiver. Figure 3-9 shows the top level layout of the receiver. The left-most block is the preamplifier. The middle block is the Schmitt trigger and the right-most block is the buffer stage.

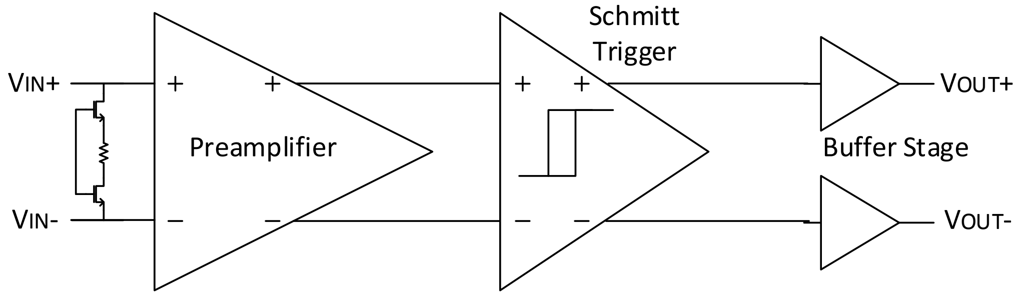

Figure 3-8: Top level schematic diagram of the receiver

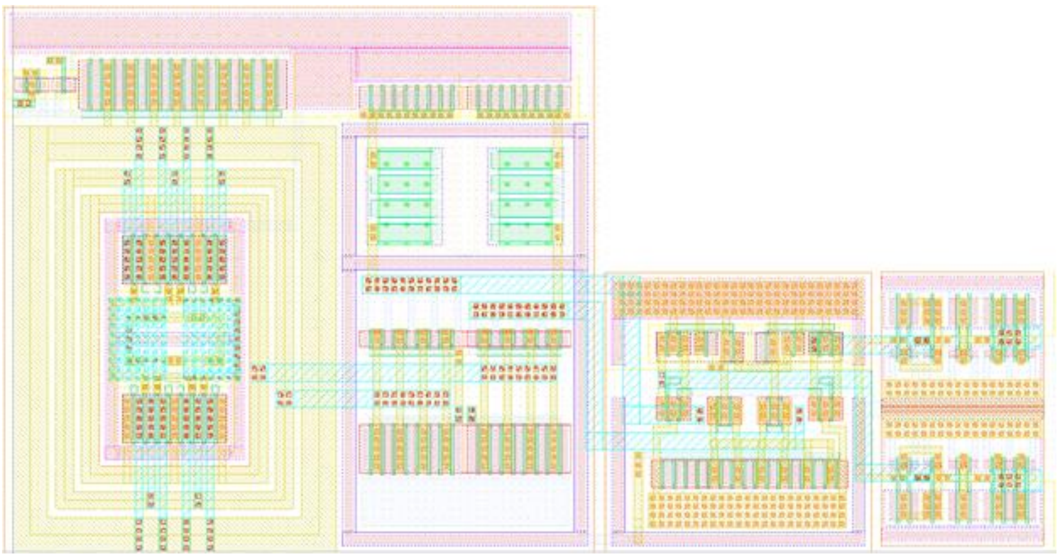

Figure 3-9: Top level layout of the receiver. It measures 60µm in height and 120 µm in width in a 0.35 µm CMOS technology.

Table 3-2 shows the LVDS receiver performance comparison with other works.

Table 3-2: LVDS receiver performance comparison

	[30] 1996	**[16] 2001**	**[29] 2002**	**This Work**
Process (µm)	0.35	0.35	0.35	0.35
Power Consumption(mW)	-	30 @ 3.3V	-	6 @ 3.3V
Maximum Data Rate (Gbps)	0.2	1	1	2
Unit Power (mW/Gbps)	-	30	-	4

CHAPTER 4

TEST CHIP IMPLEMENTATION

In this chip there are 5 main elements: High speed I/O Ports, LVDS Transmitter and LVDS Receiver, serializer, bias circuitry and serial programming interface. LVDS Transmitter and LVDS Receiver design and implementation are explained in detail in Chapters 2 and 3 respectively. In this chapter, the remaining parts are explained in detail and the full chip implementation is shown.

4.1 Serializer

Serializer basically converts a parallel digital data into a high speed serial bit stream. Serializers are usually implemented to decrease the number of digital I/O pads. By means of the serializer parallel data can be transmitted as serial data over a single output pad, at the expense of increasing the minimum required operation speed for the same bitrate. For example 16:1 serializer needs 16 times faster clock signal than the parallel data sampling clock signal if operating with single-data-rate (SDR) which means data is transferred at a single edge of the clock, as opposed to double-data-rate (DDR) which utilizes both edges to transmit the data.

In this test chip the serializer is designed to receive 16 bit parallel data from outside world with slow sample rate and to transmit high speed data to the LVDS transmitter input. The serializer consists of two main parts: (1) shift register elements and (2) signal generator.

4.1.1 Shift Registers

Serializer can be defined as a sequential shift register. Shift registers are designed with a 2:1 multiplexer and a D-flip flop. Figure 4-1 shows the schematic diagram of a 1-bit shift register. At the rising edge of the fast clock, if shift_load signal is low, the data is loaded to the register but if the shift_load signal is high, the data from the previous register (input signal) is loaded.

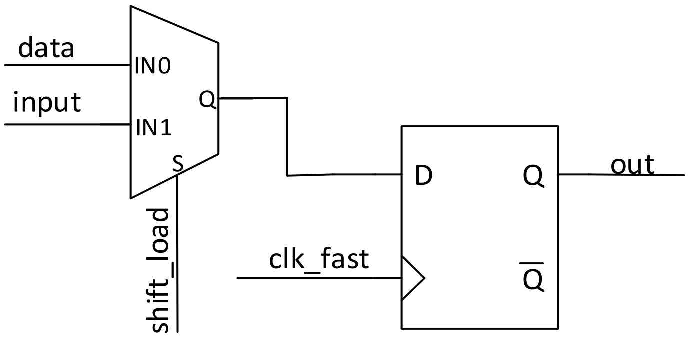

Figure 4-1: Schematic diagram of the 1-bit shift register

Shift register blocks are designed for a maximum 1.5 Gb/s data rate to provide optimum speed and power consumption for LVDS transmitter testing. Serializer is designed to operate in Double-Data-Rate (DDR) which means that the data is transferred on both falling and rising edges of the clock. Shift registers inside the serializer are grouped as even and odd registers. Figure 4-2 shows the schematic diagram of the shift registers and the output multiplexer. Even registers sample the data at the rising edge and odd registers sample the data at the falling edge of the fast clock. The output serial data is selected by the 2:1 output multiplexer using clock signal as the select bit. The logic value of the clock signal chooses the even or odd data. When the clock is at high, data from the even register is selected and when the clock is low, data from odd register is selected for the serial output data. The least significant bit of the data is transmitted first.

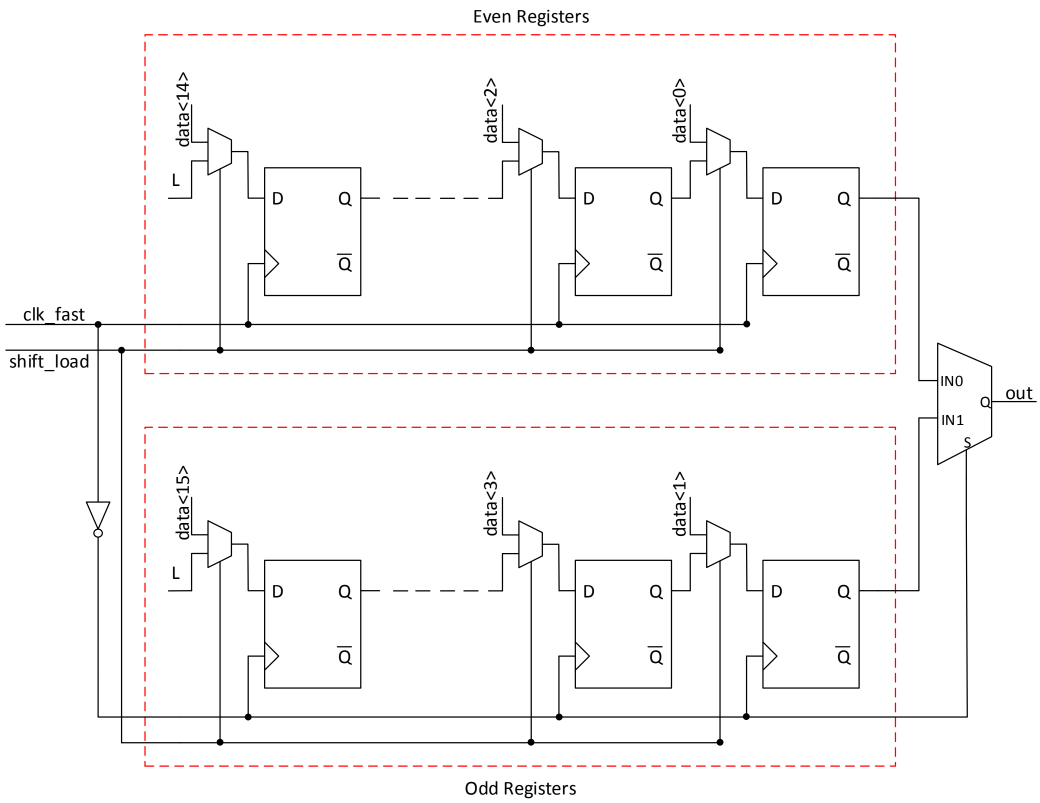

Figure 4-2: Schematic diagram of the shift registers and the output multiplexer

4.1.2 Signal Generator

The signal generator consists of four blocks: (1) Equal Delay Buffer, (2) Shift/load Signal Generator, (3) Selective Delay Cell and (4) Frequency Divider.

Serializer uses two different speed clocks in order to sample and transfer the parallel data to a serial data stream. Slow clock is used to load the parallel data to the registers and fast clock is used to shift the data in the registers. Figure 4-3 shows the schematic diagram of the slow clock generator which is generated from the fast clock by means of the frequency divider.

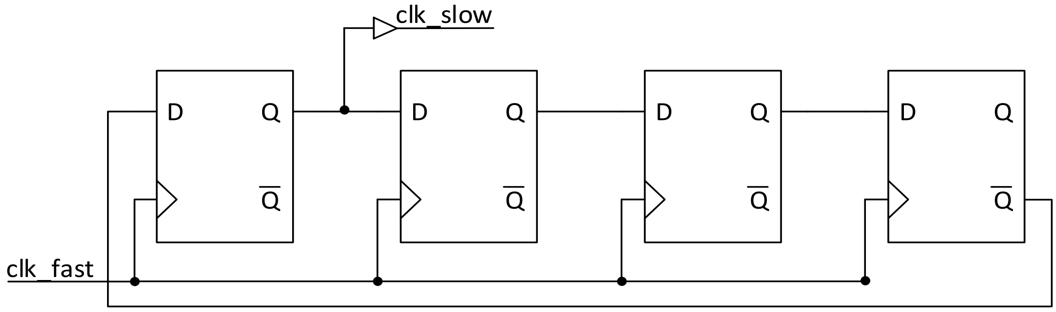

Figure 4-3: Schematic diagram of the slow clock generator (Johnson Counter)

Frequency divider is implemented with Johnson Counter. Since the 16:1 serializer operates in DDR mode, slow clock needs to be 8 times slower than the fast clock. For example, when fast clock is 1 GHz then slow clock is generated as 125 MHz to load the parallel data. The data rate for this example is 2 Gb/s.

The fast clock can be delayed with the delay cell. The delay cell is designed to delay the fast clock with 450ps steps up to 3.6ns.The fast clock can also be inverted to arrange the sampling point.

The serializer needs shift/load signal for the load and shift activity. When the shift/load signal is low, the data is loaded to the registers and when the shift/load signal is high the registers shift the data to the next register at each sample instant. Shift/load signal is generated inside the serializer. This signal controls the 2:1 Mux in the shift register.

Figure 4-4 shows the schematic diagram of the shift/load and the data frame clock generator. The data frame clock signal is also generated in order to denote the starting instance of the frame. 16-bit frame starts at the rising edge of the data frame clock.

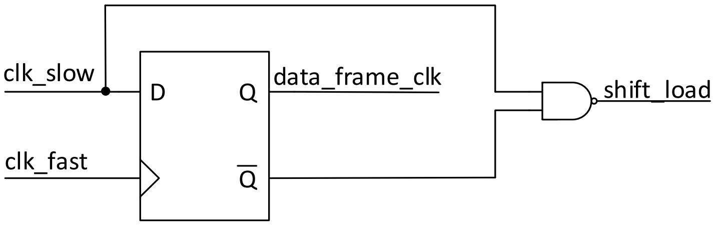

Figure 4-4: Schematic diagram of the shift load and data frame clock generator

The serializer needs fast clock and its inverse for odd and even registers in the shift registers. In order to generate the inverted clock signal, equal delayed buffer cell is designed. This cell invert the fast clock and delays both inverted and the original fast clock signals equally. There is no phase difference between these signals.

Figure 4-5 shows the timing of the all signals (parallel data, fast clock, inverted fast clock, slow clock, shift/load, data frame clock, and serial output data) in the serializer.

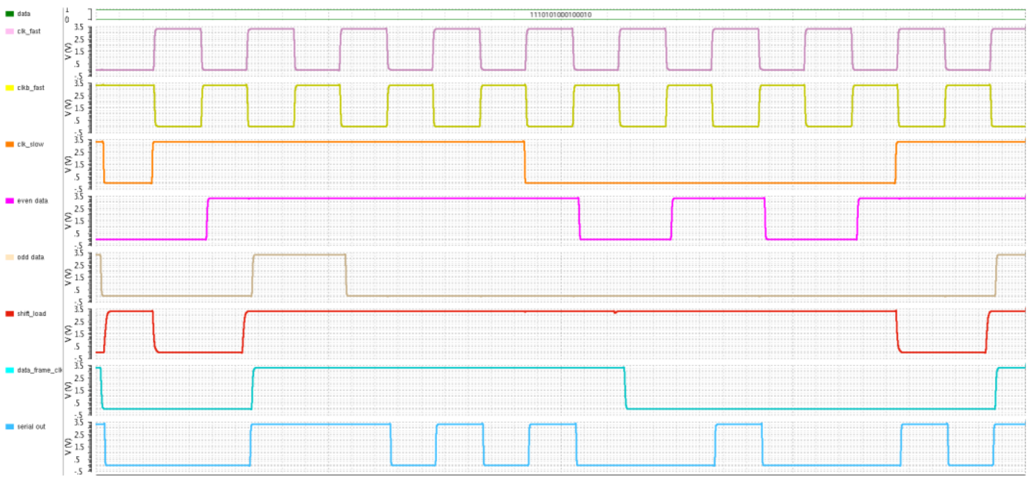

Figure 4-5: Timing signals of the serializer

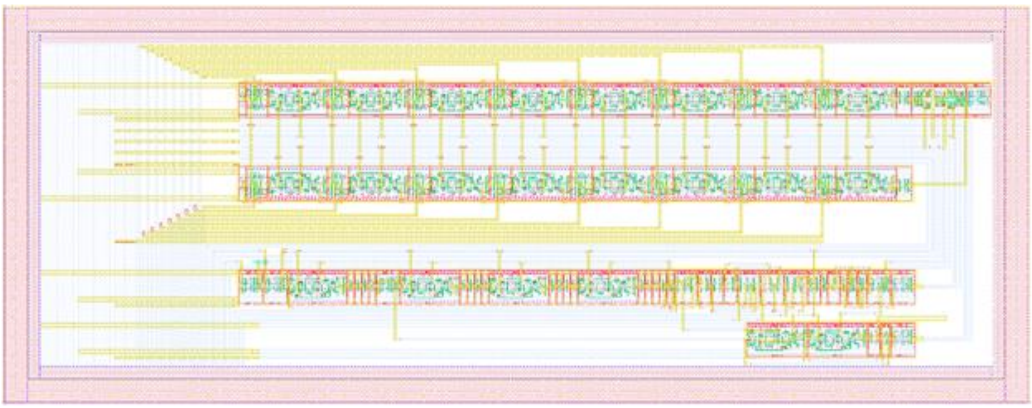

Figure 4-6: Layout of the serializer. It measures 180 µm in height and 475 µm in width in a 0.35 µm CMOS technology.

4.2 Bias Circuitry for LVDS Transmitter and Receiver

LVDS transmitter and receiver needs some bias voltages and currents for their operational amplifiers. In addition, the LVDS transmitter needs reference voltage for common mode voltage. The bias generator is implemented as configurable.

The bias current for driver is generated with the help of the current mirror. Figure 4-7 shows the driver current generation schematic in the bias circuitry by means of the current mirror. The current is multiplied with 35.

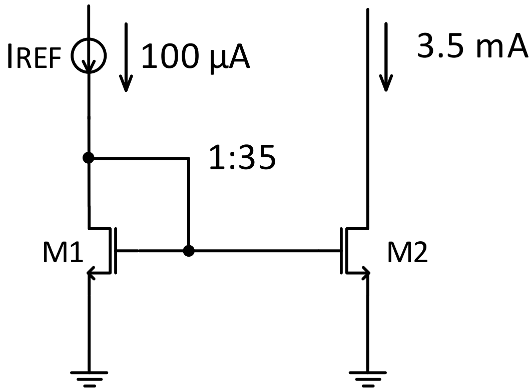

Figure 4-7: The driver current generation

The bias currents for OPAMPs of the transmitter and receiver are also generated from the reference current. The voltage to current converters convert the current to voltage needed for the gate voltages of the folded cascode transistors.

LVDS transmitter also needs a reference voltage for the common mode voltage of the driver. In some LVDS applications this reference voltage is generated outside the chip, but generating this voltage in the chip is better in terms of noise issues and minimizing the PCB complexity. Reference voltage is chosen as 1.2V for this chip and generated with resistive division. Figure 4-8 shows the schematic diagram of the reference voltage generator. The ratio of the resistors are:

$$\frac{R1}{R2} = \frac{7}{4}$$

The capacitor array (C_{REF}) is also placed between the output and the ground for noise suppression.

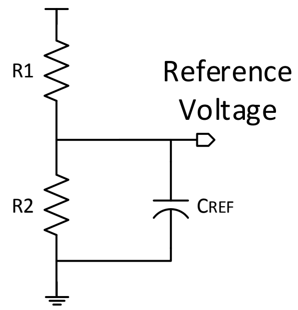

Figure 4-8: Schematic diagram of the reference voltage generator

Figure 4-9 shows the layout of the LVDS transmitter and receiver bias circuitry.

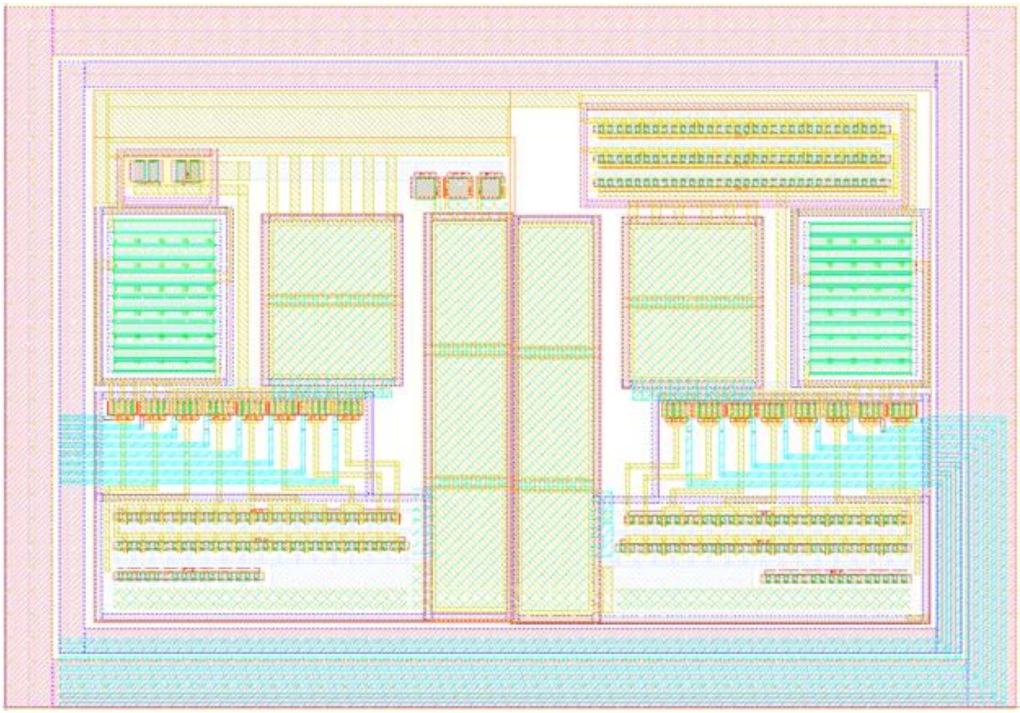

Figure 4-9: Layout of the LVDS transmitter and receiver bias circuitry. It measures 150 μm in height and 220 μm in width in a 0.35 μm CMOS technology.

4.3 Serial Programming Interface (SPI)

Serial programming interface provides the communication of the chip with FPGA and programs the blocks of the chip for different modes of operation. SPI is designed as serial shift registers. Figure 4-10 shows the block diagram of the SPI.

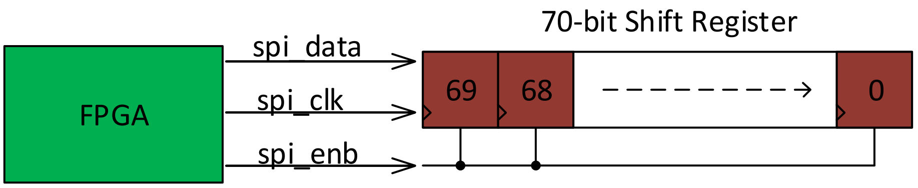

Figure 4-10: Block diagram of the SPI with FPGA

SPI uses 3-wire communication. These communication signals are: Serial Input Data, Clock Signal and Active Low Enable Signal. In order to communicate with the chip properly, the signals of SPI (spi_data, spi_clk, and spi_enb) should be sent from the FPGA. Figure 4-11 shows the SPI timing signals.

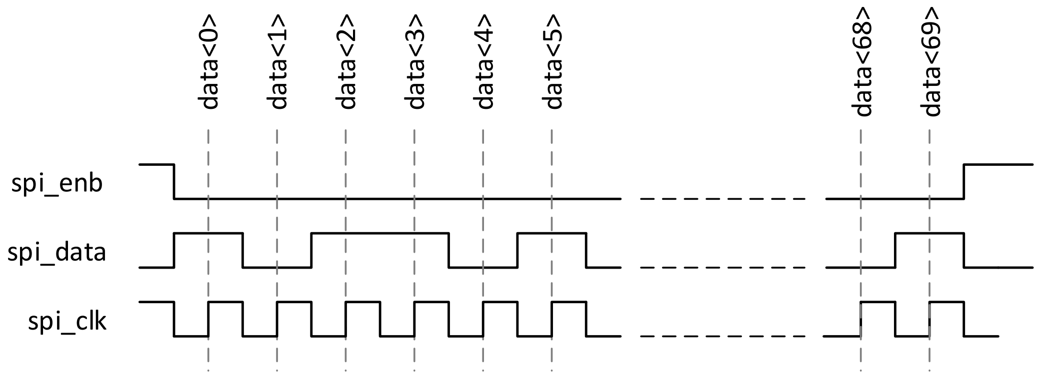

Figure 4-11: SPI timing signals

SPI can be defined as a memory element having writing and reading modes and 70 bits of memory. The FPGA should be programmed for writing the desired data to the desired sequence. The least significant bit of the data should be sent first and the data should be changed at the falling edge of the clock, because the data is sampled to the memory at the rising edge of the clock. After the spi_enb signal performs a transition from low to high, write process is finished. In order to read all the data from the memory spi_enb signal should stay in logic-0 for 70 clock cycles like in the write process. The data is read from the spi_out pad in the order of writing sequence. SPI is not designed as an address based memory, due to the low number of configuration bits required. In order to change a single bit, whole memory needs to be rewritten. Writing the memory only takes 70 clock cycles. For example, if the clock is 100 MHz then writing and reading process only takes 700 ns.

Serial programming interface configures LVDS transmitter, receiver, serializer, and bias circuitry. Test data for LVDS transmitter is generated by the SPI. Table 4-1 shows the SPI configuration bits of the LVDS test chip.

Table 4-1: SPI configuration bits of the LVDS test chip

Programmed Interface	Word Length	Explanation
LVDS Receiver	5	Power down, termination enable, buffer drive strength(3)
LVDS Transmitter (DATA)	8	Power down, termination enable, high current mode, buffer drive strength(3), pre-emphasis(2)
LVDS Transmitter (FRAME CLOCK)	6	Power down, termination enable, high current mode, buffer drive strength(3)
Serializer	3	Serializer clock delay bits(3)
Bias Circuitry	32	LVDS transmitter and receiver bias circuitry bits(2x16)
Test Data	16	Test data for LVDS transmitter

Figure 4-12 shows the layout of the SPI. It measures 525 μm in height and 650 μm in width in a 0.35 μm CMOS technology.

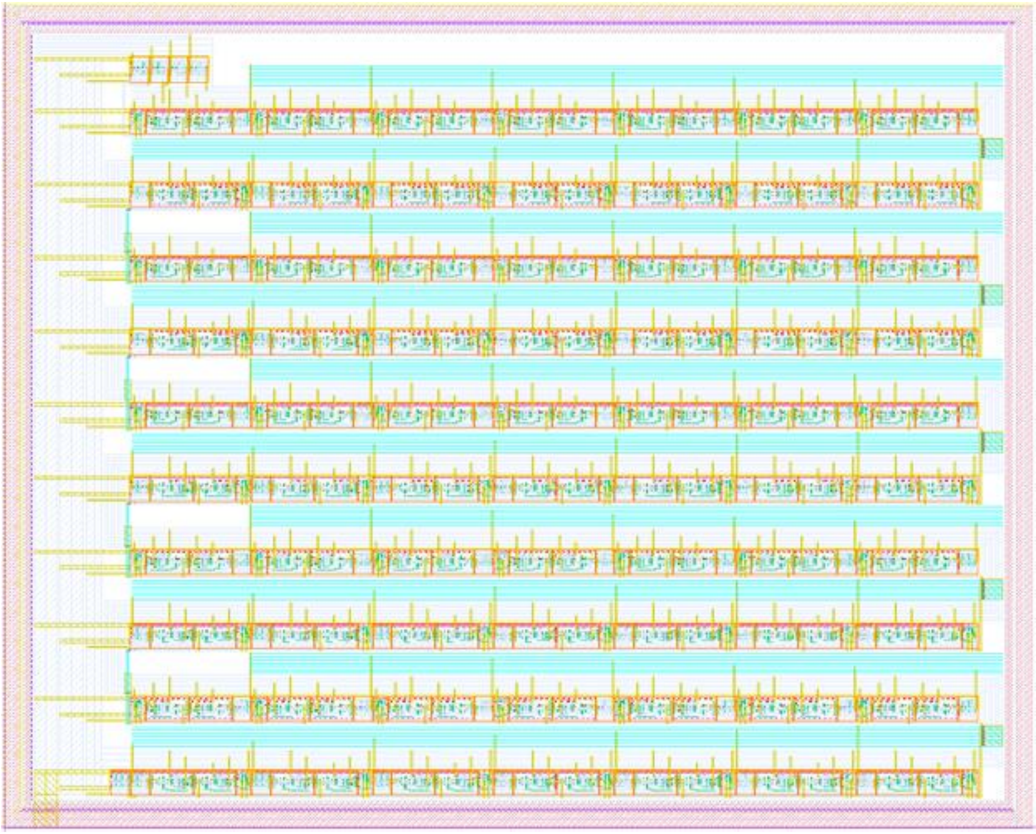

Figure 4-12: Layout of the SPI. It measures 525 μm in height and 650 μm in width in a 0.35 μm CMOS technology.

4.4 Top Level Integration

LVDS test chip includes two LVDS transmitter, a LVDS receiver, a serializer, bias circuitry for transmitter and receiver, and serial programming interface. Figure 4-13 shows the block diagram of the LVDS test chip.

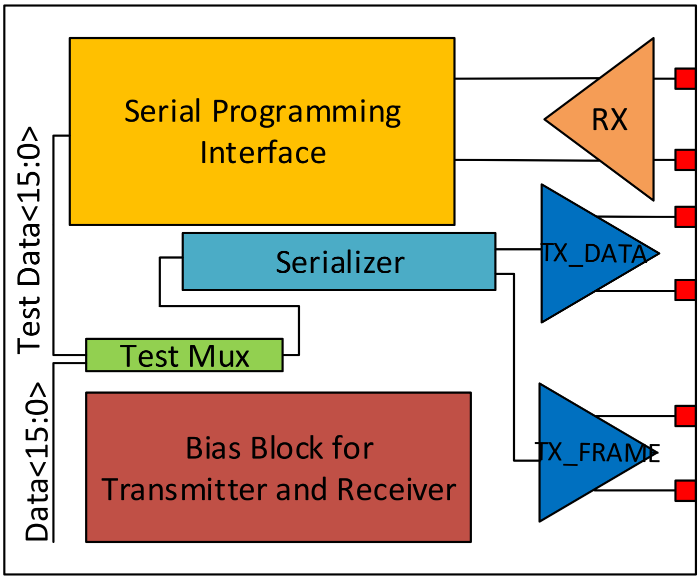

Figure 4-13: Block diagram of the LVDS test chip

Layouts of all the blocks are combined and the top-level layout is created. Figure 4-14 shows the floor-plan of the LVDS test chip. The LVDS transmitter and receiver is designed to be placed between the pads so they are very dense and small in terms of layout area. There are two transmitter ports in this test chip. One of them transmits the data and the other transmits the data frame clock which shows the beginning and the ending instances of the data. Data frame clock is used for sampling the data in the FPGA. This issue will be explained in the simulation and the test chapter.

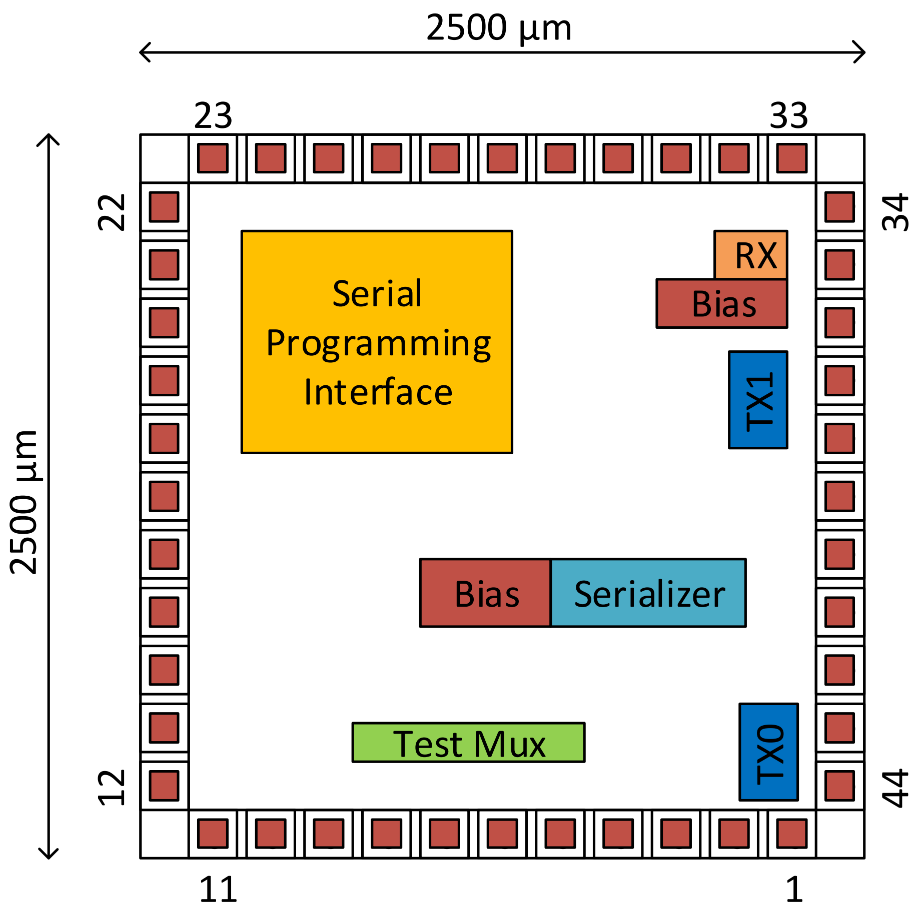

Figure 4-14: Floor-plan of the LVDS test chip

Serializer is placed between the two transmitter ports, because data and the data frame clock is generated in the serializer and routing mismatch between the two signals should be as small as possible. The serial programming interface is placed near the SPI input pads and bias circuits are placed near the necessary blocks. Chip is pad-limited so the overall area is not very dense.

The LVDS test chip measures 2500x2500 µm in 0.35 µm CMOS process and includes total of 44 pads. Table 4-2 shows the pad list of the chip and Figure 4-15 shows the top-level layout of the LVDS test chip. Figure 4-16 shows the top view of the fabricated test chip wirebonded on the test board. LVDS transmitters, receiver, serializer and SPI is shown on the figure with white squares.

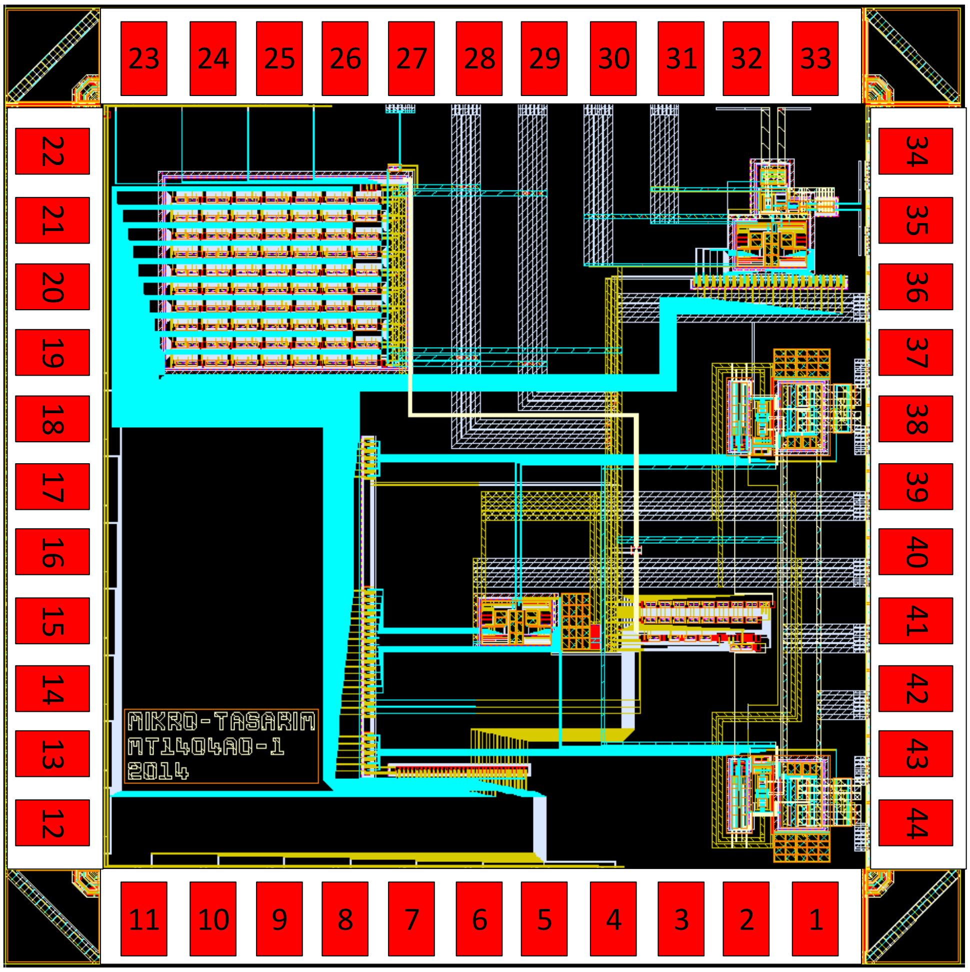

Figure 4-15: Top level layout of the LVDS test chip. It measures 2500 μm in height and 2500 μm in width in a 0.35 μm CMOS process.

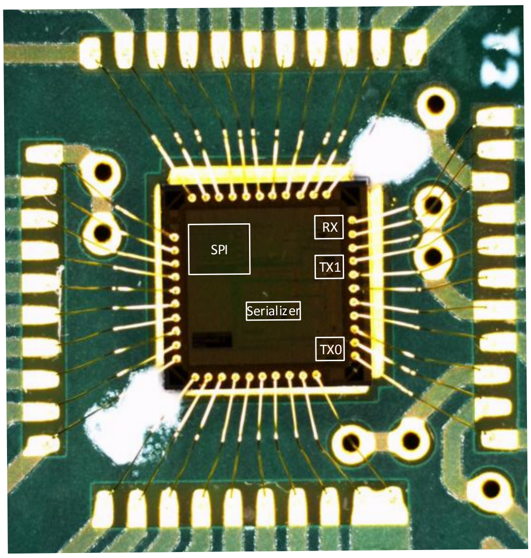

Figure 4-16: Top view of the fabricated test chip wirebonded on the test board

Table 4-2: Pad list of the LVDS Test Chip

Pad No	***Pad Name***	***Pad No***	***Pad Name***
1	ESD Ground	23	Spi_Data
2	ESD Supply	24	Spi_Latchb
3	Pad Supply	25	Rstb
4	Digital Data<0>	26	Sys Clk
5	Digital Data<1>	27	Sdout
6	Digital Data<2>	28	Digital Supply (3.3V)
7	Digital Data<3>	29	Digital Ground
8	Digital Data<4>	30	Analog Ground
9	Digital Data<5>	31	Analog Supply (3.3V)
10	Digital Data<6>	32	RX INP
11	Digital Data<7>	33	RX INN
12	Digital Data<8>	34	RX OUTP
13	Digital Data<9>	35	RX OUTN
14	Digital Data <10>	36	Analog Ground
15	Digital Data<11>	37	TX1 OUTN
16	Digital Data<12>	38	TX1 OUTP
17	Digital Data<13>	39	Analog Supply (3.3V)
18	Digital Data<14>	40	Analog Ground
19	Digital Data<15>	41	Analog Ground
20	Analog Ground	42	Analog Supply (2.5V)
21	Pad Ground	43	TX0 OUTP
22	ESD Ground	44	TX0 OUTN

CHAPTER 5

SIMULATIONS AND TEST RESULTS

This chapter presents the simulation results of LVDS chip and test setup. All simulations are performed using spice circuit level simulator. Simulation results of LVDS transmitter, LVDS receiver, and serializer is shown in section 5.1, 5.2, and 5.3 respectively. In Section 5.4 test setup is explained.

5.1 LVDS Transmitter Simulation Results

In this section, simulation results of the LVDS transmitter is shown. LVDS transmitter is designed for transmitting digital CMOS data up to 1.5 Gb/s data rate, however for different data rates, simulation results are obtained in order to compare with each other. All the simulations include the effect of bond-pads' and bond-wires' parasitic elements, and the PCB's micro strip lines. Figure 5-1 shows the simulation result showing the LVDS transmitter output with input data at 500Mb/s data rate. The output data is transmitted with approximately 1 ns of propagation delay. Figure 5-2 shows the simulation result showing the LVDS transmitter output with input data at 1 Gb/s data rate. Figure 5-3 shows simulation result showing the LVDS transmitter output with input data at 1.5 Gb/s data rate. The LVDS data can be received by the receiver and converted to CMOS digital data. All the simulations include all parasitic elements.

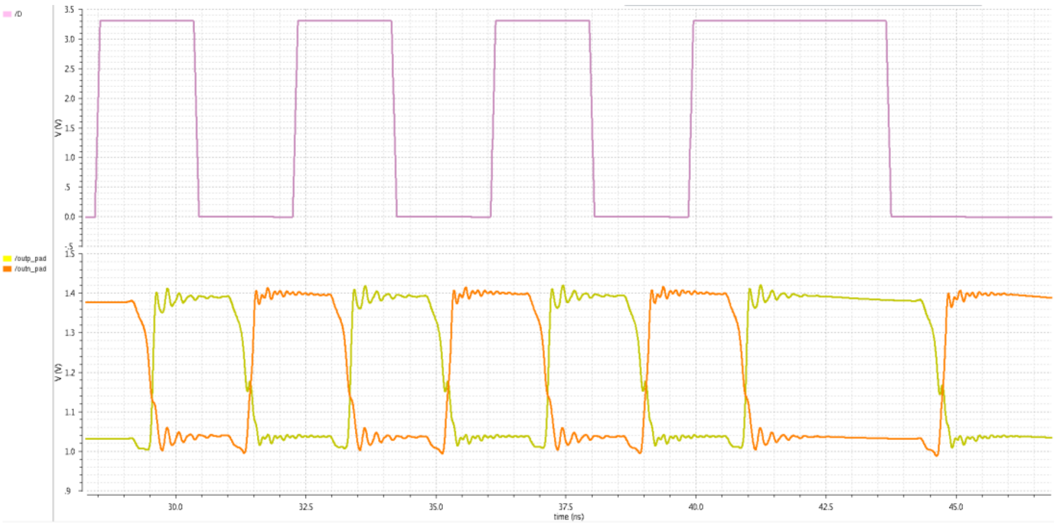

Figure 5-1: Simulation result showing the LVDS transmitter output with input data at 500Mb/s data rate

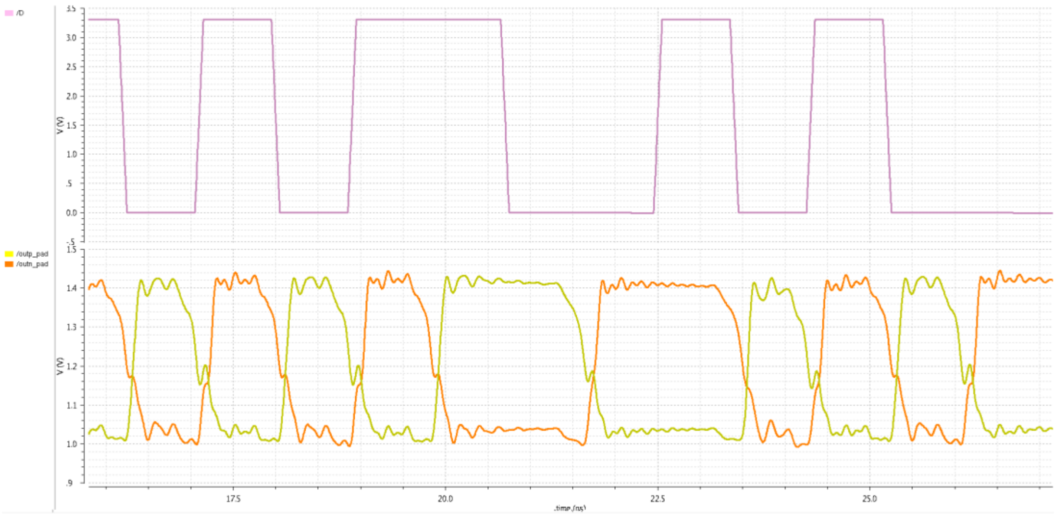

Figure 5-2: Simulation result showing the LVDS transmitter output with input data at 1Gb/s data rate

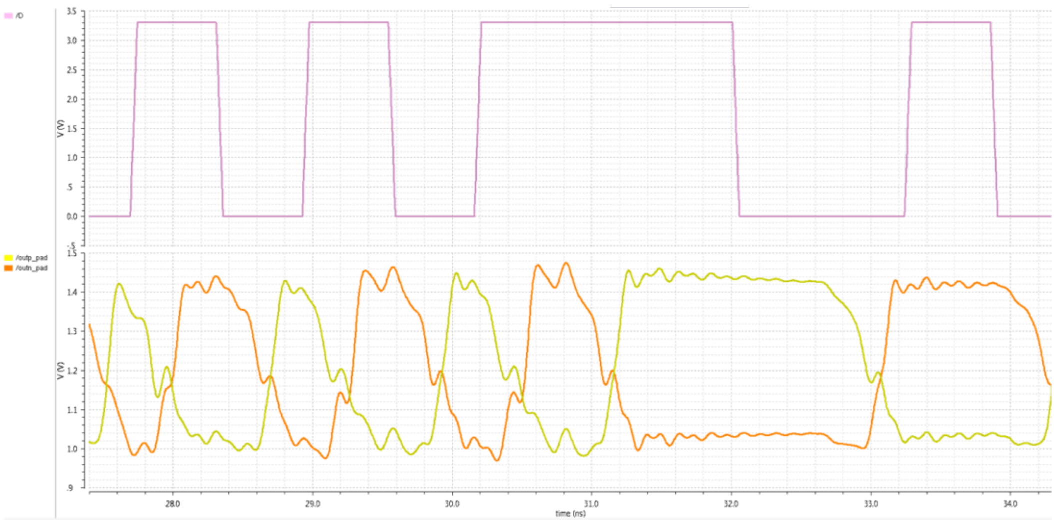

Figure 5-3: Simulation result showing the LVDS transmitter output with input data at 1.5Gb/s data rate

In order to show the effect of the pre-emphasis technique on the LVDS output signal, conventional driver and driver with pre-emphasis circuits are simulated and the results are appended. Figure 5-4 shows the simulation result of these circuits. The red and pink signals shows the w/o pre-emphasis and with pre-emphasis output signals respectively.

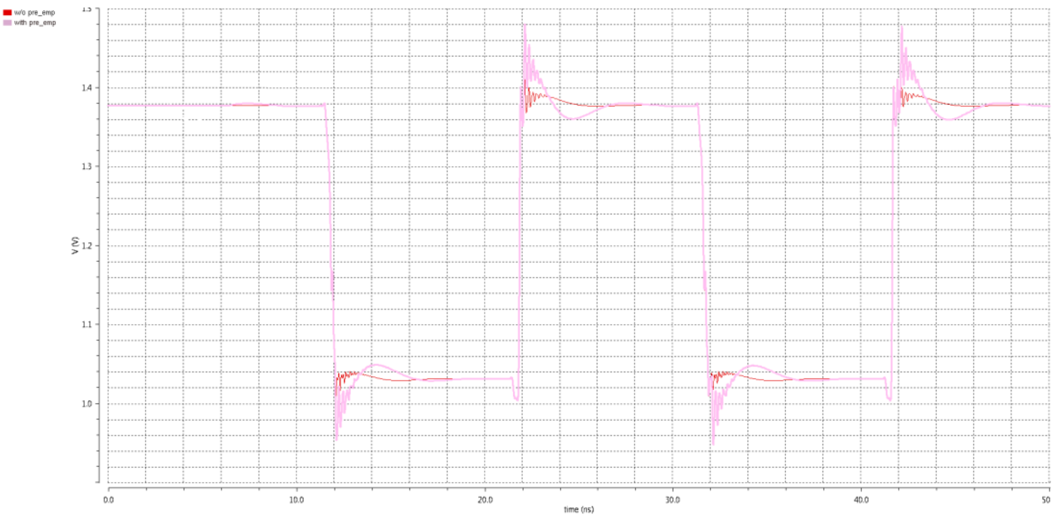

Figure 5-4: Simulation result of the conventional driver and driver with pre-emphasis

5.2 LVDS Receiver Simulation Results

In this section, simulation results of the LVDS receiver is shown. LVDS receiver is designed for receiving LVDS data and convert it to digital CMOS data up to 2 Gb/s data rate. The simulation results include 1.5 Gb/s and 2 Gb/s data rates. All the simulations include the effect of bond-pads' and bond-wires' parasitic elements, and the PCB's micro strip lines. Figure 5-5 shows simulation result of LVDS receiver differential ended output data with input LVDS data at 1.5 Gb/s data rate. LVDS data is transmitted by the designed LVDS transmitter for this simulation. The output data is with approximately 2.2 ns of propagation delay. The rise and fall time of the output CMOS data is about 80ps. Figure 5-6 shows simulation result of LVDS receiver single ended output data at 2 Gb/s data rate. The rise and fall time of the output CMOS data is about 100ps. In this simulation LVDS data is given by the simulation voltage sources. All the simulations include all parasitic elements.

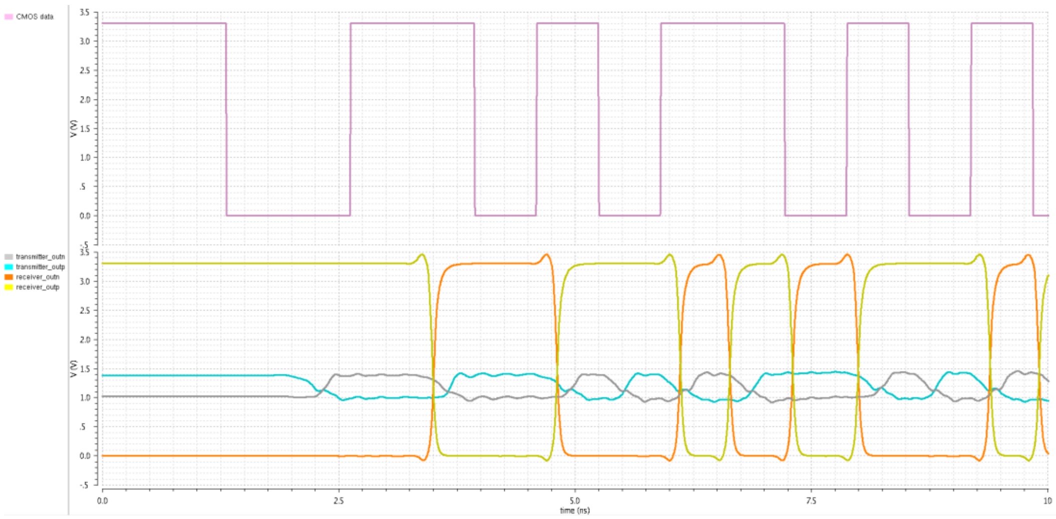

Figure 5-5: Simulation result of LVDS receiver differential ended output data with input LVDS data at 1.5 Gb/s data rate

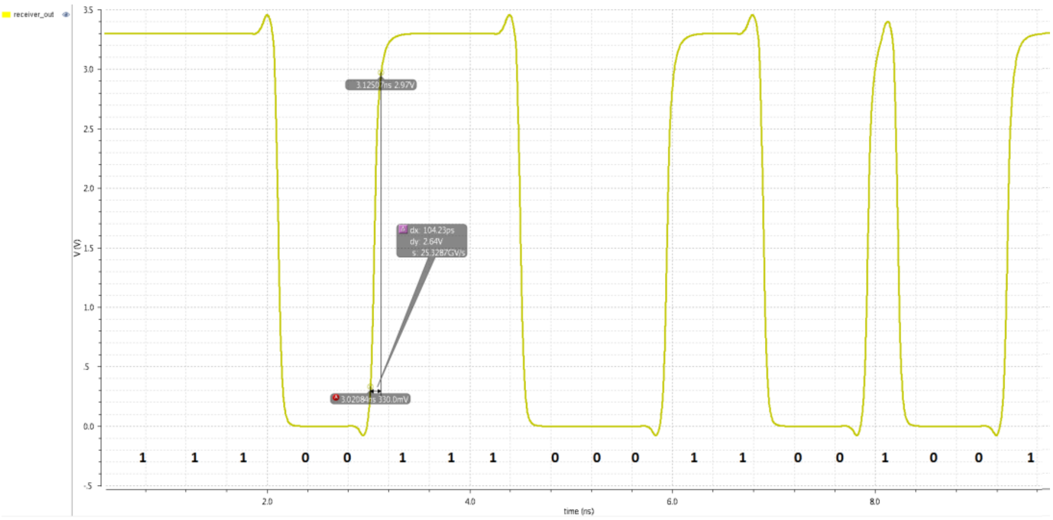

Figure 5-6: Simulation result of LVDS receiver single ended output data at 2 Gb/s data rate

5.3 Serializer Simulation Results

In this section simulation results of the serializer is shown. Serializer is designed for converting the 200 MHz 16-bit parallel data to 1.6 Gb/s serial data. In this simulation 750 MHz clock is used to serialize 16 bit data. Figure 5-7 shows the serializer simulation result at 1.5 Gb/s data rate. Rising edge of the data_frame_clk signal shows the beginning of the frame. Parallel data is chosen as 1110101000100010. The left-most data is the least significant bit (LSB) of the parallel data. The serializer is designed to send the least significant bit of the data first. The data is loaded when shift_load signal is low and shifted when the shift_load signal is high. The serial data can be observed in the figure.

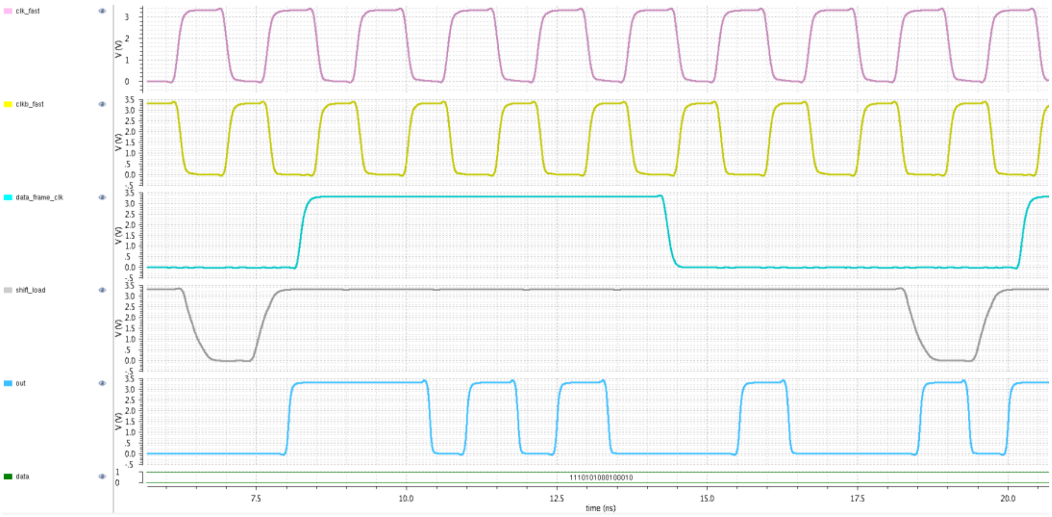

Figure 5-7: Serializer simulation result at 1.5 Gb/s data rate with 750Mhz clock 16-bit parallel data: 1110101000100010

5.4 Test Setup

This part of the thesis focused on the test setup of the LVDS chip. The test setup consists of a custom designed test board, test software and firmware. In the following sections design of the test board, software and firmware will be explained in detail.

5.4.1 Test Board

The test board is designed to test the LVDS test chip without need for anything else. The test board includes voltage regulators of the chip for different power supplies and FPGA card for configuring the LVDS test chip. The test board is designed with PCB design tool. The layout of the test board is designed at Mikro-Tasarım. The dimensions of the test board is 5 cm x 7.5 cm.

Test board needs only one 6V supply voltage for FPGA and other elements. All the necessary supply voltages are generated by the voltage regulators on the test board. LT1762 [31] is used as voltage regulator. Figure 5-8 shows the test board of the test chip with the bonded test chip. The FPGA is placed at the bottom of the test board.

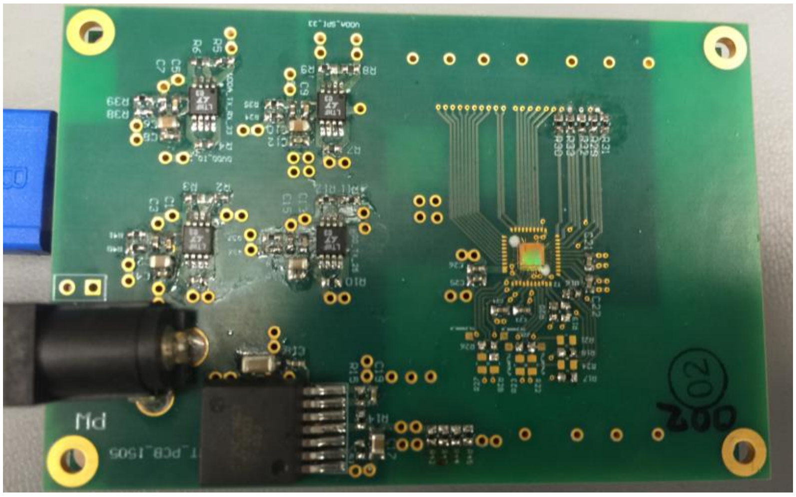

Figure 5-8: The test board of the test chip with the bonded test chip

5.4.2 Software and Firmware

Software and firmware tools are designed in order to configure the chip and observe the outputs of the chip. The chip is configured through the serial interface by means of the commercially used FPGA card OPAL Kelly XEM 6010 [32]. The outputs are observed by FPGA and oscilloscope.

5.4.2.1 Firmware

The firmware is written in Verilog and embedded to the FPGA card. The firmware consists of two main blocks. One of them is about configuring the chip and the other is about the observing the output of the chip. The configuration part generates necessary signals for SPI block of the chip. Figure 5-9 shows the simulation result of the firmware configuring the SPI block. Memory configuration data can be written to SPI registers and read from the SPI output with this firmware. The left side of the figure shows the write section and the right side of the figure shows the read section. Figure 5-10 and Figure 5-11 shows the simulation results of the write and read sections of the firmware configuring the SPI block respectively.

Figure 5-9: Simulation result of the firmware configuring the SPI block

Figure 5-10: Simulation result of the firmware (Write Section)

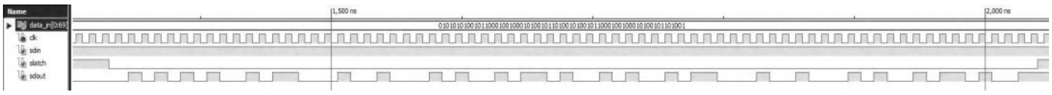

Figure 5-11: Simulation result of the firmware (Read Section)

The second part of the firmware is designed for observing the outputs of the chip. The data frame clock signal generated by the serializer and transmitted through transmitter is used to define the beginning of the data coming from the transmitter. The LVDS data is sampled at both edges of the clock.

5.4.2.2 Software

The software is written in Visual C# programming language. The software is developed at Mikro-Tasarım. The graphical user interface (GUI) of the software consists of two parts: SPI and LVDS. Figure 5-12 shows the GUI of the developed software for LVDS test chip.

SPI part of the software helps user to choose the memory configuration of the chip. First of all, firmware should be embedded to FPGA. Then chip reset and FPGA reset check boxes should be unchecked. Then necessary configurations should be done. When WRITE button is pressed, all the selected configuration is sent to chip. When READ button is pressed, the written data is read from the chip in order to be sure about the correct programming.

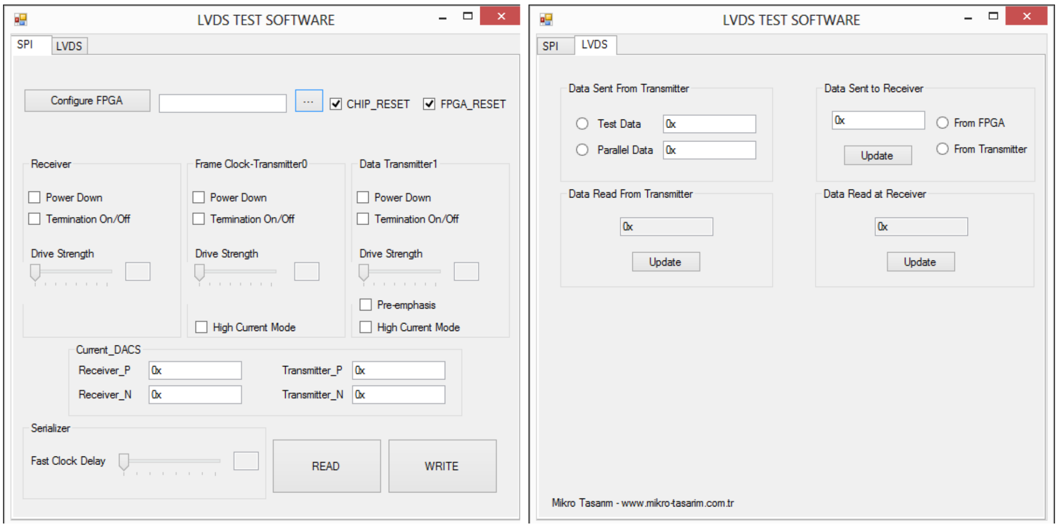

Figure 5-12: GUI of the developed software for LVDS test chip

LVDS part of the software is developed in order to observe the outputs easily. The transmitter data can be connected to receiver or receiver inputs can be driven by the FPGA. The LVDS data is read with the help of the frame clock signal generated by the serializer. The start and end points of the frame is defined by this signal. All test steps are implemented in this part.

5.5 Test Results

Test chip is fabricated and wire bonded to the test card with the help of METU MEMS Center. Figure 5-13 shows the test chip which is bonded to the test card by ball type bonder.

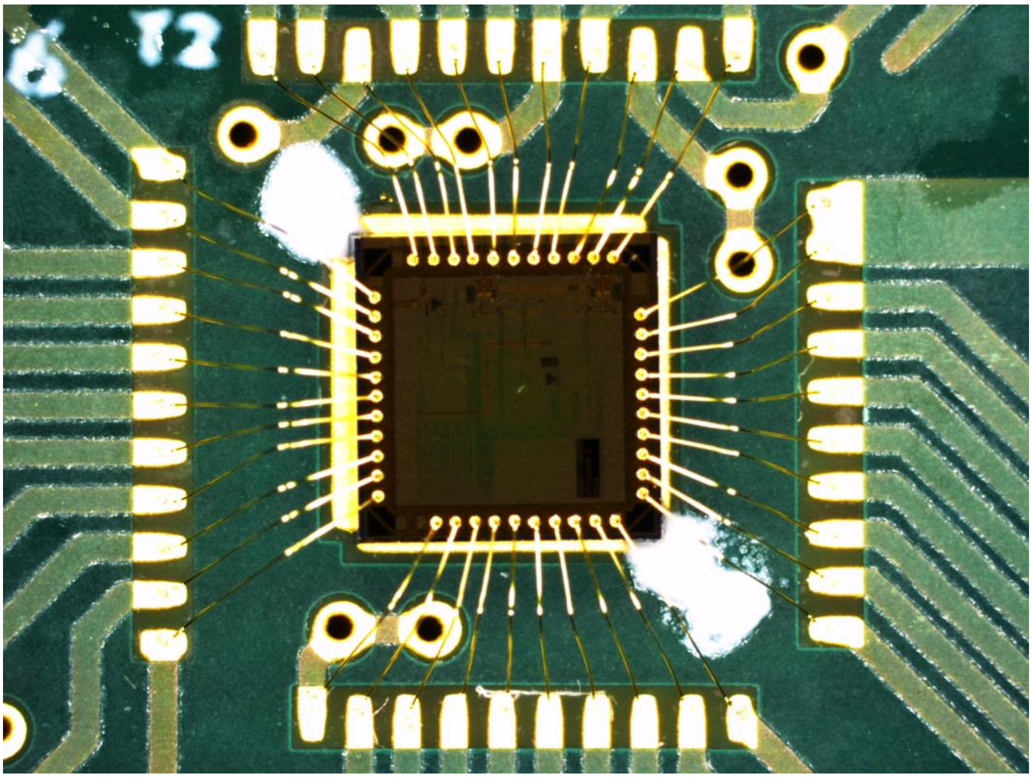

Figure 5-13: Test chip bonded to the test board by ball type bonder. The dimensions of the test chip is 2.5 mm x 2.5 mm.

First test is programming the SPI of the test chip. SPI is programmed by means of the FPGA which is placed at the bottom of the test card. Figure 5-14 shows measured test result of the SPI. After programming the test chip two LVDS transmitters and a receiver is activated. The bias generator and serializer are programmed.

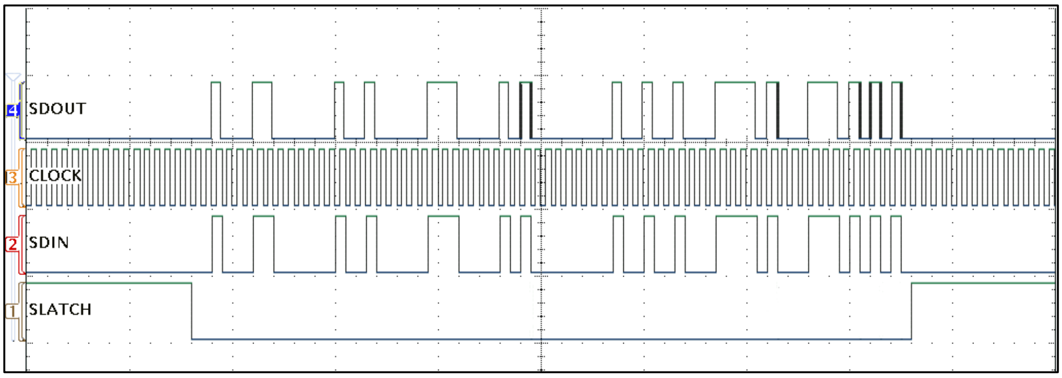

Figure 5-14: Measured test result of the SPI

First of all power analysis is done for LVDS transmitter and receiver. The test results are very similar to the simulation results. The measured power consumption of the LVDS transmitter and receiver are 20 mW and 4.5 mW @ 400 Mb/s data rate, respectively. All modes are activated and tested for the LVDS transmitters. Figure 5-15 shows measured LVDS transmitter test result with pre-emphasis at 5 ns bit rate corresponding to 200 Mb/s. Figure 5-16 shows measured LVDS transmitter test result without pre-emphasis at 5 ns bit rate corresponding to 200 Mb/s. The effect of the pre-emphasis can be observed easily.

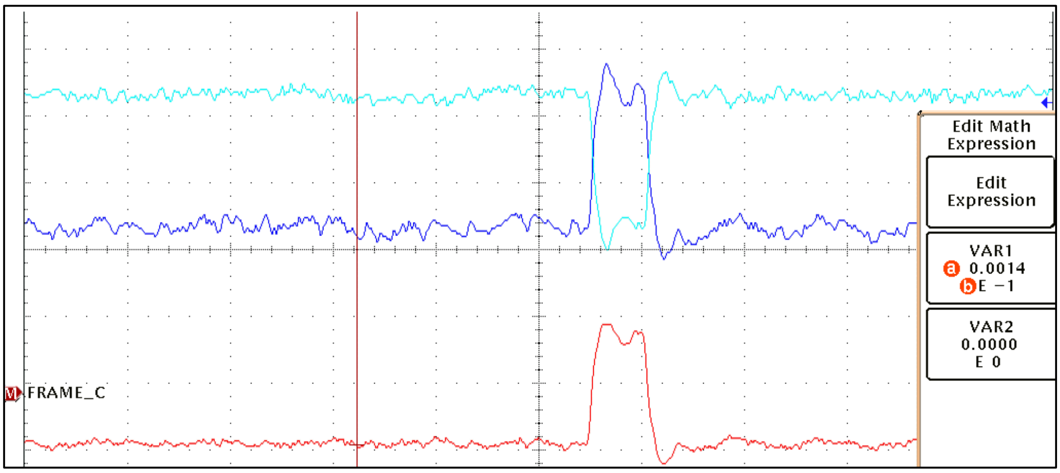

Figure 5-15: Measured LVDS transmitter test result with pre-emphasis at 5 ns bit rate corresponding to 200 Mb/s

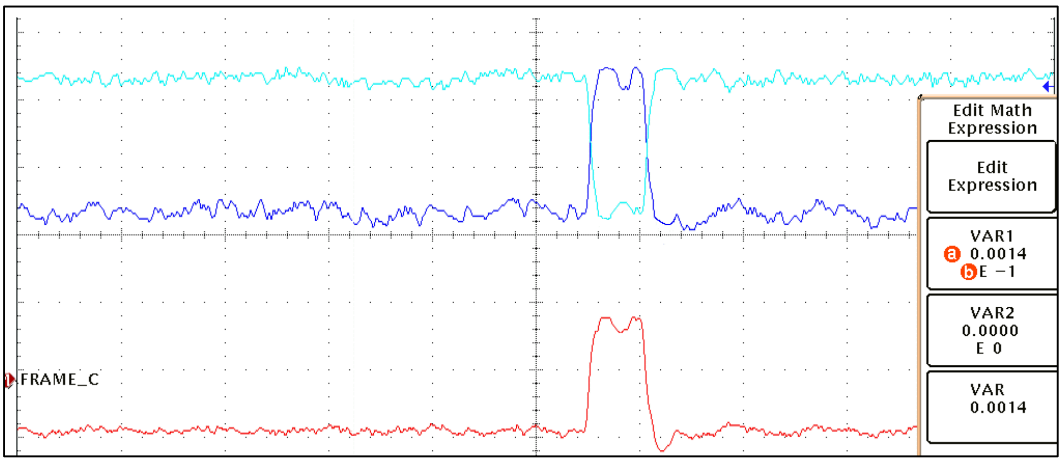

Figure 5-16: Measured LVDS transmitter test result without pre-emphasis at 5 ns bit rate corresponding to 200 Mb/s

After testing all the modes, the parallel data is given to the test chip and serializer converts the parallel data into the serial data. The serial data is observed by the LVDS transmitters. Frame clock and the data are observed by the two LVDS transmitters. Figure 5-17 shows measured serializer output thru LVDS transmitter with frame clock at 400 Mb/s data rate. Top two signals are outputs of the data transmitter. The middle signal is the difference between the output signals of the data transmitter. The bottom signal is the frame clock signal. Rising edge of the frame clock signal shows the beginning of the frame. Parallel data is chosen as 400A (hex).

Figure 5-17: Measured serializer output thru LVDS transmitter with frame clock at 400 Mb/s data rate

In order to show the effect of changing the common mode voltage, AC signal is coupled to the common mode voltage. Changing in the common mode voltage does not affect the difference between the outputs of the LVDS signal. Frame clock signal is tested in this test. The red signal is the difference signal. Figure 5-18 shows measured LVDS transmitter output with common mode sinusoidal noise.

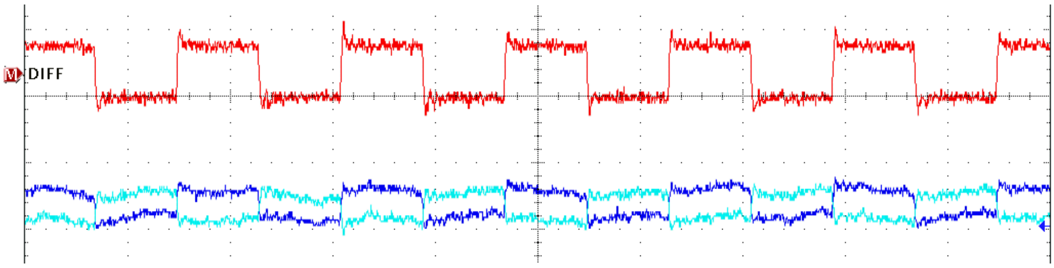

Figure 5-18: Measured LVDS transmitter output with common mode sinusoidal noise

Next, eye diagram of the LVDS transmitter will be shown. In order to show the eye diagram 16 bit pseudo random binary sequence (PRBS) generator is implemented in the FPGA. The data generated by the PRBS generator is sent to input of the receiver. Output of the receiver is sent to transmitter and the output of the transmitter is observed by the oscilloscope. Figure 5-19 shows the diagram of the test setup for measuring eye diagram. Figure 5-20 shows measured eye diagram of the LVDS transmitter at 200 Mb/s data rate.

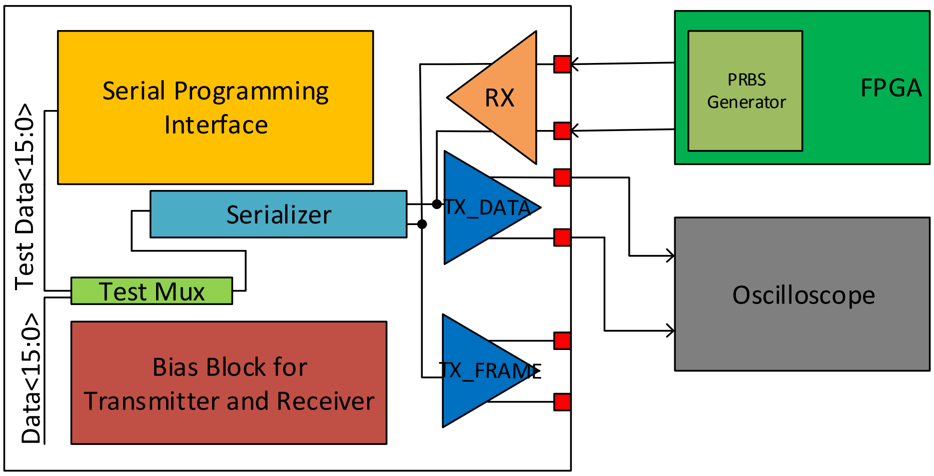

Figure 5-19: The diagram of the test setup for measuring eye diagram

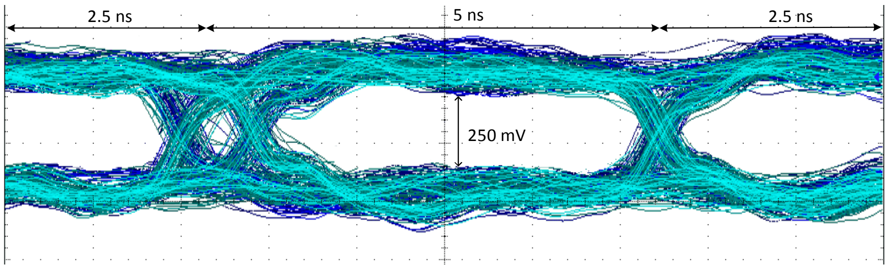

Figure 5-20: Measured eye diagram of LVDS transmitter at 200 Mb/s data rate

Finally receiver test result will be shown. The test pattern AB2A (hex) is given as parallel data to the chip. The parallel data is converted to serial data by the serializer. The serial data is transmitted thru the transmitter and connected to the input of the receiver. Figure 5-21 shows the receiver test diagram. The red arrows is observed by the oscilloscope. This digital data is also captured by the FPGA by the software.

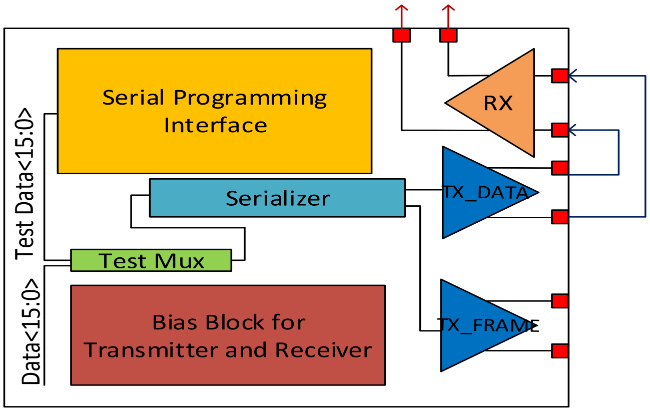

Figure 5-21: Receiver test diagram

Figure 5-22 shows the measured test result of the receiver output at 400 Mb/s data rate. The output of the receiver is CMOS.

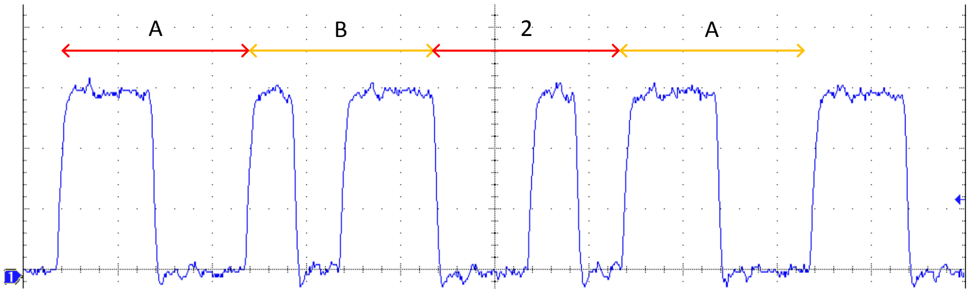

Figure 5-22: Measured test result of the receiver output at 400 Mb/s data rate

CHAPTER 6

SUMMARY AND CONCLUSIONS

The research conducted in this thesis focuses on the design of a high speed LVDS digital serial I/O interface for high resolution image sensors. The thesis begins with the high speed serial differential I/O interfaces which are appropriate for the high resolution image sensors. The designed I/O interface must be low power and low noise if it is desired to be used in an image sensor. The most appropriate topology is selected as LVDS. There are many advantages over the other most commonly used differential I/O interfaces as mentioned in the thesis.

The LVDS transmitter and receiver is designed and a test chip is implemented in order to test the I/O circuitries. The implemented test chip includes serializer, bias generator and serial programming interface circuit in order to test LVDS transmitter and receiver. The results of this work can be summarized as follows:

1. The data rate of the LVDS transmitter is 1.5 Gb/s. Power consumption of the LVDS transmitter is 45 mW at 1.5 Gb/s.
2. The reference voltage of the LVDS transmitter is 1.2 V. The voltage swing of the output voltage is 350 mV. The DC current of the driver is 3.5 mA. Termination resistor is 100Ω.
3. Pre-charge and pre-emphasis techniques are applied to the LVDS transmitter in order to decrease the jitter and increase SNR. Pre-emphasis technique can be activated by the serial programming interface.

4. The data rate of the LVDS receiver is 2 Gb/s. Power consumption of the LVDS receiver is 6 mW at 2 Gb/s.
5. The data rate of the serializer in the test chip is 1.5 Gb/s.
6. Serial programming interface can be programmed by the FPGA.
7. The test chip is implemented in a 0.35 μm CMOS process. The dimensions of the chip is 2500 μm x 2500 μm and there are 44 pads.
8. The designed LVDS transmitter and receiver fully comply with TIA/EIA-644.

Table 6-1 shows the LVDS high speed I/O ports performance table.

Table 6-1: LVDS high speed I/O ports performance table

LVDS TRANSMITTER		**LVDS RECEIVER**	
Max. Data Rate	1.5 Gb/s	Max Data Rate	2 Gb/s
Reference Voltage	1.2 V	Min Common Mode Voltage	0 V
Termination Resistance	100Ω	Max Common Mode Voltage	2.4 V
Power @ 1.5 Gb/s	45 mW	Power @ 2 Gb/s	6 mW
Output Voltage Swing (100Ω Termination)	350 mV Peak-to-Peak	Input Hysteresis	50 mV Peak-to-Peak

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