THE EFFECT OF DC LINK FILTER DESIGN AND COMPENSATION ON DYNAMIC PERFORMANCE OF VECTOR CONTROLLED DRIVE

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2015

Approval of the thesis:

THE EFFECT OF DC LINK FILTER DESIGN AND COMPENSATION ON DYNAMIC PERFORMANCE OF VECTOR CONTROLLED DRIVE

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ABSTRACT

THE EFFECT OF DC LINK FILTER DESIGN AND COMPENSATION ON DYNAMIC PERFORMANCE OF VECTOR CONTROLLED DRIVE

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February 2015, 147 pages

This study has three objectives. The first is to identify parameters that affect the dynamic performance of a vector controlled motor drive. The second is to investigate compensation methods to eliminate effect of DC link voltage variation on drive performance. The last is to identify a DC link design method so that dynamic performance of vector controlled drive can be improved.

Keywords: Dynamic Performance of Motor Driver, DC Link Compensation, DC Link Design for Dynamic Conditions

ÖZ

DC BARA FİLTRE TASARIMI VE KOMPANZASYONUNUN VEKTÖR KONTROLLÜ SÜRÜCÜNÜN DİNAMİK PERFORMANSI ÜZERİNDEKİ ETKİLERİ

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Şubat 2015, 147 sayfa

Tez kapsamında yapılan çalışmanın üç temel amacı bulunmaktadır. İlk amaç, vektör kontrollü sürücünün dinamik performansını etkileyen değişkenlerin tespit edilmesidir. İkinci amaç, DC bara gerilim dalgalanmalarının sürücü performansı üzerindeki etkisini gidermek amacıyla kompanzasyon metotlarının incelenmesidir. Son amaç, vektör kontrollü sürücünün dinamik performansını artırmaya yönelik DC bara filtre tasarım metodununun belirlenmesidir.

Anahtar Kelimeler: Motor Sürücülerin Dinamik Performansı, DC Bara Kompanzasyonu, Dinamik Koşullara göre DC Bara Filtre Tasarımı

To My Family

ACKNOWLEDGEMENTS

I would like to enounce my deep gratitude to my supervisor Prof. Dr. H. Bülent Ertan for her valuable supervision, advice, useful critics and discussions throughout this study.

I am also grateful to my thesis committee members Prof. Dr. Muammer Ermiş, Prof. Dr. Kemal Leblebicioğlu, Assoc. Prof. Dr. M. Timur Aydemir and M. Can Altungüneş for their criticism and advices.

Special thanks should be given to Halil Kavak, Gökmen Cengiz, İbrahim Erseçgin, Doğan Yıldırım, and Kenan Ahıska for their involvements in this study. Their support during this study helped me complete it in an easy way.

I wish to express my endless thanks to every member of my family, my mother Zeynep Kayhan, my father Yusuf Kayhan, my brother Yasin Kayhan and to my sisters Hilal Kılıç and Özden Balta for their unconditional love. Without their encouragements and advices, that journey would be endless for me.

I am deeply grateful to Ümit Büyükkeleş, Hüseyin Meşe, Barış Çiftçi, Nadir Usluer, Tugay Güzel, Bünyamin Bostan, and Kemal Öncü for their friendships, encouragement and support.

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ESR	(Equivalent Series Resistance)
IGBT	(Insulated Gate Bipolar Transistor)
IPM	(Intelligent Power Module)
PI	(Proportional-Integral)
PWM	(Pulse-width Modulation)
RMS	(Root Mean Square)
SPWM	(Sinusoidal Pulse-width Modulation)
SVPWM	(Space Vector Pulse-width Modulation**)**
THD	(Total Harmonic Distortion)

CHAPTER 1

INTRODUCTION

1.1. AC Motor Drives

"Electric motors are employed in many applications such as pumps, compressors, elevators, cranes, white goods, electric vehicles, electric tractions etc. Traditionally, electric motors were operated without speed control. However, with further studies it is proven that, with an adjustable speed, motor drive systems offer higher efficiency and lower maintenance. Prior to the 1950s all such applications required the use of a dc motor drive since ac motors were not capable of true adjustable or smoothly varying speed since, they inherently operated synchronously or nearly synchronously with the frequency of electrical input [8]".

Induction motors can be directly fed from the utility source. However, in order to obtain variable voltage and frequency at motor terminals, motor drivers are used. A block diagram for a drive is given in Figure 1-1.

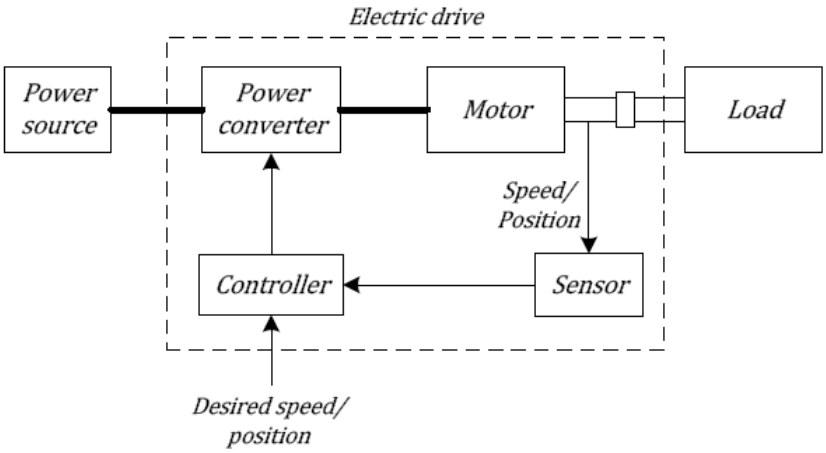


Figure 1-1 Block diagram of drive system [8]

There are mainly two types of controls; scalar or vector control. In scalar control, magnitude and frequency of the voltages are controlled. Scalar control is used in applications where dynamic performance is not important. In vector control, magnetic flux and torque of motor are controlled and this method is used when high performance is desired.

Field-oriented control which is the type of vector control used in our driver. By using this method, three phase motor quantities are identified as two orthogonal components (d-q axes); rotor flux (d-axes component) and electromagnetic torque (q-axes component). By implementing control in d-q frame, the control of flux and torque becomes independent from each other. With this configuration, the control of AC motor becomes similar to DC machine control where flux and torque are separately controlled [9].

Field oriented control is well established now. However, what is important is to implement this control method so that the torque bandwidth is as wide as possible. This issue is the subject of this investigation. For this purpose, it is essential to identify the issues which affect the drive performance.

1.2. Effective Parameters for High Dynamic Performance

In order to increase dynamic performance, first the parameters that affect the driver performance should be identified. After literature research, following subjects are found as most effective parameters on dynamic performance of motor driver.

- DC Link Ripple
- Dead Time Insertion
- PI Controller Constants
- Switching Frequency (Sampling Period)
- Parameter Sensitivity
- Integral Windup
- Decoupling Control of d and q Axes Components

In order to understand how they affect the motor driver performance, brief explanations about these parameters are given.

DC Link Ripple

In order to create adjustable voltage and frequency at output of motor driver, DC voltage is needed at input side of the motor driver. Since the power supply at high voltage ratings are expensive and need large spaces, in most of the applications, three phase or single phase grid voltage is rectified to obtain DC link voltage. Mainly, two methods are used for rectification; namely, active rectification and passive rectification. In active rectification, controllable switches are used to obtain DC link voltage whereas in passive rectification, diode rectifier is used without any control. After rectification stage, DC link capacitor is used to decrease ripple voltage on the rectifying stage and to filter high frequency currents. In our driver, passive rectification (three phase diode rectifier) is used to obtain DC link voltage. Since there is no control in passive rectification, DC link has ripple on it at 6 times grid frequency and magnitude of ripple voltage changes with respect to the power drawn by inverter. If the output stage controller bandwidth is not high enough to eliminate the effect of the ripple voltage, the output voltage, current and torque waveforms will have harmonics near the ripple frequency. For this reason, for high ripple voltages, electromagnetic torque cannot reach to its reference value and the dynamic response of the motor driver will decrease. In order to increase the drive performance and decrease harmonic contents in current and torque waveforms, DC link ripple should be compensated in each switching period with feed forward control instead of feedback control. The detailed analysis about DC link compensation is given in Chapter-4.

Dead Time Compensation

In order to eliminate short circuit between switching elements in the same leg, dead time is inserted to PWM signals in the same leg while changing states of switches. This time insertion is necessary because switching elements cannot turn on and turn

off immediately and if two switches in the same leg were ON at the same time, then the short circuit current would pass through switches and through DC link side. This is an unwanted for safety of switching elements and DC link components.

Dead time insertion is different for different kind and different rating of switches. In our hardware environment, IPM (Intelligent Power Module) from Mitsubishi Company is used and the recommended minimum dead time is 2.5 μs. This value can be thought as same for all switches in this range. For safety, the inserted dead time can be higher than minimum dead time and in our driver 5 μs dead time is inserted. If the switching frequency of IGBTs is considered, 2.5 μs (or 5μs) time becomes important with respect to switching period of driver (150 μs in our case). Because of voltage loss in dead time, the output voltage and currents will not reach to desired level and therefore, desired torque would not be obtained instantly and the change in torque levels will be obtained with some delay because of dead time insertion. In order to obtain desired torque and increase dynamic response of driver, dead time should be compensated in each sampling period by using feed forward control. The detailed analysis about dead time compensation is given in Chapter-3.

Anti Windup (Integral Windup) Mechanism

PI controller is used in the most of the modern drivers. When the actual current deviates from the reference value, the integral becomes very large and causes integral windup. In order to eliminate integral windup, several methods are proposed in the literature [5].

- Incremental Algorithm: In this method, integration is stopped if the output of PI controller reaches to saturation level. With this method, integration is stopped directly and there is no delay to decrease the output level below the saturation level. The block diagram of the incremental algorithm method is shown in Figure 1-2.

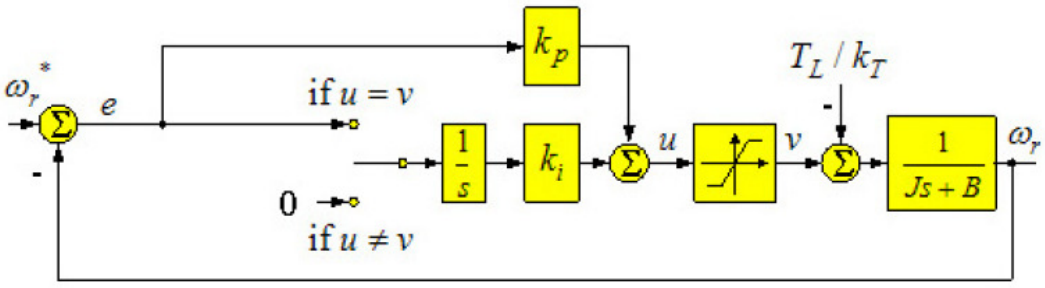


Figure 1-2 the incremental algorithm [6]

- Back Calculation: In this method, output of PI controller is fed back to integration if it is above the saturation level. By this way, the output of PI controller will decrease below the saturation level after few sample periods. The block diagram of the back calculation method is shown in Figure 1-3.

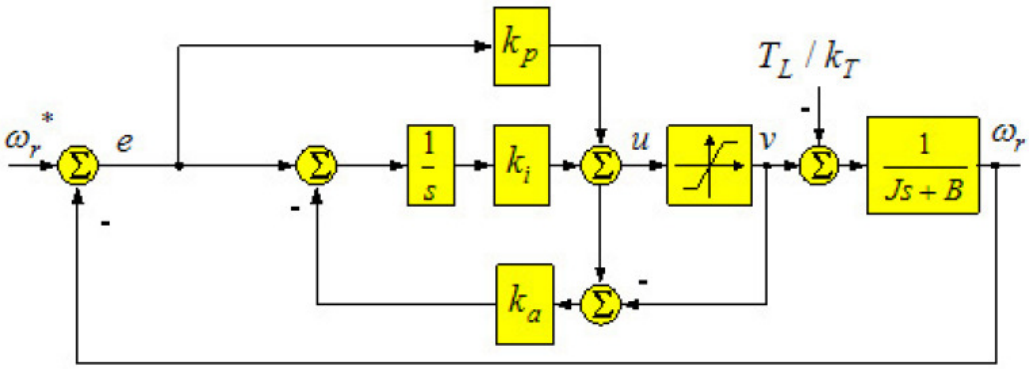


Figure 1-3 Back calculation [6]

- Conditional Integration

- Observer Approach

Integral windup is necessary in motor control applications. The reason is that when torque reference is given to motor in no-load condition or load torque is lower than reference torque, there will be error and it will increase until the load value reaches the reference torque value. If driver operates in this condition, the integration will store this error and increase the output of PI controller up to very large values. When the load torque of motor is increased, because of the stored error, the desired torque will not be obtained until the stored error finishes. In order to eliminate this phenomenon, the windup error should be eliminated. The methods to eliminate this condition are given above. In the designed driver, incremental algorithm is used for windup cancellation. The comparison between methods is not considered in this work.

Current (q and d axes) Loop PI Controller

PI controller eliminates oscillations and steady state error during operation of motor driver. Derivative controller is not used for our case because during step changes and oscillation in reference signal, derivative controller output can increase up to infinity and controller will generate undesired outputs.

In Figure 1-4 and Figure 1-5, the effects of proportional and integral constants on controller response can be seen. As seen from the figures, gain values for P and I change the settling time and oscillations of the controller output.

As seen from the figures, the effects of proportional and integral controller are dependent. Therefore, their values should be chosen carefully. There are some methods for the tuning of PI controller.

One of them is manual tuning method. In this method, initially only K_P constant is given until steady state oscillations are obtained. After the oscillations are obtained, K_P is set to half of this value. After K_P choice, K_I is increased until offsets are corrected in sufficient time for the design. Another method is Ziegler-Nichols method. Initially, K_P is increased until sustained oscillations are obtained at the

output. After obtaining this condition, K_P is set to 0.45 of this value and K_I is set to $1.2*K_P/T_U$; where T_U is the period of oscillation [3].

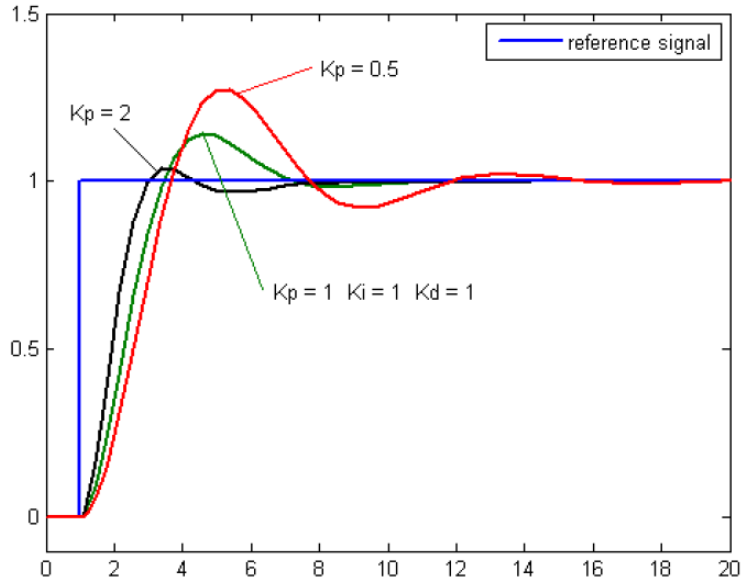


Figure 1-4 Effect of proportional controller [3]

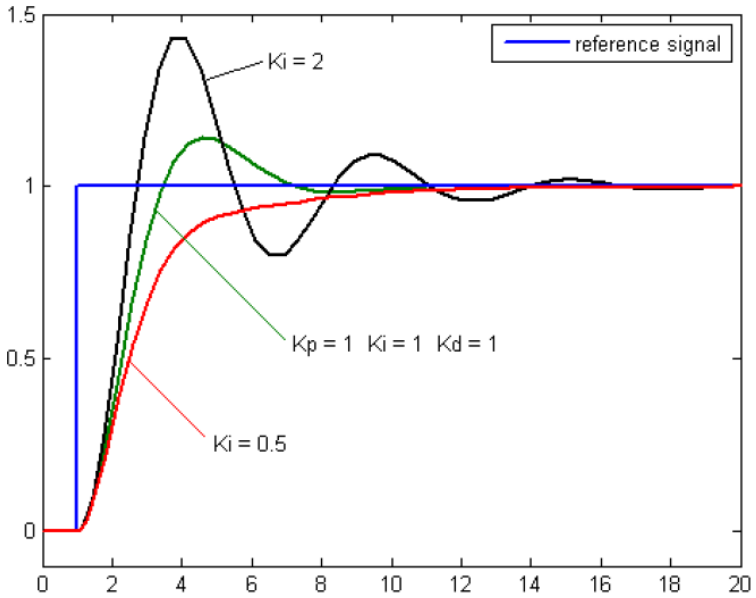


Figure 1-5 Effect of integral controller [3]

In this thesis work, values for K_P and K_I constants are taken from [1] and they are used in simulation and software environment.

Switching Frequency

There are mainly two criteria for the choice of switching frequency (for simplicity, the power loss on switching element is not considered). One of them is the limit of switching element and the other is the sampling time of controller. Based on the lower one, the switching frequency should be determined. In our design, the switching frequency is determined with respect to sampling time of DSP controller.

The sampling period of driver (or in general means controller) should be low in order to respond system dynamics. As the sampling period decreases, the sampled data from the system converges to continuous data and the controller calculates the output signals correctly and in shorter time. Therefore, the dynamic response of driver will increase as the sampling period decreases.

Parameter Sensitivity

In induction motor, vector control can be implemented as in synchronous machine if the angle of the rotor flux is exactly known. In synchronous machine, position angle is directly measured mechanically whereas in induction machine position angle cannot be directly measured. In order to obtain position angle, slip frequency component should be added to measured value from rotor [2]. The slip frequency is calculated as;

$$s * w_s = \frac{r_r}{L_r} * \frac{I_{qs}}{I_{ds}} \tag{1.1}$$

$s * w_s = slip\ frequency$

$r_r = rotor\ resistance$

$L_r = magnetizing\ inductance + rotor\ leakage\ inductance$

$I_{qs} = stator\ q - axis\ current$

$I_{ds} = stator\ d - axis\ current$

$\theta = Motor\ position$

$w_r = rotor\ speed$

$$\theta = \int (w_r + s * w_s) dt \tag{1.2}$$

As seen from the equation 1.2, the slip frequency is included in the position angle equation. Slip frequency depends on rotor resistance and rotor inductance as given in equation 1.1. In [2], it is stated that, if the rotor time constant (L_r/r_r) is not correctly known or it changes because of heating or some other reasons, the position angle will be calculated incorrectly and its effects are;

- Rotor flux will deviate from desired level
- Output torque will differ from desired torque
- Torque response will decrease
- Power loss will increase and efficiency will decrease

In order to eliminate these problems, rotor time constant should be exactly known at initial stage and their values should be updated continuously based on motor temperature. In this thesis work, the stator resistance is used in the motor position estimation equations. Its value is measured for the used motor in the experimental setup and this value is used in the drive software.

Decoupling Control of d and q Axes Components

The equivalent circuits d and q axes for induction motor are given in Figure 1-6. As seen from this figure, there is an independent voltage sources for each equivalent circuit.

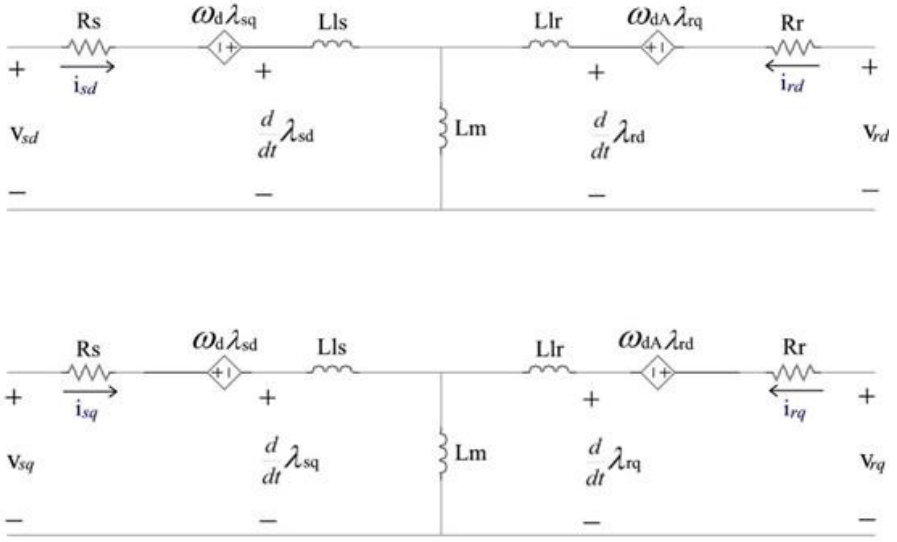


Figure 1-6 Equivalent d and q axes circuit of induction motor [10]

In induction motor control, d and q axes reference voltages are obtained at the output of PI controller. Based on equivalent circuit, it can be understood that during step changes of q axes current, d axes current will change because the d axes voltage is constant whereas the dependent voltage source value changes during step changes. After step changes, PI controller compensates error caused by decoupling; however, the delay caused by PI controller decreases the dynamic performance of motor driver. In order to increase dynamic performance, the decoupling (or cross coupling) control should be included in PI controller output. The implementation of decoupling control is given in Figure 1-7 and Figure 1-8.

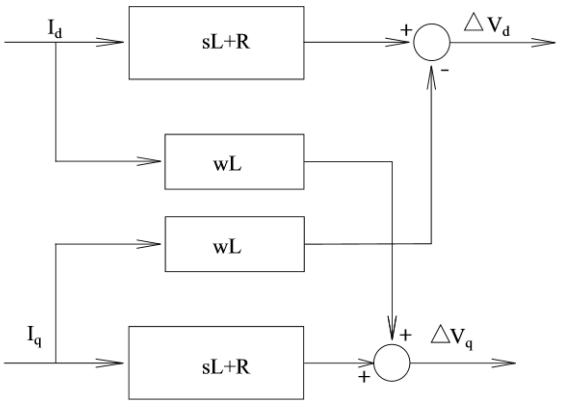


Figure 1-7 Decoupling control of d and q axes voltages [7]

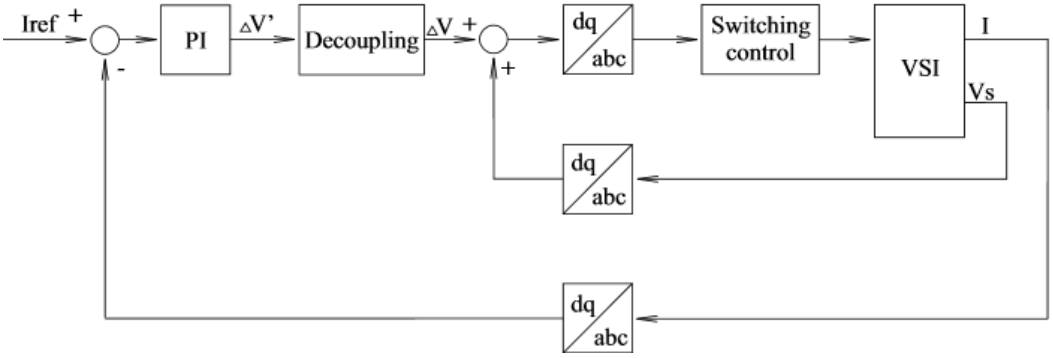


Figure 1-8 Decoupling control in control algorithm [7]

1.3. Objective of Thesis

In this thesis, firstly a motor driver is designed based on software and hardware in [1]. For the design, new DSP controller is used and hardware part is improved based on new controller. After hardware and software environment, a simulation environment for motor driver is developed to see the effects of the new algorithms before experimental tests.

In this thesis, our aim is to increase dynamic performance of motor driver by implementing hardware and software solutions. For this reason, firstly DC link compensation methods in literature are reviewed and two methods are implemented

in simulation environment. After simulation results, the method which gives better results in simulation is implemented in the experimental setup. The steady state and dynamic performance results in the simulation and experimental setup are obtained to see the effect of DC link compensation.

After DC link compensation, DC link design is implemented for steady state condition as in literature. After that, DC link design is analyzed considering dynamic conditions. By improving DC link design considering dynamic conditions, DC link voltage is maintained at certain levels where DC link is fully compensated so that desired flux level can be maintained in a wider frequency range. In addition, by decreasing power loss and peak current of DC link capacitor, lifetime of capacitor and therefore, the lifetime of driver are expected to increase.

1.4. Scope of Thesis

The thesis consists of five chapters.

This chapter gives brief explanations about parameters that affect the dynamic performance of motor driver and it explains the objective of thesis.

Chapter 2 explains hardware environment of motor driver. The circuit diagrams for each part of driver are explained.

Chapter 3 provides explanations for software environment and block diagram for algorithm.

Chapter 4 gives literature survey and explanations about DC link compensation. In addition, simulation and experimental results are obtained and analyzed. After that, DC link design is explained and it is analyzed for dynamic conditions.

Finally, in Chapter 5, the thesis is concluded with a summary of the work done. Then, future work that should be done about this subject is explained.

CHAPTER 2

HARDWARE ENVIRONMENT

In this thesis work, motor driver hardware in [1] is improved and redesigned with respect to new DSP controller. The new hardware with new DSP board is used to drive induction motor in vector control mode and scalar control mode.

2.1. Block Diagram

This section describes the hardware in detail. The block diagram of hardware is given in Figure 2-1. The processes in hardware environment are briefly explained as;

- DSP controller calculates initial values of duty cycles for three phases (software)
- 3-phase PWM block inside software environment generates PWM signals according to calculated duty cycles and adjusted frequency and dead time (software)
- DSP controller sends generated ON/OFF (PWM) signals to main board
- PWM signals are fed to transceiver block in main board and these signals are fed to isolation stage after transceiver
- Isolated and inverted PWM signals are given to IPM gate driver terminals (IPM operates opposite to input signals. When control input is high, corresponding IGBT turns off; when control input is low, corresponding IGBT turns on. Therefore, control signals are inverted in isolation stage)
- Phase currents and line-to-line voltages are measured with current and voltage transducers

- Measured voltages and currents are filtered with Sallenkey filter (low pass filter)
- Filtered voltage and current measurements are fed to ADC channels of DSP controller
- DSP controller calculates the motor position according to measured values and updates PWM signals with respect to measured and reference values

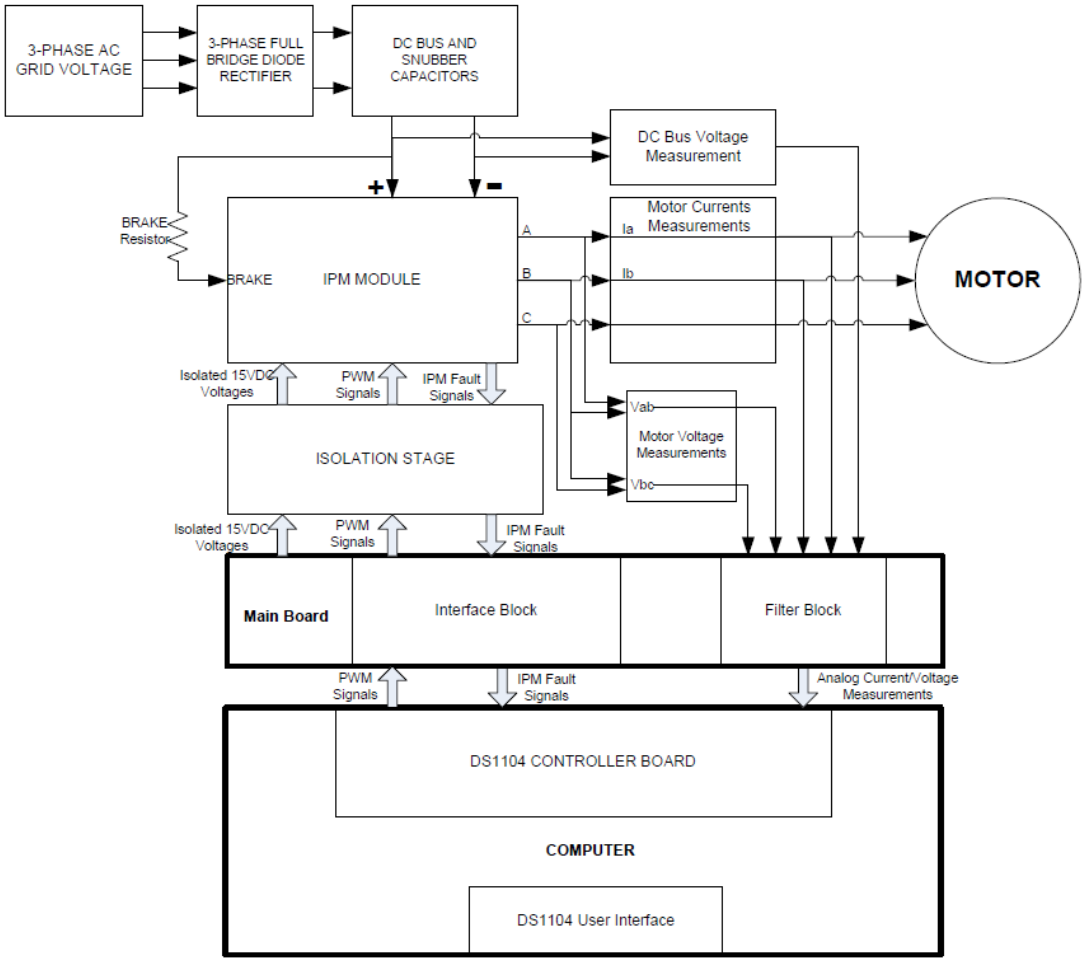


Figure 2-1 Block diagram of motor driver system

In the new hardware, some improvements are done to hardware environment given in [1]. Eight analog inputs can be measured simultaneously. Therefore, there is no need to use multiplexer to measure DC link voltage. Moreover, it is known that IPM needs

symmetrical PWM pulses and in old hardware [1], hardware solutions are implemented to obtain symmetrical pulses. However, new DSP controller generates symmetrical PWM signals and it eliminates the use of such hardware stages. In addition, with the new DSP controller, dead time can be adjusted using software. Thus, there is no need to use dead time generator and XOR gates to obtain dead time as in [1]. By adjusting dead time in software, different kinds of switching elements can be used without changing hardware environment.

2.2. DS1104 Controller Board

In the motor driver system, DS1104 board is used as a DSP controller. General properties of the controller board are listed as followed;

- 8 ADC channels
- 8 DAC channels
- 34 I/O interface
- 2 incremental encoder interface
- 3-phase PWM interface (symmetrical and adjustable dead time PWM pulses)
- 2 serial communication interface

DS1104 controller board measures the line-line voltages, DC link voltage and line currents. According to these values, motor position and duty cycles for each phase are calculated. After obtaining duty cycles, these values are sent to 3-phase PWM block and ON/OFF signals for IGBTs are generated. In 3-phase PWM block, the frequency and dead-time of the PWM signals can be adjusted. PWM signals are symmetrical and there is no need to use XOR gates in the hardware. Since dead time can be adjusted in software, there is no need to use dead time generator in hardware. In addition, it has introduced flexibility so that dead time can be adjusted any value for different IPMs or for test purposes. By eliminating some hardware component, the reliability of the hardware environment is increased.

DS1104 User Interface

DS1104 allows monitoring all of the signals inside the software environment. In addition, it allows changing parameters during operation. By this way, some gain/offset parameters and speed/torque references can be set during operation. In addition, PWM signals can be turned on and off using this interface.

2.3. Interface and Filtering Stage (Main Board)

In the driver system, there is a main board in which all connections from system parts such as current and voltage measurement boards and isolation board to DS1104 controller board are done. The circuit blocks in the main board are explained in the following parts.

2.3.1. Main Board Power Input

There are two voltage inputs in the motor driver system. One is the 3-phase AC voltage which is converted to DC link voltage (537 VDC when 380 VAC rectified) and it is used to drive induction motor. The other is 24VDC input and it is used for control parts of driver system. 24VDC input is located in main board. All of the voltages for measurement stage, isolation stage and filtering stage are produced in main board using filtered 24VDC input. In order to protect the board (control parts) in case of short circuit, 24VDC voltage input is protected with fuse. After the fuse, a common mode filter is placed in order to clear high frequency noise in the control part power input. After that, filtered voltage is fed to DC/DC converters' inputs.

2.3.2. Gate Driver Isolated 15VDC Voltages

In this part, 7 isolated 15VDC voltages are generated for the IPM (Intelligent Power Module). The IPM (PM50RL1A120) used in experimental setup needs 4 isolated power supplies; 3 for upper IGBTs and 1 for lower IGBTs and brake IGBT. However, to meet the power supply requirement for higher current ratings IPMs, 7 isolated 15VDC supplies are placed on the main board. The circuit schematic of 15VDC supplies are given in Figure 2-2.

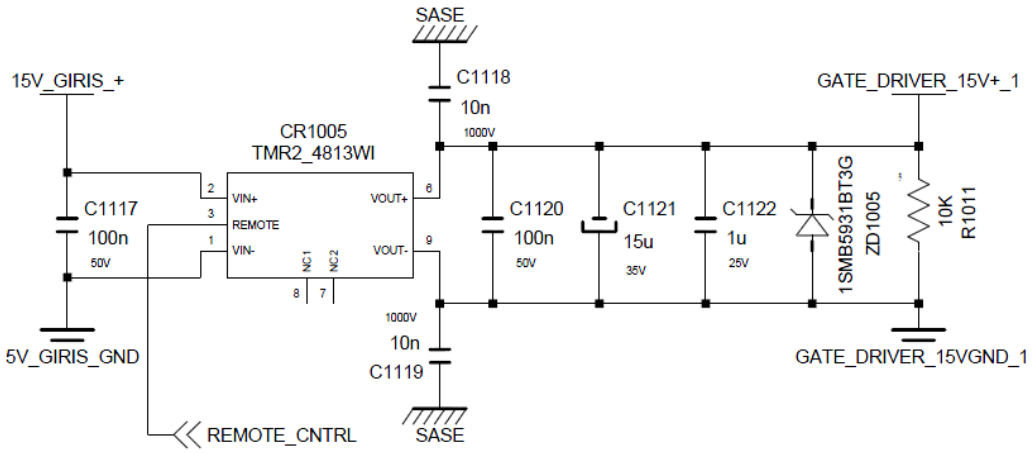


Figure 2-2 Circuit diagram of gate driver 15VDC voltages

The recommended value for control voltage of IPM is 15±1.5VDC. Therefore, converters with 15VDC outputs are placed on main board. Their outputs have maximum ±%5 error and this keeps the output voltage within the limits of IPM. IPM control part needs 55mA current from 15VDC supplies at maximum frequency and maximum current switching condition. Converter's continuous current rating is 130mA and this value satisfies IPM current need in all switching frequency range.

Converters' outputs have its own protection, however, in order to have further protection for IPM driver part; an 18V zener diode is placed parallel to 15VDC outputs. By this way, the output cannot exceed 18V. Since absolute maximum rating of IPM control part voltage is 20V, 18V zener diode provides protection driver part

of IPM. Finally, a dummy resistor placed to converter's output in order to load converter for all conditions and stabilize the output.

2.3.3. 5V and 3.3V Isolated Voltages

In this part, 5VDC voltage is produced from filtered 24VDC voltage. After that, 3.3VDC is produced from 5VDC using linear regulator. The related circuit diagrams are given in Figure 2-3 and Figure 2-4.

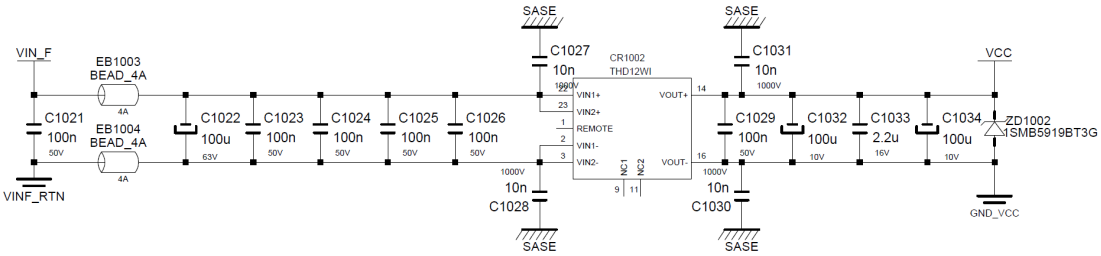


Figure 2-3 Circuit diagram of 5VDC voltage

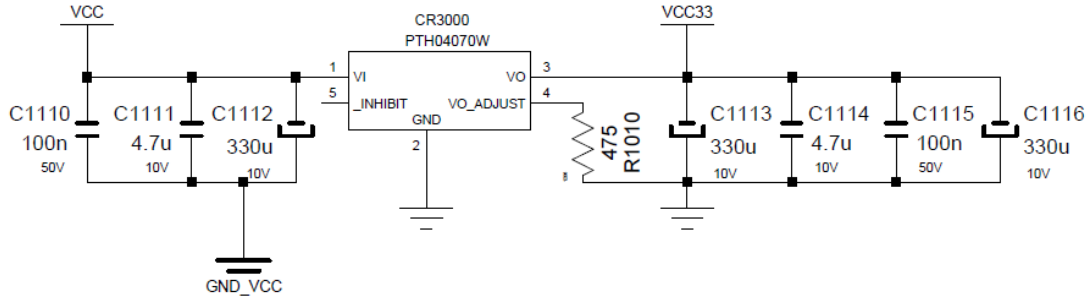


Figure 2-4 Circuit diagram of 3.3VDC voltage

5VDC and 3.3VDC is used in the digital parts of the main board. These are buffer stage, reference voltage generation stage and serial communication stage. The integrated circuits used in these parts are operated at 3.3VDC or 5VDC. Therefore, it is necessary to produce these voltages. In addition, 5VDC and 3.3VDC is produced

to be able to supply DSP controller from main board which is not valid for DS1104 controller because it is connected to computer and it takes its power from computer.

2.3.4. ±15VDC Isolated Voltages

In this part, ±15VDC voltage is produced from filtered 24VDC input voltage. The related circuit diagram is given in Figure 2-5.

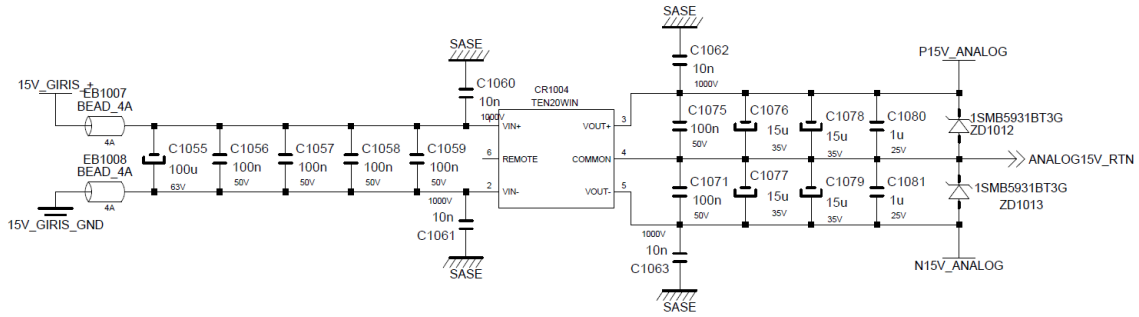


Figure 2-5 Circuit diagram of ±15VDC voltage

In the converter's outputs bulky capacitors are placed to be able to supply inrush current. In addition, 18V zener diodes are placed both sides as a further protection for components using this supply.

The ±15VDC voltages are used for current and voltage measurements and their filtering stages. Since these stages are very crucial, the supply voltages for these parts should be very clear to obtain better measurement results. Therefore, these voltages are filtered with capacitors and high frequency inductors. By this way, voltage supplies given to measurement part and filtering part are cleared from noisy environment to obtain better measurement results. The related circuit diagram is given in Figure 2-6.

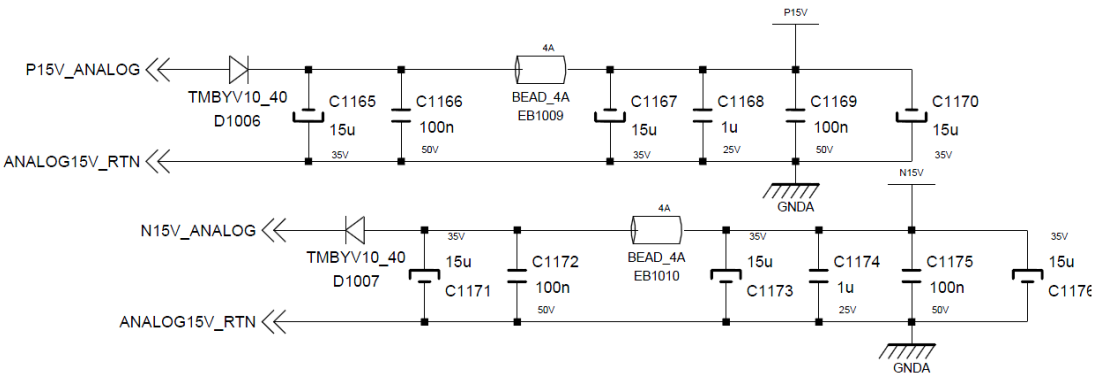


Figure 2-6 Circuit diagram of ±15VDC voltage filters

2.3.5. Filtering of Analog Measurement Signals

In the driver system for control purposes, DC link voltage, two line-to-line voltages and two phase currents are measured. For current measurements, current transducers from LEM Company are used. Their current ratings are 100A and this value is sufficient for driver current rating of 22A (peak value for inverter phase current). For voltage measurements, voltage transducers from LEM Company are used. Voltage transducers are capable of measuring AC and DC voltages and its voltage rating is 1500V. Since the drive system operates at 537VDC, voltage transducers ratings are enough to measure both line-line and DC link voltages. The related circuit diagrams are shown in Figure 2-7, Figure 2-8 and Figure 2-9.

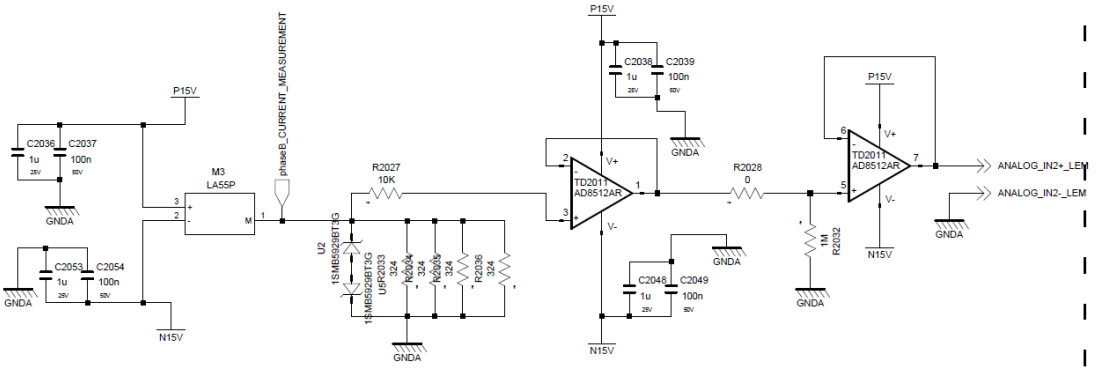


Figure 2-7 Circuit diagram of current measurement

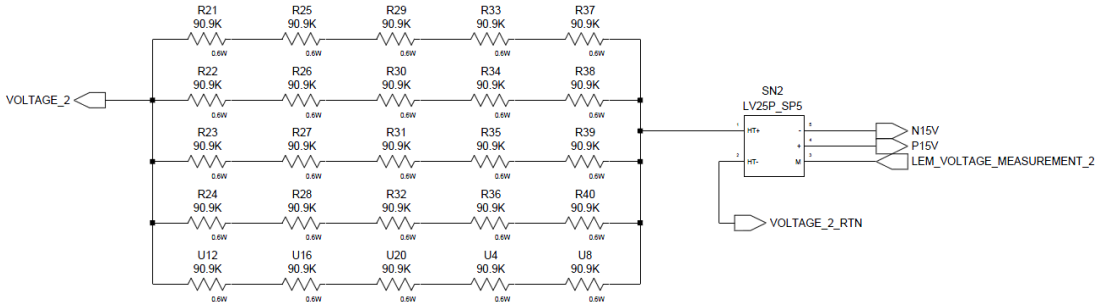


Figure 2-8 Circuit diagram of voltage measurement-1

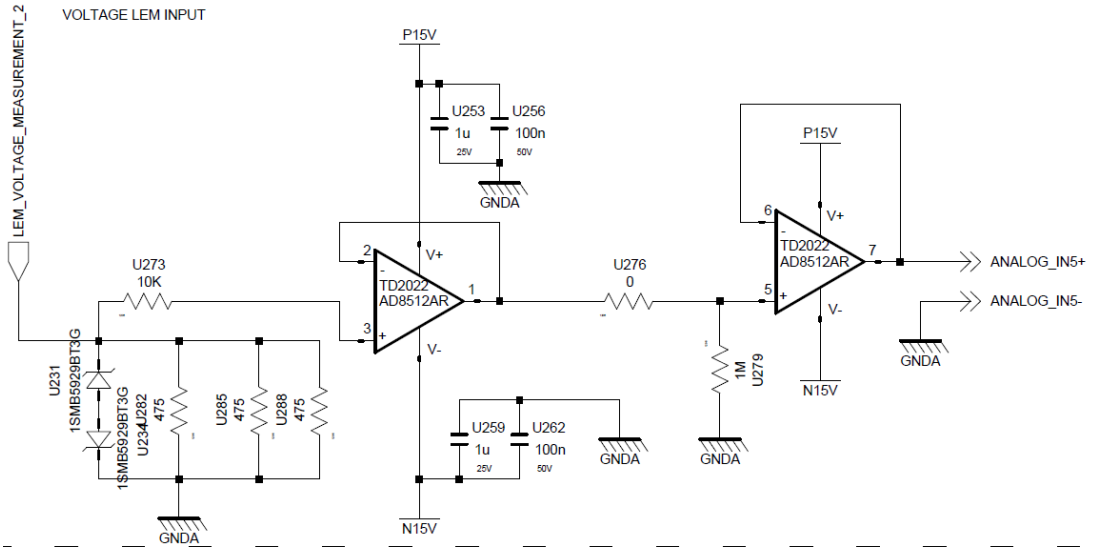


Figure 2-9 Circuit diagram of voltage measurement-2

The current transducer has a turn ratio of 1:2000. Its output is current and its value is input current / 2000. Since the output is current, in order to be able to measure, it should be converted to voltage. Thus, output of current transducer is dropped on a resistor and converted to voltage. For the resistor, recommended value for current transducer is used. In the main board, surface mount resistors are used and their power ratings are small. Considering maximum current rating of current transducer, resistors are paralleled to have safe operation in whole current range.

The voltage transducer has a turn ratio of 2.5/1. Voltage transducer operates like current transducer and its output is also current. Voltage transducer output is input current x 2.5. To measure voltage, a known resistor block is placed at the input terminal of voltage transducer and input voltage passing through this resistor block create current in the primary side. At the output, input current x 2.5 is created. Same in current transducer, this current is dropped on resistor and converted to voltage. For the resistor, recommended value for voltage transducer is used.

After obtaining analog signals for currents and voltages, these signals are filtered with low-pass filter. For the filter, Sallenkey topology is used. This is a filter composed of an op-amp, 2 resistors and 2 capacitors. By changing values of the capacitors and resistors, the gain and cut-off frequency of the filter is determined. The related circuit diagram is shown in Figure 2-10.

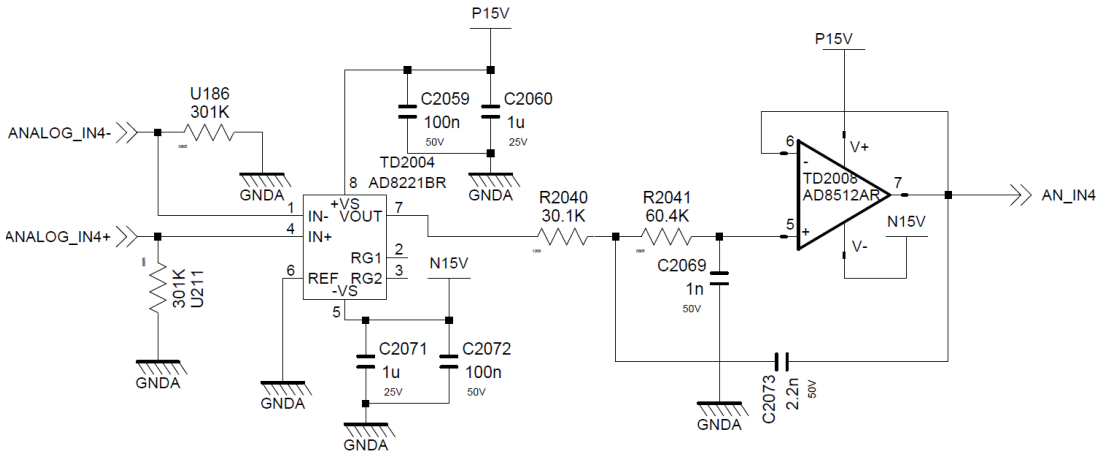


Figure 2-10 Circuit diagram of Sallenkey Filter

Before filtering stage, an instrumentation amplifier is used to be able to measure differential voltage. After that, Sallenkey filter is placed. The resistor and capacitor values are set to have cut-off frequency of 2.5 kHz, 1 gain at pass-band, and $1/\sqrt{2}$ gain at cut-off frequency. The calculations of filter parameters are given below.

From an application note [11]:

R2040 = mR, R2041 = R,

C2069 = C, C2073 = nC

For these values f_c (cut-off frequency) and Q (gain at cut-off frequency) can be calculated as followed;

$$f_c = \frac{1}{2\pi RC\sqrt{mn}} \tag{2.1}$$

$$Q = \frac{\sqrt{mn}}{m+1} \tag{2.2}$$

For the filter design,

R=60.4K

C=1nF

m=30.1/60.4 ~=0.5

n=2.2

For these values, following results are obtained for the filter.

$$f_c = \frac{1}{2\pi \times 60.4 \times 10^3 \times 1 \times 10^{-9}\sqrt{0.5 \times 2.2}} = 2516\ Hz \tag{2.3}$$

$$Q = \frac{\sqrt{0.5 \times 2.2}}{0.5+1} = 0.7 \tag{2.4}$$

The frequency response of the filter is obtained in LTspice program. The schematic and frequency response of the filter are shown in Figure 2-11 and Figure 2-12.

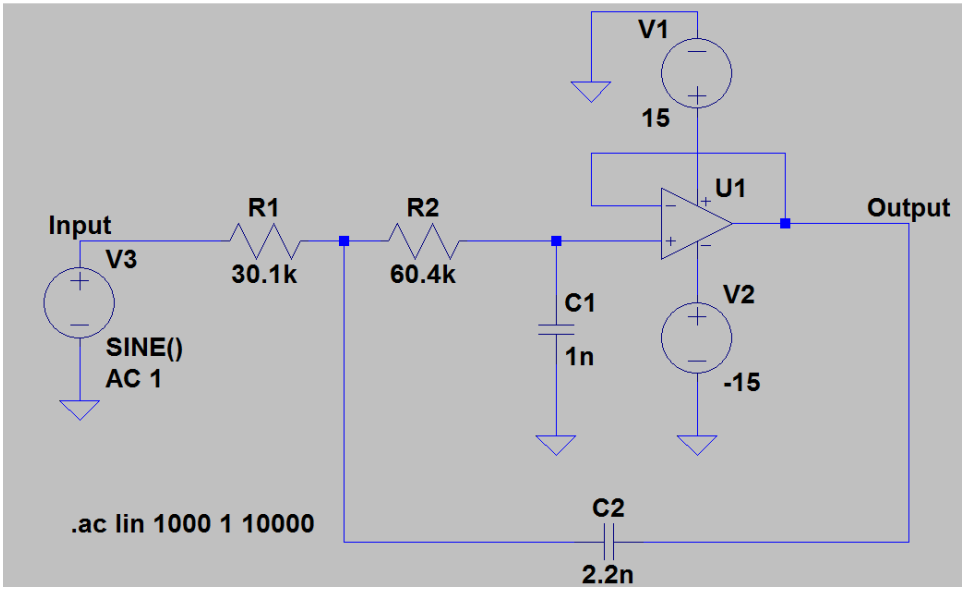


Figure 2-11 Simulation schematic for Sallenkey filter

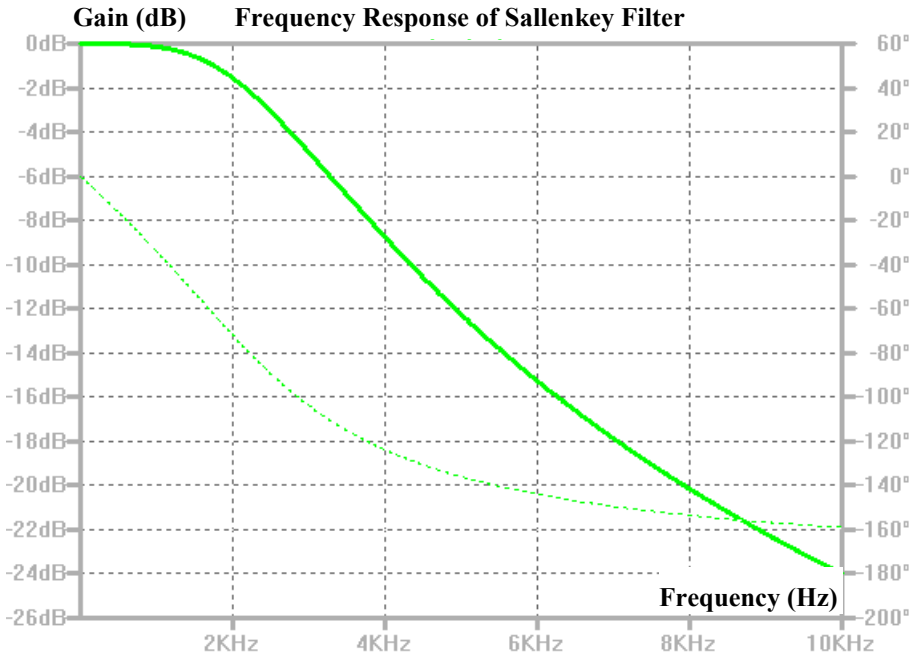


Figure 2-12 Frequency response of Sallenkey filter

As seen from Figure 2-12, the cut-off frequency of Sallenkey filter is 2.5 kHz which is the point where gain is -3dB. In addition, gain of the filter is 1 up to 0.75 kHz. Since the measured signals are 50Hz signals at most (or can be increased up to 300 Hz for DC link ripple voltage measurements), the measurements will not be affected from the gain decrease after 0.75 kHz.

2.3.6. Buffering of PWM Signals

In this part, a transceiver is used for PWM signals. Since it is not safe to draw current from DSP controller, a transceiver is used. By this way, only small amount of current is drawn from DSP to transceiver inputs and isolation part is driven by transceiver outputs. The related circuit diagram is given in Figure 2-13.

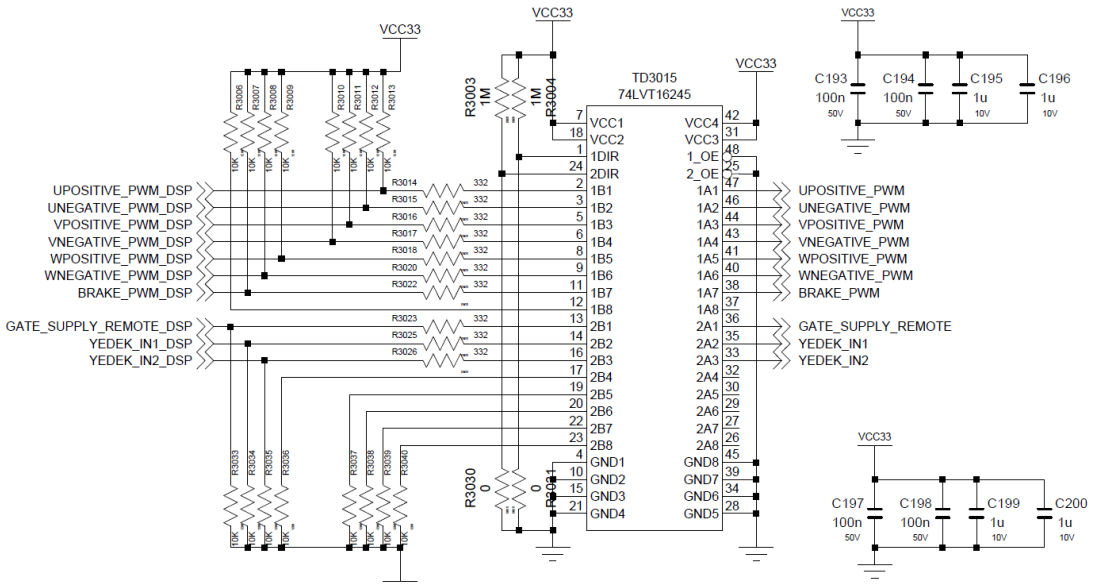


Figure 2-13 Circuit diagram of transceiver stage

2.4. Isolation Stage

In this part, PWM signals are transferred to IPM gate driver inputs using optocouplers. By this way, isolation is provided between IPM gate drivers and DS1104 controller PWM signals. This stage is placed on a new board and board

placed on input terminals of IPM. By this way, distortion of PWM signals is minimized by minimizing the connection between optocoupler outputs and IPM gate driver inputs. The related circuit diagram is given in Figure 2-14.

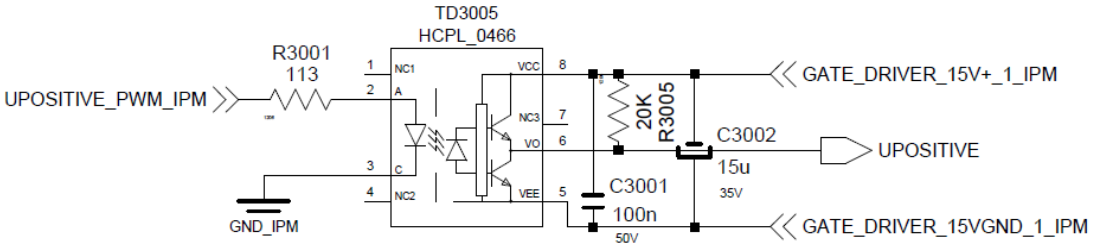


Figure 2-14 Circuit diagram of isolation stage

The output side voltages of optocouplers are isolated from each other. For the upper side IGBTs, 3 isolated 15VDC voltages are used. For the lower side and brake IGBTs, one isolated 15VDC voltage is used as recommended in IPM reference document. Moreover, the voltages are supplied with two capacitors. Smaller one (100nF) is for filtering purposes, bigger one (15µF) is for inrush currents for IPM gate driver part.

The left side signals in Figure 2-14 are coming from main board and they are PWM signals of DS1104 controller. On the right side, the output signals are generated and they are fed to IPM gate drivers. There are three signals on the right side, two of them are power supply of the gate driver and one of them is control signal of corresponding IGBT driver. There are also fault signals for IGBTs. They are read by optocouplers. The related circuit diagram is given in Figure 2-15.

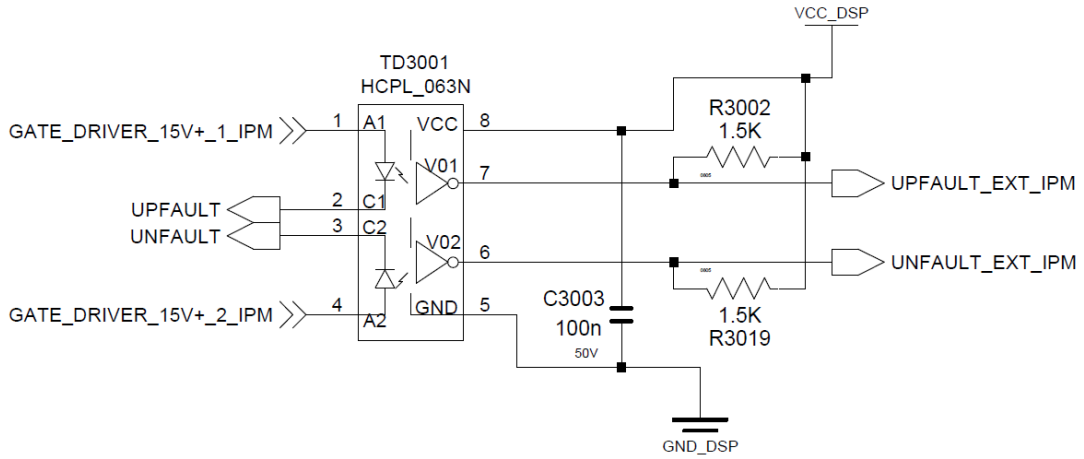


Figure 2-15 Circuit diagram of fault signals

The fault signal of IPM is an open-collector signal. When there is no fault, optocouplers cannot turn on and output becomes high. However, when there is fault, the fault transistor inside IPM conducts and optocouplers turns on over the 1.5kΩ fault resistor inside IPM. By this way, output becomes low and DS1104 controller reads this fault signals and turns off the PWM signals and stops motor.

The Choice of Optocoupler for PWM signals;

The properties of optocoupler given in IPM datasheet are;

- The propagation delay must be less than 0.8µs,
- The current transfer ratio must be high,
- The optocoupler must switch only low side

By considering these properties, optocoupler from AVAGO Company with HCPL-0466 type number is used. It satisfies all of the properties given above. Its current transfer ratio is 90% and propagation delay is about 0.5µs.

Considering current transfer ratio of optocoupler and the maximum current needed of IPM, the left side resistor is determined as 113Ω. With this resistor value, input

current of optocoupler becomes 18mA and its output can supply up to 16.3 mA and this value satisfies the maximum current need of the used IPM at maximum frequency.

2.5. Intelligent Power Module (IPM) Stage

The type number of IPM is PM50RL1A120 from MITSUBISHI Company. IPM has its own gate driver inside the module and it needs only control signals to turn and turn off IGBTs. The current requirement of IPM for control part is below 50mA for each gate. The other properties of PM50RL1A120 are given below;

- Continuous current rating: 50A
- Maximum Voltage rating: 1200V
- 7 IGBT in a pack (3Phase + Brake)

Internal block diagram of PM50RL1A120 is shown in Figure 2-16.

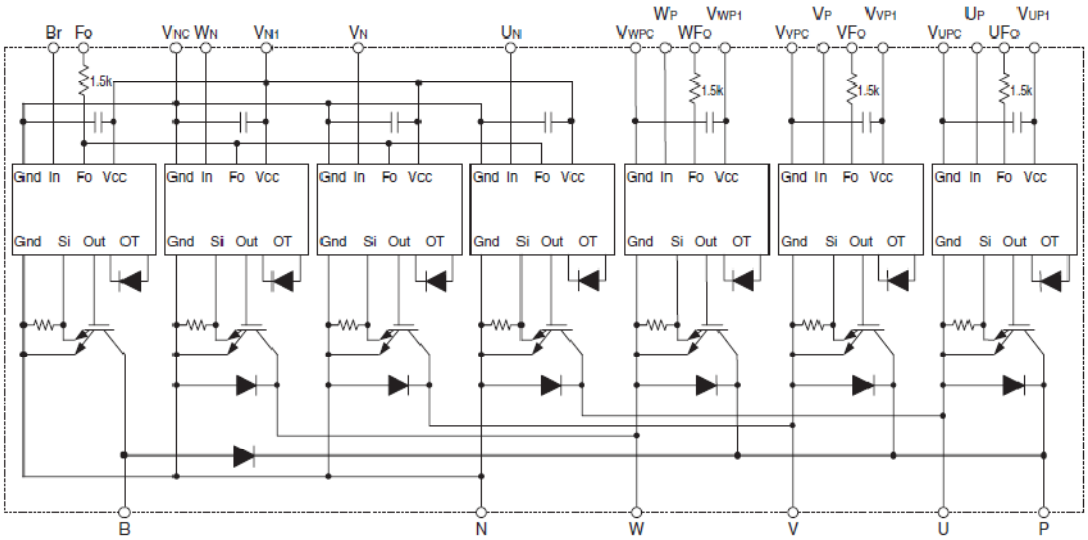


Figure 2-16 Block diagram of PM50RL1A120 [12]

As seen from Figure 2-16, there are 7 IGBTs inside the module. The gate driver voltages of upper side IGBTs are different; however, voltages for lower side IGBTs

and brake IGBT are same. Therefore, there is no need to use 7 isolated voltages for this IPM. Moreover, the fault signals of lower IGBTs and brake IGBT are same and there is only one fault signal for 4 IGBT. Thus, in the isolation stage, circuit diagram is produced only 4 fault signals. Besides from gate driver part, IGBTs has parallel diodes and the current conduction during dead time periods are provided over these diodes.

2.6. Power Stage

In order to obtain DC link voltage, 380V AC grid voltage is fed to 3 phase full bridge diode rectifier in driver system. After full bridge rectifier, charging resistor is used in order to prevent inrush currents drawn by capacitors. A disable switch is placed parallel to charging resistor to disable resistor after capacitors are fully charged. Two capacitors are used in DC Bus because the voltage rating of one capacitor is 450V and by connecting two of them series, the voltage rating of the capacitor bank becomes 900VDC. Their values are 2.4mF and with series connection total capacitance value becomes 1.2mF in the initial design of driver. However, their values are changed in DC link design part. After DC link capacitors, a snubber capacitor is used to decrease surge voltages at DC link. The related block diagram is shown in Figure 2-17.

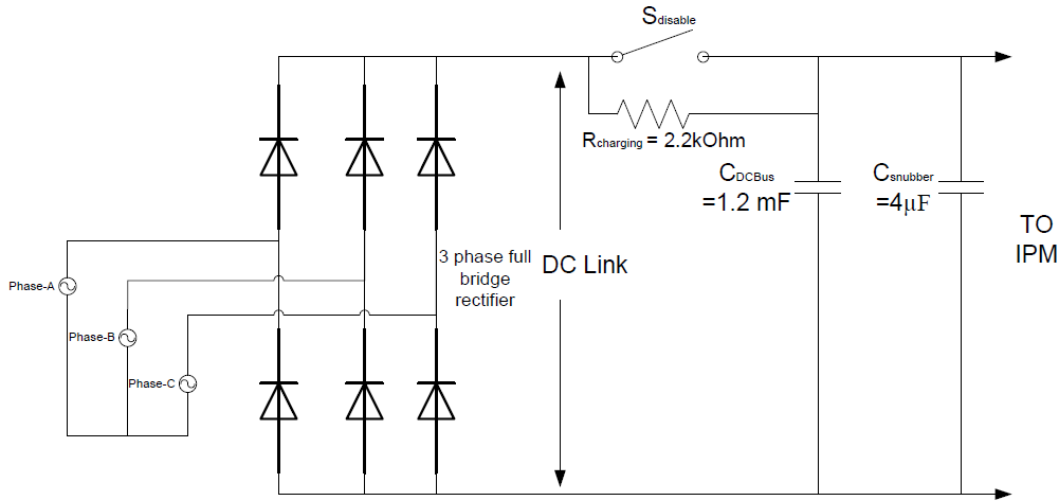


Figure 2-17 Block diagram of the power stage

The experimental setup of the motor driver is shown in Figure 2-18.

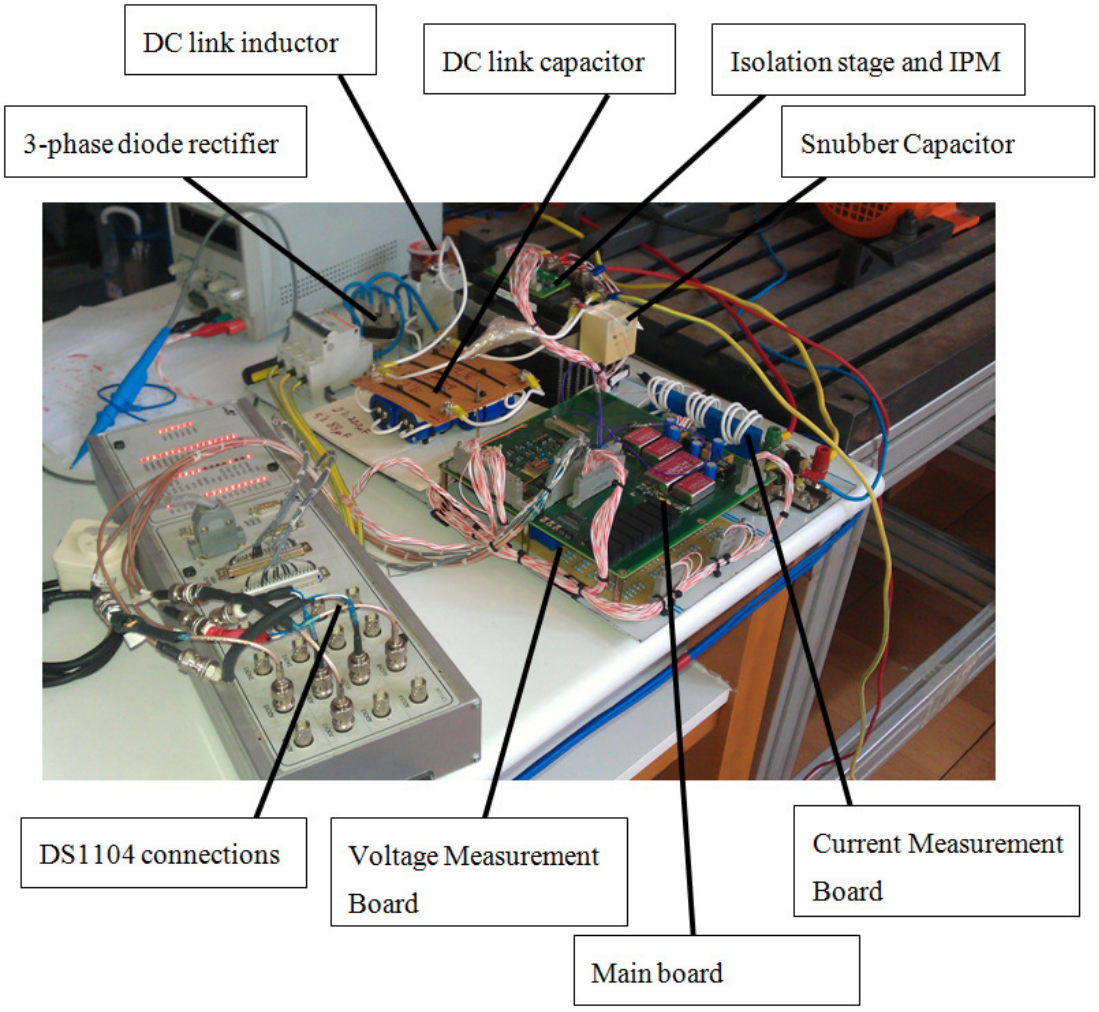


Figure 2-18 Hardware of the motor driver

CHAPTER 3

DRIVE SOFTWARE AND SOFTWARE SIMULATION ENVIRONMENT

In this part, the drive software and software simulation modules are explained. The aim of the software is to drive the motor with vector control at desired torque or speed.

For the software, generally modules in [1] are used and modified with respect to new hardware environment. After obtaining fully working software and hardware as in [1], some modules are added to software to improve motor driver performance.

Since detailed explanations about software environment are given in [1], in this part some basic explanations about previous software and detailed explanations about modifications and improvements will be given.

In [1], DS1102 controller board is used as DSP controller. For new design, DS1104 controller board is used. The new controller has MATLAB/Simulink interface, i.e., controller code can be written in MATLAB and loaded to DSP controller. In order to increase user interface, new software is written in MATLAB/Simulink environment. The new software is composed of simulink block and c-codes. After software is completed, it is loaded to DS1104 using “Incremental Build” option of MATLAB. After code is running on DSP controller, signals can be viewed online through the CONTROL DESK program. By this way, debugging and fault detection can be done very easily.

3.1. Flowchart of Drive Software

The software is written in modules. The flowchart of software is given in Figure 3-1. The processes in the drive software environment are briefly explained as:

- DSP controller set the d axes current to reference value and q axes current to zero to obtain rated flux

- After the necessary time is waited based on rotor time constant, the q axes current is set to desired level so that desired torque will be obtained

- Voltages and currents are measured and they are transformed to d and q coordinates

- Based on reference and actual current values, d and q axes voltages are generated with PI controller

- PI controller outputs are limited to avoid excessive reference voltages

- Reference d and q axes voltages are transformed to α and β axes voltages using motor position

- α and β voltages are used to calculate reference duty cycles for three phases in SVPWM module

- Reference duty cycles are updated in dead time and DC link compensation modules

- Updated duty cycles are sent to PWM module of DS1104

- DS1104 PWM module adds the adjusted dead time to gate signals and turn on/off the switches with respect to switching frequency

- Motor position is estimated and it is used in the calculations

- Dynamic braking module is activated when DC link voltage exceeds 600V

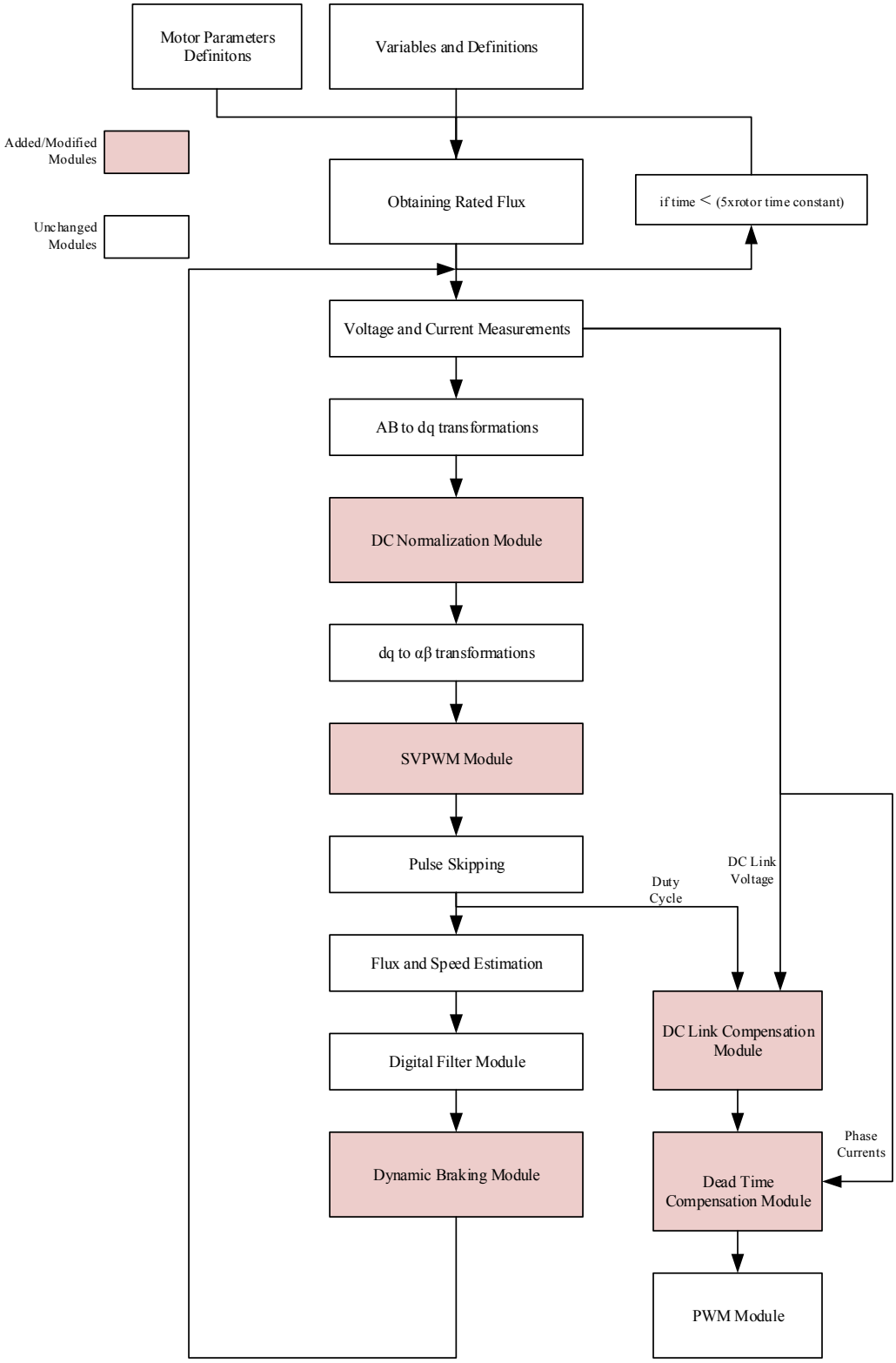


Figure 3-1 Flowchart of software

3.2. Variable Definitions and Initialization Module

In this module, all variables used in the software are defined and initialized. According to new hardware, some new variables are added to the module. Sample code for module is given below.

```
double isc=0,isd=0,isq=0,isalfa=0,isbeta=0;
double isalfaref=0,isbetaref=0,isaref=0,isbref=0;
double vsa=0,vsb=0,vsc=0;
double vsalfa=0,vsbeta=0;
double vsaref=0,vsbref=0;
```

3.3. Motor Parameters Module

In this module, motor parameters are defined. In order not to change DSP code for different motors, this module is not used in new software. Instead of this, motor parameters are written in a MATLAB file and uploaded before loading the code to DS1104. For a new motor, new MATLAB file will be created and uploaded to MATLAB environment before loading the code to DS1104.

3.4. Obtaining Rated Flux Module

The aim of the module is to obtain rated flux before vector control starts. For this purpose, motor is aligned to d-axis and DC current (rated I_d current) is flowed into motor terminals. The duration of DC current flowing is 6 times motor time constant in order to settle flux level. For the tested motor, the time constant L_r/R_r is about 64msec. Therefore, duration for rated flux module is set to 400msec. For different motors, this value should be updated in the software. Instead of this, time constant value is read from a file as in motor parameters module. Thus, motor time constant value is written in MATLAB file and it is read from the file while loading code to DSP.

3.5. Voltage and Current Measurements Module

This module is used to measure phase voltages and currents. In the new software, MATLAB/simulink block specific for DS1104 is used. In order to obtain the exact value for voltages and currents, the gain blocks are used. The gain values are determined by calculating transducer output with respect to measured values. After that, signals are measured with oscilloscope and harmonic tester and the gain values are adjusted comparing measured signals with DS1104 and harmonic tester/oscilloscope.

3.6. ABC to dq Axes Transformation Module

The aim of the module is to obtain d-q and alpha-beta axes values from 3-phase values using motor position. The related code is given below.

```
//ABC to DQ transformation module//////////
vsa=(2*(*vsab)+(*vsbc))/3;
vsb=(*vsbc-*vsab)/3;
isalfa = *isa;                  // (a,b) to () axis conversion
isbeta =  0.5773502692*(*isa+2*(*isb));
vsalfa = vsa;
vsbeta =  0.5773502692*(vsa+2*vsb);
//ABC to DQ transformation module//////////
```

3.7. PI Controller Module

PI controller module is used to obtain d and q axes reference voltages from measured and reference d and q axes currents. The related figure about module is given in Figure 3-2.

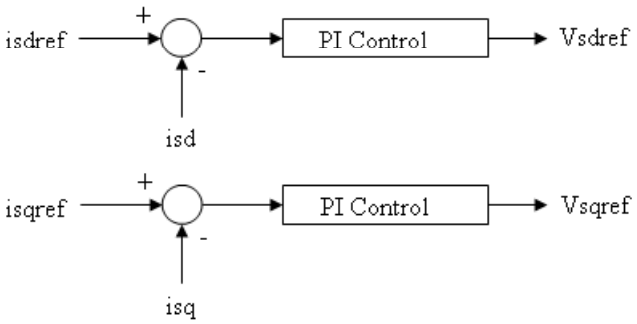


Figure 3-2 PI Controller Module [1]

Integral Windup Mechanism

As stated in introduction chapter, the integral windup mechanism is necessary for integral output to avoid cumulating errors to very large values. Therefore, an incremental windup mechanism is used in software. The related code for this block is given below. The constants for windup mechanism are determined in DC normalization stage.

```
errorisqrefint = errorisqrefint + (errorisqref*iq_antiwindup) * TS;     // taking straight forward integral
errorisdrefint = errorisdrefint +(errorisdref *id_antiwindup)* TS;
```

The integral is stopped when saturation limits are reached at d and q axes voltages. Therefore, the windup constants for d and q axes become zero when saturation is reached; otherwise, they are 1 and PI works in normal operation.

3.8. dq to αβ Axes Transformation Module

In this module, reference alpha and beta axes voltages are obtained from reference d and q axes voltages and motor position. The obtained values in this module are used in the space vector pulse width modulation module. The related code is given below.

```
//DQ to ALFA BETA ABC transformation module//////
vsrefalfa = vsdref * costeta - vsqref * sinteta;      // Obtaining alfa beta reference
voltage values/
vsrefbeta = vsdref * sinteta + vsqref * costeta;
vsaref = vsrefalfa;                 //obtaining real voltage references
vsbref =  - 0.5 * vsrefalfa + 0.866 * vsrefbeta;
//DQ to ALFA BETA ABC transformation module//////
```

3.9. Space Vector Pulse Width Modulation (SVPWM) Module

The aim of module is to generate duty cycles of the phases with respect to reference alpha-beta axes voltages and related sector.

In [1], DS1102 DSP is used as a controller and it cannot generate symmetrical PWM signals; therefore, symmetrical PWM signals are generated using some hardware components. PWM signals generated from DSP controller passed through XOR gates and dead time generator. By this way symmetrical PWM signals were obtained with necessary dead time addition. Since XOR gates generates same pulse width for %X and %(100-X), software in [1] generates pulse width up to %50. After this point, pulse width repeats itself and this cause wrong PWM signals. In order to limit pulse width to %50, the timing calculations were divided by 2 in [1]. Since the new DSP controller DS1104 can generate symmetrical PWM pulses, there is no need to use XOR gates and there is no need to divide timing calculations by 2. In addition, the new DSP controller can add dead time inside the software; therefore, there is no need to use dead time generator in the hardware.

In order for better understanding of SVPWM module, timing calculations are given briefly.

Timing Calculations

In SVPWM, there are 6 sectors each corresponds to 60^o electrical angle. For each sector, there are two equations to calculate ON times of the corresponding vector. In Figure 3-3, the sectors and corresponding vectors are shown.

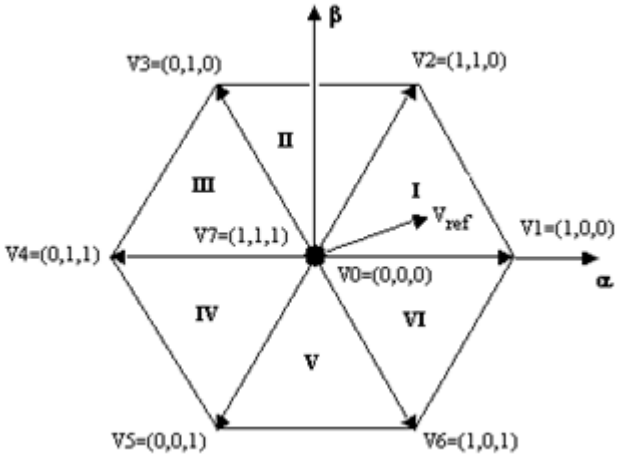


Figure 3-3 SVPWM vector diagram

In the calculations, only ON times for upper IGBTs are calculated. The lower sides IGBTs are complementary of the upper side and therefore, they are calculated simply by subtracting ON time of upper IGBT from 1. In the timing calculations, K is used which represents modulation constant. It depends on DC link voltage and period of control cycle as seen in following equation. In this equation, K is modulation constant, T_S is the sampling period and V_{DC} is DC link voltage.

$$K = \frac{\sqrt{3}}{2} * \frac{T_S}{V_{DC}} \tag{3.1}$$

The timings for sector 1 are calculated as:

$$T_k = \frac{K}{2} * \left(\sqrt{3} * V_{sref\alpha} - V_{sref\beta}\right) \tag{3.2}$$

$$T_{k+1} = K * V_{sref\beta} \tag{3.3}$$

$$T_Z = T_S - (T_k + T_{k+1}) \tag{3.4}$$

Where k corresponds to related vector and it is 1 for sector 1, 2 for sector 2 etc. T_z is the zero vector time. The reference voltage with respect to timing is as given in the following equation.

$$V_{sref} * T_S = V_0 * \frac{T_0}{2} + V_k * T_k + V_{k+1} * T_{k+1} + V_7 * \frac{T_0}{2} \tag{3.5}$$

V0 (0,0,0) and V7 (1,1,1) are both zero vectors.

The ON times of the phases with respect to above calculations are given in the following equations.

$$t_{Aon} = \frac{T_0}{2} + T_k + T_{k+1} \tag{3.6}$$

$$t_{Bon} = \frac{T_0}{2} + T_k \tag{3.7}$$

$$t_{Con} = \frac{T_0}{2} \tag{3.8}$$

The details of duty cycle calculations in SVPWM module are given in [1].

3.10. Pulse Skipping Module

In order to prevent short-circuit of IGBTs in the same leg, dead time is introduced in the software. In this application, dead time is set to 5µs. This means that duty cycles lower than 5µs will be lost in the PWM module. Therefore, duty cycles lower than 5µs are sent as 5µs to PWM module.

3.11. Flux and Speed Estimation Module

In this module, position of rotor flux is estimated using alpha-beta voltages and currents. The estimated position is used for vector control.

In the new software, this module is used as in [1]. Detailed explanations about module are given in [1].

3.12. DC Normalization Module

DC normalization module is used to limit the reference voltages given to SVPWM module. By limiting the reference values, generated duty cycles are limited. Since maximum value for duty cycle is 1, a value higher than 1 for duty cycle will distort the output waveform. Therefore, before duty cycle limitation in pulse skipping module, DC normalization module is used to limit duty cycle. The related code is given below.

```
//DC Normalization Module/////////////
limit_ref=sqrt(vsdref*vsdref+vsqref*vsqref);

if(limit_ref>UD_NORM)
{
   vsdref=vsdref*(UD_NORM/limit_ref);
   vsqref=vsqref*(UD_NORM/limit_ref);
   id_antiwindup=0;
   iq_antiwindup=0;
}
else
{
   id_antiwindup=1;
   iq_antiwindup=1;
}
//DC Normalization Module/////////////
```

In the new software, limiting is done with q and d axes voltages whereas in old software limiting is done with alpha and beta axes voltages. By this way, alpha and beta axes sinusoidal waveforms are not distorted, only their magnitudes are limited.

In addition, anti-windup gains for integral is set in this module. When reference d and q axes voltages exceed the limits, integration gain becomes 0; otherwise, it becomes 1.

3.13. Digital Filter Module

In this module, a constant for Flux-Speed Estimation module is generated. The related code is given below.

```
// Digital Filter Module/////////////////
 if (*t<0.6)              //Time is less than 0.5 sec
 {
 kd=80;              //Digital filter time constant
 }
 if (*t>0.6 && ws>80)
 {
  if (ws<0)
     {
     kd=-ws;             // rotor rotates in opposite direction
     }
  else
  kd=ws;             //Time constant of digital filter is equal to stator speed.
 }
```

3.14. Dynamic Braking Module

The aim of the module is to prevent excessive DC link voltage. When motor decelerates, DC link voltage increases because of regenerative energy coming from motor side. As the deceleration increases, more excess voltage is created on DC link. In order to get rid of this voltage, when DC link voltage reaches 600V brake IGBT is turned on and excess charge coming from motor side is dissipated on braking resistor. When voltage drops to 580V, braking IGBT is turned off for normal operation. By this way, excess DC link voltage is eliminated for IGBTs and DC link capacitors. In addition, in order to limit excessive energy on braking resistor, the brake operation lasts at most 1 second and it will not operate until 1second passes. If the voltage on DC link continues to increase up to 750V, then operation is stopped.

By this way, braking resistor energy dissipation will be lower and its size will be lower. Since the voltage rating of IPM and DC link capacitors are higher than 750V, this voltage will not harm motor driver and does not affect operation because DC link compensation is implemented and it will adjust the output voltages for changing DC link voltage. The related diagram for dynamic braking module is given in Figure 3-4.

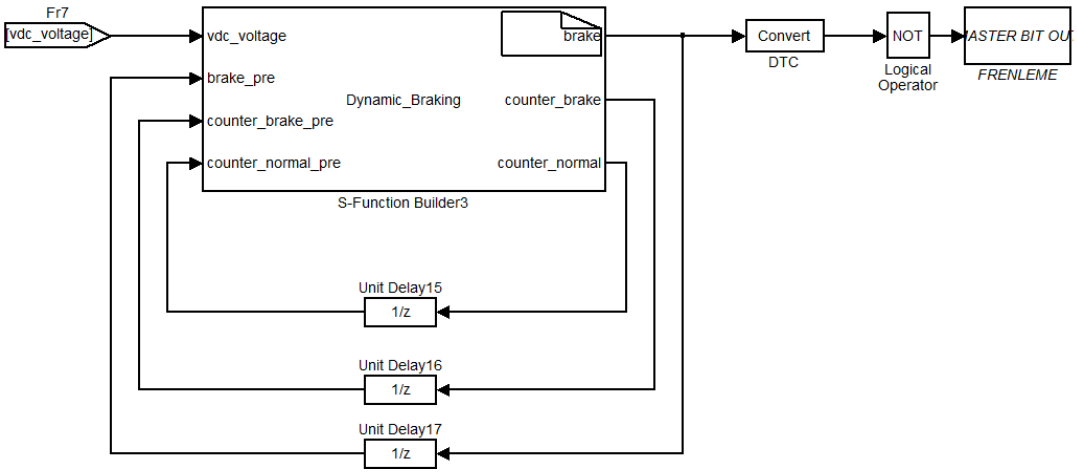


Figure 3-4 Dynamic Braking Module

The related code for dynamic braking is given below.

```
*brake=*brake_pre;
*counter_brake=*counter_brake_pre;
*counter_normal=*counter_normal_pre;

if (*vdc_voltage>600 && *counter_brake<13300) //13300 corresponds 1
second
{
   *brake=1;
   *counter_brake=*counter_brake+1;
   *counter_normal=0;
   if (*counter_brake >= 13300)  //13300 corresponds 1 second
   {
     *brake=0;
   }
}
else if (*vdc_voltage>580 && *vdc_voltage<600 && *brake==1 &&
*counter_brake<13300) //13300 corresponds 1 second
{
```

```
    *brake=1;
    *counter_brake++;
    *counter_normal=0;
    if (*counter_brake >= 13300) //13300 corresponds 1 second
    {
      *brake=0;
    }
}
else
{
    *brake=0;
    *counter_normal=*counter_normal+1;
    if(*counter_normal==*counter_brake)
    {
       *counter_brake=0;
    }
}
```

3.15. DC Link Compensation Module

Since DC link voltage is not constant during operation of driver because of diode rectification, it is convenient to compensate DC link ripple to obtain more accurate duty cycles.

In this module, the generated duty cycles in SVPWM module is updated with respect to measured DC link voltage. 537V which is the maximum value of rectified 380VAC signal is chosen for reference value of DC link.

The related diagram for the software is given in Figure 3-5. As seen from the figure, duty cycles are divided to normalized DC link voltage. By this way, when DC link voltage increases, duty cycle decreases or vice versa.

There are two regions in SVPWM method; linear region and over modulation region. In linear region, output voltages follow the reference signal whereas in over modulation region output voltages lose its linearity with respect to reference voltage and saturates at some point. In addition to that, in over modulation region the harmonic content in torque and current waveforms increases. In order to limit harmonic distortion, over modulation is not implemented up to six-step mode and it is implemented until modulation index becomes 0.952. After this point, DC link

compensation is implemented by maintaining modulation index at this level and desired output voltage could not be obtained for these cases.

Based on above explanations, DC link compensation is applied until modulation index is equal to 0.952 and when lower DC link voltages are measured, the modulation index is set to 0.952 and output voltage is obtained for this modulation index value. Therefore, d and q axes currents decrease and their ripple values increase for lower DC link voltages.

By implementing DC link compensation, output voltages set to desired level and harmonic content in current and torque waveforms caused by ripple voltage on DC link is minimized.

The detailed explanations about DC link compensation are given in Chapter-4. The block diagram of DC link compensation module is given in Figure 3-5.

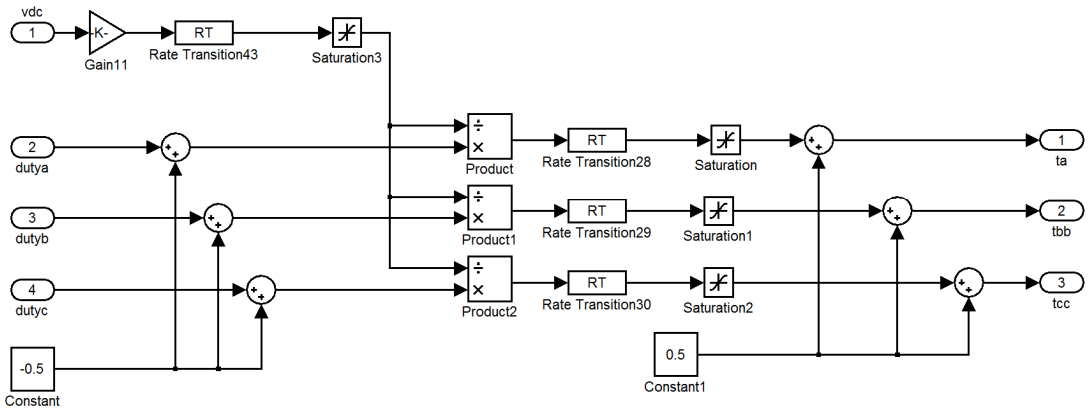


Figure 3-5 DC link compensation module

3.16. Dead Time Compensation Module

Dead time is the time delay insertion between same leg switches while switches are changing states (from turn off to turn on). This time delay is necessary to avoid short circuit between switches and to protect them. However, this time delay causes non-linearity in voltage and current waveforms. Another nonlinear effect is turn-on and

turn-off time of the switches and they can be included in dead time. Other nonlinear effects are the voltage drops on freewheeling diodes and switches. Voltage loss caused by these voltage drops can be calculated in a period and the time corresponding to these voltage drops can be calculated. Calculated time can be treated as part of dead time and they can be compensated with dead time compensation method.

3.16.1. Literature Review for Dead Time Compensation

[13] - [19] are reviewed for dead time compensation and following results are obtained.

For dead time compensation, there are three main concepts should be determined.

- Calculation of compensation time
- Determination of current direction
- Addition/Subtraction of dead time

The used methods for designed driver are given below.

3.16.1.1. Calculation of Compensation Time

Since the saturation and ON voltages of IGBT and its diode are very small compared to DC link voltage, error caused by these voltages will be very small and it can be ignored in the calculations. The compensation time equation becomes simply:

$$T_{comp} = T_{dead} + T_{on} - T_{off} \tag{3.9}$$

3.16.1.2. Determination of Current Direction

In order to compensate dead time, current direction is needed because compensation time is added when current is positive and compensation time is subtracted when current is positive. Therefore, it is very important to determine current direction.

In simulation and experimental setup, phase currents are measured with current sensor and compensation time is added/subtracted with respect to current sensor output. This method has problems around zero crossing points because near zero crossing due to DC offsets of sensor and ripples on motor current several zero crossing points occur and cause incorrect compensation and distortion of output voltages. Moreover, since current with dead time inserted case has flat region near zero crossing and this also causes problems for current direction determination because compensation starts at incorrect position and dead time compensation is not effectively implemented. However, in our driver position is estimated and implementing dead time compensation with respect to estimated position will result in incorrect compensation and output waveforms will be distorted. Therefore, current direction is determined with current sensor.

3.16.1.3. Addition/Subtraction of Compensation Time

The calculated compensation time caused by all non-linear effects are added to reference duty cycle when current is positive, the calculated time is subtracted from reference duty cycle when current is negative.

3.16.2. Software Module

In this module, the nonlinear effects caused by dead time, on-off time of IGBTs and voltage drops on IGBT and their diodes are compensated. The related calculations for compensation time are given in previous part.

By implementing, harmonic content of current waveforms are decreased. The related diagram for dead time compensation is given in Figure 3-6.

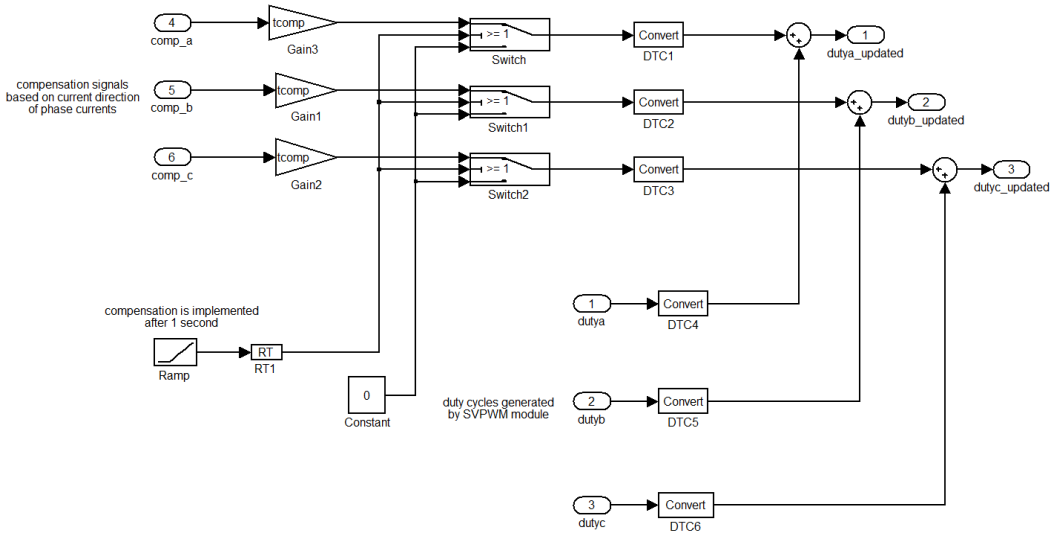


Figure 3-6 Dead time compensation module

In block diagram given in Figure 3-6, the compensated time is added or subtracted from the duty cycles with respect to current direction of phase currents. In the initial state, the compensation is not implemented during starting of the motor. After 1 second, compensation is implemented. The block diagram for compensation signal calculation is given in Figure 3-7.

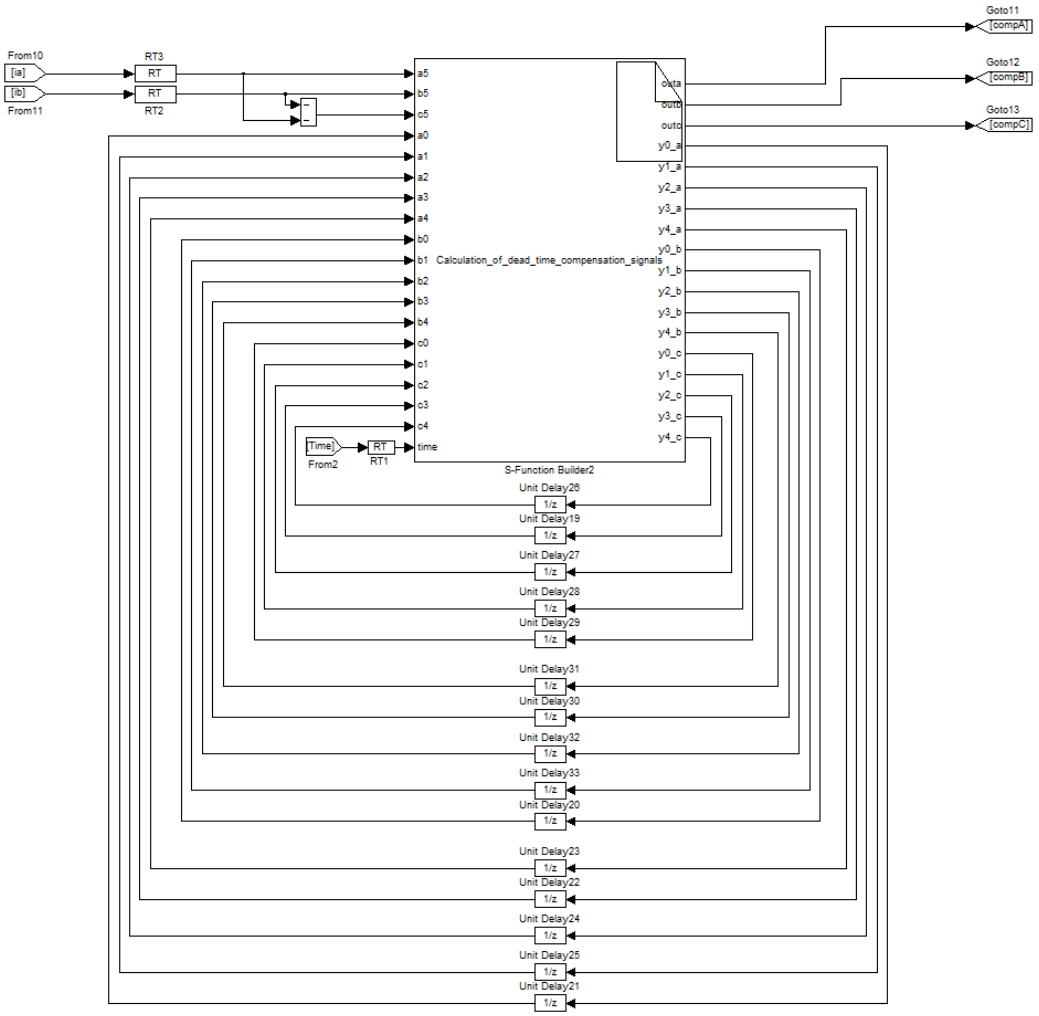


Figure 3-7 Calculation of dead time compensation signals

Since phase currents have noise because of switching, zero crossing points are more than one. In order to prevent oscillation caused by compensation near zero crossing points, when one zero crossing point is detected the compensation is implemented in that direction and direction of compensation is not changed until 10 sampling period passes. Since compensation changes its direction at least in 10 ms, 10 sampling period (correspond to 1.5 ms) will not affect dead time compensation.

In addition to above diagrams, one extra block is implemented in simulation environment. This diagram is used to insert dead time symmetrically to generated PWM signals. In conventional methods, dead time is inserted to generated PWM

signals directly and this asymmetric insertion results in moving center point of PWM by half of dead time. When switching frequency is low, this is not a big problem; however, as the switching frequency increases the dead time corresponds to important portion of switching cycle and losing the symmetry of PWM signal results in voltage loss in output waveforms. The diagram showing dead time insertion is given in Figure 3-8.

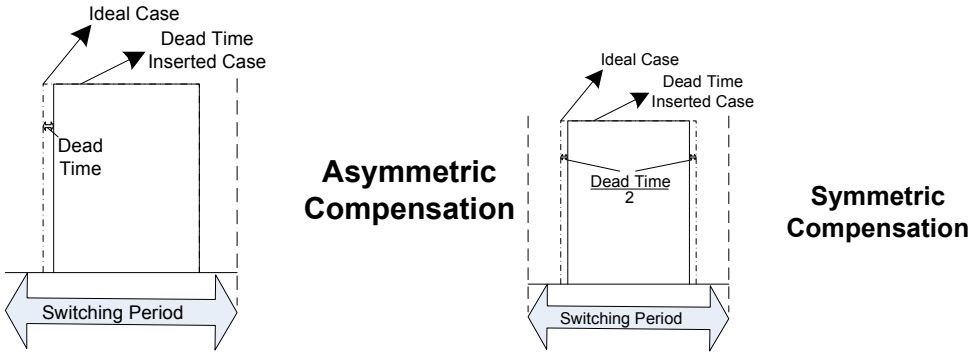


Figure 3-8 Conventional and symmetric dead time insertion

The related simulation block for symmetrical dead time insertion is given in Figure 3-9.

In experimental setup, DSP controller generates PWM signals and inserts adjusted dead time. Since inside of PWM block cannot be reached in DSP, the symmetric dead time insertion cannot be implemented in real environment with DSP. However, it can be implemented using FPGA controller which is not applicable for our case.

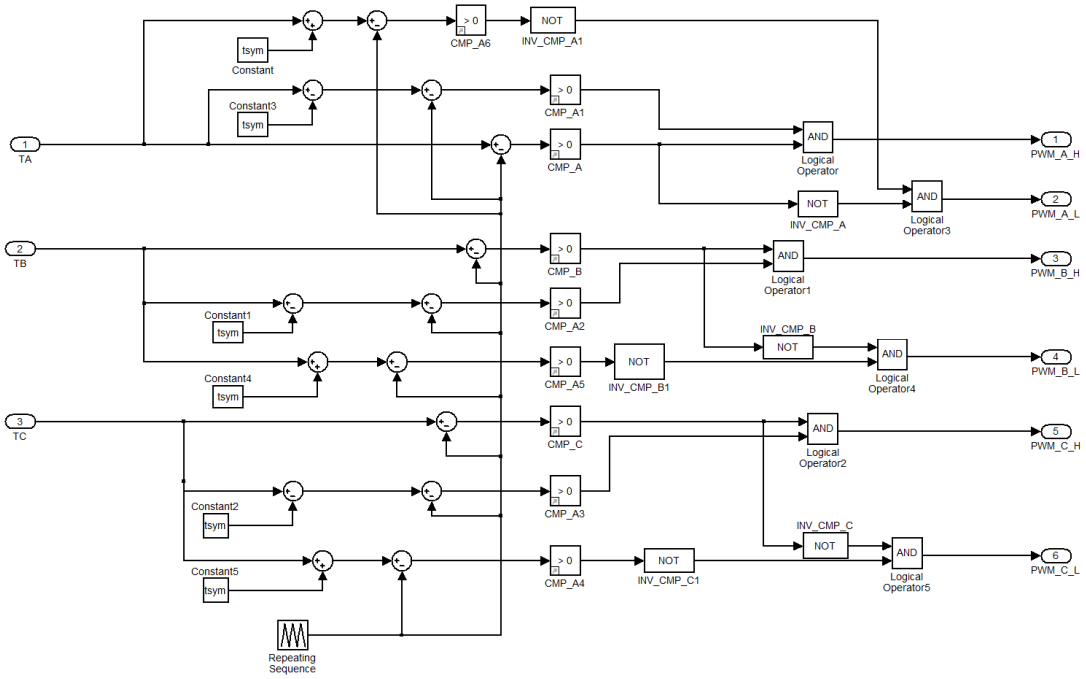


Figure 3-9 Symmetric dead time insertion module

3.17. User Interface for Motor Driver

In order to change control values during operation of motor, a user interface is created in ControlDesk program. By using this interface, all of the signal in software can be observed online. Moreover, the parameters such as speed reference, torque reference, implementation of compensations can be changed easily using the interface. The user interface for motor driver is shown in Figure 3-10.

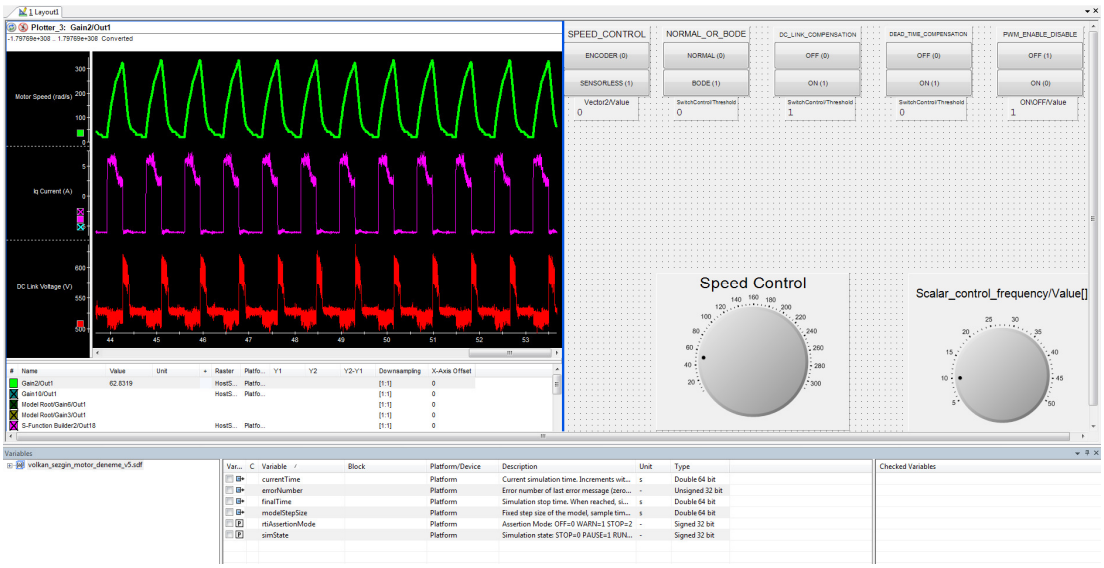


Figure 3-10 User interface program for motor driver system

3.18. Simulation Environment

In the experimental setup, trying of the new algorithms might harm the hardware environment caused by miscalculations. In addition, it is time consuming to verify the algorithms using experimental setup. Therefore, a simulation environment is developed. The new algorithms are initially tested and verified in the simulation environment. After verifying the algorithms, they are added to the drive software and they are verified experimentally.

3.18.1. Same Blocks with Software Environment

Since motor driver software is written in MATLAB/Simulink, some blocks prepared for software environment are used in simulation environment or vice versa. The list of used blocks as in software module is given below.

- Motor Parameters Definitions Module
- Variables and Definitions Module

- Obtaining Rated Flux Module
- AB to dq Transformations Module
- PI Controller Module
- DC Normalization Module
- Dq to αβ Transformations Module
- SVPWM Module
- Pulse Skipping Module
- Flux and Speed Estimation Module
- Digital Filter Module
- Dynamic Braking Module
- Dead Time Compensation Module
- DC Link Compensation Module

3.18.2. Voltage and Current Measurements Module

In simulation environment in order to measure voltage and current values, the current and voltage measurement blocks are used in MATLAB. Since the voltage and current values are exact values, no gain is inserted as in software environment. Motor voltages are pulsating signals and analog filters are used in hardware environment to filter switching frequency component and measure fundamental component. In simulation environment, digital filters are used to measure voltage waveforms. The voltage and current measurement blocks are given in Figure 3-11.

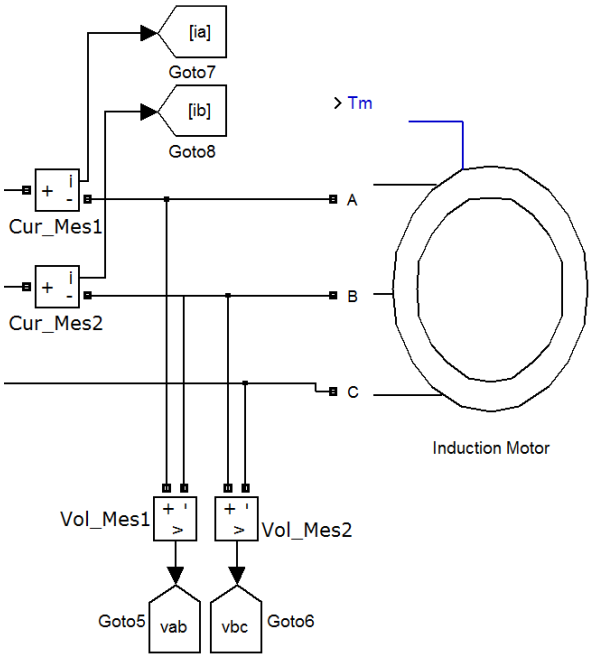


Figure 3-11 Voltage and current measurement blocks in simulation environment

3.18.3. PWM Generation Module

In software environment, the duty cycles after pulse skipping stage is sent to PWM module of DSP and PWM generation is realized inside DSP. However, in simulation environment, the pulses should be generated for IGBT gates. In order to generate PWM signals, triangular signal at switching frequency and magnitude 1 is created. After that, triangular signal is subtracted from duty cycles and the resultant signals are compared with 0. When resultant signal is greater than 0, the gate pulse becomes 1 or vice versa. In order to generate pulses for lower IGBT, the inverse of upper pulse is taken. After that, dead time is added between ON/OFF times of upper and lower IGBTs to avoid short circuit. In DC link compensation case, dead time is set to 0; however, it can be applied at any time and any value by changing one parameter in simulation environment. The related simulation block is given in Figure 3-12.

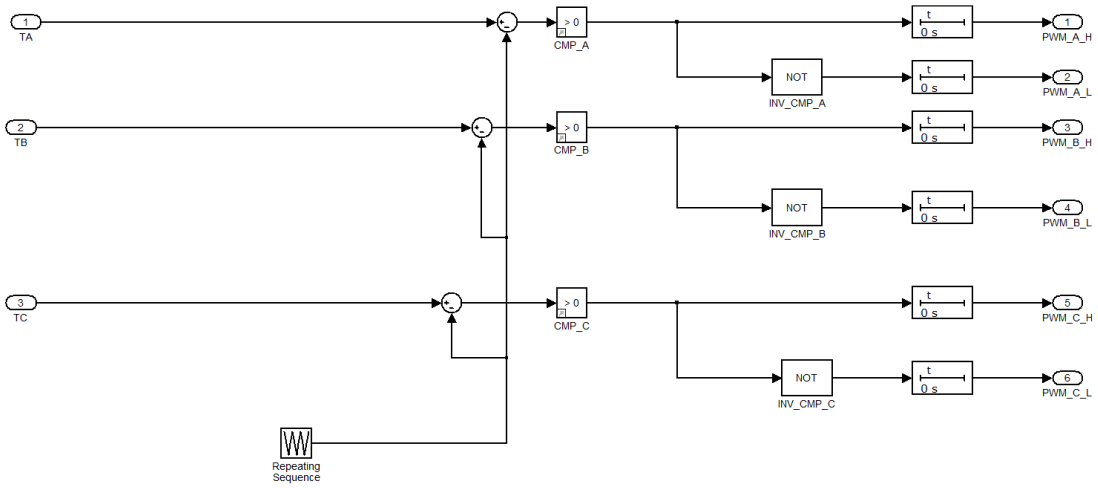


Figure 3-12 PWM generation block in simulation environment

3.18.4. Rectifier Block

In hardware environment, three phase grid voltage is rectified with diode rectifier to obtain DC link voltage. After that, DC link inductor and capacitor are placed to DC link. As in real case, three phase AC source is placed in simulation environment and three phase diode rectifier is used for rectification. After that, DC link inductor and capacitor are placed to DC link. The related block is given in Figure 3-13.

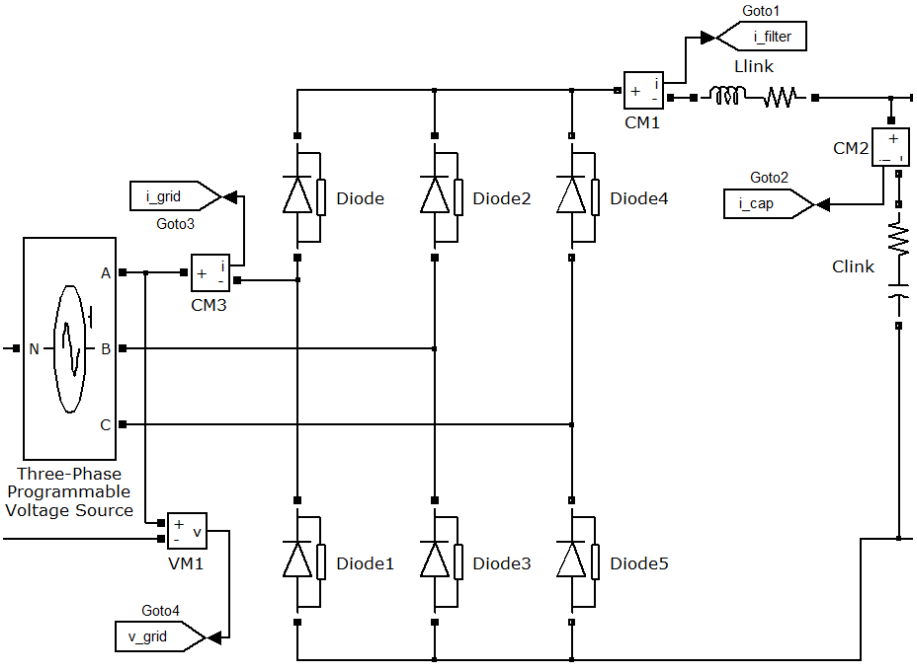


Figure 3-13 Rectification block in simulation environment

3.18.5. Intelligent Power Module Block

In hardware environment, 7-pack IGBT is used with their gate driver. Moreover, a brake resistance is used to dissipate excess energy for generating mode of motor. In simulation environment, 7 IGBT are placed and their gate signals are coming from control parts. In addition, a brake resistor is placed to dissipate excess energy as in hardware environment. The related block is given in Figure 3-14.

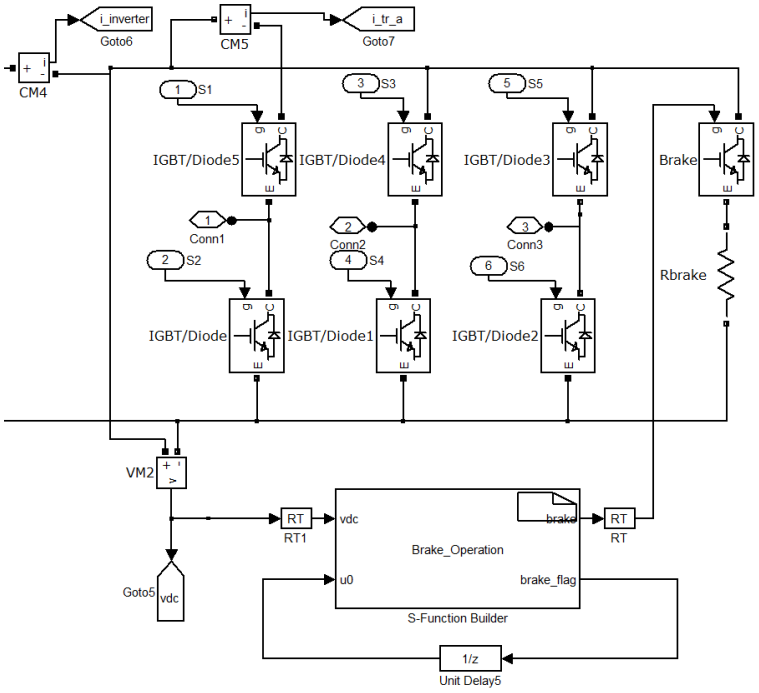


Figure 3-14 IPM block in simulation environment

3.18.6. Motor Block

In simulation environment, MATLAB/Simulink block is used for motor block. Its power rating is set to 1 kW and its speed rating is set to 2820rpm. The other parameters of motor are set as in software environment. The related block is given in Figure 3-15.

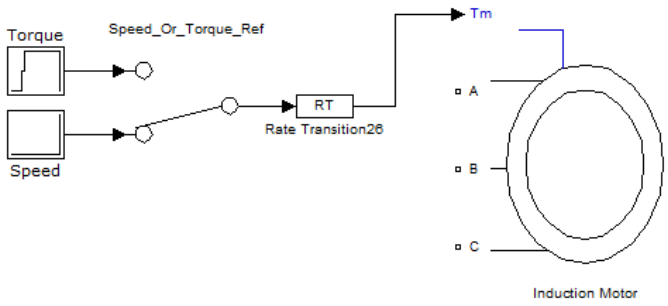


Figure 3-15 Motor block in simulation environment

CHAPTER 4

DC LINK FILTER DESIGN AND COMPENSATION

In motor driver applications, DC voltage is needed to obtain variable frequency and variable amplitude voltage at the motor terminals. DC supplies at high power/high voltage levels are expensive or do not exist. Therefore, in order to obtain DC voltage, the grid voltage (single phase or 3-phase) is rectified. There are mainly two types of rectification, namely, active and passive rectification. In active rectification, grid voltage is switched to obtain desired DC voltage and to decrease harmonic content of grid side currents and with this method DC link can be kept constant. In passive rectification, diodes are used and output voltage cannot be adjusted. The harmonic content of grid currents are high for diode rectification, however, this can be decreased to some extent by using filters in AC side or DC side.

In [20], it is stated that, the grid voltage at the connection points is 380V in three phase system in Turkey and it can vary ±5% in normal operating conditions. In emergency situations, it is allowed to vary between -8% to +6% of nominal voltage. Assuming normal operating for all times, the grid voltage can change from 361V (l-l, rms) to 399V (l-l, rms) in grid side. Driver with uncontrolled rectifier are designed for 380V AC source. Since DC link is created from grid side, these voltage drops will be seen in DC link voltage too.

In motor driver applications, DC link voltage is compensated for 300 Hz ripple component caused by rectifier or grid voltage variation as explained above. The main purpose in DC link compensation is that it is feed forward compensation, i.e., the output voltages are compensated at each sampling period instead of waiting for closed loop PI controller to compensate voltage error.

In this part, firstly DC link compensation is explained for operating region of SVPWM method. Then, the simulation and experimental results are given for compensated and uncompensated cases to see the effects of compensation.

After DC link compensation, DC link design is explained. The literature is reviewed for DC link design for motor driver applications and it is found that DC link is designed for steady state (rated power) conditions in the literature and dynamic conditions are not considered. For DC link design, the rated power of inverter is taken and the capacitance and inductance values are calculated for this value in the literature. However, in dynamic (acceleration) conditions, the torque value is set to 2 or 3 times rated torque value based on driver and motor capability to increase the dynamic performance of driver. During these periods, the power requirement of inverter increases up to 2 or 3 times rated values of inverter when speed value approaches to rated value. When driver power requirement exceeds its rated value, the designed parameters such as capacitor power loss, capacitor peak current, DC link lowest voltage, for DC link can exceed their limits. The detailed explanations for the DC link parameters are given in the following parts.

For analysis of DC link design, a simplified model for inverter is created and its components are explained. The simplified model is verified with motor driver simulation and experimental tests. After verifying the model, DC link is analyzed for 7.5 kW motor.

4.1. SVPWM Method in Linear Region and Over Modulation Region

Before going on DC link compensation part, brief explanations about SVPWM method in linear region and in over modulation region will be given. The detailed explanation about SVPWM method is given in [1].

4.1.1. SVPWM Method in Linear Region

Voltage utilization ratio is percentage of maximum output voltage to DC link voltage. As stated before, SVPWM method has more voltage utilization ratio compared to SPWM (Sinusoidal Pulse Width Modulation). In addition to that, it decreases torque pulsations and harmonic content of current waveforms.

The vector diagram of SVPWM method is given in Figure 4-1. In this figure, inner circle corresponds to linear region limits of SVPWM. The radius of the inner circle is maximum obtainable value for peak phase voltage and the edge length of hexagon is $2 * \frac{V_{dc}}{3}$.

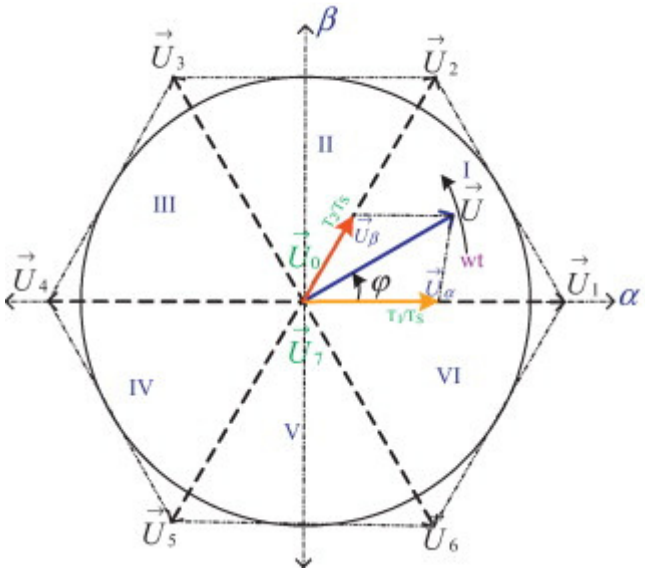


Figure 4-1 SVPWM diagram in linear region

Based on Figure 4-1, maximum value for peak phase voltage in linear region can be found as:

$$V_{peak} = Hexagon_{edge} * \sin(60) \tag{4.1}$$

$$V_{peak} = 2 * \frac{V_{DC}}{3} * \frac{\sqrt{3}}{2} \tag{4.2}$$

$$V_{peak} = \frac{V_{DC}}{\sqrt{3}} = 0.5774 * V_{DC} \quad (4.3)$$

For reference voltage inside of inner circle, the output vector is linearly changing with reference vector. For reference voltage vector outside of inner circle, the duty cycles becomes higher than 1 for some values depending on reference voltage amplitude and they saturate at the edge of hexagon. Because of saturation, harmonic content in current and torque waveforms increases.

4.1.2. SVPWM Method in Over Modulation Region

In [21], several modulation methods are examined in over modulation region. In this paper, "Gain" is defined as the ratio of output voltage to reference voltage and "M_i" is defined as ratio of output voltage to half of DC link voltage.

$$M_i = \frac{V_{out}}{V_{DC}/2} \quad (4.4)$$

$$G(V_{bus}) = \frac{V_{out}}{V_{commanded}} \quad (4.5)$$

Gain is 1 in linear region of SVPWM and linear region is up to Mi=1.15. After this point, gain is decreasing and goes to zero as the reference voltage goes to infinity which corresponds to six step operation.

Since output voltage loses its linearity, the desired voltage cannot be obtained at the output. For this reason, reference voltage is modified to obtain desired voltage at the output in over modulation region. The equation to update reference voltage and to obtain linear relation between output voltage and reference voltage is given as;

$$\frac{V_{out}}{V_{bus}} = \frac{1}{\pi} * \left\{ \sin^{-1}\left(\frac{1}{M_i}\right) + \frac{1}{M_i}\sqrt{1 - \frac{1}{M_i^2}} \right\} * M_i \tag{4.6}$$

In [22], over modulation range for different modulation topologies are examined. The modulation index is defined as;

$$m = \frac{u_1}{u_{1six-step}} \tag{4.7}$$

The voltage that can be obtained in six step operation is calculated as:

$$u_{1six-step} = \frac{2}{\pi} * U_{DC} \tag{4.8}$$

Maximum modulation index for SVPWM method in linear region becomes:

$$u_{1max} = \frac{U_{DC}}{\sqrt{3}} \tag{4.9}$$

$$m_{max} = \frac{\frac{U_{DC}}{\sqrt{3}}}{\frac{2}{\pi} * U_{DC}} = \frac{\pi}{2\sqrt{3}} = 0.907 \tag{4.10}$$

After linear region, duty cycle for three phases saturates at 1 for some points and reference duty cycles lose their sinusoidal shapes causing distortion in voltage and current waveforms. This distortion cause odd harmonics different from triple harmonics while increasing fundamental voltage magnitude.

In this paper, over modulation is divided into two regions.

- Over modulation mode I: Distorted Continuous Reference Signal
- Over modulation mode II: Distorted Discontinuous Reference Signal

In over modulation mode I, modulation index extends to 0.952 while it extends to 1 (six-step mode) in over modulation mode II.

In this method, it is mentioned that the voltage vector extends to outside of hexagon cannot be implemented and the calculation of zero vector for this vector gives unrealistic results. Therefore, the calculations should be modified for this situation. In the new calculations, only two adjacent vectors are switched and one phase will not be switched in this case. The modified equations for over modulation region and for vectors outside of hexagon are given as:

$$t_a = T_I \frac{\sqrt{3} * \cos\alpha - \sin\alpha}{\sqrt{3} * \cos\alpha + \sin\alpha} \tag{4.11}$$

$$t_b = T_I - t_a \tag{4.12}$$

The motor current waveform for different modulation index is given in Figure 4-2.

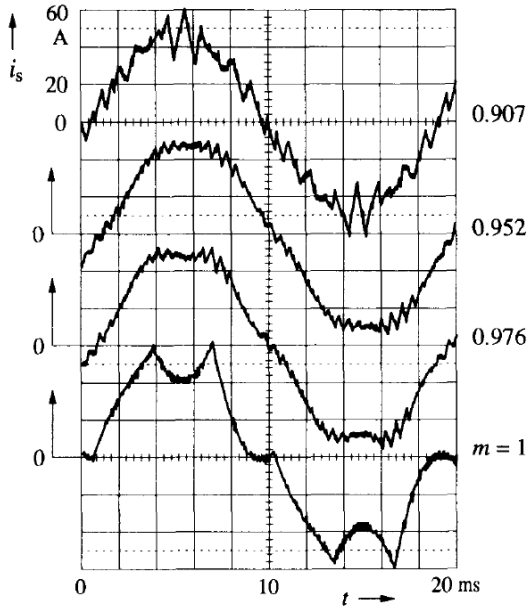


Figure 4-2 Motor current waveforms for different modulation index in [22]

In [23], continuous control for over modulation is examined. In this paper, single algorithm is proposed for linear region and over modulation region.

It is mentioned that the outputs that is outside of hexagon cannot be produced in SVPWM. Therefore, a method is proposed to obtain mean value for this vector in every 60^o interval. The method is explained as follows;

- A voltage vector is produced conventional SVPWM timing calculations when its trajectory is inside the boundary of hexagon.

- A fixed voltage and phase is produced until middle ($\pi/6$ for sector 1) of the related sector (amplitude=r, phase=a_g in Figure 4-3). After that, symmetrical component is produced with same amplitude and phase=$\pi/3$-a_g.

In this method, the intersection of hexagon and reference vector is difficult to find; however, this paper proposes a simple method for this purpose. In order to find the intersection, the point where zero vectors are calculated as zero should be determined. These points are intersection points.

Except from this, rms value of generated voltage is calculated as given in equation (4.13).

$$U_{rms}(r) = \frac{1}{\sqrt{2}} r \tag{4.13}$$

$U_{rms}(r)$=*rms value of produced voltage*

$r = amplitude\ of\ voltage\ vector$

From here it is seen that rms value is increasing with r, and worst harmonic will be seen in six step mode.

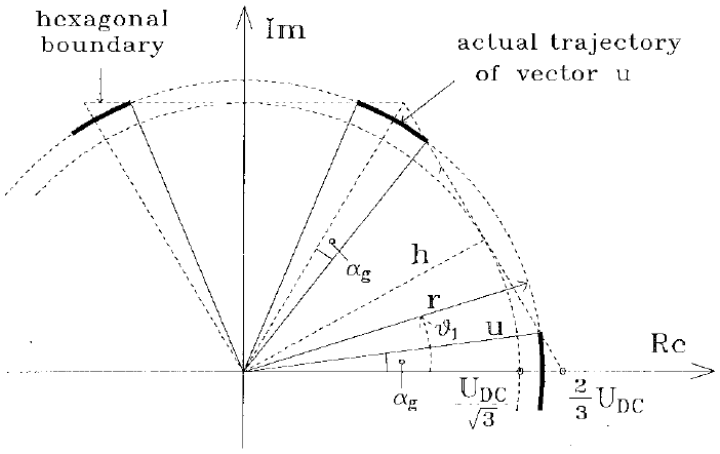


Figure 4-3 the trajectory in over modulation region

Comments on Literature:

From the literature survey about over modulation, it can be concluded that;

- Over modulation increases harmonic content in output current waveforms while increasing fundamental voltage amplitude.

- The output vector is linear in linear region and it loses its linearity in over modulation region.

- The limit for over modulation is inside of hexagon; outside of hexagon cannot be produced with SVPWM method.

- There are two regions for over modulation. These regions correspond to modulation index values 0.952 and 1. When modulation index is equal to 1, it becomes six-step operation.

Considering the methods explained in the literature, over modulation in our driver will be implemented until modulation index is equal to 0.952 in order for acceptable harmonics in current waveform and higher fundamental output voltage. For the algorithm, timing calculations will be done as if driver always operates in linear

region. After timing calculations, DC link compensation algorithm will be implemented until modulation index is equal to 0.952. After this point, modulation index will be maintained at this value and desired output voltage will not be obtained.

The calculation for modulation index for our driver is given in equations (4.14) and (4.15).

$$Modulation\ Index = M_i = \frac{V_{fund}}{\frac{2}{\pi} * V_{DC}} \tag{4.14}$$

$$V_{fund} = \frac{2}{\pi} * V_{DC} * M_i = 0.606 * V_{DC} \tag{4.15}$$

When modulation index is equal to 0.952, the reference voltage vector becomes $\frac{2}{3} * V_{DC}$ which is the edge length of the hexagon.

4.2. DC Link Compensation

Before going on DC link design, DC link compensation should be explained. After compensation, DC link design will be explained as if compensation is implemented.

4.2.1. Literature Survey about DC Link Compensation

In [24], DC link compensation for drives is explained. The rectifier side and DC link components and their simplified model is shown in Figure 4-4.

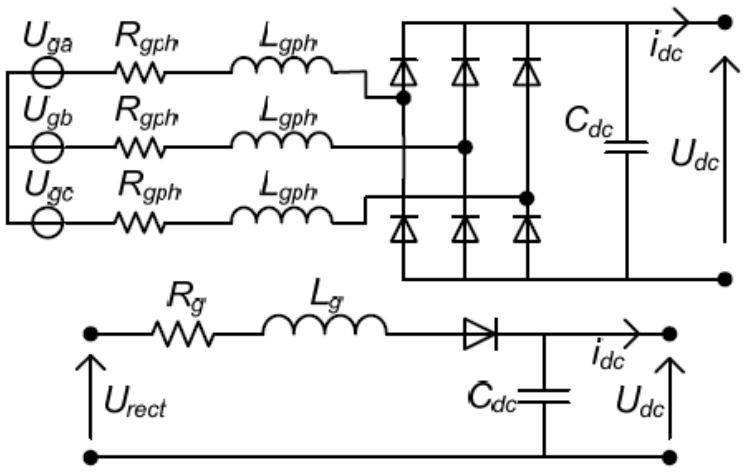


Figure 4-4 DC link and its simplified model in [24]

DC link composed of three main components, namely, rectified component at 6 times grid frequency, resonant component due to L-C oscillation and switching component. Switching component is not considered for DC link compensation in this work.

For DC link compensation, firstly compensated voltage (U_{dccomp}) is extracted by using measured DC link voltage (U_{dcmeas}), reference DC link voltage (U_{dcref}) and reference motor voltage (U_{cont}). Therefore, the reference voltage given to SVPWM block is updated with respect to SVPWM block; however, it loses linearity in over modulation region and cannot fully compensate DC link.

$$U_{dccomp} = U_{cont} * \frac{U_{dcref}}{U_{dcmeas}} \tag{4.16}$$

With this method, DC link is not fully compensated because DC link ripple is high and due to processing delays (one or two sample delay). Voltage errors caused by measurement delay are shown in Figure 4-5. In order to compensate measurement delay (one sample delay causes 150µs delay in our case and it causes 2.7^o delay and it can cause incorrect DC link voltage up to 12V), an algorithm should be implemented. For this algorithm, DC link ripple should be separated into resonant component and rectified component first. To be able to separate these components in software with band pass filter, resonant component frequency must be two times

larger than rectified component. After separating the resonant component from DC link voltage, rest of DC link is delayed by half period of ripple frequency. By this way, the DC link voltage is obtained so that there is no delay between measurement stage and voltage generation stage.

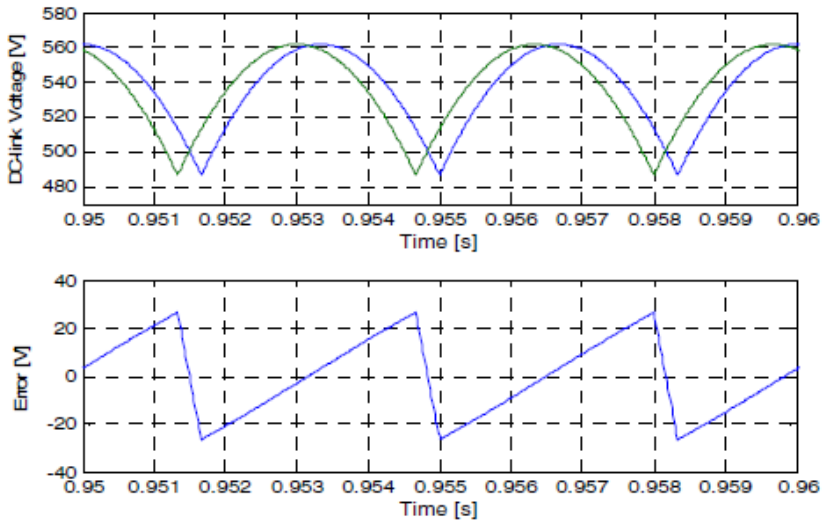


Figure 4-5 Compensation Error due to 2 sample delay in [24]

The related control diagram for this method is given in Figure 4-6.

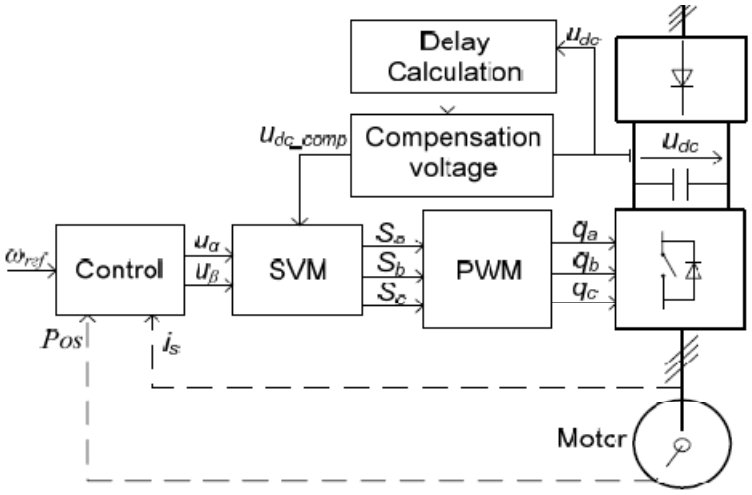


Figure 4-6 Control diagram for DC link compensation in [24]

As seen from the figure, DC link voltage is filtered to eliminate resonance component and delay caused by sampling period is added to measured voltage. After obtaining DC link voltage, this voltage is fed to SVPWM block and reference voltages for α and β axes are divided to normalized DC link voltage.

The results show that this method decreases motor current harmonics and decreases motor acoustic noise at rectified component frequency.

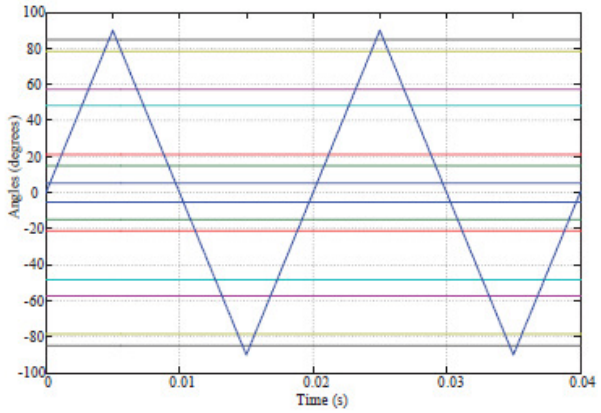
In [25], DC link voltage ripple compensation for multilevel inverters is explained. In this paper, DC link compensation is implemented changing modulation index with respect to measured DC link voltage.

The modulation index with respect to DC link voltage becomes:

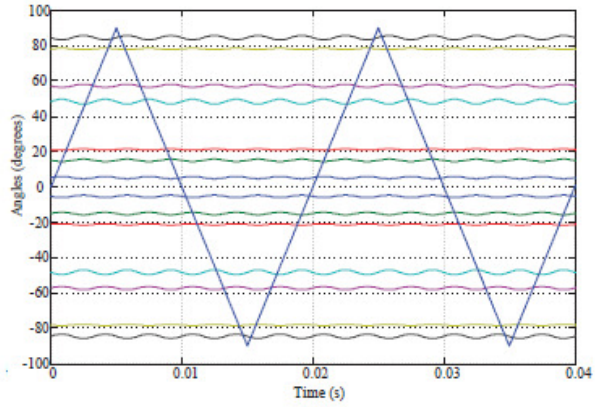
$$V'_{dc} = V_{dc}(1 + r * \sin(w_r * t)) \tag{4.17}$$

$$M' = \frac{M}{1 + r * \sin(w_r * t)} \tag{4.18}$$

Modulation index for changing DC link voltage is given in Figure 4-7.



(a) Constant DC-link voltage (M=1.2, k/m=3/4)



(b) 5% sixth harmonic ripple

Figure 4-7 Modulation index adjustment with respect to DC link voltage in [25]

The results show that DC link is fully compensated until modulation index saturates at 1. After this point, DC link cannot be fully compensated because the modulation index exceeds the limits and desired outputs cannot be obtained.

In [26], frequency converter with small DC link capacitor is explained. In this paper, small film capacitor is used instead of electrolytic capacitor in DC link in order to decrease grid side current harmonic. After that a new modulation technique is introduced for DC link compensation.

When small DC link capacitor is used, DC link ripple voltage will be high and error value in measured DC link voltage will increase. For this reason, SVPWM method

may not work properly because of this error in measurement stage. Therefore, new method is implemented to compensate DC link. This method is called as Differential SVPWM (DSPWM). This method calculates voltage integral during switching period. When integral value reaches the reference value, switch is opened. The equations for PWM generation block are;

In generic method (SVPWM), the reference voltage vector is calculated as given in equation (4.19).

$$u_{s,ref} * T_s = t_m * V_m + t_{m+1} * V_{m+1} \tag{4.19}$$

In this equation, pulse durations are determined and switches will be turned off after the duration calculated by this equation will pass. However, in this method, pulse durations are not determined and the related switch will be opened after the desired flux is obtained. The equations are given below.

$$\Delta\lambda_{s,ref} = \Delta\lambda_m + \Delta\lambda_{m+1} \tag{4.20}$$

$$\Delta\lambda_{s,ref} = t_m * V_m + t_{m+1} * V_{m+1} \tag{4.21}$$

$$\Delta\lambda_m = \int V_m dt\,, \qquad When\ V_m\ is\ active \tag{4.22}$$

$$\Delta\lambda_{m+1} = \int V_{m+1} dt, \qquad When\ V_{m+1}\ is\ active \tag{4.23}$$

Using the relations given above, flux linkage generated by related vector is calculated during switching period and switches are turned off when the flux linkage is at desired level. This method needs lower sampling period for processor to calculate voltage integration during switching period. Moreover, this method is applicable in linear region. When DC link voltage drops to levels where linear region is not enough for compensation, this method fails and it is needed to change modulation to SVPWM method.

Since this method is based on voltage integral, it actually calculates the flux linkage for switching period. When the reference flux linkage value is obtained, then the related switch is turned off.

The results show that DC link is fully compensated with given method in linear region. Since there is delay between voltage measurement and instantaneous value, SVPWM method have some errors at the output. However, this method calculates flux linkage and it obtains correct voltage at the output. The drawback of this method is that it requires higher sampling periods for integration which is not applicable for our case.

Comments on Literature

In the summarized papers, DC link is compensated but the difficulties in implementation are not mentioned.

For [24], the computational burden of processor is increased because implementing a filter is difficult and not recommended in digital environment. Moreover, the filter may take some part of rectified component while filtering resonant component and gives incorrect results because the resonant frequency is close to ripple frequency. Therefore, it is not reasonable to implement this method.

For [26], it is hard to implement integration within switching period because integration within switching period needs processor cycle frequency at least 10 times higher than switching frequency. In real cases, the limitation for switching frequency is processor cycle time for most of the applications. Therefore, it is not reasonable to implement this method.

For [25], DC link compensation is implemented in simple way by changing modulation index with respect to measured DC link voltage. This can be implemented very easily in software environment; however, output voltage is not linear in over modulation case and some lookup tables or formulas should be created

for over modulation case. Therefore, the idea in this paper can be used considering the over modulation region.

In our method, duty cycles are updated with respect to actual DC link voltage. In order to avoid calculation of negative timings or timings exceeding 1 in SVPWM block, timings are calculated for constant DC link voltage. After duty cycle generation in SVPWM module, duty cycles are updated with respect to DC link voltage. Finally, reference duty cycles are limited for 0.952 modulation index.

4.2.2. Methodology

Considering compensation both in linear region and over modulation region two methods are tested in simulation environment. The detailed explanations about modulation regions are given in previous part.

First Method:

In SVPWM method linear region, output voltages at motor terminals are same as with reference voltage. After linear region, reference voltage cannot be obtained because the duty cycles are limited to 1 and it cannot generate desired value. Therefore, reference voltage should be modified to obtain desired voltage at the output. For this reason, a lookup table for over modulation region is generated. In this table, the reference voltage values for desired output voltages are given.

Since over modulation region starts at 311V and ends at 326V, a lookup table for over modulation region is created. If more resolution is needed or the number of voltage levels is higher, then neural network or some curve fitting functions may be created.

In order to create lookup table, SVPWM is operated at different reference voltages and their outputs are recorded. After simulation results, the values are written in a table and missed voltages at the output are interpolated from neighborhood voltage levels. Finally, the lookup table is created as given in Table 4-1.

Table 4-1 Lookup Table for DC link compensation

Desired Output Voltage (V)	**Reference Voltage (V)**
311	312
312	314
313	316
314	318
315	320
316	321
317	323
318	325
319	327
320	330
321	333
321	336
322	339
323	342
324	345
325	350
326	355

From this table, it can be decided which reference voltage is needed to obtain desired voltage at the output in over modulation region. After that, SVPWM module (α and β voltages are updated with respect to lookup table in over modulation region) in the software is run with respect to this reference voltage. By this way, the generated duty cycles become compensated duty cycles.

Second Method

DC link voltage is used to calculate reference duty cycles. In equations given below, K is used for modulation constant, T_k is timing for k^{th} vector and T_Z is zero vectors.

Thus, DC link compensation can be implemented simply modifying the reference duty cycles with respect to actual DC link voltage.

$$K = \frac{\sqrt{3}}{2} * \frac{T_S}{V_{DC}} \tag{4.24}$$

$$T_k = \frac{K}{2} * \left(\sqrt{3} * V_{sref\alpha} - V_{sref\beta}\right) \tag{4.25}$$

$$T_{k+1} = K * V_{sref\beta} \tag{4.26}$$

$$T_Z = T_S - (T_k + T_{k+1}) \tag{4.27}$$

If the modulation constant is corrected with respect to actual DC link voltage, the desired output voltage can be obtained. In our method, instead of changing K value, reference duty cycles are updated after SVPWM module. The reason is that when K is updated negative zero vector (T_Z) can be calculated for lower DC link voltages. By implementing DC link compensation after SVPWM, this situation is eliminated.

The DC link compensation is implemented as in Figure 4-8. By applying compensation at this stage, the bandwidth of compensation becomes equal to sampling frequency of software. Since sampling frequency (6.6 kHz) is much higher than ripple frequency (300 Hz), the ripple on DC link can be easily compensated with this method. If we increase the sampling frequency of driver, then we can minimize voltage measurement error caused by sample delay explained in literature review. Therefore, our aim in the future is to increase the sampling frequency to obtain better performance for DC link compensation.

In order to limit compensation so that modulation index would not exceed to 0.952, there is a saturation block in compensation module and this block is preventing increase of modulation index after 0.952. When DC link voltage drops 515V, the saturation block limits the output and modulation index is maintained at 0.952.

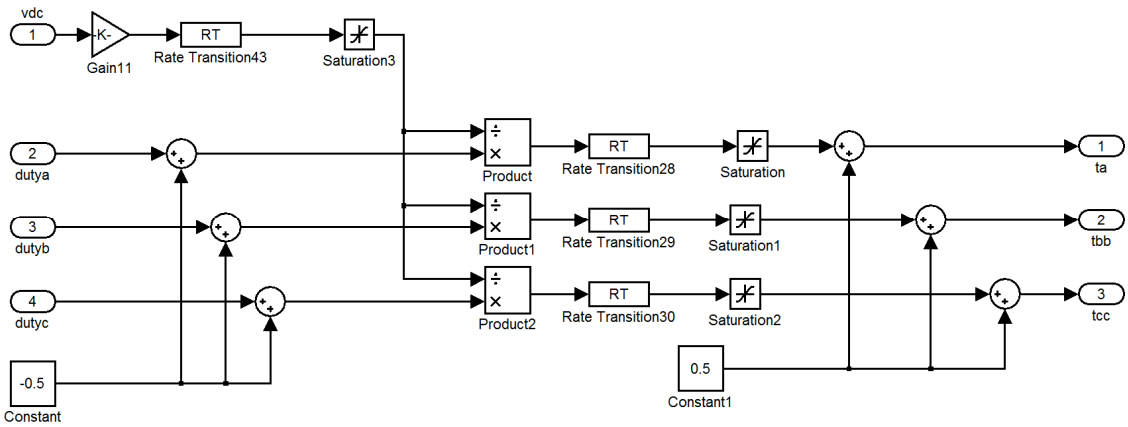


Figure 4-8 DC link compensation in linear region

The duty cycles are updated as:

$$duty_a\,(updated) = duty_a * \frac{V_{DCmeas}}{V_{DCref}} \tag{4.28}$$

$$duty_b\,(updated) = duty_b * \frac{V_{DCmeas}}{V_{DCref}} \tag{4.29}$$

$$duty_c\,(updated) = duty_c * \frac{V_{DCmeas}}{V_{DCref}} \tag{4.30}$$

V_{DCmeas}=Instantaneous DC link voltage

V_{DCref}=Reference DC link voltage (537V for our case)

Although this method causes some voltage loss in over modulation region, it is very good and implemented simply in both linear region and over modulation region.

4.2.3. Simulation Results

The motor parameters and the DC link parameters used in the simulation are given in Table 4-2.

Table 4-2 Motor and DC link parameters in simulation environment

Simulation Parameter	Value
DC Link Inductor (mH)	1
DC Link Capacitor (µF)	370
Switching Frequency (kHz)	6.6
AC Source Voltage (V, rms)	380
Rated Motor Power (kW)	1

In order to see the effects of compensation, firstly uncompensated results are obtained. After that, two compensation methods are implemented and their effects are analyzed. For the simulation, motor is run with open loop V/f control to see the ripple voltage effects; otherwise, when vector control operation is implemented, PI controller would try to compensate error and the effect of ripple voltage would not be seen clearly. Moreover, motor is run at rated torque and rated speed to maximize voltage drop on DC link. To see the effects of compensation, DC link voltage ripple, motor currents and torque waveform are measured.

The simulation results for uncompensated and compensated cases are given in the following figures.

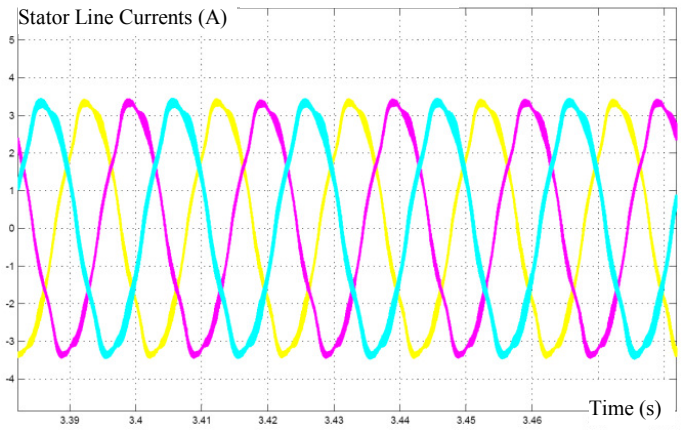


Figure 4-9 Stator currents for uncompensated case

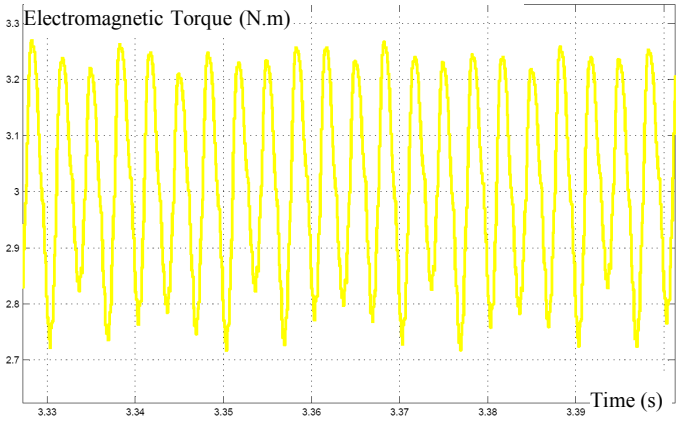


Figure 4-10 Electromagnetic torque for uncompensated case

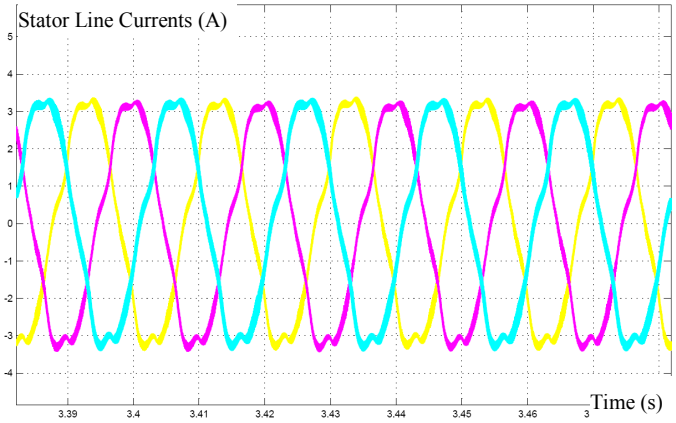


Figure 4-11 Stator currents for compensated case (1st method)

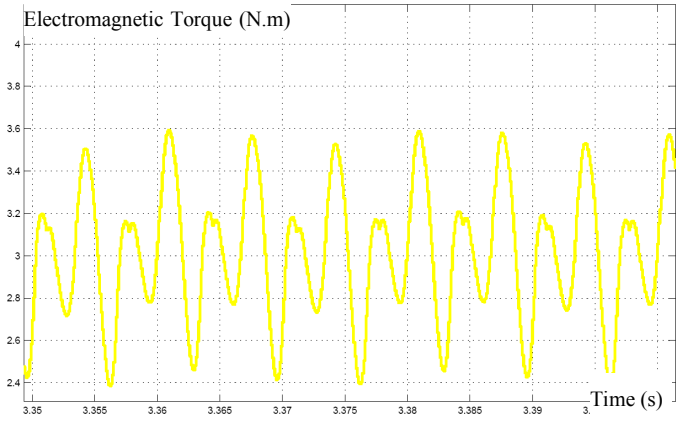


Figure 4-12 Electromechanical torque for compensated case (1st method)

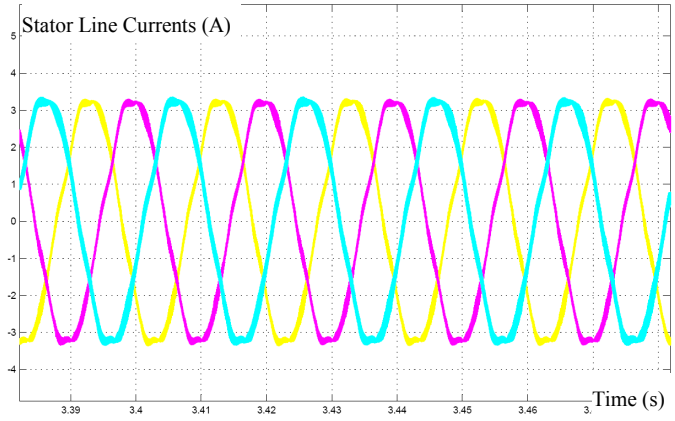


Figure 4-13 Stator currents for compensated case (2nd method)

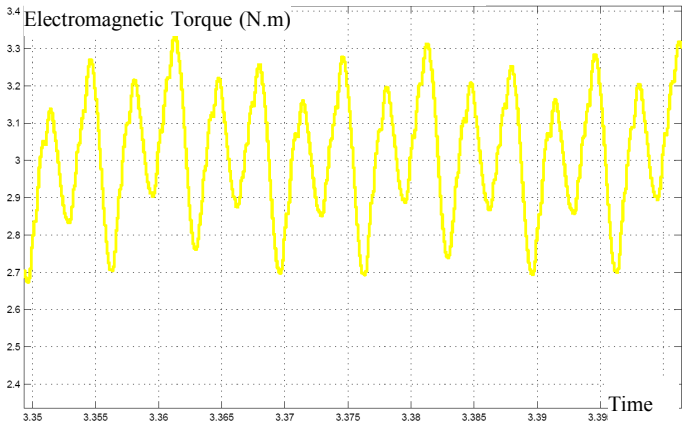


Figure 4-14 Electromechanical torque for compensated case (2nd method)

The results for compensated and uncompensated cases are shown in Table 4-3 to see the differences clearly.

Table 4-3 Simulation results for compensated and uncompensated cases

	T_L= 3 Nm	T_L= 3 Nm	T_L= 3 Nm
	Uncompensated	**Compensated (1^{st})**	**Compensated (2^{nd})**
Vline-line (V-Peak)	525,6	539,9	533,9
Voltage THD (%)	52,48	48,52	50,27
Voltage DC Offset (V)	0,01	0,07	0,251
Phase Current (A-Peak)	3,326	3,34	3,327
Current THD (%)	4,83	7,8	4,47
Current DC Offset (A)	0,0001	0,002	0,03
Torque Ripple (N.m)	0,5	1	0,5
Dc Link Voltage Ripple (V)	30	30	30
Reference Voltage (V)	537	537	537

As seen from Table 4-3, compensation effects are;

- Harmonic content in current waveforms are decreased
- Ripple on electromechanical torque is decreased
- Output voltages are increased to desired level

As seen from the results, although first method could apply higher output voltages with respect to second method, the harmonic content and ripple torque of first method is not acceptable. In future works, the first method can be improved by using some curve fitting functions for non-linear region of SVPWM.

Although second method does not fully compensate in over modulation region because of non-linearity of SVPWM, it does not cause considerable voltage loss at the output. As seen from the results, there is only 3V voltage loss (%0.57 percent of reference voltage) at worst condition of DC link voltage (for designed value) and

maximum reference voltage. Since the torque ripple and current harmonics are smaller in second method, it is used in experimental setup.

Dynamic Performance Simulation Results

In the literature, dynamic performance of a driver is generally determined as the time to reach desired torque level. The torque level and reaching time can change for driven motor. In our application, same motor is used for all conditions and the relative difference for compensation will be considered. Therefore, for the dynamic performance of the driver the settling time of torque will be measured.

The transient change for torque can be in two forms. One is to change the torque reference to higher or lower level in same direction. The other one is to change torque reference direction. For the worse case, the direction reversal case is considered in this work. For torque reversal conditions, the torque reference change its direction and output torque should respond quickly this reference for high performance driver. Since our aim is to increase the performance of the driver by compensating DC link, the dynamic performance of the driver will be measured before and after compensation. The simulation results for torque reversal condition are given in Figure 4-15 and Figure 4-16.

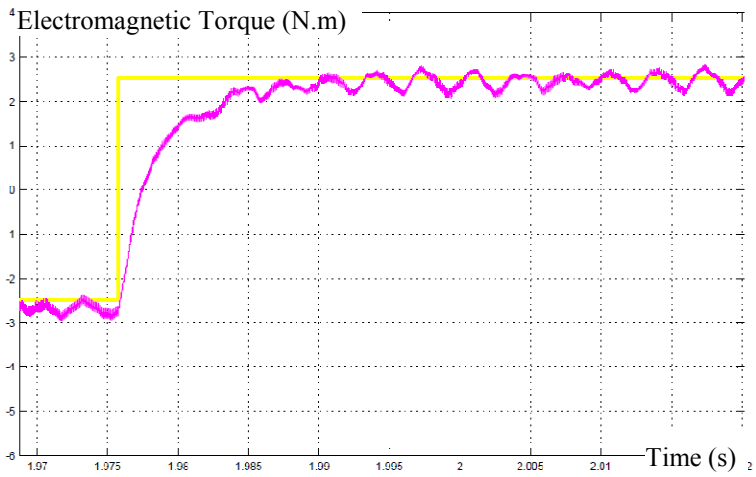


Figure 4-15 Dynamic performance test torque settling time for uncompensated case (yellow: reference torque, pink: actual torque)

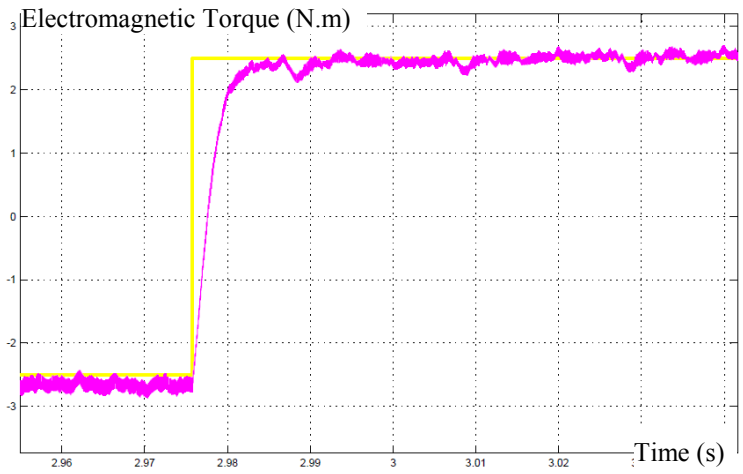


Figure 4-16 Dynamic performance test torque settling time for compensated case (yellow: reference torque, pink: actual torque)

As seen from Figure 4-15 and Figure 4-16, the settling time of torque is smaller in compensated case. In addition, the torque ripple after settling is also smaller in compensated case. The settling time of compensated case is about 9 ms whereas it is 13 ms for uncompensated case. Therefore, it can be concluded that DC link compensation increases dynamic performance of driver.

After simulation results, experimental results for V/f control and dynamic condition are obtained.

4.2.4. Experimental Results

In order to see effects of DC link compensation, motor driver is tested in experimental setup. For experiment, V/f open loop control method is used.

Table 4-4 Experimental results

	T_L= 1 Nm	T_L= 1 Nm
	Uncompensated	**Compensated (2nd)**
Vline-line (V-Peak)	363,5	374,76
Voltage THD (%)	88	85
Voltage DC Offset (V)	1	0,7
Phase Current (A-Peak)	1,2	1,2
Current THD (%)	10,01	9,9
Current DC Offset (A)	0,05	0,05
Dc Link Voltage Ripple (V)	15	15
Reference Voltage (V)	389	389

As seen from the experimental results, DC link compensation works properly. However, the output voltage is lower than desired voltage level. In experimental setup, dead time compensation is implemented; however, it cannot fully compensate voltage loss caused by dead time because current detection cannot be implemented perfectly as in simulation environment. Therefore, it compensates some part of the lost voltages. Another reason of voltage loss is that the voltage drop on IGBT and cable causes voltage loss in output voltage.

Based on the simulation and experimental results, it can be concluded that DC link is successfully compensated with proposed algorithm.

Dynamic Condition Test Results

In order to see the effects of compensation in dynamic conditions, the square wave torque reference is given to the motor. Actual torque value is measured with respect to reference torque. The results are given in Figure 4-17 and Figure 4-18. The period of square wave is 21ms.

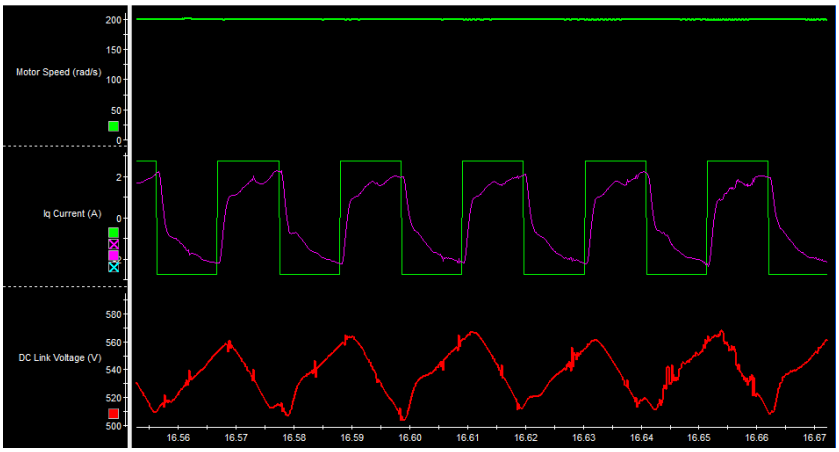


Figure 4-17 Dynamic performance test for uncompensated case (green: reference torque, pink: actual torque)

Figure 4-18 Dynamic performance test for compensated case (green: reference torque, pink: actual torque)

As seen from the figures, the actual torque value cannot reach the reference value for uncompensated case whereas it can reach the reference torque level for compensated case.

4.3. DC Link Design for Improving Dynamic Performance

4.3.1. Literature Survey

In [27], the DC link consists of DC link inductor and capacitor. Their values are chosen so that the resonant frequency of DC link components is higher than 6 times mains frequency and lower than switching frequency. In this paper, diode rectifier is used to obtain DC link voltage. The simplified model for resonance circuitry is given in Figure 4-19.

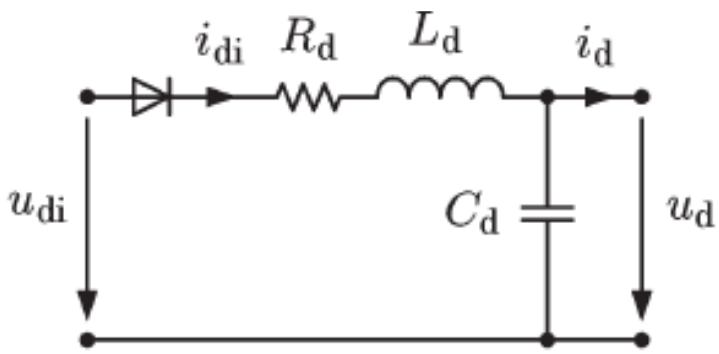


Figure 4-19 Simplified model for resonance circuitry in [1]

The resonance frequency of DC link can be calculated as:

$$w_n = \frac{1}{\sqrt{L_d * C_d}} \tag{4.31}$$

Since resonance frequency is higher than 6 times mains frequency and it is lower than switching frequency, the inductance value for chosen capacitance value is calculated as:

$$\frac{1}{w_{sw}^2 * L_{d,min}} < C_d < \frac{1}{(6 * w_g)^2 * L_{d,max}} \tag{4.32}$$

From this equation, for a chosen 24μF capacitance value, inductance value can be between 43μH and 11mH. In order not to be close to upper and lower limits for the resonant frequency, the inductance value should not be chosen close to the limits. For this application, transformer inductance is used as DC link inductance (actually it is used before diode rectifier, but it can be said as DC link inductance).

The results show that total harmonic distortion is better when DC link capacitance is lower. Although, torque ripple increases for small DC link capacitance, this ripple can be acceptable for some applications.

In [28], the usage of film capacitors instead of electrolytic capacitor is discussed. Although electrolytic capacitors have high capacitance value per volume, they have shorter lifetime and they are vulnerable to reverse voltages. Therefore, in recent applications, their usage is decreased. Instead of electrolytic capacitors, film capacitors are used in new applications because their lifetime is higher and they can stand reverse voltages. Lifetime has importance especially for renewable energy systems because they are located in remote location and increased lifetime decreases maintenance costs.

Moreover, new film capacitors can overcome internal defects by melting inside thinner metallic layer and isolating defect. This mechanism is called as self-healing.

Film capacitor has higher current capacity with respect to electrolytic capacitors. Therefore, for a design, the only concern for capacitor selection is its capacitance value.

Film capacitor has higher voltage rating. In order to reach higher voltage with electrolytic capacitors, they are connected in series. However, series connection requires balancing of voltage and this requires resistors parallel with capacitors and it increases leakage current.

The results show that film capacitor should be used in new applications because of higher lifetime; higher current capacity and capability of withstanding reverse voltages.

In [29], design considerations for DC link are explained. Some of the listed requirements for DC link are;

- The inductor current should be continuous and its ripple value should be less than a specified value.
- The capacitor ripple voltage should be less than a specified value.
- Resonance frequency of DC link should be much lower than switching frequency.

For capacitor selection, equation (4.33) is used.

$$C_F = \frac{\Delta Q_M}{\Delta V_{PP}} \tag{4.33}$$

In this equation, ΔV_{PP} is voltage ripple and it is specified for an application. In order to calculate capacitance (C_F), change of charge (ΔQ_M) value should also be known and its value is calculated considering that all power for inverter is supplied from capacitor.

For inductor selection, equation (4.34) is used.

$$L_F = \frac{\Delta v_{ti,max}}{\Delta i_{PP}} \tag{4.34}$$

After calculating inductor and capacitor values, their values should be considered in terms of resonant frequency configuration. It is considered that 6 times grid frequency should be higher than resonant frequency of DC link. The resonant frequency criterion is given as:

$$f_0 \left(= \frac{1}{2 * \pi * \sqrt{C_F * L_F}} \right) < 6 * f_I \tag{4.35}$$

In this equation, the f_I is input grid frequency and f_0 is resonant frequency of DC link components.

If C_F is known, then L_F can be calculated as:

$$L_F > \frac{1}{C_F (12 * \pi * f_I)^2} \tag{4.36}$$

The results show that DC link should be designed both voltage and current ripple. In addition, resonant frequency of DC link should also be considered while designing DC link.

In [30], LC filter design for AC motor drives is explained. In this paper, rules for DC link design are listed as;

- Calculate capacitance value for a specified ripple voltage
- Calculate ripple current
- Size capacitor bank
- Size DC link inductor

In order to calculate capacitance value, the acceptable ripple voltage for DC link should be specified. After specifying ripple voltage, capacitance value is calculated considering that all power to inverter is supplied from capacitor. The capacitance equation becomes:

$$P_{inverter} = \frac{(\frac{1}{2} * C_F * V_{max}^2 - \frac{1}{2} * C_F * V_{min}^2)}{\frac{1}{6 * f_{grid}}} \quad (4.37)$$

V_{max}= *Maximum DC link voltage*

V_{min}=*Minimum DC link voltage*

f_{grid}= *Mains frequency*

C_F= *DC link capacitance*

After calculating capacitance value for an application, ripple and rms current values for capacitor and inverter side is calculated.

After determining current values, the power losses on capacitor bank is calculated considering power loss on capacitors. When power loss is higher than expected value, the DC link inductor should be placed in order to decrease power loss on capacitor and to decrease ripple current.

$$L_F = \frac{\frac{V_L}{I_L}}{\frac{1}{6 * f_{grid}}} \quad (4.38)$$

V_L: *Inductor voltage*

I_L: *Inductor current*

L_F: *DC link inductance*

In this equation, inductor voltage is calculated to decrease capacitor loss and after calculating inductor voltage, inductor current is calculated. Finally, inductance value is calculated using these values.

After calculating DC link components, DC link resonant frequency is calculated. If the resonant frequency is higher than 6 times grid frequency, the inductance value should be increased to decrease resonant frequency below 6 times grid frequency. In order not to oversize inductor, the resonant frequency can be kept higher than 4 times grid frequency.

Comments on Literature

DC link is composed of DC link inductor and DC link capacitor. The criterion for capacitor selection is acceptable voltage ripple. The criterion for inductor selection is ripple current or resonant frequency limitation which should be decided for an application. Finally, film capacitors can be used instead of electrolytic capacitors because of higher lifetime and higher current capacity. However, it increases cost and size of the driver because it is volume/capacitance ratio is high. In addition, it can stand reverse voltages.

4.3.2. DC Link Design Procedure

As stated in previous parts, DC link is composed of capacitor and inductor in most of the applications. Therefore, DC link will be designed with inductor and capacitor for our driver. As stated in introduction part, in literature, DC link design is implemented considering rated power conditions of driver. However, in acceleration conditions, the torque value is set to 2 or 3 times rated torque value based on driver and motor capability to increase the dynamic performance of driver. During these periods, the power requirement of inverter exceeds its rated value. For this reason, DC link voltage decreases to lower values than designed value and the capacitor power loss and its peak current increases. In order to see the problem clearly, a motor driver simulation is implemented for 7.5 kW motor. For the simulation, DC link is compensated. The simulation results for rated power and dynamic conditions are given in Figure 4-20 and Figure 4-21.

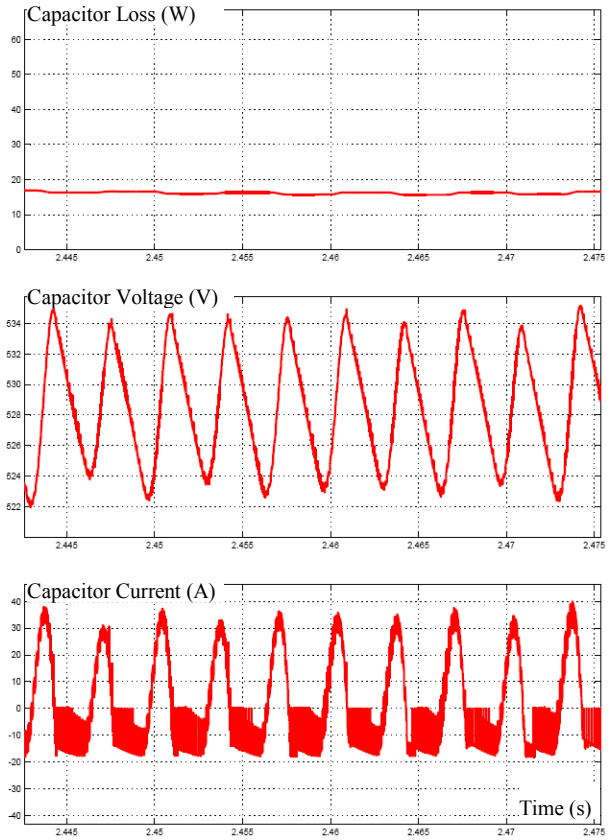


Figure 4-20 Rated power condition motor driver simulation results for designed filter

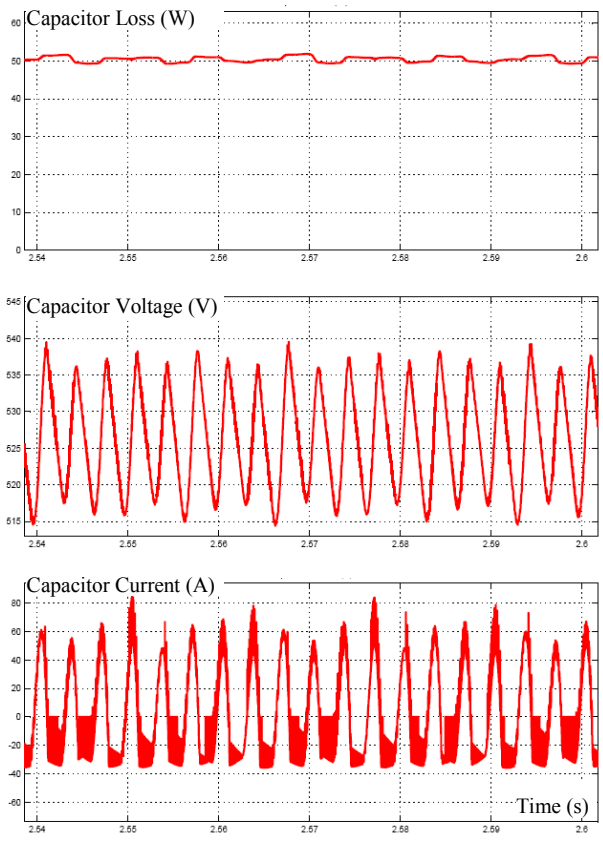


Figure 4-21 Dynamic condition simulation results for designed filter

As seen from the simulation results given in Figure 4-20 and Figure 4-21, during dynamic conditions, DC link voltage decreases to lower values than steady state values (from 522V to 515V). In addition, capacitor power loss increases to higher values than designed value (it will be given in next part) and the capacitor peak current exceeds the rated current value of capacitor (it will be given in next part).

In order to reduce the capacitor power loss and its peak current, DC link should be designed considering dynamic conditions.

In the following parts, first DC link capacitance and inductance values will be calculated for rated power conditions for 7.5kW motor. Then, the requirements for DC link analysis will be explained and their values will be observed in dynamic conditions for different inductance and capacitance values.

4.3.3. Calculation of Capacitance and Inductance Values for 7.5kW Motor

4.3.3.1. Ripple Voltage Determination

In SVPWM, the maximum obtainable fundamental voltage (peak phase value) in linear region without over modulation is $0.5774*V_{DC}$ whereas maximum obtainable fundamental voltage (peak phase value) with over modulation for 0.952 modulation index is $0.606*V_{DC}$. In Turkey, the rated voltage of motors (most of them in this voltage range) for peak phase is 311V (220V RMS). If these numbers are equated, minimum required value for DC link voltage can be found for linear and over modulation regions.

$$0.5774 * V_{DC} = 311 \tag{4.39}$$

$$V_{DC} = \frac{311}{0.5774} = 538.7\ (for\ linear\ region) \tag{4.40}$$

$$0.606 * V_{DC} = 311 \tag{4.41}$$

$$V_{DC} = \frac{311}{0.606} = 513\ (for\ over\ modulation\ region) \tag{4.42}$$

If rectified (with diode rectifier) 3-phase grid voltage is used to obtain DC link voltage, the maximum DC link voltage becomes:

$$V_{DC} = 380 * \sqrt{2} - 2 * V_D \tag{4.43}$$

Where V_D is the diode voltage drop and it is taken as 1V here. For rectification, input voltages pass through two diodes and therefore, voltage drop becomes 2V. The DC link voltage and its components are shown in Figure 4-22.

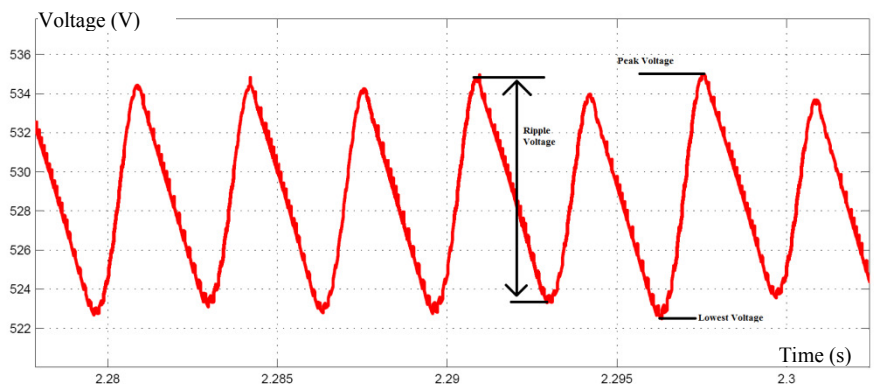


Figure 4-22 Ripple voltage, peak voltage and lowest voltage for DC link

$$V_{DC} = 537.4 - 2 = 535.4\,V \tag{4.44}$$

Based on equations given in (4.42) and (4.44), peak value of DC link voltage that can be obtained from three phase grid is 535V whereas minimum acceptable DC link voltage is 513V. Based on these voltage levels, acceptable ripple voltage for DC link is taken as 20V.

4.3.3.2. Determination of Capacitance Value [30]

To calculate the capacitance value, it is considered that all inverter power is supplied from capacitor. Therefore, the energy drop on capacitor for one cycle (one cycle corresponds to three phase rectifier ripple frequency which is 6 times grid frequency. For Turkey grid frequency is 50Hz and ripple frequency is 300Hz) should be equal to inverter power.

$$\left(\frac{1}{2} * C * (V_i^2 - V_f^{2)}\right) * f_{ripple} = P_{inverter} \tag{4.45}$$

$P_{inverter}$= 7.5kW, then

$$\left(\frac{1}{2} * C * (535^2 - 515^2)\right) * 300 = P_{inverter} \tag{4.46}$$

$$C = \frac{7500 * 2}{21000 * 300}\ F \tag{4.47}$$

$$C = 0.00238\ F = 2.38\ mF \tag{4.48}$$

Since all inverter power will not be supplied from capacitor, it seems that capacitor is oversized. In order to correct the capacitance value, part of the inverter power supplied by capacitor should be calculated. However, this situation is not considered in this thesis.

In producer catalogs, all values for capacitors do not exist. Thus, capacitor value is taken as 2.35mF (series connection of two 4.7mF capacitors).

4.3.3.3. Calculation of Capacitor Ripple Current [30]

The ripple current of capacitor for switching frequency and 300Hz component is shown in Figure 4-23.

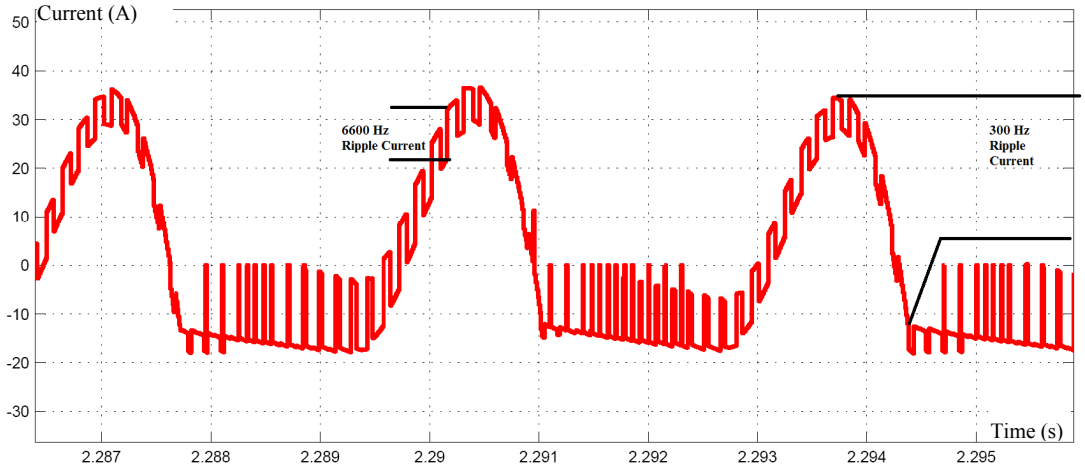


Figure 4-23 Ripple current components of capacitor

The choice of capacitor depends on its ripple current because in reference document of capacitors, acceptable ripple current value is defined and exceeding this value can harm the component. Therefore, the ripple current on capacitor should be calculated and capacitor/capacitor bank should be chosen with respect to ripple current value. The calculations for ripple currents are given below. The charge and discharge times of capacitor is shown in Figure 4-24.

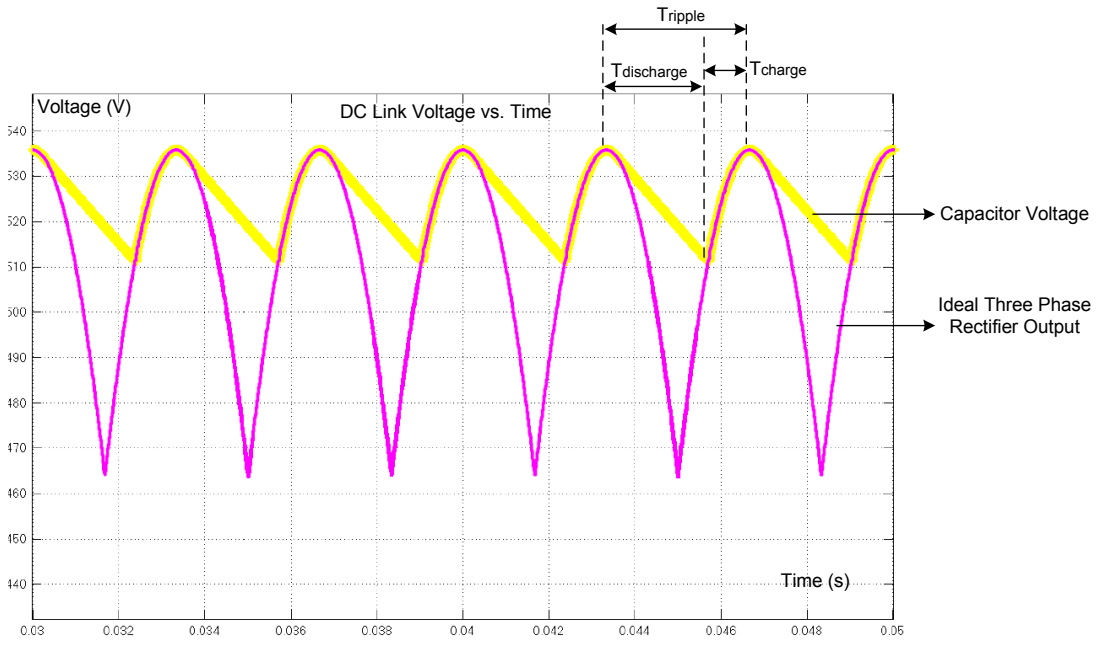


Figure 4-24 Charge and discharging states of capacitor

The charge time of capacitor= T_{charge}

The discharge time of capacitor = $T_{discharge}$

period of DC link ripple = $T_{ripple} = 1/300$ *in Turkey*

Charge current = I_{charge}

Discharge current = $I_{discharge}$

Ripple Current = I_{ripple}

Load Current supplied by capacitor= I_{load}

$$T_{charge} = \frac{arc\,cos(\frac{U_f}{U_i})}{\frac{\pi}{3} * f_{ripple}} = \frac{arc\,cos(\frac{517}{537})}{\frac{\pi}{3} * 300} = 0.87\ ms \tag{4.49}$$

$$T_{discharge} = T_{ripple} - T_{charge} = 3.33 - 0.87 = 2.46\ ms \tag{4.50}$$

$$I_{charge}(peak) = C * \frac{\Delta V}{T_{charge}} \tag{4.51}$$

$$I_{charge}(rms) = \sqrt{I^2_{charge-peak} * T_{charge} * f_{ripple}} \tag{4.52}$$

$$I_{discharge}(peak) = C * \frac{\Delta V}{T_{discharge}} \tag{4.53}$$

$$I_{discharge}(rms) = \sqrt{I^2_{discharge-peak} * T_{discharge} * f_{ripple}} \tag{4.54}$$

$$I_{ripple} = \sqrt{I^2_{charge} + I^2_{discharge}} \tag{4.55}$$

$$I_{load} = \frac{P_{inverter}}{V_{dc\,(average)}} \tag{4.56}$$

Based on equations given above, the current values are calculated for 7.5kW motor and they are given in the upcoming equations.

$$I_{charge} = 54.53\ A\ (peak\ value) \tag{4.57}$$

$$I_{charge} = 27.87\ A\ (rms\ value) \tag{4.58}$$

$$I_{discharge} = 19.3\ A\ (peak\ value) \tag{4.59}$$

$$I_{discharge} = 16.59\ A\ (rms\ value) \tag{4.60}$$

$$I_{ripple} = \sqrt{27.87^2 + 16.59^2} = 32.43\ A\ (rms\ value) \tag{4.61}$$

$$I_{load} = \frac{7500}{\frac{537 + 517}{2}} = 14.23\ A \tag{4.62}$$

The current value that passes through capacitor is 14.23 A at switching frequency (6600 Hz) and 32.43 A at ripple frequency (300 Hz). Based on the ripple current value, the capacitance/capacitance bank should be chosen.

From EPCOS Company, the capacitors with type number B437*4A5478M0 are chosen for the design and its properties are given in Table 4-5.

Table 4-5 Properties of chosen capacitor for 7.5kW motor

Properties	**Values**
Voltage Rating (V)	450
Ripple Current Rating at 100 Hz (A, RMS)	31.8
Maximum Current Rating (A, Peak)	67
ESR at 100 Hz (mΩ)	22
Capacitance Value (µF)	4700

Since the voltage rating of capacitor is 450V, two capacitors should be connected in series in order to obtain voltage rating higher than operated DC link voltage. The capacitance value after series connection becomes 2.35 mF. The ripple current capacity of capacitor bank is 31.8 A (rms) at 100 Hz and it is increasing at higher frequencies based on the chosen capacitor's datasheet. As seen from (4.61), the ripple current rating of capacitor is sufficient for the design.

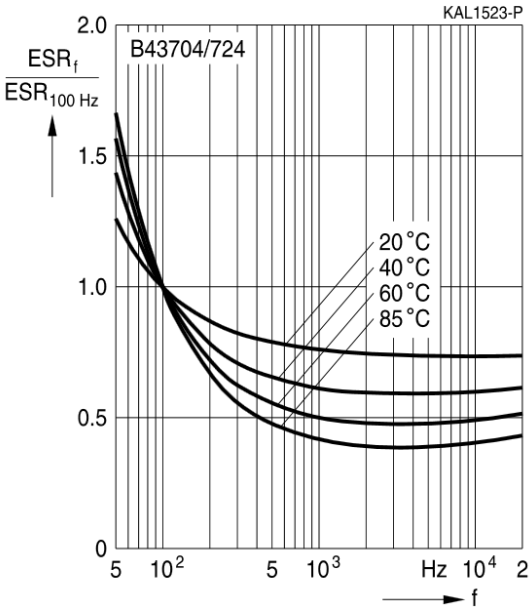


Figure 4-25 ESR values of capacitor with respect to frequency [31]

The change of ESR value with respect to frequency is given in Figure 4-25. Based on this figure and ESR value at 100Hz, ESR value is taken as 17.5 mΩ for each capacitor and after series connection ESR value is set to 35 mΩ in simulation environment.

4.3.3.4. Calculation of Capacitor Power Loss and Inductance Value [30]

After choice of the capacitors, their power loss should be calculated in order to determine whether it causes acceptable temperature rise for capacitor.

For power loss calculation, the ESR values of capacitor bank are needed and it is given in previous part.

In simulation, ESR value is taken as 35mΩ; however, to calculate power loss, it is better to use actual values of ESR for each frequency component. The values for ESR are calculated based on Figure 4-25 and they are given below.

ESR at 300 Hz = 36 mΩ

ESR at 6.6 kHz = 32 mΩ

The current values for power loss calculations are taken from ripple current calculation part.

$$P_{300\,Hz} = 0.036 * 32.43^2 = 37.86\,W \tag{4.63}$$

$$P_{6.6\,kHz} = 0.032 * 14.23^2 = 6.48\,W \tag{4.64}$$

$$P_{total} = 37.86 + 6.5 = 44.34\,W \tag{4.65}$$

The thermal resistance R_{TH} of capacitor bank is taken as 3.73°C/W (this value is taken from [32] and it is determined with respect to its size) and 40°C temperature rise is allowed for operation. Therefore, acceptable power loss of capacitors can be calculated for the temperature rise.

$$P_{cap}(acceptable) = \frac{Temperature\ Rise}{R_{TH}} = \frac{40}{3.73} = 10.73\,W \tag{4.66}$$

From equation 4.66, it is shown that for the chosen capacitor 10.73W of maximum power dissipation is acceptable for each capacitor. Therefore, the chosen capacitors cannot tolerate the existing power loss of 22.17W each. This loss should be decreased to 10.73W. Since switching loss component cannot be changed, the 300Hz component should be reduced.

From equation 4.63, it can be understood that i_{ripple} should be reduced to decrease power loss. From equation 4.51 and 4.53, it can be followed that this is possible only by reducing voltage ripple. Thus, DC link inductor is used to reduce voltage ripple and power loss of capacitor.

The inductance value should be calculated based on voltage drop, V_L on it. First, voltage drop on inductance is calculated and after that inductance value is calculated based on ripple current value.

Since there are two capacitors in DC link, the power dissipation for capacitor bank should be limited at 21.46W. Thus, 22.88W (44.34W-21.46W) is the power loss that should be reduced and 300Hz power loss component of capacitor is 37.86W. In order to reduce power loss of capacitor, the excess part of the ripple voltage should be dropped on the inductor. The inductance voltage drop equation is given in (4.67).

$$V_L = 20 * \frac{22.88}{37.86} = 12\,V\ (peak - peak) \tag{4.67}$$

In [30], the rms value of ripple voltage is calculated by dividing peak-peak value of ripple voltage by 2.11. For voltage drop on V_L given in (4.67), the rms value becomes as:

$$V_L = \frac{12}{2.11} = 5.68\,V(rms) \tag{4.68}$$

Since DC link voltage is reduced to (20-12) V, the ripple current value is also reduced. The new ripple current value at 300 Hz can be calculated using power loss on capacitor.

$$P_{loss} = ESR_{300\,Hz} * I_{rms}^2 \tag{4.69}$$

$$I_{rms} = \sqrt{\frac{P_{loss}}{ESR_{300\,Hz}}} = \sqrt{\frac{21.46}{0.035}} = 24.76\,A \tag{4.70}$$

Based on ripple current rms and voltage drop on inductor, the inductance value can be calculated using (4.71) and (4.72).

$$X_L = \frac{V_{L\,rms}}{I_{rms}} = \frac{5.68}{24.76} = 0.23 \tag{4.71}$$

$$\boldsymbol{L} = \frac{X_L}{2 * \pi * 300} = \frac{0.23}{2 * \pi * 300} = \mathbf{122}\ \mu\boldsymbol{H} \tag{4.72}$$

After determination of capacitor and inductor for DC link, their values should be evaluated based on resonant frequency criterion. This criterion is that the resonant frequency of DC link should be lower than ripple frequency in order to avoid amplification at ripple frequency [30].

$$\boldsymbol{f_{resonant}} = \frac{1}{2 * \pi * \sqrt{L * C}} = \frac{1}{2 * \pi * \sqrt{2.35 * 10^{-3} * 122 * 10^{-6}}} = \mathbf{297}\ \boldsymbol{Hz} \tag{4.73}$$

Since resonant frequency is very close to ripple frequency, capacitor or inductance value should be increased. Since the capacitor is chosen, the inductor value can be increased to obtain resonant frequency lower than ripple frequency. For the resonant frequency, 250Hz is chosen because capacitances have tolerances and they can be lower than its actual value.

$$\boldsymbol{L} = \frac{1}{f_{resonant}^2 * 4 * \pi^2 * C} = \frac{1}{250^2 * 4 * \pi^2 * 2.35 * 10^{-3}} = \mathbf{172.5}\ \mu\boldsymbol{H} \tag{4.74}$$

For inductor design, design parameters given in [38] are used. Based on the design procedure, area product, wire size, number of turns and air gap, resistance part of inductance is found. The details of equations are given in [38] and calculated parameters are given Table 4-6.

Table 4-6 Properties of designed inductor for 7.5kW motor

Properties	**Values**
Ripple Current Rating (A, RMS)	25.6
Resistance part (mΩ)	1
Inductance Value (μH)	172.5

After calculating the steady state values for inductor and capacitor, the requirements for DC link design will be analyzed in the following parts.

4.3.4. Analysis of DC Link Design for Dynamic Conditions

As given in previous part, in dynamic conditions, capacitor power loss and capacitor peak current exceed its rated value. In order to decrease peak current and power loss of capacitor, DC link should be analyzed and designed for dynamic conditions.

For the analysis, the requirements and variables are defined as given below. The requirement values with respect to variables are observed

- Requirements for Input (Grid) Side
  - Good power factor
  - Low harmonic current (low THD)
- Requirements for Output Side
  - DC voltage dip (lowest) level
  - Capacitor power loss
  - Capacitor peak current
- Variables
  - DC link inductor (L_{DC})
  - DC link capacitor (C_{DC})

- Load torque of motor (~acceleration time)
- Acceleration torque (it is taken as two times of rated torque in this work)

In order to investigate the problem, a simplified model has been developed. Although the problem can be analyzed with the detailed Matlab model, the simplified model has been utilized for the fast and easy observation of the parameters. The details of the model are given in the following part.

4.3.4.1. Development of Simplified Model

Model for Analytical Solution

Initially, the model given in Figure 4-26 is developed to obtain an analytical equation for DC link voltage in terms of rectifier output voltage, DC link inductor, capacitor and inverter current. In this model, source voltage is the output of diode rectifier and load current is DC current sink.

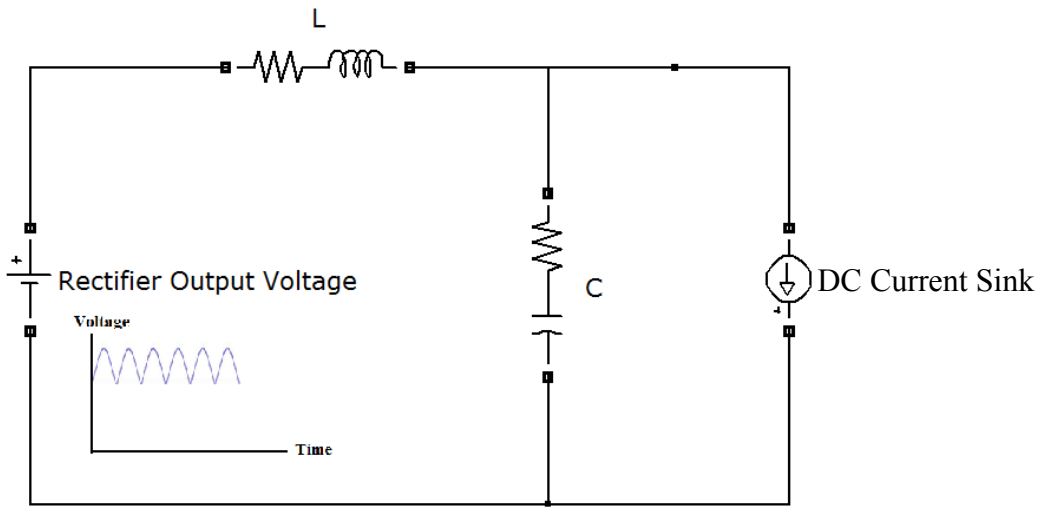


Figure 4-26 Initial model for DC link analysis

However, the analytical solution could not be obtained for this model. Therefore, a simulation environment is created for DC link analysis and the diode rectier is placed instead of voltage source in the simulation.

Model with Three Phase Diode Rectifier

The simplified model used for analysis is given in Figure 4-27. The components of model are explained in the following parts.

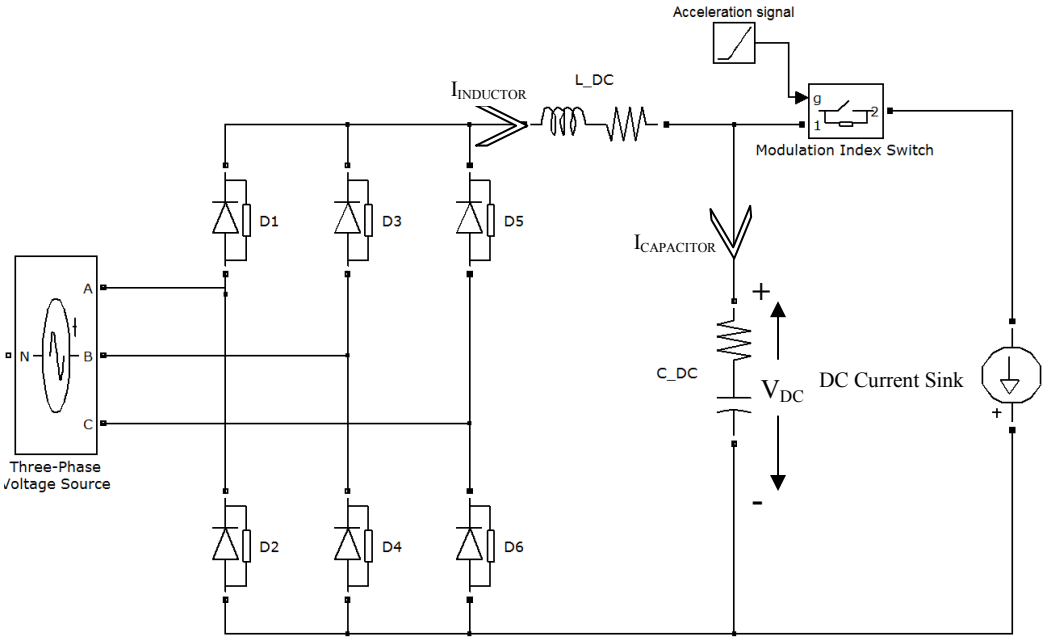


Figure 4-27 Simulation environment for DC link analysis

At the input side, 3-phase AC source is used. Its voltage and frequency values are set to 380V (l-l, rms) and 50Hz, respectively. The set values of voltage and frequency are 3-phase grid voltage and frequency levels in Turkey. Three phase diode rectifier is used to obtain DC link voltage. The DC link inductor and capacitor is placed based on calculated values in previous parts.

In the simplified model, there are two components that should be explained and they are given as:

- Modulation Index Switch
- DC Current Sink

Modulation Index Switch to Represent Motor Speed

In vector controlled drive, motor line currents are constant for constant torque operation. Since the magnitudes of line currents are constant, the output power depends on the magnitude of line-line voltages. The relation between voltage and speed can be easily understood considering acceleration condition. During acceleration period, motor line currents and motor torque are constant. Since torque value is constant during acceleration, the output power of motor increases as the speed increases based on equation (4.75). The input motor power is also increasing while output power increases and it can be calculated using line-line voltages and line currents as in equation (4.76). The phase angle between voltage and current is constant because d (related with reactive power) and q (related with active power) axes current values are constant for constant torque operation. Since the line currents are also constant in equation (4.76), only line-line voltage term remains to determine input motor power.

$$P_{out} = T * w \tag{4.75}$$

$$P_{in} = \sqrt{3} * V_{l-l} * I_{line} * cos\varphi \tag{4.76}$$

Assuming constant efficiency for the operation, the output power and input power can be linearly related with each other as in equation (4.77). The constant terms for input power and output power can be written as in equations (4.78) and (4.79). Finally, the equation in (4.81) is obtained between speed and line-line voltage. In this equation, both K_1 and K_2 are constant for constant torque operation. Thus, the line-line voltages are linearly changing with motor speed. The vector control algorithm looks like a scalar control as seen in equation (4.81).

$$P_{in} * \eta = \sqrt{3} * V_{l-l} * I_{line} * cos\varphi * \eta = T * w = P_{out} \quad (4.77)$$

$$K_1 = \sqrt{3} * I_{line} * cos\varphi * \eta \quad (4.78)$$

$$K_2 = T \quad (4.79)$$

$$V_{l-l} * K_1 = K_2 * w \quad (4.80)$$

$$V_{l-l} = \frac{K_2}{K_1} * w \quad (4.81)$$

In the simplified model, an ideal switch is used. By turning on and off this switch with respect to speed value, the duty cycle is controlled as in equation (4.81).

Since the rated value of line-line voltage is defined as $V_{DC}/\sqrt{2}$, the modulation index should be defined with respect to this value. By this way, rated output voltage will be obtained when modulation index is equal to 1 as in detailed Matlab model.

$$m = \frac{V_{l-l}}{\frac{E}{\sqrt{2}}} \quad (4.82)$$

The ideal switch that represents modulation index is controlled with respect to speed level. In other words, it is assumed that in order to keep flux constant phase voltage is proportionally increased with speed. The on and off times of the switch determine the average value of voltage transferred to load side.

To obtain the voltage across the DC current sink rising in proportion with speed; the gate signals of the modulation switch can be obtained by comparing the speed ramp signal with a triangular waveform at switches shown in Figure 4-28.

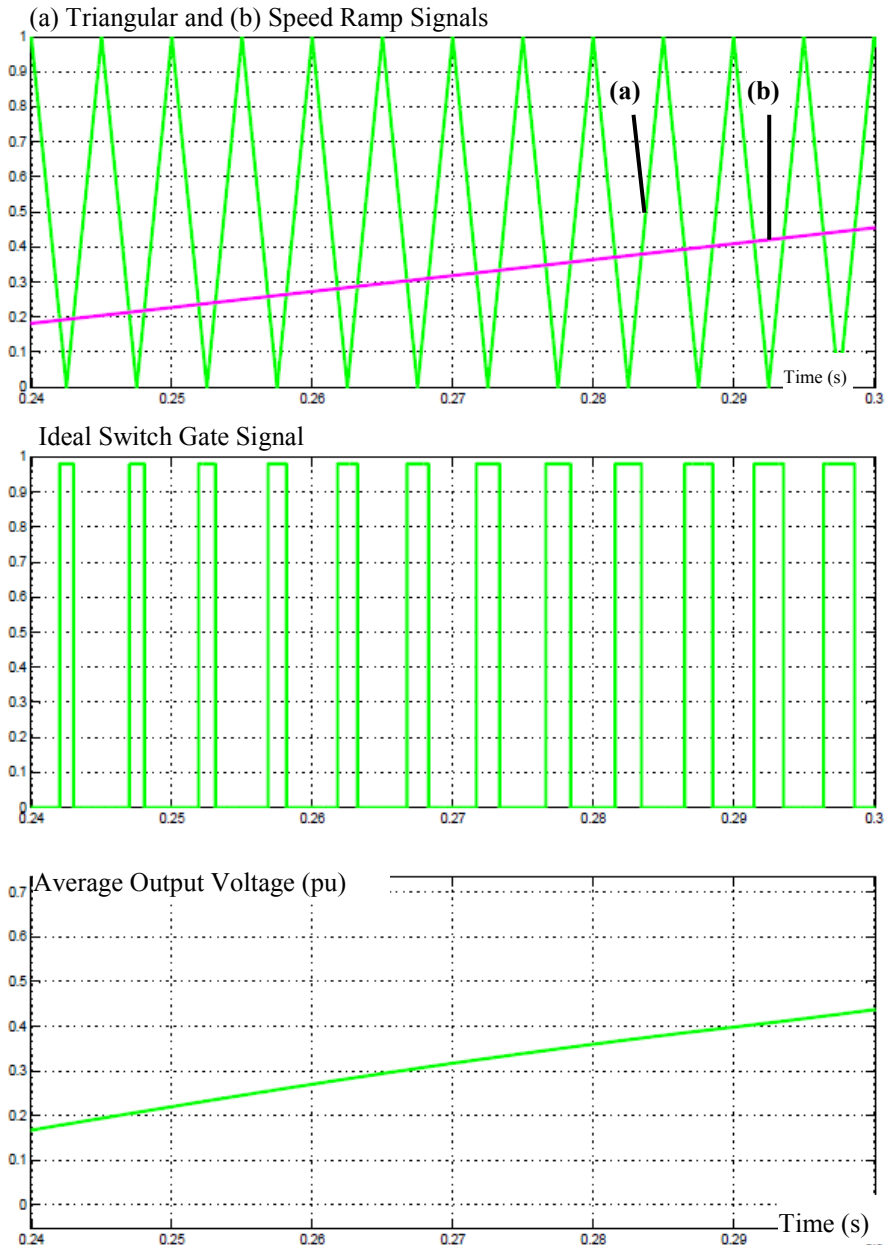


Figure 4-28 PWM generation signals and average output voltage

In Figure 4-28, the ramp signal represents the acceleration of motor and its value is given as per unit value. The triangular waveform is the comparison signal to generate gate pulses for ideal switch with respect to the speed value also has unity magnitude. As seen from Figure 4-28, the gate signal becomes high when ramp signal is higher than triangular signal, otherwise it becomes low. The ideal switch is turned on, when

the gate signal is high and it is turned off when the gate signal is low. In Figure 4-28, the average output voltage is shown as per unit value and its value is rising as the speed rises.

Inverter Model as a Current Sink

After DC link, an ideal switch and DC current sink are placed to represent inverter and motor. They are shown in Figure 4-29.

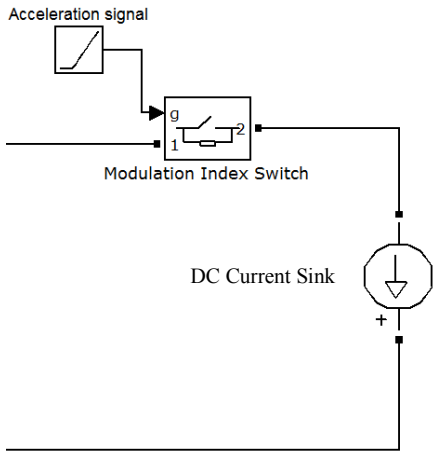


Figure 4-29 Current sink and ideal switch for inverter model

The inverter is modeled as DC current sink because the electromagnetic torque and therefore, d and q axes currents are constant.

The magnitude of DC current sink is determined with respect to applied torque value. Although the inverter current has pulsating waveform as shown in Figure 4-37, it can be averaged over ripple period (300Hz) since its period is much higher than the switching period of the inverter switches. The DC current sink and torque values can be related with the following equations.

The torque equation for field oriented control becomes as:

$$T_E = \frac{3}{2} * \frac{p}{2} * \lambda_{ds} * i_{qs} = \frac{3}{2} * \frac{p}{2} * \frac{L_m^2}{L_r} * i_{ds} * i_{qs} \quad (4.83)$$

In our driver, the aim is to obtain constant torque at the motor shaft. Since torque value is constant, both d and q axes currents and line currents are also kept constant. The magnitude of line current with respect to d and q axes current can be given as:

$$I_{line}(peak\ value) = \sqrt{I_{ds}^2 + I_{qs}^2} \quad (4.84)$$

After relating the applied torque with line current, the relation between line current and DC current sink can be derived. By this way, the inverter could be placed as current sink in the model.

In [33] and [39], it is stated that DC current sink (average input current of inverter) could be calculated using line current, modulation index and phase shift angle. The phase shift angle is defined as the angle between the fundamental phase voltage and phase current. The equation for DC current is given in (4.85).

$$I_{inverter}(DC) = \frac{3}{4} * I_{line(peak)} * m * \cos(\varphi) \quad (4.85)$$

$I_{inverter}(DC) = Average\ (DC)\ current\ of\ inverter$

$I_{line(peak)} = Magnitude\ of\ line\ current$

$m = Modulation\ index\ of\ inverter$

$\cos(\varphi) = Phase\ shift\ angle\ between\ fundamental\ voltage\ and\ current$

For our condition, the applied torque is constant; therefore, i_d and i_q currents are also constant. Since d axes current is related with reactive power and q axes current is related with active power, it can be assumed that phase shift angle of inverter for constant torque operation is constant. As explained before, line current is also

constant for constant torque operation. Hence, only modulation index term remains as a changing variable in the DC current sink equation. By representing modulation index as a switch, the equation in (4.86) is obtained for inverter model. For equation (4.86), the power factor of motor (value in the nameplate) is taken as phase shift angle value since the results are calculated for rated motor torque.

$$I_{current\ sink}(DC) = \frac{3}{4} * I_{line(peak)} * \cos(\varphi) \tag{4.86}$$

Values of Current Sink in the Simulation

During acceleration period, the torque reference is set to obtain twice the rated torque at the motor shaft. For this reason, the reference q axes current is increased to twice of rated q axes current. In this condition, the line current becomes:

$$I_{line}(rated\ torque\ operation) = \sqrt{I_{ds}^2 + I_{qs}^2} \tag{4.87}$$

$$I_{line}(2 * rated\ torque\ operation) = \sqrt{I_{ds}^2 + (2 * I_{qs})^2} \tag{4.88}$$

The simplified model is used for analysis of 7.5kW motor. The current sink value in simulation for rated power condition is adjusted with respect to rated line current of motor. For dynamic conditions, its value is set twice of rated power condition. Since the rated line current of motor is 15A and power factor is 0.88 (value on nameplate), DC current sink becomes 14A based on equation (4.86).

Table 4-7 DC Current sink values for operating conditions

	Current Sink Value (A)
Steady state condition	14
Dynamic Condition	28

4.3.4.2. Verification of Simplified Model

In the previous part, simplified model is explained and the inductance and capacitance values are calculated for 7.5kW motor. In order to make DC link analysis for this motor, first the simplified model should be verified. After that, the simplified model will be used for DC link analysis of 7.5kW motor.

In the experimental setup, 1kW motor is used. Its parameters are given in Table 4-8. The simplified model given in the previous section will be verified experimentally using this motor. Therefore, the capacitance and inductance values are calculated for 1kW motor and they are given in Table 4-9. Same capacitance and inductance values (with their equivalent series resistance values) are used for simplified model, detailed Matlab model and experimental setup.

Table 4-8 Parameters of 1kW motor used for verification purpose

Parameter	**Value**
Rated Power (kW)	1
Rated Speed (rpm)	2820
Rated Line Current (A-rms)	2.7
Rated Motor Voltage (V-l_l)	380
cosϴ	0.76
Connection Type	Y Connected

Table 4-9 Parameter of DC Link designed for 1kW motor

Parameter	Value
L_{DC} (μH) & ESR (mΩ)	1mH & 360mΩ
C_{DC} (mF) & ESR (mΩ)	0.37mF & 150mΩ

The parameters used in simplified model are given in Table 4-10.

Table 4-10 Parameters in simplified model for 1kW motor

Parameter	Value
Switching Frequency (Hz)	6600
Switching Duty Cycle (%)	99
L_{DC} (μH) & ESR (mΩ)	1mH&360mΩ
C_{DC} (mF) & ESR (mΩ)	370μ&150mΩ
Load Current (A)	1.96

The switching duty cycle is set to 99% in order to see switching effect on capacitor voltage.

In order to verify simplified model, the results at rated power condition are obtained for the simulations and experimental test. The results are given in Table 4-11.

Table 4-11 Steady state results for simulation and experimental results

Parameter	**Simplified Model**	**Detailed Matlab Model**	**Experimental Results**
Inductor Peak Current (A)	6,9	6,8	6,15
DC Link Voltage Dip (V)	523,2	523	521
DC Link Voltage Ripple (V)	10,3	10,8	10
Capacitor Peak Current (A)	6,9	7	6,5
Capacitor Power Loss (W)	1,45	1,65	-
Inverter Average Current (A)	1,95	1,98	-

As seen from Table 4-11, voltage and current values are similar for the simulations and experimental setup. However, the DC link lowest voltage is a little lower in experimental setup. The difference is due to voltage variations on AC grid voltages or non-linearity's of DC link components.

DC link voltage waveforms for the simplified model, the detailed Matlab model and experimental setup are given in Figure 4-30, Figure 4-31, and Figure 4-32. The detailed explanations about the detailed Matlab model are given in chapter-3.

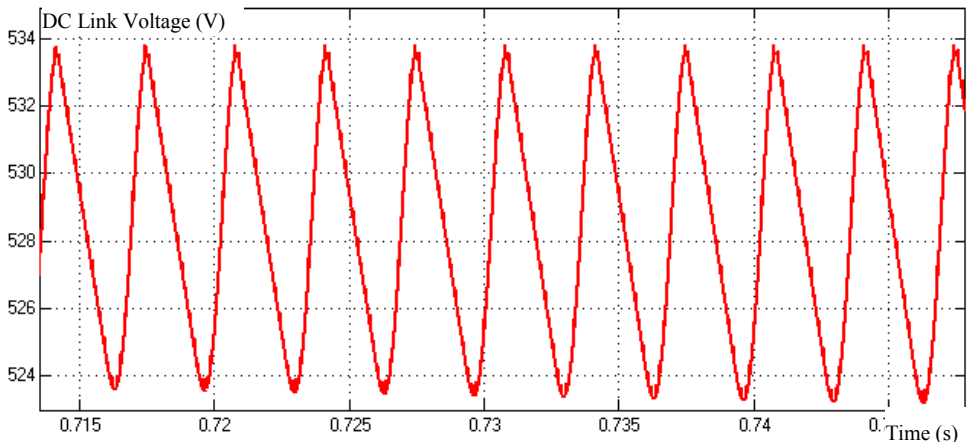


Figure 4-30 DC link voltage for rated power condition (simplified model)

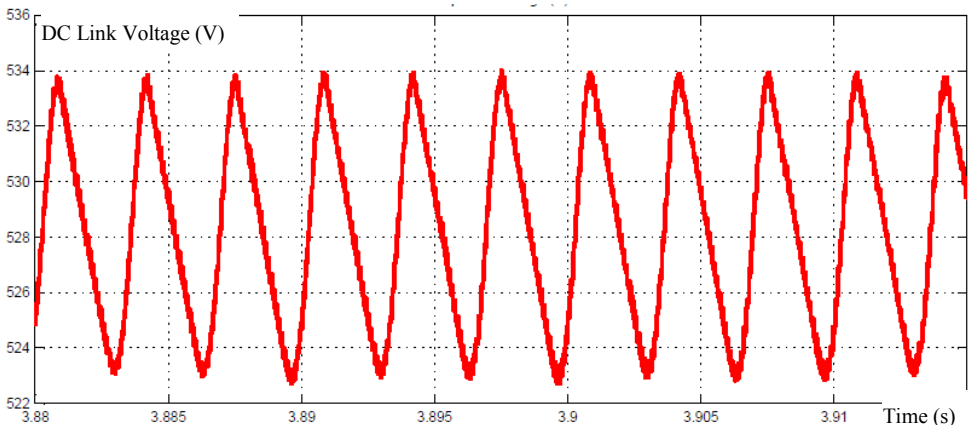


Figure 4-31 DC link voltage for rated power condition (detailed Matlab model)

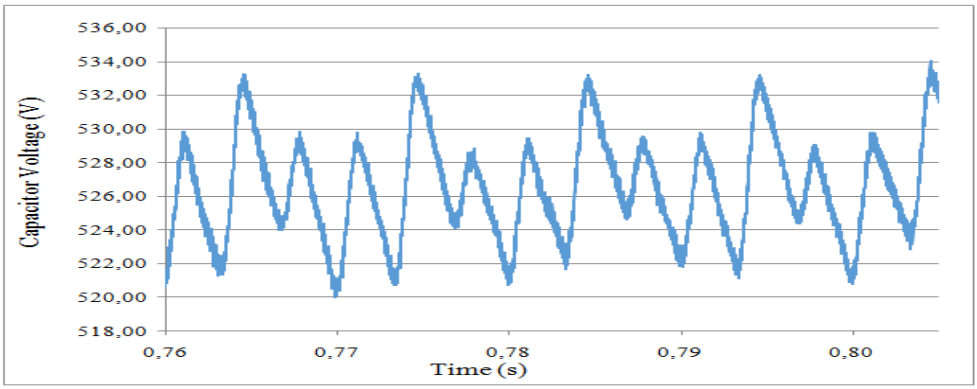


Figure 4-32 DC link voltage for rated power condition (experimental setup)

As seen from Figure 4-30, Figure 4-31 and Figure 4-32, DC link voltage waveforms for simulations and experimental setup are similar to each other. The variation in experimental setup is caused by phase voltage differences of three phase grid. However, the ripple voltage value of experimental setup is close to simulation values.

The inductor current waveforms for simplified model, simulation results and experimental setup are given in Figure 4-33, Figure 4-34, and Figure 4-35.

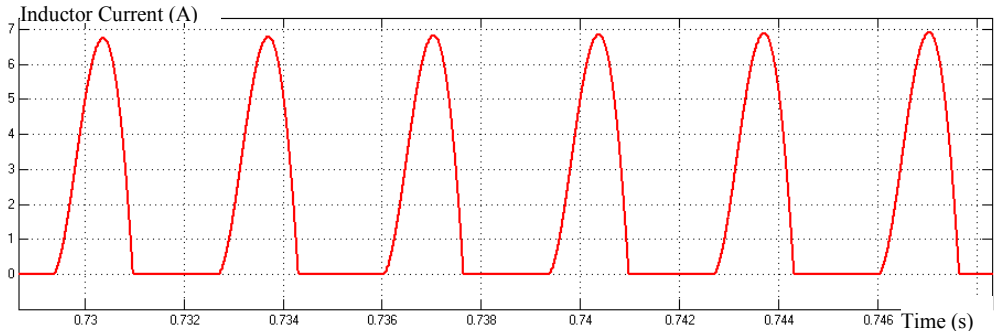


Figure 4-33 Inductor current for rated power condition (simplified model)

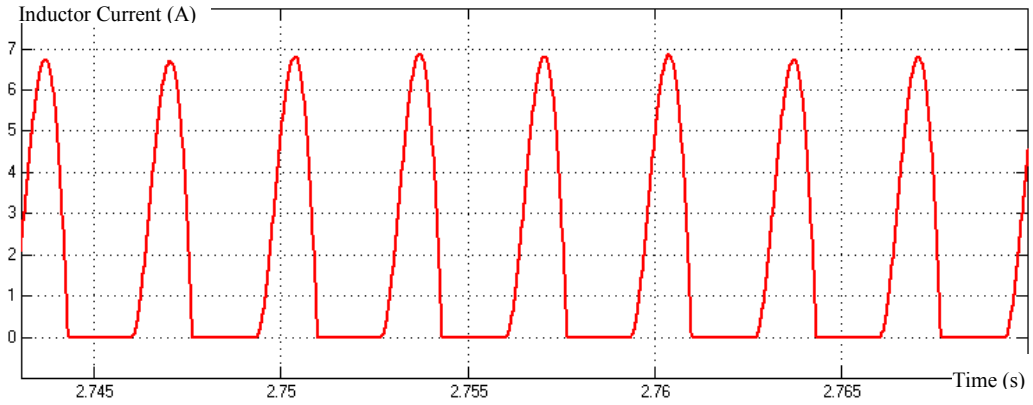


Figure 4-34 Inductor current for rated power condition (the detailed Matlab model-5ms/division)

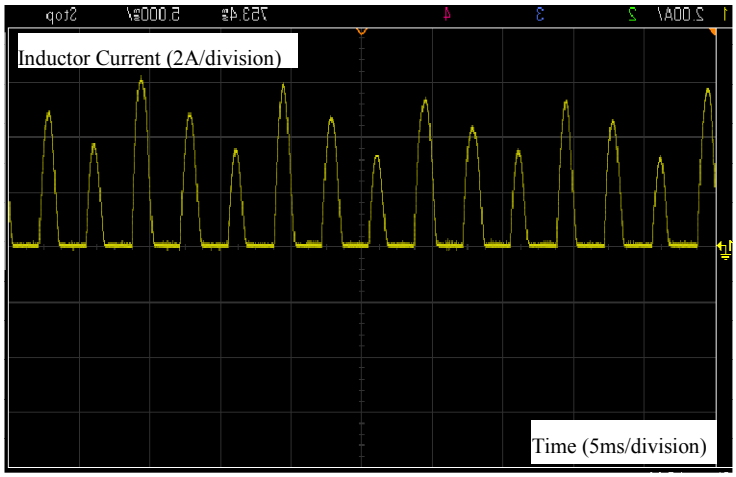


Figure 4-35 Inductor current for rated power condition (experimental setup)

As seen from Figure 4-33, Figure 4-34 and Figure 4-35, the inductor currents for simulations and experimental setup are similar to each other. The variation in experimental setup is caused by again voltage variations of three phase grid. From these results, it can be understood that in order to obtain the same or very similar results in simulation and experimental setup, a controlled AC source should be used for experiments. Since it is not applicable for our case, the variations of voltage and current waveform will be taken as experimental error.

The capacitor current waveforms for simplified model, simulation results and experimental setup are given in Figure 4-36, Figure 4-37, and Figure 4-38.

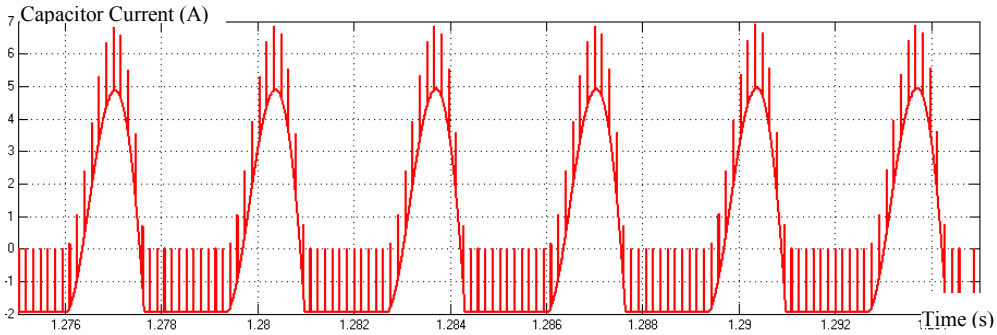


Figure 4-36 Capacitor current for rated power condition (simplified model)

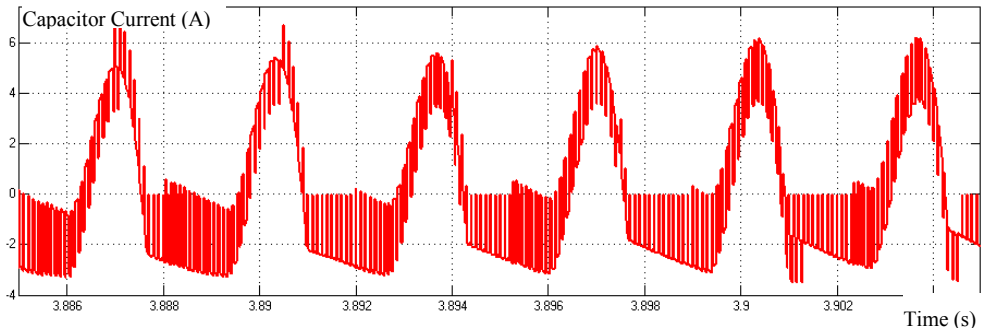


Figure 4-37 Capacitor current for rated power condition (the detailed Matlab model-2ms/division)

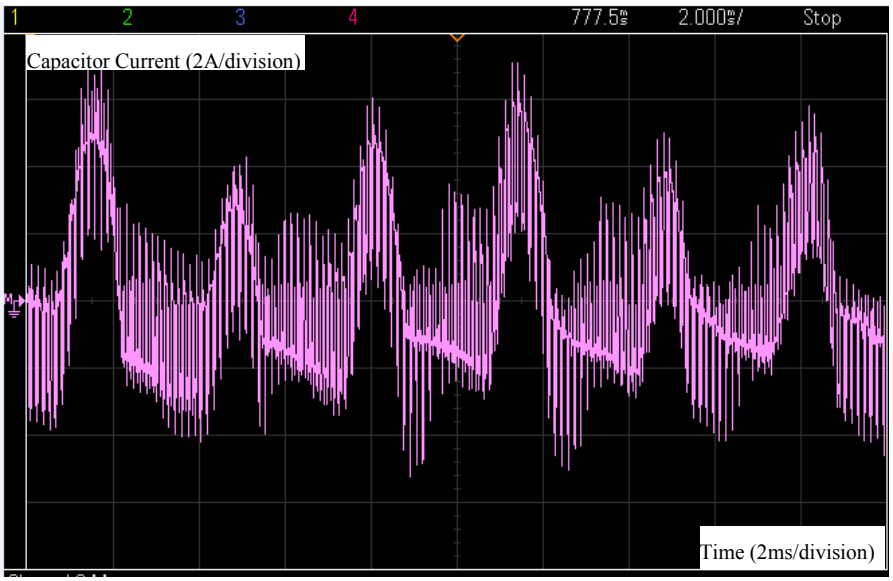


Figure 4-38 Capacitor current for rated power condition (experimental setup)

The inverter current waveforms for simplified model, simulation results and experimental setup are given in Figure 4-39, Figure 4-40, and Figure 4-41.

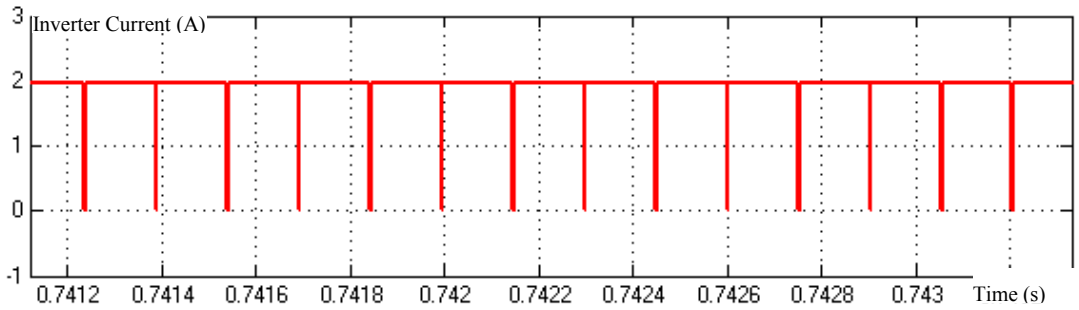


Figure 4-39 Inverter current for rated power condition (simplified model)

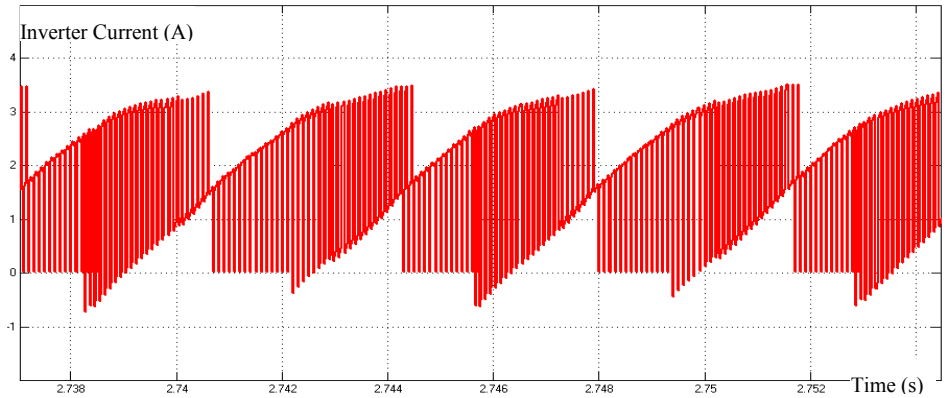


Figure 4-40 Inverter current for rated power condition (the detailed Matlab model-2ms/division)

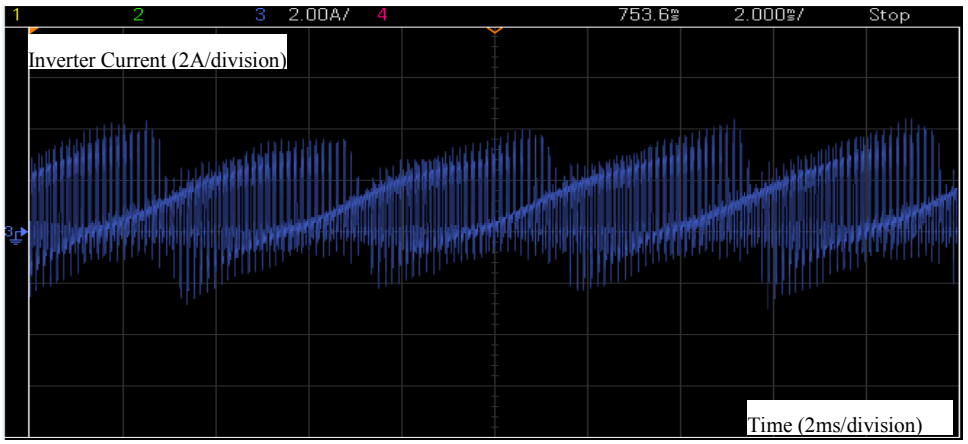


Figure 4-41 Inverter current for rated power condition (experimental setup)

The average inverter currents for simplified model and the detailed Matlab model are given in Figure 4-42, Figure 4-43, and Figure 4-44.

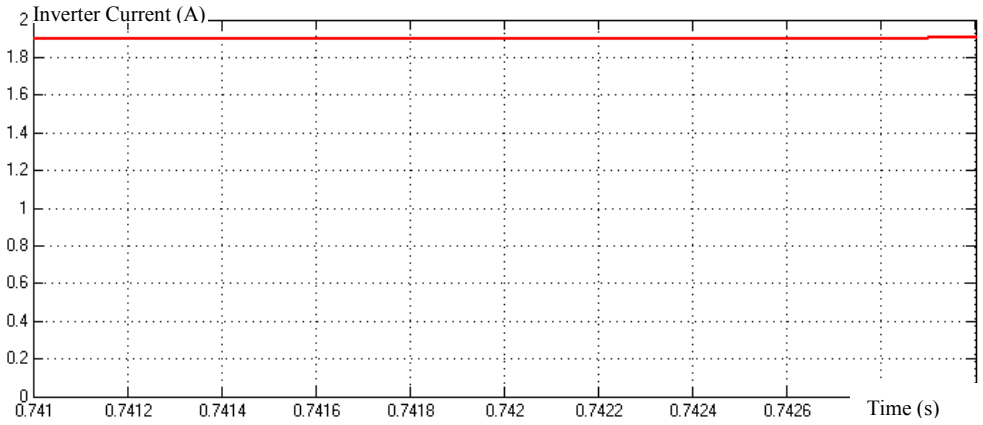


Figure 4-42 Inverter average current for rated power condition (simplified model)

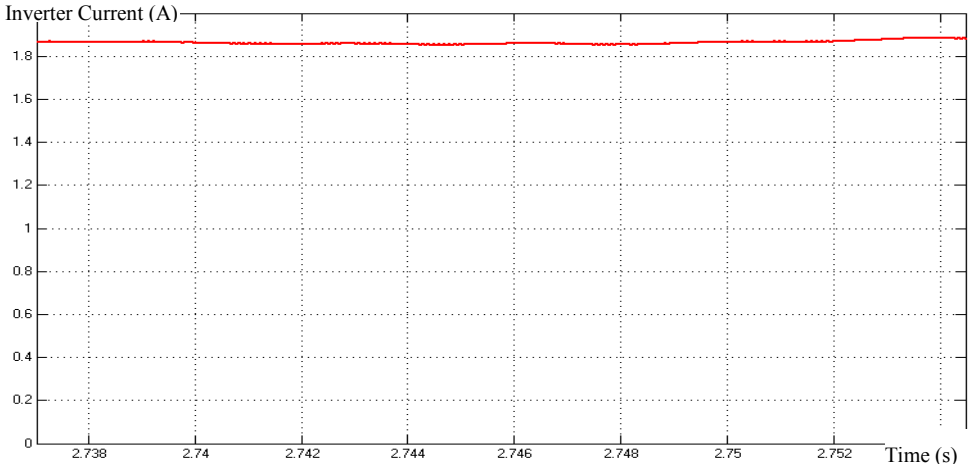


Figure 4-43 Inverter average current for rated power condition (the detailed Matlab model)

As seen from Figure 4-39, Figure 4-40 and Figure 4-41, the inverter current waveforms for the detailed Matlab model and experimental setup are similar to each other whereas the simplified model current waveform is different. The current in driver simulation and experimental setup has different amplitude at switching

frequency over 300Hz-envelope. However, the current waveform in simplified model has constant amplitude at switching frequency. As stated before, the model is based on the average current of inverter. The average inverter current for simplified model and the detailed Matlab model are given in Figure 4-42 and Figure 4-43. As seen from these figures, the average inverter currents are very close for the simplified model and the detailed Matlab model.

In order to see the effects of voltage variation or voltage difference of three phase grid, in simulation environment, phase-A voltage is increased 1.5V with respect to other phases. The voltage and current waveforms for this condition is given in Figure 4-44, Figure 4-45, and Figure 4-46.

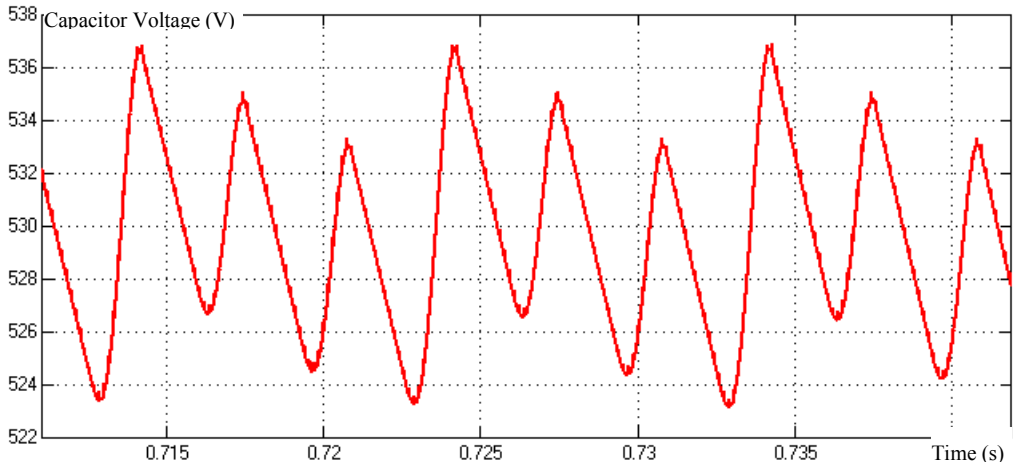


Figure 4-44 DC link voltage for rated power condition (simplified model) with 1.5V increase in phase-A voltage

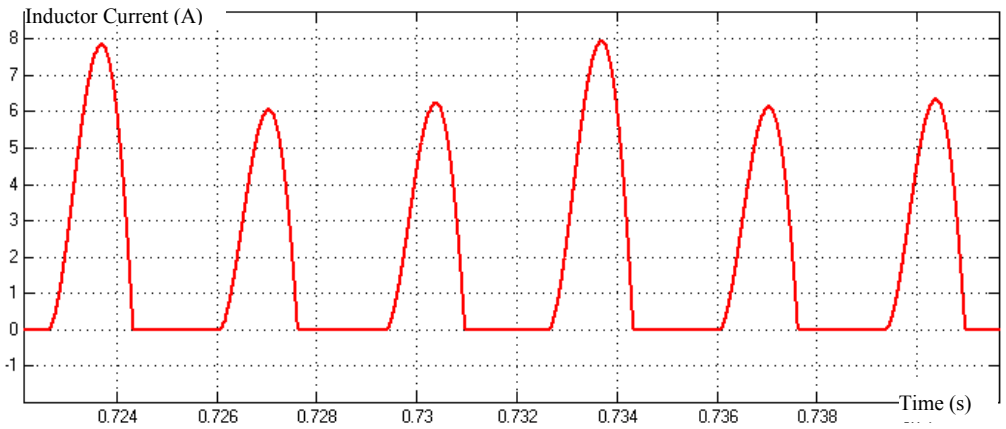


Figure 4-45 Inductor current for rated power condition (simplified model) with 1.5V increase in phase-A voltage

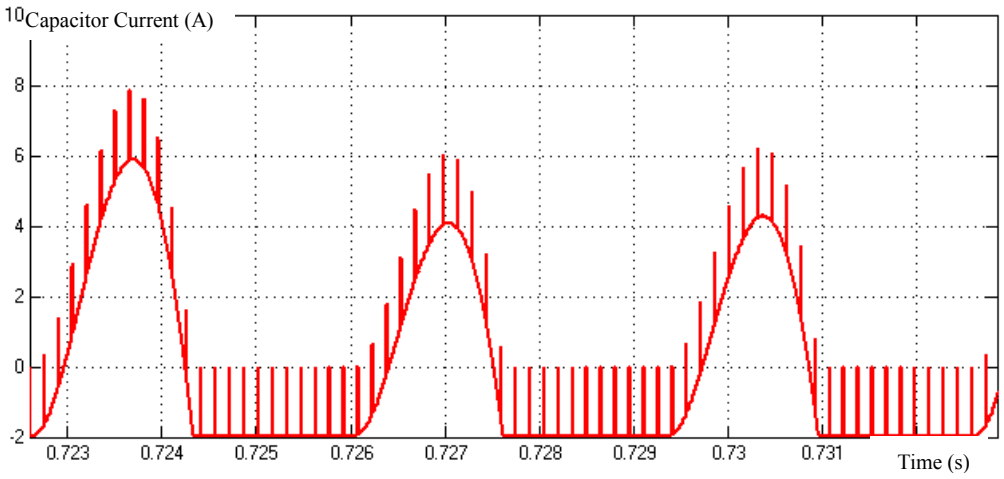


Figure 4-46 Capacitor current for rated power condition (simplified model) with 1.5V increase in phase-A voltage

Based on the results obtained from simulations and experiments, it can be stated that the voltage and current waveforms and their values are similar to each other. The difference in experimental setup is caused by voltage variations or voltage difference between phase voltages of three phase grid. By disregarding the grid side voltage differences, it can be said that the simplified model represents the experimental setup

and the detailed Matlab model. Hence, DC link analysis of 7.5kW motor can be done with simplified model.

4.3.4.3. DC Link Design for 7.5 kW Motor in Dynamic Conditions

For the DC link analysis in dynamic conditions, the requirement values for different capacitor and inductor values are obtained. The capacitance and inductance values used for analysis are shown in Table 4-12.

Table 4-12 Capacitor and inductor values for DC link analysis

		L (μH)					
		0	**57,5**	**115**	**172,5**	**258,75**	**345**
C (mF)	**0,5875**	Requirement Value					
	1,175						
	2,372						
	2,9375						
	3,525						
	4,7						

In Table 4-12, the capacitance and inductance values used for analysis are shown. For each combination of capacitance and inductance values, the requirement value is obtained with simplified model. The explanations and simulation results for the requirements are given in the following parts. In the given figures, the red color shows the desired regions for the requirements.

4.3.4.3.1. Power Factor at Grid Side

Power factor is defined as the ratio of real power (P) to apparent power (S). In [34], it is stated that in apparent power components, active power is doing work whereas reactive power is absorbing system capacity and increases losses. In order to increase the used capacity of electricity system, reactive power component should be reduced.

In our hardware, three phase diode rectifier is used to rectify 3-phase AC source. After that, DC link inductor and capacitor are placed. Since diode rectifier is uncontrolled, there is no active mechanism to increase power factor of grid side. In addition, because of diode rectifier, the grid side currents are discontinuous and their harmonic content is high. As the harmonic content of current increases, power factor decreases because real power is obtained at fundamental frequency of current waveforms whereas harmonic content of current increases reactive power. A sample current shape for grid side is given in Figure 4-47.

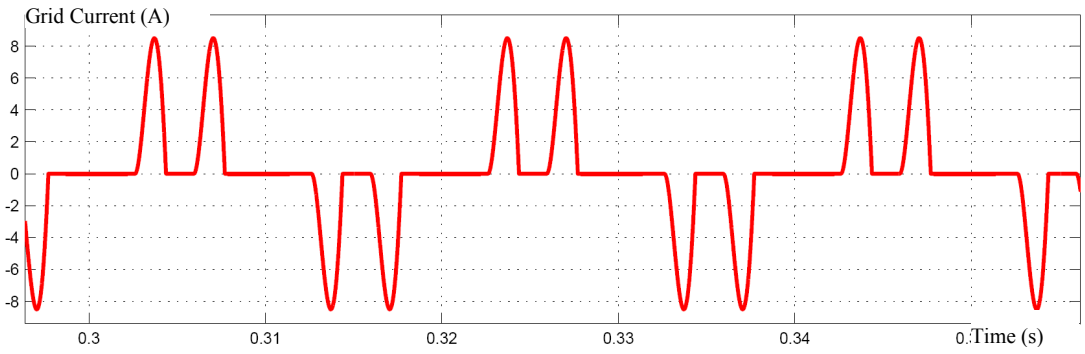


Figure 4-47 Grid current waveform for motor driver applications

Since the grid currents are discontinuous and its shape is not sinusoidal, it is not possible to calculate power factor using phase difference between voltage and current waveforms. Thus, power factor is calculated using active power and apparent power of grid side. The simulink blocks are used to obtain active power from current and voltage waveforms. This block finds out phase angle using the fundamentals of current and voltage waveforms. After that, the active power (P) is calculated by using voltage, current and phase angle. The other block, named as rms block, of simulink is used to obtain rms value of v and i multiplication in grid side, which gives apparent power (S). The relation for power factor calculation is given in equation (4.89).

$$power\ factor = pf = \frac{Active\ Power}{Apparent\ Power} = \frac{P}{S} \tag{4.89}$$

The simulation results of power factor values for changing inductor and capacitor values is given in Figure 4-48.

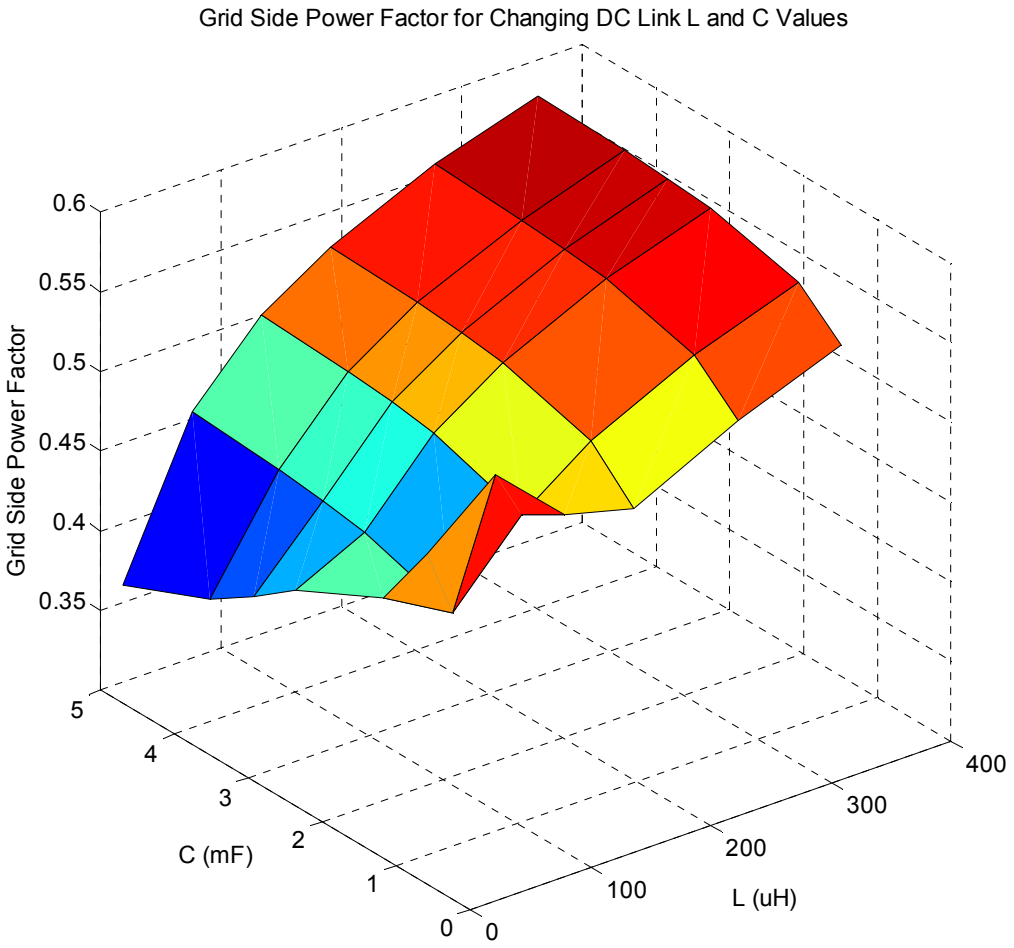


Figure 4-48 Power factor for changing values of L and C

In Figure 4-48, the red color shows the higher power factor points whereas blue color shows the lower power factor points. As seen from Figure 4-48, power factor is increasing as the inductance value increases for the same capacitance value. Power factor is maximized when the inductance and capacitance value increases to twice of

the designed value. In addition, power factor is high when there is no inductance and ¼ of designed capacitance at DC link.

Based on these results, it can be concluded that the capacitance and inductance values should be doubled to obtain highest power factor at grid side if the most important requirement for an application is to increase power factor. However, for motor driver application, DC link voltage and capacitor power loss are the most critical requirements. Therefore, these criteria should be satisfied first in dynamic conditions. After that, the capacitance and inductance values will be determined considering size and cost of DC link components while optimizing power factor value.

4.3.4.3.2. Total Harmonic Distortion at Grid Side Current

Total harmonic distortion is an important measure for quality of current or voltage waveform. There are two methods in the literature to calculate total harmonic distortion of waveforms in general. One of them compares harmonic components to fundamental whereas other compares the harmonic components to rms value of the waveform [4-18]. For the simulations, Matlab/Simulink is used and it calculates total harmonic distortion based on fundamental value as given in (4.90).

$$(based\ on\ fundamental\ value)\ THD_F = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{4.90}$$

$$(based\ on\ rms\ value)\ THD_R = \sqrt{\frac{\sum_{n=2}^{\infty} I_n^2}{\sum_{n=1}^{\infty} I_n^2}} \tag{4.91}$$

If desired, THD calculation can be converted to rms based case. In this case, THD is obtained with respect to rms value of waveform. The transformation taken from [35] is given in equation (4.92).

$$THD_R = \frac{THD_F}{\sqrt{1 + THD_F^2}} \tag{4.92}$$

The relation between THD waveforms are given in Figure 4-49.

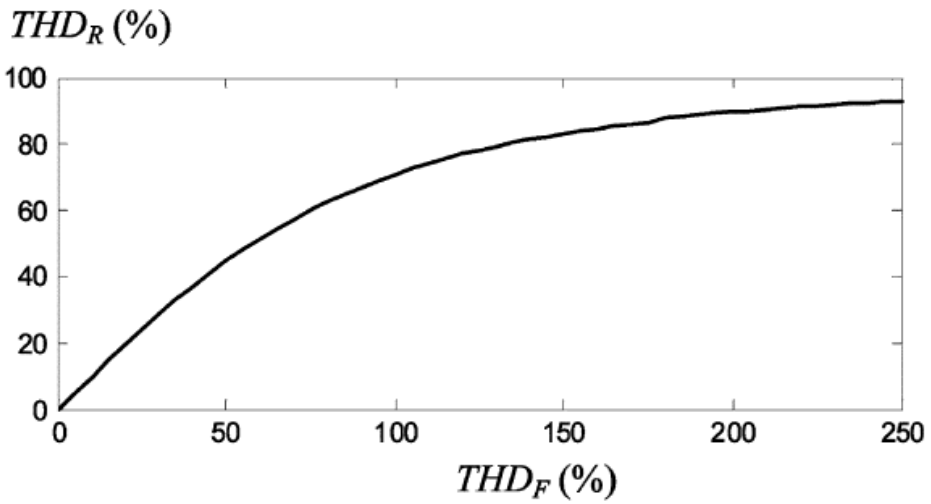


Figure 4-49 Comparison of THD values [35]

As in power factor case, there is no active mechanism to decrease harmonic content of current waveform at grid side. However, DC link inductor and capacitor can be adjusted to obtain lower THD in grid current waveform. Obtaining lower THD in grid current is same as power factor concern and it decreases the losses and increases the used capacity of system.

In order to see the effects of inductance and capacitance values on grid side THD, grid side THD is measured for changing values of L and C. The results are given in Figure 4-50.

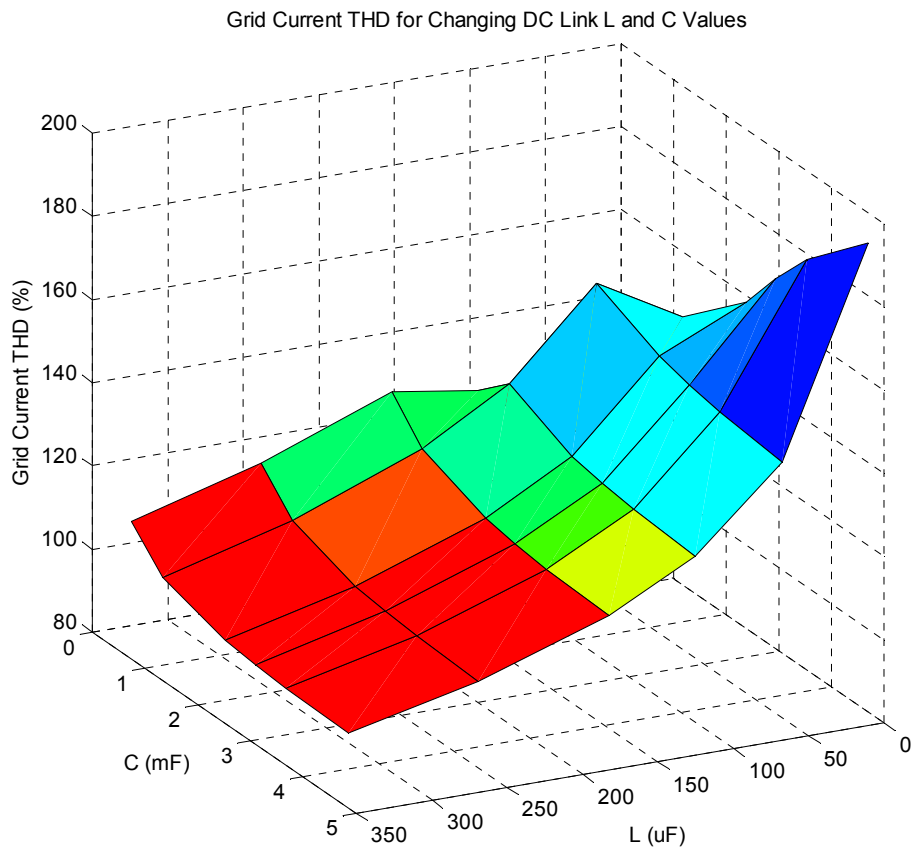


Figure 4-50 Grid Current THD for changing values of L and C

In Figure 4-50, the red color shows the higher THD points whereas blue color shows the lower THD points for the grid current waveform. As seen from Figure 4-50, grid current THD is increasing as the inductance value increases for the same capacitance value. It is maximized when the inductance and capacitance values are twice of the designed value.

Based on these results, it can be concluded that the capacitance and inductance values should be doubled to obtain highest power factor at grid side if the most important requirement for an application is to increase grid current THD. However, as explained before, for motor driver application, DC link voltage and capacitor power loss are the most critical requirements. Therefore, the capacitance and inductance values will be determined for these requirements first.

4.3.4.3.3. DC Link Lowest Voltage

For DC link design, the most important requirement is lowest DC link voltage for rated flux concern as explained before. After this, the other requirements can be improved based on lowest voltage concern.

In order to see the effects of inductance and capacitance value, DC link lowest voltage is measured for changing values of L and C. The results are given in Figure 4-51.

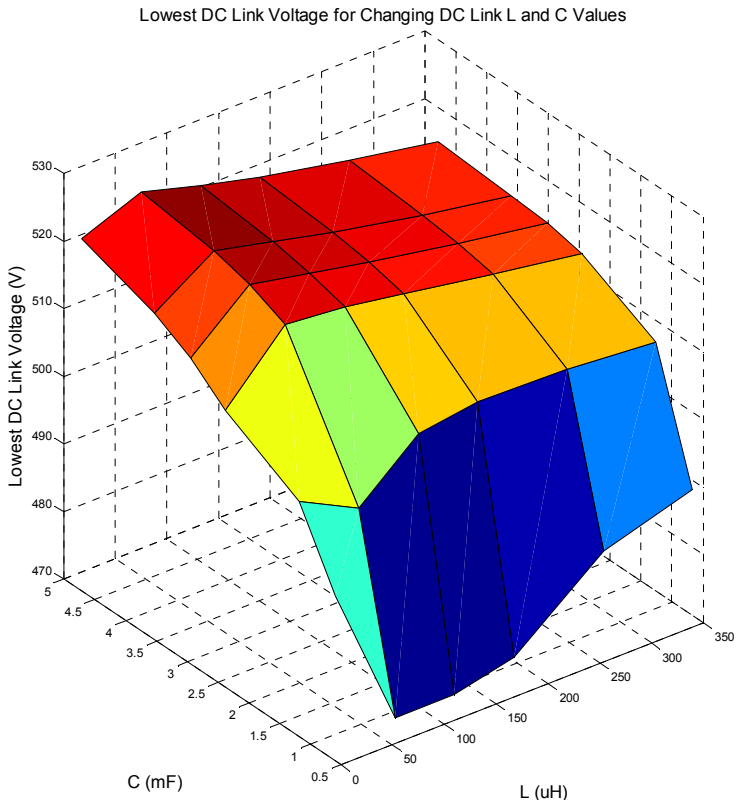


Figure 4-51 Lowest DC link voltage for changing values of L and C

In Figure 4-51, the red color shows the higher DC link voltage points whereas blue color shows the lower DC link voltage points. As seen from Figure 4-51, the DC link lowest voltage increases as the capacitance value increases for the same inductance value. In addition, increase in inductance value to some extent increases lowest

voltage level whereas after some point it decreases lowest voltage level because the voltage drop on inductor increases as its inductance increases.

As seen from Figure 4-51, the DC link voltage is maximized when capacitance value is twice of the designed value and inductance value is 1/3 of the designed value. Although, the DC link voltage value is maximized for this point, the inductance and capacitance values should be chosen considering capacitor power loss and after that cost and size concern of DC link.

4.3.4.3.4. Capacitor Power Loss and Its Peak Current

The capacitor power loss is caused by ESR (Equivalent Series Resistance) value of the capacitor. Electrolytic capacitors are used in many applications and their ESR value is high. Therefore, the power loss on them becomes high. Since the power loss is related with ESR value, it increases when the ripple current on the capacitor increases. In order for continuous operation and to increase the lifetime of capacitor, its hot point temperature should be low. This can be provided by reducing power loss of capacitor within acceptable limits.

In [36], it is stated that ESR values of electrolytic capacitors are high and ripple current causes high thermal losses. Therefore, the magnitude of ripple current should be reduced to increase lifetime of capacitor and so motor driver. In addition, in Figure 4-52, it is shown that lifetime of capacitor decreases with core temperature of capacitor. In order to decrease the core temperature, power loss on capacitor should be decreased.

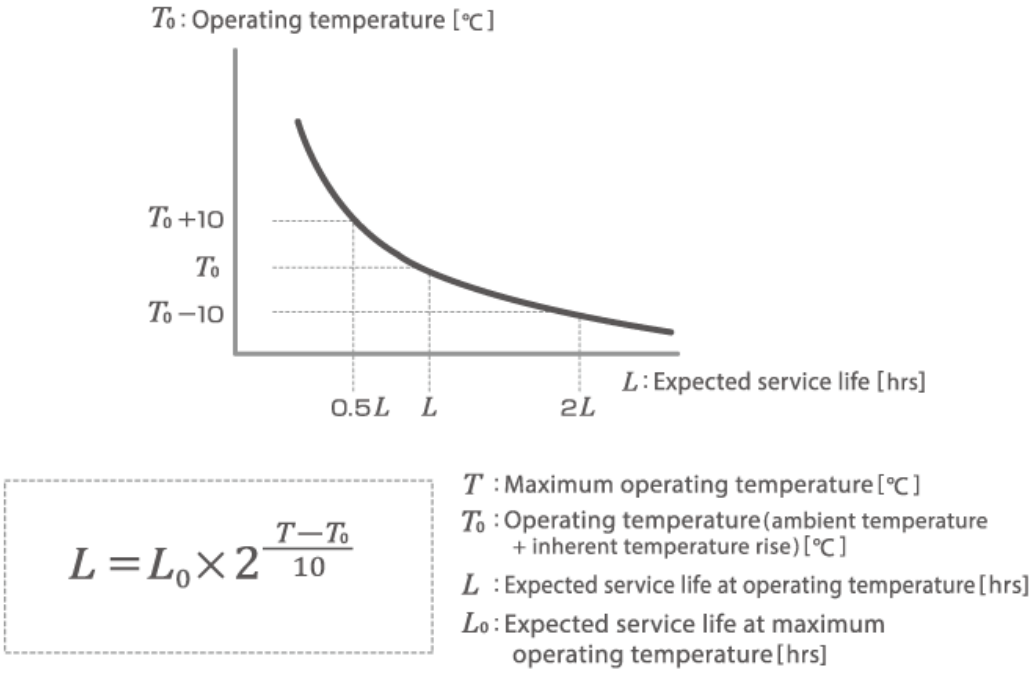


Figure 4-52 Electrolytic capacitor lifetime vs. temperature [36]

In order to see the effects of inductance and capacitance values, the capacitor power loss and its peak current are measured for different values of L and C. The results are given in Figure 4-53 and Figure 4-54.

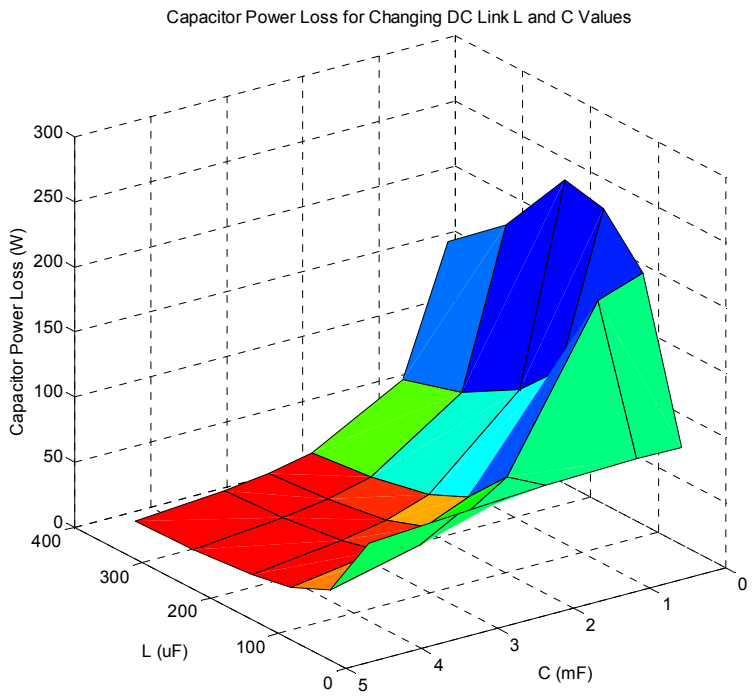


Figure 4-53 Capacitor loss for changing values of DC link capacitor and inductor

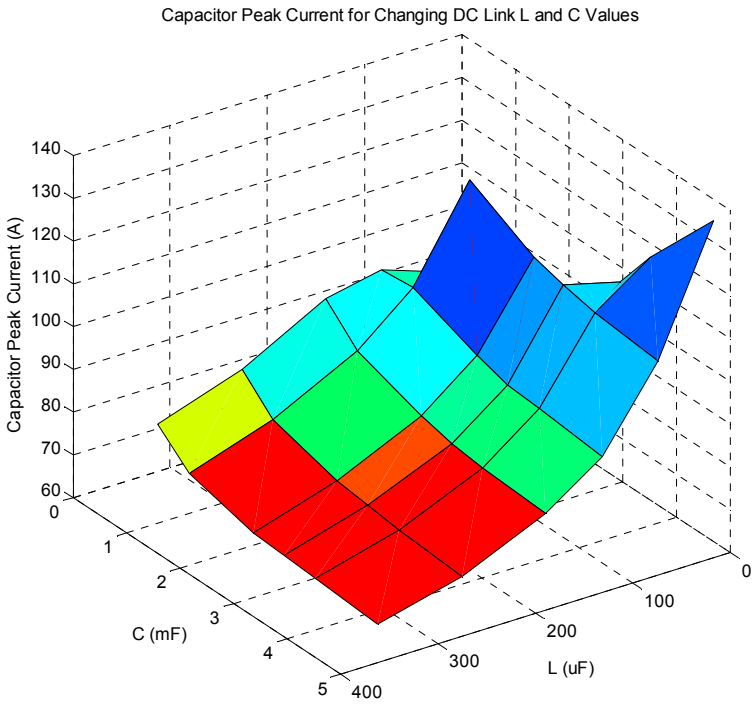


Figure 4-54 Capacitor peak current for changing values of DC link capacitor and inductor

In Figure 4-53, the red color shows the higher power loss points whereas blue color shows the lower power loss points. As seen from this figure, capacitor power loss decreases as the capacitance value increases for the same inductance value because the ripple current and ESR value of capacitor decreases.

In Figure 4-54, the red color shows the higher capacitor current points whereas blue color shows the lower capacitor current points. As seen from this figure, capacitor peak current is decreasing as the inductance value increases for the same capacitance value.

Based on these results, it can be concluded that to decrease capacitor power loss and capacitor peak current, capacitance and inductance values should be increased. In addition, their values are minimized when capacitance and inductance values are doubled as seen from Figure 4-53 and Figure 4-54.

4.3.4.4. DC Link Design Criteria for Dynamic Conditions

In order to determine the inductance and capacitance values of DC link for dynamic conditions, the DC link lowest voltage should be higher than 515V and the capacitor power loss should be lower than its permissible level. As explained before, 515V is required to obtain desired flux level in all frequency range and capacitor power loss should be low to increase the lifetime of capacitor and driver. The power loss limits for capacitance values are given in Table 4-13.

Table 4-13 Acceptable power loss limits for capacitance values

Capacitance Value (mF)	**Acceptable Power Loss (W)**
0,5875	<21,46
1,175	<21,46
2,35	21,46
2,9375	24,5
3,525	31,2
4,7	35,6

Since to obtain lower THD and higher power factor at grid side are not aimed for our application, after satisfying voltage and power loss criteria, the capacitance and inductance values will be determined considering size and cost of the DC link components.

In order to determine permissible region for voltage and power loss requirements, the requirement values for changing L and C values are given in Table 4-14 and Table 4-15. The allowed region for DC link voltage is shown with gray color in Table 4-14.

Table 4-14 DC link lowest voltage for L and C values

Lowest Voltage		**L (µH)**					
		0	**57,5**	**115**	**172,5**	**258,75**	**345**
C (mF)	**0,5875**	494,5	473	473	475	485,5	489,5
	1,175	504,9	500,4	508	509,2	508,8	507,7
	2,35	511,1	520,3	519,5	517,9	515,6	513,5
	2,9375	515,3	522,8	521	519,2	516,7	514,5
	3,525	518,3	524,2	522	**520**	517,3	515
	4,7	522,2	525,7	523,2	521	518,2	515,8

After obtaining the allowed region for DC link lowest voltage, the allowed region for the capacitor power loss should be determined. Acceptable power loss with respect to capacitance values are given in Table 4-13. Based on this table, the allowed region for power loss is determined and it is shown with gray color in Table 4-15.

Table 4-15 Capacitor power loss for L and C values

Capacitor Power Loss		**L (µH)**					
		0	**57,5**	**115**	**172,5**	**258,75**	**345**
C (mF)	**0,5875**	101,8	220	254	260	202,5	166
	1,175	101,85	208	139	108	82,5	69,2
	2,35	100,2	91	60	46,5	36,1	31,4
	2,9375	98,3	70	46	35,6	28,2	24,5
	3,525	96,2	56,5	37	**28,7**	23	20,2
	4,7	91,9	40,5	26,8	20,9	16,8	14,7

In order to decrease the size of DC link, the capacitance value should be low. To decrease the cost of the DC link, the inductance should be low because the inductor cost in motor driver application is higher than capacitor cost as stated in [37].

Considering cost and size of DC link, it is not feasible to increase the capacitance and inductance up to their maximum values. Calculations indicate that the new design approach requires a 50% higher capacitor value. By this way, DC link voltage and capacitor power loss requirements are satisfied while optimizing the DC link components for size and cost concerns.

Comparison of Old and New DC Link Designs

Simulations for rated power and dynamic conditions are implemented to see the differences between DC link designs for rated power condition and dynamic condition. The simulation results are given in Table 4-16 and Table 4-17.

Table 4-16 Rated power condition results for designed filters

	Parameter	**Old DC Link Design C=2.35mF L=172.5µH**	**New DC Link Design C=3.4mF L=172.5µH**
Input (Grid) Side	Power Factor	0.5	0.503
	Current THD (%)	129.45	127.8
	RMS Current (A)	11.48	11.48
	Peak Current (A)	48.5	47.5
Output Side	Voltage Dip (V)	524.2	525.5
	Ripple Voltage (V)	12.3	8
	Capacitor Loss (W)	18	11.9
	Capacitor Peak Current (A)	47.5	46.5

Table 4-17 Dynamic condition results for designed filters

	Parameter	**Old DC Link Design C=2.35mF L=172.5µH**	**New DC Link Design C=3.4mF L=172.5µH**
Input (Grid) Side	Power Factor	0.532	0.537
	Current THD (%)	117.05	114.94
	RMS Current (A)	20.6	20.55
	Peak Current (A)	82.5	80
Output Side	Voltage Dip (V)	517.9	520
	Ripple Voltage (V)	21.1	14
	Capacitor Loss (W)	46.5	29.6
	Capacitor Peak Current (A)	82.5	71.5

As seen from Table 4-16 and Table 4-17, if the filter is designed for dynamic conditions, the requirements are satisfied for dynamic conditions whereas they are improved for rated power conditions.

4.4. Results and Conclusion

The requirements for DC link design are analyzed in dynamic conditions with simplified model, motor driver simulation and experimental setup. From the results, it can be concluded that when DC link is designed for steady state condition, the lowest voltage, capacitor peak current and capacitor power loss exceeds the values at steady state condition. For capacitance and inductance calculations, equations in [30] are used. From rated power condition results, it is understood that capacitor is oversized for an application and the ripple voltage value did not increase to 20V at rated power condition. If the rated power condition results are compared with dynamic condition results, the analysis will be meaningful.

The results showed that the dynamic conditions should be considered for DC link design in order to meet DC link requirements. If it is not designed in this way, capacitor power loss can be increased to unacceptable levels and it can decrease lifetime of capacitor and so driver. Moreover, DC link voltage can decrease unacceptable levels so that DC link compensation cannot be implemented anymore and the desired flux level cannot be obtained in all frequency region of driver.

Based on the obtained results for our driver, DC link capacitance should be selected higher than ½ of its designed value based on [30] and inductance should be selected as designed value. Based on sample design given in [37], the inductor and capacitor costs are calculated. In the old design, the capacitor and the inductor cost are 48€ and 55€, respectively. In the new design, the capacitor cost is increased to 68€ while the inductor cost remains constant. As seen from the cost values, the cost of DC link is increased 20€ with new design and this cost increase is very small compared to cost of the motor driver system.

CHAPTER 5

CONCLUSION

In this thesis work, it is aimed to improve dynamic performance of motor driver. For this purpose, first a hardware and software environment needs to be created. For the software environment, new DSP controller, DS1104 is used because it can be programmed through MATLAB and it has better DSP controller with respect to old work. With the change of controller, the hardware is also changed. The reason is that in old controller, symmetrical pulses could not be generated; therefore, the solution is created in hardware environment using XOR gates. In addition, a dead time generator module was used in old work. However, the new controller can generate symmetrical gate pulses with adjusted dead time insertion. Therefore, the hardware is redesigned and software is changed with respect to new controller. At the end, we obtain the motor driver that is capable of field oriented control and scalar control.

In order to improve dynamic performance, first the parameters that affect the dynamic performance are identified. After identifying the parameters, we focus on DC link compensation and DC link design.

For DC link compensation, we review the literature and we implement two methods for compensation. Through simulations and experimental tests, the improving effect of DC link compensation in steady state and dynamic conditions are verified.

After DC link compensation, we work on DC link design. For this purpose, literature is reviewed and it is found that most of the DC link design includes inductor and capacitor. Therefore, DC link is designed with inductor and capacitor.

In the literature DC link design is implemented for rated power conditions and the dynamic conditions are not considered. As seen from the results given in chapter-4, the capacitor power loss and its peak current exceed its rated value with classical

design of DC link. By improving DC link design considering dynamic conditions, the capacitor power loss and its peak current are reduced below its rated values. By this way, the lifetime of capacitor and therefore the lifetime of driver are increased. In addition, the DC link lowest voltage increases with the new design. Although, the cost of the new DC link design is higher than the old one, the rise in cost value is very small compared to drive cost.

Since this work is limited with DC link compensation and its design considering dynamic conditions, the other parameters affecting dynamic performance should be researched and implemented in the experimental setup. In future work, we will focus on following parameters which are more important than others to increase dynamic performance.

- PI Controller Constants
- Decoupling Control of d and q Axes Components
- Dead Time Compensation

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