DESIGN OF AN INTERLEAVED PWM RECTIFIER FOR AC LOCOMOTIVES AND IMPLEMENTATION OF ITS LABORATORY PROTOTYPE

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ABSTRACT

DESIGN OF AN INTERLEAVED PWM RECTIFIER FOR AC LOCOMOTIVES AND IMPLEMENTATION OF ITS LABORATORY PROTOTYPE

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This research work is devoted to the design, and prototype implementation of a single-phase, unity power factor, Pulse Width Modulated (PWM) Rectifier for use in traction converters of AC locomotives. The PWM Active Rectifier is supplied from a front-end transformer, with two isolated secondary windings. The associated power stage is composed of two single-phase, H-bridge voltage-source converters, which are interleaved via a common DC link. Interleaved connection of converters is used to reduce the line current total demand distortion on the grid side of the traction transformer, to comply with the IEEE Std. 519-1992.

Control techniques and PWM methods used in AC locomotive traction applications are analyzed, compared and digitally implemented on a DSP microcontroller. The design and optimization of this system is achieved on MATLAB/Simulink simulation environment. The performance of the implemented system is tested on a low power laboratory prototype composed of the developed PWM rectifier, and a four-quadrant,

frequency-controlled induction motor drive and satisfactory results have been obtained.

Keywords: PWM Rectifier, Interleaved Connection, Phase Shifted PWM, Voltage Source Converter (VSC), AC Locomotive Traction

ÖZ

AA LOKOMOTİFLER İÇİN FAZ KAYMALI BİR DGM DOĞRULTUCU TASARIMI VE LABORATUVAR PROTOTİPİ UYGULAMASI

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Ağustos 2015, 235 sayfa

Bu araştırma çalışması, AA lokomotiflerin çekiş sisteminde kullanılmak üzere tek faz, birim güç faktöründe çalışan bir Darbe Genişlik Modülasyonu (DGM) Aktif Doğrultucu tasarımı ve prototip uygulamasına adanmıştır. DGM Aktif Doğrultucu, iki izole sekonder sargıya sahip bir giriş transformatörü üzerinden beslenmektedir. İlgili güç katı ortak bir DA Bağ üzerinden paralel bağlı iki adet tek faz, H-köprü gerilim kaynaklı çevirgeçten oluşmaktadır. Çekiş transformatörünün şebeke tarafındaki hat akımı toplam talep bozunumunu, IEEE 519-1992 standardına uygun olacak şekilde, azaltmak amacıyla çevirgeçler paralel bağlanmıştır.

AA lokomotif çekiş sistemlerinde kullanılan kontrol teknikleri ve DGM yapıları incelenmiş, karşılaştırılmış ve bir DSP mikrodenetleyici üzerinde sayısal olarak gerçekleştirilmiştir. Bu sistemin tasarımı ve eniyilenmesi MATLAB/Simulink benzetim ortamında başarılmıştır. Uygulanan sistemin başarımı geliştirilen DGM doğrultucu ve bir dört çeyrekte çalışan frekans kontrollü endüksiyon motor sürücü

sisteminden oluşan bir düşük güç laboratuvar prototipi üzerinde test edilmiş ve olumlu sonuçlar elde edilmiştir.

Anahtar Kelimeler: DGM Doğrultucu, Paralel Bağlantı, Faz Kaymalı DGM, Gerilim Kaynaklı Çevirgeç (GKÇ), AA Lokomotif Çekiş Sistemi.

To my nieces, Ecmel and Caner

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NOMENCLATURE

η	Converter Efficiency
φ	Power Angle
δ	Load Angle
θ	PLL Phase Output
B	Flux Density
C_{dc}	DC Link Capacitor
C_f	DC Link Resonant Filter Capacitor
E_{off}	Turn-off Switching Energy
E_{on}	Turn-on Switching Energy
E_{rr}	Reverse Recovery Energy
E_{ss}	Steady State Error
f_{car}	Carrier Frequency
f_h	Frequency of Harmonic h
f_r	DC Link Ripple Frequency
f_s	Supply Frequency
f_{sw}	Switching Frequency
h	Harmonic Order
I_c	Converter Current
I_C	Continuous IGBT Current
I_{CM}	Pulsed IGBT Current
I_{dc}	DC Link Current

I_{dc}^{*}	DC Link Current Reference
I_E	Continuous Diode Current
I_{EM}	Pulsed Diode Current
I_L	Load Current
I_s	Supply Current
I_s^{*}	Supply Current Reference
I_{sA}	Converter-A Current
I_{sB}	Converter-B Current
I_{sc}	Short Circuit Current
K_p	Proportional Gain
K_i	Integral Gain
k_w	Winding Factor
L_f	DC Link Resonant Filter Inductor
L_s	AC Line Filter Inductor
L_{stray}	Stray Inductance
m	Number of Converters Connected in Series
m_a	Amplitude Modulation Index
m_f	Frequency Modulation Index
n	Number of Converters Connected in Parallel
N	Turn Number
$P_{c\text{-}T}$	IGBT Conduction Loss
$P_{c\text{-}D}$	Diode Conduction Loss
P_{dc}	DC Link Power
P_{rr}	Diode Reverse Recovery Loss
P_s	Supply Active Power

P_{sA}	Converter-A Active Power
P_{sB}	Converter-B Active Power
P_{sw}	IGBT Switching Loss
Q_s	Supply Reactive Power
Q_{sA}	Converter-A Reactive Power
Q_{sB}	Converter-B Reactive Power
R_G	Gate Resistance
S_s	Supply Apparent Power
$t_{d\text{-}on}$	Turn-on Delay Time
$t_{d\text{-}off}$	Turn-off Delay Time
t_f	Turn-off Fall Time
t_r	Turn-on Rise Time
t_{rr}	Reverse Recovery Time
T_{max}	Maximum Torque
V_c	Converter Voltage
V_c^*	Converter Voltage Reference
V_{car}	Carrier Signal
V_{cA}	Converter-A Voltage
V_{cB}	Converter-B Voltage
V_{CES}	IGBT Blocking Voltage
$V_{CE\text{-}sat}$	IGBT Saturation Voltage
V_{EC}	Diode ON State Voltage
V_{dc}	DC Link Voltage
V_{dc}^*	DC Link Voltage Reference
$\widetilde{V_{dc}}$	DC Link Ripple Voltage

V_{gate}	Gate Signal
V_{GE}	IGBT Gate-Emitter Voltage
V_{mod}	Modulating Signal
$V_{r\text{-}pp}$	Peak to Peak Ripple Voltage
V_s	Supply Voltage
w_b	Base Speed
w_c	Cut-off Frequency
w_{max}	Maximum Speed
w_{res}	Resonance Frequency
w_s	Supply Frequency
X_s	Series Reactance
Y_s	Shunt Admittance

LIST OF ABBREVIATIONS

2LC	Two-level Converter
3LC	Three-level Converter
4Q	Four Quadrant
AC	Alternating Current
ADC	Analogue-to-Digital Converter
CH	Charging State
CPU	Central Processing Unit
CSR	Current Source Rectifier
DC	Direct Current
DCL	DC Link
DCMLC	Diode Clamped Multilevel Converter
DQ0	Direct-Quadrature-Zero
DSC	Digital Signal Controller
DSCH	Discharging State
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EMU	Electric Multiple Units
ePWM	Enhanced Pulse Width Modulation
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FET	Front-End Transformer

FLC	Flying Capacitor
FW	Freewheeling State
GCT	Gate Commutated Thyristor
GTO	Gate Turn-off Thyristor
I2LC	Interleaved Two-level Converter
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineering
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
ISR	Interrupt Service Routine
LFT	Low Frequency Transformer
LPF	Low Pass Filter
LRV	Light Rail Vehicle
MFT	Medium Frequency Transformer
MOSFET	Metal Oxide Field Effect Transistor
NPC	Neutral Point Clamped
OSG	Orthogonal Signal Generator
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PD	Phase Detection
PET	Power Electronics Transformer
pf	Power Factor
PFC	Power Factor Correction
PI	Proportional Integral
PLL	Phase Locked Loop

PR	Proportional Resonant
PWM	Pulse Width Modulation
RBSOA	Reverse Bias Safe Operating Area
RMS	Root Mean Square
RRSOA	Reverse Recovery Safe Operating Area
SCMC	Series Connected Multilevel Converter
SCR	Silicon Controlled Rectifier
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SOC	Start of Conversion
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TI	Traction Inverter
TM	Traction Motor
TZ	Trip Zone
VCO	Voltage Controlled Oscillator
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier
VVVF	Variable Voltage Variable Frequency

CHAPTER 1

INTRODUCTION

Railway electric traction is considered as one of the most preferred means of transportation due to its advantages such as being economical, environment friendly and having good acceleration and deceleration rates when compared to road travel with private owned vehicles [1]. Road travel demerits like unstable gasoline prices, traffic congestion and carbon emission have made railroad transportation the most efficient way of public transportation.

Railway transportation is also considered a critical component in economic development [2]. Demand in both passenger and freight rail investment (including equipment, infrastructure and service) all around the world has a projected growth of 214$ billion by 2016. One third of this amount is established by rail vehicle investment [3]. The most developed countries have placed importance on railroad enterprise and technology and should be taken as examples. Germany's railway industry is still a global technology leader. Spain, on the other hand, still holds the greatest high speed rail infrastructure program in Europe. Japan is playing for the global leadership in the market as usual and according to the study of Global Competitiveness in Rail Industry performed by Worldwatch Institute, which stands as an environmental research organization, 38 percent of Japanese railway manufacturers' income is composed of export revenue for the last ten years [3]. High speed rail is said to be one of the most vital parts of China's growth strategy, which now has become the 1st rank country on the gross domestic product (GDP) statistics [4]. Statistics show that passenger-km travelled by rail transportation doubled in China from 2001 to 2011. Officials in Turkey have also noticed this tendency and the virtues of railway transportation not

only as a public service but also a key ingredient for the economic development. Turkish State Railway authorities have recently announced that the investment objective to the rolling railroad industry is 45$ billion by 2023 [5].

Mankind has utilized electrified railway traction systems since 1830s employing various types of traction systems through time. First type of railway traction system was battery-powered with maximum speed of 7 km/h. Today, the world record of fastest rail vehicle in the world is 603 km/h set by L0 Series of Japan in April 2015 on a magnetic levitation track [6].

Today, railway traction technology is dominated by Bombardier from Canada, Alstom from France and Siemens from Germany. Two of China's rolling stock manufacturers; CSR and CNR, CAF from Spain and Hyundai Rotem from South Korea are considered the following candidates for the railway traction technology leadership [3]. Turkey still comes short of such a foundation to take its place on the top spots, but the recent regulations, efforts and statements by the state officials are promising.

Railway traction system technology is improving correspondingly with the developments in power electronics and regarding its importance for society and economic development, this technology can be considered as a vital subject in electrical machines and power electronics field of engineering.

1.1. Railway Electric Traction Systems

An electric railway vehicle is supplied from a railway electrification system instead of having an on-board prime mover or fuel supply. Today, almost all railway traction systems are electrified. Although it is advantageous, it requires significant investment cost. General structure of a railway electric traction system is shown in Figure 1.1. The traction system is designed to meet the requirements on both motor side (speed control) and catenary side (power quality).

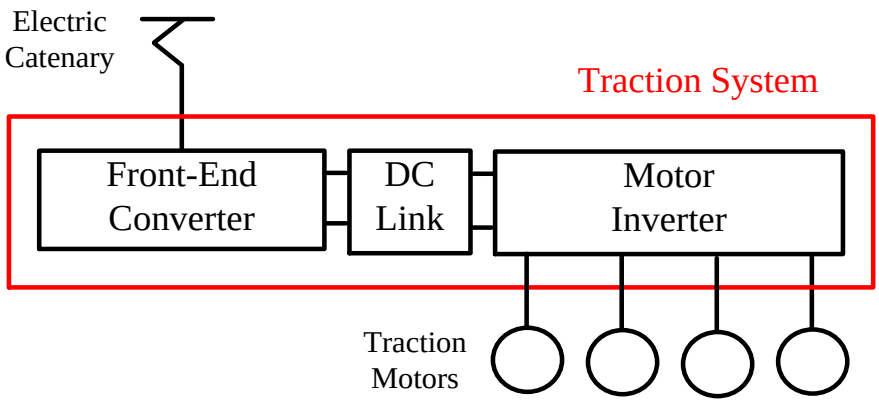


Figure 1.1: General Structure of a Railway Electric Traction System

Electric railway vehicles have the advantages of better efficiency, lower emission, lower operating costs, being more quite, more responsive and more reliable over diesel electric vehicles. It is also possible to turn the kinetic energy into electrical form and supply to the mains. On the other hand, if there is no storage system installed or their own generators, they are vulnerable to power interruptions.

Railway electrification systems usually have their own distribution lines, switches and transformers. Electric railway vehicles can be connected to the supply system via two types of contacts systems; to an overhead line via a pantograph and through a conductor rail (usually a third rail, sometimes fourth rail).

There are several types of railway electric vehicles which can be classified in two categories; urban and intercity. Urban services include streetcars, trams, metros and light rail vehicles (LRV). Intercity services include conventional trains or high speed trains and intercity vehicles are of two types; locomotives and electric multiple units (EMUs).

There are six types of railway electrification system voltages [7 - 10] as shown in Table 1.1, along with vehicles used and example traction systems around the world. The permissible voltage ranges for the standard catenary voltages are stated in BS EN 50162 standard as shown in Table 1.2 [11].

Table 1.1: Railway Electrification System Voltages and Vehicles Used

Catenary Voltage	**Vehicle**	**Example Traction System**	**Country**
600V DC	Tram	Brussels Tram	Belgium
	Streetcar	Kenosha Streetcar	USA
	Light Rail Vehicle	Edmonton Transit LRT	Canada
750V DC	Tram	Athens Tram	Greece
	Streetcar	Portland Streetcar	USA
	Light Rail Vehicle	Bergen Light Rail	Norway
	Metro	Rotterdam Metro	Netherlands
1500V DC	Metro	Buenos Aires Metro	Argentina
	Intercity Train	Sydney Trains	Australia
3000V DC	Intercity Train	Spanish National Railway	Spain
15kV, 16.7Hz AC	Intercity Train	German National Railway	Germany
25kV, 50/60Hz AC	Intercity Train	Turkish State Railways	Turkey

Table 1.2: Permissible Voltage Ranges of Standard Catenary Voltages [11]

Catenary Voltage	Minimum Non-Permanent	Minimum Permeant	Maximum Permeant	Maximum Non-Permanent
600 VDC	400 V	400 V	720 V	800 V
750 VDC	500 V	500 V	900 V	1000 V
1500 VDC	1000 V	1000 V	1800 V	1950 V
3000 VDC	2000 V	2000 V	3600 V	3900 V
15 kV AC, 16.7 Hz	11 kV	12 kV	17.25 kV	18 kV
25 kV AC, 50/60 Hz	17.5 kV	19 kV	27.5 kV	29 kV

When a railway electric traction vehicle brakes, kinetic energy is generated on the wheels; the electromechanical torque produced by the traction motors is in the opposite direction of the motor rotational speed. Thus, the kinetic energy is converted to electrical energy by the traction machines.

The electrical energy produced is transferred to the DC link of the traction system by the traction inverter. This excess energy should go somewhere; otherwise the DC link storage element will charge continuously leading to a failure of the system after exceeding the permissible DC link voltage limit. Several braking systems have been in use to deal with this excess energy. Braking types used in railway electric traction systems are shown in Figure 1.2 [12].

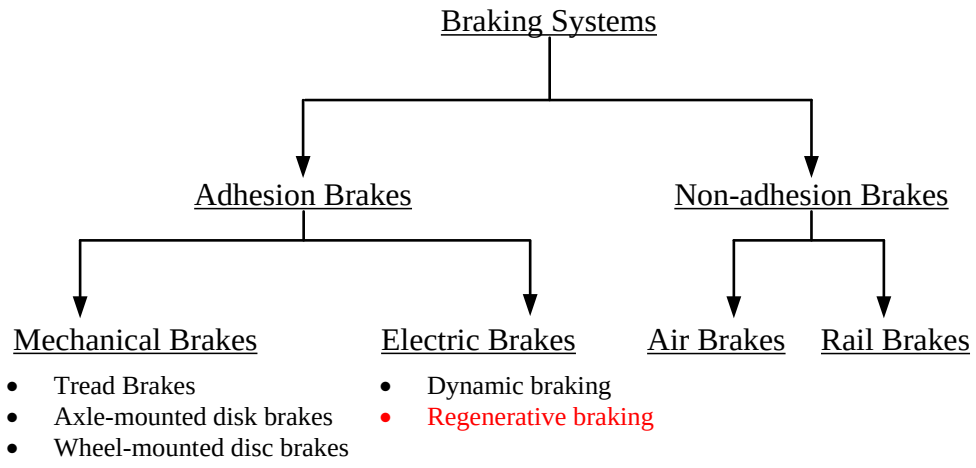


Figure 1.2: Braking Types Used in Railway Electric Traction Systems [12]

The very first type of braking applied to railway electric vehicles was a simple hand brake. Next, new braking equipment come into use employing vacuum brakes or air brakes. With the first introduction of dynamic braking systems, air brakes and dynamic braking started to be used together. Mechanical brakes are still in use for reliability issues. Principle of mechanical braking systems is the application of friction to the wheels through a mechanism such as brake shoes [12].

Adhesive braking systems rely on friction whereas non-adhesive braking mechanisms don't. Non-adhesive braking systems were developed for the cases of high speed where adhesion between wheels and the rail decrease. Rail brakes, a commonly used type of non-adhesive braking systems use eddy currents and frictional force with use of batteries to create magnetic fields and hence eddy currents [12].

Electric brakes are more economical and efficient when compared to mechanical brakes since they do not use friction elements. There are two types of electrical braking systems; dynamic braking and regenerative braking. With dynamic braking, the generated excess energy is converted to heat by dissipating on a braking resistor with a controlled braking chopper. On the other hand, with regenerative braking, this energy is fed to the mains supply in a more energy efficient manner [13]. Regenerative braking is possible in AC traction systems; i.e., traction systems supplied from AC catenaries. As of today, all AC locomotive traction systems utilize regenerative braking. 25-40 % of energy can be returned to the electric supply by locomotives using regenerative braking [14]. An illustration of dynamic braking and regenerative braking is shown in Figure 1.3.

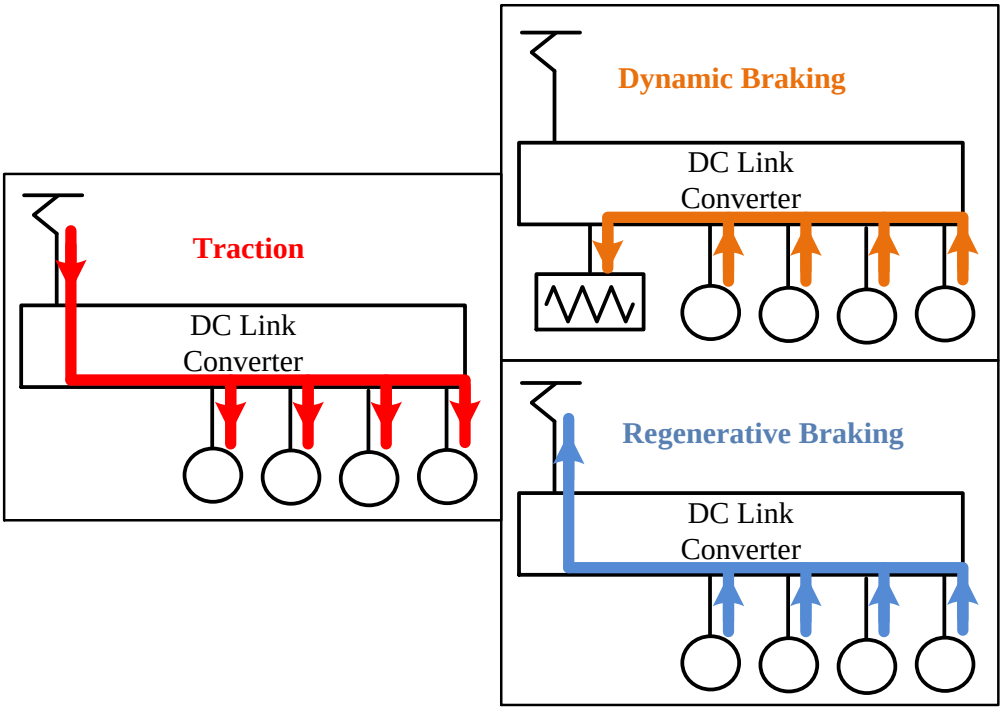


Figure 1.3: Illustration of Dynamic Breaking and Regenerative Braking

On the other hand, DC traction supply systems have a diode bridge rectifier interface on the substation which does not let the energy flow on the other direction. The only way by which regenerative braking can be utilized is the usage of excess energy of a decelerating vehicle by an accelerating vehicle on the same line at the same time.

Recently, storage systems have come into use in such DC railway systems employing batteries, ultra-capacitors or both. Energy management can be achieved in such systems. Mitrac Energy Saver developed by Bombardier is a successful example of energy storage systems having energy saving rates up to 30 percent [15]. Being commonly used in tramways and subways, another advantage of on board energy storage is that the vehicle can still operate for a period of time in the absence of supply contact making these systems possible to be used in intercity services. Illustration of energy storage systems is shown in Figure 1.4 [15].

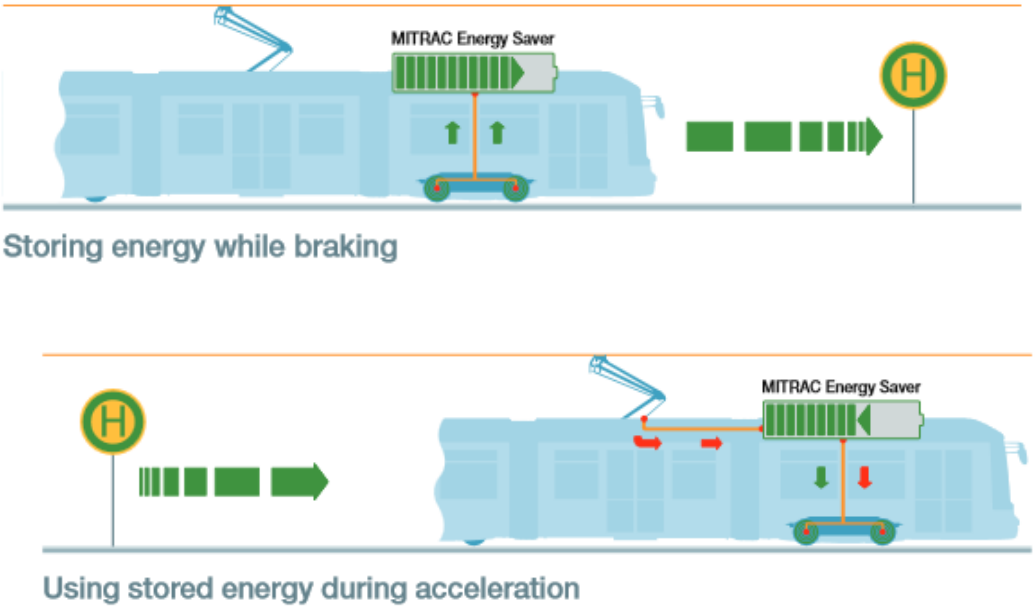


Figure 1.4: Illustration of Energy Storage Systems [15]

As mentioned earlier, intercity railway transport systems (conventional passenger trains, conventional freight trains and high-speed passenger trains) may employ two types of traction vehicles: locomotives which use concentrated traction system and EMUs which use distributed traction system [16].

In concentrated traction systems, the traction force is supplied by only two vehicles (locomotives) which are at the two ends of the train; whereas, in distributed traction systems, the traction force is distributed among most of the vehicles along the train which are called self-propelled vehicles as shown in Figure 1.5 [16].

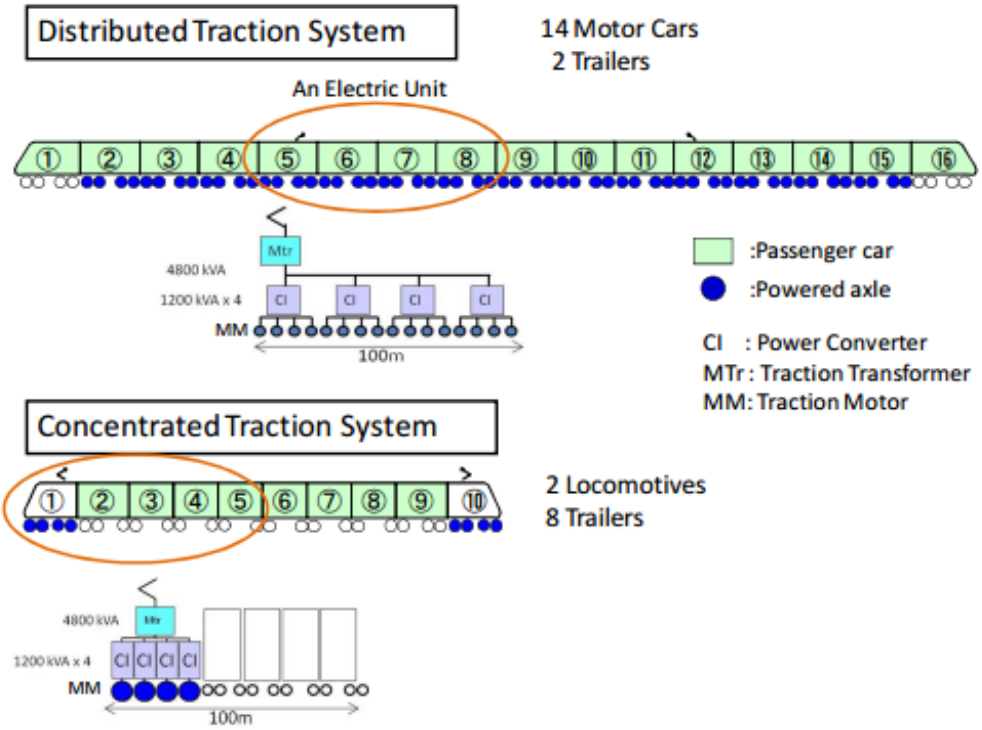


Figure 1.5: Concentrated Traction System and Distributed Traction System [16]

EMU configuration is usually preferred in high speed passenger trains and rarely used in freight trains. Locomotive configuration, on the other hand, is mostly used in higher power freight trains with lower speed levels [17].

Advantages of locomotives and EMUs over the other one can be seen in Table 1.3 [16].

Table 1.3: Advantages of Locomotives and EMUs [16]

Advantages of Locomotives	**Advantages of EMUs**
Easily replaceable under failure conditions	More energy efficiency
Maximum utilization of power cars	Redundancy
Safer operation in the events of accidents	More adhesion force
Less noisy for passengers	Better acceleration and deceleration rates
Lower initial cost	Lower maximum axial loads

1.2. Main Line Locomotive Traction Systems

Traction power supplies used for main line locomotives are listed in Table 1.4 [18, 19].

Table 1.4: Traction Power Supplies for Main Line Locomotives

Catenary Voltage	Countries
1500V DC	Netherlands, France, Slovakia, India
3000V DC	Belgium, Italy, Spain, Poland
15kV, 16.7Hz AC	Austria, Germany, Norway, Sweden
25kV, 50Hz AC	Turkey, Ukraine, Romania, Portugal
25kV, 60Hz AC	Canada, Japan, South Korea, United States

For DC catenary systems, the DC link of the converter can be fed directly from the catenary with a LC low pass filter configuration as shown in Figure 1.6. If a different voltage level on the DC link is required, a front-end converter can be used as input chopper. If the voltage on the DC link is to be higher than the catenary voltage, the input chopper is in boost configuration as shown in Figure 1.7 and if the DC link voltage is to be lower, the input chopper is in buck configuration as shown in Figure 1.8 [8, 20].

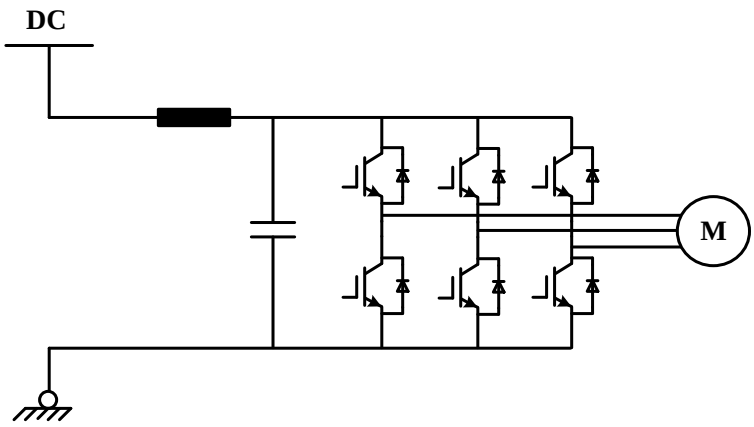


Figure 1.6: DC Traction System Configuration without Input Chopper

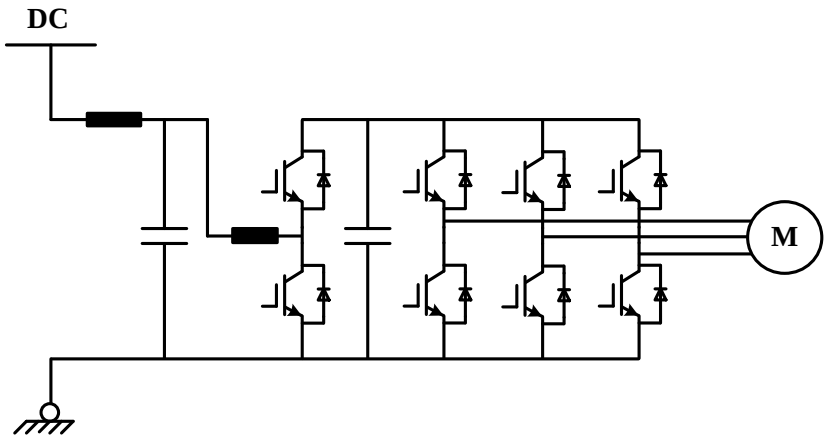


Figure 1.7: DC Traction System Configuration with Boost Input Chopper

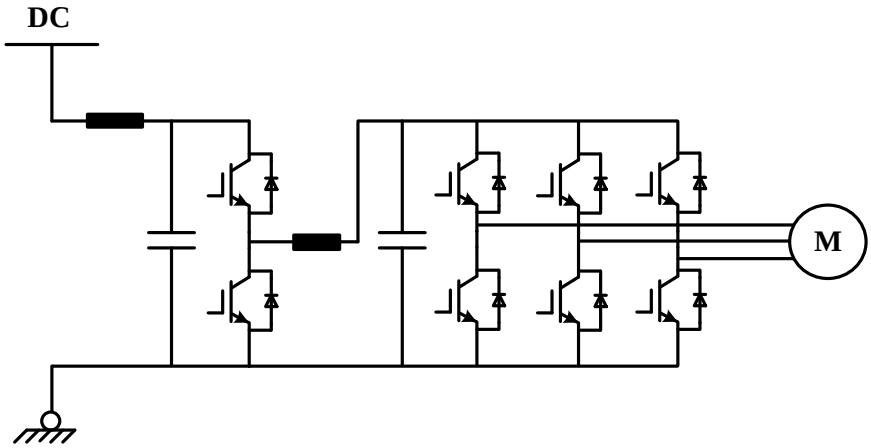


Figure 1.8: DC Traction System Configuration with Buck Input Chopper

A typical locomotive traction system supplied from AC catenary with four DC link converters is shown in Figure 1.9 [21, 22].

A high power main line AC locomotive traction system mainly consists of a front-end transformer (FET) with multiple secondary windings, dc-link converters composed of a front-end converter (FEC), DC link (DCL) and traction inverter (TI) and traction motors (TM). Detailed analysis of AC locomotive traction systems will be carried out in Chapter 2.

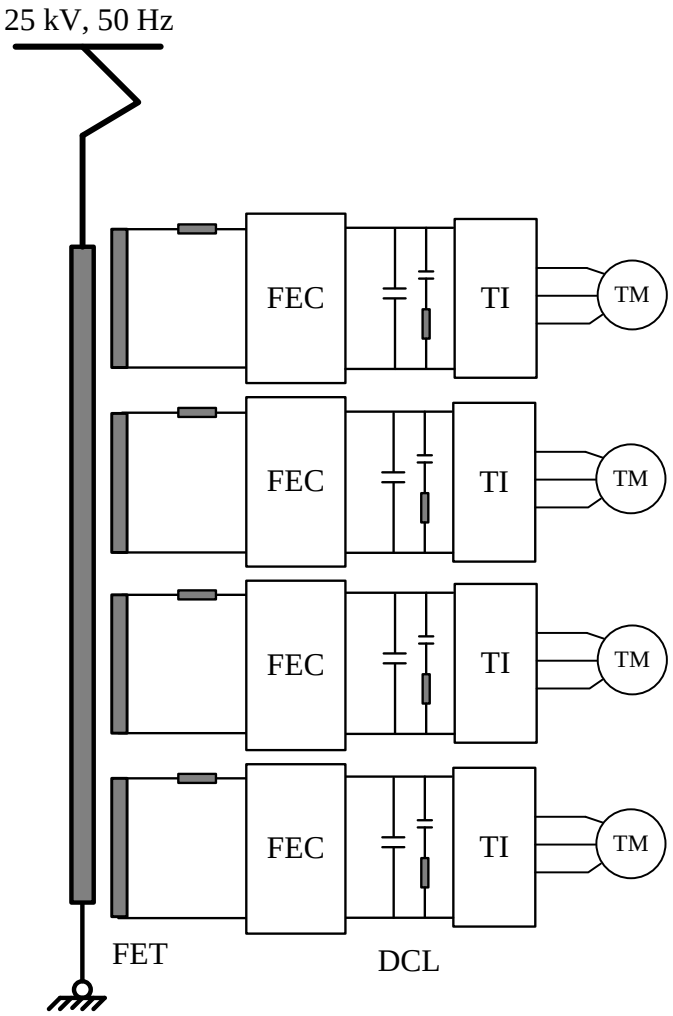


Figure 1.9: Typical Locomotive Traction System Supplied From AC Catenary

In Europe, a variety of catenary voltages exist as seen in Table 1.4. A train traveling to another country or even to another city has to be able to operate connected to distinct supplies. Such locomotives which can operate on different catenary types (AC and DC) or different voltage levels are called multisystem locomotives [23]. Vectron Universal Locomotive developed by Siemens is a good example of this type of vehicle. With a maximum speed of 200 km/h, this vehicle can operate on four types of catenary systems listed above [24].

In multisystem locomotives, the power stage at the front-end of AC locomotive traction systems can be used as the chopper circuit at DC catenaries as shown in Figure 1.10 or they may be chopperless as shown in Figure 1.11 [8, 18].

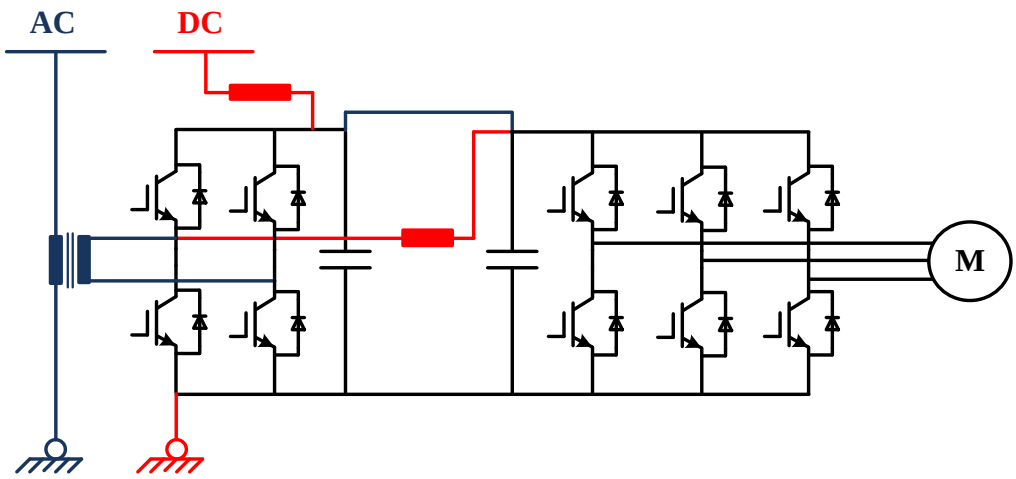


Figure 1.10: Multisystem Locomotive Traction System with Input Chopper

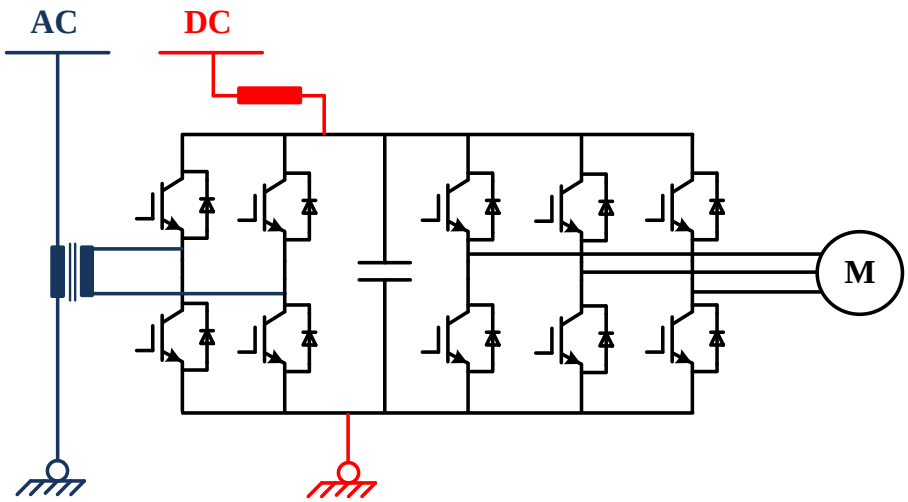


Figure 1.11: Multisystem Locomotive Traction System without Input Chopper

Power semiconductor devices are the essential part of traction converters as they are used to regulate or modulate voltage and current waveforms. Power semiconductors present on the front-end converter of AC locomotives are used to regulate the DC link voltage and modulate the converter input current waveform.

First generation of traction systems employing power electronics utilized thyristors, which are often called Silicon Controlled Rectifiers (SCR). SCRs were used in phase-controlled rectifier traction drives and chopper drives for high power

locomotives. They required auxiliary turn-off circuitry for self-commutation [25].

The second generation power semiconductor technology used in locomotive traction applications was Gate Turn-off Thyristors (GTO) which made forced commutated thyristors obsolete as they can be turned off with applied signals. After the introduction of GTO, voltage source converters became more practical [25]. Control of traction systems were implemented with analogue circuits in the era of thyristors. In 1980s, coinciding with the introduction of GTO, 16-bit microprocessors became commercially available to be used in traction control systems, enabling digital control of the power devices [26].

The latest and most common power semiconductor device used in high-power locomotive traction applications is Insulated Gate Bipolar Transistors (IGBT). They were first introduced to the electrified railway transport in 1995 with 1700V voltage blocking capability [10]. They offer a simpler, lower cost and more efficient drive than GTOs for traction power electronics applications. Moreover, IGBTs can operate at higher switching frequencies than GTOs. Although they can be switched with up to 5 kHz theoretically, the switching frequency applied to IGBTs is usually restricted up to 1 kHz in high power traction applications to meet efficiency requirements [25, 27].

Advantages of IGBTs in high power converter technology can be summarized as following [20]:

- They have easy gate drive since they are voltage controlled devices.
- They require no snubber circuits which lead to reduced weight, volume and better efficiency.
- Lower switching losses and thus higher switching frequency is possible.

IGBTs are now available with voltage ratings up to 6.5 kV and current ratings up to 2.4 kA and they are the best candidate among power semiconductor devices for high power AC locomotive traction applications [21].

Gate-Commutated Thyristors (GCT) which are often called Integrated Gate-Commutated Thyristors (IGCT) are derived from GTO structure and mostly replaced GTOs in applications with high power levels. They have the benefits of low conduction losses, less volume, lower gate inductance over GTO counterparts [28].

In the recent years, a new type of power semiconductor device, Silicon-Carbide Metal Oxide Field Effect Transistor (SiC MOSFET) has become a trend in many applications like renewable energy systems. These components allow high switching frequency operation as their switching loss is much lower compared to IGBT counterparts. SiC MOSFETs are also a candidate to become the new generation of power semiconductor device for railway traction systems [10].

Voltage and current ratings of power semiconductor devices are shown in Figure 1.12 [28].

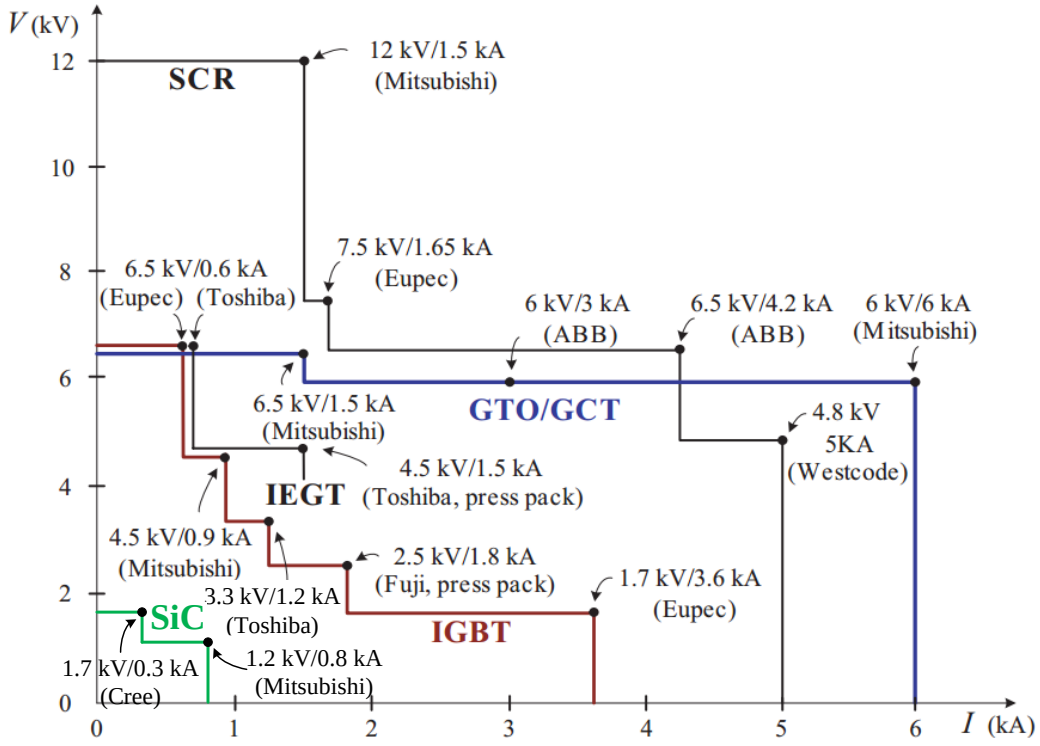


Figure 1.12: Voltage and Current Ratings of Power Semiconductor Devices [28]

Furthermore, qualitative comparison for GTO, GCT and IGBT power semiconductors is also shown in Table 1.5 [28].

Table 1.5: Qualitative Comparison for GTO, GCT and IGBT Power Devices [28]

Item	GTO	GCT	IGBT
Maximum voltage and current ratings	High	High	Low
Packaging	Press pack	Press pack	Module or Press pack
Switching speed	Slow	Moderate	Fast
Turn-on snubber	Required	Required	Not Required
Turn-off snubber	Required	Not Required	Not Required
Active overvoltage clamping	No	No	Yes
Active *di/dt* and *dv/dt* control	No	No	Yes
Active short circuit protection	No	No	Yes
Conduction loss	Low	Low	High
Switching loss	High	Medium	Low
Behavior after destruction	Short-circuited	Short-circuited	Open-circuited
Gate driver	Complex, separate	Complex, integrated	Simple, compact
Gate driver power consumption	High	Medium	Low

Traction motor is the part where the electromechanical energy conversion occurs. First type of locomotives had DC traction motors and they were widely used from mid 1800s to 1980s in traction systems [25]. Traction systems employing thyristors usually had DC traction motors. After the introduction of GTOs, three phase asynchronous motor drive became a standard in locomotive traction applications [29, 30]. In railway traction applications, induction motor has brought several advantages as improved reliability, improved power to weight ratio and improved power to volume ratio compared to DC traction motor [31]. The advantages of asynchronous traction motors can be summarized as following [32]:

- Lighter weight. Thus, it is possible to install more power per wheel set.
- Maintenance is reduced with the absence of collectors or brushes.
- Maximum torque can be obtained at any time.
- Because of the steep torque speed characteristics, spinning does not occur.

1.3. Rectifier Topologies

As mentioned previously, the traction system of a main line locomotive is composed of a front-end converter (rectifier stage) and motor-drive converter (inverter stage). The main task of the rectifier stage is to supply a constant DC link voltage (in both motoring and regenerative braking operation modes) from the AC catenary with good power quality and sufficient dynamic performance. The rectifier acts as an interface between AC catenary line and traction inverter, and holds great importance in high power traction systems.

The main requirements the rectifier stage should meet are; ensuring a constant DC link voltage for the traction inverter to operate successfully, to supply the braking energy to the AC catenary line (bidirectional active power flow), to operate at unity power factor (or at a desired power factor if reactive power absorption or injection is needed) and drawing or supplying currents with harmonic content in compliance with the standards stated in IEEE Std. 519-1992 [33]. Meeting the power quality standards is a must since adverse effects of high power loads to the AC line will be more severe, as in the case of locomotive traction load. The rectifier should be also able to regulate the catenary line voltage by supplying or absorbing reactive power when necessary. Another requirement is redundant operation. Continuous operation of a railway electric vehicle is important especially for inter-city vehicles like high-speed trains employing locomotives. When one converter fails, the operation may continue with reduced output power if there is redundancy in the rectifier stage.

High power rectifier configurations can be classified as in Figure 1.13 [34]. Basically, there are two types of rectifier systems: line commutated rectifiers and power factor correction (PFC) type rectifiers. Line commutated converters are based on diodes (uncontrolled) or SCRs (half-controlled, controlled) and PFC type rectifiers are PWM controlled employing formerly GTO and recently GCT or IGBT.

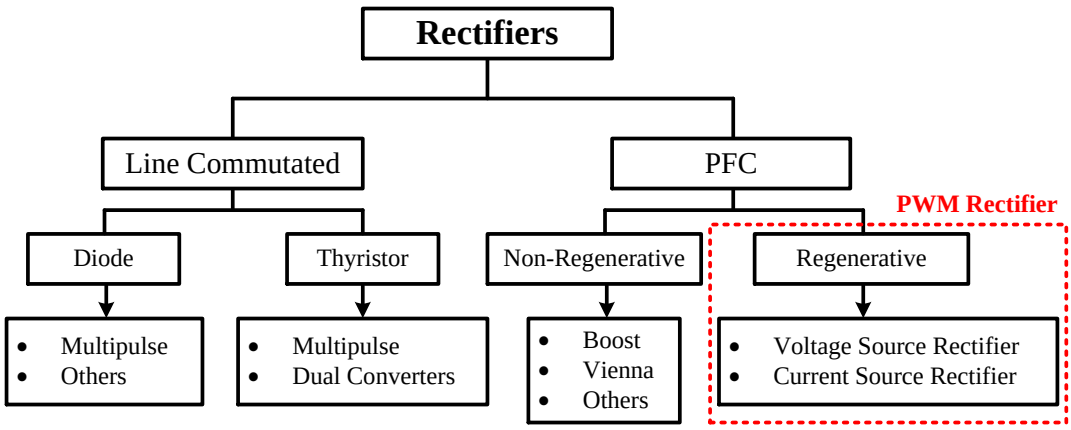
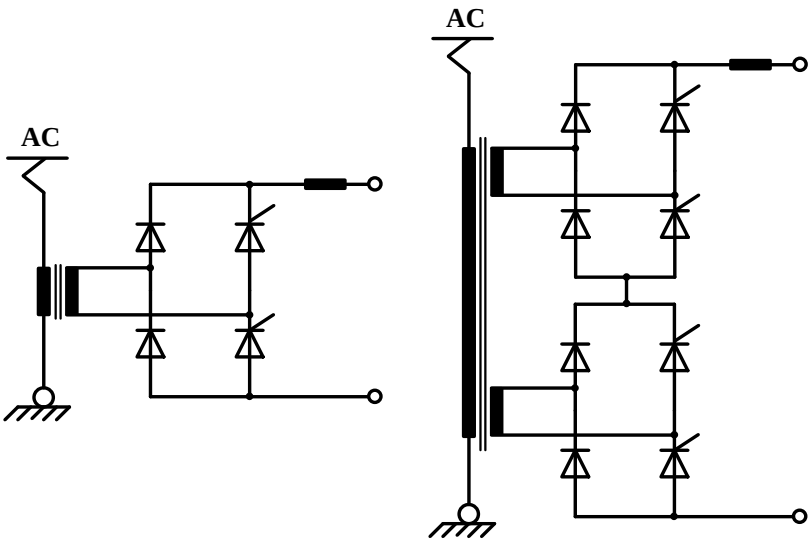


Figure 1.13: Classification of High Power Rectifiers [34]

First type of rectifiers developed in power electronics technology was diode bridge rectifiers. They have the disadvantages of uncontrollable output voltage, poor power factor and bad harmonic content. Then, phase angle controlled rectifiers came into use employing thyristors by which the regulation of DC output voltage is possible. However, power factor and harmonic content are still poor. When singly utilized, line commutated rectifiers are non-regenerative converters as they do not have the ability to operate with bidirectional active power flow [35]. Line commutated rectifiers with thyristors were mostly used in DC motor drive traction applications with half-controlled configuration (Figure 1.14-a). Series connection of two half controlled rectifiers (Figure 1.14-b) was also used to improve the power quality [26, 36]. Poor harmonic quality, especially the presence of low order harmonics increase the Root Mean Square (RMS) of the line current drawn from the AC catenary which yields higher losses, distorted supply voltage affecting other loads connected to the same Point of Common Coupling (PCC) [37]. With the advance in power semiconductor technology, active topologies came into use with higher switching frequency and thus better harmonic content [38].



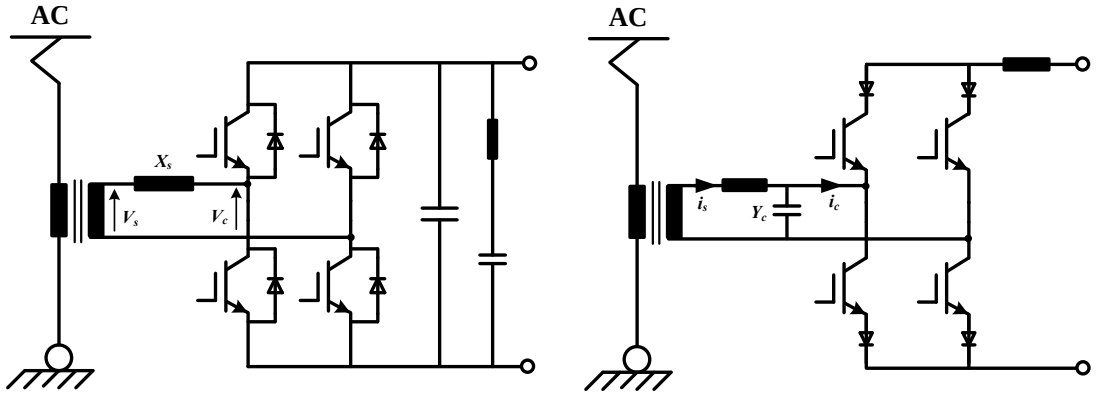
(a) (b)

Figure 1.14: Line Commutated Rectifiers Used in Traction Applications:
a) Single Half-Controlled Rectifier
b) Series Connected Half-Controlled Rectifiers

The second type of rectifiers can be further classified as regenerative and non-regenerative rectifiers. In modern locomotive traction systems, non-regenerative rectifiers are not preferred and generally regenerative type PWM converters; voltage source rectifiers (VSR) or current source rectifiers (CSR) are used. They are often called as four quadrant (4Q) converters [39, 40] due to their ability to operate in all four quadrants of the V-I plane. Moreover, they are also called as active front-end rectifiers or PWM rectifiers. Advantages of 4Q converters over other types are as follows [1, 34, 35, and 41]:

- They are fully regenerative.
- They can operate at unity power factor.
- Harmonic content of the line current is low.
- They have good dynamic performance.
- It is possible to supply reactive power to regulate the AC line voltage.

PWM Rectifier idea was first proposed in 1972 and as of now, the traction converter technology depends on it [42]. VSRs and CSRs are both active PWM converters and drive principles and control strategies are similar [34, 43]. The configuration of VSR and CSR are shown in Figure 1.15 [44].



(a) (b)

Figure 1.15: Configuration of (a) VSR and (b) CSR

VSRs operate in boost mode so that the DC output voltage is always higher than the peak value of the AC input voltage. Actually, a ratio around 30 % is common to use in AC line locomotive applications [44]. On the other hand, CSRs are developed from buck converters and are capable of providing a DC output voltage lower than the peak value of the AC input voltage. CSR topology was common for DC traction applications since regulation of DC link voltage in a wide range is possible. When three phase AC induction motors came into use with inverter drive configuration, VSR topology became a better solution for constant and higher DC link voltage operation [44].

As seen in Figure 15, the filter configuration reverses for voltage source converters (VSC) and current source converters (CSC), i.e. the series inductor becomes shunt capacitor and vice versa. The series inductor in CSR configuration is present to obtain a current source input from the AC catenary [44]. Although operation principle is similar, for VSRs, power factor is controlled by the voltage drop on the series inductor,

where it is controlled by the current sink on the shunt capacitor for CSRs [45, 46]. The active power flow at the supply terminals for VSRs and CSRs are as shown in Equations 1.1 and 1.2, respectively, where δ is the angle between supply voltage and the fundamental component of converter output voltage (load angle) and φ is the angle between supply current and fundamental component of the converter input current (phase angle) [44].

$$P_s = \frac{V_s V_c}{X_s} \sin(\delta) \tag{1.1}$$

$$P_s = \frac{I_s I_c}{Y_s} \sin(\varphi) \tag{1.2}$$

The series LC filter seen on the voltage source type topology is a resonant type filter (band-pass filter) and present to eliminate the second harmonic component on the DC link occurring due to the nature of the unity power factor operation of the PWM rectifier [47, 48 and 49]. Considering an ideal lossless system, the equality of AC input power which is the multiplication of RMS values of fundamental components of input voltage and current at unity power factor and DC output power yields a DC component and a second harmonic component, the peak value of which is equal to the DC value at the output voltage. If this second harmonic component is not filtered out properly, it is going to not the only disturb the proper operation of the traction inverter, but also cause odd numbered low order harmonics at the AC side. Furthermore, it will cause the beat phenomenon resulting in torque pulsations and mechanical vibrations [50]. The most common method to eliminate this harmonic is to use a passive LC filter tuned to 100 Hz (for 50 Hz AC catenary systems) on the DC link which is actually a bulky solution [51, 52]. There are also other methods proposed to overcome this problem without using a passive filter. These methods mostly include software solutions which reduce the adverse effects of the second harmonic component on the DC link voltage rather than eliminating it [50, 53].

The operation principles of VSR PWM rectifier topology will be further investigated in Chapter 3. In AC main line locomotive traction systems, there are a variety of voltage source type PWM rectifier topologies that have been utilized so far. The most common ones are [54]:

- Two-Level 4Q PWM Rectifier
- Three-Level 4Q PWM Rectifier
- Series Connected Multilevel PWM Rectifier
- Interleaved Two-Level PWM Rectifier

Two-level 4Q converter is the simplest and most commonly used topology in locomotive traction applications. Its simple layout and control makes it an attractive choice for topology selection [55].

Three level 4Q converter emerged from the need operate at higher DC link voltages when the blocking voltage capability of power semiconductor devices is not sufficient [22, 55, 56, 57, 58, and 59]. The most common three level 4Q converter configuration is the Neutral Point Clamped (NPC) converter and there is also another configuration called Flying Capacitor (FLC) converter which is not commonly used in traction applications [54]. Obviously, the output voltage harmonic content is better than of two-level type; however, it has demerits such as, higher component count leading to a more costly design, complex control due to the requirement of DC link voltage balancing [60, 61, and 62] and being less reliable as there are more short-circuit paths than two-level counterpart in case of a failure [63].

Series connected multilevel 4Q converter is similar to the NPC type, whereas the DC links are separated. The idea behind this topology is to eliminate the bulky front-end traction transformer, which is a step-down transformer reducing the 25kV AC catenary voltage to low voltage levels (~ 1kV), by using sufficient number of series connected converters to operate at catenary voltage. It is not a commonly preferred topology because of high component counts and very low reliability. The traction transformer contributes to the system with usage as an AC line filter and providing better adhesion to prevent slippage due to its heavy weight [64, 65 and 66].

The series connected multilevel converter topology is used along with a medium frequency transformer (MFT) configuration which is often called power electronics transformer (PET). The idea is to eliminate the bulky front-end transformer, which is a low frequency transformer (LFT), operating at 50 Hz and replace it with a

transformer with less volume and weight, operating at a higher frequency (generally over 2 kHz) [67]. For locomotives, weight of the input transformer is not a big concern; however, for EMUs the weight of each vehicle employing motor drive system is critical. The number of H-bridge modules connected in series is determined by the AC catenary voltage level and the blocking voltage capabilities of the chosen power semiconductor devices [68]. This topology is not commonly used in AC line locomotive traction systems as it requires much more components increasing the cost of the traction system. A special transformer design with multiple primary windings is also required. In addition, reliability of such a topology is questionable as there seems to be a total of more than 40 H-bridge modules connected in series in every prototype developed so far [69]. This topology especially becomes feasible in 15 kV 16.7 Hz catenary systems due to the very low system frequency [18].

Interleaved 4Q two-level converter is the most commonly utilized topology for locomotive traction applications due to its advantages of better redundancy, reduced current rating of power semiconductor devices, perfect harmonic content reducing the filter requirements on the AC side [41, 56]. The topology is quite simple such that, two two-level 4Q converters are connected in parallel on a common DC link and fed by distinct secondary windings of the input transformer. The two converters are operated in a phase shifted manner such that the first harmonic group appearing around the switching frequency become out of phase to each other being cancelled out at the primary side of the transformer. Hence, the center frequency of the first harmonic group is doubled with less magnitude. Due to the increase on the effective switching frequency, applied switching frequency can be reduced which yields lower semiconductor losses and hence higher converter efficiency. The disadvantages of this topology are requirement of multiple transformer secondary windings, more complex modulation strategy and more component count requirements [58, 70].

1.4. Control Methods

The main tasks of the control system for the rectifier stage of an AC main line locomotive traction system are providing a constant DC link voltage at steady state, keeping the power factor at the AC supply terminals at unity, synthesizing an AC input current waveform having Total Demand Distortion (TDD) and individual harmonics below the limits stated in IEEE Std. 519-1992 [33], with good transient performance and good disturbance rejection [58, 71 and 72]. The system should also operate having all the capabilities listed above during regenerative braking operating mode.

The control system of a PWM rectifier with its simplest form (two-level topology) is composed of three loops; phase locked loop, outer voltage loop and inner current loop [71]. The phase locked loop (PLL) is responsible for obtaining the phase information of the AC catenary line voltage where the rectifier is connected to. It is a critical control component for unity pf operation. The task of the outer voltage loop is to keep the DC link voltage at a desired level in all modes of operation. The inner current loop controls the AC current input of the rectifier utilizing the phase information coming from PLL and the DC current information coming from the voltage loop. This is why it is called the inner loop [72].

PLL configurations of three phase systems mostly apply reference frame transformation (from stationary reference frame to synchronously rotating reference frame) to the three phase voltages to extract the phase information. It is not possible to apply this method to single phase systems as in AC locomotive traction systems directly since there is only one phase.

Most single phase PLL methods apply phase delay to the single phase voltage to obtain an imaginary phase orthogonal to the original phase. This method has poor dynamic performance. Another method is notch filter. PLL with Orthogonal Signal Generators (OSG) is the best method and implemented in this research work.

The voltage control loop usually consists of a Proportional Integral (PI) controller. To prevent the reflection of the second harmonic component present on the DC link voltage to avoid fluctuations, notch filters tuned to 100 Hz are used [51, 73].

The current control method is usually based on linear current regulators with sinusoidal waveform tracking. Almost all AC locomotive traction systems are dependent on this method due to its superior dynamic performance. Utilization of PI controller on this loop yields steady state error on the phase of the current waveform resulting in poor power factor values. To overcome this drawback, Proportional Resonant (PR) controllers may be used [74, 75]. PR controllers tuned to the grid frequency yields no steady state error providing operation at unity pf successfully. Although infinite gain is applied to this frequency component theoretically, due to the instability problems emerging from the infinite gain, a practical PR controller is derived and used in practical applications [76, 77].

Rather than controlling the current waveform instantly, it is also possible to control the input current as DC quantities on synchronously rotating reference frame with the application of Direct-Quadrature-Zero (DQ0) transformation which is the power invariant version of Park's Transformation [57, 78 and 79]. Here, D represents the real component (active power) and Q represents the imaginary component (reactive power) in terms of the catenary voltage. Hence unity pf operation can be achieved with independent control of two orthogonal variables [80, 81]. The major drawbacks of this type of current control mechanism are the requirement of orthogonal phase generation since the system is single phase and the slower response compared to linear current control method [82].

Alternative types of current control methods can also be derived suitable for constant DC link Voltage operation including direct control of reactive power. Such methods has not yet been proven worthy in AC locomotive PWM rectifiers [83].

At the output of the whole control system, the AC catenary voltage is usually added to the modulating signal as a feedforward to elevate the dynamic performance of the system and to take the disturbances caused by the AC catenary line into account [58, 84].

1.5. Pulse Width Modulation Methods

Pulse Width Modulation (PWM) technique is the heart of any power electronics converter system. As the name suggests, PWM Rectifiers are dependent on this technique. Sinusoidal current waveform synthesizing is achieved via PWM technique. PWM signals are pulse trains with fixed frequency and magnitude and changing pulse width [85]. The pulse width is determined in each switching cycle by the modulating signal calculated in the control loops beforehand. When designing a PWM power converter, one must consider the following [85]:

- Good utilization of DC link voltage should be achieved.
- Linearity should be achieved in the whole operating range.
- Harmonic content of the synthesized waveform should meet the requirements dictated by the standards.
- Switching loss of the semiconductor devices should be below the specified limit.

Sinusoidal Pulse Width Modulation (SPWM) is the most common method used in single phase high power locomotive rectifier systems [86, 87]. With SPWM, AC waveforms can be synthesized with desired magnitude and fundamental frequency. The method is implemented by comparing the modulating signal by a carrier waveform (mostly in triangular shape). The frequency of the carrier waveform determines the frequency modulation index and hence the switching frequency of the converter. The amplitude of the modulating waveform determines the amplitude modulation index and hence the RMS value of the output voltage waveform.

SPWM method still remains the most preferred PWM method in single phase PWM rectifiers due to its simplicity of implementation and control, compatibility with today's microprocessor technology and good harmonic distortion performance [88]. With SPWM technique, no low order harmonics appear theoretically with a frequency modulation index higher than 10. Today's microprocessor technology is convenient for SPWM application. Digital Signal Controllers (DSC) equipped with Digital Signal Processors (DSP) is especially suitable as they have Enhanced Pulse Width Modulation (ePWM) modules dedicated to such implementations [7, 89].

For single phase PWM rectifiers, since the converter is voltage source type, two complementary PWM signals are used for one bridge arm operating in dual mode; i.e. one power switch is OFF when the other is ON and vice versa. An appropriate dead band is used to avoid short circuit failures of the DC link [89]. Linearity is also important for SPWM applications. The region where amplitude modulation index is less than 1 is called the liner modulation region where the magnitude of the output voltage changes linearly with modulation index. For modulation indexes higher than 1, the region is called over-modulation region where there is a nonlinear relation between output voltage and modulation index and low order harmonics would appear.

SPWM techniques can be applied in two ways; unipolar SPWM and bipolar SPWM [90]. Unipolar SPWM utilizes three different levels of the DC link voltage at the output where bipolar SPWM utilizes only two levels. With unipolar SPWM, the center frequency of the first harmonic group appears at twice the switching frequency. On the other hand, with bipolar SPWM, it appears at the switching frequency. Thus, unipolar SPWM is more advantageous in terms of harmonic content. Unipolar SPWM uses two carrier signals out of phase with each other or two modulating signals out of phase with each other while bipolar SPWM is simpler, only one carrier wave and one modulating wave is enough.

The superiority of interleaved PWM rectifier topology stems from phase shifted SPWM technique [22, 91]. The two converters which are connected in parallel on the DC link are operated in a phase shifted manner by which the center frequency of the first harmonic group at the primary side of the traction transformer is doubled. Switching frequency harmonics of each individual converter cancels each other due to phase shifting. Therefore, with phase shifted and unipolar SPWM technique, the frequency mentioned above is four times the switching frequency and the magnitude of the harmonic components around this frequency will be four times less than the original harmonics. Total Harmonic Distortion (THD) of the AC line current is therefore much less than ones in individual converters. Phase shifted SPWM technique eliminates the necessity of harmonic reduction solution that requires additional hardware like phase-shifting transformers [91].

1.6. Scope of the Thesis

In this research work, it is aimed at designing an interleaved PWM rectifier for AC locomotive traction applications and to implement its low voltage laboratory prototype. The rectifier system has the abilities of operating at unity power factor, bidirectional operation allowing regenerative braking, good input current harmonic distortion performance and sufficient dynamic performance.

Main line locomotive traction systems have been researched carefully and the main focus is given to the PWM rectifier topologies and their comparison. Interleaved two-level PWM rectifier topology is chosen for its superior features such as redundancy, best TDD performance in line current and reduction on the power semiconductor current ratings. Control techniques and PWM techniques used in locomotive traction systems have been investigated and evaluated. Linear current regulator is the most preferred method in PWM Rectifiers of main line locomotive traction applications and its application with both PI and PR current controllers are exercised.

Design of the system is achieved by theoretical calculations as well as computer simulations carried out on MATLAB/Simulink environment. The switching frequency of the rectifier is selected as 500 Hz to minimize the switching loss of the IGBTs and with such a low switching frequency, harmonic distortion standards defined for the line current have been satisfied thanks to phase shifted PWM operation. Design of passive elements has also been carried out by considering their effects on line current TDD, DC link voltage ripple and efficiency of the converter. Parameters of the control are designed by using basic tools of control theory such as transient performance analysis in time domain, root locus method for stability and frequency response method.

The designed PWM Rectifier for use in a locomotive with 5 MW output power is simulated in MATLAB/Simulink to verify its performance. Fundamental requirements of the PWM rectifier are satisfied including unity pf and constant DC link voltage operation, compliance with the IEEE Std. 519-1992 with a TDD below 5 %, regenerative braking operation with similar performance and acceptable dynamic performance.

The theoretical and simulated findings are verified by experimental work carried out on a low voltage prototype which is composed of the designed PWM rectifier, a motor drive system and a universal machine set consisting of a three phase squirrel cage asynchronous machine, a DC machine and a flywheel present to simulate the inertia of the traction vehicle. The experimental results reveal that the prototype system operates successfully, satisfying the operation requirements.

The outline of the thesis is given below:

In Chapter 2, main line locomotive traction systems are investigated in terms of their load characteristics and motor drive strategies. Analysis of PWM rectifier topologies is elaborated. The topologies are investigated via computer simulations and compared in terms of several constraints like size and cost, efficiency, line current harmonic content etc.

In chapter 3, system description and operating principles of interleaved two-level PWM rectifier is investigated. Unity power factor operation is investigated and formulated. The motoring and regenerative braking operation modes are discussed along with control techniques and PWM techniques that have been used in PWM rectifiers of locomotive traction systems.

In chapter 4, design of the interleaved two-level PWM rectifier is presented including power semiconductor device selection, selection of switching frequency, AC Line filter design, DC link capacitor and LC resonant filter design, control system design and power loss analysis.

In Chapter 5, simulation results are presented including voltage and current waveforms on both AC line and DC link along with their harmonic spectrum, regenerative braking operation, transient performance of the system, performance of different current control methods and efficiency analysis.

In Chapter 6, the theoretical and simulation results are verified by experimental results obtained on a 3.5 kW laboratory prototype. Unity power factor operation is achieved at rated output power. In addition, the two converters which are interleaved are successfully operated with phase shifted PWM and satisfactory harmonic content on the line current is obtained. The developed PWM rectifier prototype is also tested with

the motor drive system during acceleration and deceleration and its transient performance is validated.

General conclusions are given in Chapter 7 along with further research possible on this subject in the future.

In Appendix A, characteristics of the selected power semiconductor module is presented.

In Appendix B, Simulink models employed in simulation work are shown.

In Appendix C, technical specifications of the developed low voltage prototype are introduced including front-end transformer, passive elements and the IGBT modules.

In Appendix D, discretization of the s domain transfer functions present on the control system is shown which have been utilized for software implementation of the prototype system.

In Appendix E, flowcharts of the control software implemented on DSP microcontroller are presented.

In Appendix F, Control PCB schematics and layout are presented.

In Appendix G, list of the components used for the hardware implementation is given.

In Appendix H, equipment used during laboratory tests are listed.

CHAPTER 2

MAIN LINE LOCOMOTIVE TRACTION SYSTEMS AND PWM RECTIFIER TOPOLOGIES

In this chapter, the main line locomotive traction systems will be investigated. The load characteristics of a locomotive will be analyzed and contemporary motor drive strategies applied to locomotive traction motors will be discussed. Furthermore, PWM rectifier topologies will be analyzed in a detailed manner. Presentation of each topology is supported not only by literature research but also by open loop simulations performed on MATLAB/Simulink simulation environment. Finally, comparison of the PWM rectifier topologies will be introduced and topology selection for the designed PWM rectifier will be made.

2.1. Main Line Locomotive Traction Systems

The load characteristics of electric railway traction systems differ from conventional drives. First of all, the inertia of the load is much higher (up to 20 times) than the inertia of the motor in transportation loads. In addition, main line electric locomotives generally employ a gear-box system to increase the force at the wheels. Therefore, traction motors rotate at higher speeds than the wheels. Railway electric vehicles can physically operate in both linear directions. Switching from one direction to the other can only be applied when the vehicle is stationary. The switching of vehicle direction can be achieved by reversing the polarity of either armature or field terminals when

DC traction motors are used and by reversing the phase sequence of the traction inverter when AC traction motors are used.

Railway traction systems can produce torque in both directions (in terms of direction of speed). It is safe to say that, railway electric vehicles can be operated in four quadrants of the torque speed plane as shown in Figure 2.1.

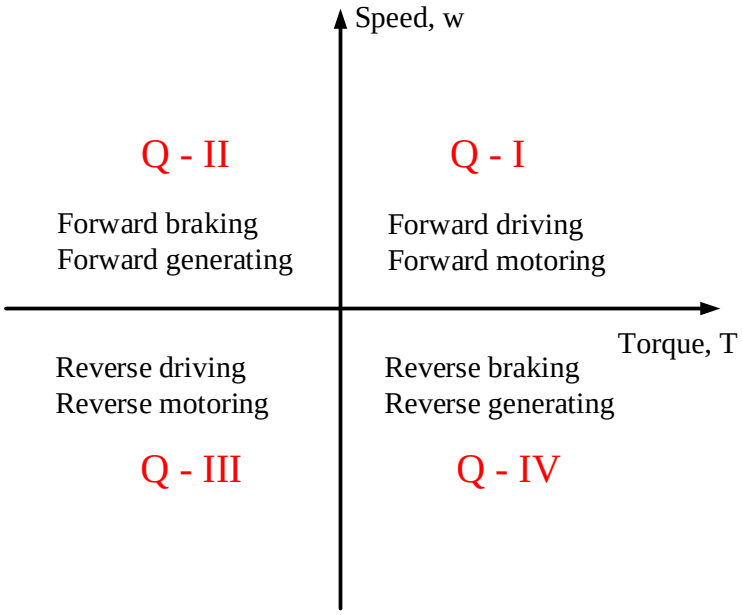


Figure 2.1: Operation of Railway Vehicles in Four Quadrants of the Torque-Speed Plane

Motor drives of railway transportation systems are usually denoted as four quadrant (4Q) drives in the literature [49]. Essentially, such motor drive systems are able to operate in two of the quadrants (2Q) of the plane shown in Figure 2.1 at the same time (forward driving/forward braking or reverse driving/reverse braking). The vehicle can switch between the 2Q's by changing its direction of linear motion.

A load characteristic of a railway vehicle is shown in Figure 2.2 only in one direction of the vehicle [92]. Characteristics for the reverse direction can be easily obtained by taking the symmetry in terms of torque axis. All quantities in Figure 2.2 are defined on load side.

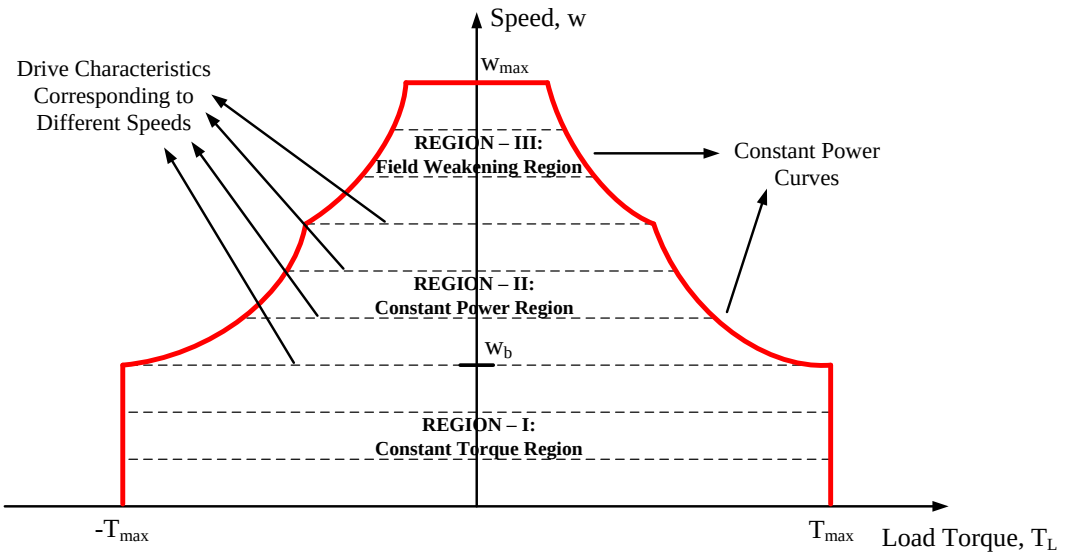


Figure 2.2: Load Characteristics of a Railway Vehicle
(only in one direction) [92]

As shown in Figure 2.2, there are three regions of operation in one quadrant: constant torque region (from zero speed to w_b), constant power region (from w_b to 2/3 of w_{max}) and reduced constant power region or field weakening region (from 2/3 of w_{max} to w_{max}) where w_b denotes the base speed which is restricted by the maximum output power of the vehicle and w_{max} denotes the maximum speed the vehicle can achieve. Drive characteristics can be defined separately for each speed as shown in Figure 2.2. T_{max} and $-T_{max}$ are the torque limits that can be achieved in motoring and braking modes of operation, respectively. The vehicle is usually preferred to accelerate at T_{max} and decelerate at $-T_{max}$ during constant torque regions.

A transportation load is composed of the following forces acting on the shaft of the traction motors as load torque:

1) **Friction Force:** This type of force occurs by the conversion of the mechanical energy to heat, between moving parts. Friction torque component is directly proportional to the speed itself.
2) **Windage Force:** This type of force occurs due to the movement of the vehicle in the air. It is also called Aerodynamic Drag Force and it is actually the force which limits the speed of the vehicle. It is independent of the mass of the

vehicle and depends on the shape (area against the air). Windage torque component is proportional to the square of the speed.

3) **Accelerating Force:** This type of force is the most dominant one during constant torque (acceleration and deceleration) regions.
4) **The Force Component Which Does the Mechanical Work:** This type of force is caused by the gravitational force when the vehicle travels on an inclined rail. The nominal output power of railway electric vehicles is generally determined by to this force. This force is independent of the speed of the vehicle and constant for any given slope.

In constant torque region, the most prominent load torque component is the accelerating torque. In constant power region, if the vehicle is on a level track, windage torque component is dominant.

2.1.1. Drive Strategies

As discussed formerly, three phase squirrel cage asynchronous traction motors are used in modern high power AC locomotives. Traction inverter is a voltage source type three phase inverter employing IGBTs as power switches. The virtue of asynchronous traction motors in transportation systems can be summarized as following [93]:

- High maximum speeds
- Robustness, reliability and low maintenance requirements
- Simple cooling system usage
- High power/weight ratio (power density)
- Low cost/power ratio
- Steep region of the torque-speed characteristics (operation in low slip)
- Limiting of the speed on synchronous speed when a wheel is slipping
- Being able to apply regenerative braking over synchronous speed
- Perfect transient performance

The voltage source traction inverter has variable voltage - variable frequency (VVVF) capability. Thus, asynchronous traction motors can be driven on a wide speed range with high speed control sensitivity. Rated voltage and rated frequency of the motor are determined by the rated magnetic flux density on the core which is limited by magnetic saturation. This phenomena stems from the famous formula of induced voltage of an induction motor as shown in (2.1). In order to achieve constant flux density operation (neglecting the voltage drop on the stator windings), constant V/f ratio should be established as seen in (2.2) where K is a constant for a given physical structure of the machine.

$$E = 4.44\, N f k_w B A \tag{2.1}$$

$$B = K\,\frac{V}{f} \tag{2.2}$$

The asynchronous motor torque-speed characteristics and the variation of mechanical and electrical quantities during all operating regions are shown in Figure 2.3 [93]. During acceleration and deceleration (in constant torque region), the voltage applied by the inverter is varied according to the applied frequency keeping the flux constant. In level track (constant power region), the applied voltage is kept constant while the frequency is increased so that the flux will decrease and so does the electromechanical torque. For higher speeds, the maximum electromechanical torque which can be produced by the traction motor further reduces due to the increase in the stator reactance with higher applied frequency.

For VVVF operation of the traction motor explained above, there exist two types of control mechanisms: scalar control and vector control [93]. Main features of scalar control are as follows:

- It is easy to design and implement.
- For low speeds, its transient performance is not good. To overcome this, voltage boost can be applied.
- It is not possible to keep the flux/pole fully constant since the induced voltage on the stator is not equal to the stator terminal voltage in practice.

- It is the only possible method when more than one traction motor is to be supplied by the same inverter.

Main features of vector control can also be listed as follows:

- It is possible to control flux and torque independently.
- When this type of control is applied, all traction motors should be supplied by their own inverter.
- It has better dynamic performance.
- It is more complex to design and more expensive to implement.

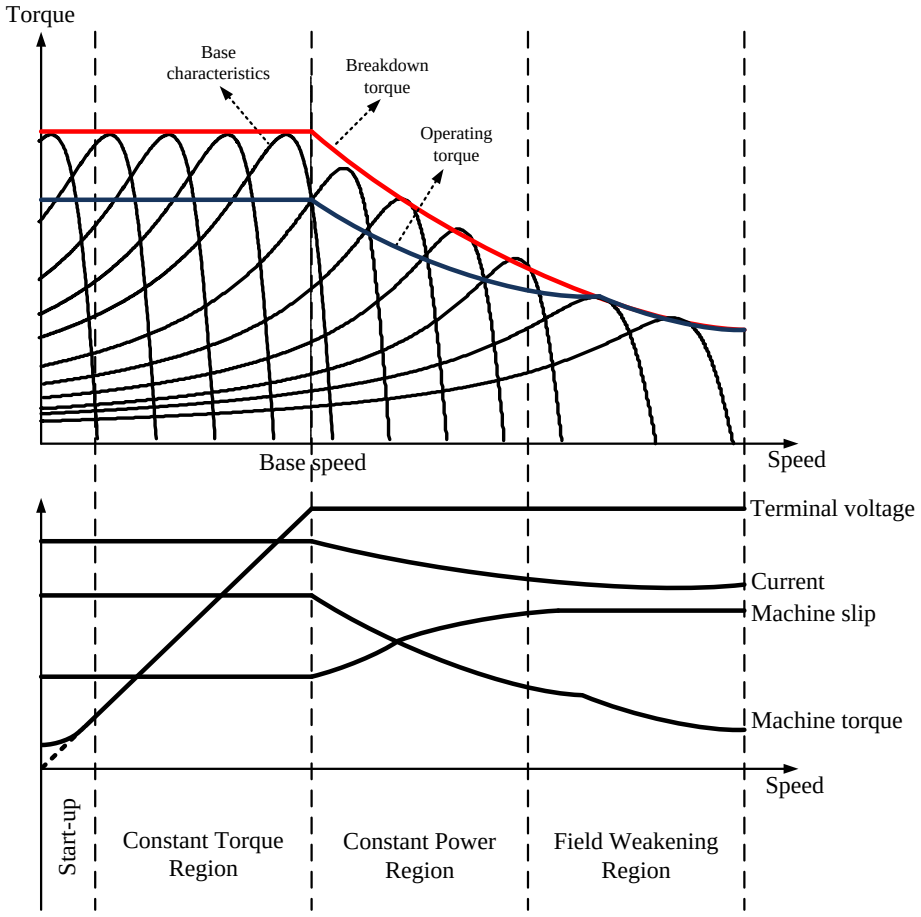


Figure 2.3: Asynchronous Motor Torque-Speed Characteristics and Variation of Electrical Quantities [93]

2.1.2. Power Quality Issues

As discussed in Chapter 1, PWM rectifiers or 4Q rectifiers are on the leading edge technology for the catenary side of the locomotive traction systems. During the design phase of traction system rectifiers, the most significant constraint which must be considered is power quality. High power loads holds great importance for AC grid due to the fact that their adverse effects on the supply grid are much more severe. One major concern for power quality compliance is reactive power generation which leads to increase on the RMS value of the line current leading to increase in the loss. Therefore, unity power factor operation is required for railway traction vehicles. Another main power quality term which matters for locomotive traction systems the most is waveform distortion. Power system should be able to maintain a nearly sinusoidal supply voltage in an uninterrupted manner. Any harmonic injected to the interconnected grid system contributes to the distortion of supply voltage and therefore, there exists power quality standards defining the limits of harmonics injected by a grid-connected system published by Institute of Electrical and Electronics Engineering (IEEE). Current harmonic distortion limits for general distribution systems (from 120V through 69kV) defined in Std. 519-1992 is shown in Table 2.1 [33]. In addition to disrupting the grid voltage, other effects of current harmonics injected to the AC grid by the locomotive traction system can be summarized as following [22, 94]:

- Harmonics injected to the AC catenary line may disrupt the railway signalization system.
- Harmonic currents cause noise on the front-end transformer which is not desired especially for distributed traction systems; i.e. EMUs.
- Harmonic currents lead to additional losses on the traction transformer and therefore, increase in the operation temperature. This will also aggravate cooling requirements.
- Voltage of the auxiliary converters which are present for the operation of low voltage equipment (lighting, monitoring etc.) be distorted due to the coupling between auxiliary transformer and main transformer.

Table 2.1: Harmonic Distortion Limits for General Distribution Systems Defined in IEEE Std. 519-1992 [33]

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h	TDD
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of odd harmonic limits above.						
Current distortion that results in a DC offset; e.g., half-wave converters are not allowed.						
All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L						
where I_{sc} = maximum short circuit current at PCC. I_L = maximum demand load current (fundamental frequency component) at PCC						

2.1.3. General Structure of PWM Rectifiers

Rectifier stage of a main line locomotive traction system employing 4Q front-end converter can be represented as in Figure 2.4. The *PWM Rectifier* block may be replaced by several topologies.

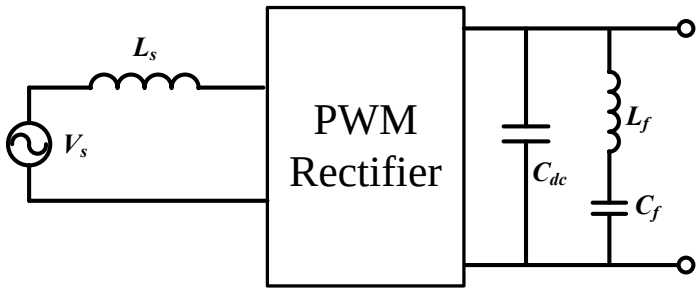
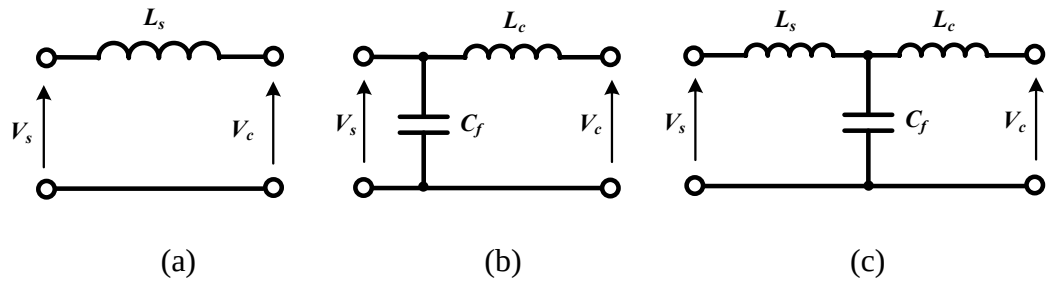


Figure 2.4: Block Diagram of Main Line Locomotive Rectifier Stage

The switching frequency applied to PWM rectifiers of locomotives is relatively low compared to conventional drives (generally 800 Hz maximum). The most apparent reason for this is to reduce switching losses of the converter. Theoretically, IGBTs can be operated up to 5 kHz; however, to obtain switching loss rates close to conduction loss, switching frequency is usually restricted up to 1 kHz for MW range power converters. Another impact of high switching frequency is the increase on the cooling requirement. A question may arise immediately; will the converter be able to comply with harmonic standards with such low switching frequencies without utilizing very bulky filters? The answer is yes. Since TDD is our interest and demand is relatively high in this application, acceptable harmonic distortion can be achieved without using extraordinary AC filters.

As shown in Figure 2.4, there exist three filters which are; AC line inductor, DC link capacitor and DC link series LC filter. In fact, there are three possibilities which may be utilized on the AC side: L filter, LC filter and LCL filter configurations of which are shown in Figure 2.5. All these configurations have been widely used and tested in various power converter applications. Superiority of LC or LCL filters is simply better filtering performance with less expensive and smaller design. The capacitor in the filter configuration introduces an additional pole to the system so that the decay in the frequency response is more drastic. On the other hand, they offer a more complex design. Rule of thumb resonant frequency calculation for LCL filters shows that the resonance frequency should be higher than ten times the grid frequency and lower than one half of the switching frequency to avoid resonance problems. Considering 50 Hz grid and a maximum of 1 kHz switching frequency selection, it is in fact impossible to design such a filter for this specific application. There is also an issue of damping requirement to prevent instability. Although LCL filter offers excellent filtering performance over resonance frequency, the gain is theoretically infinite at resonance frequency and it must be damped carefully. Passive damping which is simply implemented by adding resistors to the filter components interpolates additional losses and active damping increases the complexity of the control system and requires additional sensors [95].



(a) (b) (c)

Figure 2.5: Configuration of: (a) L Filter, (b) LC Filter, (c) LCL Filter

As it is understood, L filter is usually preferred for main line locomotive traction system PWM rectifiers. Design of this component for this particular research work will be presented in Chapter 4; however, a few aspects should be pointed out in advance. The trade-offs for AC line filter inductance design could be summarized as below:

- Higher line inductance values yield lower current harmonic distortion for the same switching frequency.
- Lower inductance leads to higher switching frequency requirement to comply with line current harmonic distortion standards and hence higher switching losses and cooling requirements.
- Dynamic response of the system gets slower as line inductance increases.
- Very low inductance values may cause controllability and stability problems as the system control range is highly dependent on this parameter.
- Higher line inductance values yield more bulky filters which makes the design much more expensive for high power applications.

The DC link capacitor design should also be carried out by taking a few constraints into account. First of all, DC link voltage ripple is directly affected by this capacitor value. A higher capacitance will perform better filtering reducing the higher order DC link voltage harmonics and hence reducing the voltage ripple. On the other hand, similar to the case of line inductance, dynamic performance of the DC link voltage control loop will worsen with higher capacitance values. In fact, this is not the most critical issue for capacitor selection because DC link voltage control loop is to be

much slower than the inner AC current loop. The most significant constraint which restricts the DC link capacitance is volume. DC link filter capacitors are the bulkiest elements of the overall PWM rectifier system. Other than capacitance value, voltage rating, ripple current rating capability and operation temperature are also effective for capacitor selection. Usually, to obtain sufficient current ratings and acceptable operating temperatures, a number of capacitors are used in parallel. One other constraint affecting the DC link capacitor selection is the capability of DC link to maintain voltages in an acceptable operation range for a selected period of time (usually one full cycle of mains voltage) in the case of power failure. This constraint usually yields higher capacitance values than of the voltage ripple restriction.

To eliminate the second harmonic component present on the DC link, another passive filter is used in PWM rectifiers of locomotive traction systems which is a series LC resonant filter type tuned to exactly this harmonic component, namely 100 Hz. This harmonic component emerges by the transformer-like operation of PWM rectifiers with changing turns ratio. Time expressions of fundamental components of AC line voltage and line current can be seen in (2.3) and (2.4), respectively, $\widehat{Vs}$ and $\widehat{Is}$ being the peak values and f_s being the supply frequency which is ideally 50 Hz and φ being the phase angle. Therefore, AC power can be expressed as in (2.5) with the use of trigonometric identities where V_s and I_s are RMS values. If system dynamics and high order harmonics are neglected for simplicity, DC link capacitor is ineffective and hence, DC link power can also be expressed as in (2.6) where I_{dc} is DC link current which is pure DC. Considering a lossless system at steady state, neglecting the higher order harmonics on both AC and DC side, these powers should be equal as shown in (2.7) and (2.8). The resultant DC link voltage expression yields two components one being pure DC (V_{dc}) and the other being a sinusoidal component ($\widetilde{V_{dc}}$) at 100 Hz as seen in (2.9) [47, 48 and 49]. At unity power factor; i.e. φ is equal to zero, the value of DC link current and the ripple component becomes directly proportional to the fundamental component of AC line current at constant DC link voltage operation as shown in (2.10) where $f_r = 2f_s = 100$ Hz.

$$v_s = \widehat{V_s}\cos(2\pi f_s t) \tag{2.3}$$

$$i_s = \widehat{I_s}\cos(2\pi f_s t - \varphi) \tag{2.4}$$

$$P_s = V_s I_s[\cos(\varphi) + \cos(4\pi f_s t - \varphi)] \tag{2.5}$$

$$P_{dc} = I_{dc} v_{dc} \tag{2.6}$$

$$P_{dc} = P_s \tag{2.7}$$

$$I_{dc} v_{dc} = V_s I_s[\cos(\varphi) + \cos(4\pi f_s t - \varphi)] \tag{2.8}$$

$$v_{dc} = V_{dc} + \widetilde{V_{dc}} = \frac{V_s I_s}{I_{dc}}\cos(\varphi) + \frac{V_s I_s}{I_{dc}}\cos(4\pi f_s t - \varphi) \tag{2.9}$$

$$V_{dc} + \widetilde{V_{dc}} = \frac{V_s I_s}{I_{dc}} + \frac{V_s I_s}{I_{dc}}\cos(2\pi f_r t) \tag{2.10}$$

The design of passive elements, mentioned in this part of the thesis, for this research work will be achieved in detail in Chapter 4.

2.2. PWM Rectifier Topologies

The topology selection for PWM rectifier is basically the decision of how many levels the converter will be composed of, which is directly affected by DC link steady state voltage level and the semiconductor blocking voltage ratings. Two - Level Converter, which is a simple H-bridge, appears to be the simplest choice, as the traction system is single phase. On the other hand, several multilevel type converters have also been considered, analyzed and implemented until now some of which are Neutral Point Clamped (NPC) Multilevel Converter or Diode Clamped Multilevel Converter (DCMLC) and Flying Capacitor (FLC) Multilevel Converter which have been usually utilized in Three - Level Converter configuration. Another multilevel converter topology is realized by series connection of two - level H bridge converters which, in literature, is referred to as Series Connected Multilevel Converter. The two - level converter topology has also been used with interleaving which, in this work, will be

denoted as Interleaved Two - Level Converter topology. This configuration with interleaving has been of interest by many locomotive traction system manufacturers due to its promising features. In this part of this research work, these four topologies which have been selected and utilized in many previous work will be analyzed, discussed and compared.

2.2.1. Two - Level 4Q Converter

The circuit diagram of the basic two - level 4Q converter topology is shown in Figure 2.6 [55]. Two - level topology which is composed of a single H - bridge has a simple layout. The two - level name stems from the utilization of two distinct levels of DC link which can be denoted as $+V_{dc}$ and $-V_{dc}$ during modulation. Actually, the resultant converter output voltage waveform consists of three different levels when unipolar SPWM technique which is the most preferred modulation strategy is used.

Possible switching states and resultant voltage levels of a two - level 4Q converter are shown in Table 2.2 [55].

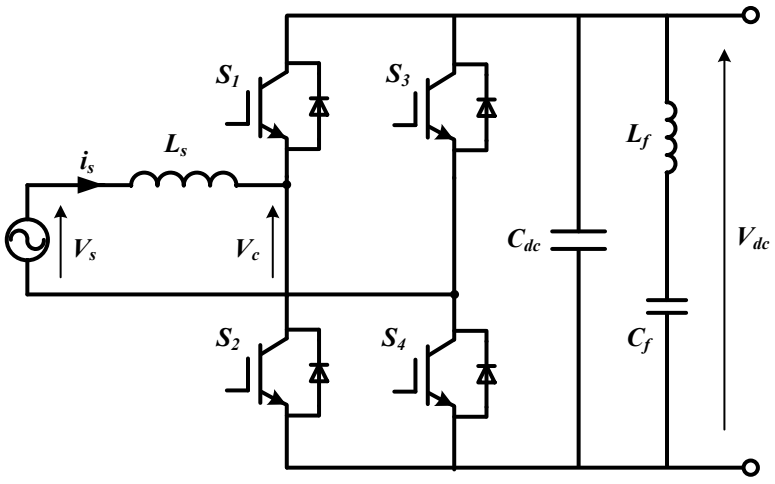


Figure 2.6: Circuit Diagram of Two - Level 4Q Converter Topology

A sample modulation in one fundamental cycle of the supply frequency is also illustrated in Figure 2.7, showing the modulating signal along with carrier signals, voltage of each converter leg and resultant converter output voltage waveform [34, 96]. The operation of two - level converter at unity pf, obtained by open loop computer simulations carried out in MATLAB/Simulink with 500 Hz switching frequency, 1 mH of AC line inductance and 1800V of DC link voltage is also shown in Figure 2.8 including supply voltage, converter output voltage and line current. Furthermore, harmonic spectrums of converter output voltage and line current are shown in Figures 2.9 and 2.10, respectively.

Table 2.2: Possible Switching States of Two - Level 4Q Converter

(S_x = 0 Switch Open, S_x = 1 Switch Closed)

State	**S_1**	**S_2**	**S_3**	**S_4**	**V_c**
1	0	1	0	1	0
2	0	1	1	0	$-V_{dc}$
3	1	0	0	1	$+V_{dc}$
4	1	0	1	0	0

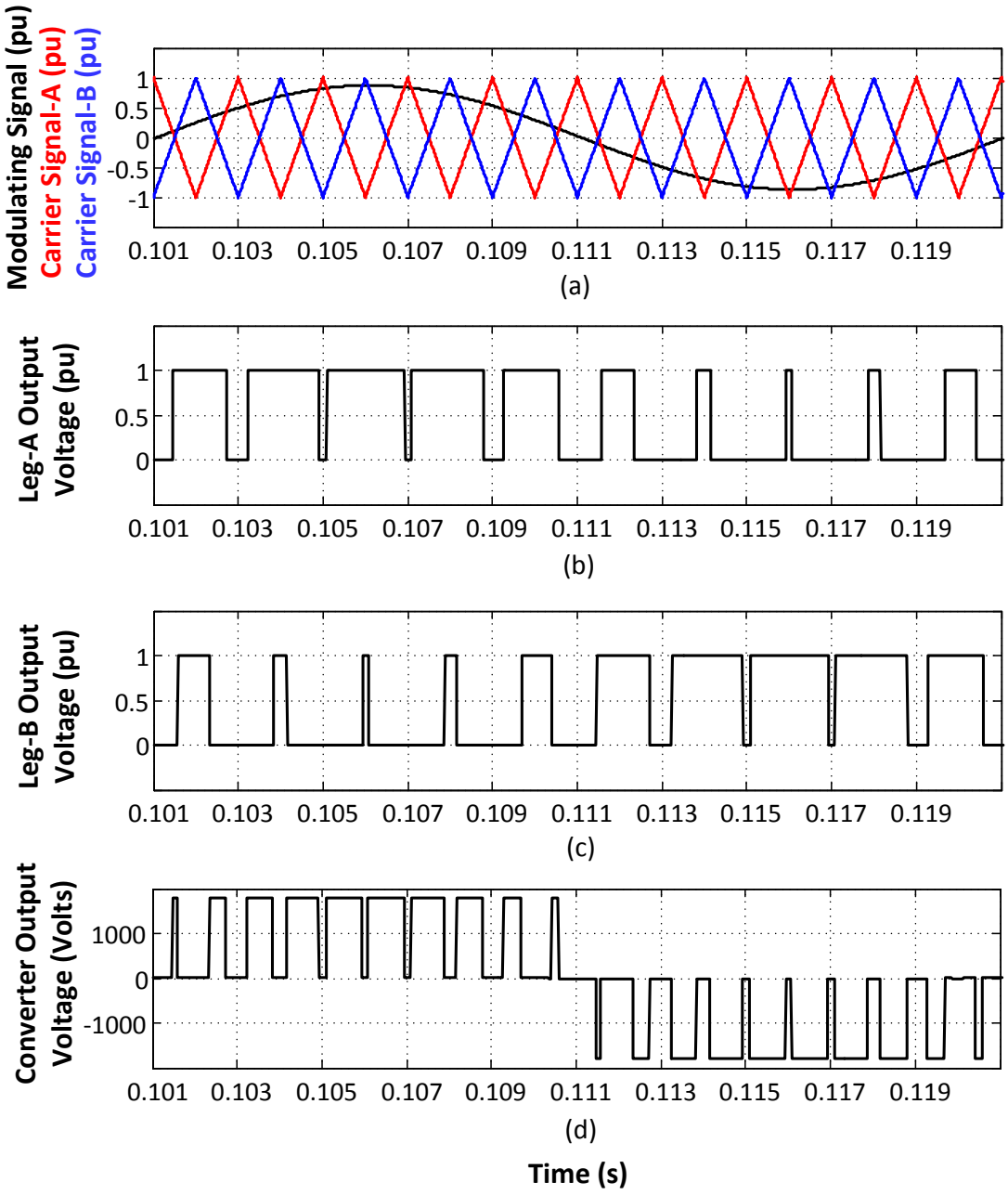


Figure 2.7: A Sample Modulation of Two - Level 4Q Converter:

(a) Modulating Signal and Carrier Signal, (b) Output Voltage of Leg-A

(c) Output Voltage of Leg-B, (d) Converter Output Voltage Waveform

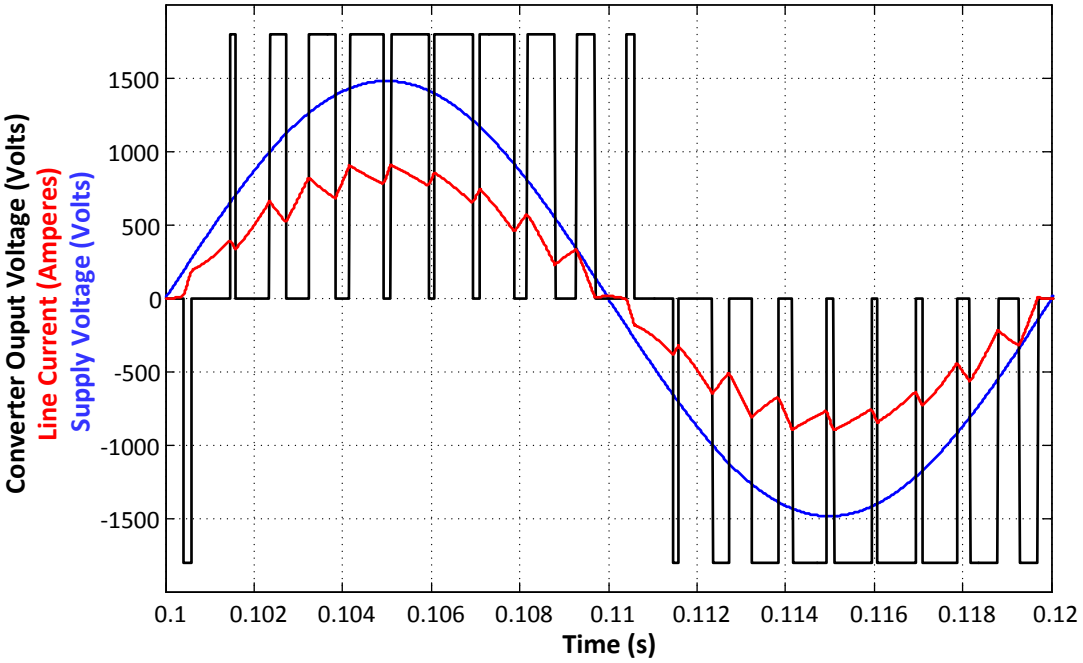


Figure 2.8: Unity pf Operation of Two - Level 4Q Converter:
(blue) Supply Voltage, (black) Converter Output Voltage, (red) Line Current

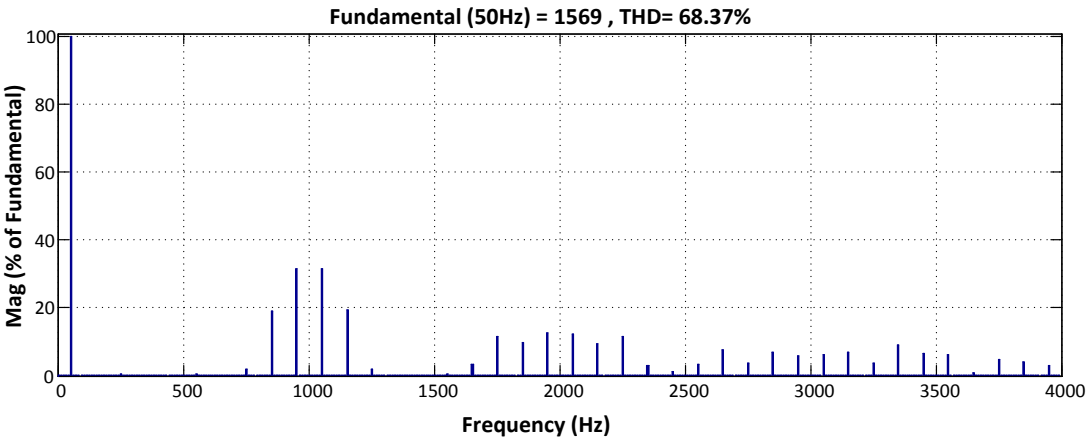


Figure 2.9: Harmonic Spectrum of Converter Output Voltage in a Two - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

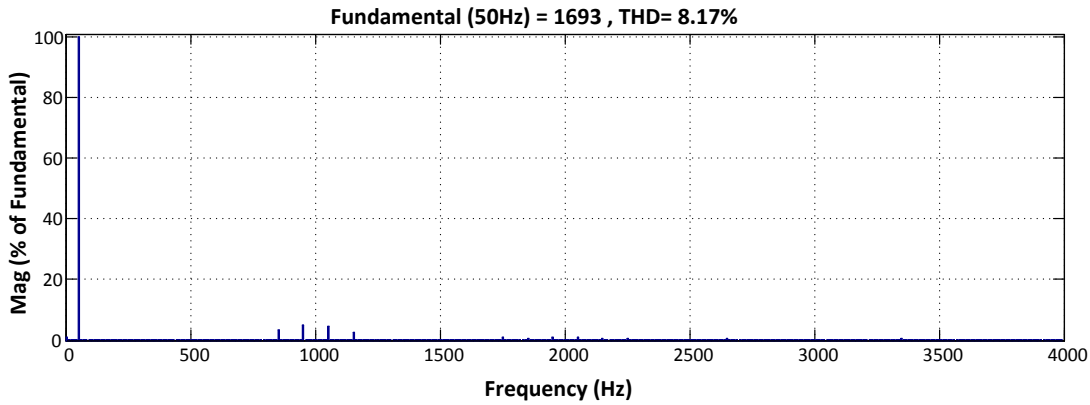


Figure 2.10: Harmonic Spectrum of Line Current in a Two - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

2.2.2. Three Level 4Q Converter

The circuit diagram of the three - level 4Q converter topology in NPC configuration is shown in Figure 2.11 [55, 58].

The three - level name stems from the utilization of three distinct levels of DC link which can be denoted as 0, $+V_{dc}/2$ and $-V_{dc}/2$ during modulation. As a matter of fact, the resultant converter output voltage waveform consists of five different levels. Due to multilevel configuration, power semiconductor blocking voltage requirement of three - level converter is half of two - level converter for equal DC link voltage [56, 57]. Possible switching states and resultant voltage levels of a three - level 4Q converter are shown in Table 2.3 [55].

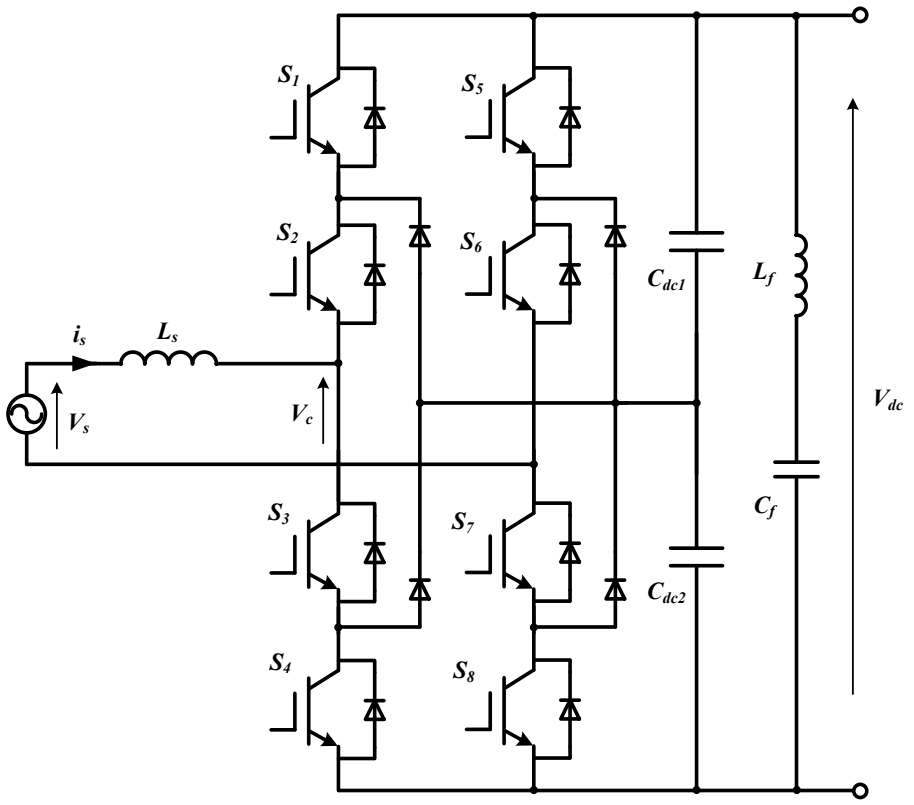


Figure 2.11: Circuit Diagram of Three - Level 4Q Converter Topology

Unipolar modulation applied to three - level converter is performed as follows [55]:

- A rectified modulating signal is compared to two out of phase carrier signals resulting in two pulse trains (pulse_a and pulse_b).
- A digital signal (sign) distinguishing the positive and negative half cycles is used to obtain the gate drive signals in each leg.
- Output voltage of each leg (v_a and v_b) can be expressed as in (2.11) and (2.12), respectively.
- The overall output voltage waveform (v_c) is the voltage difference between each leg as shown in (2.13).

$$v_a = (pulse_a \times sign) - (pulse_a \times sign') \quad (2.11)$$

$$v_b = (pulse_b \times sign') - (pulse_b \times sign) \quad (2.12)$$

$$v_c = (pulse_a + pulse_b) \times (sign - sign') \quad (2.13)$$

A sample modulation in one fundamental cycle of the supply frequency is illustrated in Figure 2.12 showing the rectified modulating signal along with carrier signals, pulse trains, digital signal, voltage of each converter leg and resultant converter output voltage waveform [58]. The operation of three - level converter at unity pf, obtained by open loop computer simulations carried out in MATLAB/Simulink with the same conditions used in two - level converters is also shown in Figure 2.13 including supply voltage, converter output voltage and line current. Furthermore, harmonic spectra of converter output voltage and line current are shown in Figures 2.14 and 2.15, respectively. It can be clearly seen from these harmonic spectra that harmonic distortion is lower than two - level converter under the same conditions.

Table 2.3: Possible Switching States of Three - Level 4Q Converter

(S_x = 0 Switch Open, S_x = 1 Switch Closed)

State	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**V_c**
1	0	0	1	1	0	0	1	1	$-V_{dc}$
2	0	0	1	1	0	1	1	0	$-V_{dc}/2$
3	0	0	1	1	1	0	0	1	invalid
4	0	0	1	1	1	1	0	0	0
5	0	1	1	0	0	0	1	1	$+V_{dc}/2$
6	0	1	1	0	0	1	1	0	0
7	0	1	1	0	1	0	0	1	invalid
8	0	1	1	0	1	1	0	0	$-V_{dc}/2$
9	1	0	0	1	0	0	1	1	invalid
10	1	0	0	1	0	1	1	0	invalid
11	1	0	0	1	1	0	0	1	invalid
12	1	1	0	1	1	1	0	0	invalid
13	1	1	0	0	0	0	1	1	0
14	1	1	0	0	0	1	1	0	$+V_{dc}/2$
15	1	1	0	0	1	0	0	1	invalid
16	1	1	0	0	1	1	0	0	$+V_{dc}$

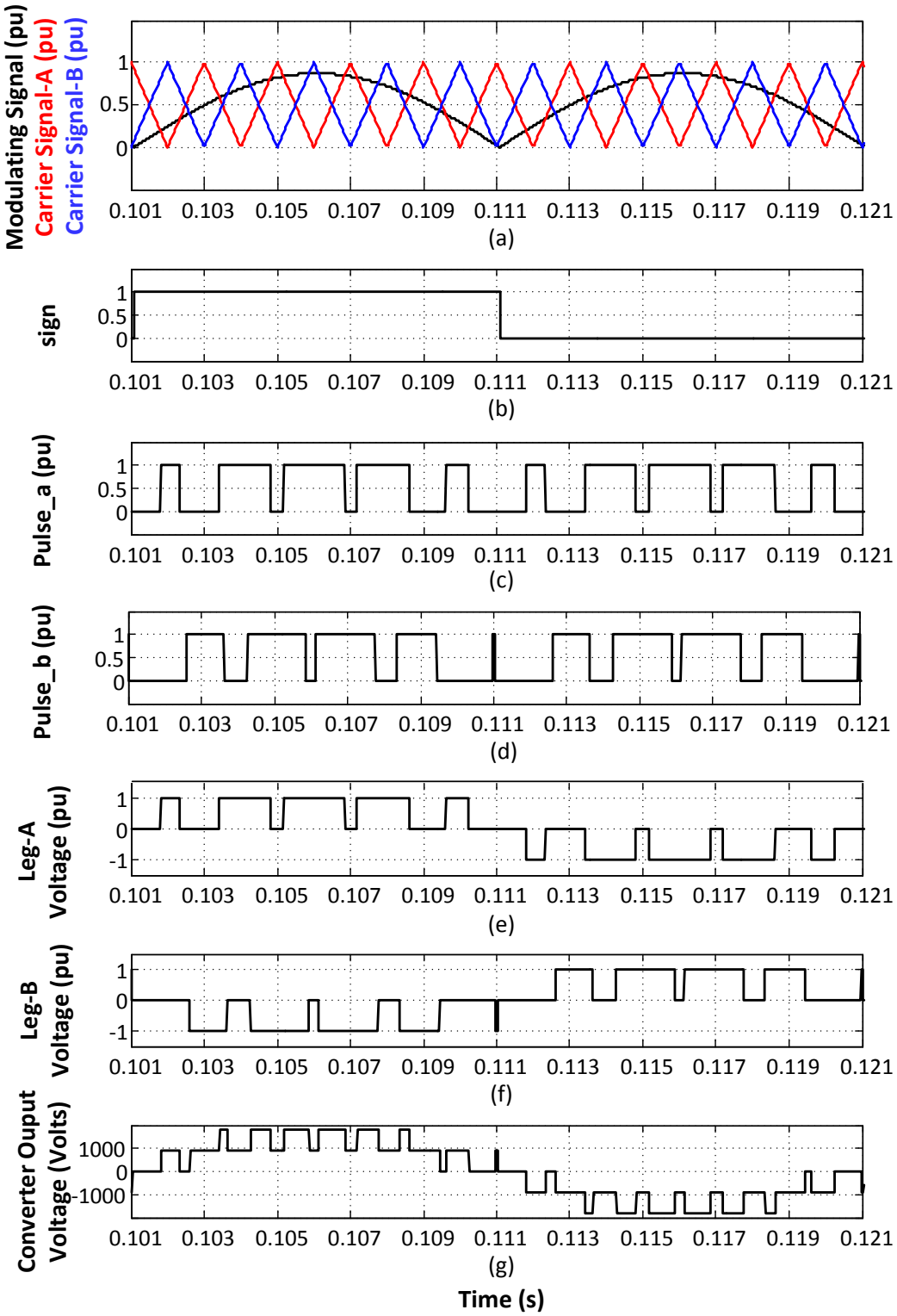


Figure 2.12: A Sample Modulation of Three - Level 4Q Converter:
(a) Rectified Modulating Signal and Carrier Signals, (b) sign, (c) pulse_a
(d) pulse_b, (e) Output Voltage of Leg-A (f) Output Voltage of Leg-B
(g) Converter Output Voltage Waveform

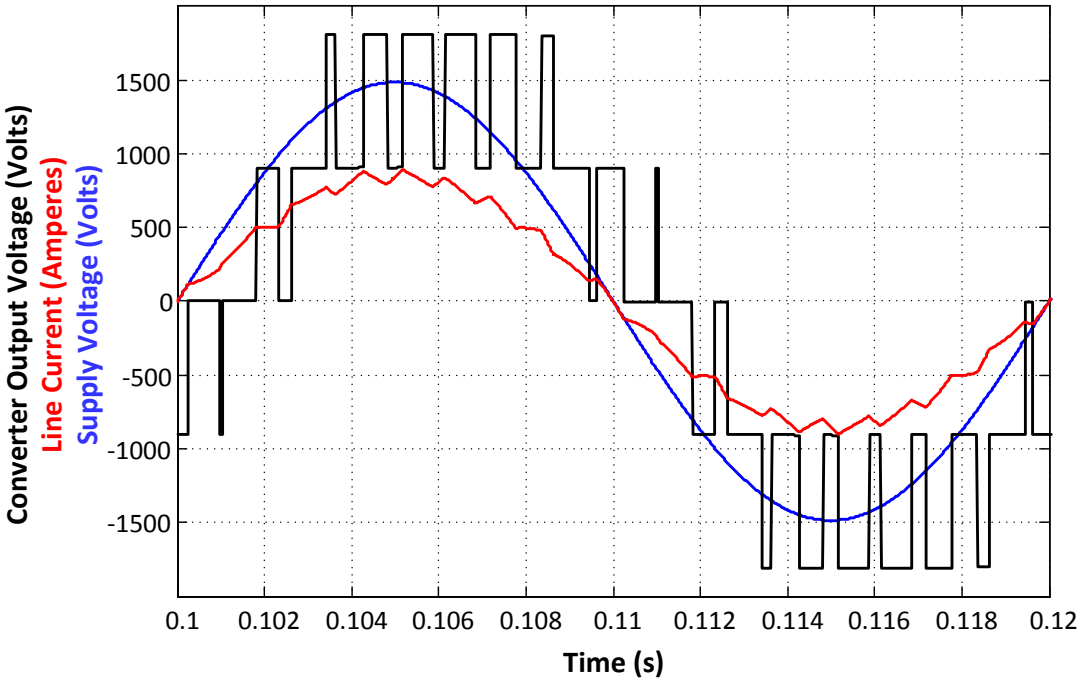


Figure 2.13: Unity pf Operation of Three - Level 4Q Converter:
(blue) Supply Voltage, (black) Converter Output Voltage, (red) Line Current

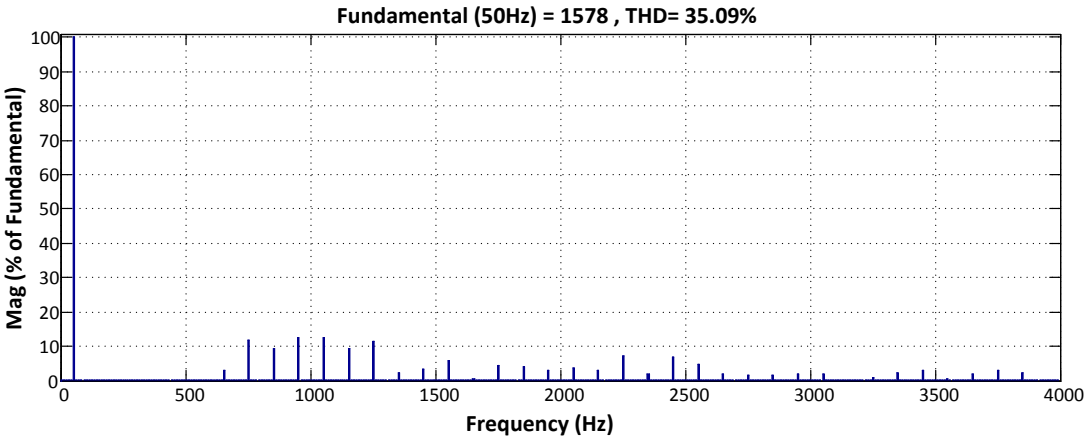


Figure 2.14: Harmonic Spectrum of Converter Output Voltage in a Three - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

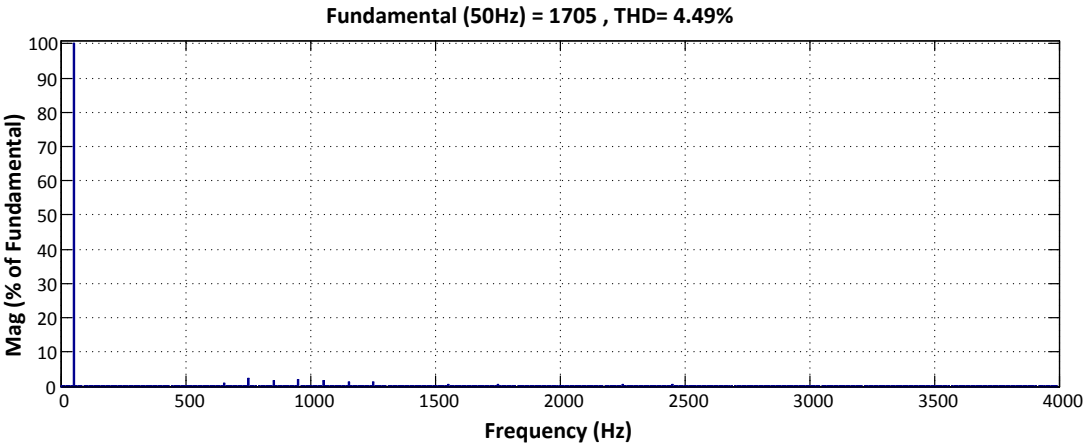


Figure 2.15: Harmonic Spectrum of Line Current in a Three - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

Three - level converters are often implemented with capacitors which is known as Flying Capacitor Multilevel Converter as shown in Figure 2.16 [61, 70]. There are not commonly used in locomotive traction systems.

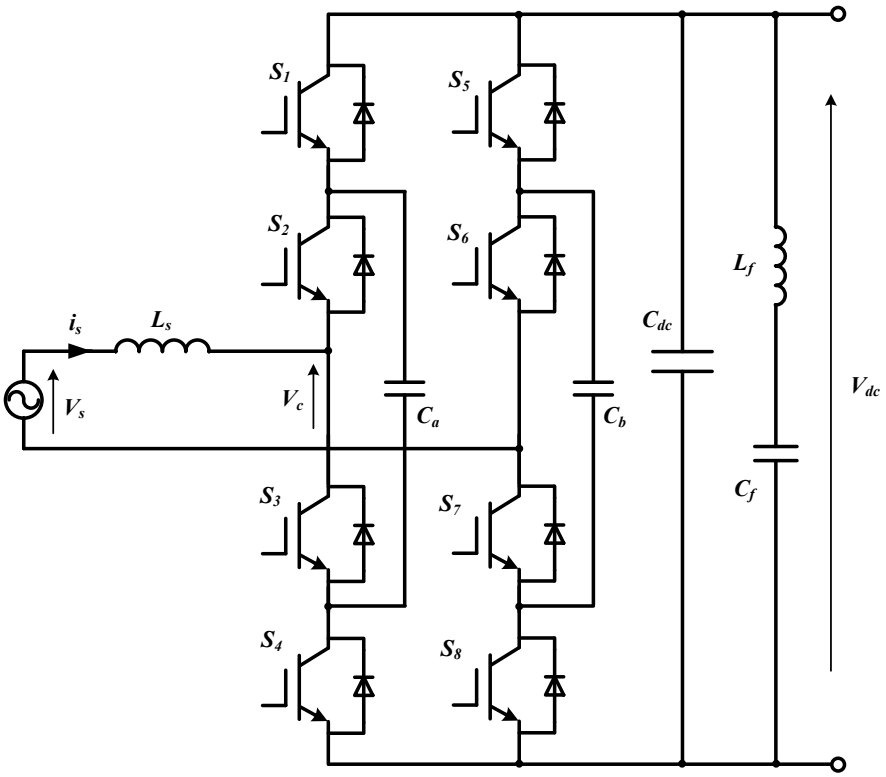


Figure 2.16: Flying Capacitor Three - Level Converter Topology

2.2.3. Interleaved Two - Level 4Q Converter

The circuit diagram of interleaved two - level 4Q converter topology is shown in Figure 2.17 [56, 73]. Interleaved 4Q converter topology is composed of two (or more) H bridges connected in parallel via a common DC link and connected to the AC supply with separate isolated front-end transformer secondary windings. Multiple converters supplying the same DC link provide redundant operation. This is one of the main reasons why this topology is frequently used for locomotive traction applications.

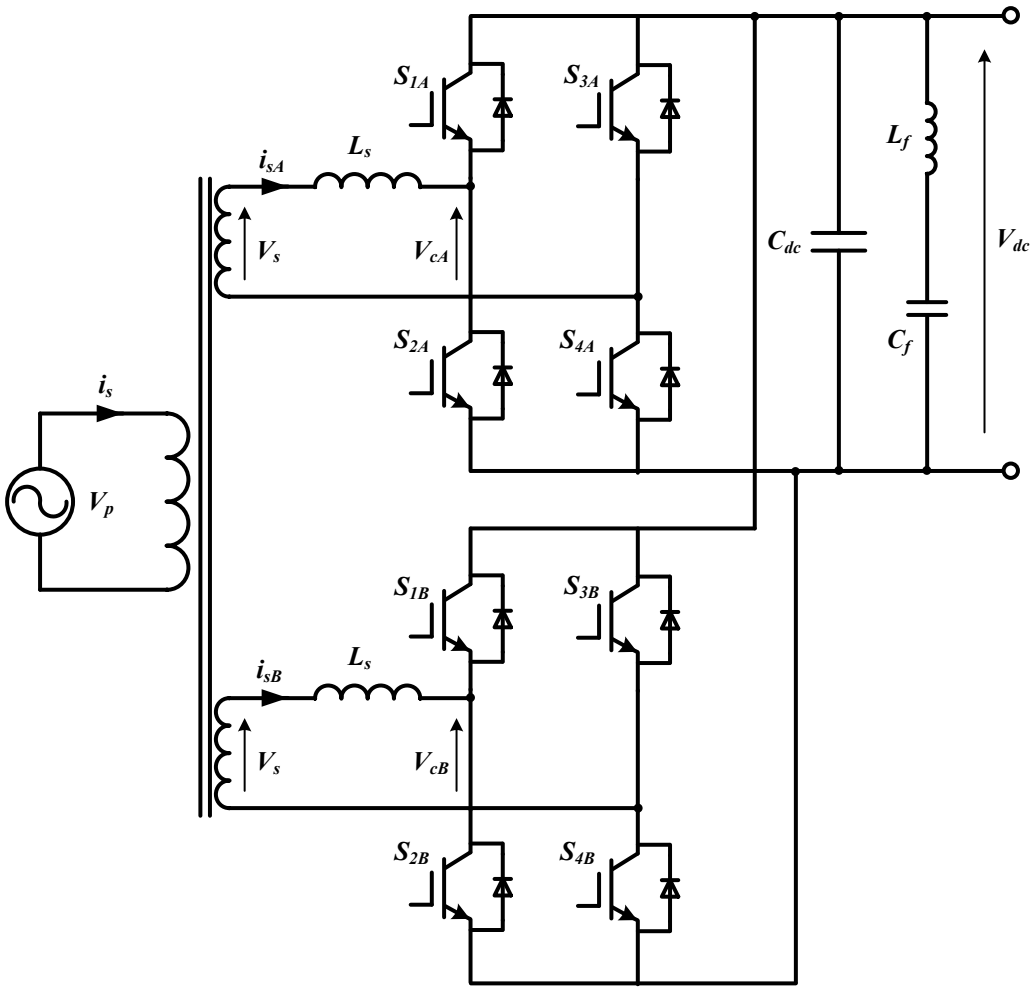


Figure 2.17: Circuit Diagram of Interleaved Two - Level 4Q Converter Topology

Operation of each H Bridge is the same as the two - level converter. The superiority of this topology is the possibility of reducing the harmonic distortion at the supply (primary side of the traction transformer) with the application of phase shifted PWM technique [55, 58 and 70]. One other advantage of interleaving is to distribute the rated power among several individual converters, and hence the current rating of power semiconductors can be reduced. That is why interleaving is a widely used technique in various power converters. The phase shift angle between converters is calculated using (2.14) where n is total number of converters connected to the same transformer [55, 97].

$$\varphi = \frac{360}{2\,n} \tag{2.14}$$

For this particular example with two 4Q converters, phase shift between the carrier waveforms of the converters is 90^0. A sample modulation in one fundamental cycle of the supply frequency is also illustrated in Figure 2.18, showing the modulating signal along with carrier signals for each converter and output voltage waveform of each converter. Unity pf operation of interleaved two - level converter, obtained by open loop computer simulations carried out in MATLAB/Simulink with 500 Hz switching frequency, 1 mH of AC line inductance and 1800V of DC link voltage is also shown in Figure 2.19 including supply voltage, converter output voltage and line current waveforms. Phase shifted operation is shown in Figure 2.20. Furthermore, harmonic spectra of input current of each individual converter and input current at the primary side of the transformer are shown in Figures 2.21, Figure 2.22 and 2.23, respectively.

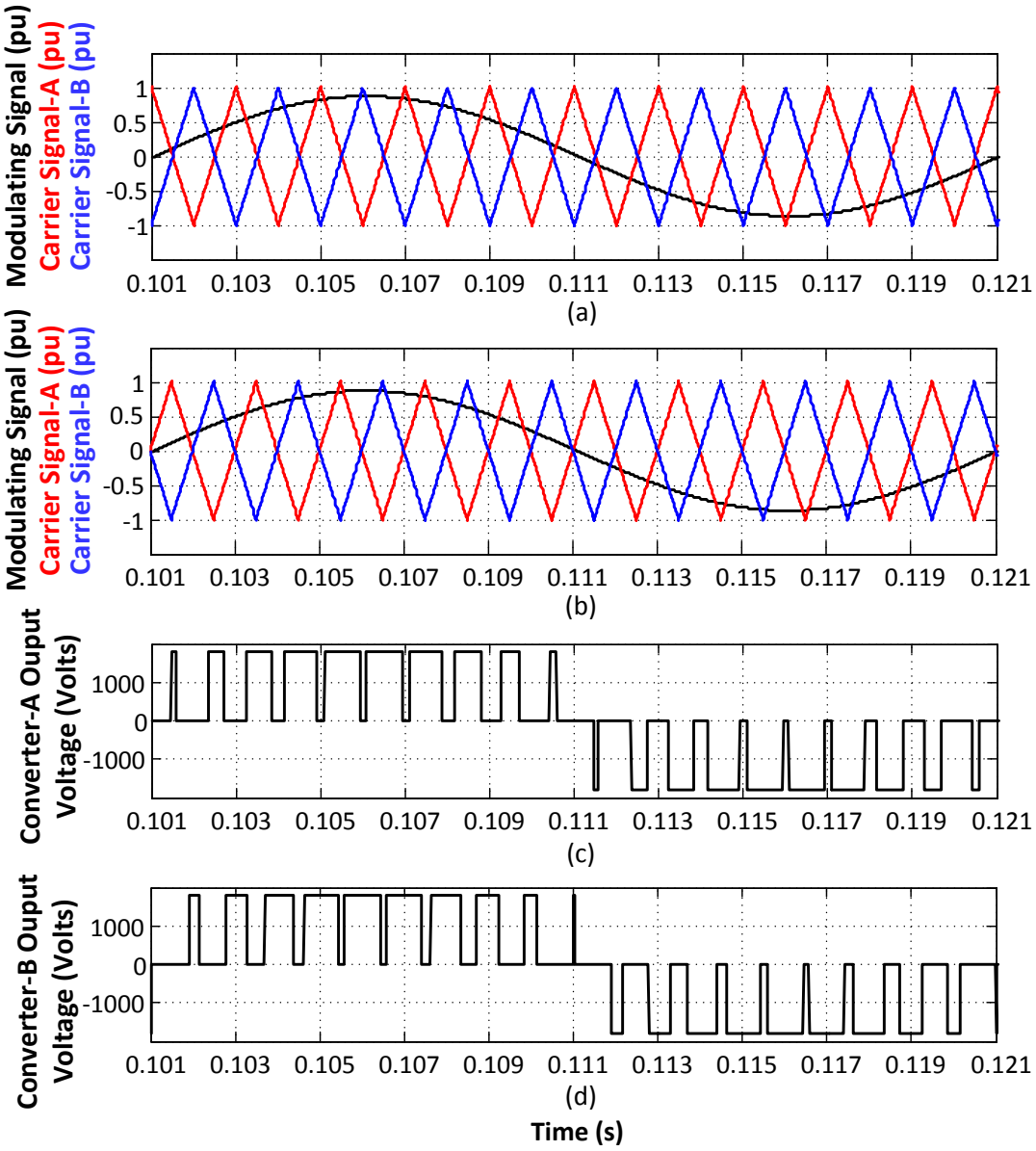
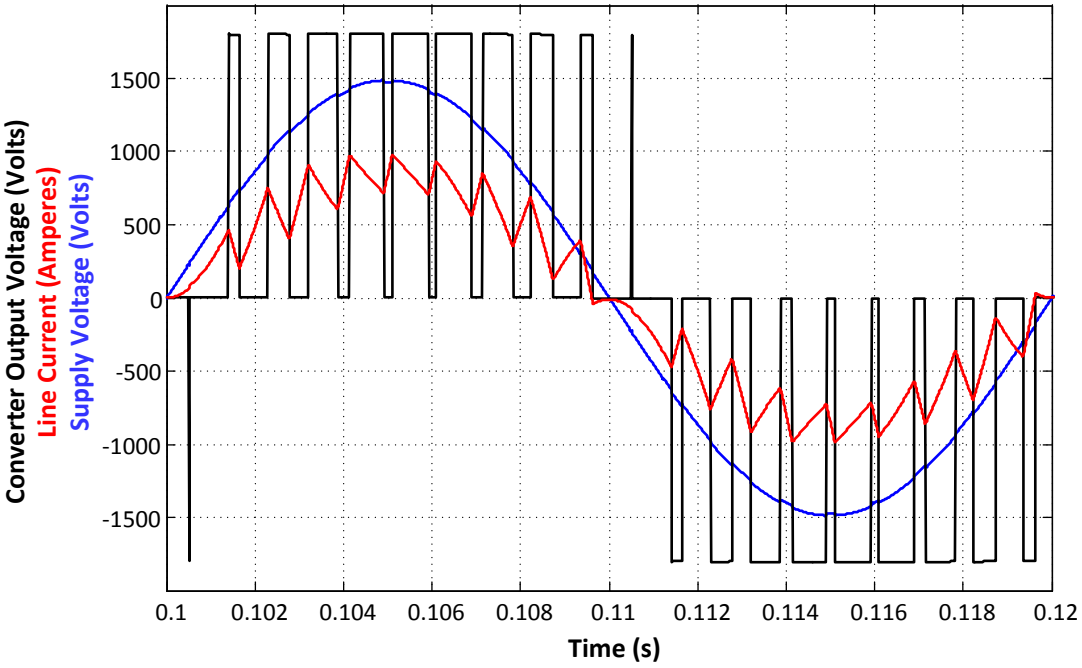


Figure 2.18: A Sample Modulation of Interleaved Two - Level Converter: (a) Modulating Signal and Carrier Signals of Converter-A

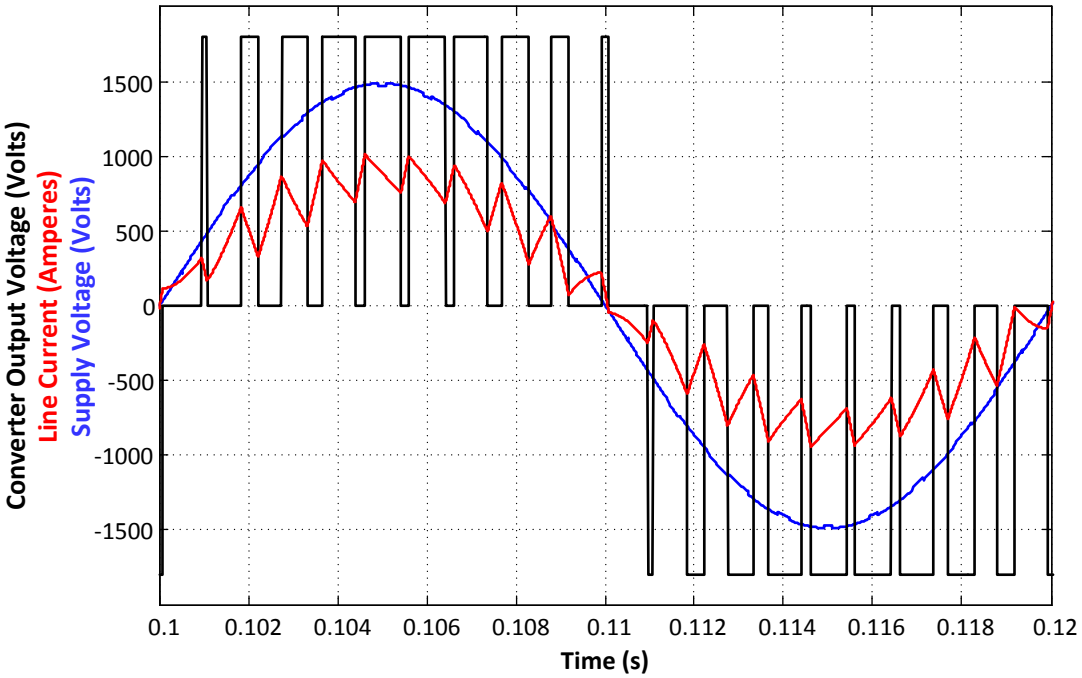
(b) Modulating Signal and Carrier Signals of Converter-B

(c) Output Voltage Waveform of Converter-A

(d) Output Voltage Waveform of Converter-B



(a)



(b)

Figure 2.19: Unity pf Operation of Interleaved 4Q Converter:
(a) Converter-A, (b) Converter-B

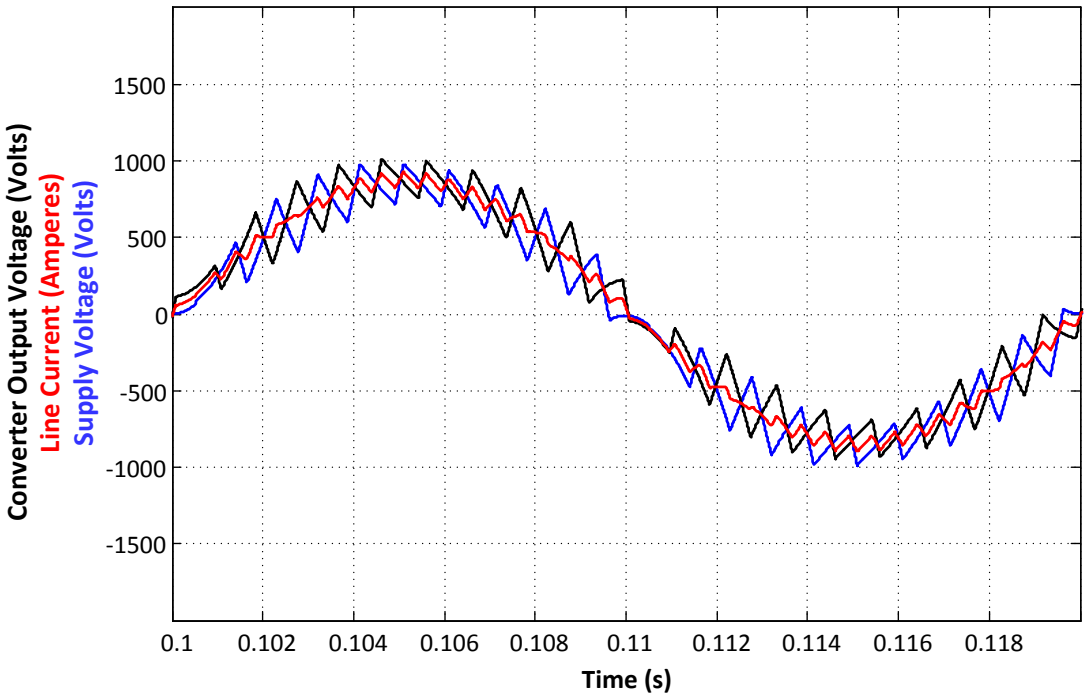


Figure 2.20: Phase Shifted Operation of Interleaved 4Q Converter:

(blue) Converter-A Current, (black) Converter-B Current, (red) Line Current

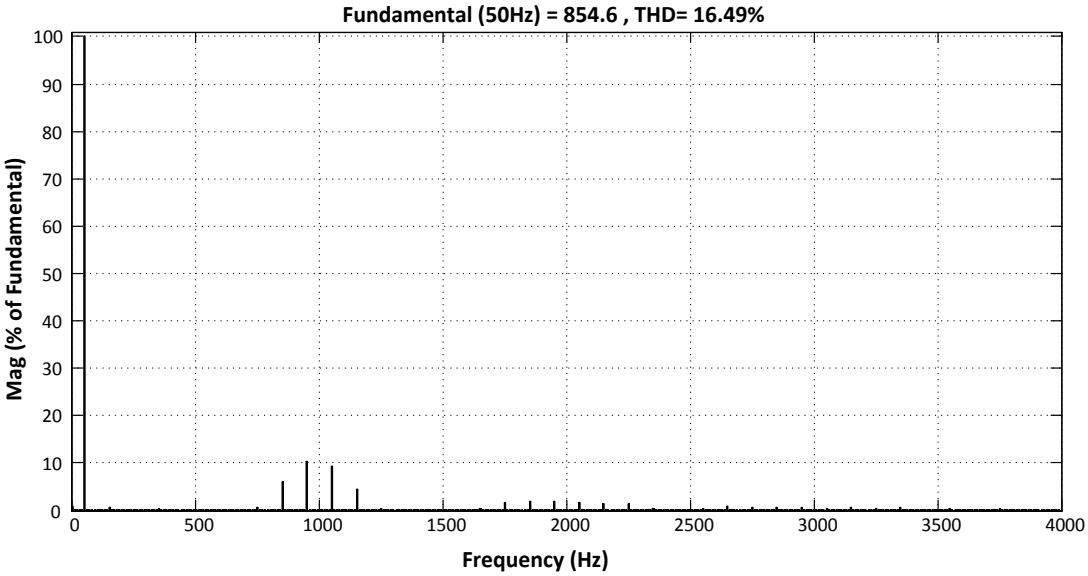


Figure 2.21: Harmonic Spectrum of Converter-A Input Current in an Interleaved Two - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

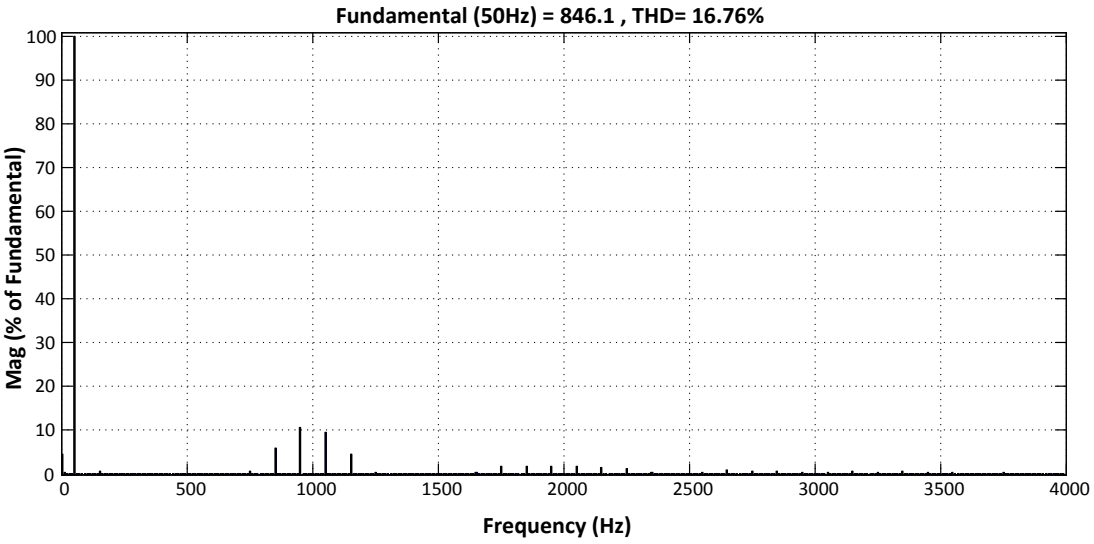


Figure 2.22: Harmonic Spectrum of Converter-B Input Current in an Interleaved Two - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

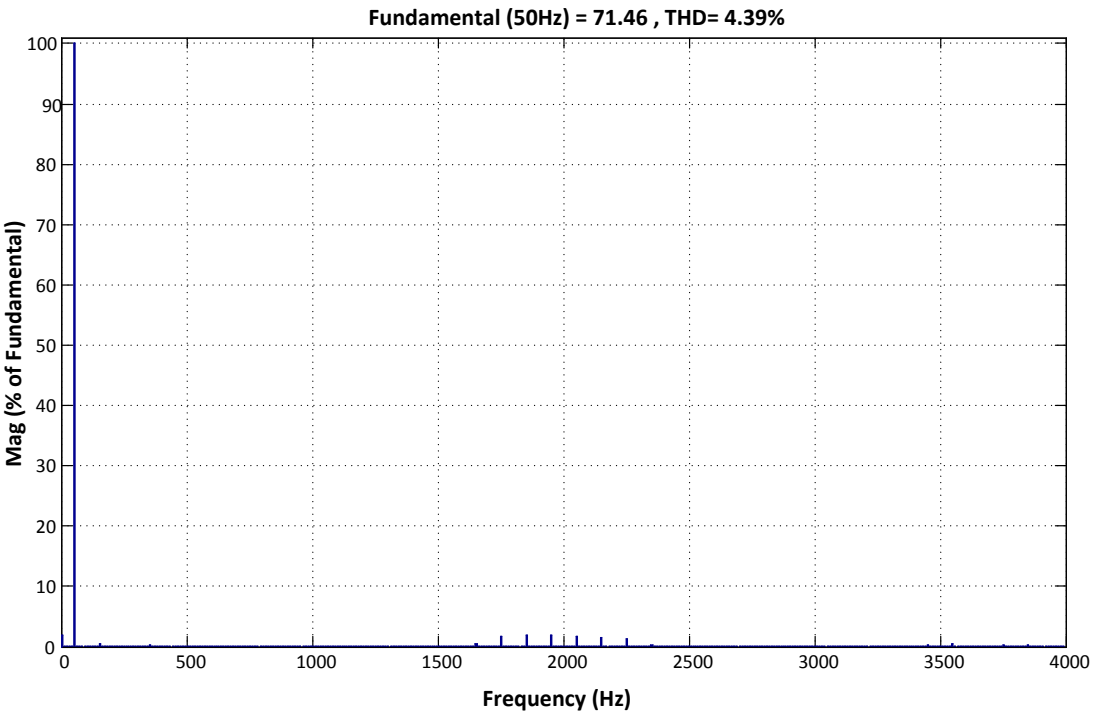


Figure 2.23: Harmonic Spectrum of Total Input Current in an Interleaved Two - Level Converter (L_s = 1 mH, f_{sw} = 500 Hz)

2.2.4. Series Connected Multilevel 4Q Converter

The series connected multilevel converter is composed of multiple H-bridge modules connected in series on the AC side for basically transformer-less operation. The front - end transformer used in topologies previously mentioned is a step down transformer to reduce the catenary voltage of 25 kV to lower voltage levels. Since it is expected to operate at catenary frequency; i.e. 50 Hz, it is a bulky component in terms of volume and weight. With the utilization of series connected multilevel converter, it is possible to eliminate this bulky transformer and replace it with a transformer operating at higher frequencies [64]. The circuit diagram of series connected multilevel 4Q converter with two series converters is shown in Figure 2.24 [65].

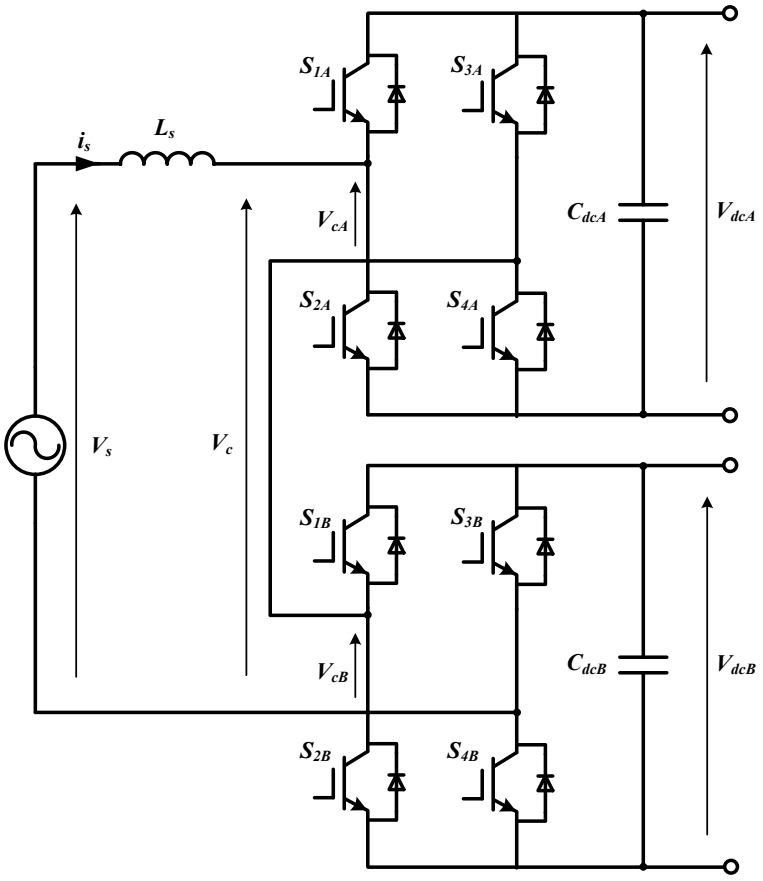


Figure 2.24: Circuit Diagram of Series Connected Multilevel 4Q Converter Topology

The number of cascaded H - bridge modules directly depends on the selection of power semiconductor device. As seen from Figure 2.24, DC links are separated and hence, their voltages should be balanced accordingly. This is a drawback for this topology since it makes the control system much more complex [66]. Although elimination of the expensive input transformer reduces the cost drastically, utilization of many H-bridges makes the overall system too expensive and hence, this topology is not commonly preferred in locomotive traction applications [69].

The output voltage of the series connected multilevel converter shown in Figure 2.24 is the sum of output voltages of each converter as shown in (2.15). Assuming equal DC link voltages as in (2.16), output voltage of each converter may have three possible levels as in the two - level converter case. By the series connection of two H-bridges, the overall output voltage waveform is a five level waveform as in the three - level converter case. Possible switching states and resultant voltage levels of the series connected multilevel converter with two H-bridge modules are shown in Table 2.4 [66].

$$v_c = v_{cA} + v_{cB} \tag{2.15}$$

$$V_{dcA} = V_{dcB} = V_{dc} \tag{2.16}$$

There are two basic PWM techniques applicable to series connected multilevel converters; phase-shifted modulation and level-shifted modulation [28]. Phase shifted PWM is achieved by introducing a phase shift between the carrier signals of each H-bridge converter shown in (2.17), m being the number of levels at the converter output voltage waveform. In the case two converters, since there are a total of five levels, the carrier signals are phase shifted by 90^0. On the other hand, level shifted modulation is implemented by using a number of m-1 carrier signals with same amplitude, frequency and phase which are vertically disposed. For phase shifted modulation, switching frequency of each power semiconductor is the same and equals to the converter switching frequency as well as device conduction periods. For level shifted modulation, switching frequency of each power device is different from the other and switching frequency of the converter. Utilization of semiconductor devices is also different in terms of conduction period, but studies show that total harmonic distortion

obtained from level-shifted modulation is better than that of the phase-shifted modulation strategy under the same operating conditions [28].

$$\varphi = \frac{360}{m-1} \tag{2.17}$$

Phase-shifted modulation strategy for the series connected multilevel converter topology in one fundamental cycle of the supply frequency is shown in Figure 2.25 where the modulating signal along with all carrier signals, output voltage of each H-bridge module and resultant converter output voltage waveform are given. Level-shifted modulation strategy is also illustrated in Figure 2.26, showing the modulating signal along with all carrier signals, output voltage of each H-bridge module and resultant converter output voltage waveform [28].

Table 2.4: Possible Switching States of the Series Connected Multilevel Converter

State	**S_{1A}**	**S_{2A}**	**S_{3A}**	**S_{4A}**	**S_{1B}**	**S_{2B}**	**S_{3B}**	**S_{4B}**	**V_c**
1	0	1	0	1	0	1	0	1	0
2	0	1	0	1	0	1	1	0	$-V_{dc}$
3	0	1	0	1	1	0	0	1	$+V_{dc}$
4	0	1	0	1	1	0	1	0	0
5	0	1	1	0	0	1	0	1	$-V_{dc}$
6	0	1	1	0	0	1	1	0	$-2V_{dc}$
7	0	1	1	0	1	0	0	1	0
8	0	1	1	0	1	0	1	0	$-V_{dc}$
9	1	0	0	1	0	1	0	1	$+V_{dc}$
10	1	0	0	1	0	1	1	0	0
11	1	0	0	1	1	0	0	1	$+2V_{dc}$
12	1	0	1	1	1	0	1	0	$+V_{dc}$
13	1	0	1	0	0	1	0	1	0
14	1	0	1	0	0	1	1	0	$-V_{dc}$
15	1	0	1	0	1	0	0	1	$+V_{dc}$
16	1	0	1	0	1	0	1	0	0

The operation of the series connected multilevel converter at unity pf, obtained by open loop computer simulations carried out in MATLAB/Simulink with the same operating conditions as those used in previous PWM rectifier topologies is also shown in Figure 2.27, including supply voltage, converter output voltage and line current. Furthermore, harmonic spectra of converter output voltage and line current are shown in Figures 2.28 and 2.29, respectively.

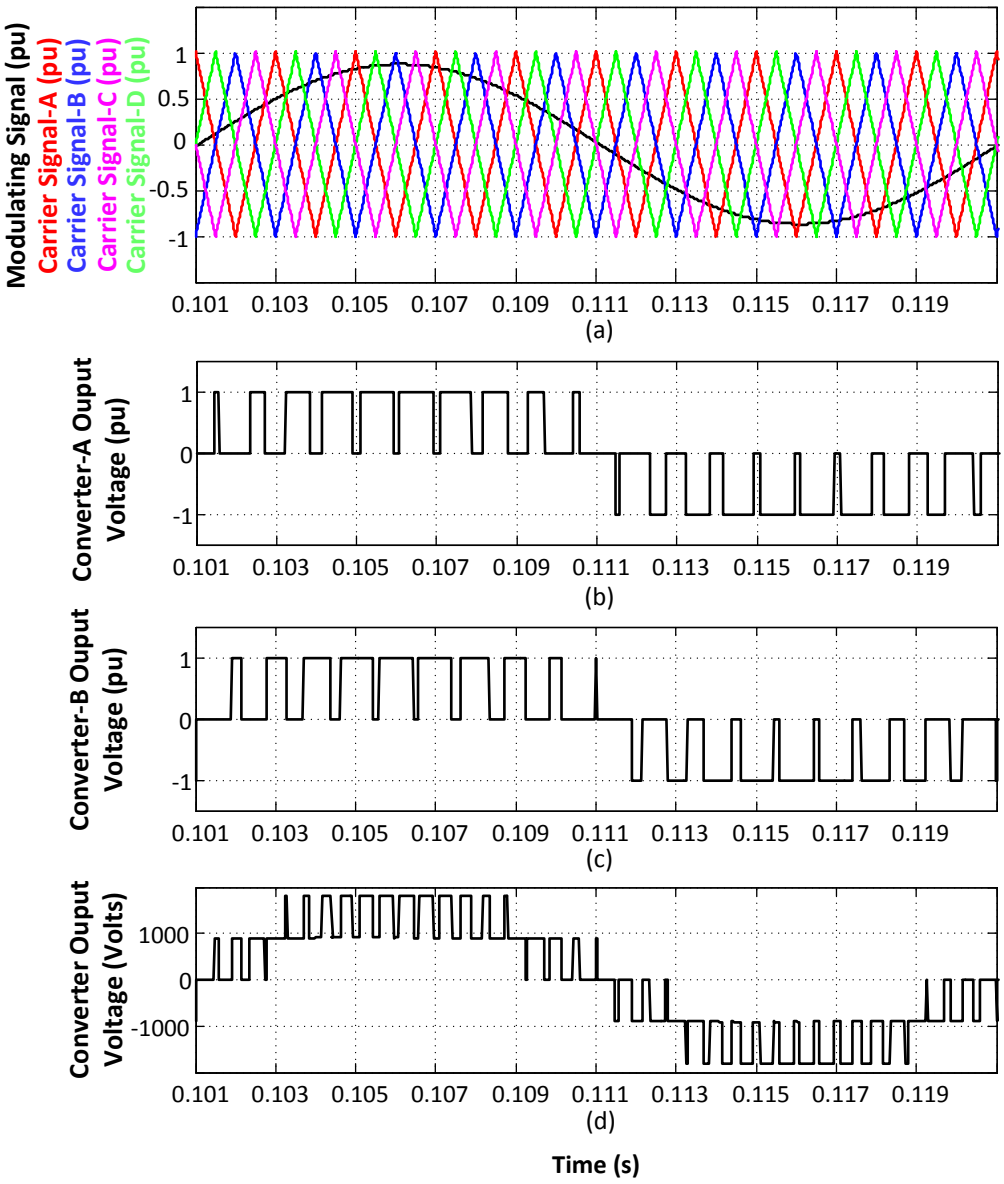


Figure 2.25: Phase Shifted Modulation Strategy of Series Multilevel Converter: (a) Modulating Signal and Carrier Signals, (b) Output Voltage of Converter-A (c) Output Voltage of Converter-B, (d) Converter Output Voltage Waveform

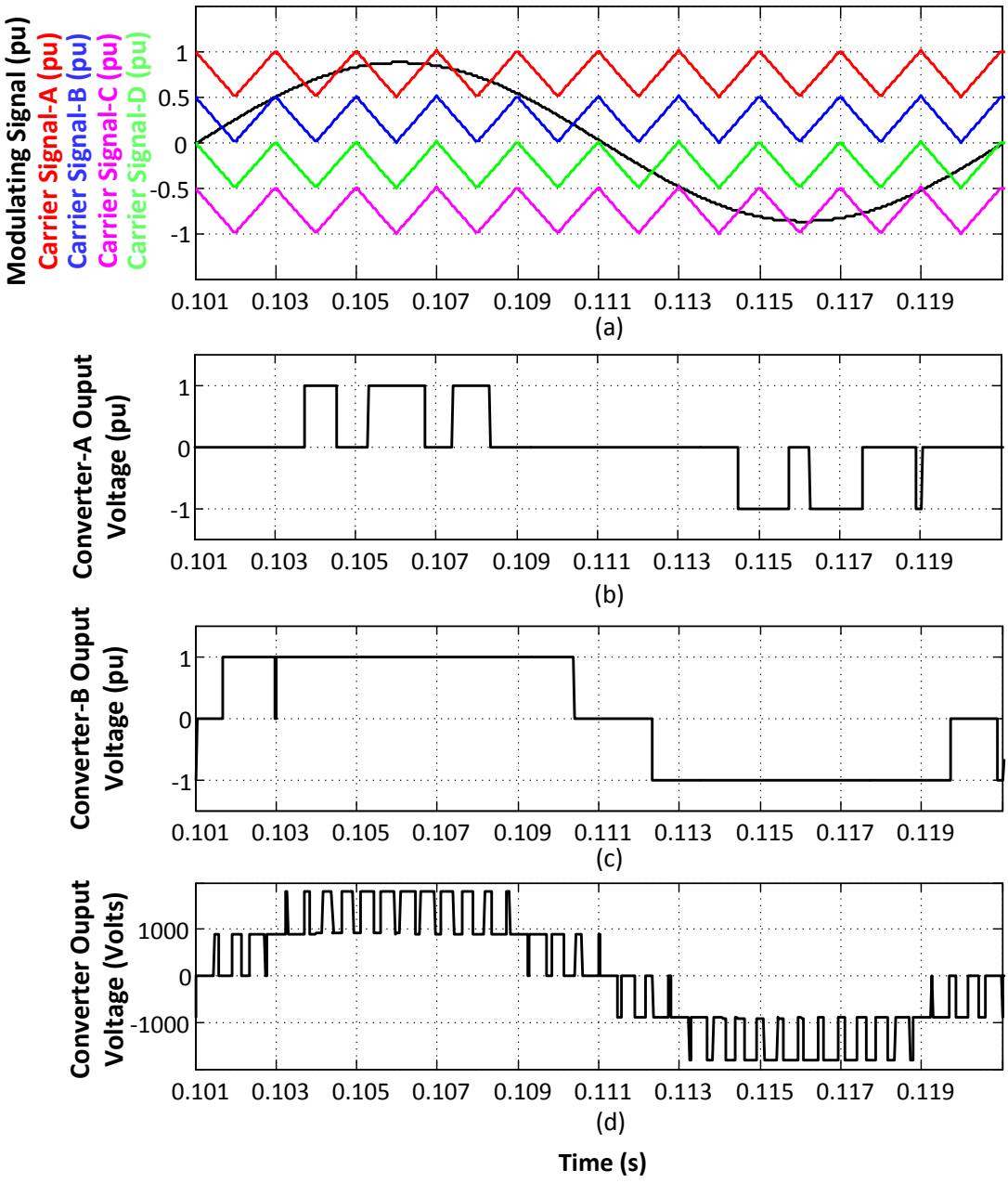


Figure 2.26: Level Shifted Modulation Strategy of Series Multilevel Converter: (a) Modulating Signal and Carrier Signals, (b) Output Voltage of Converter-A (c) Output Voltage of Converter-B, (d) Converter Output Voltage Waveform

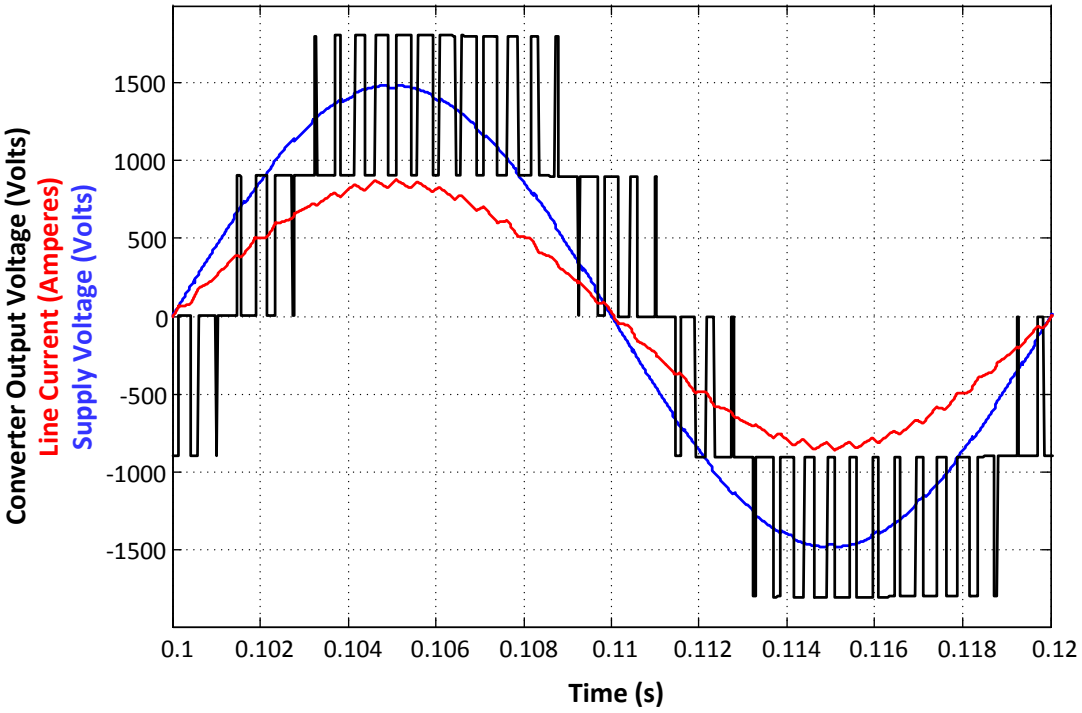


Figure 2.27: Unity pf Operation of Series Connected Multilevel Converter: (blue) Supply Voltage, (black) Converter Output Voltage, (red) Line Current

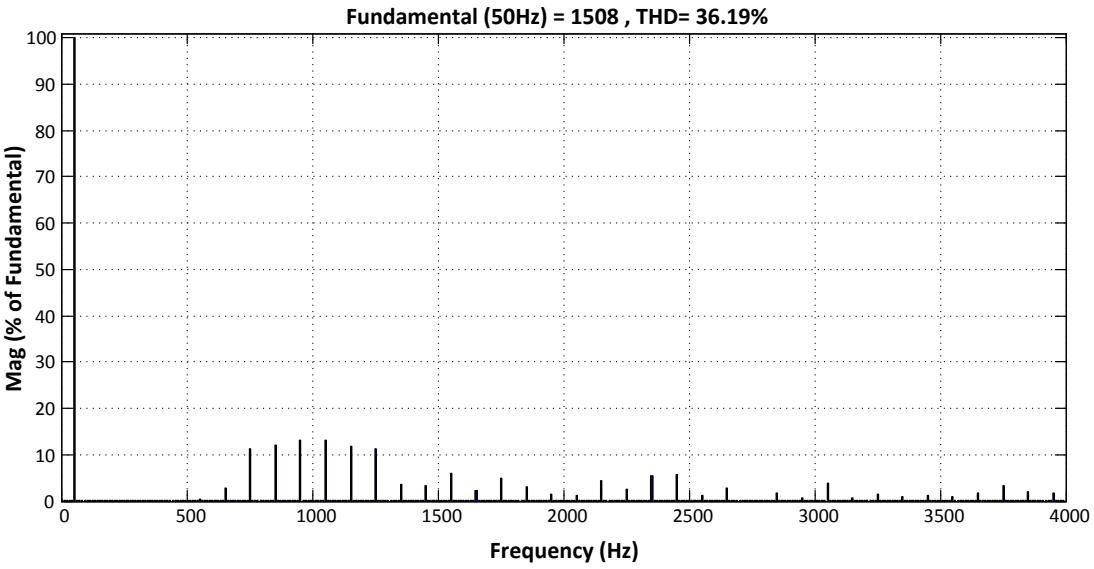


Figure 2.28: Harmonic Spectrum of Converter Output Voltage in a Series Connected Multilevel Converter (L_s = 1 mH, f_{sw} = 500 Hz)

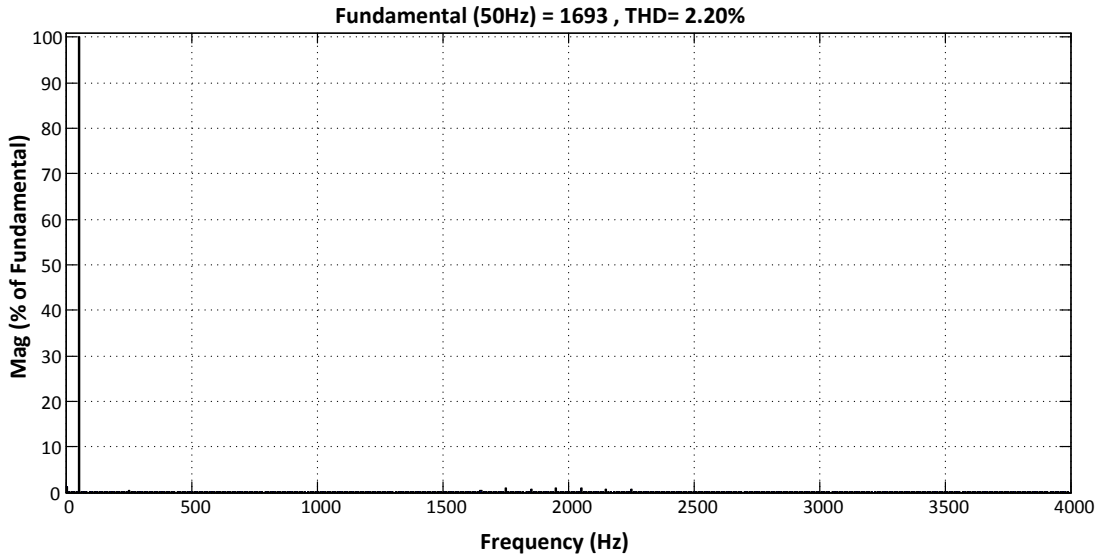


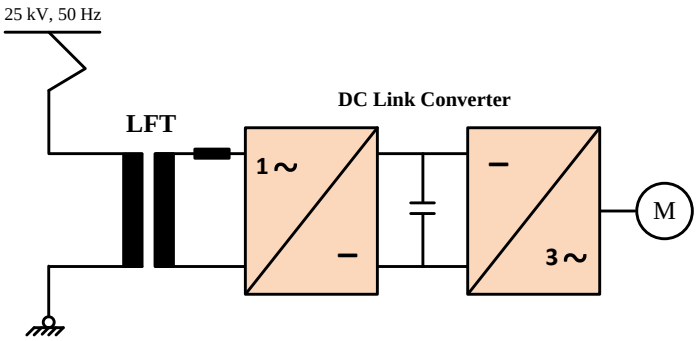
Figure 2.29: Harmonic Spectrum of Line Current in a Series Connected Multilevel Converter (L_s = 1 mH, f_{sw} = 500 Hz)

2.2.5. Other Topologies

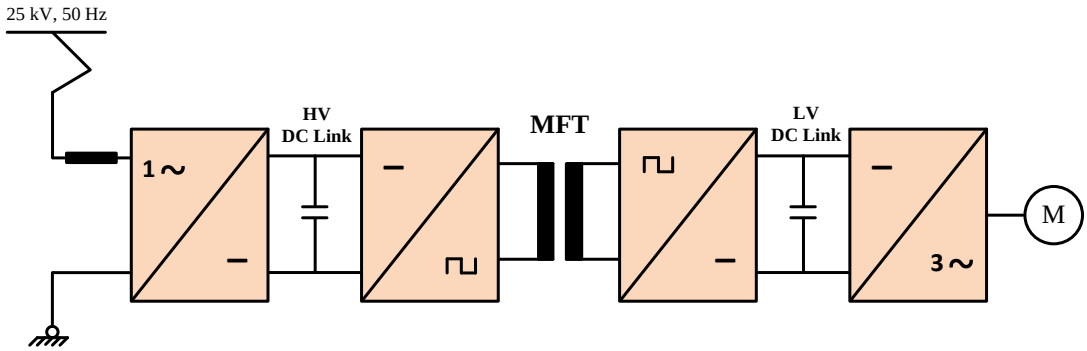
Up to now, the main focus of this research work was on locomotive traction systems employing front-end transformers and operating at mains supply frequency. There is another method used in Medium Voltage applications which utilizes medium frequency transformers (MFT). Such converters are often referred to as power electronics transformers (PET) [18, 67, 68 and 69]. This idea is already in use in DC/DC converters with isolation requirement in several applications such as grid connected photovoltaic systems and has not found much interest in AC traction applications yet. Topologies employing MFT has the advantages of reduced transformer weight and volume, better transformer efficiency and hence easier cooling. On the other hand, it has several drawbacks. First of all, since power semiconductor device technology has not yet been developed to implement voltage ratings comparable to catenary voltage levels, series connected multilevel converter topology has to be utilized with more than 40 levels (for 25 kV catenary lines). This

brings inconveniences like increase in overall cost, worsen reliability and complex control and modulation requirements.

Block diagram of locomotive traction systems employing LFT and MFT are shown in Figure 2.30 [67] and circuit diagram of locomotive traction system with series connected multilevel converter and MFT is shown in Figure 2.31 [69].



(a)



(b)

Figure 2.30: Block Diagram of Locomotive Traction Systems Employing Different Transformer Configurations: (a) LFT, (b) MFT [67]

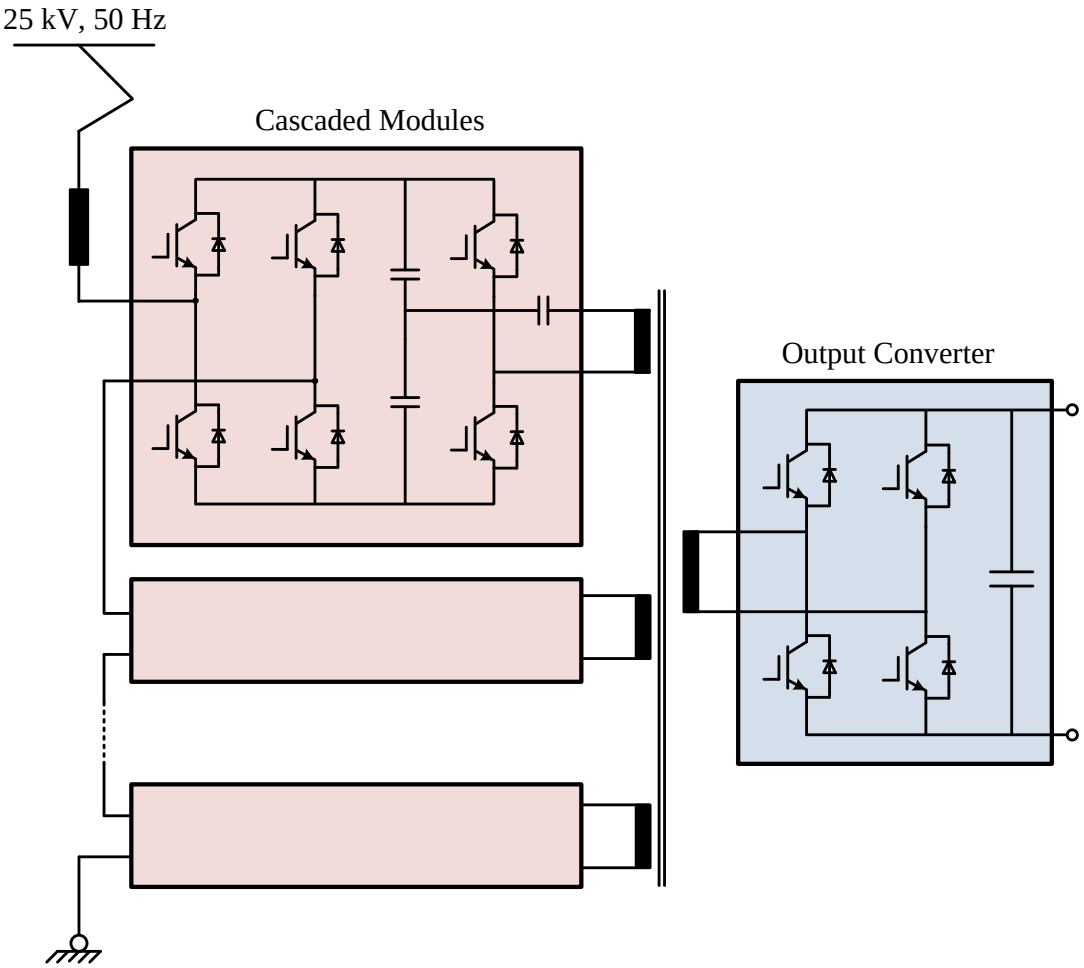


Figure 2.31: Circuit Diagram of Locomotive Traction System with Series Connected Multilevel Converter and MFT [69]

2.2.6. Comparison of PWM Rectifier Topologies

In this part, the performance of presented voltage source PWM rectifier topologies will be compared in terms of various constraints with the help of not only literature research, but also the open loop simulation work introduced in this chapter. The topologies will be referred as; 2LC for two - level converter, 3LC for three level neutral point clamped converter, I2LC for interleaved two - level converter and SCMC for series connected multilevel converter.

I2LC topology provides the best redundancy among all other alternatives. Considering one DC link converter supplying a single traction motor, it is possible to maintain the operation in case one converter fails with reduced output power for only I2LC [55, 58]. This feature is important for uninterrupted operation of the railway vehicle.

For 3LC, semiconductor blocking voltage requirement is half of the 2LC and I2LC so that, higher DC link voltages can be achieved if necessary [54]. For SCMC topology, it is also possible to use lower voltage semiconductor devices since the number of series modules can be arranged accordingly [64]. One other advantage of 3LC topology is the overvoltage stress on each power device being less than of two - level type topologies. Hence, dv/dt filter requirement is less [54].

For the same output power, semiconductor device current ratings can be reduced with the use of I2LC since the power of one DC link converter is shared between two separate converters [55]. By this means, the total output power rating of one DC link converter can be increased employing the same power devices if required.

In regards to line current harmonics, 2LC topology is the alternative which should be considered last. Due to poor harmonic distortion performance, higher switching frequencies should be applied to meet the power quality standards, which influence system efficiency negatively. Additionally, volume, weight and cost of passive filters on both AC and DC side will increase, which is not desirable. 3LC converter topology provides better harmonic content compared to 2LC due to higher number of levels at the output voltage with the same switching frequency [54, 58]. In addition, I2LC is also advantageous in terms of line current harmonic distortions thanks to phase shifted modulation by means of which the effective frequency at the primary side of the front - end transformer is four times the switching frequency whereas, it is two times the switching frequency for other topologies [70, 98] which can also be spotted from the line current harmonic spectra provided beforehand. Having harmonics at higher frequencies is also desired because of the fact that the switching frequency can be reduced without causing low order harmonics to emerge. The results show that, if one compares THD values of each topology under the same operating conditions, it will be $THD_{SCML} < THD_{I2LC} = THD_{3LC} < THD_{2LC}$.

It is already pointed out that topologies with better harmonic performance are likely to be more efficient due to the possibility of lower switching frequency operation. Hence, it is safe to say that 2LC has the worst efficiency. The superiority of I2LC converter arises from the phase-shifted operation as emphasized several times. Another good impact of I2LC on efficiency is the reduction of AC line filter size power loss of which should also be taken into account. Considering the switching loss of power semiconductors, research shows that 3LC topology is advantageous over 2LC converter at the same switching frequency because of the possibility to use IGBTs with lower blocking voltage ratings. The turn-on and turn-off energies of IGBT semiconductors increase by a factor of 3 to 5 with the increase on the blocking voltage capability [54]. Finally, due to extra clamping diodes present on 3LC topology, total conduction loss is slightly higher than that of 2LC whereas the difference in switching loss is more prominent [54].

Cost is also a major concern, but the approach for each particular design is almost unique depending on many other constraints. Nonetheless, a simple analysis can be performed, at least to have a point of view with the help of component count analysis for each topology, again under same operating conditions. First of all, a major drawback of I2LC is the requirement of higher transformer secondary windings [58]. Since there are two H - bridge converters connected in parallel via DC link, device count of this topology is two times that of 2LC topology. However, reduction of filter size and semiconductor current rating should compensate this substantially. Semiconductor device count for 3LC topology is also two times of 2LC, then again the voltage rating of power devices will be half. Component count comparison of these three PWM rectifier topologies is shown in Table 2.5 [54]. It must be noted that, this comparison is made considering one DC link converter with the same output power for each topology. Ratings of each component should also be considered along with the component count for better comparison. Furthermore, SCMC topology is not considered in this specific comparison due to the fact that the component count for this topology is incomparably high.

Table 2.5: Component Count Comparison of PWM Rectifier Topologies

Component	2LC	3LC	I2LC
IGBT modules with inverse diodes	4	8	8
Fast diode modules (clamping)	0	3	0
Number of gate drives	4	8	8
Transformer secondary winding	1	1	2
AC line filter	1	1	2
AC line current sensors	1	1	2
DC link capacitor	1	2	1
DC link voltage sensors	1	2	1

Even though multilevel type topologies (3LC and SCMLC) have several benefits, they introduce more complexity in terms of control and modulation. First of all, equalization of DC link voltages is required which is usually achieved by additional DC link voltage balancing algorithms for multilevel topologies [54, 61 and 62]. Furthermore, complexity of modulation increases with more levels utilized on the power stage.

From the viewpoint of filter sizes, topologies with better harmonic distortion performance always become prominent. It has been shown that, under same operating conditions, filter size of 3LC is at least 30 % percent smaller compared to 2LC topology [54]. For 2LC, filters more bulky than other topologies will be required to meet the harmonic distortion standards. DC link capacitor is also affected by the harmonic content created by the converter. Frequency of first harmonic group of I2LC is doubled on not only primary side of the front-end transformer, but also on the DC link. Hence, that topology is better for reduction of both AC Line filter inductor and DC link filter capacitor size. SCMLC topology offers to replace the bulky front-end transformer with a medium frequency transformer so that volume and weight of the overall system is reduced considerably in spite of the fact that power semiconductor component count is much higher [46]. Heat sink size is also a big concern when volume of the system is critical. Low loss systems are advantageous not only due to good efficiency performance, but also due to the reduction of volume and weight since

cooling requirement will be less and hence heat sink will be smaller. Therefore, topologies to which smaller switching frequencies can be applied are advantageous. Another aspect to compare the PWM rectifier topologies is common mode voltages which cause common mode currents and hence Electromagnetic Interference (EMI) problems. Studies have shown that 3LC offers a better performance than 2LC in terms of common mode voltages [54, 99]. Comparison of PWM rectifiers can be summarized as in Table 2.6. This comparison is based on a system with the same output power for all topologies.

Table 2.6: Comparison of PWM Rectifier Topologies

✔✔: Very Good, ✔: Good, **X**: Bad, **XX**: Very Bad

Constraint	**2LC**	**3LC**	**I2LC**	**SCMLC**
Redundancy	✔	✔	✔✔	**X**
Power Device Voltage Rating	**X**	✔	**X**	✔
Power Device Current Rating	**X**	**X**	✔	**X**
Line Current Harmonics	**X**	✔	✔	✔✔
DC Link Harmonics	**X**	✔	✔✔	✔
Efficiency	**X**	✔	✔✔	**X**
Component Count / Cost	✔✔	**X**	**X**	**XX**
Control Complexity	✔	**X**	✔	**X**
Modulation Complexity	✔	**X**	**X**	**X**
Filter Size	**X**	✔	✔✔	✔
Volume and Weight	**X**	✔	✔	✔✔
Common Mode Voltages	**X**	✔	**X**	✔✔

In conclusion, interleaved two - level 4Q PWM rectifier topology is selected for this particular research and development work. Main reasons behind this choice are superior harmonic distortion performance, redundancy, good efficiency, reduction on power device current ratings and, reduction on filter sizes.

CHAPTER 3

SYSTEM DESCRIPTION AND OPERATING PRINCIPLES OF INTERLEAVED TWO - LEVEL 4Q CONVERTERS

In this chapter, interleaved two - level 4Q converter systems will be described; operation principles and modes will be explained. After a brief description of the topology, the achievement of unity pf operation will be introduced. Behavior of the converter in each operation mode will be analyzed in detail. General control structure, control variables and applicable control techniques available in the literature will be given. PWM techniques used in two - level PWM rectifiers and phase shifted operation with interleaved connection will be described. Finally, comparison of control techniques and PWM methods will be discussed.

3.1. Introduction

Single phase interleaved two-level 4Q converter circuit diagram is shown in Figure 3.1 [73, 100 and 101]. The converter consists of; a traction transformer with multiple isolated secondary windings, a series reactor on the AC side of each converter, H-bridge type IGBT converters connected in parallel on a common DC link, a high frequency filter capacitor on DC side and a series LC filter tuned to twice the supply frequency on the DC side. In main line locomotive traction systems, constant DC link voltage operation is applied.

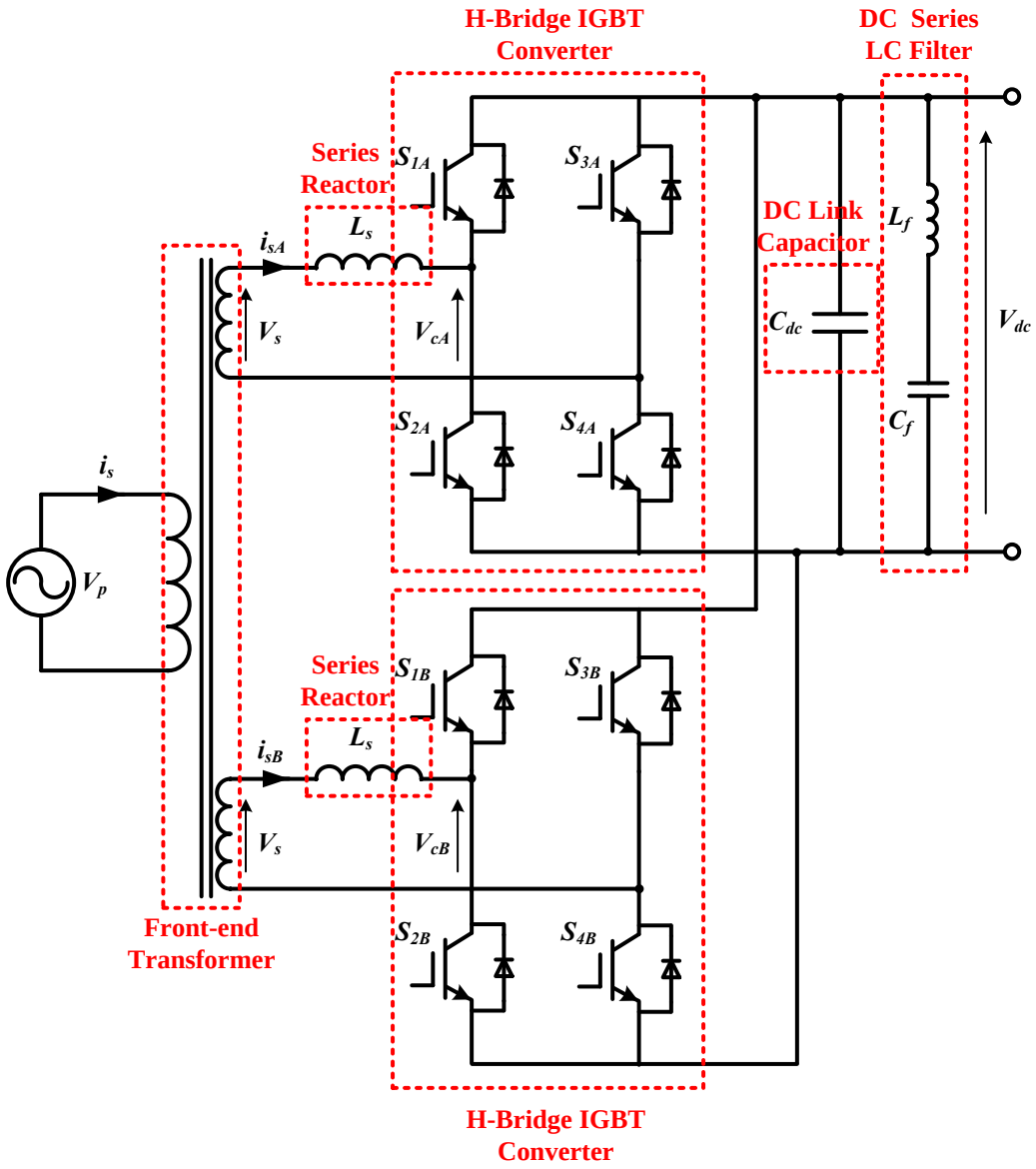


Figure 3.1: Single Phase Interleaved Two-Level 4Q Converter Circuit Diagram

Properties of this PWM rectifier system can be summarized as follows [35, 100]:

- It has bidirectional active power flow capability so that regenerative braking is possible [37, 76].
- It can operate at unity pf.
- Line current harmonic distortion is low and can further be reduced by phase-shifted operation.

- Its transient performance is good.
- It is redundant; i.e., the system still continues to operate even if one of the converters fails.
- Reactive power can be drawn from or supplied to the catenary for reactive power compensation or line voltage regulation purposes.

3.2. Single Line Diagram and Unity Power Factor Operation

Single line diagram of the interleaved two - level 4Q converter is shown in Figure 3.2.

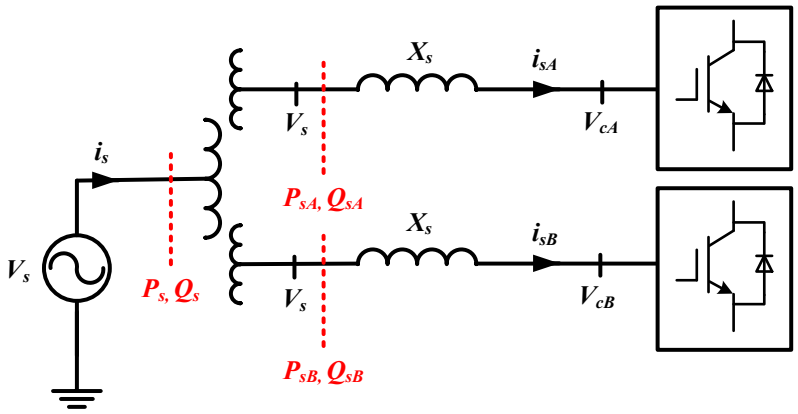
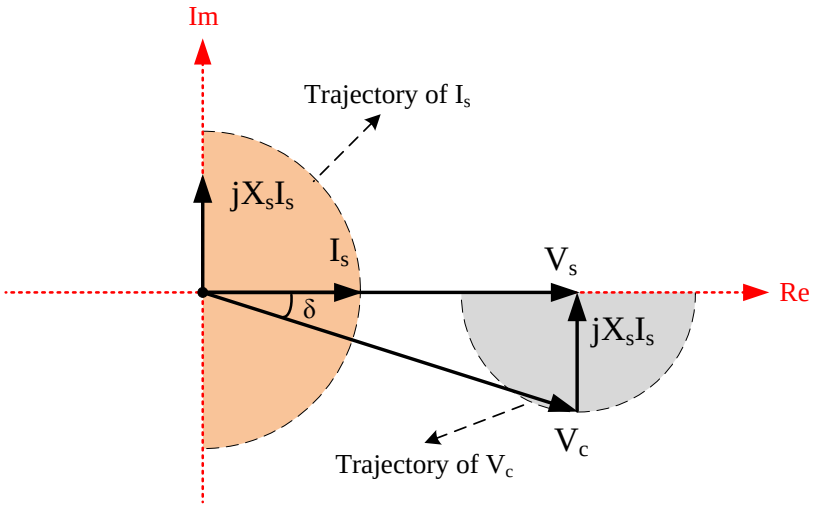
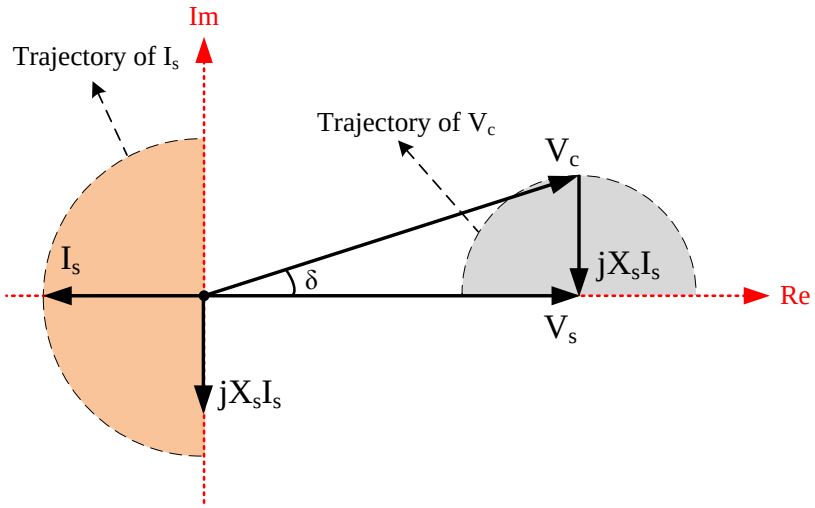


Figure 3.2: Single Line Diagram of the Interleaved Two - Level 4Q Converter

The phasor diagrams corresponding to unity power factor operation for rectification mode and inversion mode for only one converter are shown in Figure 3.3 with supply voltage being taken as the reference phasor [35, 41, 73, 100, 101, and 102]. Same principles are valid for the other converter. Moreover, resistances of series reactor and front-end transformer are neglected for simplicity. The trajectory of the converter output voltage phasor with for each operation mode with varying phase angle and constant magnitude of line current is also illustrated.



(a)



(b)

Figure 3.3: Phasor Diagrams for:
(a) Rectification Mode of Operation, (b) Inversion Mode of Operation

As seen in Figure 3.3, it is possible to control active and reactive power in both directions. First and fourth quadrants of the complex plane correspond to inversion and rectification modes, respectively, in terms of converter output voltage phasor.

3.3. Operation Principles and Modes

By the utilization of the single line diagram and the phasor diagram shown in Figures 3.2 and 3.3, active and reactive power transfer can be formulated in terms of control variables (amplitude modulation index, m_a and load angle, δ) as derived in (3.1) to (3.9) for only one converter [35]:

$$\overrightarrow{I_s} = \frac{\overrightarrow{V_s} - \overrightarrow{V_c}}{jX_s} \tag{3.1}$$

$$\overrightarrow{S_s} = \overrightarrow{V_s}\,\overrightarrow{I_{sA}}^{*} \tag{3.2}$$

$$\overrightarrow{S_s} = V_s \left(\frac{V_s - \overrightarrow{V_c}}{jX_s}\right) \tag{3.3}$$

$$\overrightarrow{S_s} = \frac{{V_s}^2 - V_s\,V_c\cos(\delta) - jV_s\,V_c\sin(\delta)}{jX_s} \tag{3.4}$$

$$\overrightarrow{S_s} = \frac{V_s\,V_c\sin(\delta)}{X_s} + j\,\frac{{V_s}^2 - V_s\,V_c\cos(\delta)}{X_s} \tag{3.5}$$

$$\overrightarrow{S_s} = P_s + jQ_s \tag{3.6}$$

$$V_c = \frac{m_a\,V_{dc}}{\sqrt{2}} \tag{3.7}$$

$$P_s = \frac{V_s\,V_{dc}m_a\sin(\delta)}{\sqrt{2}\,X_s} \tag{3.8}$$

$$Q_s = \frac{\sqrt{2}{V_s}^2 - V_s\,V_{dc}m_a\cos(\delta)}{\sqrt{2}\,X_s} \tag{3.9}$$

The derivations are made assuming constant DC link voltage operation. It is clear now that active and reactive power can be controlled with the use of control variables; amplitude modulation index (m_a) and load angle (δ) as seen in (3.8) and (3.9). One other deduction made from this analysis is the significant effect of series reactance to the control system. Usually, only the filtering capability of this reactor is considered during design stage. A higher inductance value corresponds to better filtering since

the impedance seen by any harmonic component having a specific frequency f_h is $X_s = 2\pi f_h L_s$. On the other hand, higher filter inductance is not desired in terms of filter volume, weight and cost in power electronics. On the other hand, selecting the filter inductance very low is also not desired since it affects the sensitivity of the control system as can be seen in (3.8) and (3.9). System controllability should also be taken account in addition to line current harmonics, volume, cost etc. Design of filter inductor will be explained in Chapter 4.

Equations 3.8 and 3.9 have been utilized to obtain the variation of power factor with modulation index and load angle as shown in Figure 3.4. DC link voltage (V_{dc}) of 1800V, supply voltage (V_s) of 1050V and line inductance is 1 mH are used for this simulation.

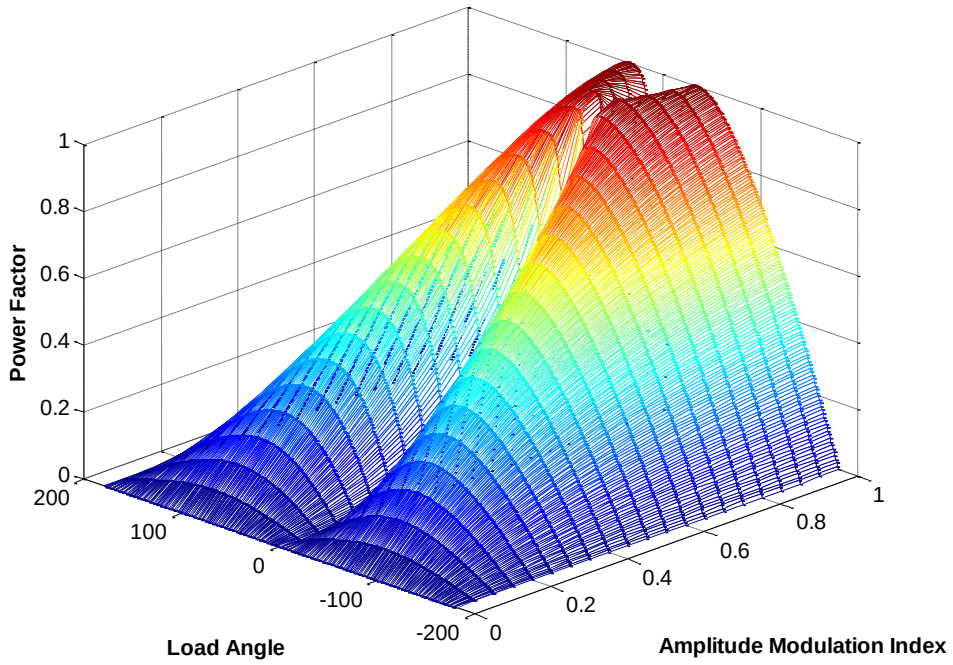


Figure 3.4: Variation of Power Factor with m_a and δ

As shown in Figure 3.4, there are two knaps of the characteristics where power factor gets close to unity (brown area). These two parts correspond to motoring and regenerative braking operation modes. It is also observed that, in the range of power factor values close to unity, load angle does not vary in a wide range unlike STATCOM systems where reactive power compensation is the aim. Amplitude

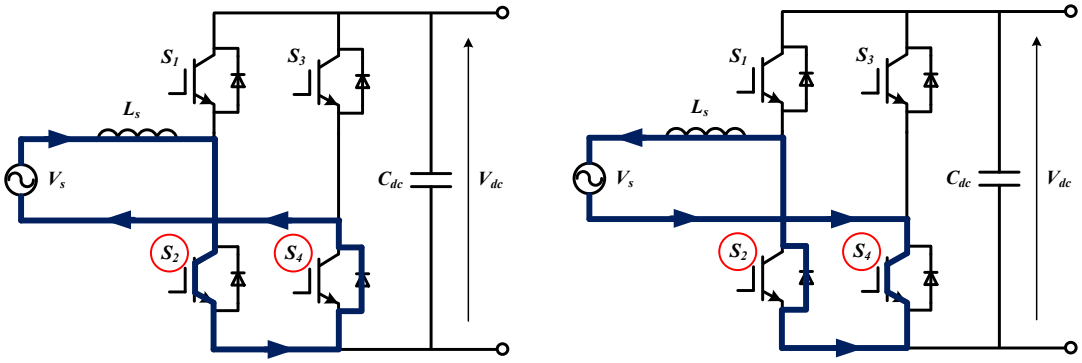
modulation index is to be between 0.8 and 1. These observations are helpful for the design of the control system.

Switching states of a two-level 4Q converter can be seen in Table 3.1.

Table 3.1: Switching States of a Two - Level 4Q Converter

State	**S_1**	**S_2**	**S_3**	**S_4**	**V_c**
1	0	1	0	1	0
2	0	1	1	0	$-V_{dc}$
3	1	0	0	1	$+V_{dc}$
4	1	0	1	0	0

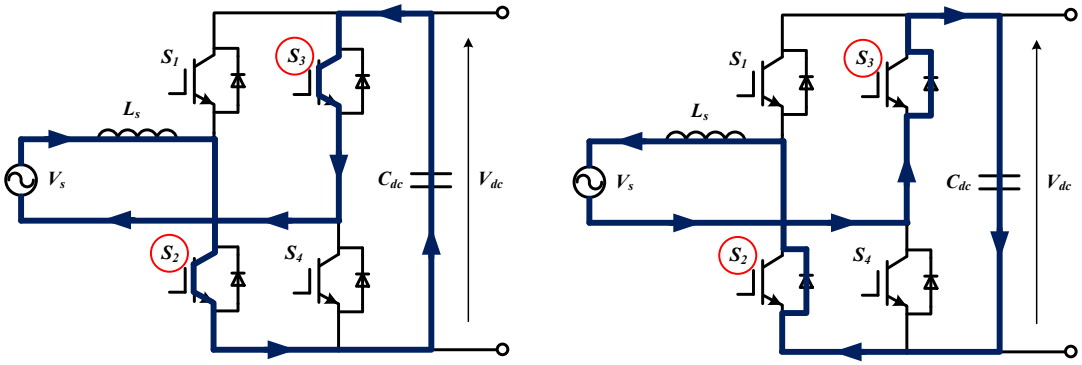
These four states actually correspond to eight modes if both directions of current are considered. These operation modes are shown in Figures 3.5 to 3.8 where active switches are also shown. Another mode definition can be made in terms of the state of the converter. A 4Q converter can be in freewheeling state (FW) where there is no power transfer with the DC link and the series AC reactor is being charged. Second state which is charging state (CH) corresponds to energy storage on the DC link capacitor. Finally, discharging state (DSCH) corresponds to the state where DC link capacitor discharged. These three states are also marked on operation modes shown below.



(a) (b)

Figure 3.5: Two-Level Converter Operation Mode - I & II:

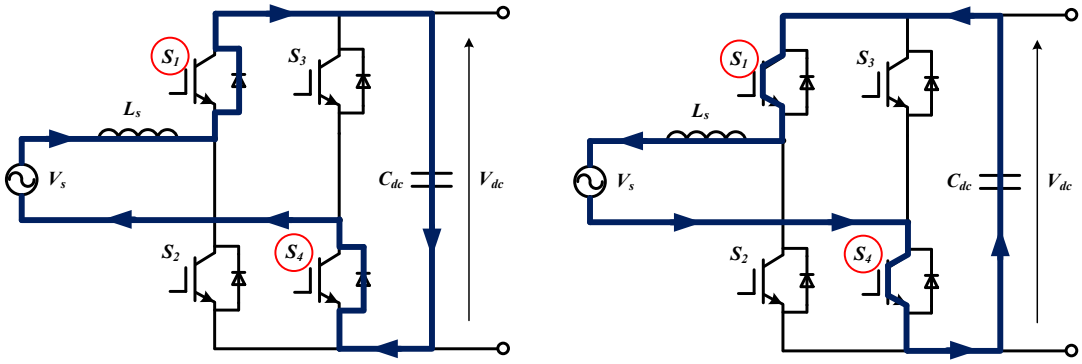
(a) Mode - I (FW State), (b) Mode - II (FW State)



(a) (b)

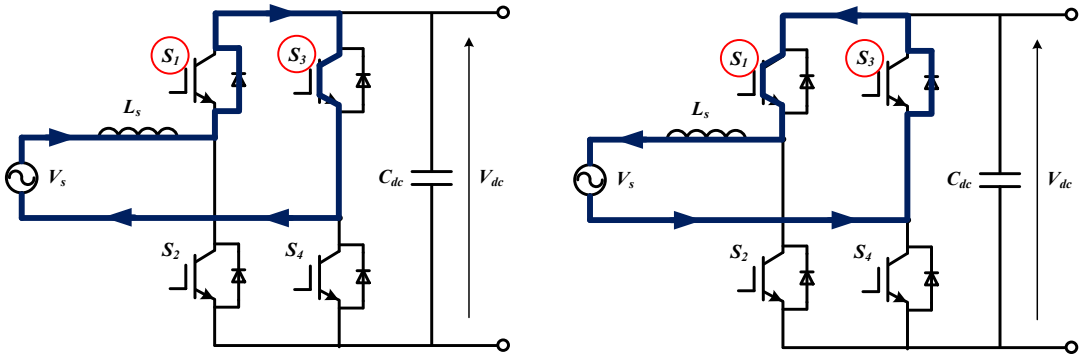
Figure 3.6: Two-Level Converter Operation Mode - III & IV:

(a) Mode - III (DSCH State), (b) Mode - IV (CH State)



(a) (b)

Figure 3.7: Two-Level Converter Operation Mode - V & VI:
(a) Mode - V (CH State), (b) Mode - VI (DSCH State)



(a) (b)

Figure 3.8: Two-Level Converter Operation Mode - VII & VIII:
(a) Mode - VII (FW State), (b) Mode - VIII (FW State)

It is already stated that PWM rectifiers are capable of operating in both directions. So, there are two operation modes: rectification mode and inversion mode [37, 73, and 103]. These two modes correspond to motoring and regenerative braking modes, respectively, in terms of drive characteristics. Analysis of the interleaved two - level converter operation principles will be further discussed for the two distinct modes of operation. The analyses are done for only one two - level converter because same rules are valid for each converter connected in parallel via DC link.

3.3.1. Rectification Mode of Operation

Unity power factor operation of a two - level 4Q converter at rectification mode can be seen in Figure 3.9 [104]. Converter output voltage waveform and its fundamental component, input current and supply voltage are shown in one fundamental cycle of supply voltage. Modes of operation which have been discussed above are shown along with applied gate signals and conduction devices (T denotes IGBT and D denotes antiparallel diode) for each operation mode. In addition, device voltages and current are shown where positive device current corresponds to IGBT current and negative device current corresponds to diode current for each power switch.

Main states of this operation mode are Mode - IV in positive half cycle) and Mode - V in negative half cycle. Motoring mode of operation corresponds to rectification mode of the 4Q converter where diodes are conducting during main states in both half cycles. Auxiliary states (freewheeling states) of this mode are Mode - I and Mode - VII in positive half cycle and Mode - II and Mode - VIII in negative half cycle. There are also two unexpected states which belong to the regenerative braking operation mode which are Mode - III in positive half cycle and Mode - VI in negative half cycle. These modes are present due to the phase difference between supply voltage and converter output voltage (load angle).

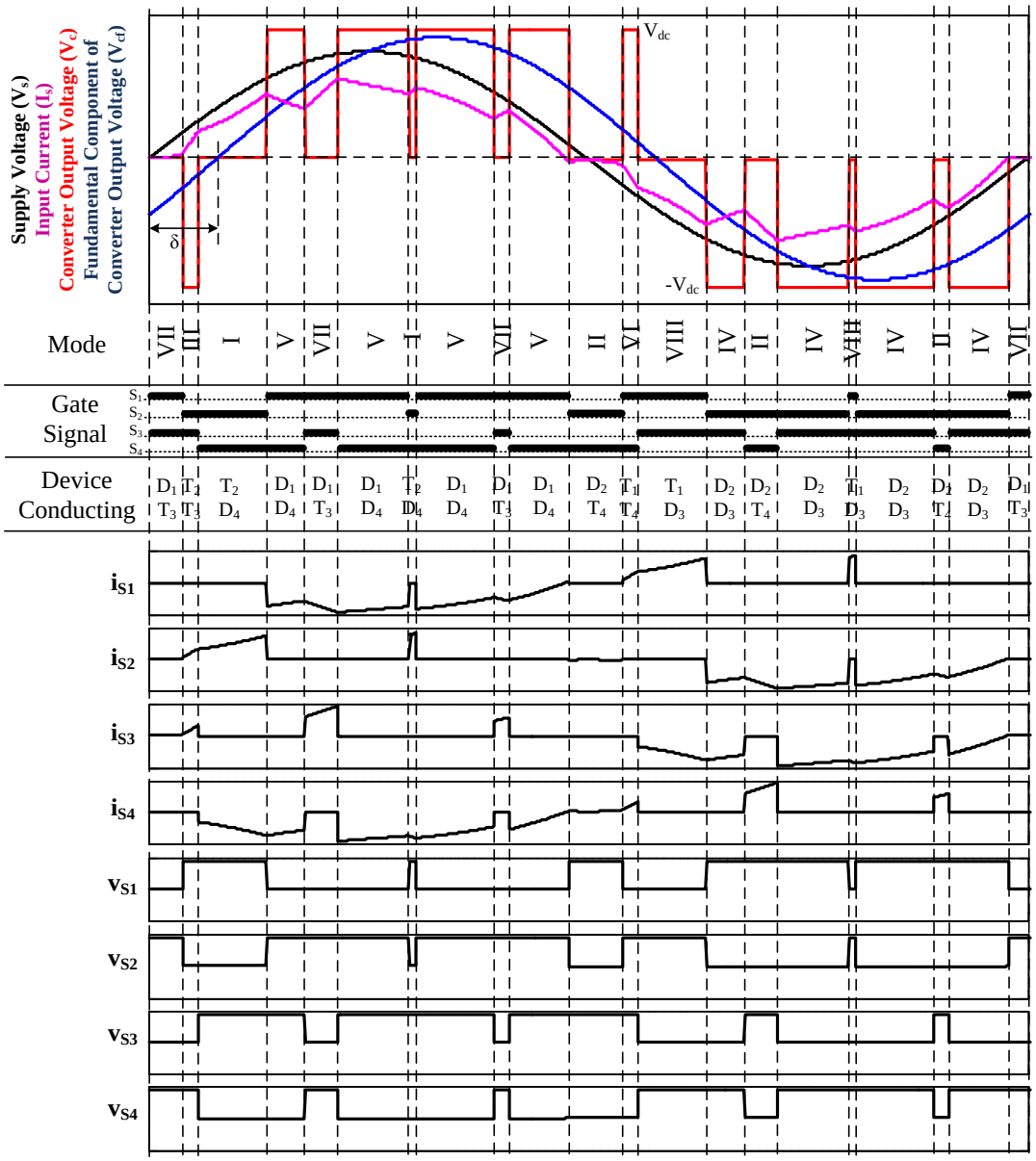


Figure 3.9: Two - Level PWM Rectifier Waveforms during Rectification Mode of Operation

3.3.2. Inversion Mode of Operation

Unity power factor operation of a two - level 4Q converter at inversion mode can be seen in Figure 3.10 [104]. Converter output voltage waveform and its fundamental component, input current and supply voltage are shown for one fundamental cycle of supply voltage. Modes of operation which have been discussed above are shown along with applied gate signals and conduction devices (T denotes IGBT and D denotes antiparallel diode) for each operation mode. In addition, device voltages and current are shown where positive device current corresponds to IGBT current flow and negative device current corresponds to diode current flow for each power switch.

Main states of this operation mode are Mode - VI in positive half cycle) and Mode - III in negative half cycle. Regenerative braking mode of operation corresponds to inversion mode of the 4Q converter where IGBTs are conducting during main states in both half cycles. Auxiliary states (freewheeling states) of this mode are Mode - II and Mode - VIII in positive half cycle and Mode - I and Mode - VII in negative half cycle. There are also two unexpected states which belong to the motoring operation mode which are Mode - IV in positive half cycle and Mode - V in negative half cycle. Just like motoring mode case, these modes are present due to the phase difference between supply voltage and converter output voltage (load angle).

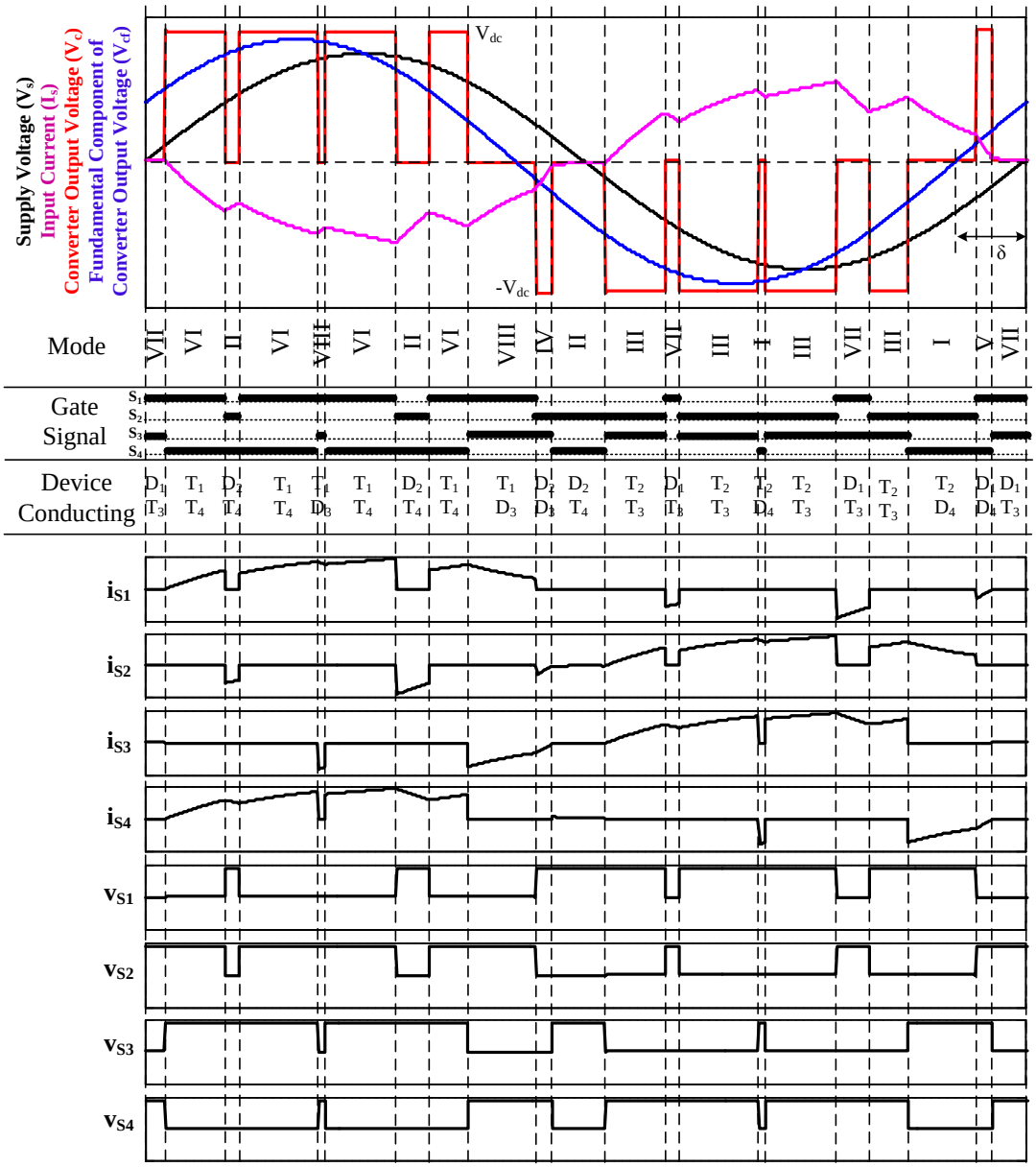


Figure 3.10: Two - Level PWM Rectifier Waveforms during Inversion Mode of Operation

3.4. Control Techniques

The requirements of the PWM rectifier of a locomotive traction system which should be met by the control system can be listed as follows [29]:

- DC link voltage should be kept constant at its set point in all operating modes.
- Unity power factor should be achieved at the supply terminals.
- The line current should be sinusoidal with total demand distortion and individual harmonic content low enough to meet the harmonic distortion standards.
- Dynamic performance should be good.
- Sufficient disturbance rejection should be achieved.
- If reactive power compensation or supply voltage regulation is desired, the system should be able to operate at a desired power factor (generally between 0.8 and 1).

The general structure of the control system is composed of three control loops [62, 102, 105, and 106]; phase locked loop (PLL) where phase information of the supply voltage is extracted, outer voltage loop where DC link voltage is controlled and inner current loop where AC line current is controlled as shown in Figure 3.11.

Phase information of the supply voltage obtained by PLL is used to adjust the power factor of the PWM rectifier and to ensure unity pf operation. Phase of the current reference is set by this PLL output. The output of outer voltage loop is used to set the magnitude of current reference. Simultaneous control of DC link voltage and AC line current is performed as following: When the DC link voltage increases over the set value, the output of the DC Link voltage control loop will be negative causing a lower current reference so that the current drawn from the AC supply will reduce and thus the DC link voltage will get closer to the set point. On the other hand, if the DC link voltage decreases under the set value, this output will be negative causing a higher current reference so that the current drawn from the AC supply will increase and thus the DC link voltage will get closer to the set point.

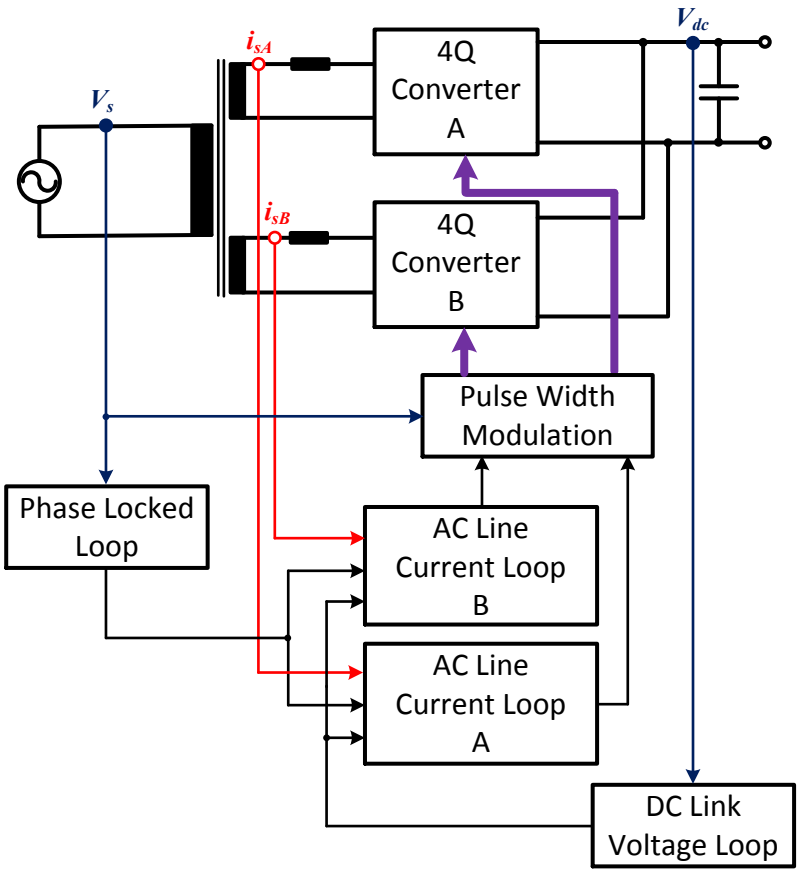


Figure 3.11: Multi-loop Structure of the Interleaved Two - Level PWM Rectifier Control System

Detection of the grid voltage phase where the converter is connected is critical for all grid tied systems like traction systems, photovoltaic system, STATCOM systems etc. In addition, phase detection is not the only issue affecting the PLL design. It is required to be able to reject the disturbances offered by the catenary voltage such as; notches and dips, voltage unbalance, phase loss, frequency variations. The simplest method for the detection of phase of the supply voltage is the conventional zero cross detection method. It is not usually preferred due to the requirement of additional hardware and its vulnerability to supply voltage (catenary) disturbances and software based PLL methods are favored [73]. The general structure of software based PLL is shown in Figure 3.12 and is composed of three major blocks; phase detection (PD), controller or low pass filter (LPF) and voltage controlled oscillator (VCO).

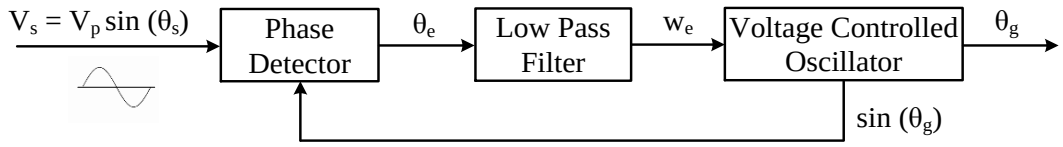


Figure 3.12: General Structure of Software Based PLL

θ_s: Supply Phase, θ_e: Phase Error, θ_g: Generated Phase

PD part detects the phase difference (phase error) between the actual supply voltage and the output signal generator by PLL. Detected phase error is fed to the LPF block which usually contains one gain term and one term with a single pole just like a PI type controller where the high frequency harmonic components are also filtered thanks to the low pass filter structure. VCO generates sine and cosine output signals by using the phase information created by integrating the frequency.

For three phase systems, phase detection is generally achieved by applying reference frame transformation (from stationary frame to synchronously rotating reference frame) to the three phase supply voltage set. For single phase systems, as in locomotive traction system case, it is not possible to apply this method directly because only one phase is attainable and can be measured. To be able to apply reference frame transformation, methods based on generating an imaginary phase which is orthogonal to the single phase catenary voltage have been employed. The simplest form of this additional phase generation is to apply a 90^0 phase delay to the original voltage phase. Even though it is easy to implement, this technique lacks reliability due to its slow response. Another technique is to use an all-pass filter (APF) for the generation of the orthogonal phase with same amplitude, transfer function of which is shown in (3.10). The amount of phase delay can be calculated as in (3.11) where w_s is the supply fundamental frequency and w_c is the characteristic frequency and should be the same as the catenary frequency (50 Hz) for the required phase delay [73].

$$H(s) = -\frac{s - w_c}{s + w_c} \tag{3.10}$$

$$\Phi = -2\,tan^{-1}\left(\frac{w_s}{w_c}\right) \tag{3.11}$$

Another method for the generation of the orthogonal phase is using an Orthogonal Signal Generator (OSG) as shown in Figure 3.13. Two sinusoidal signals phasors of which are orthogonal to each other are created where V_α is in-phase with the supply voltage and V_β is 90^0 lagging from it at steady state. These two components can be utilized for reference frame transformation application. The generation of orthogonal signals from the supply voltage is achieved by the transfer functions shown in (3.12) and (3.13) where w_s is the supply frequency in rad/sec.

$$H_\alpha(s) = \frac{V_\alpha}{V_s} = \frac{kw_s s}{s^2 + kw_s s + {w_s}^2} \tag{3.12}$$

$$H_\beta(s) = \frac{V_\beta}{V_s} = \frac{k{w_s}^2}{s^2 + kw_s s + {w_s}^2} \tag{3.13}$$

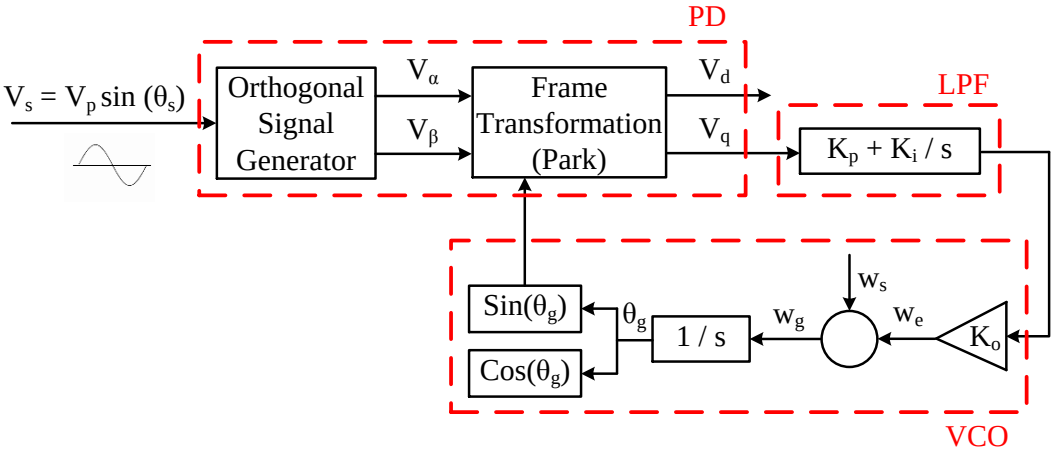


Figure 3.13: PLL with OSG Based Phase Detection

Rather than reference frame transformation, phase detection can also be achieved by multiplying the original phase voltage and phase voltage output of the PLL as shown in Figure 3.14. When the two sinusoidal signals (measured and generated) are multiplied as shown in (3.14), the result contains two terms; a constant term carrying

the phase error information and a sinusoidal term frequency of which is the sum of the supply frequency and generated frequency as shown in (3.15). Frequency of this sinusoidal component is 100 Hz when the generated phase is equal to the supply phase at steady state. This additional component may create oscillations on the succeeding blocks and affect proper operation. A notch filter (band-stop filter) tuned to 100 Hz is usually employed at the output of phase detection block to avoid undesired oscillations as shown in Figure 3.15.

$$V_p \, sin(\theta_s) \, sin(\theta_g) = \frac{1}{2}\left[\cos(\theta_s - \theta_g) - \cos(\theta_s + \theta_g)\right] \tag{3.14}$$

$$V_p \, sin(\theta_s) \, sin(\theta_g) = \frac{1}{2}\left[\cos(\theta_e) - \cos(2\pi(f_s + f_g)t)\right] \tag{3.15}$$

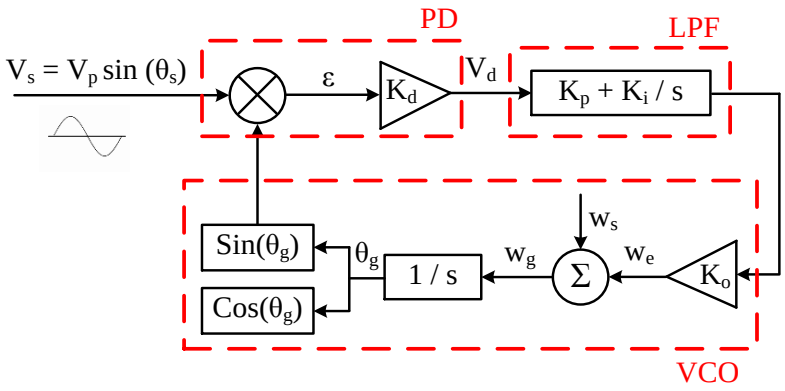


Figure 3.14: Phase Detection by Multiplying Original and Generated Voltages

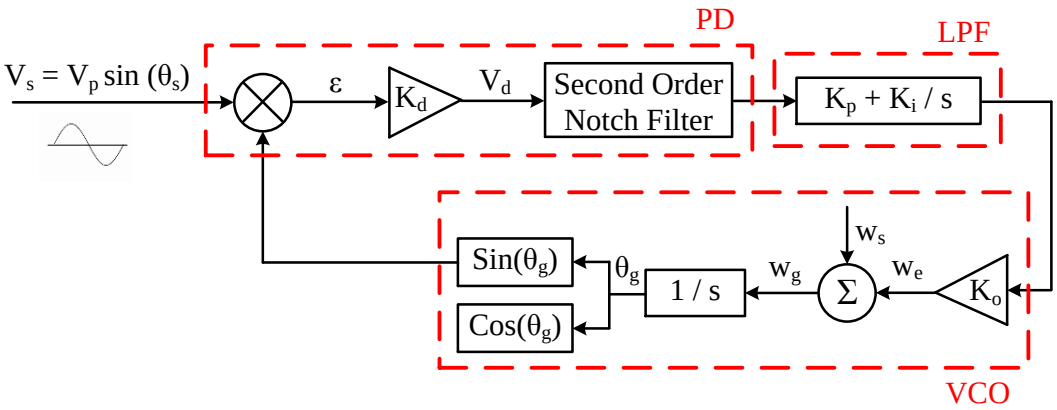


Figure 3.15: Utilization of Notch Filter in PLL to Avoid 100 Hz Oscillations

DC link voltage control loop contains a proportional-integral (PI) type regulator almost always as shown in Figure 3.16. It is usually designed to be slower than the AC current loop. As discussed previously, DC link voltage naturally contains a second harmonic component and this component is usually filtered by a series LC resonant filter tuned to 100 Hz. Nonetheless, the high frequency oscillation center frequency of which is twice the switching frequency usually follows an envelope of 100 Hz frequency component regardless of how small it is. This second harmonic component is reflected to the whole control system when DC link voltage is measured and may cause oscillations at the AC current magnitude leading to low order harmonics and the worst of all, even harmonics, presence of which are strictly restricted by the current harmonic distortion standards. To overcome this, a notch filter (band-stop filter) tuned to exactly 100 Hz which is also often utilized in PLL as discussed before is usually used on the outer voltage loop [58, 73, 75, and 105]. Transfer function of a typical notch filter is shown in (3.16).

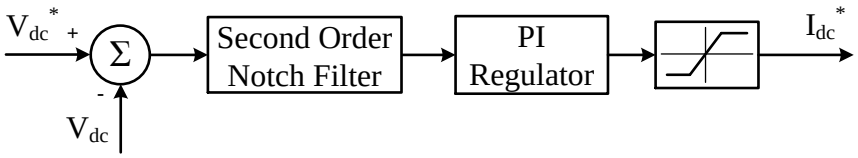


Figure 3.16: DC Link Voltage Control Loop Employing Band Stop Filter

$$V_p \, sin(\theta_s) \, sin(\theta_g) = \frac{1}{2}\left[\cos(\theta_s - \theta_g) - \cos(\theta_s + \theta_g)\right] \qquad (3.16)$$

AC current control can be implemented by various techniques. First of all, it can be controlled as a sinusoidal waveform which is called linear current regulator. Advantages of this technique are good transient performance and ease of implementation. Another method, which is originally employed in three phase converters, is current control based on DQ0 transformation. With this technique, sinusoidal quantities are transferred to a reference frame which is synchronously rotating at the supply frequency detected by PLL. Therefore, they can be controlled

as constant DC quantities. A set of AC currents can be decomposed into its active and reactive components and hence these components can be controlled independently. As in single phase PLLs, this technique also requires the generation of an orthogonal phase from the measured single phase current to be used in the reference frame transformation. Furthermore, the response of this technique in PWM rectifier systems is much slower than linear current control technique. Current control techniques in PWM Rectifiers of main line locomotive traction systems will be further discussed in the next section.

To improve the dynamic performance of the control system supply voltage is used as a feed forward signal before PWM operation and added to the modulating signal in all types of current control methods. Secondary purpose of this feed forward is to ensure that disturbances created by grid voltage (changes in magnitude, phase and low order harmonic content) are taken into account by the control system [58, 84].

3.4.1. Linear Current Regulator

The most common current controller used in PWM rectifiers of main line locomotive traction systems is per phase, linear current regulator thanks to its good dynamic performance and ease of implementation. As the name suggests, current of each converter is controlled as an AC quantity (sinusoidal waveform tracking). Block diagram of the control system based on linear current regulator is shown in Figure 3.17 [101].

Due to the fact that line current is controlled as its original sinusoidal waveform at every PWM cycle, the response of this type of control is fast and its transient performance is good compared to other types of current control. On the other hand, it requires sinusoidal waveform tracking which has its own demerits. Linear current control can be implemented by two different types of controller: Proportional-Integral (PI) current controller and Proportional Resonant (PR) current controller.

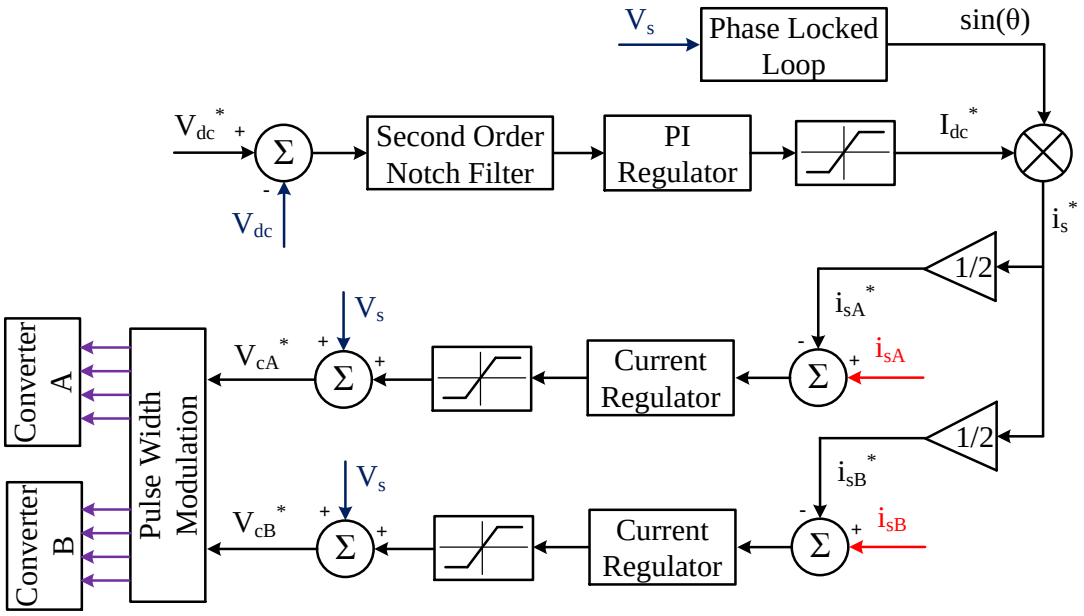


Figure 3.17: Control Block Diagram of PWM Rectifier Based on Linear Current Regulator

3.4.1.1. Current Control Based on PI Regulators

The Current Regulator block in the current control loop is usually replaced by PI type regulators as in DC link voltage control loop. The transfer function of a PI regulator is shown in Equation 3.17.

$$G_c(s) = K_p + \frac{K_i}{s} \tag{3.17}$$

The problem with the traditional PI regulators on the inner loop is the steady state error on the phase of the AC line current due to sinusoidal waveform tracking. Because of this steady state error, unity power factor operation cannot be completely achieved [105]. Another drawback of the PI current regulators is poor disturbance rejection performance. For better dynamic performance, the AC supply voltage is directly fed to the control system at the output of the current control loop as a feed forward as

mentioned before. If the supply voltage contains low order harmonics (3rd, 5th, 7th etc.), the control system with PI current regulators cannot achieve strong rejection of these harmonic components and these components are reflected to the line current [105].

3.4.1.2. Current Control Based on PR Controllers

PR type regulators can be used instead of PI controllers to eliminate the steady state error at the AC line current and to achieve exactly unity power factor operation [74, 76, 77, 100, and 107].

The transfer function of an ideal PR regulator can be seen in Equation 3.18 where w_o is the resonance frequency which is $2\pi 50 \approx 314$ rad/sec for AC line current control at supply fundamental frequency.

$$G_c(s) = K_p + \frac{2K_i s}{s^2 + {w_0}^2} \tag{3.18}$$

Ideally, the second order pole creates an infinite gain at the resonance frequency to achieve zero steady state error. However, its bandwidth is too narrow and may cause stability problems in digital control systems. Therefore it should be damped somehow. A practical PR controller, transfer function of which is shown in Equation 3.19, has been developed to overcome the instability problem [105, 108]. The bandwidth around the resonance frequency is widened and the gain which was theoretically infinite is damped. The trade-off between damping and bandwidth can be adjusted by the parameter w_c, which is called the cut-off frequency.

$$G_c(s) = K_p + \frac{2K_i w_c s}{s^2 + 2w_c s + {w_0}^2} \tag{3.19}$$

In order to illustrate this, frequency response of PR regulators for both the ideal and practical cases at different cut-off frequencies have been obtained as can be seen in Figure 3.18.

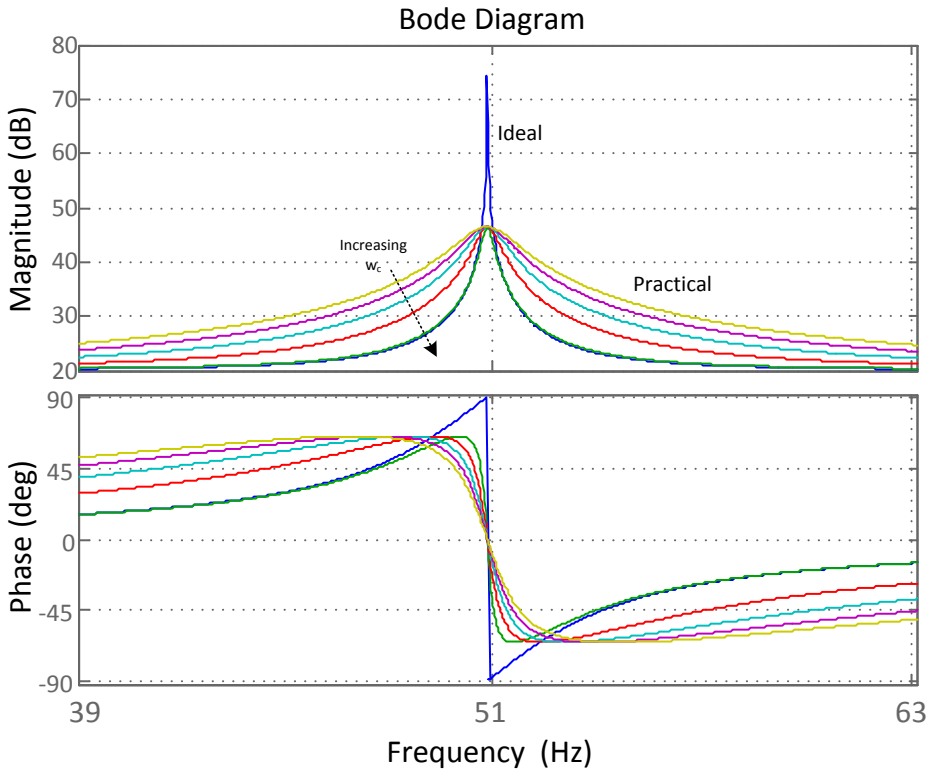


Figure 3.18: Frequency Response of PR Regulators for Ideal and Practical Cases

PR regulators can also be utilized to eliminate harmonic components at specific orders by using additional resonant loops tuned to the frequencies of selected harmonics as shown in Figure 3.19 [105, 107]. The resultant transfer function is shown in Equation 3.20 where h is the order of selected harmonic components.

$$G_c(s) = K_p + \frac{2K_i s}{s^2 + {w_0}^2} + \sum_{h=3,5,7\ldots} \frac{2K_{ih} s}{s^2 + (hw_0)^2} \qquad (3.20)$$

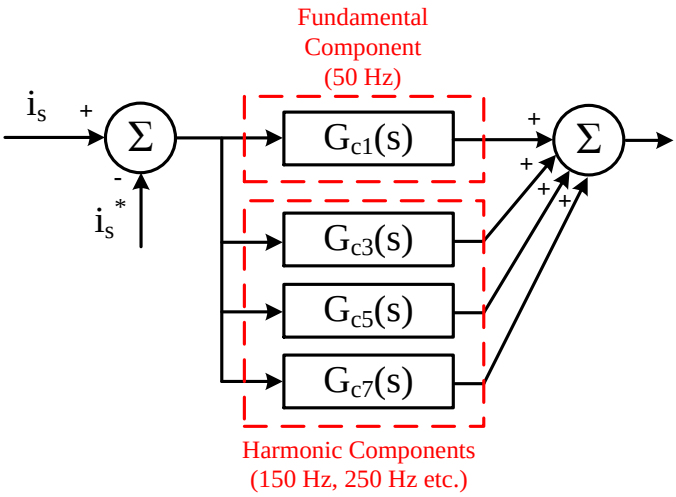


Figure 3.19: Harmonic Elimination with PR Regulators

3.4.2. Control Based on Synchronously Rotating Reference Frame

Instead of controlling the line current as its original sinusoidal waveform, it can be controlled with constant DC quantities by applying reference frame transformation [80, 81 and 82]. For a three phase system, the measured set of currents which are originally on stationary reference frame can be transformed into the synchronously rotating reference, rotational speed of which is determined by the PLL; i.e., supply voltage frequency. The resultant components which are orthogonal to each other represent active and reactive parts of the three phase current set. This method is commonly utilized in three phase converters because per phase linear current regulator technique would require separate controllers for each phase, however only two controllers will be required if frame transformation is applied. This method can also be adapted to a single phase system as in the case of single phase PLL explained before.

The advantages of this technique are the independent control of active and reactive power as DC quantities, zero steady state error and hence unity power factor operation and good disturbance rejection. On the other hand, this method has the disadvantages

of being complex and difficult to implement compared to linear current regulator, the necessity of orthogonal signal generation as the system is single phase and slow dynamic response.

The block diagram of the control system with current control based on synchronously rotating reference frame is shown in Figure 3.20 [81].

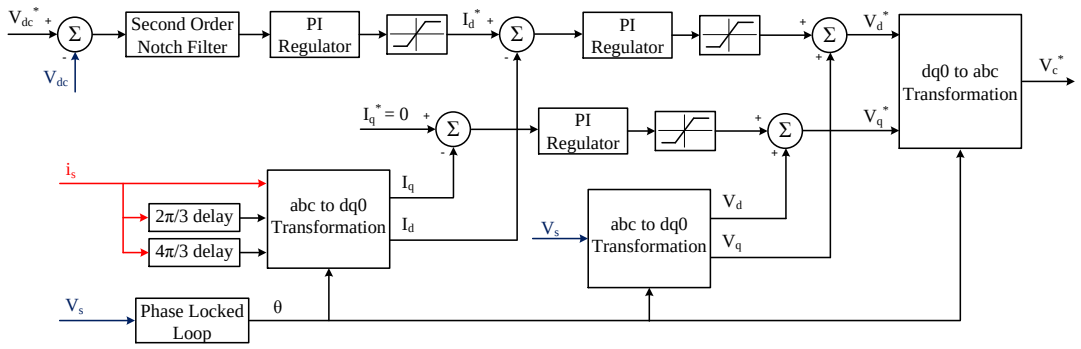


Figure 3.20: Control Block Diagram of PWM Rectifier with Current Control Based on Synchronously Rotating Reference Frame

In single phase systems like locomotive traction systems, such a control technique is not widely used since the transformation requires a minimum of two independent phases in the system. The frame transformation can be achieved by either creating an imaginary phase orthogonal with the original phase with techniques such as OSG as discussed in PLL techniques or applying a phase delay to the original phase as shown in Figure 3.20 which leads to slower response.

Position of the reference frame to which the measured current will be transformed is determined by the phase output of PLL. If the system is successfully synchronized with the grid, resultant D and Q components will represent active and reactive components of the line current, respectively. As in the case of linear current control regulators, the output of the DC link voltage control loop is used as the reference of active component of the line current. The reference of Q component is usually set to zero for unity power factor operation (no reactive power transfer). The two currents are controlled as DC quantities simply with PI regulators. To add the supply voltage

as a feed forward to improve the dynamics of the system, it should be transformed to the synchronously rotating reference frame as shown in Figure 3.20. However, since D and Q components of the supply voltage are already generated in PLL block if one of the PLL methods based on reference frame transformation is used, they can be used directly for feed forward purposes. The resultant components are transformed back to the original stationary reference frame to obtain the modulating signal which is achieved by inverse DQ0 Transformation.

The DQ0 and Inverse DQ0 Transformations which are also mentioned as Park Transformation and Inverse Park Transformation, respectively, are performed as shown in the phasor diagram in Figure 3.21. Supposing a set of three phase currents are represented as in (3.21), the transformation of this set (abc) to αβ0 is achieved as in (3.22) which is often called Clarke's Transformation. The transformation of αβ0 to dq0 is also implemented as in (3.23). The overall transformation from abc to dq0 will therefore be as in (3.24). The inverse Park Transformation from dq0 to abc is also shown in (3.25).

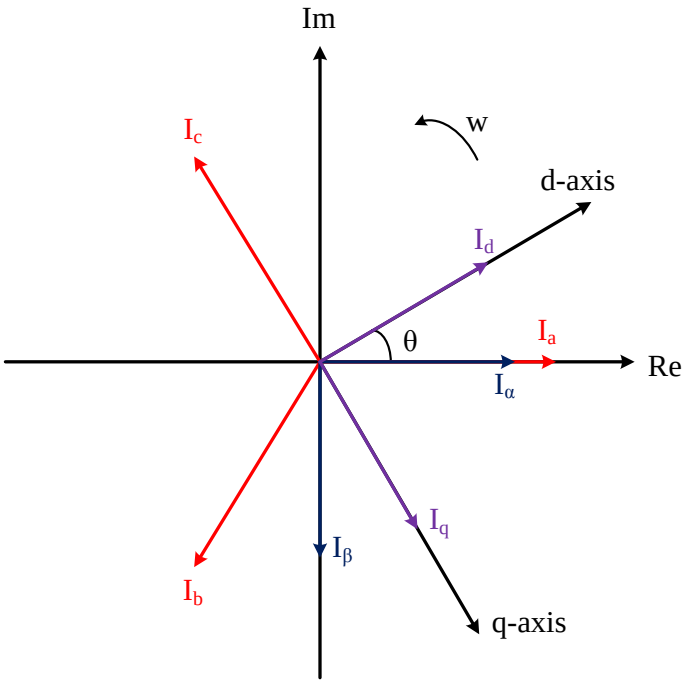


Figure 3.21: Phasor Diagram of the Reference Frame Transformation

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} \cos(wt) \\ \cos(wt - {}^{2\pi}/_{3}) \\ \cos(wt - {}^{4\pi}/_{3}) \end{bmatrix} \tag{3.21}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} 1 & -{}^{1}/_{2} & -{}^{1}/_{2} \\ 0 & {}^{\sqrt{3}}/_{2} & -{}^{\sqrt{3}}/_{2} \\ {}^{1}/_{2} & {}^{1}/_{2} & {}^{1}/_{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.22}$$

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) & 0 \\ \cos(\theta) & -\sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} \tag{3.23}$$

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} \cos(\theta) & \cos(\theta - {}^{2\pi}/_{3}) & \cos(\theta + {}^{2\pi}/_{3}) \\ \sin(\theta) & \sin(\theta - {}^{2\pi}/_{3}) & \sin(\theta + {}^{2\pi}/_{3}) \\ {}^{1}/_{2} & {}^{1}/_{2} & {}^{1}/_{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.24}$$

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos(\theta - {}^{2\pi}/_{3}) & \sin(\theta - {}^{2\pi}/_{3}) & 1 \\ \cos(\theta + {}^{2\pi}/_{3}) & \sin(\theta + {}^{2\pi}/_{3}) & 1 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} \tag{3.25}$$

3.4.3. Reactive Power Control

In most common control techniques applied to PWM Rectifiers, line current is controlled directly and power factor is controlled indirectly. Some methods can be developed where reactive power, and hence power factor, is directly controlled although such technique have not been used in main line locomotive traction systems yet.

In grid connected power converters, usually there exist three control variables: DC link voltage (V_{dc}), amplitude modulation index (m_a) and load angle (δ). As discussed previously, locomotive traction systems with voltage source converters employ constant DC link voltage operation and hence V_{dc} cannot be a control variable and

should be a *controlled* variable. A block diagram showing a control technique developed based on direct control of the reactive power is shown in Figure 3.22 [83].

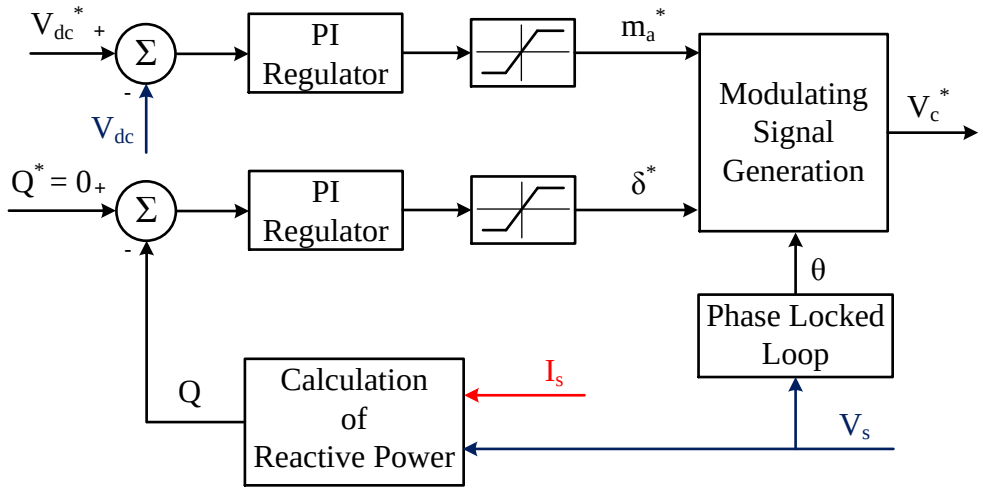


Figure 3.22: Block Diagram of the Control Technique Based on Direct Reactive Power Control

This method can be considered an alternative to the current control technique based on synchronously rotating reference frame if line current is not to be controlled with sinusoidal waveform tracking. The advantage of this is that cycle based control where control variables are calculated only once in a fundamental cycle of the supply frequency can be applied. On the other hand, this technique has proven to have poor dynamic performance.

3.5. Pulse Width Modulation Techniques

Output voltage of a power converter is established by switching of power semiconductor devices. The widths of each pulse present on this voltage waveform, and hence the time of each switching event, is determined by Pulse Width Modulation (PWM) block of the control system. Control variables that have been presented so far

are utilized for PWM operation [85]. Therefore, it is safe to say that the realization of converter output voltage waveform calculated during the control loops is achieved with PWM techniques.

In the past, PWM had been implemented with analogue circuits. With the advance in the digital electronics technology, single chip microprocessors dedicated to this type of applications have been used [76, 89]. The best example is Digital Signal Controllers (DSCs) architecture of which employs Digital Signal Processors (DSPs). Today, DSCs are widely used in several applications of power converters such as, photovoltaic systems, motor drive systems and electric traction systems. Enhanced Pulse Width Modulation (ePWM) modules involved in DSPs offer easy and flexible implementation [56, 109].

3.5.1. Sinusoidal Pulse Width Modulation

The most common PWM method used in single phase PWM rectifiers is Sinusoidal PWM (SPWM) thanks to its simplicity [89]. It is implemented by comparing a sinusoidal reference signal (the modulating signal) with one or more carrier signals (usually a triangular or saw-tooth waveform) to generate the pulses to be applied to the power switch gates the most simple of which is shown in Figure 3.23.

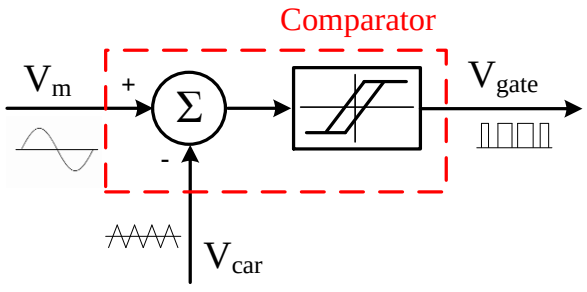


Figure 3.23: Implementation of SPWM with One Carrier Signal

In DC/DC converters, the only variable controlled during PWM operation is the duty cycle which is constant at steady state. On the other hand, SPWM has a more complex structure since the waveform to be crated is a sinusoidal waveform. In one fundamental cycle of the supply frequency, duty cycle has to be changed even at steady state. In addition to duty cycle, two definitions have been made for SPWM method useful for the design: amplitude modulation index (m_a) and frequency modulation index (m_f) [28, 110] equations of which are shown in (3.26) and (3.27), respectively, for a single phase system where V_m is the modulating signal, V_{car} is the carrier signal.

$$m_a = \frac{\widehat{V_m}}{\widehat{V_{car}}} \tag{3.26}$$

$$m_f = \frac{f_{car}}{f_m} \tag{3.27}$$

The magnitude of the fundamental component at the PWM rectifier output voltage is determined by amplitude modulation index. If the peak value of the carrier signal is adjusted to V_{dc}, m_a is usually set between 0 and 1 for linear modulation. If m_a is set to higher than 1, fundamental component of the output voltage changes nonlinearly with modulation index which is called the over-modulation region. There is also a point apart from which the output voltage cannot be increased; i.e., maximum utilization of the DC link voltage is achieved. That point corresponds to the square wave operation [110]. The modulation regions of single phase SPWM obtained by computer simulations (m_f = 10) are shown in Figure 3.24. Usually, over-modulation region is not used and the control system range is arranged such a way that the whole range of operation is in linear region. It is due to the fact that low order odd harmonics (3^{rd}, 5^{th} etc.) show up in over-modulation region.

Frequency modulation index sets the switching frequency to be applied to the rectifier. Thus, the harmonic content (frequency and magnitude) is actually determined by this index. For the simplest SPWM operation shown in Figure 3.23, harmonics only appear around the switching frequency and its multiples if linear modulation is assured [110].

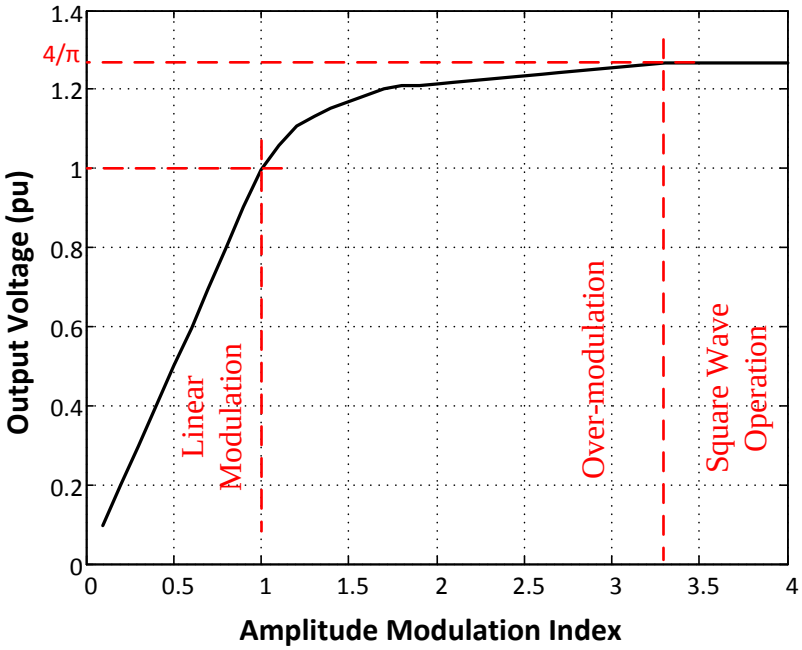


Figure 3.24: SPWM Modulation Regions

In VSC applications, a pair of complementary signals is used to drive one bridge arm (half bridge) as in PWM rectifier case. An appropriate amount of dead band should be introduced between these two PWM signals so that the two power switches on the same bridge arm are ensured not to be ON state simultaneously leading to a short circuit of the DC link [89].

3.5.1.1. Unipolar SPWM

In single-phase applications, SPWM technique can be further classified as: Unipolar SPWM and Bipolar SPWM [28, 90, and 110]. Unipolar SPWM is implemented with the use of two out-of-phase carrier signals or two out-of-phase modulating signals and the two half bridge arms are switched independently resulting in a unipolar output voltage waveform. A sample unipolar SPWM application is shown in Figure 3.25 and the harmonic spectrum of the resultant rectifier output voltage can be seen in Figure

3.26 with m_a = 0.8 and m_f = 10. As seen on the harmonic spectrum, the center frequency of the first harmonic group appears at twice the switching frequency.

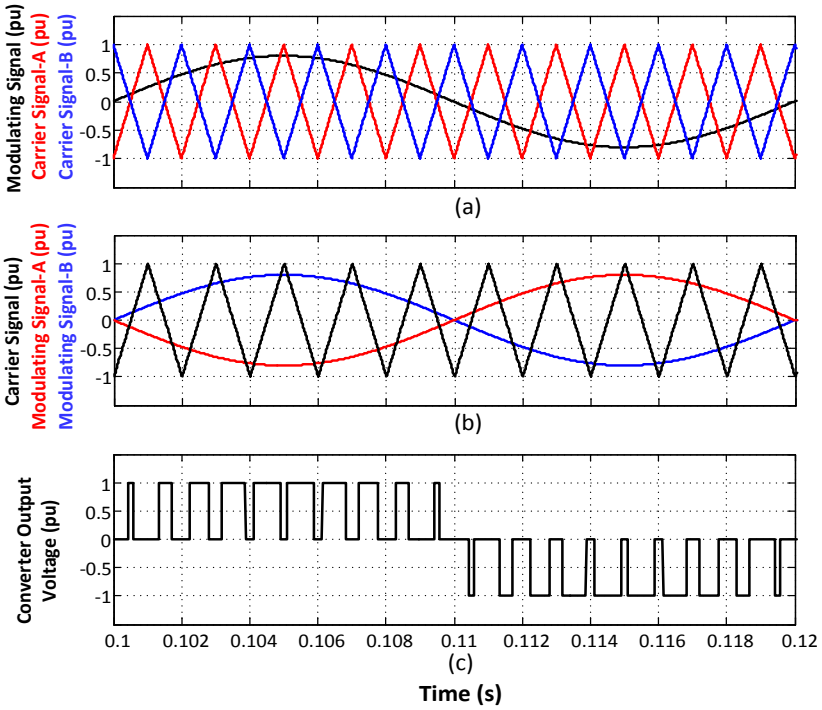


Figure 3.25: Application of Unipolar SPWM: (m_a = 0.8 and m_f = 10)

(a) Two Carrier Signals and One Modulating Signal

(b) One Carrier Signal and Two Modulating Signals

(c) Resultant Output Voltage (Scaled to V_{dc})

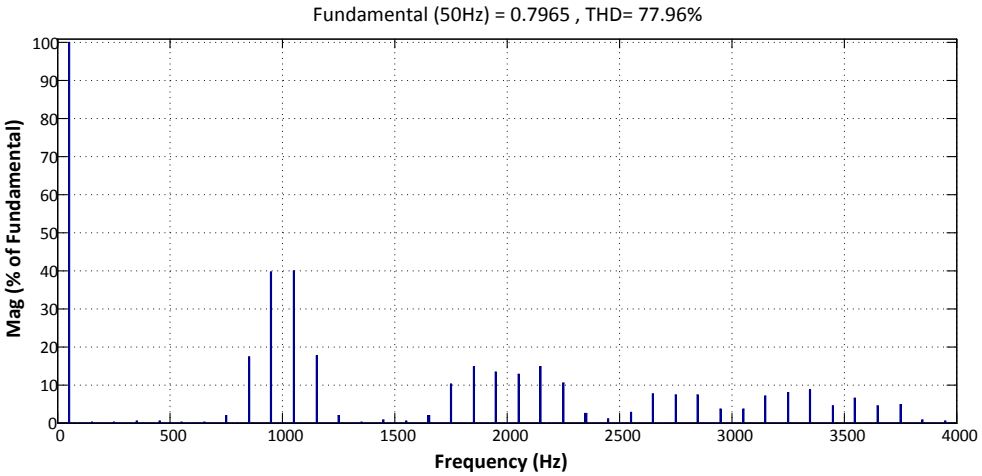


Figure 3.26: Harmonic Spectrum of Rectifier Output Voltage with Unipolar SPWM (m_a = 0.8 and m_f = 10)

3.5.1.2. Bipolar SPWM

Bipolar SPWM is the simplest form of SPWM applications where only one modulating signal and one carrier signal are used which results in a bipolar output voltage waveform.

A sample bipolar SPWM application is also shown in Figure 3.27 and the harmonic spectrum of the resultant rectifier output voltage is shown in Figure 3.28 with the same modulation indices used in unipolar SPWM. Output voltage harmonics appear around the switching frequency and its multiples.

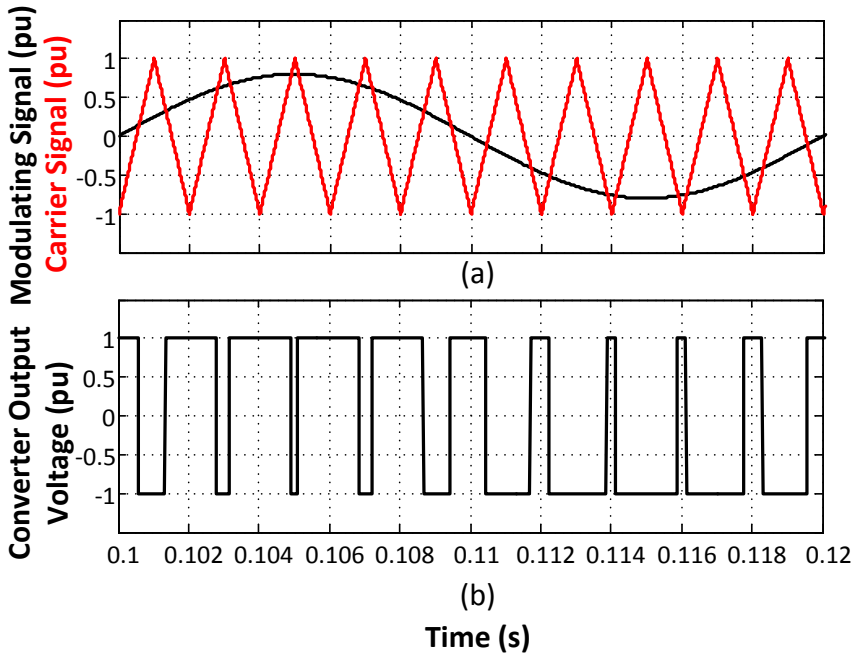


Figure 3.27: Application of Bipolar SPWM: (m_a = 0.8 and m_f = 10)
(a) Carrier Signal and Modulating Signal
(b) Resultant Output Voltage (Scaled to V_{dc})

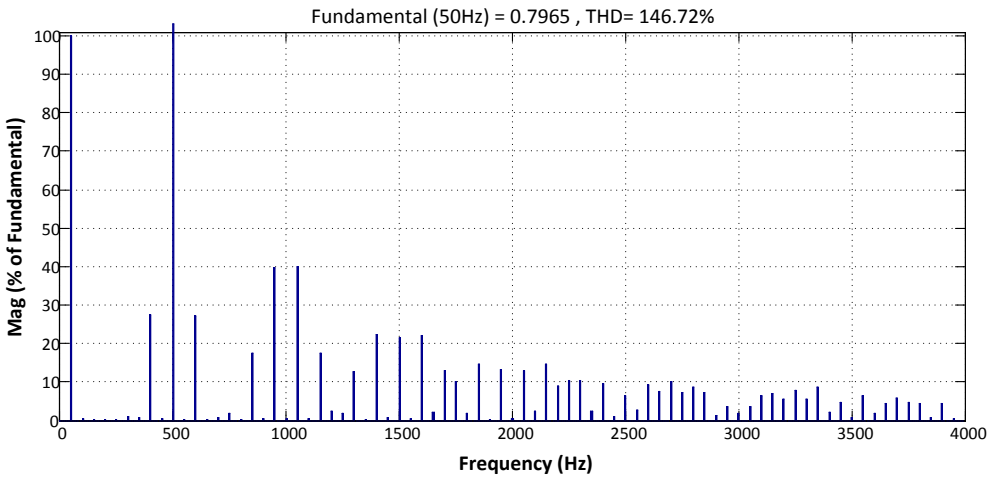


Figure 3.28: Harmonic Spectrum of Rectifier Output Voltage with Bipolar SPWM (m_a = 0.8 and m_f = 10)

3.5.1.3. Phase Shifted SPWM

PWM methods introduced so far are applicable for single phase two-level 4Q converters. With unipolar SPWM method, line current harmonic distortion standards can be complied successfully. Interleaved connection of two 4Q converters makes phase-shifted SPWM possible to apply by which harmonic distortion of the line current can be drastically reduced on line current [58].

The method is applied with the utilization of carrier signals for each converter that are not in-phase, but phase-shifted. The phase shift angle between two converters is determined from (2.14), n being the number of converters connected to the front-end transformer. If two 4Q converters are interleaved and supplied by the same transformer, the phase shift angle is found to be 90^0. Therefore, four carrier signals 90^0 apart from each other are used for two interleaved 4Q converters.

As mentioned before, the center frequency of the first harmonic group is twice the switching frequency for one 4Q converter operated with unipolar SPWM technique. With the application phase shifted SPWM method for two interleaved converters, the harmonic components for each 4Q converter around this frequency cancel each other out due to the fact that these harmonic appear out-of-phase with each other. Thus, for the line current (at the primary side of the traction transformer), the center frequency of the first harmonic group is doubled and appears at four times the switching frequency. THD of this current at the primary side is much less than of each individual converter (around one quarter) and thanks to that, lower switching frequencies can be applied to meet the harmonic distortion requirements leading to better converter efficiency.

The harmonic cancellation occurs on the DC link, too. The center frequency of the harmonics on the DC link current also appears at four times the switching frequency with phase-shifted SPWM technique. This yields a reduction for the DC link capacitance requirement as the peak-to-peak ripple voltage on the DC link is dependent on the harmonic content of the DC link current.

A sample phase-shifted SPWM application is shown in Figure 3.29 under the same conditions used in unipolar and bipolar SPWM. The harmonic spectrum of the line current is shown this time, in Figure 3.30 to illustrate the harmonic cancellation. It is shown that the harmonics first appear at 2 kHz which is four times the switching frequency.

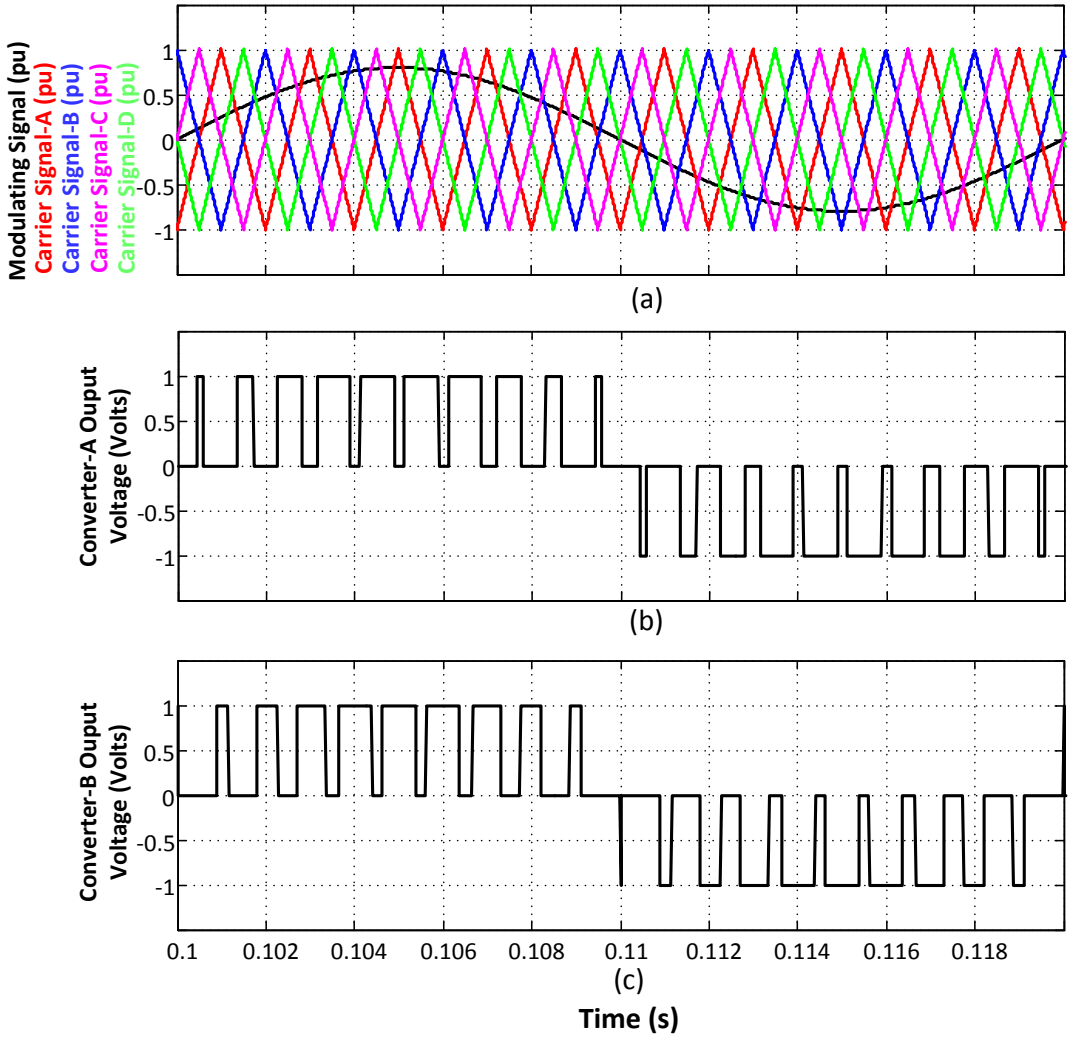


Figure 3.29: Application of Phase-Shifted SPWM: (m_a = 0.8 and m_f = 10)

(a) Carrier Signals and Modulating Signal

(b) Resultant Output Voltage of Converter-A (Scaled to V_{dc})

(c) Resultant Output Voltage of Converter-B (Scaled to V_{dc})

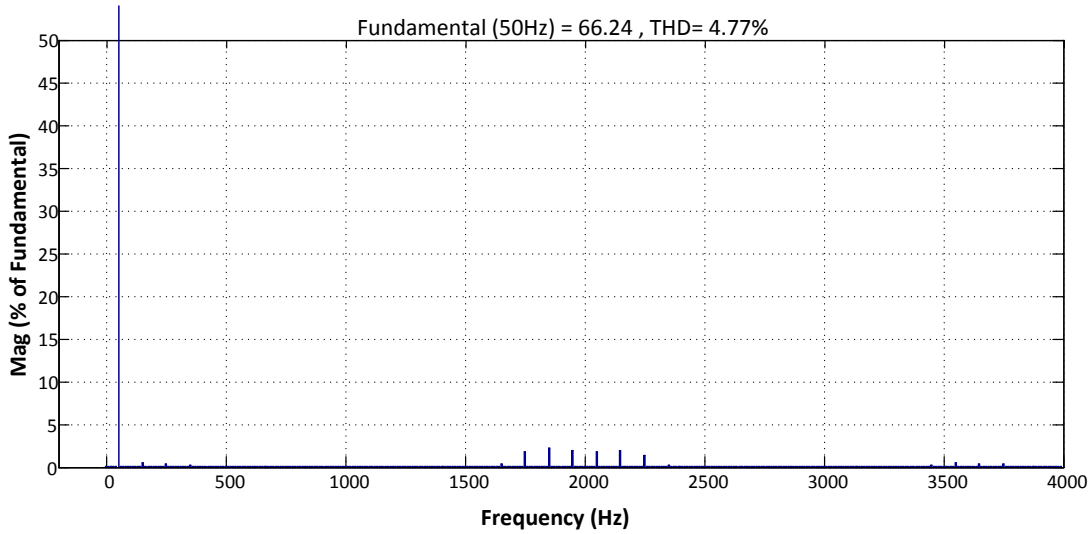


Figure 3.30: Harmonic Spectrum of Line Current with Phase-Shifted SPWM (L_s = 1 mH, m_a = 0.8 and m_f = 10)

3.6. Discussions

PWM rectifier topology selection has already been made and the operation principles and modes of the interleaved two – level converter have been introduced. Furthermore, control and PWM techniques suitable for this application are presented. Among the single phase PLL techniques analyzed in detail, OSG based PLL is used for this application which does not require the elimination of the second harmonic with notch filters and has good dynamic performance. DC link voltage control is implemented with conventional PI regulators design of which is presented in Chapter 4. Among the current control techniques, per phase linear current regulator seems to be the most appropriate selection for its superior dynamic performance. Current control performed on synchronously rotating reference frame is also analyzed, but it requires the generation of orthogonal phase and it has slow transient response. Linear current regulator with both PI and PR regulator is implemented in this research work to observe their performance and to show the elimination of steady state error which causes reactive power flow when PR controllers are used. Single phase PWM techniques are also analyzed and unipolar SPWM technique is selected due to its

ability to double the frequency of the first harmonic group. Phase shifted SPWM is also implemented by which the TDD on the line current can be reduced by a factor of 2.

CHAPTER 4

DESIGN OF INTERLEAVED 4Q CONVERTER BASED PWM RECTIFIER

4.1. Introduction

In this chapter, design of an interleaved two-level PWM rectifier will be performed for use in a main line locomotive traction system. The locomotive has a total of 5 MW output power and is composed of four DC link converters connected to separate secondary windings of a traction transformer and supplying four traction motors each of them having 1.25 MW of rated output power. Design of only one DC link converter is considered in this work which is composed of a rectifier, DC link and traction inverter.

As expressed before, the PWM rectifier should meet the requirements below:

- Supplying a constant DC link voltage with acceptable ripple for the proper operation of traction inverter.
- Operating at unity power factor.
- Being able to operate in both directions. In other words, supplying the braking energy back to the catenary line.
- Drawing or injecting current to the catenary line with harmonic content complying IEEE Std. 519-1992.

- Being able to operate at a desired power factor (in the range of 0.8 - 1.0) power reactive power compensation or catenary voltage regulation purposes if necessary.
- Good transient performance against the disturbances emerging from both the motor side and the catenary side.

These requirements have been considered as a guideline during the PWM rectifier design procedure. The design methodology followed in this research and development work consists of several phases. First of all, the system parameters of the main line locomotive have been listed and the technical specifications of the design have been revealed along with the operation range of the system. Systems parameters to be used as constraints (efficiency, harmonic content etc.) of the design procedure have been selected and their limits have been specified. The parameters (switching frequency, passive elements etc.) affecting these constraints have been discovered. Then, power semiconductor devices, the most fundamental elements of the system have been selected. With the utilization of computer simulations carried out on MATLAB/Simulink environment and numerical analyses performed using MATLAB tool, impacts of the system parameters with the selected power switches have been observed and design of these parameters have been performed. The control system design has been achieved with the use of system model and based on traditional control design procedures. Both steady state and transient state performance of the system have been considered. With the selected parameters during the design phase, efficiency analysis of the system has been carried out. Analytical and numerical methods have been derived for the calculation of each loss component.

The simulation results presented in Chapter 5 will be based on the design considerations given in this chapter. The design of a small scale laboratory prototype and the corresponding experimental results will be presented in Chapter 6.

4.2. Design Specifications

The PWM rectifier topology has been chosen as the interleaved 4Q converter for its advantages such as; redundancy, good harmonic distortion performance and reduction on the current rating of power. It should be noted that, one two-level 4Q converter is operated with half of one DC link converter power and thus a total of eight secondary windings is required on the input traction transformer. During the design phase, only the power stage shown in Figure 4.1 is considered rated output power of which is 1.25 MW.

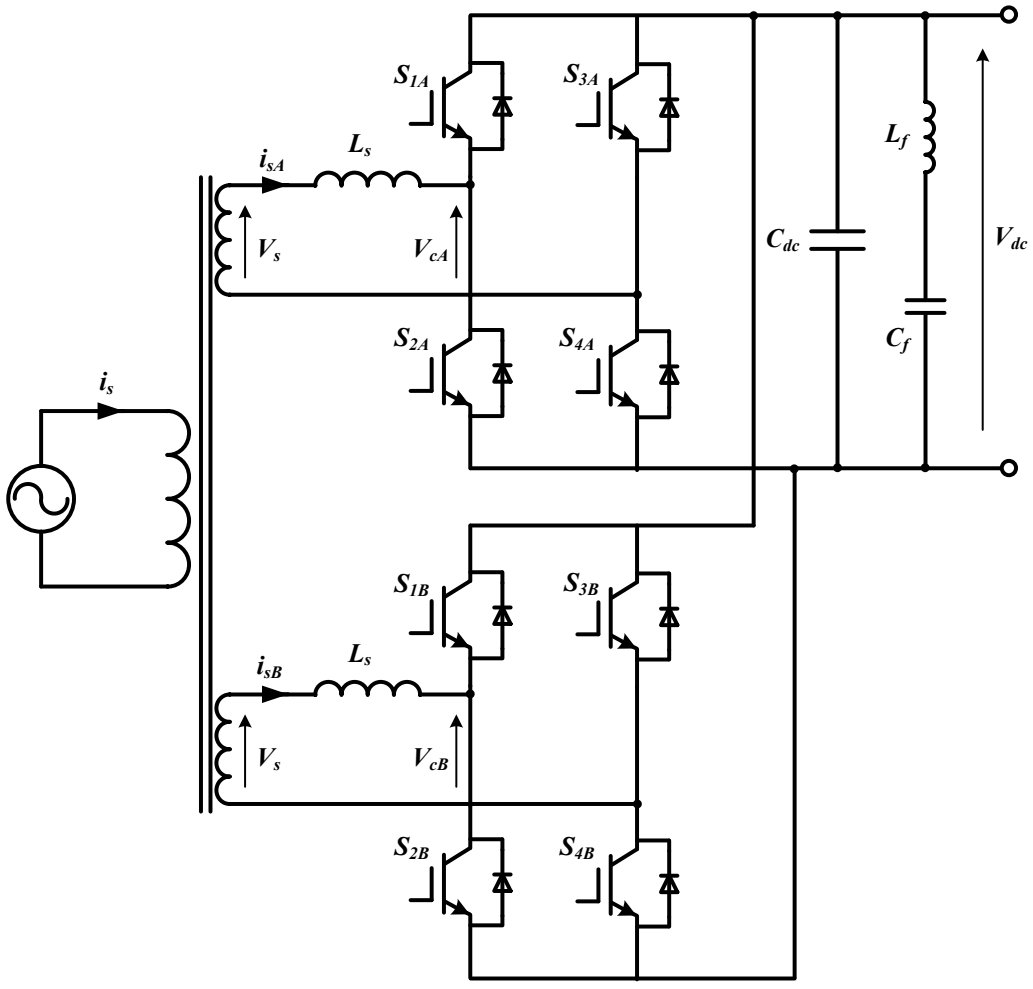


Figure 4.1: Power Stage of the PWM Rectifier Used for the Design Procedure

The technical specifications of the PWM rectifier shown in Figure 4.1 are given in Table 4.1. These parameters are to be used throughout the design procedure unless otherwise specified.

Table 4.1: Technical Specifications of the PWM Rectifier

Rated Output Power	1.25 MW
Catenary Voltage	25 kV
Rated Line Frequency	50 Hz
Transformer Secondary Voltage	1050 V
DC Link Voltage	1800 V
Input Power Factor	1.0
Input current for Each Converter	600 A

The operation range of the system is between -1.25 MW (rated power during regenerative braking mode of operation) and +1.25 MW (rated power during motoring mode of operation).

The system is to be able to operate at unity power factor and constant DC link voltage. Moreover, the system constraints considered during the design phase are; TDD on the line current (primary side of the input transformer), system efficiency and peak-to-peak voltage ripple on the DC link. In addition, transient performance of the system is also considered during the design procedure with indices of settling time, rise time, maximum overshoot and minimum undershoot.

The limits specified for the selected system parameters during the PWM rectifier design phase are shown in Table 4.2. TDD constraint on the line current is chosen to comply with the harmonic distortion standards. In Table 4.3, the system parameters to be designed which affect the selected system requirements are listed. Design of DC link series LC filter tuned to the second harmonic component is considered separately since the specified constraints are not directly affected by this component.

Table 4.2: The Limits Specified for the System Parameters

System Parameter	Limit
TDD of the Line Current	5 %
Overall Efficiency	98.5 %
Peak-to-peak DC Link Voltage Ripple	1.5 %

Table 4.3: Parameters to Be Designed

Parameter	Range
Switching Frequency (f_{sw})	300Hz - 800Hz
AC Line Inductance (L_s)	0.5mH - 1.5mH
DC Link Capacitance (C_{dc})	3mF - 6 mF

4.3. Selection of Power Semiconductor Devices

Power semiconductor device candidates to be used in this work have been introduced and their features have been discussed in Chapter 1. IGBTs have proven to be advantageous for use in high power locomotive traction application thanks to their benefits such as; commercial availability with voltage and current ratings suitable for this particular application, being suitable for voltage source type converters as they are voltage controlled devices, easy gate drive, no turn-on or turn-off snubber requirement and reduced volume and weight compared to other device types.

Voltage and current ratings of the power devices (IGBT and anti-parallel diode) are determined by computer simulations. In Figure 4.2, voltage waveforms of power devices are shown for a full cycle of the fundamental supply frequency for only one 4Q converter. Current waveforms of IGBTs and anti-parallel diodes are also shown in Figure 4.3 and 4.4, respectively.

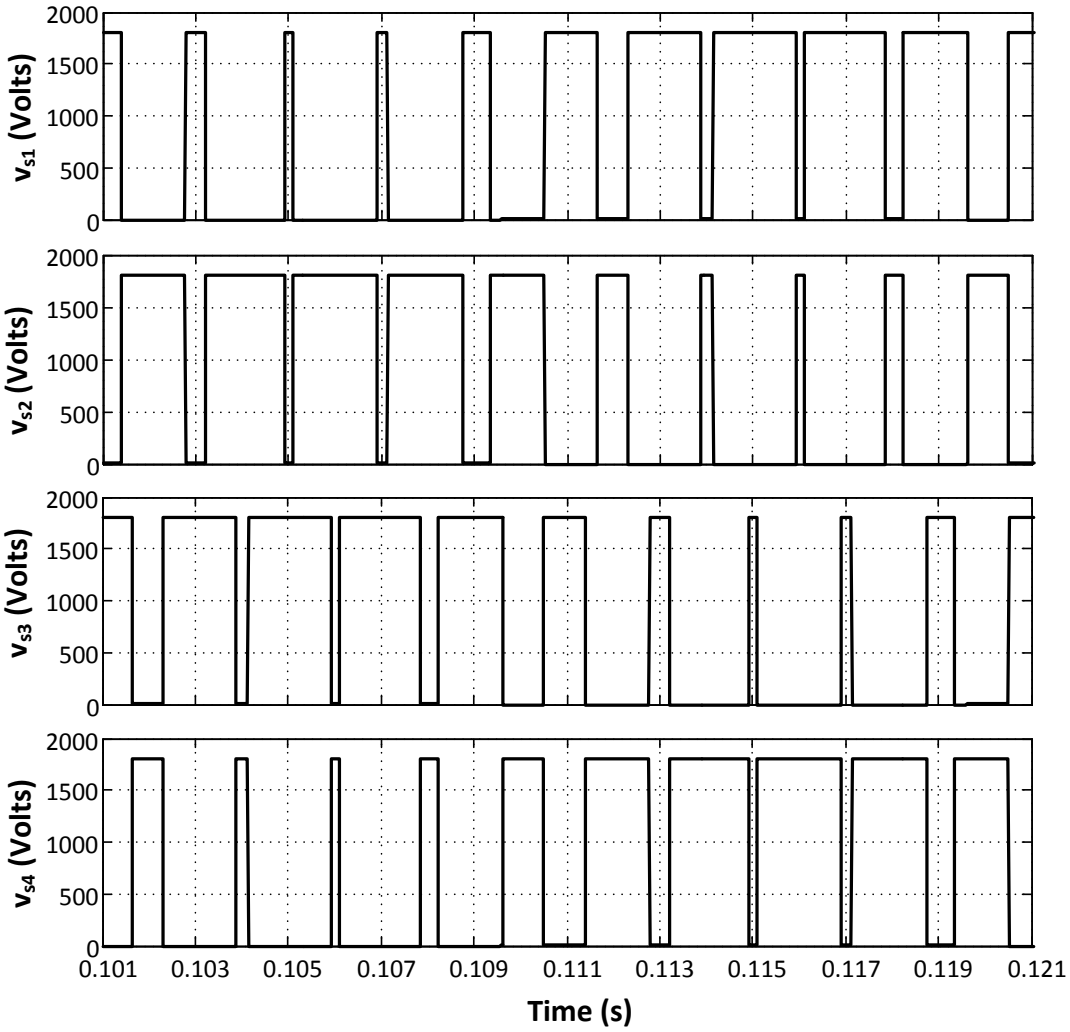


Figure 4.2: Voltage Waveforms of Power Devices for One 4Q Converter

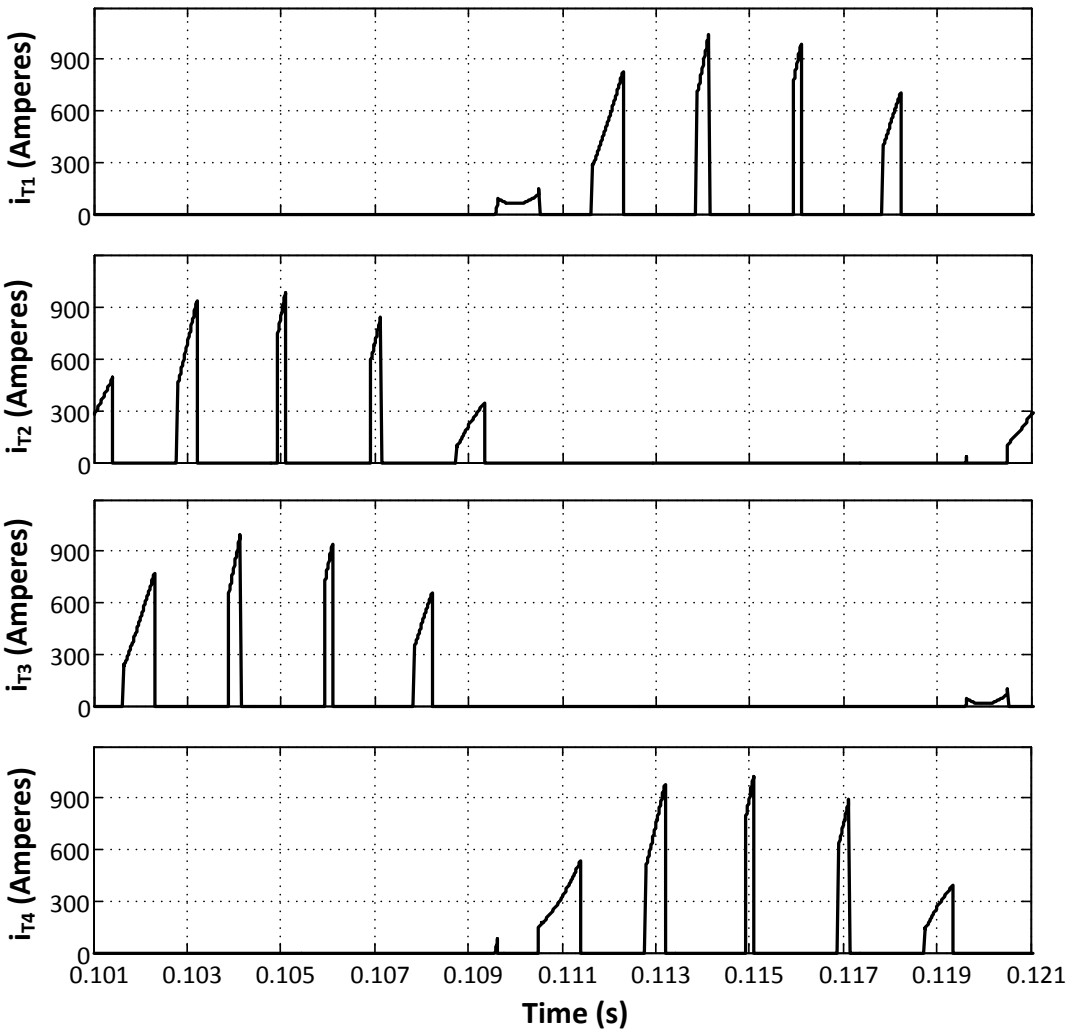


Figure 4.3: Current Waveforms of IGBTs for One 4Q Converter

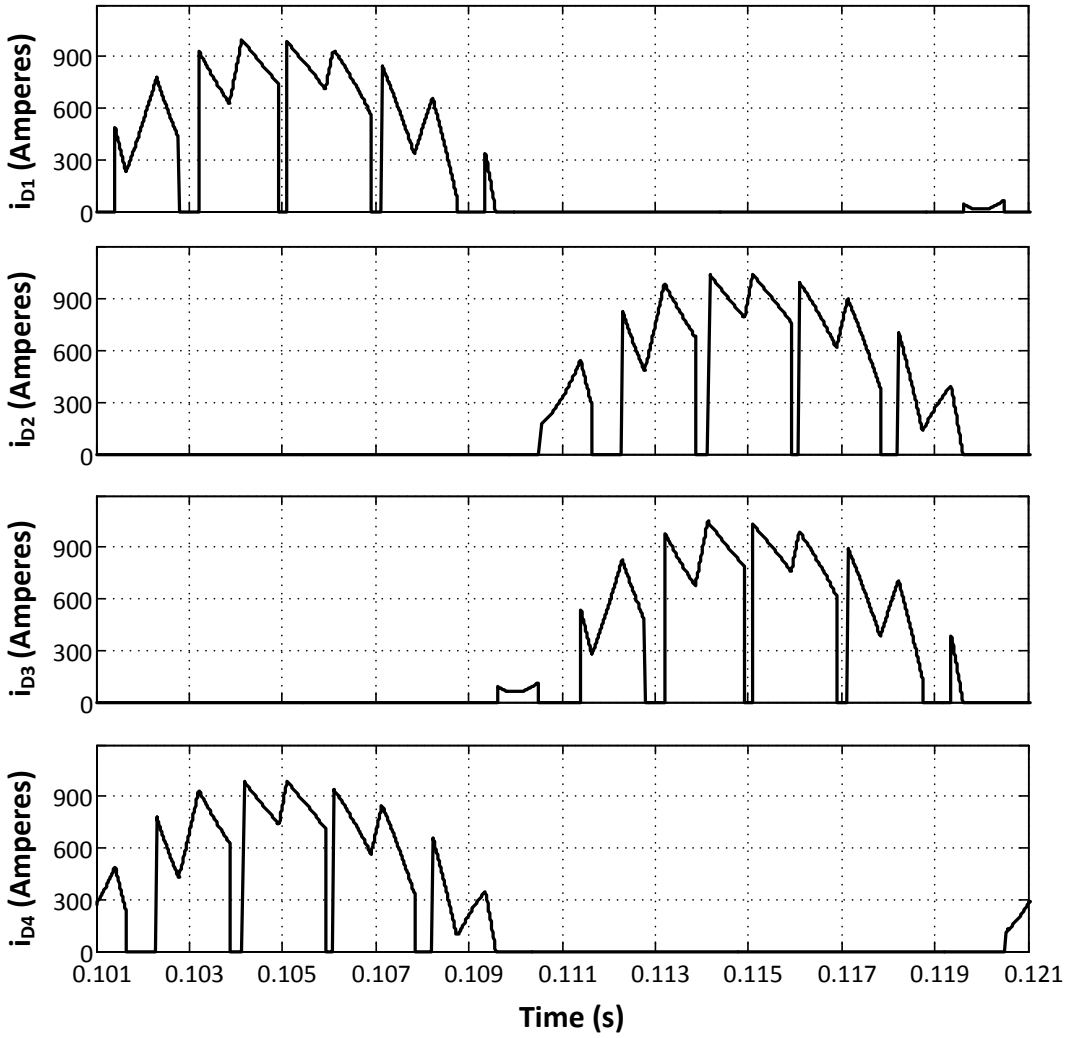


Figure 4.4: Current Waveforms of Anti-parallel Diodes for One 4Q Converter

The peak value of the switch voltage is 1800 V as expected assuming ideal switching. Stray inductances of the semiconductor modules, DC link capacitor and DC bus bar also affect the selection of power device voltage rating. During turn-off of an IGBT, the sudden change on the stray inductance current gives rise to the switch voltage above the DC link voltage amount of which can be calculated as in (4.1) where. Due to this phenomena and other possible increase on the DC link in the permissible range, voltage rating of the power semiconductor modules is usually selected to be higher than 1.5 times of the nominal DC link voltage which is 2700V in this case. The closest blocking voltage rating of a commercially available IGBT module is 3300V.

$$V_T = V_{dc} + L_{stray}\, {di}/{dt} \tag{4.1}$$

The IGBT current peak value is found as 1100A and RMS is found as 170A. The diode current has same peak value and RMS value of 415A. Since the system is on motoring mode in this simulation, the converter operates on rectifying mode. Therefore, diode currents should be taken into account for the design. It will not be an overdesign for IGBTs because the results will reverse when the converter operates in inversion mode (regenerative braking). Based on these findings, the closest current rating to be selected is 1200A.

CM1200HC-66H HVIGBT module from Mitsubishi is selected as the power semiconductor device important characteristics of which are shown in Appendix A section [111]. Parameters of this power module are shown in Table 4.4. Power switch selection is also verified by use of the safe operating areas specified for both IGBT and diode shown in Appendix A section. In addition, IGBT voltage rise due to the stray inductance shown in (4.1) is calculated for the worst case (peak of the transistor current) assuming a maximum of 200 nH stray inductance (including IGBT module, DC link capacitor and DC bus bar) as in (4.2) and using the total turn-off time as the sum of rise time and fall time given in Table 4.4.

$$V_T = 1800 + 200 \times 10^{-9} \times \frac{1050}{3.5 \times 10^{-6}} = 1860\ V \tag{4.2}$$

Table 4.4: Parameters of Selected Power Module (CM1200HC-66H) [111]

Blocking Voltage (V_{CES})	3300V
Continuous IGBT Current (I_C)	1200A
Pulsed IGBT Current (I_{CM})	2400A
Continuous Diode Current (I_E)	1200A
Pulsed Diode Current (I_{EM})	2400A
Saturation Voltage of IGBT ($V_{CE\text{-}sat}$) @1200A	3.3V
On State Voltage of Diode (V_{EC}) @1200A	2.8V
Turn-on Delay Time ($t_{d\text{-}on}$)	1.6 μs
Turn-off Delay Time ($t_{d\text{-}off}$)	2.5 μs
Turn-on Rise Time (t_r)	1.0 μs
Turn-off Fall Time (t_f)	1.0 μs
Turn-on Switching Energy (E_{on})	1.60 J
Turn-off Switching Energy (E_{off})	1.55 J
Reverse Recovery Time (t_{rr})	1.4 μs
Reverse Recovery Energy (E_{rr})	0.90 J
Stray Inductance (L_{stray})	10 nH

4.4. Selection of Switching Frequency

It has already been discussed that relatively low switching frequencies (up to 800 Hz) are used in high power locomotive traction applications [112, 113]. Interleaved connection and phase shifted operation of two 4Q converters enable further reduction of the switching frequency due to its superior TDD performance on the line current [58].

Selection of the PWM switching frequency actually affects the whole performance of the rectifier system. First of all, harmonic distortion on the AC line current and DC link current directly depend on it which means switching frequency affects sizes

of passive filters. Additionally, switching loss of the IGBTs and reverse recovery loss of anti-parallel diodes, and hence the system efficiency, are affected by switching frequency. Cooling system is designed based on the power device losses. Thus, it is safe to say that switching frequency determines the cooling system and affects system volume.

AC side of the system can be modelled for any harmonic component denoted by h as shown in Figure 4.5. The current for any frequency component is determined by the voltage drop on the series reactor as shown in (4.3). Assuming an ideal catenary line with no harmonic distortion; i.e., $V_{s-h} = 0 \ \forall h$, any harmonic component of the line current depends on the frequency of this harmonic, magnitude of the converter output voltage at this harmonic frequency and the line inductance. THD of the current of one 4Q converter can therefore be formulated as in (4.4).

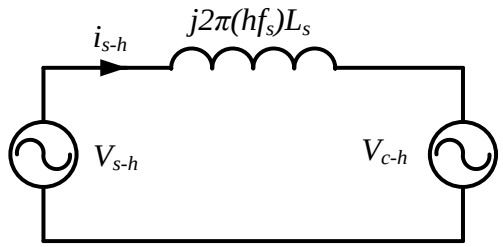


Figure 4.5: Model of the AC Side for a Given Harmonic Component

$$I_{s-h} = \frac{V_{s-h} - V_{c-h}}{2\pi h f_s L_s} \tag{4.3}$$

$$THD = \frac{\sqrt{\sum_{k=2}^{50} {I_{s-k}}^2}}{I_{s1}} \times 100 \ \ where \ I_{s-h} = \frac{V_{c-h}}{2\pi h f_s L_s} \tag{4.4}$$

It is clear that increasing the switching frequency yields harmonic components appearing at higher frequencies and lower amplitudes for a given line inductance value.

Variation of line current TDD with switching frequency is shown in Figure 4.6 for different line inductance values.

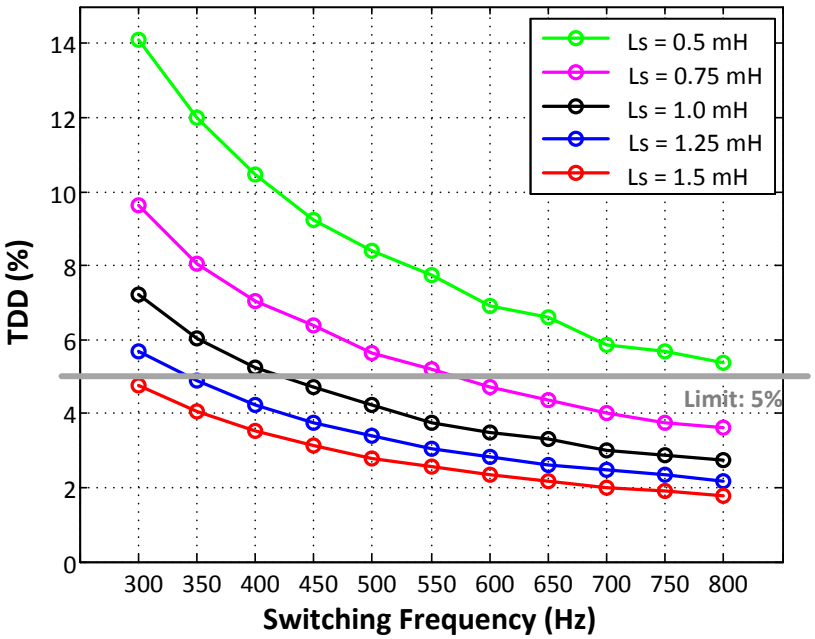


Figure 4.6: Variation of Line Current TDD with Switching Frequency for Different Line Inductance Values (C_{dc} = 5 mF)

It is shown in Figure 4.6 that a minimum of 1 mH line inductance value is required to limit the switching frequency to 500 Hz. From this result, 500 Hz switching frequency and 1 mH line inductance is considered to be an appropriate selection. Further analyses to determine the system parameters are done in following sections.

4.5. Design of Passive Elements

There are four passive components in the PWM rectifier system: The front-end traction transformer, the AC line inductor, the DC link capacitor, the DC link series LC resonant filter.

4.5.1. Front-End Transformer

The front-end transformer of the main line locomotive traction system is used for the purposes listed below:

- It provides isolation between the catenary line and the motor drive system.
- Consisting separate secondary windings, it also provides isolation between individual PWM rectifiers to prevent circulating currents between them.
- The medium voltage of the catenary (25 kV) is stepped down by this transformer to a low voltage level compatible with the DC link voltage. It is 1050 V for this particular locomotive traction system.

As discussed in Chapter 2, the front-end transformer for the conventional traction system topology operates at catenary frequency, and hence a bulky element of the system. A locomotive traction system topology has also been introduced where this low voltage transformer is replaced by a medium voltage transformer reducing the transformer volume and weight drastically. However, that topology has not yet been proven worthy in real applications and has its own demerits. Therefore it is not preferred in this work and the system topology has already been chosen as the interleaved two - level 4Q converter employing a low frequency transformer. In fact, volume and weight is not considered to be a big concern for locomotive application because the traction converter system is located on separate vehicles unlike EMUs.

The transformer being at the input side can even be turned into an advantage with the utilization of its leakage reactance as an AC line filter which is a common usage in locomotive traction applications [113, 114]. By doing so, the size of the filter reactor present on each PWM rectifier can be reduced.

The transformer is assumed to be ideal for this particular design meaning that it has no saturation, no copper and core loss and no leakage inductance for simplicity. Therefore, only the conversion ratio of the front-end transformer is taken into account which is 25000:1050.

4.5.2. AC Line Filter

The AC filter configuration has been selected as L type filter as discussed before. The series reactor on the AC line has several duties on the PWM rectifier system. First of all, it is used as the storage element so that the converter can operate in boost mode. Second, it is used for the filtration of the line current harmonics to comply with the harmonic distortion standards. It is also a control parameter as shown by the active and reactive power expressions in 3.8 and 3.9 derived previously. The range of the control variables for unity power factor operation directly depends on the line inductance value.

In high power applications as in locomotive traction system, the line inductance value can be selected smaller compared to conventional motor drive applications as discussed before. Several analytical methods for the calculation of the line inductance for a PWM rectifier have been discussed in literature [41]. A different approach is developed in this work supported by both analytical and numerical methods carried on computer simulation environments. Calculation of this parameter should be performed considering its effects on the system performance in all aspects. The line filter cost, volume and weight all of which should be minimized are the basic constraints. Therefore, the filter inductance is designed as low as possible. It is also known that the transient response time of the system increases with the increasing line inductance value which is not desired. On the other hand, its effects on the system controllability and stability should also be taken into account and this aspect demarcates the lower boundaries of this parameter. Considering all these, line inductance value is limited in the range from 0.5 mH to 1.5 mH. The exact calculation of this parameter is achieved by considering its effects to the selected system performance indices: TDD of the line current, efficiency and DC link peak to peak voltage ripple.

The effect of the filter inductance to the line current TDD and the variation of line current TDD for different values of line inductance has already been given in the previous section. Variation of the converter efficiency with switching frequency for different line inductance values is shown here, in Figure 4.7. In this analysis, only

losses due to semiconductor devices and the series line reactor have been taken into account. Actual efficiency analysis of the system is described in detail in following sections.

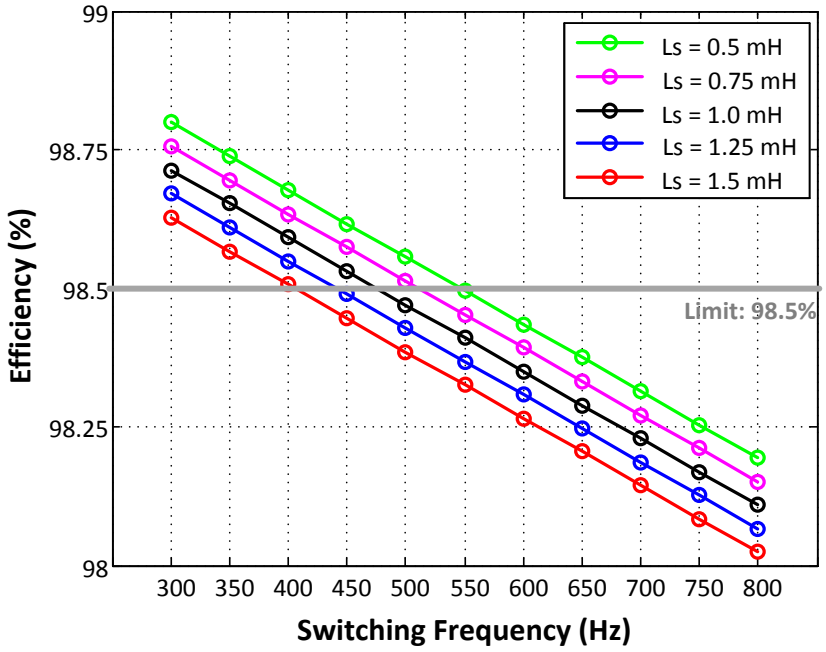


Figure 4.7: Variation of Converter Efficiency with Switching Frequency for Different Line Inductance Values (C_{dc} = 5 mF)

The effect of the line inductance on the DC link voltage ripple has also been analyzed and the variation of DC link peak-to-peak ripple voltage with switching frequency is shown in Figure 4.8 for different line inductance values.

These results also supports the selection of 500 Hz switching frequency and 1 mH line inductance value found before.

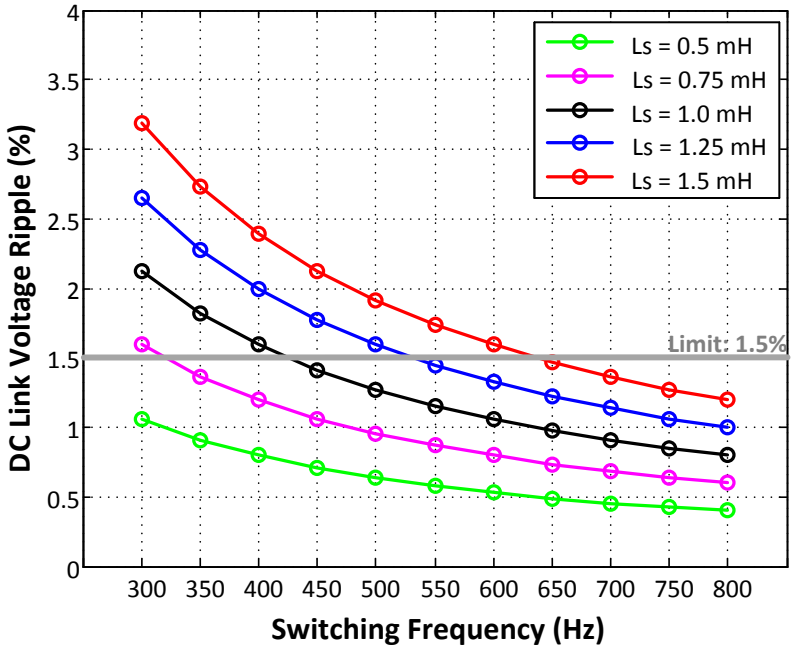


Figure 4.8: Variation of DC Link Peak-to-Peak Ripple with Switching Frequency for Different Line Inductance Values (C_{dc} = 5 mF)

4.5.3. DC Link Filter

The cost, volume and weight constraints mentioned for the AC line filter are also valid for the design of DC link filter capacitor. Other than this, there are also several aspects for the design of this component. First of all, for a DC link converter application, the DC link voltage, nominal value of which is selected as 1800V, is usually required to be maintained above a specific value for a period of time (usually a full cycle of supply voltage) in case of power failure. This limit is selected as 1350V in this application. Knowing that the DC link nominal current is 700A, the required DC link capacitance to maintain this voltage for 20ms can be calculated as in (4.5) and (4.6). This approach usually leads to an overdesign and the result of it will not be applied in this research work.

$$I_{dc} = C_{dc} \frac{\Delta V_{dc}}{\Delta t} \tag{4.5}$$

$$C_{dc} = I_{dc}\,\frac{\Delta t}{\Delta V_{dc}} = 700 \times \frac{20 \times 10^{-3}}{1800 - 1350} = 31\ mF \tag{4.6}$$

The usual design approach for the DC link capacitor is based on the DC link voltage ripple. This performance index is affected by all system parameters (L_s, f_{sw} and C_{dc}) and modelling of this ripple requires a very complex analysis, however it can be derived with proper approximations. The DC link input current is composed of a DC component which is transferred to the load, a second harmonic component which is filtered by the LC filter and high frequency harmonic components which flow through the DC link capacitor. The ripple voltage on the DC link is formed by the high frequency harmonics on DC link capacitor current. These harmonics are scattered around a center frequency of four times the PWM switching frequency for the interleaved two-level 4Q converter topology. Since the total high frequency harmonic content of the DC link current is known, the peak-to-peak voltage ripple can be calculated by approximating the high frequency components as one component on exactly the center frequency as shown in Equations 4.7 to 4.10.

$$I_c = C_{dc}\,\frac{dV_{dc}}{dt} \tag{4.7}$$

$$V_{dc-r} = \frac{1}{C_{dc}}\int I_{c-r}\,dt = \frac{1}{C_{dc}}\int \widehat{I_c}\,\sin(2\pi 4 f_{sw} t)\,dt \tag{4.8}$$

$$V_{dc-r} = \frac{\widehat{I_c}\,\sin(2\pi 4 f_{sw} t)}{C_{dc} 2\pi 4 f_{sw}} \tag{4.9}$$

$$\widehat{V}_{dc-r} = \frac{\widehat{I_c}}{C_{dc} 2\pi 4 f_{sw}} \tag{4.10}$$

Therefore, the peak-to-peak value of the DC link voltage ripple can be approximately calculated as in (4.11) considering the peak value of the ripple current on the DC link is 480A which is determined by simulation.

$$V_{r-pp} = \frac{19.1}{C_{dc}\, f_{sw}} \tag{4.11}$$

Variation of the peak-to-peak DC link voltage ripple with changing switching frequency for different DC link capacitor values is obtained and shown in Figure 4.9.

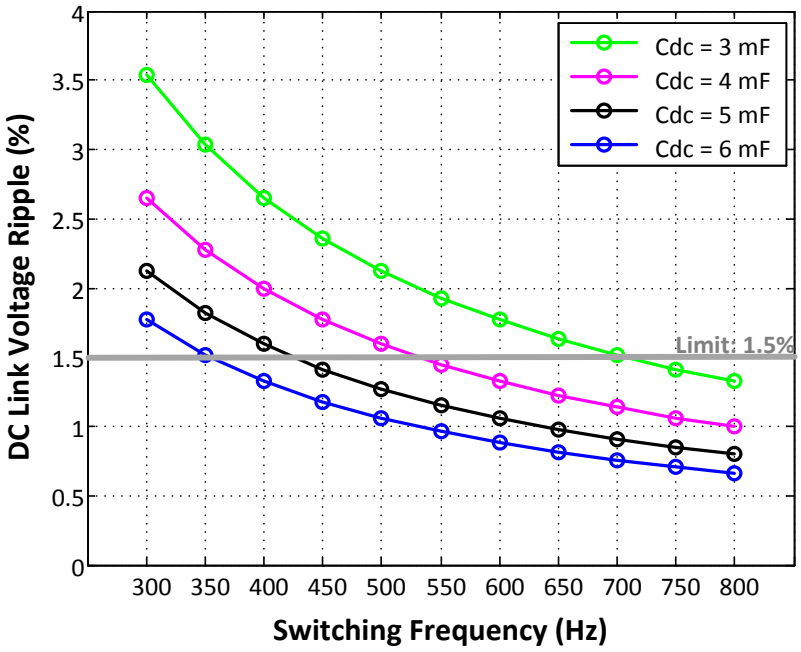


Figure 4.9: Variation of DC Link Peak-to-Peak Ripple with Switching Frequency for Different DC Link Capacitor Values (L_s = 1 mH)

To observe the effect of the DC link capacitance on the harmonic distortion, the variation of TDD against changing switching frequency for different DC link capacitor values is also shown in Figure 4.10.

The results demonstrated on Figures 4.9 and 4.10 reveal that, if the previously selected switching frequency value (500 Hz) is also considered, a DC link capacitance of 5 mF is the best choice.

To finalize the design of the DC link capacitor, the requirements of the overall DC link capacitor are summarized in Table 4.5. To meet the voltage requirement, series connection and to meet the ripple current requirement, parallel connection of multiple capacitors may be required.

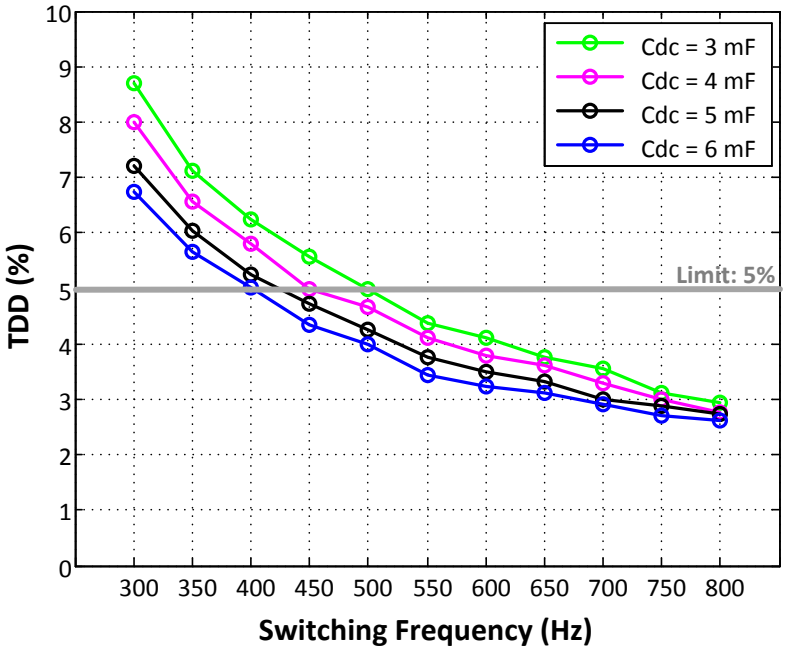


Figure 4.10: Variation of TDD with Switching Frequency for Different DC Link Capacitor Values (L_s = 1 mH)

Table 4.5: The Requirements of the DC Link Capacitor

Capacitance	5 mF
Voltage (DC)	2000V
Ripple Current (RMS)	300A

4.5.4. DC Link Series LC Filter Tuned to Second Harmonic

The DC link series LC filter is used to eliminate the harmonic component present on the DC link current, the frequency of which is at twice the supply frequency. The resonant frequency of a series connected LC network is shown in (4.11) and the LC multiplication becomes as in (4.12).

$$w_{res} = \frac{1}{\sqrt{C_f\, L_f}} = 2\pi \times 100 \tag{4.11}$$

$$L_f C_f = 2.533 \times 10^{-6} \tag{4.12}$$

It is already shown that the peak value of the current on the DC link LC filter at rated power is the same as the rated line current 1190A. The selection of capacitor (C_f) and inductor (L_f) values can be based on the AC voltage on the capacitor, the expression of which is shown in (4.13).

$$V_{Cf} = \frac{I_f}{2\pi f C_f} \tag{4.13}$$

The variation of the filter capacitor peak value different capacitance values is shown in Figure 4.11. It should be pointed out that the actual voltage on the filter capacitor is the sum of this AC component and the DC link voltage.

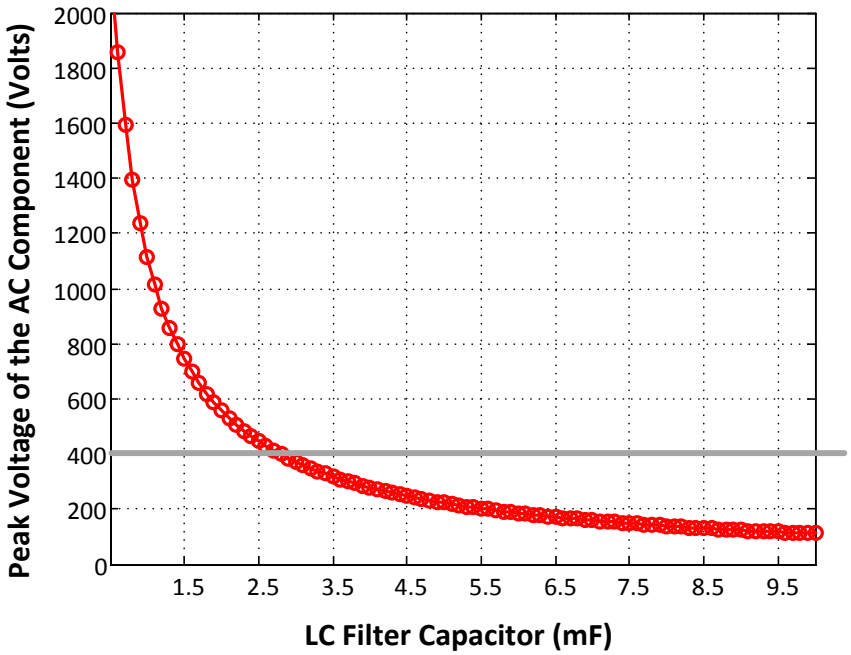


Figure 4.11: Variation of LC Filter Capacitor Voltage

The trade-off here is between the capacitance value and the voltage rating of this capacitor. A high capacitance value is never desired for reduced converter size and cost. On the other hand, as visualized in Figure 4.11, the voltage on the capacitor is inversely proportional with the capacitance value. The voltage limit is selected as 400V so that the closest capacitor value which is 2.8 mF, is selected. The corresponding filter inductor value is therefore calculated as 0.9 mH from Equation 4.12. The requirements of the DC link LC filter capacitor are summarized in Table 4.6. It should be noted that the physical design of these two components should be performed considering the fact that their values must be constant for all operation modes and output power rates due to the resonant nature of the filter.

Table 4.6: The Requirements of the DC Link LC Filter Capacitor

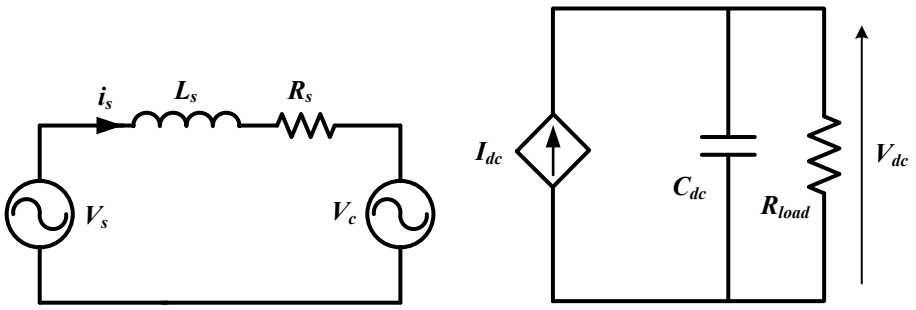
Capacitance	2.8 mF
Voltage (DC)	2300V
Ripple Current (RMS)	842A

4.6. Design of Control System

Control techniques applied to PWM Rectifier of main line locomotive traction systems have been presented in Chapter 3. In this research work, linear current regulator based control technique is designed and implemented with both PI and PR based current controllers. As mentioned previously, the control circuit is composed of four main parts: Phase locked loop, DC link voltage control loop, AC line current control loop and pulse width modulation. The PLL method is selected as the OSG based single phase PLL, block diagram of which has already been given in Figure 3.13.

The design of the voltage and current control system is based on the system model derived for both AC and DC side which is shown in Figure 4.12. The following approximations have been made in this modelling:

- The PWM rectifier is modelled as a linear system.
- Only one 4Q converter is considered since the operation of the two-level converters in interleaved 4Q rectifier topology are identical except the PWM carrier waveform phases.
- The DC link and AC line are considered as dependent but separate circuits.
- The AC line is modelled considering only the voltage and current components at fundamental frequency neglecting the harmonics.
- The DC link is modelled for only DC quantities neglecting the harmonics.
- The converter output (V_c) is considered as an ideal voltage source, magnitude and phase of which are determined by the control variables (m_a and δ).
- The converter is modelled as an ideal and dependent current source on the DC side, magnitude of which is determined by the line current.
- The series LC filter tuned to the second harmonic component is not included in the model.



(a) (b)

Figure 4.12: Modelling of the PWM Rectifier: (a) AC Side, (b) DC Side

The time domain expressions of the system in terms of the variables to be controlled ($i_s(t)$ and $V_{dc}(t)$) based on these models are obtained by using basic circuit theory as shown in (4.14) and (4.15).

$$v_s(t) = v_c(t) + L_s \frac{di_s(t)}{dt} + R_s i_s(t) \tag{4.14}$$

$$I_{dc}(t) = C \frac{dV_{dc}(t)}{dt} + \frac{V_{dc}(t)}{R_{load}} \tag{4.15}$$

Laplace transformation is applied to Equations 4.14 and 415 to obtain the system model in the s domain as shown in (4.16) and (4.17) and the plant transfer functions are obtained as in (4.18) and (4.19).

$$V_s(s) = V_c(s) + sL_s I_s + R_s I_s(t) \tag{4.16}$$

$$I_{dc}(s) = CV_{dc}(s) + \frac{V_{dc}(s)}{R_{load}} \tag{4.17}$$

$$G_{pi}(s) = \frac{I_s(s)}{V_c(s)} = \frac{1}{R_s + sL_s} \tag{4.18}$$

$$G_{pv}(s) = \frac{V_{dc}(s)}{I_{dc}(s)} = \frac{R_{load}}{1 + sC_{dc}R_{load}} \tag{4.19}$$

Overall system block diagram including controllers, plants and measurements is shown in Figures 4.13 and 4.14. Measurements are considered as first order delays, transfer functions of which is shown in Equation 4.20 where τ is the measurement time constant. The plant transfer functions have already been introduced in Equations 4.18 and 4.19. The converter is considered as linear for simplicity with a unity gain as shown in (4.21). The DC voltage loop controller is a PI controller transfer function of which can be seen in (4.22). The AC current loop can be composed of two types of controllers as expressed in Chapter 3 and their transfer functions are shown in (4.23) and (4.24).

$$H(s) = \frac{1}{1 + s\tau} \tag{4.20}$$

$$G_{conv}(s) = 1 \tag{4.21}$$

$$G_{cv}(s) = \frac{Y_v(s)}{E_v(s)} = K_{pv} + \frac{K_{iv}}{s} \tag{4.22}$$

$$G_{ci}(s) = K_{pi} + \frac{K_{ii}}{s} \tag{4.23}$$

$$G_{ci}(s) = K_{pi} + \frac{2K_{ii}w_c s}{s^2 + 2w_c s + {w_0}^2} \tag{4.24}$$

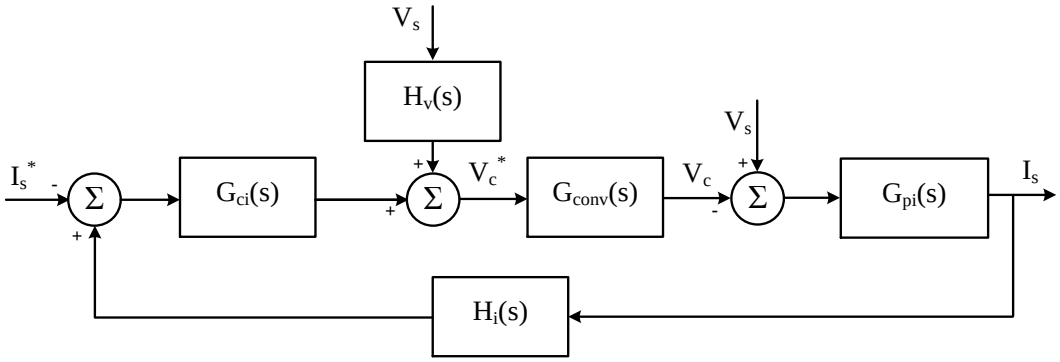


Figure 4.13: Overall System Block Diagram (AC Side)

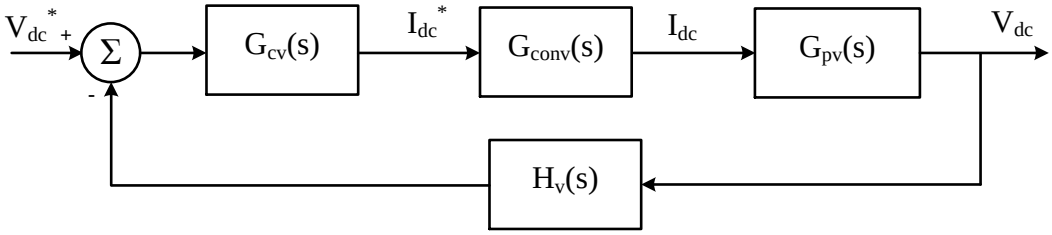


Figure 4.14: Overall System Block Diagram (DC Side)

The open loop transfer function of the DC voltage loop is shown in Equations 4.25 and 4.26 and the closed loop transfer function is shown in Equation 4.27.

$$G_v(s) = G_{cv}(s)G_{conv}(s)G_{pv}(s) \tag{4.25}$$

$$G_v(s) = \left[K_{pv} + \frac{K_{iv}}{s}\right][1]\left[\frac{R_{load}}{1 + sC_{dc}R_{load}}\right] \tag{4.26}$$

$$G_v(s) = \frac{G_v(s)}{1 + G_v(s)H_v(s)} \tag{4.27}$$

The design of the outer loop is performed based on the model (Figure 4.14) and the transfer functions (Equations 4.25 - 4.27). The actuating signal of this loop is the DC link current reference (I_{dc}) which is used to form the AC current reference to be used in the inner loop. The control design is carried out with three aspects of the control theory: steady state performance, transient performance and stability analysis.

First, steady state error of the closed loop system against step input, r(t) is analyzed as seen in (4.28) and (4.29) and found as zero as expected independent of the controller parameters. In other words, for a stable system, DC link voltage will be equal to its set value at steady state.

$$E_{ss} = \lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s) = \lim_{s\to 0}\left(s\frac{1}{1+G_v(s)H_v(s)}R(s)\right) \tag{4.28}$$

$$E_{ss} = \lim_{s\to 0}\left(s\frac{1}{1+\left[K_{pv}+\frac{K_{iv}}{s}\right][1]\left[\frac{R_{load}}{1+sC_{dc}R_{load}}\right]\left[\frac{1}{1+s\tau}\right]}\frac{1}{s}\right) \tag{4.29}$$

The controller design; i.e., determination of K_p and K_i, is performed and the performance of the performance of the resultant system is tested on MATLAB using the closed loop transfer function derived above. This design is based on the transient state performance of the DC link voltage controller. The transient response of the DC link voltage controller is shown for different values of control parameters in Figures 4.15 - 4.17. Fine tuning is also implemented by checking the transient response under different load conditions as shown in Figure 4.18 and the control parameters are selected as K_p = 1 and K_i = 80 by the transient response analysis. The system performance has also been checked by MATLAB tools with the selected parameters as shown in Table 4.7.

Table 4.7: Performance of the DC Link Voltage Controller with K_p = 1, K_i = 80

Rise Time	9 ms	Maximum Overshoot	2.17 %
Settling Time	25.5 ms	Minimum Undershoot	0 %
Peak Time	22.1 ms	Steady State Error	0 %

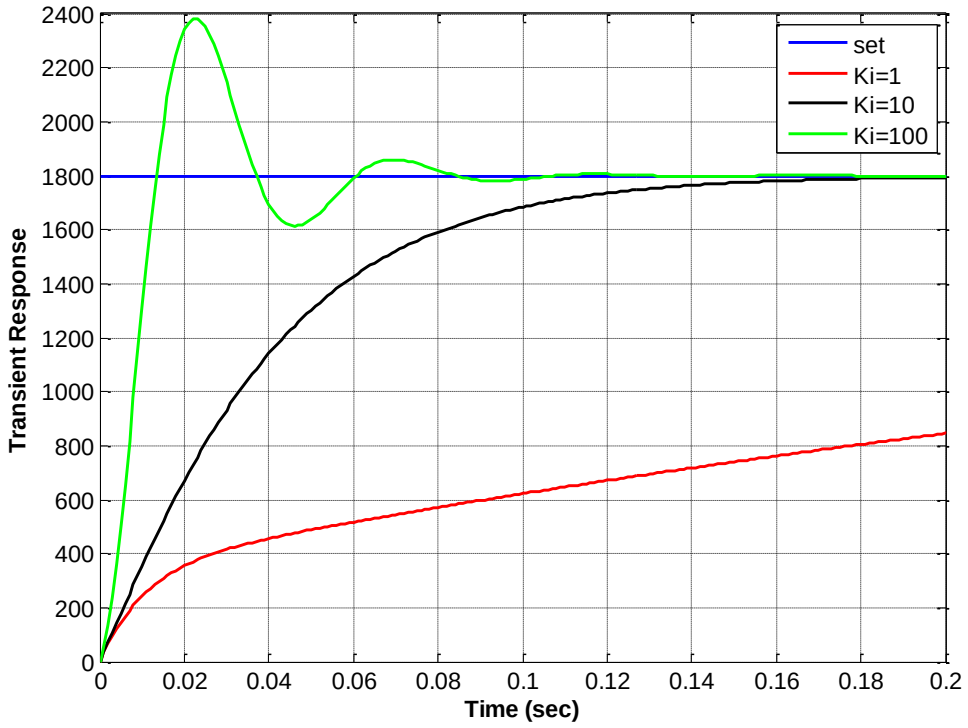


Figure 4.15: DC Link Voltage Controller Response (K_p = 0.1)

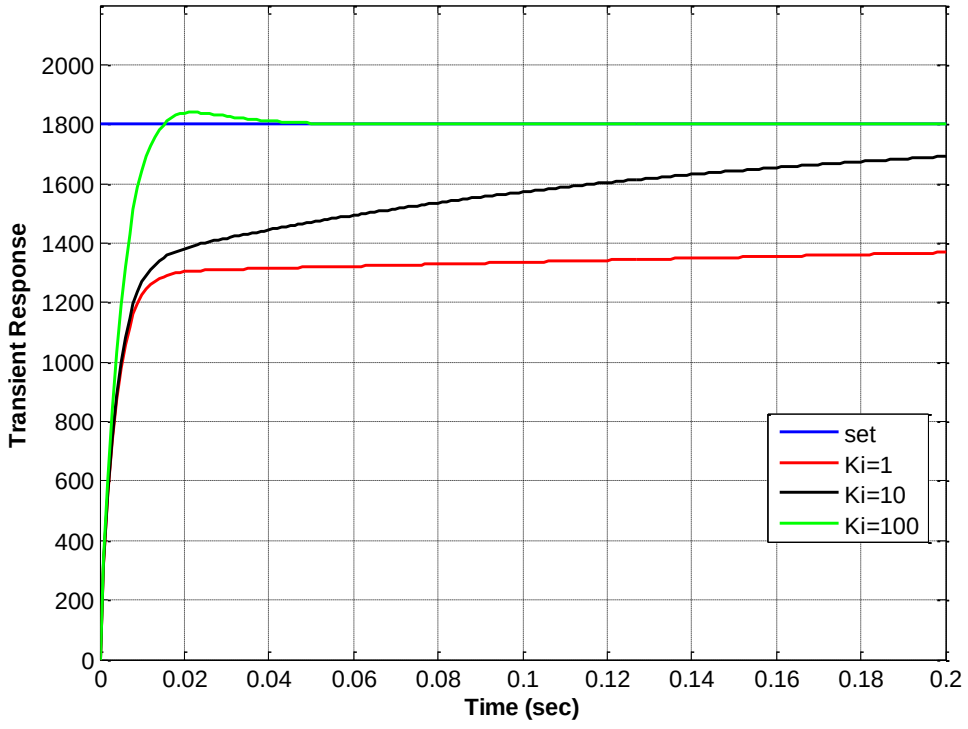


Figure 4.16: DC Link Voltage Controller Response (K_p = 1)

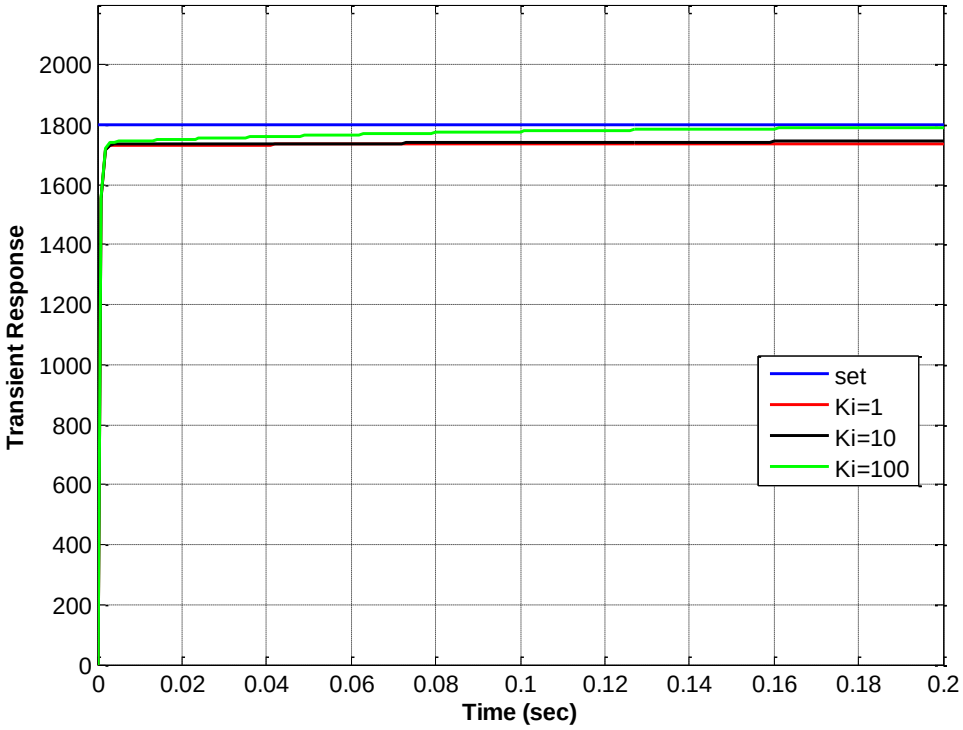


Figure 4.17: DC Link Voltage Controller Response (K_p = 10)

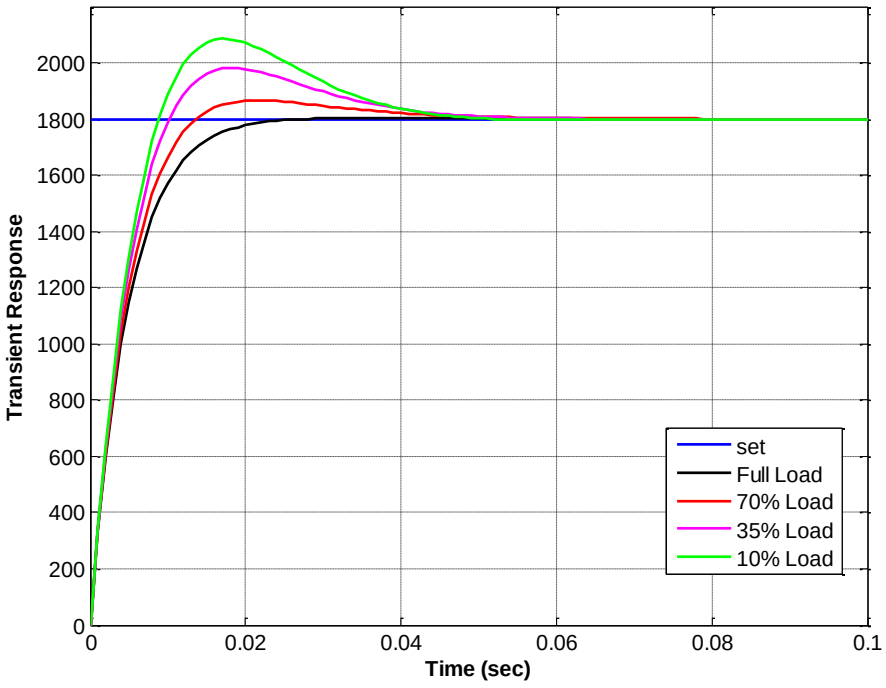


Figure 4.18: DC Link Voltage Controller Response for Different Loads

The most convenient stability analysis of a closed loop system is applying Routh-Hurwitz Stability Criterion. A closed loop system is said to be stable if all the poles of the system transfer function have real negative real parts. Characteristic equation of the closed loop transfer function can be checked for the Routh Hurwitz Criterion to determine whether the system is stable or not. Moreover, the range of controller parameters can be determined by using this criterion. The characteristic polynomial of the DC voltage loop is shown in Equation 4.30 with R_{load} = 2.592 Ω (determined considering the rated output power), C_{dc} = 5 mF (previously designed), τ = 40 μs (determined by the voltage sensor response time) and the determined controller parameters.

$$q(s) = 6.7 \times 10^{-9}s^5 + 1.7 \times 10^{-4}s^4 + 6 \times 10^{-2}s^3 + 6.7s^2 + 233s \qquad (4.30)$$

The stability check is achieved by using MATLAB and it is observed that all the poles of the closed loop transfer function have negative real parts so that the designed system is stable.

Root locus method is also applied to the system for a more detailed analysis of stability. The loci of each pole of the characteristics polynomial can be plotted by root locus method to observe their trajectory with changing control parameters so that it can be assured that the poles stay on the left half plane (have negative real parts). Only one control parameter is used for the root locus plot (K_p) and the ratio between the two parameters is selected as 80. The resultant locus of the roots is shown in Figure 4.19.

It is proven by the root locus method that the poles of the system lay on the left-half plane for a wide range of gain. To better analyze the system bandwidth, frequency response of the controller with the selected parameters have been obtained as shown in Figure 4.20 by which the system performance indices of bandwidth, gain margin and phase margin are determined using MATLAB tools.

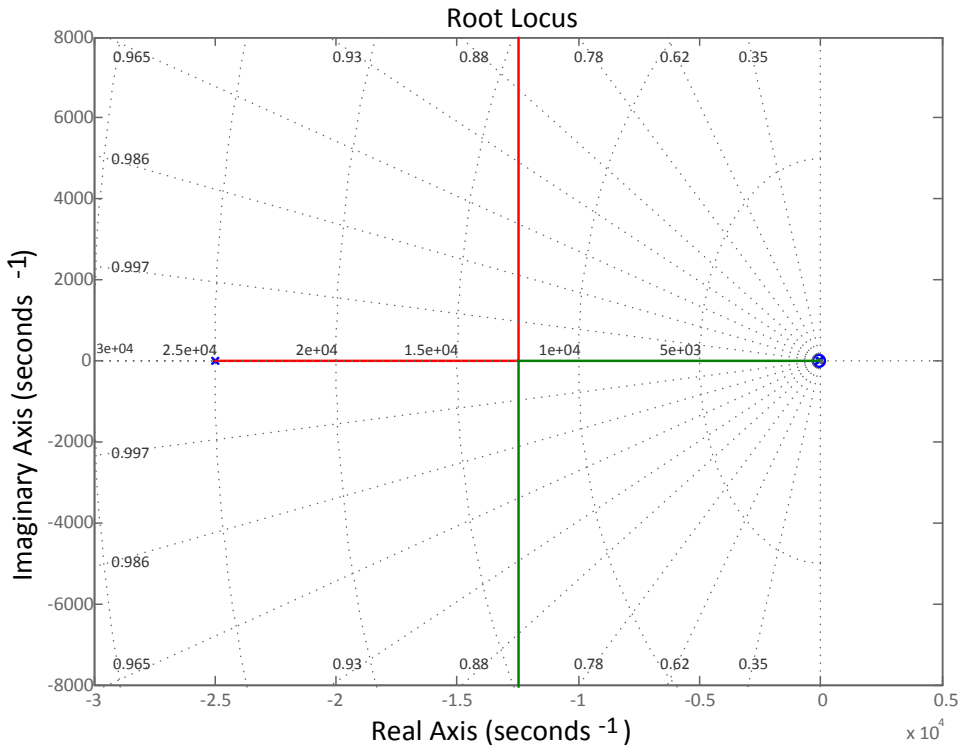


Figure 4.19: Root Locus of the DC Link Voltage Controller

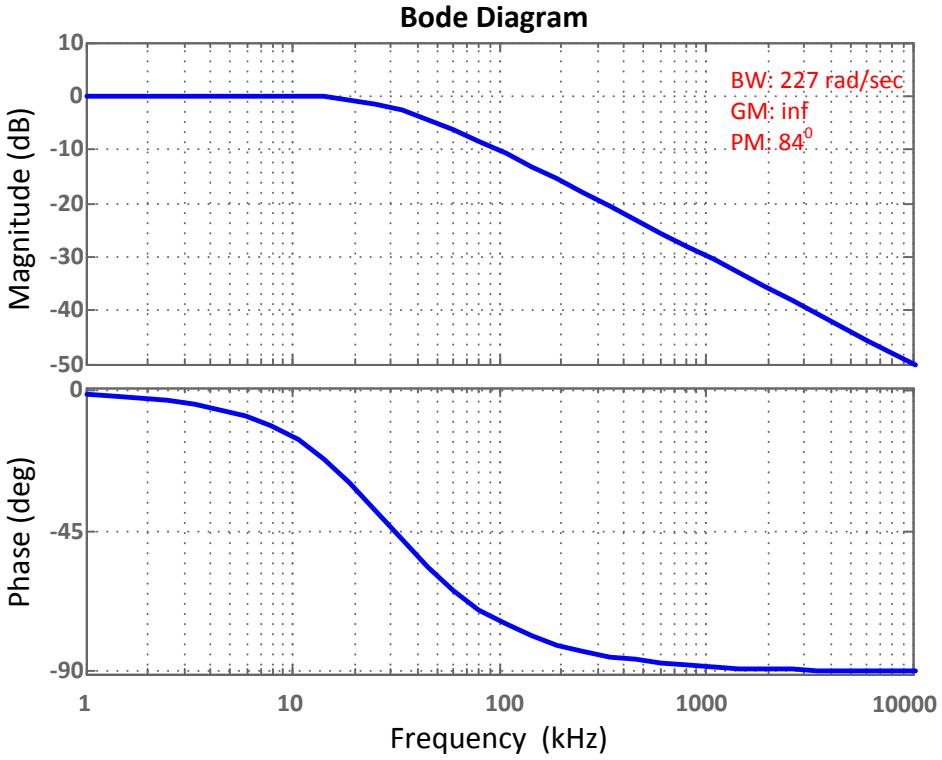


Figure 4.20: Frequency Response of DC Link Voltage Controller

Modulating waveform is the actuating signal of the AC current loop for linear current regulator based control technique and carries control variable information (amplitude modulation index and delta). The ranges of these two variables are obtained for the whole system operation range with unity power factor including the regenerative braking mode of operation, with the utilization of Equations 3.8 and 3.9. In Figure 4.21, variation of m_a against input power and in Figure 4.22, variation of the δ against input power is shown. Both characteristics correspond to unity pf; i.e., no reactive power transfer.

The AC current control loop design is implemented with the same procedure followed in DC voltage control loop. Transfer function of the AC current loop is shown in Equations 4.31 and 4.32 for the feedback loop and in Equations 4.33 and 4.34 for the feed forward loop. The closed loop transfer function is also shown in Equation 4.35.

$$G_i(s) = \frac{Y(s)}{E(s)} = -G_{ci}(s)G_{conv}(s)G_{pi}(s) \tag{4.31}$$

$$G_i(s) = \frac{Y(s)}{E(s)} = \left[K_{pi} + \frac{K_{ii}}{s}\right][1]\left[\frac{1}{R_s + sL_s}\right] \tag{4.32}$$

$$G_i(s) = \frac{Y(s)}{D(s)} = G_{pi}(s) - G_{pi}(s)G_{conv}(s)H_v(s) \tag{4.33}$$

$$G_i(s) = \frac{Y(s)}{D(s)} = \left[\frac{1}{R_s + sL_s}\right]\left[1 - \frac{1}{1 + s\tau}\right] \tag{4.34}$$

$$G_i(s) = \frac{-G_i(s)}{1 - G_i(s)H_i(s)} \tag{4.35}$$

AC current controller design is performed with both PI and PR controller and the performance of the resultant performance is tested on MATLAB using the closed loop transfer function derived above. This design is based on the transient state performance of the DC link voltage controller and steady state performance. The response of the AC line current controller is shown for different values of control parameters in Figure 4.23 (PI regulator) and in Figure 4.24 (PR regulator). The selected resultant parameters are $K_p = 90$, $K_i = 2$ for PI regulator and $K_p = 10$, $K_i = 10$, $w_o = 314$ rad/sec, $w_c = 1$ rad/sec for PR regulator.

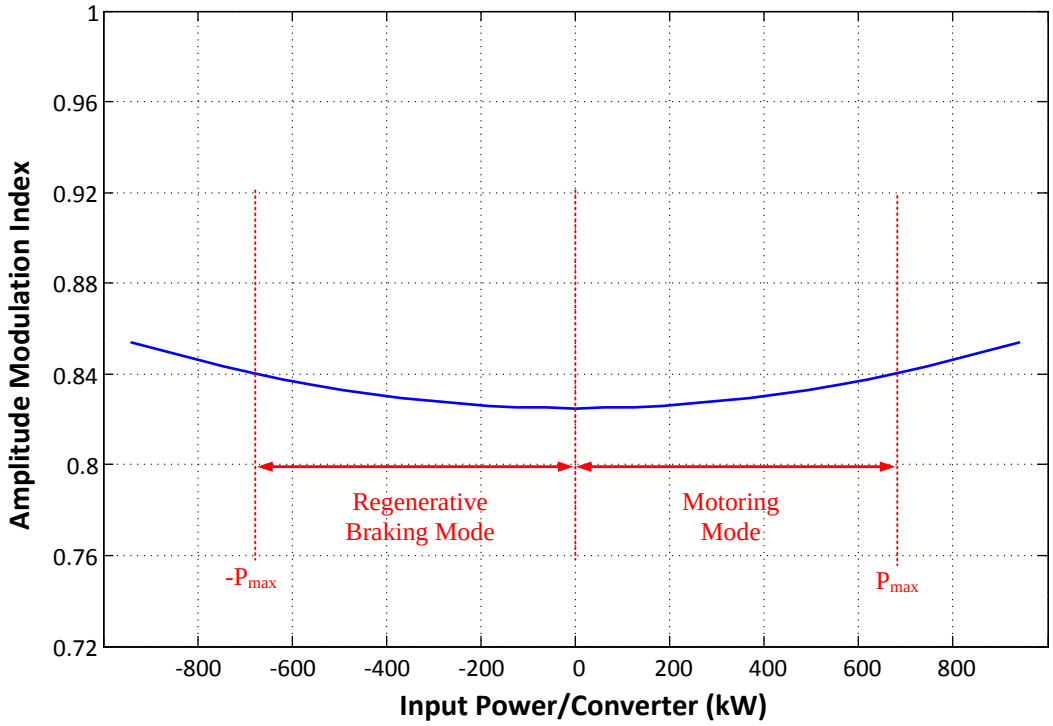


Figure 4.21: Variation of m_a with Input Power at Unity pf

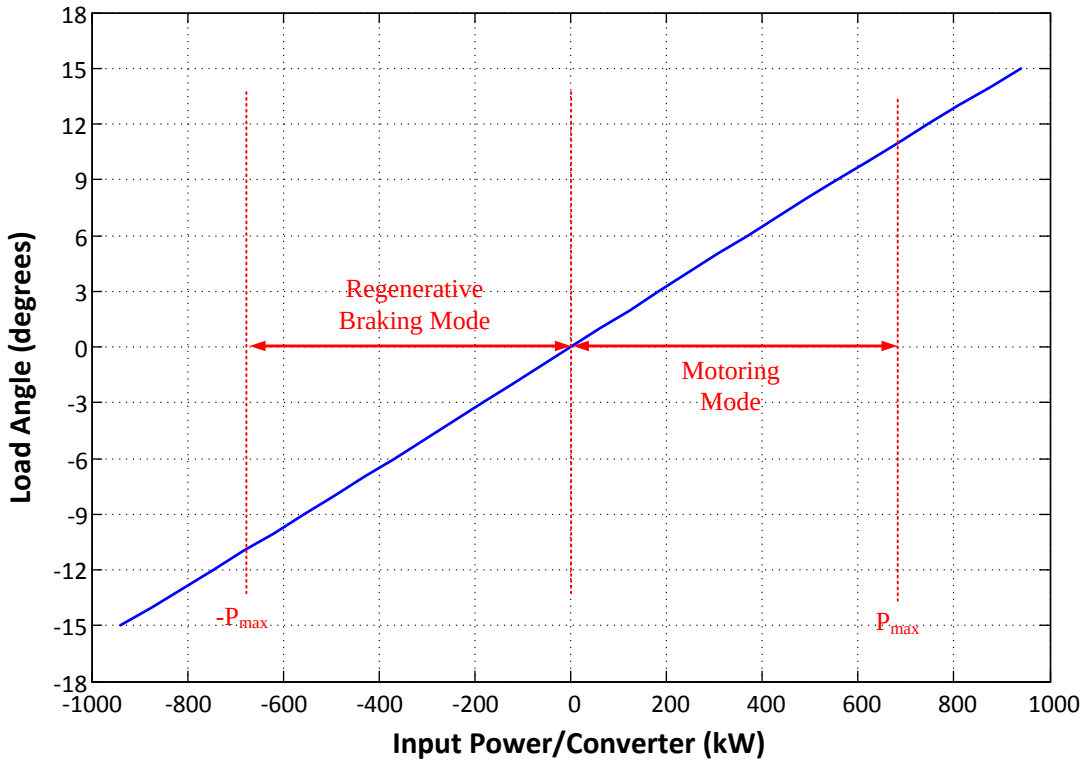


Figure 4.22: Variation of Load Angle with Input Power at Unity pf

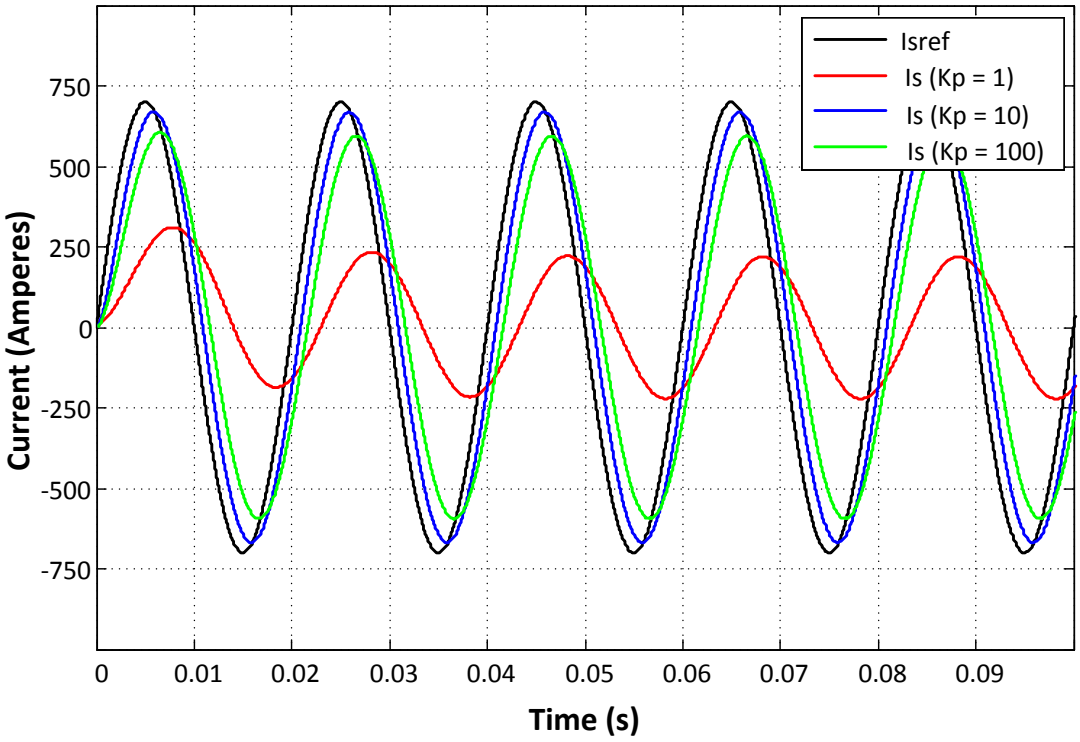


Figure 4.23: AC Line Current Controller Response (PI Regulator - $K_i = 1$)

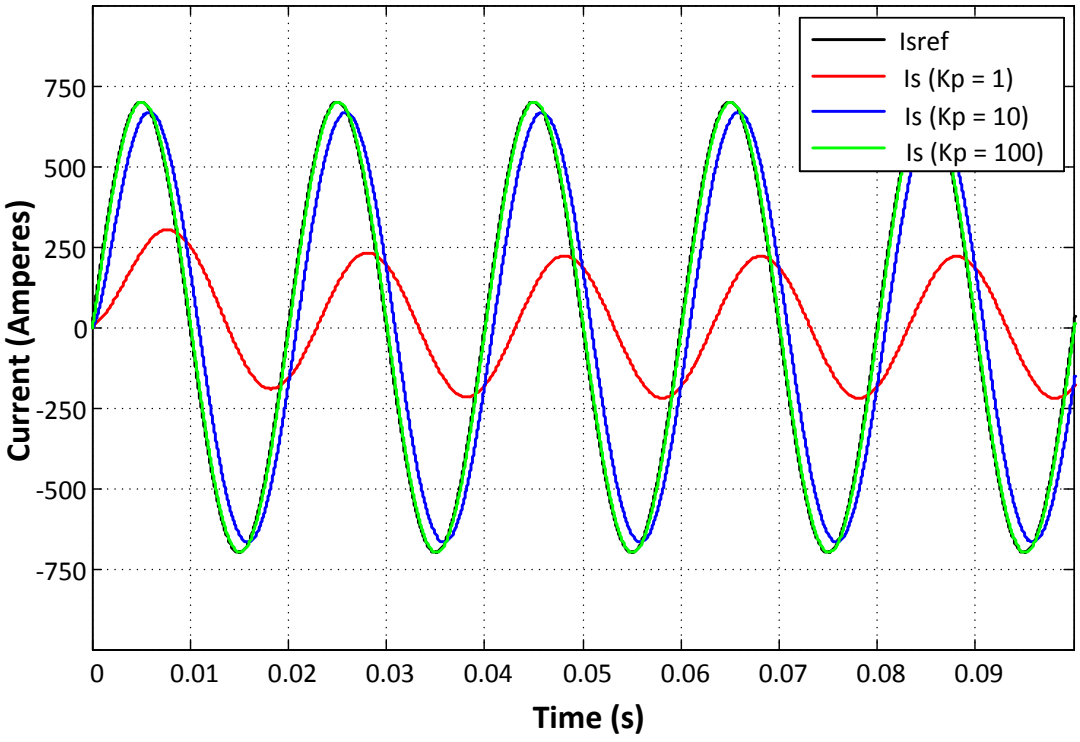


Figure 4.24: AC Line Current Controller Response (PR Regulator - $K_i = 1$, $w_c = 1$)

4.7. Efficiency Analysis

Loss components on the interleaved two - level PWM rectifier system are as follows:

- Transformer losses: Copper loss, core loss
- Line reactor losses: Copper loss, core loss
- IGBT losses: Conduction loss, switching loss (turn-on and turn-off)
- Diode losses: Conduction loss, reverse recovery loss
- DC link capacitor losses: ESR loss
- DC link series LC filter inductor losses: Copper loss, core loss
- DC link series LC filter capacitor losses: ESR loss

In this research work, front-end transformer is assumed to be ideal and therefore its loss analysis has not been carried out. The passive elements (inductors and capacitors) are designed, but their physical design for the high power locomotive is not included in the scope of this thesis. Therefore, their loss analyses have only been achieved for the prototype system and will be presented in Chapter 6.

On the other hand, power semiconductor device losses (including IGBT and Diode) and converter efficiency has been calculated with analytical methods presented here and with the help of IGBT module characteristics given in Table 4.4 and Appendix A [111].

IGBT conduction loss can be calculated by integrating the conduction energy when the device is at ON state. This energy can be determined by the device ON state voltage, current and duration. The saturation (ON state) voltage of the selected IGBT is given as 3.3V; however, the actual saturation voltage characteristics against collector current of an IGBT is given in Figure A.2 and should be used for an accurate analysis. Current waveform of IGBT can be seen in Figure 4.25 where on state time durations are highlighted. With the use of the data in Figure 4.25, total conduction energy of one IGBT for a full fundamental cycle of supply frequency can be calculated

as in (4.36). Then, IGBT conduction power loss can be determined by (4.37) since the fundamental supply frequency is 50 Hz.

$$E_{c-T} = \int V_{sat}\, I_c\, dt \tag{4.36}$$

$$P_{c-T} = E_{c-T} \times 50 \tag{4.37}$$

Same procedure can be applied to the antiparallel diode conduction loss calculation. The ON state voltage characteristics of the diode against emitter current is given in Figure A.2. Current waveform of diode is also given in Figure 4.26 where on state time durations are highlighted. The total conduction energy of one diode for a full fundamental cycle of supply frequency can be calculated as in (4.38). Then, diode conduction power loss can be determined by (4.39).

$$E_{c-D} = \int V_{on}\, I_E\, dt \tag{4.38}$$

$$P_{c-D} = E_{c-D} \times 50 \tag{4.39}$$

The conduction loss of one IGBT and one diode are calculated as **174 W** and **511 W** respectively with the implementation of the above procedure using MATLAB tools.

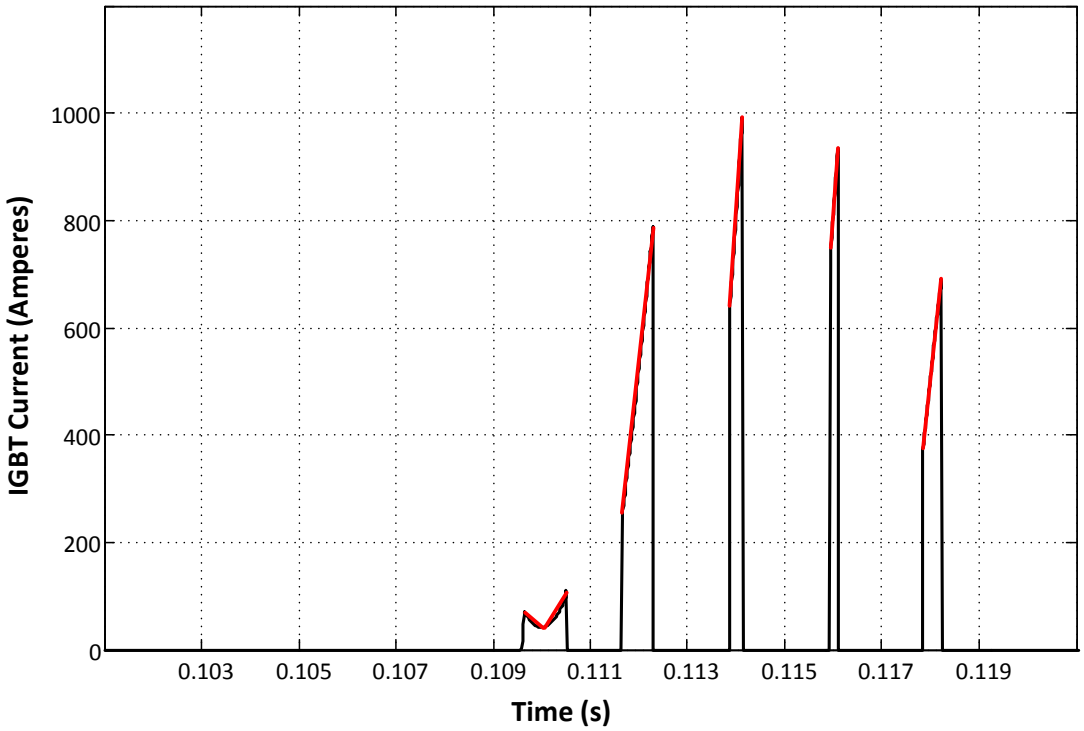


Figure 4.25: Current Waveform of One IGBT

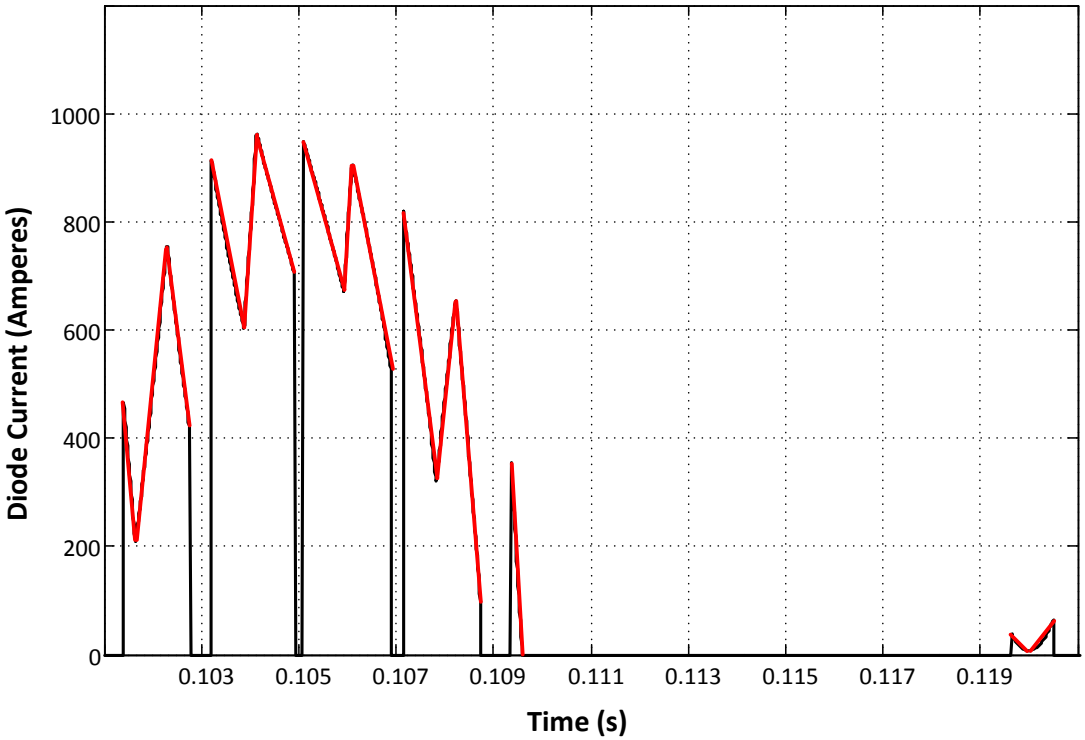


Figure 4.26: Current Waveform of One Diode

The switching characteristic of an IGBT is shown in Figure 4.27 [28] where V_G is the applied gate signal, V_{GE} is the actual gate-emitter voltage and I_C is the collector current of the IGBT. IGBTs go into the conducting state a period of time after the ON signal is applied to the gate which is called the turn-on delay time ($t_{d\text{-}on}$). This is also true for the OFF state transition and it is called the turn-off delay time ($t_{d\text{-}off}$). They are given as 1.6 µs and 2.5 µs, respectively in Table 4.4. The transitions are not smooth practically and the increase of the current at turn-on and decrease of the current at turn-off are not instantaneous as seen in Figure 4.27. The time required for the IGBT current to increase from 10 % to 90 % is called the rise time (t_r) and the time required for the IGBT current to decrease from 90 % to 10 % is called the fall time (t_f) which are also listed in Table 4.4 as 1.0 µs.

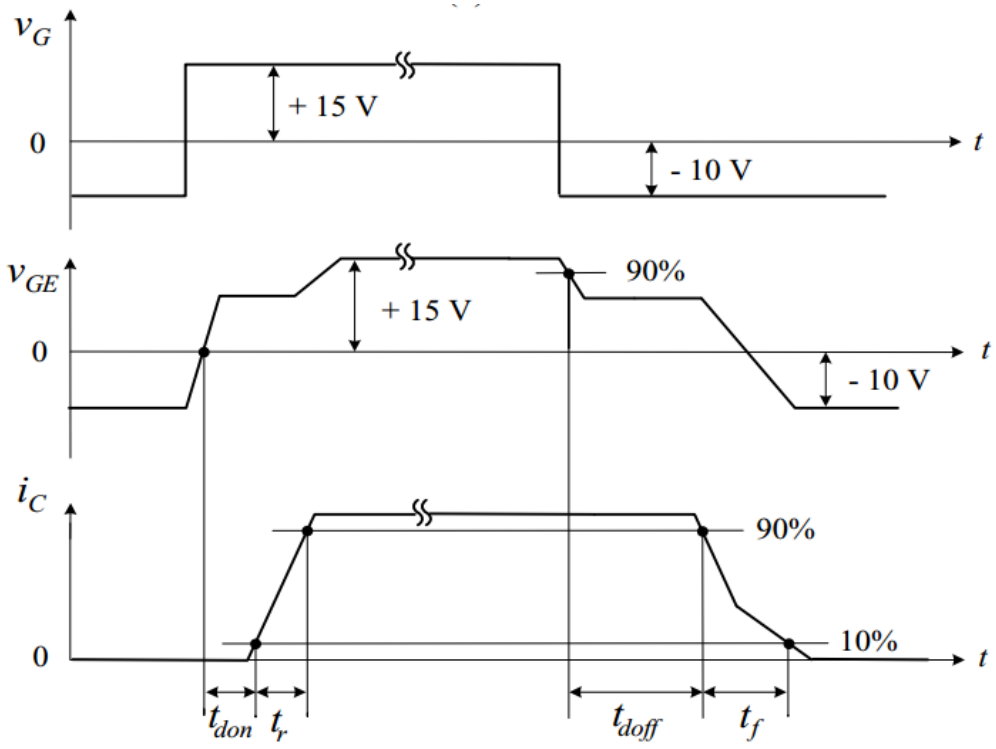


Figure 4.27: Switching Characteristic of an IGBT [28]

There is a simpler method to calculate the switching loss of an IGBT without using the switching times. The switching energies (E_{on} and E_{off}) are defined against collector current at the switching instant as given in Figure A.3 and can be used to calculate the

switching power loss. The turn-on and turn-off switching instants of one IGBT are shown for one cycle of supply voltage in Figure 4.28.

The total switching energy of one IGBT for a full fundamental cycle can be calculated as in (4.40). Then, IGBT switching power loss can be determined by (4.41).

$$E_{sw} = \sum_{turn-off} E_{off} + \sum_{turn-on} E_{on} \tag{4.40}$$

$$P_{sw} = E_{sw} \times 50 \tag{4.41}$$

A similar procedure can be applied to calculate the reverse recovery loss of antiparallel diodes by using the turn-off instants of one diode for a fundamental cycle shown in Figure 4.29. The reverse recovery energy characteristic against emitter current is given in Figure A.3 and used to determine the total reverse recovery energy of one diode as shown in (4.42). Then, the reverse recovery power loss can be determined by (4.43).

$$E_{rr} = \sum_{turn-off} E_{rr} \tag{4.42}$$

$$P_{rr} = E_{rr} \times 50 \tag{4.43}$$

The switching loss of one IGBT and the reverse recovery loss of one diode are calculated as **467 W** and **109 W** respectively with the implementation of the given procedure on MATLAB.

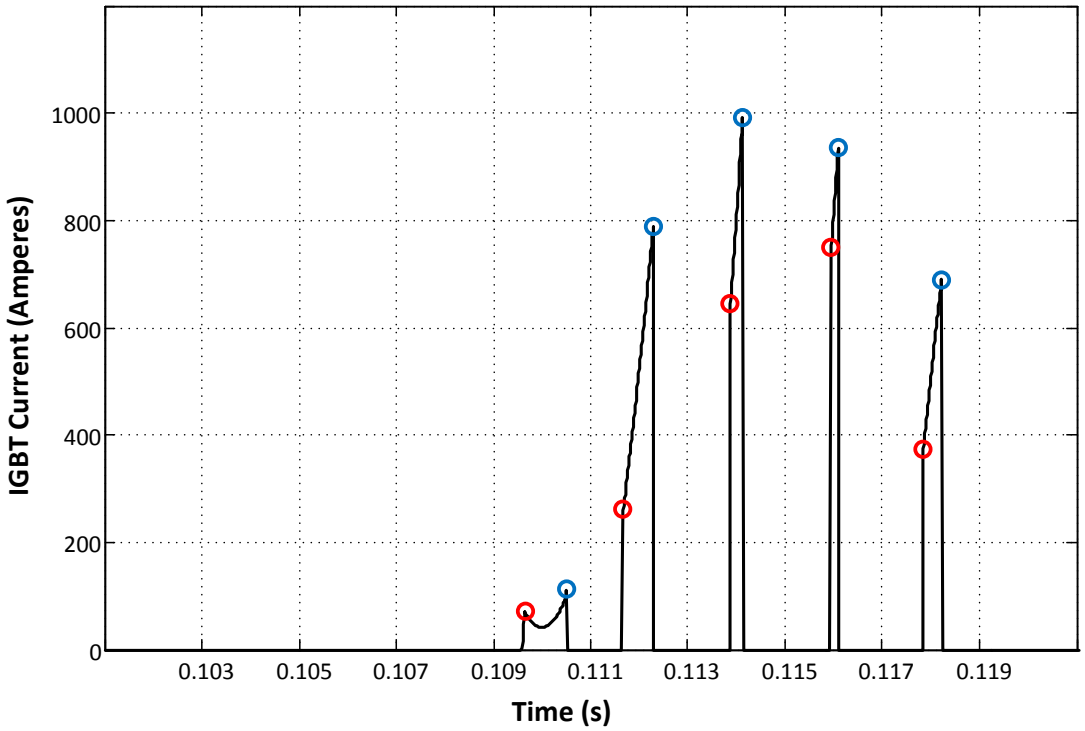


Figure 4.28: Turn-on and Turn-off Switching Instants of One IGBT

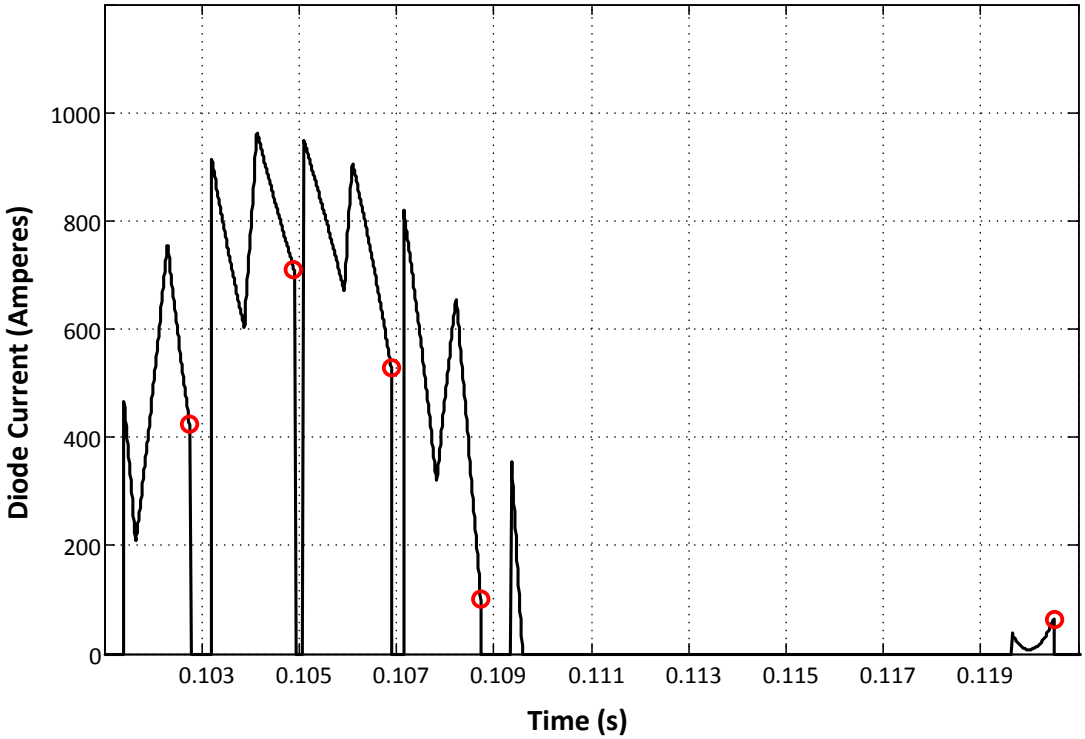


Figure 4.29: Turn-off Instants of One Diode

The power loss analysis of the PWM rectifier is summarized in Table 4.7 and the total power loss is found as 10.1 kW at rated output power in motoring mode of operation considering that there are a total of eight IGBTs and eight Diodes. The efficiency of the rectifier is calculated by using the expression given in Equation 4.44 as 99.2 %.

Table 4.8: Power Loss Analysis of the PWM Rectifier

Loss Component	**One**	**Total**
IGBT Conduction Loss	174 W	1392 W
IGBT Switching Loss	467 W	3736 W
Diode Conduction Loss	511 W	4088 W
Diode Reverse Recover Loss	109 W	872 W
Total Power Loss	1261 W	10.1 kW

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{4.44}$$

The power loss and efficiency calculation presented here is valid for full power operation in motoring mode where the converter is in rectification mode. Therefore, conduction period of diodes is much longer than that of IGBTs. For regenerative braking mode of operation, the efficiency of the system changes due to the fact that the converter operates in inversion mode and conduction time of IGBTs is longer than that of diodes. It is also known that the on-state voltages of IGBT and diode are not the same. Efficiency analysis in regenerative braking mode of operation at full power has also been carried out by following the same procedure shown in this part. IGBT and diode current waveforms for one cycle of fundamental frequency at rated power are shown in Figures 4.30 and 4.31, respectively, on which conduction periods and turn-on and turn-off times are also highlighted. The power loss calculation during regenerative braking mode of operation is based on processing of these data on a routine implemented on MATLAB and the data of the selected IGBT module presented in Appendix A.

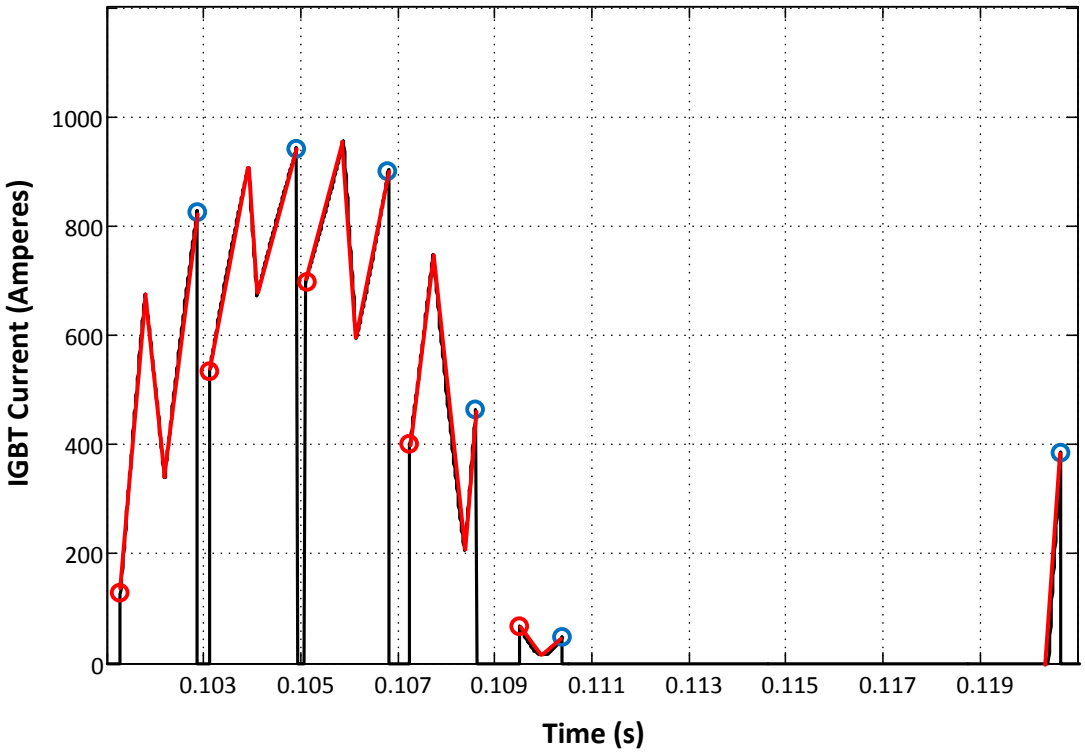


Figure 4.30: IGBT Current Waveform in Regenerative Braking Mode of Operation

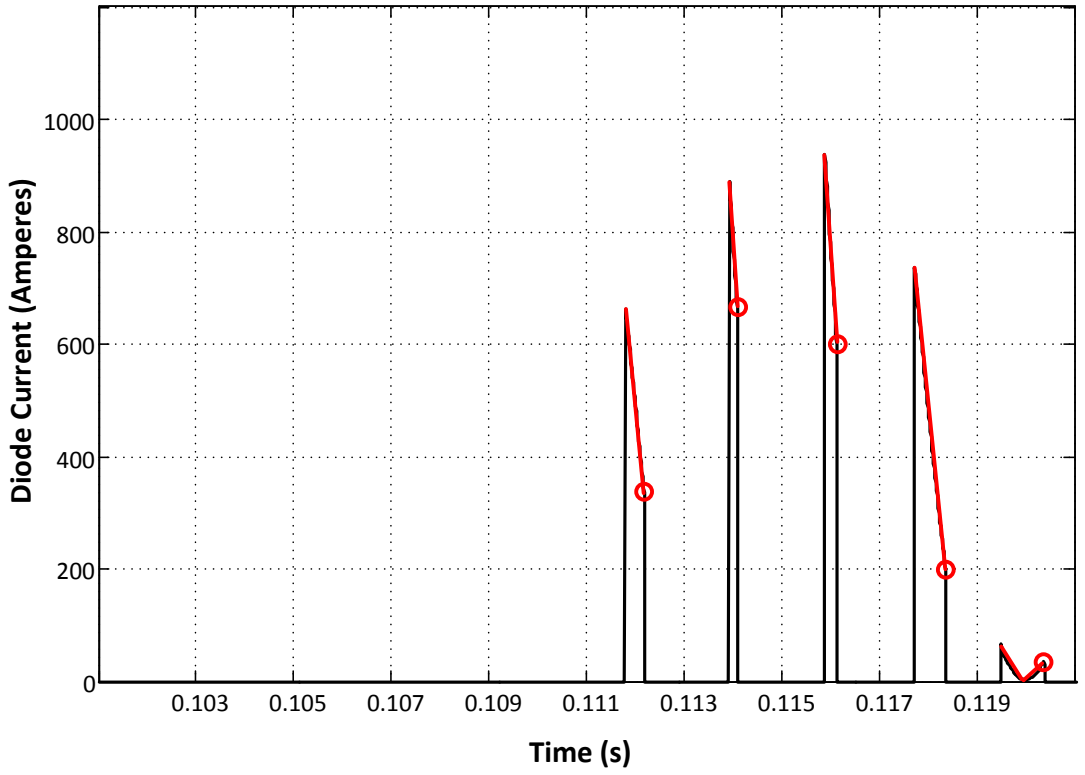


Figure 4.31: Diode Current Waveform in Regenerative Braking Mode of Operation

The power loss analysis of the PWM rectifier in regenerative braking mode of operation is given in Table 4.8 and the total power loss is found as 9.9 kW at rated output power. The efficiency of the rectifier in regenerative braking mode is calculated as 99.2 % which is almost the same as the one in motoring mode.

Table 4.9: Power Loss Analysis of the PWM Rectifier in Regenerative Braking Mode of Operation

Loss Component	**One**	**Total**
IGBT Conduction Loss	568 W	4544 W
IGBT Switching Loss	480 W	3840 W
Diode Conduction Loss	83 W	664 W
Diode Reverse Recover Loss	107 W	856 W
Total Power Loss	1238 W	9.9 kW

4.8. Summary

In this chapter, design of the PWM rectifier is performed and explained in detail. First of all, power semiconductor devices are selected with the help of IGBT and diode voltage and current waveforms obtained by computer simulations. The general design methodology is based on the variation of system constraints such as efficiency, voltage ripple and TDD with system parameters. First, switching frequency is determined by considering mostly its effect on the line current harmonic content. Then, it is validated that the resultant converter efficiency is above the specified limit with the selected switching frequency. Values of passive elements (inductances and capacitances) are to be selected as low as possible to reduce size, weight and cost. Exact AC line inductance value selection is performed to comply with the 5 % TDD limit. Designed AC line inductor and DC link capacitor values are validated by their effects on the DC link peak to peak voltage ripple. DC link series LC filter tuned to second harmonic

component is a resonant filter so that the multiplication of the two individual passive components is definite. Through their design, voltage rating of the filter capacitor is considered. In order to design the control system; i.e., select the controller parameters, PWM rectifier power stage (plant) is modelled with some approximations for simplification. DC side and AC side are modelled as dependent but separate plants. From the models, plant transfer functions are formulated. Design of the control loops are designed using their open loop and closed loop transfer functions, several methods used in control theory and MATLAB tool. Design of these loops are fundamentally based on transient analysis and its indices such as maximum overshoot, rise time, settling time etc., stability analysis with Routh Hurwitz Stability Criterion and Root Locus Method, steady state analysis and frequency response methods. Finally, efficiency analysis of the interleaved two-level PWM rectifier is performed with the selected system parameters, power semiconductor devices and other components. Power semiconductor losses are first formulated and their voltage and current waveforms are used along with the device parameter characteristics such as saturation voltage, switching energy etc. on a MATLAB routine to determine the system efficiency for both motoring and regenerative braking operation modes at rated power. The results of the design procedure can be summarized as shown in Table 4.9.

Table 4.10: System Parameters Determined During Design Procedure

IGBT Module Voltage Rating	3300 V
IGBT Module Current Rating	1200 A
Switching Frequency	500 Hz
AC Line Inductance	1 mH
DC Link Capacitance	5 mF
DC Link LC Filter Capacitance	2.8 mF
DC Link LC Filter Inductance	0.9 mH

CHAPTER 5

SIMULATION RESULTS

5.1. Introduction

In this chapter, the simulation work performed on MATLAB/Simulink simulation environment will be presented. The simulation models used in this work can be seen in Appendix B section. The models are composed of catenary line, front-end transformer, power stage of the PWM rectifier, control block of the PWM rectifier, motor drive system and traction motor. Technical specifications of the simulation work can be found in Table 5.1.

Table 5.1: Technical Specifications of the Simulation Work

Rated Output Power	1.25 MW	AC Line Inductance	1 mH
Catenary Voltage	25 kV	DC Link Capacitance	5 mF
Catenary Frequency	50 Hz	DC Link LC Filter Inductance	0.9 mH
Rated Line Current	50 A	DC Link LC Filter Capacitance	2.8 mF
Transformer Secondary Voltage	1050 V	DC Link Voltage PI Con. K_p and K_i	1/80
Rated Current/Converter	600 A	AC Line Current PI Con. K_p and K_i	90/2
DC Link Voltage	1800V	AC Line Current PR Con. K_p and K_i	10/10
Switching Frequency	1 kHz	AC Line Current PR Con. w_o and w_c	314/1

5.2. Phase Locked Loop and Pulse Width Modulation

Phase output of the PLL module at steady state can be seen in Figure 5.1 along with the supply voltage. Transient performance of the PLL module is verified in Figure 5.2 against sudden magnitude change, in Figure 5.3 against sudden frequency change and in Figure 5.4 against sudden phase change.

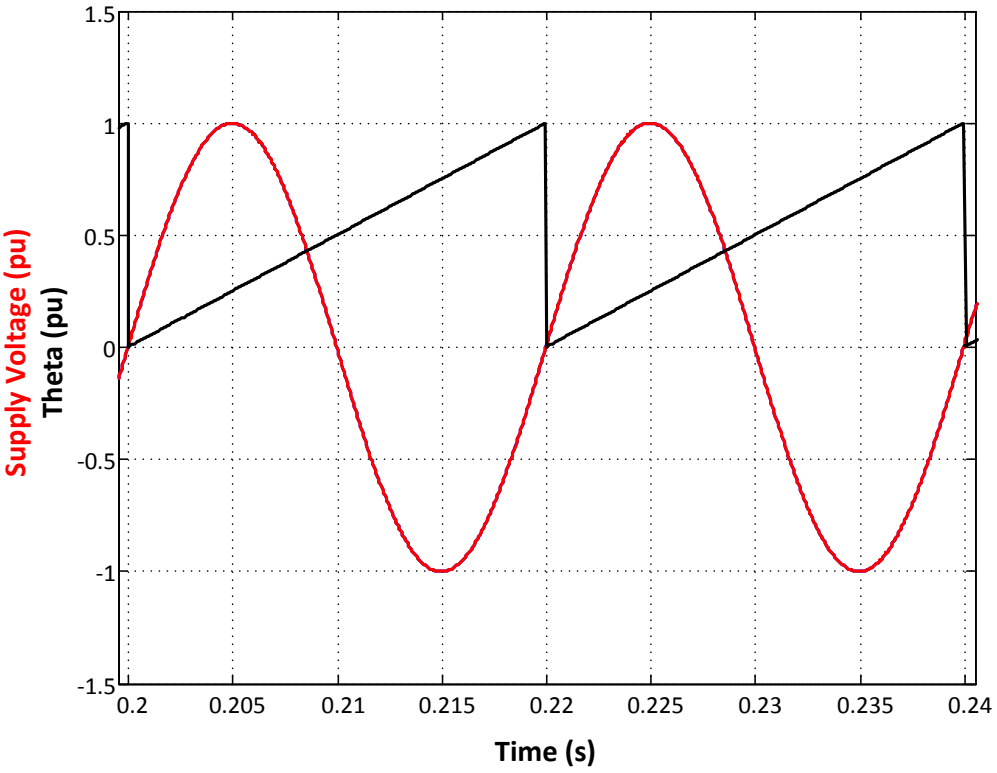


Figure 5.1: Steady State Performance of PLL with Phase Output and Supply Voltage

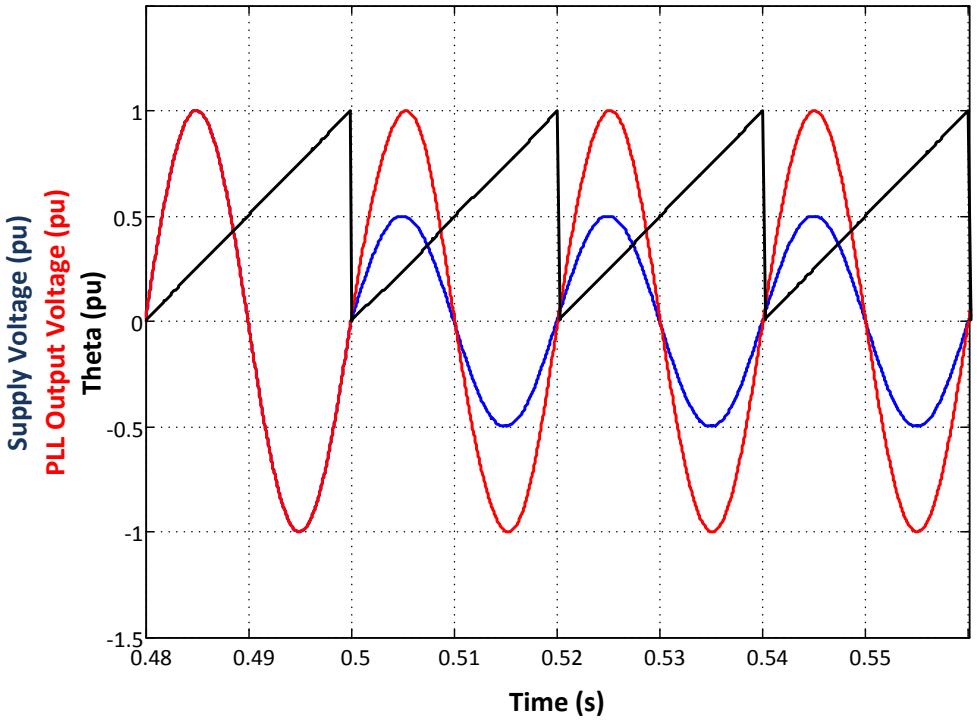


Figure 5.2: Transient Performance of the PLL against Sudden Magnitude Change (1/2 @ t = 0.5 sec)

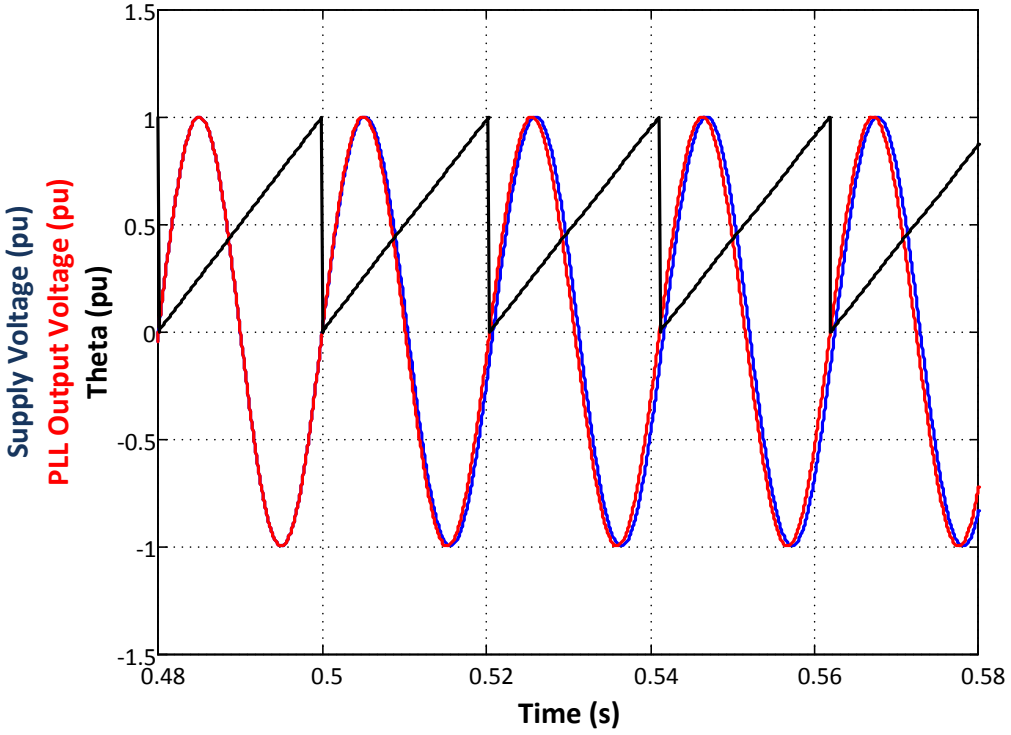


Figure 5.3: Transient Performance of the PLL against Sudden Frequency Change (2 Hz @ t = 0.5 sec)

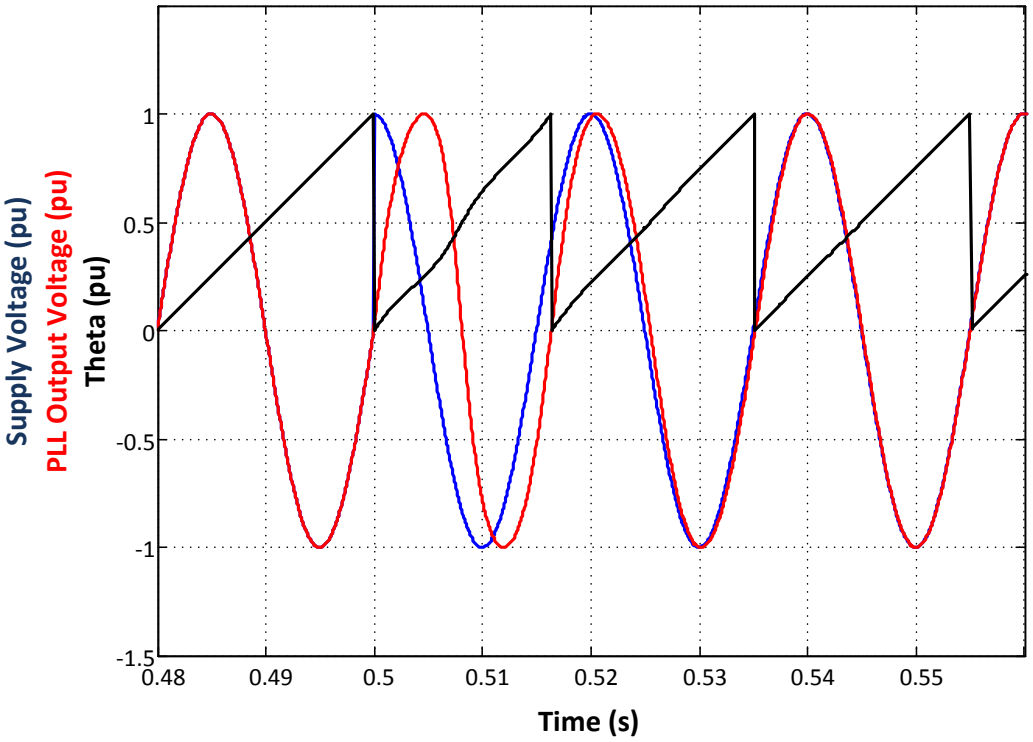


Figure 5.4: Transient Performance of the PLL against Sudden Phase Change (90^0 @ t = 0.5 sec)

The phase shifted PWM operation is seen in Figure 5.5 showing gate drive signals of two corresponding IGBTs of each module. In Figure 5.6, the converter output voltage waveforms of each converter are shown separately.

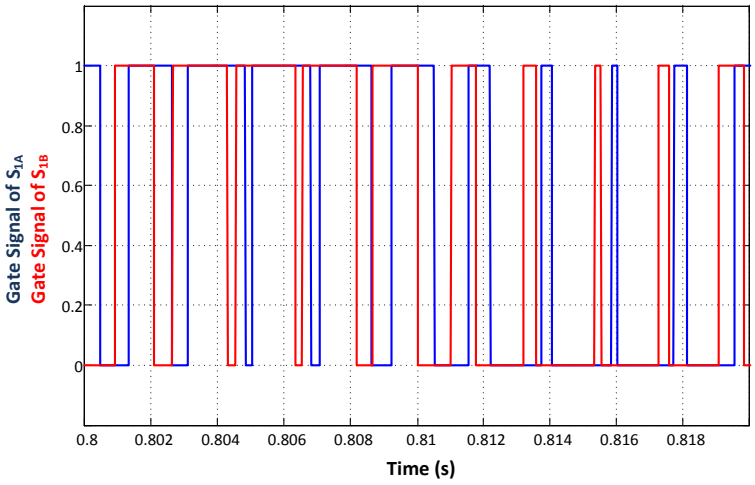


Figure 5.5: Phase Shifted PWM Operation

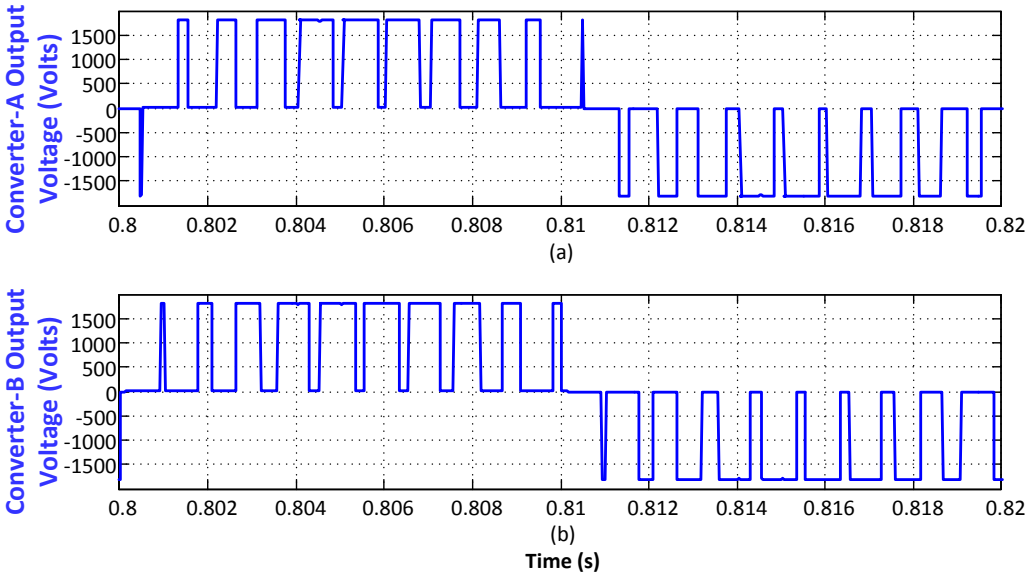


Figure 5.6: Converter Output Voltage Waveforms: (a) Converter A, (b) Converter B

5.3. Unity pf Operation

Unity power factor operation is visualized in Figure 5.7 showing supply voltage and primary side current of the front-end transformer. In addition, the input currents of each converter and total input current are shown in Figure 5.8.

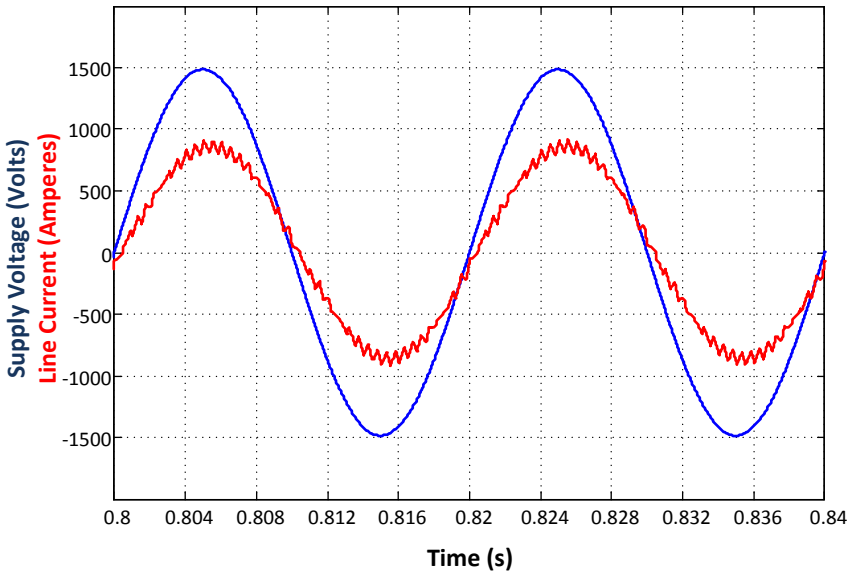


Figure 5.7: Unity Power Factor Operation in Motoring Mode

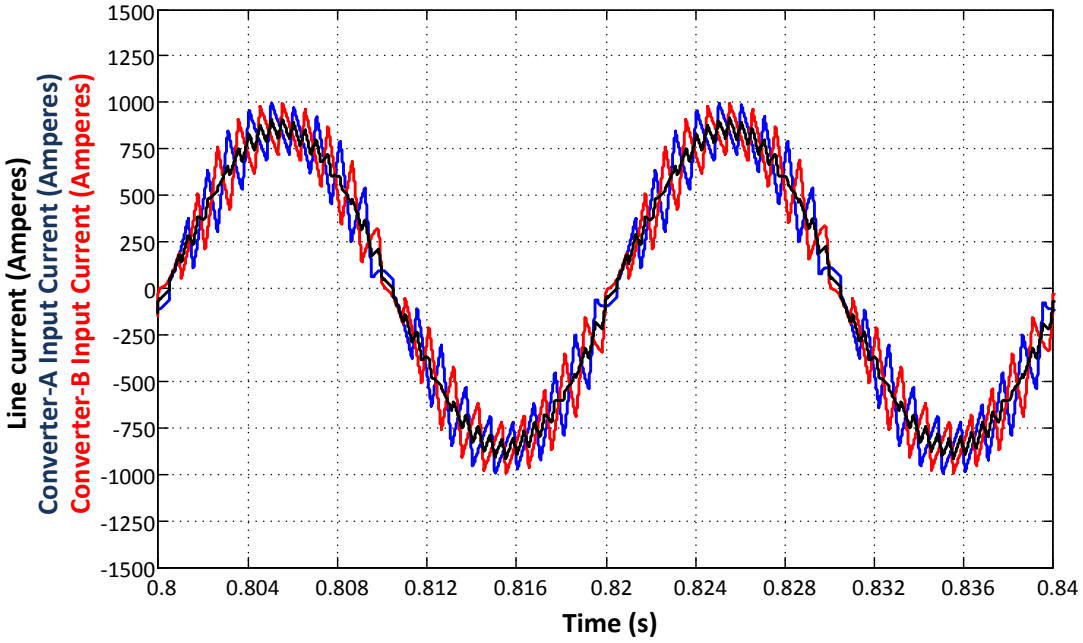


Figure 5.8: Converter Input Currents and Total Input Current

5.4. Regenerative Braking Operation Mode

Regenerative braking mode of operation is shown in Figure 5.9 showing supply voltage and primary side current of the front-end transformer. In addition, the input currents of each converter and total input current are shown in Figure 5.10.

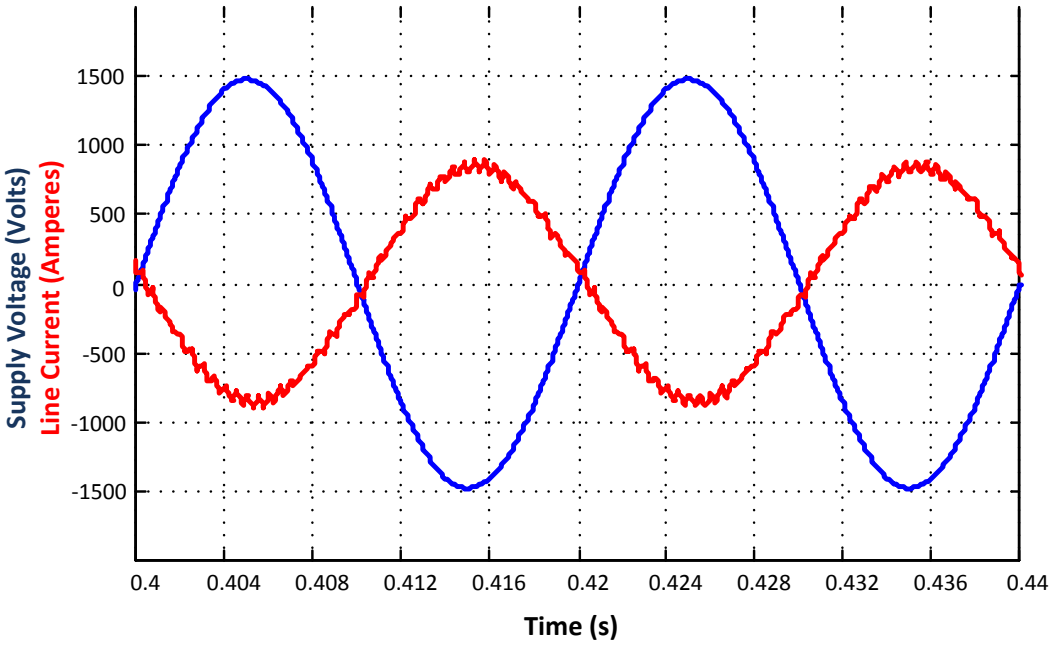


Figure 5.9: Unity Power Factor Operation at Regenerative Braking Mode

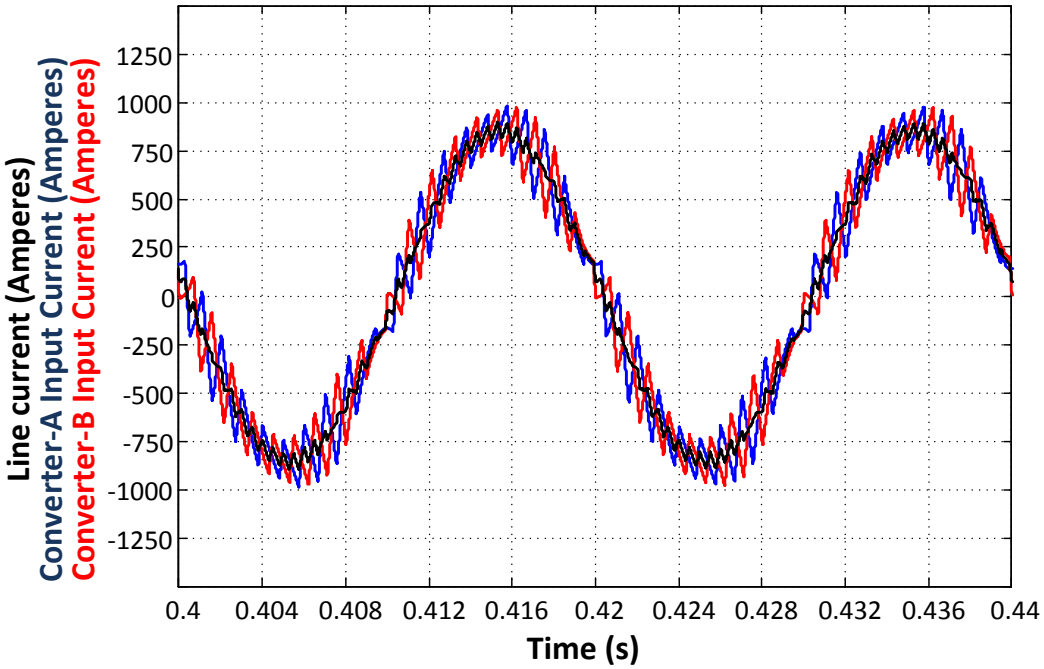


Figure 5.10: Converter Input Currents and Total Input Current during Regenerative Braking Operation Mode

5.5. DC Link Voltage and Current Waveforms

DC link voltage at steady state and DC link voltage ripple are shown in Figures 5.11 and 5.12, respectively. DC link input current is shown along with DC link output current in Figure 5.13, with DC link capacitor current in Figure 5.14 and with DC link series LC filter current in Figure 5.15.

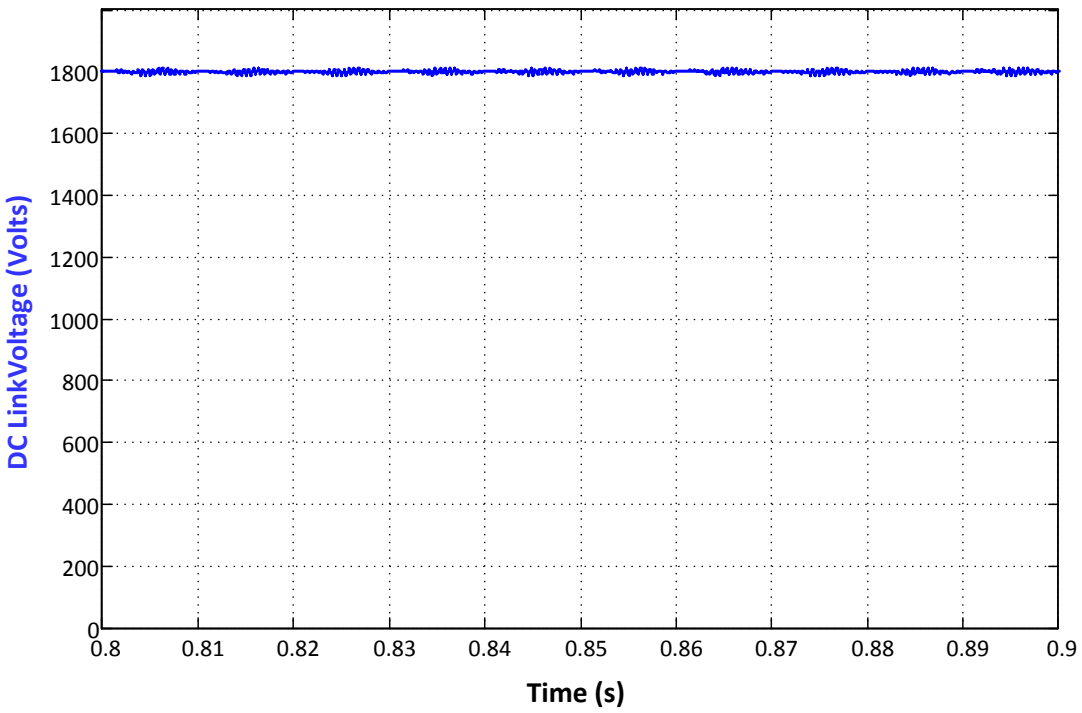


Figure 5.11: DC Link Voltage at Steady State

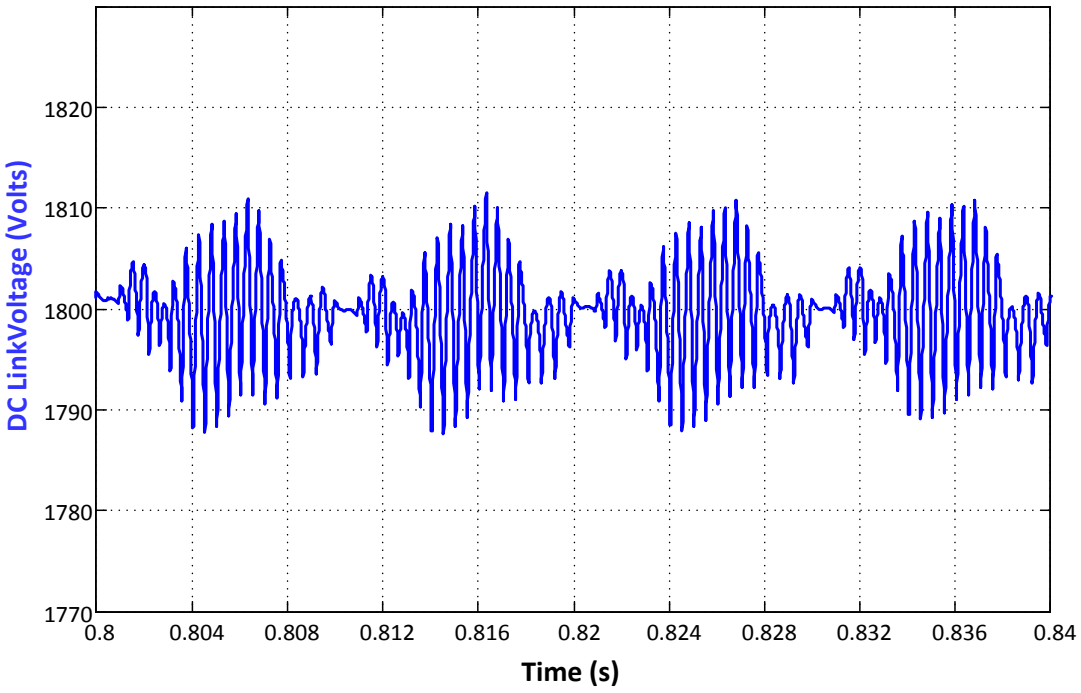


Figure 5.12: DC Link Voltage Ripple

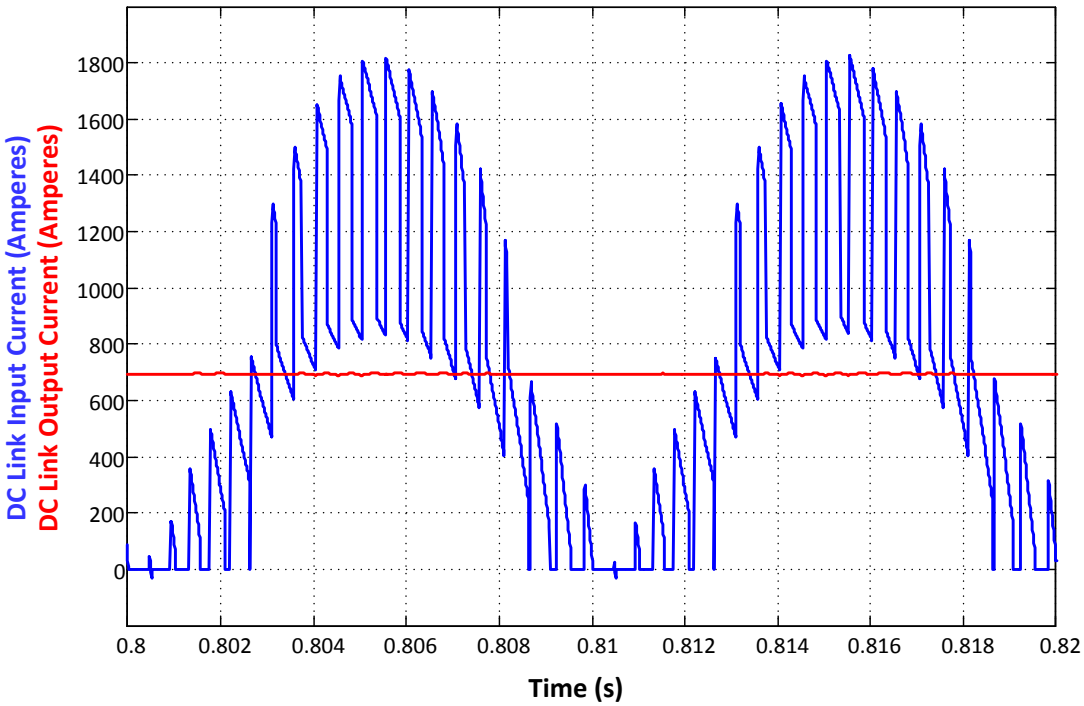


Figure 5.13: DC Link Input Current and Output (Load) Current

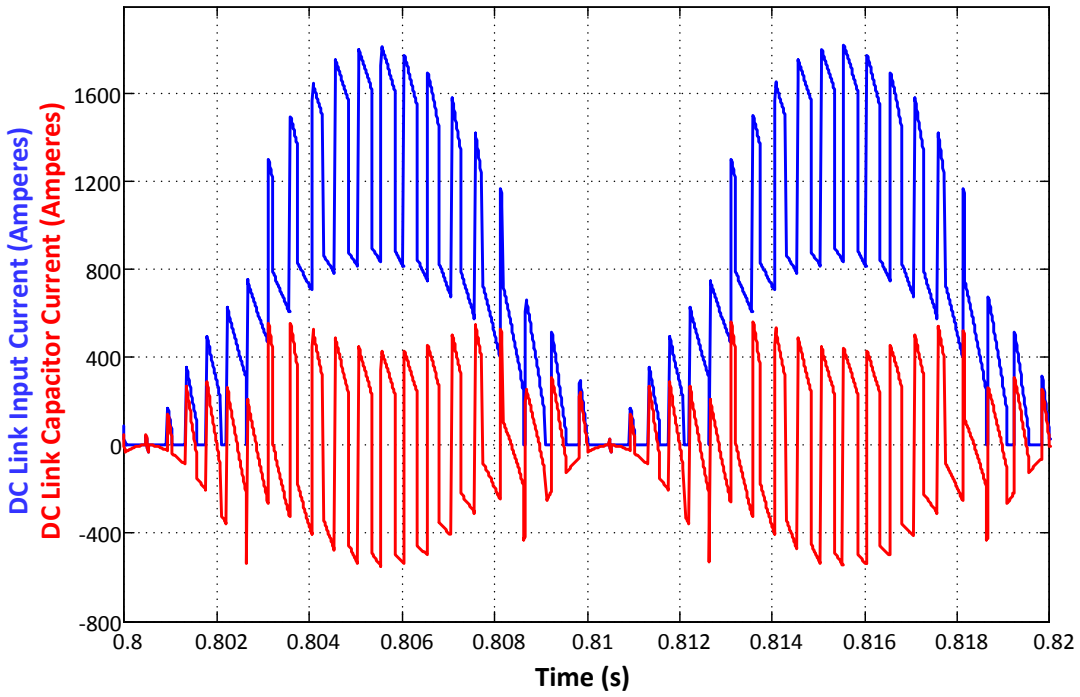


Figure 5.14: DC Link Input Current and Capacitor Current

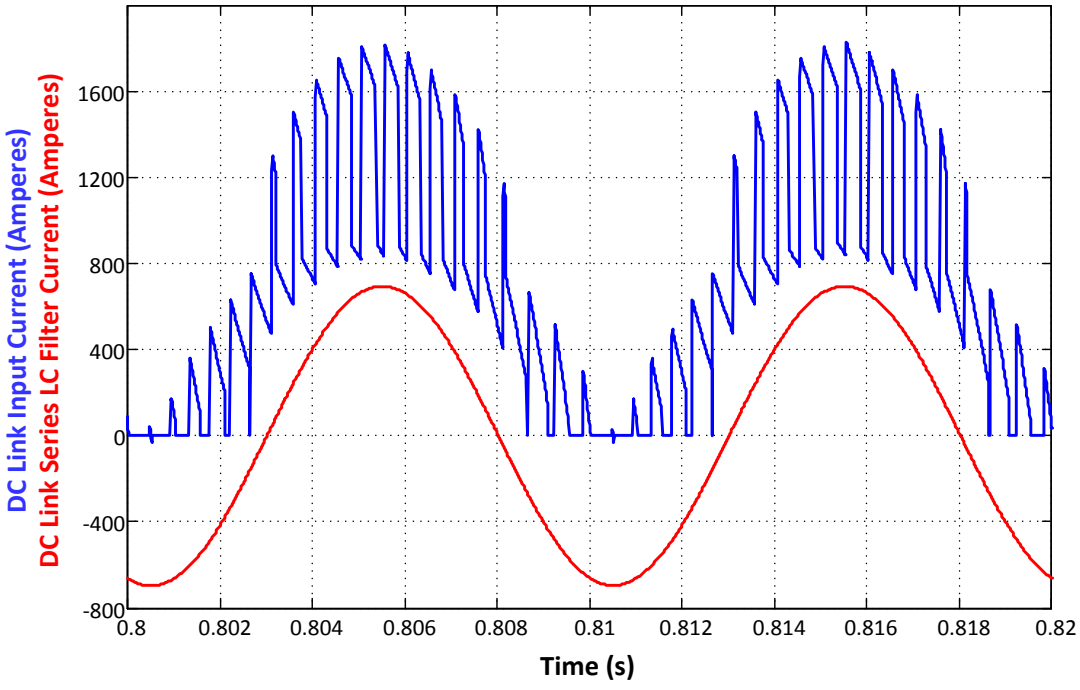


Figure 5.15: DC Link Input Current and Series LC Filter Current

5.6. Harmonic Analysis

The harmonic spectrum of total input current, converter-A input current and converter-B input current are shown in Figures 5.16, 5.17 and 5.18, respectively, with their THD values. The harmonic spectrum of DC link voltage and DC link current are shown in Figures 5.19 and 5.20, respectively.

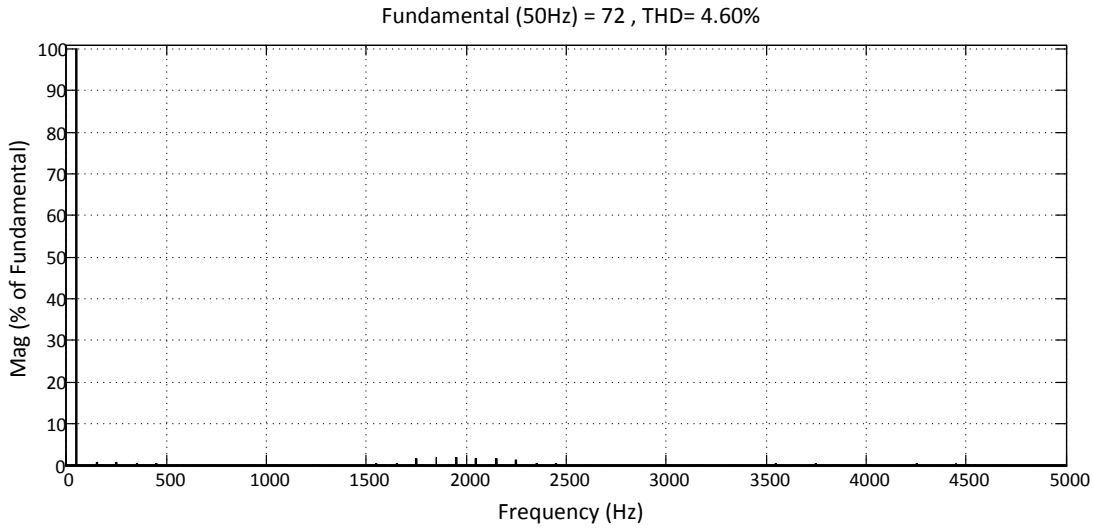


Figure 5.16: Harmonic Spectrum of the Total Input Current

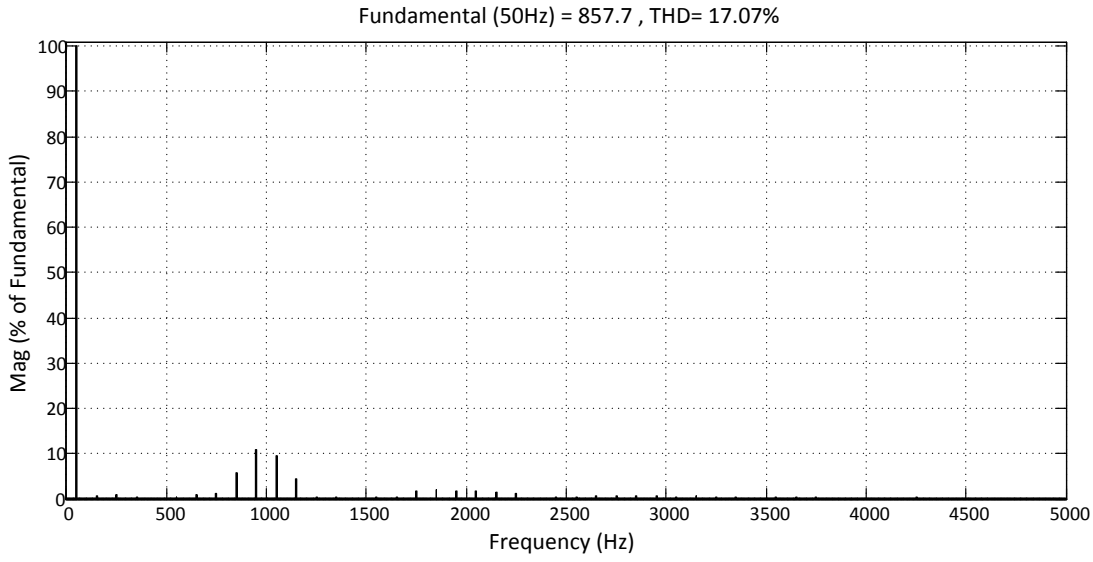


Figure 5.17: Harmonic Spectrum of the Converter-A Input Current

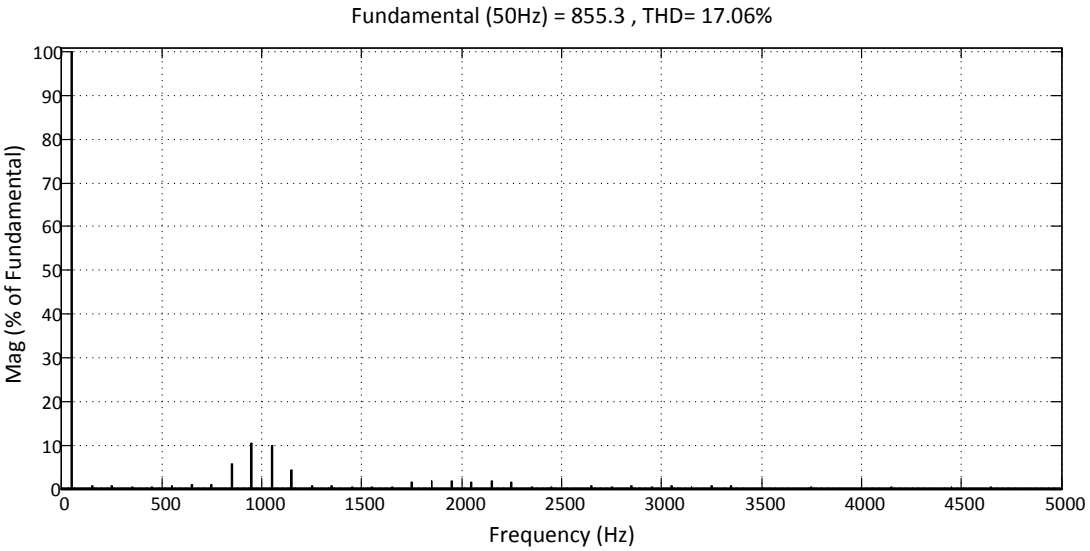


Figure 5.18: Harmonic Spectrum of the Converter-B Input Current

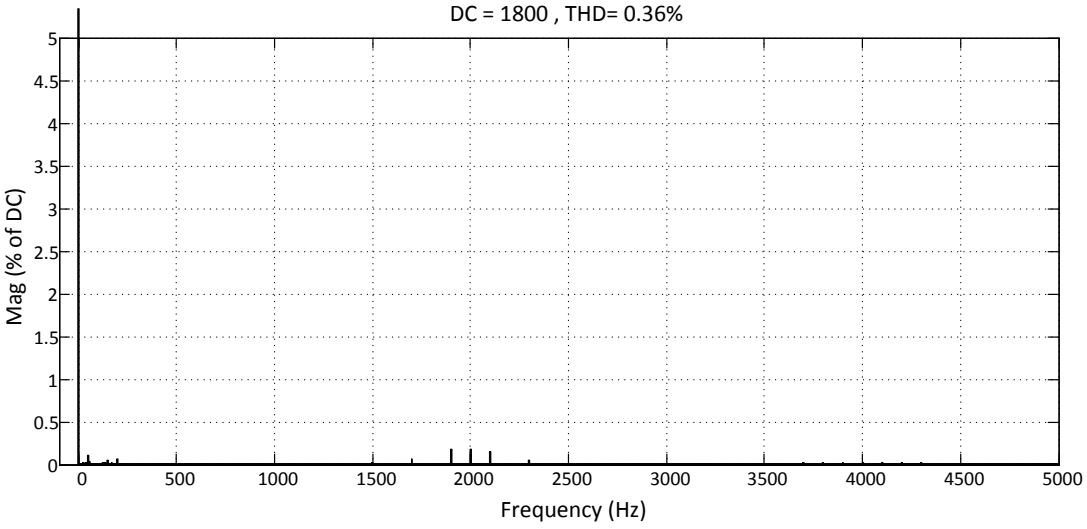


Figure 5.19: Harmonic Spectrum of the DC Link Voltage

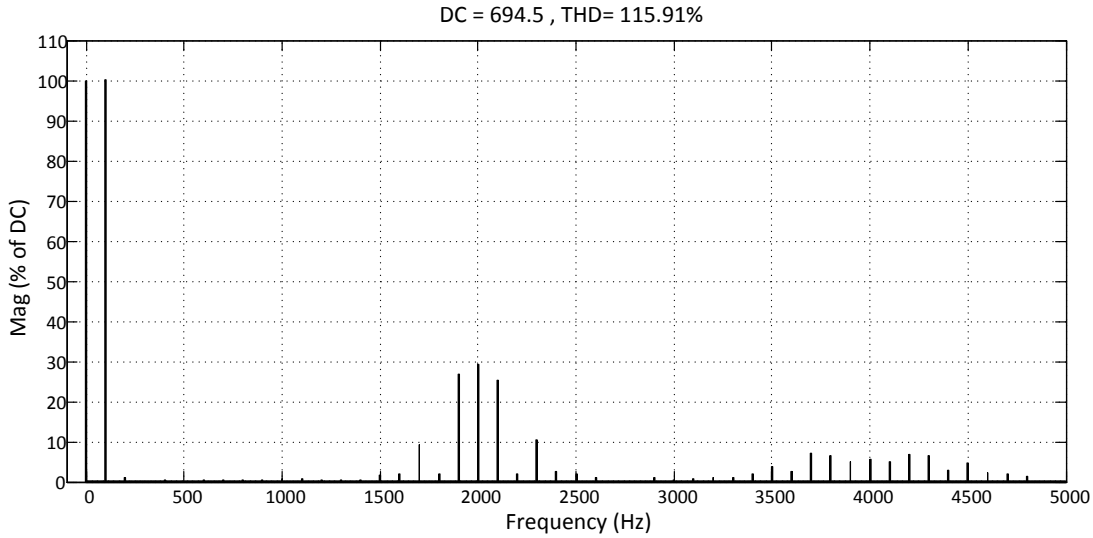


Figure 5.20: Harmonic Spectrum of the DC Link Current

5.7. Transient Performance

The transient performance of the system is visualized by the application of a step load change from 10 % to 100 % as shown in Figure 5.21 and from 100 % to 10 % as shown in Figure 5.22 showing the response of the DC link voltage. In addition, the response of input current is shown in Figures 5.23 and 5.34 to the same load changes.

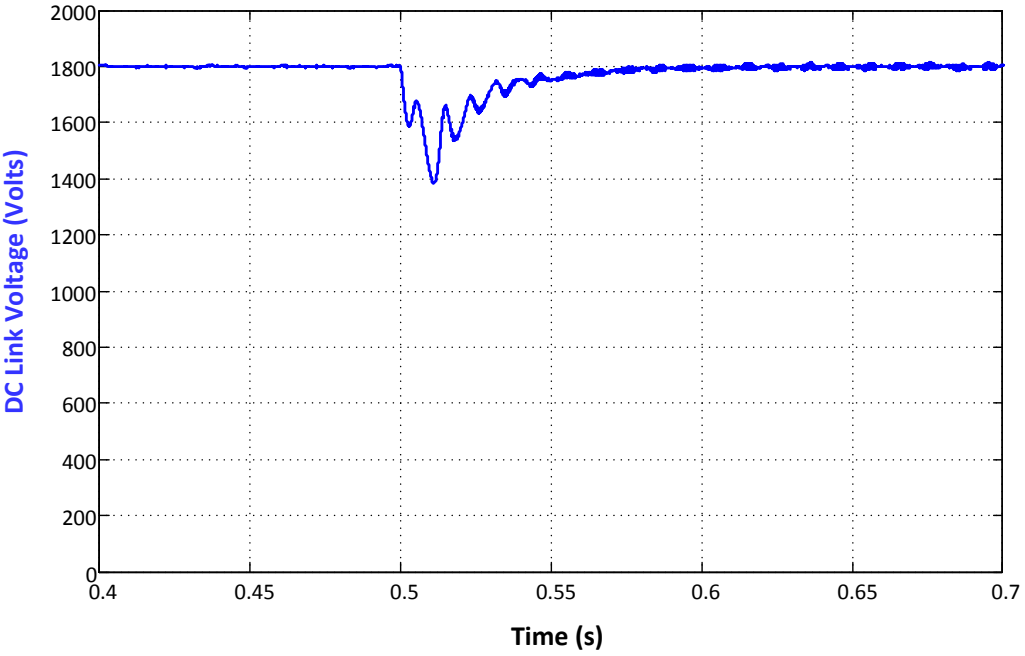


Figure 5.21: DC Link Voltage Transient Response to the Step Load Change from 10 % to 100 %

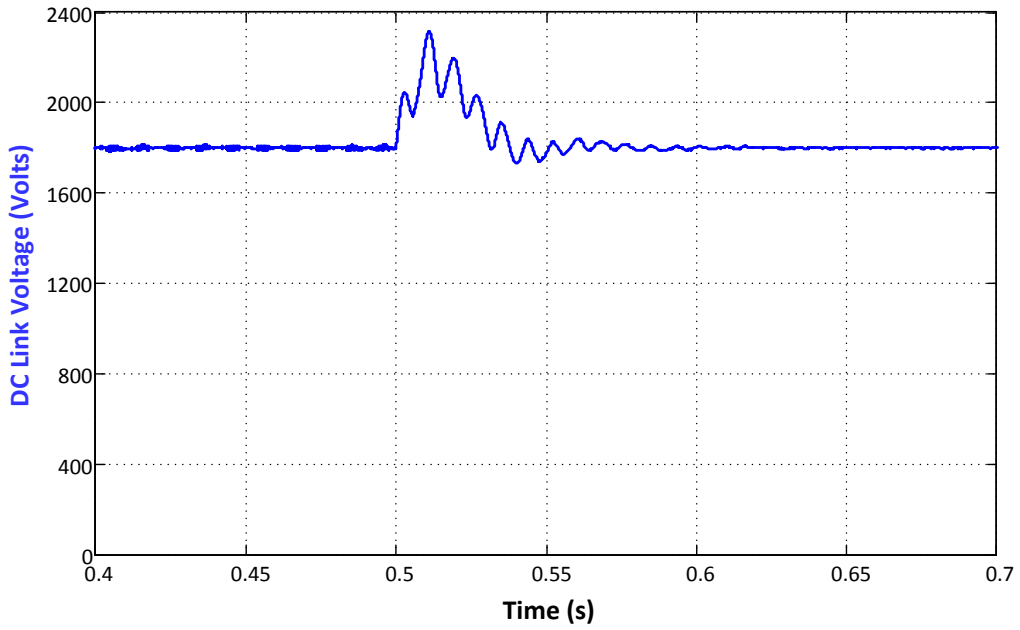


Figure 5.22: DC Link Voltage Transient Response to the Step Load Change from 100 % to 10 %

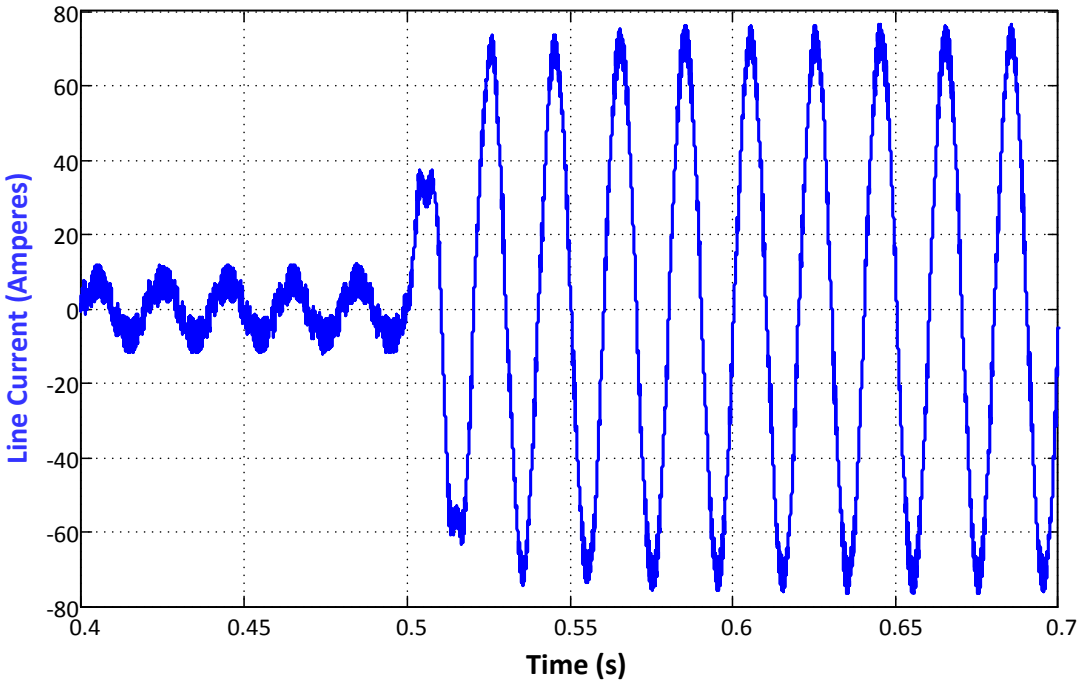


Figure 5.23: Input Current Transient Response to the Step Load Change from 10 % to 100 %

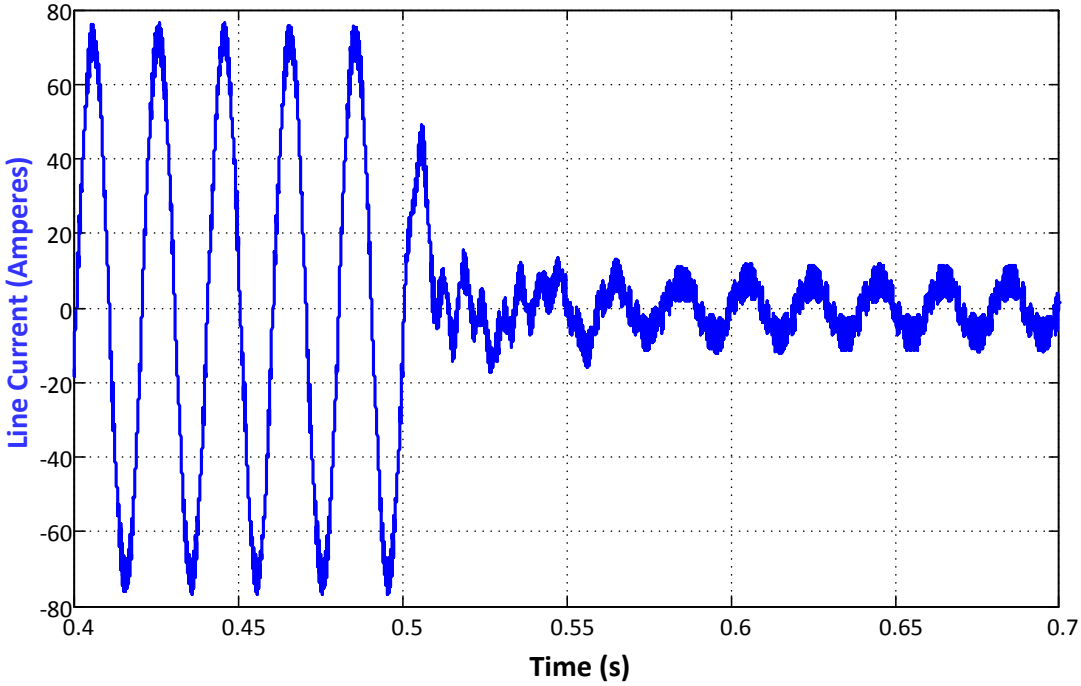


Figure 5.24: Input Current Transient Response to the Step Load Change from 100 % to 10 %

5.8. System Performance With PR Current Controller

The performance of the system with PR current controller can be seen in Figure 5.25 showing supply voltage and primary side current of the front-end transformer. Furthermore, the input currents of each converter and total input current are shown in Figure 5.26 with supply voltage.

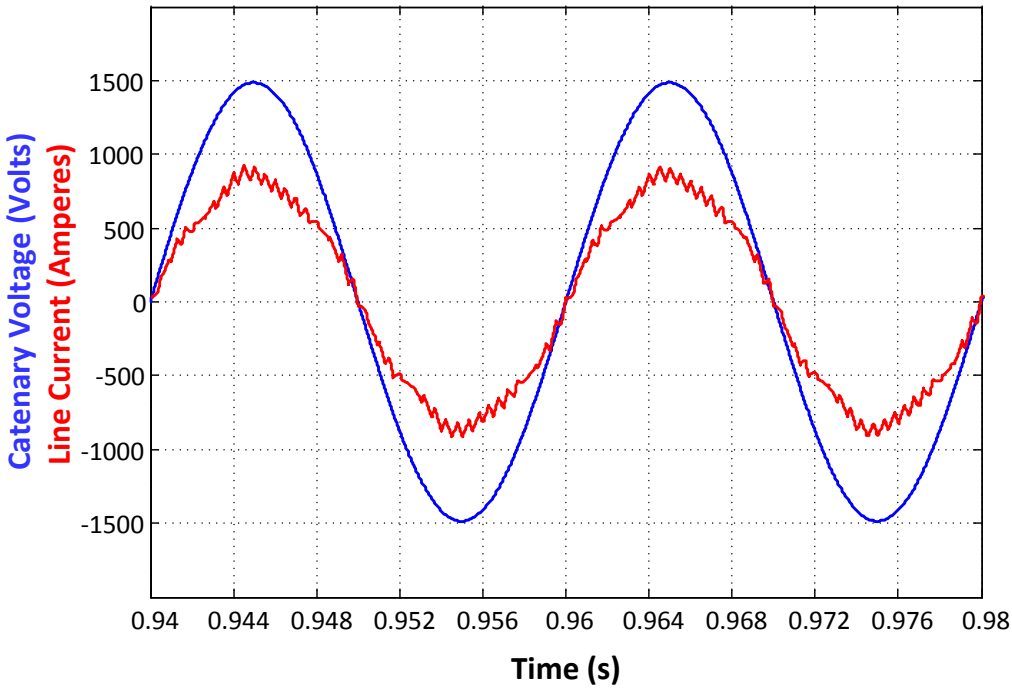


Figure 5.25: The Performance of the System with PR Current Controller

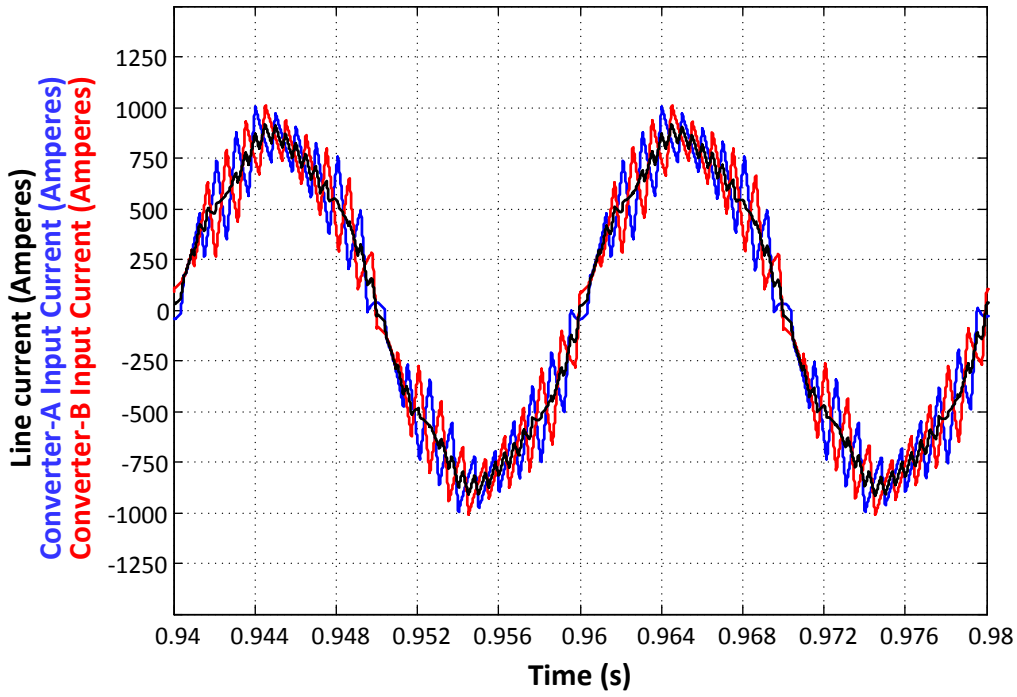


Figure 5.26: Converter Input Currents and Total Current with PR Current Controller

5.9. Efficiency Analysis

Input power and output power of the PWM rectifier under rated conditions are shown in Figure 5.27. These results yield 99.2 % rated efficiency. Additionally, the variation of PWM rectifier efficiency for lower power rates is shown in Figure 5.28.

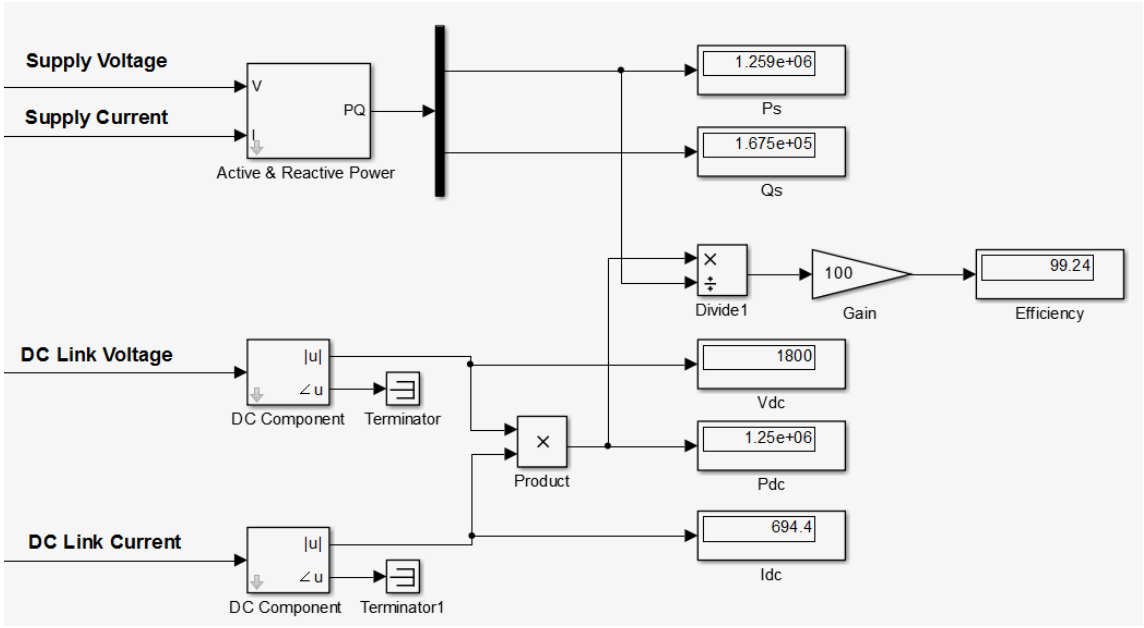


Figure 5.27: Input Power and Output Power of the PWM Rectifier under Rated Conditions and Rated Efficiency

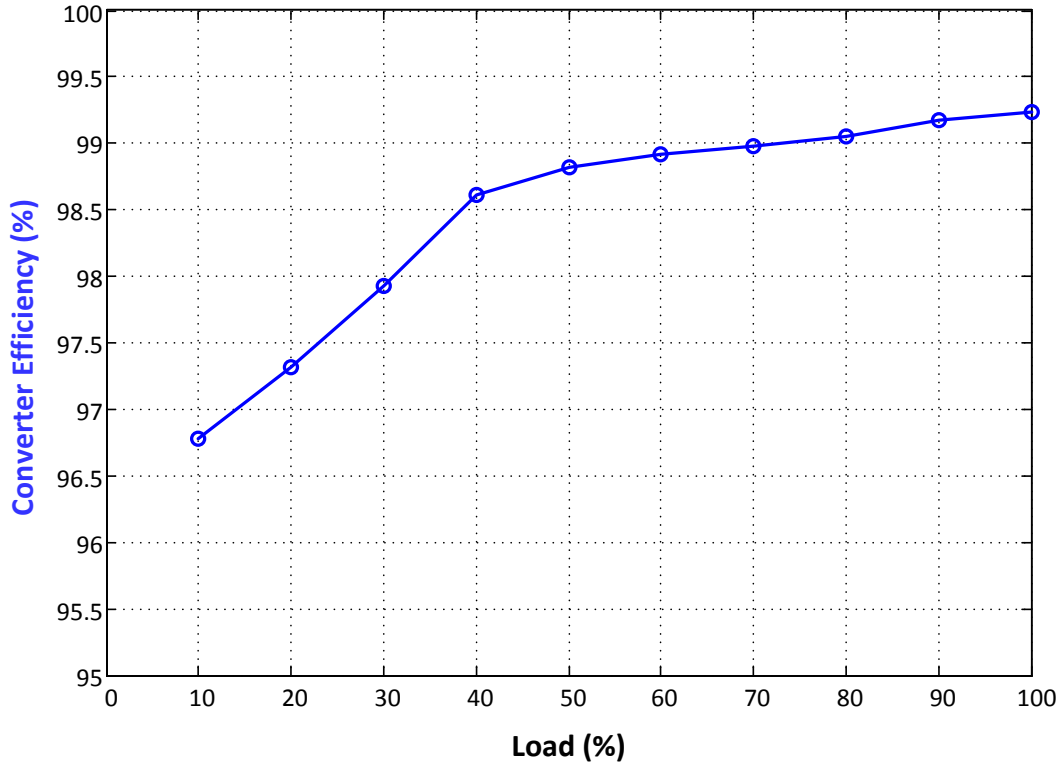


Figure 5.28: Variation of PWM Rectifier Efficiency for Lower Power Rates

5.10. Discussions

System performance resulting from the simulation work is summarized in Table 5.2.

Table 5.2: System Performance Resulting From the Simulation Work

Rated Efficiency (Motoring)	99.2 %	Power Factor with PI Controller	0.992
Rated Efficiency (Reg. Brk.)	99.2 %	Power Factor with PR Controller	1
TDD of Line Current	4.6 %	Maximum Overshoot	20 %
TDD of Converter-A Current	17.1 %	Rise Time	0.14 s
TDD of Converter-B Current	17.1 %	Settling Time	0.18 s
DC Link Voltage Ripple	1.4 %	Steady State Error	0 %

Following conclusions can be drawn from the simulation results:

- Input power factor is not exactly unity when PI current regulator is used, as expected. With the utilization of PR regulator, unity power factor operation is achieved. On the other hand, utilization of linear current regulator with PR regulator resulted in slightly higher TDD values. Revision on the controller parameters may be necessary for further improvement.
- Phase shifted operation is validated by the harmonic spectrum and TDD results. TDD of the input current of each converter is around 17 % whereas TDD of the line current is below 5 % meeting the harmonic distortion requirements.
- Converter efficiency resulting from the simulation work with the power semiconductor models used in Simulink is consistent with the theoretical efficiency calculation. It is proven that line current TDD standards can be complied with switching frequency rates as low as 500 Hz resulting in efficiencies higher than 99 %.
- The converter performance during motoring mode of operation is achieved for regenerative braking mode at rated power.

- The DC link voltage ripple result at rated output power is below the specified limit confirming the design of passive filters.
- The second harmonic component on the DC link current is successfully filtered by the series LC filter which is tuned to 100 Hz. However, during transient state, this harmonic component is amplified on the DC link voltage resulting in overshoot and undershoot values higher than expected. A more detailed transient response based control system design (including the effects of the LC filter) seems to be required to overcome this.

CHAPTER 6

EXPERIMENTAL RESULTS

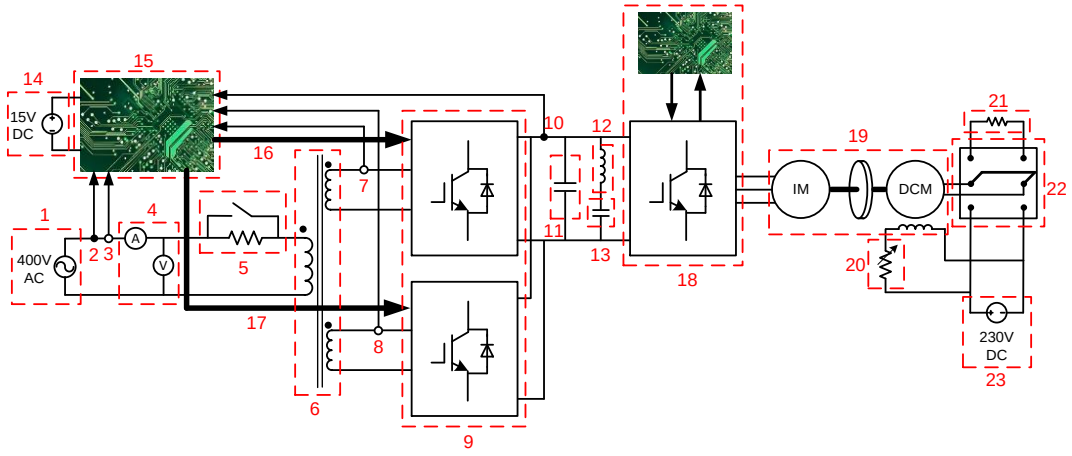
6.1. Introduction

In this chapter, the experimental work carried out on the prototype system developed in Electrical Machines and Drives Laboratory will be presented. The block diagram and the photograph of the experimental setup are shown in Figures 6.1, 6.2 and 6.3, respectively. Generally, the prototype system is composed of the developed PWM Rectifier power stage and control stage, motor drive apparatus employing three phase inverter, control card and software, and the universal machine set with a three phase squirrel cage induction machine, flywheel, torque and speed transducers and DC machine.

Technical specifications of the developed PWM rectifier prototype system can be found in Appendix C including IGBT modules, front-end transformer and passive filters. Discretization of the transfer functions for use in the digital control system can be seen in Appendix D. Moreover, implementation of the digital control software on TMS320F28335 DSP is explained in Appendix E with flowcharts. The control PCB of the prototype system is explained in Appendix F including schematics and layout. The component list of the low voltage prototype is shown in Appendix G. Finally, the laboratory equipment used for the tests is listed in Appendix H section. Technical specifications of the experimental work can be found in Table 6.1.

Table 6.1: Technical Specifications of the Experimental Work

Rated Output Power	3.5 kW	Switching Frequency	1 kHz
Supply Voltage	380 V	AC Line Inductance	40 mH
Catenary Frequency	50 Hz	DC Link Capacitance	5 mF
Rated Line Current	10 A	DC Link LC Filter Inductance	2.53 mH
Transformer Secondary Voltage	380 V	DC Link LC Filter Capacitance	1 mF
Rated Current/Converter	5 A	DC Link Voltage PI Con. K_p and K_i	0.1/0.05
DC Link Voltage	700 V	AC Line Current PI Con. K_p and K_i	5/10



1. AC Supply of the Laboratory
2. LEM Voltage Transducer (LV25-P)
3. LEM Current Transducer (HXS20-NP)
4. Single Phase Wattmeter (XX)
5. Soft Start Circuitry (Switch + Rheostat)
6. Input Transformer
7. LEM Current Transducer (HXS20-NP)
8. LEM Current Transducer (HXS20-NP)
9. Semikron IGBT H-Bridge Modules
10. LEM Voltage Transducer (LV25-P)
11. DC Link Capacitor Bank
12. DC Link LC Filter Inductor
13. DC Link LC Filter Capacitor
14. TENMA Power Supply
15. Control PCB
16. Semikron IGBT Gate Drive Modules
17. Semikron IGBT Gate Drive Modules
18. Control Techniques Unidrive AC Motor Drive Unit
19. Universal Machine Set (Asynchronous Machine + Flywheel + DC Machine)
20. Field Current Control Rheostat
21. Load Resistor Rheostat
22. Bidirectional DC Switch
23. DC Supply of the Laboratory

Figure 6.1: The Block Diagram of the Experimental Setup

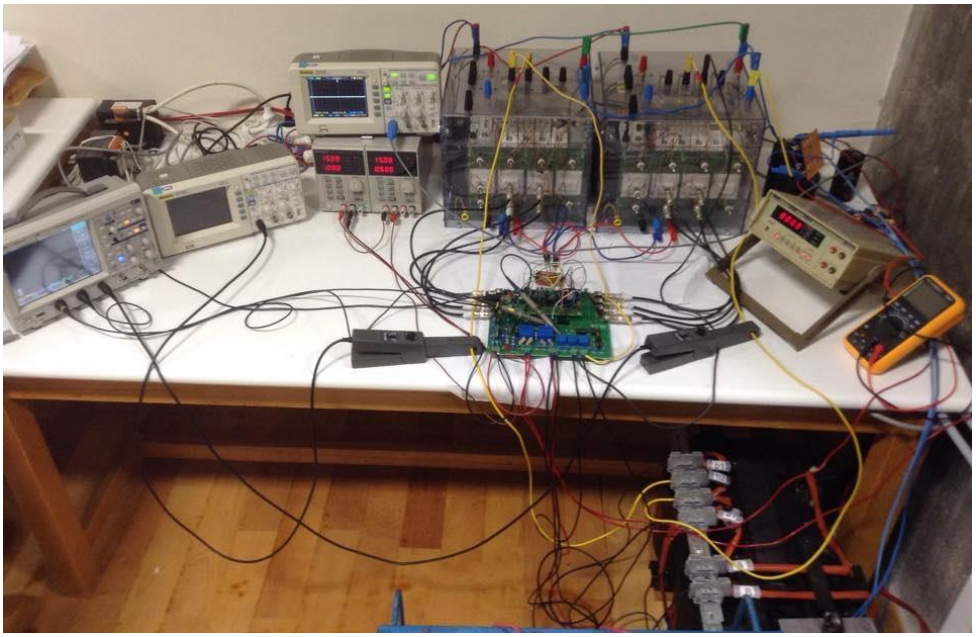


Figure 6.2: The Photograph of the Experimental Setup (PWM Rectifier Side)

Figure 6.3: The Photograph of the Experimental Setup (Inverter Side)

6.2. Phase Locked Loop and Pulse Width Modulation

The performance of PLL module implemented on DSP microcontroller can be seen in Figure 6.4.

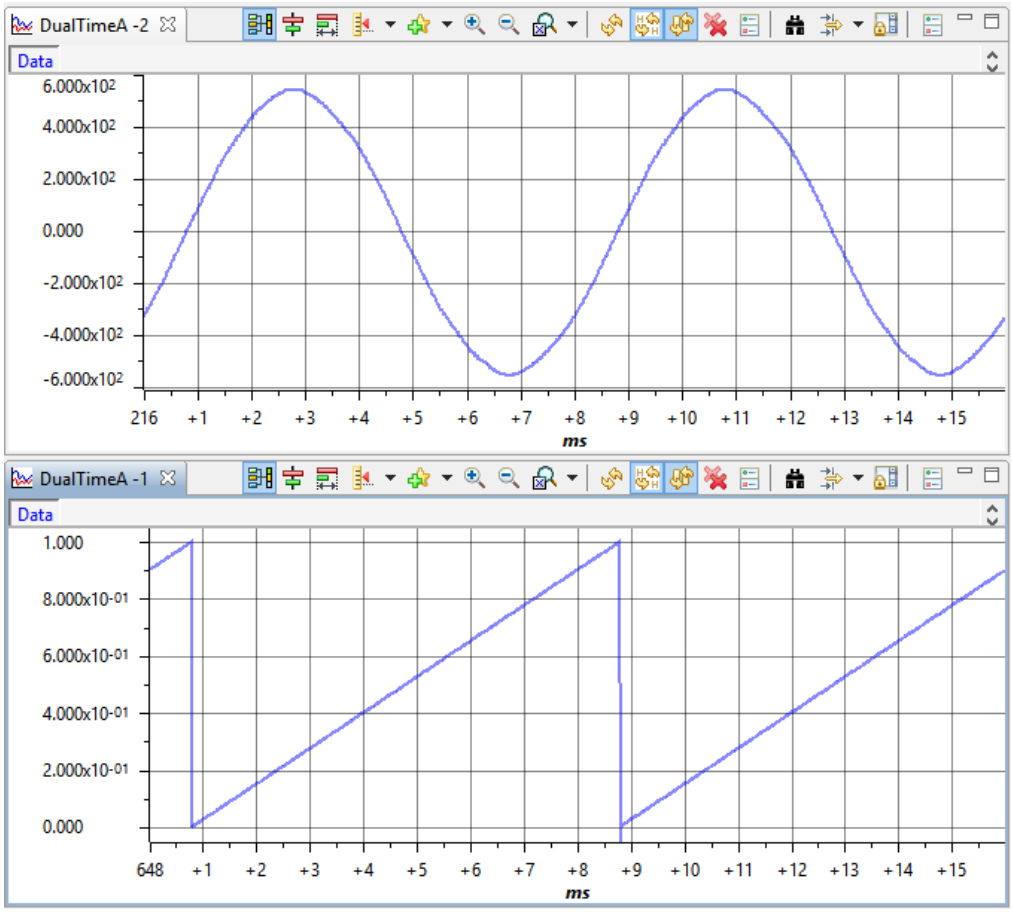


Figure 6.4: The Performance of PLL Module: Phase Output of PLL and Supply Voltage

The phase shifted PWM operation is shown in Figure 6.5 showing gate drive signals of two corresponding IGBTs of each module (S_{1A} and S_{1B}). Moreover, dead band between two IGBTs employing the same bridge arm is shown in Figure 6.6 (S_{1A} and S_{2A}).

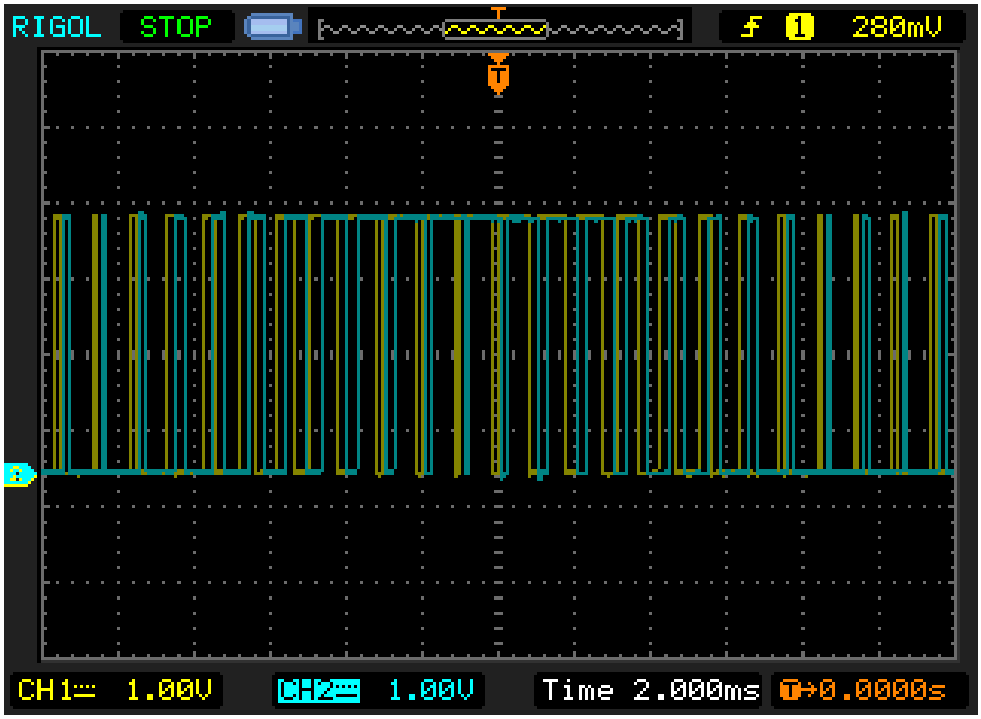


Figure 6.5: Phase Shifted PWM Operation

(CH1: S_{1A} Gate Signal, CH2: S_{1B} Gate Signal)

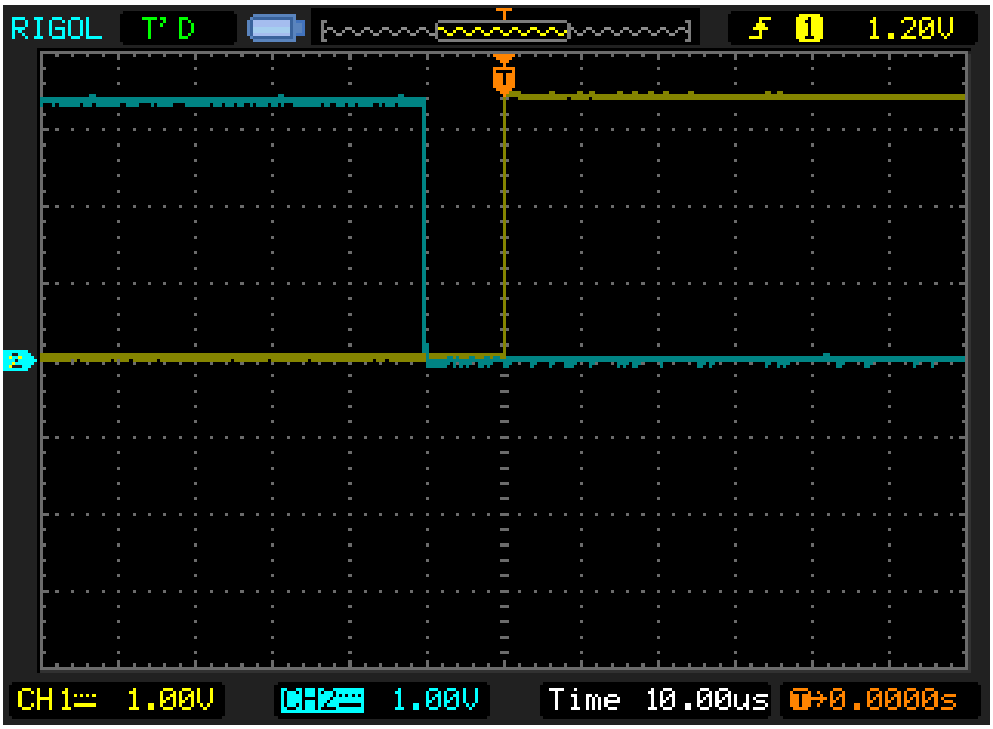


Figure 6.6: Dead Band between Two IGBTs Employing the Same Bridge Arm

(CH1: S_{1A} Gate Signal, CH2: S_{2A} Gate Signal)

6.3. Unity Power Factor Operation

Experimental verification of unity power factor operation is shown in Figure 6.7 showing supply voltage and primary side current of the front-end transformer. In addition, the input currents of each converter are shown in Figures 6.8 and 6.9 with supply voltage.

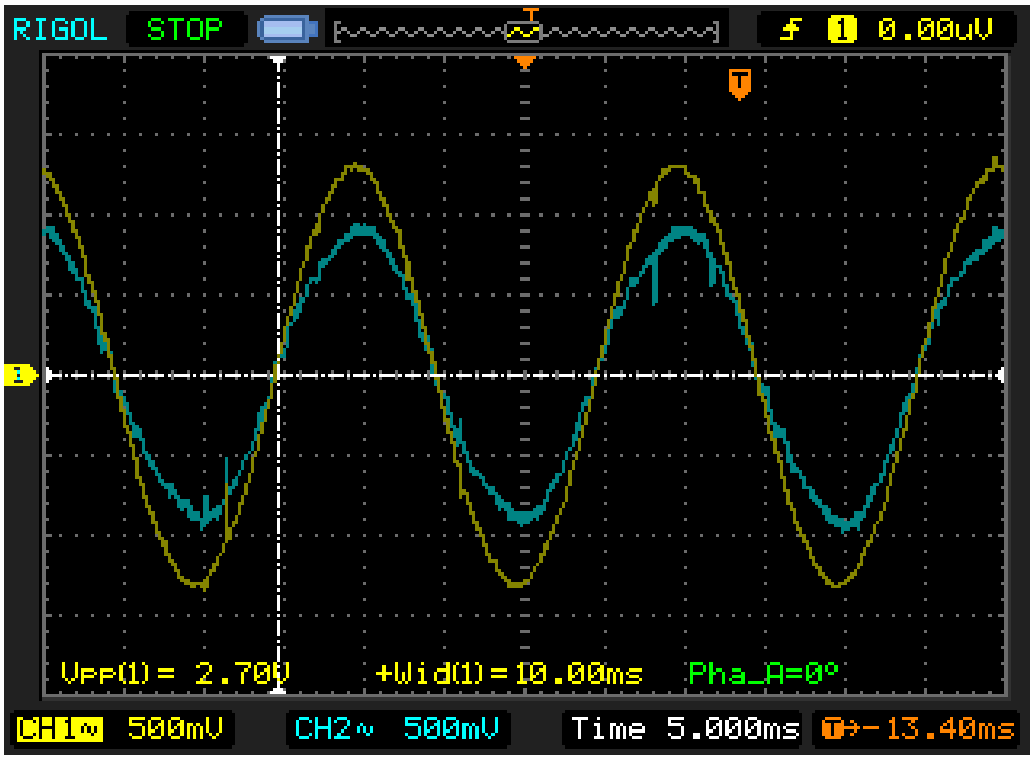


Figure 6.7: Experimental Verification of Unity Power Factor Operation
(CH1: Supply Voltage (2.51mV/V), CH2: Total Input Current (67mV/A))

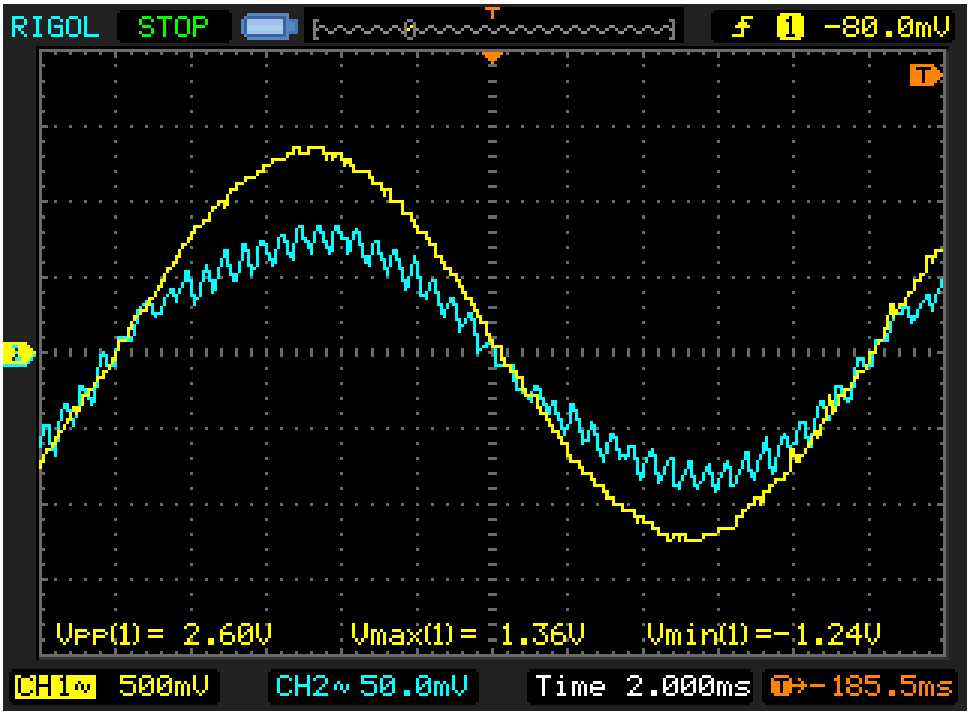


Figure 6.8: Unity Power Factor Operation of Individual Converters

(CH1: Supply Voltage (2.51mV/V), CH2: Converter-A Input Current (12mV/A))

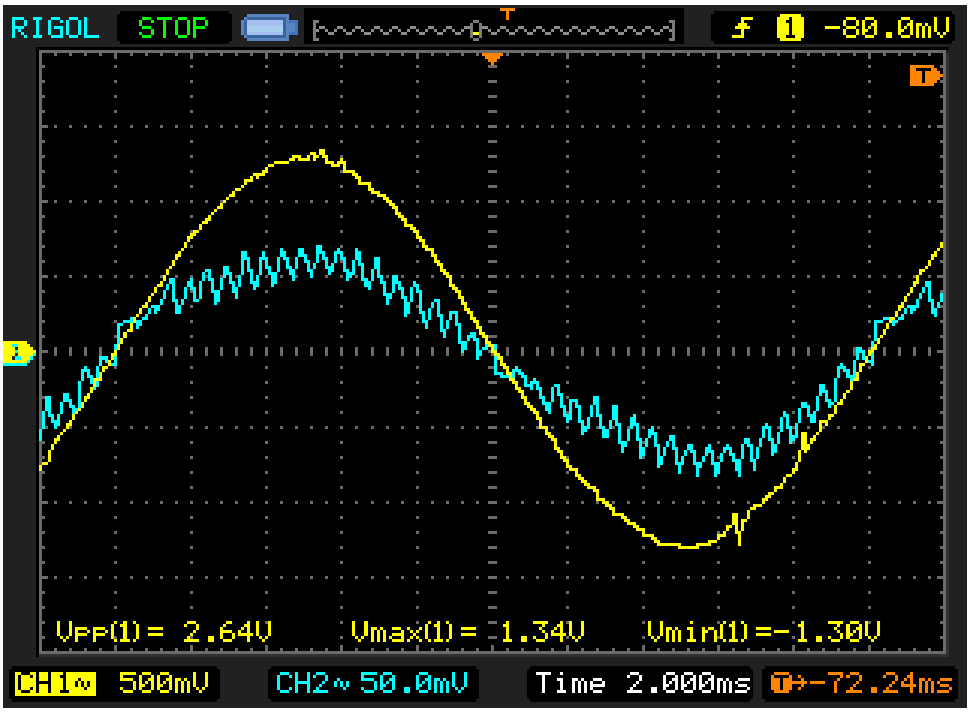


Figure 6.9: Unity Power Factor Operation of Individual Converters

(CH1: Supply Voltage (2.51mV/V), CH2: Converter-B Input Current (10mV/A))

6.4. DC Link Voltage and Current Waveforms

Experimental result of DC link voltage at steady state and DC link voltage ripple are shown in Figures 6.10 and 6.11, respectively. DC link output current is shown in Figure 6.12 and DC link LC filter current is shown in Figure 6.13.

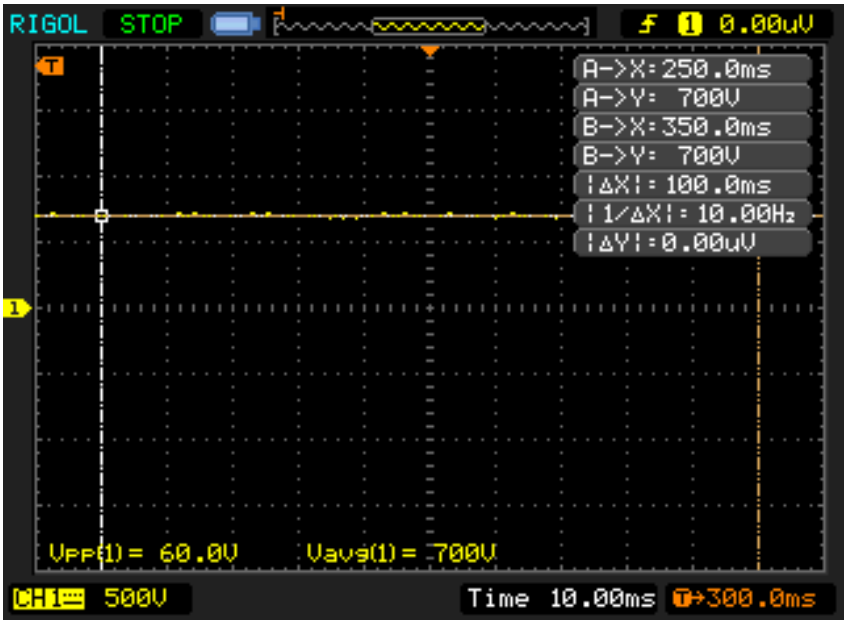


Figure 6.10: Experimental Result of DC Link Voltage at Steady State

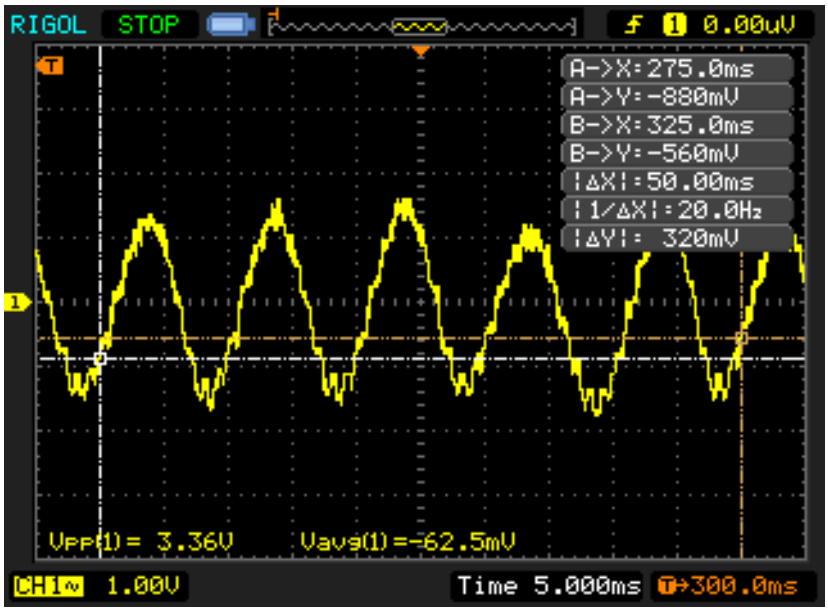


Figure 6.11: Experimental Result of DC Link Voltage Ripple

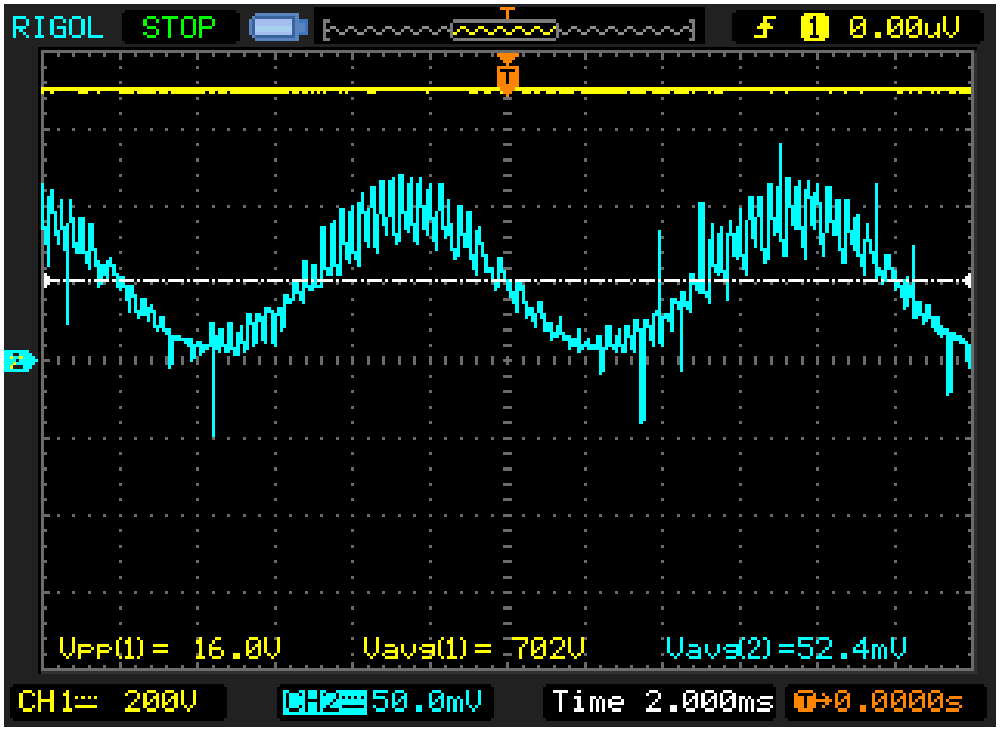


Figure 6.12: Experimental Result of DC Link Input Current

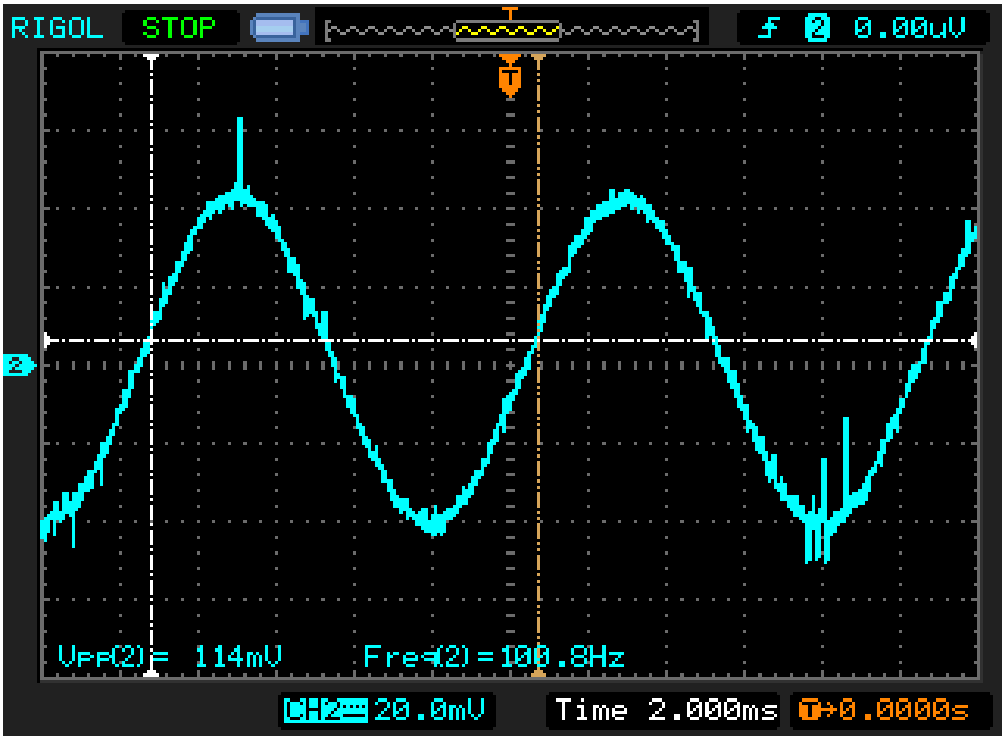


Figure 6.13: Experimental Result of DC Link LC Filter Current (2.5mV/A)

6.5. Harmonic Analysis

The harmonic spectrum of total input current, converter-A input current and converter-B input current are shown in Figures 6.14, 6.15 and 6.16, respectively. The harmonic spectrum of DC link voltage and DC link current are shown in Figures 6.17 and 6.18, respectively.

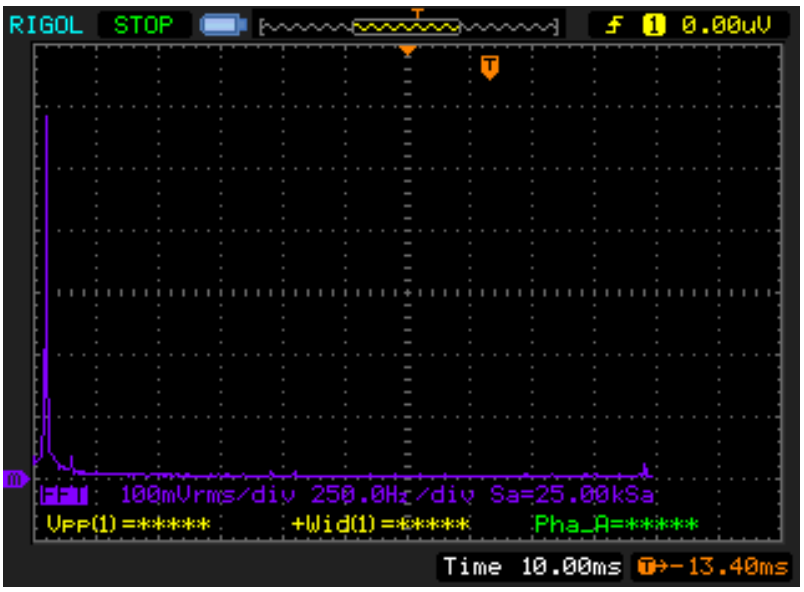


Figure 6.14: Harmonic Spectrum of the Total Input Current - Experimental Result

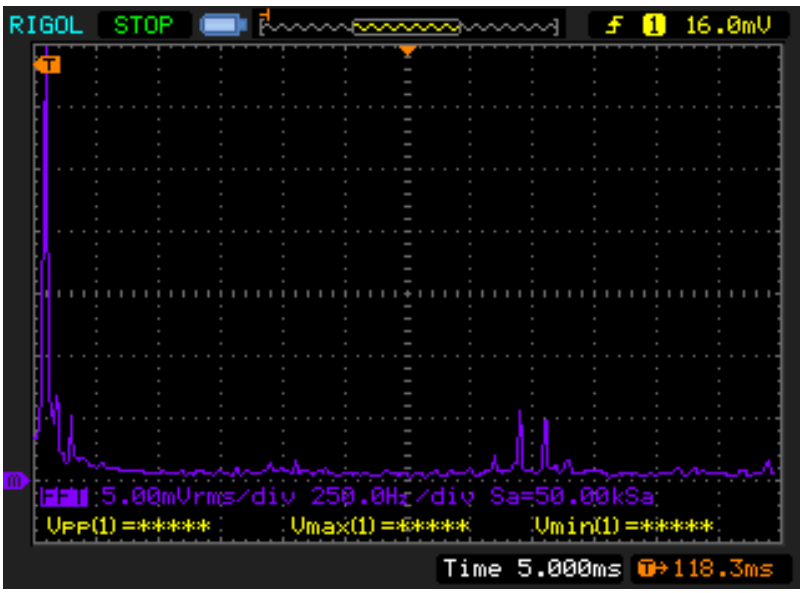


Figure 6.15: Harmonic Spectrum of the Converter-A Current - Experimental Result

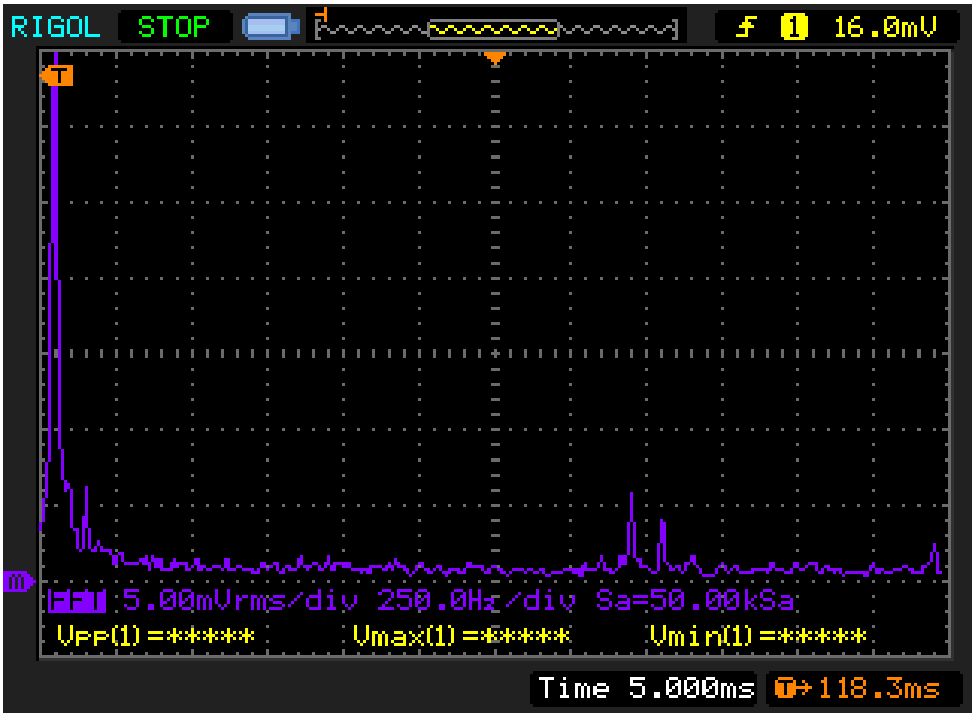


Figure 6.16: Harmonic Spectrum of the Converter-B Current - Experimental Result

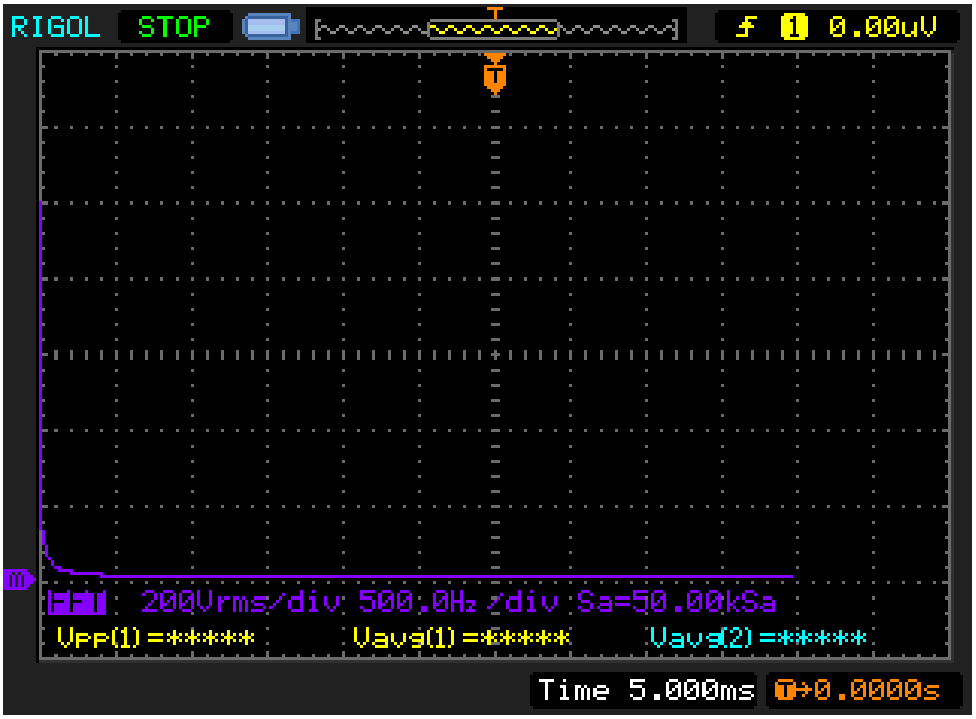


Figure 6.17: Harmonic Spectrum of DC Link Voltage - Experimental Result

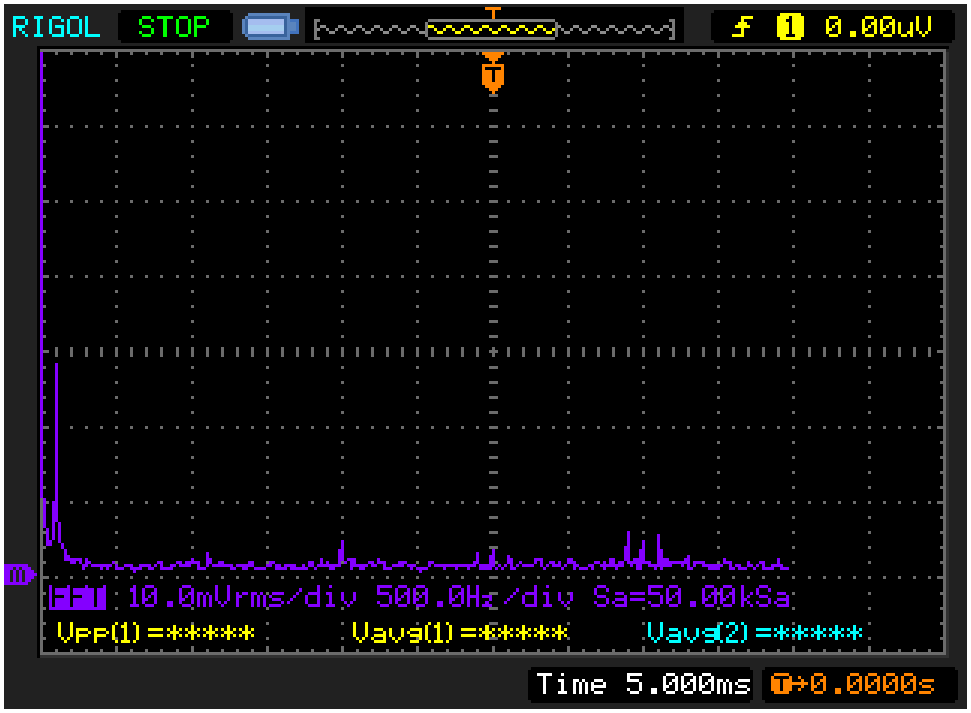


Figure 6.18: Harmonic Spectrum of DC Link Input Current - Experimental Result

6.6. Transient Performance of the System

The transient performance of the system is tested experimentally for the DC Link voltage. DC link voltage response is shown in Figures 6.19 to 6.22 where the transient performance indices of maximum overshoot, rise time, settling time and steady state error are shown, respectively.

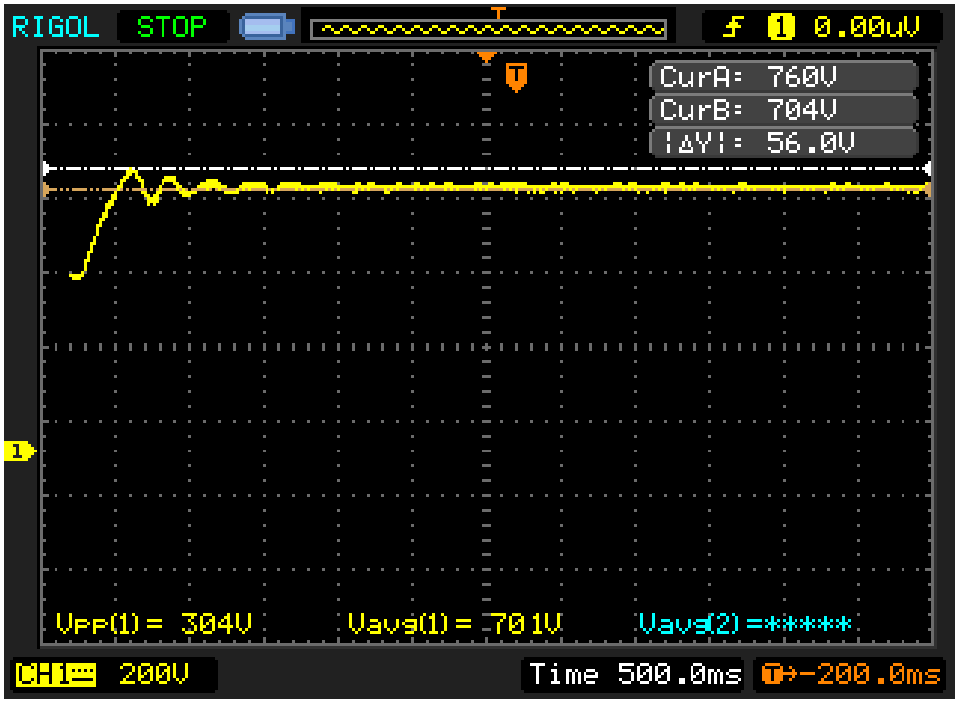


Figure 6.19: DC Link Voltage Transient Response – Overshoot (8.5 %)

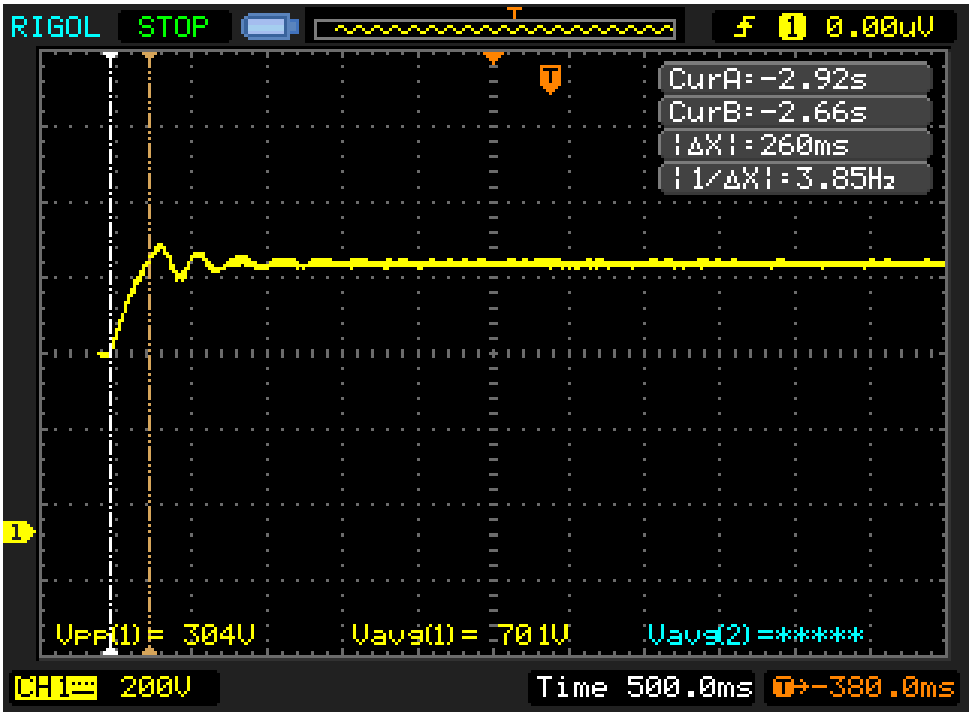


Figure 6.20: DC Link Voltage Transient Response – Rise Time (260 milliseconds)

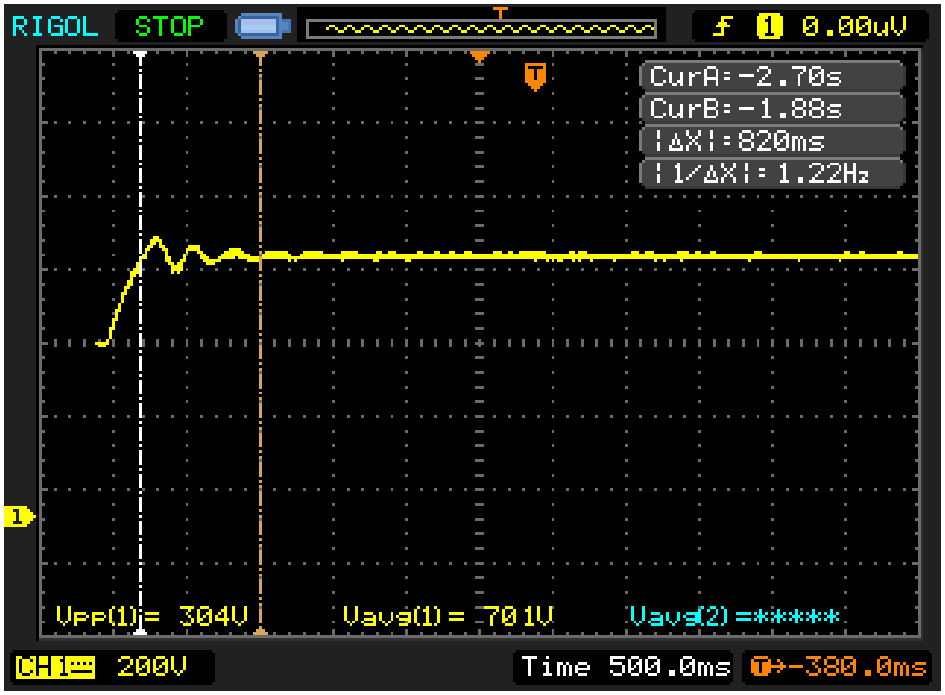


Figure 6.21: DC Link Voltage Transient Response – Settling Time (820 milliseconds)

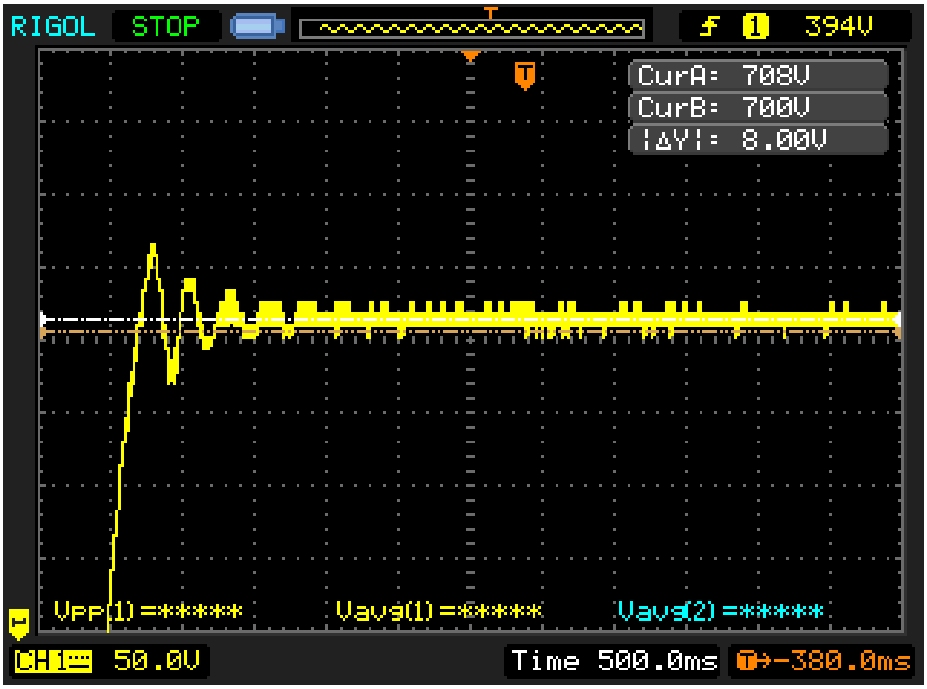


Figure 6.22: DC Link Voltage Transient Response – Steady State Error (1 %)

6.7. Discussions

In Table 6.2, overall system performance obtained by the experimental results is presented.

Table 6.2: Overall System Performance Resulted From the Experimental Work

Rated Efficiency (Motoring)	94 %	Power Factor with PI Controller	≈ 1
TDD of Line Current	6 %	Maximum Overshoot	8.5 %
TDD of Converter-A Current	22 %	Rise Time	0.26 s
TDD of Converter-B Current	21 %	Settling Time	0.82 s
DC Link Voltage Ripple	1 %	Steady State Error	≈1 %

The performance of the designed and simulated PWM rectifier system is validated with the experimental results presented in this chapter. The following items are the results consistent with theoretical expectations and are sufficient to reveal the success of the experimental work performed in this research work:

- The interleaved two-level 4Q PWM rectifier topology is tested successfully at rated conditions. Previously presented control requirements; constant DC link voltage operation and unity power factor operation, are met.
- Phase shifted PWM technique is utilized in success which can be observed by the harmonic spectrum of the line current where the center frequency of the first harmonic group is four times the switching frequency. In addition, reduction on the line current TDD is achieved.
- The peak-to-peak ripple voltage at the DC link is below the specified limits.
- The second harmonic component at the DC link current is filtered successfully by the series LC filter.
- The Input power and output power of the PWM rectifier, obtained from the experimental setup under rated conditions yield overall converter efficiency of 94 % and this result is consistent with not only the theoretical calculations

performed using the technical specifications of the prototype system in Appendix C, but also the simulation work performed for the prototype system. The theoretical loss analysis of the prototype system can be seen in Table 6.4.

- The transient performance of the DC Link is tested with step input, and the resultant performance indices are considered to be acceptable for a transportation load. Further improvement on these parameters can be achieved with the calibration of DC link voltage control loop parameters. The increase of the integral term yields faster response; i.e., lower settling time. On the other hand, the overshoot will get worsen in this case.
- Sharing of the current by the two converters connected in parallel via the DC link is equal and the converter is expected to be able to operate at half of the rated power if one converter fails.

On the other hand, the unforeseen discrepancies emerged from the experimental results can be found below along with their possible reasoning:

- The dips and notches observed on the AC current waveforms are considered to be caused by the noise of the current probes.
- The steady state error seen on the DC link voltage is caused by the sensitivity of the voltage sensors and can be corrected with careful calibration of the sensors with software.
- The low order harmonic present on the line current (2^{nd}, 3^{rd} etc.) may be caused by two things; the presence of these harmonic components on the supply voltage and their reflection to the line current and the low frequency ripple at the DC link voltage which is reflected to the overall control system. This situation is considered to be overcome by using additional band stop filters on the control system.

The comparative analysis of theoretical, simulation and experimental results of the prototype system can be seen in Table 6.3.

Table 6.3. Comparative Analysis of Theoretical, Simulation and Experimental Results of the Prototype System

Result	Theoretical	Simulation	Experimental
TDD of line current	5 %	5.7 %	6 %
TDD of converter-A current	20 %	21.9 %	22 %
TDD of converter-B current	20 %	21.2 %	21 %
Power factor	1	0.998	0.999
DC link peak to peak ripple	0.1 %	0.6 %	1.0 %
Overall efficiency	94.9 %	94.7 %	94.1 %

Table 6.4. Theoretical Loss Analysis of the Prototype System

Loss Type	Loss
Transformer copper loss	124 W
Transformer core loss	38 W
IGBT conduction loss	1 W
IGBT switching loss	11 W
Diode conduction loss	3 W
Diode switching loss	4 W
DC link capacitor ESR loss	1 W
DC link LC filter capacitor ESR loss	1 W
DC link LC filter inductor copper loss	3 W
DC link LC filter inductor core loss	1 W
Total	187 W

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

In this research work, design and low voltage laboratory prototype implementation of an interleaved PWM rectifier for use in main line locomotive traction systems has been carried out.

Various PWM rectifier topologies such as the two-level converter, three-level converter, series connected multilevel converter and interleaved two-level converter have been investigated and compared in terms of several performance indices such as line current harmonic content, converter efficiency, reliability, redundancy etc. Among the rectifier topologies presented in the literature, the voltage source based topology which is composed of single phase two - level H-bridge converters connected with a common DC link, fed by isolated secondary windings of a front-end transformer and controlled with phase shifted SPWM method is selected for its superior harmonic distortion performance, redundancy and power sharing among separate converters which results in the reduction of power semiconductor current ratings.

The rectifier stage of the DC link converter is responsible for maintaining constant DC link voltage at its set value, drawing current from the catenary at unity power factor, synthesizing sinusoidal input currents meeting the harmonic distortion

standards published in IEEE Std. 519-1992 and having dynamic response fast enough against disturbances by not only catenary line but also traction motors.

The developed PWM rectifier system is able to operate at unity power factor and can transfer both active and reactive power in a bidirectional manner. Therefore, the energy generated by the asynchronous traction motors during braking of the vehicle can be fed back directly to the AC grid through the catenary line. The catenary line, rated voltage of which is 25 kV, is allowed to be in the range of 19 kV and 27.5 kV presented by the standard BS EN 50163:2004. The rectifier stage of the traction system can be operated at a desired power factor different from unity and hence can absorb or inject reactive power to the AC grid by which the catenary line voltage can be regulated to its rated value by the main line locomotive.

The operation of the selected PWM rectifier topology in a main line locomotive traction application and its power stage architecture is carefully analyzed and formulated for both motoring and regenerative braking modes of operation. The system utilizes a multi-loop control structure composed of phase locked loop, DC link voltage control loop and AC line current control loop to meet the aforementioned requirements. Control techniques applicable for each loop presented in the literature are studied. Linear current control technique is realized to be the best candidate for its advantages of easy implementation and good transient performance.

The design phase is generally based on the variation of selected performance indices, which have been derived from the system requirements, with system parameters such as PWM switching frequency and passive filters on both AC and DC sides. The system performance is aimed to achieve a line current TDD below 5 %, converter efficiency above 98.5 % and DC link peak to peak ripple voltage below 1.5 %. To do so, effect of each system parameter on these criteria is analyzed by theoretical derivations and computer simulations. The PWM rectifier is modelled as two dependent but distinct plants for control system design. Control system design is based on stability, transient performance and steady state performance design of which is performed by the employment of control design tools on MATLAB.

With simulation work carried out on MATLAB/Simulink environment and SimPowerSystem toolbox, the high power PWM rectifier system design is validated.

Near unity power factor operation in both motoring and regenerative braking modes at rated output power is visualized with constant DC link voltage operation. The interleaved two - level PWM rectifier topology with 500 Hz of switching frequency, 1 mH of line inductance and 5 mF of DC link capacitance is shown to meet the objective performance indices. The doubling of the effective switching frequency and TDD reduction on the primary side current is achieved with desired converter rated efficiency. It is shown that utilization of PI regulators on the current control loop yields a steady state error different than zero and input power factor cannot be kept at unity. It is also observed that this situation can be dealt with the usage of PR regulators and exact unity power factor operation can be achieved. The elimination of the second harmonic component present on the DC link via series connected resonant type LC filter is also shown.

Evaluation of this research by experimental results is performed on the developed low voltage and low power laboratory prototype which is composed of the developed PWM rectifier, AC motor drive unit and a universal machine set which can be considered as a transportation load simulator with its relatively high inertia. PWM rectifier performance is validated with rated power of 3.5 kW. The following conclusions can be drawn within the scope of this research work:

- Interleaving of converters makes redundant operation possible. In other words, the railway vehicle operation is not fully interrupted in case of a failure of one converter on the rectifier stage.
- It is possible to obtain successful efficiency rates with acceptable harmonic content on the line current with the utilization of phase shifted SPWM technique.
- Regulation of AC current linearly with sinusoidal waveform tracking method yields the best dynamic performance. The steady state error of this technique causing power factor rates lower than unity can be eliminated with the employment of PR regulators. However, careful design is required to avoid stability problems occurring due to the resonance nature of this controller.

- Regenerative braking operation at power levels as high as the rated power of motoring mode is possible with the same system performance. Therefore, energy efficient traction systems can be built without the utilization of additional on-board energy storage systems.
- The design and verification of the PWM rectifier for high power locomotive by simulation work have been justified with comparative analysis performed for the low power laboratory prototype system.
- With the utilization of the front-end transformer leakage inductance, additional AC line inductor requirement can be eliminated which contributes to the reduction of system cost, volume and weight.

7.2. Future Work

In the future, this research work can be elevated with the following possible applications:

- Selective Harmonic Elimination Method (SHEM) which is usually employed as a PWM technique in multilevel converter applications can be applied and tested. The technique is based on the calculation of a set of pulse angles corresponding to the absence of selected harmonics to be eliminated by an optimization algorithm. It has been rarely tried on single phase two - level converter applications and never been used in locomotive traction applications. The interleaved connection of two converters can be utilized for the application of a novel method called "Phase Shifted SHEM" and its performance can be compared with the conventional phase shifted SPWM technique.
- As one can notice, the front-end transformer of the traction system has isolated secondary windings number of which depends on the number of DC link converters and the number of H-bridges connected in parallel on one DC link (interleaving). To increase redundancy and decrease the current rating of

power semiconductor modules, the tendency is to employ as many converters as possible. On the other hand, any additional H-bridge corresponds to the need of additional transformer secondary winding. To illustrate, the design performed in this work suggest that the input transformer should have nine isolated windings (eight for the traction converter and one auxiliary winding) which is not common in railway traction manufacturing. A study based on the elimination of the circulating currents between the two H-bridges when they are supplied by a common AC source without an isolating transformer can be carried out by which the total number of converters on the rectifier stage can be increased with the employment of conventional transformer having five secondary winding (four for the traction converter and one auxiliary).

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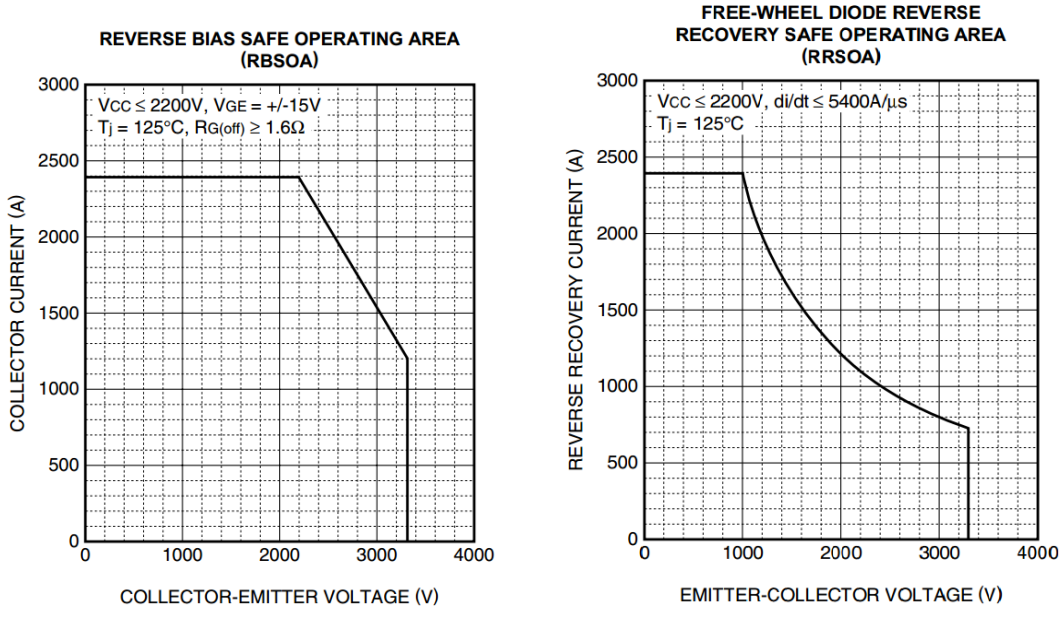
APPENDIX A

IGBT MODULE CHARACTERISTICS

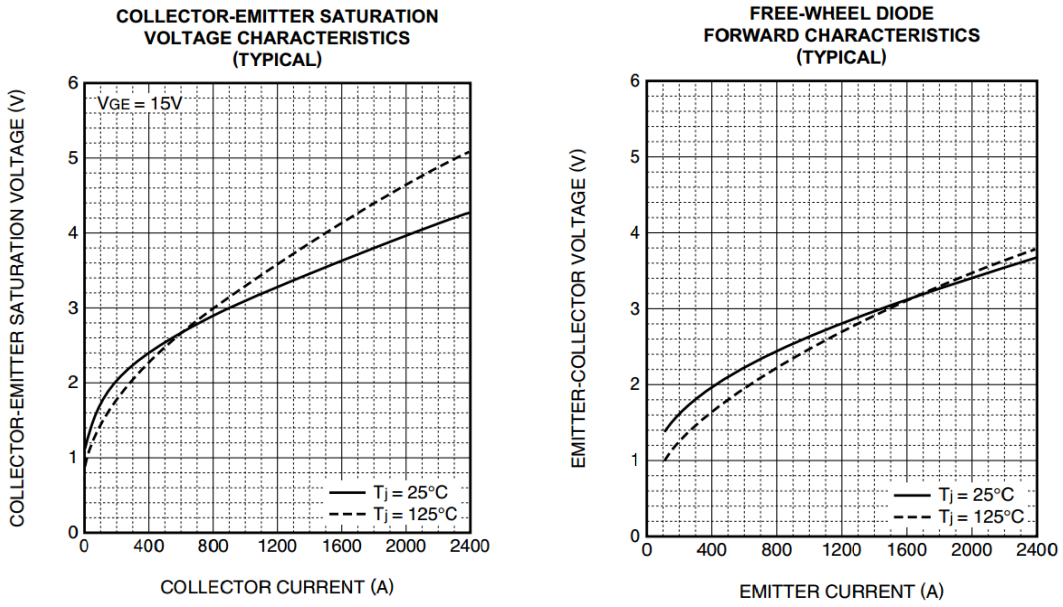
In this section, several characteristics of the selected IGBT module are presented to be used for the verification of voltage and current ratings and calculation power semiconductor losses of the designed PWM rectifier. In Figure A.1, reverse bias safe operating area (RBSOA) and free-wheel diode reverse recovery safe operating area (RRSOA) are presented [111].



(a) (b)

Figure A.1: Safe Operating Areas of the Selected IGBT Module [111]
(a) RBSOA, (b) RRSOA

Collector-Emitter Saturation Voltage vs Collector Current characteristics of the IGBT and Emitter-Collector Voltage vs Emitter Current characteristics of the antiparallel diode which have been used for conduction loss calculation are shown in Figure A.2 [111]. In addition, turn-on, turn-off and reverse recover energies in terms of collector current are shown in Figure A.3 for use in switching loss calculation of the IGBT and reverse recover loss of the diode [111].



(a) (b)

Figure A.2: Saturation Voltage Characteristics of the IGBT Module [111]
(a) V_{CE} vs I_C Characteristics of IGBT, (b) V_{EC} vs I_E Characteristics of Diode

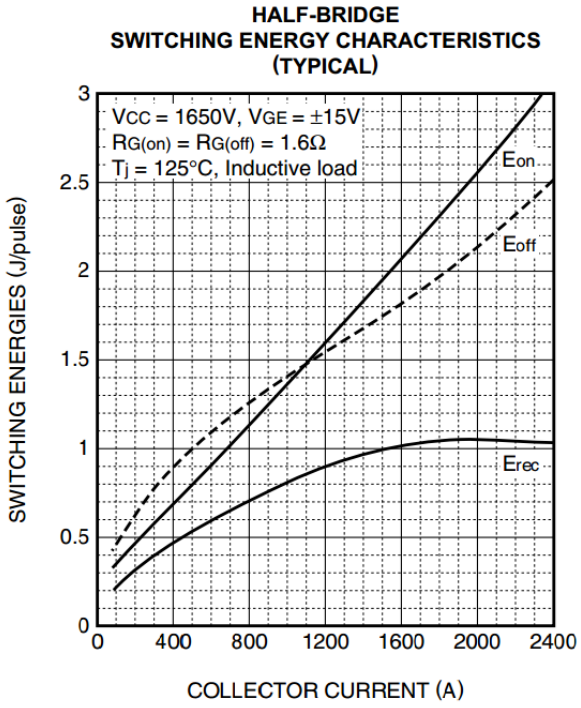


Figure A.3: Switching Energy Characteristics of the IGBT Module [111]

APPENDIX B

SIMULINK SIMULATION MODELS

The models of the simulation work performed on MATLAB/Simulink environment are presented in this section. Model of the overall system is shown in Figure B.1. The system is composed of; catenary model, PWM rectifier power stage, PWM rectifier control block, PWM rectifier modulation block and traction inverter / traction motor models of which are shown in Figures B.2 to B.6.

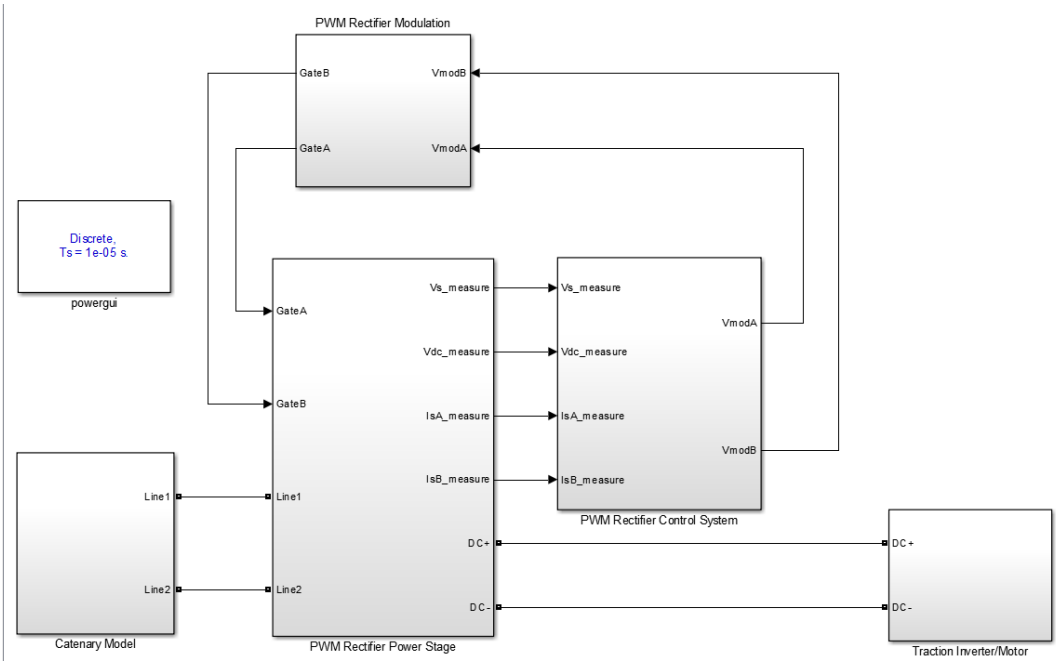


Figure B.1: Simulation Model of the Overall System

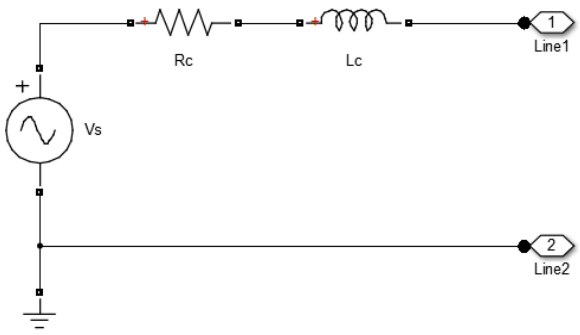


Figure B.2: Simulation Model of the Catenary

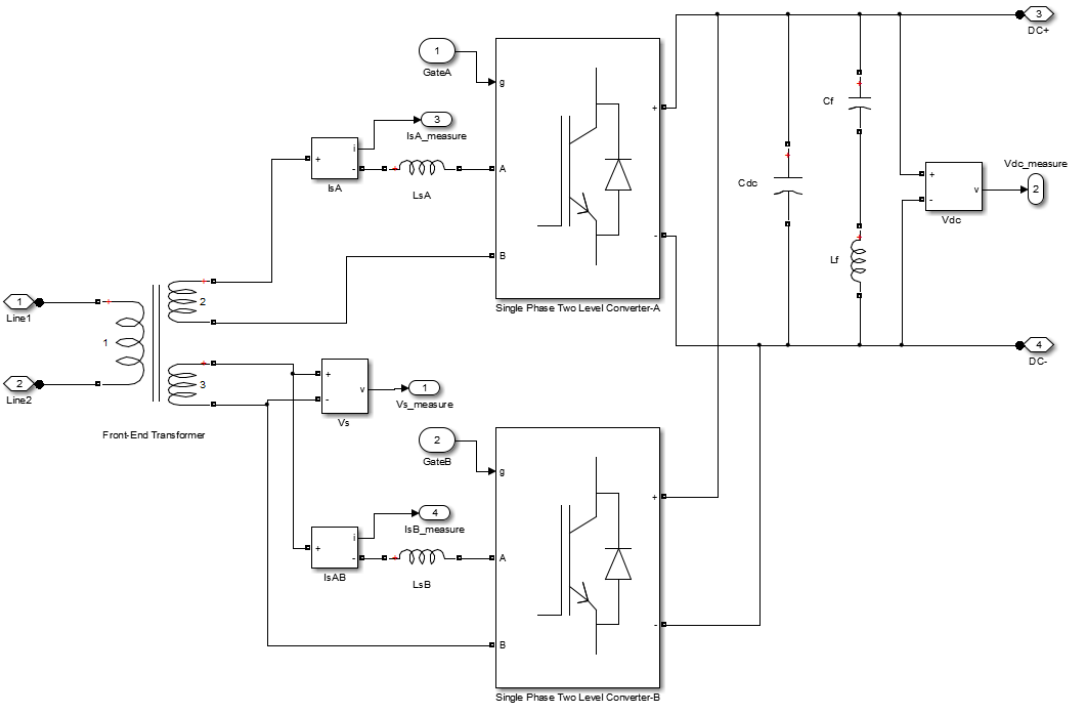


Figure B.3: Simulation Model of the PWM Rectifier Power Stage

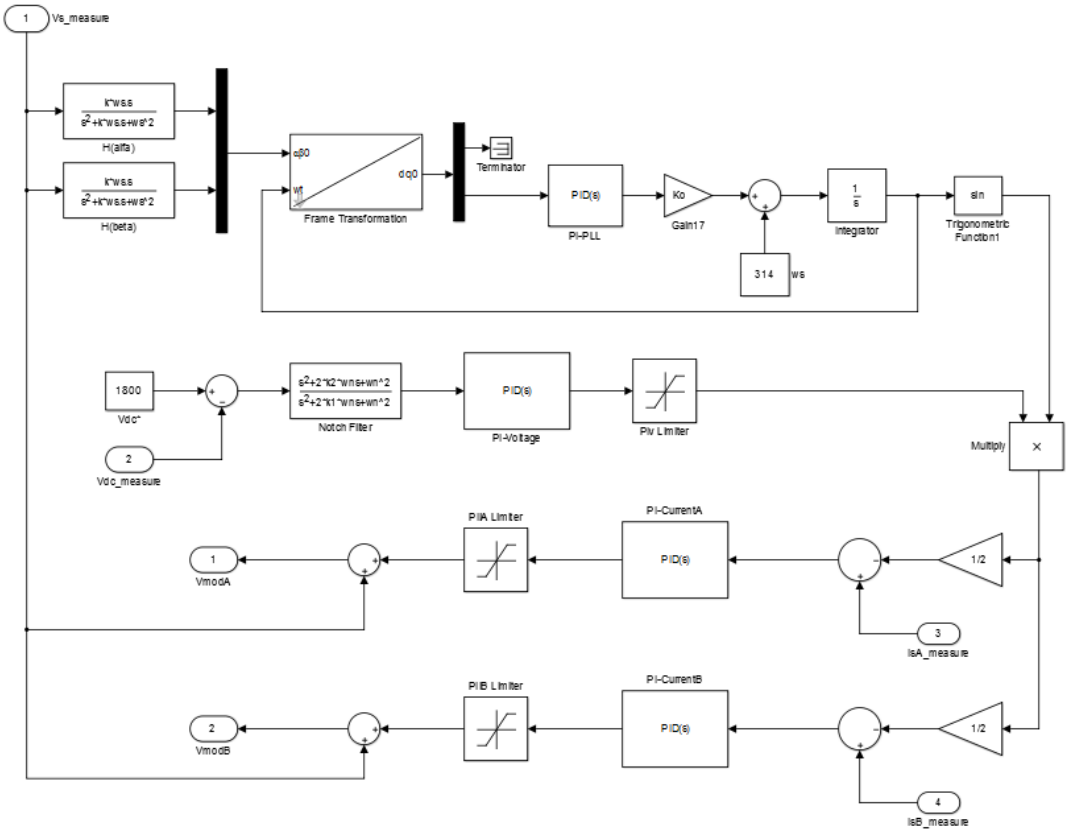


Figure B.4: Simulation Model of the PWM Rectifier Control Block

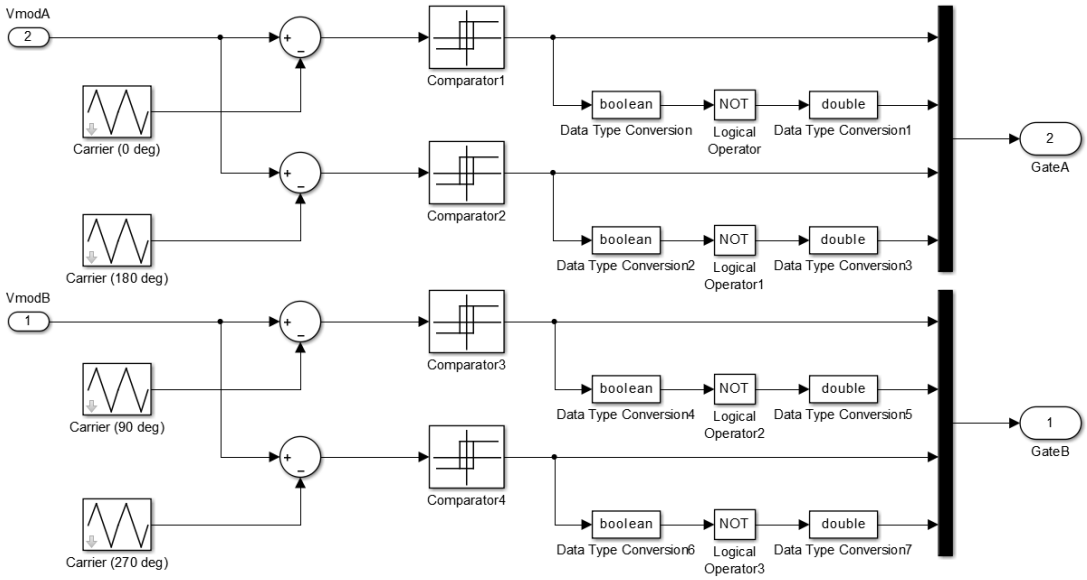


Figure B.5: Simulation Model of the PWM Rectifier Modulation Block

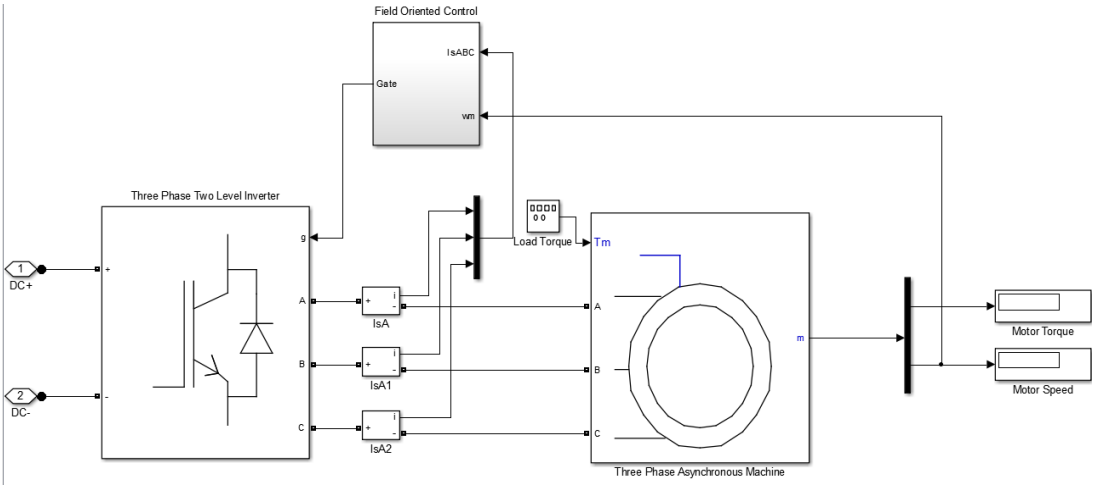


Figure B.6: Simulation Model of the Traction Inverter/Traction Motor

APPENDIX C

TECHNICAL SPECIFICATIONS OF THE DEVELOPED PWM RECTIFIER PROTOYPE SYSTEM

The low voltage PWM rectifier prototype is composed of a front-end transformer with two isolated secondary windings and unity conversion ratio, the power stage with two H-bridges with IGBT modules including heat sinks and gate drive units, DC link capacitor bank, DC link series LC filter and a control board. It should be pointed out that additional series reactors at the AC side of each 4Q converter have not been utilized due to the fact that leakage inductance of the front-end transformer is sufficient enough to meet the harmonic distortion requirements.

Technical specifications of the transformer can be seen in Table C.1. In addition, equivalent circuit parameters of the transformer are shown in Table C.2.

Table C.1: Technical Specifications of the Front-End Transformer

Rated Power	6 kVA	Primary Winding Resistance	0.73 Ω
Rated Primary Voltage	440 V	Secondary Winding Resistance	0.78 Ω
Rated Secondary Voltage	440 V	Open Circuit Loss	35 W
Rated Frequency	50 Hz	Copper Loss	299 W
Conversion Ratio	1:1:1	Rated Efficiency	95 %
Rated Primary Current	13.6 A	Regulation at Unity pf	6.7 %
Rated Secondary Current	6.8 A	Short Circuit Voltage	18 %

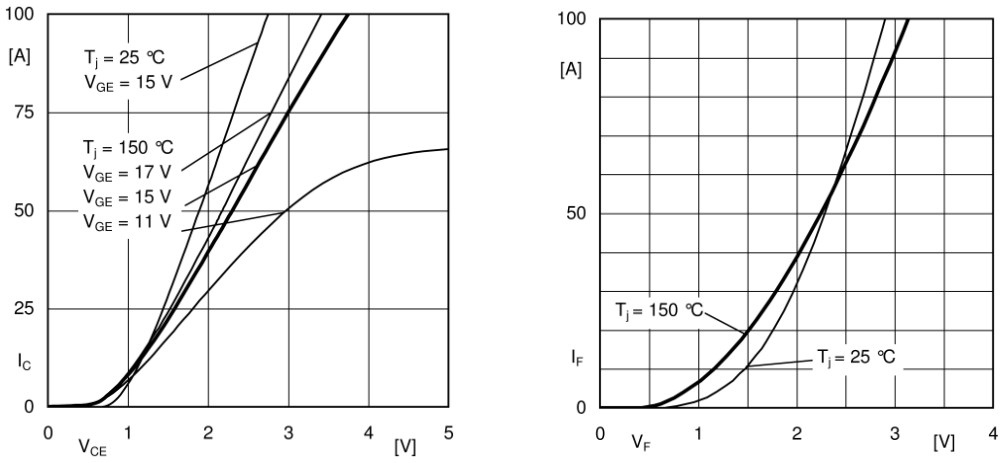
Table C.2: Equivalent Circuit Parameters of the Front-End Transformer

$R_{cu,p}$	0.73 Ω	L_p	19.2 mH
R_c	5.53 kΩ	L_m	1.61 H
$R_{cu,s1}$	0.78 Ω	L_{s1}	18.1 mH
$R_{cu,s2}$	0.78 Ω	L_{s2}	17.8 mH

The power semiconductor device selected for the experimental work of this study is 1200V/50A SKM50GB12T4 IGBT half-bridge modules from Semikron [115]. Technical specifications of the IGBT module are listed in Table C.3. Additionally, collector-emitter voltage vs collector current and emitter-collector voltage vs emitter current characteristics to be used in IGBT and diode conduction loss calculation are shown in Figure C.1 and turn-on, turn-off and reverse recovery energies in terms of collector current are shown in Figure C.2 to be used in IGBT switching loss and diode reverse recover loss calculation [115].

Table C.3: Technical Specifications of the IGBT Module Used in the Low Voltage Prototype [115]

Blocking Voltage (V_{CES})	1200V
Continuous IGBT Current (I_C)	50A
Pulsed IGBT Current (I_{CM})	81A
Continuous Diode Current (I_E)	50A
Pulsed Diode Current (I_{EM})	65A
Saturation Voltage of IGBT ($I_{CE\text{-}sat}$) @50A	1.85V
On State Voltage of Diode (V_{EC}) @1200A	2.22V
Turn-on Delay Time ($t_{d\text{-}on}$)	98 ns
Turn-off Delay Time ($t_{d\text{-}off}$)	325 ns
Turn-on Rise Time (t_r)	29 ns
Turn-off Fall Time (t_f)	75 ns
Turn-on Switching Energy (E_{on})	5.5 mJ
Turn-off Switching Energy (E_{off})	4.5 mJ
Reverse Recovery Energy (E_{rr})	3.8 mJ



(a) (b)

Figure C.1: Saturation Voltage Characteristics of the IGBT Module [115]
(a) V_{CE} vs I_C Characteristics of IGBT, (b) V_F vs I_F Characteristics of Diode

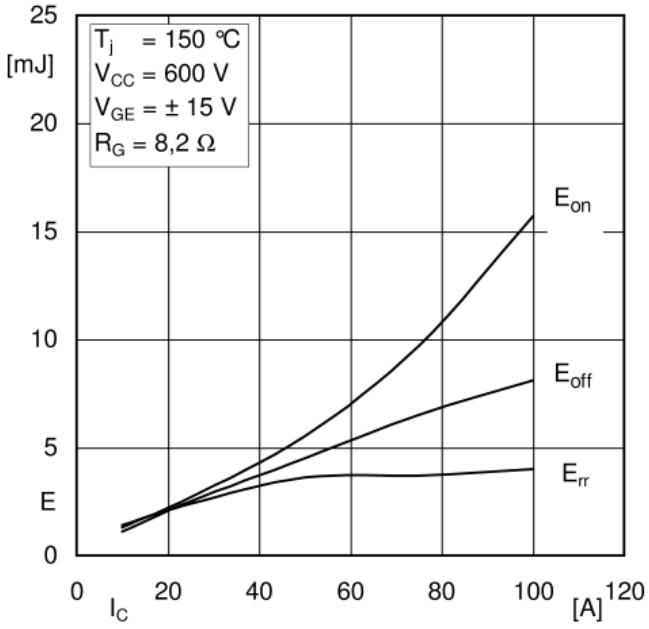


Figure C.2: Switching Energy Characteristics of the IGBT Module [115]

Finally, technical specifications of the series LC filter inductor are shown in Table C.4, series LC filter capacitor in Table C.5 and DC link capacitor bank in Table C.6.

Table C.4: Technical Specifications of the Series LC Filter Inductor Used in the Low Voltage Prototype

Inductance	2.62 mH	Core Type	Ferrite, N87
Rated Current	3.54 A	Core Shape	Double E
Rated Frequency	100 Hz	Peak Flux Density	0.24 T
Turn Number	128	Copper Loss	2.5 W
Air Gap Length	3.3 mm	Core Loss	0.5 W

Table C.5: Technical Specifications of the Series LC Filter Capacitor Bank Used in the Low Voltage Prototype

Capacitor Type	Aluminum Electrolytic
Series Connection	2
Parallel Connection	1
Equivalent Capacitance	0.98 mF
Voltage Rating	800 V
Ripple Current Rating	8 A
Equivalent ESR and ESL	73 mΩ / 20 nH

Table C.6: Technical Specifications of the DC Link Capacitor Bank Used in the Low Voltage Prototype

Capacitor Type	Aluminum Electrolytic
Series Connection	2
Parallel Connection	3
Equivalent Capacitance	4.9 mF
Voltage Rating	800 V
Ripple Current Rating	23.8 A
Equivalent ESR and ESL	29 mΩ / 14 nH

APPENDIX D

IMPLEMENTATION OF THE DIGITAL CONTROL SYSTEM FOR THE LOW VOLTAGE PROTOTYPE

Design of the control system in continuous time has already been introduced in Chapter 4 in detail. For hardware implementation and digital control, the control system is discretized for the real time software implementation using a microcontroller with Digital Signal Processor (DSP) architecture. In this section, discretization of transfer functions (in s domain) in the control loops is presented. Each transfer function obtained in discrete time (z domain) is then converted to a difference equation to be coded as a software macro routine.

Discretization of the PI regulator is shown in (D.1) and (D.2), and the resultant difference equation is shown in (D.3).

$$G(z) = \frac{Y(z)}{E(z)} = K_p + \frac{K_i}{1 - z^{-1}} \tag{D.1}$$

$$Y(z) = Y(z)z^{-1} + E(z)(K_p + K_i) - E(z)z^{-1}K_p \tag{D.2}$$

$$y[n] = y[n-1] + e[n]\left(K_p + K_i\right) - e[n-1]K_p \tag{D.3}$$

Discretization of the PR regulator is shown in (D.4) and (D.5), and the resultant difference equation is shown in (D.6).

$$G(z) = \frac{Y(z)}{E(z)} = K_p + \frac{2K_i w_c - 2K_i w_c z^{-1}}{1 + 2w_c + {w_o}^2 - 2(1 + w_c)z^{-1} + z^{-2}} \tag{D.4}$$

$$\begin{aligned} Y(z) = {} & Y(z)z^{-2}\left(\frac{-1}{1 + 2w_c + {w_o}^2}\right) + Y(z)z^{-1}\left(\frac{2 + 2w_c}{1 + 2w_c + {w_o}^2}\right) + E(z)z^{-2}\left(\frac{K_p}{1 + 2w_c + {w_o}^2}\right) \\ & + E(z)z^{-1}\left(\frac{-2K_p - 2w_c K_p - 2w_c K_i}{1 + 2w_c + {w_o}^2}\right) + E(z)\left(\frac{K_p + 2w_c K_p + 2w_c K_i + {w_o}^2 K_p}{1 + 2w_c + {w_o}^2}\right) \end{aligned} \tag{D.5}$$

$$\begin{aligned} Y[n] = {} & Y[n-2]\left(\frac{-1}{1 + 2w_c + {w_o}^2}\right) + Y[n-1]\left(\frac{2 + 2w_c}{1 + 2w_c + {w_o}^2}\right) + E[n-2]\left(\frac{K_p}{1 + 2w_c + {w_o}^2}\right) \\ & + E[n-1]\left(\frac{-2K_p - 2w_c K_p - 2w_c K_i}{1 + 2w_c + {w_o}^2}\right) + E[n]\left(\frac{K_p + 2w_c K_p + 2w_c K_i + {w_o}^2 K_p}{1 + 2w_c + {w_o}^2}\right) \end{aligned} \tag{D.6}$$

Finally, discretization of the orthogonal signal generator employed in PLL is shown in Equations D.7 to D.10 and the resultant difference equations are shown in Equations D.11 and D.12.

$$G_{beta}(z) = \frac{V_{beta}(z)}{V_s(z)} = \frac{\frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4} - \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-2}}{1 - \frac{2(4 - {w_n}^2{T_s}^2)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-1} - \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-2}} \tag{D.7}$$

$$G_{alfa}(z) = \frac{V_{alfa}(z)}{V_s(z)} = \frac{\frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4} + \frac{4k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-1} + \frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-2}}{1 - \frac{2(4 - {w_n}^2{T_s}^2)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-1} - \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-2}} \tag{D.8}$$

$$\begin{aligned} V_{beta}(z) = {} & \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s(z) + \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-1}V_s(z) \\ & + \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s(z)z^{-2} + \frac{2(4 - {w_n}^2{T_s}^2)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{beta}(z)z^{-1} \\ & + \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{beta}(z)z^{-2} \end{aligned} \tag{D.9}$$

$$\begin{aligned} V_{alfa}(z) = {} & \frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s(z) + \frac{4k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}z^{-1}V_s(z) \\ & + \frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s(z)z^{-2} + \frac{2(4 - {w_n}^2{T_s}^2)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{alfa}(z)z^{-1} \\ & + \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{alfa}(z)z^{-2} \end{aligned} \tag{D.10}$$

$$\begin{aligned} V_{beta}[n] = {} & \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n] + \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n-1] + \frac{2kw_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n \\ & - 2] + \frac{2\left(4 - {w_n}^2{T_s}^2\right)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{beta}[n-1] + \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{beta}[n-2] \end{aligned} \tag{D.11}$$

$$\begin{aligned} V_{alfa}[n] = {} & \frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n] + \frac{4k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n-1] + \frac{2k^2w_nT_s}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_s[n \\ & - 2] + \frac{2\left(4 - {w_n}^2{T_s}^2\right)}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{alfa}[n-1] + \frac{2kw_nT_s - 4 - {w_n}^2{T_s}^2}{2kw_nT_s + {w_n}^2{T_s}^2 + 4}V_{alfa}[n-2] \end{aligned} \tag{D.12}$$

APPENDIX E

FLOWCHARTS OF THE CONTROL SOFTWARE

The control software is implemented on TMS320F28335 Digital Signal Controller from Texas Instruments. The selected controller is composed of 150 MHz Digital Signal Processor.

There are four types of data sampled by the Analogue to Digital Converter (ADC) units which are the supply voltage, input current of each converter and DC link voltage. Two ADC sequencers are used with different timing (start of conversion, SOC interrupt) for control purposes. Sampling rate of ADC Sequencer 1 and Sequencer 2 are 20 kHz and 1 kHz, respectively. Sequencer 1 is synchronized with PLL algorithm where only the supply voltage is sampled (1 channel) and Sequencer 2 is synchronized with the rest of the control loops and all the data are sampled (5 channels) on it. Since PWM frequency (switching frequency) is selected as 1 kHz, main control algorithm is run at the same rate. There is also an additional timer which is the Central Processor Unit (CPU) timer at 10 kHz task of which is informing the watchdog periodically.

PWM operation is achieved with the utilization of Enhanced Pulse Width Modulation (ePWM) module with its own counter period of which is 1 msec. Four ePWM channels are used to drive the eight IGBTs present on the interleaved converters with their dual output ports (ePWMxA and ePWMxB). The ePWM counters corresponding to each converter are arranged with 90 degrees phase shift for phase shifted PWM operation. There is also a dead band of 10 μsec between all the dual ePWM outputs to avoid the short circuit of the DC link if one IGBT fails to turn-off on time.

There are a total of 5 interrupt service routines (ISR) two of which are the two ADC sequencers. Two additional interrupts are synchronized with the counters of ePWM1 and ePWM3 and their purpose is to update the calculated duty cycles in the control loops. All these four interrupts are timed and periodic. The fifth interrupt which serves as the protection module is arranged by the Trip Zone (TZ) module and is not periodic. At each PWM cycle, the sampled data are checked whether they are in the specified permissible range or not. If any of the voltage or current value is out of the range, PWM operation is disabled and no gate signal is formed to protect the power stage equipment from overvoltage, overcurrent etc. This interrupt has the highest priority as expected.

The timing sequence of all the mentioned modules is shown in Figure E.1 based on which the software is implemented. The flowcharts of the main function, interrupts and the main loop are shown in Figure E.2. Moreover, flowcharts of the PLL routine, control loops and protection subroutine are shown in Figure E.3.

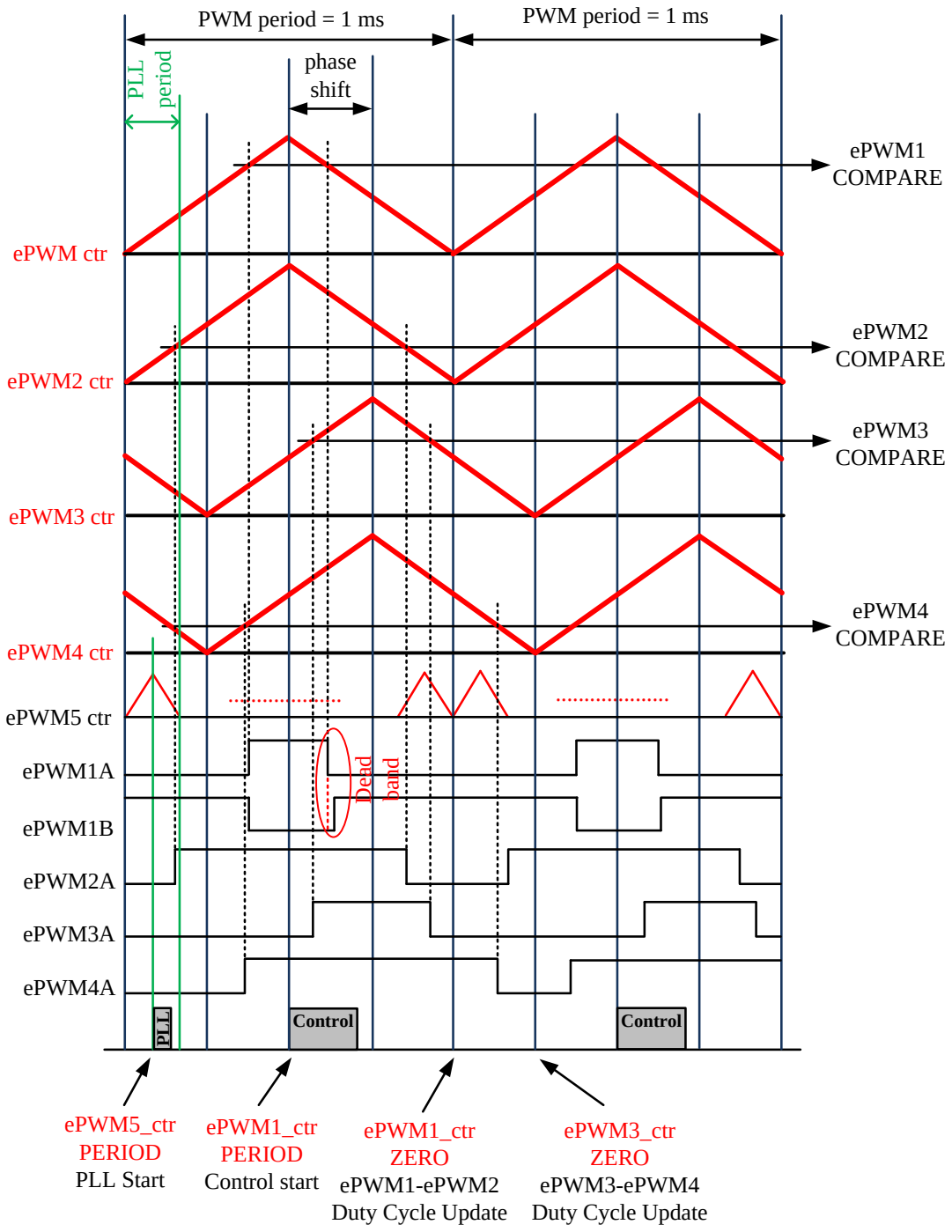


Figure E.1: Timing Sequence of the Software

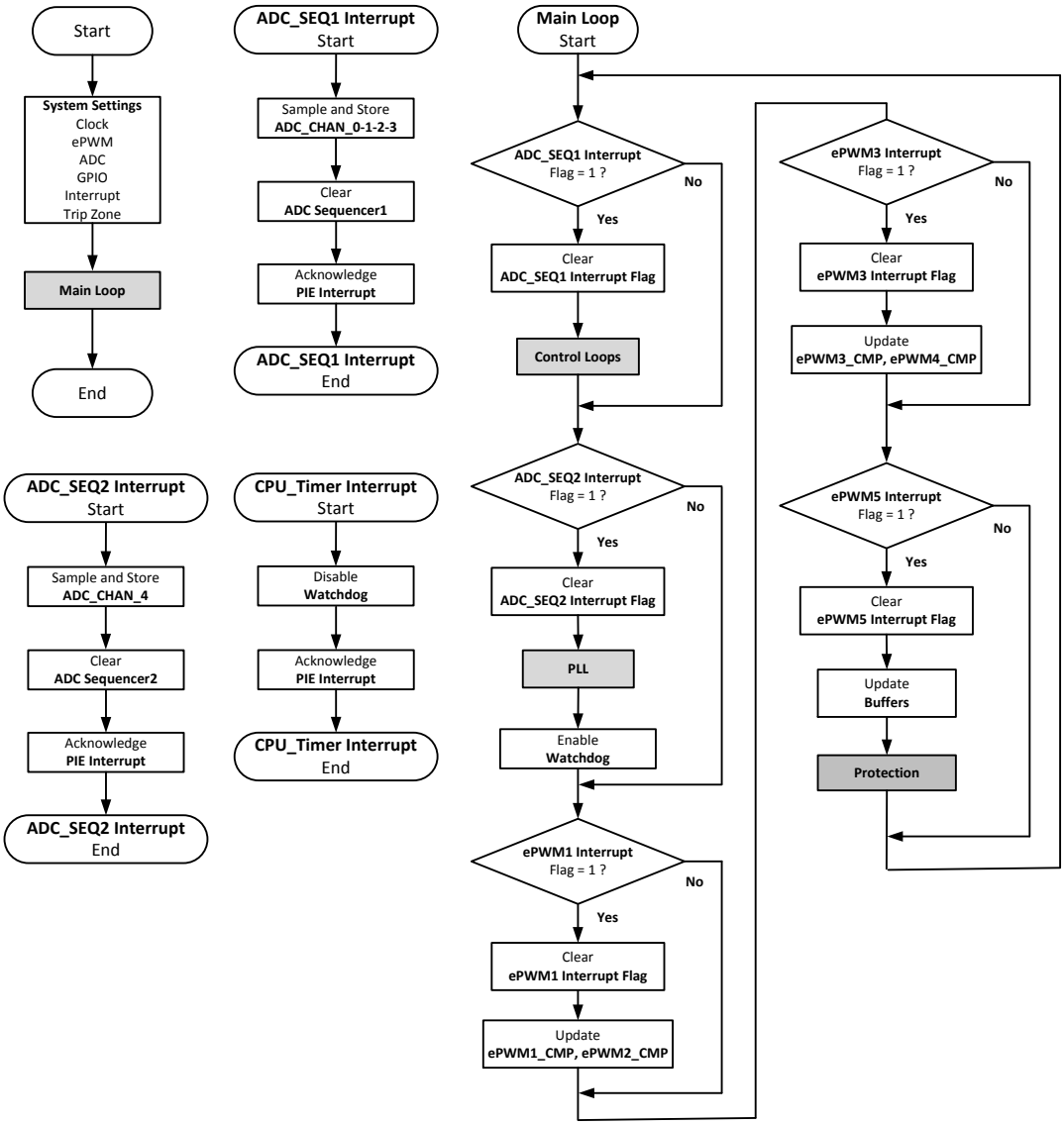


Figure E.2: Software Flowcharts - I

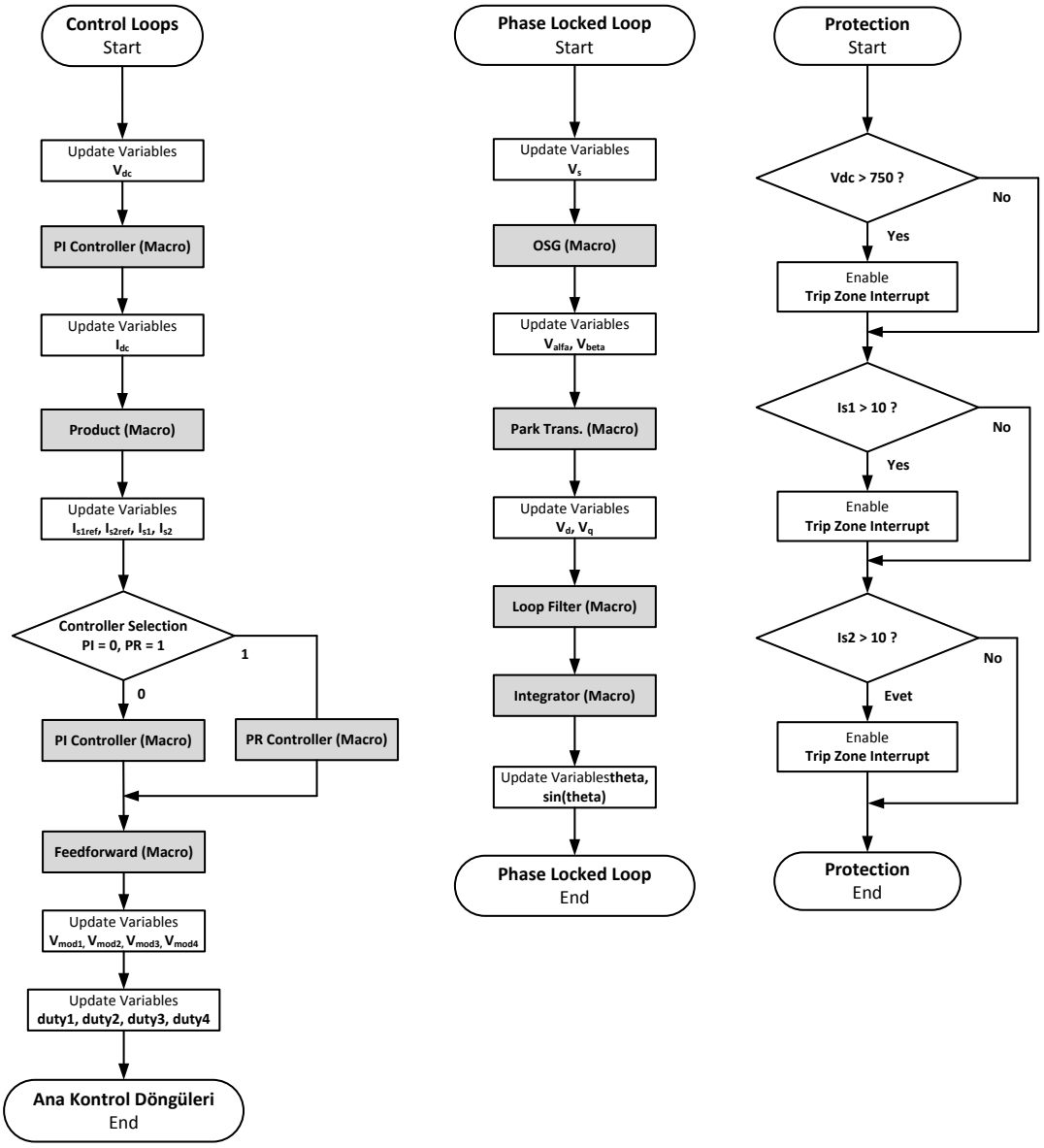


Figure E.3: Software Flowcharts - II

APPENDIX F

PCB SCHEMATİCS AND LAYOUT

The control Printed Circuit Board (PCB) is composed of the following modules:

- Power Supply (+15V, -15V, +5V, -5V, +1.5V, +3.3V)
- Measurement (Supply Voltage, DC Link Voltage, Line Current, Converter-A Input Current, Converter-B Input Current)
- Protection (Overvoltage, Overcurrent)
- Gate Drive
- DSP Experimenter Kit (TMS320F28335)

PCB schematics are shown in Figures F.1 to F.7 and layout is shown in Figure F.8.

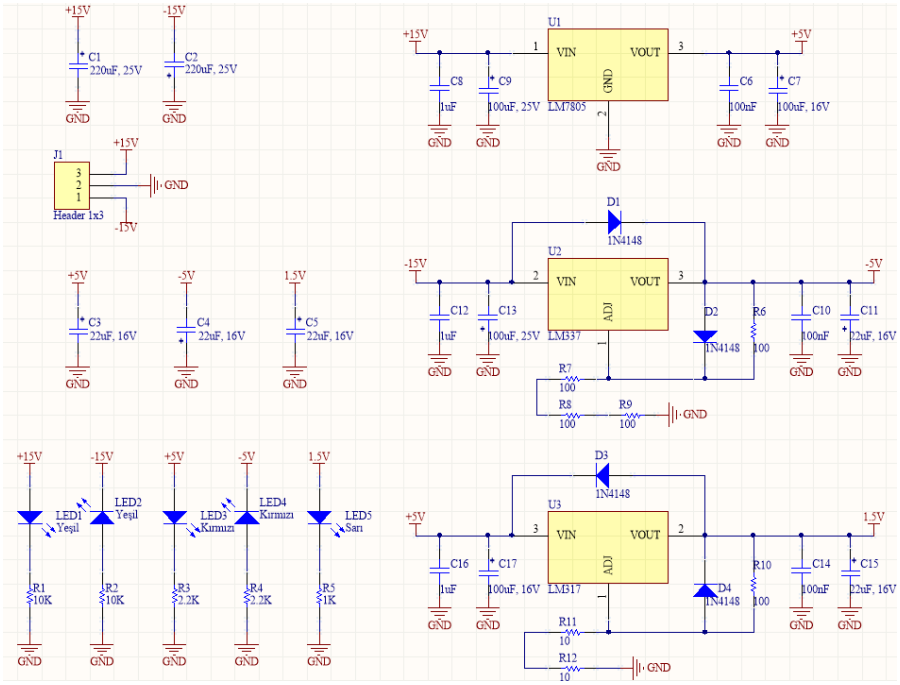


Figure F.1: PCB Schematic I (Power Supply)

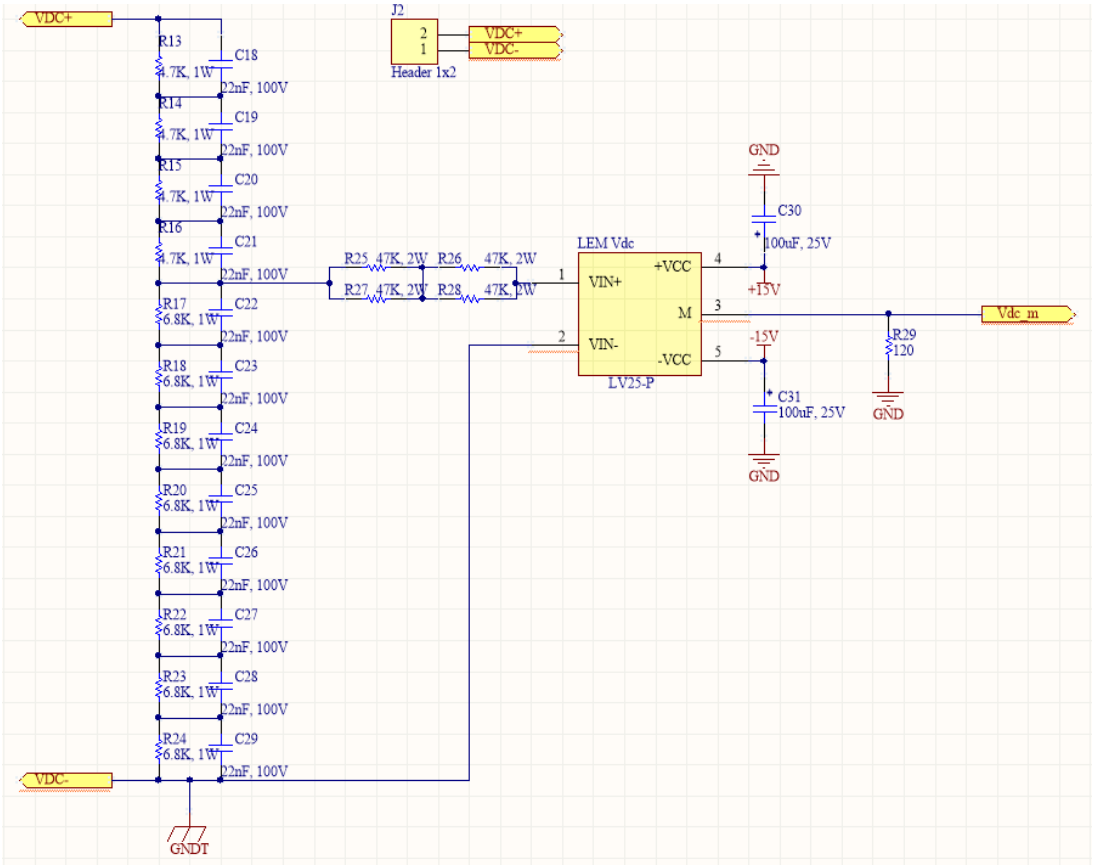


Figure F.2: PCB Schematic II (DC Link Voltage Measurement)

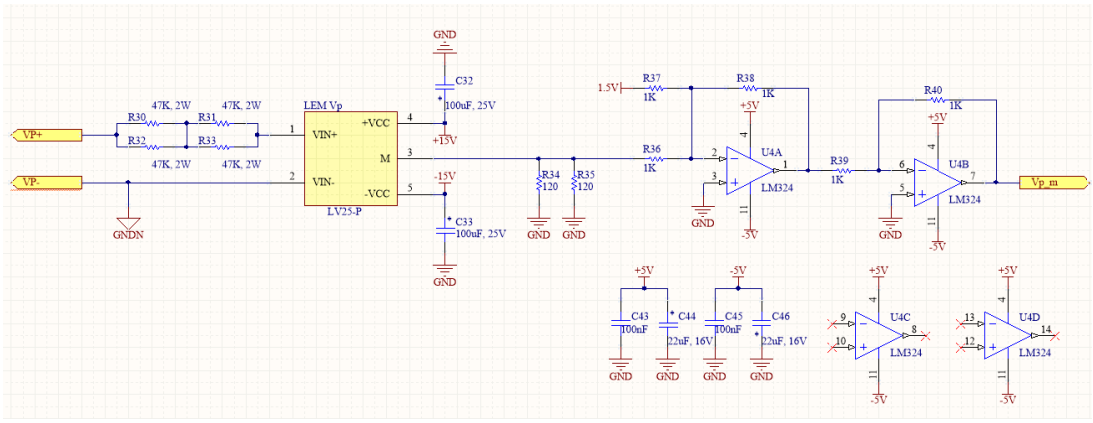


Figure F.3: PCB Schematic III (Supply Voltage Measurement)

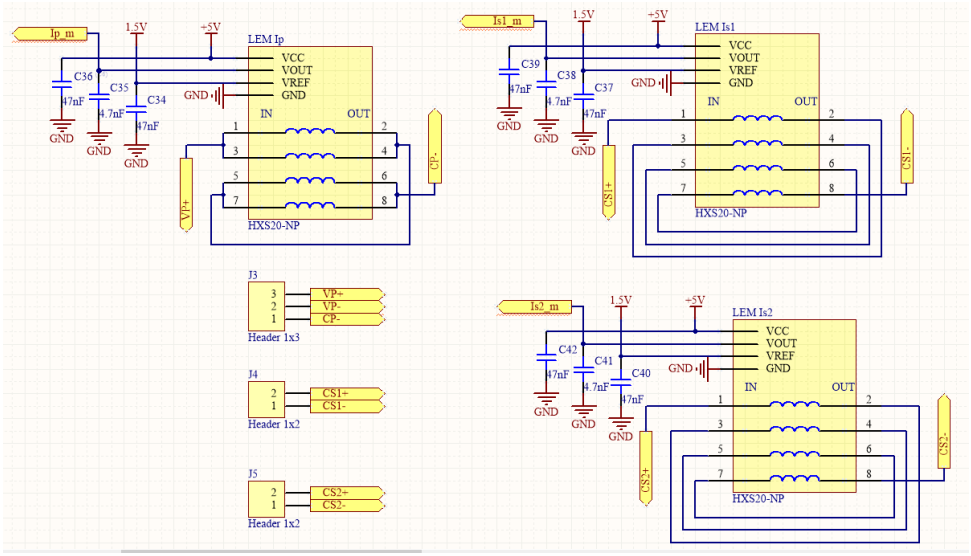


Figure F.4: PCB Schematic IV (Current Measurements)

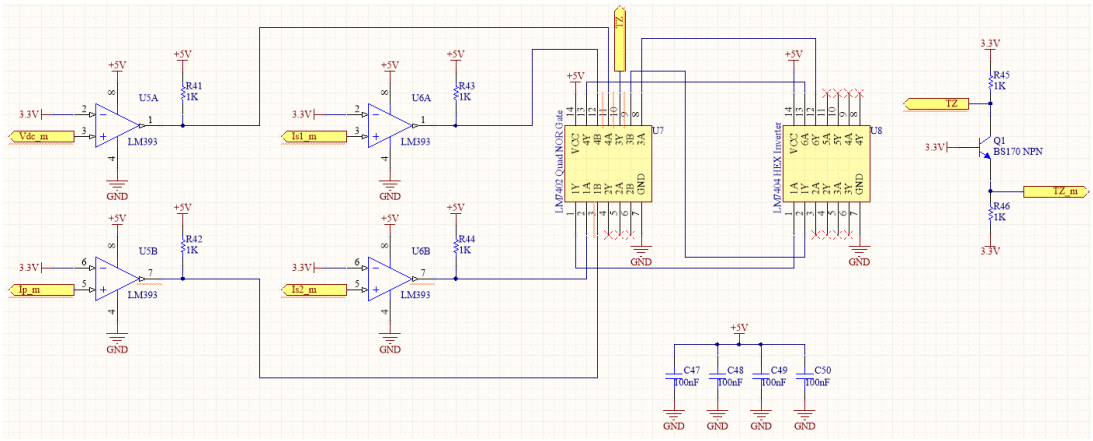


Figure F.5: PCB Schematic V (Trip Zone Protection)

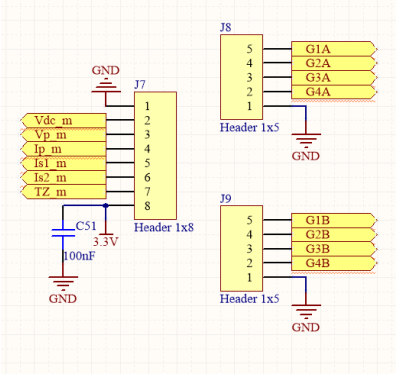


Figure F.6: PCB Schematic VI (DSP Interface)

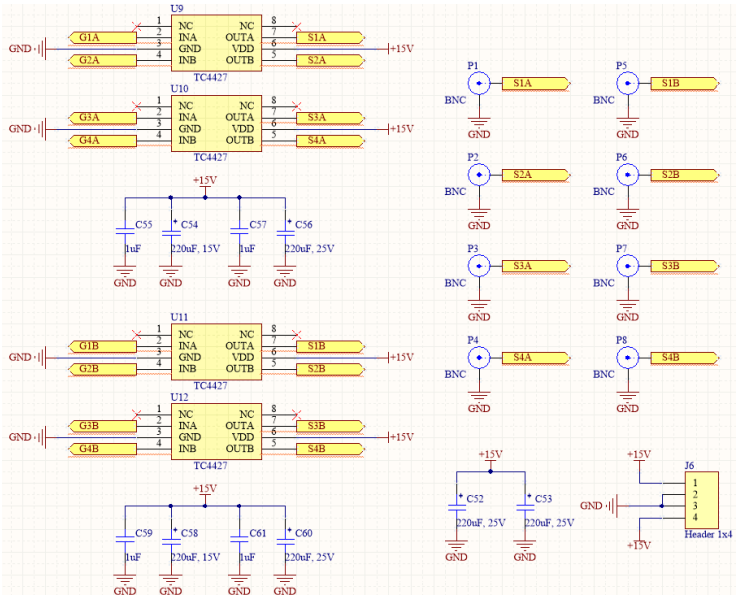


Figure F.7: PCB Schematic VII (Gate Drive)

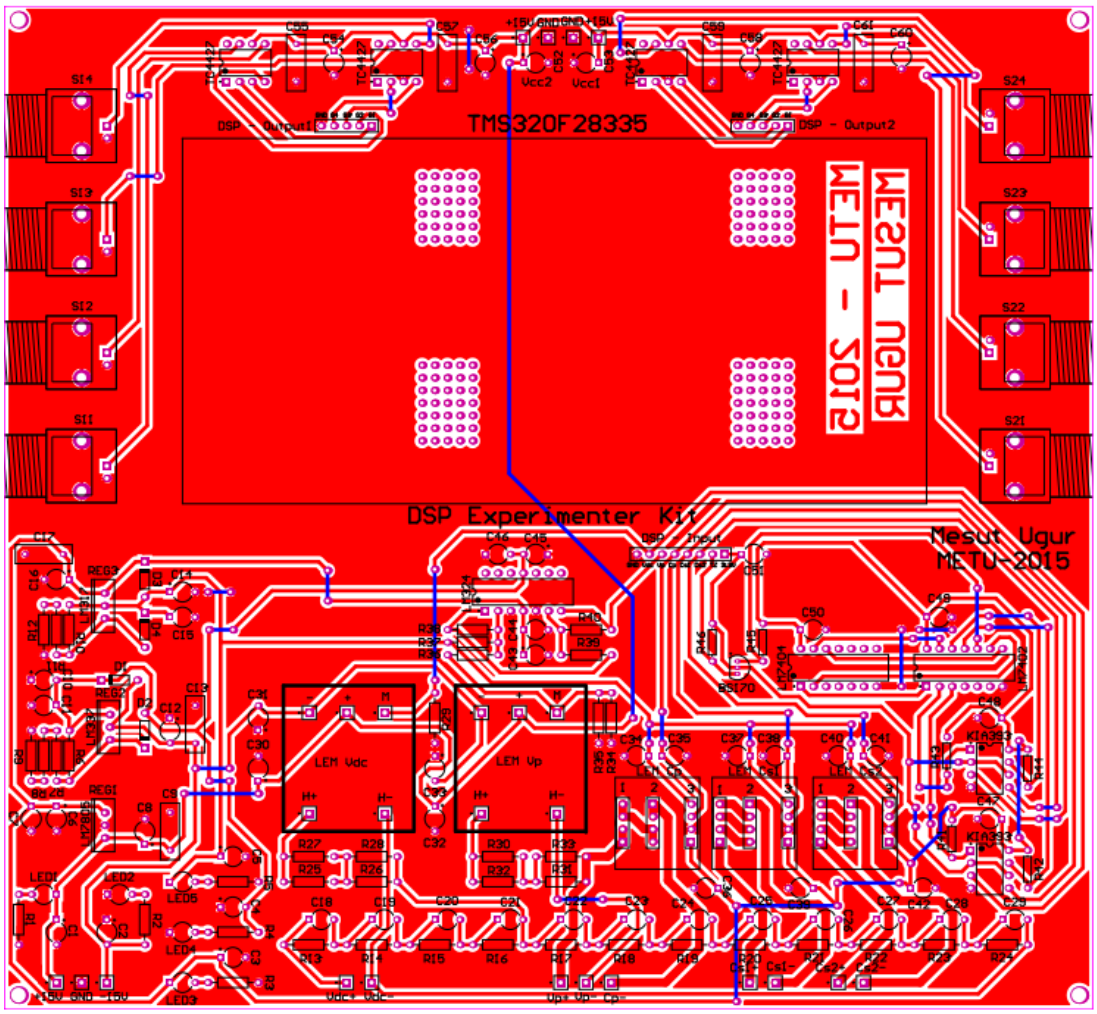


Figure F.8: PCB Layout

APPENDIX G

COMPONENT LIST OF THE LOW VOLTAGE PROTOTYPE

Single phase transformer with two isolated secondary windings

IGBT H-Bridge (2 items)

- 1200V, 50A IGBT modules with antiparallel diode
- IGBT gate drive units

Control Board

- HXS20-NP 20A LEM Current Transducer (3 items)
- LV25-P 500V LEM Voltage Transducer (2 items)
- TMS320F28335 DSP
- Voltage Regulator (3 items)
- OPAMP (5 items)
- TC4427 MOSFET drive IC (4 items)
- Capacitors and Resistors

DC Link Capacitor - Alum. Elect., 400V, 6.3 mF (6 items)

DC Link Series LC Filter Capacitor - Alum. Elect., 400V, 2.2 mF (2 items)

DC Link Series LC Filter Inductor – Ferrite Double E Core, 2.3 mH

Universal Machine Set

- Three Phase Asynchronous Machine (3.5 kW, 400V, 50 Hz)
- DC Machine (3.5 kW, 230V)
- Torque & Speed Transducer
- Flywheel

Control Techniques AC Motor Driver

APPENDIX H

LABORATORY EQUIPMENT USED FOR THE TESTS

Extech MultiPro 530A Multimeter

Tenma 0-30V 3AX2 Power Supply

Tektronix P5122 200MHz 1000V High Voltage Probe

Fluke 62 MAX+ IR Thermometer

HIOKI 3184 Digital Power HI Wattmeter

Fluke 80i 110s AC/DC Current Probe

Passive Voltage Probe

Rigol DS1052E 50MHz Digital Oscilloscope

LeCroy 324 200MHz Digital Oscilloscope

VARSAN 13.5kVA Three Phase Variac

240V 20A Bulky Rheostat

13.5kW Resistive Load Bank