STRUCTURING OF SURFACE FOR LIGHT MANAGEMENT IN MONOCRYSTALLINE Si SOLAR CELLS

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ABSTRACT

STRUCTURING OF SURFACE FOR LIGHT MANAGEMENT IN MONOCRYSTALLINE Si SOLAR CELLS

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Texturing of a silicon wafer is the first process of production of screen printed solar cells to reduce the reflection losses by producing pyramids on the surface of the silicon wafer. Being a cheap and time efficient process, texturing is used in all industrial applications. For mono-crystalline silicon wafers, the process is carried out by using an alkaline solution which consists of potassium hydroxide (KOH), isopropyl alcohol (IPA) and de-ionized water (DI-water) which is heated to 75- 80^{o}C, and wafers are put in it up to a certain time to get random pyramids on the surface. These pyramids reduce the reflection and increase light trapping, and thus increase the efficiency.

In this study, the magnetic agitation was used to optimize the process parameters like, the concentrations of KOH and IPA, process temperature, and process time. To minimize the process duration and process temperature, ultrasonic agitation was used, and almost uniformly distributed small pyramids (3 μm in average) were obtained. To observe the surface characteristics, reflection

measurements and SEM images were taken. Then, the simulations of uniformly textured wafers with textured one side and two sides were made to observe the absorption ability with different thicknesses and different pyramid heights. Then, solar cells were fabricated by using new process parameters and agitation.

To characterize the solar cells, reflection, external quantum efficiency (EQE), current-voltage (I-V), and Suns-Voc measurements were carried out. It was observed that cells based on wafers textured with new parameters and ultrasonic agitation could be used to reach higher conversion efficiency values compared to reference cells.

Key Words: *Texturing, KOH- IPA Solution, Ultrasonic and Magnetic Agitation, Pyramids*

ÖZ

TEK KRİSTAL YAPILI SİLİSYUM GÜNEŞ HÜCRELERİNDEKİ PUL YÜZEYİNİN IŞIK YÖNETİMİ İÇİN ŞEKİLLENDİRİLMESİ

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Ağustos 2015, 108 sayfa

Yüzey şekillendirilmesi silikon pul üzerinde piramitler oluşturarak yansıma kayıplarını azaltan güneş pili üretim aşamalarının birincisidir. Ucuz ve zaman tasarruflu olması, yüzey şekillendirilmesi işlemini tüm endüstride kullanılır yapmıştır. Tek kristal yapılı silikon pullar için bu işlem potasyum hidroksit (KOH), izopropil alkol (IPA) ve iyonize su alkalin karışımının 75- 80^{o}C ısıtılması ve pulların yüzeyinde rastgele piramit oluşturmak için belli bir süre bu karışıma konulması ile gerçekleştirilir. Bu piramitler yansımayı azaltır ve ışık hapsetmeyi, bu da verimliliği arttırır.

Bu çalışmada, manyetik karıştırıcı kullanılarak KOH ve IPA konsantrasyonu, işlem ısısı ve işlem süresi gibi işlem parametreleri eniyileştirildi. Bundan sonra, işlem süresi ve işlem sıcaklığını azaltmak için ultrasonik karıştırıcı kullanıldı ve hemen hemen homojen bir biçimde küçük piramitler (ortalama 3 μm) elde edildi. Yüzey karakteristiğini incelemek için yansıma ölçümü ve SEM görüntüleri alındı.

Sonra, tek taraflı ve çift taraflı düzenli dağılmış piramitlere sahip pulların simülasyonu, bu pulların soğurma kabiliyeti farklı kalınlıklarda ve farklı piramit boyutlarında gözlemlemek için yapıldı. Yeni işlem parametreleri ile güneş hücreleri üretildi.

Bu güneş hücrelerini karakterize etmek için yansıma, EQE, akım voltaj, Suns-Voc ölçümleri yapıldı. Yeni parametrelerle ve ultrasonik karıştırma ile yüzeyleri şekillendirilen pullardan üretilen hücrelerin referans olarak üretilen hücreden daha yüksek verime sahip olduğu gözlemlendi.

Anahtar Kelimeler: *Yüzey şekillendirilmesi, KOH-IPA solüsyonu, Ultrasonik ve Manyetik Karıştırma, Piramitler*

To My Dearest Family

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CHAPTER 1

INTRODUCTION

Energy is vital for human beings. The sources of energy, which are used mostly today, are coal, natural gas, and petroleum. But these sources are limited (i.e. not renewable), and they pollute air, water, and soil. These problems are forcing people to find new energy sources. Some new energy sources such as solar, wind, water, nuclear energy etc. have already been in use of people. However, some of these sources suffer from problems such as high cost, limited availability, geological difficulties, and environmental disturbances. For example, for a hydroelectrical power application, there must be rivers and waterfalls available. In addition, in all such power stains the natural environment is somewhat disturbed. Among the new sources, solar energy is the most promising and most available energy source in the world. Power coming from the Sun is about 174 petawatts (1 PW=10^{15} watts) and 51% of it is absorbed by oceans and land. In other words 89 PW can be used as an energy source [1]. When converted to other energy types such as electricity, the solar energy has the potential to provide all energy demand of the human being on our planet. This conversion can be done in two ways: it can be converted to heat by concentration and then used to generate steam for power generating turbines, or one can use photovoltaic (PV) solar cells which convert the solar power to electricity directly. The former one is called Solar Thermal Electricity (STE) which is outside the scope of this study. The latter is the most widely used technology for the solar energy conversion today. With the recent price reductions and improvements in the performance, the PV industry has grown very rapidly in all around the world. At the end of 2014, the total installed PV capacity exceeded 200 GWp, which is a significant value proving the potential of PV technology in energy supply. Solar cells which are the basic building elements of PV power applications comprises several

different technologies such as crystalline Si (c-Si, mono and multi), thin film systems (a-Si, CdTe and CIGS). Among them c-Si wafer based cells are the most commonly used solar cells in PV industry. Figure 1 compares the share of different technologies in PV market today. From the technology and performance point of view, we see enormous development in recent years. The conversion efficiency, which is the major performance parameter for solar cells, has been improved with intensive research and development activities. For wafers based Silicon (Si) solar cells, efficiency of the cell has reached 26% which is very close to the upper theoretical limit for these types of cells [2].

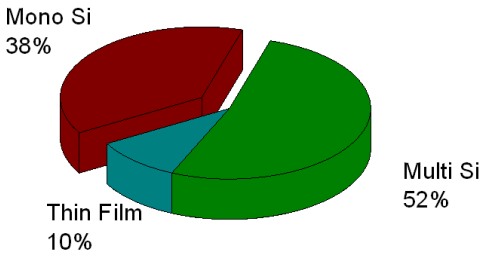


Figure 1: Percentage of different types of PV cells production in 2013 [2]

The cost of the generated electricity is a very important issue for choosing the solar energy instead of the fossil fuels. To decrease cost per watt of solar cells, either the cell efficiency should be increased or the cost of production should be reduced. We observe R&D activities in both directions in many different locations around the world. New device architecture and approaches are being designed and implemented towards lower cost of energy generation [2]. Optimizations of the current production steps and improving them have also been investigated intensively.

In this thesis, we focus on the texturization process of mono-crystal Si wafers, which is the first step of producing a c-Si solar cell. The aim of texturization is to create three dimensional structures on the surface of the wafer to reduce the reflection, and thus improve the absorption of the solar radiation. However, forming the best structure on a Si wafer surface with minimum material loss is still an issue

which needs to be addressed. By a proper optimization, one can obtain best absorbing condition with minimum material loss. The aim of the study is to develop a methodology to decrease the amount of removed Si, the temperature of solution, the amount of chemical used for etching, and finally to obtain the lowest reflection from the surface.

1.1 History of Photovoltaic Technology

Alexandre-Edmond Becquerel, a French physicist, discovered the photovoltaic effect in 1839. Figure 2 shows his setup [3]. Two platinum (Pt) electrodes were put in an acidic solution containing silver bromide AgBr or silver chloride AgCl which are light sensitive material. When these light sensitive materials are illuminated, they decompose into their ions, such as Ag^{+} and Cl^{-} ions, which are then collected by the electrodes leading to electric current flow in the outside circuitry.

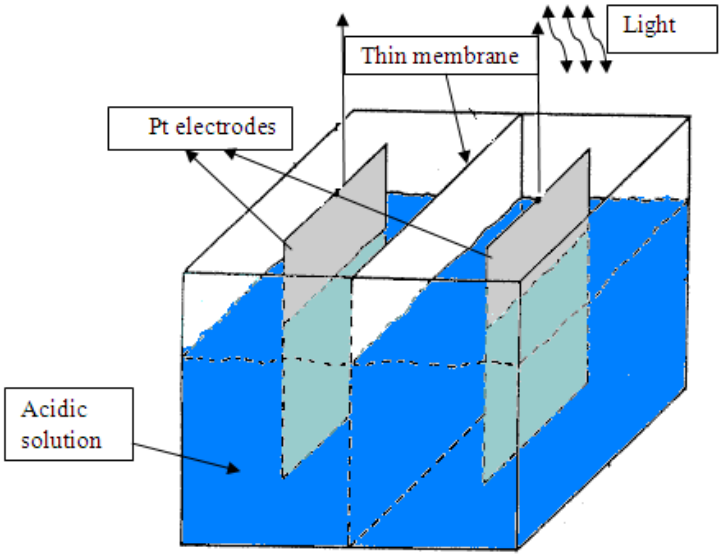


Figure 2: Becquerel experimental setup to show the photovoltaic effect [3]

In 1876, by using solid selenium contacted with platinum, Adams and Day observed photovoltaic effect. Then, Chapin, Fuller and Pearson used Si to produce solar cell with an efficiency of 6% in Bell Laboratories in 1954 [4]. This was the first

reported solar cell produced using Si. During the development of Si solar cells, some theoretical approaches were put forward. In 1961, the efficiency of Si solar cell being a maximum point of 33% was found by William Shockley and Hans Queisser [5]. After that point, the development steps of production a Si solar cell can be sorted as;

- In 1974, an etch solution consisting of sodium hydroxide (NaOH) was used to texture the silicon surface, and the reflection losses due to a flat surface was reduced [6].
- In 1975, instead of using expensive vacuum metallization to produce front Silver (Ag) and back Aluminum (Al) contacts, Ralph et al. used the screen printing method used for the first time [6]. They produced antireflection coatings by using titanium oxide and silicon dioxide. Their produced silicon solar cells became the standard cell with the efficiency of about 10% in the 1970s [6].
- In 1984, silicon nitride (SiN_x) was used as an antireflective coating by Kimura [6].
- In 2006, 86% of wafer based solar cells were produced using screen printing to form Ag front and Al back contacts, and chemical vapor deposition was used to deposit SiNx as the antireflection coating on the front surface [6].

Today, the most commonly used metallization method in PV industry is the screen printing method to produce Si solar cells, due to the low cost and practical applications [7]. About 19% efficiencies have been obtained in industrial production by improving the screen printing solar cells up to now.

There are three reasons why the Si solar cells are dominant in photovoltaic industry. One of them is that Si is the second most abundant element in the Earth. Second one is the electrical properties of Si. The electrical properties of Si are; a) electron hole pairs can be generated under radiation, and b)Si can conduct these electrons and/or holes, and this conductivity can be modified by introducing atoms of other elements [6]. The last one is that Si has been used and studied for more than 40 years in semiconductor industry.

1.2 Types of Solar Cells

1.2.1 c-Si Wafer Based Solar Cells

Wafer based solar cells have 90% share of photovoltaic market today [2]. There are two types of wafers which are used to produce this type of solar cells. One of them is the mono-crystalline silicon wafer. The entire wafer is in a single crystal form edge to edge for mono-crystalline Si wafer. The other one is multi-crystalline wafer which consists of different crystalline domains with different crystal orientation. As can be seen from the Figure 3, one can easily distinguish which one is mono or multi-crystalline solar cell.

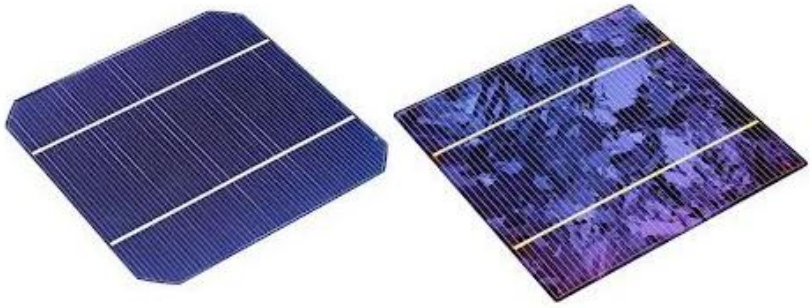


Figure 3: Right is multi-crystalline solar cell. Left is mono-crystalline solar cell

Although mono-crystalline solar cells have higher efficiencies (about 24% in lab environment), multi-crystalline solar cells, which have efficiency about 21% in lab environment, are dominant in photovoltaic market [2]. The reason of this situation is that multi-crystalline solar cells have lower production cost than mono-crystalline solar cells have.

1.2.2 Thin Film Solar Cells

Thin film solar cells are produced by using a chemical or physical process to deposit the active material on substrate. The substrate can be glass or another flexible material as shown in Figure 4 [8]. The major thin film materials are Amorphous Si

(a-Si), Cupper Indium Gallium (di) Selenide (CIGS) and Cadmium Telluride (CdTe) [9].

Figure 4: CIGS solar cells on flexible substrate [8]

By using a few micron thick material, very high absorption can be achieved. This ability provides less material consumption during production of thin film solar cells. But thin film solar cells have lower efficiency values compared to Si, and in addition sunlight can spoil their forms and make them instable. These problems make thin film solar cells less popular in photovoltaic technology when compared with c-Si solar cell technology.

1.2.3 Other Solar Cell Types

Dye sensitized solar cells (DSSCs), tandem solar cells and organic solar cells are examples of some other solar cell types. These new approaches are aiming to reach low cost and/or high efficiency through non-vacuum production techniques, or tandem structures trying to exceed the Shockley-Queisser limit. For DSSC and organic cells, efficiencies as high as 10-11% have been demonstrated [10]. For tandem cells, efficiencies up to 46 % have been achieved [2].

In tandem solar cells, III-V semiconductors like InAs, GaAs, InP are used and they have the ability of absorbing different regions of solar radiation at different layers of solar cells. This results in efficiencies up to 30.8% under 1 sun illumination [11]. Due to the high production cost, tandem solar cells are used with systems to

concentrate the sun light to obtain high efficiency (about 40%) from small areas [2]. This is called Concentrated Photovoltaics (CPV).

For organic solar cells and DSSCs, their production cost is cheap, but they have lowest efficiencies when compared with the others. Although they have low efficiencies, their applications make them attractive. Organic solar cells can be applied on large flexible substrates by a process based on roll to roll production technique [12]. DSSC can be used as transparent solar cells over windows enabling a more aesthetic and large surface integration in Building Integrated Photovoltaic (BIPV) applications [13]. These cell types also suffer from the efficiency degradation with time.

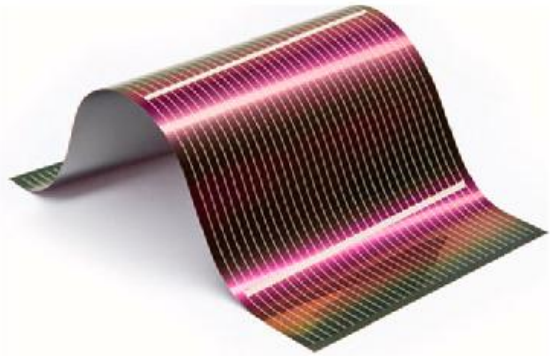


Figure 5: Organic Solar Cell [14]

1.3 Basic Concepts of Photovoltaic Science and Technology

1.3.1 Solar Irradiation

The sun generates huge amount of energy which is about 63 MW/m^2 at its surface. At just outside the Earth atmosphere, this energy is measured as 1360 W/m^2 which is very small quantity compared to the energy at sun's surface [15]. Due to the atmosphere consisting water vapor, dust particles, gas molecules (carbon dioxide, ozone), parts of the solar radiation passing through it is absorbed, reflected or scattered. This leads to the solar intensity spectrum on the Earth's as shown in Figure 6.

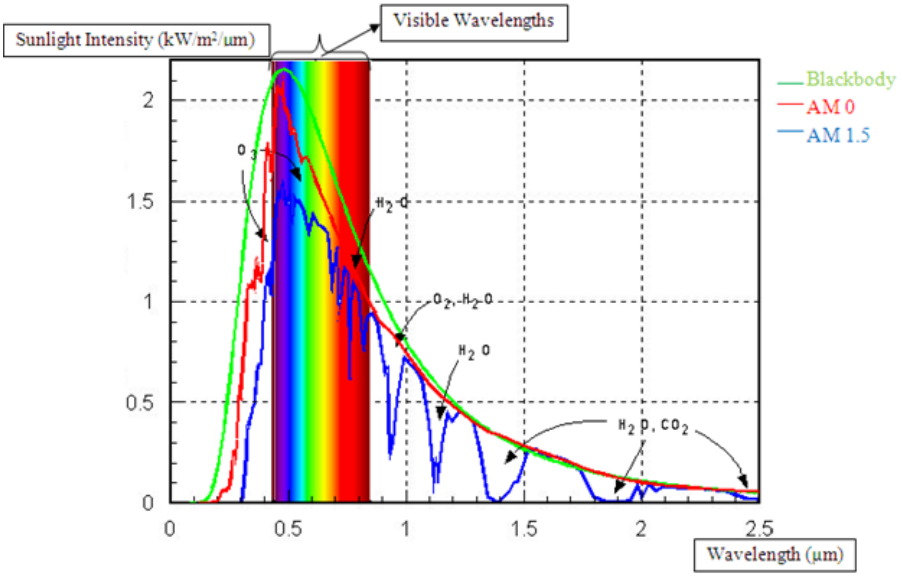


Figure 6: Solar Radiation Spectrum[3]

The Air Mass (A.M.) is defined as the ratio of path length of solar radiation through the atmosphere to the shortest possible path length [3]. It is defined as;

$$\text{Air Mass (A.M.)} = 1/\cos(\varphi) \qquad (1)$$

Where φ is called zenith angle which is the angle between the sun and its vertical axis.

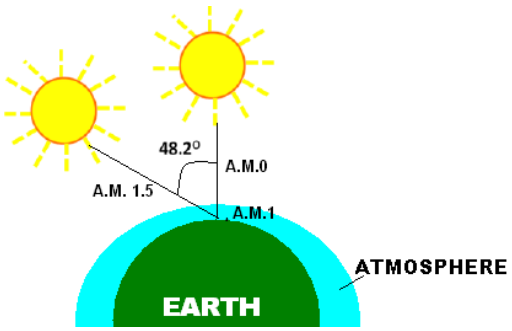


Figure 7: The path length in units of Air Mass, changes with the zenith angle

Figure 7 shows A.M. 0, A.M. 1 and A.M. 1.5. A.M. 0 refers to the spectrum just outside the atmosphere i.e. "zero atmosphere". This quantity is used to characterize solar cells which are used for space power applications. A.M. 1 refers to the spectrum when the sun is at the vertical direction and A.M. 1.5 refers to the spectrum when the sun makes an angle 48.2^{o} with respect to the normal. Solar cells used for commercial applications are characterized with respect to A.M. 1.5. This optical path length results in a power of approximately 1000 W/m^2 which is defined as "1 SUN".

1.3.2 Basics of Solar Cell Operations

A solar cell is a device which is produced by combining p-type and n-type semiconductors like diodes. Its current-voltage characteristics are similar to diodes in dark condition. This characteristic can be expressed by the following formula in dark;

$$I = I_0(e^{\frac{qV}{nkT}} - 1) \tag{2}$$

In the equation, I_0 is reverse saturation current, q is electron charge, V is voltage applied between the terminals of the cell, k is Boltzmann constant, T is the cell temperature in Kelvin, and n is ideality factor which is 1 for ideal case. Under illumination, I_{op}, which is the optically generated current, term is subtracted from the Equation 2 and the equation becomes;

$$I = I_0\left(e^{\frac{qV}{nkT}} - 1\right) - I_{\mathrm{op}} \tag{3}$$

The Figure 8 shows I-V curve for a solar cell under dark and illumination condition.

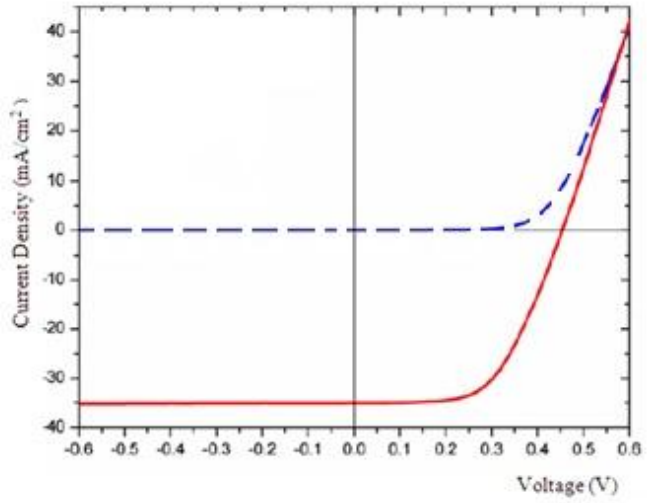


Figure 8: I-V curve of a Solar Cell. Blue dash line is under dark, and red solid line is under illumination [16]

To get the conventional I-V curve of solar cell, red curve is mirrored about horizontal axis and the 1st quadrant is taken.

Short Circuit Current (I_{sc})

The short circuit current is defined as the point which I-V curve intersects the I-axis. In other words, I_{sc} is obtained when the applied voltage between the terminals of solar cell is zero or equal. From the Equation 3, one can easily say that I_{sc} equal to I_{op}. This is the maximum current which can be generated by a solar cell.

Open Circuit Voltage (V_{oc})

The open circuit voltage is defined as the point which I-V curve intersects the V-axis. In other words, the net flowing current through the solar cell is zero. From Equation 3, V_{oc} is the maximum voltage which is generated by a solar cell and can be obtained as;

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{I_{op}}{I_0} + 1\right) \tag{4}$$

The Figure 9 illustrates the typical I-V curve of a solar cell.

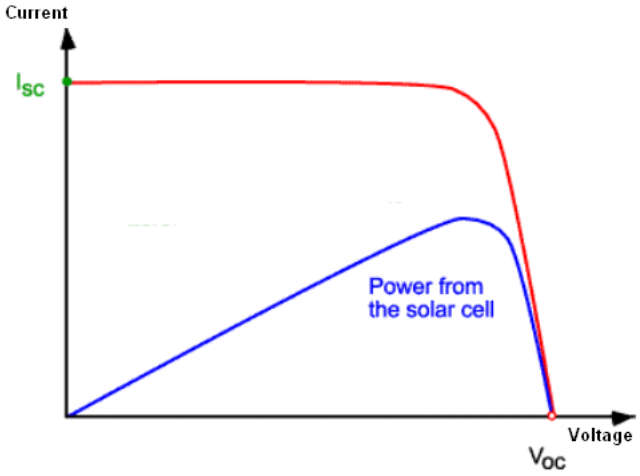


Figure 9: Typical I-V curve of a solar cell

Shunt Resistance (R_{sh})

Shunt resistance is one of the main reasons of the power loss in solar cells. It is mainly due to easy current channels due to the defects across the junction region. When R_{sh} is low, the generated current follows these current channels leading to recombination, and thus reduction of the open circuit voltage across (V_{oc}) the solar cell. This causes a reduction in the generated power. This situation is illustrated in the following figures; Figure 10 and Figure 11.

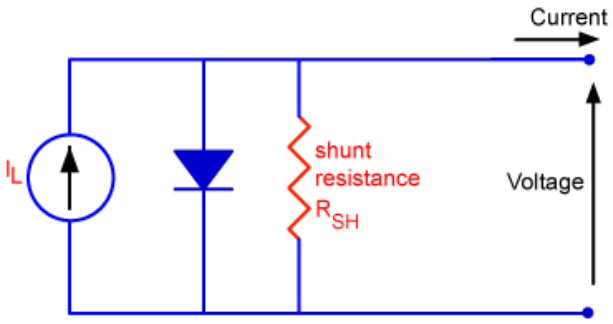


Figure 10: Circuit diagram of a solar cell including the shunt resistance [3]

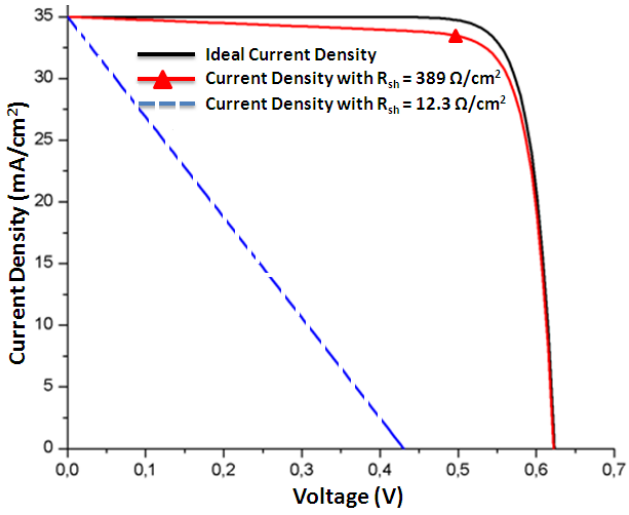


Figure 11: Variation of I-V curve with respect to shunt resistance R_{sh}. For ideal case R_{sh}=10 kΩ cm^2 [3]

One can understand from the Figures that to get high power from a solar cell R_{sh} should be as high as possible. Shunt resistance can be expressed as [3];

$$R_{sh} = \left(\frac{1}{\frac{dI}{dV}}\right) \quad \text{at V} = 0 \tag{5}$$

which is easily determined from the slope of the I-V at V=0.

Series Resistance (R_s)

There are three main factors which form the series resistance for a solar cell namely: the movement of current through the emitter and base of the solar cell, the contact resistance between the metal contact and the silicon, and the resistance of the top and rear metal contacts [17]. As the R_s increases, the fill factor decreases, and I_{sc} also decreases for higher values of R_s as shown in the Figure 12.

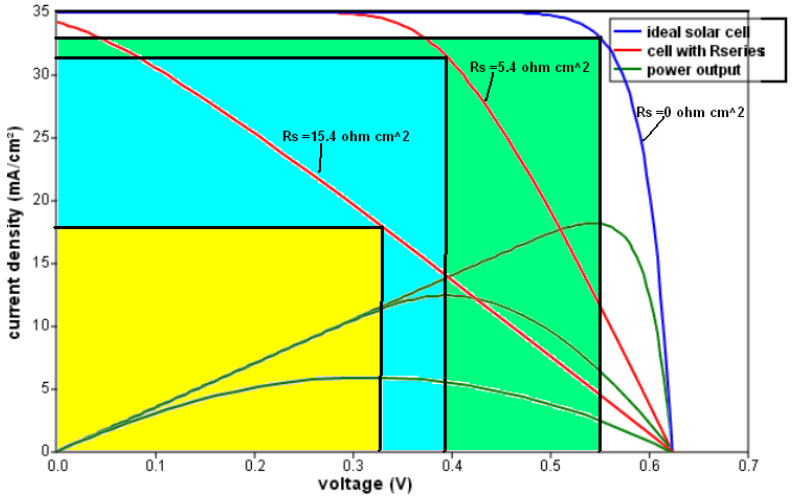


Figure 12: Variation of I-V curve with respect to series resistance R_s [3]

For ideal case, the series resistance I should be zero. The series resistance can be expressed as [3];

$$R_s = \left(\frac{1}{\frac{dI}{dV}}\right) \quad \text{at V} = V_{oc} \tag{6}$$

The series resistance is calculated from the slope of the I-V curve at V = V_{oc}.

Fill Factor (FF)

Fill factor is the ratio of maximum power to the product of short circuit current and open circuit voltage. The voltage at maximum power is shown as V_{mp}, and the current at maximum power is shown as I_{mp}. The fill factor is defined as;

$$\text{FF} = \frac{I_{mp}\text{x } V_{\text{mp}}}{I_{\text{sc}} \text{ x V}_{\text{oc}}} \tag{7}$$

The fill factor is also defined as the ratio of the area A to area B as shown in the Figure 13.

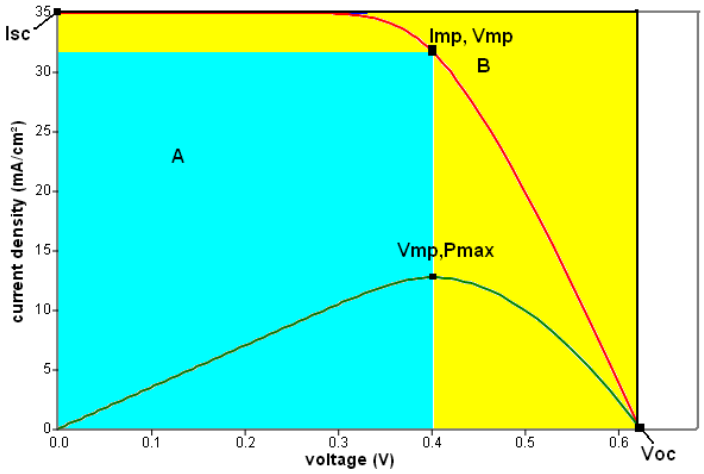


Figure 13: I-V curve of a solar cell with R_s=5.1 ohm cm^2 [3]

Conversion Efficiency

The efficiency of a solar cell is defined as the ratio of the maximum output power which is maximum power as shown in Figure 13 to the input power, and it is commonly used parameter to identify which cell is better than the other. The efficiency is expressed as;

$$\eta = \frac{P_{max}}{P_{in}} = \frac{I_{mp} \mathrm{x}\, V_{\mathrm{mp}}}{P_{in}} = \frac{I_{\mathrm{sc}}\ \mathrm{x}\, \mathrm{V_{oc}}}{P_{in}} \mathrm{FF} \qquad (8)$$

Here to define P_{in}, under which condition the efficiency is measured must be considered. For commercial solar cell, A.M. 1.5 conditions are used. For this condition, P_{in} is defined as the area of the solar cell multiplied by 1kW/m^2. This value is equal to 24.3 W for a 156 × 156 mm^2 cell.

Quantum Efficiency (Q.E.)

Quantum efficiency is the ratio of the number of collected carriers by the solar cell to the number of photons for a given energy incident on the solar cell [18].

If all incoming photons at a certain wavelength is absorbed, and all the generated minority carriers are collected, the quantum efficiency at that wavelength will be 1 as shown in the Figure 14.

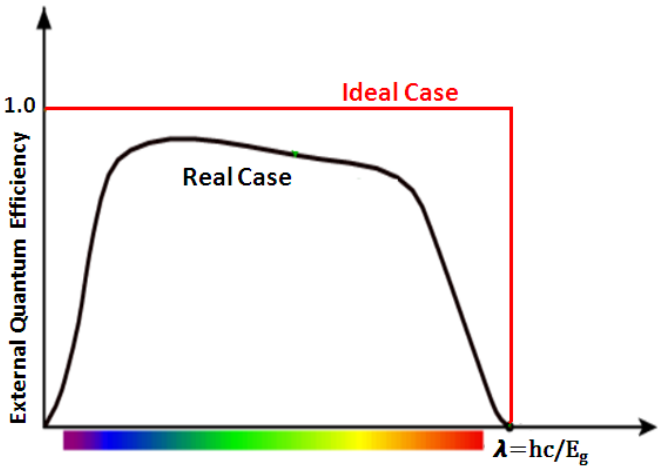


Figure 14: Quantum Efficiency of a solar cell [3]

Recombination effects are responsible for the reduction in quantum efficiency of a solar cell. For example blue light is absorbed near the surface, and if the front surface passivation is not good, the quantum efficiency is reduced about these wavelengths as shown in Figure 14. For silicon, silicon is transparent below 1.12 eV which is the energy band gap of silicon and quantum efficiency is zero for wavelengths beyond 1107 nm.

Spectral Response

Spectral response (S.R.) is a parameter which is the ratio of the current generated by the solar cell to the power incident on the solar cell [3]. It is expressed as;

$$Spectral\ Response\ \left(\frac{A}{W}\right) = \frac{q\lambda}{hc}\mathrm{QE} = \frac{QE}{\lambda(\mu m)}1.2398 \qquad (9)$$

CHAPTER 2

FUNDAMENTALS OF CRYSTALLINE SILICON SOLAR CELL TECHNOLOGY

2.1 Introduction

Screen printing method is the most commonly used method to produce silicon based solar cells by solar cell industry. The production steps are shown in Figure 15.

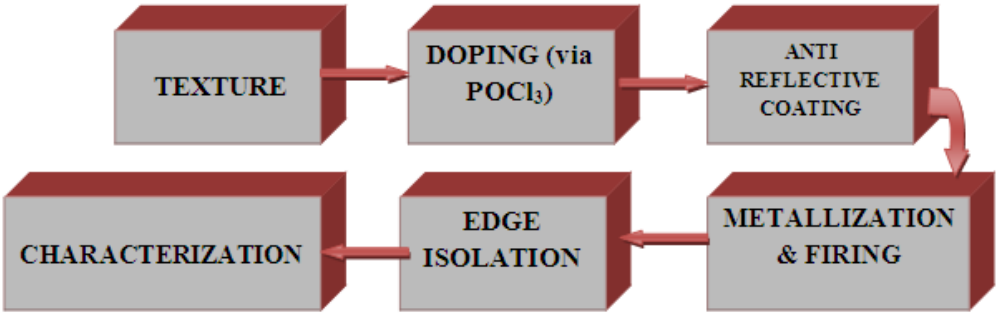


Figure 15 : The production steps of screen printed crystal silicon solar cell

Texturing is the first step of the production steps to form upright pyramids on a Si-wafer, then a doping process is used to obtain p-n junction, after that an anti-reflective coating which is a thin film of SiN_x is made to passivate the emitter and reduce the reflection. Then the screen printing method is used to deposit front and back contacts, and electrical contacts between the Si wafer and the pastes are established by a firing process. Finally, edge isolation is made to isolate the front from the back side of the wafer, and characterization of the solar cell is conducted. Figure 16 shows the structure of such a solar cell [6].

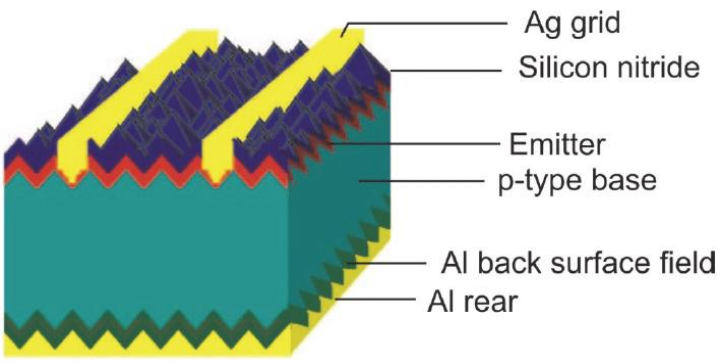


Figure 16: The structure of a screen printed solar cell [6]

2.2 Texture: Wet Chemical Texture

Texturing of a silicon wafer is the first process of production of screen printed solar cells to reduce the reflection losses by producing pyramids on the surface of the silicon wafer. The process is carried out by using an alkaline solution which consists of potassium hydroxide (KOH) or sodium hydroxide (NaOH), isopropyl alcohol (IPA) and de-ionized water (DI-water) which is heated to 75-80^{o}C, and wafers are put in it up to a certain time. This solution is known as KOH-IPA solution in the photovoltaic industry.

The anisotropy of the etch solution is used to obtain pyramids on the wafer. This anisotropic behavior of the solution is due to different crystal orientations having different etch rates. KOH or NaOH etches (100) and (110) surfaces of the Si-crystal with a higher rate with respect to (111) surface [19]. Coverage of the surface with pyramids is obtained by optimizing temperature, time, concentrations of DI-water, IPA and KOH or NaOH. In chapter 3, texturing process will be covered in detail.

2.3 Doping

Doping is the second process of production of screen printed solar cells. Before doping, a pre-cleaning step is applied for textured wafers in order to remove all inorganic-organic contaminants and the natural oxide that may have grown on the

wafer surface by using DI-water, hydrofluoric acid (HF), hydrochloric acid (HCl) and cleaned wafers are dried in hot air.

In general, doping is used to change the electrical properties of semiconductors like conductivity, resistivity etc. by adding impurity atoms into crystalline lattice. In solar cell industry, it is done by solid state diffusion process. This process takes place into a tube shaped oven heated to 800–900^{o}C to provide enough energy in order to change a lattice atom with an impurity atom.

Silicon is an element of Group IV-A of periodic table and its atomic number is 14. The Silicon electron configuration is $1s^2 2s^2 2p^6 3s^2 3p^2$. It means that a silicon atom has to make four bonds to be stable as shown in Figure 17 a. When a V-A group atom having five valance electrons (in solar industry, phosphorous (P) is used) is added to obtain n type silicon, the P atom makes 4 bonds with the nearest Si atom and the rest electron of it will be weakly bonded to it as shown in Figure 17 b. The weekly bonded electron can be separated easily even at room temperature to move through the lattice, and it makes the conductivity higher than before.

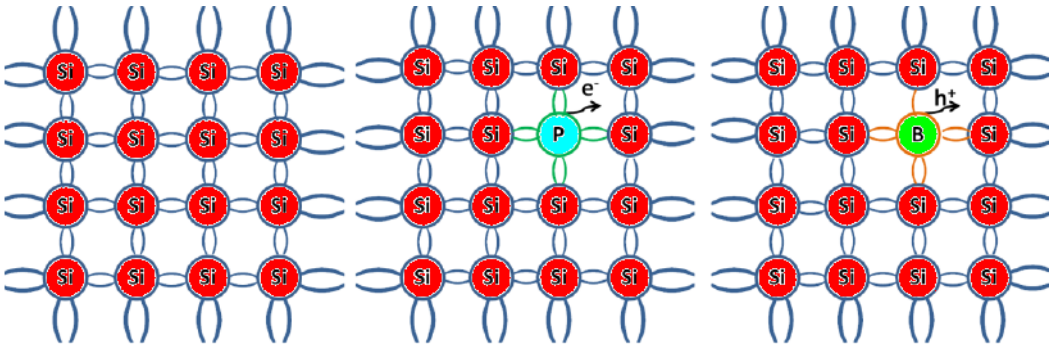


Figure 17: (a) Crystal structure of intrinsic Si; (b) P doped Si crystal structure; (c) B doped Si crystal structure

An element of III-A group like Boron (B) having three valance electrons is doped; there will be a missing electron which is equivalent to an additional hole, in the structure as shown in Figure 17 c. More holes make the conductivity higher than before. This type of material is called as p-type Si.

Standard solar cells are produced on p-type solar cells. N type layer is formed by using liquid phosphorous oxychloride $POCl_3$. $POCl_3$ is converted into gas form by nitrogen gas which flows through the liquid, and it is sent into a tube furnace at a temperature about 840°C. During the flow of this mixture O_2 gas is also sent to the furnace, and the following reactions take place;

$$4POCl_3(g) + 3O_2(g) \rightarrow 2P_2O_5(g)+6Cl_2 \quad (10)\ [20]$$

$$2P_2O_5(g)+5Si(s) \rightarrow 5SiO_2(s)+4P(s) \quad (11)\ [20]$$

$$xSiO_2+yP_2O_5 \rightarrow xSiO_2.yP_2O_5 \quad (12)\ [20]$$

In the first reaction, $POCl_3$ reacts with O_2, and P_2O_5 is formed. This reaction occurs in predeposition step. Then, P_2O_5 reacts with Si, and SiO_2 is formed on the surface of the wafer, and P atoms are released as shown in the second reaction. P atoms diffuse into Si crystal and replace Si atoms, and the p type region is converted into n type. This reaction occurs in drive-in step. In the third reaction, P_2O_5 reacts with SiO_2, and the phosphorous silicate glass (PSG) is formed. After doping, PSG is removed by using HF solution.

2.3.1 P-n Junction

As mentioned in the previous section, majority carriers are holes and electrons, in p type and n type respectively. There are also ionized and fixed atoms in crystal lattice which are negatively charged (like B^-) in p type and positively charged (like P^+) in n type as shown in Figure 18.

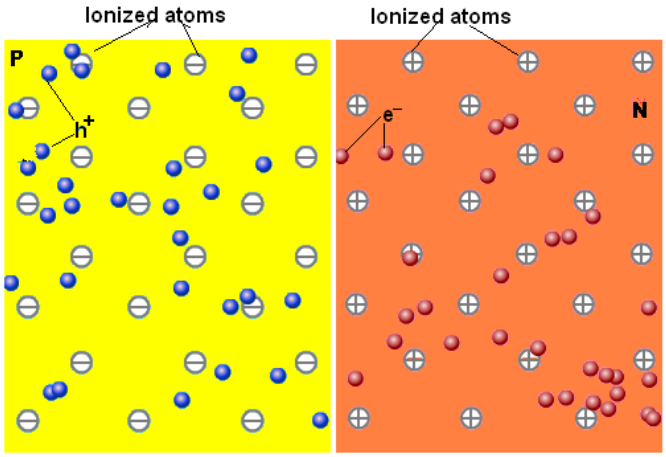


Figure 18: P type and N type semiconductors respectively [3]

When p type and n type semiconductors are combined, electrons from the n-type region diffuse to p type region and leave behind uncompensated positive ions. Similarly, holes in p-type diffuse to n type and leave behind uncompensated negative ions. The uncompensated ions generate an E-field, which prevents substantially the diffusion of e^- to p type and h^+ to n type in equilibrium condition. The Figure 19 illustrates that situation;

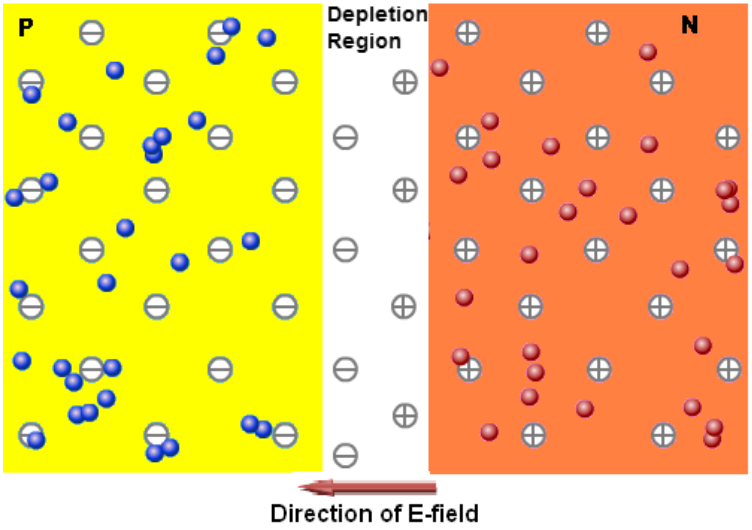


Figure 19 : P-n junction [3]

The region in which there are no free carriers is called depletion region. Also, thanks to E field, the minority carriers (h^+ for n type and e^- for p type) which are close to the depletion region or generated within a diffusion length distance can drift to the other side and be collected easily. And a "built in" potential V_{bi} due to E field is formed at the junction.

2.3.2 Modeling of Solid State Diffusion

The doping process takes places by solid state diffusion of the dopant atoms. This process is explained by Fick's theory of diffusion which was derived by Adolf Fick in 1855. The Fick's first law is [21];

$$J = -D\frac{\partial C(x,t)}{\partial x} \tag{13}$$

- ***J*** is the diffusion flux which is defined as the amount of solute transferred per unit area per unit time and has the units of *mol/cm^2.s*.
- ***D*** is diffusion coefficient or diffusivity of the material defining how easily an atom could move throughout a known medium. Diffusivity defined with the units of *cm^2/s* , changes as a function of temperature and concentration.
- ***C(x,t)*** is the concentration of atoms per unit volume of the medium and defined with the units of *mol/cm^3*.
- $\frac{\partial C(x,t)}{\partial x}$ is known as the concentration gradient which is the driving force of the diffusion process.

The matter flows in the direction of decreasing solute concentration is stated by using the negative sign in the eq. 13. In addition, spatial change in diffusion flux must be equal to the change in solute concentration per unit time within a very small volume of the system as imposed by the continuity. This situation is expressed in Eq. 14 [21];

$$\frac{\partial J(x,t)}{\partial x} = -\frac{\partial C(x,t)}{\partial t} \tag{14}$$

Inserting eq. 13 into eq. 14, the Fick's 2nd law of Diffusion for one dimensional flow is obtained as shown in eq. 15 [21];

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial}{\partial x}\left[-D\frac{\partial C(x,t)}{\partial x}\right] = D\frac{\partial^2 C(x,t)}{\partial^2 x} \tag{15}$$

Eq. 15 can be solved by using different boundary conditions. One of them is that constant source concentration at the surface corresponding to the initial condition C(x,0) = 0 and boundary conditions C(0,t)= Cs and C(∞ ,t) =0 leads to a solution in the form of complementary error function as expressed in Eq. 16 below where C_s is the surface concentration of dopant atoms [21].This situation formulize the predeposition step of the diffusion process in which dopant including process gas is fed to the system with a constant flow rate.

$$C(x,t) = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right) \tag{16}$$

The drive in process takes place after predeposition step. In this process, a thin layer of dopant atoms is already present on the wafer surface. For this process, initial condition is C(x,0)=0 and the boundary conditions are $\int_0^\infty C(x,t)dx = Q_T$ and C(∞, t) =0 , where Q_T is the total amount of dopant per unit area and will diffuse into the Si. The resultant solution satisfying the initial and boundary conditions will be in the form of Gaussian distribution function whose mathematical expression is given in eq. 17 [21].

$$C(x,t) = \frac{Q_T}{\sqrt{\pi Dt}}\exp\left(\frac{-x^2}{4Dt}\right) \tag{17}$$

2.4 Anti Reflecting Coating (ARC)

The surface of the cell is usually covered by SiNx layer as anti reflection coating. Deposition of the SiN_x:H layer is done by using plasma-enhanced chemical vapor deposition (PECVD). There are two significant reasons of deposing a SiN_x:H layer on the front side of the wafer. One of them is to reduce the reflection losses. The reflection index of the SiN_x:H layer is about 2 which is between that of Si (3.5) and that of air (approximately 1) for a wavelength of 600 nm. This makes the layer working well as an antireflective coating. So, the wafer with SiN_x has lower reflection comparing with that of the bare wafer, and more light can be absorbed in the solar cell [6]. The other reason is the passivation effect of the layer on the emitter. The SiN_x:H layer is very rich in hydrogen H, hydrogen also diffuses into the Si-wafer and passivates some impurities or crystal defects [6].

As a passivation and antireflective layer, silicon dioxide (SiO_2) can also be used. However, use of SiO_2 has two disadvantages. The first one is that the processing temperature (about 1000^oC) is high, and it does not passivate as efficient as SiN_x:H. The other one is the refraction index of SiO_2 (1.5) is low.

Theory

Optical behavior of a surface is related to the dielectric constant. Dielectric constant can be described as in eq. 18 [22];

$$\sqrt{\varepsilon_s} = n_s - ik_s \tag{18}$$

In eq. 18, ε_s is dielectric constant, n_s is real part of the refractive index, and k_s is the imaginary part of the refractive index, which is used to define absorption coefficient (α)as shown in eq. 19 [22].

$$\alpha = \frac{4\pi k_s}{\lambda} \tag{19}$$

Reflectance for the light travelling from a medium with refractive index n_0 to a medium with refractive index n_s at normal incidence is expressed as in eq. 20 [22];

$$R = \left(\frac{n_0 - n_s}{n_0 + n_s}\right)^2 \tag{20}$$

If the material is coated with an ARC thin film with refractive index n_1, the eq. 20 becomes for the light of wavelength λ [22];

$$R = \frac{(n_0 - n_s)^2 + \left(\left(\frac{n_s n_0}{n_1}\right) - n_1\right)^2 tan^2\delta_1}{(n_0 + n_s)^2 + \left(\left(\frac{n_s n_0}{n_1}\right) + n_1\right)^2 tan^2\delta_1} \tag{21}$$

where δ_1 is defined as the phase shift in the film with thickness d_1 and can be expressed as in eq. 22 [22];

$$\delta_1 = \frac{2\pi n_1 d_1 cos\theta_1}{\lambda} \tag{22}$$

θ_1 is the angle between the light ray and the normal of the film surface.

When θ_1 is zero (i.e. light at normal incidence), the minimum reflection is obtained at $\delta_1 = \pi/2$ which leads to eq. 23;

$$d_1 = \frac{\lambda}{4n_1} \tag{23}$$

To minimize the reflection once more, the light reflected from the rear and front sides of the thin film should be out of phase so interfere destructively [23]. To get this situation, n_1 can be chosen to satisfy the eq. 24 below [22].

$$n_1 = \sqrt{n_0 n_s} \tag{23}$$

By using the equations above, for a single wavelength the reflection can be made zero. Since the peak power of the solar spectrum is close to wavelength 600 nm, refractive index and thickness of ARC thin film is chosen to minimize reflection at this wavelength in photovoltaic industry [24]. At 600 nm, refractive index of Si is n_s= 3.939, air refractive index is n_0=1. Therefore n_1 can be chosen as approximately 2, and d_1 can be chosen as 75 nm.

2.5 Metallization Screen Printing

Generated minority carriers in the depletion region and within the diffusion length distance from the depletion region are collected by metal contacts which are silver contacts on front and aluminum contacts on rear of the wafer. These contacts are applied using screen printing method.

To get Ag metal in physical contacts with the front side of the cell, the paste containing lead borosilicate glass (PbO-B_2O_3-SiO_2) and organic compounds is used. During the firing process, the lead borosilicate glass etches the ARC film (SiN_x thin film) and provides adhesion of Ag contacts. The firing process takes place at around 875^oC .

For Al back contact, a similar process takes place. To overcompensate the phosphorous doping on the backside and to form proper Back Surface Field (BSF), the quantity of paste is very important [6].

The temperature of firing process must be adjusted to get good and optimal solar cells. For temperatures below 800^oC, good electrical contact between pastes and silicon does not form, and this leads very high series resistance [6]. For

temperatures higher than 900°C, the pastes can diffuse too deeply into silicon and cause short circuits between the front and back contacts [6].

When a metal and a semiconductor are combined, the electrical contact forms in two ways; Schottky and Ohmic contact. These contacts are related to whether the work function of metal is grater or less than the semi conductor.

Schottky Contact

When a metal and a semiconductor are combined, charge transfer occurs until the Fermi levels get the same position. To understand this situation, we look energy band diagrams shown in Figure 20.

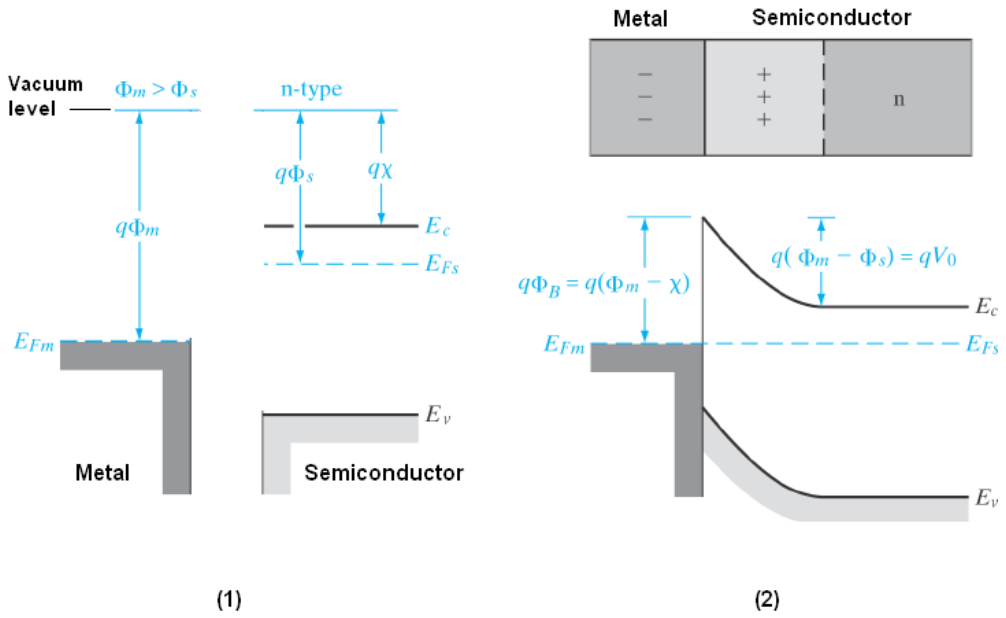


Figure 20:(1) Energy band diagrams of a metal and an n-type semiconductor before combined, (2) Band diagrams after combination of a metal and an n-type semiconductor [25]

In the Figure above, χ is the electron affinity, Φ_m and Φ_s are work function for metal and semiconductor respectively. Φ_m must be greater than Φ_s for combination of metal and n-type semiconductor to get Schottky contact. As shown in Figure 20 (2) conduction and valance band of semiconductor will bend downwards

to prevent further electron diffusion from semiconductor to metal after combination of the materials. Schottky barrier (Φ_B) is formed and electron flow is stopped. Due to electron flow to metal, there are uncompensated donor ions, and these ions induce negative charges at metal side as shown in the Figure 20.

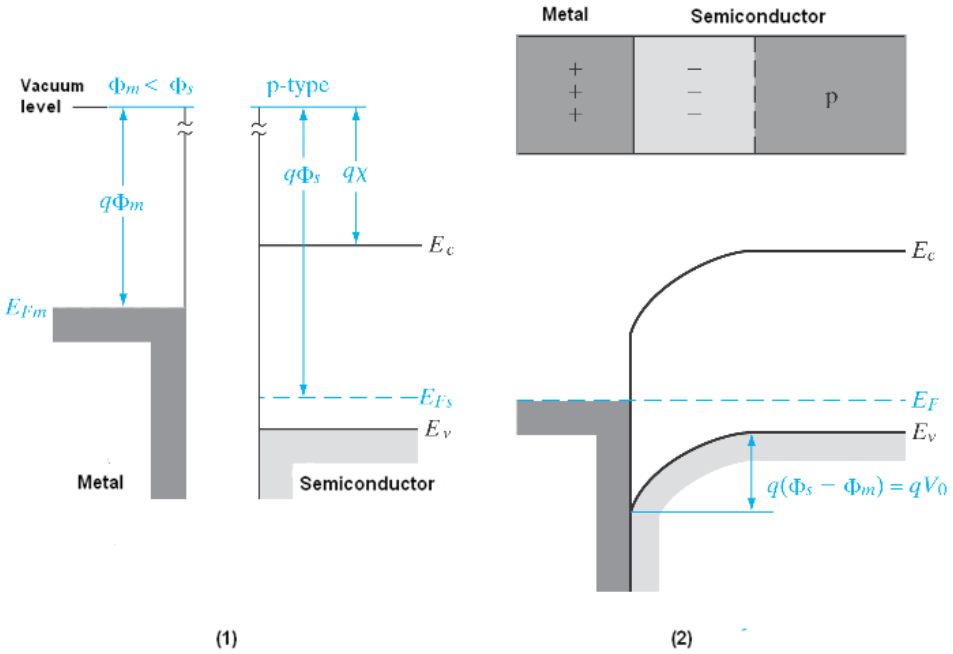


Figure 21: :(1) Energy band diagrams of a metal and a p-type semiconductor before combined, (2) Band diagrams after combination of a metal and a p-type semiconductor [25]

Figure 21 shows the energy band diagrams for a metal and a p-type semiconductor before and after the combination. To form Schottky barrier for a metal and p-type semiconductor, Φ_m must be less than Φ_s. The bending of the conduction/valance band is upward to prevent hole flow between two sides.

Ohmic Contact

For Ohmic contacts, there is no or negligible potential barrier being formed by combination of a metal and a semiconductor. In this case, I-V characteristic is linear and independent of the polarity of applied voltage [25] as shown in Figure 22.

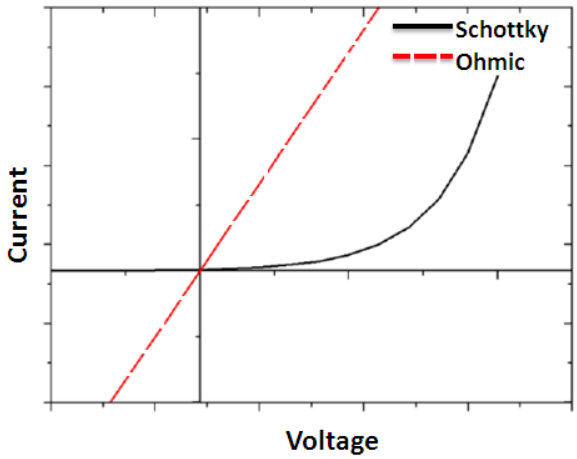


Figure 22: I-V curve for Ohmic and Schottky contact

For ohmic contact, relation between work functions is reversed. In other words, Φ_m must be less than Φ_s for n-type semiconductor-metal combination, and Φ_m must be greater than Φ_s for p-type semiconductor-metal combination. Energy band diagrams are shown for n-type and p-type in Figure 23 and Figure 24 respectively.

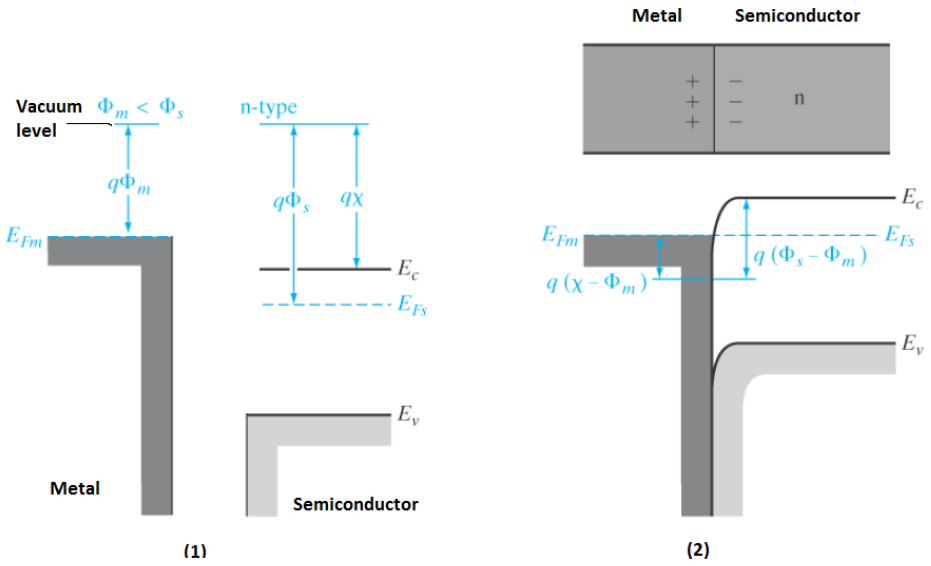


Figure 23: :(1) Energy band diagrams of a metal and an n-type semiconductor before combined, (2) Band diagrams after combination of a metal and an n-type semiconductor for Ohmic contact [25]

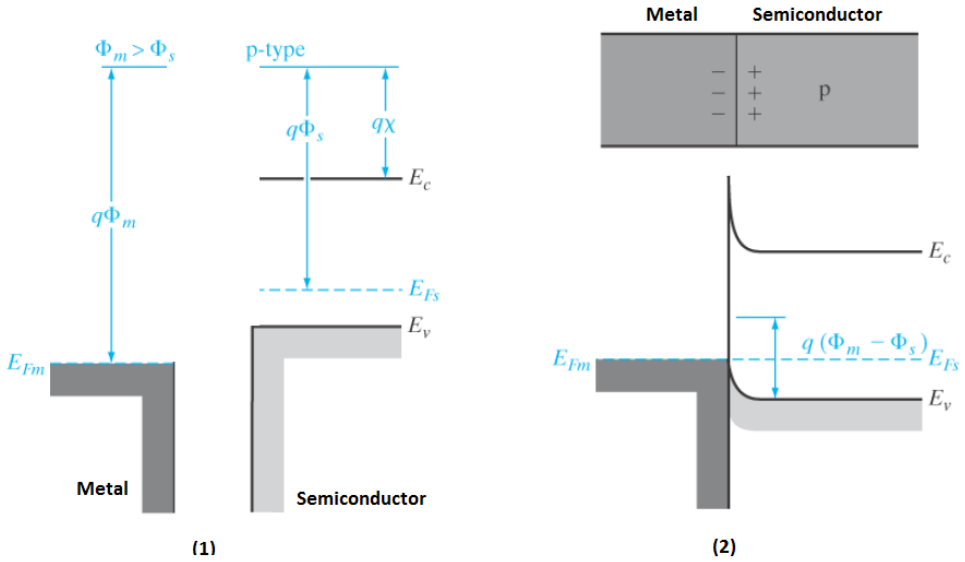


Figure 24: (1) Energy band diagrams of a metal and a p-type semiconductor before combined, (2) Band diagrams after combination of a metal and a p-type semiconductor for Ohmic contact [25]

Although current is allowed in one direction due to the potential barrier for Schottky contact, current can flow in both directions for Ohmic contact. Therefore, front and back contact of solar cells are required to be Ohmic. As mentioned above, Ag is used for front side for n type region, and Al is used for back side for p type region to get Ohmic contact.

2.6 Edge Isolation

During the doping process, front side, back side and edges of p-type silicon wafer is doped to produce n-type region. Although Al is diffused and converts the n-type region formed at backside into highly doped p-type (p^+) region in metallization process, edges are not converted. This situation forms possible paths for generated minority carriers to be able to flow to p-side through the edges, instead of being collected at an external load. Figure 25-1 on the next page illustrates this situation. Edge isolation disconnects the electrical contact between the front and the back contacts. This is accomplished by either plasma/chemical etching which removes n

regions on edges completely or by laser ablation which forms shallow grooves on the solar cell. Figure 25-2 shows the operation of solar cell after edge isolation.

Finally, the solar cells current-voltage characteristics of solar cells are obtained by measurements under AM1.5 spectrum illumination conditions in order to characterize.

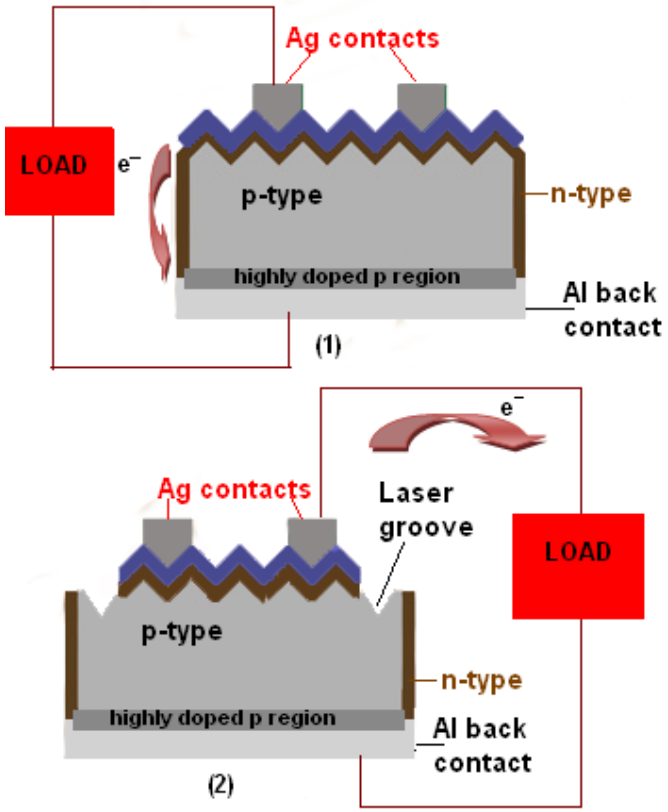


Figure 25: Solar cell operation before (1) and after (2) edge isolation [26]

CHAPTER 3

FUNDAMENTALS OF CHEMICAL ETCHING PROCESS AND LIGHT TRAPPING

3.1 Introduction

Absorption of photon is the critical process for solar cell devices because absorbed photons generate electron hole pairs which form the output power of the solar cells. As mentioned above, the band gap of silicon is 1.12 eV, and wavelength between 300-1100 nm is suitable for the photovoltaic conversion as shown in Figure 26.

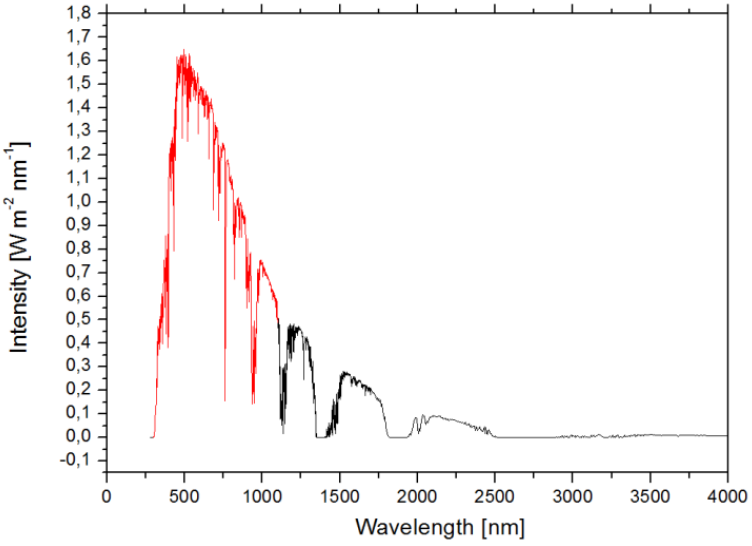


Figure 26: AM 1.5 spectrum at global tilt [27]

The Figure 27 shows the thickness which is needed to absorb the incoming wavelength. As can be seen from the Figure, wafers with 400 µm thickness are needed to absorb 90 % of incoming intensity with wavelength between 300-1000 nm.

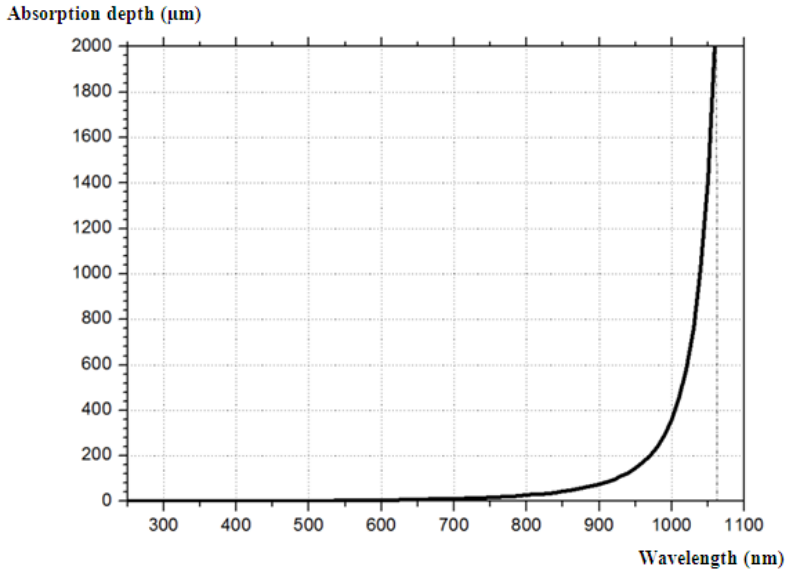


Figure 27: Absorption depth of Si for 90% absorption [12]

Use of thicker wafers causes problems like difficulties in collection of generated electron-hole pairs having minority carrier diffusion lengths 14 µm for n type and 140 µm for p type [23], heavy modules, high cost etc. In other words, thicker wafers have high absorption but they have low collection probability whereas thinner wafers have high collection probability whereas they have poor absorption at long wavelengths. To avoid these problems, surface texturing is used.

Although there are several dry texturing process techniques reported in the literature to produce low reflective textured surfaces, structures produced by dry process like needle, tips, wires etc. are not suitable for reliable passivation of c-Si surface in solar cells [28]. On the other hand, pyramids formed as a result of different etch rates of (100) and (111) planes are of the orders of micrometer scale. These properties of alkaline texture make it an essential step for the industrial mono-c applications.

Figure 28 (a) shows the crystalline structure of Si which is a face centered cubic structure with a base of two identical atoms located at the (0, 0, 0) and (1/4, 1/4, 1/4) position. Every silicon atom is located at the center of a tetrahedron and is covalently bonded to four other atoms. The number of free bonds of silicon atoms is the difference in surface planes which are represented by Miller indices as shown in Figure 28 (b). Si atoms have one free bond in the (111) plane, which means Si atoms in this plane are bounded to the Si crystal with three other Si atoms. On the other hand, Si atoms in the other planes, like (100) and (110), are bounded with two other Si atoms and have two free bonds. Therefore, energy needed to dissolve Si atoms in (111) plane is higher than energy required to dissolve atoms in (100) and (110) planes. The energy differences lead that texturing of Si wafer with KOH-IPA solution which is an anisotropic etching process (i.e. etching rate is orientation dependent). In the next section, explanation of the etching process is given [29].

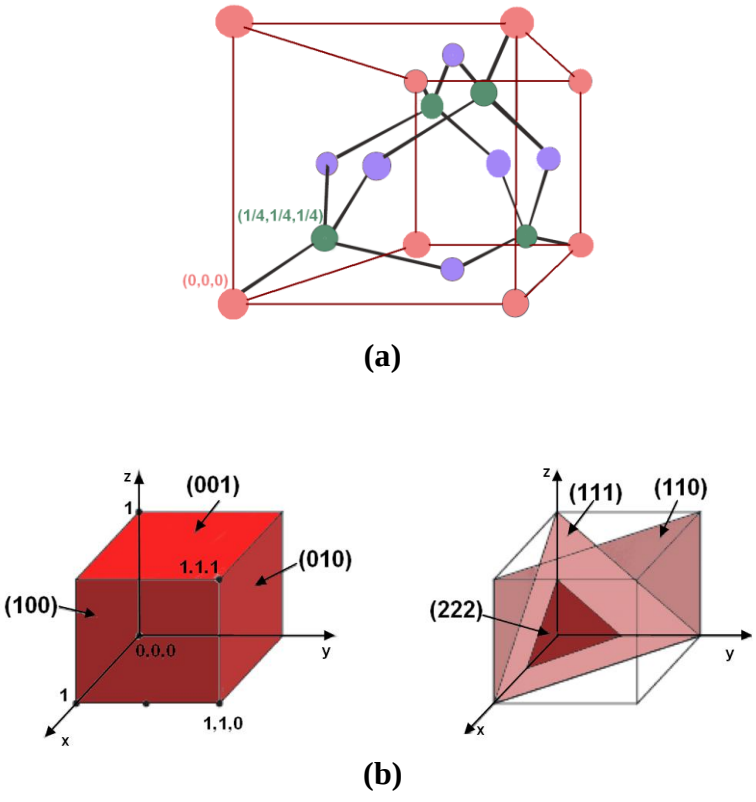
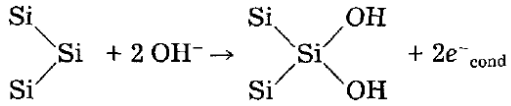


Figure 28: (a) The silicon crystal (b) Miller indices in a cubic structure

3.2 Wet Chemical Etching with KOH/IPA Solution

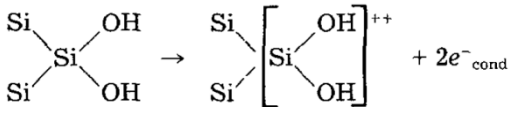
Although there are many explanations [29]–[32] about the anisotropic and selectivity effects of alkaline etch solutions on mono-crystalline silicon, the process keeps its mystery, and further investigations should be done [6] . Among these explanations, H. Seidel et al. [29] described well the mechanism of the etching process [6]. In this section, the KOH based etching process is explained by using Seidel explanations.

Two hydroxide ions OH^- from the alkaline solution bind to Si atoms having two free bonds on plane (100) and two electrons from OH^- are injected in the conduction band of the silicon as indicated in Equation 25.



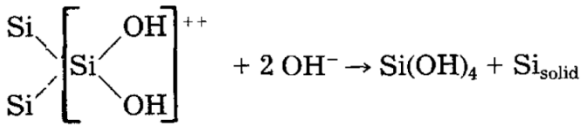
(25)

The strength of Si-Si back bonds weakens due to the bonds between Si and OH. A soluble silicon hydroxide (Si-OH) complex is obtained by breaking the Si-Si back bonds of the $Si(OH)_2$ which happens when two electrons from back bonds are excited to the silicon conduction band. This is shown in Equation 26. The reactions shown in Equations (25) & (26) occur more or less simultaneously.



(26)

The positive silicon hydroxide complex reacts with another two hydroxide ions from the solution and orthosilicic acid $Si(OH)_4$ is produced as shown in Equation 27.



(27)

The $Si(OH)_4$ can now get mixed into the solution by diffusion, and it is unstable due to the high pH value greater than 12 of the solution. For these pH values, the detachment of two protons from $Si(OH)_4$,which forms the following complex as shown in Equations 28 & 29, will occur. This silicate species was observed by Raman spectroscopy measurements [31].

$$Si(OH)_4 \rightarrow SiO_2(OH)_2^{--} + 2H^+ \quad (28)$$

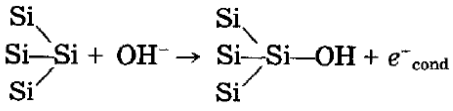
$$2H^+ + 2OH^- \rightarrow 2H_2O \quad (29)$$

The electrons located near the surface from Equations (25) & (26) in the conduction band can be transferred to the water molecules close to the surface of silicon, thus hydroxide ions and hydrogen atoms are produced, and they recombine to molecular hydrogen as shown in Equations (30) & (31).

$$4H_2O + 4e^- \rightarrow 4H_2O^- \quad (30)$$

$$4H_2O^- \rightarrow 4OH^- + 4H \rightarrow 4OH^- + 2H_2 \quad (31)$$

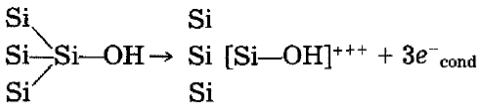
Si atoms on (111) plane have one free bond and react with one hydroxide ion as shown in Equation (32).



(32)

Three back bonds of the surface silicon atom have to be broken. In analogy to Equations (26) & (27), this will happen when three electrons are transferred to the

conduction band , and three OH^- will bind to Si-OH complex as shown in Equations (33) & (34). The reaction will continue as described above for a (100) plane.



(33)

$$[Si\text{-}OH]^{+++} + 3\ OH^- \rightarrow Si(OH)_4 \quad (34)$$

According to Seidel study, there is no significant role of the potassium cations K^+ and IPA in the etching process of Si, and they can be neglected during forming reaction equations [6].

The effects of IPA found in the literature in the etching process can be listed below;

- As the concentration of IPA increases, the etch rate decreases [33].
- Its role is to move away H_2 bubbles from surface by decreasing the silicon surface tension and improving the wettability of the wafer surface [34], [35]. When this happen, the attraction between the etching solution and the surface will form easily, and homogenous texturing will occur.
- IPA adjusts the relative water concentration of the etchant [29]. It attracts water concentration around itself, so it regulates the etching rate for solutions with a constant KOH concentration and constant temperature [6].

3.3 Surface Morphology and Light Trapping

Due to the difference in the etching rates of different planes, square based pyramids are formed during the etching process. The Figure 29 shows the steps of formation of pyramids. A wafer with (100) orientation is dipped into the KOH/IPA solution and etching starts. As mentioned above, (100)

plane is etched faster than (111) plane and the proportionality between them is 600/1. The process continues with high etch rate until all surfaces become (111) planes. After that point, the process will be very slow; i.e. no change will be observed.

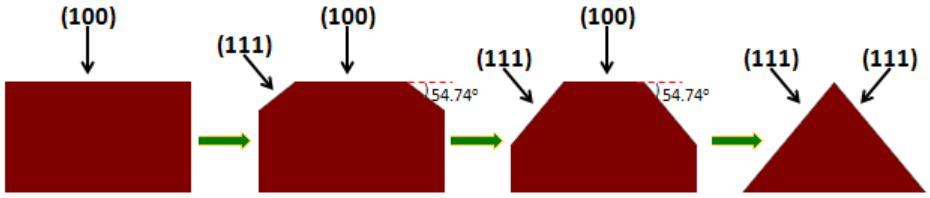


Figure 29: Formation of square based pyramids of (100) oriented Si wafer

The pyramids, whose bases are formed by (100) planes and sides are formed with (111) planes, will be formed on the surface of the mono-Si wafer at the end of the process.

To observe surface morphology of textured wafers, scanning electron microscope (SEM) is used, because SEM pictures have strong signal contrast, lateral resolution and depth of sharpness [36]. By using SEM pictures, the edge of pyramids can be measured and the height of the pyramids (pyramid size referred in the literature) can be determined as shown in the Figure 30. As shown in the Figure, the height of the pyramids is equal to “s” which is equal to half of the edge.

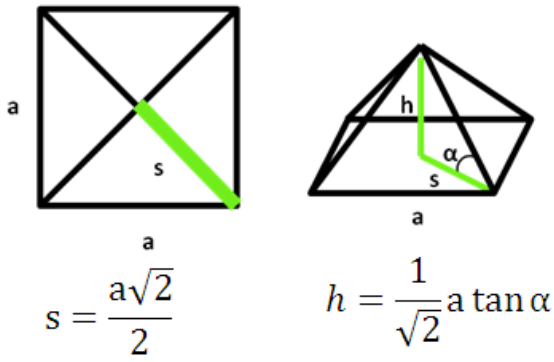


Figure 30: Square pyramid with base length "a", height "h" and half of the diagonal of base "s". The angle "α" between the pyramid edge and its projection "s" is equal to "45°" due to crystallographic structure [36].

The formation of the pyramids on the wafer increases the optical path length which is the distance being travelled by a photon without being absorbed. In other words, texturing process makes silicon thicker optically without changing the actual thickness of it and increases the probability of photon absorption. The Figure 31 illustrates this situation.

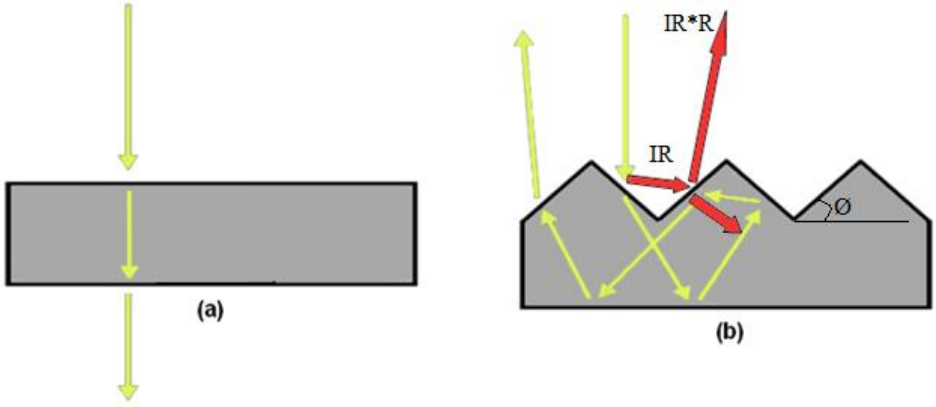


Figure 31: (a) Reflection from non-textured Si (b) Reflection from textured Si

As shown in the Figure 31 (a), the incoming light hits the surface and goes on its path in the Si. It reaches the back side and leaves the Si. In this case huge amount of light is reflected from the surface and leaves without being absorbed.

The Figure 31 (b) shows that incident light striking the textured surface. In this case, some amount of incident light will be transmitted into wafers and some will be reflected. Therefore, square of non-textured wafer reflection will be the limit one can reach .The probability for more than one bounce of light depends on the angle "Ø" (equal to 54.7^{o} in our case) which is the angle between Si surface (in our case (100) plane) and the faces of the pyramids (in our case (111) plane) [37]. If the angle "Ø" is less than 30^{o}, the normally incident light will not receive more than one bounce. If Ø is between 45^{o} and 60^{o}, the double bounce of normally incident light will occur. If Ø is greater than 60^{o}, the triple bounce of light will occur [37]. When the reflected light reaches the other pyramid, some amount of it will be again reflected and transmitted. Therefore, the transmitted light into the wafer will be increased and the reflection will be decreased. In the wafer, the light will not leave as in the first case and it will be reflected more than one and the optical path will be increased. As the optical path increases inside the wafer, more light will be absorbed and more electron hole pair will be generated. In other words, the efficiency will increase.

CHAPTER 4

EXPERIMENTAL PROCEDURES

4.1 PROCESS FLOW OF SOLAR CELL FABRICATION

4.1.1 Texturing of Silicon Wafer

Process flow of Si solar cell production starts with texturing process. An ultrasonic bath shown in Figure 32 is used to agitate the KOH-IPA solution, and its frequency is 35 kHz. It is capable of processing 25 wafers per run. Ultrasonic source is used to get uniform temperature distribution and solution homogeneity during reaction. The percentage of ingredients will be mentioned in chapter 5.

Figure 32: Ultrasonic cleaner

For magnetic stirring texturing process, a hot plate, teflon holders a glass beaker (2.5 liter volume) shown in Figure 33 are used. The hot plate has a stirring speed controller and temperature controller.

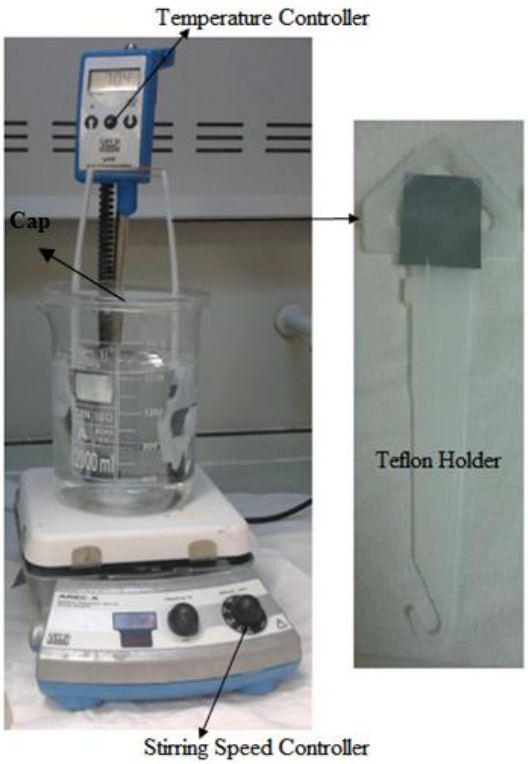


Figure 33: Hot plate and teflon holder

The process is followed by rinsing the textured wafers with DI-water, cleaning in HF-HCL solution and drying them in hot nitrogen gas. While removing metal impurities on the Si-wafer surface is done by HCl, the native oxide and the impurities on surface are removed by HF which makes the wafer surface free of trace metals [33].

4.1.2 Doping

Standard doping recipe optimized at GUNAM Laboratories is used to get 55 Ω/□ sheet resistance. Doping process is done by using *SEMCO Engineering Incorporation MINILAB Series* doping furnace. The dopant source is liquid

phosphorous oxychloride $POCl_3$ transported into furnace by N_2. Figure 34 shows the schematic of doping furnace [9]. The process flow is mentioned in the section 2.3.

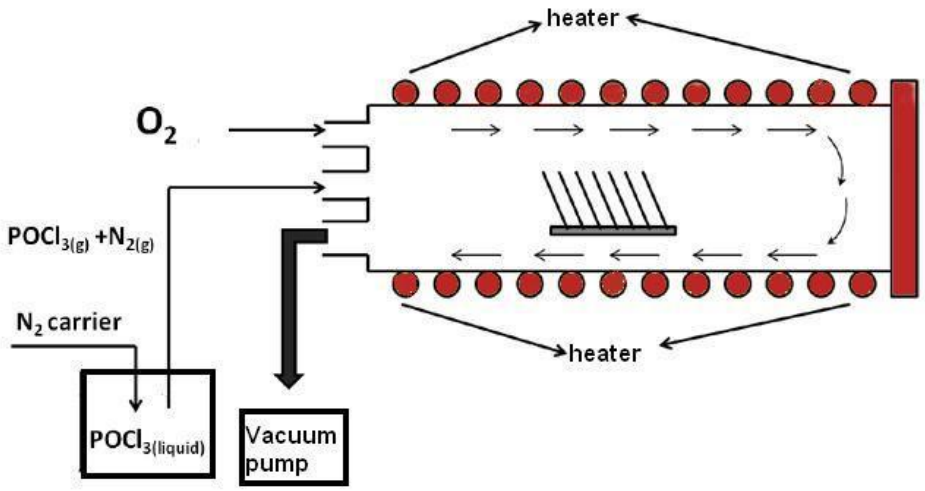


Figure 34: Schematic of doping furnace [9]

4.1.3 Anti-Reflecting Coating

By using *SEMCO Engineering Incorporation MINILAB Series*, a-SiNx deposition is carried out in PECVD chamber. The chamber can take 10 wafers per run. The schematic representation of the chamber is shown in Figure 35.

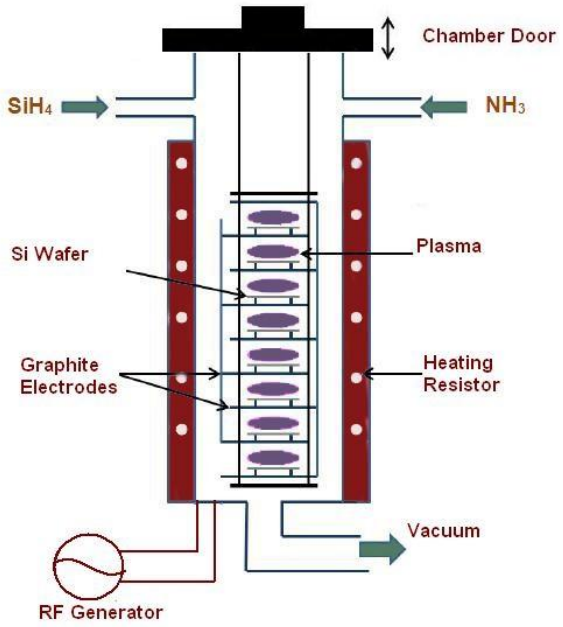


Figure 35: The schematic representation of PECVD chamber [9]

The chamber is filled with SiH_4 and NH_3 gases. The process is carried out at 380^oC and 1 Torr. An RF generator, which works at 375 W with 50 kHz, is used to obtain plasma. The chemical reaction of process is shown in Equation 35.

$$3SiH_{4(g)} + 4NH_{3(g)} \rightarrow Si_3N_{4(s)} + 12H_{2(g)} \quad (35)$$

4.1.4 Metallization and Co-Firing

ASYS EKRA-XL1 screen printing system has been used for metallization of textured, doped, and coated with ARC Si-wafers. The system is in GÜNAM laboratory and is shown in Figure 36.

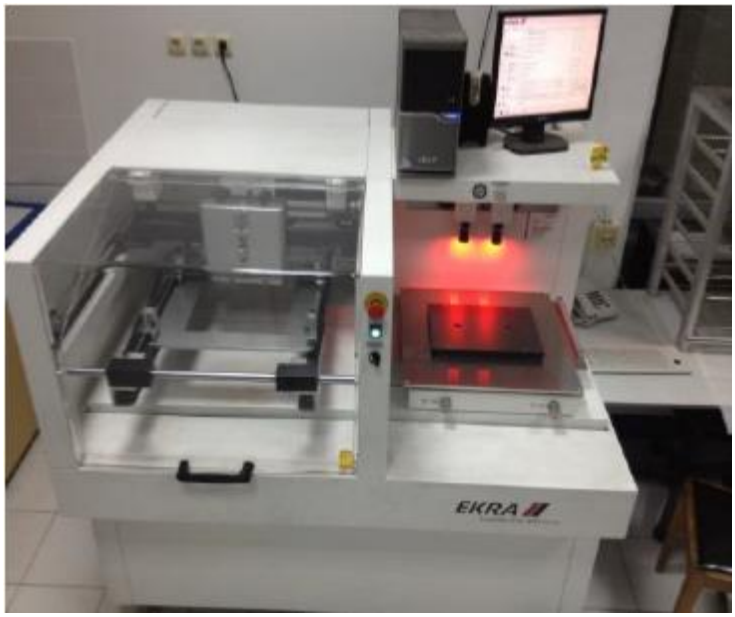


Figure 36: *ASYS EKRA-XL1* screen printing system

Backside is covered fully with Al, and front side is covered using a metallization mask with Ag as mentioned in the section 2.5. The design of mask is done by considering two issues. One of them is the shadowing effect. The busbar's and finger's width should be as small as possible to obtain more interaction between incoming light and front surface of the wafer. As mention above, more light means more short circuit current. The design of back and front contacts are shown in Figure 37. The other one is to obtain lowest resistance, because the contact resistance increases, the efficiency decreases.

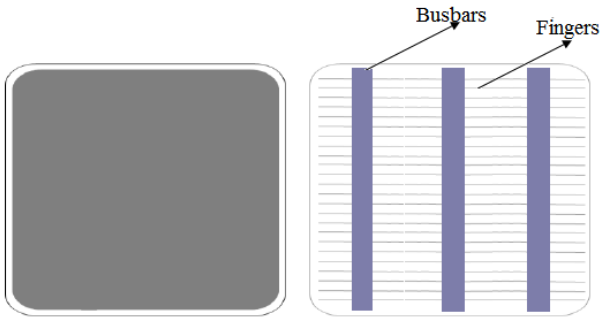


Figure 37: Al mask for backside is in left, Ag mask for front side is in right

To overcome these two requirements, the width and height of the finger shown in Figure 38 should be optimized. The ratio of the width and height is called aspect ratio. The width of finger should be as small as possible to overcome shadowing effect, and the height of finger should be as long as possible to get large finger cross sectional area which leads less resistivity. The aspect ratio can be between 0.20 and 0.30 in screen printing metallization [38].

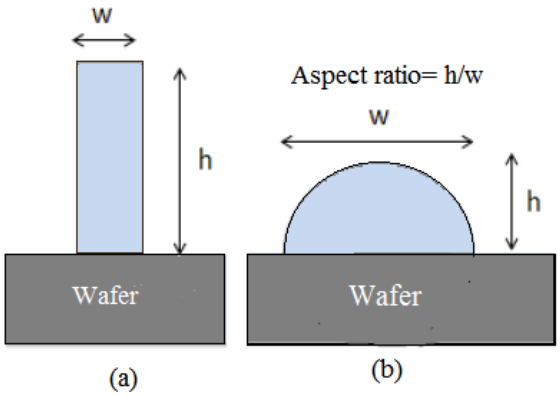


Figure 38: (a) Ideal case (b) Real case

After finding the optimized aspect ratio and printing front contact and back contact, the contacts are dried. Wafers with dried contacts are ready to co-firing process by using a conveyor belt. During the process, the wafers are exposed to high temperature under atmospheric condition. The temperature profile of the firing furnace is like a sharp Gaussian distribution function with a peak temperature around 830^{o}C. At the end of process, Al is melted and forms p^{+} back surface field, and Ag diffuses through the ARC layer and forms front contact without melting.

4.1.5 Edge Isolation

The last process for producing a Si-solar cell is the edge isolation. The process is carried out by using an IR marking laser. The edges of wafer are scanned. At the end of the process, 10-15 µm deep grooves are formed and the connection between the back and front (p and n region) is interrupted.

4.2 Average Pyramid Heights and Pyramid Density, Mass Loss

By using SEM images, two parameters namely; average pyramid heights (APH) and pyramid density (PD) can be found. To find these parameters, I used an open source program "Imagej". The program can identify the tips of the pyramids and give the number of pyramids in the SEM images as shown in Figure 39. Also by using the program, the area of the picture can be obtained. By using these quantities, PD is equal to number of pyramids divided by area of image as shown in Equation 36.

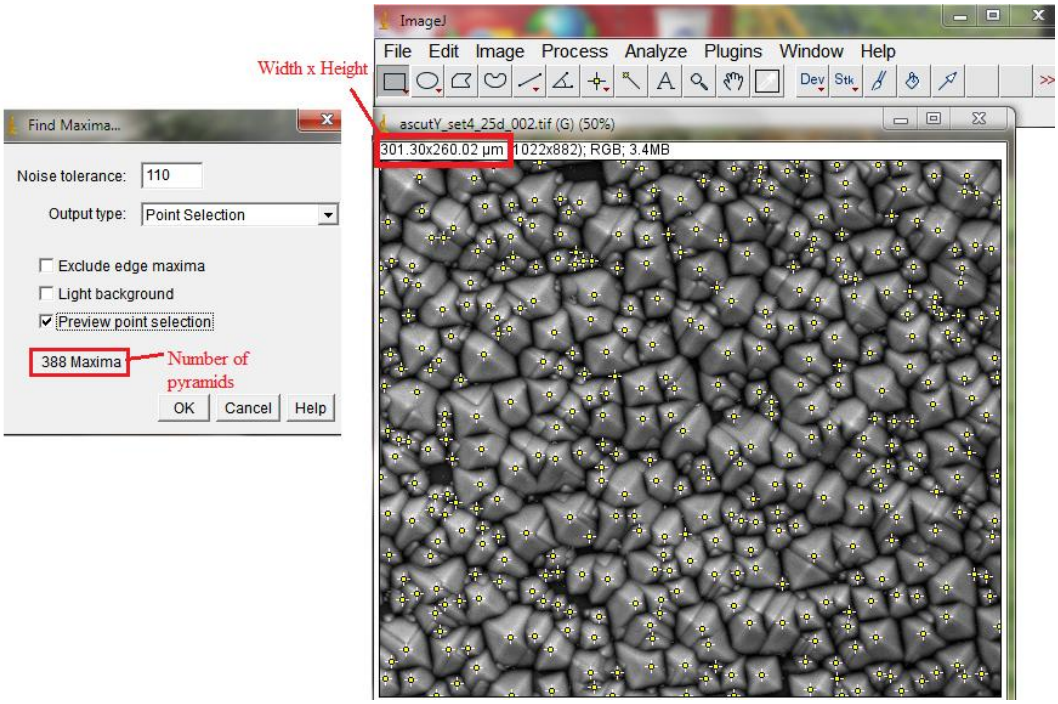


Figure 39: Finding number of pyramids by using the program

$$Pyramid\ Density\ (PD) = \frac{\text{Number of pyramids}}{\text{Area of Image}} \qquad (36)$$

To find the average pyramid height, it is assumed that the bases of pyramids do not nest each other and the surface is covered with pyramids as shown in

Figure 40. As mentioned in section 3.3, the height of the pyramid is equal to "s". APH can be found by using the equation 37, 38 and 39.

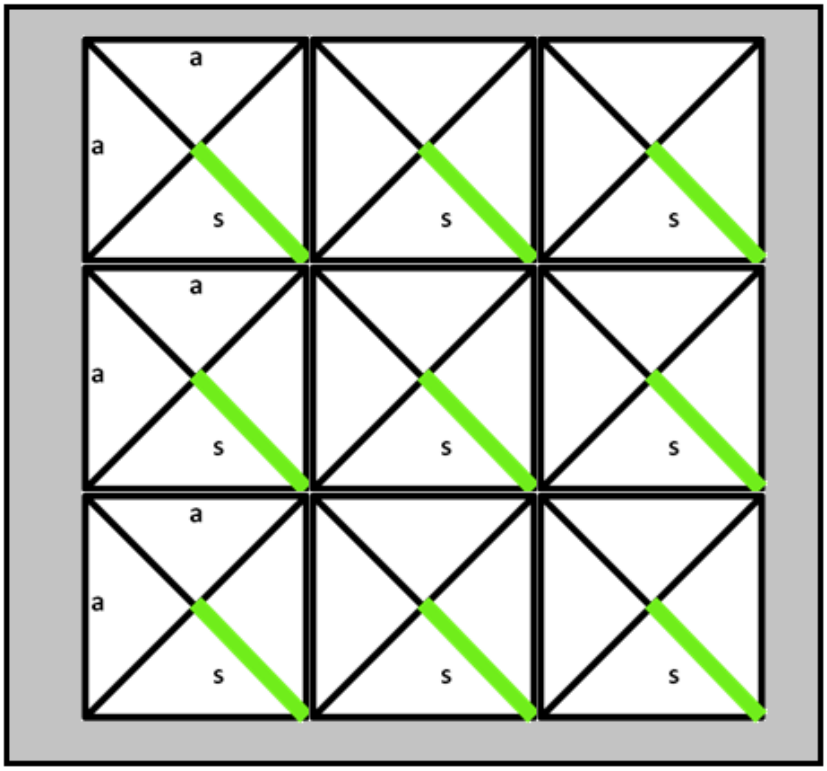


Figure 40: Wafer surface with uniform upright pyramids

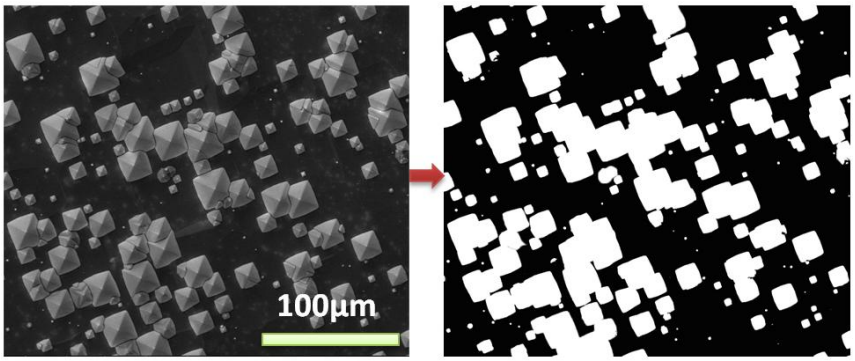
$$Area\ of\ Image = Number\ of\ Pyramids\ x\ a^2 \tag{37}$$

$$a = \sqrt{\frac{\text{Area of Image}}{\text{Number of Pyramids}}} = \sqrt{\frac{1}{PD}} \tag{38}$$

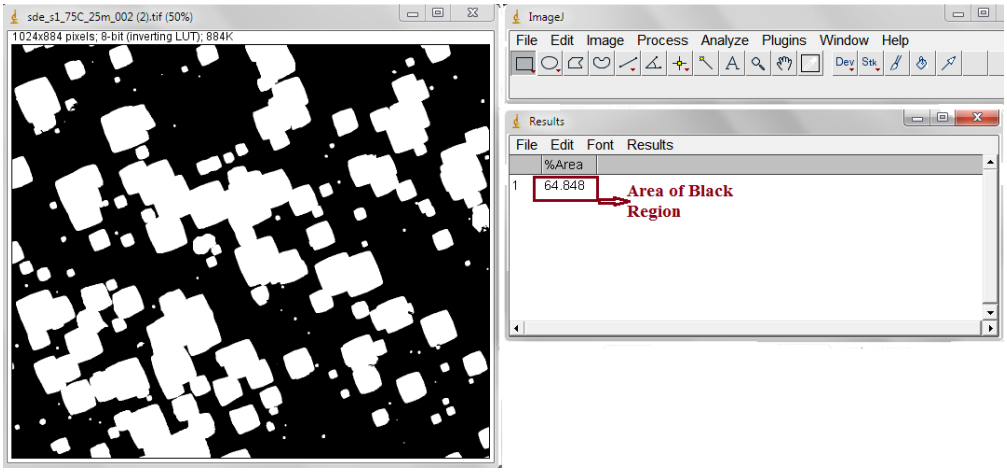
$$APH = \frac{a\sqrt{2}}{2} = \sqrt{\frac{1}{PD}} x \frac{\sqrt{2}}{2} = s \tag{39}$$

Using "ImageJ", the area covered by pyramids can be estimated from the SEM images. The image is converted to black-white image as shown in Figure 41(a)

where the black area is non-textured surface and the white area is surface with pyramids. Then, the black-white image is analyzed by the program that gives area of the black region as shown in Figure 41(b). By subtracting this quantity from 100, the textured area can be obtained.



(a)



(b)

Figure 41: a) SEM image after converting black–white b) Area of black region

Mass loss of textured wafers is measured by using a balance, *Scaltec SBA31* shown in Figure 42. The mass loss is calculated by measuring the weight of wafer before and after texturing process and taking the ratio.

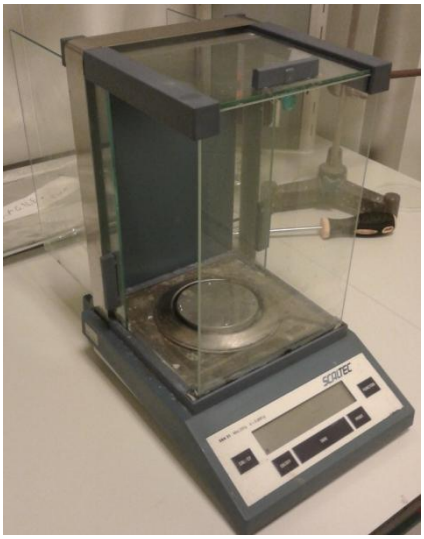


Figure 42: Scaltec SBA31 balance

4.3 Characterization of Solar Cells

4.3.1 Reflection Measurements

First characterization step is reflection measurement of textured wafers. Reflection of a wafer shows the quality of the texturing process. In other words, as the area without pyramids increases, the reflection increases. Also reflection of wafers with ARC is measured.

The measurement setup is shown in Figure 43. The setup consists of an integrating sphere, a lock-in amplifier, a chopper and controller, a calibrated silicon detector, a halogen lamp, a monochromator, a focusing lens and a PC.

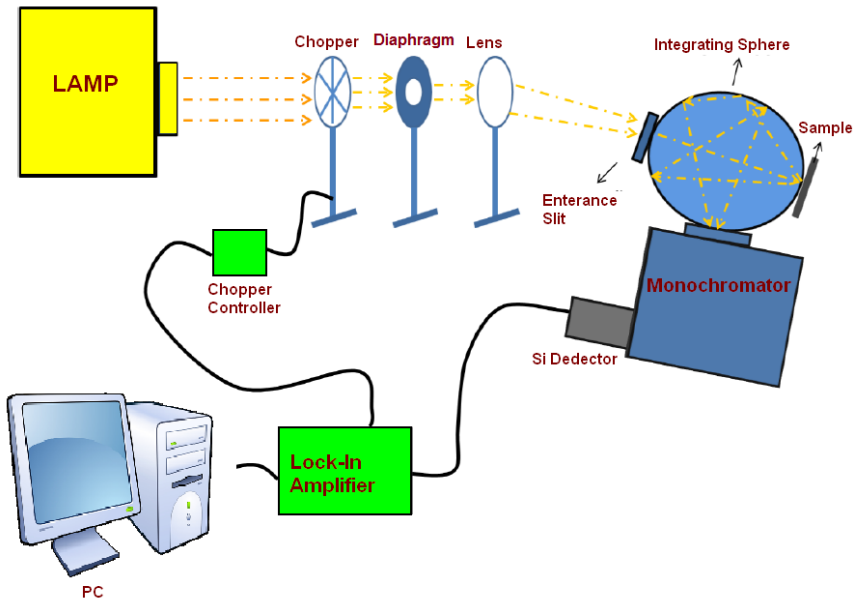


Figure 43: Reflection measurement setup [9]

Light coming from the halogen lamp is modulated by the chopper whose frequency is not equal to multiples of 50 Hz to prevent the affects of network electricity. Frequencies which are not equal to chopper's frequency are filtered by the connection between chopper controller and lock-in amplifier. After that, the spot of modulated light is decreased by the diaphragm and focused on the wafer surface by the converging lens. The reflected light is collected at the entrance slit of monochromator after many reflections. The light passing through the monochromator is detected by the Si-detector which is connected to the computer via the lock-in amplifier. The reflection is measured between 350 nm and 1100 nm. To calculate the reflection of the sample, the (total) reflectance of BaSO4 reference disk that is used in (our regular) total reflectance measurements has been measured using NIST traceable Spectralon Diffuse Reflectance Standard (WS-1-SL) from Labsphere [39]. Therefore, the reflection of the sample will be equal to the ratio of the sample's intensity to that of calibration disk.

4.3.2 I-V Measurements

The measurement is carried out in GÜNAM laboratory by using AM1.5G calibrated *QUICK SUN-120CA-XL Solar Simulator* which is shown schematically in Figure 44. Simulator's software provides cell efficiency, fill factor, series resistance, shunt resistance, open circuit voltage, short circuit current and maximum power point as output data.

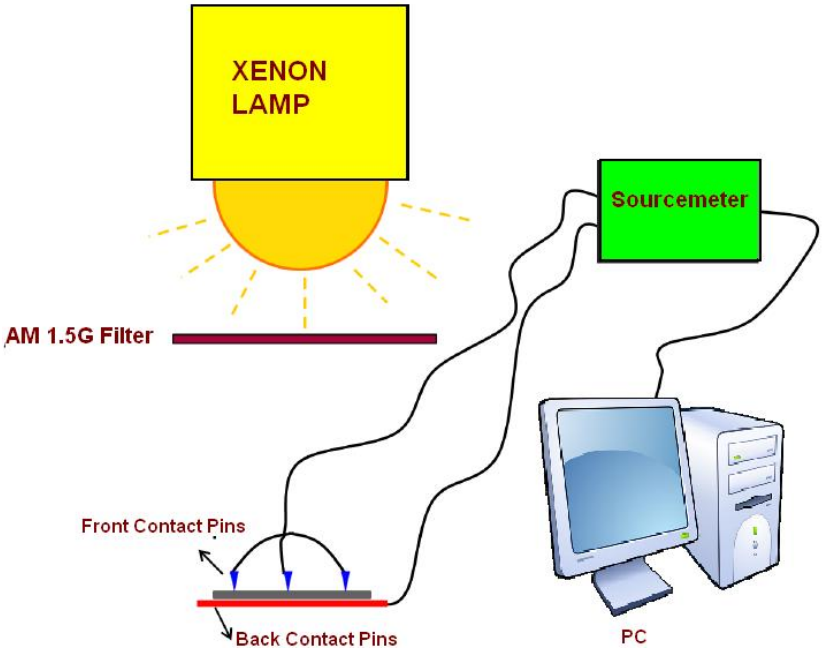


Figure 44: Schematic presentation of solar simulator [9]

4.3.3 Electroluminescence Measurements

The measurement is carried out by using a MBJ closed box Electroluminescence system in GÜNAM laboratory. The measurement is done by applying bias to the cells to force them to radiate. No radiation will be observed in dead regions where radiation does not occur and the generated picture gives us information about cracks and contacts problems.

4.3.4 External Quantum Efficiency (EQE) Measurements

In this measurement, the number of electrons generated per incident photon as a function of wavelength is determined. EQE measurement provides information about the effects of contacts, the junction quality, and recombination dynamics across the device. The setup is shown in Figure 45.

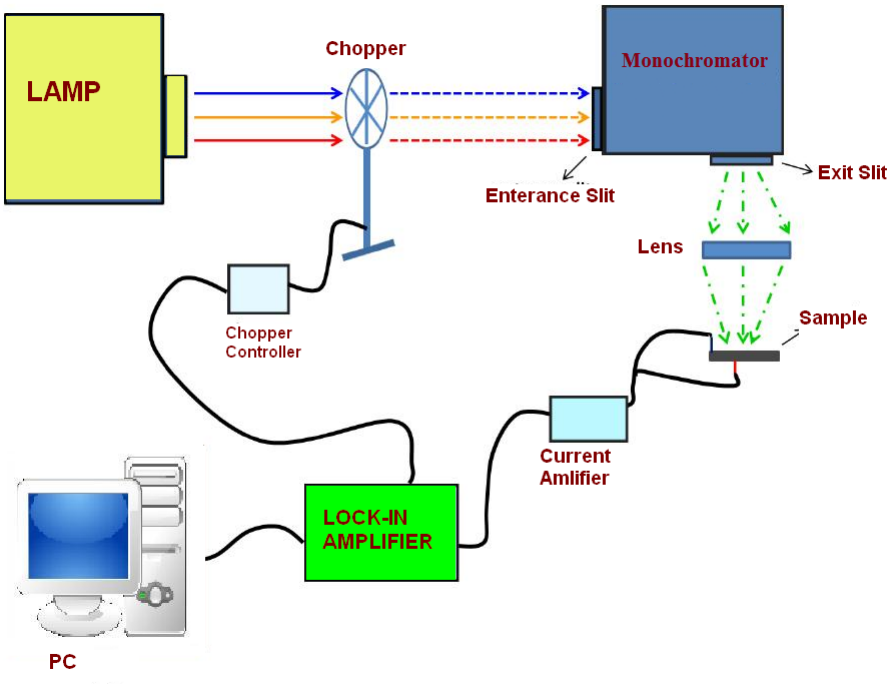


Figure 45: Schematic representation of EQE measurement setup [9]

The light is modulated by the chopper and passes through the monochoromator. Then it is focused on the wafer between the fingers by the converging lens. The generated electron hole pairs are collected by two probes which are connected to the front Ag busbar and Al back surface. The resultant response is monitored after the collected signal amplification by lock-in amplifier.

4.3.5 Suns-Voc Measurements

The measurement is carried out using Suns-Voc system in GÜNAM laboratory. The results of the measurement give us information about the base material and passivation quality. In addition, the I-V behavior of the cell can be predicted by analyzing the obtained data under zero series resistance assumption which leads to estimate some important cell parameters like pseudo efficiency, pseudo fill factor etc., because the effect of shunt and series resistance could have been separated from each other. Power loses due to series resistance can be estimated by comparing efficiency measurement results obtained by using solar simulator and Suns-Voc [40].

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Texturing Process with Magnetic Agitation

In the first part of the study, the effects of temperature, time, and concentration of the ingredients were investigated by using the hot plate. In addition, the effect of surface morphology was investigated by using as-cut and saw damage etched (SDE) wafers. In this part, 5x5 $cm^{2,}$ p-type, 1-3 Ω-cm, (100) CZ-Si wafers were textured. After texturing process, reflection measurements and SEM images were taken to obtain texture quality and surface morphology.

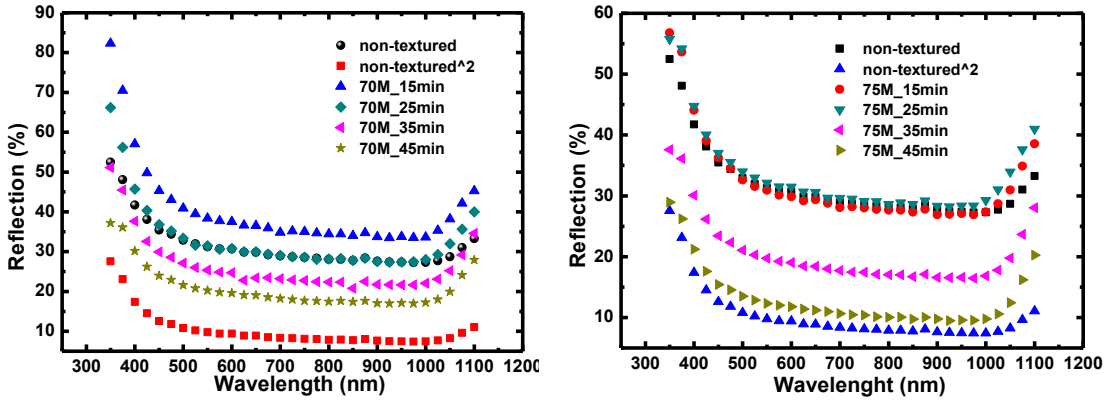
5.1.1 Effect of Process Duration

To observe the effect of process duration, the etching solution consisting of 1500 ml DI-water, 63 g KOH, and 80 ml IPA was prepared. The etching duration was up to 45 minutes. The temperatures were 70, 75, and 80^{o}C. Table 1 shows the parameters of six different as-cut and SDE wafer texturing processes using chemical solutions based on KOH/IPA/DI-water for magnetic agitation.

Table 1: Parameters of three different AS-CUT/SDE wafer texturing processes using chemical solutions based on KOH/IPA/DI-water for magnetic agitation.

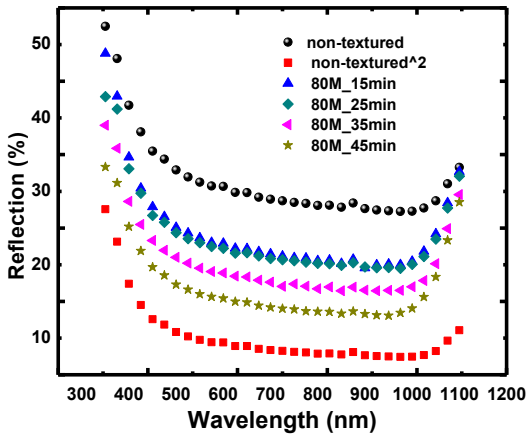
Process Name	IPA (vol%)	KOH (wt%)	Temperature (C)	Agitation rate (rpm)	Process Time (min)
70M	5.4	4.2	70	50	15,25, 35,45
75M	5.4	4.2	75	50	15,25, 35,45
80M	5.4	4.2	80	50	15,25, 35,45

Figure 46 shows the reflection measurement results for as-cut wafers. As can be seen from the figure, as the process time increases, the reflection decreases. The minimum reflection is obtained for 45 min texturing. When the reflection results at three different temperatures are compared, the minimum reflection is obtained in process 75M. Therefore, the optimum temperature for these concentrations is 75^{o} C for as-cut wafers being textured with magnetic agitation.



(a) **(b)**

Figure 46: Reflection of textured as-cut wafers for process 5.4vol% IPA, 4.2wt% KOH with magnetic agitation at (a) 70^{o}C (b) 75^{o}C (c) 80^{o}C



(c)

Figure 46: (Continued)

Figure 47 shows SEM images of as-cut wafers for process 5.4vol% IPA, 4.2wt% KOH at 75^{o}C. As can be seen from the images, as the texturing time increases, area with pyramids increases which leads to lower reflection. The pyramid heights can be identify clearly, and they are between 1.5 -11 µm for 15 min texturing, 3 -16 µm for 25 min texturing, 9 -20 µm for 35 min texturing. After 35 min texturing, the bases of pyramids nest and it makes difficult to identify the heights correctly. It can be said that as the process duration increases, the pyramid heights also increase.

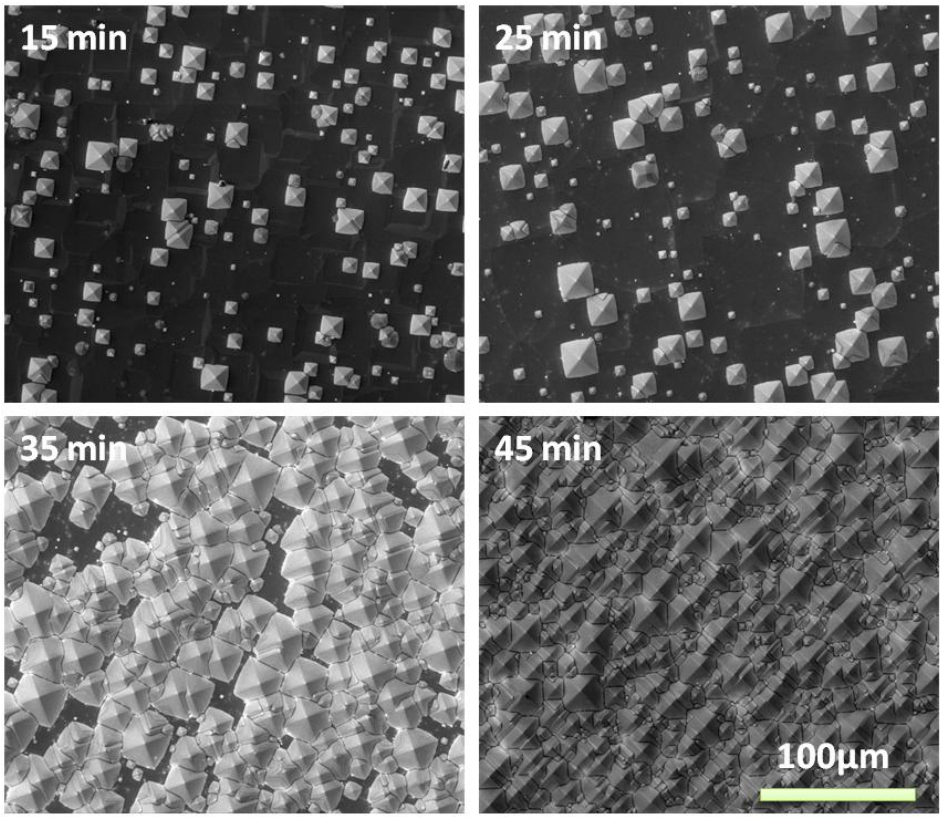


Figure 47: SEM images of textured as-cut wafers with magnetic agitation with a solution consisting of 5.4vol% IPA, 4.2wt% KOH for 15, 25, 35 and 45 min at 75 C

Figure 48 shows the reflection measurement results for SDE wafers. The results show the same trend as that of as-cut wafers. As the process duration increases, reflection decreases. Again the minimum reflection is obtained by 75^{o} C 45 min texturing and it is almost equal to reflection values of as-cut wafer with respective wavelengths.

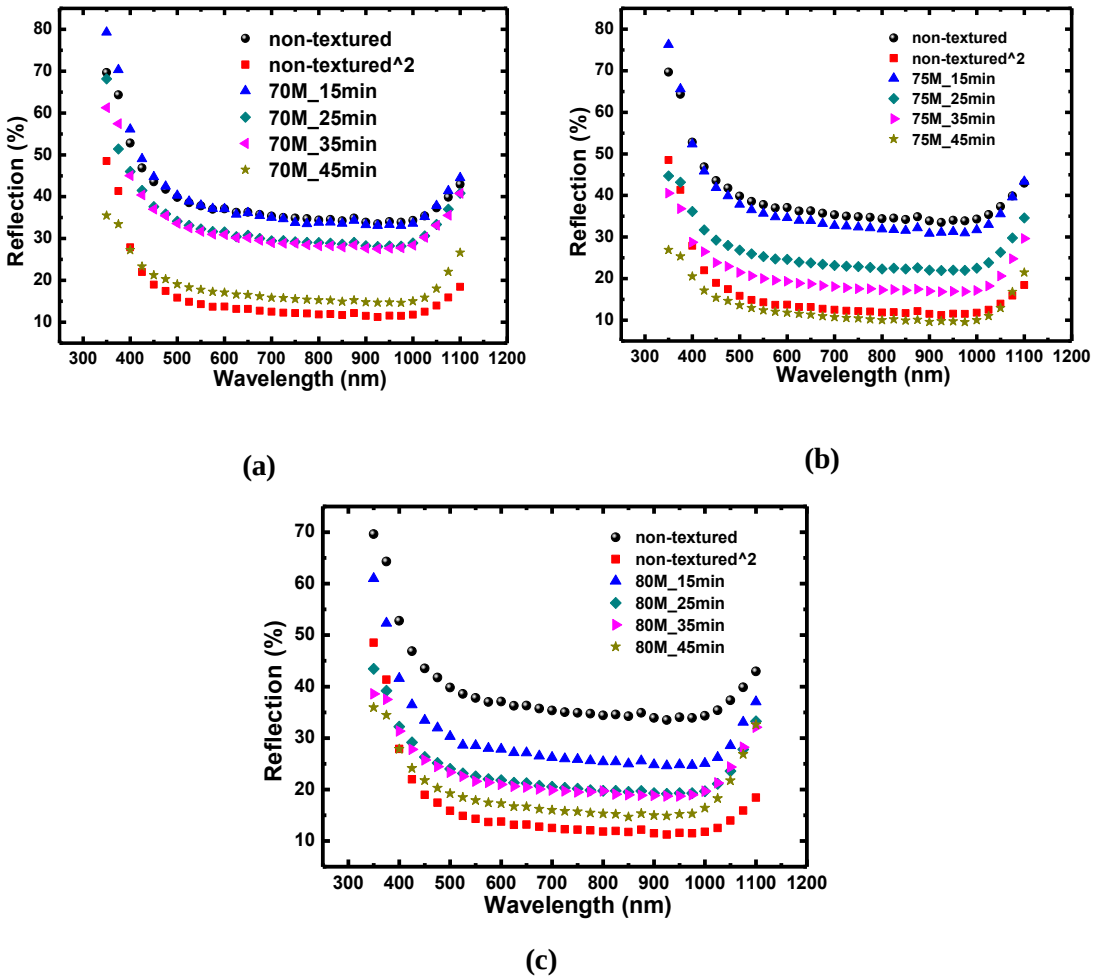


Figure 48: Reflection of textured SDE wafers for process 5.4vol% IPA, 4.2wt% KOH with magnetic agitation at (a) 70° C (b) 75° C (c) 80° C

Figure 49 shows the SEM images of SDE wafers textured at 75° C. Again the area without pyramid decreases by increasing process duration. The pyramid heights are 3 -10 µm for 15 min texturing, 4.5-16 µm for 25 min texturing, 5 -20 µm for 35 min texturing. The pyramid heights also increase with process duration.

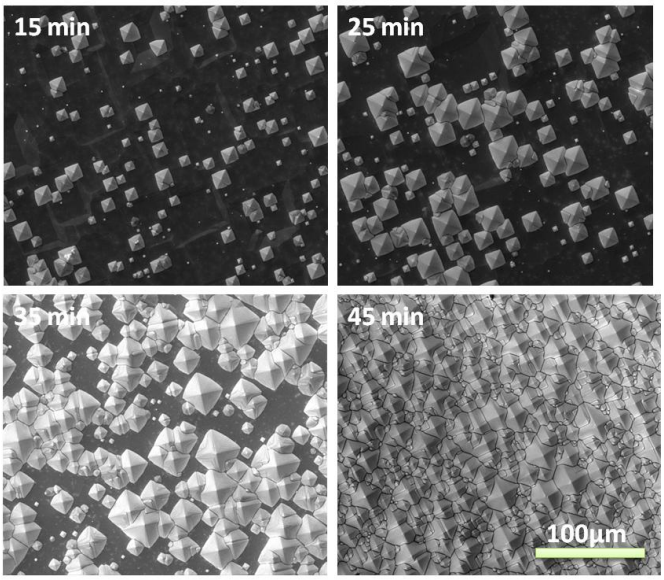


Figure 49: SEM images of textured SDE wafers with magnetic agitation with a solution consisting of 5.4vol% IPA, 4.2wt% KOH for 15, 25, 35 and 45 min at 75 C

5.1.2 Effect of KOH Concentration

To see the effect of KOH concentration, wafers were textured by using concentrations given in Table 2. In these processes, KOH concentration was decreased to 3.33 wt%, and the other parameters were the same as indicated in Table 1.

Table 2: Parameters of three different AS-CUT/SDE wafer texturing processes using chemical solutions based on KOH/IPA/DI-water for magnetic agitation.

Process Name	IPA (vol%)	KOH (wt%)	Temperature (C)	Agitation rate (rpm)	Process Time (min)
70K	5.4	3.33	70	50	15,25, 35,45
75K	5.4	3.33	75	50	15,25, 35,45
80K	5.4	3.33	80	50	15,25, 35,45

Figure 50 shows the reflection measurements of the as-cut wafers. At 70^{o} C, it can be seen that the reflection of 70K process is lower than that of 70M process for all process durations when the Figure 48 (a) and Figure 50 (a) are compared. At 75^{o} C, when the Figure 48 (b) and Figure 50 (b) are compared, reflection for 75K is lower than that of 75 M process for 15, 25, and 35 min process durations. The reflection value for 75K is larger than that of 75M for 45 min process duration, but the difference is almost 1%. At 80^{o} C, the situation is the same as 70K. Therefore, decreasing the KOH concentration to 3.33wt % makes the magnetic agitation more effective for shorter process durations than 45 min.

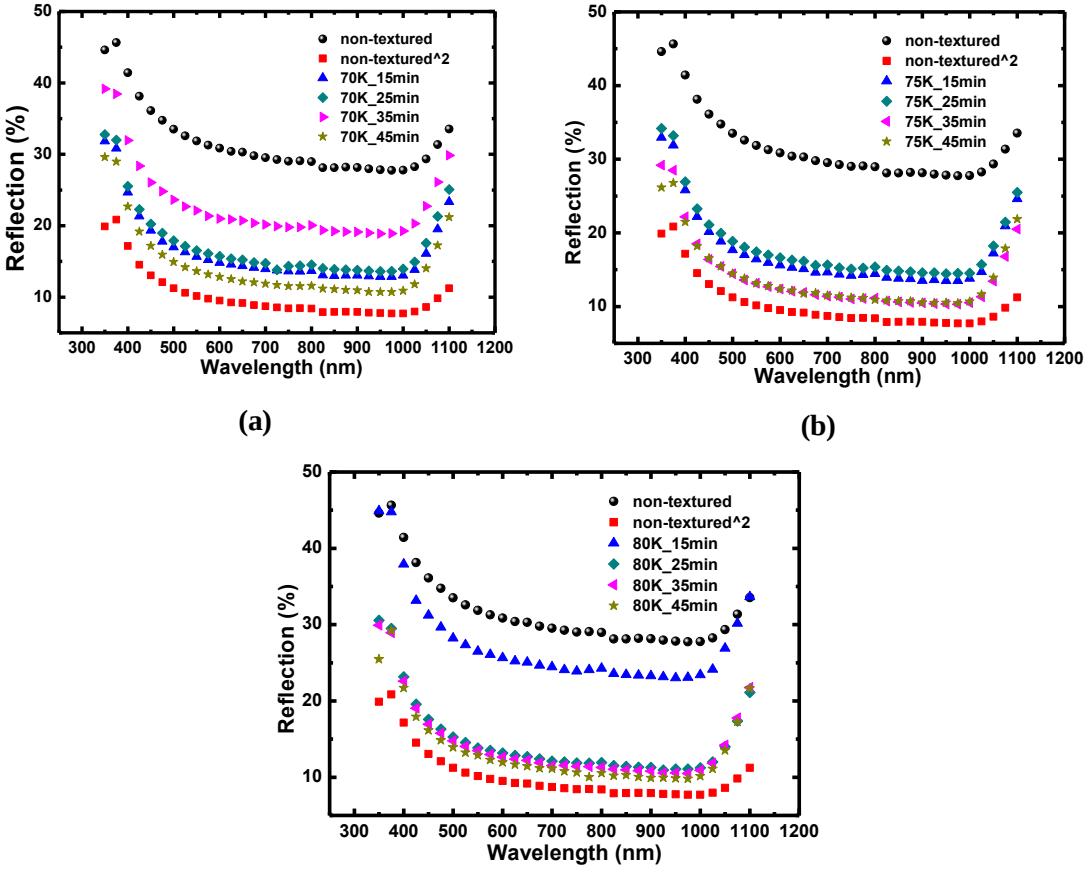


Figure 50: Reflection of textured as-cut wafers for process 5.4vol% IPA, 3.33wt% KOH with magnetic agitation at (a) 70^{o} C (b) 75^{o} C (c) 80^{o} C

Figure 51 shows the SEM images for process 75K. When pyramids heights are compared, 75K pyramid heights are smaller than that of 75M. As process duration increases, area without pyramids decreases as shown in Figure 52 showing area covered by pyramids. From Figure 52 , the area filled by pyramids for 75K process is larger than that of 75M for 15 min, 25 min and 35 min process durations.

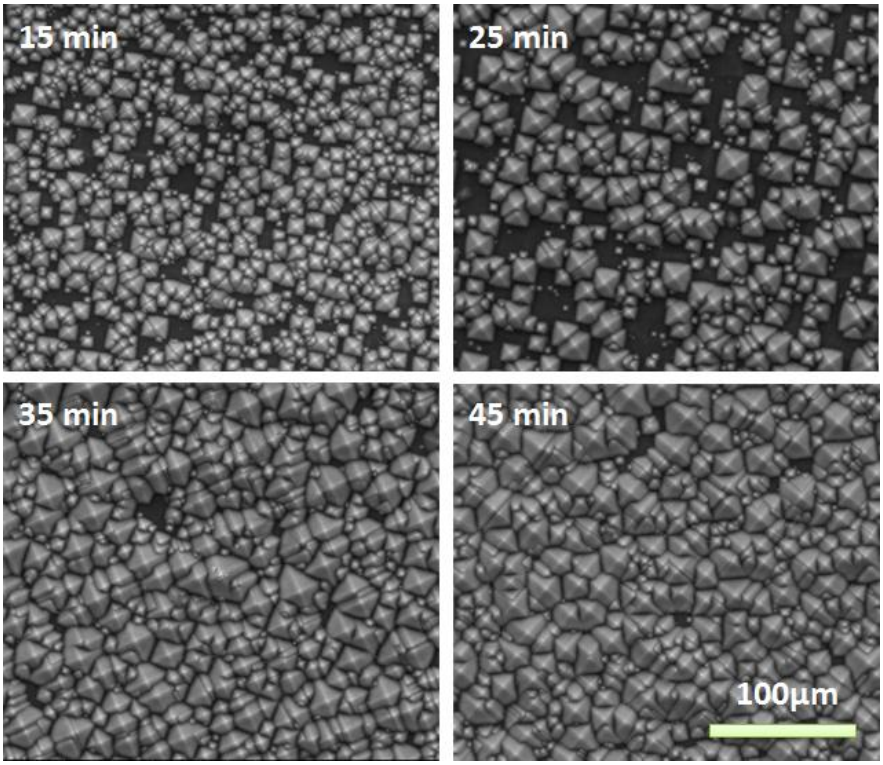


Figure 51: SEM images of textured as-cut wafers with magnetic agitation with a solution consisting of 5.4vol% IPA, 3.33wt% KOH for 15, 25, 35 and 45 min at 75 C

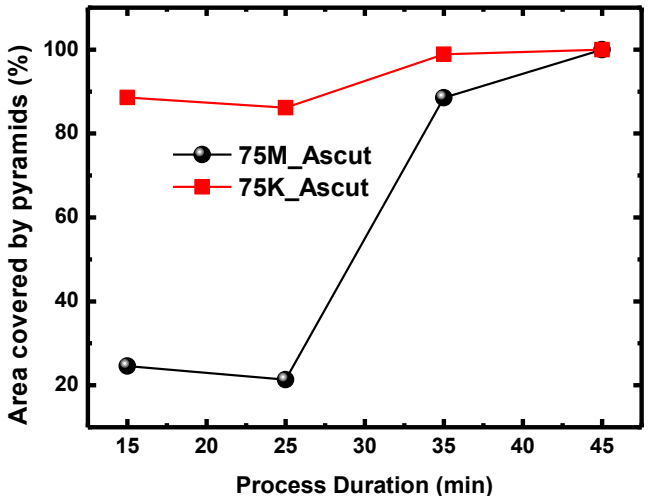


Figure 52: Area covered by pyramids with respect to time and KOH concentration for AS-CUT wafers at 75°C

Figure 53 shows the images of 80M and 80K for 45 min process duration. As can be seen from the figure, although the wafer textured with 4.2wt% KOH is not covered with pyramids fully, the whole surface of the wafer textured with 3.33wt% KOH is covered. From the SEM images, it can be concluded that increasing process duration or temperature is not enough to get fully covered surface, i.e. all components of the etch solution must be optimized.

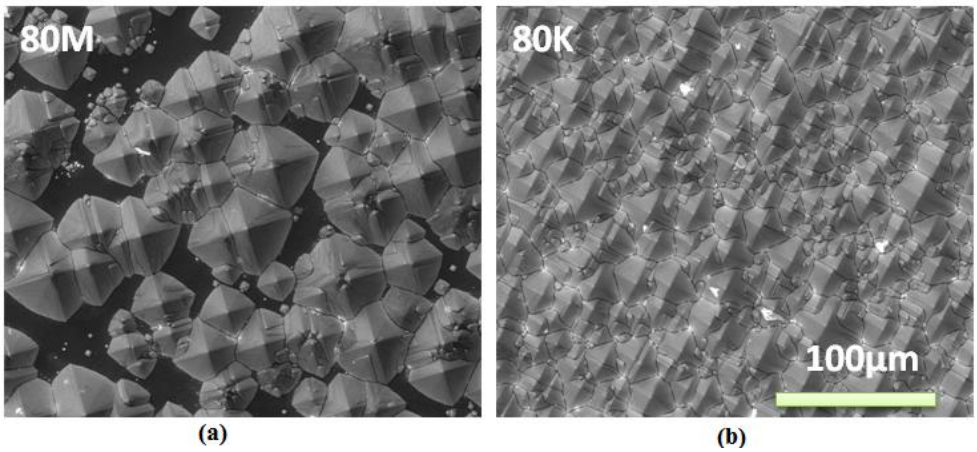


Figure 53: SEM images of samples (a) textured with 5.4wt% KOH (b) textured with 3.33wt% KOH at 80°C

Figure 54 shows the reflection measurements for SDE wafers. When the results are compared, the wafers textured with 4.2wt% KOH have again larger reflection values than the wafers textured with 3.33wt% KOH up to 10% for 15 min, 25 min, and 35 min process durations. For 45 min process duration, the differences are about 2%, 1%, and 5% at 70, 75, and 80^{o}C respectively.

When Figure 50 and Figure 53 are compared, the reflection for as-cut and SDE wafers are different from each other about %2 in average at same process temperature and same process time. It showed that the process with these parameters was less sensitive to surface morphology than the process parameters with 4.2wt% KOH.

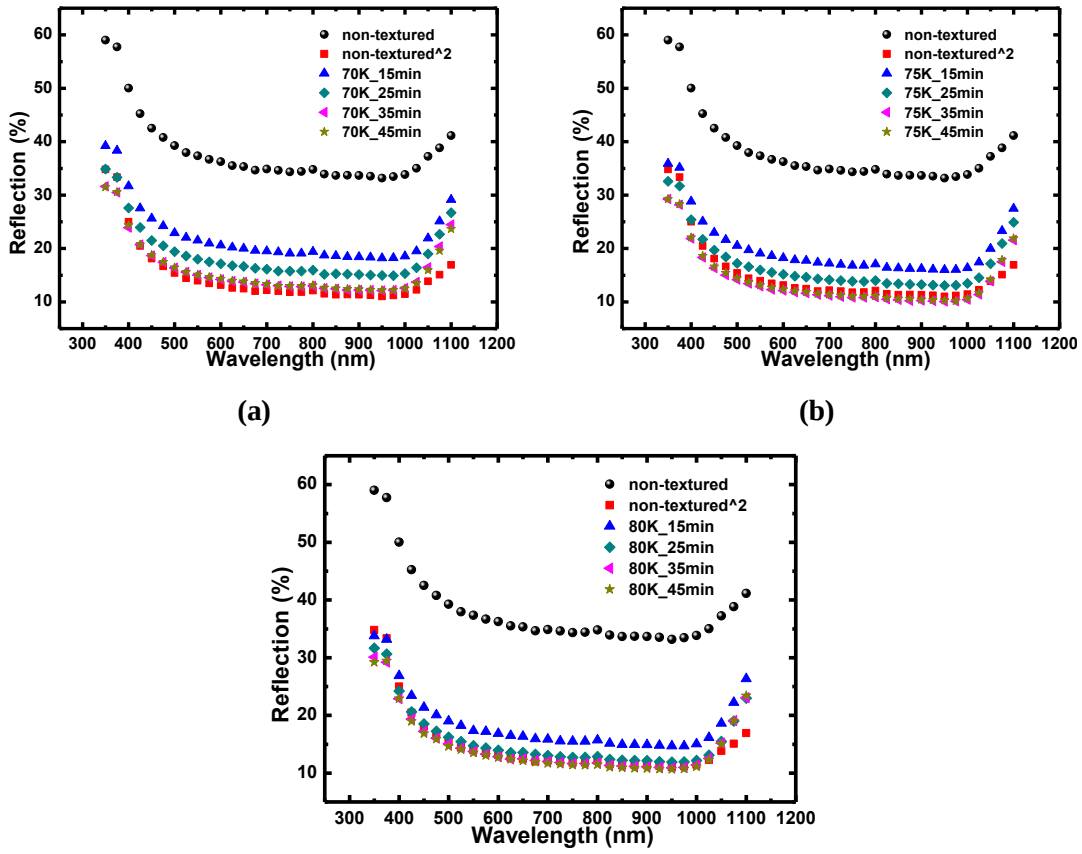


Figure 54: : Reflection of textured SDE wafers for process 5.4vol% IPA, 3.33wt% KOH with magnetic agitation at (a) 70^{o}C (b) 75^{o}C (c) 80^{o}C

Figure 55 and Figure 56 show the SEM images of SDE wafers textured at 75°C and the graph of covered area with respect to time respectively. The wafers textured with 3.33wt % KOH have larger area with pyramids than wafers textured with 4.2wt % KOH have for process durations up to 35 min as can be seen from the figures. For 45 min process time, both are covered fully with pyramids.

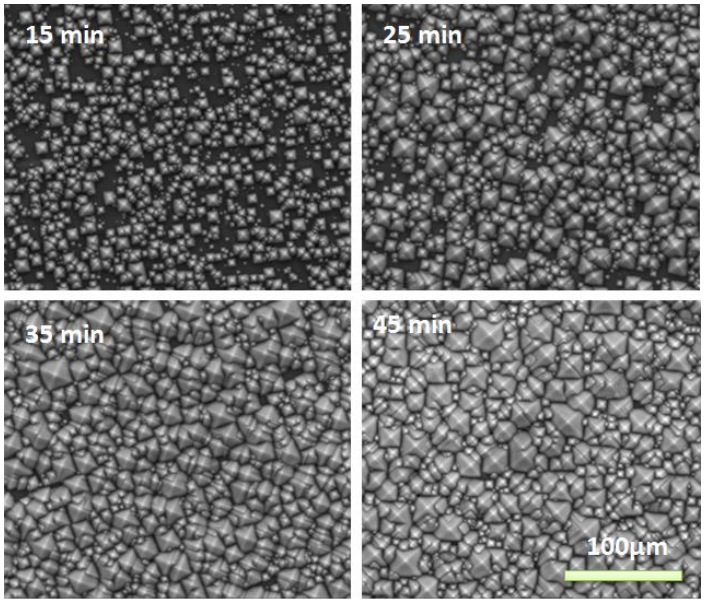


Figure 55: SEM images of textured SDE wafers with magnetic agitation with a solution consisting of 5.4vol% IPA, 3.33wt% KOH for 15, 25, 35 and 45 min at 75°C

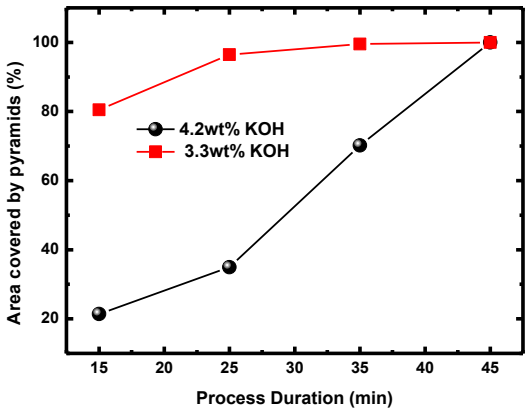


Figure 56: Area covered by pyramids with respect to time and KOH concentration for SDE wafers at 75°C(Lines are just added to guide the eye)

It is realized that both SDE and as-cut wafers textured with magnetic agitation with a solution consisting of 5.4vol% IPA, 3.33wt% KOH have low reflection and large coverage with pyramids for process durations 15 min, 25 min, and 35 min. Figure 57 shows the area covered by pyramids with respect to different process durations and temperatures. As can be seen from the Figure 57, process does not depend on surface morphology very much for the solution with 3.3wt% KOH and the minimum coverage is about 80% for 15min process duration. For the following experiments, KOH concentration was kept constant as 3.33wt%, and the other parameters were changed to get full covered wafers with pyramids.

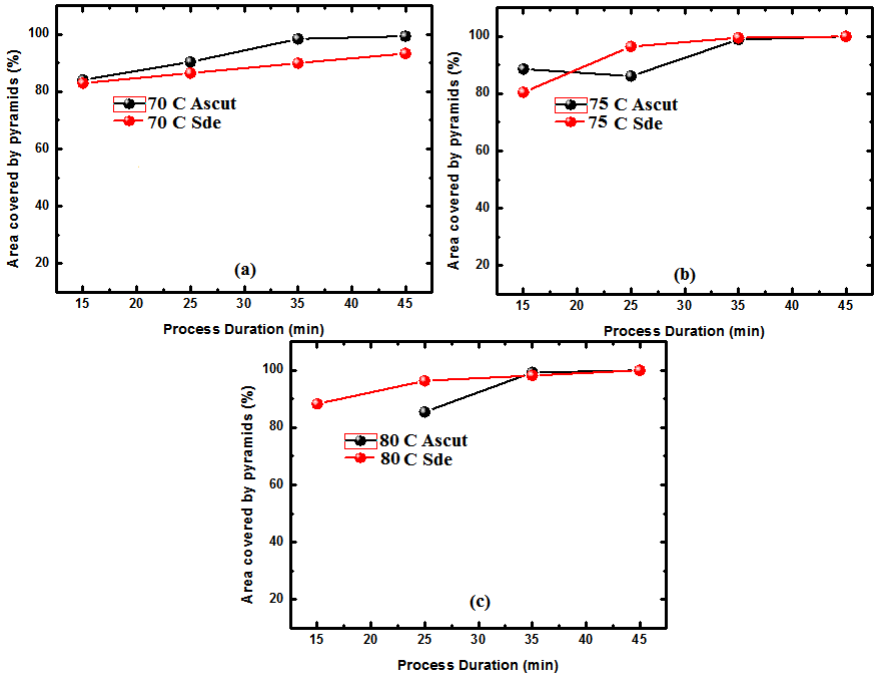


Figure 57: Area covered by pyramids of textured wafers with magnetic agitation with a solution consisting of 5.4vol% IPA, 3.33wt% KOH for 15, 25, 35 and 45 min at (a) 70°C (b) 75°C (c) 80°C

5.1.3 Effect of using a cap to Keep IPA Constant

Closing the beaker increases the pressure on the solution, and the evaporation of water and IPA decreases. This makes the concentrations almost constant during process. To see this effect on process, wafers were textured with parameters given in Table 3.

Table 3: Parameters of two different AS-CUT/SDE wafer texturing processes using chemical solutions to observe effect of using a cap

Process Name	IPA (vol%)	KOH (wt%)	Temperature (C)	Agitation rate (rpm)	Process Time (min)
75MC	5.4	4.2	75	50	25,45
70KC	5.4	3.33	70	50	15,25

Figure 58, Figure 59 and Figure 60 show the reflection results, SEM images of as-cut wafers and SEM images of SDE wafers for processes 75M and 75MC. As can be seen from Figure 58, reflection decreases dramatically for as-cut and SDE wafers, but they are still high. Figure 59 and Figure 60 indicate that coverage with pyramids increases from 21% to 92% for as-cut wafer and from 35% to 82% for SDE wafer. The results show that using cap can decrease reflection or increases coverage for process 75M_25min.

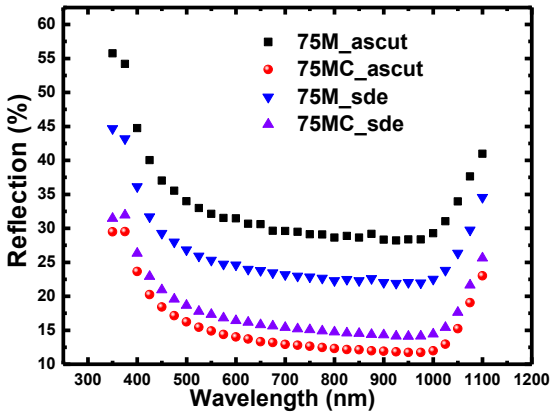


Figure 58: Reflection measurements of wafers textured with a solution consisting of 4.2wt % KOH, 5.4vol % IPA, 25 min at 75°C with and without a cap.

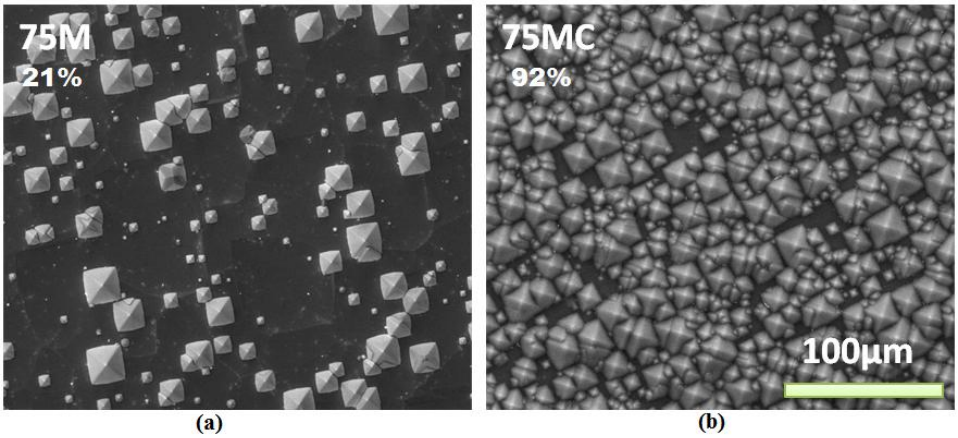


Figure 59: SEM images of as-cut wafers textured with a solution consisting of 5.4vol % IPA, 4.2wt % KOH for 25 min process duration at 75°C a) without cap (coverage 21%) b) with cap (coverage 92%)

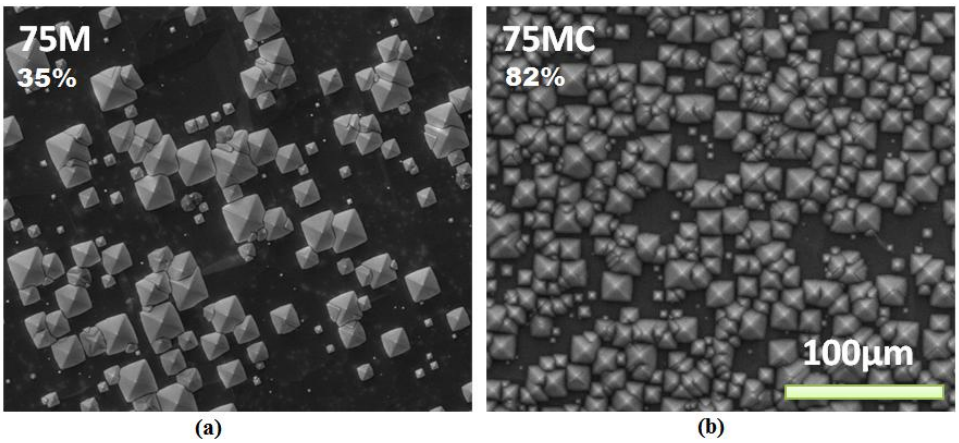


Figure 60: SEM images of SDE wafers textured with a solution consisting of 5.4vol % IPA, 4.2wt % KOH for 25 min process duration at 75°C a) without cap (coverage 35%) b) with cap (coverage 82%)

Figure 61 and Figure 62 show reflection measurements and SEM images of wafers with a solution consisting of 4.2wt % KOH, 5.4vol % IPA, 45 min at 75 C with and without a cap. From Figure 61, using a cap decreases the AM 1.5 weighted reflection about 0.5% for as-cut and 0.8% for SDE wafers. When the images shown in Figure 62 are analyzed, the average pyramid heights and density are 6.74 µm and 1.12×10^4 mm^{-2} for as-cut, 7.5 µm and 0.889×10^4 mm^{-2} for SDE wafers textured

without using a cap. Using a cap decreases the pyramid height to 2.38 µm for SDE and to 2.19 µm for as-cut, and increases pyramid density to $0.883x10^5$ mm^{-2} for SDE and to $1.04x10^5$ mm^{-2} for as-cut.

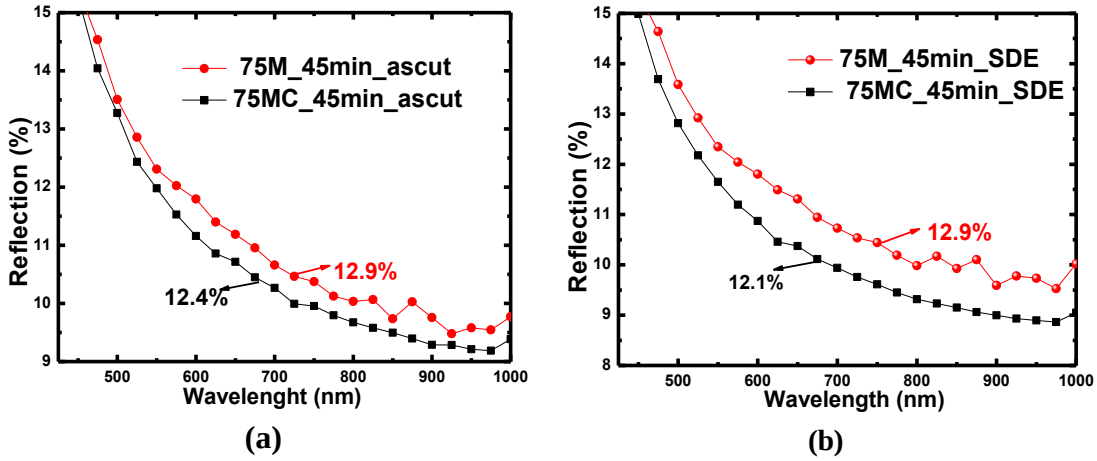


Figure 61: Reflection measurements of wafers textured with a solution consisting of 4.2wt % KOH, 5.4vol % IPA, 45 min at 75°C with and without cap a) as-cut b) SDE

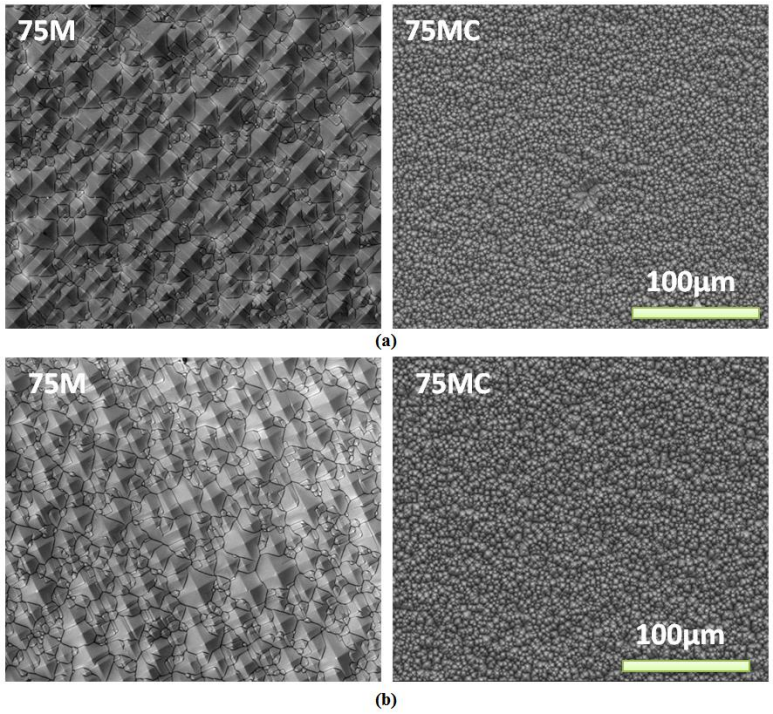
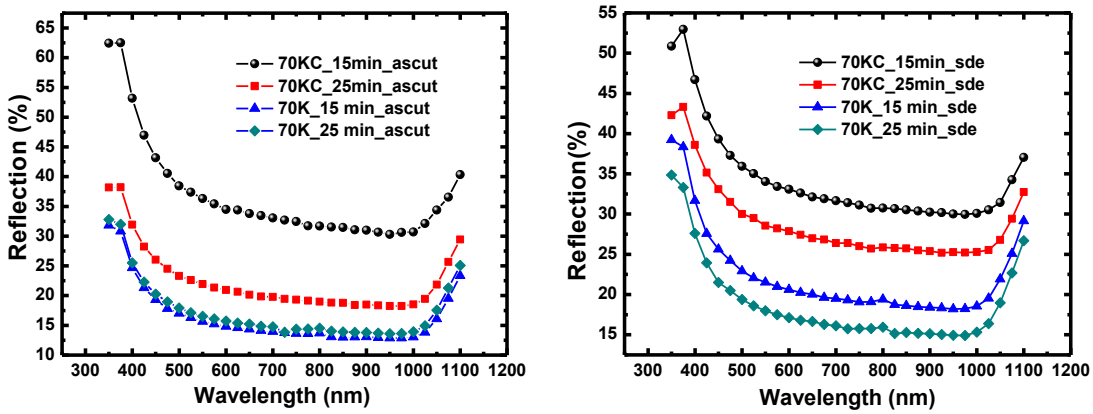


Figure 62: SEM images of wafers textured with a solution consisting of 5.4vol % IPA, 4.2wt % KOH for 45 min process duration at 75°C a) as-cut b) SDE with and without using a cap

Figure 63 shows the reflection measurements of wafers textured with a solution consisting of 3.33wt % KOH, 5.4vol % IPA, 15min and 25 min at 70 C with and without cap. Using a cap increases the reflection very much. Therefore, SEM images of this process were not taken.

These results show that only using a cap is not enough to get fully covered surfaces for short process durations (i.e. like 15 min and 25 min), and small pyramids shows lower reflection than big ones although the difference is not very much. After that point,effects of increasing the speed of magnetic stirring were observed.



(a) **(b)**

Figure 63: Reflection measurements of wafers textured with a solution consisting of 3.33wt % KOH, 5.4vol % IPA, 15min and 25 min at 70°C with and without cap a) as-cut b) SDE

5.1.4 Effect of Magnetic Stirring Speed

To see the effect of magnetic stirring speed, wafers were textured with parameters given in Table 4. These parameters were chosen because previous process 70KC whose parameters given in Table 3 gives high reflection values. The aim was to see whether there would be a recovery in texturing or not.

Table 4: Parameters of the solutions to observe the effect of the magnetic stirring speed

Process Name	IPA (vol%)/ ml	KOH (wt%)	Temperature (C)	Agitation rate (rpm)	Process Time (min)-Wafer Surface
70KCS	5.4	3.33	70	125	15,25-ASCUT 25,35-SDE
75KCS	5.4	3.33	70	125	25,35-SDE

Figure 64 shows the reflection results for process 70KCS as-cut wafers. When the agitation speed was increased to 125 rpm, the reflection decreased. The reflection and the coverage are related as the reflection decreases, coverage increases, so coverage also increases with increasing speed. But the reflection value was higher than the desired one about 10% for 15min and 5% for 25min and wavelengths between 550 and 1000 nm. Therefore I did not put the SEM images of these wafers.

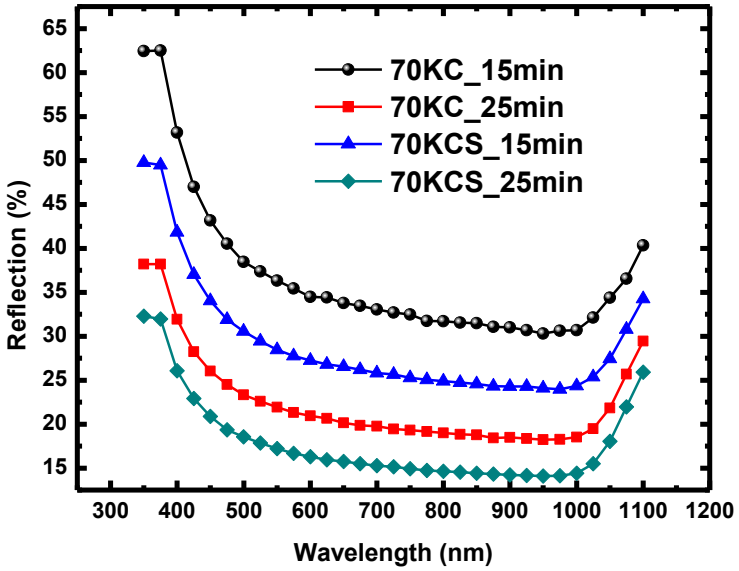


Figure 64: Reflection measurements for as-cut wafers textured with a solution consisting of 3.33wt % KOH, 5.4vol % IPA, 15min and 25 min at 70°C with a speed of 50 and 125 rpm

Figure 65 shows the reflection measurements for SDE wafers textured with solution parameters given above. At 70°C, SDE wafers showed high reflection values for process durations 25min and 35 min, although the process was carried out by using cap and with a high agitation speed. Process was repeated at 75°C with a high agitation speed, and the reflection values decreased to sublimit which is square of reflection of non-texture SDE wafer. Therefore, to get fully textured SDE wafers at short process time with using a cap, minimum temperature should be 75°C.

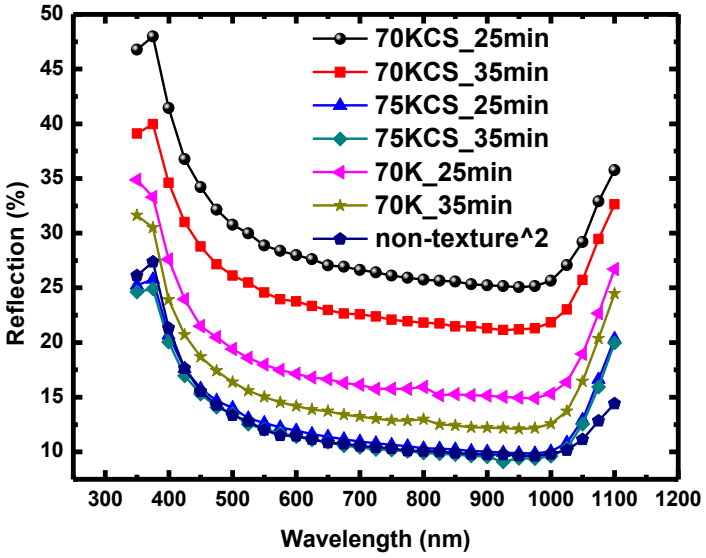


Figure 65: Reflection measurements for SDE wafers textured with a solution consisting of 3.33wt % KOH, 5.4vol % IPA, 25min and 35 min at 70 and 75°C with a speed of 50 rmp and 125 rpm

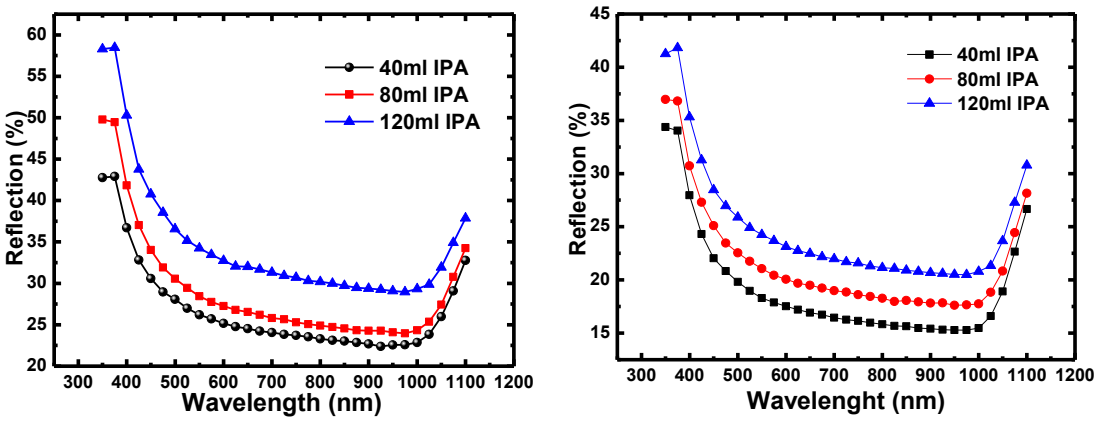
5.1.5 Effect of IPA Concentration

To see the effect of IPA concentration, wafers were textured with parameters given in Table 5. In this experiment, the parameters were 70°C, 3.33wt % KOH, 125 rpm agitation speed, process durations 15 min and 25 min like process parameters of 70K. The differences from 70K were using a cap and the agitation speed. The IPA was added in three different volume 40 ml, 80 ml, and 120 ml.

Table 5: Parameters of three different AS-CUT/SDE wafer texturing processes using chemical solutions to observe effect of IPA concentration

Process Name	IPA (vol%)/ (ml)	KOH (wt%)	Temperature (^{o}C)	Agitation rate (rpm)	Process Time (min)
1I	2.67/40	3.33	70	125	15,25
2I	5.4/80	3.33	70	125	15,25
3I	8/120	3.33	70	125	15,25

Figure 66 shows the reflection measurements of wafers textured with parameters given in Table 5. As can be seen from the figure, as the IPA concentration increases, reflection also increases for 15 min and 25 min process durations. In other words, area with pyramids decreases. Figure 67 shows mass loss of wafers. It can be seen from the figure that increasing IPA decreases the etch rate and mass loss with respective process durations.



(a) **(b)**

Figure 66: Reflection values of as-cut wafers wafers textured with a solution consisting of 3.33wt % KOH, different IPA concentrations a) 15min and b) 25 min at 70^{o}C with a speed of 125 rpm

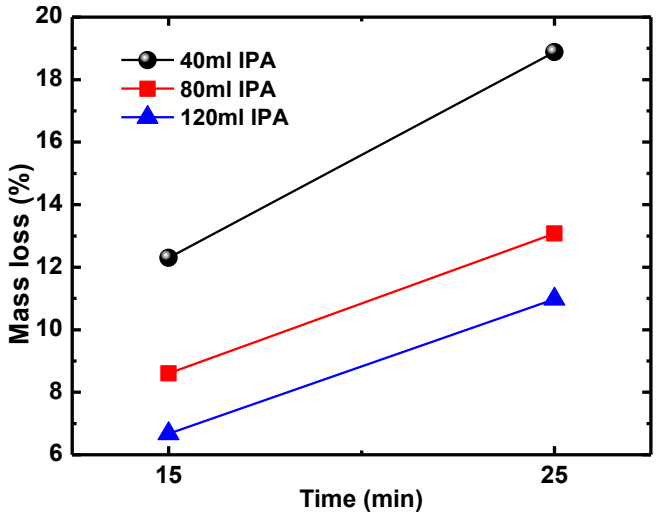


Figure 67: Mass loss with respect to time and changing IPA concentration (Lines are just added to guide the eyes)

Although minimum reflection values were obtained by using 40ml IPA, the following experiments were not done with this amount. We observed that the surface of the wafer after texturing process has some features as shown in Figure 68. This may be due to low IPA concentration causing less wettability of the surface, and H_2 bubbles generated during the etching process may not leave the surface as quickly as possible. That is why these features are not seen the wafers textured with a solution consisting of 80 ml and 120 ml IPA. Therefore, the concentration of IPA was kept as 5.4 vol% for other experiments.

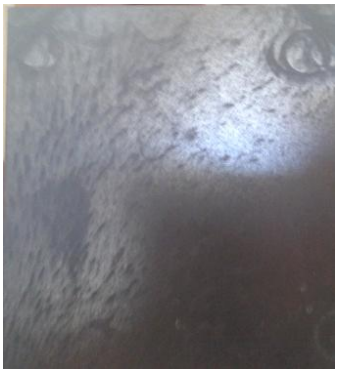


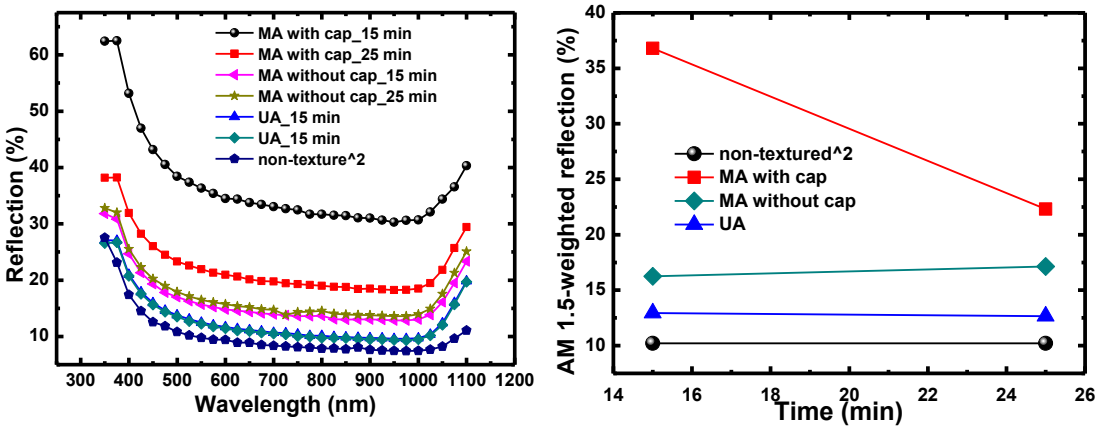
Figure 68: Textured wafer with a solution consisting of 40ml IPA, 3.33wt % KOH, 15 min at 70°C

5.2 Texturing Process with Ultrasonic Agitation

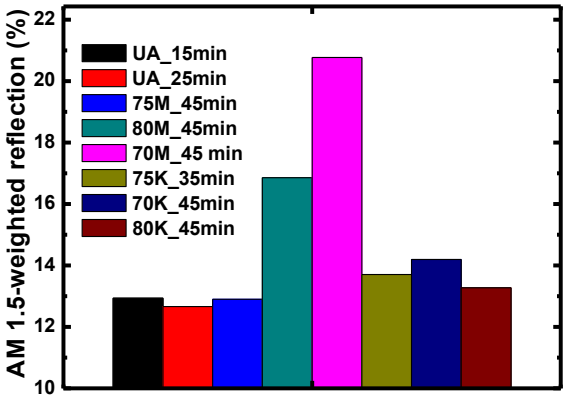
To observe the ultrasonic effect, the caustic etching solutions were prepared as 3.33 wt% KOH, 5.4 vol% IPA at 60^{o}C and 70^{o}C for process durations 15 min, 25 min, 35min, and 45 min.

Firstly, 5x5 cm^{2}, p-type, 1-3 Ω-cm, (100) CZ-Si wafers wafers were textured. The solution was prepared in the glass beaker shown in Figure 33 and stirred by using magnetic agitation and heated up to 70^{o}C. The heated solution was put in big ultrasonic cleaner which was filled by water and heated to 70^{o}C to make the solution temperature stable. The as-cut wafers were textured for process durations 15min and 25 min like process 70K or 70KC.

Figure 69 shows a) reflection values, b) and c) AM 1.5-weighted reflection (AM 1.5-WR) values. When the reflection values and AM 1.5-WR values are compared, there is a dramatic fall in the reflection of textured wafers for process durations 15min and 25 min about 5%, 10% and 20% when compared with process without cap, process 25min , and process 15min with cap respectively, as seen in Figure 69 (a). In Figure 69 (c), the AM 1.5-WR values are almost same except for processes 70M_45min and 80M_45min which were not textured well. Therefore, the ultrasonic agitation provided low reflection values, which were obtained for process duration 45min at process temperature at 75^{o}C or 80^{o}C with magnetic agitation, for process durations 15min and 25min at 70^{o}C.



(a) **(b)**



(c)

Figure 69: (a) Reflection values for textured as-cut wafers with magnetic agitation (MA) and ultrasonic agitation (UA) (b) AM 1.5-weighted reflection (AM 1.5-WR) values (c) Lowest reflection values obtained up to now(Lines are just added to guide the eyes)

The surface of as-cut wafers textured with ultrasonic agitation was fully covered by pyramids for process durations 15min, and 25min. Therefore the SEM pictures were not put here. Figure 70 shows the SEM images in cross sectional view of wafers whose reflection values are lowest ones. As can be seen, the pyramid heights are up to 17 µm for wafers textured with magnetic agitation, and the pyramid heights are up to 4 µm for wafers textured with ultrasonic agitation. Therefore, the

pyramid density of wafers textured with ultrasonic agitation is larger about 4 times than that of wafers textured with magnetic agitation.

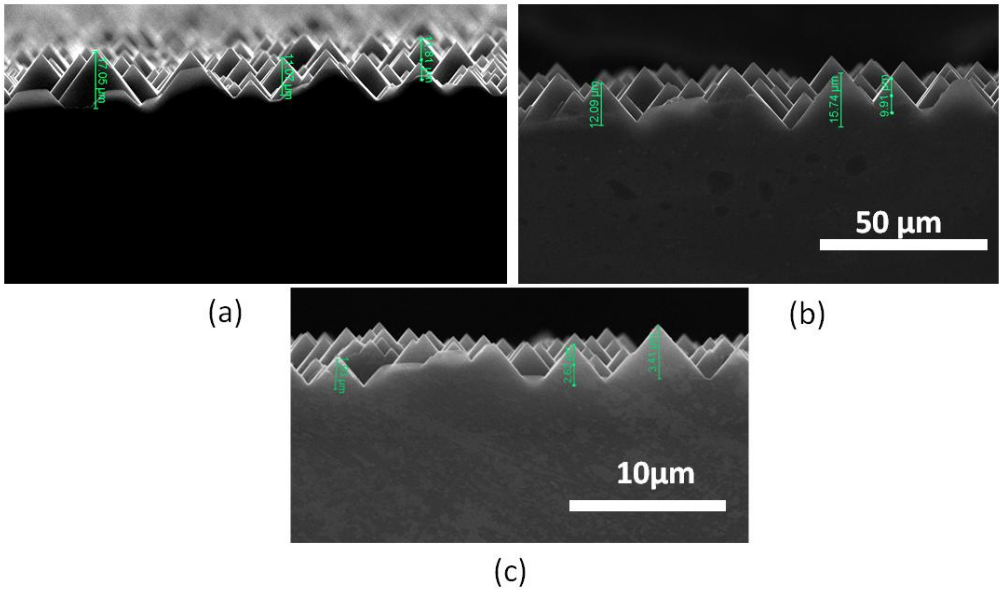


Figure 70: SEM images of a) 75M_45min as-cut wafer b) 80K_45min SDE wafer c) UA_15min as-cut wafer

After that point, ultrasonic texturing processes for process durations 15min and 25min were repeated, and reproducibility of the process was provided. Then, 15.6x15.6 cm^2, p-type, 1-3 Ω-cm, (100) CZ-Si, 25 wafers for each process durations were textured with parameters given in Table 6, by using a cassette. These wafers were used for solar cell production.

Table 6: Parameters of two different AS-CUT wafer texturing processes using chemical solutions

Process Name	IPA (vol%)/ ml	KOH (wt%) / g	Temperature (^oC)	Agitation	Process Time (min)
70UA	5.4/ 427	3.33/266	70	Ultrasonic	15,25,35,45
60UA	5.4/427	3.33/266	60	Ultrasonic	15,25,35,45

Figure 71 shows the reflection measurements and AM 1.5 weighted ones. At 60°C, reflection values decreases sharply from 15 min to 25 min, and 25 min to 35 min. But reflection values decrease slightly at 70°C as texturing time increases.

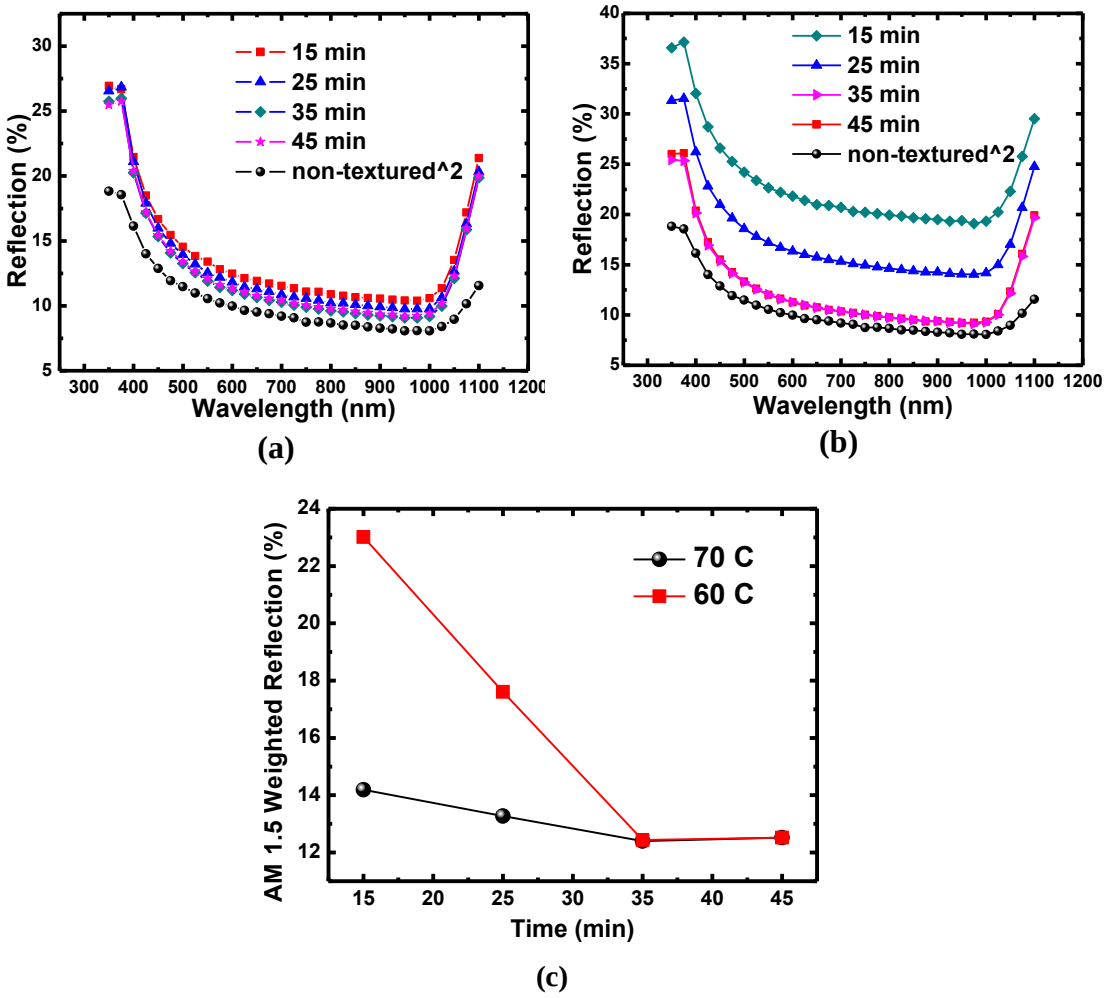


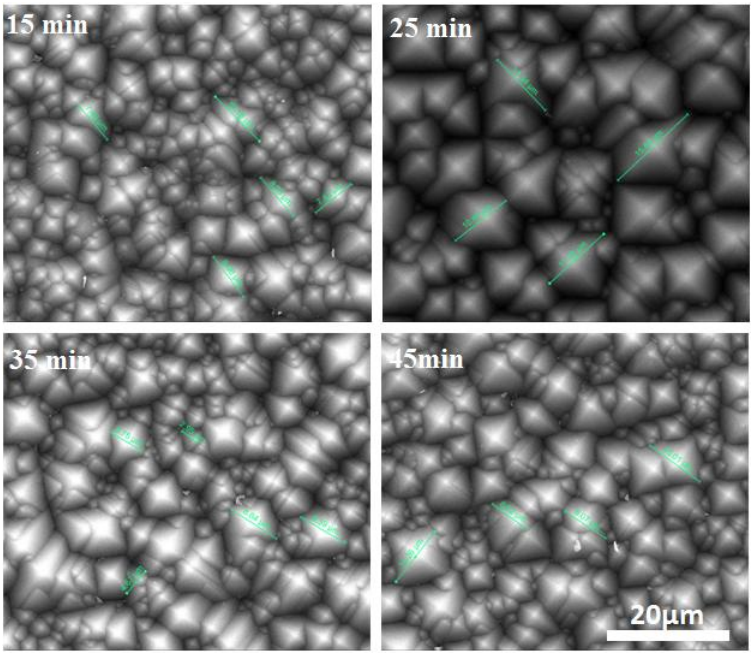
Figure 71: Reflection measurements of as-cut wafers textured by ultrasonic agitation at a) 70°C b) 60°C c) AM 1.5 weighted reflection values (Lines are just added to guide the eyes)

Figure 72 a) shows the surface of wafer textured for 15 min at 70°C. The coverage is inhomogeneous with small pyramids between 0.8-1.5 µm and large pyramids between 3-6µm. Although surface is covered fully, the reflection values is high (see Figure 71) because the pyramids have round tips and corners.

Figure 72 a) shows the SEM image of wafer textured for 25 min at 70°C. The coverage almost homogenous with pyramids heights between 4-7 µm. Due to the homogeneity of pyramids and completed pyramids, the reflection value lower than that of wafer textured for 15 min about 1% (see Figure 71)

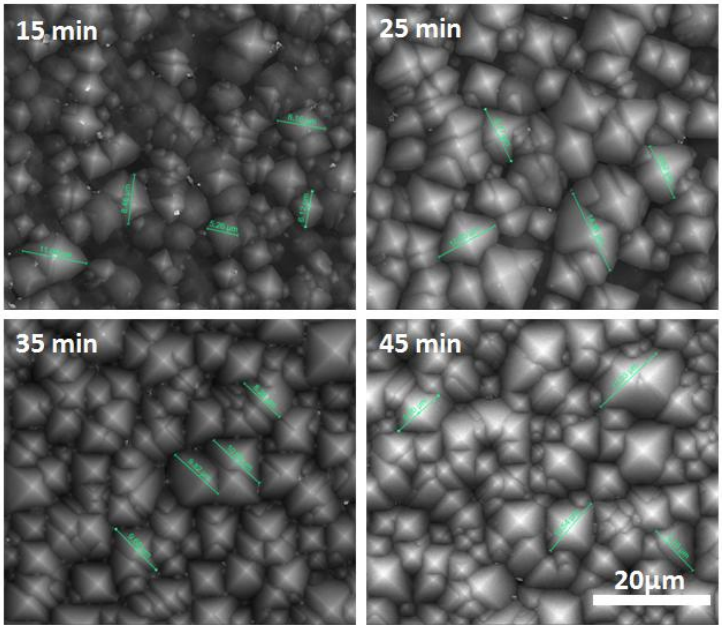
Figure 72 a) shows the SEM images of wafer textured for 35 min and 45 min at 70°C. The distribution of pyramids is almost same and inhomogeneous. There are almost same in amount of large pyramids (4-6 µm) and small pyramids (1.5-3 µm).The reflection values almost same as seen in Figure 71.

Figure 72 b) shows the SEM images of wafer textured for 15min, 25min, 35min and 45min at 60°C. For 15min and 25 min, the surface is covered with pyramids but some of them are not completed, and this makes reflection values higher than that of wafers textured at 70°C (see Figure 71). But the coverage of 25 min process is higher than that of 15 min process. For 35 min and 45 min, surface is fully covered with pyramids. The reflection values are almost same.



(a)

Figure 72: SEM images of as-cut wafers textured by ultrasonic agitation at a) 70°C b) 60°C



(b)

Figure 72: (Continued)

Figure 73 shows a) the average pyramid height, b) pyramid density with respect to time and temperature. The average pyramid heights or pyramid densities of wafers textured for 15 min and 25 min at 60°C are not added because the surface of them is not fully covered (see Figure 72(b)). The pyramid height of 25 min process duration is the highest value at 70°C. While the density increases from 35 min to 45 min process time at 70°C, this value decreases at 60°C.

Figure 73 c) shows the mass loss with respect to time at both process temperatures. The mass loss sharply increases from 15 min to 25 min process durations at 70°C and 60°C. After that point, the amount of etched wafer increases again but the increment of the mass loss decreases as 2% from 25 min to 35 min, 0.6% from 35min to 45 min at 70°C. It shows that number of (111) planes increases and the etch rate decreases. The mass loss at 60°C is lower than the mass loss at 70°C about 2%, and the reflection values of wafers textured for 35 min and 45 min at 70 and 60°C are almost same (see Figure 71). In other words, the lowest reflection

values can be obtained by etching low amount of wafer (about 7%) at 60°C for 35 min process duration.

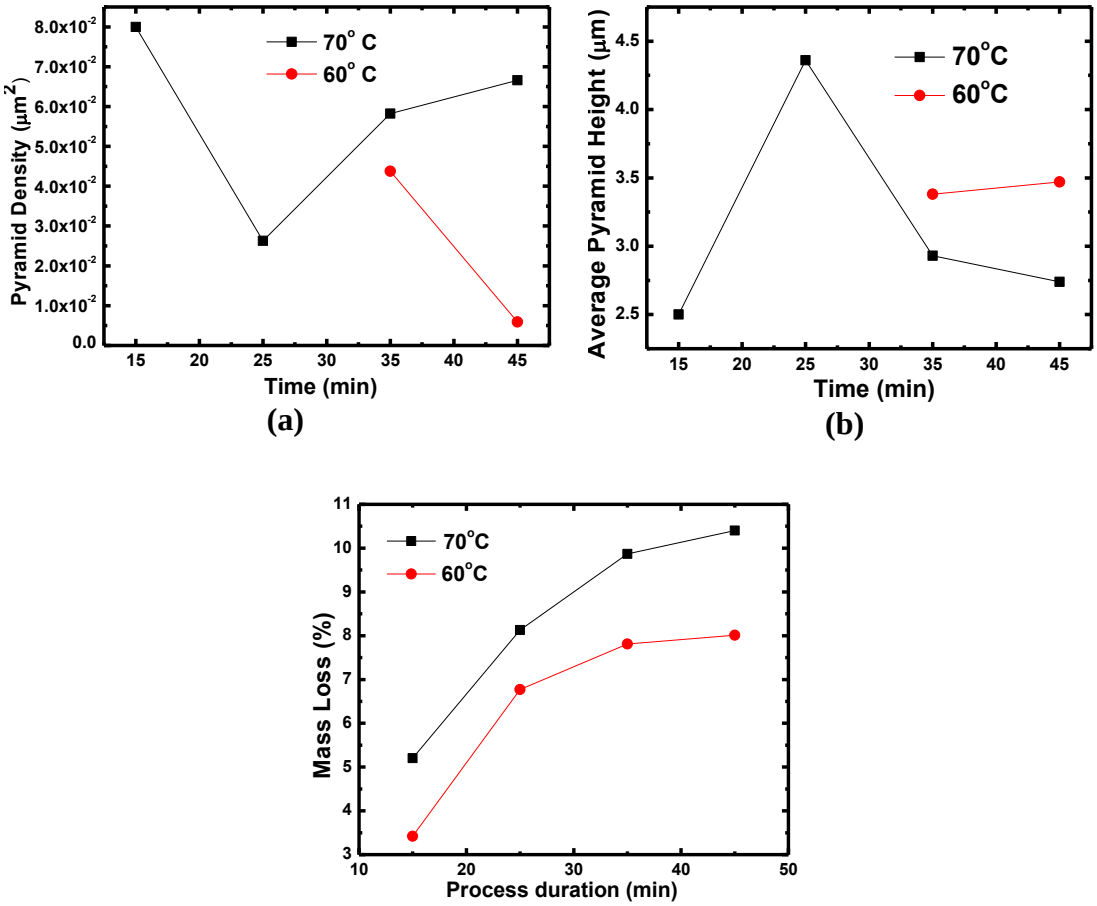


Figure 73: a) Pyramid density b) Average Pyramid height c) Mass loss for as-cut wafers textured with ultrasonic agitation at 70 and 60°C(Lines are just added to guide the eyes)

5.3 Simulation of Light Trapping

To simulate Si wafer light trapping, we used an optical system design (OSD) program (Zemax) and a three dimensional solid element modeling program (Solidworks).

We modeled the wafer textured and non- textured, and put it into the OSD program. Before making simulations, the absorption and refractive index of mono-Si data is implemented to produce a glass type acting like mono-Si into the OSD

program. The data is taken from PVCDROM and Table 7 shows these values from 250 nm to 1100 nm [41].

Table 7: Absorption coefficient and refractive index values of mono-Si

Wavelength (nm)	Absorption Coefficient (cm^{-1})	n (Refractive Index)	Wavelength (nm)	Absorption Coefficient (cm^{-1})	n (Refractive Index)
350	1.04E+06	5.483	730	1.54E+03	3.741
360	1.02E+06	6.014	740	1.42E+03	3.732
370	6.97E+05	6.863	750	1.30E+03	3.723
380	2.93E+05	6.548	760	1.19E+03	3.714
390	1.50E+05	5.976	770	1.10E+03	3.705
400	9.52E+04	5.587	780	1.01E+03	3.696
410	6.74E+04	5.305	790	9.28E+02	3.688
420	5.00E+04	5.091	800	8.50E+02	3.681
430	3.92E+04	4.925	810	7.75E+02	3.674
440	3.11E+04	4.793	820	7.07E+02	3.668
450	2.55E+04	4.676	830	6.47E+02	3.662
460	2.10E+04	4.577	840	5.91E+02	3.656
470	1.72E+04	4.491	850	5.35E+02	3.65
480	1.48E+04	4.416	860	4.80E+02	3.644
490	1.27E+04	4.348	870	4.32E+02	3.638
500	1.11E+04	4.293	880	3.83E+02	3.632
510	9.70E+03	4.239	890	3.43E+02	3.626
520	8.80E+03	4.192	900	3.06E+02	3.62
530	7.85E+03	4.15	910	2.72E+02	3.614
540	7.05E+03	4.11	920	2.40E+02	3.608
550	6.39E+03	4.077	930	2.10E+02	3.602
560	5.78E+03	4.044	940	1.83E+02	3.597
570	5.32E+03	4.015	950	1.57E+02	3.592
580	4.88E+03	3.986	960	1.34E+02	3.587
590	4.49E+03	3.962	970	1.14E+02	3.582
600	4.14E+03	3.939	980	9.59E+01	3.578
610	3.81E+03	3.916	990	7.92E+01	3.574
620	3.52E+03	3.895	1000	6.40E+01	3.57
630	3.27E+03	3.879	1010	5.11E+01	3.566
640	3.04E+03	3.861	1020	3.99E+01	3.563
650	2.81E+03	3.844	1030	3.02E+01	3.56
660	2.58E+03	3.83	1040	2.26E+01	3.557
660	2.58E+03	3.83	1050	1.63E+01	3.554
670	2.38E+03	3.815	1060	1.11E+01	3.551
680	2.21E+03	3.8	1070	8.00E+00	3.548
690	2.05E+03	3.787	1080	6.20E+00	3.546
700	1.90E+03	3.774	1090	4.70E+00	3.544
710	1.77E+03	3.762	1100	3.50E+00	3.541
720	1.66E+03	3.751			

5.3.1 Simulation of SDE wafer

Figure 74 shows the model of simulation. In this model, there are two rectangle detectors in front and back of the wafer, one rectangle source and a SDE wafer. By using this model, reflection detected light intensity by front detector, transmission detected light intensity by back detector, and absorption, which is obtained by subtracting addition of reflection and transmission from one hundred, can be obtained. The wafer thickness is taken as 160 µm because wafers are etched about 10 µm per side to remove the saw damages, and the wafers used in our laboratory have thickness about 180 µm.

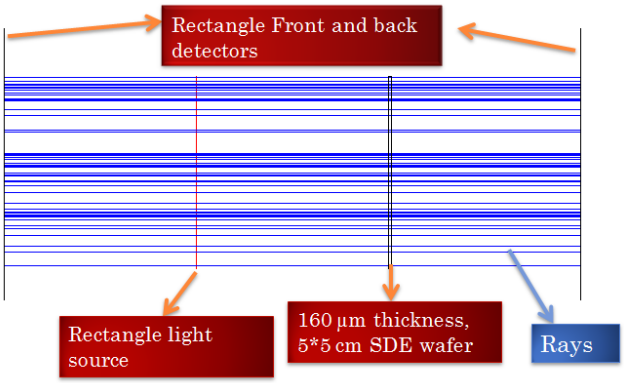


Figure 74: Model of SDE wafer reflection simulation

Figure 75 a) shows the measured reflection value and simulation result of SDE wafer. As can be seen, the reflection values of simulation is different from measured ones about 9% for 350 nm and 375 nm, about 2% between 400 nm and 1025 nm, and the difference is about 4% between 1050 nm and 1100 nm. Our measurements have an error about 1 %, so the values of simulation obtained between 400nm and 1025 nm differs about 1% from measured reflection values.

Figure 75 shows a) reflection, b) transmission, and c) absorption of light for wafer thickness of 2, 4, 8, 20, 100, and 180 µm. The reflection, transmission and absorption values of 350 nm and 500 nm are constant as the thickness increases. It

means that for these wavelengths wafer thickness equal and higher than 2 μm is enough for absorption of light entering the wafer.

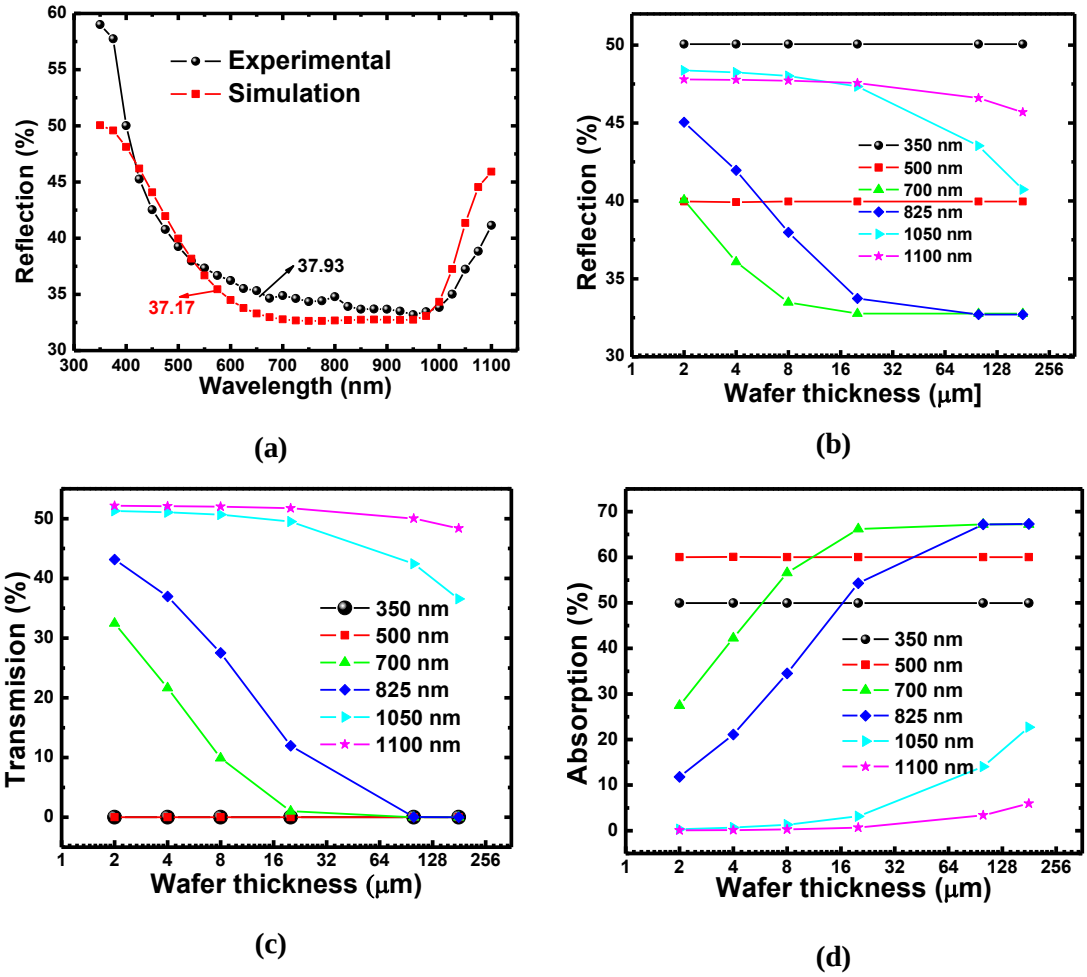


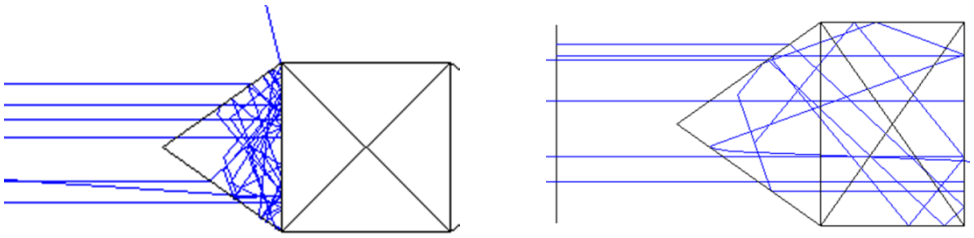
Figure 75: a) Reflection data b) Reflection c) Transmission d) Absorption with respect to changing thickness (Lines are just added to guide the eyes)

For wavelengths 700 nm and so on, the reflection values decreases as the thickness increases. It shows that reflection is not due to front reflection, but also due to light reflected from back surface of the wafer. To obtain zero transmission, the thickness must be at least 20 μm for 700 nm, 100 μm for 825 nm, and the thickness must be higher than 2 mm and 8 mm, which are not shown, for 1050 and 1100 nm respectively.

5.3.2 Simulation of Wafer with Uniformly Distributed Pyramids

First of all, the aim was to simulate random pyramids but we faced with a problem. The problem is that when one pyramid is put on a rectangle volume, the

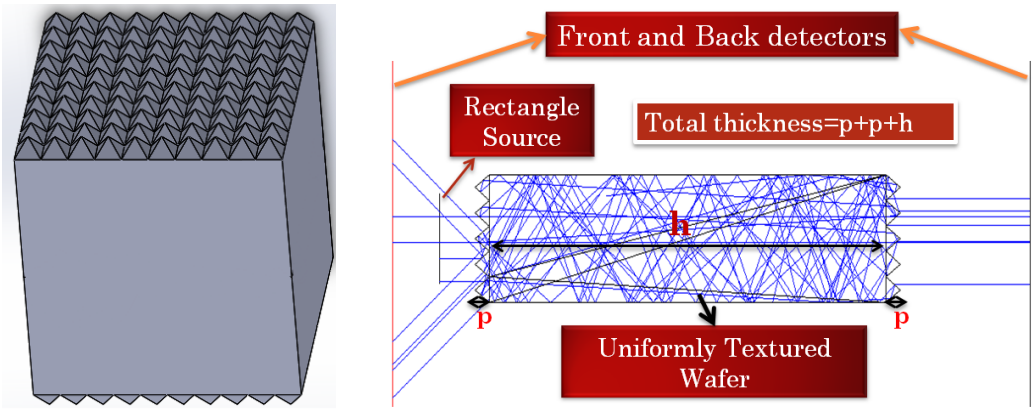
OSD program perceives as there are a pyramid, air, and a rectangle volume. Therefore, light passing through the pyramid is reflected back without entering the rectangle volume. The situation is illustrated in Figure 76 (a). Figure 76 (b) shows the working model.



(a) (b)

Figure 76: Simulation of textured wafer obtained by a) assembling one pyramid on a rectangle volume b) cutting the a part of rectangle volume

The problem was not solved. Therefore, we modeled a wafer surface with uniformly distributed pyramids as shown in Figure 77 (a). The simulation model is shown in Figure 77 (b). Here, there is a uniformly textured wafer model instead of SDE wafer model (see Figure 74) .

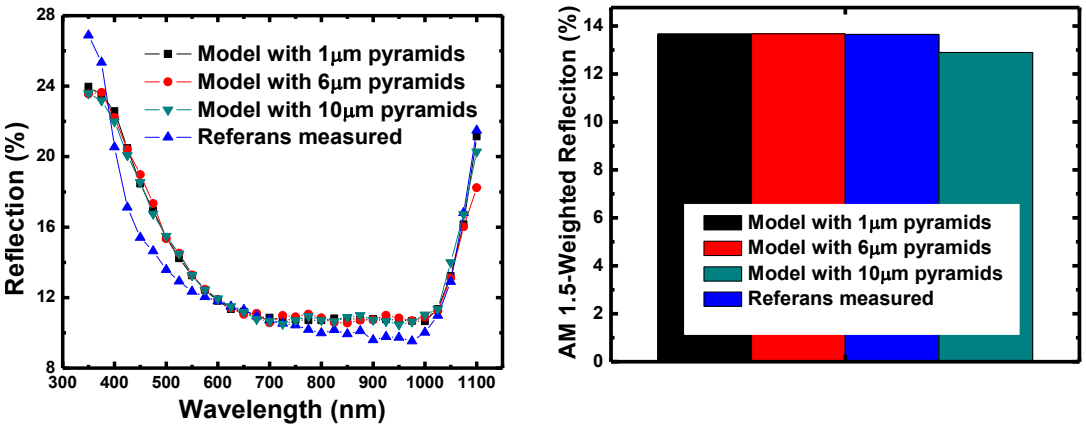


(a) (b)

Figure 77: a) Uniformly textured wafer model b) Simulation model

In the simulations, the total thickness is kept as constant, and it is equal to sum of heights of front and back pyramids, bare wafer thickness as shown in Figure 77 (b). Figure 78 shows reflection values of reference wafer (randomly textured with

average pyramid height 7.5 µm), and model with 1, 6, 10 µm pyramids. From the figure, the AM 1.5-weighted reflection values of models are higher than reference about 1%. Although Zemax does calculations by using geometric optic, there are small differences for wavelength higher than 1050 nm as shown in figure. This is due to the fluctuations in reflected light from back surface of the wafer for these wavelengths.



(a) **(b)**

Figure 78: a)Reflection values for model with 1,6,10 µm pyramids b) AM 1.5-Weighted Reflection

In addition, two side textured wafers with 6 µm pyramid heights and different total thicknesses were simulated. The absorption result is shown in Figure 79. From the figure, the absorption decrease with decrease in thickness between 925 nm and 1100 nm, and the absorption values are same between 350 nm and 925 nm.

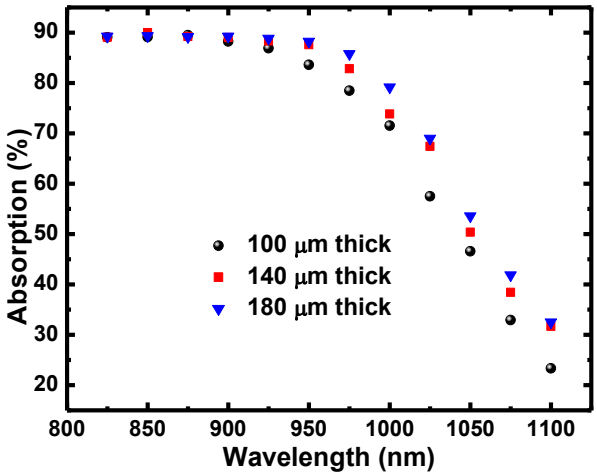


Figure 79: Absorption graph of two side textured wafer with 6 µm pyramid height

We also simulated one side textured wafers with different total thicknesses and different pyramid heights. Thicknesses higher than 180 µm were not taken, because it will be not cost effective and nowadays trend is production of solar cells with thin wafers.

Table 8: Parameters of models

Model Name	Total Thickness (µm)	Pyramid Heights (µm)
100_1side	100	1-6-10
140_1sdie	140	1-6-10
180_1side	180	1-6-10

Figure 80 shows the absorption values for wafers with different pyramid sizes and thicknesses. The wavelength is taken from 950nm to 1100nm, because the absorption values almost same up to 950 nm.

In Figure 80 (a), one side textured wafers have higher absorption than two side textured. Because total reflection probability of light passing through the wafer and facing with flat surface is higher than that of light facing with surface with pyramids as shown in Figure 77 (b) Figure 81.

As can be seen from Figure 80 (b)- (c)- (d), increasing thickness increases the absorption for the same pyramid sizes. When thickness is constant and the pyramid sizes are changed, the absorption values increases with increasing pyramid sizes after 1025 nm.

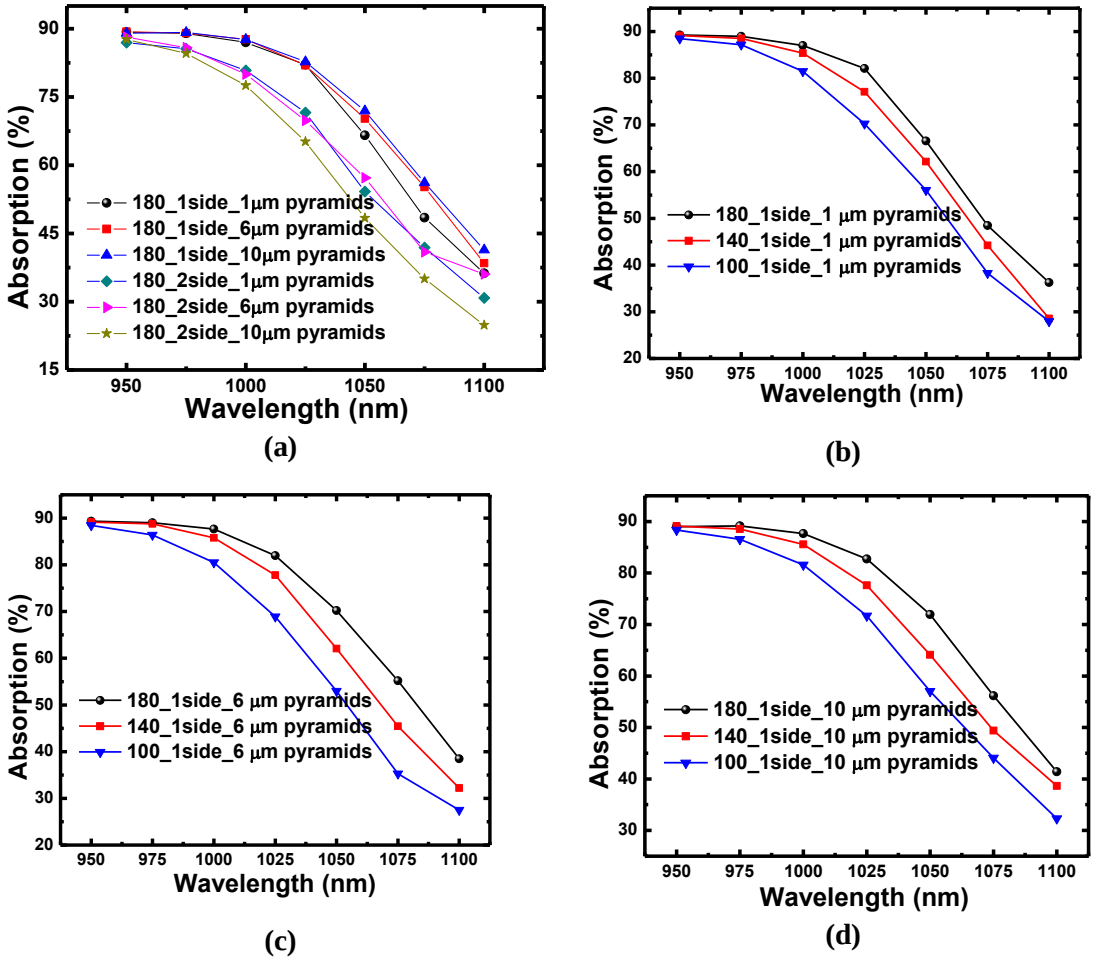


Figure 80: Absorption of a) one side and two side textured wafer, b)one side wafer with 1 μm pyramids, c) one side wafer with 6 μm pyramids d) one side wafer with 10 μm pyramids

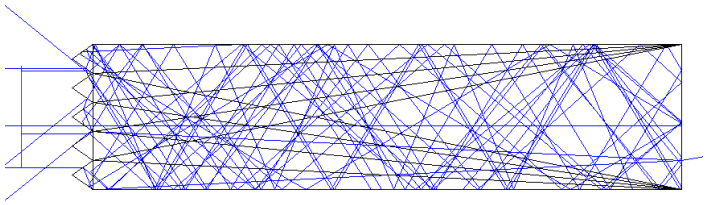


Figure 81: Model of a wafer with one side texturing

5.4 Solar Cell Results

Screen printed Cz silicon solar cells with dimensions 15.6x15.6 cm^2 were produced. The wafers of cells were 70UA and 60UA whose parameters were given in Table 9. For each texture parameter, 10 wafers were used (total 90 wafers) to produce solar cells. To get optimum SiN_x layer, each set was divided into groups with 5 wafers, and average values were taken from one of these groups. The reference cell was the standard cell produced in GÜNAM laboratory.

Table 9: I-V measurement results by Solar Simulator

	Texture Temperature (^oC)	Time of texturing (min)	Average Jsc (mA)	Average Voc (V)	Average FF (%)	Average Efficiency (%)	Average Series (mΩ)
70UA	70	15	34.612	0.623	79.715	17.204	6.91
	70	25	34.648	0.623	79.717	17.218	6.89
	70	35	35.686	0.623	78.996	17.587	7.17
	70	45	35.687	0.623	79.051	17.601	7.16
60UA	60	15	33.651	0.62	79.535	16.734	7.14
	60	25	34.71	0.625	79.546	17.264	7.01
	60	35	34.453	0.622	79.744	17.235	6.91
	60	45	35.617	0.623	79.314	17.608	6.94
Reference	75	45	34.434	0.619	79.659	16.989	6.84

Table 9 shows the I-V measurement results by Solar Simulator. Figure 82 shows the related curves. Average J_{sc} increases as process duration increases at different temperatures. And the J_{sc} of reference is lower than the average J_{sc} of the cells textured with ultrasonic agitation. In Figure 82 (b), reference has the lowest V_{oc} and the cells textured for 10 min at 70^{o}C have the highest value about 626 mV. The others have almost same average V_{oc} values about 623 mV except for 15 min texturing at 60^{o}C. In Figure 82 (c), fill factor values are about 79%. Figure 82 (d) shows all the efficiencies with respect to all J_{sc} values of 100 cells. As can be seen, efficiency is almost linearly proportional to J_{sc}, and the highest efficiency is 17.737%

of cell textured for 45min at 60°C and the related I-V curve is shown in Figure 82 (f). Average cell efficiency of reference is the lowest one when compared with the others except for cell textured for 15 min at 60°C as shown in the figure (e). Average cell efficiency increases with increase in process duration at different process temperature.

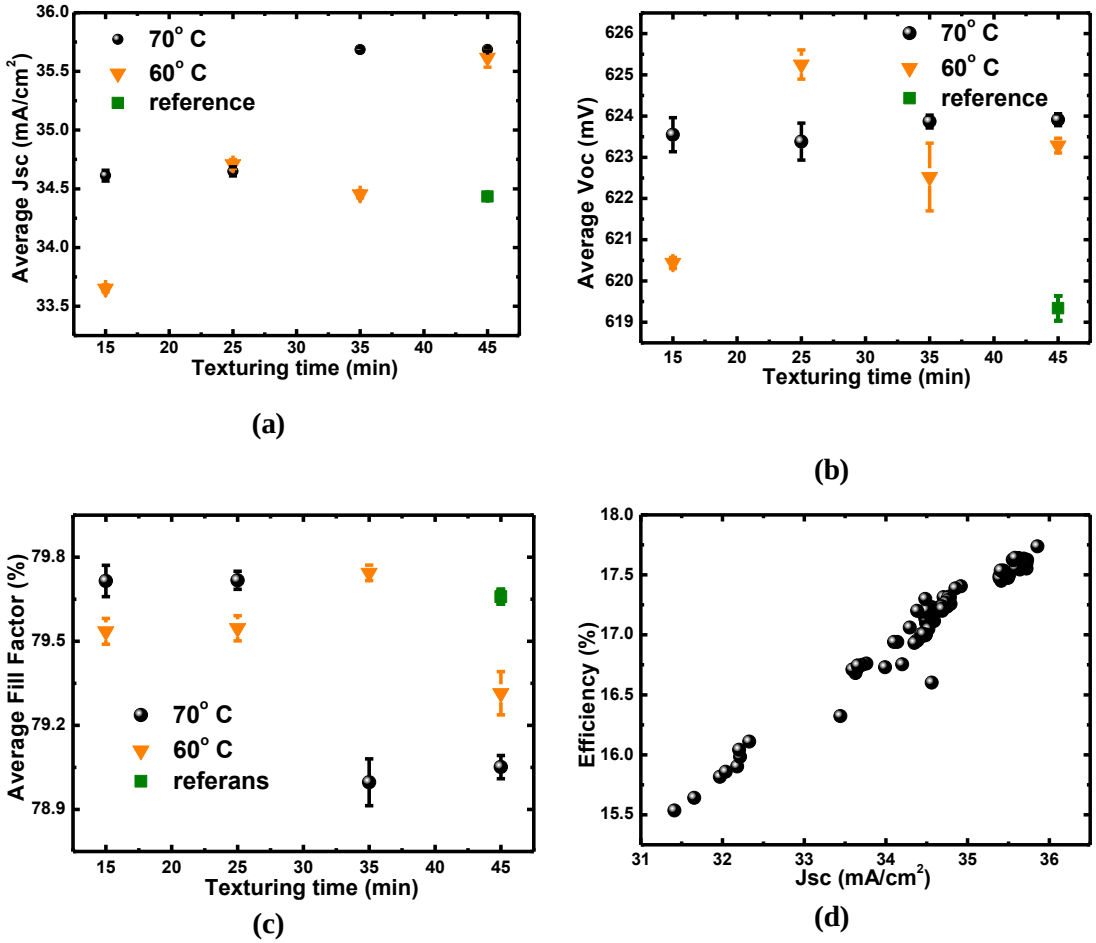


Figure 83: Graphs of Average a) Jsc b) Voc c) Fill factor e) Efficiency with respect to texturing time d) Efficiency- Jsc, f) I-V curve of best cell

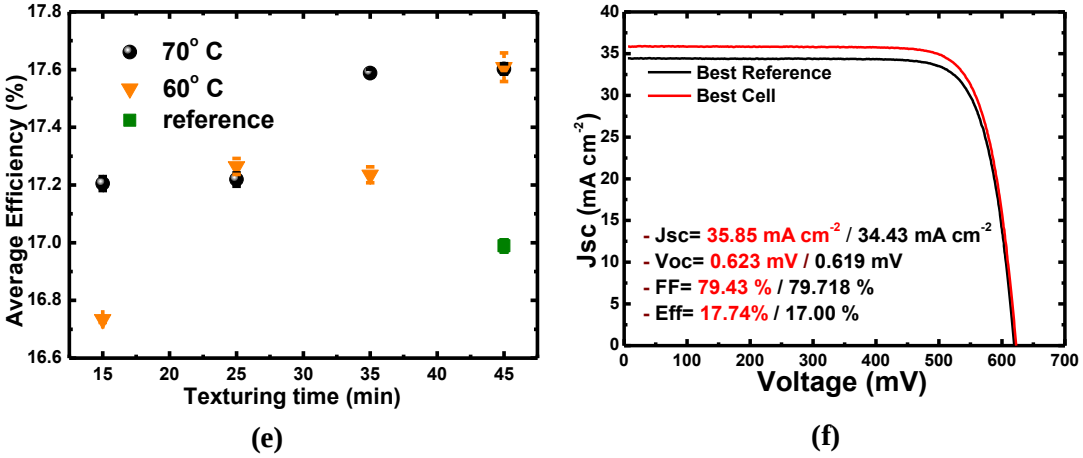


Figure 82: (Continued)

Figure 83 shows the mass loss and the J_{sc} values with changing texturing time. As the mass loss increases with increase in process duration, J_{sc} increases. One can expected that Jsc of thick wafer should be higher than that of thin wafer for same reflection values for wafers without ARC. Because the absorption increases when thickness is increased (see Figure 79). In our case, wafers textured for 35 min and 45 min at 60°C are thicker than wafers textured for 35 min and 45 min at 70°C. But the J_{sc} values are almost same. It is because the mass loss is too low to observe such a change in J_{sc}. In Figure 79, mass loss about 22% (i.e. 140 µm thickness) decreases the absorption about 2%, but in our case maximum mass loss is about 10%.

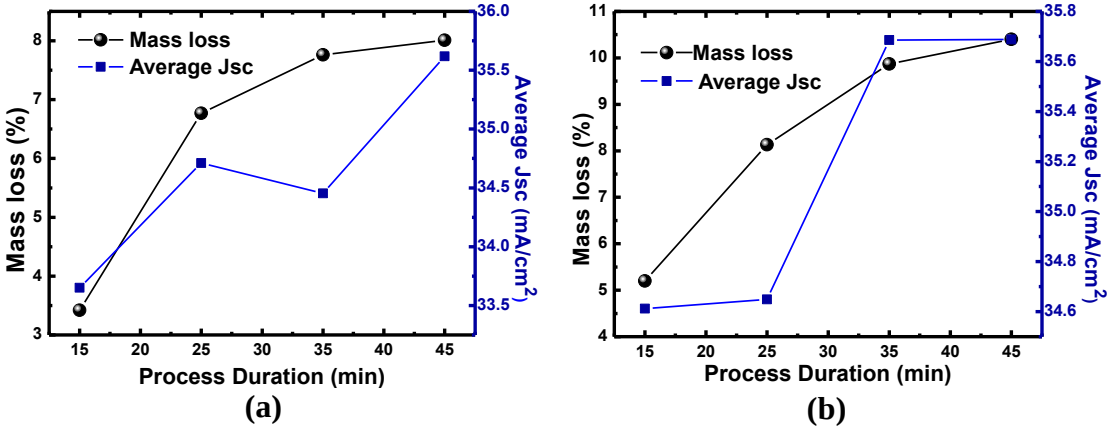


Figure 83: Mass loss and Jsc with changing process durations a) at 60°C b) at 70°C

Figure 84 shows how the average J_{sc} changes with the AM 1.5 weighted reflection of wafers with ARC and texturing time. As the reflection decreases, the J_{sc} values increases except for 35 min at 60°C. This set shows also the unexpected value of efficiency, so there should be a production error for this set.

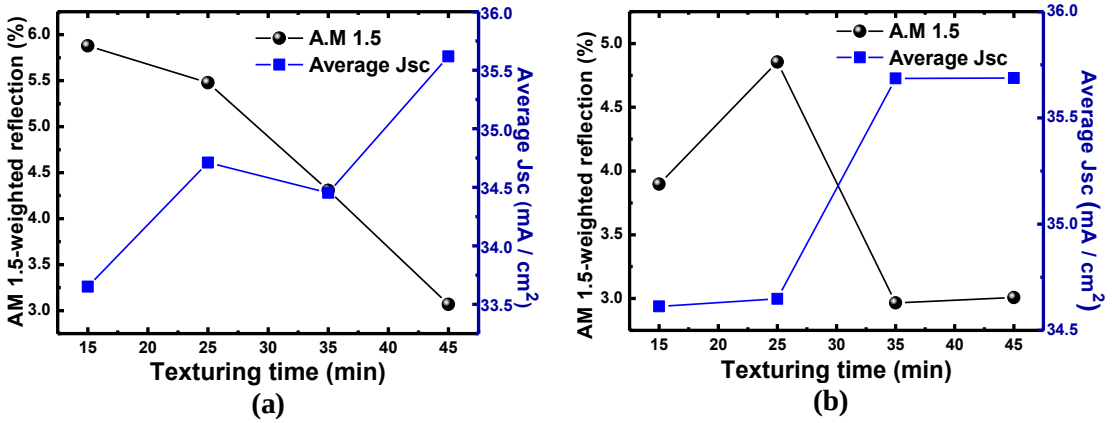


Figure 84: AM 1.5-weighted reflection and Average Jsc values with respect to changing texturing time a) at 60°C b) 70°C

To see the performance of produced cells without effects of series resistance, the cell parameters were measured by Suns-Voc system. The measurement results are shown in Table 10.

Table 10: Suns-Voc measurement results

	Texture Temperature (°C)	Time of texturing (min)	Average Jsc (mA)	Average Voc (V)	Average FF (%)	Average Eff (%)
70UA	70	15	34.612	0.615	83.113	17.694
	70	25	34.648	0.614	83.087	17.700
	70	35	35.686	0.614	83.101	18.222
	70	45	35.687	0.615	82.94	18.232
60UA	60	15	33.651	0.614	82.587	17.071
	60	25	34.71	0.617	82.891	17.767
	60	35	34.453	0.616	82.804	17.582
	60	45	35.617	0.614	82.864	18.132
Reference	75	45	34.434	0.609	83.013	17.42

Figure 85 shows the pseudo efficiencies and fill factors. Pseudo efficiencies and fill factors are higher than real ones. Real efficiencies and FF are cell parameters depending on series resistance, and they decrease with increase in series resistances.

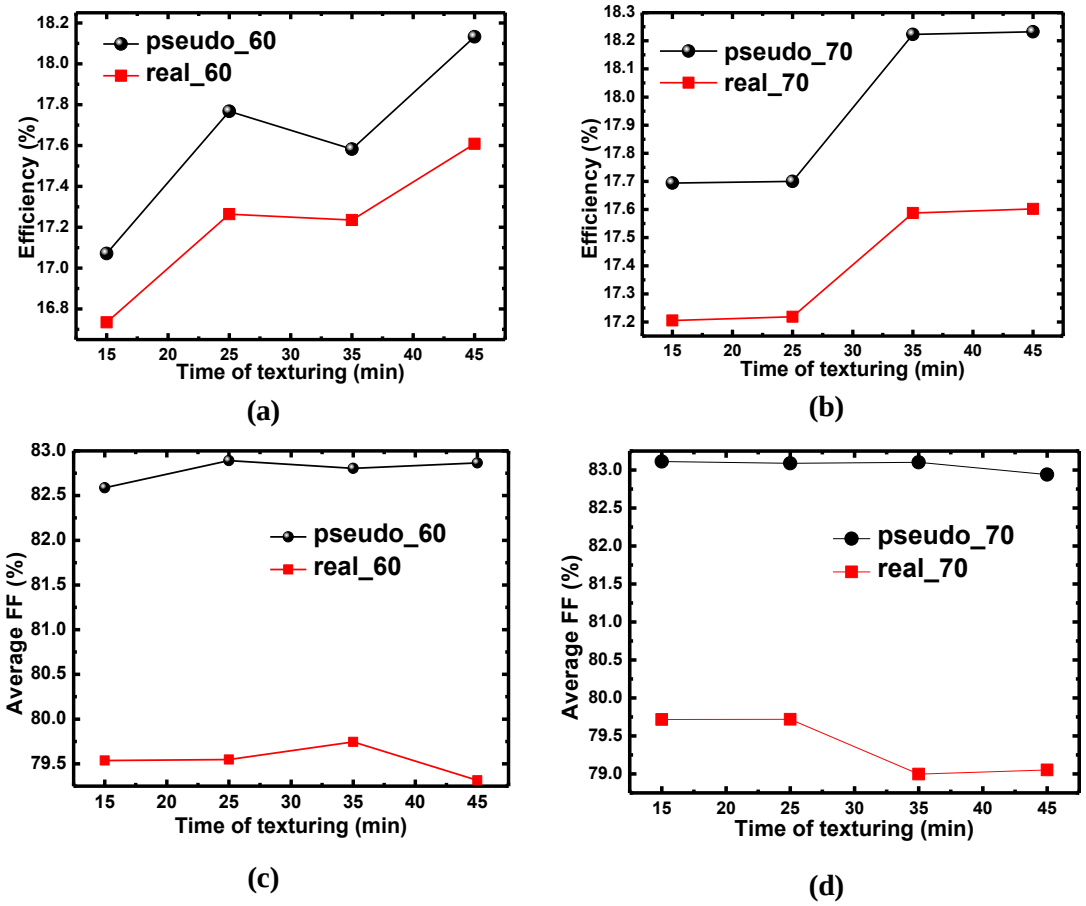


Figure 85: Pseudo and real efficiencies and fill factors a),c) at 60°C b),d) at 70°C process temperature

As shown in Table 10, the Voc value of reference is lower than the others about 5 mV. If we use Equation 4 to find the saturation currents and then use the I_{sc} of 70UA_45 min to find reference cell V_{oc}, we see that the calculated Voc of reference increases about 0.9 mV which is much smaller than 4 mV. It shows that increase in Voc is not only due to the increase in Jsc. To understand the reason, J_{01} and J_{02} values were compared.

As shown in Figure 86 (a), J_{01} values are order of 10^{-12} A/cm^2 which is the normal range and the values almost same except for reference. The J_{01} of reference is slightly higher than the others. Thus, reverse saturation current component is due to the emitter and bulk recombination.

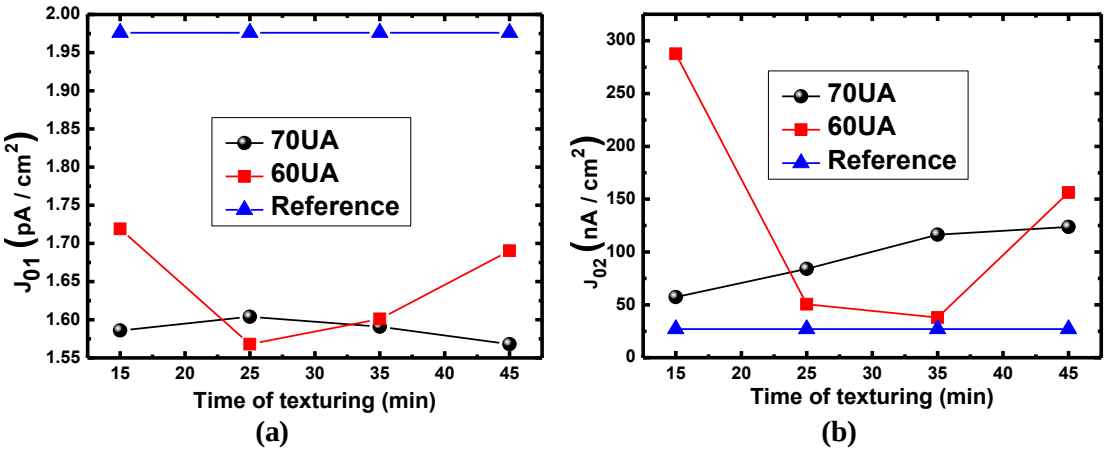
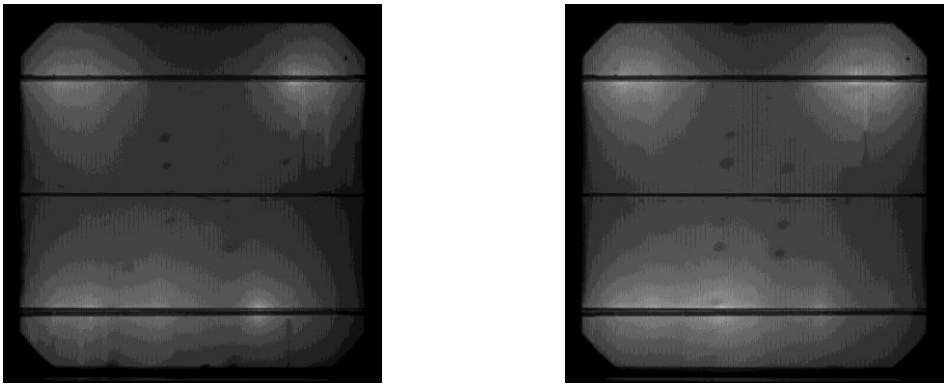


Figure 86: a) J_{01} b) J_{02} with respect to texturing time

Figure 86 (b) shows J_{02} values which are order of 10^{-10} A/cm^2 for wafers 60UA 25min and 35min, 70UA 15min, and reference. For the others, they are in order of 10^{-9} A/cm^2. The values of J_{02} higher than 10^{-10} A/cm^2 shows possible junction related problems [42].

We can than conclude that low Voc values for the reference sample is possibly due to the higher recombination of electron hole pairs at the front surface and low junction quality that leads to higher reverse saturation current.

To observe whether there are high series resistance due to contacts or not, electroluminescence images like shown in Figure 87 of produced cells were taken. The all images show almost same characteristics, so the others are not added here. All images have dots which are due to the contact point of transporters in firing furnace. There is only dead space at the edges of cells which are cut during edge isolation.



(a) **(b)**

Figure 87: Electroluminescence images of a) Reference b) 70UA 45min solar cell

Finally, external quantum efficiencies (EQEs) were measured to observe the response of cells to different wavelengths. EQE is proportional to passivation and reflection for short wavelengths, and it is proportional to light trapping for long wavelengths in general.

Figure 88 a) and b) show the EQE and reflection results of cells with highest efficiencies and reference. For 45 min texturing process at 60^{o}C, the EQE is higher than that of reference cell between 350 nm and 700 nm, while reflection is lower than that of reference. Although the reflection value is slightly higher than that of reference beyond 700 nm, the EQE is higher than that of reference between 850 nm and 1050 nm. For 45 min texturing process at 70^{o}C, the situation is similar. Between 350nm and 700nm, the reflection value of 70UA_45min cell is lower than reference; EQE is higher than that of reference. And EQE is higher than that of reference between 750 nm and 1100 nm, as the reflection is also higher than that of reference. These results show that the blue response and the light trapping are higher than those of reference cell.

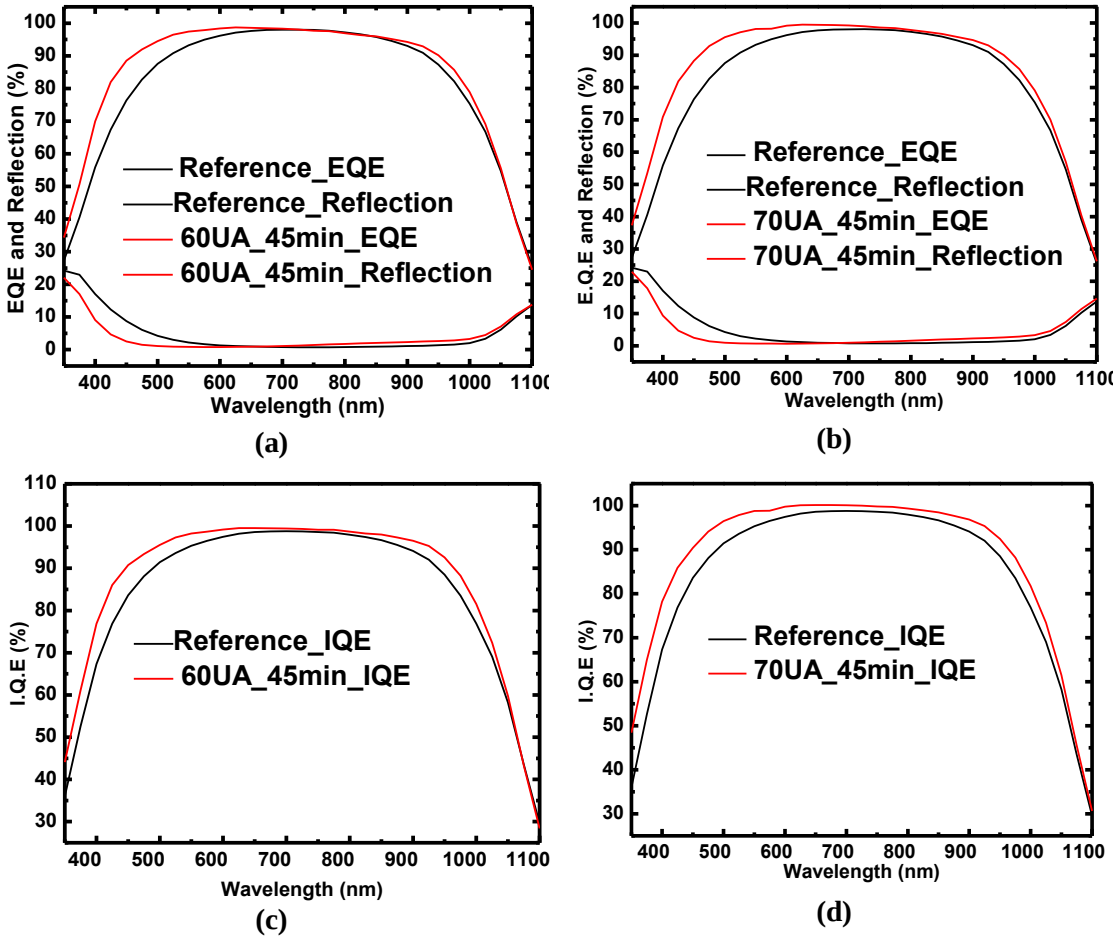


Figure 88: EQE and Reflection-IQE of solar cells produced by using wafers textured for 45 min a)-c) at 60°C and b)-d) at 70°C

To observe whether the blue response is higher due to only the reflection value or not, internal quantum efficiency -wavelength (IQE) curves are also added as shown in Figure 88 c) and d). Because IQE shows the performance of cells by excluding the reflection losses.

IQE values are higher than that of reference as shown in Figure 88. It can be said that the passivation quality of wafers with ultrasonic texturing is higher than that of reference. To understand the reason, the SEM images of reference wafer after texturing process was taken. Because, although all process steps are optimized for the reference, the produced cells with wafer that were textured with ultrasonic agitation shows better performance than the reference cells. If the quality of process

steps, junction quality and wafer quality (see Figure 86 for junction quality and bulk quality) are same for all samples, the only difference will be the surface morphologies.

Figure 89 shows the SEM images of wafers whose EQE, IQE and reflection values are given in Figure 88. As can be seen, the surface morphologies of wafers textured with ultrasonic agitation are more homogenous than the reference cell. The reference cell has more small pyramids on big pyramids and big pyramids formed by small pyramids. This inhomogenity of the surface makes difficult to get good passivation quality which is related to the front surface recombination of the cells.

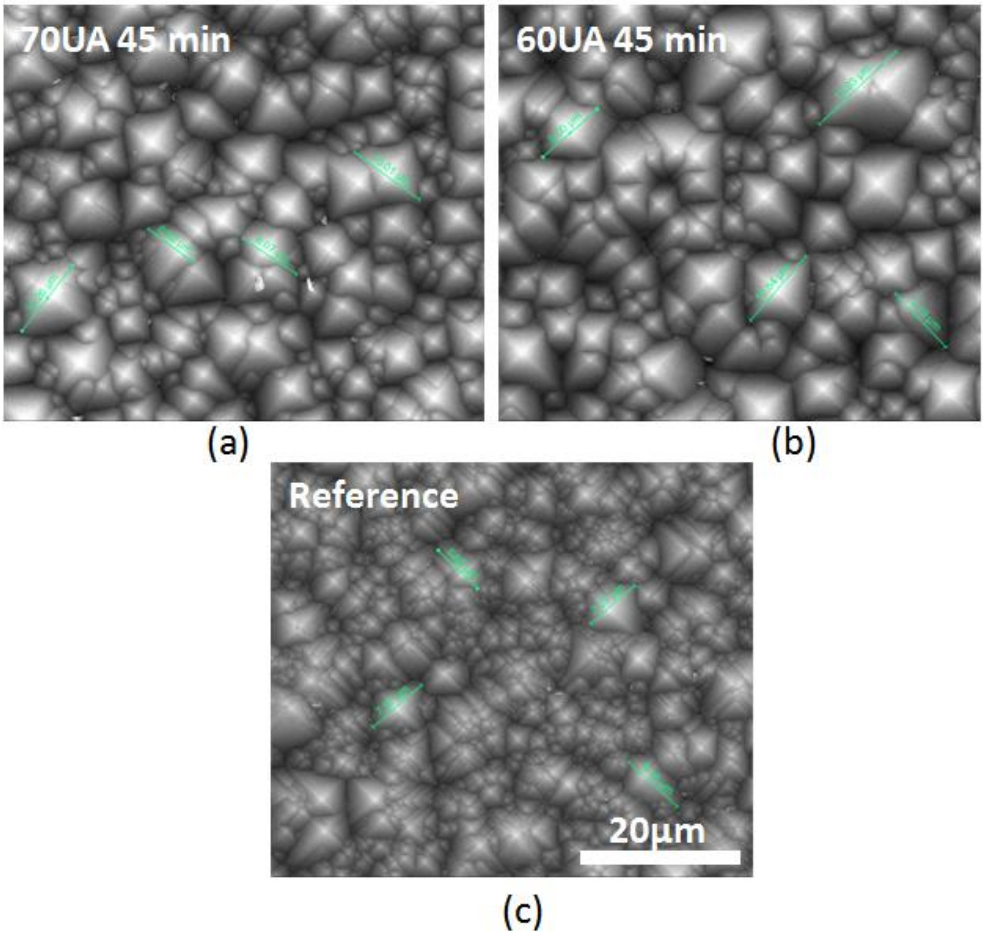


Figure 89: SEM image of a) 70UA 45min b) 60UA 45 min c) reference wafer after texturing process

CHAPTER 6

CONCULUSIONS

Texturing process is the first step of solar cell production. This process is carried out by using KOH-IPA solution to minimize the optical losses by forming random pyramids on wafer surface and thus increases the efficiency of the solar cell. In this study, the process parameters like temperature, time, and concentrations of KOH & IPA were optimized by using magnetic agitation. Then process temperature and duration were minimized by using ultrasonic agitation. Major conclusions of our studies are summarized below.

The results related with magnetic agitation are;

1. As the process duration increases, covered area and pyramid sizes increases for magnetic agitation. But it is not enough to get fully covered surfaces by just increasing the time. All process parameters must be optimized.
2. For process parameters 4.2 wt% KOH, 5.4vol% IPA, as-cut and SDE wafers had lowest reflection values for 45 min process duration at 70, 75 and 80^{o}C. But when the reflection results for 45 min were compared, lowest value was obtained at 75^{o}C. The difference between the highest and lowest reflection was 8% and 6% for as-cut and SDE respectively for 45 min process time.
3. For process parameters 3.3 wt% KOH, 5.4vol% IPA, again the lowest reflection values were obtained for 45 min process time. The difference between the highest and lowest reflection was 1% and 2% for as-cut and SDE respectively for 45 min process time. It shows that these process parameters were less sensitive to temperature when compared with previous one. Wafers textured with 3.3wt% KOH had lower reflection values than wafers textured with 4.2wt % KOH for 15, 25, and 35 min texturing time. This shows that decreasing KOH

concentration from 4.2 wt% to 3.3 wt% improved the process for short process times.

4. A cap was used to close the glass beaker in which processes were carried out. Closing the beaker increases the pressure on the solution and the evaporation of water and IPA decreases. This makes the concentrations almost constant. For process parameters 4.2 wt% KOH, 5.4 vol% IPA at 75^{o}C, the wafers textured for 15 min and 25 min had lower reflection than before. When the process was carried out for 45 min, the pyramid densities increased for both as-cut and SDE and this decreased the reflection slightly.
5. Increasing speed and changing IPA concentration did not improve process for 15 min and 25 min very much.
6. There are some problems faced during texturing process with magnetic agitation.

- The reproducibility of the process was hard for some cases in which the process duration was lower or equal 25 min for all process temperature especially 70^{o}C.

- The surfaces of wafers were not uniformly textured, and there were differences in reflection between the faces again for process durations lower or equal to 25 min.

These results show that it is hard to minimize process parameters especially time and temperature by using magnetic agitation. We decided to change agitation type with ultrasonic agitation.

1. As time increases, reflection decreases again.
2. The wafer surface was fully covered by texturing with 3.3wt% KOH, 5.4 wt% IPA for 15 min at 70^{o}C and 35 min 60^{o}C.
3. 15 min texturing had higher reflection due to pyramids with round tips.
4. The pyramid density of ultrasonic agitation was higher than that of magnetic one about 5 times. Therefore small pyramids were obtained.
5. Having low boiling point (82.4^{o}C), which makes it necessary to re-dose IPA into the solution due to evaporation, is the main problem of the standard

solution and causes consuming high concentrations of IPA and leads to high production costs, because IPA is expensive. Therefore by using ultrasonic agitation, cost effective process was obtained by decreasing temperature and shorting process time.

We did also simulations of SDE, one side and two side uniformly textured wafers. The results are;

1. The reflection for SDE wafer is not only due to light reflected from front surface but also back surface for wavelength higher than 700 nm and thickness lower than 70 μm.
2. The absorption decreases for wavelength higher than 850 nm as thickness decreases for simulation model one side and two side textured wafers whose thicknesses higher or equal to 100 μm.
3. One side textured wafers shows higher absorption than two side textured, because the total reflection probability of light not coming perpendicular to flat surface is higher than that of light to surface with pyramids.

The solar cell results of wafers textured with ultrasonic agitation are;

1. The J_{sc} value was higher than the reference cell (34.4 mA/ cm^2) about 1.25 mA/ cm^2 for wafers with efficiency about 17.6%
2. The V_{oc} values were higher than the reference cell (619 mV) about 4 mV for almost all wafers textured with ultrasonic agitation.
3. The efficiencies were higher than the reference cell (17%) about at least 0.2% and at most 0.7%. The highest efficiency was 17.74% of wafers textured for 45 min 60^{o}C with ultrasonic agitation.
4. From EQE and IQE results, the wafers textured with ultrasonic agitation had uniformly distributed pyramids with heights less than 4 μm leading had better blue response, surface passivation and light trapping.

To sum up, the texturing process with ultrasonic agitation has a potential to minimize the process parameters. If more experiments are made about this texturing technique, more cost effective processes will be able to obtain. If the solar cell

production parameters are optimize for wafers textured with ultrasonic agitation, higher efficiency values will be obtained.

BIBLIOGRAPHY

[1] "Enviromental & Regulatory Specialists." [Online]. Available: http://earsi.com/ggp01.htm. [Accessed: 12-Oct-2014].

[2] "ISE Photovoltaics Report." [Online]. Available: https://www.ise.fraunhofer.de/en/downloads-englisch/pdf-files-englisch/photovoltaics-report-slides.pdf. [Accessed: 10-Nov-2014].

[3] "PVCDROM." [Online]. Available: http://pveducation.org/pvcdrom/. [Accessed: 12-Nov-2014].

[4] D. M. Chapin, C. S. Fuller, and G. L. Pearson, "A new silicon p-n junction photocell for converting solar radiation into electrical power," *J. Appl. Phys.*, vol. 25, pp. 676–677, 1954.

[5] W. Schockley and H. J. Quesisser, "Detailed balance limit of efficiency of pn junction solar cells," *J. Appl. Phys.*, vol. 32, pp. 510–519, 1951.

[6] J. Nestor and X. Quiebras, "Wet chemical textures for crystalline silicon solar cells," pp. 1–124, 2013.

[7] M. A. Green, "Silicon Solar Cells: State of Art," *Philosophical Transactions of The Royal Society A*, 2013. [Online]. Available: http://dx.doi.org/10.1098/rsta.2011.0413. [Accessed: 12-Nov-2014].

[8] "Nanosolar CIGS Solar Cells." [Online]. Available: http://www.solarfeeds.com/rip-nanosolar/. [Accessed: 01-Jan-2015].

[9] M.S. Thesis,E. H. Çiftpınar, *Selective Emitter Formation via Single Step Doping Through Laser Patterned Mask Oxide Layer for Monocrystalline Silicon Cells*: Middle East Technical University, 2014.

[10] M.S. Thesis, S. H. Sedani, *Fabrication and Doping of Thin Crystalline Si Prepared by E-Beam Evaporation on Glass Substrate*: Middle East Technical University, 2013.

[11] B. M. Kayes, L. Zhang, R. Twist, I. Ding, and G. S. Higashi, "Flexible Thin-Film Tandem Solar Cells With > 30 % Efficiency," *IEEE J. Photovoltaics*, vol. 4, no. 2, pp. 729–733, 2014.

[12] M.S. Thesis, F. Es, *Fabrication and Characterization of Single Crystalline Silicon Solar Cells*: Middle East Technical University, 2010.

[13] G. M. Research, "Building Integrated Photovoltaics: An emerging market." [Online]. Available: http://www.solarserver.com/solar-magazine/solar-report/solar-report/building-integrated-photovoltaics-an-emerging-market.html. [Accessed: 15-Dec-2014].

[14] "NSF / ONR Workshop on Key Scientific and Technological Issues for Development of Next-Generation Organic Solar Cells." [Online]. Available: http://web.utk.edu/~opvwshop/. [Accessed: 01-Jan-2015].

[15] C. S. Solanki, "Solar Photovoltaics: Fundamentals Technologies And Applications," PHI Learning Pvt. Ltd., 2009, pp. 323–324.

[16] B. Hoffman, V. Sivakov, S. W. Schmitt, M. Y. Bashouti, M. Latzel, J. Dluhoš, and J. Jiruse, "Wet – Chemically Etched Silicon Nanowire Solar Cells: Fabrication and Advanced Characterization," P. X. Peng, Ed. 2012, pp. 211–230.

[17] "Series Resistance." [Online]. Available: http://pveducation.org/pvcdrom/solar-cell-operation/series-resistance. [Accessed: 01-Feb-2015].

[18] "Quantum Efficiency." [Online]. Available: http://www.pveducation.org/pvcdrom/solar-cell-operation/quantum-efficiency. [Accessed: 01-Feb-2015].

[19] J. D. Plummer, M. D. Deal, and P. B. Griffin, "Silicon VLSI technology: fundamentals, practice and modeling," Prentice Hall, 2000, pp. 618–619.

[20] R. N. Ghoshtagore, "Phosphorus diffusion processes in SiO2 films," *Thin Solid Films*, vol. 25, no. 2, pp. 501–513, 1975.

[21] K. Sakamoto, K. Nishi, F. Ichikawa, and S. Ushio, "Segregation and Transport Coefficients of Impurities at the Si/SiO2 Interface," *J. Appl. Phys.*, vol. 61, no. 4, pp. 1553–1555, 1987.

[22] M.S. Thesis, M. Bilgen, *Comparison of Crystal Si Solar Cells Fabricated on P-Type and N-Type Float Zone Silicon Wafers*: Middle East Technical University, 2013.

[23] J. Nelson, *The Physics of Solar Cells*, 1st ed. London: Imperial College Press, 2003.

[24] “Anti-Reflection Coatings.” [Online]. Available: http://pveducation.org/pvcdrom/design/anti-reflection-coatings. [Accessed: 01-May-2015].

[25] B. Streetman and S. Banerjee, *Solid State Electronic Devices*, 6th ed. PHI Learning, 2009.

[26] F. Colville and C. Dunsky, “Lasers Support Emerging Solar Industry Needs,” *Photonic Spectra*, 2008. [Online]. Available: http://www.photonics.com/Article.aspx?AID=33002. [Accessed: 01-Feb-2015].

[27] “Reference Solar Spectral Irradiance: ASTM G-173.” [Online]. Available: http://rredc.nrel.gov/solar/spectra/am1.5/astmg173/astmg173.html. [Accessed: 23-Jun-2015].

[28] M. Moreno, D. Murias, J. Martínez, C. Reyes-Betanzo, a. Torres, R. Ambrosio, P. Rosales, P. Roca i Cabarrocas, and M. Escobar, “A comparative study of wet and dry texturing processes of c-Si wafers for the fabrication of solar cells,” *Sol. Energy*, vol. 101, pp. 182–191, 2014.

[29] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, “Anisotropic etching of crystalline silicon in alkaline solutions,” *J. Electrochem. Soc.*, vol. 137, no. 11, p. 3612, 1990.

[30] D. B. Lee, “Anisotropic etching of silicon,” *J. Appl. Phys.*, vol. 40, no. 11, pp. 4569–4574, 1969.

[31] E. D. Palik, “A raman study of etching silicon in aqueous KOH,” *J. Electrochem. Soc.*, vol. 130, no. 4, p. 956, 1983.

[32] J. B. Price, “Anisotropic etching of silicon with KOH-H2O-isopropyl alcohol,” *J. Electrochem. Soc.*, vol. 120, no. 3, p. C96, 1973.

[33] I. Kashkoush, G. Chen, and D. Nemeth, “Characterization of c-Si Texturization in wet KOH/IPA and its Effect on Cell Efficiency,” pp. 5–8.

[34] A. K. Chu, J. S. Wang, Z. Y. Tsai, and C. K. Lee, “A simple and cost-effective approach for fabricating pyramids on crystalline silicon wafers,” *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 8, pp. 1276–1280, 2009.

[35] L. Wang, F. Wang, X. Zhang, N. Wang, Y. Jiang, Q. Hao, and Y. Zhao, “Improving efficiency of silicon heterojunction solar cells by surface texturing of silicon wafers using tetramethylammonium hydroxide,” *J. Power Sources*, vol. 268, pp. 619–624, 2014.

[36] K. Birmann, M. Demant, S. Rein, and B. Bläsi, "Optical Characterization of Random Pyramid Texturization," *Small*, no. September, pp. 5–9, 2011.

[37] J. D. Hylton, a. R. Burgers, and W. C. Sinke, "Alkaline Etching for Reflectance Reduction in Multicrystalline Silicon Solar Cells," *J. Electrochem. Soc.*, vol. 151, no. 6, p. G408, 2004.

[38] M.S. Thesis, O. Demircioğlu, *Optmization of Metallization in Crystalline Silicon Solar Cells*: Middle East Technical University, 2012.

[39] "High Lambertian reflectance over their effective spectral range." [Online]. Available: https://www.labsphere.com/wp-content/uploads/2015/05/Spectralon-Diffuse-Reflectance-Standards.pdf. [Accessed: 13-Dec-2014].

[40] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material device and characterization," in *Proc. 25th Photovoltaic Specialists Conference*, 1996, pp. 457–460.

[41] "Optical Properties of Silicon." [Online]. Available: http://pveducation.org/pvcdrom/materials/optical-properties-of-silicon. [Accessed: 01-May-2015].

[42] O. Breitenstein, J. Bauer, P. P. Altermatt, and K. Ramspeck, "Influence of Defects on Solar Cell Characteristics," *Solid State Phenom.*, vol. 156–158, pp. 1–10, 2009.