# MEDIUM POWER-WIDEBAND ENVELOPE TRACKING RF POWER AMPLIFIER DESIGN

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**MEDIUM POWER-WIDEBAND ENVELOPE TRACKING RF POWER AMPLIFIER DESIGN**

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# ABSTRACT

MEDIUM POWER-WIDEBAND ENVELOPE TRACKING RF POWER AMPLIFIER DESIGN

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An inevitable trade-off between efficiency and linearity challenges RF researchers more than ever in today's wireless communication systems. The reason is the tight linearity requirements of the high peak-to-average power ratio (PAPR) signals. Linearity is crucial because modern communication systems transmit non-constant envelope modulation signals. Efficiency is also crucial because portable systems have limited source of power and dissipated heat power increases cooling system cost. Various power amplifier architectures have been demonstrated to achieve high efficiency for high PAPR signals. One of them has different property. This one is fundamentally immune to changes in the frequency of the carrier; it depends only on the envelope of the RF signal.

This dissertation focuses on the design of Envelope Tracking Power Amplifier (ETPA) for enabling broadband wireless communication with high efficiency. First, load and supply modulation techniques are reviewed. In second chapter, main blocks of ETPA are described and efficiency formulas are given. Then, 10W LDMOS RFPA is designed with the help of CAD programs and implemented on the PCB. In third chapter, hybrid envelope amplifier topology is introduced to maximize efficiency for large back-offs and implemented on the PCB. Finally, ET system is tested with 5 MHz-WCDMA with 9.7 dB PAPR. Drain efficiency and ACPR measurements are tabulated. To better understand the ET operation, simulations with ADS are done.

Comparison table of constant supply voltage RFPA and ET PA is added to show the efficiency enhancement.

Keywords: Envelope Tracking, RF Power Amplifier, Efficiency enhancement, Envelope amplifier, Power back-off

# ÖZ

ORTA GÜÇLÜ-GENİŞBANT ZARF TAKİP METODU RADYO FREKANS GÜÇ YÜKSELTECİ DİZAYNI

Şirin, Emre
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Günümüz kablosuz haberleşme sistemlerindeki verimlilik ve doğrusallık arasındaki kaçınılmaz ilişki RF araştırmacıları her zamankinden daha çok zorlamaktadır. Bunun sebebi tepe-ortalama oranı yüksek sinyallerin katı doğrusallık gerektirmesidir. Doğrusallık gereklidir çünkü modern haberleşme sistemleri değişken zarf modülasyonlu sinyalleri yayar. Verimlilik de gereklidir çünkü taşınabilir sistemler sınırlı güç kaynağına sabittir ve açığa çıkan ısı gücü soğutma sistemlerinin maliyetini arttırır. Bir çok güç yükseltici yapısının tepe-ortalama oranı yüksek sinyaller için yüksek verimlilik elde ettiği gösterilmiştir. Bir tanesi diğerlerinden farklıdır. Bu, merkez frekans değişiminden etkilenmez; sadece RF sinyalin zarfına bağlıdır. Bu tez genişbandlı kablosuz haberleşmeyi yüksek verimlilikle yapmayı mümkün kılan geniş bandlı zarf takip RF güç yükselteci tasarımına odaklanmıştır. İlk olarak, yük ve besleme modülasyonu teknikleri açıklanmıştır. İkinci kısımda, zarf takip güç yükseltecinin ana bloklarını açıklanmış ve verimlilik formülleri verilmiştir. 10W LDMOS RFGY benzetim programlarıyla tasarlanmıştır. Üçüncü kısımda, verimliliği maksimum hale getirmek için kullanılan hibrit zarf yükseltici topolojisi tanıtılmış, üretilmiştir. 4. kısımda, zarf takip yöntemini daha iyi anlamak için, ADS programı ile benzetim yapılmıştır. Son olarak, zarf takibi sistemi 9.7dB PAPR'ı olan 5MHz-WCDMA sinyali ile test edilmiştir. Verimlilik ve doğrusallık ölçümleri tablolaştırılmıştır. Verimlilik artışını göstermek için sabit beslenen RFGY ve zarf takibi GY karşılaştırma tablosu eklenmiştir.

Anahtar Kelimeler: Zarf Takibi, Radyo frekansı güç yükseltici, verimlilik arttırma, zarf yükseltici, zayıflatılmış güç

To my wife

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| | |
|---|---|
| RFPA | Radio Frequency Power Amplifier |
| WCDMA | Wideband Code Division Multiple Access |
| ET | Envelope Tracking |
| EA | Envelope Amplifier |
| ADS | Advanced Design System |
| WiMAX | Worldwide Interoperability for Microwave Access |
| OFDM | Orthogonal Frequency Division Multiplexing |
| LTE | Long-term Evolution |
| PAPR | Peak to average power ratio |
| DPD | Digital predistortion |

# CHAPTER 1

# INTRODUCTION

## 1.1 Overview

High speed data transfer in a spectrally efficient way is the ultimate goal for many communication engineers. In wireless communication systems this can be done with the help of complex digital modulation schemes such as Worldwide Interoperability for Microwave Access (WiMAX) in orthogonal frequency division multiplexing (OFDM), CDMA2000, wideband code-division multiple access (WCDMA), or Long-term Evolution (LTE). Such modulation techniques have similar properties; high peak to average power ratio (PAPR) and large bandwidth. PAPR is defined as the ratio of the peak power of a given signal to its average power. Figure 1.1 shows the RFPA evolution from class-AB/B to envelope tracking (ET) with the wireless communication standard evolutions. As can be seen from this figure, PAPR of the evolved signals constantly increases with the growth of fourth-generation (4G) services. Before 2005, for 2G and 3G systems, class AB/B with various linearity enhancement methods was enough to amplify the signals with 3-9 dB PAPR. Between 2005 and 2009, Doherty with digital predistortion (DPD) was implemented to improve the efficiency and linearity. However, due to the nature of the LTE signal, PAPR is increased to 8.5-13 dB and ET has become mandatory for high efficiency.

The traditional amplification method for the high PAPR signals is to "back off" the linear Class-A or Class-AB PA's output power to minimize distortion. The reason is the fact that linear mode PA's efficiency is proportional to the output power, e.g:

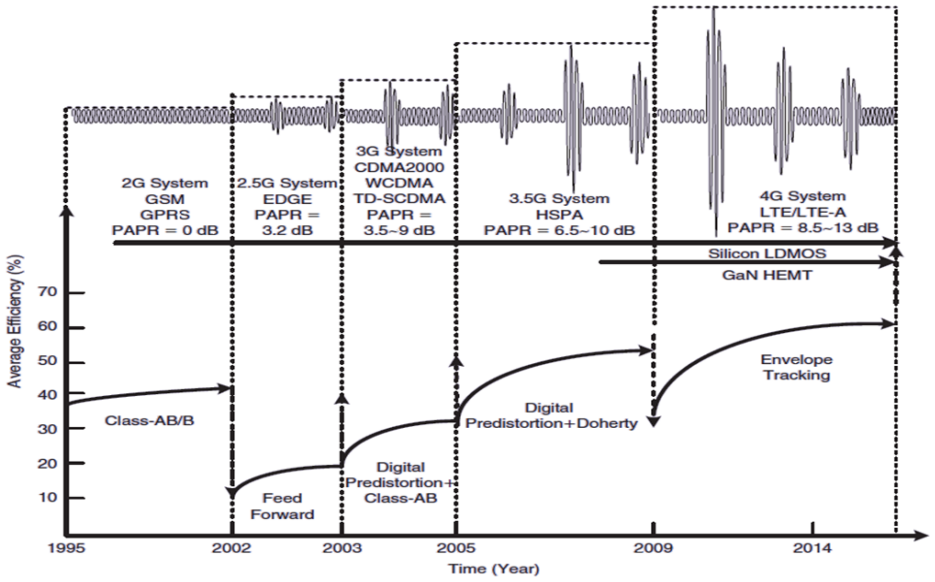



Figure 1.1: The RFPA evolution from class-AB/B to envelope tracking (ET) with the wireless communication standard evolutions, Figure is adapted from [27]

$$n_{linPA} = f(P_{out}) \ , \tag{1.1}$$

where the efficiency is

$$n_{linPA} = \frac{P_{out}}{P_{dc}} \tag{1.2}$$

As can be seen from the Figure 1.2, the efficiency of a Class-A amplifier decreases with output power Pout (relative to its peak value) in proportion to Pout/Poutmax. Similarly, for a Class-B amplifier, the efficiency varies as $\sqrt{\frac{Pout}{Poutmax}}$. At 10 dB power backoff of class-A and class-B amplifiers, the efficiencies fall from 50% to 5% and from 78.5% to 25%, respectively.

Various PA architectures have been demonstrated to achieve high efficiency for high PAPR signals. These techniques can be categorized into two groups: load modulation (Doherty, Outphasing) and supply voltage modulation (Envelope Elimination and Restoration, Envelope Tracking). These efficiency enhancement methods are discussed briefly in the following pages.

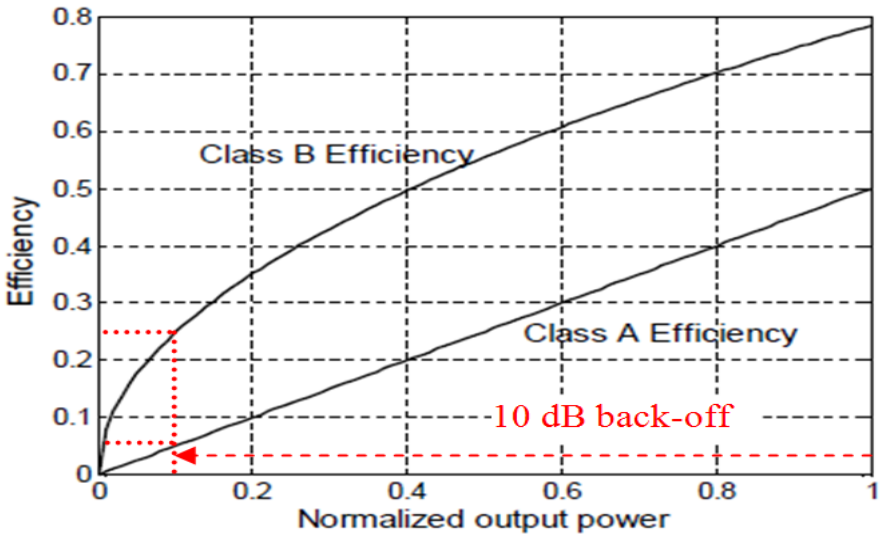



Figure 1.2: Normalized output power versus efficiency

## 1.2 Load Modulation Techniques

The concept of load modulation is simple but powerful. In essence, two amplifiers share a common load which modifies the current and voltage waveforms within each transistor to conserve high efficiency for signals at less than peak output power.

Figure 1.3 illustrates how two trans-impedance amplifiers (as a typical field effect transistor behaves in its linear mode of operation) can be used to apply RF currents into a common load. If both devices instantaneously provide the same current, these RF currents add in phase, doubling the voltage across the load. This means when I1=I2, both devices see the load resistance 2R. Impedance is defined as the ratio of the voltage and current waveforms. By this definition, the load impedance 'seen' from one device is modified, or modulated, by the current from the other device. Of course, the physical load is unchanged, but the apparent load as defined by the relationship between the I-V waveforms seen at the output plane of the first active device is modified by the other.

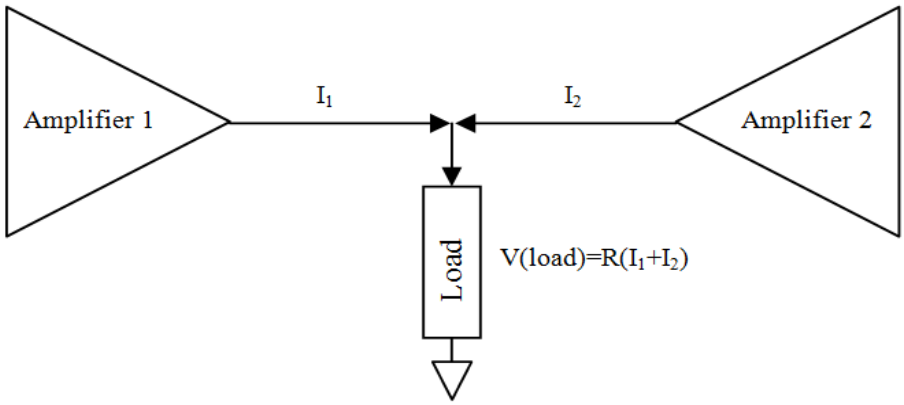



Figure 1.3: Load modulation concept

### 1.2.1 Doherty PA

The basic Doherty power amplifier consists of a main amplifier and an auxiliary amplifier, as shown in Figure 1.4. The input signal is passed through a power divider, splitting the power equally to each amplifier with a 90 degree phase difference. After amplification, the outputs of the two amplifiers are combined via a quarter-wave transmission line that acts as an impedance inverter. As a result of using active load modulation on the main amplifier via the auxiliary amplifier attached to the quarter-wave impedance transformer, high efficiency in the presence of signals with high PAPR can be achieved.

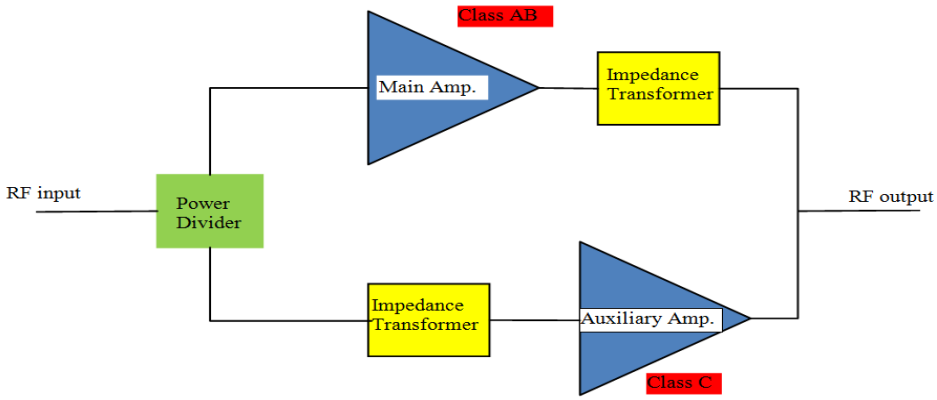



Figure 1.4: The basic Doherty power amplifier

The main and auxiliary transistors are biased differently, such that at lower signal amplitudes only the main stage is operational. The load seen by the main amplifier at low power levels is R. As the amplitude increases, this stage moves into compression and its efficiency increases, as with a conventional class AB amplifier. Further increases in amplitude will begin to switch on the peaking amplifier which is biased typically in class C. This is the point at which load modulation begins. By peak power, both devices are being fully driven and the effective load for both main and peaking amplifiers is R/2.

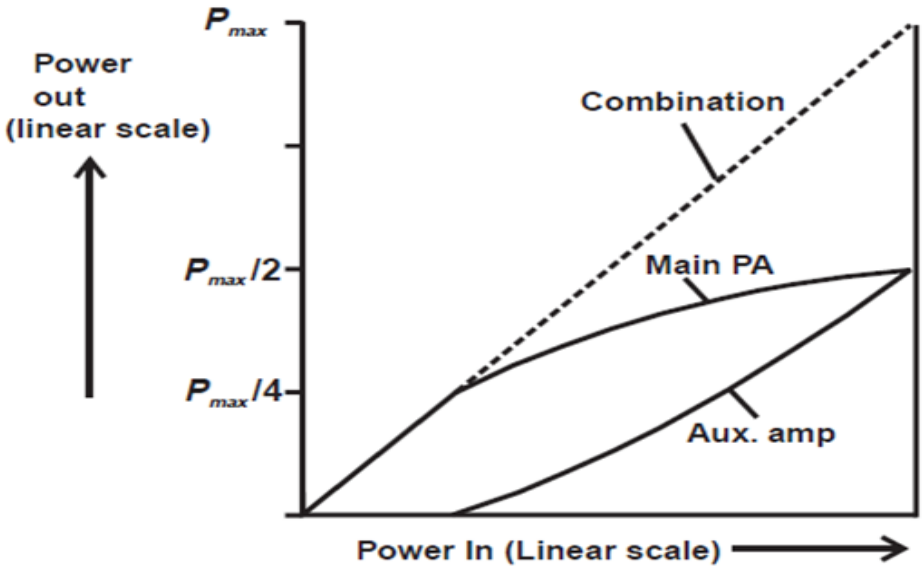



Figure 1.5: Pin vs Pout curve of typical Doherty amplifier

However, considering again the basic load modulation diagram in Figure 1.3, it can be seen that with both devices conducting, the voltage at the load is increased and therefore the apparent load is increased instead of decreased. This is the opposite sense to what is required in our Doherty amplifier. Ideally, when more power is required, the load impedance of the main amplifier should decrease, allowing more current and hence more power to be supplied. This problem is solved in a Doherty amplifier by including an impedance inverter on the main device output, as shown in Figure 1.6. With the inclusion of a quarter wave transmission line, or its lumped element equivalent, the operational sense of the load modulation is corrected. However, this impedance inverter introduces a bandwidth limitation.

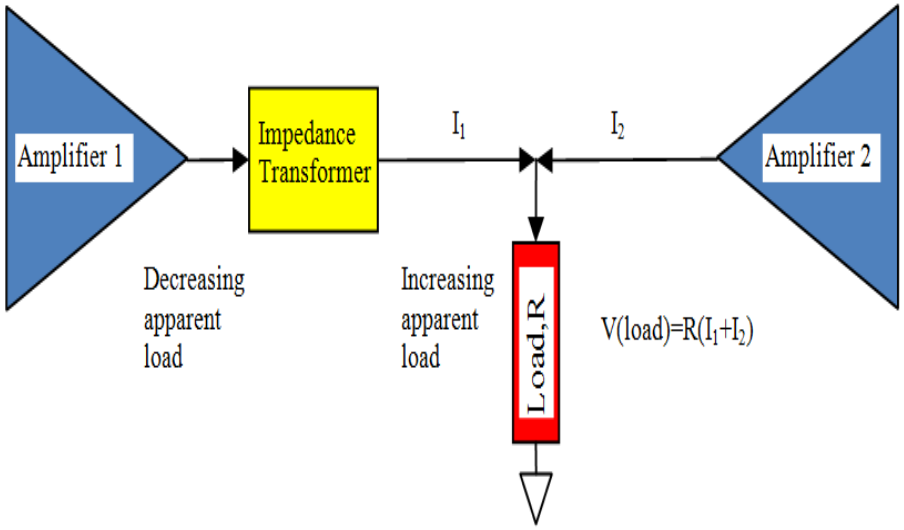



Figure 1.6: The Doherty arrangement

In Doherty configuration, limited efficiency enhancement in back-off is serious problem. The main source of this problem is the low conduction angle of the Class-C biased auxiliary amplifier. For that case, authors in [5],[30], suggested the adjustment of the auxiliary amplifier gate voltage as a function of the input signal strength. This resulted in higher peak-envelope- power (PEP) and better linearity, at the cost of a substantial increase in complexity, attributed to the external bias control and delay adaptation. Alternatively, the uneven power drive Doherty PA has been investigated in [19],[20]. In order to reach enough peaking RF current levels required for full load modulation, an uneven Wilkinson power divider is used at the Doherty PA input that provides more input power to the peaking PA than to the main PA. The power split ratio can be optimized for proper operation. An asymmetrical Doherty configuration has been also analyzed to improve the average power efficiency and linearity, in [21], [3].

### 1.2.2 Chireix Outphasing PA

The Chireix outphasing technique was first invented in 1935 by Chireix [7] and Cox [8] used the principle of this technique in a new form of power amplification called

linear amplification using nonlinear components (LINC) in 1974. The basic configuration of the Chireix outphasing technique is shown in Figure 1.7. Similar to Doherty, Chireix used two power transistors and a non-isolating power combiner to enable load modulation based efficiency enhancement. However, unlike the Doherty method, these RF amplifiers are nonlinear and driven by constant amplitude input signals which are produced by the modulator. This modulator converts AM information of the amplitude modulated complex signal to PM information and drives both of the RF transistors. This signal processing step is known as signal decomposition. After the amplification, these phase modulated signals are added with the help of in-phase combiner. At the output of the combiner, amplified complex signal is reconstructed.

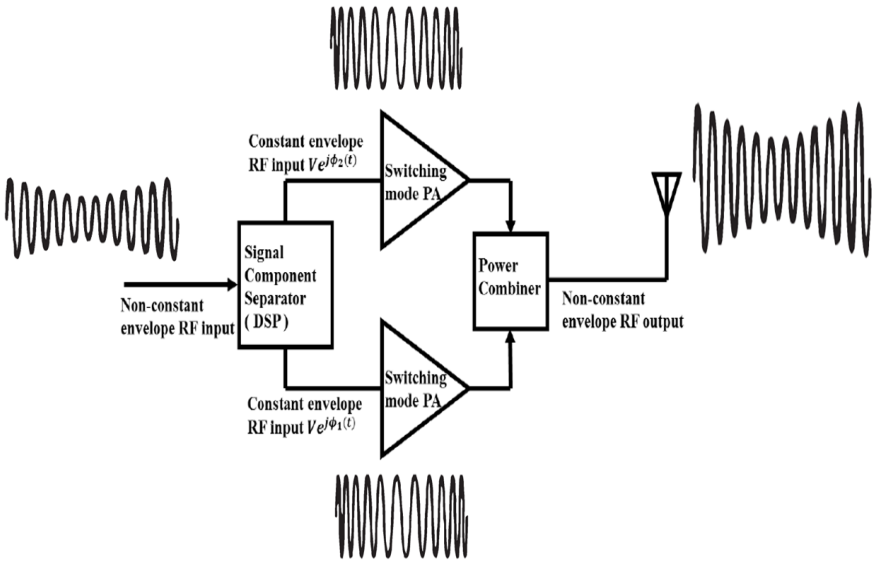



Figure 1.7: Outphasing power amplifier

Several important differences between the two architectures are also existed. Firstly, the Doherty architecture relies on the active devices acting as current sources. The Chireix architecture relies on the devices acting as voltage sources. Secondly, the currents in a Doherty PA are combined in a single ended load, whereas the voltages in a Chireix combiner are applied, conceptually, to a floating load which can be seen from Figure 1.8. Thirdly, the Doherty amplifier requires an impedance inverter to change the sense of the load modulation to achieve the desired goal of increased efficiency, whereas the load modulation in the Chireix amplifier is achieved purely with

phase control of the output voltage waveforms. The phase-mismatch problem at the input conditioner and the impedance matching at the output combiner are two issues related to Chireix PA. These problems are deeply investigated and solutions are given in [28]. Finally, in the Doherty amplifier the load impedance of the amplifier is modulated between R/2 and R, while that of the peaking amplifier is modulated between infinity and R/2. In the Chireix, the range of load modulation for both amplifiers extends from R/2 to infinity which can be seen in Figure 1.8.

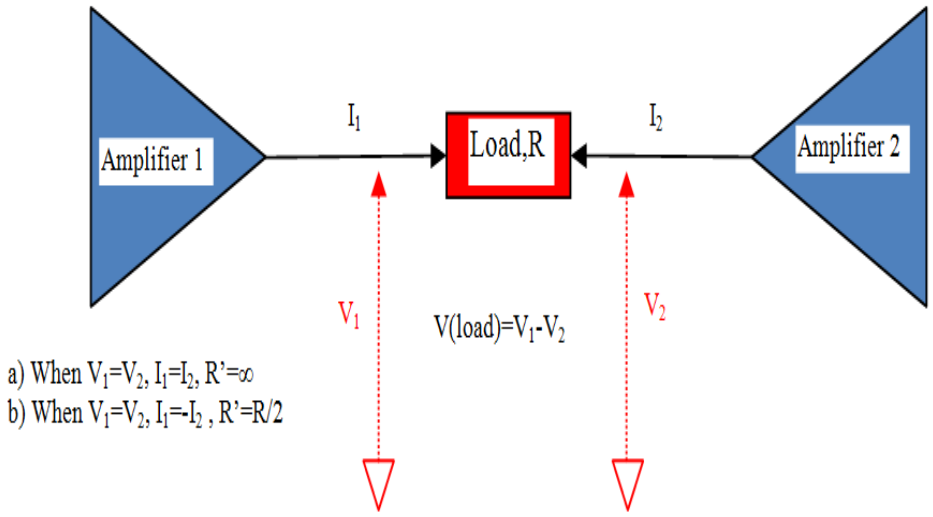



Figure 1.8: The Outphasing arrangement

There are two problems related to Chireix method which are RF bandwidth limitations due to the use of impedance inverter and complex DSP in order to generate the input-phase modulated signals. A more recent application of this technique in a high power RFPA system for WCDMA applications can be found in [22] and [2].

## 1.3 Supply Voltage Modulation Techniques

In Figure 1.9, a dc power supply for a PA with and without the supply voltage modulation technique can be seen. When the input signal is noncontant-envelope modulated signal, the PA with fixed supply voltage is adjusted for maximum power level and dissipates a lot of dc power at lower level. This inefficient operation consumes a

lot of power internally and generates heat. Therefore, the transmitters require additional thermal management equipment to guarantee their reliability, which increases the cost and size of the systems. Figure 1.9 (b), shows the concept of supply modulated PA. Compared to PAs with fixed supply voltage, the dc supply is controlled with envelope of the input signal to amplify the signal appropriately, and the dissipated power of the PA is minimized. The most important part is the supply modulator which uses envelope information of the input signal to generate drain voltage of the RF PA. This part should have a large bandwidth, larger than the envelope of the signal bandwidth, as well as high efficiency across this bandwidth. The detailed properties of supply modulator will be given in the following chapter.

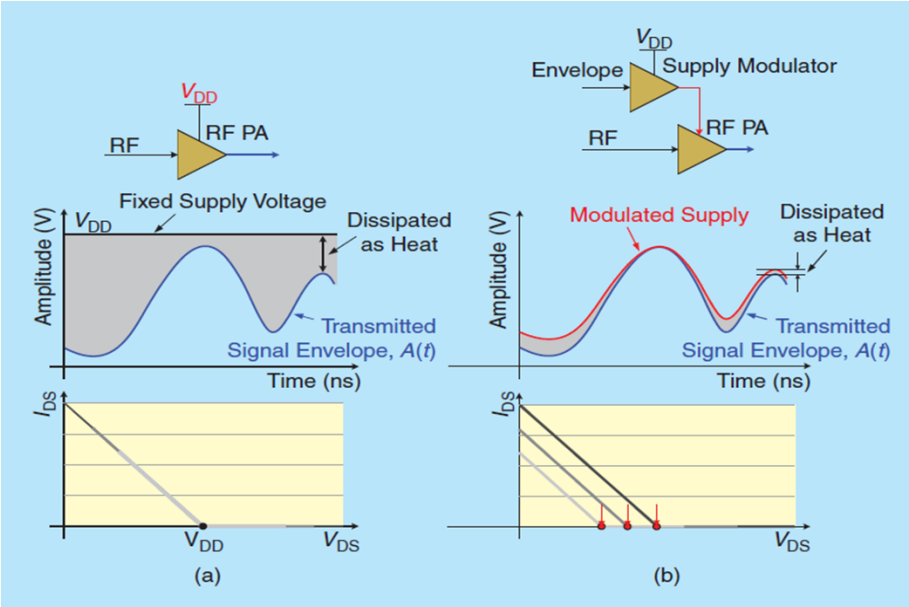



Figure 1.9: General power amplifier with a fixed supply voltage. (b) Concept of a supply-modulated power amplifier. (Figure is adapted from [4])

### 1.3.1 Envelope Elimination and Restoration

The Envelope elimination and restoration technique was proposed by Kahn, [23], to increase the efficiency of single sideband (SSB) transmitters. SSB modulated signals have similar properties with modern communication signals such that both of them carry amplitude and phase information in the transmitted signal. So, Kahn's technique is very important today to solve the linearity-efficiency compromise in some manner

for non-constant complex modulated signals. Kahn EER system is shown in Figure 1.10. Basically it includes a switch mode PA, a limiter, an envelope detector and an envelope modulator. This technique split RF phase information phi(t) and amplitude information A(t) of the original signal. Phase modulated signal, having a constant magnitude, is injected to the input of a high-efficiency PA. This switch-mode PA is implemented as Class D or E which have theoretical efficiency of 100%. The amplitude information A(t) is applied to the drain of the PA through the ideal supply modulator which has the efficiency of 100%. In this way, the amplitude information and phase information are combined with 100% efficiency at the output theoretically.

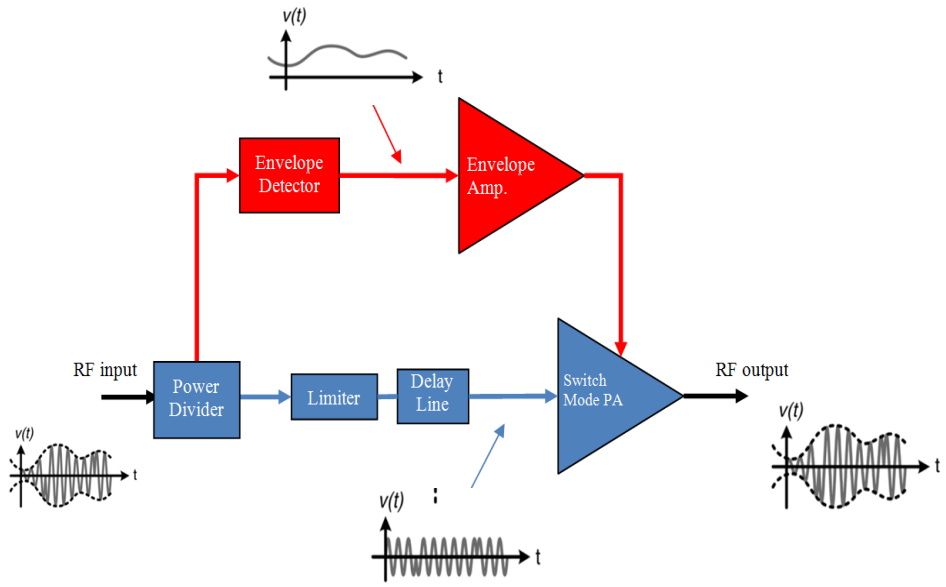



Figure 1.10: The EER configuration

Many researches on the EER PA have been reported with excellent performance. In [12], F. Wang represented an EER system used for WLAN 802.11g application. The RF bandwidth of the WLAN OFDM signal is 16.56 MHz and PAR reaches 8-10dB. The EER overall efficiency was measured as 36% at 19 dBm output power, the PAE was greater than 28%, and the linearity requirements were met by implementing the baseband pre-distortion technology and adaptive time-alignment.

In [17], Kim described maximum power generation distribution region concept. In this letter, the high-efficiency PA under the Hybrid EER operation was verified using the inverse class-F amplifier implemented in LDMOSFET at 1 GHz. Two amplifiers

were optimized at 30 V Vds and at maximum power-generation distribution region, 12 V Vds, respectively. The H-EER transmitter has been evaluated with a single-carrier WCDMA signal with a 3.84-MHz bandwidth and 9.8-dB PAPR. The H-EER transmitter using the PA optimized at the peak region had an output power of 29.2 dBm with an overall drain efficiency (DE) of 38.4%, and its overall PAE was 35.5% with a gain of 11.2 dB. On the other hand, the transmitter using the average high-efficiency PA had 2.5 dB more output power with efficiency of 41.2%, enhanced by 6.5%.

Although EER offers high efficiency in theory, it also has several problems, [13]. The first problem is the constant-envelope phase-modulated RF signal which has a very wide bandwidth, approximately ten times wider than that of the modulated signal. The second problem is very low gain in low-power regions with low power added efficiency (PAE) due to saturated operation of the switching PA. Third problem is linearity. The most important factors affecting the linearity are the envelope bandwidth and alignment of the envelope and phase modulations. As a rule of thumb, the envelope bandwidth must be at least twice the RF bandwidth and the misalignment must not exceed one tenth of the inverse of the RF bandwidth [25]. Therefore, EER has limited use in base stations and handset applications.

### 1.3.2 Envelope Tracking

The other supply modulation technique is Envelope Tracking (ET) which is a hot topic for RF designers. In this technique, drain voltage supply of the RF PA is modulated with envelope of the input signal. Although ET is very similar to EER, their characteristics are quite different owing to the RF input signal. In the case of ET, the input signal is non-constant and it uses a linear mode PA such as class A, AB or B. Therefore, although the efficiency is slightly lower than that in EER, all other problems of the EER system are solved.

The ET system's basic configuration is shown in Figure 1.11. The input RF signal is split into two paths; the envelope path and the RF path. On the RF path, the input RF signal is input into a linear RFPA. On the envelope path, the envelope of the input signal is detected and the detected envelope signal is amplified by the envelope am-

plifier. The ET technique is ideal for multimode (MM) multiband (MB) PAs because it is fundamentally immune to changes in the frequency of the carrier; it depends only on the envelope of the RF signal. Unlike the Doherty and Chireix outphasing techniques, the ET system does not require an impedance inverter. Hence, this system has a major advantage in terms of bandwidth.

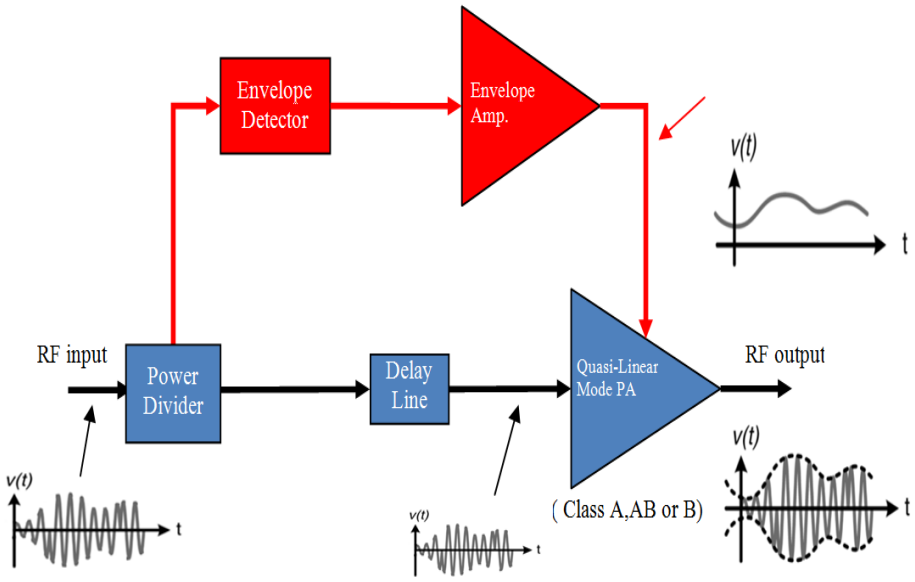



Figure 1.11: The Envelope Tracking Configuration

## 1.4 Literature Research

An envelope tracking (ET) is a suitable technique for efficiency enhancement at the back-off output power region and is implemented by many researchers. The efficiency of the envelope tracking power amplifier (ET PA) is proportional to the efficiency of the supply modulator. There are mainly three method to realize supply modulator; low-dropout (LDO) linear amplifier, switching amplifier and hybrid switching amplifier (HSA).

A linear regulator, also called a low dropout (LDO), uses variable series resistance (an active semiconductor) in a feedback loop to control output voltage Vout. This variable series resistor dissipates excess voltage. This arrangement results in a low-efficiency process of DC–DC conversion. The efficiency of the LDO decreases fur-

ther as the difference between the input and the output voltage increases. Therefore, it is not suitable for high PAPR signals. Conventional solution based on a linear regulator was compared to three different circuit architectures for the power supply in GSM and EDGE PA applications [29]. These three circuits were a hysteretic control switcher, and two linear assisted architectures: LDO+Switcher and AB+Switcher. It was shown that the three configurations have significantly better efficiency compared to the conventional solution. The configurations differ in terms of efficiency, the size of filtering components, bandwidth, and linearity.

In [14], Hanington designed a highly efficient power amplifier using GaAs MESFET and dc-dc boost converter for CDMA application with switching frequency of 10 MHz. By dynamically controlling the supply voltage of GaAs MESFET amplifier, 1.64 times higher efficiency was achieved compared to constant voltage system. The design was capable of tracking 1.22 MHz envelope bandwidth of IS-95 digital cellular standard.

In [15], Hariharan showed that conventional PWM controlled switching regulators need to have a very high switching frequency at the expense of efficiency to meet the spectral requirements of different wireless standards. A substitute architecture using 3rd order Delta-Sigma modulator with OSR of 32 met the spectral requirement of GSM with 10 dB margin and showed 8% better efficiency than the PWM system running at the same clock frequency. The feasibility of using the Delta-Sigma buck regulator for envelope tracking applications was also explored. For a 13% Vout change, the Delta-Sigma buck regulator met the spurious requirements of the GSM system. This work showed that a Delta-Sigma buck regulator with its very good spurious performance and higher efficiency is a viable alternative for powering GSM system and other wireless standards.

Today, hybrid switching amplifier (HSA) is the most popular supply modulator. The HSA is a combination of a switching amplifier and a linear amplifier, [26]. In this architecture, the switching amplifier provides the required current as a slave amplifier, while the linear amplifier accurately generates the required voltage as a master amplifier and compensates for the ripple current of the switching amplifier. Usually, the switching amplifier supplies the low-frequency component of the envelope signal

with high efficiency, and the linear amplifier provides the other high-frequency component with high speed. Since most of the power of the envelope signal is located at a low frequency, this architecture is suitable for wideband operation with high efficiency. The switcher is hysteretically controlled by the current flow from the linear amplifier. When the linear amplifier supplies a current, the switcher is turned on and vice versa.

In this paper, [10], a W-CDMA base-station power amplifier using GaN HFETs on Si substrates was presented with average efficiency of 50.7%, together with average output power of 37.2W and gain of 10.0 dB. The amplifier also showed good linearity corresponding to EVM of 1.74% and good ACLR. This high efficiency and excellent linearity was attributed to the high performance of both the GaN HFET power amplifier and the envelope amplifier. By combining a wideband linear stage and a high-efficiency switcher stage, the envelope amplifier provided high efficiency with good signal integrity. This study has demonstrated that ET power amplifiers using GaN HFETs are promising candidates for next-generation wireless communications.

By combining the robust and reliable operation of the high performance LDMOS device with an envelope tracking amplifier configuration, an amplifier has been presented that shows high efficiency and output accuracy on single W-CDMA signal, [24]. Under the influence of a WCDMA source, an average efficiency of 40.4% with average output power of 27 W and gain of 14.9 dB was achieved with an output EVM of 3.3% with memoryless DPD and better than 1.0% EVM with memory mitigation. To deal with the high PAR problem, a de-cresting procedure (adjustment of the PAR of the input signal) was employed. This procedure was performed digitally on the envelope of the signal to optimize the efficiency, adjacent channel leakage ratio (ACLR), and error vector magnitude (EVM) performance. The original W-CDMA input signal with 9.8-dB PAR was de-crested to have a PAR of 7.67 dB.

To minimize distortion by the time-delay difference between envelope and RF paths, which is known to be one of the major distortion mechanisms in EER or ET systems, [25], synchronization is performed by maximizing the amplitude and phase correlation between the input and down-converted output signals [11].

In addition to the differential delay, there are other sources of nonlinearity in the

ET amplifier such as AM–AM and AM–PM distortion created by the varying drain bias voltage. These are called AM and PM distortion, [1], and are a result of the variation of the transconductance and output capacitance of the FET with drain bias. A novel digitally assisted dual-switch envelope amplifier architecture had been presented in this paper, [6], to improve the efficiency of ET base-station PAs excited with wideband signals. This technique utilized DSP circuits to generate a switch control signal to force the main switcher providing the majority of current required by the RF PA, and used an auxiliary switcher to compensate for dc imbalance and provide low-frequency current using analog hysteretic feedback. A wideband linear stage was used at low power to maintain the envelope signal accuracy. The technique significantly improved the efficiency of the envelope amplifier, especially for applications requiring high PAPR signals. The overall system was demonstrated by using GaAs high-voltage HBT PAs. For a variety of signals ranging from 6.6- to 9.6-dB PAPR and up to 10-MHz RF bandwidth, the overall system PAE exceed 50%, with normalized root-mean-square errors below 0.8% and the first adjacent channel leakage power ratio (ACLR1) of 55 dBc after digital predistortion with memory mitigation, at an average output power above 20 W and over 10-dB gain.

In [9], a highly efficient dual-switch hybrid switching supply modulator for an envelope tracking power amplifier was presented. The supply modulator had a combined structure of a linear amplifier and a switching amplifier. The switching amplifier is generally controlled by a basic control method such as a hysteretic comparator or a PWM controller. For an improved efficiency, a new control technique for the switching amplifier was proposed. The switching amplifier employed two buck converters and realized an adaptive slew rate control of the switching amplifier's current. An implemented envelope tracking PA delivers an efficiency of 39.1% at an output power of 27 dBm for long term evolution signal (LTE) with 10 MHz channel bandwidth.

Instead of using traditional HSA, another novel supply modulator was also presented in this paper, [31]. This GaN MOSFET supply modulator for envelope tracking power amplifier was optimized for ultra wide band up to LTE 60 MHz. It contains five parts as fast envelope detector, small signal gain blocks, GaN stage driver, final GaN totem pole stage and sigma-delta modulation buck switcher with filtering. The sigma-delta modulation is inherently linear and with the effects of oversampling and noise shap-

ing, the output low frequency components are with high efficiency, better linearity and signal quality at the expense of sophisticated output re-construction filter design. Also to alleviate the serious distortion issue in wide band scenarios, a compatible feed forward loop to linearize the modulator was proposed and verified by SPICE simulation, which is for the sake of realizing high efficiency trading off linearity.

## 1.5 Comparison of Efficiency Enhancement Techniques

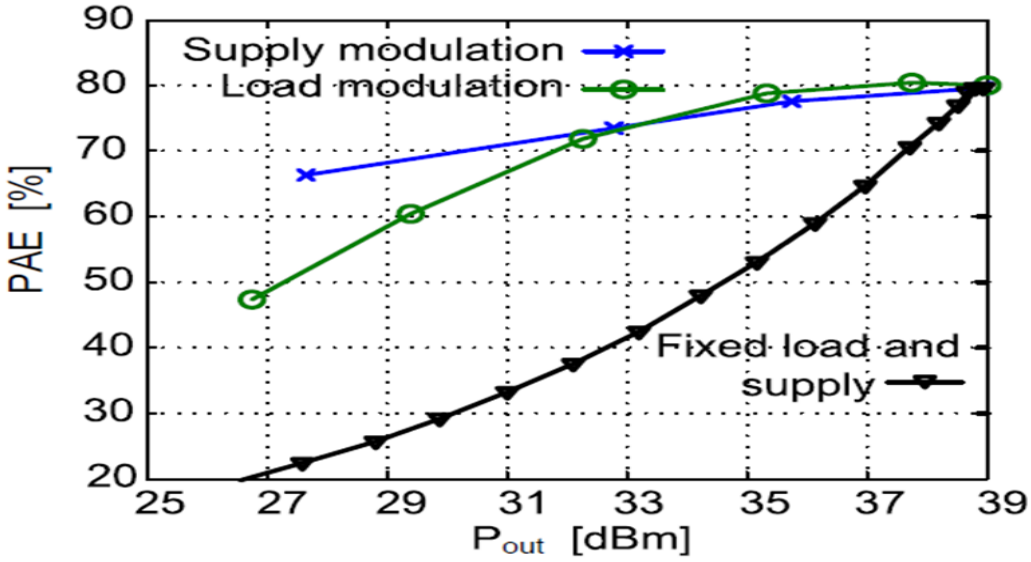



Figure 1.12: Comparison between the PAE results achieved for the supply and load modulation cases versus Pout. The results with fixed load impedance and supply voltage are also included for reference. (derived from [16] )

In Figure 1.12, derived from [16], comparison between the PAE results for the supply and load modulation is plotted in blue and green, respectively. As shown in this figure, from 6.5 dB back-off level to peak power level, both techniques perform almost equally well. However, at 10 dB back-off, supply and load modulation provide a power-added efficiency (PAE) of 68%, and 58%, respectively which means that at higher back-off levels, the supply modulation can improve the PAE of the GaN transistor more than the load modulation. The reason is the different loss mechanisms in each of the techniques. The losses in the load modulation are mainly due to the parallel losses rather than series losses which are dominant in the supply modulation.

In conclusion, supply voltage modulation techniques should be preferred when high PAPR input signals are used.

## 1.6 Research Objectives and Organization of the Thesis

Efficient amplification of RF signals with high PAPR is very important topic for researchers. Various power amplifier architectures have been demonstrated. With the growth of new generation services, ET technique has drawn a lot of attention. The reason is the fact that at higher back-off levels,such as 10 dB, the efficiency improvements achieved by ET PA outperform the other methods.

In this thesis, the fully analog ET PA at 900 MHz is designed, produced and tested with W-CDMA 5 MHz, 9.17 dB PAPR. This systems consists of the RFPA and the envelope amplifier. Many studies have been published on ET PAs. However, most of them have focused on the PA and envelope amplifier separately. To maximize the efficiency of the system, the link between them is examined carefully.

This dissertation consists of six chapters which are organized as follows:

In introduction chapter, the efficiency degredation of the linear mode PA's and necessity of the efficiency enhancement techniques were discussed. Two main techniques in the literature, load and supply modulation, were introduced. To show the importance of the supply modulation, comparison of the techniques was included.

In Chapter 2, ET system is deeply investigated. The main blocks of the system are defined and efficiency formulas are given. Since the overall efficiency of an ET PA is the multiplication of the RF PA efficieny and envelope amplifier efficiency, a broadband and efficient supply modulator is indicative of the overall efficiency. This chapter also includes the design, implementation and tests of the medium power Class-AB amplifier. MW6S010N, 10W CW LDMOS from Freescale, is used as transistor.

In Chapter 3, broadband and efficient envelope amplifier design, implementation and tests are done. Envelope amplifier consists of three parts; linear amplifier stage, switch mode amplifier stage and sensing stage. Each stage is carefully designed with the CAD program, LTspice. After the implementation on the PCB, it is tested with

resistive load.

To better understand the ET operation, simulations with ADS is done in chapter 4. Memory effect of the PA, which was designed at chapter 2, is tested with two tone harmonic balance simulation. Fixed drain bias PA is simulated with W-CDMA input signal. Shaping table is derived from constant gain curve. Finally, ET is implemented and efficiency improvement is shown.

Chapter 5 presents the overall system test of the ET PA. 5 MHz WCDMA signal with 9.7 dB PAPR is used as an input. Efficiency and ACPR measurements are tabulated.

In Chapter 6, the dissertation is concluded with a summary of this work. Future works are discussed.

# CHAPTER 2

# ENVELOPE TRACKING SYSTEM

## 2.1 Theory of Envelope Tracking

In conventional constant bias power amplifiers, like class A, AB or B, the maximum efficiency occurs at saturation, with a single-tone signal as depicted in Figure 1.1. As the output power of the power amplifier backs off from the saturation point, the efficiency degrades. This creates an issue in the presence of high PAPR signals where the envelope of the transmitted signal varies as a function of time. Thus, the difference between the DC power provided and the envelope power transmitted can be characterized as energy dissipation, as depicted in Figure 2.1.

The theory behind the Envelope Tracking (ET) can be understood by considering the transistor biasing of the power amplifiers. Figure 2.2 shows the voltage and current waveforms and load lines of a class-A PA, class-B PA, and class-B ET PA. The black solid lines represent the case of maximum linear output power (Pout.max), and the gray solid lines represent the case with output power (Pout) that is tenth of Pout.max (10 dB lower Pout). In this figure, zero knee voltage and uniform transconductance ( gm) are assumed to simplify calculation.

When the class-A PA delivers tenth of Pout.max, its dc power consumption does not change and its efficiency is significantly degraded by the fixed Vdc and Idc where Vdc is the the DC supply voltage. So the drain efficiency of Class-A at 10 dB back-off condition will be given by;

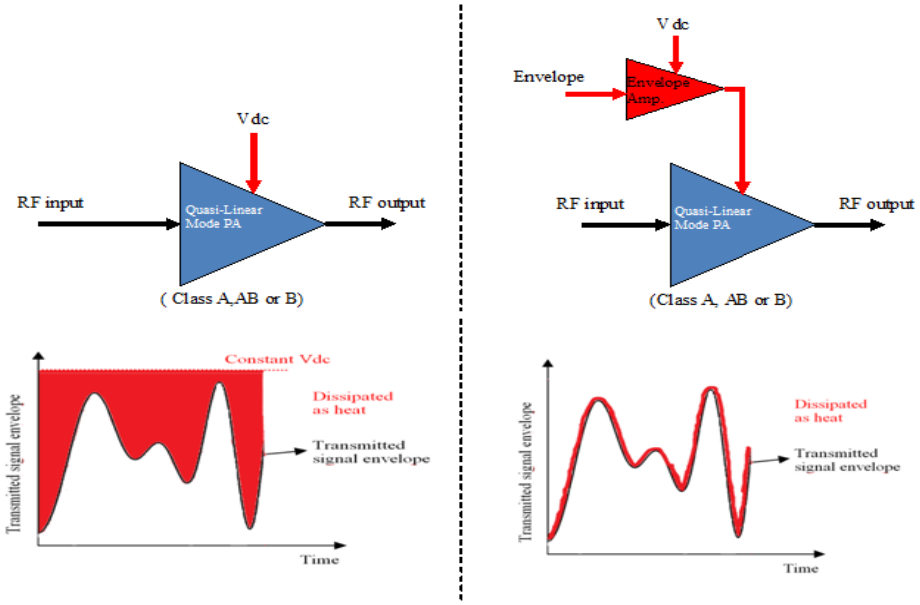



Figure 2.1: Block diagram of constant supply power amplifier (left) and the envelope tracking power amplifier (right) and comparison of the energy dissipation

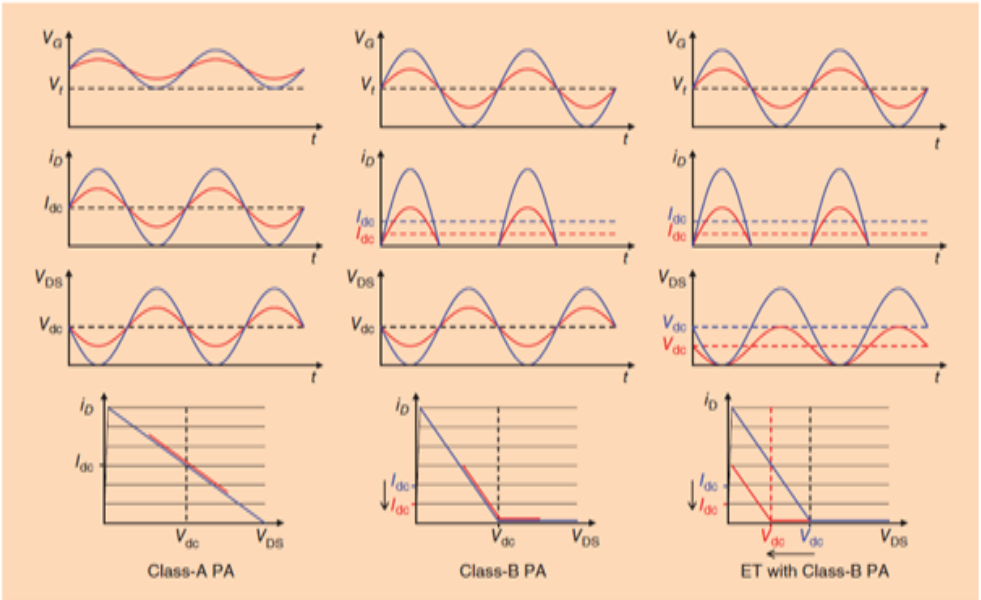



Figure 2.2: The voltage-current waveforms and load lines of a class-A PA, class-B PA, and class-B ET PA

$$n(classAat10dBPBO) = 0.5\frac{Pout}{Pout.max} = 5\% \ , \tag{2.1}$$

For the class-B PA, Idc decreases as Pout decreases, but Vdc is fixed. Its efficiency decreases much slower than that of the class-A PA because of the decreased Idc, which is proportional to the square root of Pout. So the drain efficiency of Class-B at 10 dB back-off condition will be given by;

$$n(classBat10dBPBO) = \frac{\Pi}{4}\sqrt{\frac{Pout}{Pout.max}} = 25\% \ , \tag{2.2}$$

For the class-B ET PA, Vdc is modulated by the supply modulator and Idc is automatically controlled by the class-B bias. Therefore, its efficiency is constant for the entire output power range. Under the assumption of zero knee voltage and an ideal supply modulator,

$$n(ETclassBat10dBPBO) = \frac{\Pi}{4} = 78.5\% \ , \tag{2.3}$$

Figure 2.3 depicts the efficiencies of the three PAs according to Pout for ideal case of Vknee=0. The class-B ET PA has efficiency of 78.5 % for all output power range by tracking peak efficiency points of the class-B PA.

## 2.2 Hybrid Envelope Amplifier

Its simplified schematic is shown in Figure 2.4. It can be seen as comprising of a switching stage and a linear stage. They work together in parallel with a hysteresis control scheme to deliver the amplified envelope signal.

The switching stage will efficiently supply most of the output power, since most of the power in the envelope is at low frequencies, while the linear stage will have a much higher bandwidth, and maintains the output signal integrity. The Rload and Cload here represent a simplified model of the drain of the PA. This model of the PA assumes that the envelope amplifier closely tracks the output envelope, and the value of Rload is dependent on the power level. To get a better idea of how the linear stage

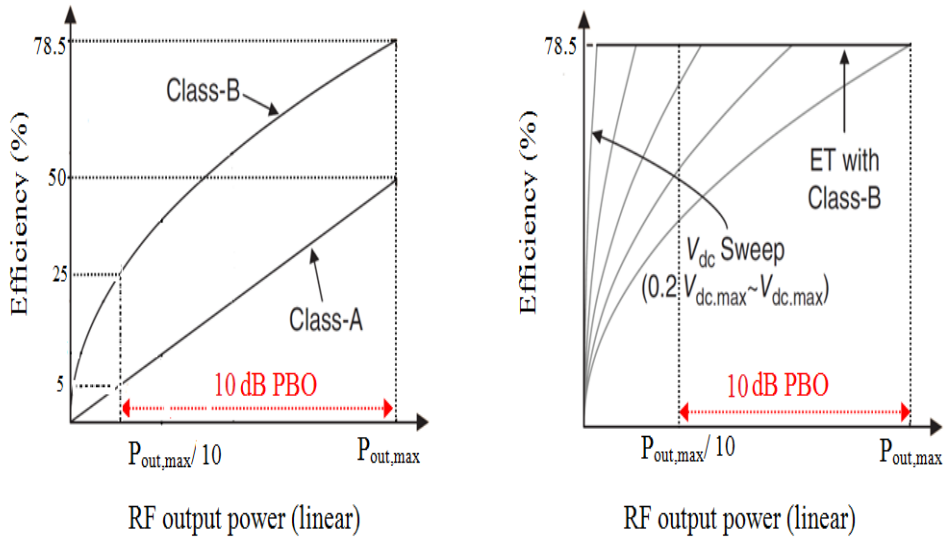



Figure 2.3: Efficiency curves of class-A PA, class-B PA and class-B ET PA

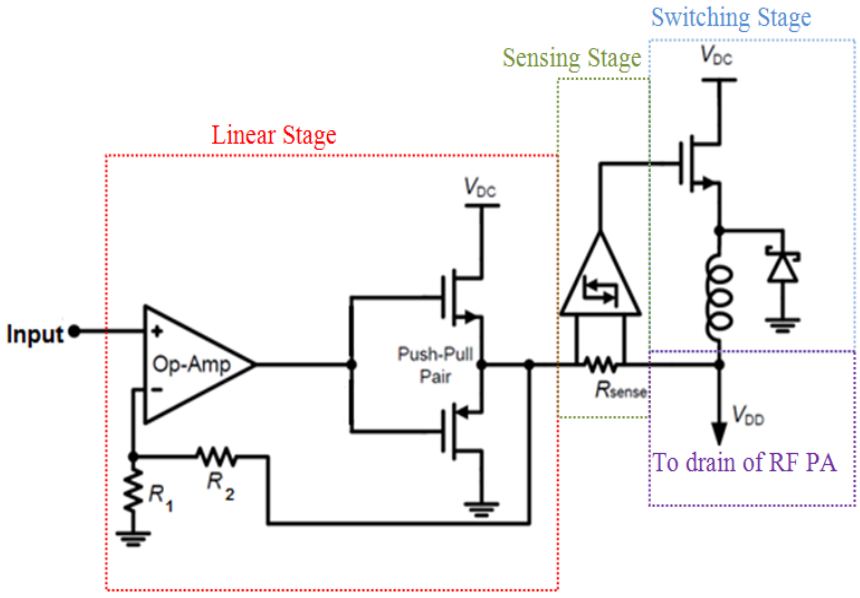



Figure 2.4: Simplified schematic for the hybrid envelope amplifier

and the switching stage works together, the whole process can be roughly described with two states in Figure 2.5.

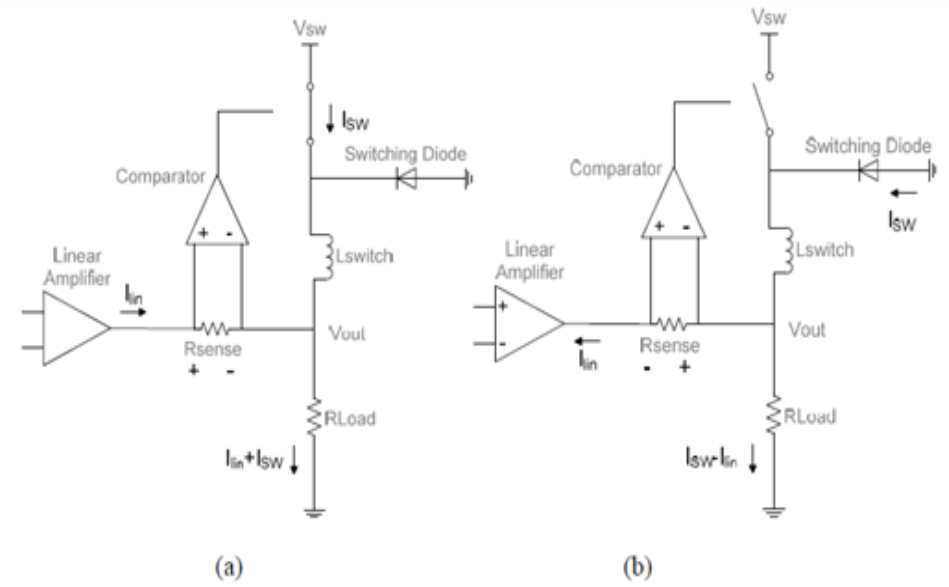



Figure 2.5: Hybrid envelope amplifier topology's (a) state1 and (b) state2

During state 1, a signal is input into linear amplifier so that it starts to supply current to Rload , causing a voltage to form across Rsense . This turns on the switching transistor, and a current starts to be drawn from the voltage source Vswitch into the load through inductor Lswitch until all of the current is now being supplied by the switching stage.

Once the current flowing through Lswitch becomes greater than the output current, the amplifier goes into state 2 where the linear amplifier will start to sink current in order to maintain the correct output voltage. This creates a negative voltage across Rsense that causes the comparator to turn off, thus closing the switching transistor. The current through Vsw now comes from the switching diode, and starts to fall until it is below the actual output current. This whole process is repeated each period.

For the envelope amplifier, the efficiency can be described as

$$n_{EA} = \frac{P_{out}}{P_{DCin}} = \frac{P_{out}}{P_{out} + P_{loss}} , \tag{2.4}$$

where Pout is the amplifier's average output power and Ploss represents total power loss inside the envelope amplifier. The circuit simulator can simulate the power loss by extracting and calculating the transient current and voltage of each stage.

$$P_{loss} = P_{staticloss} + P_{dynamicloss} \ , \tag{2.5}$$

Where Pstaticloss refers to any power consumption of the biasing circuit inside the envelope amplifier, such as the bias current of the linear stage, the sensing stage and the switcher stage driver. The static power loss is independent of the amplifier's output power. By properly selecting low power devices, the static power loss can be reduced. Pdynamicloss has a complicated loss mechanism. Linear stage and switcher stage dynamic loss mechanisms should be analyzed separately. The efficiency of the envelope amplifier is highly correlated with the unique properties of envelope signals, which can be utilized to improve the envelope amplifier's overall efficiency significantly. An efficient switcher stage is employed for the low-frequency component,where the majority of signal power is concentrated, while the wideband, but comparatively inefficient linear stage is used for the high-frequency component. Chapter 3 will give a detailed analysis and modeling of the high efficient hybrid envelope amplifier.

### 2.2.1 Linear Stage

The linear stage can be realized with an output stage corresponding by a rail-to-rail push-pull configuration as shown in Figure 2.6.

The load and the switch stage are respectively simplified as a resistor and a DC current source. Referring to Figure 2.6, the linear stage dynamic power loss can be estimated by (2.8)

$$P_{linloss} = P_{NMOSloss} + P_{PMOSloss} \tag{2.6}$$

$$P_{NMOSloss} = (V_{DC} - V_{out}) * (I_{out} - I_{sw}) \qquad \text{if Iout>Isw} \tag{2.7}$$

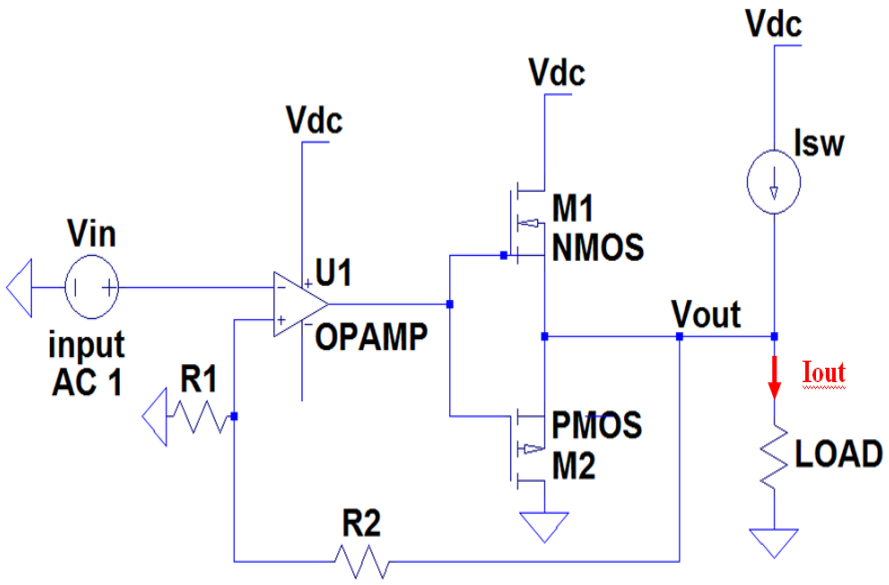



Figure 2.6: Simplified linear stage

$$P_{PMOSloss} = V_{out} * (I_{sw} - I_{out}) \qquad \text{if Isw>Iout} \tag{2.8}$$

Where VDC is the supply voltage, Vout is the output voltage at the load, Isw is the switcher stage current, and Iout is the drain current flowing into the RF PA.

### 2.2.2 Sensing Stage

The sensing stage, in Figure 2.7, is used to turn on and off the switcher MOSFET by sensing the current flowing into or out of the linear stage. This stage has considerably large effect on the efficiency of the overall envelope amplifier. A very low ohmic value current sensing resistor $R_{sense}$ is implemented to sense current flowing through a resistance between the linear stage and the overall envelope amplifier outputs. Comparator with internal hysteresis is used to detect the voltage difference between the terminals of $R_{sense}$.

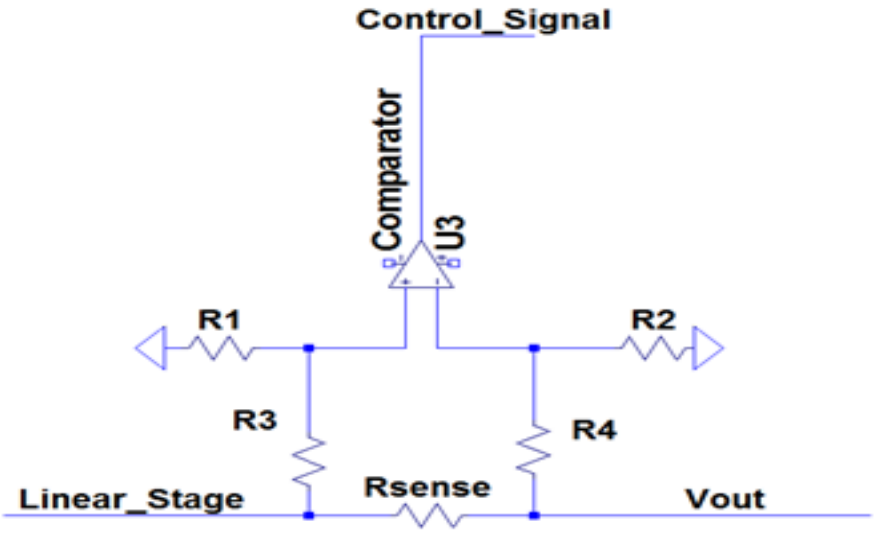



Figure 2.7: Simplified sensing stage

### 2.2.3 Switching Stage

Figure 2.8 shows the topology of the switcher stage, which is composed of a driver, a switching power MOSFET, a Schottky diode, and a power inductor.

The power losses in the switching power MOSFET and Schottky diode are the combination of the switching losses and the conduction losses, as shown in 2.9.

$$P_{SWloss} = P_{switchingloss} + P_{conductionloss} \tag{2.9}$$

$$P_{switchingloss} \approx Q_G * V_{GS} * f_{sw} + 12 * I_D * V_{DC} * (t_{on} + t_{off}) * f_{sw} + 12 * C_{out} * V_{DC}^2 * f_{sw} \tag{2.10}$$

$$P_{conductionloss} = D * I_D^2 * R_{ON} + (1 - D) * I_L * V_F \tag{2.11}$$

where $Q_G$ is the gate charge of the switching power MOSFET
$V_{GS}$ is the gate-to-source turn-on voltage of the switching power MOSFET

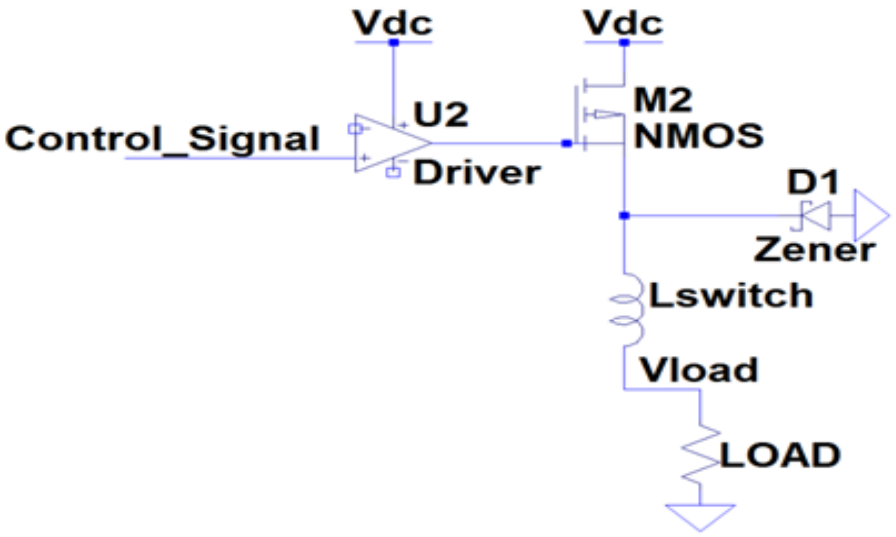



Figure 2.8: Simplified switching stage

$f_{sw}$ is the average switching frequency

$I_D$ is the drain current when the switcher is on

$t_{ON}$ is the switcher turn-on time

$t_{OFF}$ is the switcher turn-off time

$C_{out}$ is the total output capacitance at thesource of the switching power MOSFET

D is the average duty cycle ratio of the switching pulse

$R_{ON}$ is the "on"resistance of the switching power MOSFET

$I_L$ is the load current when the switcher is off and the Schottky diode is conducted

$V_F$ is the forward voltageof the Schottky diode

The switching losses consist of gate charge loss, commutation loss, and output capacitance switching loss of the power MOSFET during switching. (2.10) estimates each portion. The gate charge loss is proportional to the device gate charge and the switching frequency. Generally, the larger size of the device, the larger the charge and the loss. For the second term,$t_{ON}$ and $t_{OFF}$ can be estimated through the gate charge diagram provided from the device datasheet. The third term depends on the output capacitance of the power MOSFET, diode and associated paralleled devices. This loss is proportional to the area of the power MOSFET and the diode as well as

the switching frequency.

(2.11) estimates the conduction loss of switching power MOSFET and Schottky diode. The power MOSFET's $R_{ON}$ dominates the power loss. The conduction loss is generally inversely proportional to the MOSFET size and scales with the switcher's output power. In the second term, the maximum forward voltage drop $V_F$, dominates the major power consumption in the diode. Choosing a smaller $V_F$ Schottky diode helps to decrease the power loss during the operation.

$$f_{sw} = \frac{R_{sense} * V_{out} * (V_{DC} - V_{out})}{2 * V_{DC} * L_{switch} * V_{hyst}} \qquad [18] \qquad (2.12)$$

The overall and each stage power loss and efficiency can be calculated using the transient circuit simulation results, which will be analyzed in Chapter 3 in detail.

## 2.3 Class-AB RF PA Design

When designing the power amplifier, some initial design considerations have to be taken into account before doing any simulation or fabrication. The first step is to choose the device to be used, in which the power rating, operating frequency and the transistor technology are determined. The second step is to choose the RFPA mode of operation and the operating bias condition. The third step is to check the device stability at the operating frequency of interest. All these steps are necessary in any RFPA design.

For the RFPA design, the 10W LDMOS MW6S010N from Freescale is chosen because this technology has been widely used in the communication industry. As mentioned in the datasheet, this 10W LDMOS offers a typical operating voltage of 28V and maximum drain voltage of 65V. This power transistor is produced for base station applications at frequencies from HF to 1500MHz. In order to show any improvement in the RFPA performance, it was decided to operate the RFPA in the Class AB region; a compromise choice between the classical linear Class A mode and the classical efficient Class B mode. The nonlinear device model that is provided by Freescale was used in the non-linear simulator ADS, the computer-aided design (CAD) tool from

Keysight.

To plot the DC I-V curve of the device, the schematic of Figure 2.9 is constructed. The results can be seen from Figure 2.10. The gate bias voltage is chosen so that the quiescent drain current, $I_{DQ}$ , is 125mA corresponding to quiescent gate voltage of 2.8V which is marked with marker m2.

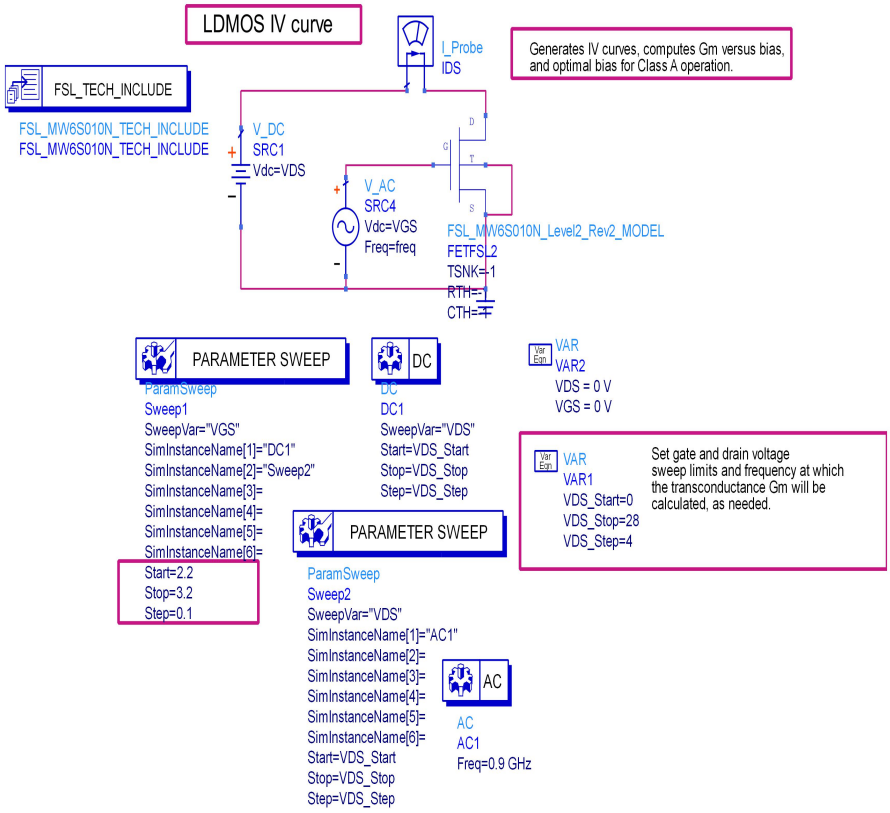



Figure 2.9: The schematic of the device to plot the DC I-V curve

After the device has been chosen and the mode of operation has been decided, the device is now simulated to find its optimum impedance. The first simulation step is to perform a harmonic balance one tone load pull simulation, Figure 2.11. The load pull is defined as an analysis by using a set of contours on a Smith chart where load impedances on the contours are analyzed on the achievable optimum output power on the contours. The optimum matching impedance is found by calculating the optimum output power, the power-added-efficiency (PAE) and the drain efficiency at a specified

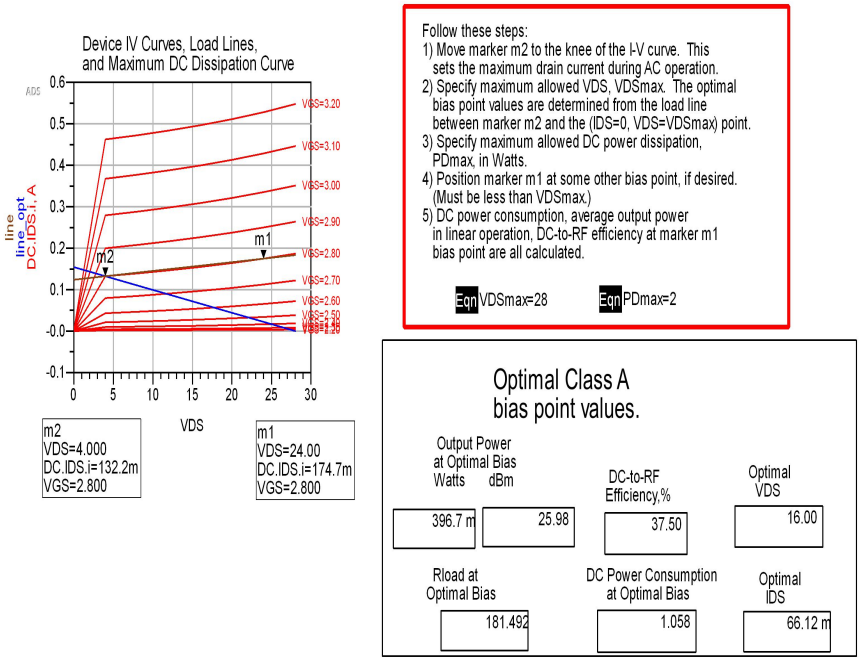



Figure 2.10: The device DC I-V curve

coverage radius. In Figure 2.12, results of the load pull simulation can be seen which will be used to design the input and output matching networks.

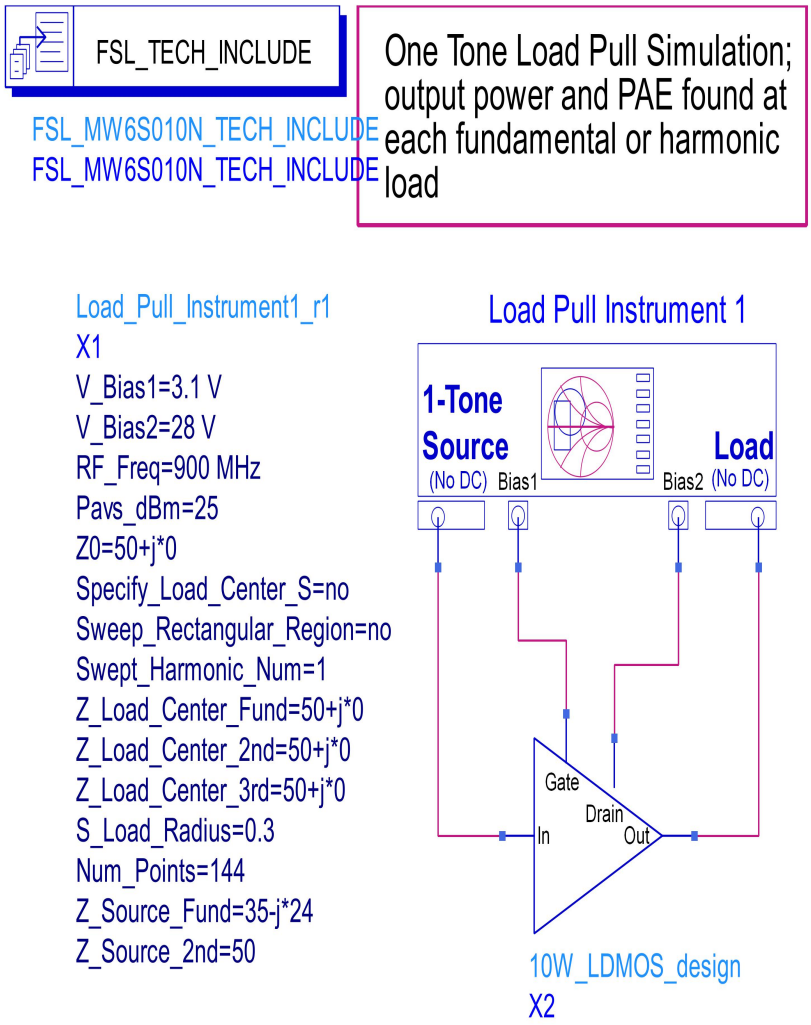



Figure 2.11: The harmonic balance one tone load pull simulation schematic

Figure 2.13 shows the relation between the PAE and output power.

When designing RFPAs, the impedance matching network is required to maximize the power transfer for specific gain and output power. The matching network is also needed to minimize any reflection coming from the load or source so that the device can operate with best performance. There are two impedance matching networks in RFPA design, namely the input matching network (IMN) and output matching network (OMN). IMN is the network to match the source impedance and the device input impedance while OMN is the network to match the device output impedance

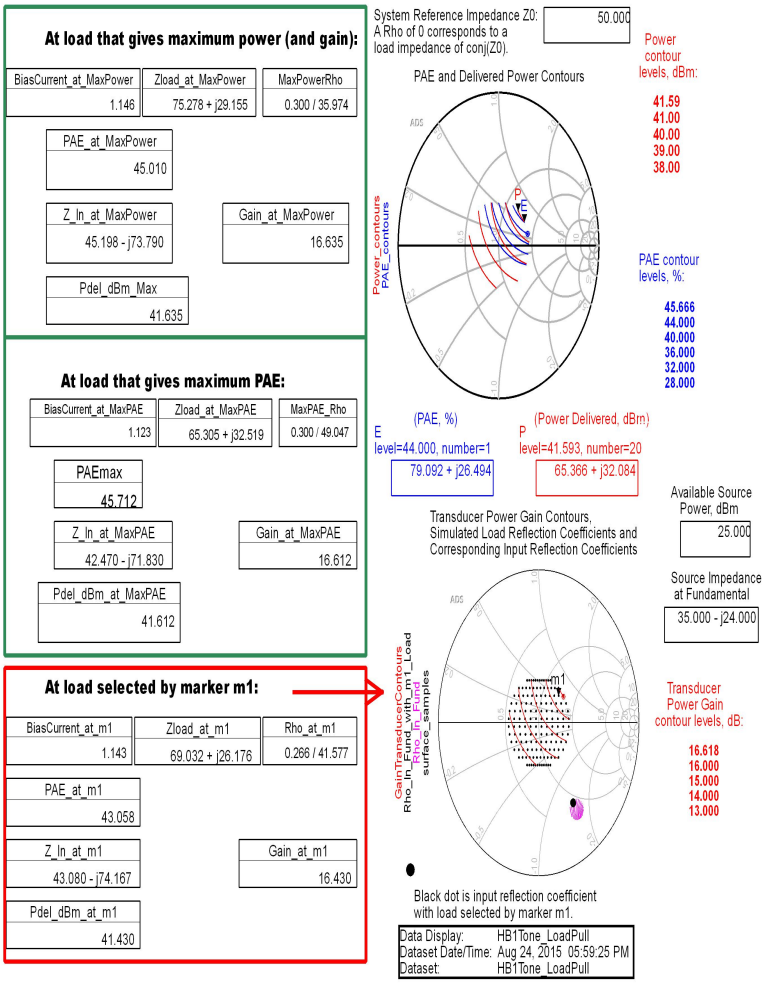



Figure 2.12: The harmonic balance one tone load pull simulation results

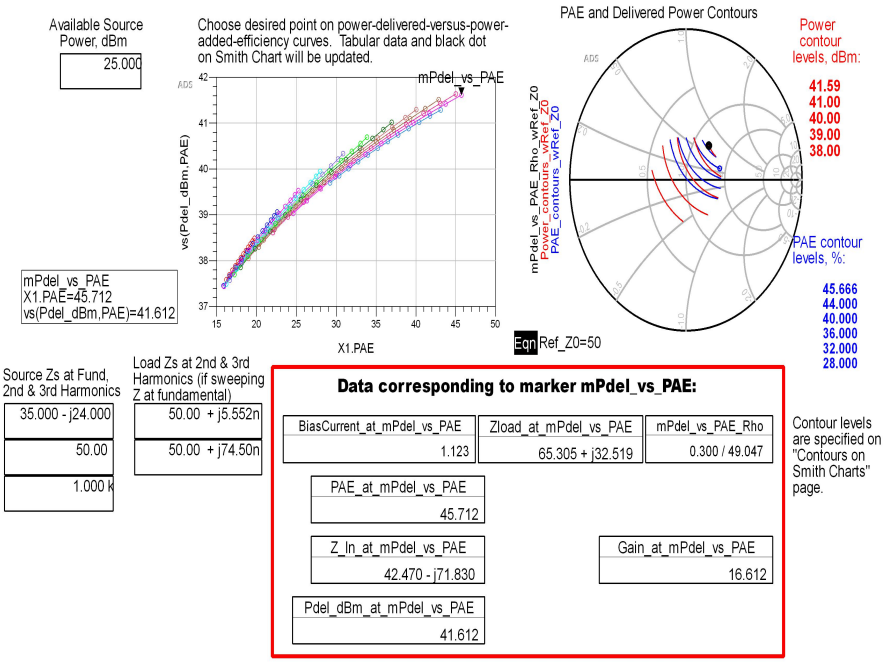



Figure 2.13: Output power vs. PAE curve

and the load impedance. Both source and load impedance environment is the standard 50Ω. There is a series of ADS simulation performed in the process of designing the final IMN and OMN. In each simulation step the elements in the matching network and the bias network are tuned for performance and stability. The finalized schematic which includes IMN,OMN and high frequency laminate can be seen from Figure 2.14.

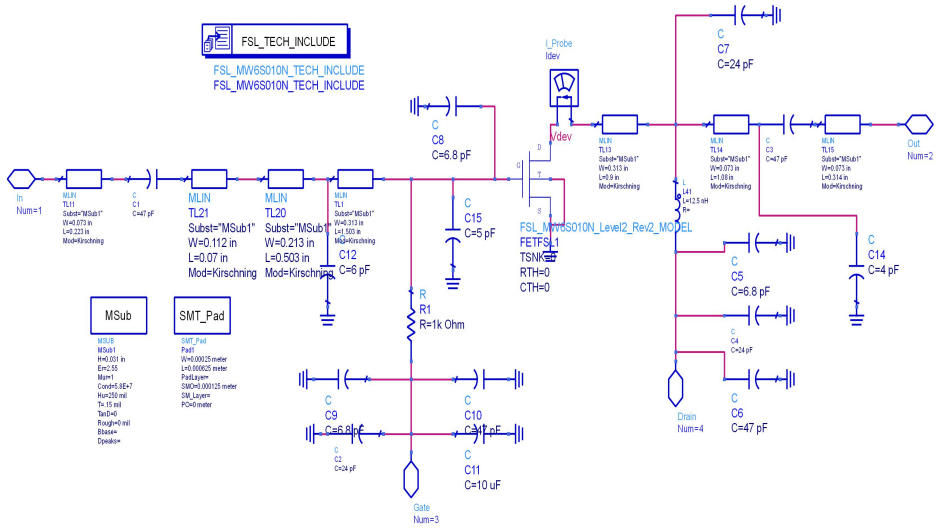



Figure 2.14: 10W LDMOS RF PA design with matching networks

The layout of the RFPA, Figure 2.15, is drawn based on the properties of the high frequency laminate which is RO4003 with 0.8mm thickness. Finally, the complete fabricated RFPA with the passive components connected is also shown in Figure 2.16.

The measurement results of the fabricated RFPA is plotted with many cases. As can be seen in Figure 2.17, 28V biased RFPA's output power can reach 40 dBm at 900 MHz with 19 dB gain. However, when drain voltage is swept, gain is compressed to 12 dB and maximum output power becomes 33 dBm for 8V bias voltage. This shows

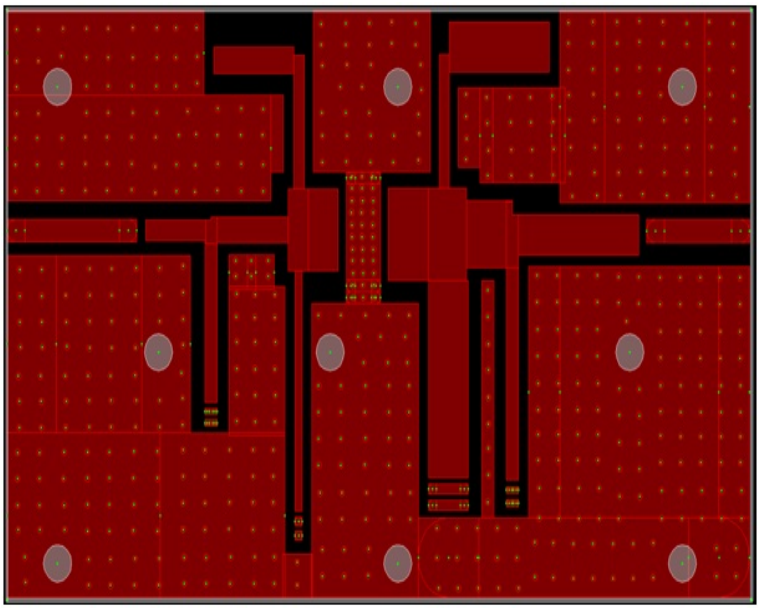


Figure 2.15: Layout of the designed RFPA with 0.8mm RO4003 as a laminate

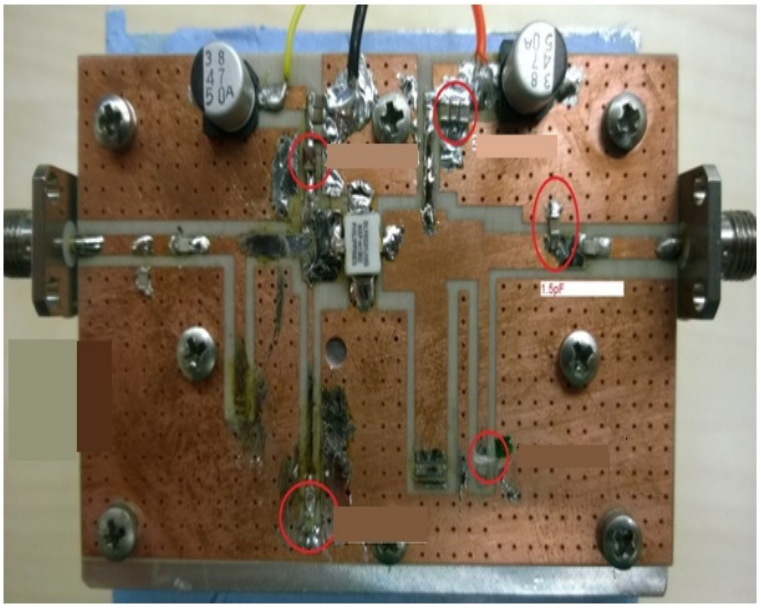



Figure 2.16: The photo of the 10W LDMOS Class AB RFPA

that performance of the RFPA highly depends on the drain voltage which is an important practical PA design problem. The nonlinear behavior of the output capacitance as a function of the supply voltage allows proper output matching only for a limited drain voltage range.

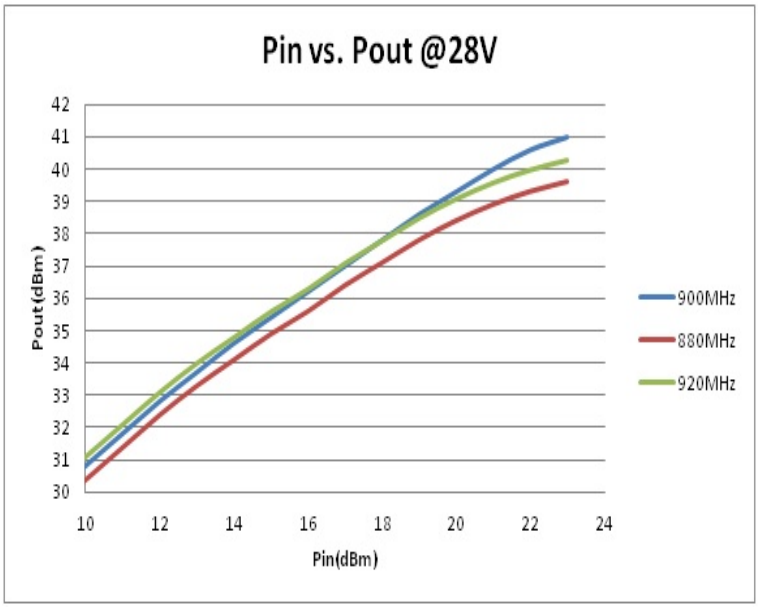



Figure 2.17: Measured Pin vs. Pout for RFPA @ 28V bias

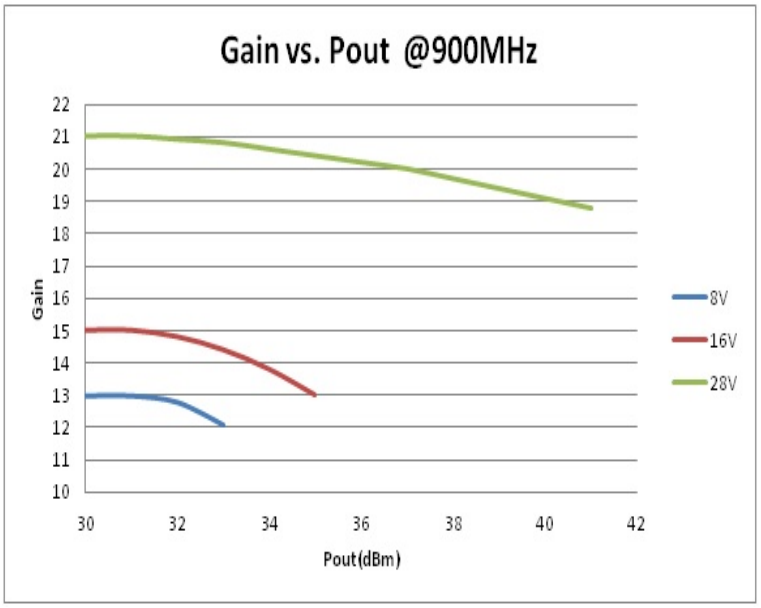



Figure 2.18: Measured Gain vs. Pout for RFPA @ 900 MHz with different drain bias voltages

# CHAPTER 3

# HYBRID ENVELOPE AMPLIFIER DESIGN, IMPLEMENTATION AND TESTS

In the envelope tracking system, the envelope amplifier design is one of the biggest challenges for practical applications. In this research, a broadband envelope amplifier is designed, which consists of a fast linear stage, a sensing stage and a efficient switcher stage. The optimum choice of the envelope amplifier is a hybrid architecture because of the characteristics of the input envelope signal. Taking the 5 MHz WCDMA envelope spectrum as an example, as shown in Figure 3.1 and Figure 3.2, more than $60\%$ of the power is concentrated at DC and extremely low frequency near DC. The band beyond 5 MHz occupies less than $15\%$ of the overall signal power.

The above power characteristic of the envelope signal implies that a hybrid envelope amplifier should achieve higher efficiency over a wide bandwidth. Hybrid means it combines both the linear stage and the switcher stage, as shown in Figure 2.4. The linear stage provides a voltage source, which amplifies the envelope input with certain gain to maintain the linearity. Meanwhile, the switcher stage is a current source, which provides the majority of the envelope power at low frequency. The sensing stage is employed to coordinate the output power portion between linear and switcher stage. The important thing is that most of the current must be supplied by the switching stage to maximize the efficiency. This is accomplished with the switching inductor, $L_{sw}$. Inductor value changes the switching frequency of the switching stage. Switching frequency was given by 2.12 in chapter2. Therefore, to minimize the switching frequency, depending on the bandwidth of the envelope signal, not the center frequency of carrier signal, the inductor value should be changed.

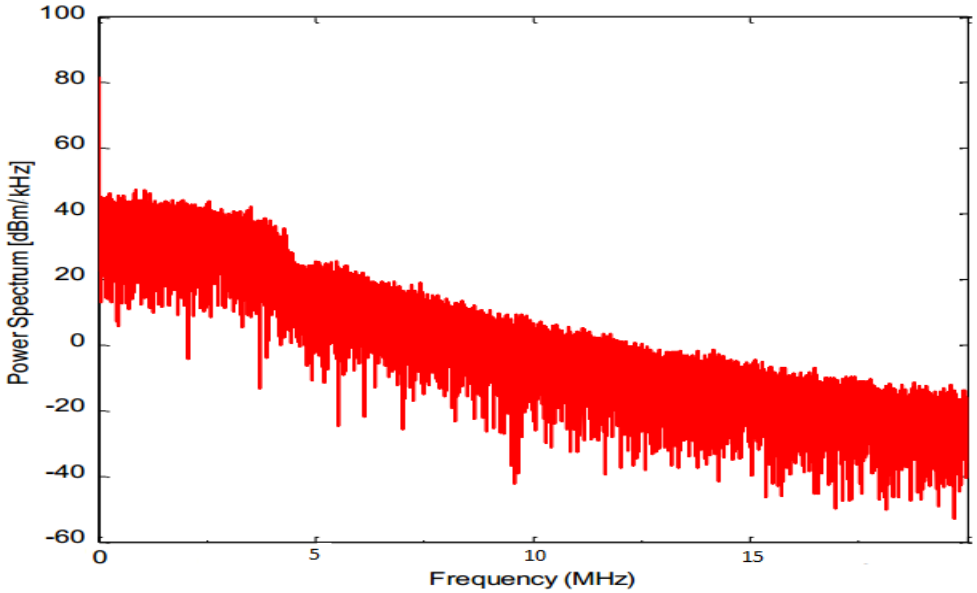



Figure 3.1: 5MHz WCDMA Envelope Signal Power Spectrum

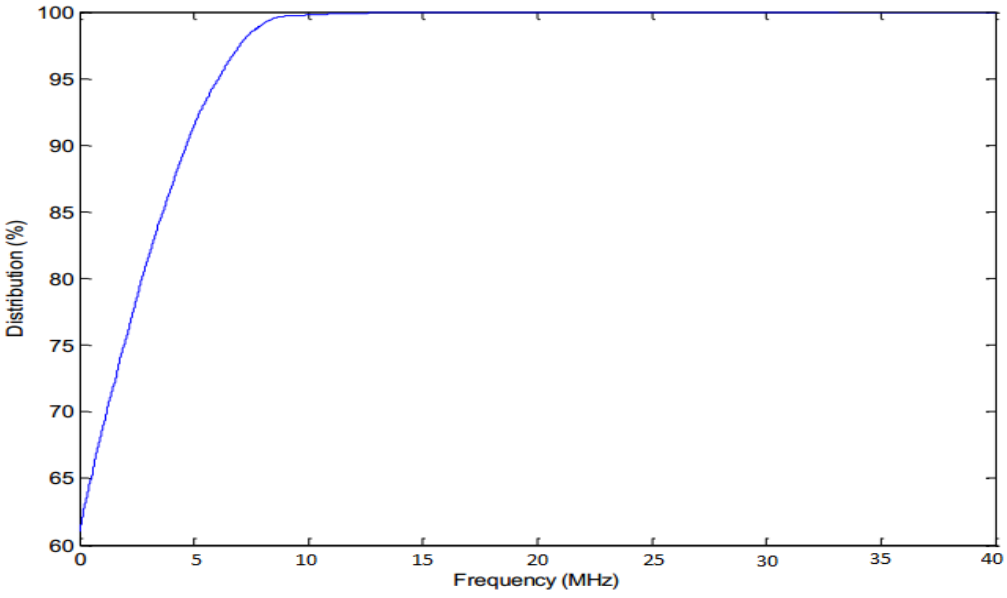



Figure 3.2: 5MHz WCDMA Envelope Signal Power Cumulative Distribution

Figure 3.3 shows the abstracted hybrid circuit model of the envelope amplifier. The output voltage $V_o$, is controlled by the voltage source (linear stage). The output current $I_{out}$ is a combination of the linear stage $I_{LIN}$ and the switch stage $I_{SW}$.

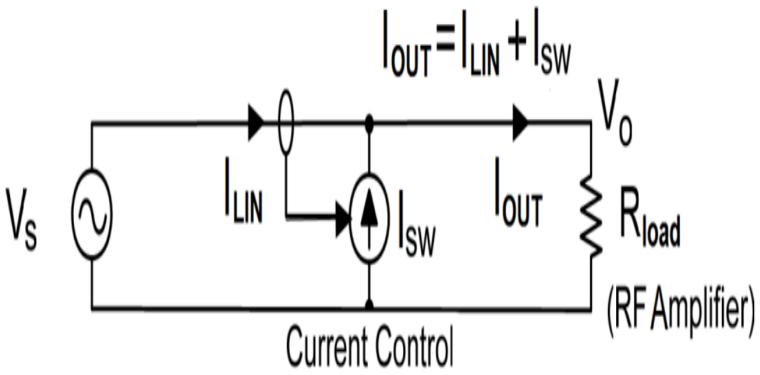



Figure 3.3: The Circuit Model of Hybrid Envelope Amplifier

As shown in the envelope amplifier circuit diagram Figure 3.3, an operational amplifier (op-amp) is employed as the linear voltage source and a switching buck converter is employed as the current source. The sensing stage is composed of a current sense resistor $R_{sense}$ , which senses the linear stage current $I_{LIN}$ , and a hysteresis comparator to control the switching buck converter, which consists of a N-channel power MOSFET, a Schottky diode, and a power inductor. When the NMOS switcher is turned on, the voltage at the cathode of the diode pulls up to $V_{DC}$ and at that time the Schottky diode is off. When the NMOS switcher is turned off, the big inductor tends to pull out the current from Schottky diode and thus the diode is on. The current flowing back and forth through the linear stage is minimized as an error signal due to the current feedback. This operation principle is accurate when the switching noise generated by the switcher stage is filtered out in the linear stage and the input envelope signal doesn't exceed the slew rate limitation of the switcher stage.

The purpose of the envelope amplifier design is to maximize the circuit efficiency and bandwidth, while at the same time to maintain the linearity of the envelope signal. Therefore, in the following parts, the design of each stage will be guided by this rule.

## 3.1 Fast Linear Stage Design

Figure 3.4 shows the fast linear stage schematic, which includes two stages: an op-amp gain stage and a classical push-pull output stage. A feedback network is also essential in the linear stage.

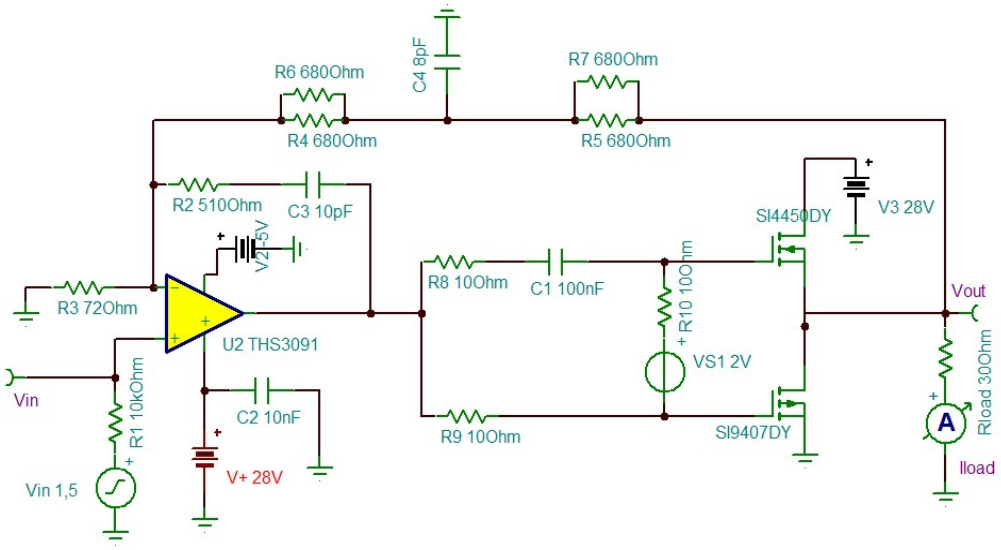



Figure 3.4: The fast linear stage schematic

The gain stage is the first critical part in the envelope amplifier. The criteria of choosing the op-amp are:

- High output dynamic range, i.e., $V_{outmax}$ and $I_{outmax}$
- High gain-bandwidth (GBW)
- High slew rate (SR) for high speed

Several commercial op-amps are listed in Table 3.1. From the list, the current feedback op-amp THS3091 is the best choice, due to its best performance in the specifications mentioned above.

For the output stage, the push-pull circuit is a good choice, because it consists of two source followers driving the same load. It can both source and sink current. The

Table 3.1: High Speed Opamp

| Part no. | $V_{outmax}(V)$ | $I_{outmax}(mA)$ | GBW(MHz) | Slew Rate (V/$\mu$sec) |
|---|---|---|---|---|
| THS3091 | 30 | 250 | 235 | 7300 |
| THS3062 | 30 | 145 | 300 | 7000 |
| LMH7171 | 36 | 100 | 220 | 4100 |
| LT1226 | 36 | 7 | 1000 | 400 |
| ADA4870 | 40 | 1000 | 70 | 2500 |
| AD818 | 36 | 50 | 130 | 500 |

choice of the power MOSFETs for this pair is determined by the output peak current to be handled by the linear stage. For this ET PA application, the maximum linear stage current can be up to 1 A, therefore, the NMOS and PMOS can be implemented by Vishay's SI4450DY and SI9407DY, respectively, because they both support up to 2A and up to 60 V maximum drain source voltage. More importantly, they have relatively low gate charge $Q_{GS}$and a balanced figure of merit (FOM), which could be defined as the product of turn-on resistance $R_{DSon}$ and reverse transfer capacitance $C_{rss}$. A detailed comparison of key parameters will be tabulated in Switcher stage section.

One disadvantage of the push-pull output is the zero-crossing distortion. Therefore, according to the gate threshold voltages $V_{th}$ noted in the datasheets, about 2V DC bias is added between two gates of the output pair. At the chosen bias point, the power MOSFETs pair will be initially conducting, such that the transistors move into a class AB bias without the dead-zone. But too much DC bias (higher than 4 V) is dangerous, because the transistors will go into thermal runaway as they heat up.

The dual feedback network is used to stabilize the linear stage with specific gain. The network functions as a crossover passive filter. The gain of linear stage, together with design of the filter cut-off frequency, is shown in (3.1) and (3.2).

$$A_v = 1 + \frac{R_4||R_5 + R_9||R_{10}}{R_3} \qquad \text{at low frequency} \tag{3.1}$$

$$A_v = 1 + \frac{R_6 + R_3||R_4||R_5}{R_3||R_4||R_5} \qquad \text{at high frequency} \tag{3.2}$$

Finally, fast linear stage is produced with RO4003 as laminate which can be seen from Figure 3.5.

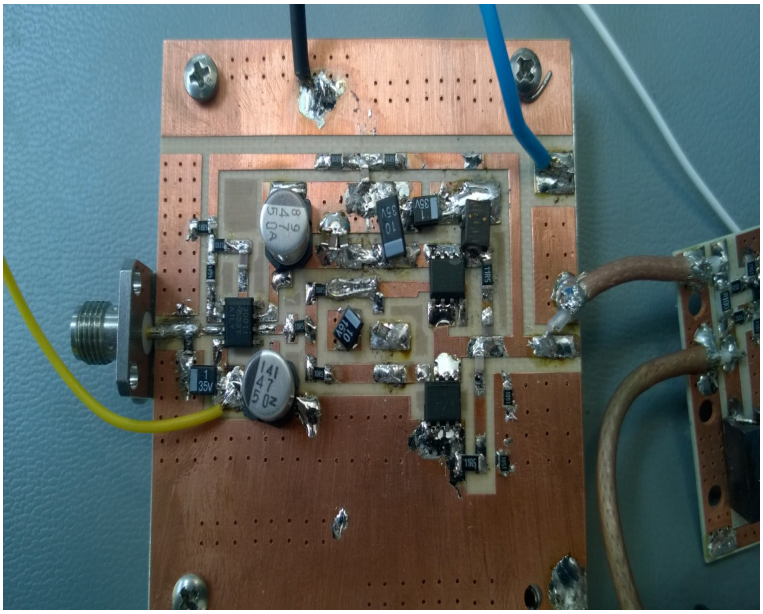


Figure 3.5: Fabricated fast linear stage photo

## 3.2 Sensing Stage Design

Figure 3.6 shows the sensing stage schematic, which is used to turn on and off the switcher by sensing the current flowing into or out of the linear stage. The sensing stage can also smooth the power split between switcher stage and linear stage by hysteresis control.

First of all, a very low ohmic value current sensing resistor $R_{sense}$ is implemented to sense current flowing through a resistance between the linear stage and the overall envelope amplifier outputs. In this design, $R_{sense}$= 0.1 $\Omega$. Secondly, comparator with internal hysteresis is used to detect the voltage difference between the terminals of $R_{sense}$. The LMV7219 is a low-power, high-speed comparator with internal hysteresis of 7 mV. The internal hysteresis ensures clean output transitions even with slow-

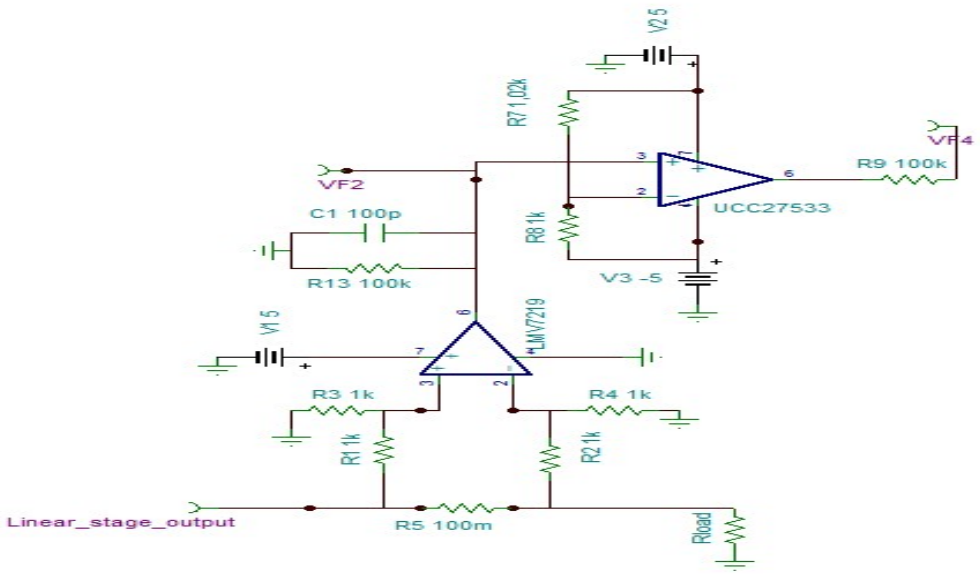



Figure 3.6: The Sensing Stage Schematic

moving inputs signals. This device achieves a 7ns propagation delay while consuming only 1.1mA of supply current at 5V. 2.12 shows that both $R_{sense}$ and $V_{hysteresis}$ are critical for proper operation of envelope amplifier.

### 3.3 Switching Stage Design

Figure 3.7 shows the schematic of the fast switcher stage. The switching control signal is generated from the comparator in the previous stage. After passing the digital isolator, the switching control signal is driven by the switcher driver and outputted to the switcher. Typically, the switcher is a switching buck converter, including a switching power MOSFET, a Schottky diode, and a big power inductor. The switching buck converter is adopted for its easy implementation and high efficiency. Inside the buck converter, the large switching voltage signal from the source of the power MOSFET will be turned into the flat current signal, which in fact is a low frequency current with many small step variations. This low frequency current in combination with the high frequency current from the linear stage comprises the envelope amplifier output current signal provided to the RF transistor load.

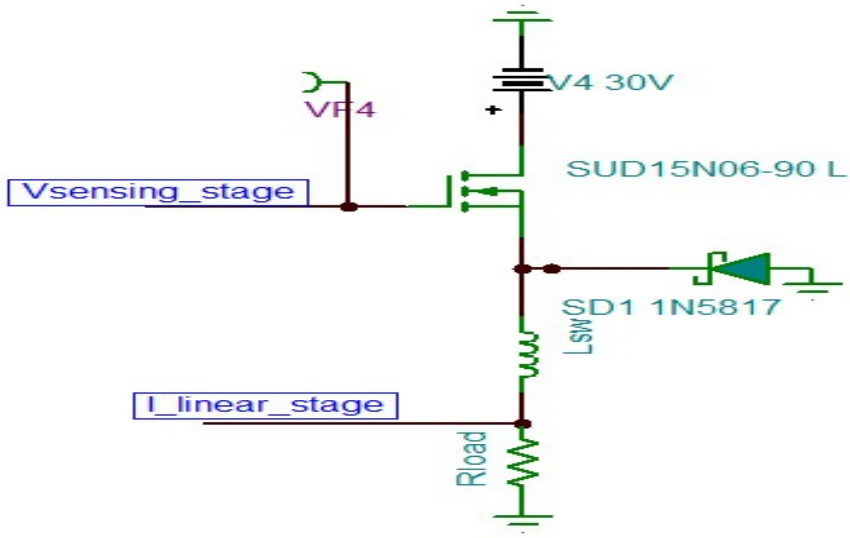



Figure 3.7: The Fast Switching Stage Schematic

Table 3.2: High Power Mosfet

| Vendor | Part no. | $V_{DSmax}(V)$ | $R_{DSon}$(mΩ) | $C_{rss}$ (pF) | $Q_G$(nC) |
|---|---|---|---|---|---|
| Fairchild | FDD5614P | -60 | 130 | 75 | 9.5 |
| Fairchild | FDD4685 | -40 | 35 | 220 | 19 |
| Vishay | SUD15N06-90L | 60 | 90 | 75 | 12 |
| Vishay | Si7850DP | N | 22 | 120 | 18 |

Table 3.2 lists several switching power MOSFET candidates. Based on the mechanism of the switching loss analysis in section 2.3.2, Vishay's SUD15N06-90 L is a good choice, because it has low total gate charge $Q_G$ and low reverse transfer capacitance $C_{rss}$ to achieve the short rise and fall time, as well as low turn-on resistance $R_{DSon}$ for minimum switching power loss for high efficiency. As a high speed gate driver, UCC27533 from TI has been chosen. It has only 15 ns and 7 ns rise and fall times, respectively.

As for the Schottky diode, 1N5817 is selected, based on its low transition capacitance $C_T$ and low forward voltage $V_F$. It can operate at a high frequency and support extremely fast switching.

To determine the value of the inductor value, $L_{sw}$, 2.12 should be analyzed. Note that $L_{sw}$ and $f_{sw}$ are inversely proportional. This means, minimum $f_{sw}$, which decreases the dynamic losses, is possible if $L_{sw}$ value is maximized. In order to provide most of the current through switching stage, the inductor should be able to supply current at any rate of change. Assuming that the output voltage Vout is sinusoidal and the drain of PA is resistive, the maximum inductor value can be derived. [18]

$$V_{out} = V_o \sin(2\pi f_s t) = I_{out} * R_{load} \tag{3.3}$$

assume that $V_{out}$ is sinusoidal and load is resistive

$$I_{out} = \frac{V_o \sin(2\pi f_s t)}{R_{load}} \tag{3.4}$$

$$\frac{\partial i_{out}}{\partial t} = \frac{2\pi f_s V_o \cos(2\pi f_s t)}{R_{load}} < \frac{V_{dd} - V_o \sin(2\pi f_s t)}{L_{sw}} \tag{3.5}$$

any rate of change of current must be supplied by switcher stage

$$L_{sw} < \frac{R_{load}(V_{dd} - V_o \sin(2\pi f_s t))}{2\pi f_s V_o \cos(2\pi f_s t)} \tag{3.6}$$

To find the maximum inductance value, differentiate 3.6 and equating it to zero.

$$L_{sw} = \frac{R_{load} * \sqrt{V_{dd}^2 - V_o^2}}{2 * \pi * f_s * V_o} \tag{3.7}$$

Finally, sensing stage and switching stage are produced with RO4003 as laminate which can be seen from Figure 3.8.

## 3.4 Hybrid Envelope Amplifier Simulations

In order to better design the envelope amplifier, a system model based on PSpice has been developed for simulating the circuit behaviors. The models of THS3091, SI4450DY and SI9407DY,SUD15N06-90 L were acquired from TI and Vishay. The

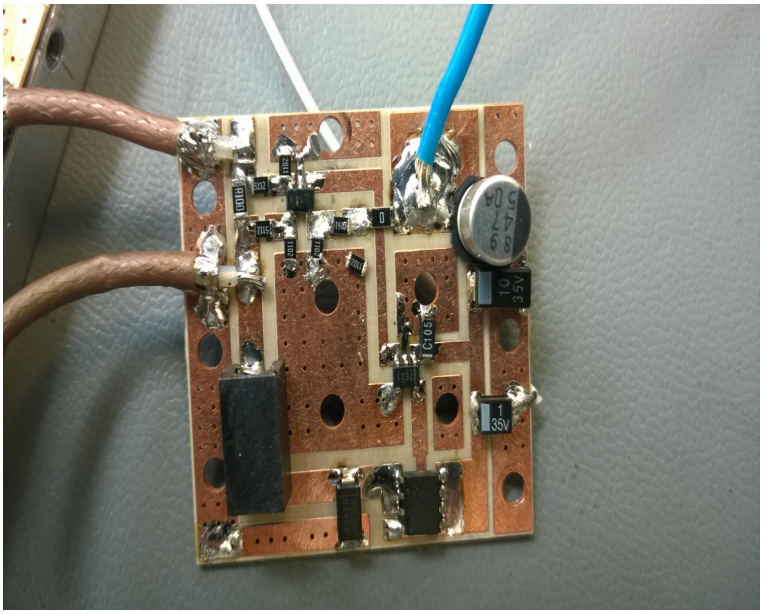


Figure 3.8: Fabricated sensing and switching stage photo

push-pull pair's gate-to-gate biasing circuit was modeled as a 2V DC voltage source for simplicity. As an input signal, 5MHz sinusoidal signal is used with $Vampl = 1.25V$ and $Vdc = 1.5V$. For the RF power amplifier load, the 30 $\Omega$ resistor is a good approximation.

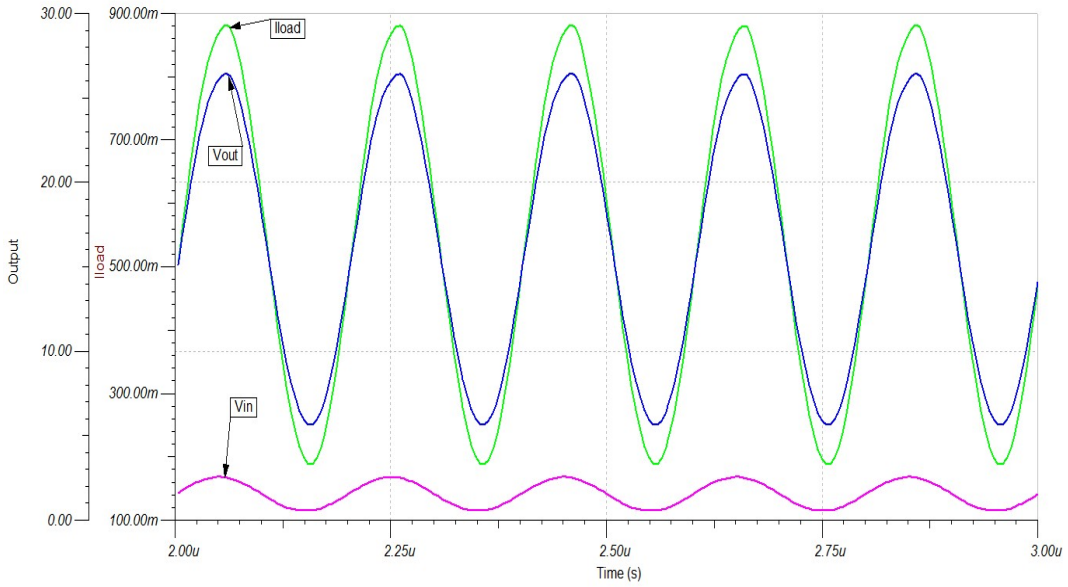



Figure 3.9: The fast linear stage gain characteristic in time domain

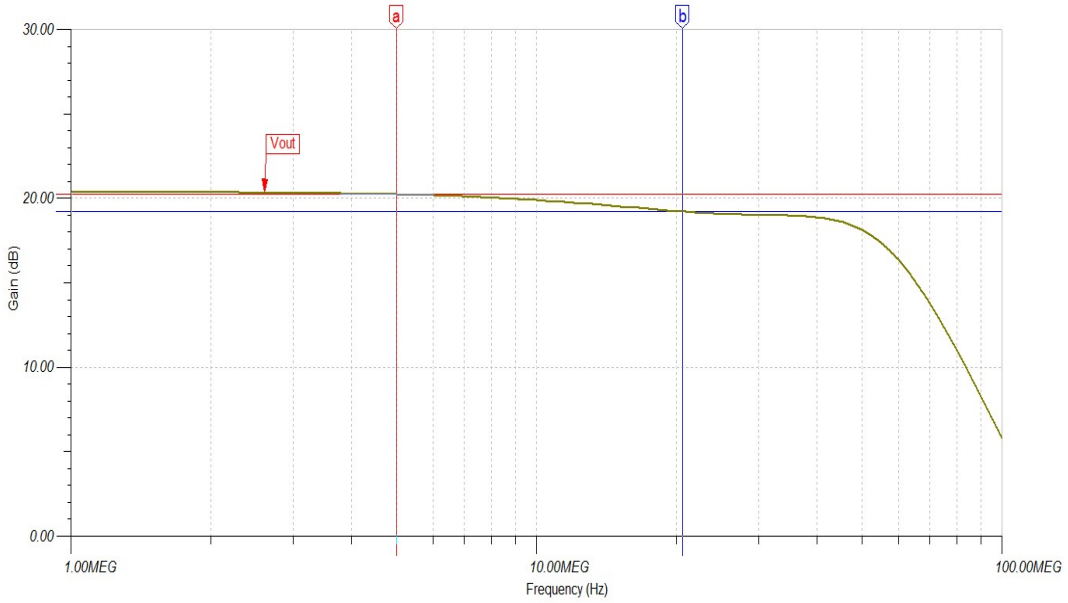



Figure 3.10: The Fast Linear Stage Frequency Response Simulation Results

# CHAPTER 4

# ENVELOPE TRACKING SIMULATION WITH ADS

In this chapter, to better understand the ET operation, simulations with ADS will be done. Prior to applying envelope tracking to a power amplifier, it is useful to test it for memory effects. If an amplifier has memory effects, its output is not just a function of its input at the current instant of time. Its output also depends on what the input was prior to the current instant of time. These memory effects may be caused by the behavior of the active device(s), or by the bias network. Figure 4.1 shows a harmonic balance test for memory effects.

The easiest way to test for memory effects is to run a two-tone harmonic balance simulation in which the frequency spacing between the input tones can be swept. If the amplitudes of the lower and upper third-order intermodulation distortion sidebands are not equal, then the amplifier is exhibiting memory effects. The simulation results, Figure 4.2, show memory effects are minimal, even when the frequency spacing between the two input signals is 5 MHz.

Another thing to do before applying ET to a power amplifier is that designer should see how its PAE varies with output power, with the drain bias voltage swept as a parameter. The schematic of Figure 4.3 simulates the power amplifier as a function of drain bias voltage. Here, the drain bias voltage is swept to see how gain and gain compression vary. The input signal and gate voltage is kept constant.

Figure 4.4 shows a transducer power gain versus output power plot, with the blue dots indicating interpolated data at 16.2 dB gain.

In Figure 4.5, The blue dots indicate the efficiency curve that could be attained via

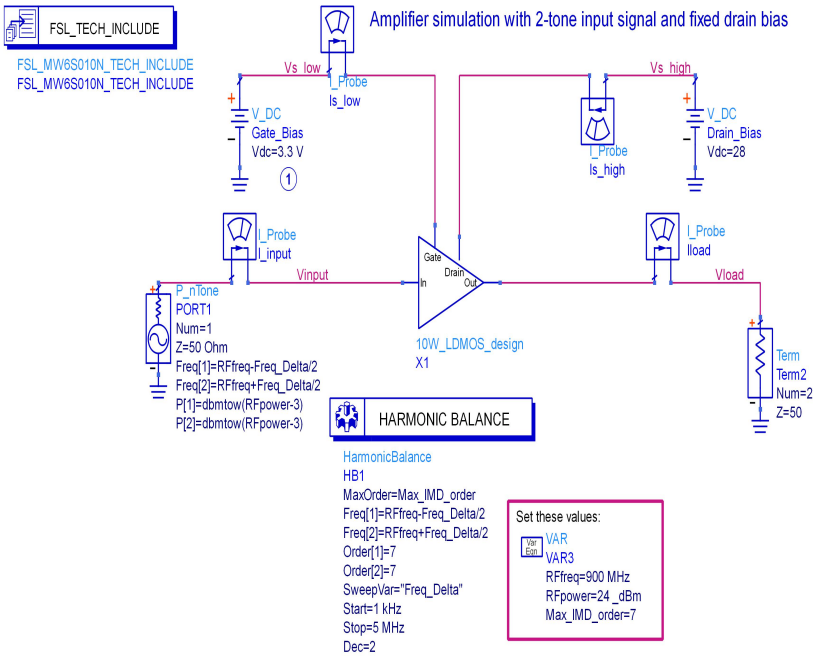
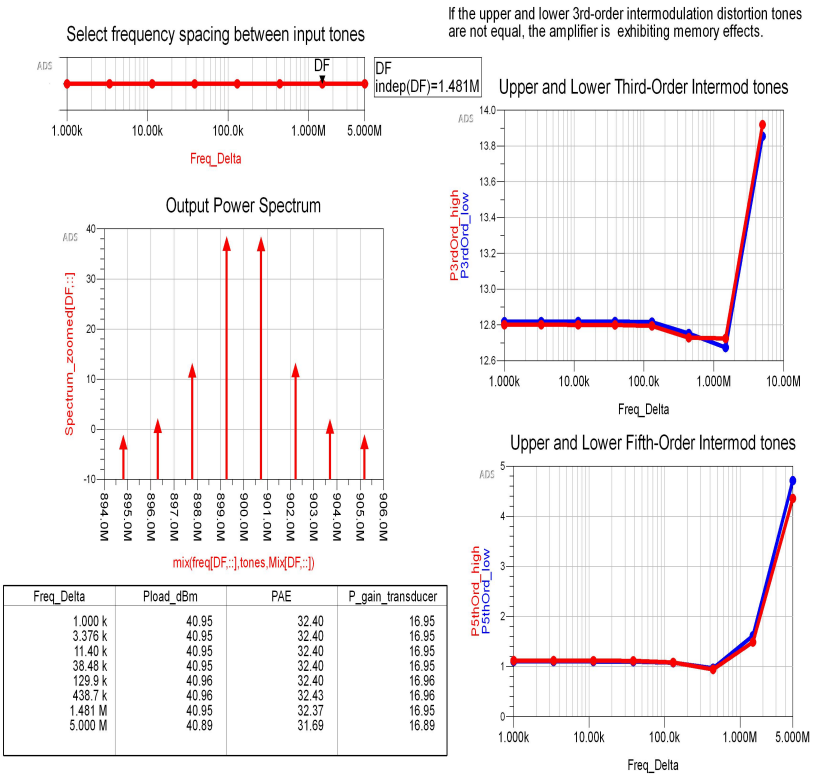



Figure 4.1: Two tone harmonic balance test for memory effects




| Freq_Delta | Pload_dBm | PAE | P_gain_transducer |
|---|---|---|---|
| 1.000 k | 40.95 | 32.40 | 16.95 |
| 3.376 k | 40.95 | 32.40 | 16.95 |
| 11.40 k | 40.95 | 32.40 | 16.95 |
| 38.48 k | 40.95 | 32.40 | 16.95 |
| 129.9 k | 40.96 | 32.40 | 16.96 |
| 438.7 k | 40.96 | 32.43 | 16.96 |
| 1.481 M | 40.95 | 32.37 | 16.95 |
| 5.000 M | 40.89 | 31.69 | 16.89 |

Figure 4.2: Memory effects test result

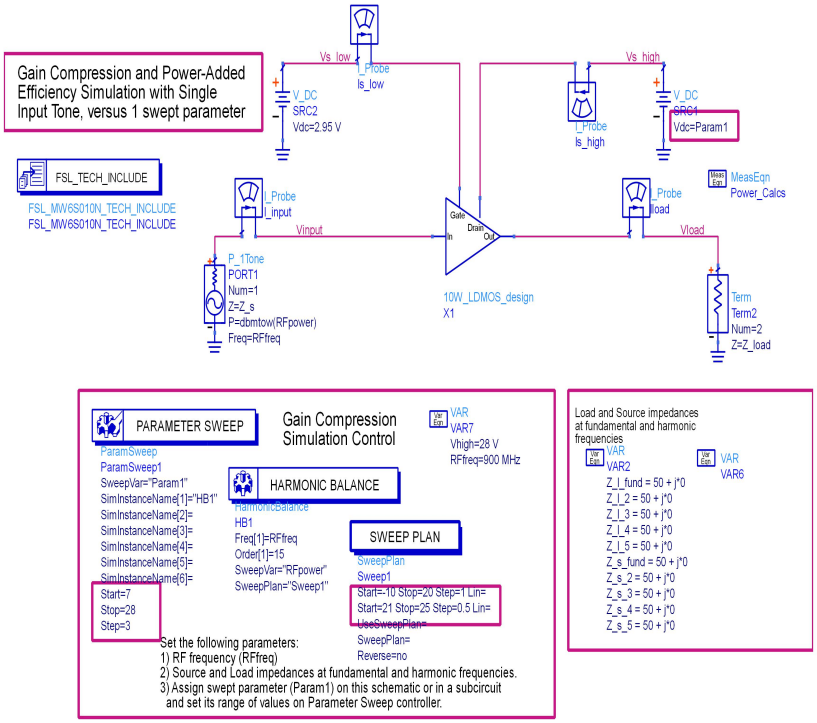
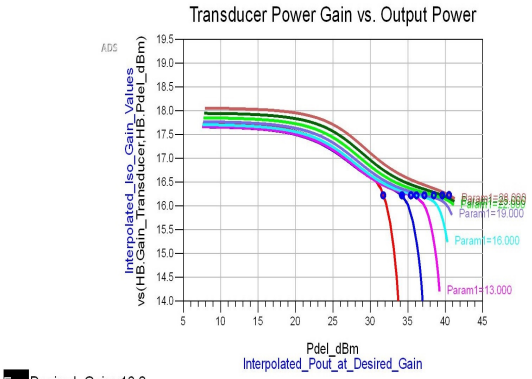



Figure 4.3: Gain compression and PAE simulation schematic




Eqn Desired_Gain=16.2

Eqn Interpolated_Pout_at_Desired_Gain=interpolate_y_vs_x(HB.Pdel_dBm,HB.Gain_Transducer,Desired_Gain,0.05,"linear")

Eqn Interpolated_Iso_Gain_Values=indep(Interpolated_Pout_at_Desired_Gain)

Eqn Interpolated_Pavs_dBm_at_Desired_Gain=Interpolated_Pout_at_Desired_Gain-Interpolated_Iso_Gain_Values

| HB.Param1 | Interpolated_Pout_at_Desired_Gain | Interpolated_Pavs_dBm_at_Desired_Gain |
|---|---|---|
| 7.000 | 31.723 | 15.500 |
| 10.000 | 34.224 | 18.000 |
| 13.000 | 35.424 | 19.200 |
| 16.000 | 36.173 | 19.950 |
| 19.000 | 37.223 | 21.000 |
| 22.000 | 38.473 | 22.250 |
| 25.000 | 39.622 | 23.400 |
| 28.000 | 40.525 | 24.300 |

Figure 4.4: The transducer power gain vs. output power

envelope tracking, and using a shaping table to maintain a constant gain of 16.2 dB. The curves (increasing drain bias, from left to right) show how, for lower output powers, the PAE increases as the drain bias is decreased. For example, the second curve from the left (drain bias 10 Volts) indicates that if this bias could be used when the output power is near 34 dBm, the PAE could be about 43% versus about 15% with a fixed drain bias of 28 Volts.

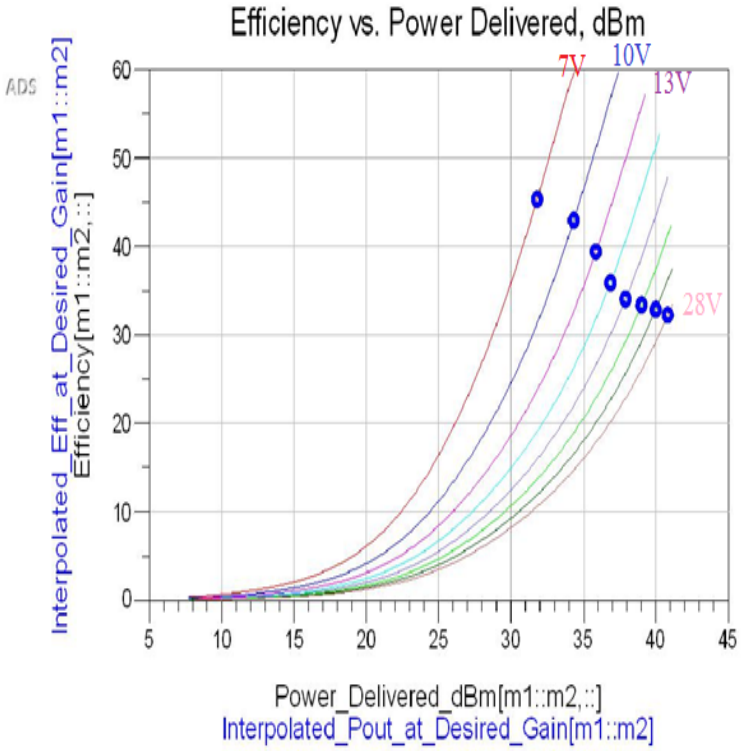



Figure 4.5: Efficiency vs. power delivered at 16.2 dB gain

Figure 4.6 shows for a particular available source power what the drain bias should be to maintain a constant gain.

For example, when the available source power is 26 dBm, the drain bias needs to be set to approximately 17 volts, for 16 dB gain. The corresponding output power will be the available source power plus the gain (26+16)=42 dBm.

Prior to simulating an amplifier with envelope tracking, you may want to examine the test signal you will be using. The signal has bursts of different power levels, leading

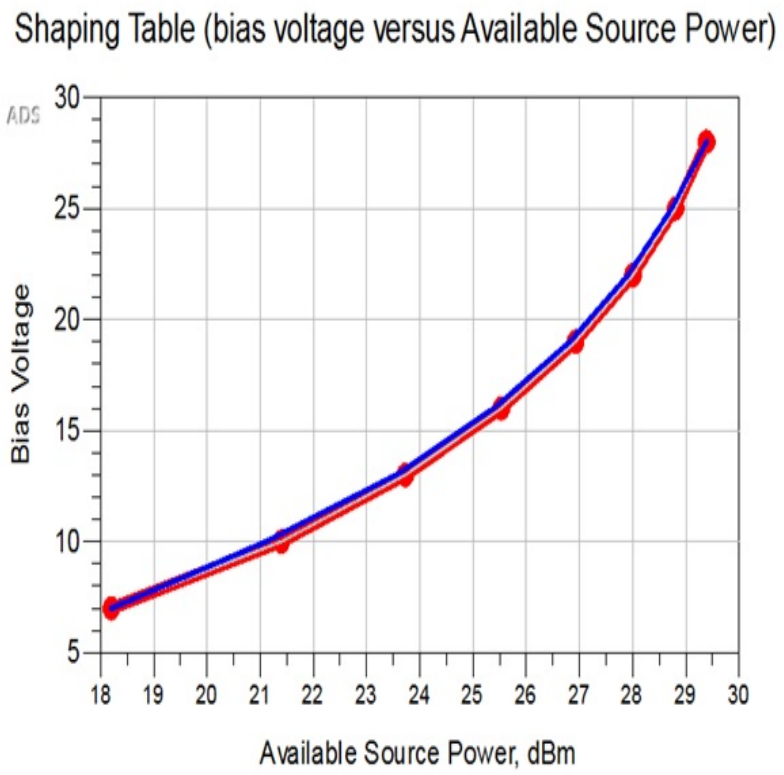



Figure 4.6: Shaping table for constant gain

to a high peak-to-average power ratio.

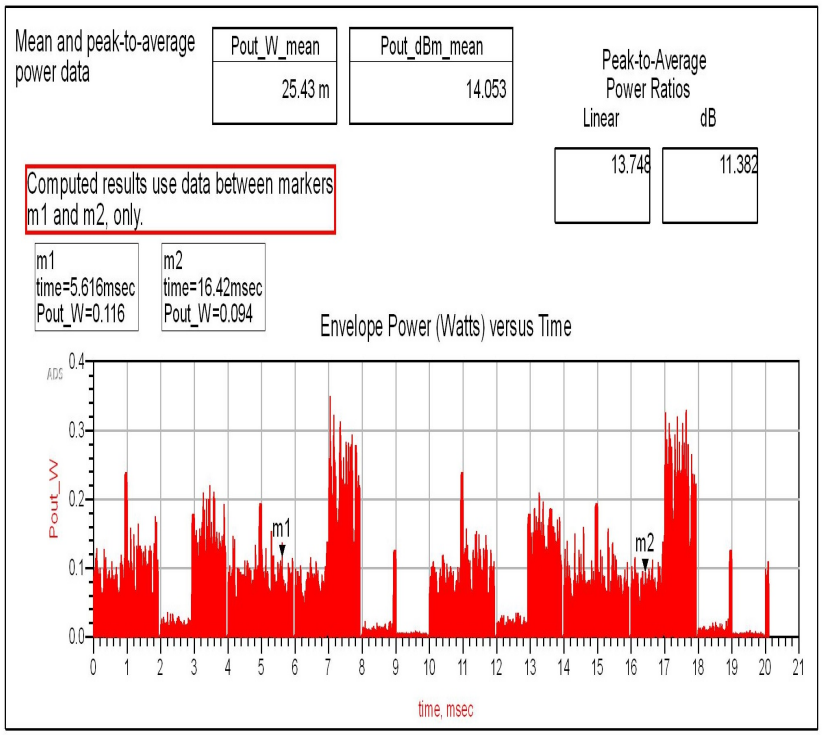



Figure 4.7: Envelope power(W) vs. time

## 4.1 Simulating the Power Amplifier with a Fixed Drain Bias

Figure 4.9 shows the simulation of the power amplifier with a WCDMA signal and a fixed drain bias. This is the simplest simulation setup.

The results in Figure 4.10 show a pretty low mean PAE, 6.79%, which illustrates the need for envelope tracking.

## 4.2 Applying Envelope Tracking to the Amplifier

The schematic in Figure 4.11 applies envelope tracking to the same amplifier.

Figure 4.12 shows the improvement in PAE. The gain on the source in the schematic has been adjusted such that the mean power delivered to load is approximately the

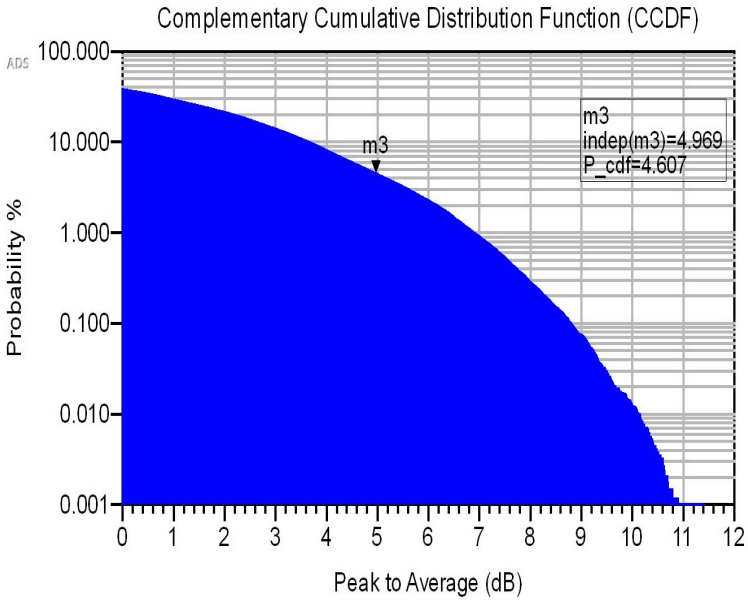



Figure 4.8: Complementary cumulative distribution function of modulated input signal

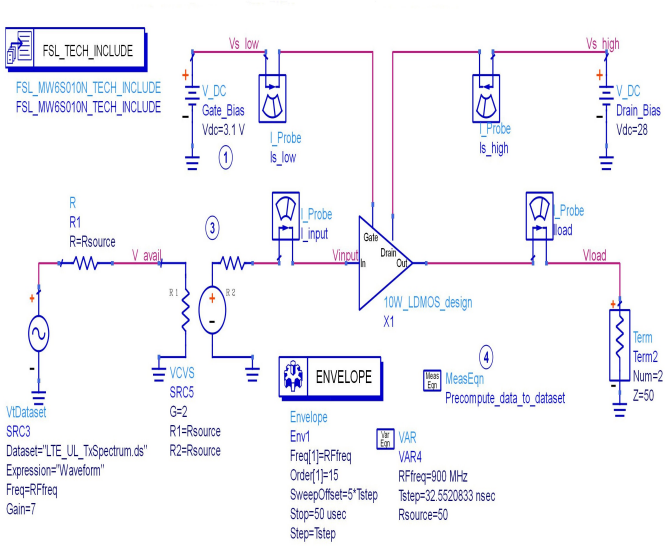



Figure 4.9: Amplifier with WCDMA signal and a fixed drain bias

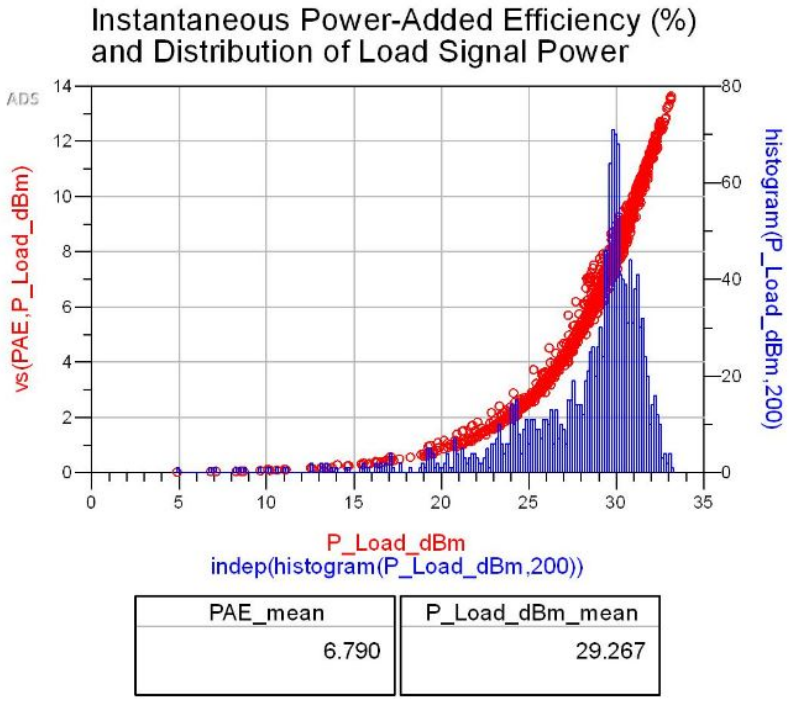



Figure 4.10: Instantaneous PAE and distribution of load signal power

same in both cases. The blue curve represents the amplifer with envelope tracking. The red curve, which has lower PAE, represents the amplifier with 28V fixed drain bias.

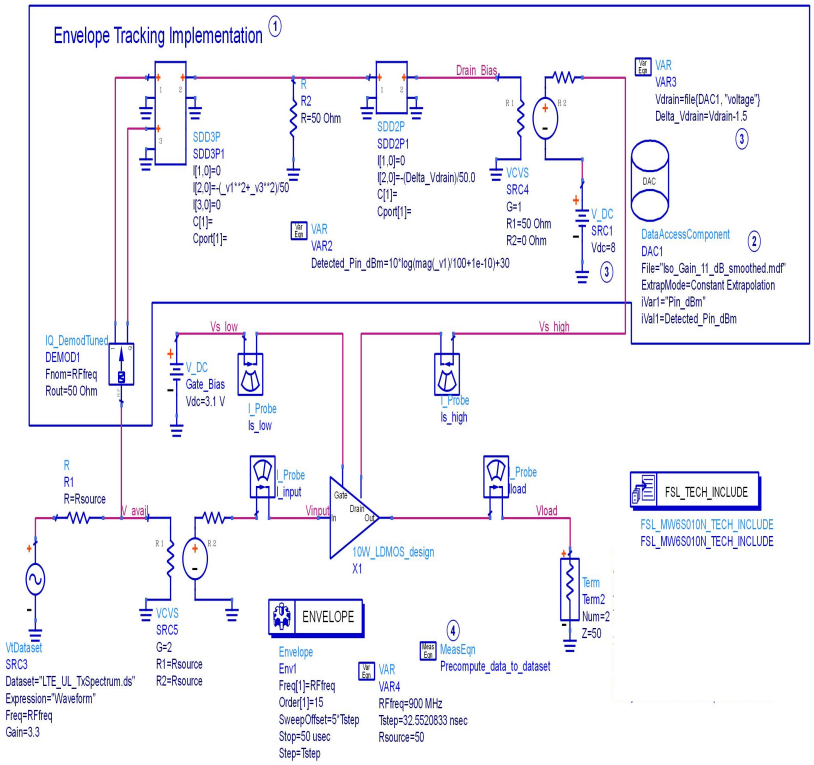



Figure 4.11: Envelope tracking scheme

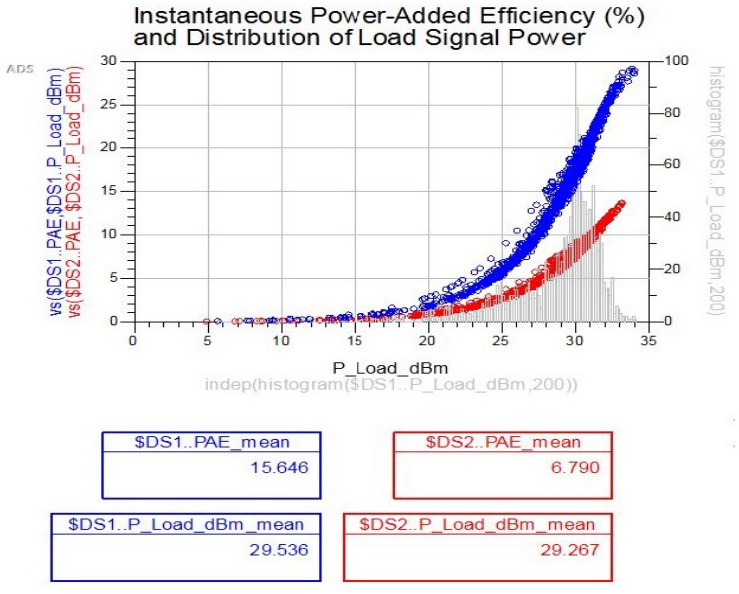



Figure 4.12: Comparison of instantaneous PAE vs. distribution of load signal power

# CHAPTER 5

# WCDMA SIGNAL MEASUREMENTS OF THE ENVELOPE TRACKING SYSTEM

In previous chapters, RF PA and hybrid envelope amplifier are designed and tested seperately. In this chapter, in order to evaluate the application of the envelope amplifier, the whole ET system is set up for testing. Figure 5.1 shows the integrated system which consists envelope amplifier and class AB RFPA. Figure 5.2 shows the measurement setup. The WCDMA signal with 5MHz bandwidth is used a standard-compliant 3GPP WCDMA test signal created using Agilent N700B Signal Studio. A single carrier WCDMA signal at 900 MHz with a PAR of 9.17dB was downloaded to an Agilent MXG signal generator. The envelope of the WCDMA signal is produced with the help of arbitrary waveform generator(AWG). On the envelope path, the envelope amplifier, which is designed in Chapter 3, amplifies the envelope signal and injects into the drain of the class AB RF PA, which is also designed in chapter 2. On the RF path, the WCDMA signal is delayed by a length of cable and subsequently delivered to the input port of the power amplifier. The output of RFPA is connected to an Agilent Spectrum Analyzer to measure the average output power and also the linearity performance of this WCDMA signal in terms of its ACPR.

The complete photo of the measurement setup with MXG signal generator, spectrum analyzer and supplies can be seen from Figure 5.3.

All of the measurements for the RFPA in this setup are compared to the RFPA biased at a fixed voltage of 28V. The comparison is done with the RFPA biased at 28V, which is the same voltage as the peak voltage of the amplified envelope signal. The maximum average output power for the 10W LDMOS device is 31 dBm consider-

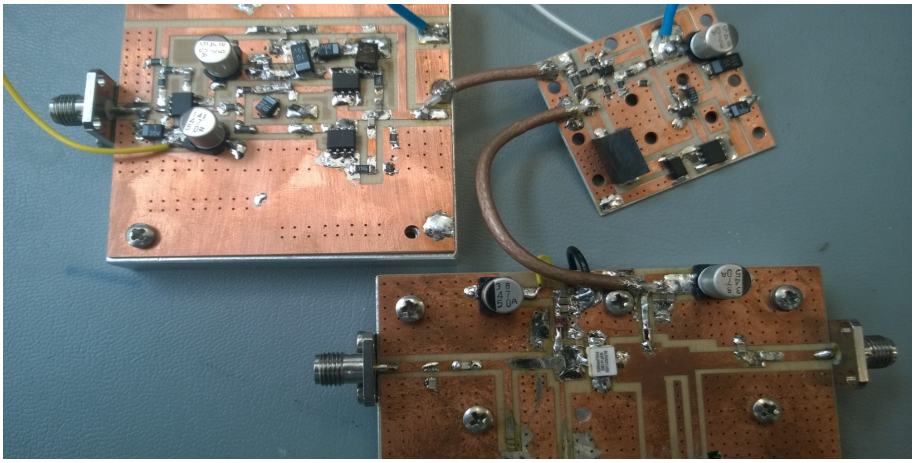


Figure 5.1: Integrated envelope amplifier and RFPA

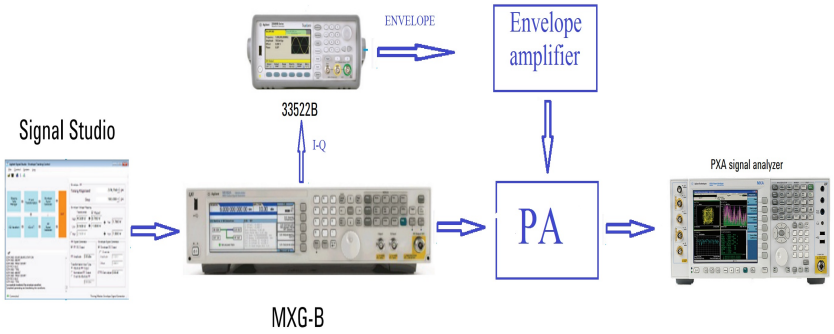



Figure 5.2: ET measurement system

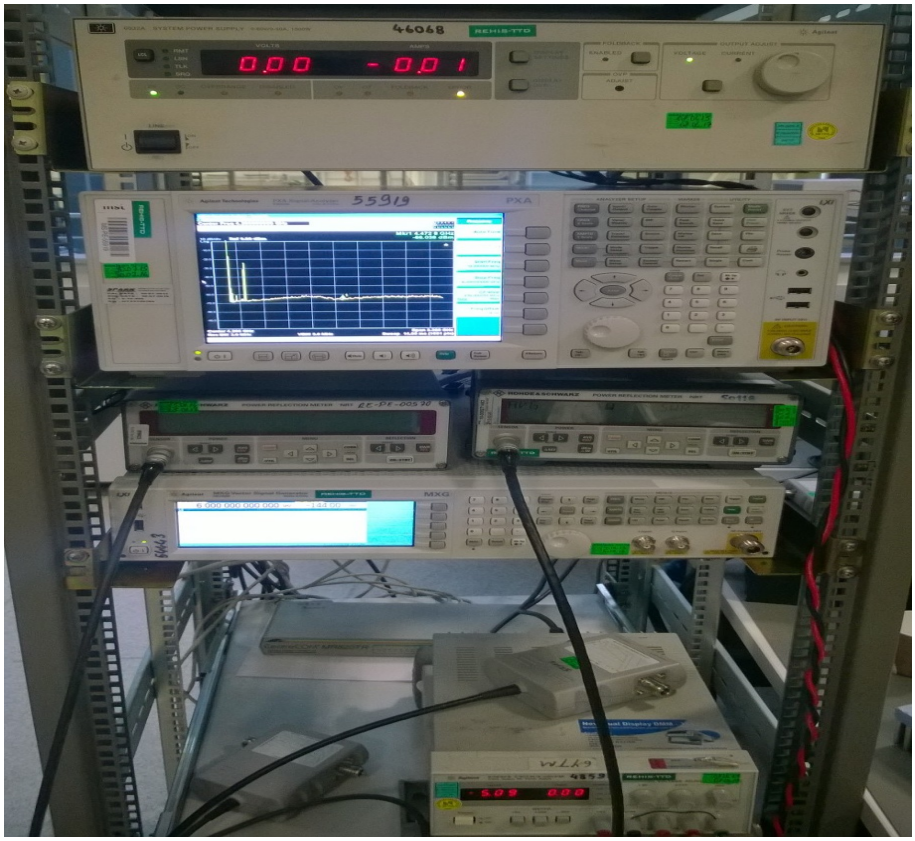



Figure 5.3: ET measurement system setup photo

Table 5.1: Comparison of constant supply PA and ET PA

| Part no. | $RFPAbiasedwith28V$ | $RFPAwithET$ |
|---|---|---|
| Drain Voltage | 28V | 8V-28V |
| Gain | 19 | 16.2 |
| Average Pout | 32 | 31 |
| Power diss. of Env. Amp. (W) | - | 0.8 |
| Power diss. of LDMOS | 19.5 | 6.1 |
| Total DC power | 19.5 | 6.9 |
| PAE(%) | 8 | 18 |

ing 9.17dB PAR of the WCDMA signal used in this measurement. The measured efficiencies of the constant Vdc RFPA and ET system for 5 MHz WCDMA signal with 10 dB PAPR are tabulated in Table 5.1. As an efficiency improvement method, envelope tracking increases the efficiency of the linear PA from 8% to 18%.

In Figure 5.4, the spectrum of the output RF signals are also plotted to show the ACPR levels. The yellow trace shows the output spectrum of the ET RF PA with 5 MHz WCDMA signal at the input. The blue trace shows the output spectrum of the Class AB biased RF PA with same input. The red trace shows 5MHz WCDMA signal itself. The ACPR is measured at +/-5 MHz offset in 5 MHz bandwidth for 5 MHz WCDMA. For ET PA, ACLR is 39.1 dBc which is higher than input WCDMA signal.

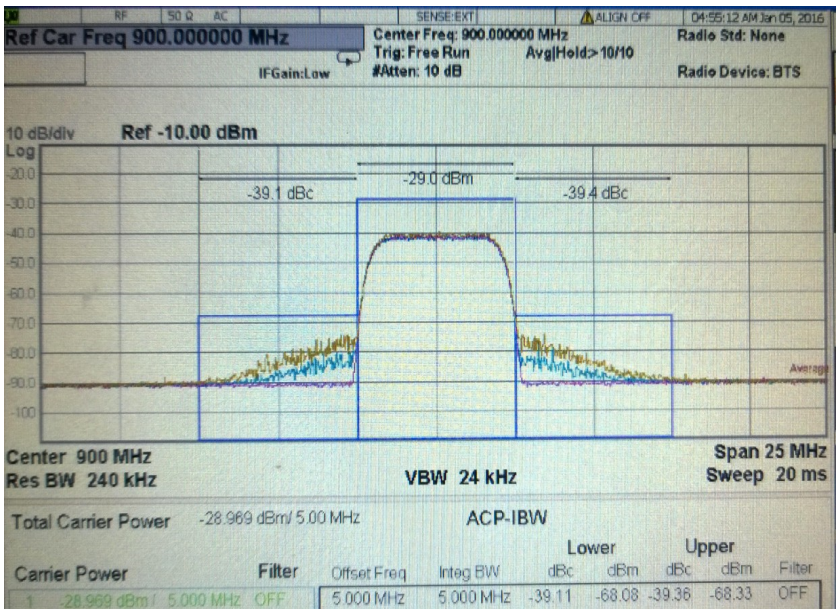



Figure 5.4: Measured spectrum of W-CDMA output signal

# CHAPTER 6

# CONCLUSIONS

In the thesis, fully analog envelope tracking system has been designed with the help of CAD tools. A medium power W-CDMA base station power amplifier, using MW6S010N, 10W LDMOS device from Freescale, has been introduced. To increase the efficiency, envelope tracking technique with wideband-efficient hybrid envelope amplifier has been implemented.

The comparison of the effciency enhancement technique for high PAPR signals prove that at higher back-off levels, the supply modulation can improve the PAE of the RF PA more than the load modulation.

To better understand the concept of the envelope tracking, main blocks of the system were deeply investigated. Since the overall efficiency of an ET PA is the multiplication of the RF PA efficieny and envelope amplifier efficiency, a broadband and efficient supply modulator is indicative of the overall efficiency. Hybrid envelope amplifier has been designed and tested with resistive load. Efficiency formulas have been described to see the importance parameters for component selection as an opamp and mosfet. Simulations with ADS have been done to show the achieveable performance with WCDMA input signal.

For ET RFPA, under the influence of a WCDMA source, an average efficiency of 18% with average output power of 1 W and gain of 16.2 dB have been achieved. This study has demonstrated that ET power amplifiers using LDMOS are promising candidates for 10 dB PAPR input signals.

## 6.1 Future Work

Future work on the wideband ET RFPA would be interesting on the following topics:

- ET model including AM/PM and memory effect,

- The interaction analysis between envelope amplifier and RF power amplifier,

- Time alignment between RF path and envelope path,

- Combination of Doherty and ET architectures.

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