A LOW-POWER ANALOG-TO-DIGITAL CONVERTER INTEGRATED CIRCUIT FOR DATA ACQUISITION APPLICATIONS

A THESIS SUBMITTED TO
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

SERHAT KOÇAK

IN PARTIAL FULLFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2016

Approval of the thesis:

A LOW-POWER ANALOG-TO-DIGITAL CONVERTER INTEGRATED CIRCUIT DESIGN FOR DATA ACQUISITION APPLICATIONS

submitted by **SERHAT KOÇAK** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. M. Gülbin Dural Ünver
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Gönül Turhan Sayan
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Tayfun Akın
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Examining Committee Members:

Prof. Dr. Haluk Külah
Electrical and Electronics Eng. Dept., METU _____

Prof. Dr. Tayfun Akın
Electrical and Electronics Eng. Dept., METU _____

Prof. Dr. Nevzat Güneri Gençer
Electrical and Electronics Eng. Dept., METU _____

Assoc. Prof. Dr. Barış Bayram
Electrical and Electronics Eng. Dept., METU _____

Assoc. Prof. Dr. Ali Ziya Alkar
Electrical and Electronics Eng. Dept.,Hacettepe Univ. _____

Date: 05.02.2016

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Serhat Koçak

Signature:

ABSTRACT

A LOW-POWER ANALOG-TO-DIGITAL CONVERTER INTEGRATED CIRCUIT FOR DATA ACQUISITION APPLICATIONS

Koçak,Serhat

M.S, Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Tayfun Akın

February 2016, 108 pages

Data acquisition systems have been used in different kinds of applications such as sensing applications, wireless communication, and healthcare. Each of these applications requires a different and unique system in order to achieve high quality acquisition. These different and unique systems employ various components such as analog-to-digital converters, digital-to-analog converters, and external electronics. Each of these components offers an optimal solution in order to satisfy the system requirements. Analog-to-digital converters known as ADCs are the main devices in the data acquisition systems which interface between the physical parameters and digital systems. Low power and high performance ADCs are preferable, since the systems are comprised of many components which lead to significant amount of power consumption. This thesis presents the design, and implementation of an analog-to-digital integrated circuit for low power data acquisition applications. 0.35 μm CMOS technology is used in order to implement the proposed ADC. In this thesis, different ADC topologies are investigated, and successive approximation register known as SAR ADC is chosen since, that structure which is low noise, dissipates low power at medium resolution, and medium speed. In this work, each part of the ADC is analyzed in

order to design an optimal ADC structure. Low power solutions for the differential rail to rail comparator and digital-to-analog converter are proposed for high performance ADC. A flexible and programmable digital controller which consists of the successive approximation register is implemented in order to perform the binary search algorithm. An output serializer is employed in order to reduce the number of pads. A programmable bias generator is designed to provide bias currents to the analog blocks. The designed chip occupies 2mmx2mm silicon area, and the power dissipation of the core of the designed chip is less than 1 mW which is suitable for low power data acquisition applications. The performance of the SAR ADC is evaluated based on the simulation results which conclude that, the designed SAR ADC is a promising solution for the low power data acquisition applications. A compact test setup including a compact PCB card, a FPGA card and a PC is designed for performing the ADC characterization tests.

Keywords: Analog-to-digital converters, digital to analog converters for data acquisition applications, successive approximation register, a low power, low noise design, capacitive digital-to-analog converters

ÖZ

SİNYAL ALMA UYGULAMALARI İÇİN DÜŞÜK GÜÇ TÜKETİMLİ ANALOG-SAYISAL ÇEVİRİCİ TÜMLEŞİK DEVRESİ

Koçak,Serhat

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi : Prof. Dr. Tayfun Akın

Şubat 2016, 108 sayfa

Sinyal alma sistemleri, algılama uygulamaları, kablosuz haberleşme ve sağlık gibi farklı uygulama alanlarında kullanılmaktadır. Bu uygulamaların herbiri, yüksek kazanç elde edebilmek için değişik ve özgün sistemlere ihtiyaç duymaktadır. Bu farklı ve özgün sistemler, analog-sayısal çeviriciler, sayısal analog çeviriciler ve dışsal elektronikler gibi bileşenler kullanmaktadır. Bu bileşenlerin herbiri sistem gereksinimlerini karşılamak için optimal bir çözüm sunar. Analog-sayısal çeviriciler fiziksel parametrelerle sayısal dünya arasında iletişim sağlayan sinyal alma sistemlerinin temel bileşenidir. Düşük güç tüketimli, yüksek performanslı analog-sayısal çeviriciler daha çok tercih edilmektedirler;çünkü sinyal alma uygulamalarında çok sayıda önemli güç tüketen bileşen bulunmaktadır. Bu tez düşük güç tüketimli sinyal alma uygulamaları için düşük güç tüketimli analog-sayısal çevirici tasarımını ve uygulamasını içermektedir. Analog-sayısal çevirici için 0.35 μm CMOS teknolojisi kullanılmıştır. Bu tezde değişik yapıda analog sayısal çevirici yapıları incelenmiştir ve düşük gürültülü ardışık yaklaşıklama kaydedicili analog sayısal çevirici ortalama çözünürlükte ve hızda az güç tükettiği için seçilmiştir. Bu

çalışmada her bir bileşen optimal bir yapı tasarlayabilmek için analiz edilmiştir. Tam diferansiyel yapı olan ve negatif güç geriliminden pozitif gerilimine sinyalleri içeren bir karşılaştırıcı ve sayısal analog çevirici için düşük güç tüketimli çözümler sunulmuştur. İkili arama algoritmasını uygulamak için ardışık yaklaşıklama kaydedicili yapıyı içeren esnek ve programlanabilir bir mikro-denetleyici kullanılmaktadır. Çipin boyutunu azaltmak için seri veri sağlayan bir yapı kullanılmıştır. Analog bloklara akım sağlayabilmek için programlanabilir bir akım üreteci bloğu kullanılmıştır. Tasarlanan çip 2mmx2mm alanında silikon alan yer kaplamakta ve 1 mW'ın altında güç tüketmekte olup düşük güç tüketimli sinyal alma uygulamaları için kullanılabilir. Ardışık yaklaşılama kaydedicili analog sayısal çeviricinin performansı simülasyon sonuçları baz alınarak değerlendirilmiştir. Bu simülasyon sonuçlarına göre tasarlanan analog-sayısal çevirici düşük güç tüketimli sinyal alma uygulamaları için kullanılabilir. Analog sayısal çevirici karakterizasyon testleri için, çevre kartı, FPGA kartı ve bilgisayar sistemini içeren bir sistem tasarlanmıştır.

Anahtar kelimeler: Analog-sayısal çeviriciler, sinyal alma uygulamarı için sayısal-analog çeviriciler, ardışık yaklaşıklama kaydedici, düşük güç tüketimli, düşük gürültü seviyeli tasarım, kapasitif sayısal-analog çeviriciler

To my family

ACKNOWLEDGEMENTS

I would like to express my gratitude towards my advisor Prof. Dr. Tayfun Akın for his supervision and guidance throughout this study. I would like to thank Dr. Selim Eminoğlu for his endless support and trust through my graduate life.

I would like to thank Mehmet Ali Gülden, Osman Samet İncedere, Nusret Bayhan and Murat Işıkhan for their technical guidance and sharing their knowledge and experience at every stage of this study.

I also would like to thank to my manager Umut Ekşi for his support during my thesis period and all of the colleagues at Mikro-Tasarım, Suhip Tuncer Soyer, Cem Yalçın, Mithat Cem Boreyda Üstündağ, Özge Turan, Hakan Çeçen, Mertcan Ergün, Sercan Şahin, Aslı Doğan, Mustafa Karadayı, Oğuz Kazan, Alper Karakuzulu, Ramazan Yıldırım, Mehmet Akdemir, Murat Aktürk, Hayrettin Anıl Baş and Emine Aytekin for their invaluable friendship and support during this work.

I also would like to thank Mikro-Tasarım San. ve Tic. Ltd. Şti. for providing access to the IC design software, for fabricating the test chip implemented in this thesis and for supporting the test board fabrication.

Last but not least, I would like to give my special thanks to my mother and my father for their endless trust, encouragement and patience in every moment of my life. Without their invaluable support, I would not achieve this success.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

Data acquisition systems are the main devices which interface between the physical parameters, and the digital systems. The physical parameters such as speed, temperature, magnetic field or voltage can be sensed by different kinds of sensors. In order to extract the required information from these different sensors, the physical parameters called as analog signals should be processed in either analog systems or digital systems. Today, digital systems are more preferable, since they offer low cost, high speed and accurate complex systems. In order to use analog signals into digital systems, analog signals should be converted into digital signals. Analog-to-digital converters known as ADCs are employed in the data acquisition systems in order to perform the analog-to-digital conversion.

Today, data acquisition applications include different kind of applications such as sensing applications, digital audio or healthcare systems. For each application, an optimal conversion solution is provided by different kind of ADC structures. Sensing applications including precision measurements and signal conditioning applications, and ranging from DC to KHz require sensitive systems. Low noise, low physical parameters dependence such as temperature or supply voltage, and low gain error have to be satisfied in order to measure the sensitive parameters such as pressure, acceleration or speed. $\Delta\sum$ ADCs and successive approximation register ADCs known as SAR ADCs are the popular structures for these applications. In digital audio systems, 16-bit linear $\Delta\sum$ ADCs and DACs are used instead of traditional logarithmic converters [1]. For healthcare applications, pipelined and $\Delta\sum$ ADCs can be used in order to have high resolution and large

signal bandwidth in the order of tens of MHz [2]. The aim of this thesis is to design and implement of a low power, low noise analog-digital converter integrated circuit design for data acquisition applications. Table 1-1 shows the preliminary specifications of the SAR ADC. The input signal is ranging from DC to 10 KHz. The target resolution is 12 bit with 20 KS/s sampling rate. The static errors INL and DNL should be less than 1 least significant bit (LSB) voltage. The power consumption of the core of the proposed ADC should be less than 1mW which is the main objective of this thesis. The proposed SAR ADC should occupies a silicon area less than 9 mm^2 in 0.35 μm CMOS technology.

Table 1-1: Preliminary specifications of the SAR ADC

Parameter	Value
Resolution	12 bit
Sampling Rate	20 KS/s
Power Consumption	<1mW
Technology	0.35 μm CMOS
Area	<9mm^2
INL	< 1 LSB
DNL	<1 LSB

In this work, the successive approximation register known as SAR is chosen due to low power, and low noise structure, and it is suitable for medium resolution applications. This thesis describes the design of a low power Successive approximation register known as SAR ADC for data acquisition applications. The SAR ADC has a fully differential rail to rail structure which is comprised of DACs array, a precision comparator, and the digital logic for implementing the successive approximation algorithm. The prototype SAR ADC has a highly configurable digital controller, and bias generator. The configurable and flexible digital controller offers a flexible functionally tests. In other words, each digital block can be tested separately. The digital controller implements the Successive approximation algorithm, and it generates the required digital signals for the analog blocks such as comparator and bias generator. A programmable bias generator is used to provide different bias currents. A bandgap circuit which is temperature and supply independent is employed in order to generate the reference voltage. A fully differential and rail to rail comparator is used in order to perform the comparison. An offset cancellation scheme is used in order to reduce the offset voltage error of the comparator caused by the mismatches. The output of the proposed ADC should be serially sent to external electronics in order to reduce the number of pads and chip size.

Chapter 1 introduces the basic information about the analog-to digital conversion, and the motivation of this study. Section 1.1 briefly discusses the basic information about data conversion. Section 1.2, explains the general performance parameters of the ADCs. Section 1.3 shows the different ADC structures. Section 1.4 explains the motivation, and the goals of the proposed design. Section 1.5 states the research objectives and thesis organization for this thesis.

1.1 Data Conversion

In electrical engineering, a signal can be defined as a function which can carry information. Signals are divided into two categories which are analog and digital signals. Analog signals are the continuous signals over continuous time. Voltage, current, and charges can be given as an example of analog signals. Figure 1-1 shows a simple analog sinusoidal signal with 1ms period and 3.3V amplitude. The signal is continuous over the time, and the amplitude is between 3.3V and -3.3V. A simple sinusoidal continuous function can be referred as an analog signal, since both the amplitude and time are continuous functions.

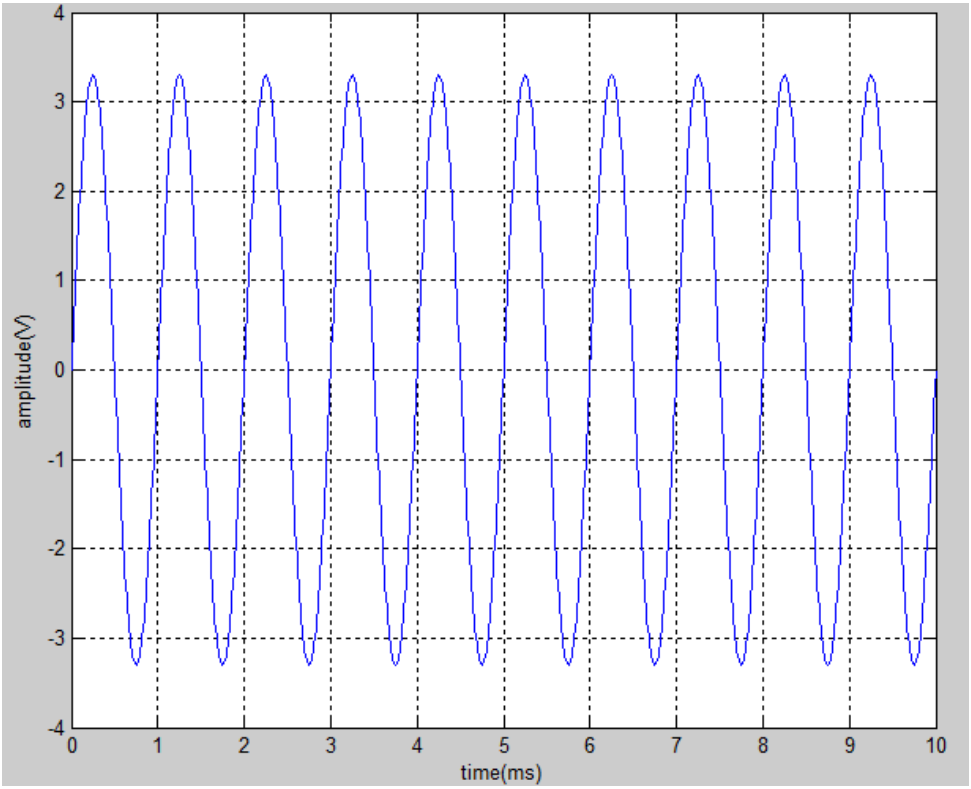

Figure 1-1: A simple sinusoidal analog signal with 1ms period and 3.3V. amplitude.

On the other hand, digital signals are discontinuous and they are represented mathematically by an indexed sequence of numbers [3]. These numbers are called as digits. Binary number system is the basic system that represents the digital signals. Figure 1-2 shows a simple digital signal with 0V and 3.3V. The 3.3V means 1, and 0V means 0 in the digital systems.

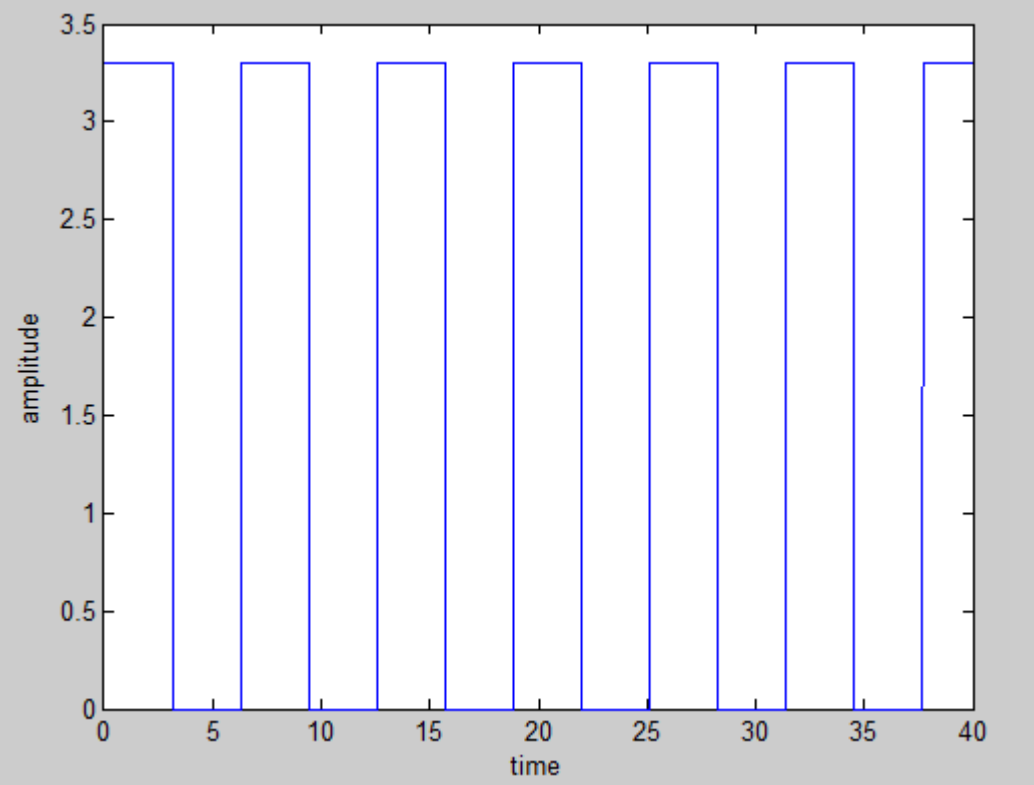

Figure 1-2: A simple digital signal with 0V and 3.3V.

Signal processing can be performed in either analog domain or digital domain. In some applications, only analog signal processing or digital signal processing can be used in which implies that a data conversion between the analog domain and digital domain is required. Analog-to-digital converters and digital-to-analog converters are the devices that provide the data conversion. Figure 1-3 shows a circuit symbol of N-bit digital word. Digital-to-analog converters known as

DACs take digital words as an input and generate analog signals according to the input.

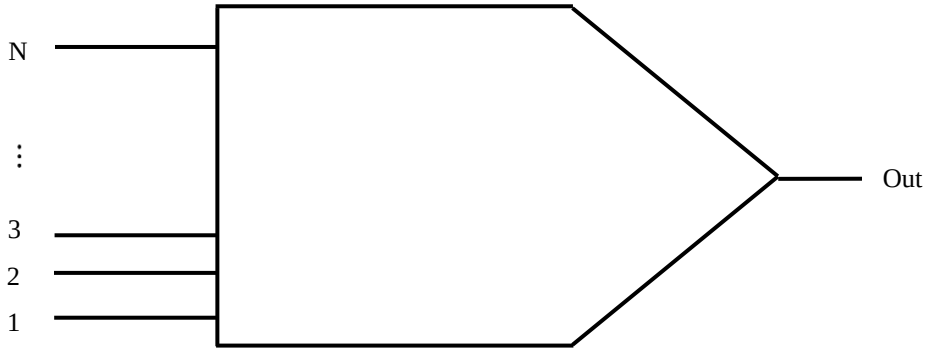

Figure 1-3: Circuit symbol of N-bit digital word DAC.

Due to the fact that digital signals are not continuous and they are discrete values, the output of the DAC cannot be an exact analog signal. As a result, the output of the DAC has a quantization error Figure 1-4 shows a 3-bit DAC output its quantization error. The quantization error can be defined as a difference between the ideal analog input and ideal DAC output. It is an inevitable result of converting the digital signal into analog signal. However, by using low pass filter, the output of DAC can become smoother [4]. Typically, the quantization error is represented in terms of least significant bit (LSB). For an ideal DAC, the quantization error should not exceed the half of the least significant bit voltage.

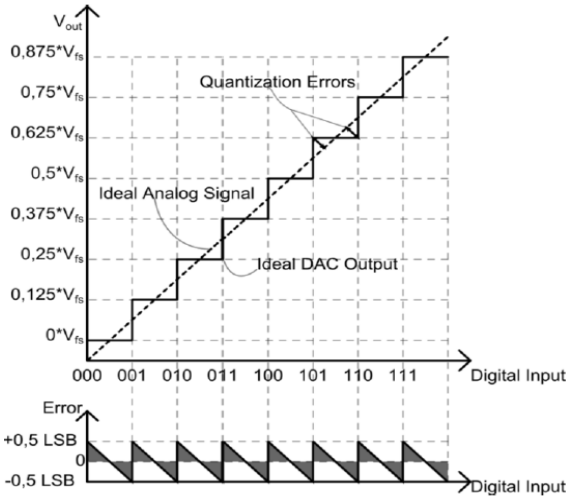

Figure 1-4: 3-bit DAC output and quantization error [5].

Figure 1-5 shows the circuit symbol of an N bit-ADC. Analog-to-digital converters known as ADCs take the analog signals as an input and generate the digital outputs according to the given input. Typically, the conversion is performed by comparing the input analog signal against an analog reference voltage [6]. There are different kinds of ADC structures in the literature such as pipeline, flash or SAR ADC.

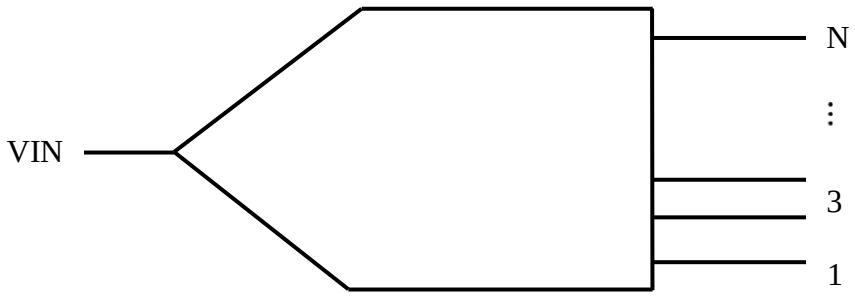

Figure 1-5: Circuit Symbol of an N-bit ADC.

Figure 1-6 shows the analog input, digitized output signal, and quantization error. The outputs of the ADCs are comprised of finite number of digits. For this

reason, ADCs also have a quantization error which can be reduced by increasing the resolution of the ADC, since the total range of the analog input is divided by the number of outputs. If the number of outputs increases, mapping can be performed better.

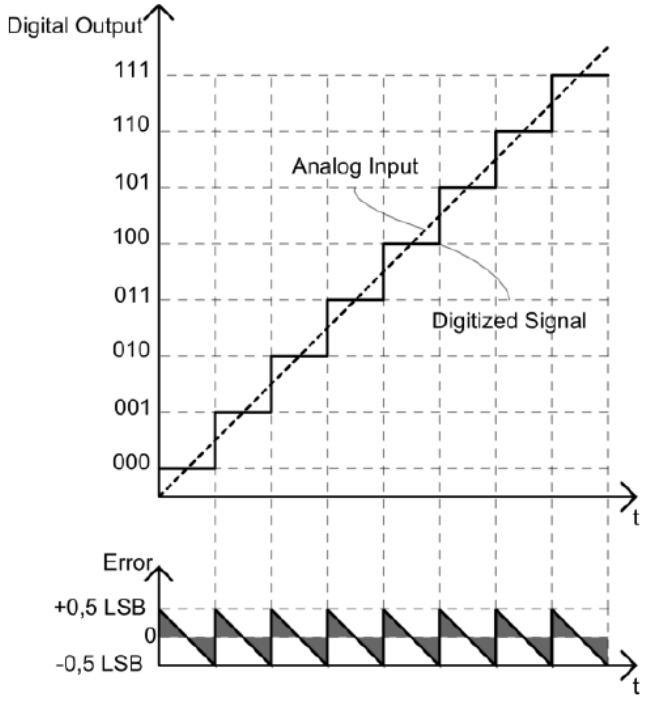

Figure 1-6: Analog input, digitized output signal, and quantization error [4].

Section 1.2 analyses the performance parameters of the ADC.

1.2 ADC Performance Parameters

ADC performance parameters are mainly divided into two groups which are static parameters and dynamics parameters. Static parameters are concerned for the context of the signals at very low frequency. On the other hand, dynamic parameters are examined for high frequency.

1.2.1 Static Parameters

Static parameters can be classified into four groups which are offset error, gain error, differential nonlinearity and integral nonlinearity. Figure 1-7 shows the static error metrics for data conversion.

- Offset Error: The amount of vertical difference between the actual output value and the ideal output value. It is valid for a whole range of the ADC. It can be expressed in terms of LSBs. Offset errors can be cancelled by measuring a reference value and subtract that value from the future samples.
- Gain Error: The difference between the slope of the actual value and the slope of the ideal output. Gain error is expressed in terms of percentage.
- Differential Nonlinearity (DNL): The size of the quantization step for an ideal ADC is defined as the quotient of the analog input range and 2^N where N is the number of bits. This size can be deviated from its ideal value. DNL quantifies the deviation of the step size from its ideal value. It is related to the ADC architecture, and it cannot be totally removed. However, it can be reduced by choosing proper architectures and blocks.
- Integral Nonlinearity (INL): INL quantifies the maximum deviation of the output from the straight line which connects the two end points of the output curve [7]. It is measured from the center of the step size. It is expressed in terms of LSB. The effects of the INL cannot be totally cancelled. It can be only reduced by choosing proper architectures.

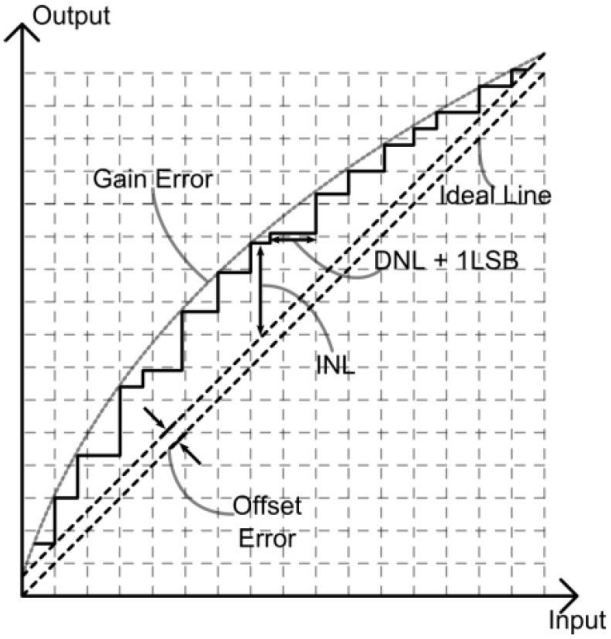

Figure 1-7: Static Error metrics for data conversion [4].

1.2.2 Dynamic Parameters

Dynamic parameters become an important issue when the frequency of the signals is high. At low frequencies, the effects of the dynamic parameters are relatively small. However, at high frequencies, it can affect the performance of the data conversion systems. In literature, common parameters such signal to noise ratio (SNR), total harmonic distortion (THD), signal to noise and distortion ratio (SNDR), harmonic distortion (HD) and spurious free dynamic range (SFDR) are discussed.

- Signal to Noise Ratio (SNR): It is defined as the ratio of the output signal voltage level to the output noise level.
- Total Harmonic Distortion (THD): It is defined as the ratio of the sum of powers of the harmonic frequency components to the power of the fundamental frequency component [8].

- Signal to Noise and Distortion Ration (SNDR): This parameter is comprised of SNR and THD parameters. The ratio of the RMS value of the signal amplitude to the RMS value of all of the spectral components gives SNDR [8].
- Harmonic Distortion (TD): It quantifies the specific n^{th} order harmonic distortion.
- Spurious free Dynamic Range (SFDR): The largest tonal signal is defined by this quantity. It is the ratio of the power of signal to the power of the largest undesired [9].

1.3 ADC Types

There are numerous types of ADC structures such as pipeline, successive approximation, flash and subranging ADC. Each of these ADC structure is used for a different kind of application. Today, most ADC applications can be comprised of four main segments [10]. These segments are data acquisition, precision industrial measurement, voice band and audio and high speed. Figure 1-8 shows the ADC architectures, applications, resolution, and sampling rates. Pipeline ADC, SAR ADC, and Sigma-Delta ADC are the popular ADC structures in the given segments. Besides their application areas, according to the working principle of the ADCs, they are divided into two groups which are Nyquist-Rate ADCs and oversampled ADCs. The nyquist theorem states that, the sampling frequency should be the two times higher than the maximum frequency of the input signal in order to prevent any aliasing. As a result, nyquist ADCs can handle the input frequencies up to half of the sampling frequency. On the other hand, in oversampled ADCs, the frequency of the input signal is less than the half of the sampling rate of the ADC. Thus, maximum achievable signal bandwidth is higher in Nyquist rate ADCs compared to the oversampled ADC. In this thesis, a

Nyquist rate ADC is proposed so that, in this section, some popular nyquist rates ADCs are analyzed.

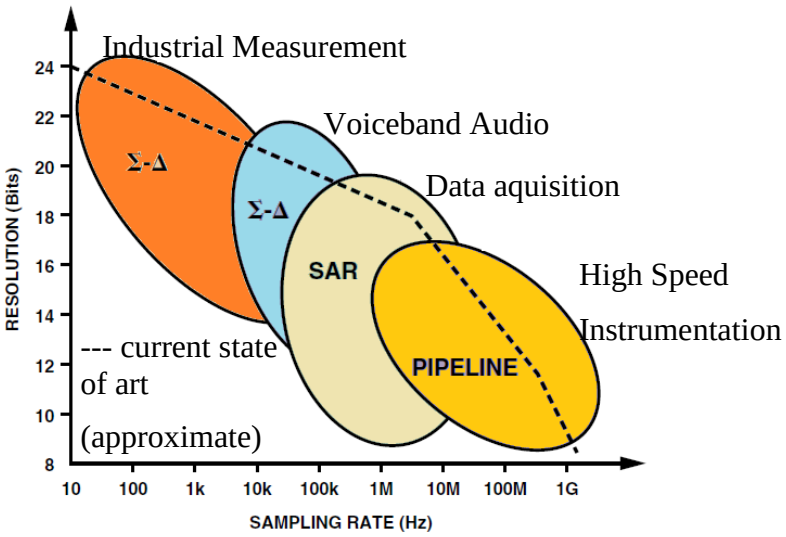

Figure 1-8: ADC architectures, applications, resolution and sampling rates [1].

1.3.1 Flash ADC

Flash ADCs known as parallel ADCs convert the analog signal into digital signal at high sampling rates. For the applications which require large signal bandwidth, flash ADCs can be used. High speed data acquisition, satellite communications or radar processing can be given as an example of the application areas for the flash ADC. Figure 1-9 shows a simple flash structure. The structure of the flash ADC is consist of a multiple number of analog comparator, and a decoder which generates the digital output according to the digital thermometer code. The analog input signal is connected to the each comparator input. The other inputs of each comparator are connected to a fixed reference voltage. Therefore, a comparison can be performed between the input signal and reference voltage for each comparator. In this structure, the conversion is performed in one step. Therefore,

high sampling rates can be possible. On the other hand, there are some drawbacks such as the number of logic and its power consumption. For an N bit-Flash ADC, 2^N-1 comparators are needed and 2^N-1 reference voltages should be generated. Thus, the density of the decoding logic circuitry increases. As a result, the power consumption, and the number of transistors increases. Therefore, Flash ADCs have low resolution while consuming considerable amount of power.

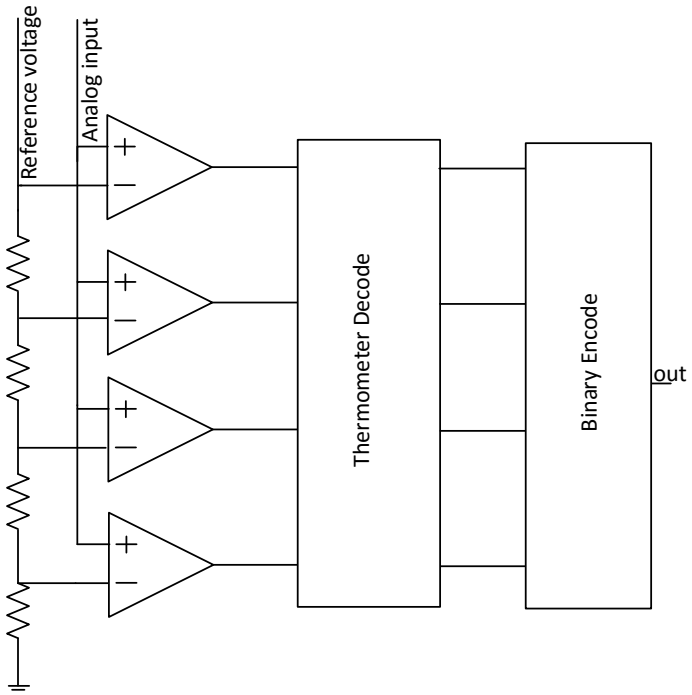

Figure 1-9: Simple flash architecture [10].

1.3.2 Subranging ADC

Subranging ADC is a multi-step parallel converter which is an alternative approach to the flash ADCs for the medium resolutions and high speed rates. The flash ADC structures cannot be used for high resolution applications due to the number of transistors and its power consumptions. The subranging ADCs employ the two step conversion techniques in order to reduce the complexity of the system and power consumption. Figure 1-10 shows a simple subranging architecture which performs the conversion in two steps. After the input voltage is sampled and held, the MSB bits are determined by the coarse conversion. The output of the coarse flash ADC is connected to a DAC which generates an analog voltage according to the output of the coarse flash ADC. The output of the DAC is then subtracted from the sampled and held analog input signal. The difference creates a residue voltage which is the input of the fine flash ADC. This residue voltage is fed into the fine flash ADC which determines the LSB bits.

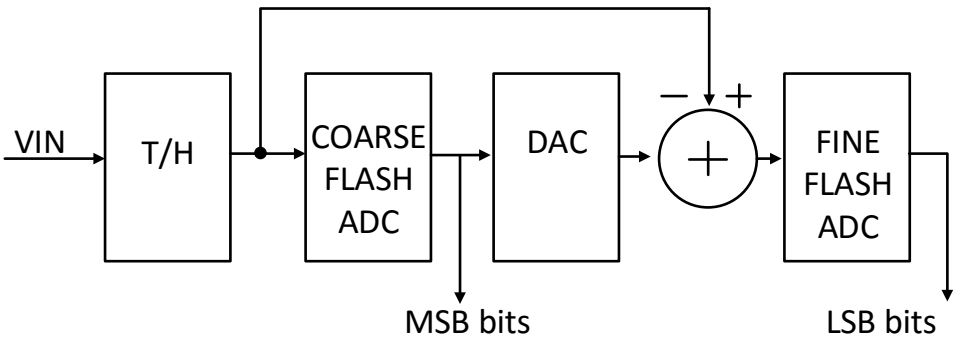

Figure 1-10: Simple subranging architecture [11].

Subranging ADCs can reduce the complexity of the structure compared to the flash ADCs. An N-bit subranging ADC requires ($2^{N/2}$-1) comparator where the flash ADC requires 2^{N}-1 comparators. As a result, an N-bit subranging ADC

requires less silicon area and dissipates less power compared to flash ADCs. On the other hand, there are some drawbacks such as speed and gain bandwidth. The speed of the subranging ADC is lower than flash ADCs if same clock frequency is used since, subranging ADCs require extra steps in order to complete the conversion. The gain bandwidth of the circuits in the subranging ADC is twice the gain bandwidth of the same types of circuits in the flash ADCs which leads to a reduced SNR value. In order to handle these disadvantages, parallel pipeline ADC structures are used.

1.3.3 Pipeline ADC

A pipeline analog-to-digital converter provides a high sampling rate and high resolution at the same time. This structure is a very popular among the ADC architectures for the very high sampling rates such as 100 MS/s. Pipelined ADC structure is comprised of multiple stages. All of the stages operate at the same time. Figure 1-11 shows a 12 bit pipeline ADC structure. Each stage has its own sample-and-hold circuit, ADC, DAC, and gain amplifier. Therefore, all stages can work simultaneously. In this structure, the input signal is fed through 3-Bit flash ADC while the input signal is sampled and held. Then, the output of the 3-bit ADC is connected to the 3-bit DAC which generates a residue voltage. The residue voltage is then subtracted from the sampled and held input voltage and gained up by a factor of A. This process is performed in each stage until the conversion is completed. In each stage except the final stage, at the output of the flash ADC, 3 bits are determined. At the final stage 4-bits are determined.

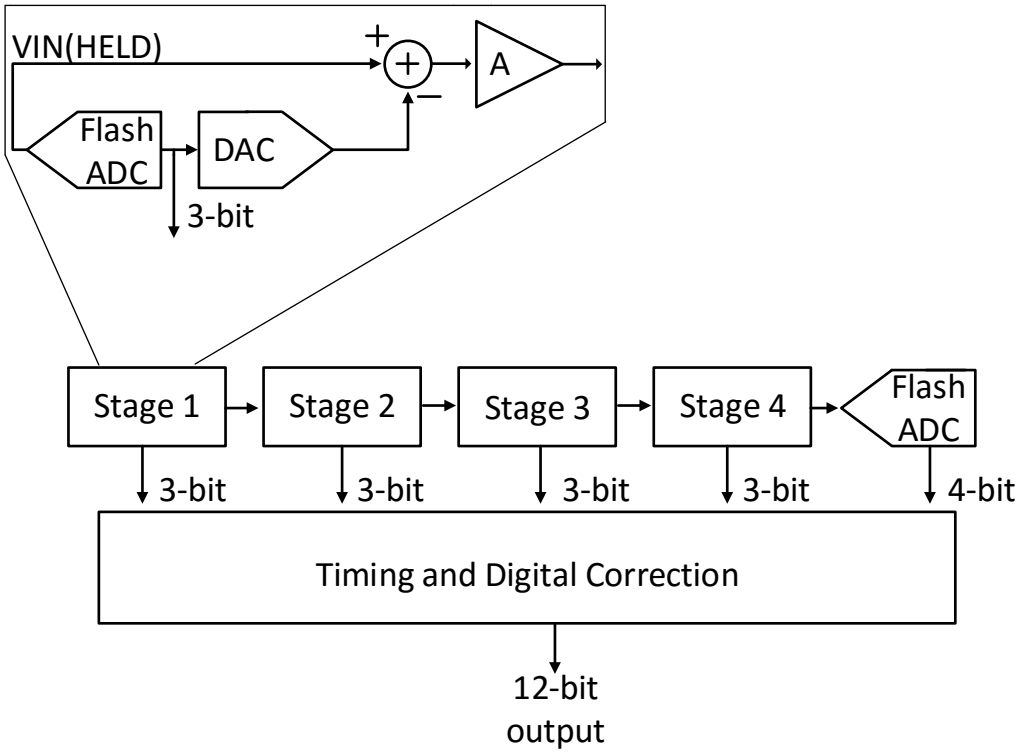

Figure 1-11: A 12 bit pipeline ADC structure [12].

1.3.4 Successive Approximation (SAR) ADC

Successive approximation register ADC known as SAR is a serial analog-to-digital converter which implements the binary search algorithm. In the previous sections, parallel ADCs are discussed. SAR ADC has a basic structure which consists of a sample and hold circuit, a precise DAC, a fine comparator, and digital logic in order to perform SAR algorithm. The conventional SAR ADCs have a few components which lead to dissipate low power consumption at the low sampling rates, and medium resolution. Figure 1-12 shows a SAR ADC structure. An N-bit DAC can be resistive or capacitive structure. At the beginning of the conversion, the analog input voltage is sampled and held. In the meantime, the output of the N-bit DAC is adjusted to the middle of the full scale voltage. Then a comparison is performed between the analog input and the output of the

DAC voltage. Depending on the output of the comparator, the output voltage of the DAC is set by the input digital words that are generated in the N-bit Register. For instance, if the analog input voltage is greater than the output of the DAC, in the next cycle, DAC generates a voltage at the middle of the upper half of the previous try. On the other hand, if the V_{IN} is smaller than the output voltage of the DAC, this time DAC generates a voltage at the middle of the lower half. This comparison continues until the conversion is completed. For a N-bit SAR ADC, the conversion takes N step.

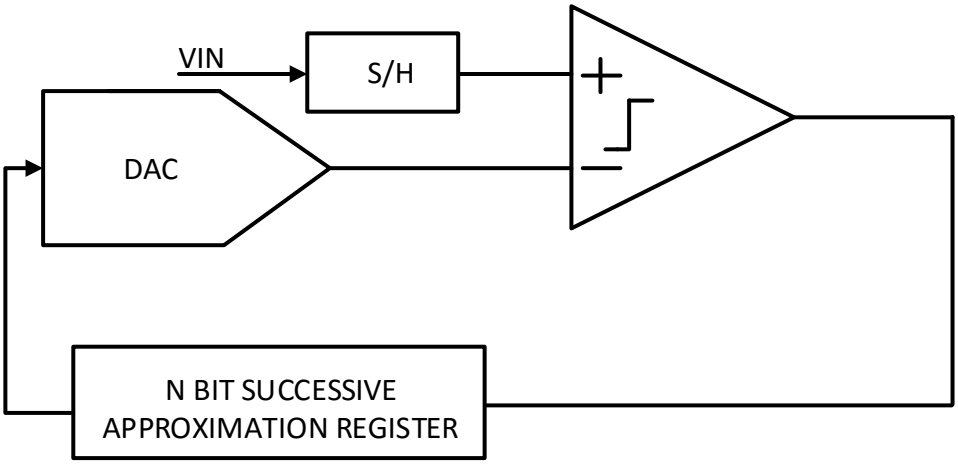

Figure 1-12: SAR ADC structure [13].

1.4 The Motivation of the Thesis

The main purpose of this thesis is to design and implement a low power, low speed analog-to-digital converter which does not require large silicon area. The commercial ADCs dissipate considerable amount of power, which leads to a power hungry systems. Besides that, commercial ADCs need too much external components such as capacitors, resistors, and voltage regulators in order to operate, which cause the design of large PCBs. Due to the PCB routings and power planes; the system noise seriously affects the performance of the whole system. The designed ADC in this thesis can be embedded into the sensor chip applications. As a result, the external components can be reduced which means that the size of the PCB can become smaller. The power dissipation of the whole system can be reduced by using full custom SAR ADC. A moderate resolution which is 12 bit is sufficient for this work. The proposed ADC will be used in different sensor applications ranging from DC to KHz. More specifically, the designed ADC is to be used as a test ADC in which the significant voltages in the sensor chip can be monitored. The proposed SAR ADC can monitor only one voltage which can be upgraded to monitor multi-voltage by using simple multiplexers. Power is the main concern for this design since battery life is a crucial concern in sensor applications. SAR ADCs can provide low power solutions which can operate at low frequencies, and at medium resolutions. Moreover, SAR ADCs does not require too many components which mean that the required silicon area can be small. Other types of topologies either consume too much power or require large silicon area at the desired resolution. As a result, SAR ADC structure is the optimized choice for this study.

1.5 Research Objectives and Thesis Organization

The main objective of this thesis is to develop a low power, moderate resolution small ADC prototype for sensor applications. The silicon area should be as small as possible. Therefore the standalone ADC should have minimum number of pads. The resolution of the ADC is 12 bit with a sampling rate 20 KS/s. The main task of this designed ADC is to monitor the important voltages that cannot be observed from the outside of the chip. The first prototype is a standalone version. However, after the characterizations it will be integrated into sensor chips. The detailed objectives of this study are given below.

1. Development of a system model of the SAR ADC. The whole system should be analyzed at the system level in order to extract the basic information about the SAR ADC.
2. Design and implement the SAR ADC. The proposed ADC should be low power and low noise. In order to test the chips properly different test structures should be added to the chip.
3. The printed circuit board with firmware and software should be designed. The whole test system should be low noise and basic parameters such as static parameters and dynamic parameters should be measured. The organization of the thesis is given as follows:

Chapter 2 analyses the SAR ADC at the system level.

Chapter 3 explains the detailed information about the implementation of the SAR ADC. It discusses the analog blocks and digital blocks in detail.

Chapter 4 clarifies the test system for the implemented ADC.

Chapter 5 concludes the thesis and gives information about the future work.

CHAPTER 2

SYSTEM DESIGN AND ANALYSIS OF THE SAR ADC

System level design of an ADC is an important step for designing a converter. Before implementing an ADC at transistor level, the system should be analyzed at the system level, since whole system should be clarified without any doubt. In the analog domain, switched capacitor circuits can exhibit some nonlinear behaviors caused by process variations or layout issues. Sometimes, it is difficult to foresee these behaviors at the transistor level design. By modeling the proposed ADC structure, these non-ideal behaviors can be examined and necessary parameters can be extracted from the system level simulations.

Chapter 2 reviews the modeling of the SAR ADC. Section 2.1 introduces a single ended SAR ADC, in order to understand the basic principle of the SAR ADC. Section 2.2 explains the ADC architecture used in this work. Section 2.3 analyses the analog blocks such as DAC array and comparator. Section 2.4 discusses the digital blocks at the system level. Section 2.5 shows the top level simulation of the SAR ADC in order to verify the operation of the system.

2.1 Introduction

In a generic SAR ADC structure, there are 3 main blocks which are a DAC array, a comparator and a simple digital controller for performing the binary search algorithm. DAC array is an important block for the SAR ADC which can be a resistive type or a capacitive type. Both of them are very sensitive to the process variations, and mismatches arise from layouts. As a result, some undesired non-idealities such as static errors INL and DNL can arise from these variations. These non-idealities can sometimes seriously affect the performance of the circuit. For example, DNL can cause missing codes which degrade the performance of the ADC. For this reason, a system level design is required in order to study the main architecture of the ADC. Before starting with the main architecture used in this study, a simple single ended SAR ADC is analyzed. Figure 2-1 shows a single ended SAR ADC architecture. The input voltage is sampled and held at the positive node of the comparator. The negative node of the comparator is connected to the output voltage of the DAC. At each cycle, the input voltage is compared with the output voltage of the DAC. According to the comparison result, the output voltage of the DAC is updated.

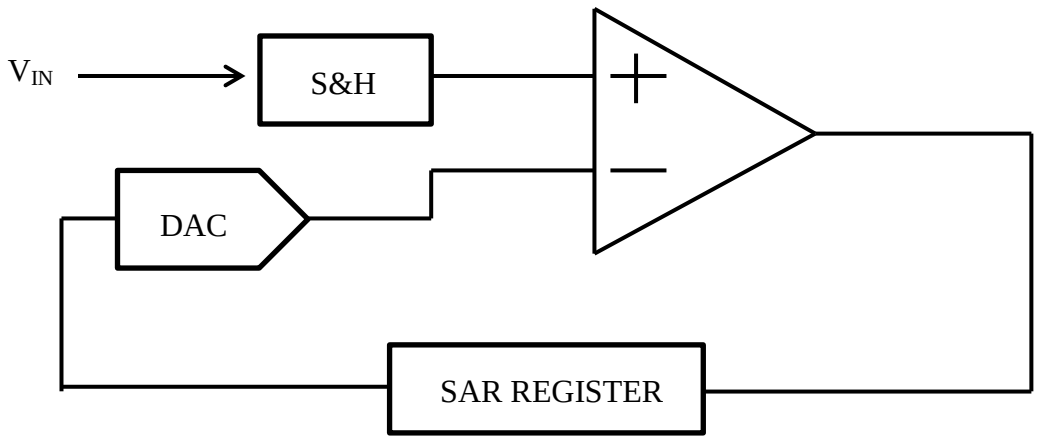

Figure 2-1: Single ended SAR ADC structure.

Figure 2-2 shows the output voltage of the DAC when 12 bit SAR ADC is used. The input voltage is 3.3V and it is compared with the output voltage of the DAC array. The reference voltage of the DAC array is 3.3V. Thus, the first comparison is performed between 3.3V and 1.65V, since the MSB bit goes to high and the remaining bits equal to 0. Then, the output of the DAC is updated according to the comparison result and another conversion cycle is performed. For 12-bit ADC, 12 clock cycles is required in order to perform 12 different comparisons. The conversion result of the full scale voltage 3.3V is “111111111111” which is the highest output code.

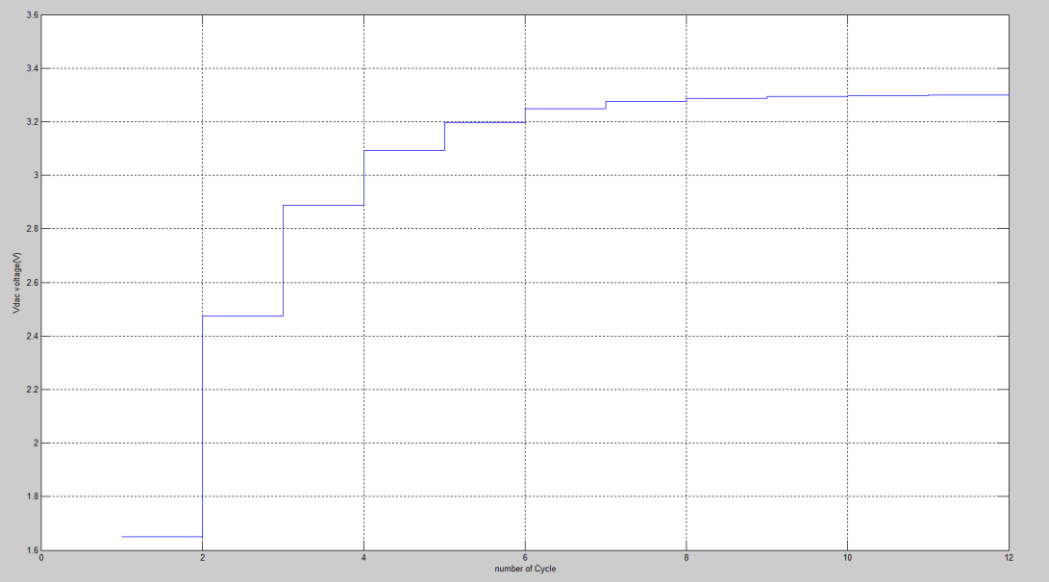

Figure 2-2: Output Voltage of the DAC when 12 bit ADC is used.

Section 2.2 analyses the system architecture used in this work.

2.2 SAR Analog-to-Digital Converter Architecture

The proposed SAR ADC structure is a fully differential rail to rail structure which means that the input voltage range covers the supply voltages. In this structure, there are two input signal channels. For each signal channel, there is a DAC array which is composed of unit capacitors. The capacitors in the array are used for sampling the signals and performing the conversion. Figure 2-3 shows the system architecture of the proposed SAR ADC. It has two symmetric DAC arrays which are comprised of the split binary weighted capacitors. A differential input voltage is applied to the inputs of the DAC array. The output of the comparator is one if the voltage at the positive terminal is greater than the other at the other terminal otherwise the output is zero. The proposed ADC is a 12 bit SAR ADC in which the MSB bit is a sign bit. The remaining 11 bits are decided by the result of the comparison. The digital controller generates the 11 bits according to the comparison result and these 11 bits are fed into the input of the DAC arrays which generate the appropriate voltages.

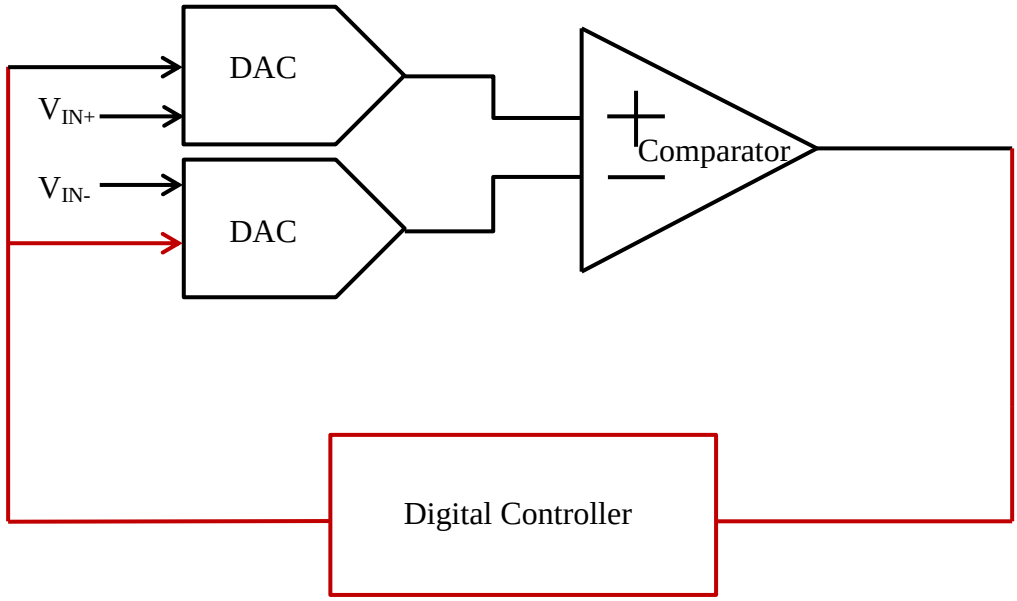

Figure 2-3: System Architecture of the proposed SAR ADC.

The analog blocks are the critical part of this study. Many performance parameters and specifications of the ADC are determined by these blocks. The following section discusses the analog blocks in detail.

2.3 Analog Blocks

This section introduces the model of each analog block in detail. Section 2.3.1 discusses the model of the comparator and its important parameter. Section 2.3.2 investigates the DAC array structure and its impacts on the static performance parameters of the ADC.

2.3.1 Comparator

In the SAR ADC, a fully differential, and rail to rail comparator is employed. The comparator model is simply based on the subtraction of the two inputs. Figure 2-4 shows a comparator model with the series offset voltage. The modeling is performed in the following orders: The two inputs are subtracted from each other, and then a constant offset voltage is summed up with this difference. After that, the result is multiplied with a constant value which is the gain of the comparator. Then, the result is saturated to full logic level and a comparison is performed with zero in order to decide which one is high. One of the important parameter for the comparator is the offset voltage. It is a static error which arises from mismatches of the transistors or process variations [14]. It can be either positive or negative voltage which can be connected to either positive terminal or negative terminal of the comparator in the models. The offset voltage can affect the result of the comparison. In order to reduce the effect of the offset voltage, proper offset cancellation techniques such as dynamic offset cancellation method can be used.

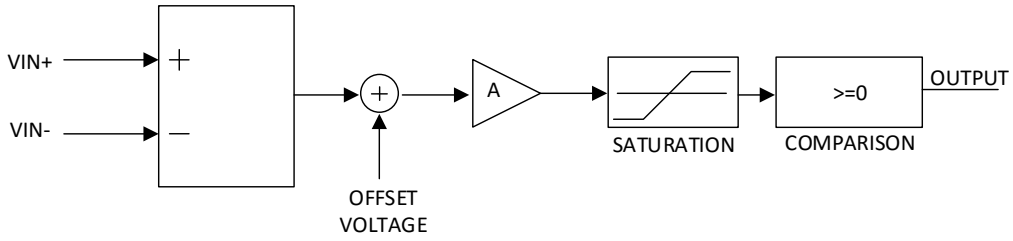

Figure 2-4: Comparator model with the series offset voltage.

2.3.2 Digital-to-Analog Converter

Digital-to-analog converter is an important block in the SAR ADC structures since; it is a key aspect for the performance of the ADC [15]. In conventional SAR ADCs, DACs can be used for two different operations:

1. Capacitive DACs can be used as a sample and hold block in order to reduce the number of components. In this case, an additional sample and hold block is not required. Today, in many ADC structures, bottom sampling technique is used in order to sample and store the input voltage at the input nodes of the comparator [16].
2. Different kinds of DACs are used for performing the binary search algorithm. At each cycle, according to the result of the previous comparison, DAC output is updated and new voltages are generated at the input nodes of the comparator.

In literature, there are different kinds of DAC structures which are mainly capacitive DAC arrays, resistive DAC array and hybrid DAC array that composed of both resistive and capacitive structure. Figure 2-5 shows an ADC structure with capacitive digital-analog converter. A binary weighted capacitor array is employed in the ADC structure which generates the required voltages at the input of the comparator. The top plates of the each capacitor are connected to

each other and no series capacitor is used at this node. The input voltage is sampled on the capacitor array by using bottom plate sampling technique which does not require any additional sample and hold circuit. The comparison is performed with reference the voltage which is connected to the positive node of the comparator. A reference voltage at the output of the DAC array is used to reset the output voltage at the beginning of the conversion.

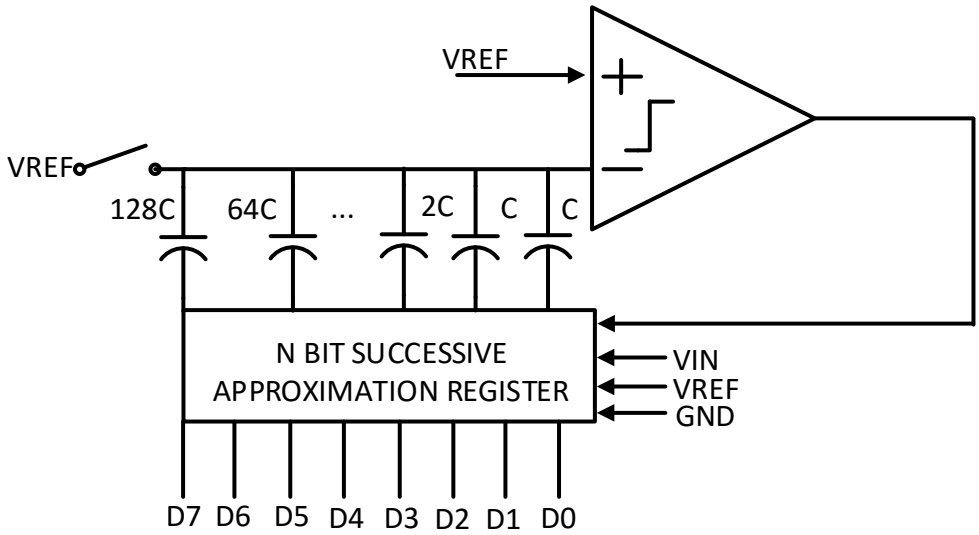

Figure 2-5: ADC structure with capacitive digital-to-analog Converter [17].

Figure 2-6 shows the resistive digital-to-analog converter array with the switches. The switches are programmed by the digital controller depending on the result of the previous comparison result. The output voltage of the DAC is generated by simply dividing the V_{HIGH}. An additional sample and hold block is required which occupies an additional silicon area. The resistors dissipate a considerable amount of power, since a current flow through the resistors.

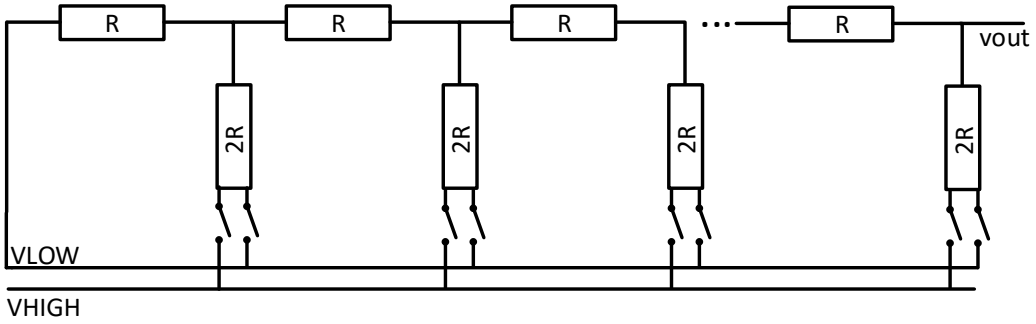

Figure 2-6: Resistive Digital-to Analog Converter Array [4].

Figure 2-7 shows a hybrid digital-to analog converter array. The hybrid DAC array is divided into two arrays which are referred as main DAC and sub DAC. The main DAC array consists of binary weighted capacitors which provide the sampling and holding the input signal and perform the binary search algorithm. The sub DAC is comprised of R-2R resistive ladder and the output of the resistive array is connected to the capacitor series with the output of the sub-DAC array. Thus, the output voltage of the sub-DAC can be stored in one of the capacitors in the main DAC.

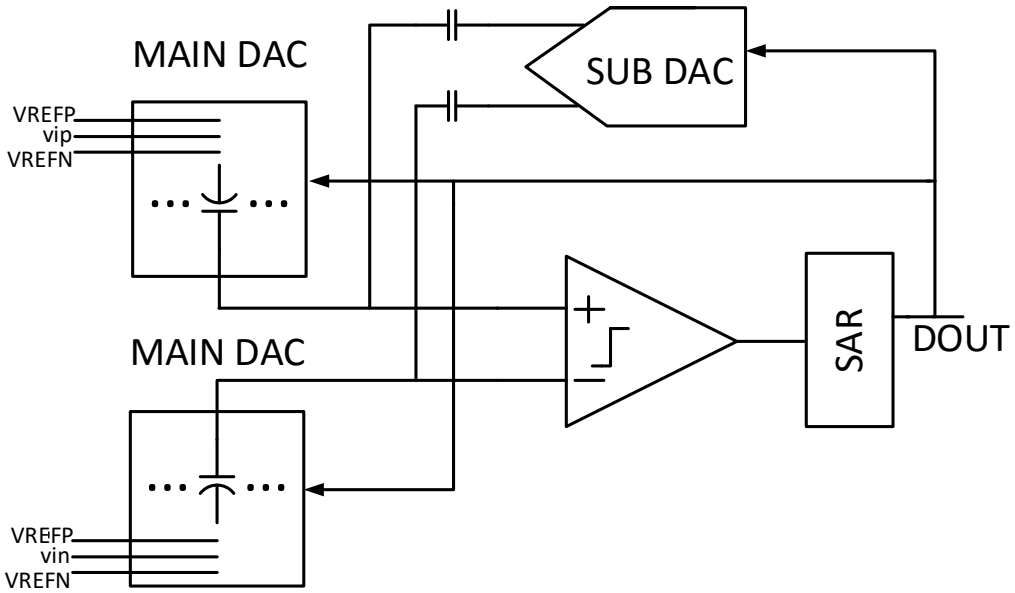

Figure 2-7: Hybrid Digital-to Analog Converter Array [18].

Each of the DAC structure shown in the previous figures is used for different kinds of SAR ADC. When deciding the structure of the DAC array, different considerations should be taken into account such as power consumption, noise, settling, mismatch parameters or required silicon area. Resistive DACs dissipates considerable amount of power for high resolutions which is not suitable for this work. Thus, in this thesis, a capacitive DAC array is preferred since; capacitors can be used for both sampling and holding the input signals and providing the required voltage variations in order to perform the binary search algorithm without any significant power consumption. There are different kinds of capacitive DAC arrays such as parallel binary weighted capacitor array, split capacitor array with series capacitor, or C-2C capacitor array. Each DAC structure offers a different solution and it provides different advantages. The resolution of the proposed ADC is 12 bit in which the MSB bit is a sign bit. Thus, an 11-bit capacitor array is required in order to perform the binary search algorithm. The proposed design consists of a fully differential rail to rail comparator which means that, two identical capacitor arrays are required in this work. The analysis given in this section is based on the single capacitor array, since identical DAC arrays are used in the structure. The most common capacitive DAC array consists of all parallel binary weighted capacitors. Figure 2-8 shows the conventional parallel binary weighted capacitor array. All the capacitors are built from unit capacitors. The largest capacitor consists of 2^{N-1} unit capacitors where N is the number of bits. Due to the fact that, there is no series capacitor at the top plate of the capacitor node, there is no parasitic capacitor caused by the bottom plate or top plate of the series capacitor. Sampling, charging and discharging functions are all performed on the same capacitor arrays. Thus, additional sample and hold circuit is not required.

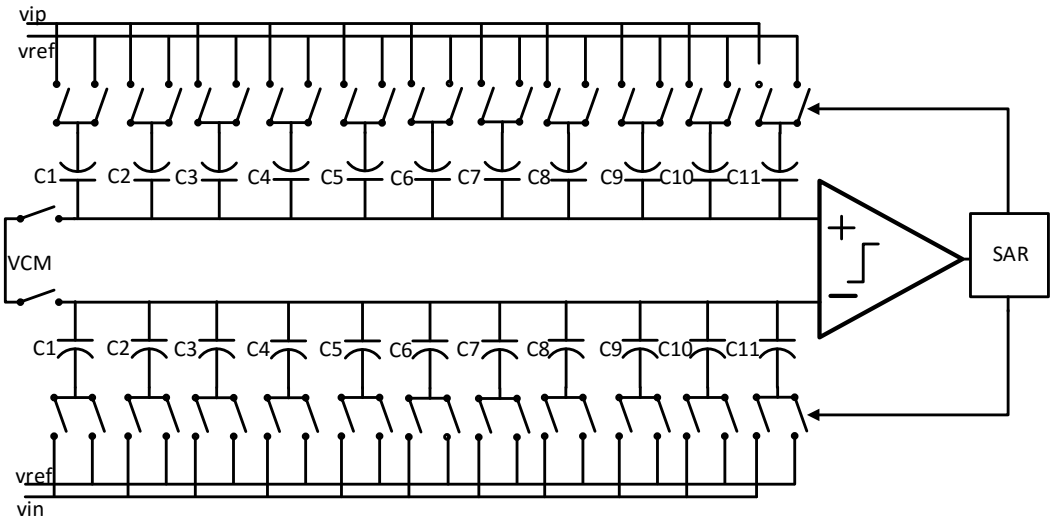

Figure 2-8: Conventional Parallel binary weighted capacitor array [19].

Figure 2-9 shows an 11 bit binary weighted capacitor array which shows each capacitor value. V_X is the voltage at the input nodes of the comparator. Each capacitor is connected to the common node referred as V_X. On the other hand, the bottom plate of each capacitor is connected to the switches called as D, which provides the connection to reference voltage, common mode voltage or input signal. C_{CM} is used for dividing the reference voltage by exactly two at each step [20]. This capacitor is connected to the input signal at the sampling phase. After sampling, it is connected to the common mode voltage and it does not change upon a new sampling phase.

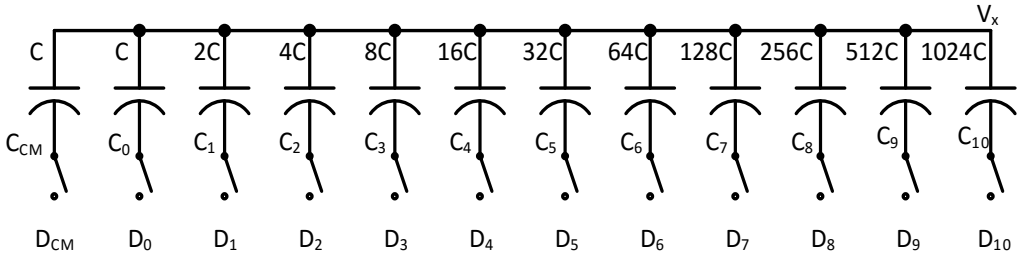

Figure 2-9: 11 bit binary weighted capacitor array.

The binary weighted capacitive DAC array requires large silicon area, since there are 2^NC unit capacitors where N denotes the resolution. The proposed SAR ADC is 12 bit and the layout area should be as small as possible. For this reason, this structure cannot be used in this work. Another approach is that the binary weighted capacitor array can be split into two or more sub arrays using one or more series capacitors [21]. Splitting the DAC array in one or more sub arrays does not change the voltage variation at the input node of the comparator, as long as the same capacitor ratios are kept. Figure 2-10, Figure 2-11, and Figure 2-12 shows different types of split capacitor topologies. In each structure, there exists a series capacitor which can be referred as a bridge capacitor. The sub arrays are connected together with these bridge capacitors, and the values of the series capacitors are adjusted to the certain values that provide the proper voltage division. The advantage of these topologies is the reduction of the number of capacitors used in the DAC array. As a result, the silicon area can be reduced by using the split array with series capacitor.

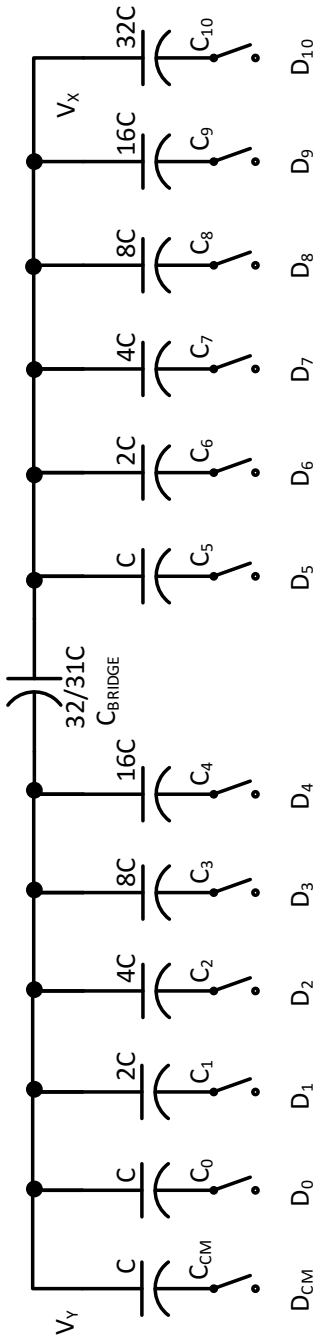

Figure 2-10: Two sub binary weighted capacitor array (2bw1C_{BRIDGE}).

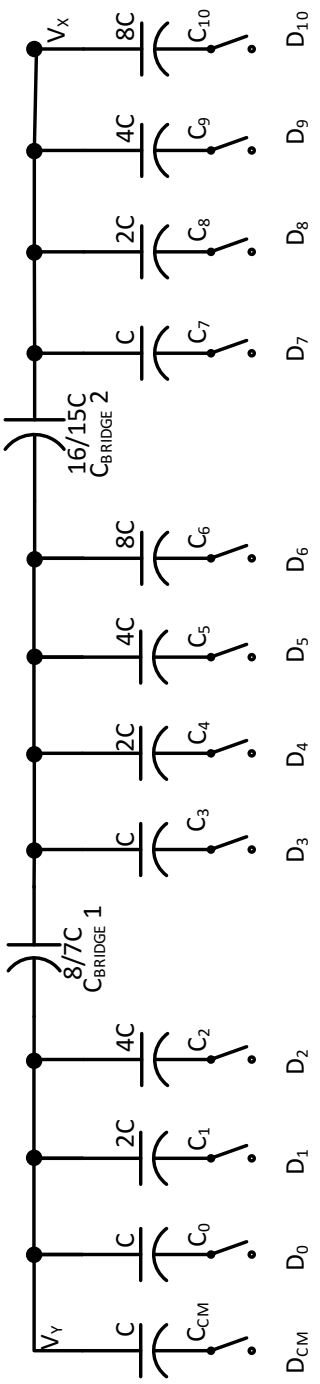

Figure 2-11: Tree sub binary weighted capacitor array (3bw2C_{BRIDGE}).

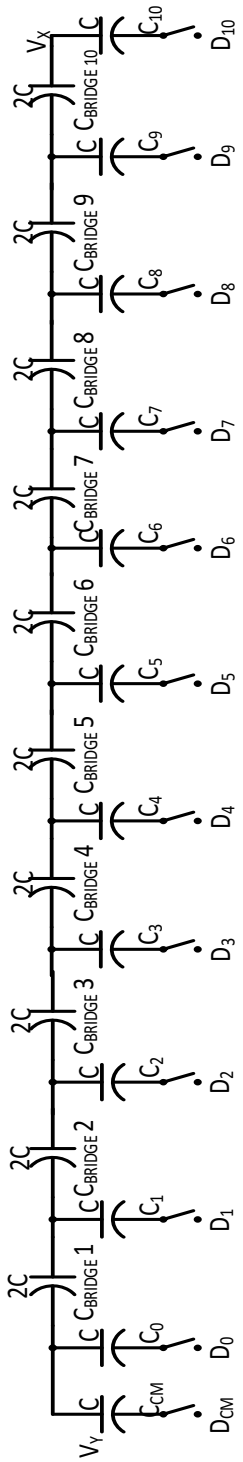

Figure 2-12: C-2C ladder digital-to-analog converter topology.

Besides the silicon area, the linearity errors due to the process variations and layout issues should be investigated for each DAC topology. The maximum linearity error occurs when the switching scheme is "100….00" which implies that the MSB equals to one and the remaining bits are set to zero [22]. In this work, the three topologies shown in Figure 2-10, Figure 2-11, and Figure 2-12 are investigated in detail. For each topology, the worst case in which the MSB bit is HIGH, and the remaining bits are LOW is analyzed. For two sub array with series capacitor (2bw1C_{BRIDGE}), the output voltage can be written as the following:

$$V_x = \frac{C_{10}}{\frac{(C_{CM} + \sum_{k=0}^{4} C_k) \cdot C_{BRIDGE}}{(C_{CM} + \sum_{k=0}^{4} C_k) + C_{BRIDGE}} + \sum_{k=5}^{9} C_k + C_{10}} v_{REFP} \qquad (2.3.2.1)$$

where V_{REFP} refers to the reference voltage of the capacitor array which is 3.3V in this work. In order to analyze the voltage at node V_X, mismatches should be taken into consideration. In 0.35 um CMOS technology, the standard deviation of the mismatch of the capacitor is written as the following,

$$\sigma(\frac{\Delta C}{C}) = \frac{A_C}{\sqrt{W\ L}} \qquad (2.3.2.2)$$

where $\sigma(\frac{\Delta C}{C})$ represents the standard deviation of the fraction of the difference ΔC to the absolute value C, and A_C is the process dependent parameter which is 0.65 % μm in the 0.35 μm CMOS technology. W and L are the width and length of the unit capacitor. The standard deviation equation can be modified in order to show the standard deviation of a unit capacitor. The standard deviation of a unit capacitor can be written as the following:

$$\sigma(C_U) = \frac{\sigma(\frac{\Delta C}{C})}{\sqrt{2}}\mu_C \qquad (2.3.2.3)$$

where μ_C is the means of the unit capacitor. While calculating the voltage distribution of the V_X, the unit capacitor is chosen as 620 fF in order to determine the most appropriate structure. The sizing of the unit capacitor will be discussed detailed in terms of settling time, noise and other considerations in chapter 3 in detail. Figure 2-13 shows the Gaussian distribution and histogram of the unit capacitor. 2000 samples are taken in order to examine the effects of the unit capacitor. The unit capacitor can be slightly different than the actual value due to the process variations. The y axis called as Counts shows the number of occurrence for a given capacitor value. The mean of the Gaussian distribution is 620 fF.

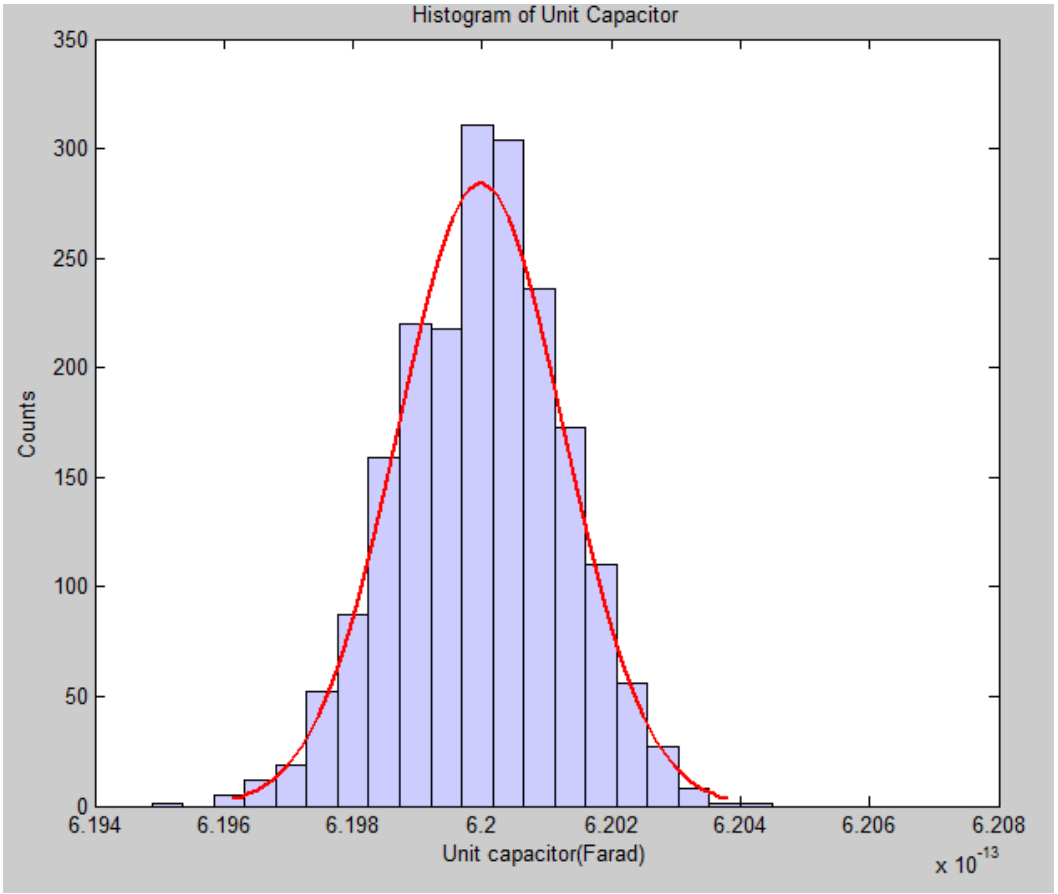

Figure 2-13: Gaussian distribution and histogram of the unit capacitor.

Figure 2-14 show the histogram and voltage distribution of V_X when one series capacitor and two sub DAC array exists. The mean of the voltage distribution is 0.8246 V. In order to ensure that, the linearity performance of the DAC is met, the following equation must be met:

$$3\sigma(D_{IN} = 1024) < 0.5\text{LSB} \tag{2.3.2.4}$$

where LSB can be written as;

$$\text{LSB} = \frac{6.6}{2^{12}} \approx 1.61\, mV \tag{2.3.2.5}$$

The standard deviation of the DAC output is calculated as 22.47 μV. Three times this value which is 67.433 μV is less than the half of the LSB voltage and the probability that $V_X \in (\mu - 3\sigma, \mu + 3\sigma)$ is 99.7 % which concludes that a good linearity performance is met.

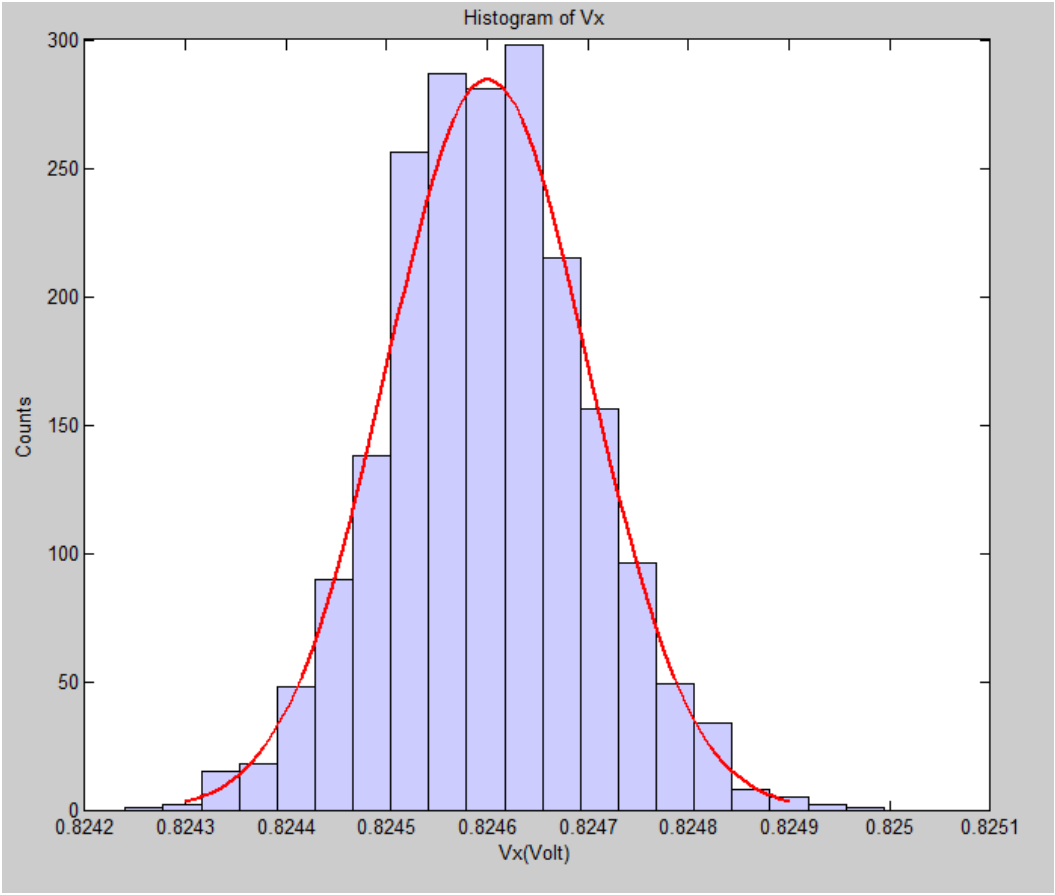

Figure 2-14: Histogram and gaussian distribution of V_X when one series capacitor and two sub DAC array exist.

Figure 2-15 shows the histogram and Gaussian distribution of V_X when two series capacitor and three sub DAC array exist. The standard deviation is 44.59 μV, and three times standard deviation is 133.78 μV which is greater than the standard deviation calculated for two sub DAC array with one series capacitors.

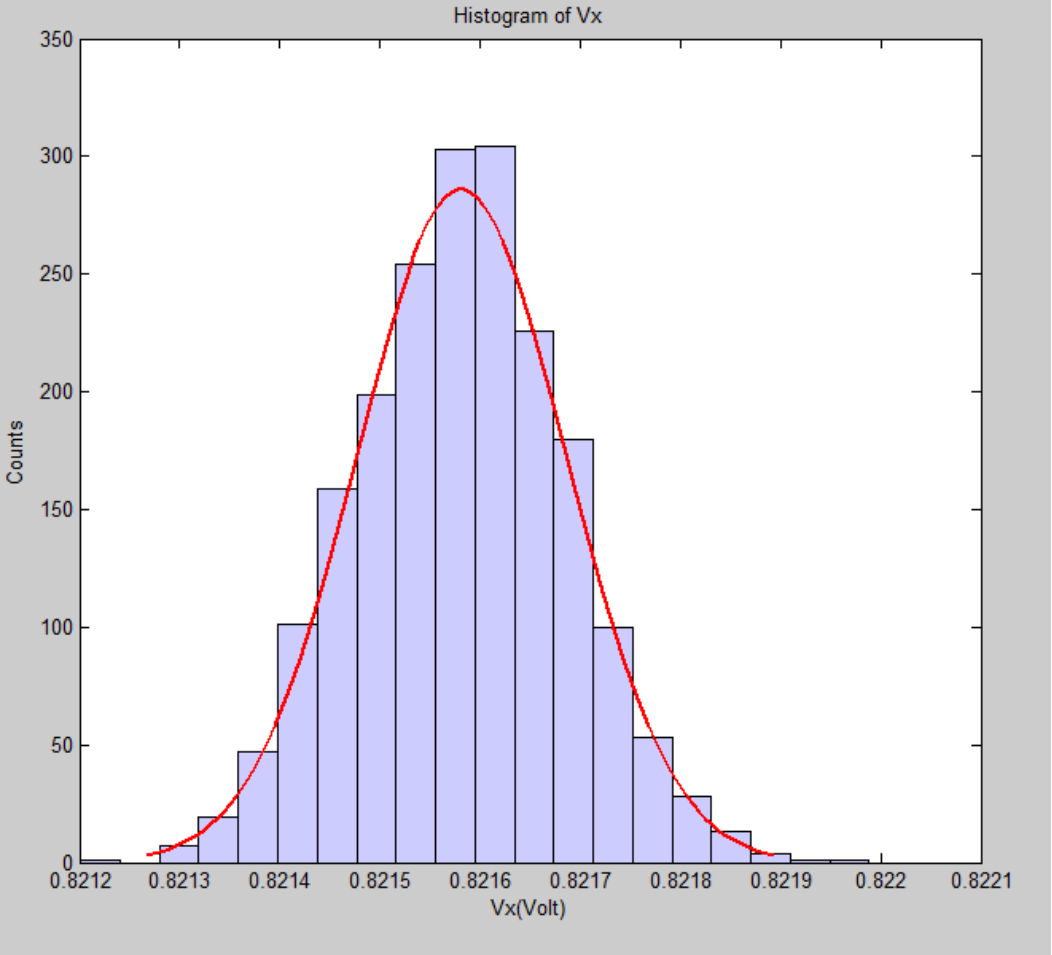

Figure 2-15: Histogram and Gaussian distribution of V_X when two series capacitor and three sub DAC array exists.

Figure 2-16 shows the histogram and Gaussian distribution of V_X when a C-2C ladder is implemented. The standard deviation is 68.118 µV. Three times standard deviation is 204.35 µV. For the given three topologies, the standard deviation is less than the half of the LSB which shows that, these topologies are not affected seriously for the given unit capacitor by the process variations. However, the best performance is obtained with the two sub DAC array with one series capacitor.

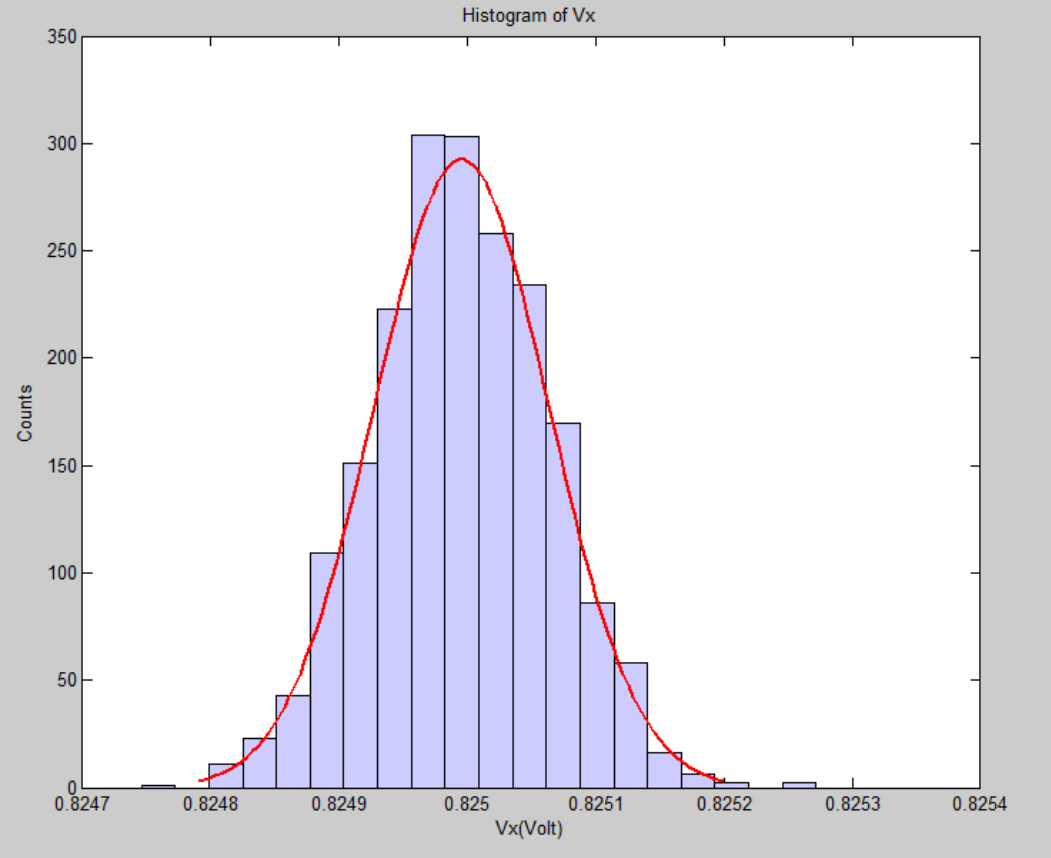

Figure 2-16: Histogram and Gaussian distribution of V_X when a C-C2 ladder is implemented.

The capacitive DAC array can also be affected by the parasitic capacitors connected to the output node of the DAC array. These parasitic capacitors can degrade the linearity performance of the converter. The parasitic capacitors arise from the bottom plate and top plate of the series capacitors. The pure binary weighted capacitor array without any series capacitor does not encounter with these parasitic capacitors, since there is no series capacitors at the output node of the DAC array. On the other hand, the series capacitor is existed in the split DAC array topologies. In these topologies, parasitic capacitors can be seen at the top and bottom plate of the series capacitors, and the effects of these parasitic capacitors are not constant for different input voltages [23]. As a result, these parasitic capacitors alter the charge conservation equations at the output nodes of

the DAC output voltage in which leads to the degradation of the linearity. Figure 2-17 shows the equivalent circuit of the 2bw1Cs digital-to-analog converter array. The parasitic capacitor is modeled at the bottom plate of the series capacitor, since the parasitic capacitor of the bottom plate of the series capacitor dominates the parasitic capacitor caused by the top plate of the series capacitor. According to the digital input, m and p show the number capacitors connected to either reference voltage or common mode voltage. The charge conservation equations at node V_X and V_Y can be the followings:

$$C_{P1}(V_{CM} - V_{DD}) = mC(V_Y - V_{REFP}) + (32 - m)(V_Y - V_{CM}) + \frac{32}{31}C(V_Y - V_X) + C_{P1}(V_Y - V_{DD}) \quad (2.3.2.6)$$

$$0 = pC(V_M - V_{REFP}) + (63 - p)C(V_M - V_{CM}) + \frac{32}{31}C(V_X - V_Y) \quad (2.3.2.7)$$

by solving the system of the equations the effect of the parasitic capacitor can be observed.

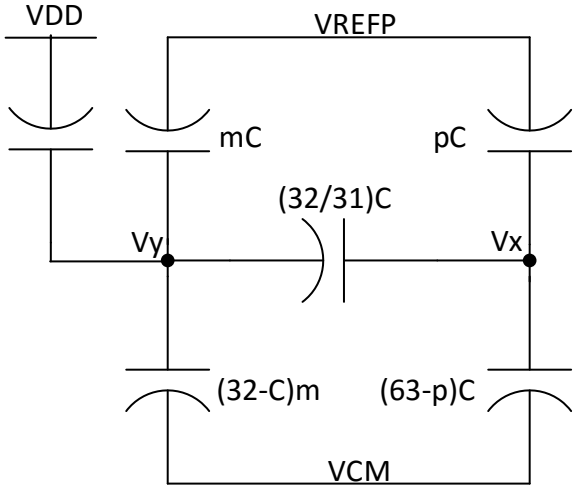

Figure 2-17: Equivalent circuit of the 2bw1Cs digital-to-analog converter array.

Figure 2-18 show the DNL graph estimation of the 2bw1Cs capacitor array. The graph shows the DNL error for each input code. In conventional ADCs, in order

to have a good linearity performance, the DNL should be kept below the half of the LSB voltage. The DNL graph shows that, the maximum and minimum DNL values are around half of the LSB voltage which implies that, there should not be a missing code in the designed DAC.

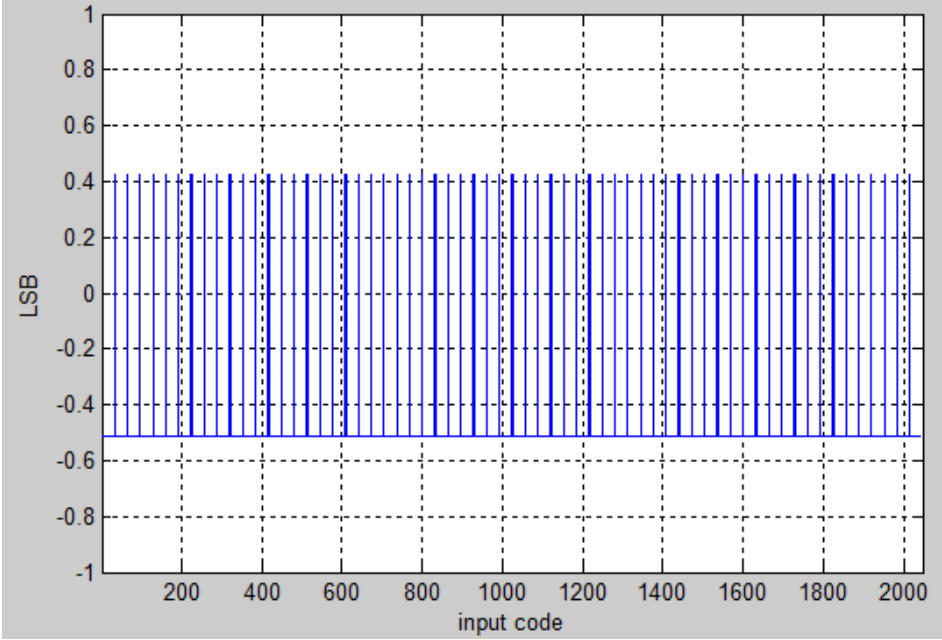

Figure 2-18: DNL graph estimation of the 2bw1Cs capacitor array.

The INL parameter should also be examined in order to evaluate the linearity performance of the DAC. Figure 2-19 shows the INL graph estimation of the 2bw1Cs capacitor array. The INL is kept below half of the LSB voltage over the entire input code. The result shows that, the effects of the parasitic capacitors create a INL and DNL errors less than the half of the LSB voltage.

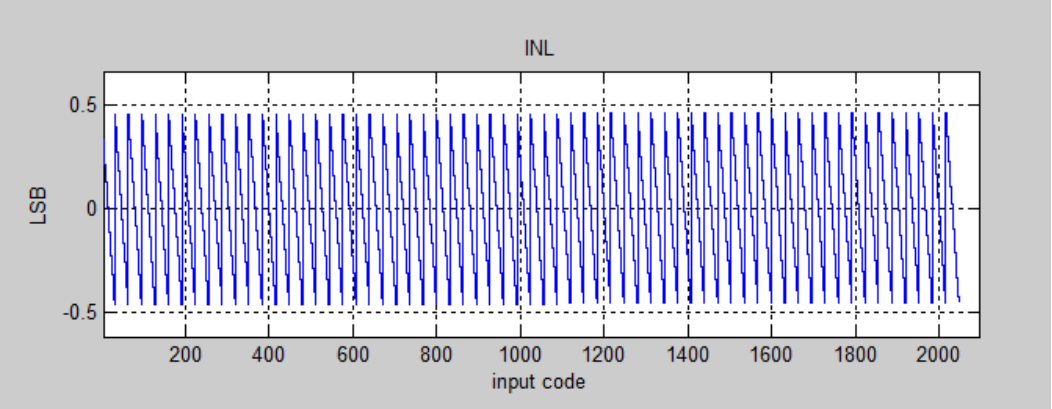

Figure 2-19: INL graph estimation of the 2bw1Cs capacitor array.

Figure 2-20 shows the output voltage of the DAC versus input code. The output voltage of the DAC increases linearly. The initial code is zero which means a minimum voltage referred as common mode voltage is observed at the output of the DAC. As the input code increases, the output voltage of the DAC increases, since more capacitors are connected to the reference voltage when the input code becomes greater. A magnified view for a portion of the graph shows how the output voltage increases step by step. It shows that, for each input code, there is an output voltage which means that there is no missing code in this design.

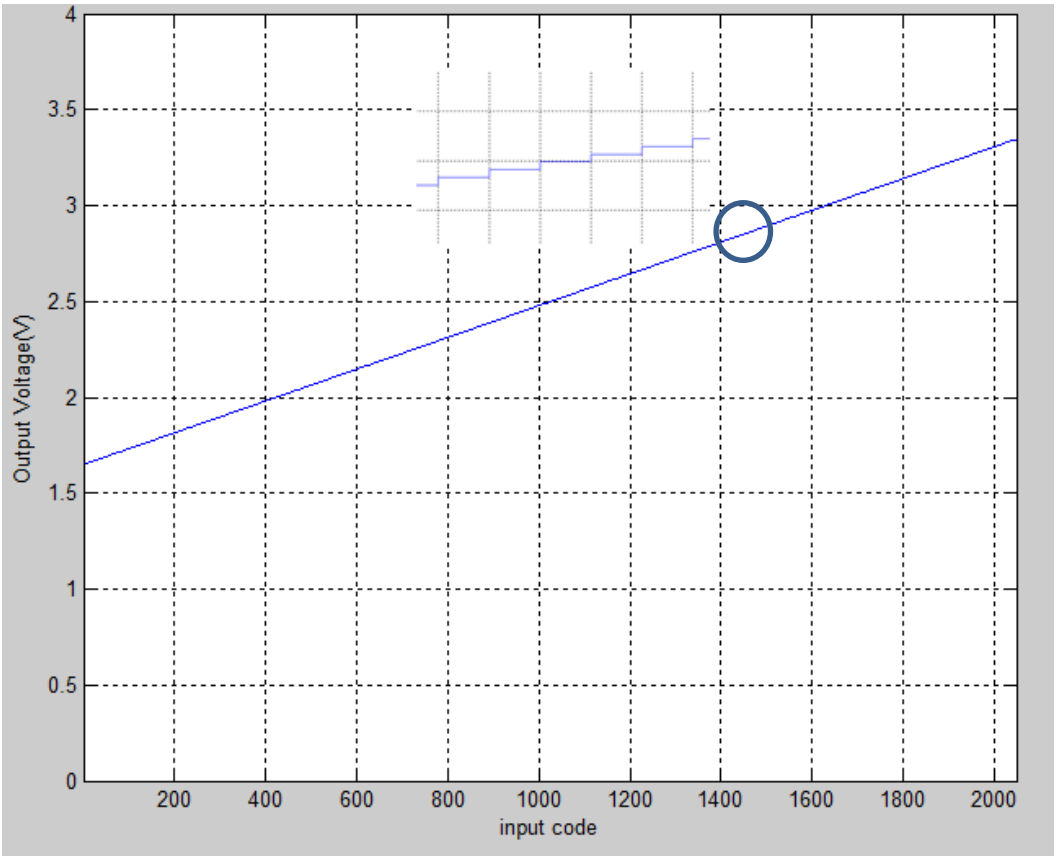

Figure 2-20: Output voltage of the DAC array versus input code

C-2C topology has the maximum number of series capacitor compared to other structures. For this reason, that topology is affected more compared to the other structures. As a result, the most appropriate choice for the DAC array in terms of the parasitic capacitors is the two binary weighted sub arrays with one series capacitor. The next chapter evaluates the capacitors based on the setting time, and noise performance.

2.4 Digital Blocks

In this thesis, there are five main digital blocks which are timing generator, output serializer, serial interface, memory, and successive approximation register. In this section, the proposed design is evaluated at system level. For this reason, this block is modeled in such a way that it simply performs the binary search algorithm. The detailed discussion about these blocks is given in Section 3.3.

2.5 Top Level Simulation

This section shows the top level simulation of the proposed SAR ADC. In the previous sections, all the analog blocks are discussed at system the level. The comparator is modeled as a device that subtracts the two different voltages, adds an offset voltage to the difference, multiplies that result with gain, and saturates the result to full logic. After that, the comparison is performed. If the result of the comparison is 1, the corresponding bit equals to 1. Otherwise, it becomes to 0. The capacitive DAC array is a 2bw1C topology which is two binary weighted DAC array with one series capacitor. It improves the linearity performance compared to the other structures. The digital block simply performs the binary search algorithm. Figure 2-21 shows the output voltage of the DAC for the proposed differential SAR ADC. The inputs are 0V and 3.3V respectively which means a 3.3V differential input voltage is applied. At the first cycle, the input voltages are compared with respect to each other and the sign bit is determined. Then, at the each cycle, the capacitive DAC array generates the necessary voltage variations according to the last comparison result. At the end of the conversion, the output voltages of the DAC array approach to the common mode voltage which is set to 1.65V in the designed ADC.

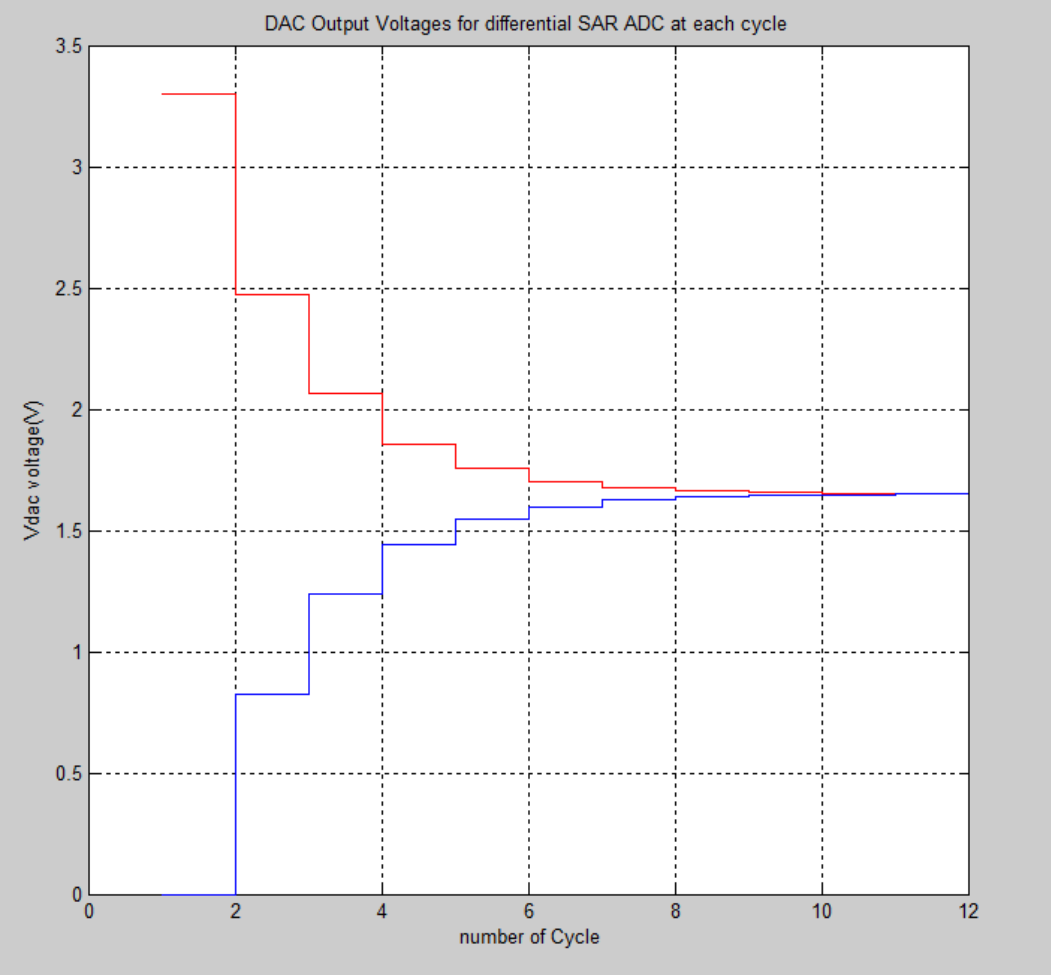

Figure 2-21: DAC output voltage for the proposed differential SAR ADC.

In conclusion, this chapter discusses the basic components of the SAR ADC at the system level. The basic parameter such as linearity is extracted. Important structures such as capacitive DAC array are discussed. Advantages and drawbacks of these structures are highlighted. The next chapter analyses the design and implementation of the proposed SAR ADC.

CHAPTER 3

IMPLEMENTATION OF THE SAR ADC

This chapter analyses the physical implementation of the SAR ADC. Section 3.1 introduces the basic information about the implementation of the SAR ADC. Section 3.2 investigates the implementations of the analog blocks in detail. In Section 3.3 explains the digital blocks. Section 3.4 clarifies the top level integration. Section 3.5 shows the top level simulations of the SAR ADC. Section 3.6 summarizes the implemented SAR ADC and compares the proposed work with the previous works.

3.1 Introduction

The implementation of the SAR ADC is a crucial step which should be carefully analyzed. The resolution of the proposed SAR ADC is 12 bit which is sufficient for the data acquisition applications. The proposed design should be low power, and low noise which are the main two concerns in this work. The proposed ADC is designed for low speed data acquisition applications and it will be worked into various sensor applications. The frequency of the input signal is ranging from 1Hz and 10 KHz. The sampling frequency of the SAR ADC is 20 KS/s which obeys the Nyquist rate. The sampling frequency of the SAR ADC is important, since it seriously affects the response time of the designed comparator. The SAR ADC has a fully differential rail to rail comparator which means that the inputs can cover the supply rails. The following sections cover the design of the analog and digital blocks.

3.2 Analog Blocks

This section investigates the analog blocks in detail. The analog block consists of DAC arrays and its switches arrays, a fully differential rail to rail comparator and a bias block which provides the required bias currents to the main analog blocks. The digital-to-analog converter is used for generating voltage variations for the comparator and performs the sampling and holding functions by using the switches. In this structure, additional sampling and hold block is not required. The comparator determines which of the input signal is greater than the other one. Section 3.2.1 evaluates the implementation of the digital-to-analog converter based on the electrical characteristics such as noise and settling time. It determines the value of size of the unit capacitor according to the given restrictions. Section 3.2.2, discusses implementation of the switches that are used with capacitive DAC array. Section 3.2.3 explains the structure of the comparator and offset cancellation utility. In Section 3.2.4 introduces the bias block.

3.2.1 Digital-to-Analog Converter

Digital-to-analog converter is an important block that directly affects the performance of the SAR ADC. Chapter 2 investigates the capacitive DAC array topology at the system level. In the proposed SAR ADC, 2bw1Cs topology which is comprised of two sub array and one series capacitor is chosen. Figure 3-1 shows the two binary DAC with one series capacitor. Two sub arrays are connected to each other via a series capacitor. The values of the capacitors are lower than the values of the capacitors in the pure binary weighed array. The unit capacitor is determined based on the electrical characteristics.

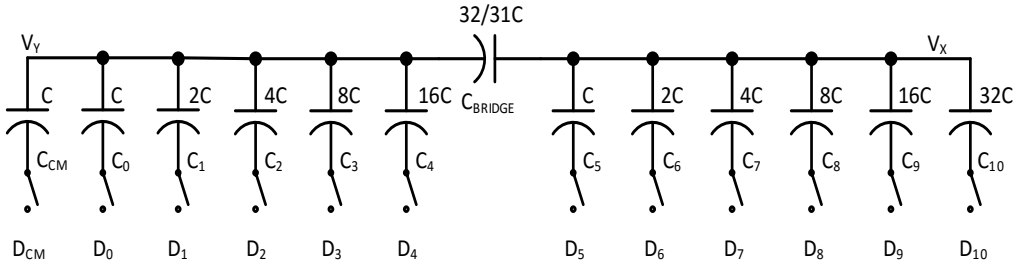

Figure 3-1: Two binary DAC with one series capacitor.

In 0.35 μm CMOS technology, the MIM capacitors referred as metal-insulator-metal capacitors are used. The thermal noise or Johnson-Nyquist noise which is referred as kTC noise limits the size of the unit capacitor. In general, in order to design a high performance ADC, the overall noise which is mainly dominated by the comparator and DAC array should be less than the half of the LSB voltage. It means that, the noise of the each component should be around the quarter of the LSB voltage. In the capacitor array, the noise can be written as:

$$V_{noise,RMS} = \sqrt{\frac{kT}{C}} \tag{3.2.1.1}$$

where k is the Boltzmann constant and T is the temperature. Figure 3-2 shows the RMS noise voltage with respect to the unit capacitor value. In order to have a noise less than the half of the LSB, the minimum unit capacitor should be 6.38 fF which is well below the minimum capacitor value permitted by the process.

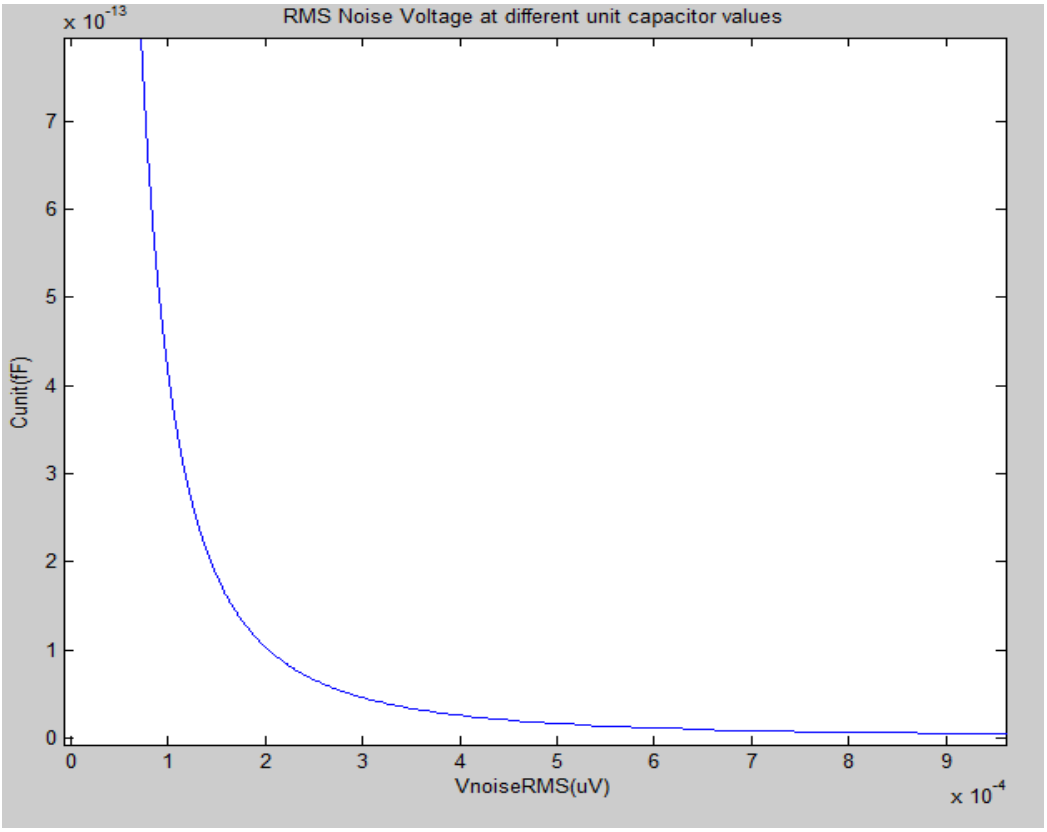

Figure 3-2: RMS noise voltage with respect to the unit capacitor value.

The SNR due to the thermal noise can be written as the following:

$$SNR_{Thermal} = \frac{P_{Signal}}{P_{Thermal}} = 10log_{10}\left(\frac{\frac{1}{2}\left(\frac{FS_{d-e}}{2}\right)^2}{\frac{2kT}{C_U}}\right) \qquad (3.2.1.2)$$

where k is the Boltzmann constant, T is the temperature and FS_{d-e}shows the full differential range which is 6.6V for the proposed designed ADC. The theoretical SNQR which is signal to quantization noise ratio should be written as the following

$$SQNR_{Theoritical} = 6.02\text{n} + 1.76 \quad (3.2.1.3)$$

where, n represents the number of the bits. For 12 bit ADC, the theoretical SQNR is 74 dB. In order to have a good system the thermal SNR should be greater than the theoretical value which can be written as the following:

$$SNR_{Thermal} \geq SQNR \quad (3.2.1.4)$$

$$C_U \geq 10^{\frac{6.02n+1.76}{10}} 4kT\left(\frac{2}{FS_{d-e}}\right)^2 \approx 38.2\text{fF} \quad (3.2.1.5)$$

which implies that the minimum capacitor should be 38.2 fF for satisfying the SNR requirement. Although, the unit capacitor can be selected as small as possible according to the restrictions shown above, due to the off switch capacitances of the switches connected to the input nodes of the comparator, the unit capacitor should be chosen as large as possible. The capacitive DAC array consists of many unit capacitors in which their values are not large. For this reason, any off switch capacitance introduce a parasitic capacitance which leads to a wrong voltage division. As a result, wrong decisions can be made in some comparisons. In this work, the unit capacitor is chosen as 620 fF which can decrease the thermal noise at the output of DAC and reduce the effects of the parasitic capacitors.

In the layout, the width and the length of the unit capacitor should be close to each other in order to decrease the effects of the process gradients caused by the layout. The layout of the DAC array is simple and common centroid technique is applied in the layout. Dummy capacitors are added in order to reduce the side effects caused by the process. Figure 3-3 shows the one capacitor array whose height is 500 μm and width is 300 μm.

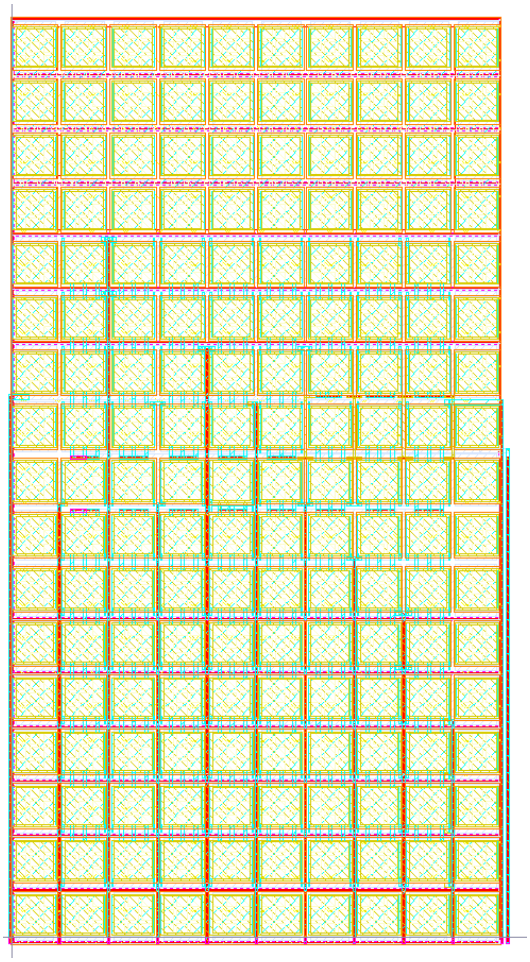

Figure 3-3: One DAC capacitor array whose height is 500 μm and width is 300 μm.

3.2.2 Switches

Switches are important structures for the capacitive DAC array. The switched capacitor DAC array is used for sampling the input signal and providing the necessary voltages in order to perform binary search algorithm. For this reason, many switches are required in order to pass the input signal or reset the voltage at the specific nodes. This section analyses the basic structure of the switches and it discusses the settling time of the DAC array.

3.2.2.1 Switch Structure

In order to decrease the number of switches, a simple structure should be chosen. The switches connected to the bottom plate of the capacitors in the array, passes the input signal, common mode voltage or two different reference voltages. On the other hand, the switches at the node of the top plate of the capacitors reset the voltage at the given node. Figure 3-4 shows the switches and DAC array in the proposed SAR ADC. The bottom plate of the each capacitor is connected to a different switch. Each capacitor can connect to the either input voltage or reset voltage. For this reason, a smart solution should be determined in order to decrease the number of switches.

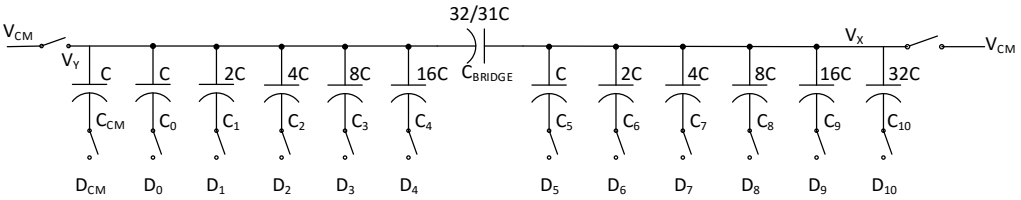

Figure 3-4: Switches and DAC array in the proposed SAR ADC.

In conventional SAR ADCs, the structure of the switches can be divided into two categories which are mux-like switches and shared-like switches. Figure 3-5 shows the mux-like structure for the capacitive array. The proposed structure consists of four different switches which are directly connected to each of the capacitor. As a result, the structure becomes a complex system and too much switches are required which leads to large silicon area. Besides that, the routings of these switches become complex which cause to unwanted parasitic capacitors. The parasitic capacitors can change the value of the capacitor which the voltage division at the input node of the comparator does not work properly. Therefore, mux-like switch cannot be used in this work.

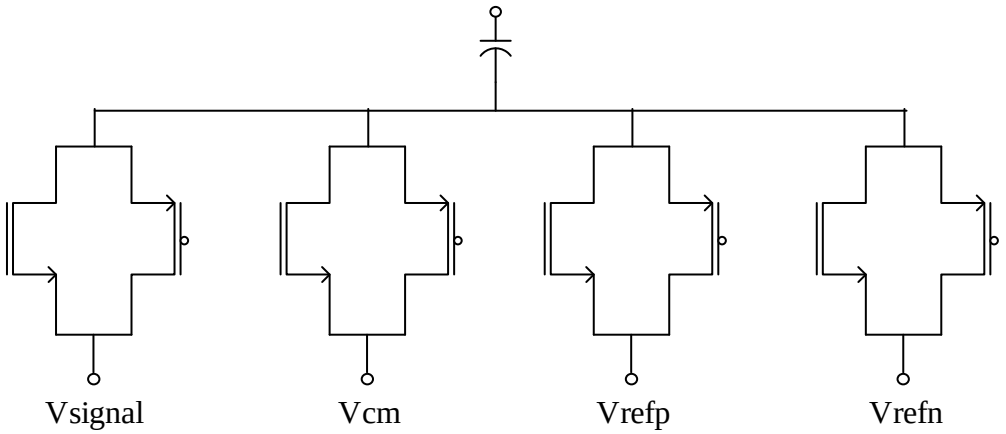

Figure 3-5: Mux-like structure for the capacitive array.

Figure 3-6 shows the shared-like structure for the capacitive DAC array. For each DAC array, there is one input signal switch, V_{CM} switch, V_{REFP} and V_{REFN} switches. Each of the bottom plate of the capacitor is directly connected to just two switches which mean that, the number of the switches is minimized.

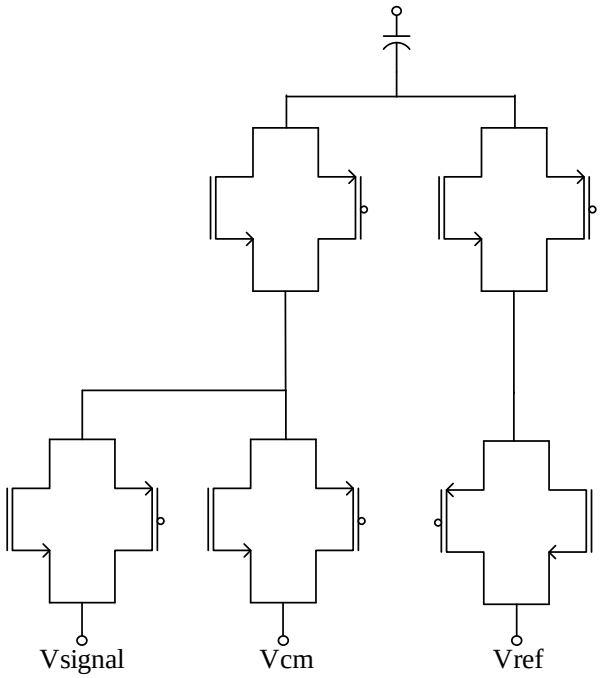

Figure 3-6: Shared-like structure for the capacitive DAC array.

3.2.2.2 Settling Time

The sizes of the switches are determined by considering the settling time of the DAC array. The bottom plates of the capacitors are connected to the transmission gates. Thus, it is useful to study the RC equivalent model of the capacitor array with the transmission gates. The switches have on-resistance can be written as the following:

$$R_{ON} = \frac{1}{C_{OX}\,\mu\left(\frac{W}{L}\right)V_{OV} - V_{DS}} \qquad (3.2.2.2.1)$$

where W and L are the width and length of the transistor. C_{OX} and μ are the process parameters belonging to either pmos or nmos transistor. V_{OV} is the overdrive voltage and V_{DS} is identified as Drain-Source voltage. For each capacitor in the array, the maximum voltage difference between the initial and final state occurs when there is a transition from D_{IN} =0 to D_{IN} = 1024. In this case, the voltage difference equal to the half of the reference voltage. The bottom plate of the MSB capacitor is connected to the reference voltage. On the other hand, the bottom plates of the rest of the capacitors are connected to the common mode voltage. Figure 3-7 shows the RC equivalent model of the DAC array should be analyzed for the situation given above shows the RC equivalent model of the DAC array when D_{IN} = 1024. The switches are represented as resistance, since they introduce resistance when they are ON. The resistance connected to the V_{CM} voltage is comprised of the resistance of the V_{CM} switch and the constant switch connected to the each capacitor. On the other hand, the MSB capacitor has a resistance of the constant switch and the resistance of the V_{REFP} switch.

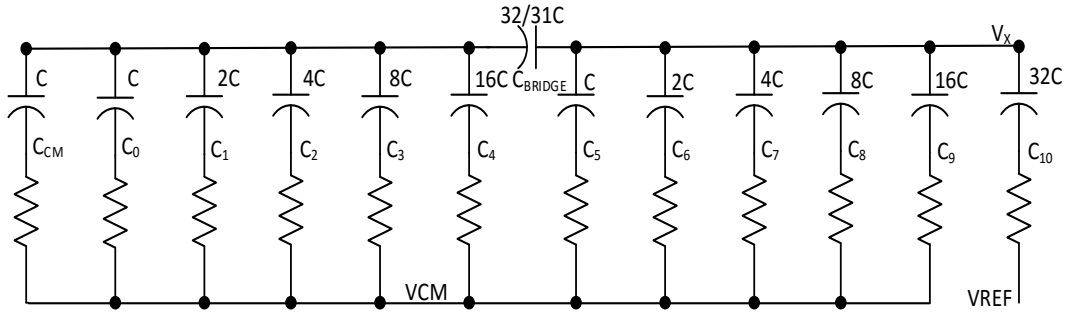

Figure 3-7: RC equivalent model of the DAC array when DIN=1024.

The voltage V_X can be written as the following:

$$V_X(t) = V_{X-INITIAL} + \frac{(V_{REFP} - V_{CM})}{2} - V_{X-INITIAL}\,(1 - e^{-t/\tau}) \qquad (3.2.2.2.2)$$

The time constant τ can be estimated by the following equation:

$$\tau = \left(\frac{R_{Transmission} + R_{VCM}}{10} + 2R_{transmission}\right) 32C \qquad (3.2.2.2.3)$$

In order to settle within 0.5 LSB, the required time should be written in the following equation [24]:

$$t = RC \ln(2^N) \qquad (3.2.2.2.4)$$

where N is the number of bit and it is 12 for this study. Thus, the settling time should be 8.3 RC. Figure 3-8 shows the resistance of the transmission gates over full input voltage range. The resistance reaches the highest value where the input

voltage is approximately 2.35V. At that voltage, the resistance is 420 Ω. The resistance of the switches that passes the common mode voltage is 4.4K at 1.65V.

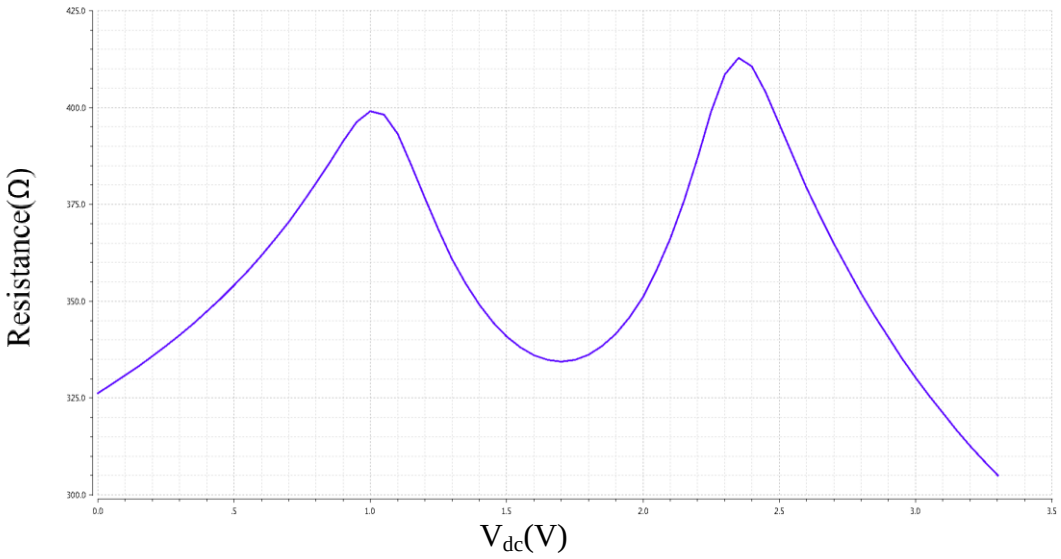

Figure 3-8: Resistance of the transmission gates over full input voltage range.

RC time constant for the MSB capacitor can be described by the following formula:

$$t = 32R_{Equivalent}C\ln(2^N) \approx 217\ \text{ns} \qquad (3.2.2.2.4)$$

Since, the ADC works at 20 KS/s, 217 ns time is sufficient in order to discharge and charge the capacitors. Figure 3-9 shows the layout of the switch array. The height is 90µm and the width is 235 µm.

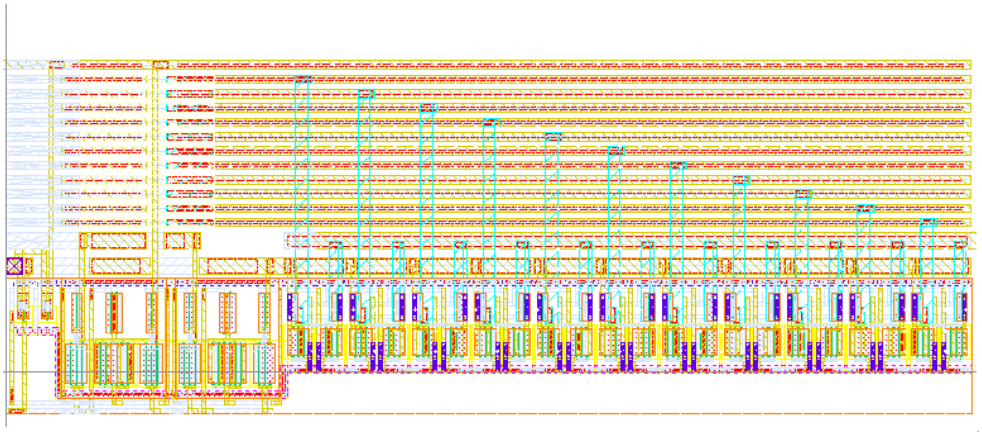

Figure 3-9: Layout of the switch array. The height is 90 µm and the width is 235µm.

3.2.3 Comparator

In conventional SAR ADC, the comparator can be defined as the heart of the ADC structure. Comparators are used to discriminate the small voltage referred as LSB voltage. According to the output voltage of this block, the binary search algortihm can be performed.In analog blocks, most of the power is dissipated on the comparator. Thus, low power structure should be designed. The proposed SAR ADC has a fully differential, and rail to rail comparator. The power voltages are 0V and 3.3V. Thus, the inputs are between 0V and 3.3V. Figure 3-10 shows the architecture of the propsed comparator. The comparator block has four stages. First three stages are fully differential rail to rail amplifier and they are used as gain stages. Normally, the required gain can be obtained from one gain stage. However, in this case, due to the offset voltage of the comparator caused by mismatches, the offset voltage can also be increased which is an undesired situation. For this reason, in conventional SAR ADCs, more than one gain stage is used in order to relax the gain requirements. The fourth stage is comprised of a single stage preamplifier which has a single output, and a buffer are used for establishing full logic levels between power rails. Switches connected to the input of each preamplifier are used for offset cancellation.

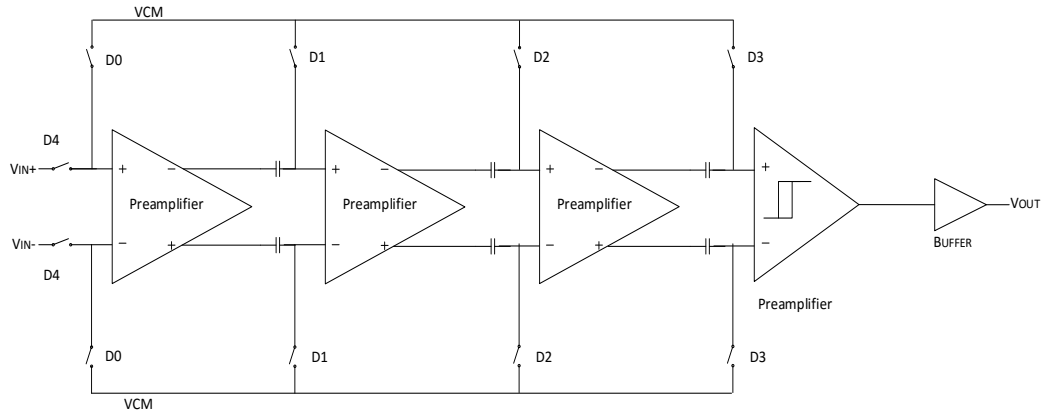

Figure 3-10: Architecture of the proposed comparator.

In the literature, static and dynamic latched comparators are available. The dynamic latch comparators suffer from a high input referred offset voltage. For this reason, in this thesis, static comparator is chosen. Figure 3-11 shows the topology of the preamplifier stage. The proposed preamplifier stage is a rail to rail amplifier with a bias current 500 nA. It consists of two stages. In the first stage, pmos and nmos differential pairs are used. In order to enhance the gain of the amplifier, additional cross coupled transistors M4 and M5 are used. These two cross coupled transistors provide additional gain by a positive feedback.

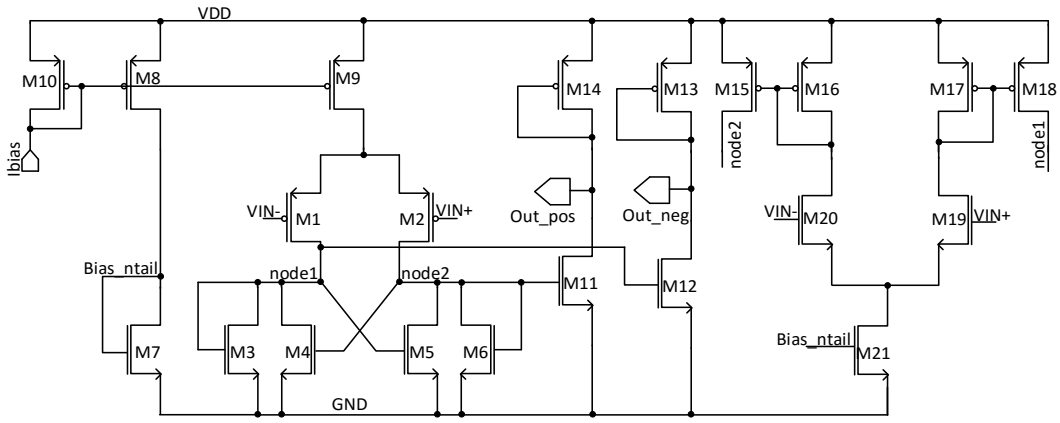

Figure 3-11: Topology of the preamplifier stage.

The positive feedback constant referred as α is described by the following formula:

$$\alpha = (W/L)_5/(W/L)_6 \qquad (3.2.3.1)$$

The positive feedback constant is taken as 0.5 in designed circuit in order to enhance the gain and fasten the decision. In the second stage, the gain is further enhanced by using diode connected transistors which are M13 and M14. Figure 3-12 shows the DC gain of the preamplifier versus input voltage characteristic. The minimum voltage gain level is 22.5 dB when only one differential pair is ON. Both pairs are active when the input voltage is between 0.5V and 2.4V. At this time, the voltage gain is about 25.8 dB. Beyond the 2.4V input voltage, the pmos differential pair starts to turn off and the voltage gain decreases to about 22.5 dB. The comparator provides a sufficient gain over the entire input range which means that it can operate rail to rail. It shows that, after three stage, the LSB voltage becomes sufficiently large to pull the LSB voltage to the one of the power rails by using a single stage amplifier and buffer.

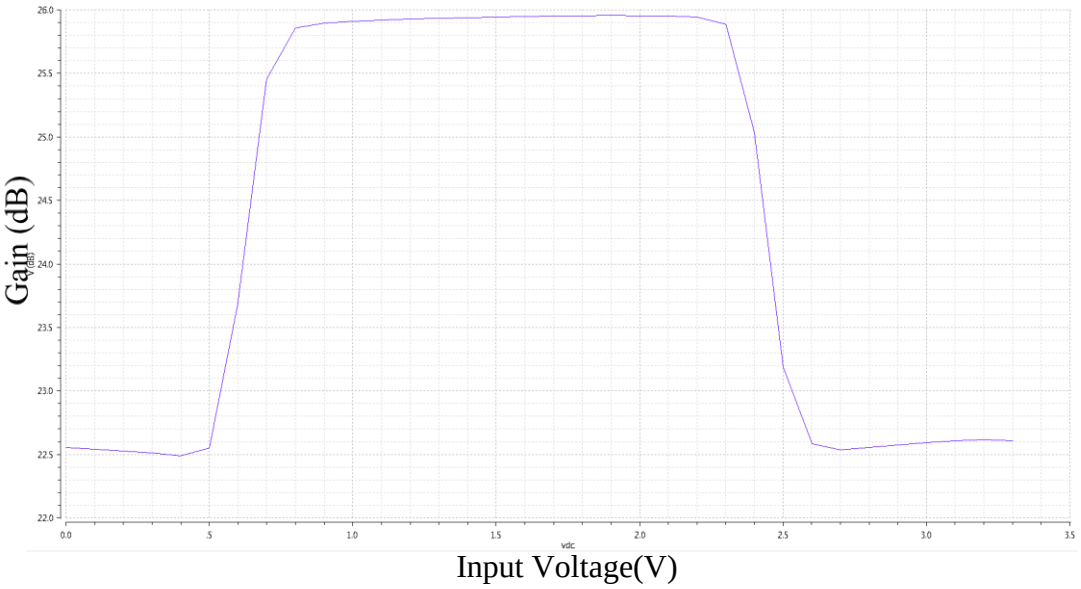

Figure 3-12: The DC gain of the preamplifier versus input voltage characteristic.

The input referred noise of the comparator is an important parameter and it determines the sensitivity of the ADC, since the desired ADC has to discriminate the LSB voltages, and it should be very sensitive. The most important stage for the input referred noise is the first stage,since, the output referred noise of the each stage is divided by the gain of the previous stage. Figure 3-13 shows the input referred noise voltage of the comparator over the input voltage range. When the input voltage is between 0V and 0.5V, the input referred noise is around 24 μV since only pmos input differential stage is turned on. In this range, the noise is mainly dominated by the pmos differential pairs M1 and M2. When the input voltage is beyond the 0.5V, both input differential pairs are turned on. In addition to the noise caused by the pmos differentail pair, the nmos differential pair leads to some flicker noise. As a result, the overall input referred noise increases up to 54 μV. When the input voltage is greater than 2.4V, the pmos input differential stages starts to turns off. Thus, the gain starts to drop and approaches to 22.5 dB which increase the overall noise. The flicker noise caused by the nmos differentail pair dominates the overall noise over the entire input range. Therefore, the input refered noise increases. Around the power rail which is 3.3V, the input referred noise tends to decrease since, the gain increases a little bit in that region. In this comparator structure, the overall noise is dominated by the flicker noise, since the proposed ADC operates at low frequencies. In conventional ADCs, the noise should be less than the half of the LSB voltage ,which implies that, the comparator and DAC array should separately has a noise floor less than the one fourth of the LSB voltage. The maximum input referred noise of the comparator in the designed ADC is 94 μV which is kept below the one fourth of the LSB voltage.

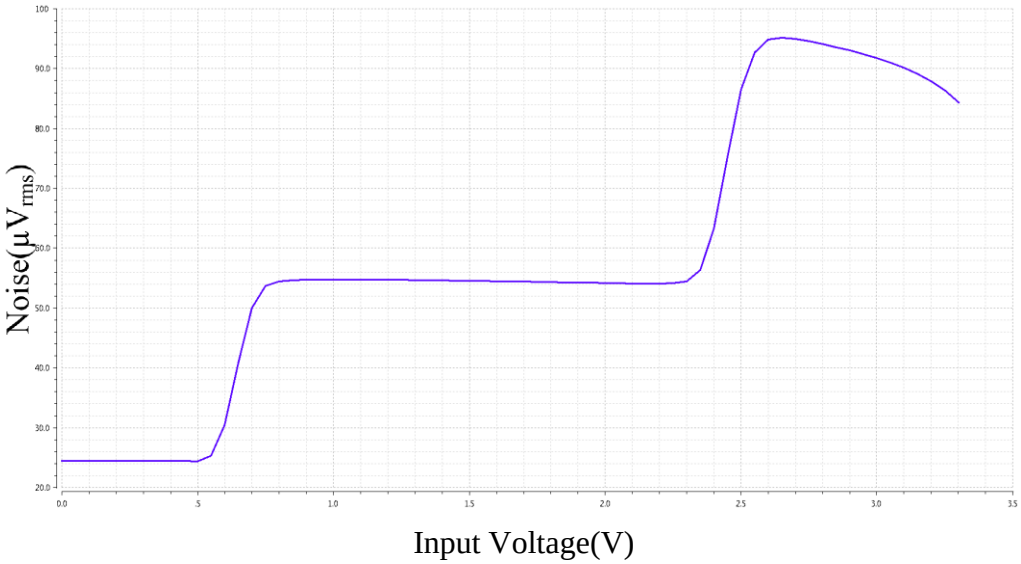

Figure 3-13: The input referred noise voltage of the comparator over the input voltage.

Figure 3-14 shows the layout of a single stage amplifier. The height is 300 μm and the width is 35 μm. The layout is drawn vertically in order to minimize the horizontal width. In order to reduce the mismatches arises from the process variations and layout issues; the layout is comprised of two symmetrical parts.

Figure 3-14: Layout of the single preamplifier. The height is 300 µm and the width is 35 µm.

After three gain stages, there is one more stage which can be called as output stage. In this stage, there is a single stage amplifier and a buffer. Figure 3-15 shows the schematic diagram of the output stage amplifier. The structure of the output stage amplifier resembles to the previous gain amplifiers. It consists of additional transistors. The I_B current is provided by current mirror transistors. In this stage, the outputs of the gain stage are converted to either logic zero or logic one. M10 and M7 transistors are used to convert the differential amplifier into single stage amplifier. Cross coupled transistors M5 and M6 provide additional gains to the overall system.

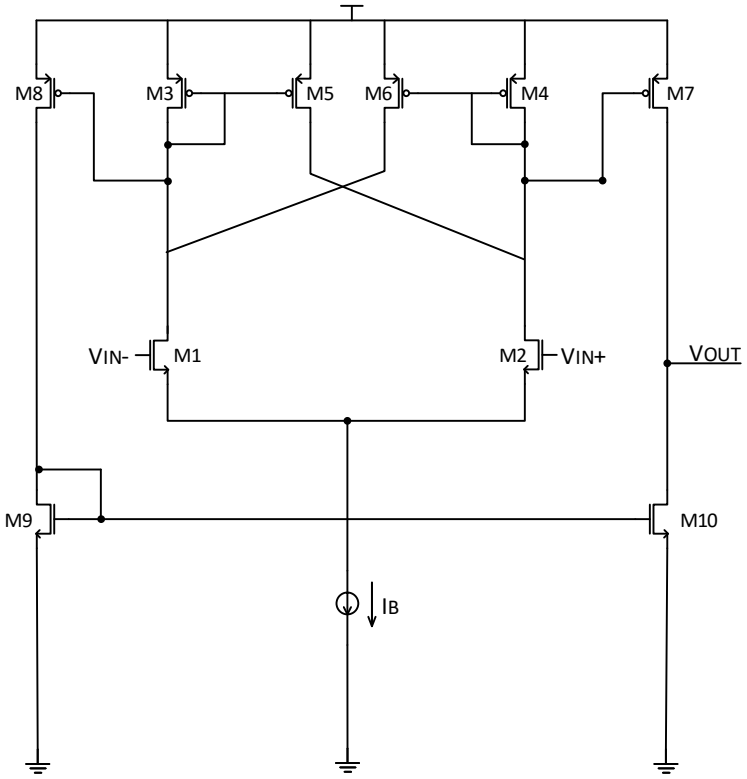

Figure 3-15: Schematic diagram of the output stage amplifier.

Figure 3-16 shows the output response of the output stage amplifier. Blue signal is the positive signal which is a sine wave. The input voltage is a sin wave with a frequency 10 KHz, amplitude 1.65V, and a 1.65V DC voltage. Thus, it can swing from 0V to 3.3V. The negative input of the amplifier is constant at 1.65V. When

the input voltage is greater than 1.65V, the output is pulled up to 3.3V. On the other hand, when the input voltage is less than 1.65V, the output is pulled down to 0V. Thus, after three gain stages, the output stage amplifier can pull up to 3.3V or pull down to 0V the input voltages. The output of the amplifier is connected to a simple buffer.

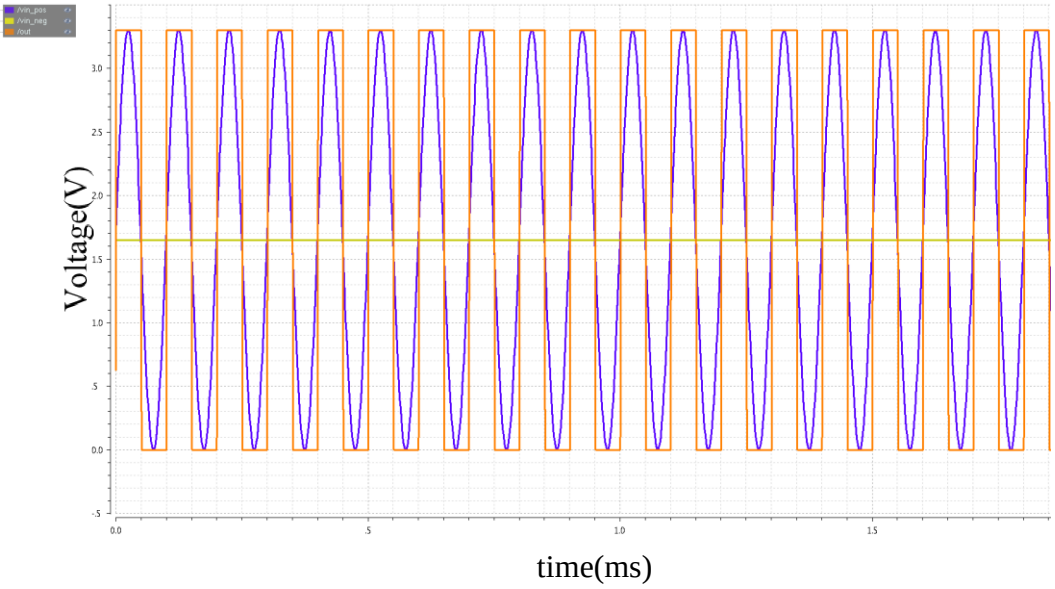

Figure 3-16: Output response of the output stage amplifier. Blue signal is the positive signal which is a sine wave.

Figure 3-17 shows the layout of the output stage amplifier. The height is 330 µm and the width is 25 µm Output stage amplifier. The height is 330 µm and the width is 25 µm. The output stage amplifier is drawn vertically in order to minimize the horizontal width. The layout is comprised of two identical parts which minimize the mismatches arises from the mismatches and layout issues.

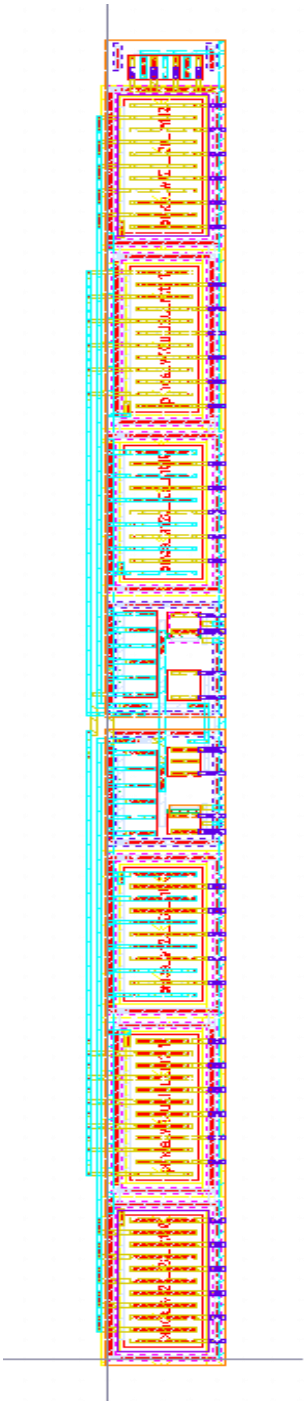

Figure 3-17: Layout of the output stage amplifier. The height is 330 µm and the width is 25 µm Output stage amplifier.

In conventional comparators, due to the mismatches arises from the process variations, offset voltage can be seen which is not good for high precise ADCs. The standard deviation of the offset voltage can be described by the following formula:

$$\sigma^2(V_{OS}) = \sigma^2(\Delta V_T) + \sigma^2\left(\frac{\Delta\beta}{\beta}\right)\left(\frac{I_D}{gm}\right)^2 \quad (3.2.3.2)$$

which is dependent to the transistor parameters. In general, the offset voltage is in the order of micro volt. However, after three gain stages, it becomes a significant voltage and can affect the result of the comparison. In order to minimize this voltage, some offset voltage cancellation techniques can be used. In literature, there are several approaches which are using large devices, trimming or input/output offset cancellation techniques. Using large devices and trimming is not suit for the proposed ADC structure. Input offset cancellation requires high gain and large capacitance which limits the charge injection error. Thus, in this work, output offset cancellation technique is used. The output offset cancellation operates as follows: At the beginning of the each cycle, the inputs and outputs of the preamplifiers are shorted. A common mode voltage is applied to these nodes. It means that, the offset voltage can be stored on the capacitors connected to the output of the amplifiers. In the comparison phase, the offset voltage is subtracted from the output voltage of the preamplifiers. Therefore, the effect of the comparator is minimized for each clock cycle. The architecture of the comparator shown in Figure 3-10, includes switches which are labeled as D0, D1, D2 and D3.D4 is the input switch which is composed of a transmission gate. These switches are built from single nmos transistors with dummy transistors in order to minimize the charge injection. These switches are turned off during the comparison phase, and at the beginning of the each clock cycle, the transistors are ON and these nodes are connected to common mode voltage. Thus, the output

offset cancellation is performed. Figure 3-18 shows the timing scheme from the proposed cancellation scheme. The timing signals are generated from one signal generated which is generated in the digital controller. During the offset cancellation, first the input switch is closed by using the Phi4 signal. Other switches are opened by using the remaining signals. After the offset cancellation phase, the input switches are opened and the remaining switches are closed. At this time, in order to minimize the charge injection from the closed switches dummy transistors are ON in the comparison phase.

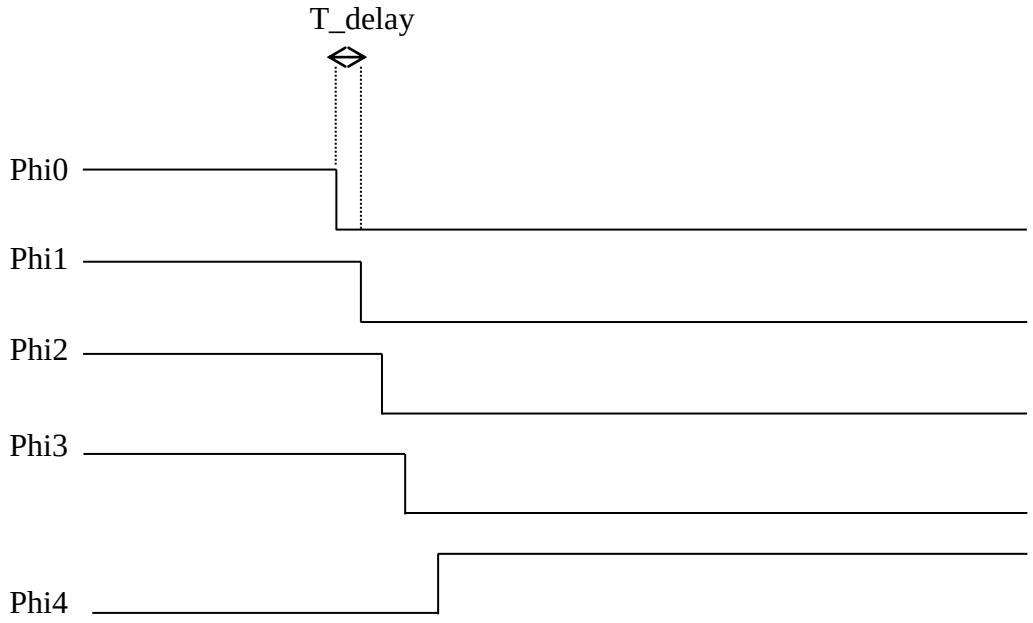

Figure 3-18: Timing scheme for the proposed cancellation technique.

The generated five signals can have time delay with respect to each other and this delay can be adjusted by the delay elements. Figure 3-19 shows the simple structure of a delay element. It is comprised of simple inverters. The amount of the delay is in the order of nanoseconds which is sufficient for creating the timing signals. The delay is an option. In the offset cancellation block, all signals can be generated without any delay by programming the multiplexers used in the offset cancellation block.

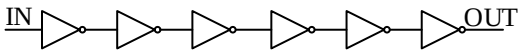

Figure 3-19: Simple structure of a delay element.

Figure 3-20 shows the layout of the offset cancellation block. . The height is 185 µm and the width is 230 µm. The block is surrounded by a guarding which is used for preventing any latch up.

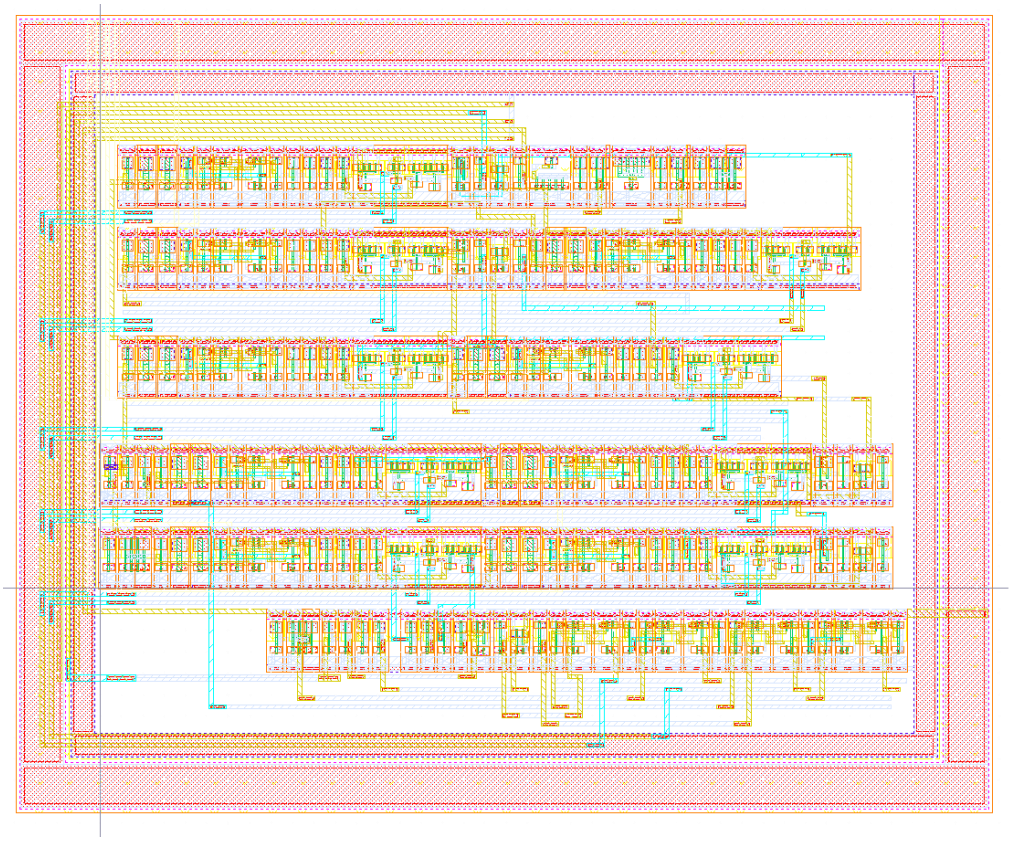

Figure 3-20: Layout of the offset cancellation block. The height is 185 µm and the width is 230 µm.

The power consumption of the comparator is 116.16 µW. The minimum voltage discriminated by comparator is 1.61 mV which is called as LSB voltage. At this differential voltage, 800ns is required in order to make a decision. The comparison time depends on the input voltage difference. If it is large enough, the decision time can be even smaller.

Figure 3-21 shows the top layout of the comparator. 450 µm and the width is 190 µm. In order to reduce the delay caused by the routings, the offset cancellation block is located near the comparator. Thus, the delay caused by routings can be minimized.

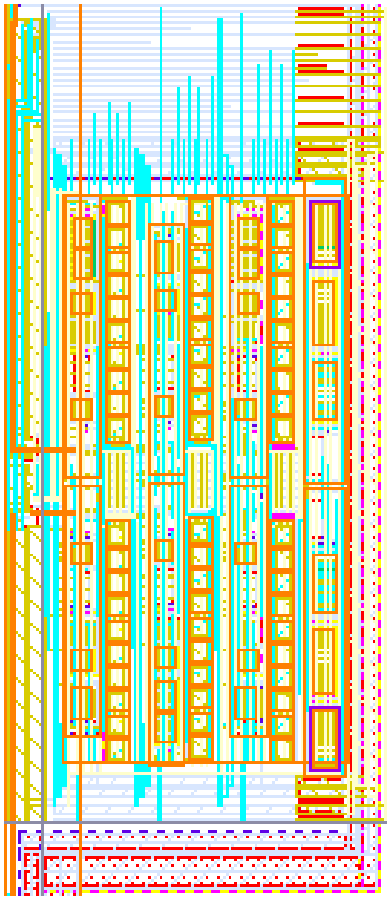

Figure 3-21: Top layout of the comparator. The height is 450 µm and the width is 190 µm.

Figure 3-22 shows the top level simulation of the comparator. Positive input signal is the blue signal while the yellow signal is the negative input signal. The positive input signal is a sine wave with a frequency 10 KHz. The amplitude of the signal is 1.65V and the DC voltage is 1.65V. Thus, it can cover the whole input range. The negative input signal referred as V_{OFF} is the inverse of the positive input signal. When the positive input signal is greater than the negative one, the output is logic one. On the contrary, if the negative input signal is greater than the positive one, the output is logic zero.

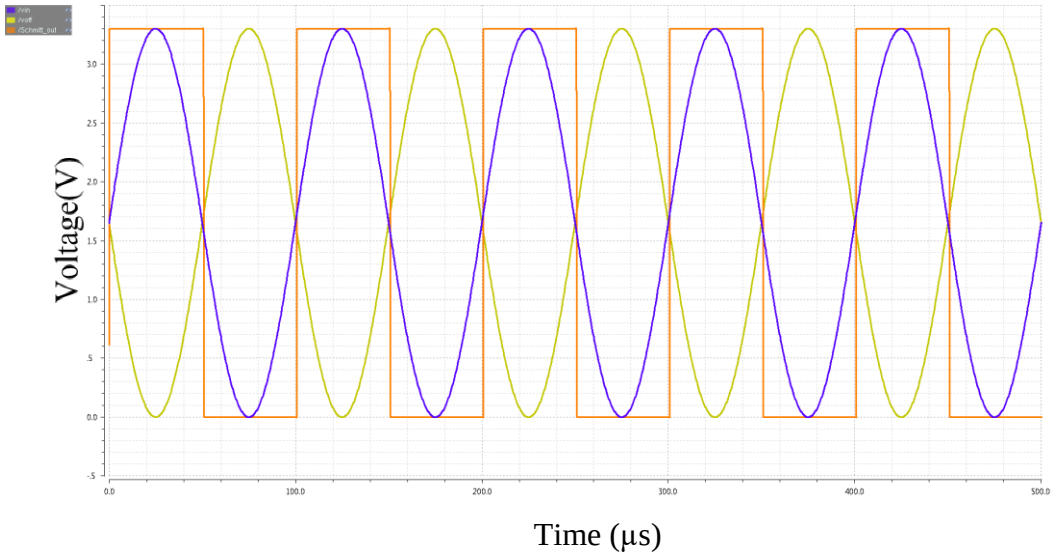

Figure 3-22: Top level simulation of the comparator. Positive input signal is the blue signal while the yellow signal is the reverse one.

3.2.4 Bias Generator

The bias block generates the required bias currents and voltage to the comparator. In many mixed analog/digital systems, due to the supply noise, temperature and changes in the voltage, the performance of the devices is seriously degraded [25]. For this reason, a reasonable supply and temperature independent bias generator is required. In this thesis, the bias generator is comprised of a bandgap voltage generation block, a reference current generation block and four current DACs. The proposed bandgap is a supply and temperature independent block. The reference circuit is used for generation a reference voltage around 1.2V which is the bandgap energy of the silicon. In the literature, the main components of the bandgap circuits are the negative temperature coefficient base-emitter voltage of BJT and the positive temperature coefficient voltage. In order to generate a temperature independent voltage, positive and negative coefficient voltages are summed up with the right coefficients. The positive coefficient voltage can be generated from the current which is proportional to absolute temperature and a resistor. Figure 3-23 shows the proposed bandgap reference circuit [26]. The currents flows through three branches are same. These currents are proportional to absolute temperature. The multiplier factor of the BJT called as N and the resistor R1 determine the absolute temperature referred as PTAT.

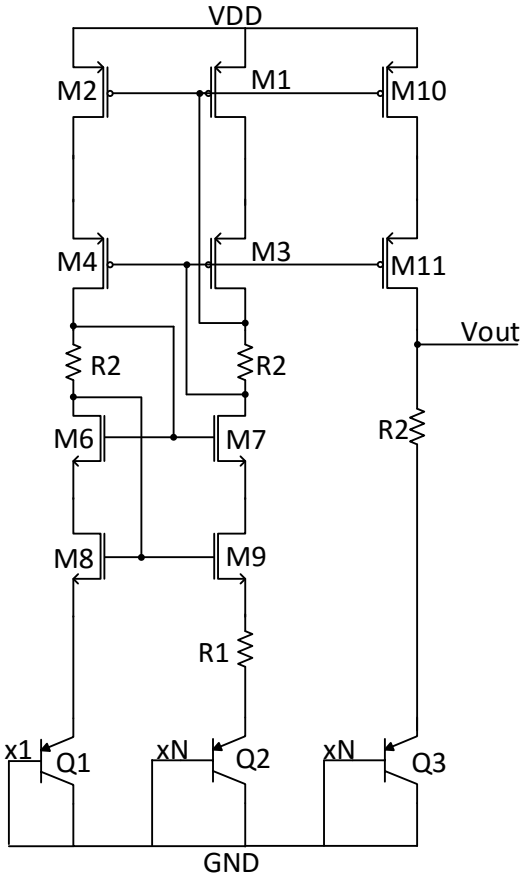

Figure 3-23: Proposed bandgap reference generation circuit [26].

The current flow through each branch can be written in the following equation [26]:

$$I_{Branch} = \frac{V_t lnN}{R_1} \tag{3.2.4.1}$$

where V_t is described as thermal voltage, R1 is a resistor, N is the BJT multiplier and I_{branch} is current which flows through each branch. Then, the output voltage can be calculated from the following formula:

$$V_{Out} = V_{BE} + V_t lnN \frac{R2}{R1} \quad (3.2.4.2)$$

The output voltage of the bandgap reference is a function of the base-emitter voltage, thermal voltage, the ratio of the R2 and R1 and the BJT multiplier. When the derivative of the equation 3.2.4.2 is taken with respect to temperature, the derivative of the base-emitter voltage results a negative voltage. On the other hand, the derivative of the thermal voltage brings a positive voltage. As a result, by choosing the proper value of the R1, R2 and BJT multiplier, a temperature independent voltage which is around 1.21V can be generated. In this thesis, the value of the bandgap voltage is 1.22V. As an option, the external bandgap voltage can be used. The bandgap voltage is used for generating a reference current. The reference current is 2 µA and it is the input of the current DACs. In this work, four current DAC are used. Three of them generate the bias currents of the preamplifiers in the comparator and one of them is used for the output stage amplifier. The current DACs are composed of simple current mirrors, capacitors for minimizing the noise and switches. By using the switches, the current DACs can be programmed via digital controller with 4 bit selection. In the bias generator, two different type of current DAC is available. For the preamplifier, the current DAC has a range of 250nA and 3.75uA with 250nA steps and for the output stage amplifier; the range of the current DAC is 1 µA and 15 µA with 1 µA steps.

3.3 Digital Blocks

This section clarifies the realization of the digital controller in detail. The digital controller generates the required timing signals for the operation of the SAR ADC. Besides that, the bias generator is controlled by the digital controller since the bias currents are adjustable. The digital controller consists of five main blocks

which are successive approximation register, output serializer, timing generator, serial programming interface, and memory. Figure 3-24 shows the block diagram of the digital controller. Serial Programming Interface communicates with external electronics such as FPGA. Successive approximation register provides the necessary control signals to the DAC and generates the output bits. The timing block generates the required timing signals for the digital blocks and analog blocks. Digital memory keeps the static signals for the digital blocks and analog blocks. In the next sections, the each block is analyzed in detail.

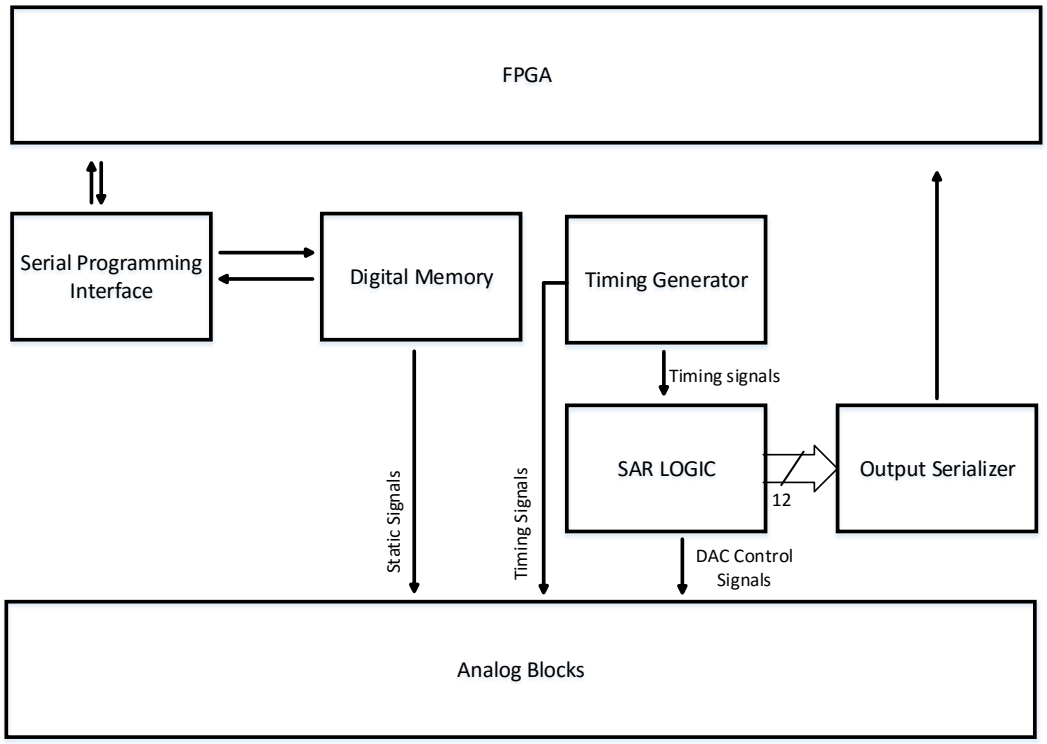

Figure 3-24: Block diagram of the digital controller.

3.3.1 Serial Programming Interface

The serial programming interface which is synchronous is used for the communication with the external electronics such as FPGA. It is comprised of four wires for communication which are serial data input, serial clock, active low enable signal and serial data output. The length of the serial input is 18 bit. 16 bits are reserved for input data and 2 bits are for address. Figure 3-25 shows the serial programming interface register for the proposed SAR ADC. The external electronics such as FPGA has to send the input data to serial programming interface (SPI) from low significant bit (LSB) to most significant bit (MSB). The SPI samples the serial data at each rising edge of the clock. It means that, the external electronics has to write or read the data at the falling edge of the clock

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
address<1:0>		data<15:0>															

Figure 3-25: Serial programming interface register for the proposed SAR ADC.

Figure 3-26 shows the timing diagram of the serial programming interface. For each 18 bit word, the communication lasts 18 clock cycles. During this period, the active low signal remains low. After 18 clock cycles, the active low enable signal goes high and SPI does not write the serial data into its registers. After 18 bit cycle, the 16 bit data is written to corresponding address. The serial output wire provides to read the previous written data on the SPI. Thus, the previous data can be read from this port.

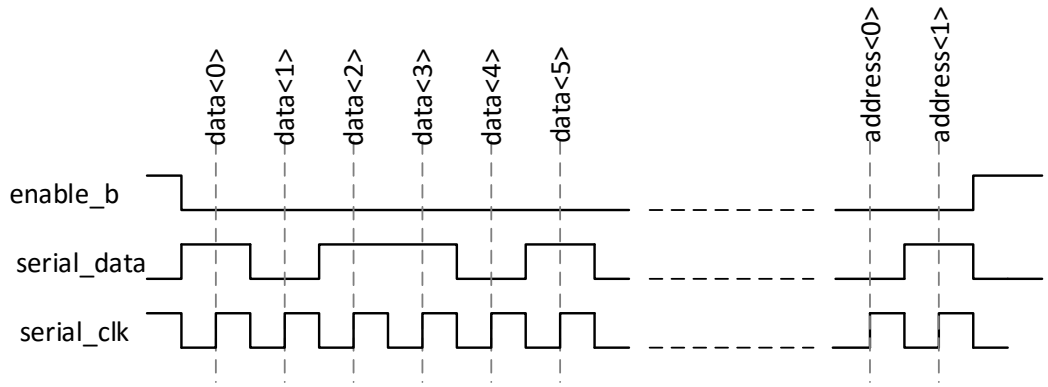

Figure 3-26: Timing diagram of the serial programming interface.

3.3.2 Digital Memory

The digital memory consists of 16-bit words. After 18 clock cycle, the write pulse for the memory is generated and the serial input data is written to the memory according to the given address. The digital memory is simply comprised of registers and 48 bit registers are used in this design and it stores the required static signals for the digital blocks or analog blocks such as bias generator and comparator.

3.3.3 Timing Generator

Timing block is the main part of the digital controller. It generates the required digital timing signals for the digital and analog blocks. The system operates at 20 KS/s. For each comparison of the differential voltage, 16 clock cycles is required. Thus, the system clock is 320 KHz. Table 3-1 shows the definition of each function at each cycle. In order to generate the required signals, a 4 bit counter is used. In the 0^{th} state, the input voltage is sampled on the capacitive DAC array. Meanwhile, the outputs of the SAR logic are reset in order to ensure that, all the registers are cleaned. In the sampling phase, the bottom plates of the capacitors

are connected to the input signal while the top plates of the capacitors are connected to the common mode voltage.

Then, in the next cycle which is the first state, the sampled signal is held on the capacitor and the input signal is transferred to the input nodes of the comparator by connecting the bottom plates of the capacitors to the common mode voltage. In this case, the top plates of the capacitors are being float which provides to transfer the input voltage to the input nodes of the capacitor array. After first two clock cycle, the conversion starts. Firstly, the MSB sign bit is determined. From the third state, the offset cancellation signal is generated in order to minimize the effects of the offset voltage of the comparator caused by mismatches. After twelve clock cycle, all the bits are determined and the end flag is created for loading the 12 bit data into the serializer. The last clock cycle is reserved for the output serializer, since the serial data is adjusted to LSB after two clock cycle.

Table 3-1: Definition of each function at each cycle

State	Definition of the function
0	Initial State Sample,reset SAR logic
1	Hold state
2	Conversion starts. MSB bit is determined
3	bit 10 is determined
4	bit 9 is determined
5	bit 8 is determined
6	bit 7 is determined
7	bit 6 is determined
8	bit 5 is determined
9	bit 4 is determined
10	bit 3 is determined
11	bit 2 is determined
12	bit 1 is determined
13	bit 0 is determined
14	load serializer
15	adjust the serial data output

Figure 3-27 shows the required timing signals for the operation of the SAR ADC. Sampling_en and samplingb_en are the signals that initialize the sampling phase. After that cycle, hold phase is performed. The sampled input voltage is transferred to the input node of the comparator. In the third cycle, the conversion is started by determining the MSB bit. According to this bit, the reference voltages are adjusted to either 3.3V or 0V. The offset cancellation signal is used to perform the offset cancellation. After the conversion ends, the load signal is generated. The last cycle is reserved for the output serializer. The data is ready after two clocks of the load signal. It means that, in order to set the LSB bit in the output serializer at the beginning of the next comparison cycle, a dummy clock cycle is used.

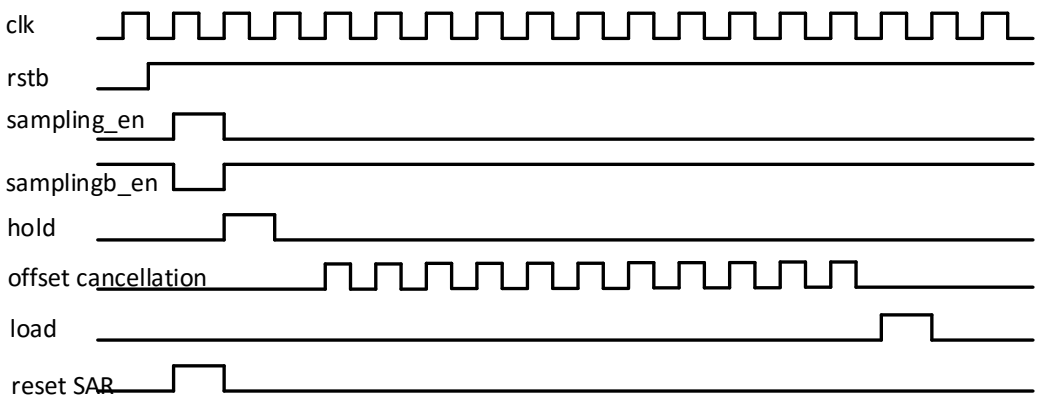

Figure 3-27: Required timing signals for the operation of the SAR ADC.

3.3.4 Successive Approximation Register (SAR)

Successive approximation register known as SAR is the basic block of SAR ADC that performs the binary search algorithm. According to the output of the comparison, the voltage is either increased or decreased by the capacitive DAC array. In literature, some popular approaches are introduced [27], however, in this thesis, the designed structure is based on the proposed structure given in [28]. Figure 3-28 shows the structure of the SAR logic in the proposed SAR ADC. The structure consists of two rows of the registers with SET and RESET. When the conversion starts, the related starting signal is generated. Then the first register in the top row is set. It means that the output of this register is adjusted to one. As a result, the first register in the bottom row is set to one. In other words, bit10 is set to one. According to this bit, the capacitor array adjusts the appropriate voltage and comparison is performed. If the result of the comparison one, then the output does not change, and it keeps its value until a reset signal is generated. On the contrary, if the comparison result is zero, the output voltage is set to zero. Then bit9 is set to one, and the capacitor array changes the voltages according to new inputs. A comparison is performed and according to the output, bit9 is determined. The rest of the bits are determined in the same way. At the end of the conversion, the end flag is generated which is used for loading the 12 bit data into the output serializer. The MSB bit is determined in a different register. At the beginning of the conversion, the sampled voltages are compared. In the meantime, the capacitors do not distribute the charge. In order to test the SAR logic independently, a test input can be directly applied to the SAR logic.

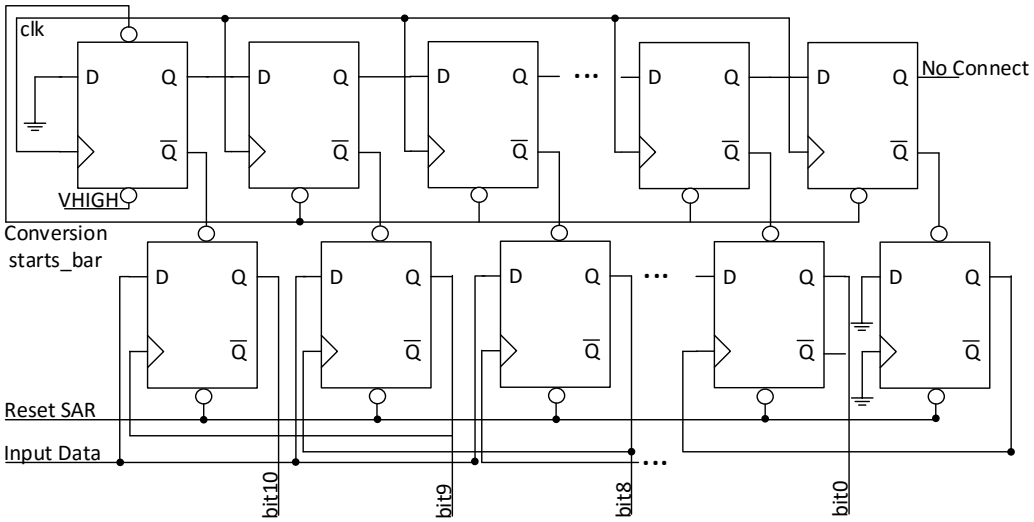

Figure 3-28: Structure of the SAR logic in the proposed ADC.

3.3.5 Output Serializer

The output serializer is used in order to reduce the number of pads. For this reason, the data is serially sent to the external electronic. Output serializer is comprised of two identical registers. At the end of the conversion, the load signal is generated. The 12-bit data are loaded into the first register in the output serializer in parallel. Then the registers start to shift the data to right. The output serializer first sends the LSB bit. The shift operation is performed at the rising edge of each clock. The shift operation is ended when the secondary register is reset. In order to understand the beginning and the end of the data a second signal called as serial latch is generated. When this signal is high, the data is available. As a result, the serial data can be sampled at the falling edge of the clock in the external electronics. Figure 3-29 shows the layout of the digital controller. The height is 1190 μm and the width is 930 μm.

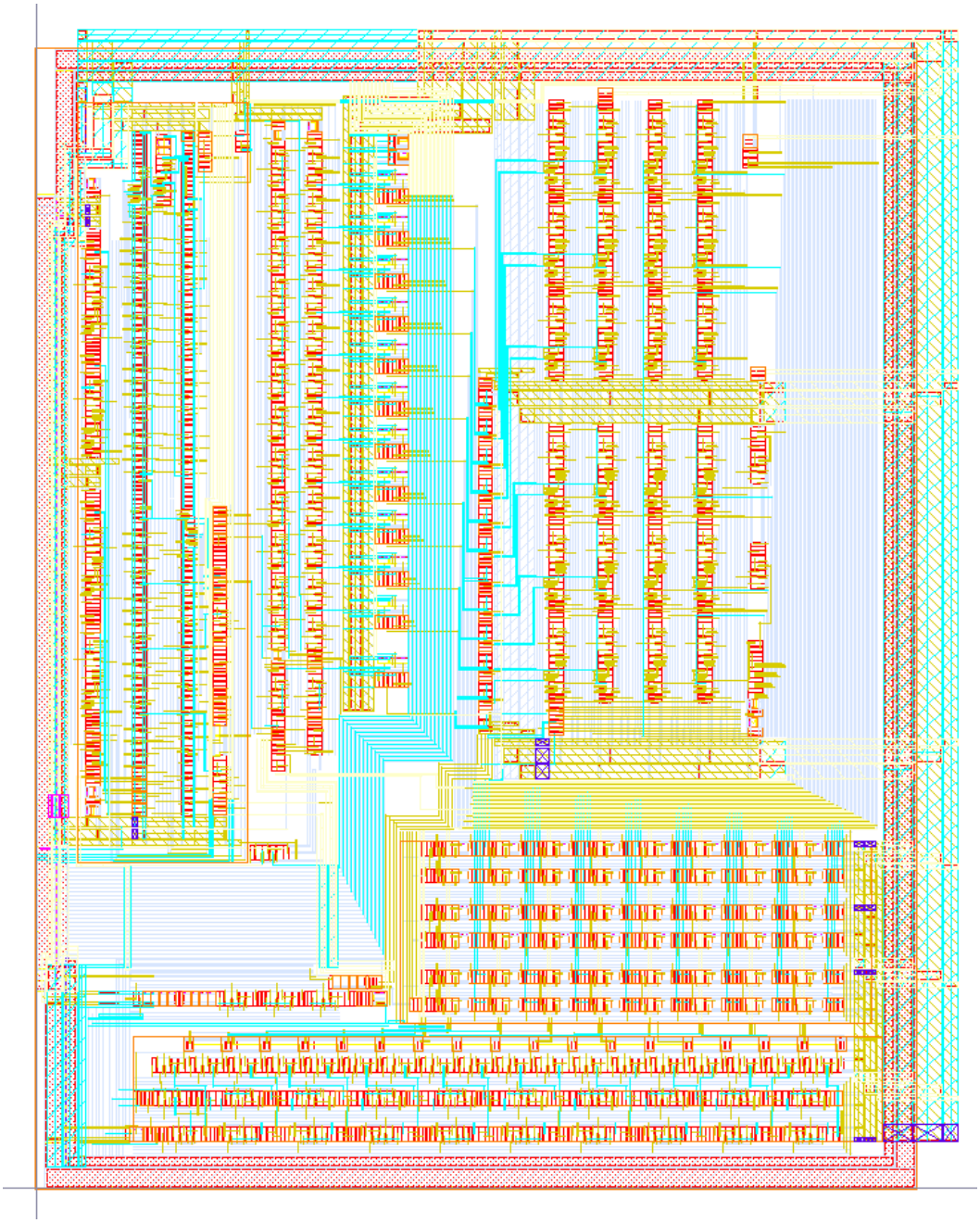

Figure 3-29: Layout of the digital controller. The height is 1190 µm and the width is 930 µm.

3.4 Top level integration

The top level of the designed chip consists of analog and digital circuits. Figure 3-30 shows the floor plan of the top layout. The left side of the chip is reserved for the analog inputs. For this reason, the capacitive array and the switches are located at the left side of the chip. The top pads are reserved for analog supplies and grounds. Thus, the bias generator is placed at the top of the chip. The right side and the bottom right side are reserved for digital powers and digital signals. The chip measures 2000µm x 2000µm in 0.35 µm CMOS technology.

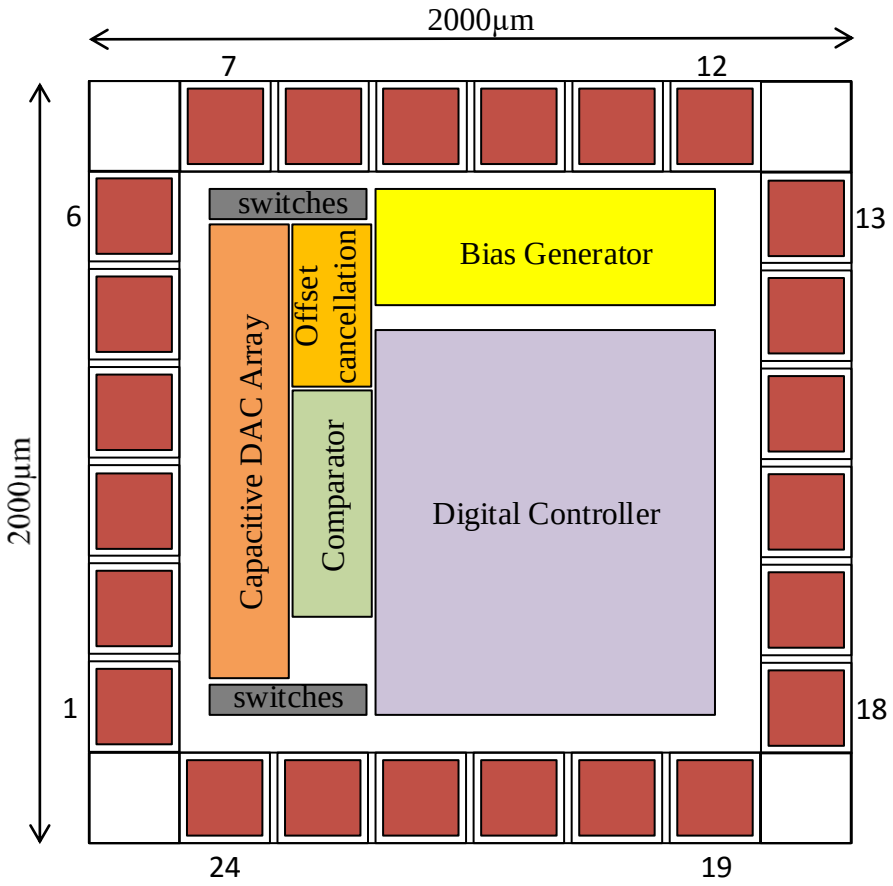

Figure 3-30: Floor plan of the top layout.

It consists of 24 pads. Table 3-2 shows the pad list of the SAR ADC. The analog supplies include the analog bias voltages for the analog blocks, common mode

voltage and reference voltages for the capacitive DAC array. The digital input signals are located at the bottom side of the chip. The SPI block is placed at the bottom of the chip. Thus, the routings are minimized. The outputs of the SAR ADC are at the right side of the chip. The serializer is also placed at that location. As a result, the routings of these signals are also minimized. Therefore, the parasitic capacitors and resistors due to the routings are reduced. At the digital output of the chips, digital output buffers are placed in order drive the load caused by the PCB and external electronics.

Table 3-2: Pad list of the SAR ADC

Pad No	***Pad Name***	***Pad No***	***Pad Name***
1	Pad Ground	13	Serial_dataout
2	Pad Supply	14	sdout
3	Vin_positive	15	Serial_latchout
4	Vin_negative	16	Digital Supply
5	ESD Ground	17	Digital Ground
6	ESD Supply	18	Digital Ground
7	Analog Supply	19	s_latch
8	Analog Supply	20	sdin
9	Analog Supply	21	sys_clk
10	Analog Ground	22	rstb
11	Analog Ground	23	Analog Supply
12	Analog Supply	24	Analog Supply

Figure 3-31 shows the top layout of the chip. The height is 2000µm and the width is 2000µm in 0.35 µm CMOS technology. Each block is marked on the figure. The chip was sent to foundry for fabrication. The layout of the chip is drawn according to the given floor plan of the chip.

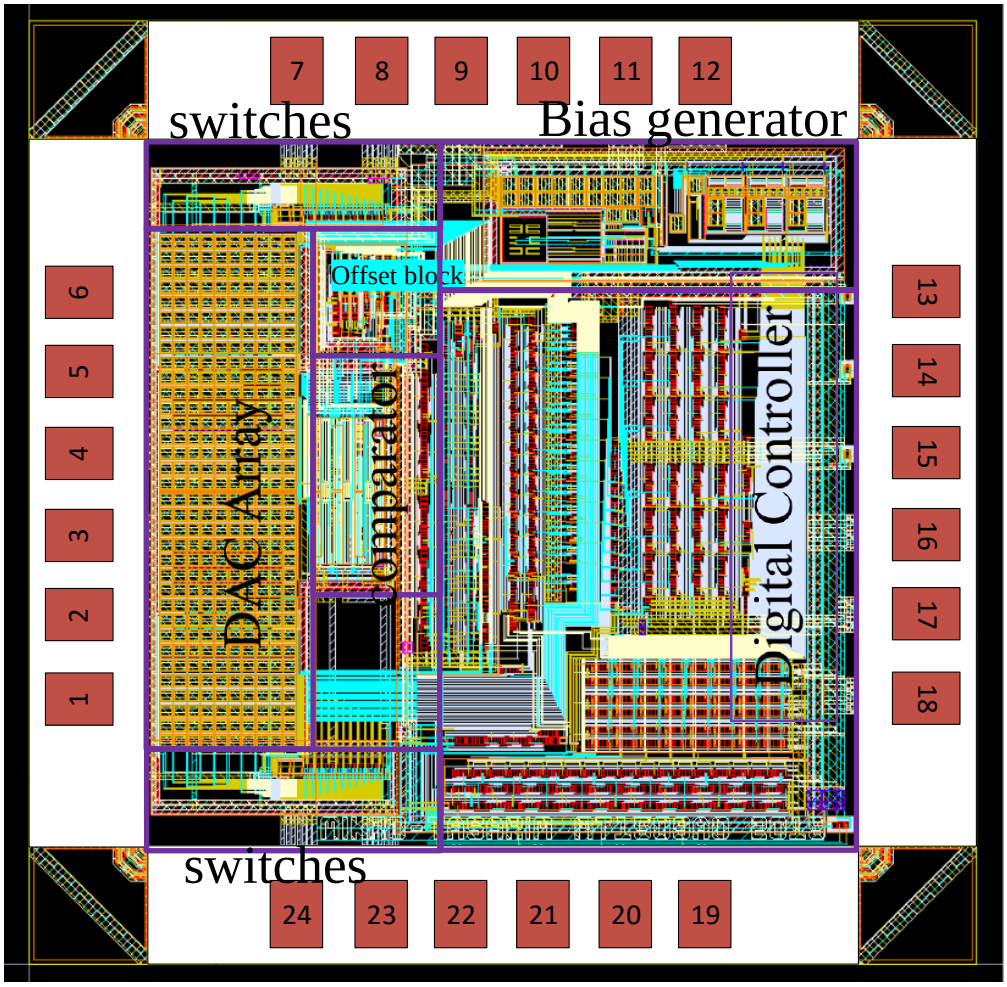

Figure 3-31: Top Layout of the chip. The height is 2000µm and the width is 2000µm in 0.35 µm CMOS technology. Each block is marked. The chip was sent to foundry for fabrication.

3.5 Top level Simulations

The top level simulations are important in order to verify the operation of the SAR ADC. The designed SAR ADC is a fully differential rail to rail with 3.3V supply voltage. It means that, the input differential voltage can be either +3.3V or -3.3V. For this reason, the MSB bit is a sign bit. When the MSB bit is zero, it means that a positive voltage is converted. On the contrary, if the input voltage is negative, the MSB bit is one. In the top level verifications, the full input range is simulated in order to ensure that, the SAR ADC covers the whole input range. Figure 3-32 shows the output voltages of the capacitive DAC array when the differential voltage equals to 3.3V. Due to the fact that, the full range voltage is converted, the expected digital output should be “011111111111”. Two full conversion cycles is presented. The MSB is zero, since positive differential voltage is applied to the comparator.

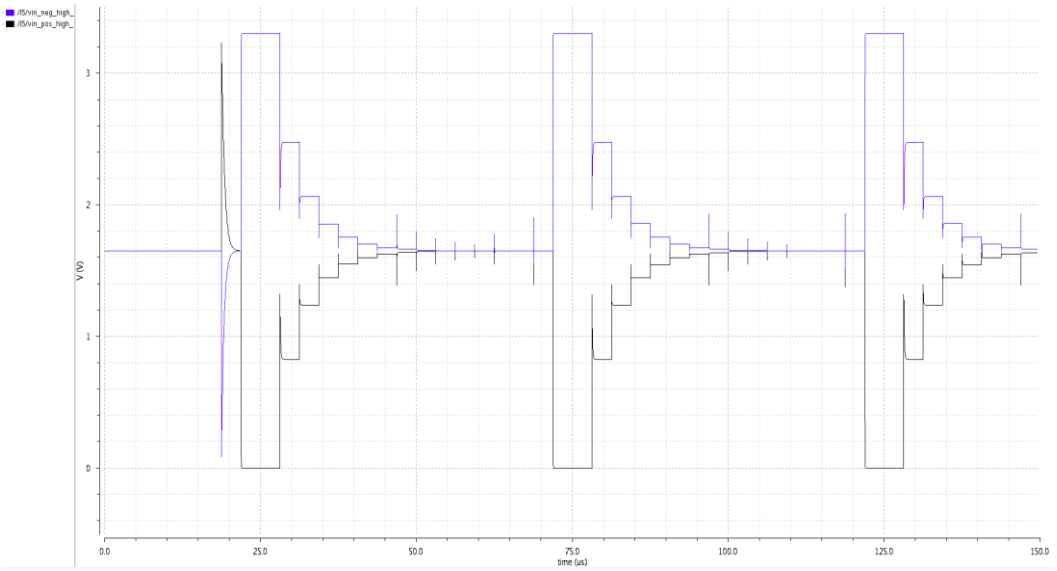

Figure 3-32: Output voltages of the capacitive DAC array when the differential voltage equals to +3.3V

Figure 3-33 shows the 12-bit digital outputs when the differential voltage equals to +3.3V. The MSB bit called as SAR_out<11> is zero and all the rest of the bits equal to one as expected.

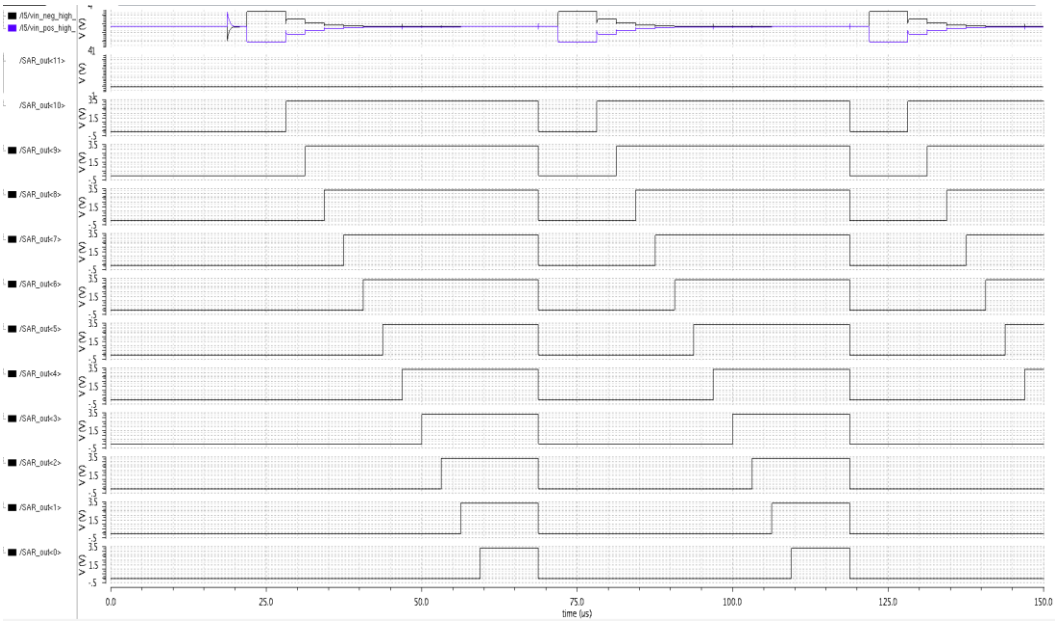

Figure 3-33: 12-bit digital outputs when the differential voltage equals to +3.3V.

Figure 3-34 shows the serial output of the conversion with serial latch, clock and the output voltages of the capacitive DAC array respectively. The serial data is available when the serial latch goes to high. The first bit is the LSB bit is which is sent to external electronics. For this reason, the last bit of the serial data is zero which represents the MSB bit. The output serializer operates while the second conversion is performed.

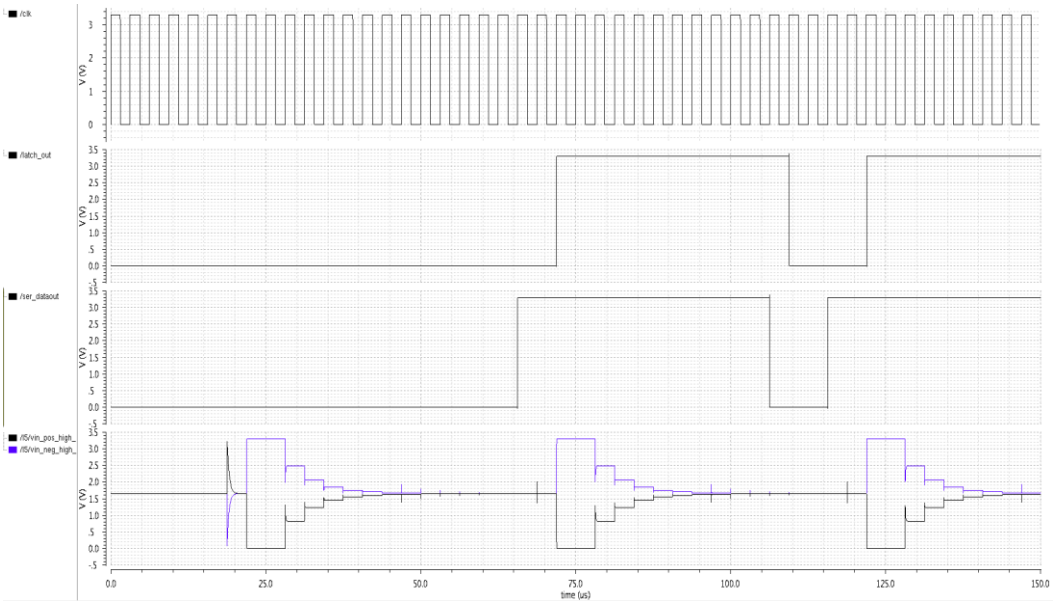

Figure 3-34: The serial output of the conversion with serial latch, clock and the output voltages of the capacitive DAC array respectively.

Figure 3-35 shows the output voltages of the capacitive array when the differential voltage equals to +1.65V and Figure 3-36 shows the serial output with latch signal when the differential voltage equals to +1.65V. The expected digital output of the conversion is “010000000000” which can be seen from the simulation results.

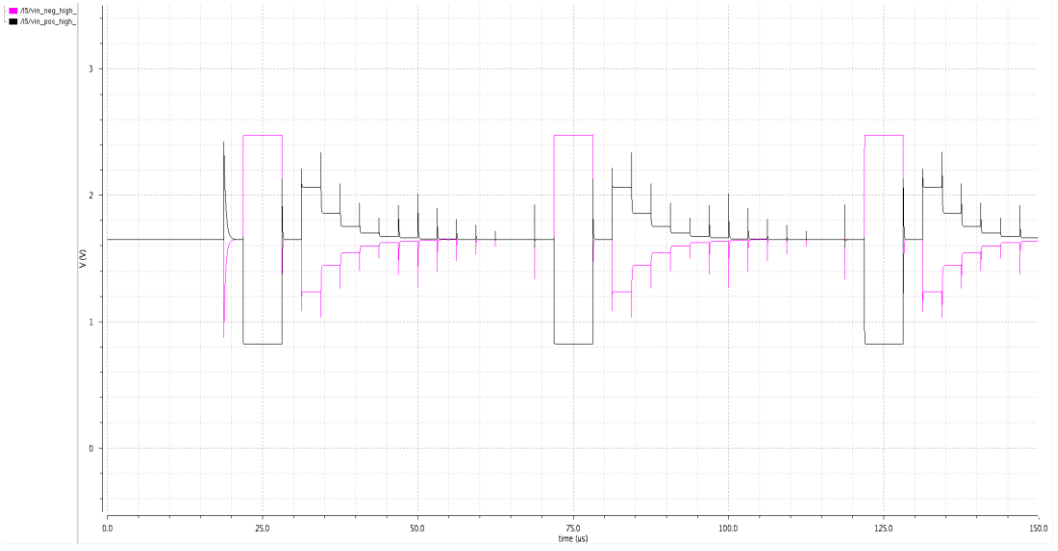

Figure 3-35 : Output voltages of the capacitive array when the differential voltage equals to +1.65V.

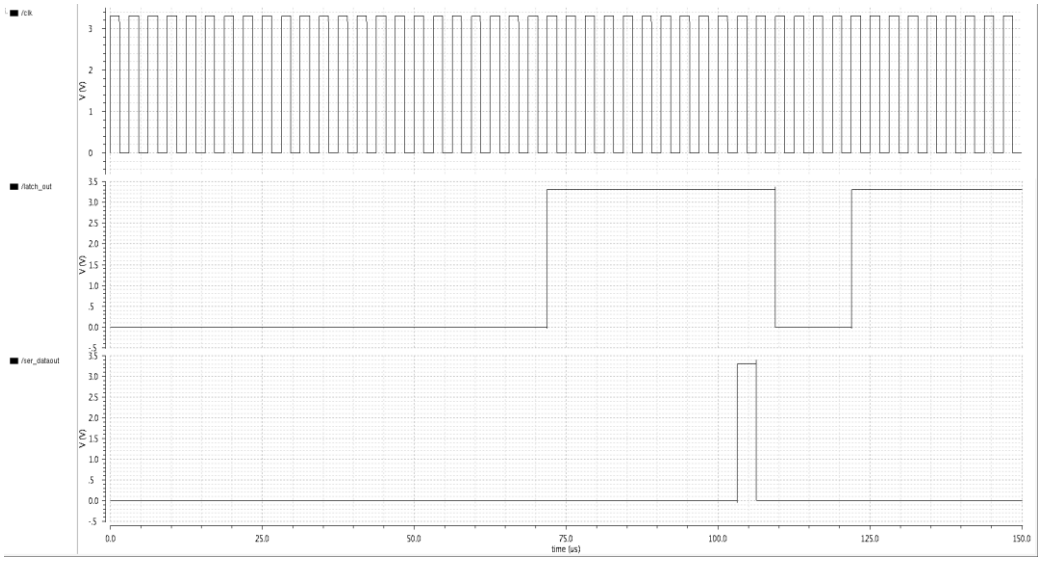

Figure 3-36: Serial output with latch signal when the differential voltage equals to +1.65V.

Figure 3-37 shows the output voltages of the capacitive DAC array when differential the voltage equals to -3.3V and Figure 3-38 shows the serial output of negative differential voltage conversion. The data output is one when the latch signal goes to high. The MSB bit equals to one, since a negative differential voltage is applied.

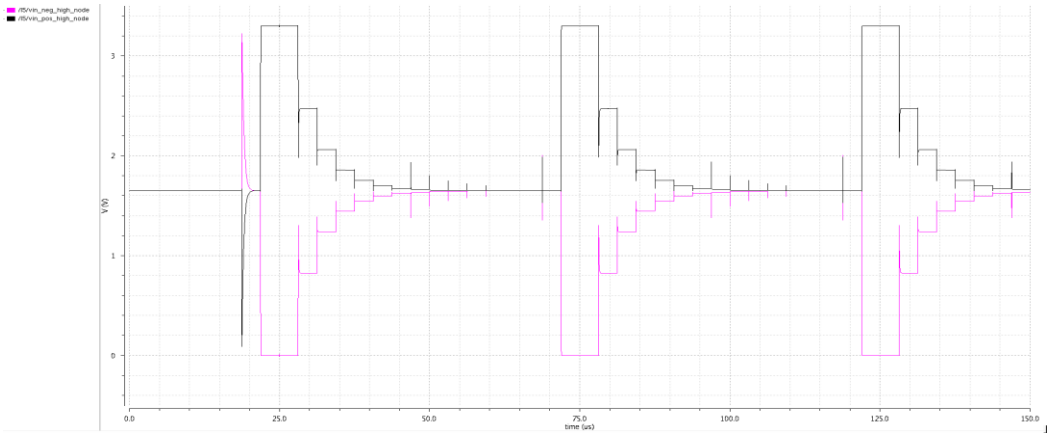

Figure 3-37: Output voltages of the capacitive array when the differential voltage equals to -3.3V.

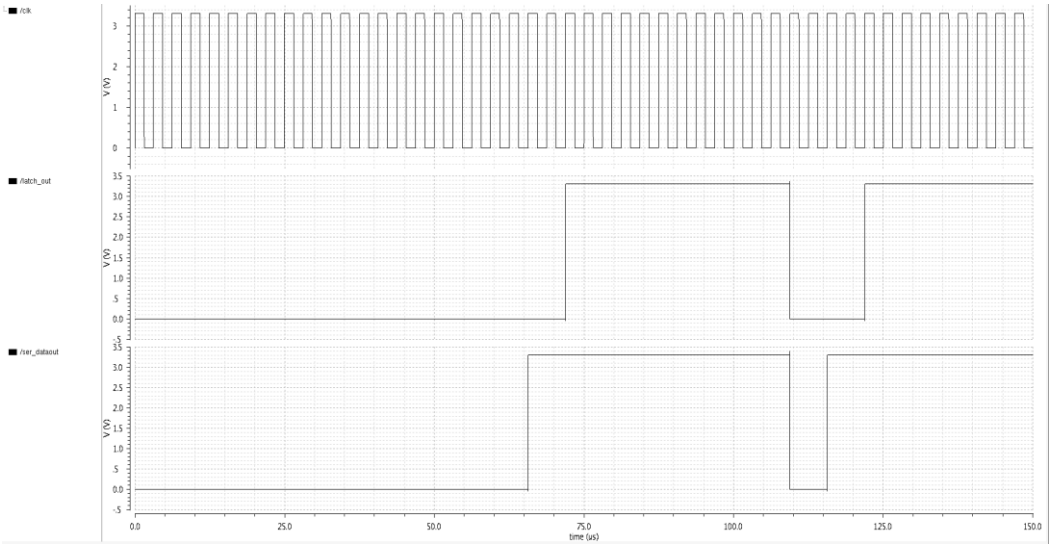

Figure 3-38: The serial output of the negative voltage conversion.

Figure 3-39 shows the output voltages of the capacitive DAC array when the differential voltage equals to 0V and Figure 3-40 shows the output voltages of the capacitive DAC array when the differential voltage equals to 0V. For the differential zero voltage, the MSB can be either zero or one. Both of the outputs are expected. In the simulations, the MSB bit one.

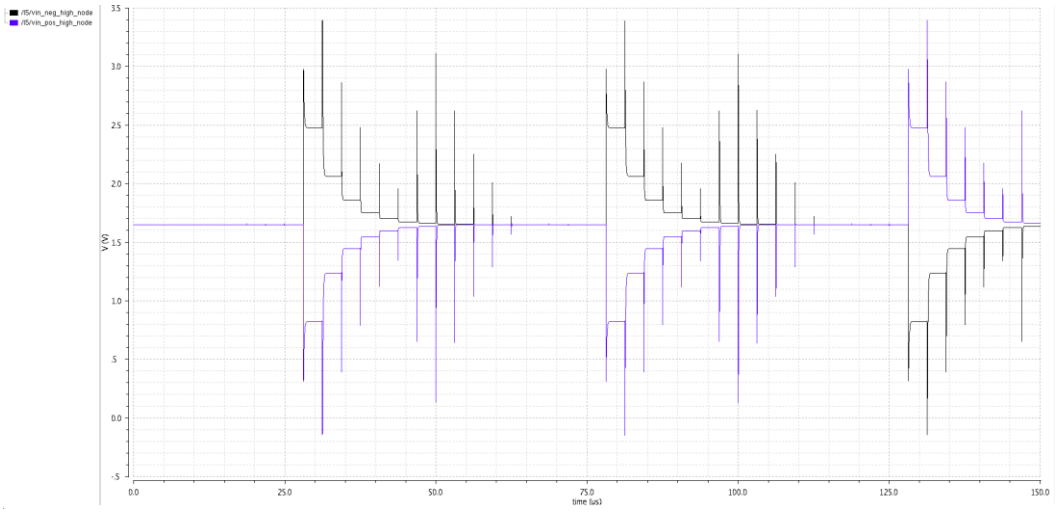

Figure 3-39: Output voltages of the capacitive DAC array when the differential voltage equals to 0V.

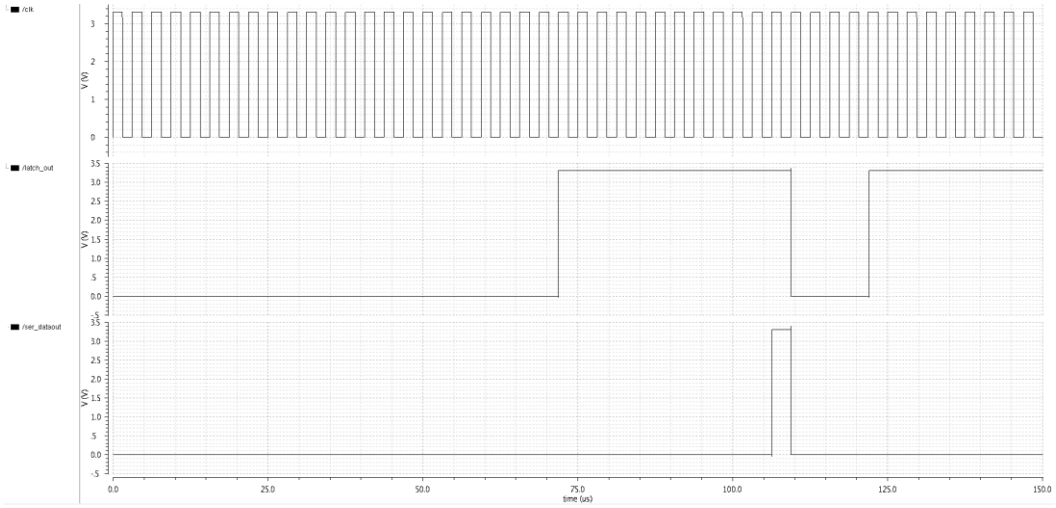

Figure 3-40: Output voltages of the capacitive DAC array when the differential voltage equals to 0V.

Figure 3-41 shows a differential input signal at 1 KHz and reconstructed analog signal. The amplitude of the differential input signal is between 3.3V and -3.3V which covers the whole input range. The reconstructed analog signal looks like a delayed version of the original input signal, since; the ADC's latency is 50 µs which is the one conversion time. The output of the ADC is connected to DAC which has no latency, and consists of resistors.

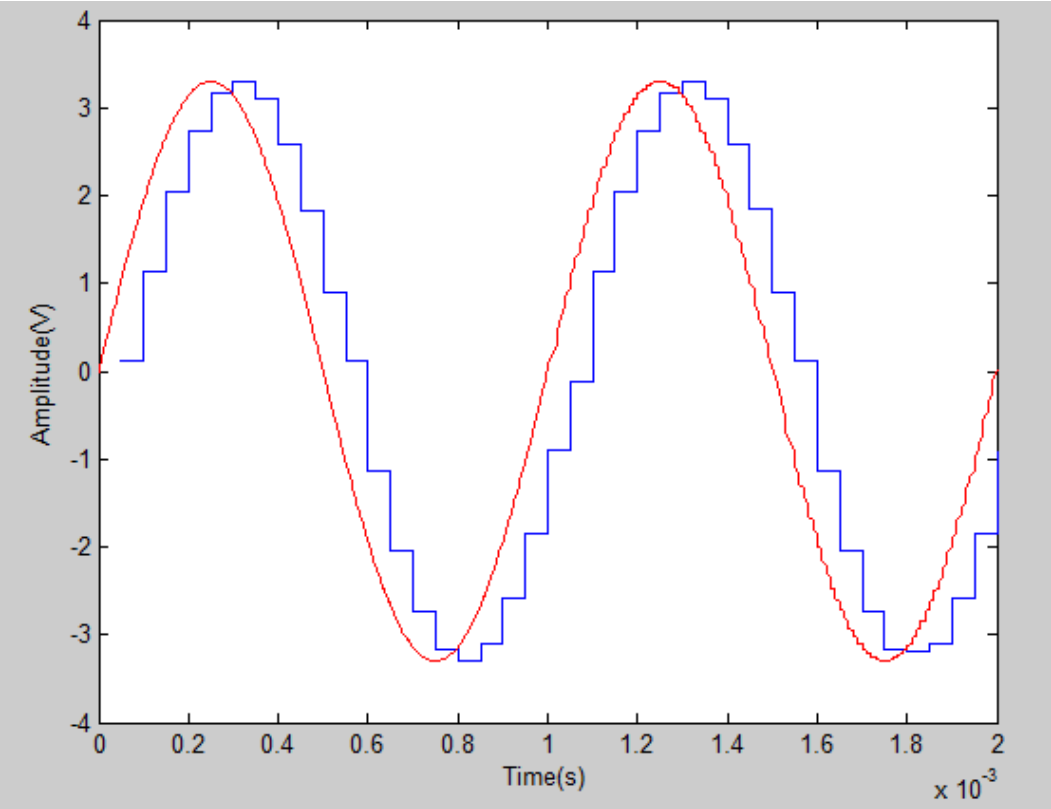

Figure 3-41: Differential input signal at 1 KHz and reconstructed analog signal.

3.6 Literature Comparison and Summary

The resolution of the designed SAR ADC is 12 bit with a sampling rate 20 KS/s. The total noise level is kept below half of the LSB, since the maximum noise value of the comparator is 94 μV and the maximum noise value of the capacitor array is about 81 μV. The standard deviation of the output voltage of the capacitor array is less than the half of the LSB voltage for the worst case. The INL and DNL errors are below the half of the LSB voltage which means that no missing codes are expected. The designed SAR ADC is used for data acquisition systems for the sensor applications. By using the proposed SAR ADC, the significant voltages can be monitored. The SAR ADC requires a small silicon area. Therefore, it can be easily embedded into the different chips. The designed ADC operates at low frequencies, since it will be used in low speed data acquisition applications. The power consumption of the core of the designed SAR ADC is less than 1 mW which is the main specification of the design. The analog core dissipates 116 μW. The capacitor array dissipates 60 μW during charging and discharging. The core of the digital blocks consumes 330 μW. The total power dissipation of the core is around 786 μW. The power consumption of the programmable bias generator without the bandgap circuit is 280 μW. The designed ADC has an extra block referred as bandgap reference which is not included in many designed ADCs in the literature. For this reason, for the fair comparison, the power consumption of this block is ignored. The programmable bias generator is also a unique property for the SAR ADCs which is not included in the many designed ADCs. Table 3-3 shows the comparison of the proposed ADC with the previous designs. The power consumption of the proposed ADC is much lower than the two of the previous works which is the main objective of this thesis. In this work, the expected static errors INL and DNL are kept below the half of the LSB voltages. The INL and DNL errors are reduced compared to the other designs. The supply voltage of the proposed ADC is 3.3V which is a moderate voltage. Although the previous designs have lower supply voltages, the

normalized power consumption of the designed ADC is still lower than the two of the previous designs. The normalized power of the design in [31] is calculated by considering that half of the power is digital power and the remaining power is analog power. Besides that, the designed ADC has a rail to rail comparator which is not introduced into the previous works. As a result, the designed ADC offers a wide range input voltage range between the supply voltages. The designed ADC has a bandgap circuit which provides a supply independent and temperature independent reference voltage. Thus, the reference current does not depend on the external parameters which lead to low noise design. The output serializer is also an important advantage since, 12 parallel signals require more silicon area.

Table 3-3: Comparison of the proposed ADC with the previous designs

Parameter	Design in [29]	Design in [30]	Design in [31]	This work
Architecture	SAR	power-switch-opamp based	SAR	SAR
Technology	0.13µm CMOS	0.8 µm BiCMOS	0.6 µm CMOS	0.35 µm CMOS
Resolution(bits)	12	10	12	12
Sampling Rate(KS/s)	11000	2.9	1000	20
Supply Voltage	1V	2.8V	5V	3.3V
INL(LSB)	-3.0/3.0	-0.98/0.98	0.5	$<\pm 0.5$
DNL(LSB)	-0.8/0.8	-0.67/0.67	0.5	$<\pm 0.5$
Power(µW)	3570	17.9	15000	786
Normalized Power(µW)	3223	11.6	5035	786

CHAPTER 4

TEST OF THE SAR ADC

This chapter analyses the test setup in order to characterize the designed ADC which was sent to the foundry for the fabrication. Section 4.1 overviews the general information about the test setup. Section 4.2 analyzes the designed proximity card for the SAR ADC. Section 4.3 explains the firmware and Section 4.4 clarifies the software issues. Section 4.5 summarizes the test types for the ADC characterization.

4.1 Test Setup

The test setup consists of three main components which are a proximity card, a FPGA card, and a PC. The designed ADC is placed on a proximity card which provides the necessary connection to the external electronics and power supplies. An external electronics such as FPGA can be used in order to generate the required digital signals for the ADC. The communication can be provided between the FPGA and the serial programming interface of the chip. A software tool with graphical user interface is used for simplifying the programming and the characterization of the ADC. The results of the characterization can be written in a text file in which can be processed in MATLAB .Figure 4-1 shows the test setup for the characterization of the SAR ADC. The test setup has 16-bit DAC in order to provide the required input voltages. Other 16-bit DACs provide the required reference voltages and common voltages to the ADC. Low dropout

linear adjustable regulators are used to provide the analog and digital supplies. The digital inputs of the ADC are programmed by the FPGA. The output of the SAR ADC is directly connected to the FPGA which means that, the output can be sampled with the system clock of the SAR ADC. A PC is used for collecting the required data and processes the data in order to characterize the SAR ADC.

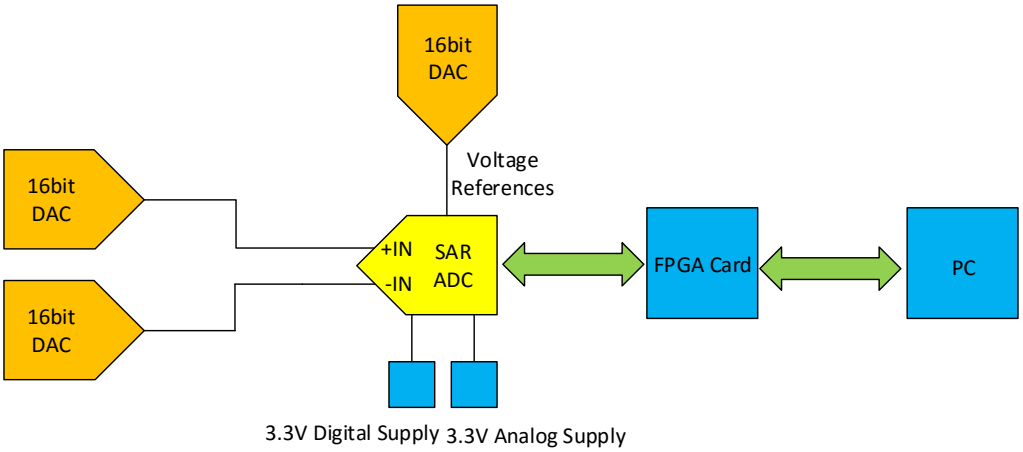

Figure 4-1: Test setup for the characterization of the SAR ADC.

4.2 Proximity Card

The designed ADC is placed on the PCB called as proximity card. The proximity card includes the required powers and signals for the ADC. The characterization of an ADC is a detailed process. Some commercial components should be used in order to turn on the designed ADC. In order to make a compact system, the size of the proximity card is same as with the FPGA card and the designed proximity card is placed on the FPGA card. As a result, the system becomes compact and the noise due to the routings and couplings can be minimized. Commercial low dropout regulators are used in order to provide the required supply voltages. These regulators provide 3.3V analog supply and 3.3V digital supply. The common mode voltage and reference voltage of the capacitor array should be low

noise and fixed voltage. Otherwise, the voltage division in the capacitor array can be changed. For this reason, commercial precious 16-bit DACs are used in order to provide the reference voltages. Besides that, the inputs of the ADCs should be swept from 0V to 3.3V in order to test the performance parameters. As a result, 16bit precious DACs are used. 16 bit DACs are controlled by the FPGA. Thus, the desired voltage can be easily generated. Figure 4-2 shows the layout of the designed proximity card. It includes voltage regulators, DACs, buffers, and connectors for the FPGA and power. The top and bottom view of the PCB is shown in order to see the component placement. The designed ADC is placed in the middle of the card. The voltage regulators are placed around the chip. The 16-bit DAC is located at the left side of the chip. The connection between the FPGA and proximity card is provided by the connectors place on the bottom layer. The voltage of the FPGA is also provided from the switched supply regulator placed on the designed proximity card. Thus, a simple power adopter and USB cable is used for operating the system.

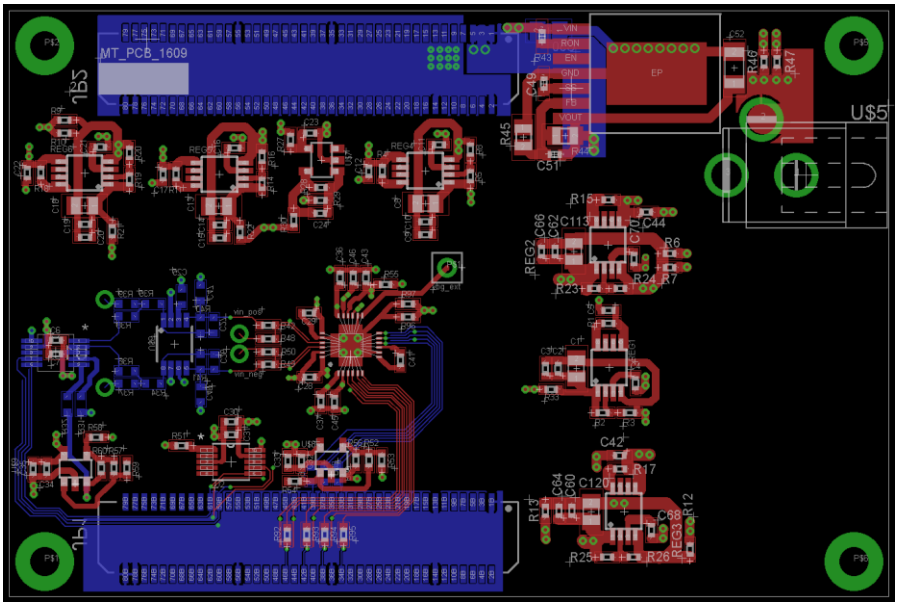

Figure 4-2: Layout of the designed proximity card. It includes voltage regulators, DACs, buffers, and connectors for the FPGA and power. The top and bottom view of the PCB is shown in order to see the component placement.

4.3 Firmware

The required digital signals are generated by the external electronics such as FPGA. In the commercial markets, there are various types of FPGA cards. Figure 4-3 shows the OPAL Kelly XEM6310 FPGA card. It consists of a Spartan-6 processor and various components including flash, regulators and oscillators. The proximity card is placed on the FPGA card via connectors. The FPGA card provides USB 3.0 connection.

Figure 4-3: Opal Kelly XEM 6310 FPGA card [32].

In order to program the FPGA card, a firmware should be written. The firmware is written in the Verilog. It provides the basic signals for the SPI block of the chip. The clock signal and reset signals are the basic signals generated from the FPGA. Then, some input data should be written into the memory registers of the SAR ADC in order to program the chip. The FPGA is not used for only input

signals but also for the outputs of the SAR ADC. The outputs of the SAR ADCs are serial data, serial latch, and the sdout. These output signals are captured by the FPGA card. The output serializer in the SAR ADC generates the outputs at the rising edge of the clock. Therefore, the FPGA has to sample these signals at the falling edge of the same clock. Therefore, the system can be synchronous.

4.4 Software

The software is written in Visual C# programing language. The graphical User interface is comprised of two parts. First part is used to program the SPI of the chip. Second part is reserved for the ADC characterization. Figure 4-4 shows the SPI tab of the GUI for the SAR ADC test and Figure 4-5 shows the ADC characterization tab of the GUI for the SAR ADC test. In the first tab, the SPI of the chip can be configured. The initial condition for the chip and FPGA is reset mode. Firstly, the generated bit file is selected and the FPGA is configured by using configure FPGA button. Secondly, the FPGA is turned on by unchecked the FPGA reset button. Then, the chip is turned on. At that step, the digital inputs are generated in the FPGA. By writing the required settings into the chip registers, the chip can operate. In the second tab, the characterization of the SAR ADC can be performed by adjusting the 16 bit DAC. The outputs are written in a text file in order to process the data in the MATLAB. The 16-bit DACs can be configured in this tab.

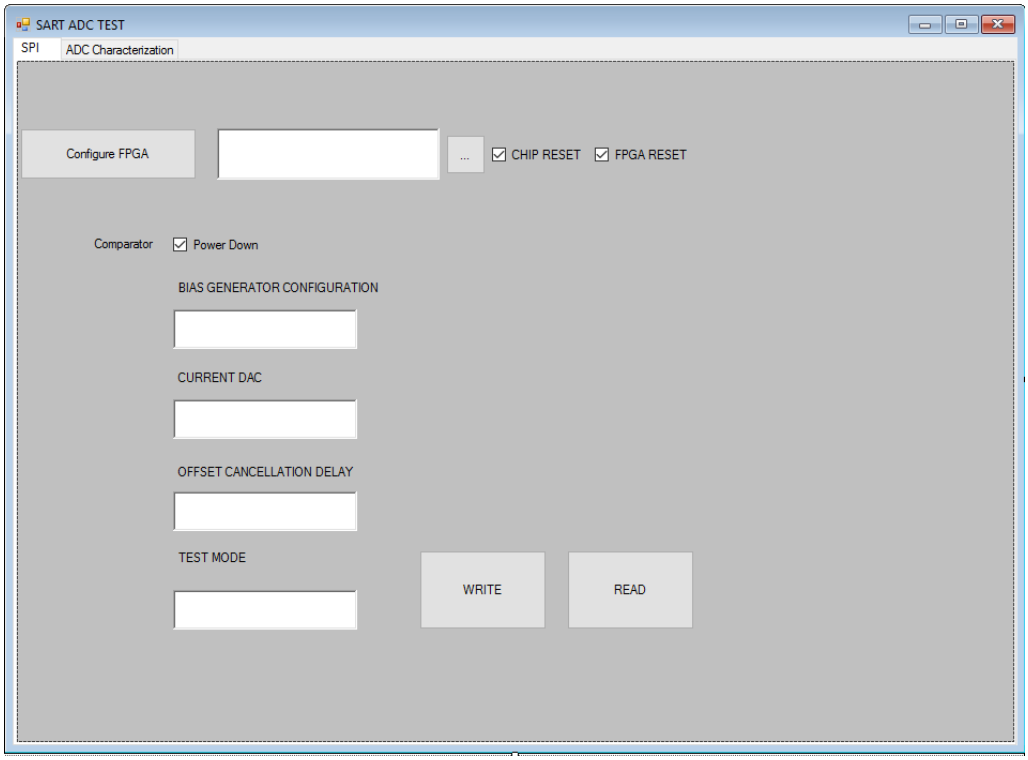

Figure 4-4: SPI tab of the GUI for the SAR ADC test.

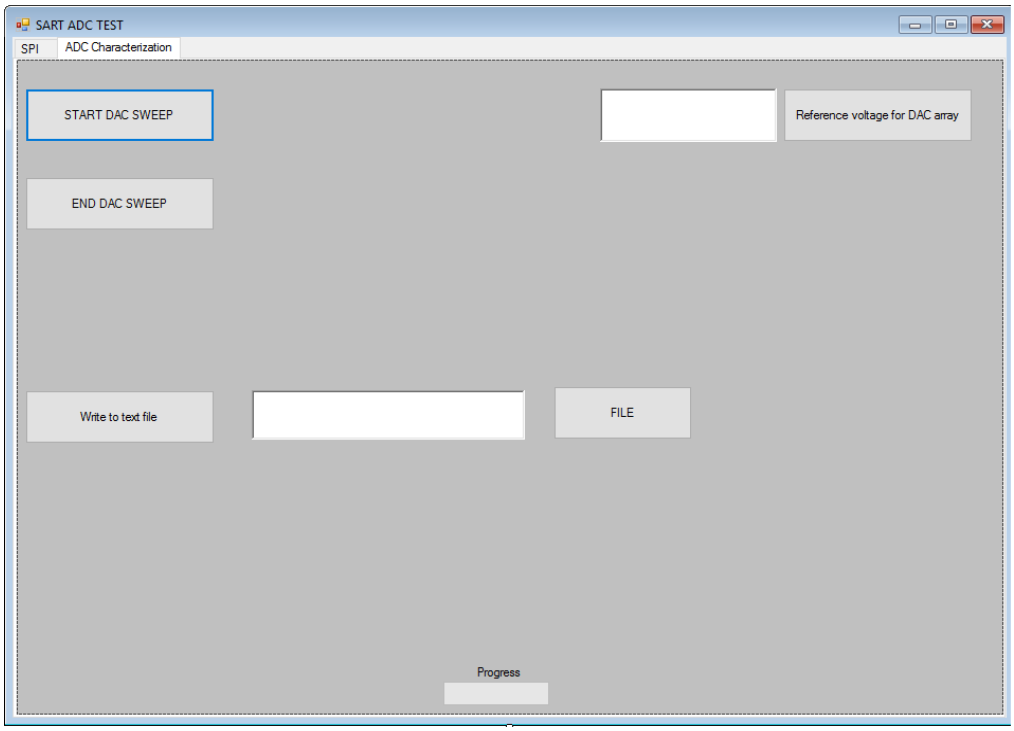

Figure 4-5: ADC Characterization Tab of the GUI for the SAR ADC test.

4.5 Test Types

The designed test setup is used in order to measure some basic parameters such as INL, DNL, SNR and ENOB. In order to measure the INL and DNL parameters, a ramp signal is generated from the 16-bit DAC. The input voltage is swept from the 0V to 3.3V and it is increased by the half of the LSB voltage in order to sample more than one data for each output code. For the SNR and ENOB calculation, a sinusoidal input is required at the inputs of the designed ADC and the output data is collected. After the collection of the output voltages, best fit is method is used to calculate the SNR and ENOB from the sample output voltages. The ENOB test covers the linearity error tests.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The main research objective of this thesis is to design and implement a low power analog-to-digital converter for data acquisition applications. For this purpose, a low power SAR ADC is designed and implemented in 0.35 μm CMOS technology. In order to verify the functionality of the chip, necessary simulations are performed. The outputs are observed according the given input differential voltages. The required performance parameters are analyzed in detail. The designed and implemented chip was submitted to foundry. The achievements of this work can be summarized as follows:

1. The system architectures of the ADCs for data acquisition systems are investigated. Optimized and application specific structure is evaluated based on the power consumption, noise and static parameters.

2. The capacitive DAC array and resistive DAC array structures are investigated based on the required silicon area, noise, static performance and power consumptions. A split capacitive DAC array is chosen in order to save silicon area.

3. The designed ADC has a flexible structure. The bias generator can be configured by the digital controller. Thus, the power consumption can be adjusted. Offset cancellation delay can be set by the digital controller. Each block in the digital controller can be tested individually. Thus, each block can be verified individually.

4. A system model is developed in MATLAB. Critical parameters are analyzed in detail. The implementation of the circuit is based on the system model of the SAR ADC.

5. The power consumption of the core of the chip is less than 1mW which satisfies the main objective of this research.

6. The linearity parameters INL and DNL of the designed ADC are less than half of the LSB which is well below the LSB voltage.

7. The die occupies 2mmx2mm silicon area which is less than 9 $mm^{2.}$.The number of pads is decreased by employing an output serializer.

8. A low noise, and compact test setup is prepared with commercial chip in order to reduce the complexity and noise of the system.

Besides the achievements, some items should be carried out as future work.

1. The reference voltage and common mode voltage of the capacitive DAC array should be generated into the chip. Thus, a proper voltage without noise and distortion can be used in the analog blocks.
2. The capacitive DAC array can be minimized by using small unit capacitors. However, small unit capacitors are affected by the off switch capacitances at the input nodes of the comparator. An optimized solution should be determined.
3. The power consumption can be further reduced by removing flexible structures after verifying the circuit in detail.

REFERENCES

[1] W. Kester, "Which ADC architecture is right for your application?," 2005.

[2] C. Hammerschmidt, "National Semi to commercialize sigma delta ADC," 2008.

[3] J. H. McClellan, R. W. Schafer, and M. A. Yoder, *Signal Processing First*: Pearson/Prentice Hall, 2003.

[4] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*: Oxford University Press, 1998.

[5] Y. U. Mahsereci, "A Successive Approximation Register Analog-To-Dgital Converter For Low-Cost Microbolometers " Msc. Thesis, Electrical and Electronics Engineering, METU, 2012.

[6] D. F. Hoeschele, *Analog-to-digital, digital-to-analog conversion techniques*: Wiley, 1968.

[7] S. K. Tewksbury, F. Meyer, D. Rollenhagen, H. Schoenwetter, and T. Souders, "Terminology related to the performance of S/H, A/D, and D/A circuits," *Circuits and Systems, IEEE Transactions on,* vol. 25, pp. 419-426, 1978.

[8] E. R. Hnatek, *A user's handbook of D/A and A/D converters*: Wiley, 1976.

[9] G. Manganaro, *Advanced Data Converters*: Cambridge University Press, 2011.

[10] C. Donovan and M. P. Flynn, "A "digital 6-bit ADC in 0.25-um CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 432-437, 2002.

[11] M. Integrated, "Understanding Flash ADCs."

[12] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 2139-2151, 2004.

[13] G. Beanato, "Design of a Very Low Power SAR Analog-to-Digital Converter," Msc. Thesis, Electrical and Electronics Engineering, EPFL.

[14] J. P. Crooks, S. E. Bohndiek, C. D. Arvanitis, R. Speller, H. XingLiang, E. G. Villani, *et al.*, "A CMOS Image Sensor With In-Pixel ADC, Timestamp, and Sparse Readout," *Sensors Journal, IEEE,* vol. 9, pp. 20-28, 2009.

[15] A. Bonetti, "Low-Power and Compact Successive Approximation ADC for Bio-Electronic Chips," Master Thesis, Electrica and Electronics Engineering, Politecnico di Milano, 2010-2011.

[16] B. Razavi, *Principles of data conversion system design*: IEEE Press, 1995.

[17] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for Smart Dust," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1123-1129, 2003.

[18] N. Verma and A. P. Chandrakasan, "A 25/spl mu/W 100kS/s 12b ADC for wireless micro-sensor applications," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 822-831.

[19] L. Chun-Cheng, C. Soon-Jyh, H. Guan-Ying, and L. Ying-Zu, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 731-740, 2010.

[20] D. Johns and K. W. Martin, *Analog integrated circuit design*: John Wiley & Sons, 1997.

[21] R. J. Baker, I. o. Electrical, E. Engineers, and I. S.-S. C. Society, *CMOS: Circuit Design, Layout, and Simulation*: Wiley, 2008.

[22] L. Zengjin, Y. Haigang, Z. Lungui, S. Jiabin, and X. Shanhong, "Modeling of capacitor array mismatch effect in embedded CMOS CR SAR ADC," in *ASIC, 2005. ASICON 2005. 6th International Conference On*, 2005, pp. 982-986.

[23] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, "Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog

Converters Used in Successive Approximation ADCs," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 58, pp. 1736-1748, 2011.

[24] F. B. Boschker, "Design of a 12bit 500Ms/s standalone charge redistribution Digital-to-Analog Converter," Msc. Thesis, Electrical Engineering, Mathematics and Computer Science, University of Twente, 2008.

[25] T. L. Brooks and A. L. Westwick, "A low-power differential CMOS bandgap reference," in *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, 1994, pp. 248-249.

[26] B. Razavi, *Design of Analog CMOS Integrated Circuits*: Tata McGraw-Hill, 2002.

[27] Z. Yan, C. Chi-Hang, U. F. Chio, S. Sai-Weng, U. Seng-Pan, R. P. Martins, *et al.*, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 1111-1121, 2010.

[28] T. O. Anderson, "Optimum Control Logic for Successive Approximation Analog-to-Digital Converters," 11/1972.

[29] J. J. Kang and M. P. Flynn, "A 12b 11MS/s successive approximation ADC with two comparators in 0.13 um in CMOS," in *VLSI Circuits, 2009 Symposium on*, 2009, pp. 240-241.

[30] G. Bonfini, A. S. Brogna, C. Garbossa, L. Colombini, M. Bacci, S. Chicca, *et al.*, "An ultralow-power switched opamp-based 10-B integrated ADC for implantable biomedical applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 51, pp. 174-177, 2004.

[31] G. Promitzer, "12 bit low power fully differential switched capacitor non-calibrating successive approximation ADC with 1MS/s," in *Solid-State Circuits Conference, 2000. ESSCIRC '00. Proceedings of the 26rd European*, 2000, pp. 176-179.

[32] “XEM 6310 FPGA USB 3.0 Module,” ed: OPAL Kelly.