A STUDY ON A LOW PHASE NOISE CHARGE PUMP PHASE-LOCKED LOOP AT 2.8 GHZ

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A STUDY ON A LOW PHASE NOISE CHARGE PUMP PHASE-LOCKED LOOP AT 2.8 GHZ

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ABSTRACT

A STUDY ON A LOW PHASE NOISE CHARGE PUMP PHASE-LOCKED LOOP AT 2.8 GHZ

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Today, the most challenging problem that Phase Locked Loop (PLL) designers face with is the design of ultra-low phase noise PLL at high frequencies. In this research, a high frequency charge-pump phase-locked loop (CPPLL) with low phase noise is studied. At the beginning stage, a gate grounding Colpitts Voltage Controlled Oscillator (VCO) using a High Electron Mobility Transistor (HEMT) is designed. The provided VCO achieved -131dBc/Hz at 1 MHz offset phase noise with the 2.6-3 GHz oscillating frequency ranges. Inserting a PLL chip around the VCO can reduce the achieved phase noise. Therefore, to investigate this phenomenon a CPPLL is simulated. The CPPLL components, namely the Phase Frequency Detector (PFD), Charge Pump (CP), and the frequency divider are investigated individually. The loop filter design is also taken into account as it plays a vital role in determining the loop bandwidth of the CPPLL. Finally, the phase noise of the implemented CPPLL is simulated. Assuming noiseless crystal oscillator, the phase noise is calculated as -120 dBc/Hz at 100 Hz offset. The phase noise is decreased successfully 90 dBc compared to the VCO phase noise (-32 dBc/Hz at 100 Hz). When the noise of the crystal oscillator is included, the phase noise at 100 Hz reached to -101 dBc/Hz. Related simulations are conducted on microwave simulation tool (ADS).

Keywords: PLL, phase noise, CPPLL, VCO, HEMT, ADS, PFD, CP

ÖZ

2.8 GHZ'DE DÜŞÜK FAZ GÜRÜLTÜLÜ YÜK POMPALI FAZ KILITLEMELI DÖNGÜ ÜZERİNE BİR ÇALIŞMA

Keykhali, Mahsa
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Günümüzde; faz kilitlemeli döngü (PLL) tasarımlarıyla uğraşan araştırmacıların karşılaştığı en zor problem, yüksek frekansta çalışan, düşük faz gürültüsüne sahip olan PLL tasarımları yapmaktır. Bu çalışmada, yüksek frekansta çalışan düşük faz gürültülü yük pompalı faz kilitlemeli döngü (CPPLL) tasarımı yapılmıştır. İlk bölümde, yüksek hareketli electron transistörler (HEMT) kullanılarak, topraklanmış kapılı Colpitts voltaj kontrollü osilatör (VCO) tasarlanmıştır. Tasarlanan VCO 2.6-3 GHz frekans aralığında çalışmakta olup, faz gürültüsü 1 MHz'de -131 dBc/Hz'dir. Voltaj kontrollü osilatörün çevresine PLL çip yerleştirilerek faz gürültüsü azaltılabilir. Bu durumu gözlemlemek amacıyla CPPLL benzetim çalışmaları yapılmıştır. CPPLL tasarımı yapılırken; Faz Frekansı Detektörü (PFD), Yük Pompası (CP) ve frekans bölücüler ayrı ayrı incelenmiştir. Ayrıca, CPPLL'in döngü bant genişliğinin belirlenmesinde önemli bir rol oynadığı için döngü filtre tasarımı da dikkate alınmıştır. Son olarak, CPPLL'in faz gürültüsü için benzetim çalışmaları yapılmıştır. Gürültüsüz kristal osilatör varsayılarak, faz gürültüsü 100 Hz'de -120 dBc/Hz olarak bulunmuştur. Faz gürültüsü, voltaj kontrollü osilatörün faz gürültüsüne (100 Hz de -32 dBc/Hz) göre 90 dBc azaltılmıştır. Kristal osilatörün gürültüsü eklendiğinde ise, 100 Hz'deki faz gürültüsü -101 dBc/Hz'e ulaşmıştır. İlgili benzetim çalışmaları, mikrodalga benzetim aracı ADS ile yapılmıştır.

Anahtar Kelimeler: PLL, Faz Gürültüsü, CPPLL, VCO, HEMT, ADS, PFD, CP

Dedicated to,

my husband Nasser for his love and support,

my mother who was always there for me,

the memory of my father, I wish he were alive.

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LIST OF ABBREVIATIONS

ADPLL	All-Digital PLL
ADS	Advanced Design System
BW	Band Width
C	Capacitor
CCO	Current Controlled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
CMFB	Common Mode Feed Back
CP	Charge Pump
CPPLL	Charge Pump PLL
CSA	Current Steering Amplifier
DCO	Digitally Controlled Oscillator
DF	Data Followed
DFF	D-Flip-Flop
DPLL	Digital PLL
FEPFD	Falling-Edge PFD
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
ILD	Injection-Locking-Divider
LC	Inductor Capacitor
LPF	Low Pass Filter
LPLL	Linear PLL
MWCNT	Multi Wire Carbon Nano Tube
MPTPFD	Modified Precharge Type PFD
NDR	Negative Differential Resistance
NMOS	N-channel Metal Oxide Semiconductor
NRZ	None Return to Zero
PD	Phase Detector
PFD	Phase Frequency Detector

PLL	Phase Locked Loop
PMOS	P-channel Metal Oxide Semiconductor
R	Resistor
RF	Radio Frequency
SR	Set-Reset
SRAM	Static Random Access Memory
SymFET	Symmetric graphene tunneling Field Effect Transistor
TSPC	True-Single-Phase-Clocking
VCO	Voltage Controlled Oscillator

CHAPTER 1

INTRODUCTION

1.1 Motivation

Harmonic Motion Microwave Doppler Imaging (HMMDI) method is recently proposed by researchers in Middle East Technical University (METU) [5]. This method is a non-invasive hybrid breast imaging technique for tumor detection [6]. The HMMDI method is shown in Figure 1.1. In HMMDI a microwave signal is transmitted to the tissue which has a harmonic motion due to ultrasound excitation. The backscattered signal is phase modulated due to this motion. The fist spectral component of the received signal is called as Doppler signal. This Doppler signal contains information about dielectric and elastic properties of the tissue. The main goal in this method is to sense the Doppler signal. The vibration frequencies are in the range of a few Hz, while the carrier microwave frequency is in a range of a few GHz. Therefore, the phase noise of the transmitter should be as low as possible to realize the Doppler signal. This thesis study is an attempt to design a low phase noise signal generator for the HMMDI system developed at METU.

Phase noise plays a vital role in many communication systems as the performance of the systems can be significantly affected by the phase noise. Signal regeneration techniques were developed to minimize the phase noise [7]. Phased locked loop (PLL) is one of them that have been used largely.

PLL is a kind of timing and frequency control circuit. Timing and frequency control circuit designates the use of timing and frequency synthesis in any circuit, especially the circuits used in communication areas. As timing and frequency control circuits

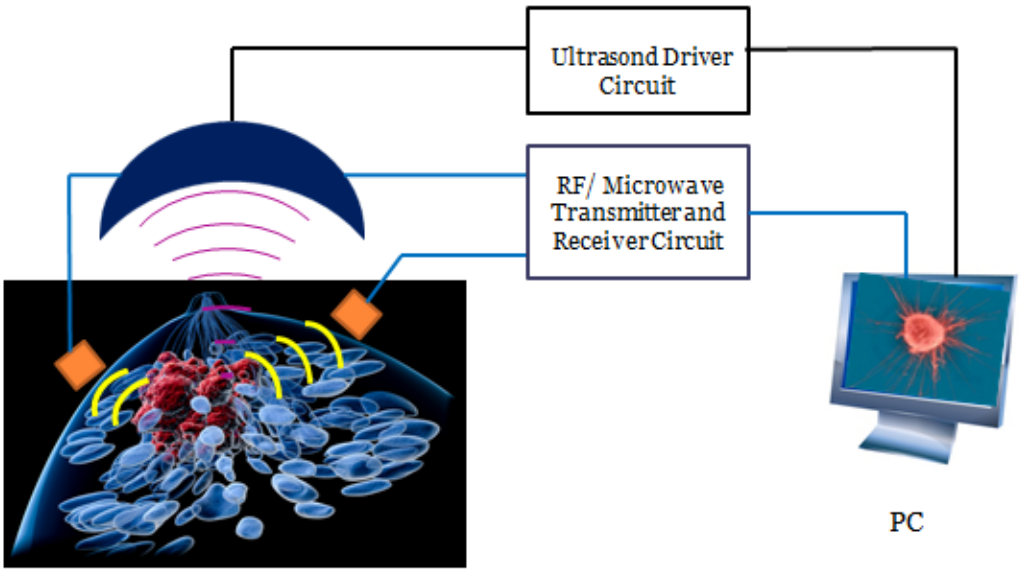


Figure 1.1: Harmonic Motion Microwave Doppler Imaging

are used everywhere, including our laptops and mobile devices for time and frequency synchronization purposes, the importance of these circuits in today's world can not be ignored. The timing and frequencies of input signal and feedback signal are matched using these circuits, as a result, a signal in phase with the input signal is generated. A PLL tracks phase noise of the reference frequency within its loop bandwidth, relaxing the close-in phase noise requirements of the VCO. For PLL applications, the reference input signal generated by a high purity crystal oscillator has very low phase noise, and the PLL serves to lock the output frequency on a multiple of the input frequency. Negative feedback path made the PLL operates by trying to lock to the phase of a very stable input signal.

Phase-locked loops can be used, for example, to generate stable output frequency signals from a fixed low-frequency signal. In a phase locked loop, the error signal from the phase detector is the difference between the input signal and the feedback signal. Implementation of these signals in multichannel wireless systems is also a tedious task. A multichannel wireless system utilizes multi-band frequencies in a single system for different applications of different frequencies. In this case, the timing and frequency circuit plays a vital role in choosing the frequency which is suitable for a particular application among the bands of frequencies present in the system.

1.1.1 Literature Review

In 1932, the first application of a PLL is introduced [8]. After that various types of PLLs have been developed [1]. In 2008, a low power, low phase noise PLL is designed, that introduced Phase Noise per Unit Power PNUP, for all of the blocks of the PLL [9]. A digital PLL (DPLL) is provided in 2010. The designed PLL can improve the lock time [10]. Following the studies done in the field of PLL, in 2011, a capacitor free PLL is designed with analog Voltage Controlled Oscillator (VCO) while other components are digital. In this design, inclusion of digital components eliminates the use of capacitor and resistor in the circuit [11]. In 2012, a semi digital PLL is offered. The most important future of this design is that, it can be applied for a wide reference frequency ranges, without any variation in block parameters [12]. A PLL introduced in 2014, consisted of a built-in static phase offset (SPO) detector [13]. The All-Digital PLLs are studied in [14, 15]. Finally, the charge pump PLLs are introduced in [16, 17]. In Table 1.1 the characteristics of various PLL circuits are presented.

Table 1.1: Characteristics of recent PLL circuits in the literature.

Ref	**Technology**	**Output frequency (GHz)**	**Power consumption (mW)**	**Phase noise (dBc/Hz)**	**area** (mm^2)
[9]	0.25 SOI	6.8	32.75	-90 @ 100 kHz	-
[10]	0.18 mm CMOS	200 MHz–1 GHz	-	-	-
[11]	45 nm	1-1.4	-	-	0.081
[12]	65 nm	-	8.4	-115 @ 5 MHz	0.052
[13]	65 nm CMOS	0.4 - 1.0	0.92 - 2.31	-82.78 @ 100 kHz	0.079
[15]	65 nm CMOS	0.39-1.41	0.78 @ 900 MHz	-	0.0066
[17]	65 nm CMOS	1	19	-	0.12

1.1.2 Fundamentals of Phase-Locked Loops

An oscillator's output signal is synchronized with a reference input signal in both frequency and phase by the use of a PLL circuit. When the PLL is locked, the phase error of the reference signal and the oscillator's output is constant (not essentially zero) in other words, reference signal and the oscillator output are synchronized. If a phase error occurs the feedback control mechanism will reduce the phase error. The feedback control system of a PLL is shown in Figure 1.2 [4].

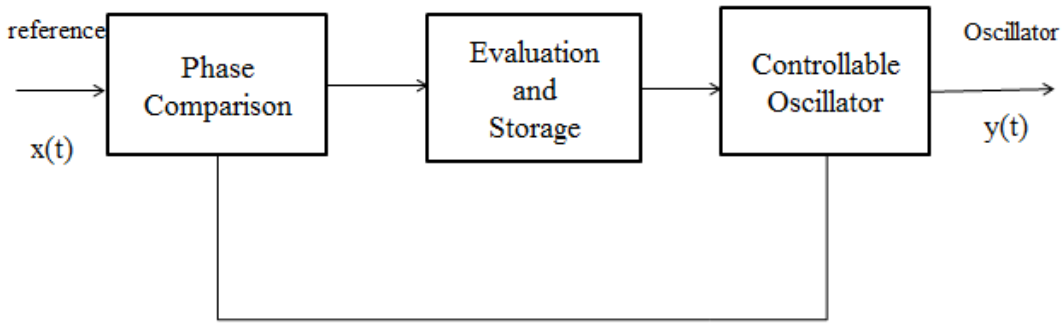


Figure 1.2: Phase-locked loop feedback mechanism. x(t) is the input and y(t) is the output of the system.

In Figure 1.2, the operation of a PLL is summarized in three steps of phase comparison, evaluation and storage, and a controllable oscillator. Following is detailed description of each component:

1. Comparison: Phase (or frequency) of the reference signal is compared with the phase of the produced signal using this block. An error signal proportional to the phase difference is generated. ($V_{error} = K_{PD}\Delta\phi$), where K_{PD} is the gain of a phase detector that makes the ideal transfer function of this block and $\Delta\phi$ is the phase error of the reference signal and the oscillator's output.

2. Evaluation and Storage: A control variable resulted in comparison is generated by this block then the stored value (voltage or current) is modified to apply to the oscillator. In general, a Low-Pass Filter (LPF) is applied which smooths the variation caused by the input noise.

3. Controlled Oscillator: This block is a nonlinear stage whose role is production of

an oscillation that is frequency controlled using a lower frequency voltage or current input. The controlled oscillator can be a Voltage Controlled Oscillator (VCO) or a Current Controlled Oscillator (CCO).

1.1.3 Phase-Locked Loop Types

As depicted in Table1.2 [4], PLLs are divided in 4 groups that will be reviewed as follows:

Table 1.2: PLL classification

PLL Type	Comparison	Evaluation	Storage	Oscillator
Linear PLL (LPLL)	Analog multiplier	LPF	Analog voltage on filter capacitor	VCO
Digital PLL (DPLL)	EXOR PD or JKPD	LPF	Analog voltage on filter capacitor	VCO
Charge-pump PLL (CPPLL)	PFD	Charge pump and LPF	Analog voltage on filter capacitor	VCO
All-digital PLL (ADPLL)	EXOR PD or JKPD or PFD	Digital LPF	Digital word	Digitally controlled oscillator (DCO)

1.1.3.1 Linear PLL

Linear PLL (LPLL) is the fundamental type of PLLs that includes an analog mixer phase detector (analog multiplier), LPF and a VCO as demonstrated in Figure 1.3 [4]. It should be noted that the control voltage of a VCO is the low frequency component of the multiplier output elicited by the LPF. The input amplitude dependency and the nonlinear gain builds up the major drawbacks of this PLL.

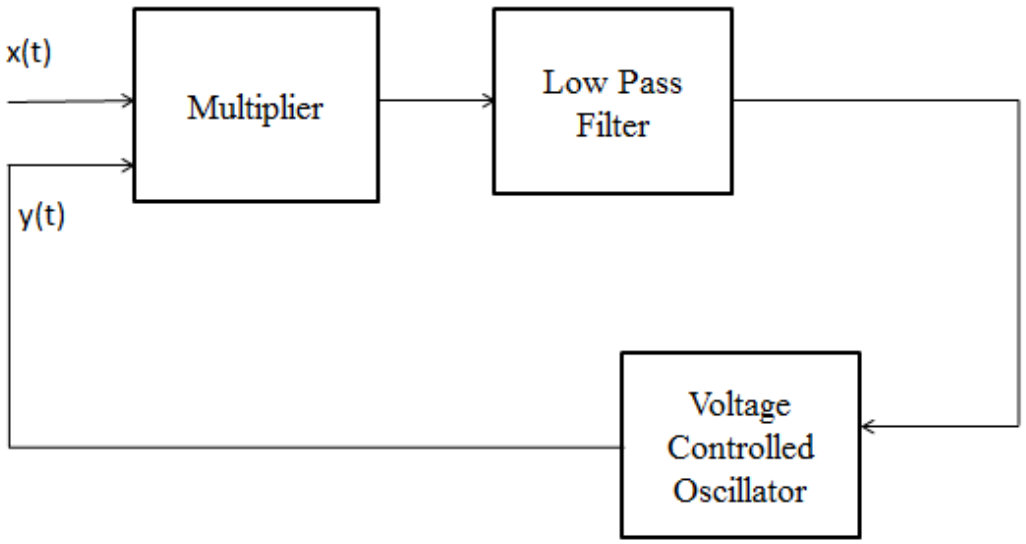


Figure 1.3: Linear PLL block diagram. x(t) is the reference signal and y(t) is the feedback signal.

1.1.3.2 Digital PLL

The drawbacks of the LPLL improved by XOR PD implementation. On the other hand, the use of XOR PDs caused input duty cycle sensitivity. Therefore, use of JK flip flops can be a solution to this problem. The block diagram of digital PLL is demonstrated in Figure 1.4 [4]. Digital PLL, in spite of it's name, contains mostly analog blocks except PD. The PD generates a continuous signal as an input to analog loop filter.

1.1.3.3 All-Digital PLL

The All-Digital PLL block diagram that is shown in Figure 1.5 [4] have some advantages such as, reduction of lock time that makes it suitable choice for microprocessors with power management networks. Moreover, accurate storage of the phase and frequency information is applicable using digital methods.

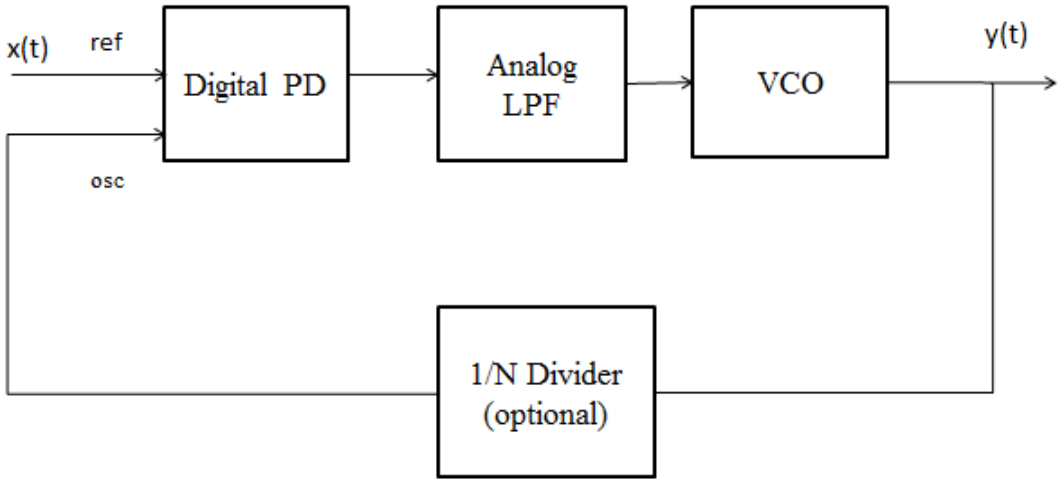


Figure 1.4: Digital PLL block diagram. x(t) and y(t) denote the input and output signals, respectively. ref is the reference signal, and osc is the feedback signal at the input.

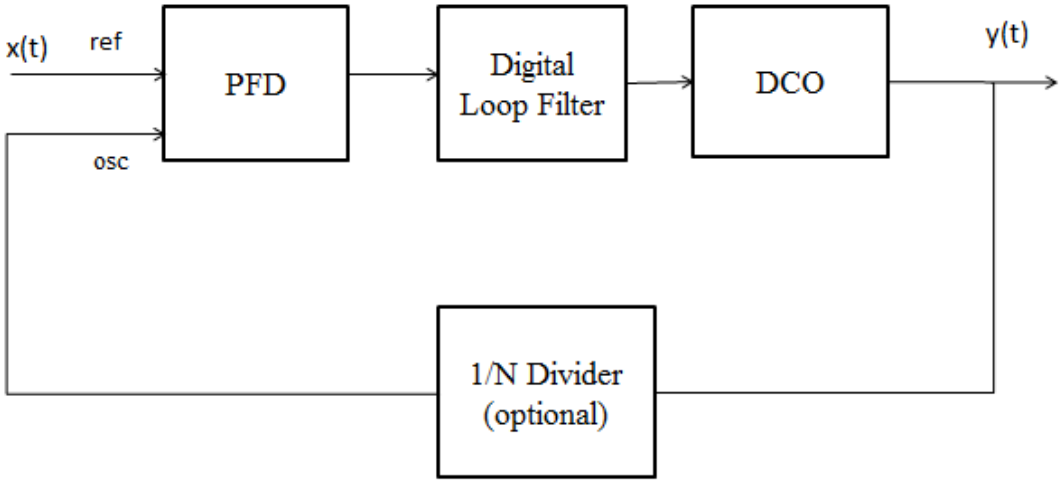


Figure 1.5: ALL-Digital PLL block diagram. x(t) and y(t) denote the input and output signals, respectively. ref is the reference signal, and osc is the feedback signal at the input.

1.1.3.4 Charge Pump PLL

The Charge Pump PLL (CPPLL), offered as a solution to the phase locking problem, including Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter and an oscillator. The block diagram of the general CPPLL is illustrated in Figure 1.6 [4], where a first order passive filter is applied.

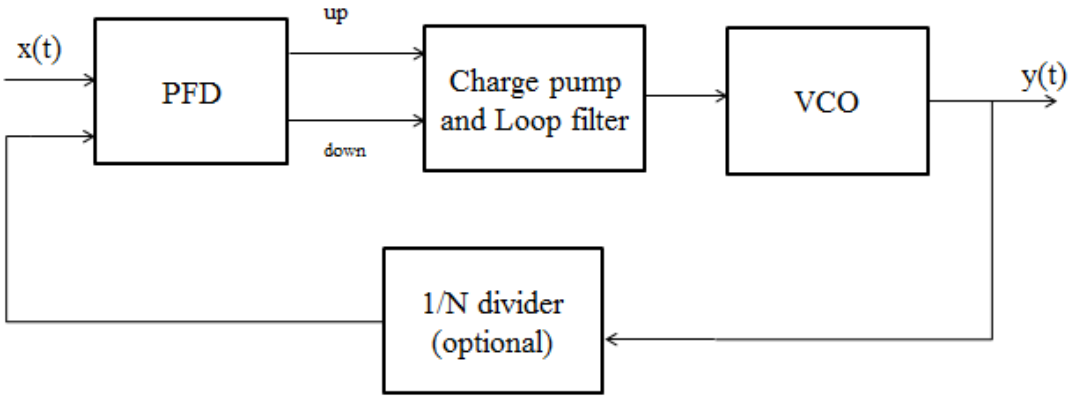


Figure 1.6: Charge Pump PLL block diagram

The difference of this type of PLL from other types is the PFD capability in not only detecting the phase but also tracking the frequency [4].

The VCO, is the main block of the PLL. In other words, it acts as the heart of the PLL. Therefore, in Table 1.3 the summary of the performance characteristics of the studied VCOs in literature review is presented.

Table 1.3: The performance characteristics of the illustrated VCOs in literature review

Ref	Technology	Freq(GHz)	Tuning range (GHz)	DC power (mw)	Supply (v)	Phase noise(dBc/Hz)
[18]	0.5μm GaAsPHEM	49	48.7-49.7	75	5	-100 @ 100kHz
[19]	65nm CMOS	3.6	-	5.6	1	-123 @ 600kHz -126 @ 800kHz -137 @ 3 MHz
[20]	SymFET	3.05-3.07	-	0.23	0.3	-117 @ 1 MHz
[21]	90 nm CMOS	5.2	4.62-5.81 (22.9%)	1.35	2.7	-130.1 @ 600kHz
[22]	0.18μm CMOS	10.94	7.5%	0.346	0.46	-107.8 @ 1 MHz
[23]	0.18μm BiCMOS	2.4	2.07-2.77 (29.16%)	1.7	0.6	-133.3 @ 1 MHz
[24]	-	24.29 24.10	23.3-25.90 (10.54%) 23.25-25.74 (10.33%)	-	-	-88.34 @ 1 MHz -92.039 @ 1 MHz
[25]	0.25μm BiCMOS SiGe:C	19.9 20.06	415MHz(V_{tune}=0-5 V) 130MHz (V_{tune}=0-5 V)	22.35 12.5	2.5 2.5	-106 @ 1 MHz -96.5 @ 1 MHz
[26]	0.18μm CMOS	2.16	2.12-2.25	-	-	-110 @ 1 MHz
[27]	0.35μm BiCMOS	2.33	26 %	-	2.5	-121 f_c=1.91 @ 600 kHz -117 f_c=2.03 @ 600 kHz -115 f_c=2.63 @ 600 kHz

In this work, having a pure signal with low phase noise is the main goals to achieve the desired results at the proceeding steps. Therefore, design of a low phase noise PLL is planned. The Charge Pump PLL (CPPLL) is preferred. The proposed CPPLL frequency synthesizer block diagram is shown in Figure 1.7. CPPLL is composed of a phase and frequency detector (PFD), charge pump (CP), loop filter, Voltage Controlled Oscillator (VCO), and frequency divider.

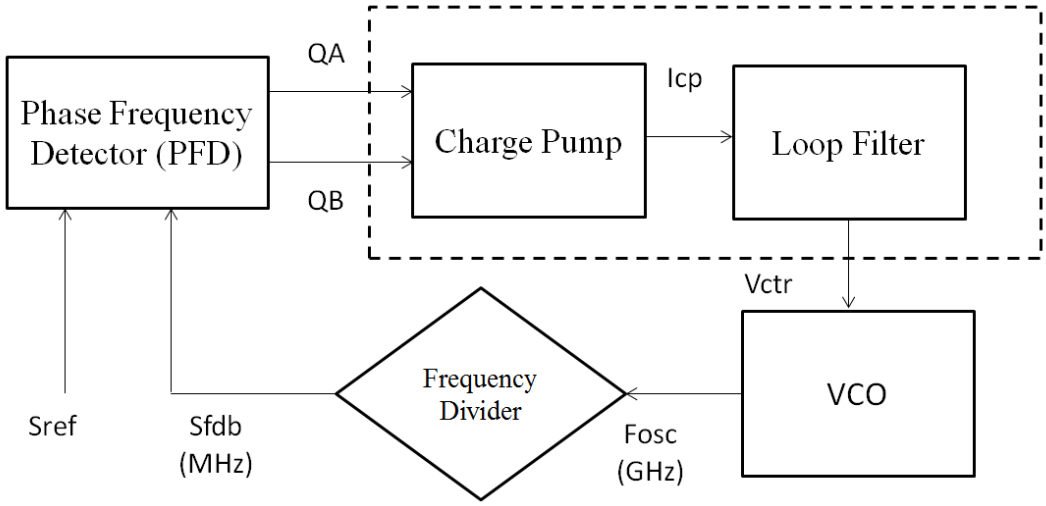


Figure 1.7: The main building components for CP-PLL. Sref is the reference signal, Sfbd is the VCO output signal after division, Fosc is the VCO output frequency, Vctr is the control voltage of VCO, Icp is the current generated in charge pump, QA and QB are the up and down signals generated in PFD output, respectively.

1.2 Scope of this thesis

1. To reduce the phase noise of the microwave transmitter by realizing -120 dBm to -100 dBm Doppler signal at few Hz beside a carrier frequency of a few GHz for the HMMDI method.

2. To design a voltage controlled oscillator that works in a few GHz frequency ranges with low phase noise.

3. To design a PLL with the ultimate goal of reducing the VCO's phase noise in frequencies close to the carrier frequency.

4. To analyze the phase noise performances of the implemented PLL.

1.3 Thesis Organization

In chapter 2, the basic concepts of the PLL will be studied. In this chapter, a review of the fundamentals of the PLL will be offered. The VCO basics and the phase noise concepts will be introduced. A review of the PFD, one of the important components of the PLL will be offered. The CP and loop filter basics will be studied. The chapter will be finalized by the review of the frequency divider.

Chapter 3, contains the design of the PLL constructing blocks. In this chapter, first, the VCO design will be discussed. Then, the frequency divider design and implementation will be introduced. The phase frequency detector design will be offered next. Finally, the charge pump and loop filter design will be presented.

In chapter 4, the simulation results of the implemented PLL (using ADS) are presented. In this chapter the analog-digital PLL will be offered, fist. Then the all-analog PLL will be presented.

Chapter 5, includes the phase noise analysis of the implemented PLL. The influence of the PLL on the VCO's phase noise is discussed in this chapter.

Finally, chapter 6, will provide the conclusion and future works of this study.

CHAPTER 2

PHASE-LOCKED LOOPS

In this chapter, the basic concepts of the PLL will be studied. A review of the fundamentals of the PLL will be offered. The VCO basics and the phase noise concepts will be introduced. A review of the PFD, one of the important components of the PLL will be offered. The CP and loop filter basics will be studied. The chapter will be finalized by the review of the frequency divider.

2.1 Basic concepts

2.1.1 Voltage Controlled Oscillator

An ideal VCO is characterised as 2.1

$$\omega_{out} = \omega_0 + K_{VCO}V_{cont} \tag{2.1}$$

where ω_0 is the free running frequency at V_{cont}=0 and K_{VCO} is called as the gain or sensitivity of the oscillator [1].

The VCO is considered as a time invariant system in study of PLLs. In this system, the control voltage is defined as the input of the system and the excess phase of the carrier is the system's output. The excess phase can be defined as 2.2

$$\phi_{out}(t) = K_{VCO} \int V_{cont}dt \tag{2.2}$$

Accordingly, the transfer function of the VCO is

$$\frac{\phi_{out}}{V_{cont}}(s) = \frac{K_{VCO}}{s} \tag{2.3}$$

2.1.2 Phase Detector

The operation of an ideal phase detector is defined as the generation of an output signal as a result of the phase difference of the input signals. In Figure 2.1, the characteristics of an ideal phase detector is shown [1]. The phase detector characteristics is given in equation 2.4

$$V_{out}(t) = K_{PD}\Delta\phi \tag{2.4}$$

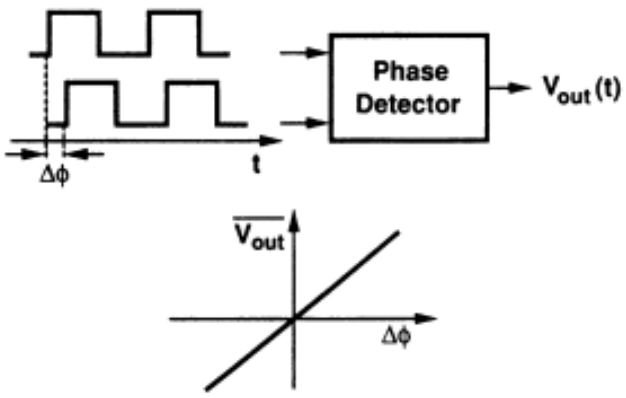


Figure 2.1: An ideal phase detector characteristic [1]. $\Delta\phi$ is the phase error generated by the phase detector. V_{out} is the output voltage of the phase detector.

2.2 Phase-Locked Loop

2.2.1 Basic structure

A phase-locked loop is a feedback system. The basic PLL structure is depicted in Figure 2.1. As seen, the basic PLL includes a phase detector, low pass filter and a VCO [1].

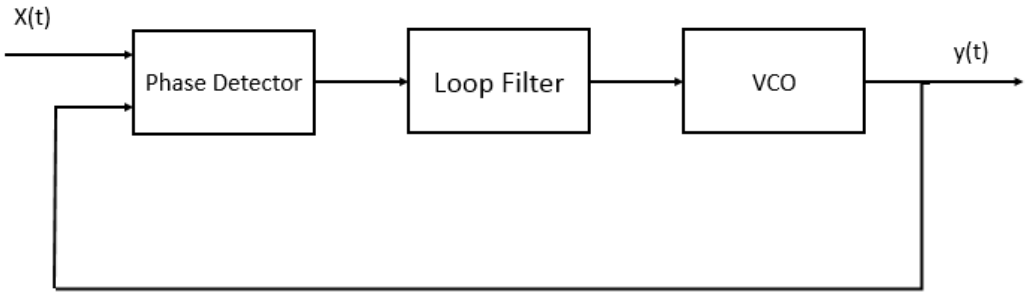


Figure 2.2: Basic PLL structure. X(t) is the reference signal and y(t) is the output signal of the PLL.

The operation of the PLL in locked condition can be summarized as: Generation of an output signal whose dc value is proportional to $\Delta\phi$ by phase detector. Then, the high-frequency components are concealed by the low-pass filter, allowing the dc value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency and with a phase difference equal to $\Delta\phi$. Eventually, the LPF generates the proper control voltage for the VCO.

2.2.2 Loop dynamics

Usually, a linear approximation is done in PLL design. Since, the PLL has a non-linear behaviour [1]. In Figure 2.3, a linear model of the PLL is depicted.

According to the Figure 2.3, The open loop transfer function can be given as

$$H_O(s) = K_{PD}G_{LPF}(s)\frac{K_{VCO}}{s} \tag{2.5}$$

In addition, the closed loop transfer function H(s) is given by the following equations

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PD}K_{VCO}G_{LPF}(s)}{s + K_{PD}K_{VCO}G_{LPF}(s)} \tag{2.6}$$

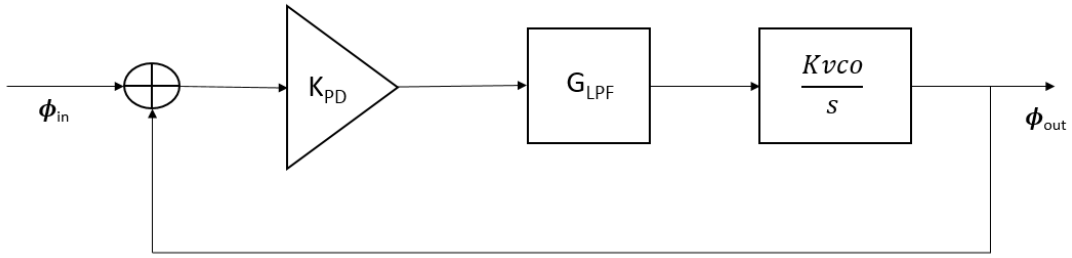


Figure 2.3: PLL linear model. $K_{PD}, G_{LPF}(s), \frac{K_{VCO}}{s}$ denote the phase detector, loop filter, and VCO transfer functions, respectively.

The transfer function of the simplest low pass filter is as follows

$$G_{LPF}(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \tag{2.7}$$

Consequently, by replacing the $G_{LPF}(s)$ in 2.6 one obtains

$$H(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} \tag{2.8}$$

or

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.9}$$

where ω_n is the natural frequency and ζ, the damping factor of the system as defined below

$$\omega_n = \sqrt{\omega_{LPF}K} \tag{2.10}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}} \tag{2.11}$$

In the above expressions, $K = K_{PD}K_{VCO}$ is the loop gain of the closed loop system.

2.3 Charge pump PLL

The CPPLL is the preferred PLL type in this work. The CPPLL is reviewed in chapter 1, according to the Figure 1.6 , if a phase error of $\Phi_e = \Phi_{in} - \Phi_{vco}$ occurs in the loop, an average charge pump current of $\frac{I_{CP}}{2\pi}$ is generated. The control voltage of the VCO can be changed as given below in equation 2.12

$$V_{ctrl}(s) = \frac{I\phi_e}{2\pi}(R + \frac{1}{C_P s}) \tag{2.12}$$

Therefore, the closed loop transfer function can be calculated as follows:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}\frac{K_{VCO}}{N}R_P s + \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{N}} \tag{2.13}$$

Based on the above equation, ω_n and ζ are obtained as follows:

$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{N}} \tag{2.14}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi N}} \tag{2.15}$$

2.4 PLL components

2.4.1 Voltage Controlled Oscillator

One of the most important blocks of PLL is VCO. The out of band phase noise performance is determined by VCO. Both ring oscillators and LC oscillators are commonly used in the GHz range applications. Low phase noise and low power consumption made LC oscillators more attractive than the ring oscillators. LC oscillator also has different types such as Colpitts and Hartley. The Colpitts Oscillator is an LC Oscillator circuit identified by a tapped capacitor configuration. It is commonly used in high

frequency communication applications due to low phase noise and the ability of oscillation at high frequencies. Less chip area demand of Colpitts oscillator than most of the other passive device oscillators made it an attractive component in semiconductor design [28].

2.4.1.1 General Considerations

Most RF oscillators studied are feedback circuits. Figure 2.4 shows a simple feedback system with the following transfer function:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \tag{2.16}$$

where H(s), is the open loop gain of the given feedback system.

A self sustaining mechanism can occur at frequency of s_0 if H(s_0)=+1 and the oscillation amplitude remains constant if s_0 is purely imaginary, H(s_0=jω_0)=+1. Therefore, to have steady oscillation, two conditions must be satisfied simultaneously at ω_0 :

(1) |H(jω_0)|=1

(2) <H(jω_0)=0 (or 180^0 if the dc feedback is negative)

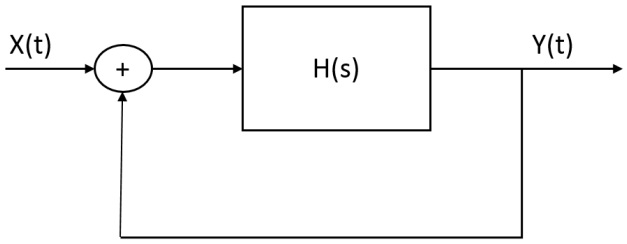


Figure 2.4: Oscillator feedback system. H(s) is the open loop transfer function, x(t) and y(t) denote the input and output of the system, respectively.

These conditions are called Barkhausens criteria [2]. According to these conditions, any feedback system oscillates in case that both loop gain and phase shift are chosen properly. In most RF oscillators, however a frequency selective network (LC tank) is placed in the loop path to stabilize the frequency, this frequency selective network is called "resonator".

2.4.1.2 Basic LC Oscillator Topologies

Only one active device can be seen in most of the discrete RF oscillators not only to reduce the noise but also to lower the costs. According to the feedback model of oscillators shown in Figure 2.4 (a), it is assumed that a one transistor LC oscillator may consist of an LC tank at the collector of a bipolar transistor and the feedback signal imposed to the base or emitter as seen in Figure 2.5 [2].

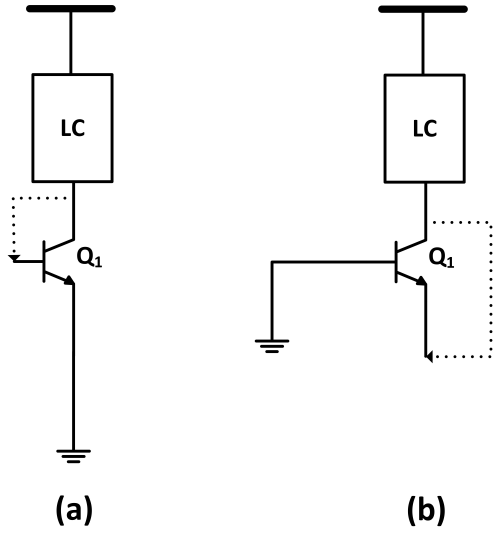


Figure 2.5: (a) Collector to base feedback (b) Collector to emitter feedback [2].

Applying the tanks with capacitive or inductive dividers makes passive impedance transformation as seen in Figure 2.6 (a) and (b), resulted in circuits named as Colpitts and Hartley oscillators, respectively.

The Colpitts oscillator is mostly preferred to Hartley oscillator since it consists of one inductor. However, both types of oscillators can produce only single ended output.

2.4.1.3 Voltage-Controlled Oscillators

Most of the RF oscillators are in need of an adjustable frequency. In Voltage Controlled Oscillator (VCO) the output frequency is changed by change of the input voltage. The essential question that happens here is that, how the frequency can be varied?

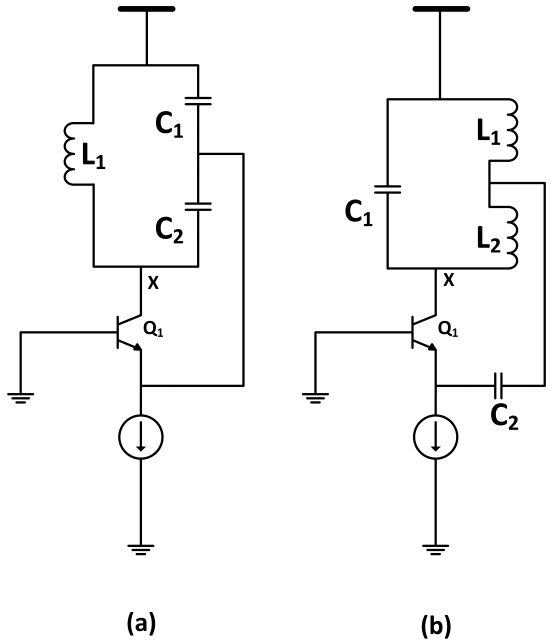


Figure 2.6: LC oscillators. (a) Colpitts (b) Hartley [2].

In LC implementations part of the LC tank, the capacitance is generated by means of a reverse-biased diode (varactor). Therefore, the resonance frequency can be controlled by means of the dc voltage across the junction.Two tank structures including a varactor diode are depicted in Figure 2.7.

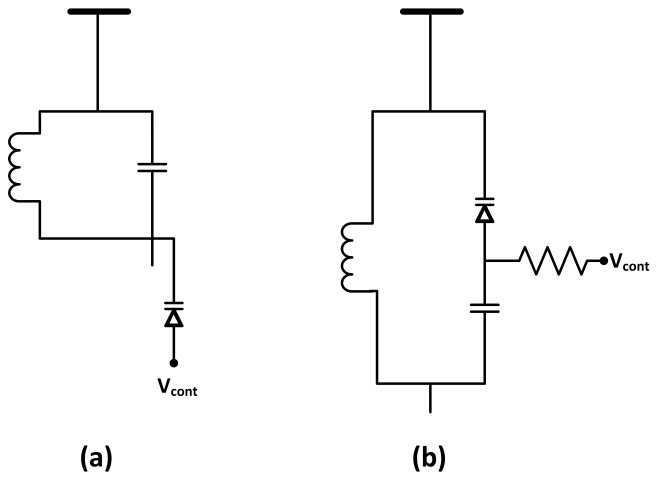


Figure 2.7: Varactor diode added tanks [2]

2.4.2 Phase frequency detector

The PFD role in PLL frequency synthesizer is defined as the detection of the phase and frequency differences of the reference clock and the internal VCO clock. As soon as the synthesizer is activated, an unlocked state happened if the divided VCO output is irrelevant that of the reference. An appropriate output signal is produced by the PFD according to the phase relationships of the input signals that means one leads or lags the other. The phase difference or phase error produced by the PFD is altered to a DC control voltage of the VCO leads to a signal with the desired frequency throughout the charge pump and low pass loop filter. Various types of PFDs included basic PFD, Hogg PFD and Alexander PFD are studied in [29]. The CMOS types of PFDs are studied as conventional PFD in [30, 31], Modified Precharged Type PFD (MPTPFD), provides better speed performance rather than the conventional PFD in [4, 30, 32]. In addition, the Falling-Edge PFD (FE-PFD) with a simple structure than the MPTPFD is studied in [30]. A pass transistor DFF PFD and a latch-based PFD are proposed in [3]. In this research, we mostly used basic PFD [29,33] and the latch-based PFD [3] is used and implemented.

2.4.2.1 Basic PFD

The phase-frequency detector shown in Figure 2.8 is the most widely preferred architecture in frequency synthesizers. This type of PFD includes two edge-triggered D-Flip Flops and one AND gate leads to two outputs of QA and QB, or UP and DOWN, respectively [29, 33]. In this circuit, when QA=QB=0, if A goes high makes QA=1 while B is high, the reset of both flip flops is activated resulted in QA=QB=1.

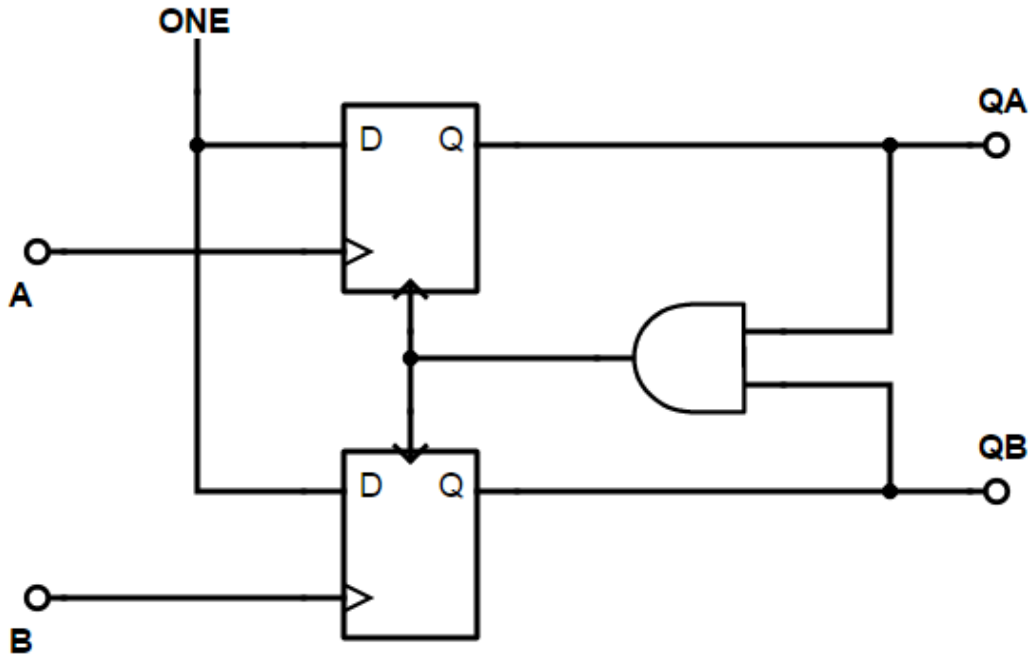


Figure 2.8: Basic PFD. A is the clk of the upper D flip-flop. B the clk of the lower D flip-flop. QA and QB are the outputs of the PFD. ONE the data of the D flip flops.

2.4.2.2 Pass-transistor DFF PFD

A pass transistor DFF PFD is proposed in [3]. The circuitry of this type of PFD which is similar to a dynamic two-phase master-slave pass transistor flip flop is depicted in Figure 2.9. The performance of the proposed PFD can be summarized as, when the outputs are high the slave asynchronously reseted but the master reseted synchronously. Consequently, in case of the slave latch is transparent the reset is allowed. In case of master latch reseted when it is transparent, a significant short-circuit current generated, resulted in enormous power consumption.

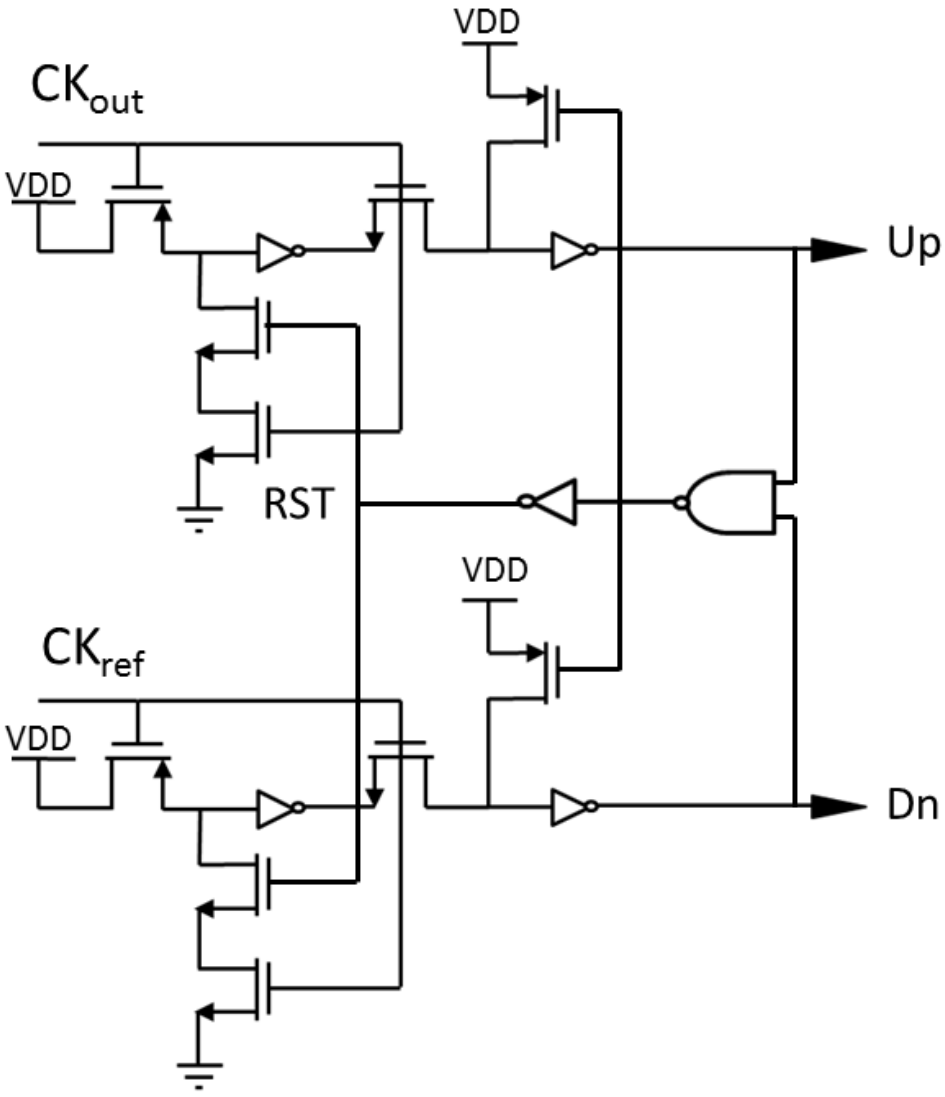


Figure 2.9: Pass-transistor DFF PFD, including the inverters, NAND gate and CMOS transistors [3].

2.4.3 Charge pump and loop filter

PFD driven charge pump produces current pulses that charge or discharge the loop filter capacitor. Figure 2.10 shows a simple charge pump structure. Effective charge pump requirements can be summarized as [34]:

1-Charge/discharge current should be equal at any output node.

2-Charge injection and feed-through (due to switching) should be minimized at the output.

3-Charge sharing between output node and any floating node should be minimized.

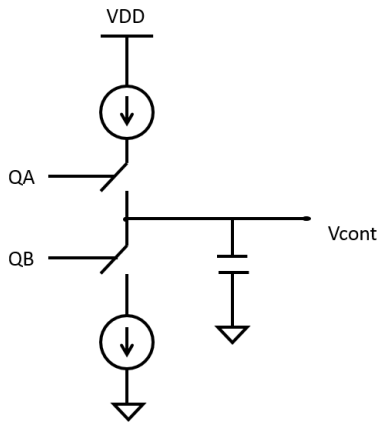


Figure 2.10: Basic charge Pump.

Current mismatching is defined as the magnitude difference of charging and discharging currents [35]. Single-ended charge pumps, charge pump with an active amplifier and charge pump with current steering switches are studied in [4] and [34]. In addition, the differential charge pumps are presented in [36, 37] and [38]. In this thesis, we try to develop a charge pump as the basic charge pump shown in Figure 2.10 using CMOS transistors as single-ended charge pumps.

2.4.3.1 Single-Ended Charge Pumps

A single ended charge pump is most commonly preferred since it leads to lower power consumption and autonomous operation with no additional loop filter. In Figure 2.11 a simple implementation of the single-ended charge pump and its variations are depicted [4].

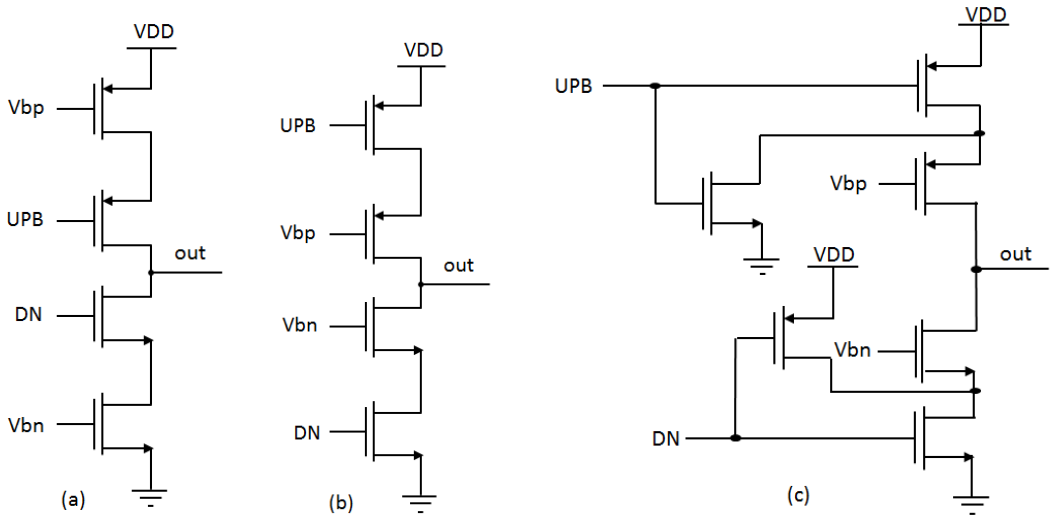


Figure 2.11: Single-ended charge pump diversity [4].

In Figure 2.11 (a), a replica bias circuit from a reference current generates the bias voltages of the V_{bp} and V_{bn} resulted in best matching between I_{UP} and I_{DWN}. The circuit provided in Figure 2.11 (a) has some drawbacks included the charge injection to the output node and charge sharing. Adding a drain to source shorted dummy transistor on each side of the switch transistor or as depicted in Figure 2.11 (b) shifting the switch transistors towards the rails can be a solution to the former problem. Anyhow, for both designs due to the existence of the floating nodes in certain node the charge sharing problem still remains. In Figure 2.11 (c), a so modified circuitry contains charge removal transistors to abolish the charge sharing is offered. The provided circuitry made a large reduction in phase offset. Furthermore, the intrinsic $\frac{1}{f}$ noise decreased remarkably.

2.4.3.2 Loop Filter

The stability characteristics and the dynamic behaviour of the PLL depend on the loop filter. Loop filter sets the closed loop bandwidth, a key design parameter for noise suppression, as lower bandwidth suppresses the input noise and higher bandwidth suppresses VCO noise. The noise characteristics of a PLL also depends on the loop filter as it determines the closed loop bandwidth. Smaller bandwidth results in longer lock time but lower jitter; whereas larger bandwidth results in faster lock with worse jitter performance. The fact that input noise is low-pass filtered and the VCO noise is high-pass filtered through the loop to the output also makes the loop bandwidth a very important design parameter [4].

There are two types of loop filters, active and passive. A passive low-pass filter is the general approach for high speed PLL implementation [39]. Passive filter has the advantages of reduced noise and lower circuit complexity. They are formed by only R (resistor), C (capacitor) elements, and often used as the charge pump loads to generate the control voltage proportional to the phase error. Figure 2.12 shows the schematic of a lead-lag passive filter. The reason of calling lead-lag is that the pole placed at a lower frequency than the zero. The transfer function of this filter type is given as

$$H(s) = \frac{R_2 + \frac{1}{sC}}{R_1 + R_2 + \frac{1}{sC}} = \frac{sCR_2 + 1}{sC(R_1 + R_2) + 1} \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{2.17}$$

Where τ_1=R_1C and τ_2=R_2C

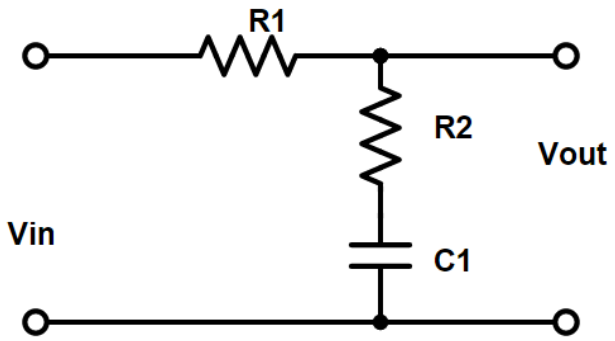


Figure 2.12: The passive lag filter schematic

2.4.4 Frequency divider

The frequency divider chain of the PLL frequency synthesizer plays an important role in modern integrated transceivers operating at microwave frequencies. When the VCO output frequency is in the order of several GHz, implementing the frequency division at such high frequencies is a challenge. Different approaches can be attempted depending on the frequency that needs to be divided. In other words, the frequency divider role is production of a clock signal runs many times faster than the reference clock [40].

Design of a digital counter included a digital logic resetting the counter after a number of input clock cycles equal to the division ratio have been counted is the simplest approach to implement a clock frequency division. Limited maximum frequency of operation due to the digital logic with which the counter is implemented builds up the most critic disadvantage of this solution. Such kind of frequency divider generally performs up to few GHz (typically no more than 3-4 GHz). However, low power consumption, and the possibility of being programmable by dynamically changing the resetting logic (and thus the division ratio) contributes to the most important advantages of this type of frequency divider.

Applying a purely analog solution is usually preferred in case of higher frequency division [41]. D-flip flops are commonly used as divider. The Yuan-Svensson D-FF and the Huang-Rogenmoser D-FF are presented in [39]. In addition, high speed divide-by-two and dual-modulus dividers are introduced [2]. In [41], the multi GHz frequency dividers are addressed.

2.4.4.1 CMOS D-FF

Circuit schematic of the conventional D flip-flop is as shown in figure 2.13. When clk=0, inverted D get to the node X. Node Y charged up to the VDD and M7 and M8 get off. Therefore, when the clk is in low state, the input of the final inverter holds its previous value and the output Q is stable. When the clk=1, X=1, node Y is discharged. The third inverter M8-M9 is on during the high phase and the node value of Y is passed to the output Q.

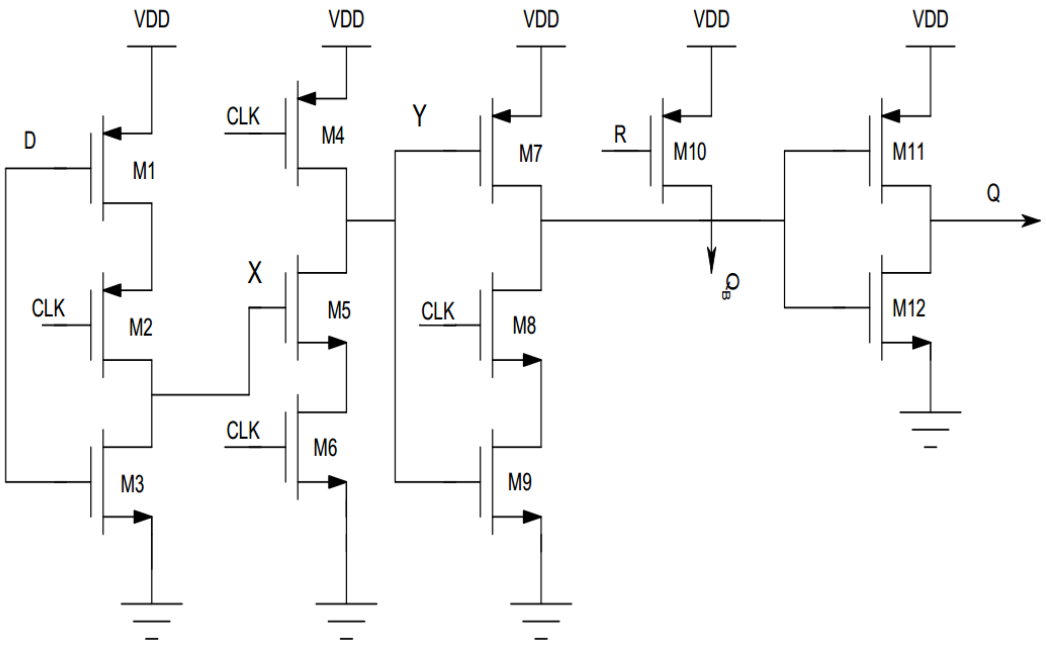


Figure 2.13: Conventional D flip-flop

CHAPTER 3

PLL BLOCKS DESIGN AND ANALYSIS

In this chapter, the design of the constructing blocks of the PLL will be presented. First, the VCO design will be discussed. Then, the frequency divider design and implementation will be introduced. The phase frequency detector design will be offered next. Finally, the charge pump and loop filter design will be presented. The simulations in this chapter are implemented in Advanced Designed System (ADS).

3.1 The VCO design proposed in this thesis study

In this work a novel VCO structure is offered which included a single High Electron Mobility (HEMT) transistor. The proposed circuitry is depicted in Figure 3.1. The proposed structure, is a gate grounding Colpitts oscillator. As discussed before, the Colpitts oscillator has an intapped capacitance between the drain and source of the transistor used. In this study, a varactor is used between the drain and the source of the HEMT transistor. The reason of selecting this structure, is obtaining low phase noise in PLL design. Since there is only one transistor, the noise will be reduced. In addition, the circuitry is simpler than the LC cross coupled structures which are commonly used in the VCO design.

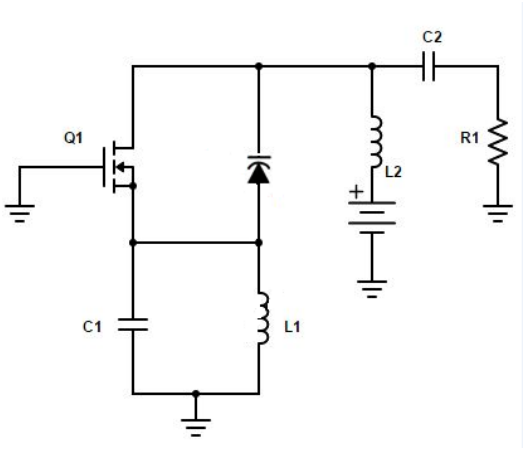


Figure 3.1: Schematic of the proposed VCO.

3.1.1 HEMT transistor

The HEMT is a form of field effect transistor, FET, that is used to provide very high levels of performance at microwave frequencies. The HEMT offers a combination of low noise figure combined with the ability to operate at the very high microwave frequencies. Accordingly, the device is used in areas of RF design where high performance is required at very high RF frequencies. Since the operation frequency of the HMMDI is in the range of a few GHz, HEMT is preferred in the design of VCO. The HEMT transistor biasing is demonstrated in Figure 3.2.

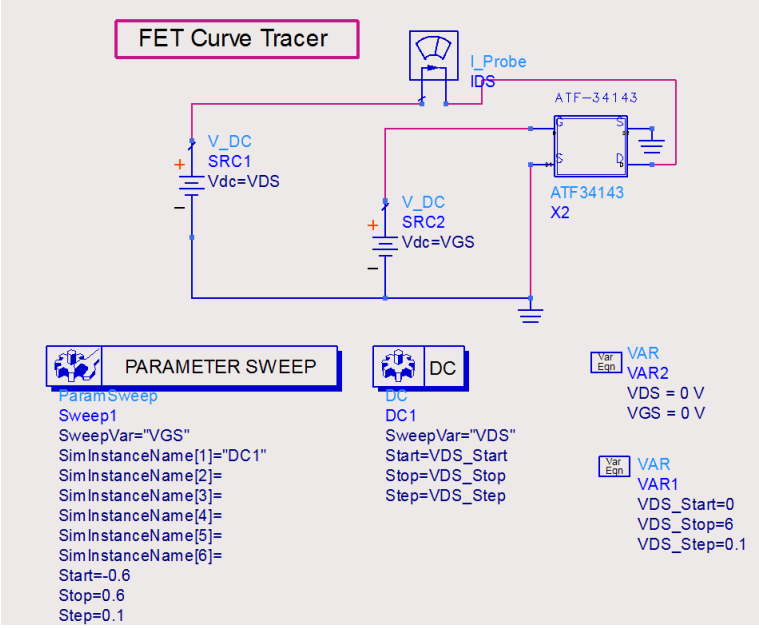


Figure 3.2: Applied HEMT transistor biasing in ADS

According to Figure 3.2, the biasing simulation of the aimed transistor is shown. The gate-source voltage VGS is the sweep parameter. DC simulation is applied and the drain-source voltage is defined as the variable in that simulation. The drain-source current IDS versus VDS for different VGS values is shown in Figure 3.3.

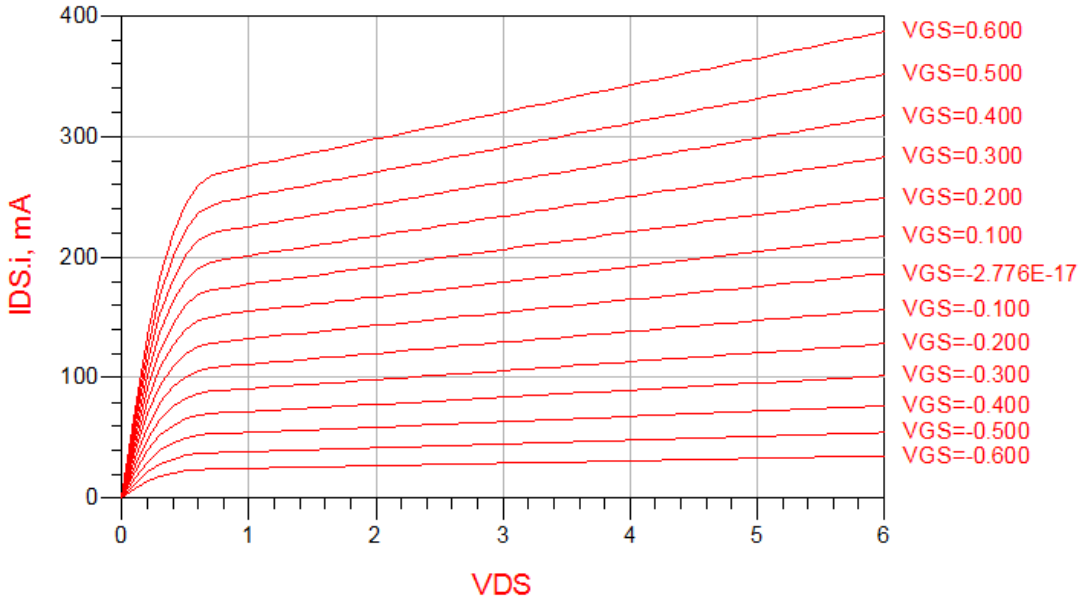


Figure 3.3: HEMT I-V characteristics in ADS

As it is seen in Figure 3.4, the ATF34143 model of HEMT transistors is preferred. It is a dual source transistor which is actually a packaged transistor. Inside the package, a FET transistor is used with the Statz model. In Statz model, the parameters of the FET transistor especially, the parasitic capacitances are given.

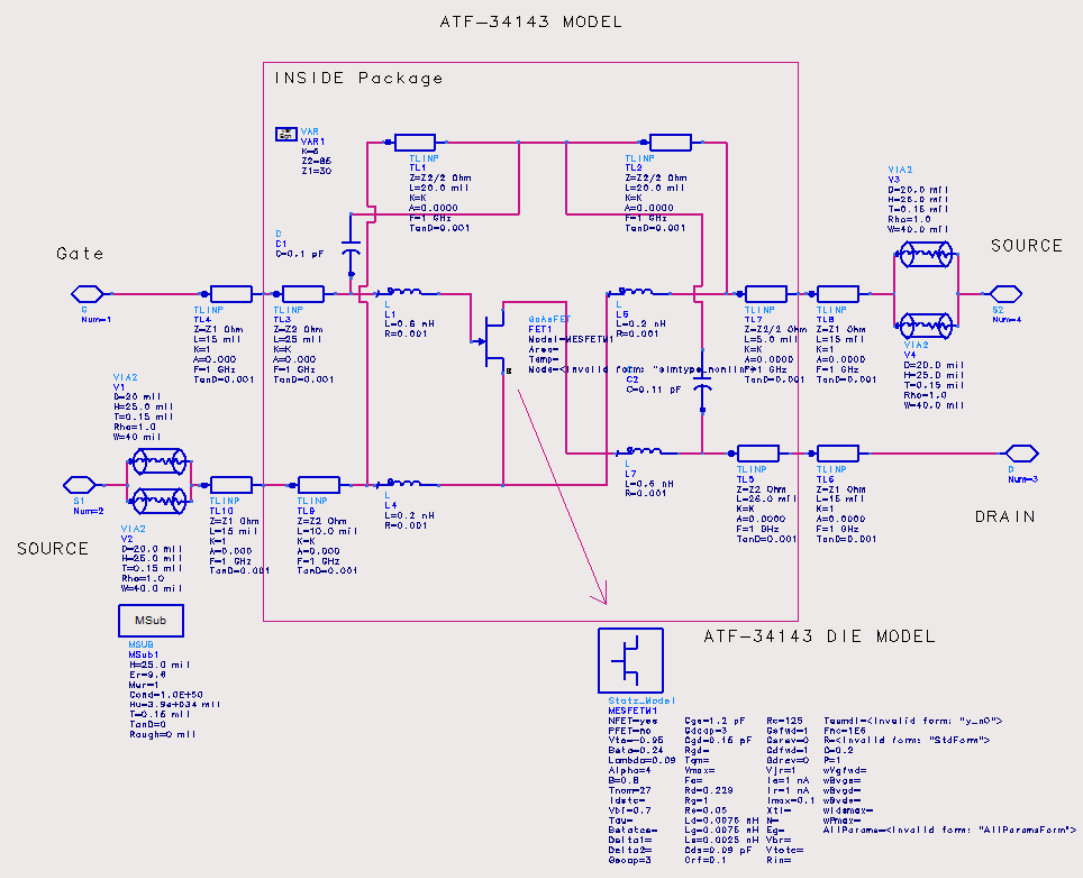


Figure 3.4: Applied HEMT circuitry

In next the step of the VCO design the Colpitts oscillator given in Figure 3.1 is developed. To do this, first of all a DC simulation is required. Therefore, as seen in Figure 3.5, a DC simulation is applied to examine if the proposed circuitry satisfies the startup conditions for oscillation [33]. The simulation results of the circuitry offered in Figure 3.5, is depicted in Figure 3.6.

According to Figure 3.6, it is obvious that the loop gain is larger than 1 and the phase is 0. Therefore, the circuit is ready to oscillate, so the Harmonic Balance (HB) and transient simulations are applied to analyze the performance of the proposed VCO.

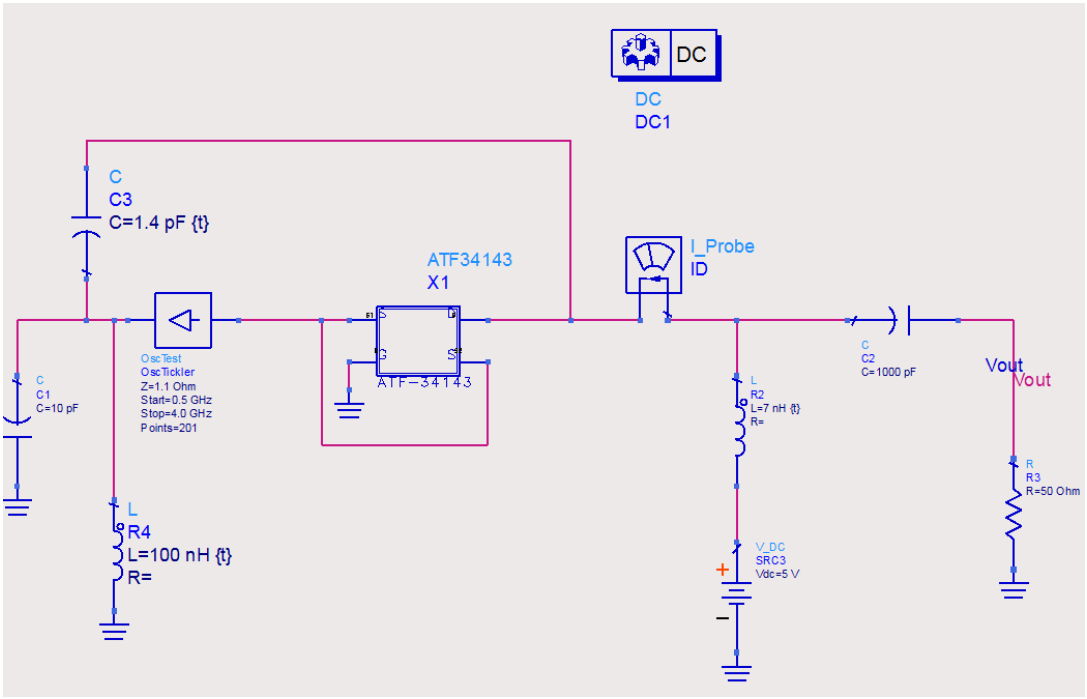


Figure 3.5: ADS schematic of proposed VCO

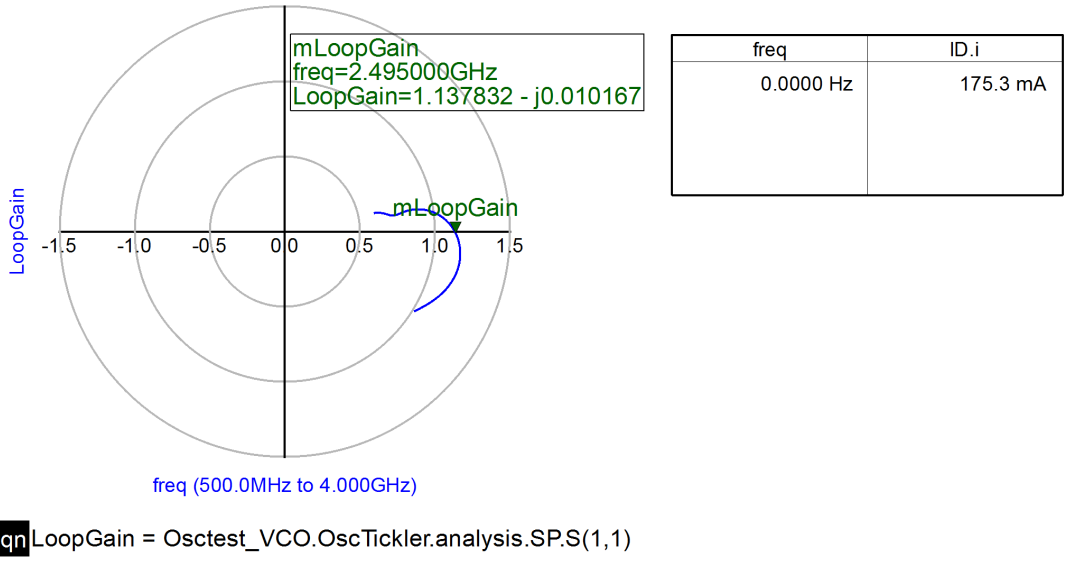


Figure 3.6: Simulation results that satisfy the startup conditions

In Figure 3.7, the proposed VCO given in 3.1, is implemented in ADS and HB and transient simulations are applied. In addition, the HB NOISE CONTROLLER, seen in the circuitry given in 3.7 is used for phase noise simulation analysis. In this step, we use a capacitance between the drain and source of the HEMT, and to have the output frequency variable, the capacitance value is tuned.

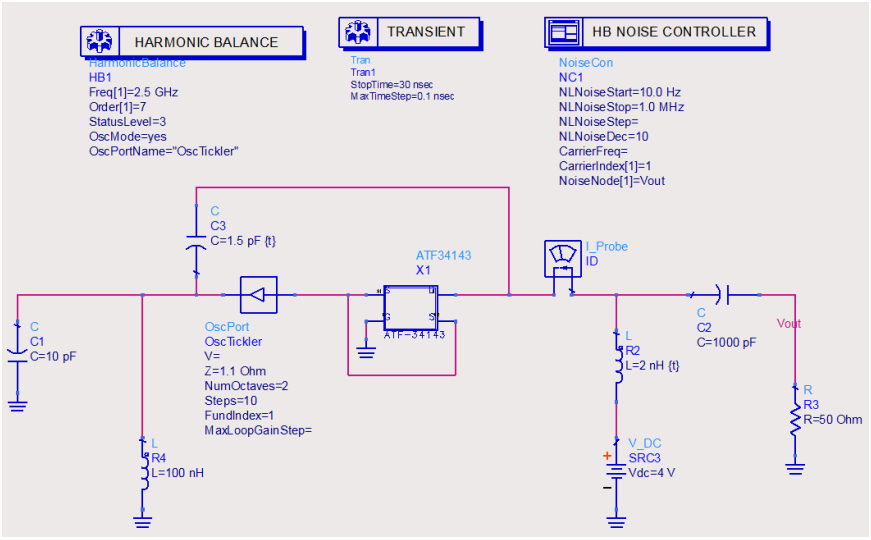


Figure 3.7: Schematic circuitry of the final VCO

The phase noise performance of the proposed VCO can be figured in Figure 3.8.

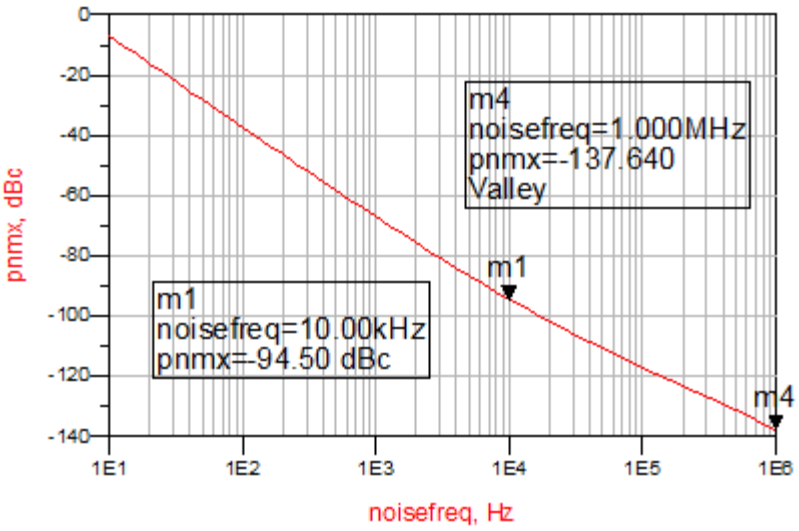


Figure 3.8: Phase noise performance of the proposed VCO

The proposed VCO provided a phase noise of about -137.64 dBc/Hz at 1 MHz offset. Figure 3.9 illustrates the other simulation results of the VCO seen in Figure 3.7.

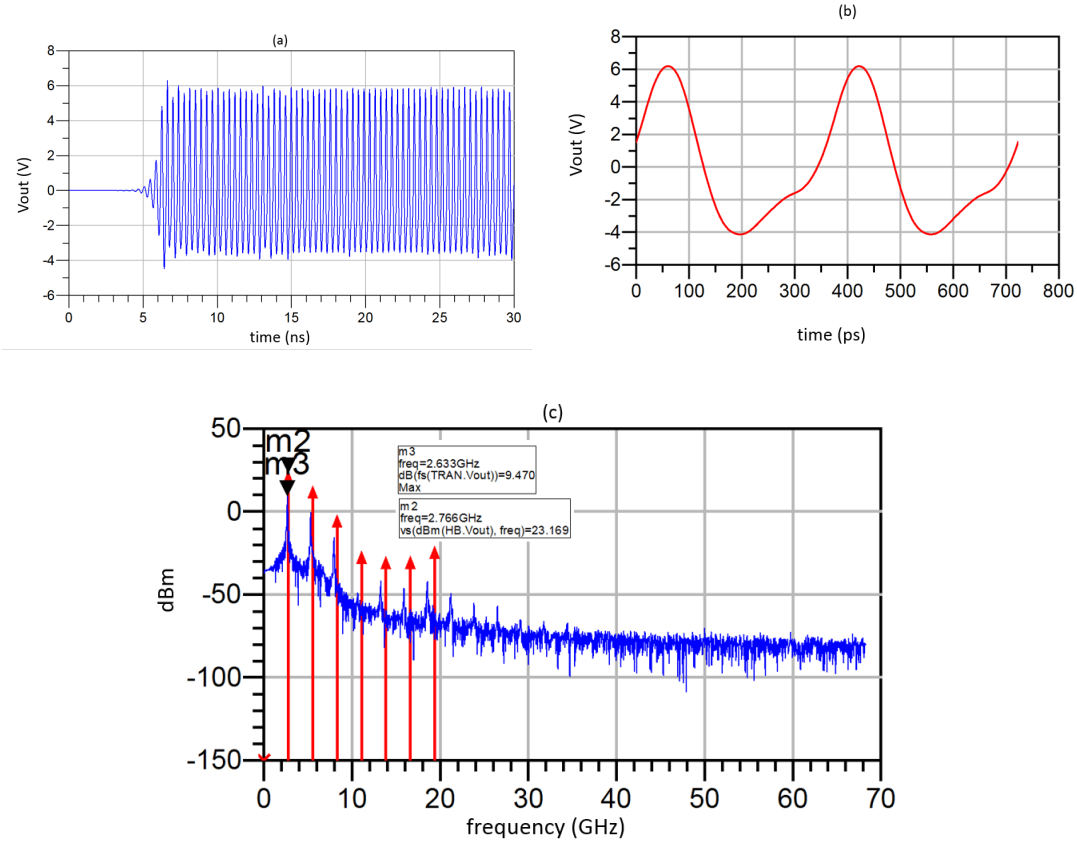


Figure 3.9: Simulation results of final proposed VCO. (a) the transient simulation results that gives the response of the circuit at the time domain (b) Inverse Fourier transform of the HB simulation results (c) the HB simulation results along side the Fourier transform of the transient response

3.1.2 Varactor

VCO design simulations are made in ADS enviroment. In these simulations capacitors and inductors are tunable. This is not possible in practice. Accordingly, instead of using tuned capacitor it is preferred to use a varactor. In this case, the capacitance value changes by varying the applied voltage. Varactor is a component that has different capacitance values under different DC biases. It is responsible to provide the required bandwidth for the VCO. In this work SMV1283 is preferred whose circuitry is depicted in Figure 3.10.

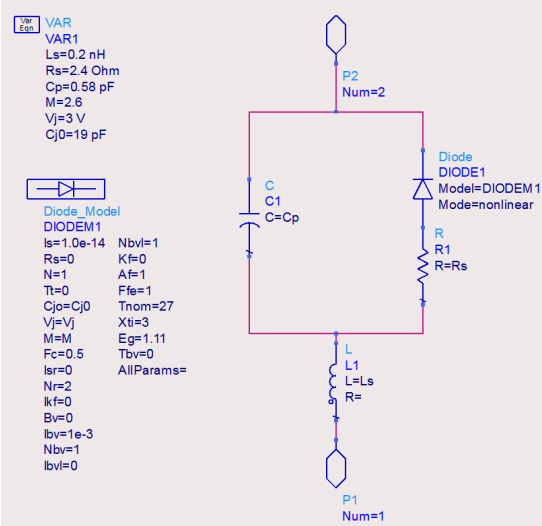


Figure 3.10: Used varactor circuitry in ADS

To generate the varactor model in ADS, using the parameters values in datasheet and adding that values to the diode model in general circuitry of a varactor in ADS, the model is defined. In Figure 3.11, the biasing of the given varactor is illustrated. In addition, C-V characteristics of the applied varactor is given in Figure 3.12. In Figure 3.11, the s-parameters simulation is applied, where the Vbias value is swept as seen in the parameter sweep section.

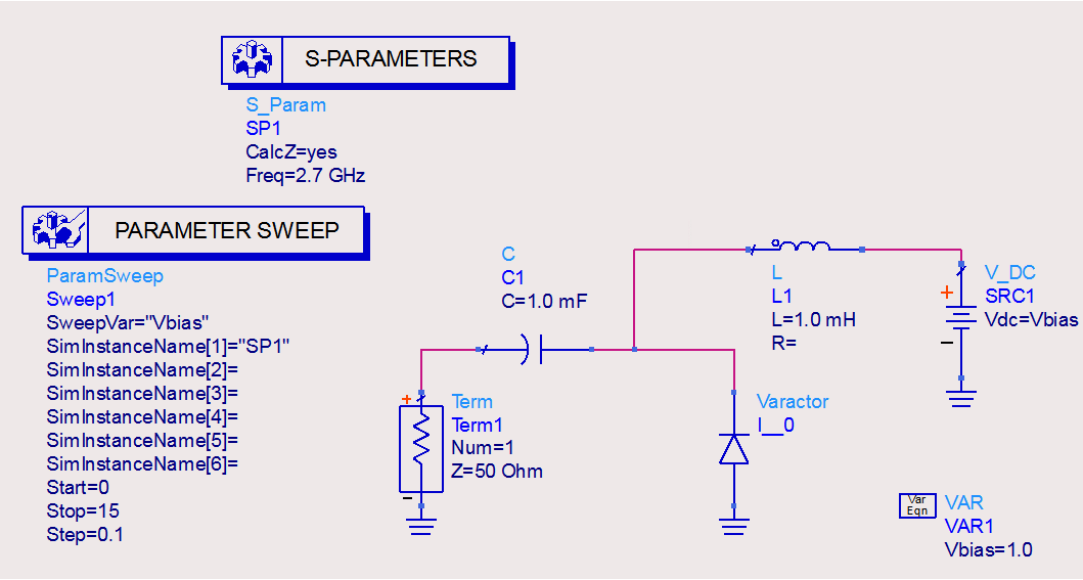
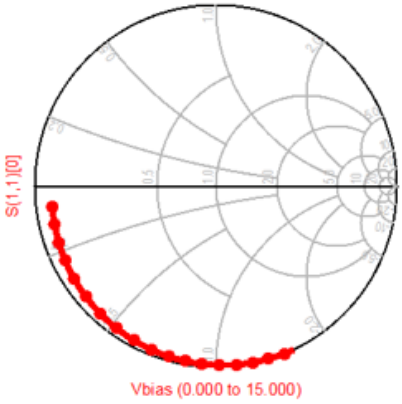


Figure 3.11: The varactor biasing circuitry as implemented using ADS



(a)

Zin = R +1/(j*2*pi*freq*C),

so -imag(Zin) = 1/(2*pi*freq*C), or

C = -1/(2*pi*freq*imag(Zin))

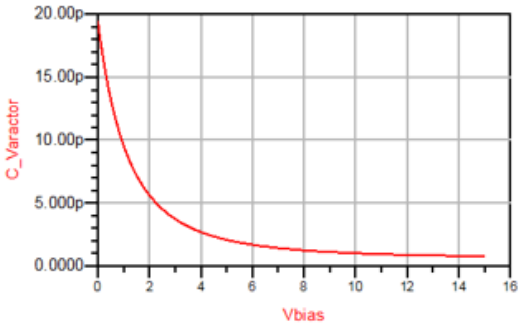
Eqn C_Varactor=-1/(2*pi*freq[0,0]*imag(Z11[0]))

Vbias	C_Varactor
0.0000	19.39 p
100.0 m	17.88 p
200.0 m	16.52 p
300.0 m	15.31 p
400.0 m	14.22 p
500.0 m	13.24 p
600.0 m	12.35 p
700.0 m	11.55 p
800.0 m	10.82 p
900.0 m	10.15 p
1000. m	9.548 p
1.100	8.994 p
1.200	8.485 p
1.300	8.018 p

(b)

Vbias	Z(1,1)[0]
0.000	2.260 - j3.039
0.100	2.248 - j3.297
0.200	2.236 - j3.568
0.300	2.223 - j3.850
0.400	2.209 - j4.145
0.500	2.195 - j4.452
0.600	2.181 - j4.772
0.700	2.166 - j5.104
0.800	2.151 - j5.448
0.900	2.135 - j5.805
1.000	2.118 - j6.174
1.100	2.101 - j6.554
1.200	2.084 - j6.947
1.300	2.066 - j7.352
1.400	2.048 - j7.768
1.500	2.029 - j8.196
1.600	2.010 - j8.635
1.700	1.991 - j9.086
1.800	1.971 - j9.548
1.900	1.951 - j10.020

(c)



(d)

Figure 3.12: Simulation results of given varactor (a) the Vbias effect on varactor capacitance is seen on Smith chart for 15 values of the Vbias, they have negative imaginary values (b) Vbias versus varactor capacitance equations and the obtained values are shown in a table (c) the Smith chart shown in (a) values of Vbias versus varactor capacitance (d) varactor capacitance versus Vbias result

According to the simulation results shown in Figure 3.12 (d), while increasing the Vbias value the varactor capacitance is decreased, therefore the resonance frequency increases as shown in the following frequency expression:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

When the varactor model is employed in the VCO circuit with tuned capacitor, the resulted circuitry is given in Figure 3.13. In this circuit L1, C3 and L are used for the biasing the varactor. The inductors will short circuit in DC and capacitances will open circuit. Therefore, the DC, will move over the varactor and does not allow the current to flow in to the drain of the transistor.3.13

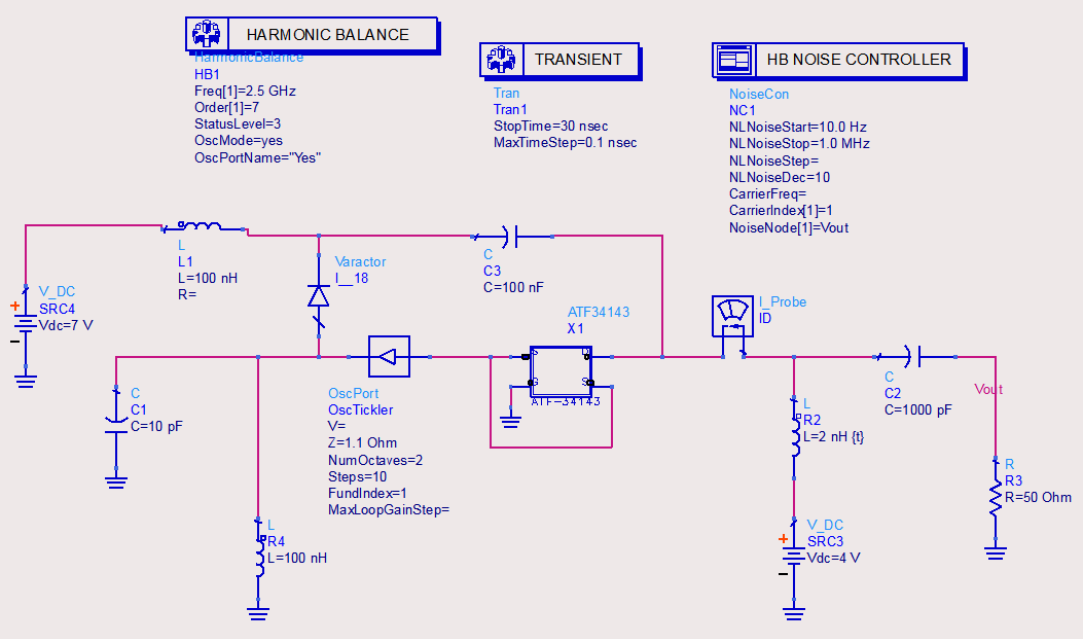


Figure 3.13: The VCO circuit employing a varactor, as applied in ADS.

The simulation results are provided in Figure 3.14. The phase noise performance of the proposed Colpitts VCO with varactor tapped between drain and the source of the HEMT transistor, is shown in Figure 3.15.

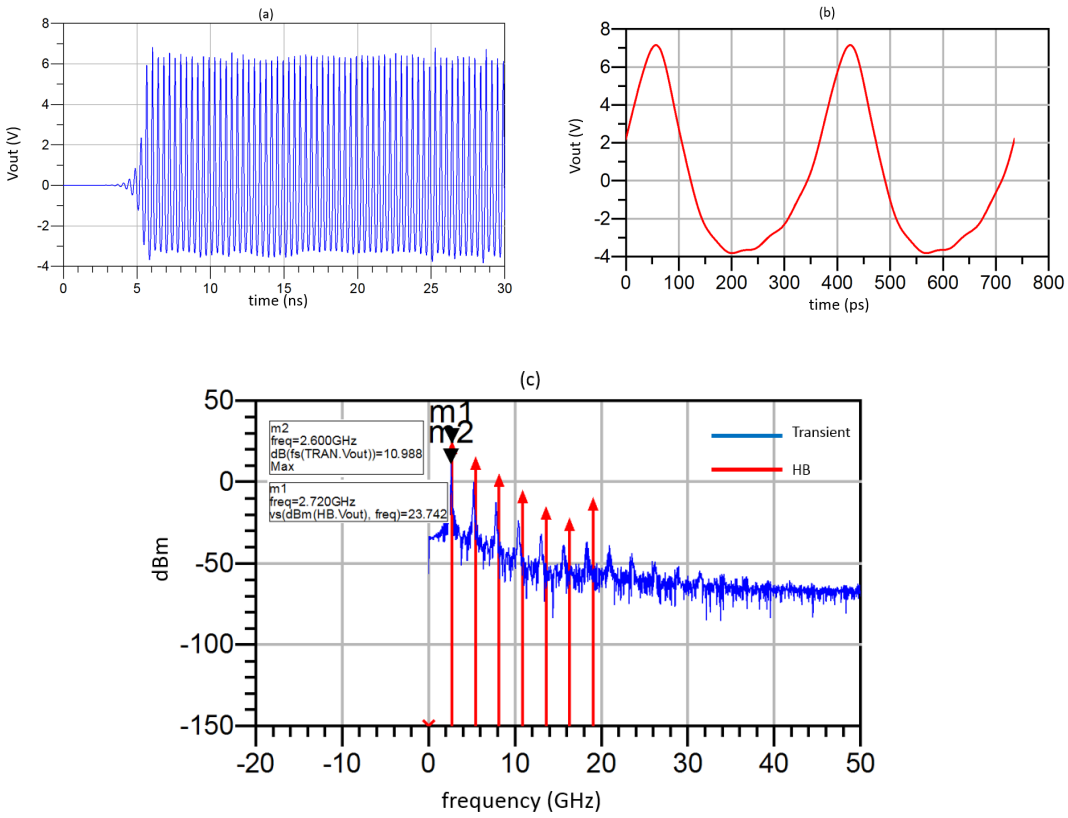


Figure 3.14: Simulation results for Final VCO using varactor (a) the transient simulation results that gives the response of the circuit at the time domain (b) Inverse Fourier transform of the HB simulation results (c) the HB simulation results along side the Fourier transform of the transient response. Accordingly, both of the simulations resulted in approximately 2.7 GHz output frequency

3.2 The Frequency divider design proposed in this thesis study

Due to the high frequency and wide range of operation, the design of the frequency divider requires much attention. A frequency divider is designed such that it is fast enough to operate at the highest frequency, and still be able to operate properly at lower frequency, with the minimum power consumption [39].

The divide-by-2 block is implemented using a simple D-FF. In order to achieve the maximum possible operating frequency, it is necessary to select the appropriate implementation for the D-FF, choosing between the different circuit topologies is available. Standard cells D-FF are usually implemented exploiting a positive feedback memory element, with the additional logic needed for clear, preset, and other func-

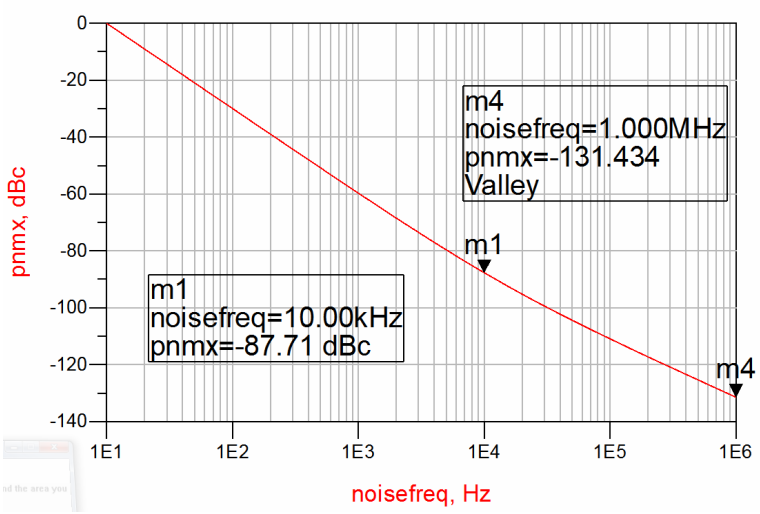


Figure 3.15: Phase noise performance of the proposed VCO inserting varactor.

tionalities that may be desired [41]. Accordingly, we firstly design divide-by-2 using the logic gates in ADS, the schematic of the implemented circuitry is depicted Figure 3.16 and the achieved results are given in Figure 3.17.

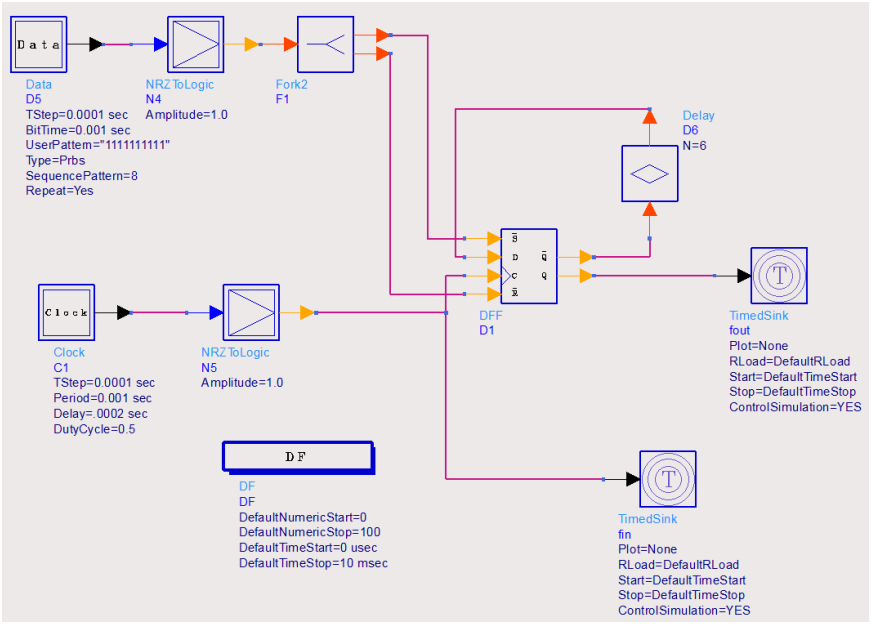


Figure 3.16: Divide-by-2. A single D flip flop is used.

In ADS, to design the frequency divider, using logic gates, Data Followed (DF) is applied. The Clock and Data are used as the inputs of the DFF and to see the results of the logic gate the Time sinks are placed at the node where the results are observed. In consequent divide-by-4 also developed in ADS together with investigation of a si-

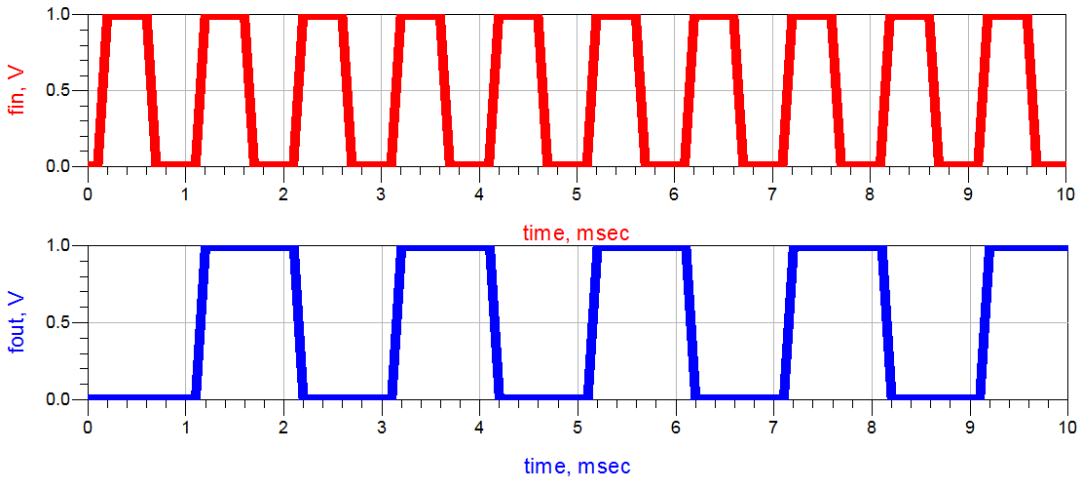


Figure 3.17: Simulation results for Divide-by-2. The upper is the reference signal. The lower is the output signal.

nusoidal input. The developed circuitry is shown in Figure 3.18. As seen in Figure 3.18, the divide-by-4 consists of two DFF and its implementation is as same as the divide-by-2 circuit. The results are depicted in Figure 3.19.

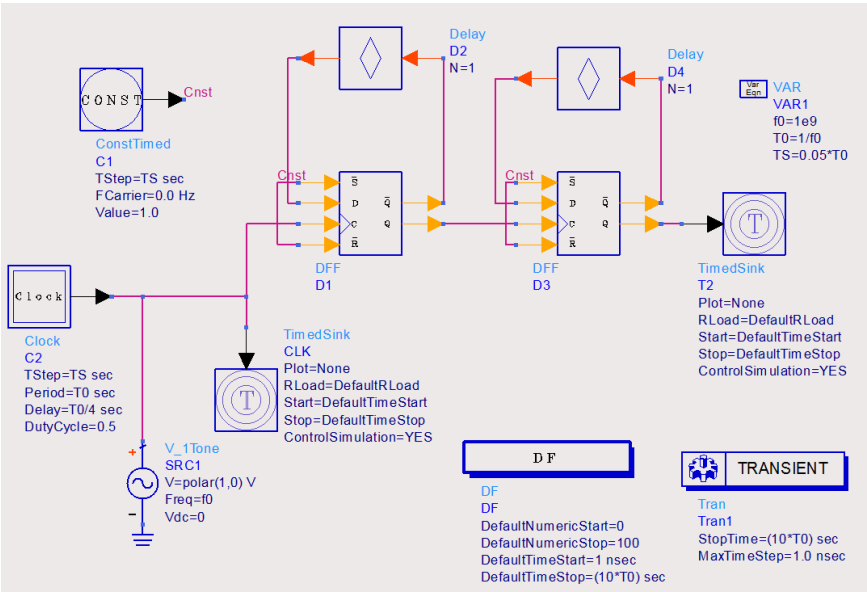


Figure 3.18: Divide-by-4. Two D flip-flops are used.

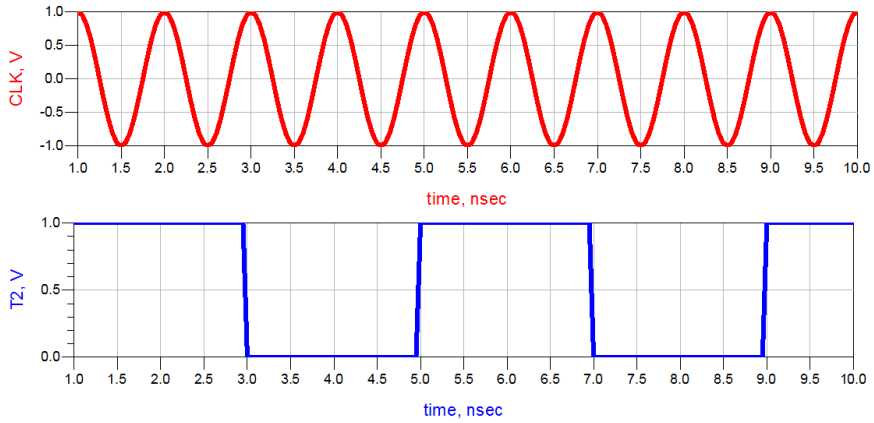


Figure 3.19: Simulation results for Divide-by-4. Upper is the sinusoidal input and the lower relates to the generated output signal.

According to the simulation results demonstrated in Figure 3.19, the sinusoidal input has no effect on the general performance of the circuit. In proceeding step divide-by-16 is also implemented whose schematic and simulation results can be seen in Figure 3.20 and Figure 3.21, respectively.

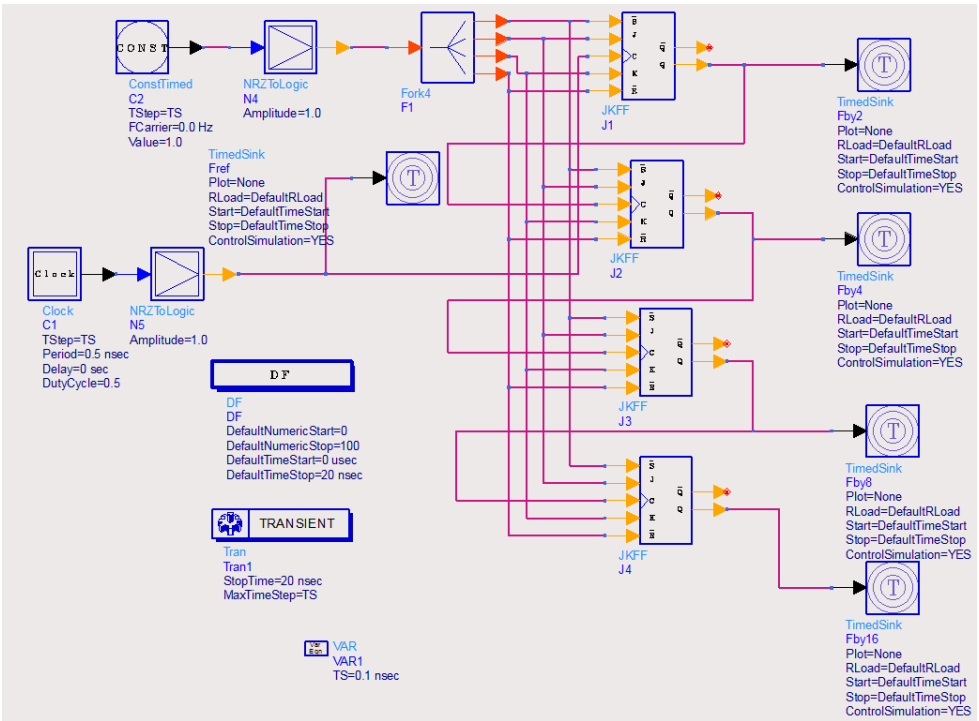


Figure 3.20: Divide-by-16.

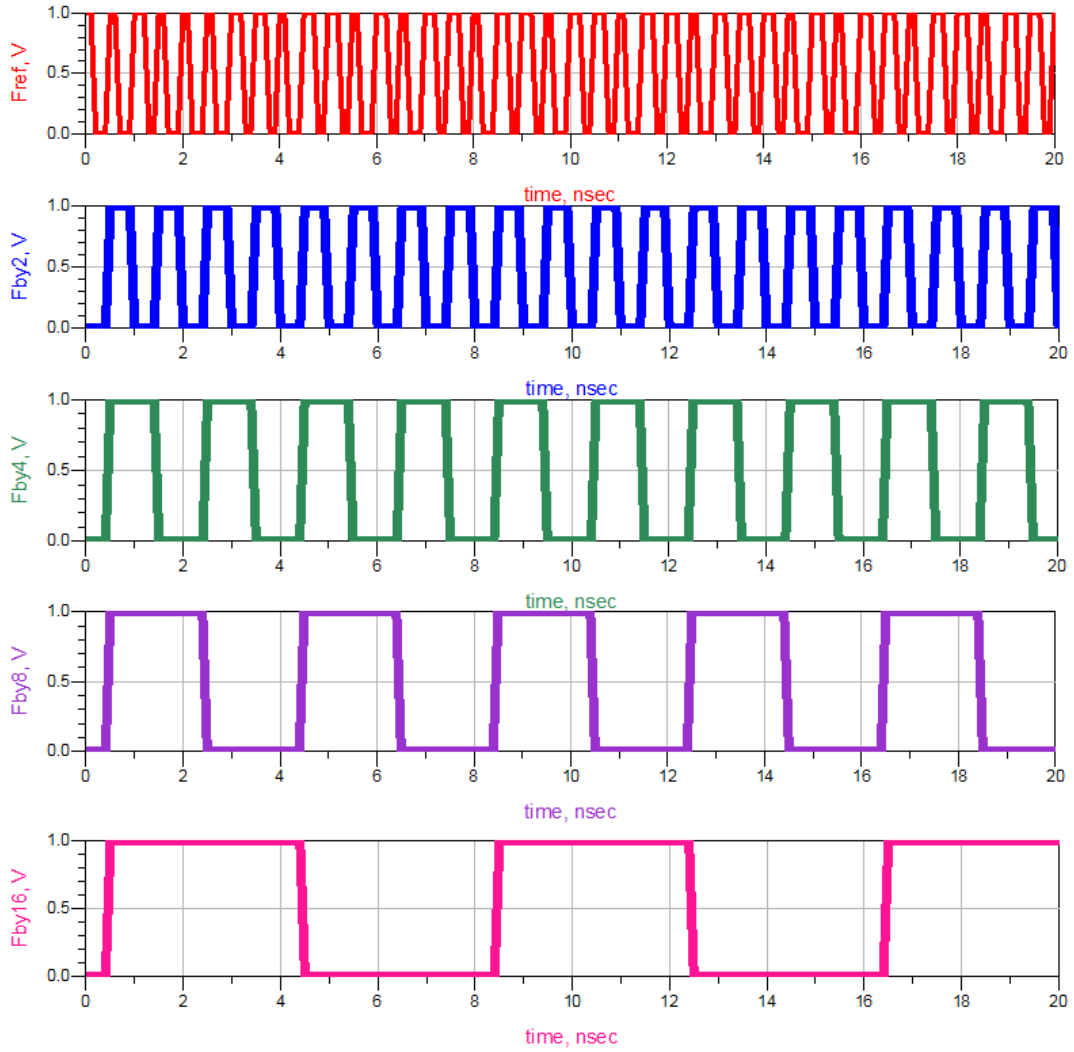


Figure 3.21: Simulation results for Divide-by-16. The reference signal (first row) is divided by two in (second row), the third row shows the output signal that is divided by four, and the fourth row contributes to the divider by 8 and the last row is the divide by 16 output.

In Figure 3.20, it is obvious that to design divide-by-16, four DFF is used. For each D flip-flop a time sink is used at the output that shows the input, divide-by-2, divide-by-4, divide-by-8 and finally, the divide-by-16 output signals in Figure 3.21.

During this work we had noticed that we are in need of the designing the frequency divider in transistor level. Therefore, developing the frequency divider in transistor level is accomplished. At beginning step a NAND gate which is depicted in Figure 3.22 is developed.

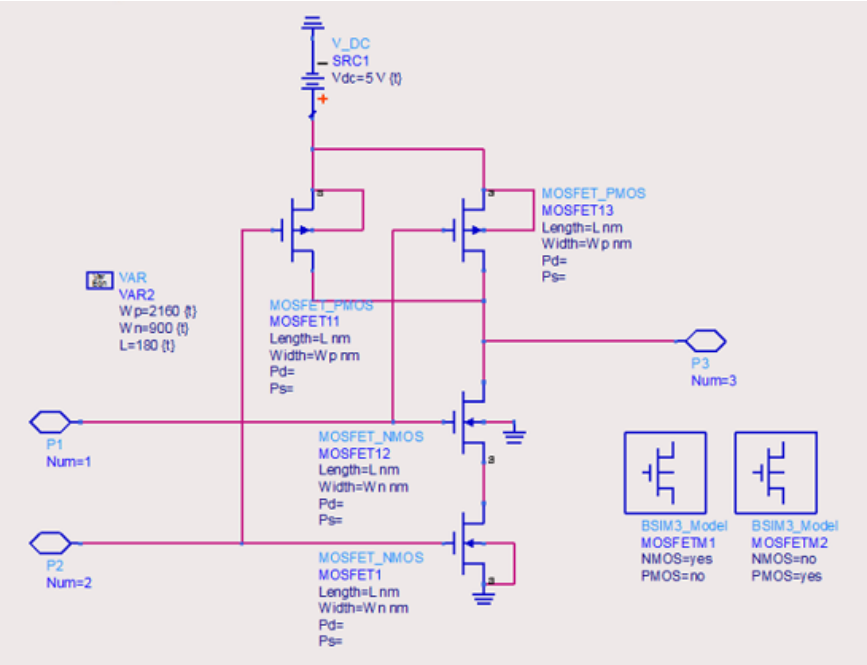


Figure 3.22: Transistor level designed NAND gate.

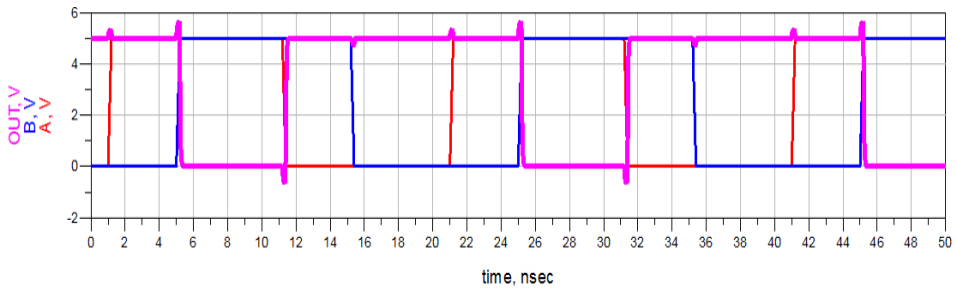


Figure 3.23: Simulation results for transistor level designed NAND gate. The red one is the upper input. The blue is the lower input signal. Pink one relates to the output of the circuit

The achieved results are shown in Figure 3.23. As seen in Figure 3.23, the simulation results presents that when A=B=0 the OUT=1 and when A=B=1, the OUT=0.

In addition to two input NAND gate we were in need of three input NAND gate to develop the DFF. Thus, a three input NAND gate that is depicted in Figure 3.24 is implemented. The results are given in Figure 3.25.

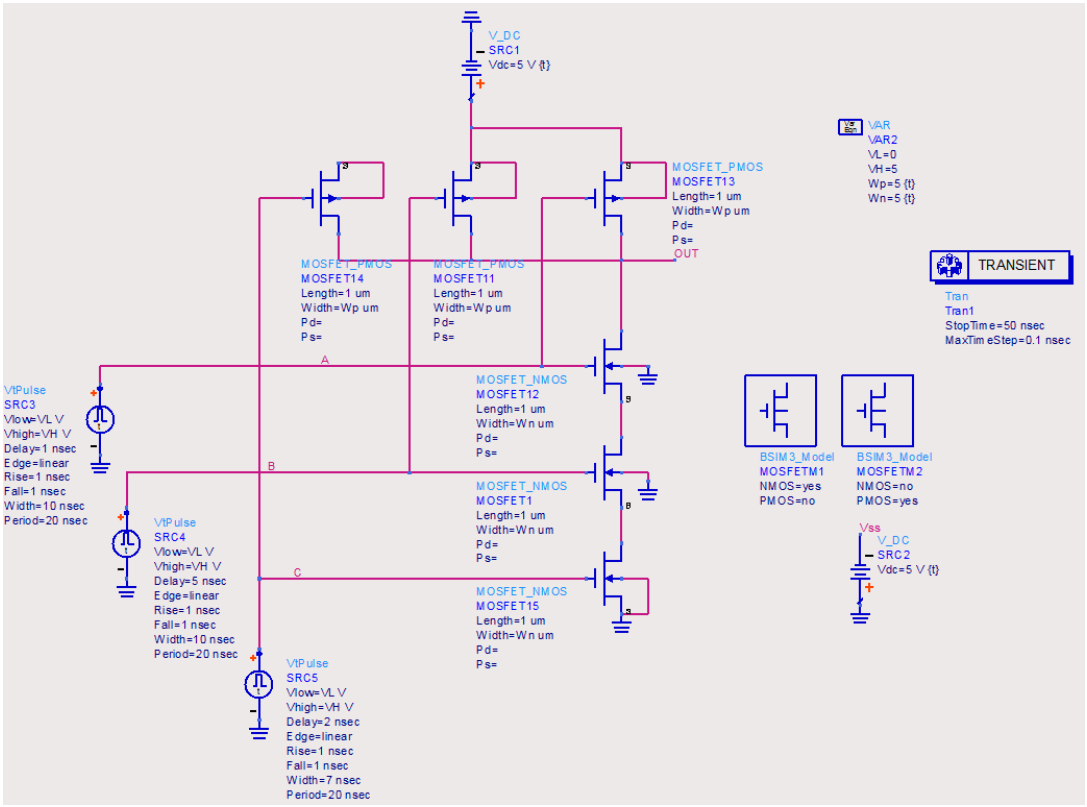


Figure 3.24: Transistor level designed three input NAND gate.

The simulation results of the three input NAND gate, shows that if A=B=C=1 the OUT=0 while the A=B=C=0 resulted in OUT=1. This is the behaviour of a NAND gate. Using the provided NAND gate we can develop the conventional DFF with added reset circuitry depicted in Figure 3.26 with results seen in Figure 3.27. When Q2=Reset=1, the Q goes low, that is proves the behaviour of the circuit.

In Figure 3.28 a CMOS DFF, as same as the conventional DFF is implemented. Using the provided analog DFF designed frequency divider is designed. In Figure 3.29 the schematic of the designed frequency is offered and the corresponding simulation results are shown in Figure 3.30.

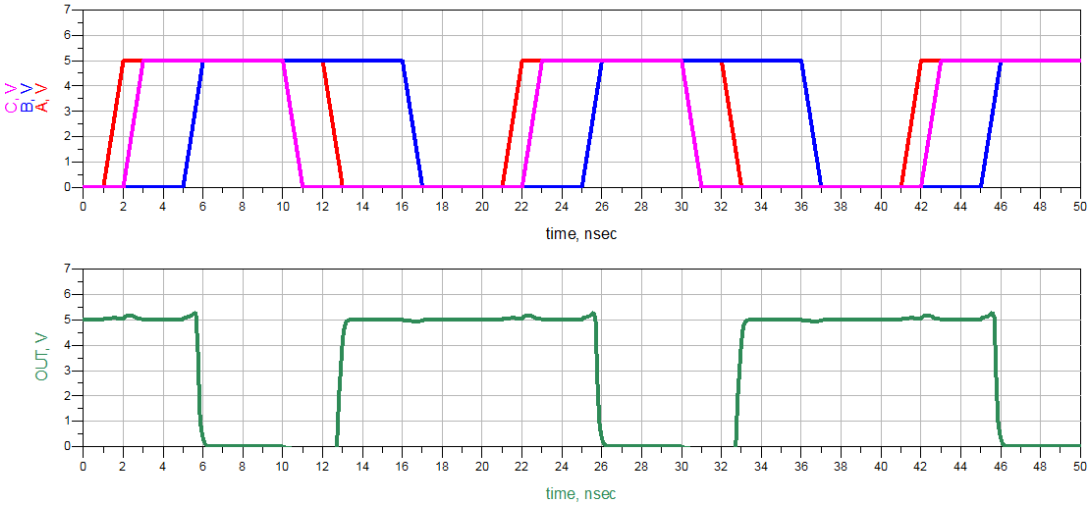


Figure 3.25: Simulation results for transistor level designed three input NAND gate. The first row shows the inputs of the NAND gate. The red is the upper input, blue is the middle input, and the pink is the lower input. The second row shows the output of the circuit.

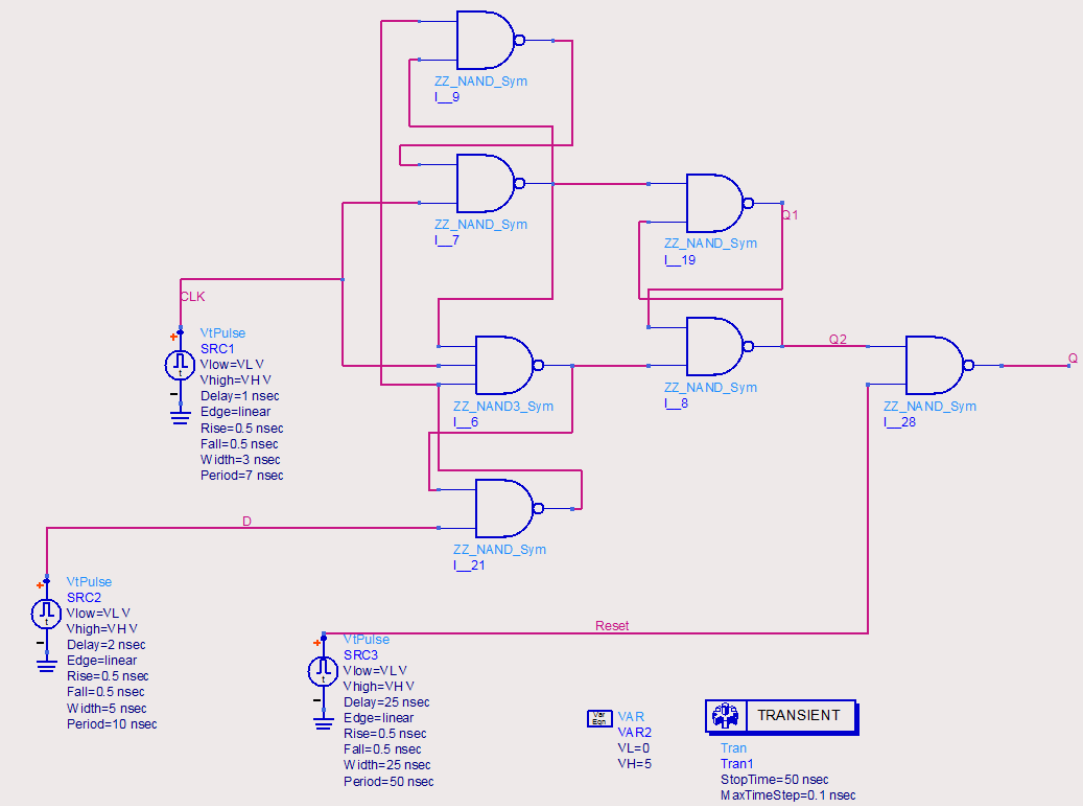


Figure 3.26: Conventional DFF designed using NAND gates

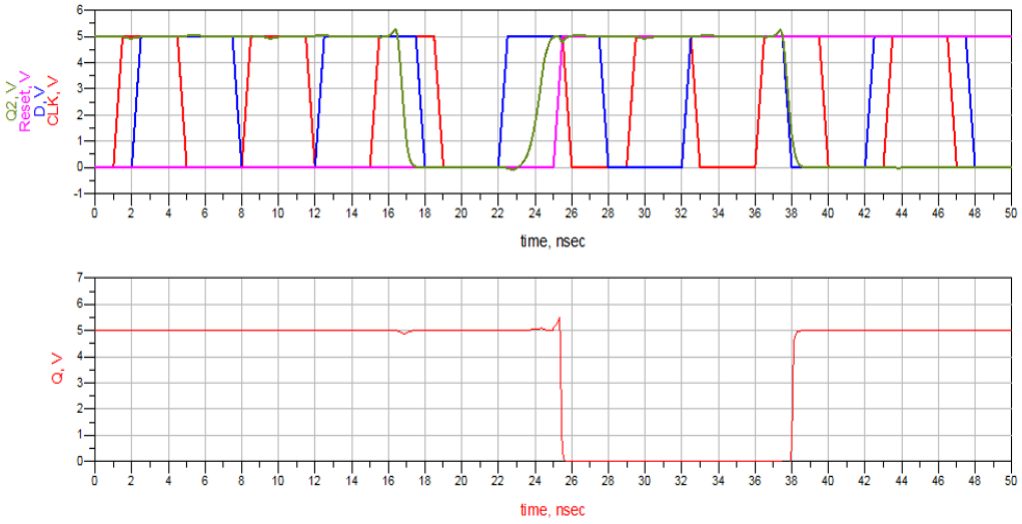


Figure 3.27: Simulation results for transistor level designed DFF. The red is the CLK , blue the data, pink is the reset and green shows the output, Q, of the DFF.

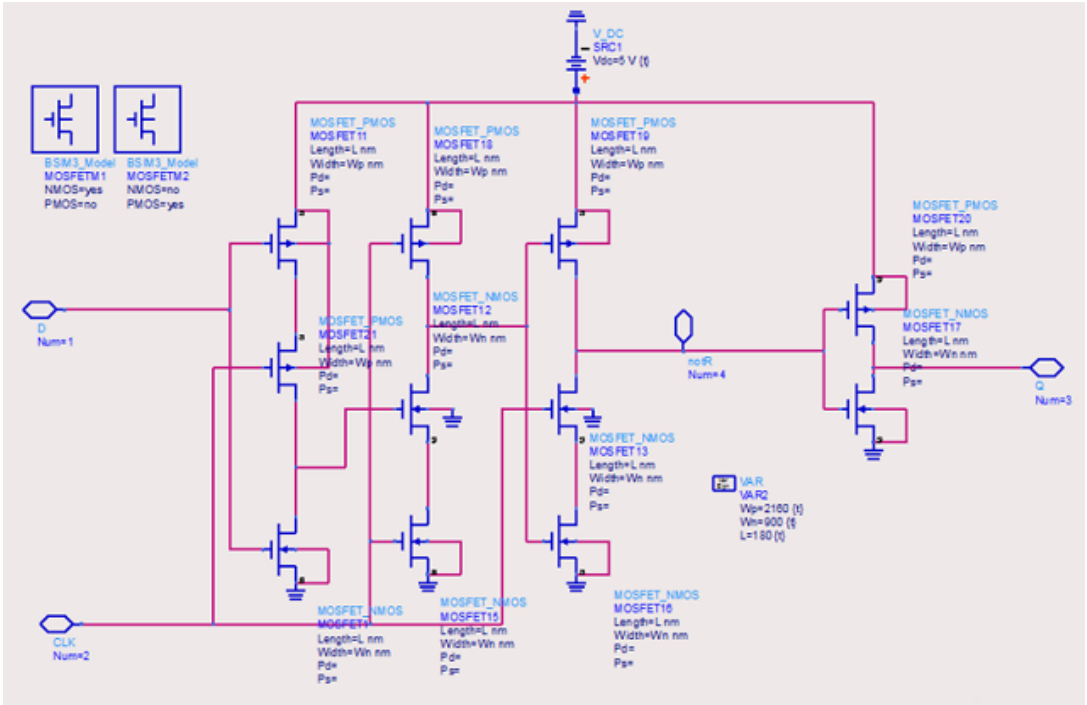


Figure 3.28: Analog DFF.

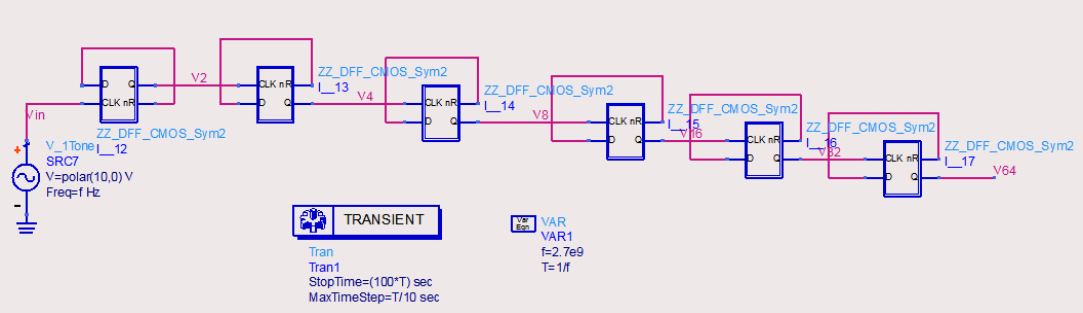


Figure 3.29: Final developed frequency divider. Six number of the CMOS DFFs are used. The transient simulation is applied.

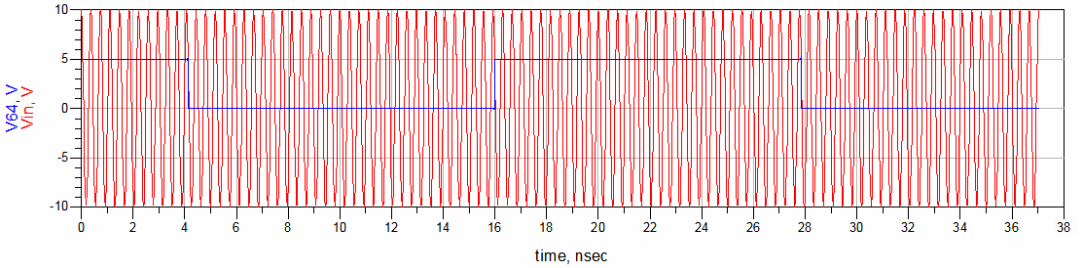


Figure 3.30: Simulation results for final developed Frequency Divider. The red is the input signal and the blue one contributes to the output of the frequency divider.

Referring the simulation results given in Figure 3.30, the input frequency is divided by 64, resulted in output signal, that is also seen in Figure 3.30.

3.3 The PFD design proposed in this thesis study

Phase Frequency Detector (PFD), is one of the main components of the PLL. The PFD do the job of comparison in the PLL loop. In other words, the PFD detects the phase and frequency differences of the input signals. One input is the reference signal and the second is the VCO feedback signal the output of the VCO, whose frequency is divided in frequency divider and reach the PFD. The PFD, generates two outputs which are commonly, called as UP and DOWN. In this research, mainly the basic PFD is used in addition, the analog PFD is designed in ADS. The analog PFD is used in the PLL simulation to investigate the phase noise analysis of the PLL.

3.3.1 Basic PFD

The basic PFD, is the most commonly preferred PFD in the PLL applications. Therefore in this thesis study we firstly implemented the basic PFD, that is discussed in chapter 2 with detailed. Therefore, in this section the developed basic PFD with obtained results are presented.

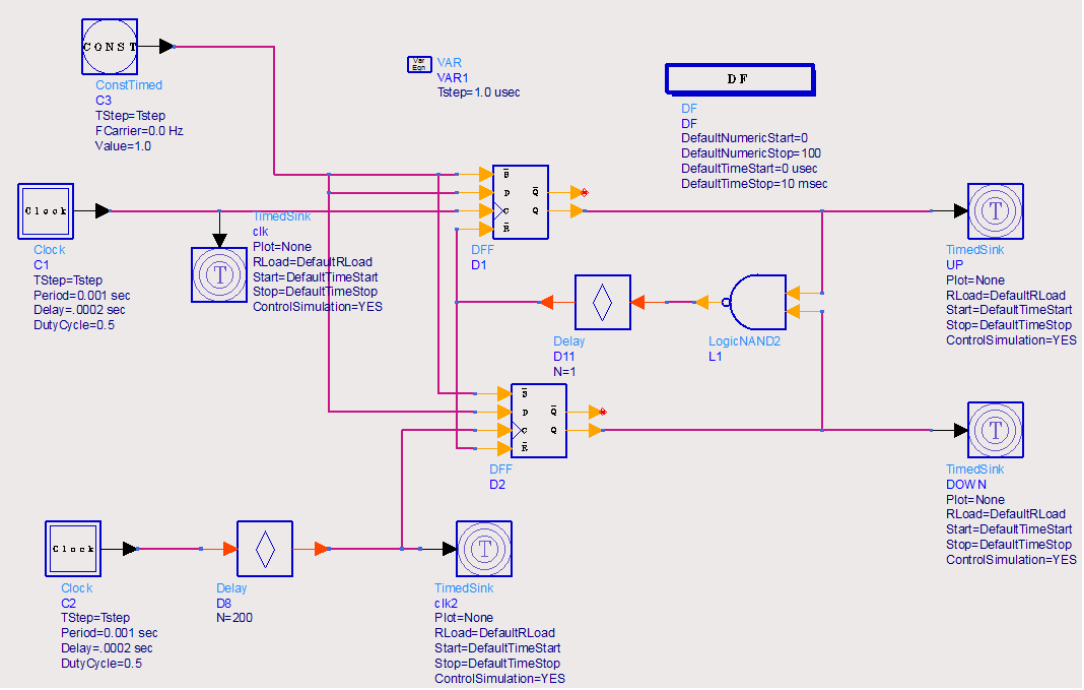


Figure 3.31: ADS schematic of Basic PFD, composed of two DFF and one NAND gate, with DF simulation and Time sinks to generate the simulation results

To implement the basic PFD in ADS as in Figure 3.31, the DF (Data Fallowed) simulation is used. The timing diagram of it can be offered such as depicted in Figure 3.32. Referring to the Figure 3.31, Signal CLK arrives at the DFF1, made the output 'UP' high (This state will be remained until CLK is clocked high again). DFF2 receives CLK2 made 'DOWN' high. Then, NAND gate will receive two ones as it's inputs. A low output that is the clear to the DFFs caused the DFFs to reset with CLK and CLK2 and became low. A 'pulse' out of DOWN will be seen as DOWN only went high when CLK2 was high but was immediately reset due to the NAND.

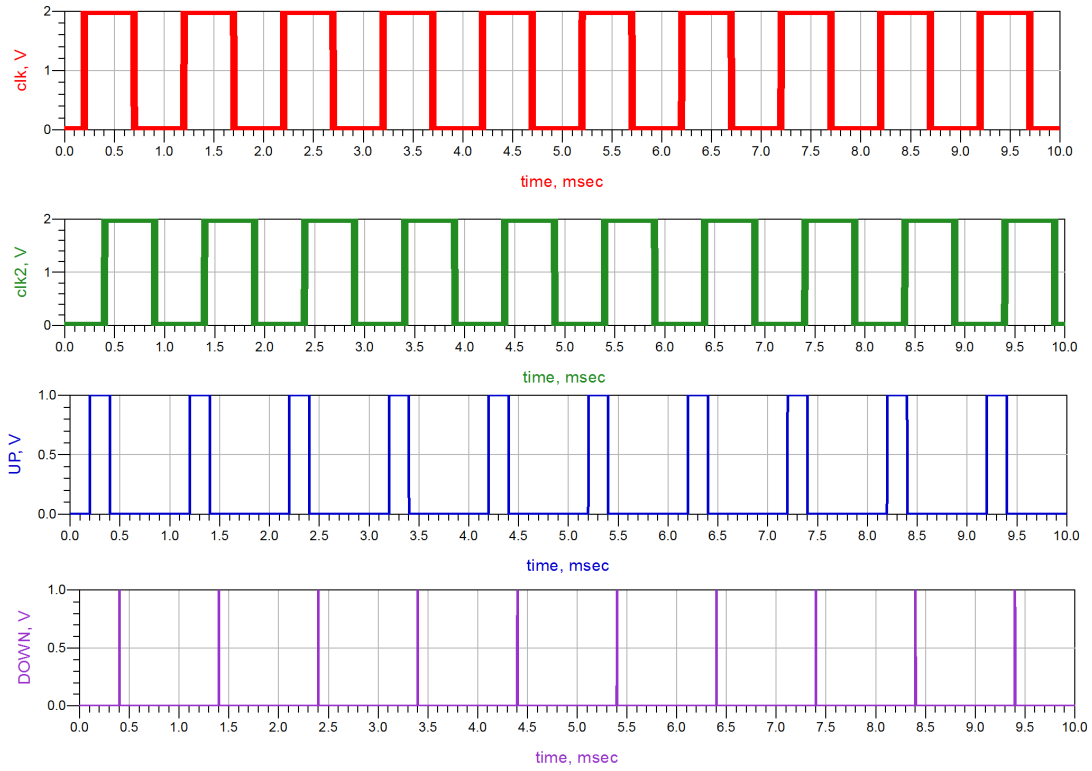


Figure 3.32: Timing Diagram of Basic PFD. The inputs signals of the PFD (first row and second row), The UP signal generated by PFD (the third row), The DOWN signal of the PFD output (the fourth row).

3.3.2 CMOS PFD

As discussed in the previous chapter in this thesis study the transistor level design of PFD is also essential. Therefore, the CMOS PFD similar to the one that illustrated in Figure 2.9 is designed. The CMOS NAND gates 3.22 and inverters 3.22 are used in this design.

The ADS implemented PFD is depicted in Figure 3.35 followed by the results given in Figure 3.36. Also during the simulation it is realized that the transistors sizes should be in nm ranges not in μm due to the GHz ranges demands of frequency.

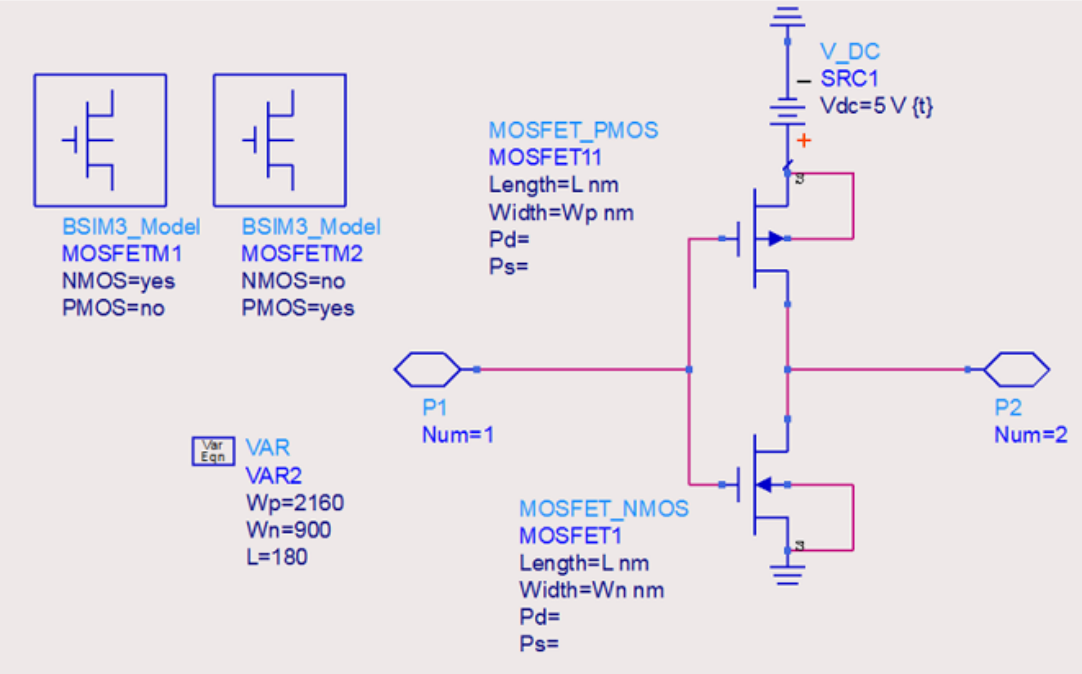


Figure 3.33: Inverter implementation. Two NMOS and PMOs transistors used.

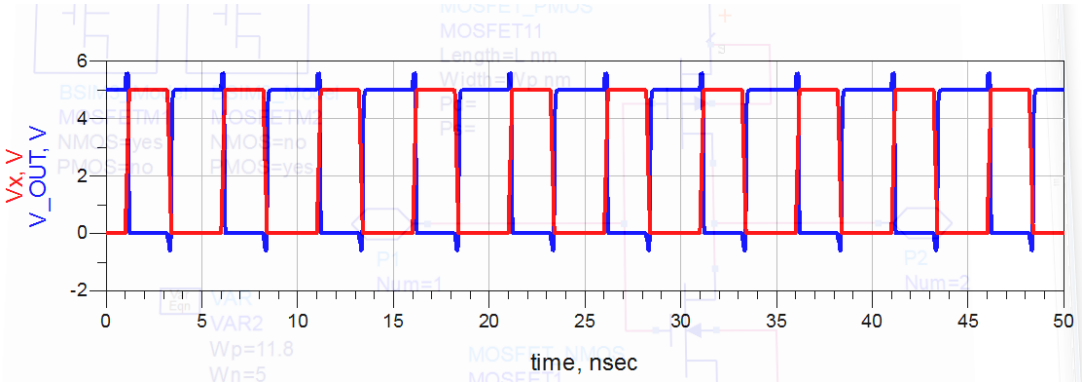


Figure 3.34: Simulation results for inverter, the input voltage is the red and the output is the blue one.

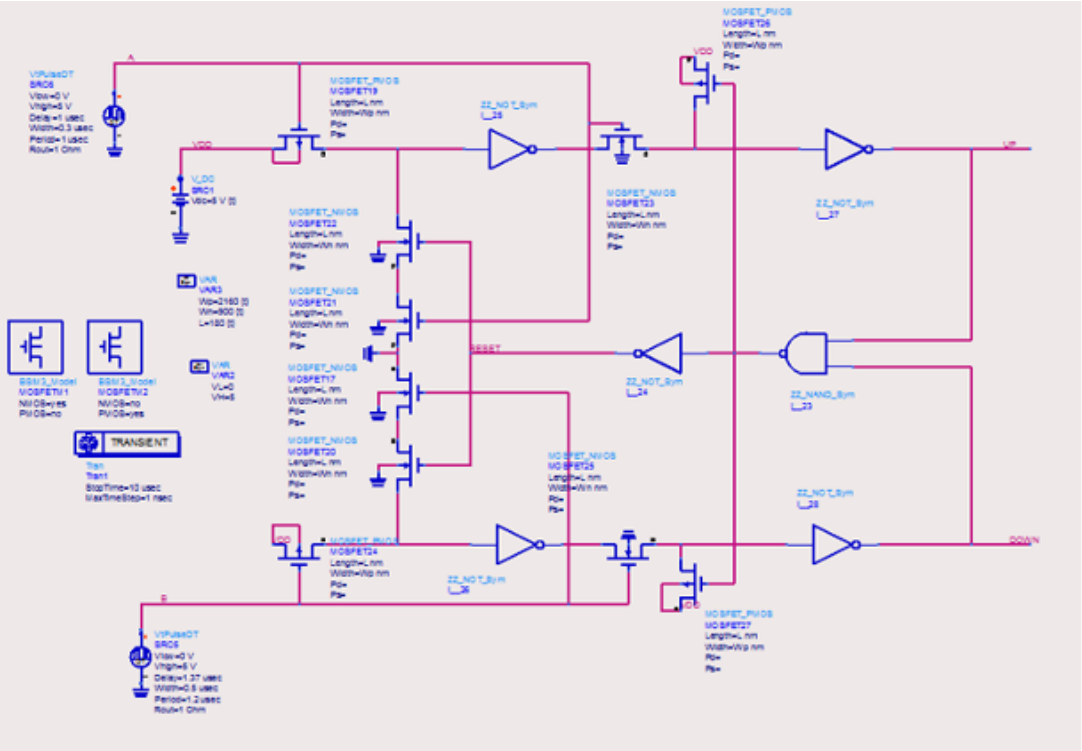


Figure 3.35: Analog PFD including the inverters, the NAND gate and the CMOS transistors.

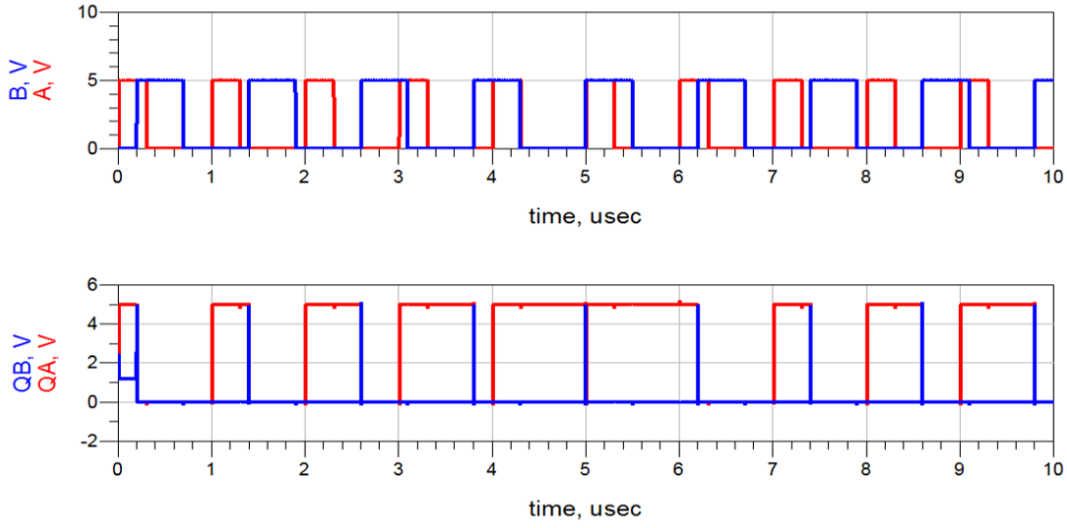


Figure 3.36: Analog PFD simulation results. A and B (in first row) are the PFD inputs with a phase difference. QA and QB (in second row) represents the PFD outputs. The operation is as same as the basis PFD.

The designed CMOS PFD performance is as we expected. The main goal of designing the CP is to produce two output signals of UP and DOWN or QA and QB. These QA and QB voltages are used to open the switches of the CP. The switches should not be opened at the same time. When one is on, the other should be off. The obtained results in Figure 3.36 are proved this behaviour. Consequently, in the PLL design it will be used.

3.4 The Charge pump and loop filter design proposed in this thesis study

In this research to develop the basic charge pump which is depicted in Figure 2.10, a charge pump using NMOS and PMOS transistors is designed. The ADS implementation of the investigated CP is presented in Figure 3.37.

As a comparison to the basic charge pump given in Figure 2.10, in the charge pump illustrated in Figure 3.37, we use NMOS and PMOS transistors for switches and the current sources. Moreover, a switch is added to the circuit before the loop filter. The reason of it can be explained as, the transient analysis of the charge pump needed the place of the switch before the loop filter as the capacitor shorted at t=0 which discharged the capacitor and when t>0, it will be opened. The simulation results of the offered charge pump is depicted in Figure 3.38.

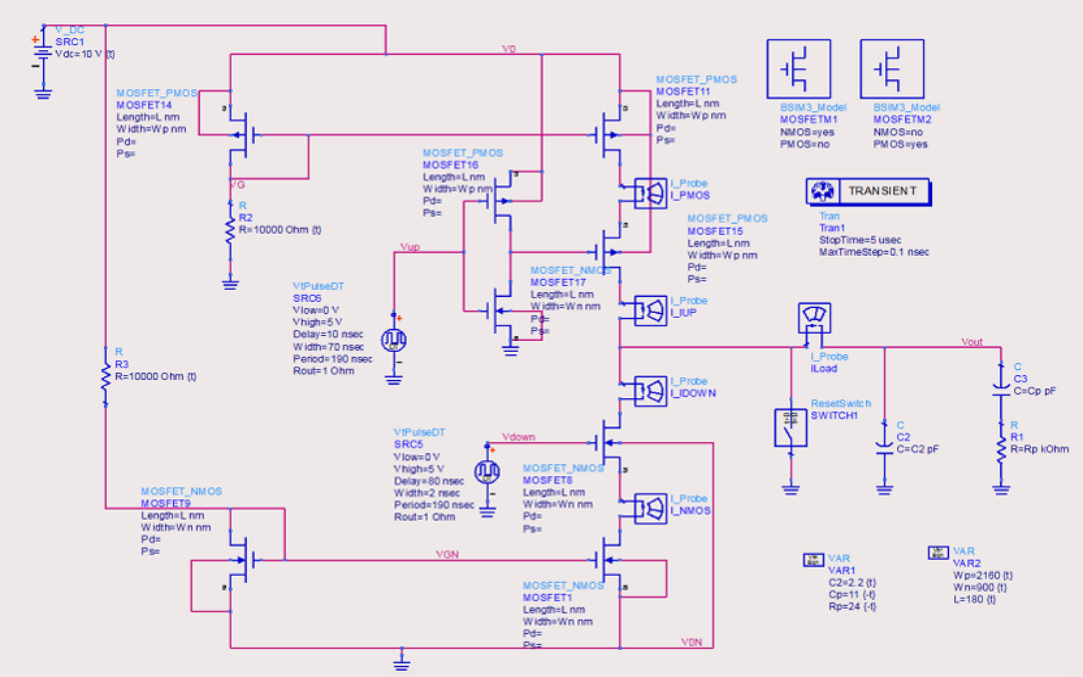


Figure 3.37: ADS schematic of the developed charge pump with loop filter using CMOS transistors

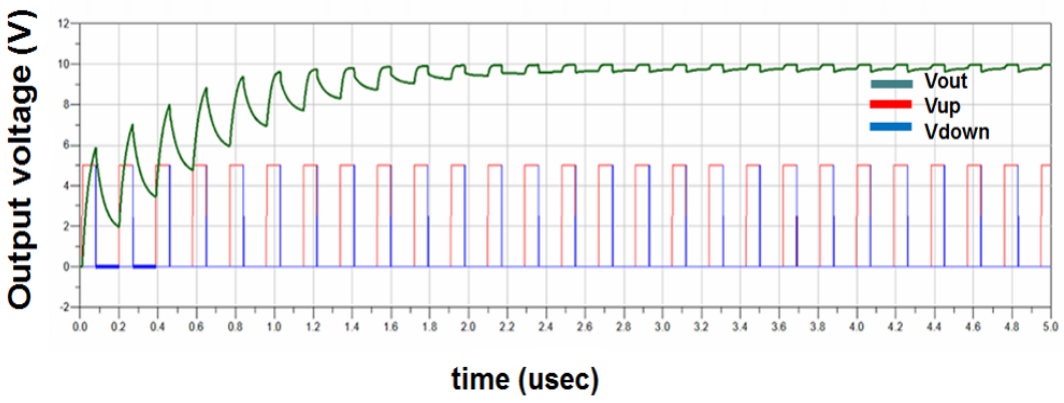


Figure 3.38: ADS developed charge pump simulation results. Vup is the charge pump upper switch input (the UP signal come from PFD), Vdown is the lowe switch input voltage (the PFD DOWN signal), and Vout is the CP and loop filter output voltage. The output voltage will be used as the control voltage of the VCO.

3.4.1 Charge pump design summary

In this section a summary of the provided charge pump will be offered. As a starting point the relationships for NMOS and PMOS transistors currents are given in equations 3.2 and 3.4, respectively:

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{th})^2 \tag{3.2}$$

$$I_{Dp} = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})(V_{GS} - |V_{th}|)^2 \tag{3.3}$$

Where V_{th}=0.7 V, K_n=$\frac{1}{2}\mu_n C_{ox}$ and K_p=$\frac{1}{2}\mu_p C_{ox}$

To continue the design the biasing of the transistors should be noted. Accordingly, the biasing of the PMOS transistor is offered in Figure 3.39.

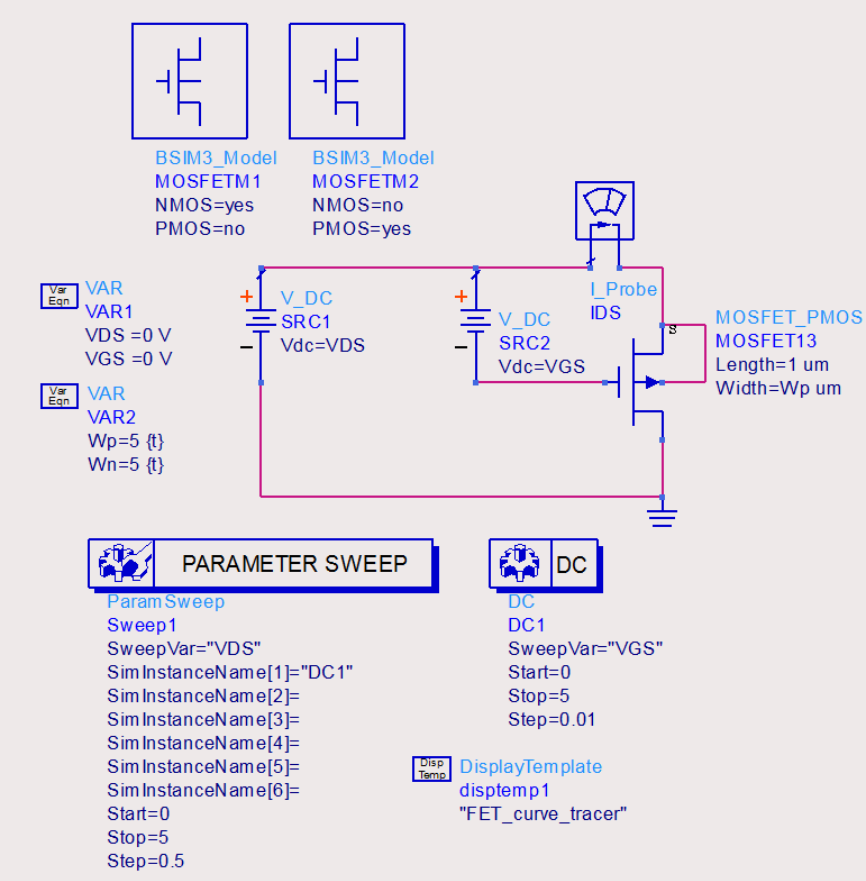


Figure 3.39: PMOS transistor biasing in ADS

The biasing simulation results are given in Figure 3.40.

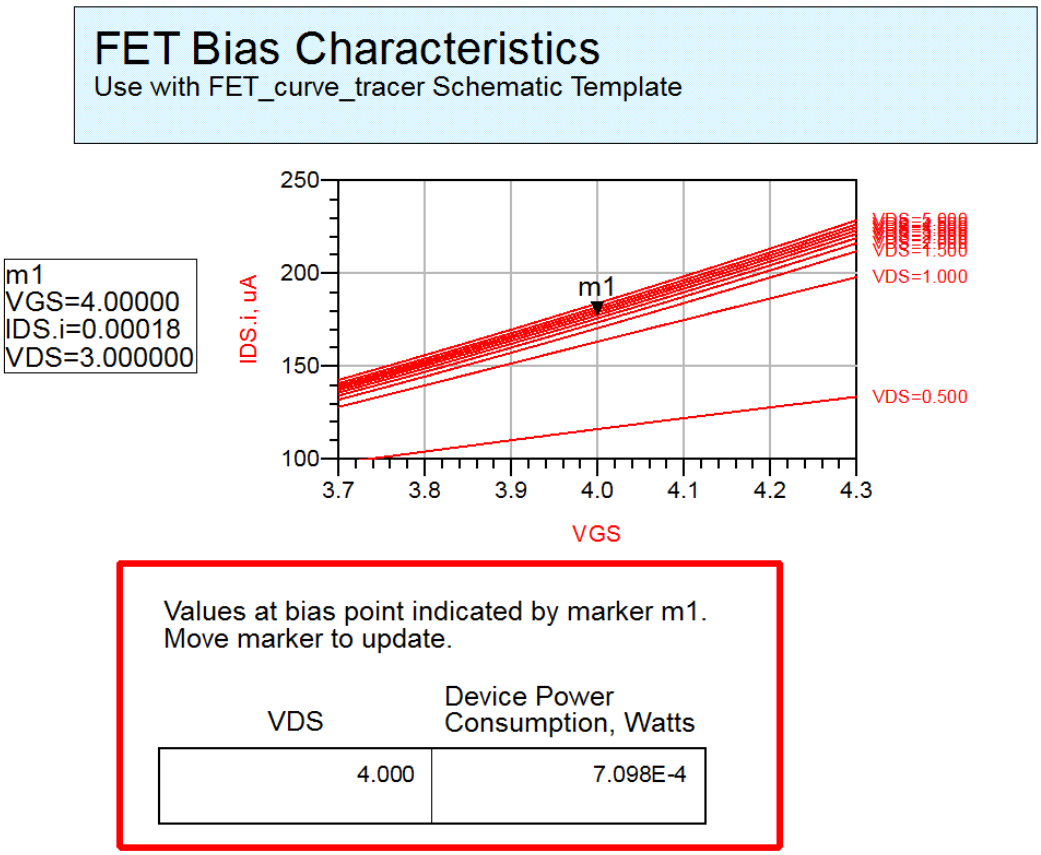


Figure 3.40: PMOS transistor biasing results (V_{GS}=4 V and I_D= 180 μA)

Replacing the simulation results given in Figure 3.40, for PMOS transistor in equation 3.4 the K_P value is obtained as equation 3.5:

$$180\mu A = K_p(5)(4 - 0.7)^2 \tag{3.4}$$

$$K_p = 3.3\mu A/V^2 \tag{3.5}$$

After biasing the NMOS transistor, the same procedure can be done for NMOS transistor for V_{GS}=4 V and I_D= 420 μA as equations, 3.6 and 3.7 :

$$420\mu A = K_n(5)(4 - 0.7)^2 \tag{3.6}$$

$$K_n = 7.7\mu A/V^2 \tag{3.7}$$

As it is discussed in previous sections to avoid the current mismatching the NMOS and PMOS transistors should have the equal currents as equation 3.8. Therefore, the solution is given as equation 3.9:

$$I_{Dn} = I_{Dp} \tag{3.8}$$

$$K_n W_n = K_p W_p \tag{3.9}$$

Resulted in equations 3.10 and 3.11,

$$\frac{K_n}{K_p} = \frac{W_p}{W_n} \tag{3.10}$$

$$\frac{W_p}{W_n} = \frac{7.7}{3.3} \tag{3.11}$$

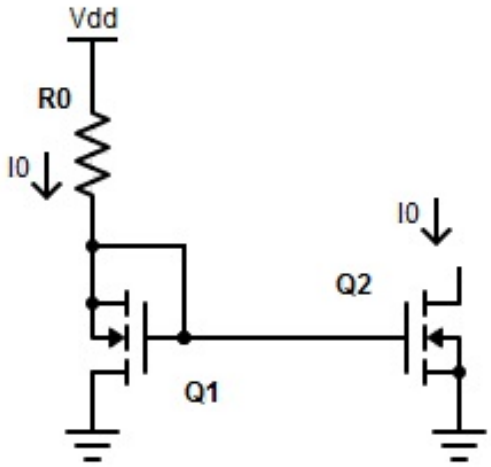


Figure 3.41: Charge pump current source

According to the Figure 3.41 the coming relations can be written as equations 3.12 and 3.13 :

$$I_0 = K_n(\frac{W}{L})(V_{GS} - V_{th})^2 \tag{3.12}$$

$$I_0 = \frac{V_{DD} - V_{GS}}{R_0} \tag{3.13}$$

It is assumed that R_0=250 Ω, V_{DD}=5 V,I_0=1 mA. Replacing the assumed values in equations 3.12 and 3.13, W_n=7.92 and W_p=18.473 are obtained.

CHAPTER 4

SIMULATION RESULTS FOR IMPLEMENTED PLLS

To design a low phase noise PLL operating in a few GHz frequency range, the PLL design is implemented in different steps. In this chapter first, the initial PLL that is implemented in ADS using both digital and analog blocks is introduced. Then, the design of the PLL in transistor level, using only analog blocks is reviewed.

4.1 Analog-Digital PLL

The PLL is simulated in ADS. In the designed PLL, the above mentioned VCO using HEMT transistor, the CMOS CP, the basic PFD, and the frequency divider using DFFs are used. The performance of the PFD and the CP are evaluated in a separate simulation. Other PLL components are also simulated individually. Figure 4.1 shows the PFD and CP implementation in ADS. The main goal of this design is to evaluate the performance of designed basic PFD in the same circuit with CP. The limitation of this design was the selection of the simulation type, since both digital and nalog blocks were used. In addition, choosing the appropriate inputs for the PFD, that an make the phase difference in the PFD was also challenging. The Delay after the lower clock is used to make a phase difference.

The performance of the above circuitry is presented in Figure 4.2. The phase difference of the inputs of the PFD is obvious (the upper). The PFD outputs (the middle) are proper to activate the CP, and the circuit output (the lower one) shows the CP behaviour. The output voltage of the CMOS CP fluctuates according to the phase error of the PFD and reaches to the steady-state when the error is nearly zero.

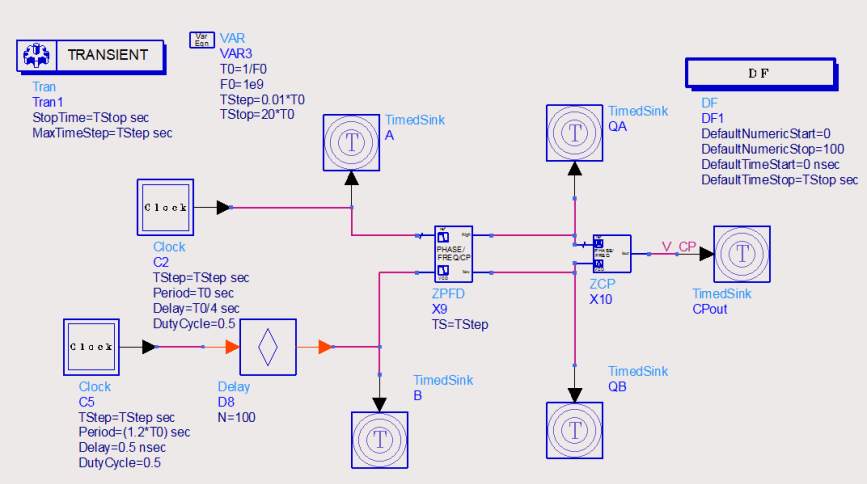


Figure 4.1: ADS implementation of the PFD and the CP. To run the basic PFD, the DF simulation used. The CMOS CP is applied. Due to the DF simulation, the time sinks and clocks are used.

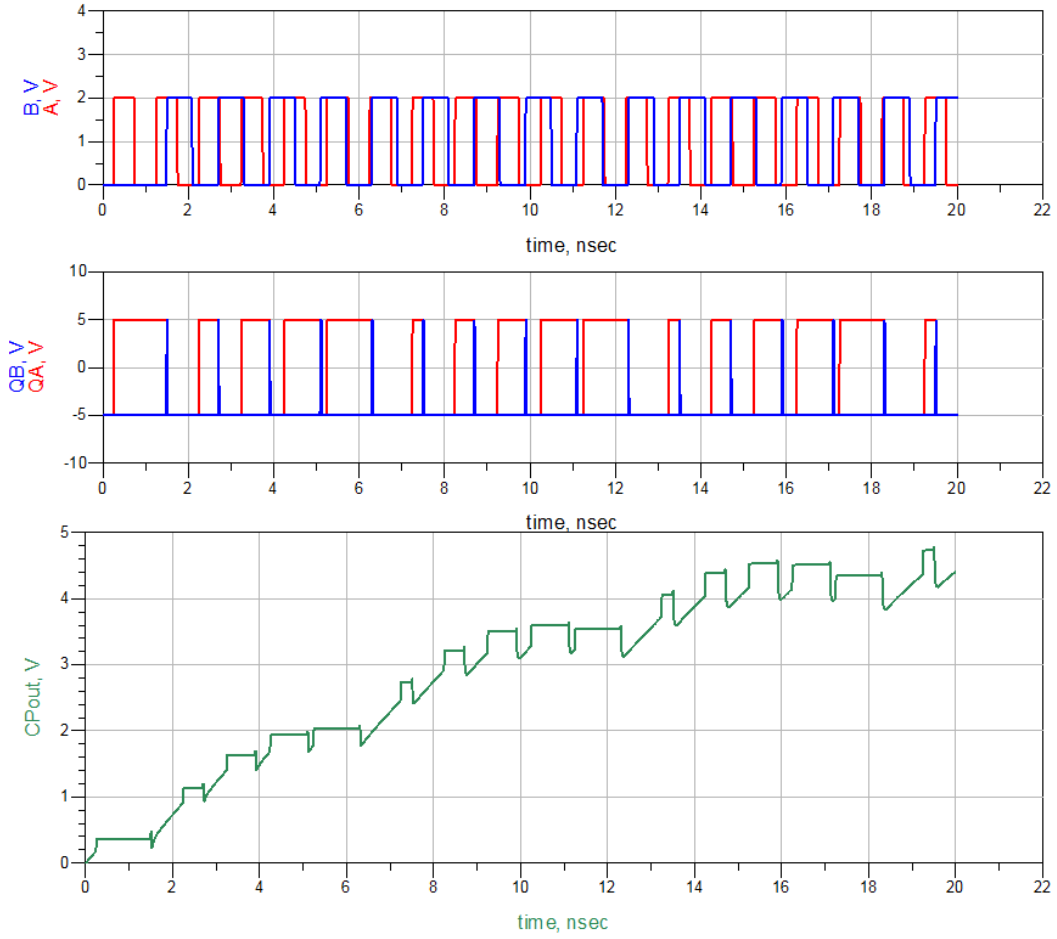


Figure 4.2: PFD-CP simulation results. A and B are the PFD inputs (the upper). QA and QB are the PFD outputs (the middle), and CPout is the CP output (the lower).

The VCO and frequency divider simulation is also conducted in separate simulation. In order to implement the circuit in ADS (Figure 4.3), the designed VCO included the varactor is used. The frequency divider designed using the DFFs of ADS library is applied. As same as the above simulation the DF simulation is used. The same limitations we faced. The VCO input given about 7 V.

The analysis of the above circuit is carried out (Figure 4.4). The VCO output frequency is divided by four. Since the used divider included two DFFs. The spectrum of the VCO output is also shown in this figure. The VCO output frequency is obtained around 3 GHz.

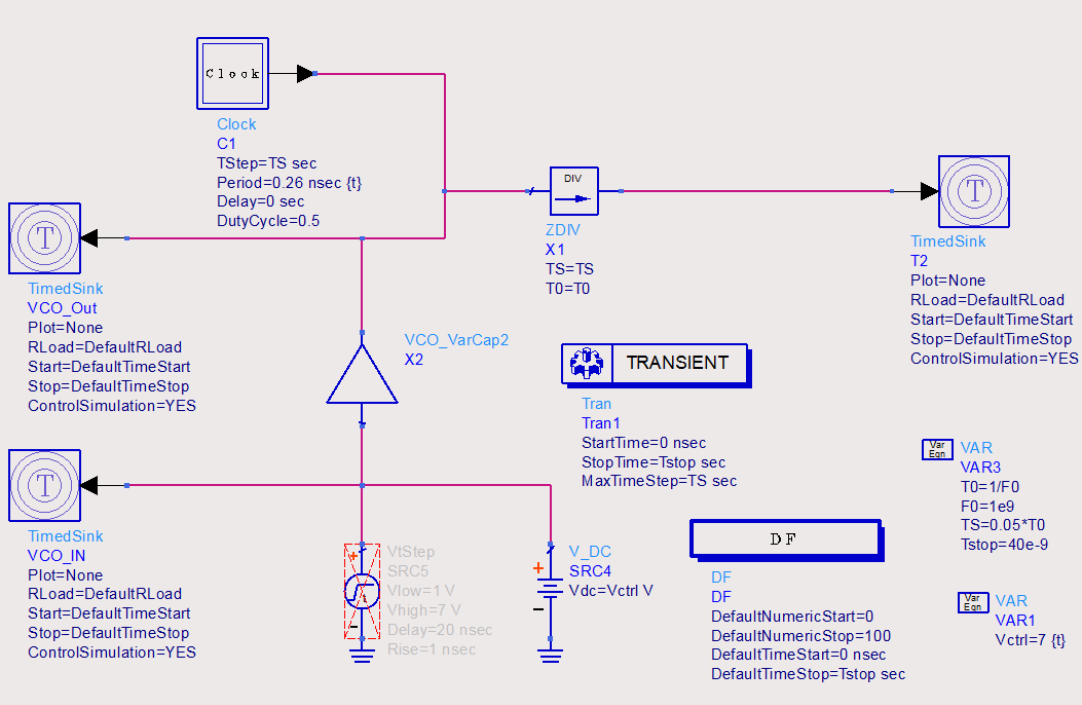


Figure 4.3: VCO along with frequency divider simulation. DF simulation is applied due to the frequency divider that is digital block. In addition transient simulation is used to simulate the behaviour of the VCO.

Eventually, the PLL is constructed using the PFD, CP, VCO and the frequency detector connection in a loop. The ADS Implementation of the PLL is shown in Figure 4.5.

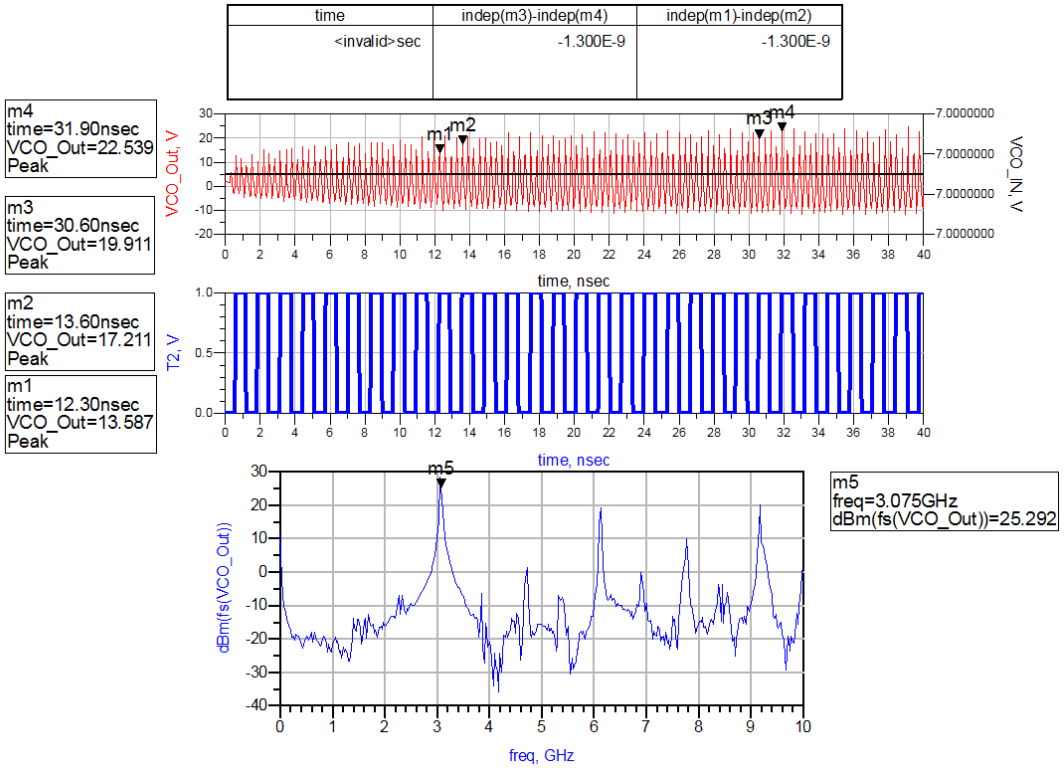


Figure 4.4: VCO-DIV simulation results. The frequency of the VCO output signal (first row) is divided by 4 using the designed frequency divider (second row). Third row shows the spectrum of the VCO output signal.

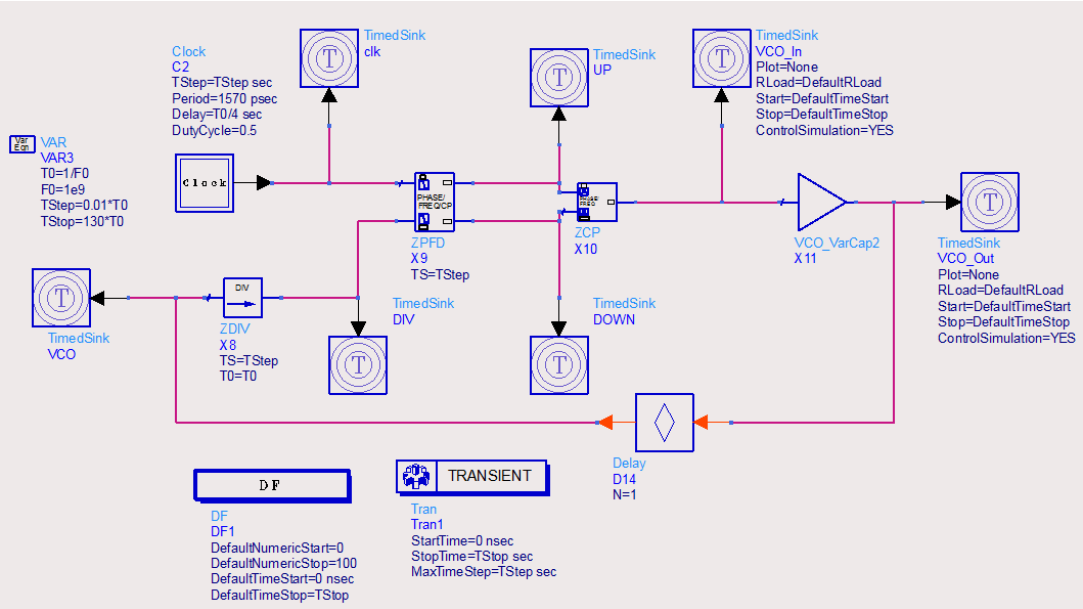


Figure 4.5: Analog-digital PLL schematic. The VCO-DIV and PFD-CP circuits are used. DF simulation used due to the digital blocks of PFD and frequency divider. Transient simulation is used for simulation of the analog blocks of CP and VCO

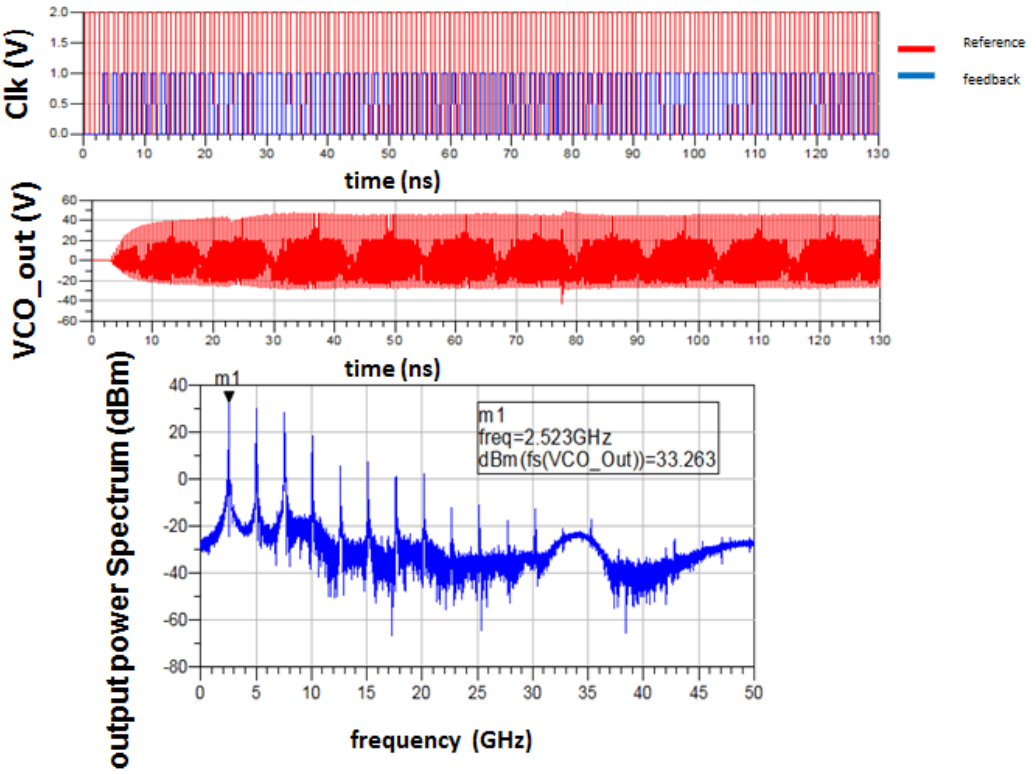


Figure 4.6: Resulted PLL simulation results. The reference clock (clk) and the frequency divider output (first row). The VCO output signal (the second row) and its spectrum (fourth row).

As an interpretation to the simulation results obtained in Figure 4.6, the VCO_{in}, finally reached the steady-state, the essential factor that determines the PLL locked condition. Furthermore, the final signal obtained by the Furrier transform of VCO_{out}, provides a frequency of the 2.523 GHz. However, the phase noise which is one of the most critic factors in this thesis study, can not be simulated. Since both analog and digital blocks are available in the analog-digital PLL circuitry, we can not implement the HB simulation. The HB simulation is essential in simulating the phase noise.

In proceeding section, the CMOS PFD and frequency divider will be evaluated with the designed VCO and the CMOS charge pump.

4.2 All Analog PLL

Following the discussion done in previous section in order to make phase noise analysis possible in this thesis study. We try to design all-analog PLL. To achieve this goal, the digital blocks of the analog-digital PLL, that is presented in previous section, in transistor level. Therefore, using the analog PFD demonstrated in Figure 3.35 and the frequency divider illustrated in Figure 3.28 in addition the CP designed in Figure 3.37 and the designed VCO discussed in Figure 3.13, the all-analog PLL is simulated in transistor level. Accordingly, fist the PFD and the CP are simulated together as seen in Figure 4.7, the simulation results are presented in Figure 4.8.

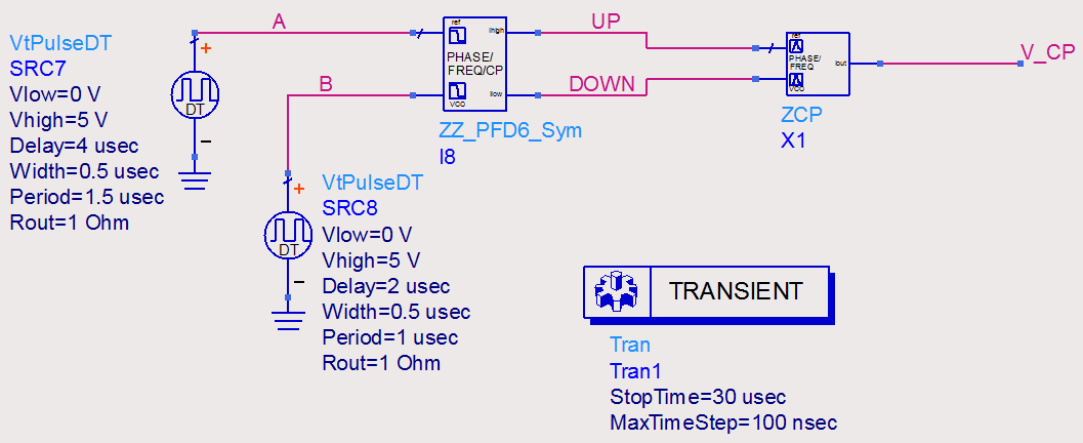


Figure 4.7: Analog PFD-CP. CMOS PFD and the CMOS CP we mainly design using the CMOS transistors with loop filter added is used.

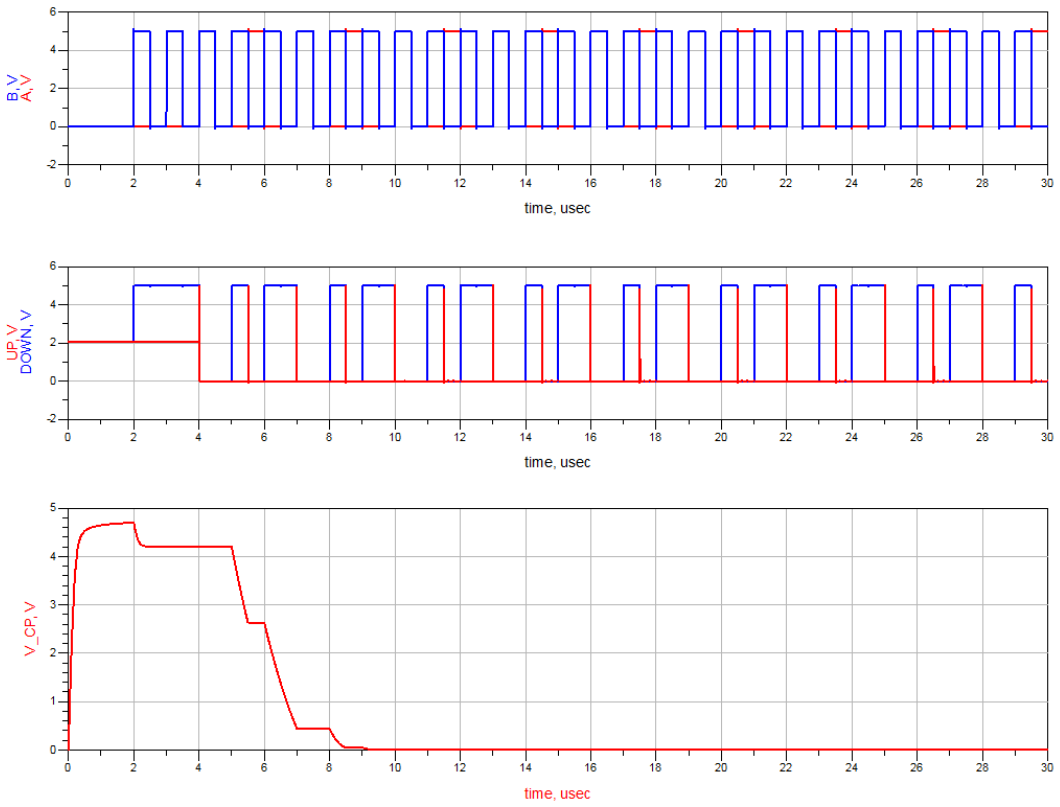


Figure 4.8: Analog PFD-CP simulation results. The PFD inputs, A and B,(first row) with a phase difference and the related outpus from PFD (second row). The CP output voltage fluctuations resulted by the PFD output (third row).

The VCO and the frequency divider are also simulated together in ADS (Figure 4.9). In this circuit a divider by 2 is used. The main goal, is to examine that the VCO and frequency detector can serve their demands and work together or not. Therefore, the frequency divider, that is provided in Figure 3.28 is used. In proceeding steps of the thesis by increasing the number of the D flip-flops, we will try to increase the divider ratio. The simulation results are given in Figure 4.10.

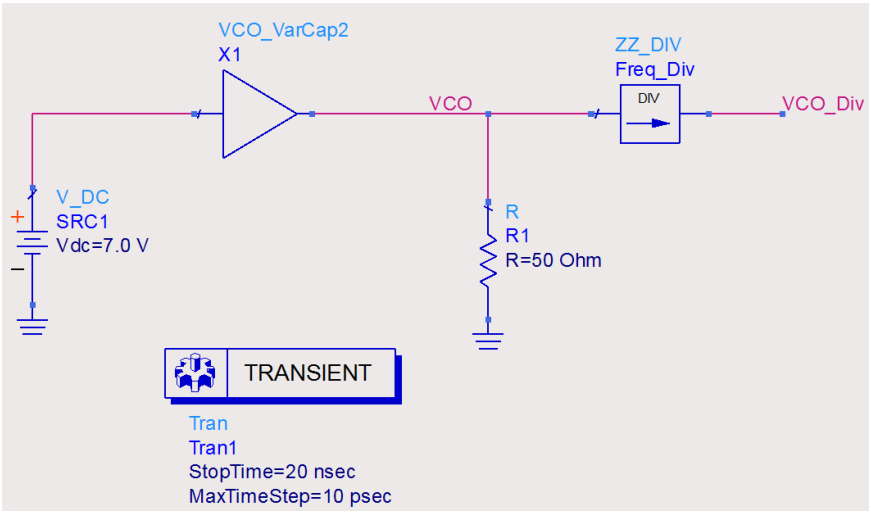


Figure 4.9: Analog VCO-DIV. The designed VCO and a single CMOS D flip-flop as a divider.

4.3 Discussion

Although the obtained control voltage of the VCO reached to the steady-state and the frequency of the obtained VCO signal was 3.5 GHz, the HB simulation could not be converged. HB simulation analyze the signals in the frequency domain. Since the output of the frequency divider is a rectangular signal, there exist a lot of harmonic components. Therefore, the HB simulation can not converge and hence the phase noise could not be obtained.

In PLL, especially when the divider number is increased, the simulation time increased millions times. Therefore to reach the lock state, the PLL should perform millions time. The time points needed for a single simulation increasingly increased [42].

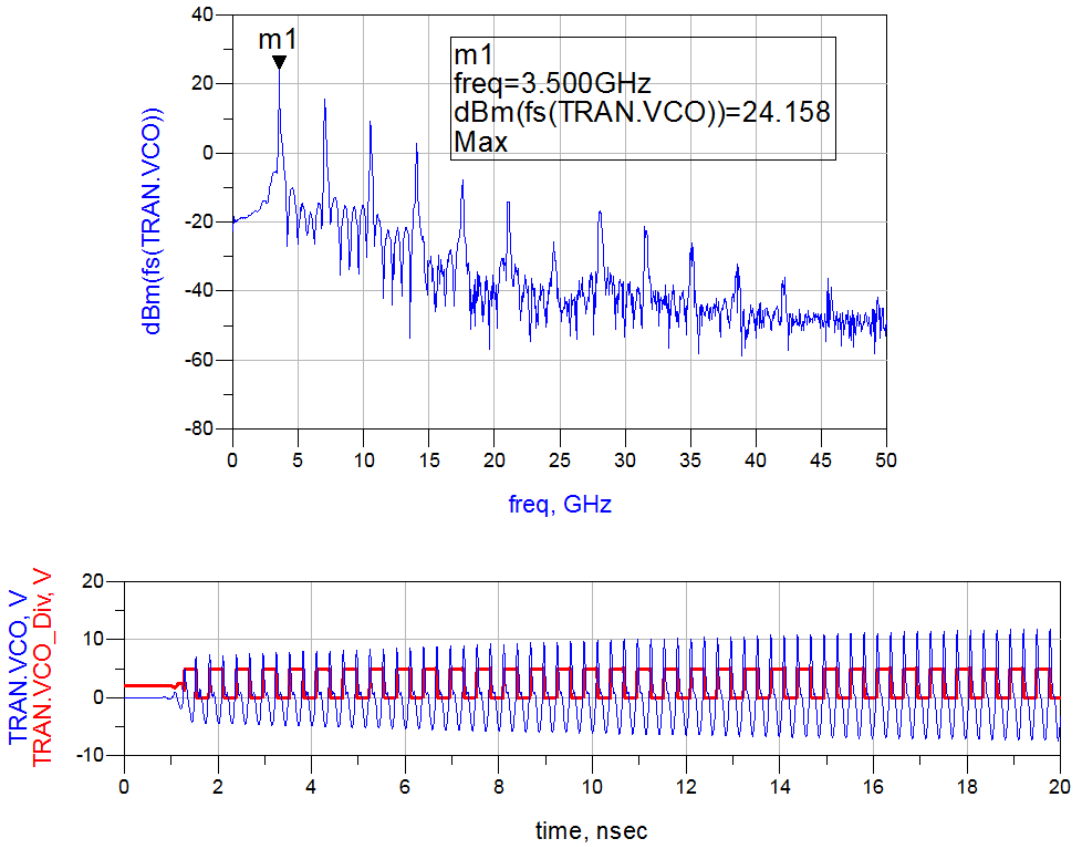


Figure 4.10: Analog VCO-DIV simulation results. The VCO output signal spectrum (the upper). The VCO output signal (blue in lower), and the PFD output (red in the lower).

CHAPTER 5

PLL PHASE NOISE ANALYSIS

The closed-loop PLL noise is an important factor of the total system performance in modern digital communications which use phase modulation. The PLL noise model includes the effect of the blocks forming the PLL as well as the VCO [43]. In section **??**, the phase noise basics are reviewed. In this chapter the PLL noise analysis will be illustrated in detail. First, using the loop dynamics studied in section 2.2.2, analytical methods will be discussed. Then, using the analytical results, the phase noise analysis of the CPPLL, will be done in ADS.

5.1 PLL Noise Analysis

Phase noise of a VCO placed inside a PLL is shaped by the PLL noise transfer functions [43]. A free running VCO phase noise is simply called VCO phase noise while the phase noise of a VCO inside a locked PLL is called PLL output phase noise. The overall PLL output phase noise is characterized by the noise contributions of all the blocks in a PLL [43]. In Figure 5.1 the PLL noise model that is preferred in this thesis study is shown.

According to the noise model that is shown in Figure 5.1, in this study the PFD and CP noises are modelled together, the VCO and frequency divider noises are also modelled.

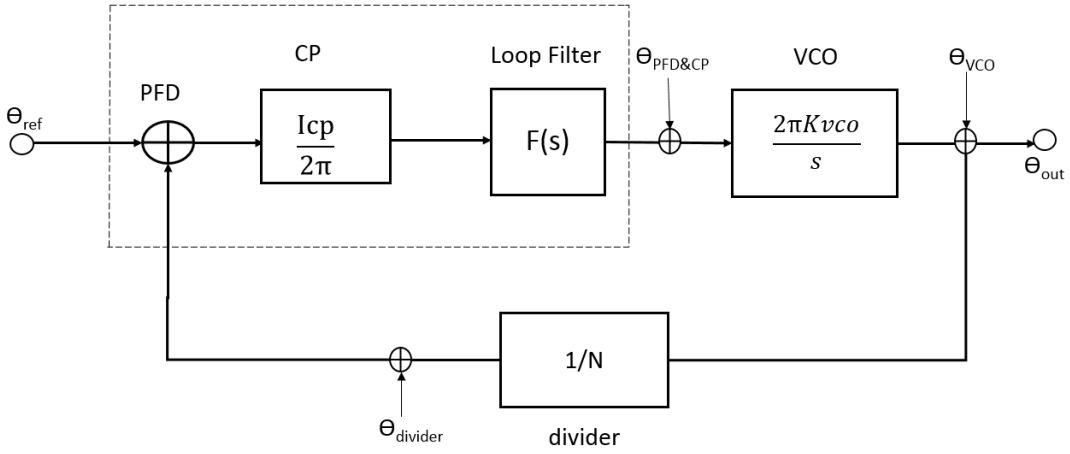


Figure 5.1: PLL noise model used in this study. Θ_{ref}, the reference oscillator noise voltage, Θ_{PFD-CP}, the PFD and CP noise, Θ_{VCO}, the VCO noise voltage, and Θ_{DIV}, the frequency divider noise voltage.

5.2 PLL Noise Modeling and Simulation

To investigate the PLL close loop phase noise some analytical methods should be applied. Hence, to begin with the K_{VCO}, gain or sensitivity of the implemented VCO is simulated as depicted in Figure 5.2.

According to Figure 5.2 and equation 2.1, K_{VCO} is calculated as K_{VCO} = 0.132 GHz/V, and the VCO range is 3.011-2.560 GHz frequency.

Hence, some parameter values which are essential for PLL noise model construction are [44]

a-) K_{VCO}=0.132 (GHz/V)

b-) I_P= 1 mA

c-) ω_{-3dB}=0.1ω_n

d-) BW_{loop}=2.5ω_n

e-) C_2=0.2C_P

f-) f_{out}=2.8 GH

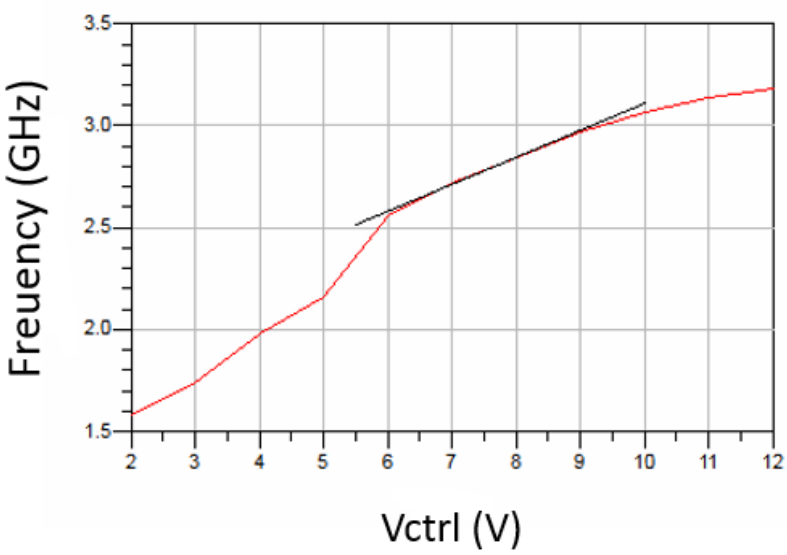


Figure 5.2: Applied VCO gain or sensitivity. The result of the HB simulation on the designed VCO, to see the frequency changes of the VCO with the control voltage variations. The line is applied, to approximate the linear region.

Applying the parameter values and the equations of 2.14 and 2.15, the PLL closed loop parameters can be summarized as seen in Table 5.1.

Table 5.1: PLL closed loop parameters. the reference frequency (f_{ref}), the divider ratio (N), the natural frequency (ω_n), the loop filter components (C_P, R_P and C_2).

f_{ref} (MHz)	N	$\omega_n \times 10^6$	C_P (PF)	R_P (KΩ)	C_2 (PF)
30	93	7.54	3.97	60.8	0.8
43	64	10.8	2.8	66	0.56
22	128	5.52	5.38	67.5	1.076

The phase noise analysis of the designed PLL, is implemented based on the following steps:

1. Phase noise simulation of single blocks of PLL.
2. Achieved data saving in a file.
3. S-domain PLL model generation.
4. Noise addition at the certain points.
5. The model running at the output.

Consequently, in the following section, we will try to apply the main steps, discussed above, to each block of the CPPLL. All the blocks that are studied in this section, are the transistor level designed blocks that are presented in chapter 3. In addition, in phase noise simulation of each block of the PLL, the phase noise in SSB (dBc/Hz) is related to the phase noise in power spectral density ($\frac{rad^2}{Hz}$) as [43]

$$\Theta^2_{rms}(f_m) = 2(10^{\frac{L(f_m)}{10}}) \tag{5.1}$$

where the f_m is the carrier frequency offset, and $L(f_m)$ defines the SSB phase noise.

5.2.1 VCO noise analysis

In chapter 3.1, the phase noise analysis of the VCO is discussed. However, in this section it is attempted to simulate the phase noise of the VCO in such a way that it can be applicable for the PLL noise analysis. The VCO schematic for the phase noise analysis is depicted in Figure 5.3.

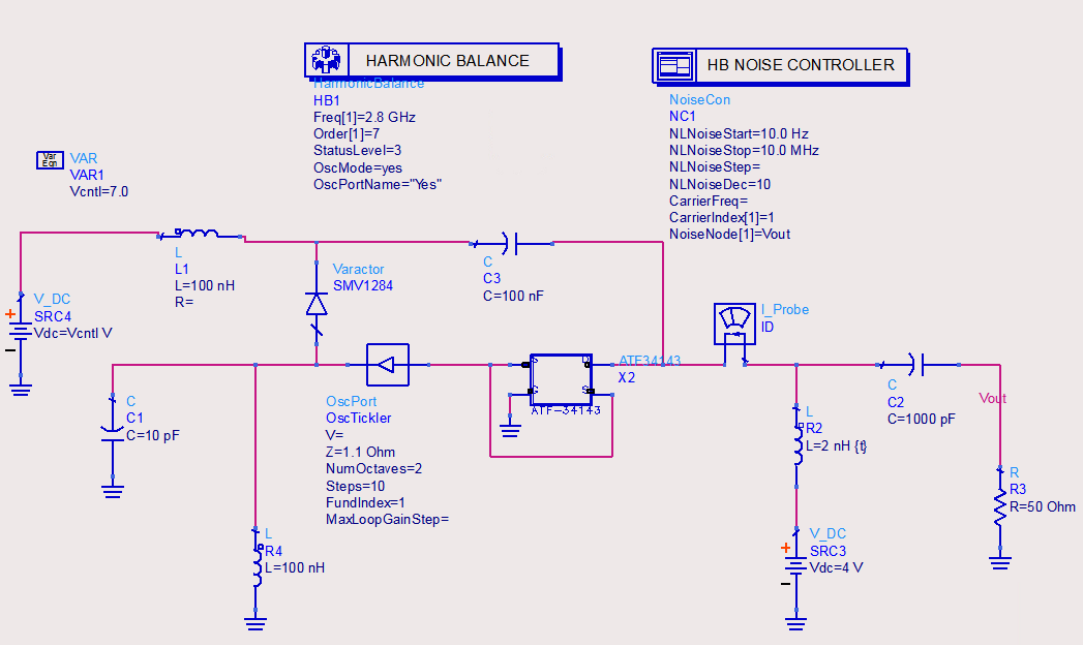
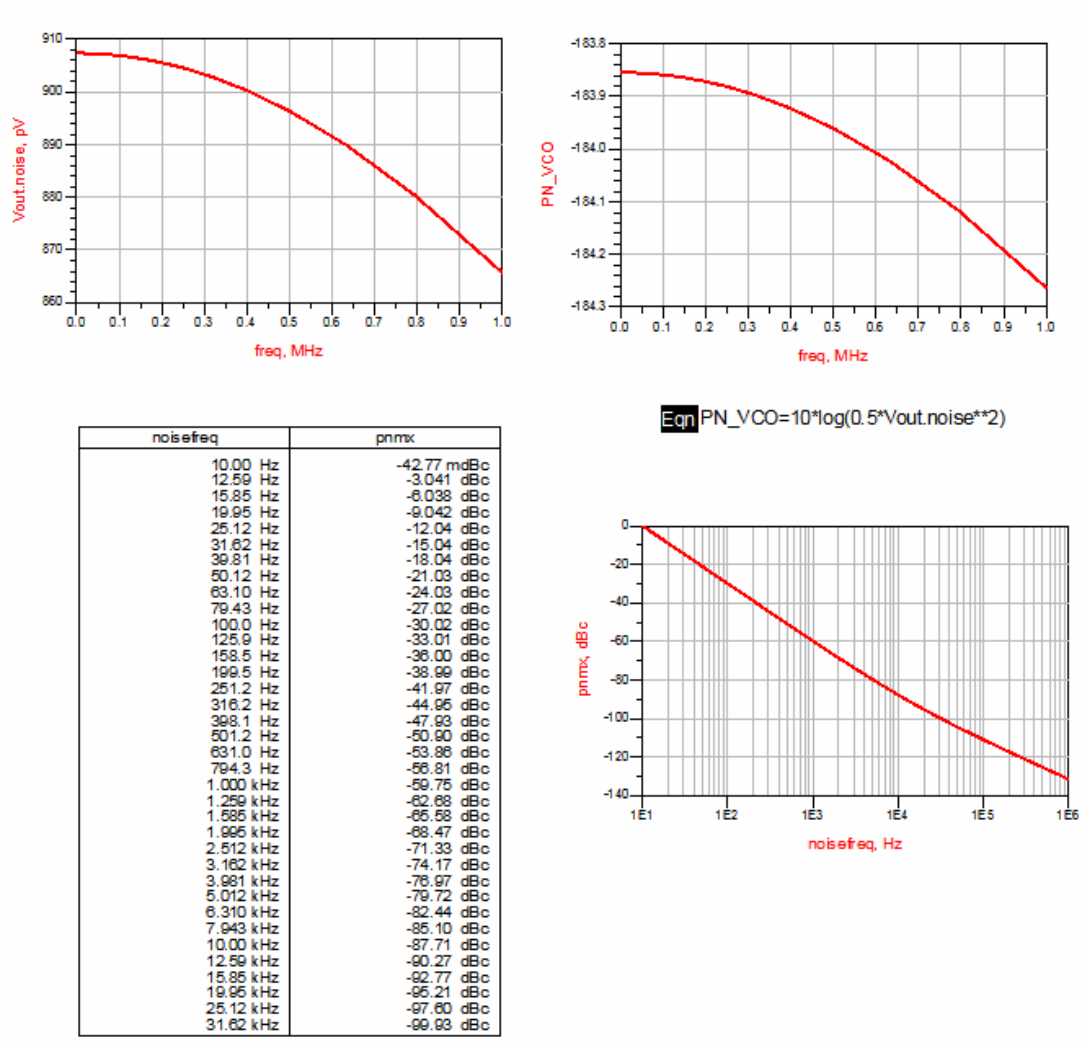


Figure 5.3: VCO noise analysis. The HB noise controller is used along with the HB simulation. To make the phase noise simulation possible, the noise option in HB simulation is activated.

In Figure 5.4, the simulation results of the phase noise analysis of the implemented VCO are presented.



noisefreq	pnmx
10.00 Hz	-42.77 mdBc
12.59 Hz	-3.041 dBc
15.85 Hz	-6.038 dBc
19.95 Hz	-9.042 dBc
25.12 Hz	-12.04 dBc
31.62 Hz	-15.04 dBc
39.81 Hz	-18.04 dBc
50.12 Hz	-21.03 dBc
63.10 Hz	-24.03 dBc
79.43 Hz	-27.02 dBc
100.0 Hz	-30.02 dBc
125.9 Hz	-33.01 dBc
158.5 Hz	-36.00 dBc
199.5 Hz	-38.99 dBc
251.2 Hz	-41.97 dBc
316.2 Hz	-44.95 dBc
398.1 Hz	-47.93 dBc
501.2 Hz	-50.90 dBc
631.0 Hz	-53.86 dBc
794.3 Hz	-56.81 dBc
1.000 kHz	-59.75 dBc
1.259 kHz	-62.68 dBc
1.585 kHz	-65.58 dBc
1.995 kHz	-68.47 dBc
2.512 kHz	-71.33 dBc
3.162 kHz	-74.17 dBc
3.981 kHz	-76.97 dBc
5.012 kHz	-79.72 dBc
6.310 kHz	-82.44 dBc
7.943 kHz	-85.10 dBc
10.00 kHz	-87.71 dBc
12.59 kHz	-90.27 dBc
15.85 kHz	-92.77 dBc
19.95 kHz	-95.21 dBc
25.12 kHz	-97.60 dBc
31.62 kHz	-99.93 dBc

Figure 5.4: Simulation results for VCO noise analysis, the noise voltages of the VCO (the first row left), the phase noise of VCO in SSB spectrum (the first row right), the phase noise values versus noise frequency in table (the second row left), the phase noise in dBc/Hz (the second row right).

5.2.2 PFD and CP noise analysis

Following the phase noise simulation of the VCO, the phase noise modelling of the PFD and CP is done. The schematic of the PFD-CP phase noise analysis is provided in Figure 5.5.

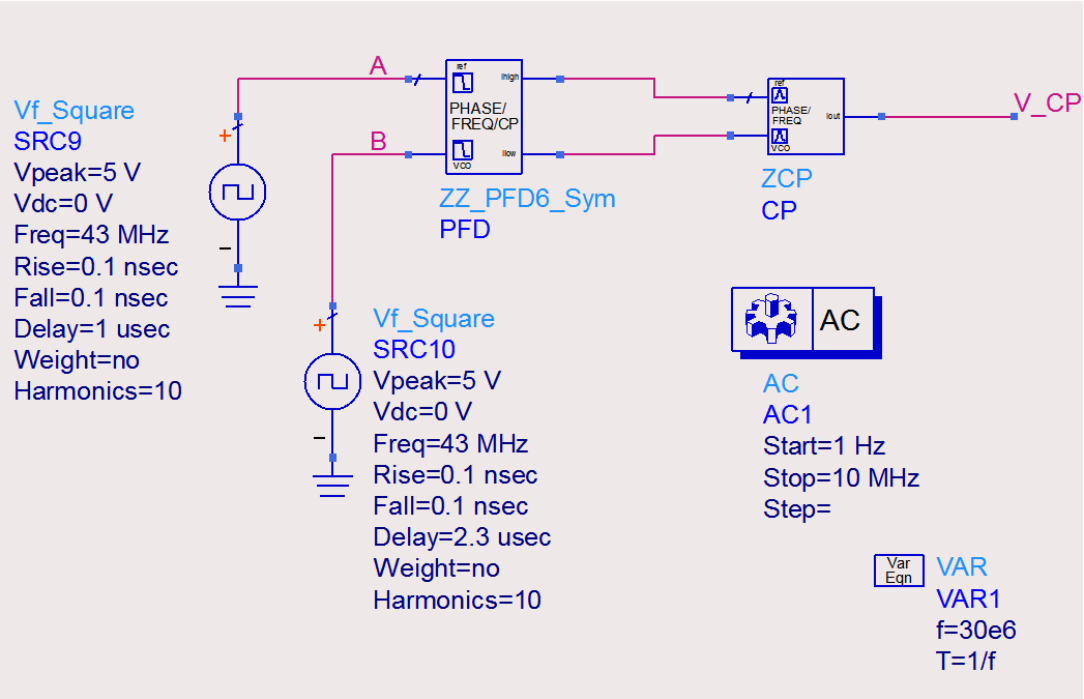
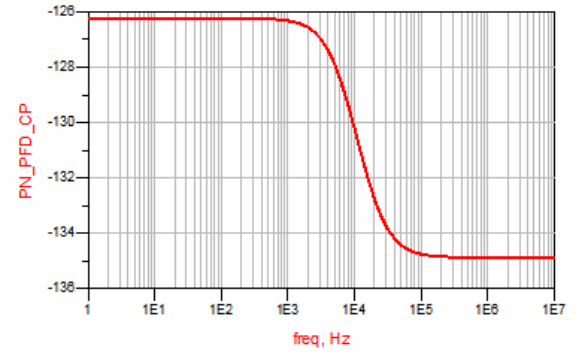


Figure 5.5: PFD-CP noise analysis. The AC analysis is applied to achieve the phase noise analysis.

In Figure 5.6, the noise analysis results of the PFD and CP connection is shown. In this Figure, phase noise results are depicted in SSB spectrum that is derived from the noise voltages values using the equation of 5.1.



freq	V_CP.noise
1.000 Hz	689.6 nV
1.259 Hz	689.6 nV
1.585 Hz	689.6 nV
1.995 Hz	689.6 nV
2.512 Hz	689.6 nV
3.162 Hz	689.6 nV
3.981 Hz	689.6 nV
5.012 Hz	689.6 nV
6.310 Hz	689.6 nV
7.943 Hz	689.6 nV
10.00 Hz	689.6 nV
12.59 Hz	689.6 nV
15.85 Hz	689.6 nV
19.95 Hz	689.6 nV
25.12 Hz	689.6 nV
31.62 Hz	689.6 nV
39.81 Hz	689.6 nV
50.12 Hz	689.6 nV
63.10 Hz	689.6 nV
79.43 Hz	689.6 nV
100.0 Hz	689.6 nV
125.9 Hz	689.5 nV
158.5 Hz	689.5 nV
199.5 Hz	689.4 nV
251.2 Hz	689.2 nV
316.2 Hz	689.0 nV
398.1 Hz	688.6 nV
501.2 Hz	687.9 nV
631.0 Hz	687.0 nV
794.3 Hz	685.4 nV

Figure 5.6: Simulation results for PFD-CP noise analysis. The noise voltages of the PFD and CP (the lower left), the phase noise of the PFD and CP in SSB spectrum (the upper left), and the right one shows the values of the PFD and CP noise voltages versus frequency

5.2.3 Frequency divider noise analysis

The designed frequency divider noise analysis is also implemented. According to the parameter values of the designed PLL, given in Table 5.1, the frequency divider ratio can be selected as 64 or 128. Since, in this thesis study, the frequency divider is designed using D flip-flops. Where, the divider ratio is a power of two. However, the N=64, is selected as the divider ratio. The more the number of the D flip-flops, the high the simulation time. The circuit schematic for noise analysis of the frequency divider is shown in Figure 5.7.

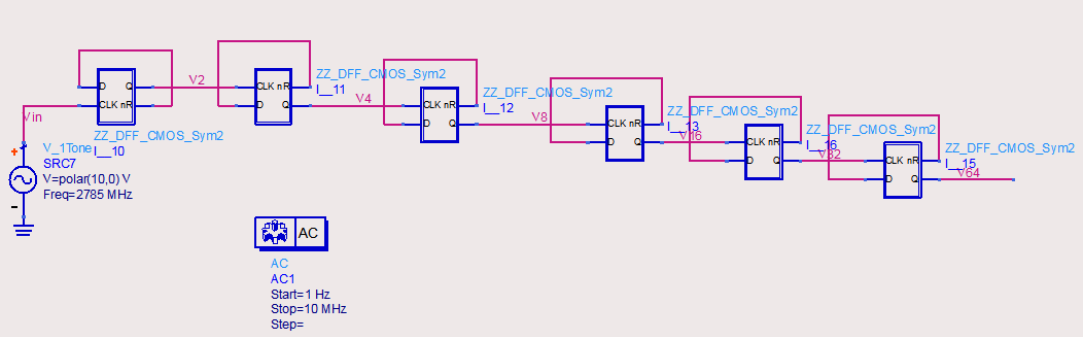
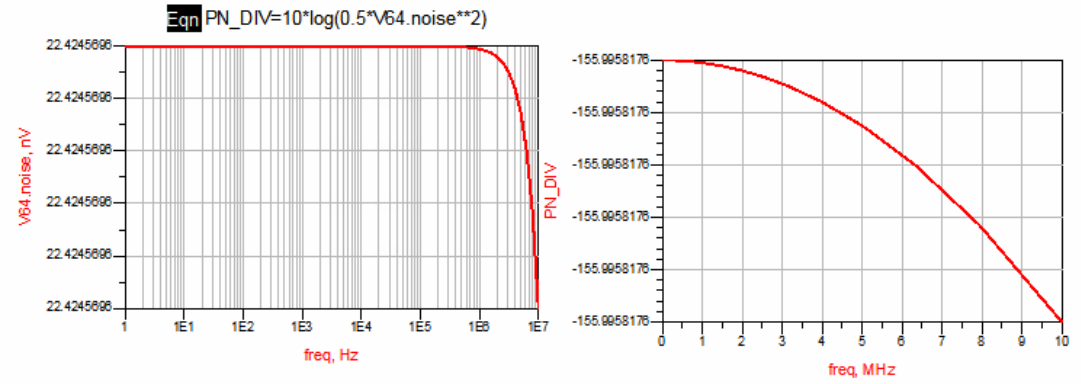


Figure 5.7: Frequency divider noise analysis. The divider ratio is 64, so 6 D flip-flops are used. The AC analysis is applied to simulate the phase noise.

Figure 5.8, illustrates the phase noise analysis results for the implemented frequency divider. The phase noise analysis done for the frequency divider in a same method that is applied for the PFD and the CP analysis.



freq	V64.noise
1.000 Hz	22.42 nV
1.259 Hz	22.42 nV
1.585 Hz	22.42 nV
1.995 Hz	22.42 nV
2.512 Hz	22.42 nV
3.162 Hz	22.42 nV
3.981 Hz	22.42 nV
5.012 Hz	22.42 nV
6.310 Hz	22.42 nV
7.943 Hz	22.42 nV
10.00 Hz	22.42 nV
12.59 Hz	22.42 nV
15.85 Hz	22.42 nV
19.95 Hz	22.42 nV
25.12 Hz	22.42 nV
31.62 Hz	22.42 nV
39.81 Hz	22.42 nV
50.12 Hz	22.42 nV
63.10 Hz	22.42 nV
79.43 Hz	22.42 nV
100.0 Hz	22.42 nV
125.9 Hz	22.42 nV
158.5 Hz	22.42 nV
199.5 Hz	22.42 nV
251.2 Hz	22.42 nV
316.2 Hz	22.42 nV
398.1 Hz	22.42 nV
501.2 Hz	22.42 nV
631.0 Hz	22.42 nV
794.3 Hz	22.42 nV

Figure 5.8: Simulation results for frequency divider noise analysis. (the fist row left) noise voltages of the frequency divider, (the fist row right) phase noise of the frequency divider in SSB spectrum, (the second row) gives the noise voltage values of the frequency divider in table.

5.2.4 CPPLL noise analysis

In this section, to achieve the phase noise analysis of the aimed PLL, the noise analysis for the VCO, CP, PFD and frequency divider is applied. Then, the S-domain PLL model of the desired CPPLL is constructed. The noise models shown in Figure 5.9 are used. Eventually, by applying each block's noise to the output of that port, the phase noise of the closed loop PLL is shaped. The circuit schematic of the achieved PLL model is depicted in Figure 5.10.

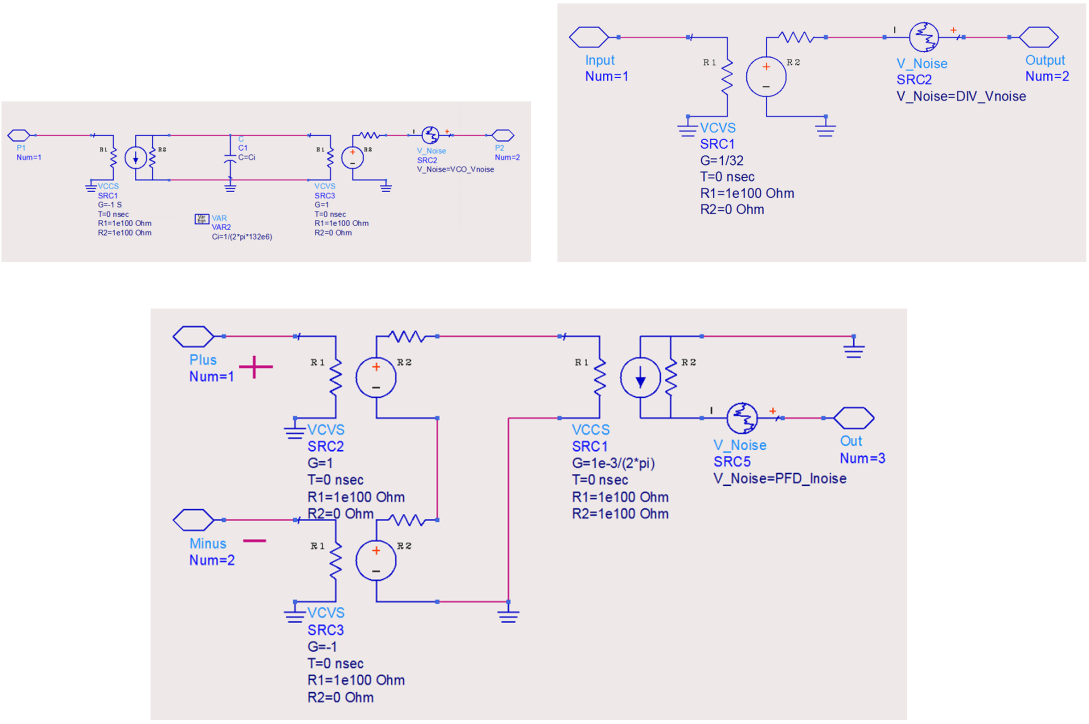


Figure 5.9: CPPLL components noise models. Noise model of the VCO (the fist row left), noise model of the frequency divider (the fist row right) and noise model of the PFD and CP (second row).

The obtained simulation results for the aimed CPPLL noise analysis is given in Figure 5.11 and Figure 5.12. Figure 5.12, provides a comparison of the phase noise analysis of the implemented VCO and achieved PLL with VCO inside.

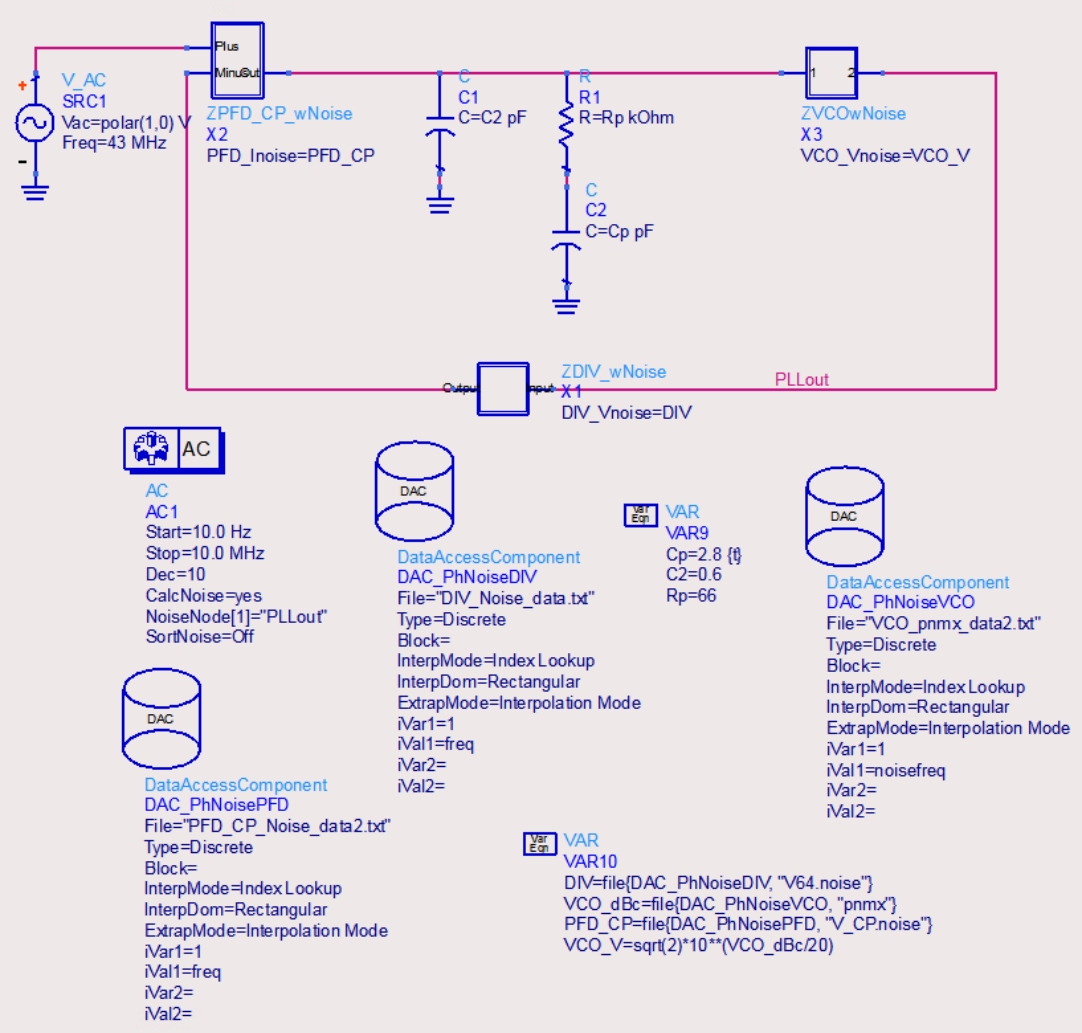


Figure 5.10: PLL noise analysis. Each Data Access Component (DAC), in this circuit, contains the noise data, we have saved using the noise voltage values that are shown in tables for each block of the PLL. The AC nalysis is applied to get the phase noise analysis of the PLL.

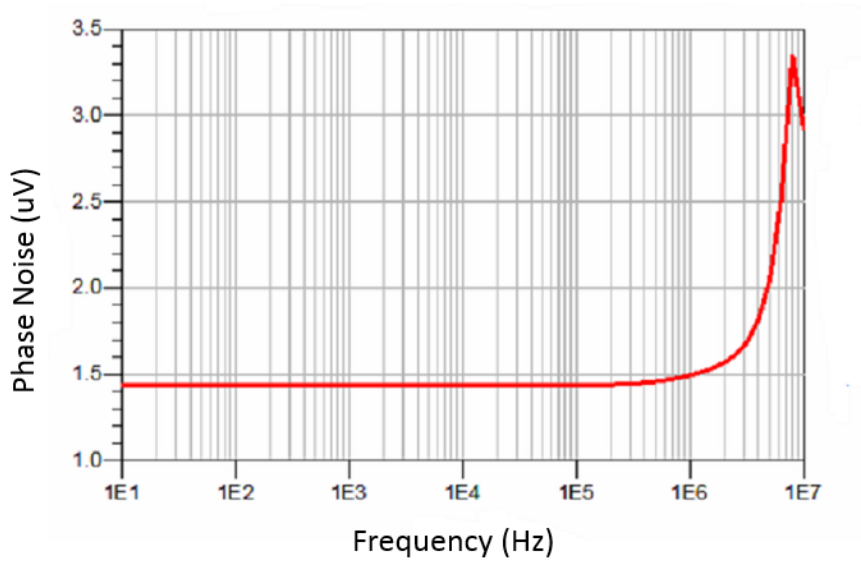


Figure 5.11: Simulation results for the CPPLL noise analysis.

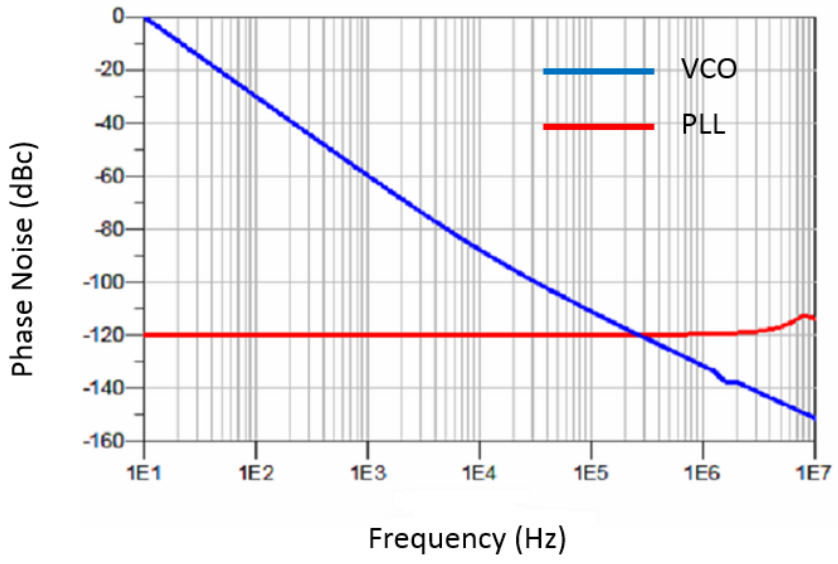


Figure 5.12: Simulation results for the CPPLL noise analysis. Phase noise comparison between the implemented VCO and the resultant PLL.

According to the Figure 5.12, the phase noise of the VCO is reduced while applying the PLL loop around the VCO. Especially, the phase noise reduction is obvious in low frequencies. The main goal of this thesis study was the low phase noise achievement in low frequencies. The PLL contributes the phase noise of -120 dBc/Hz at 100 Hz, while the VCO has -32 dBc/Hz phase noise at 100 Hz. Therefore, the phase noise reduction performance of the PLL is considerable.

As seen in Figure 5.10, the reference oscillator's noise is ignored. However, if the reference oscillator noise is also take into account, the resulted noise analysis is depicted in Figure 5.13. The noise analysis results are shown in Figures 5.14 and 5.15.

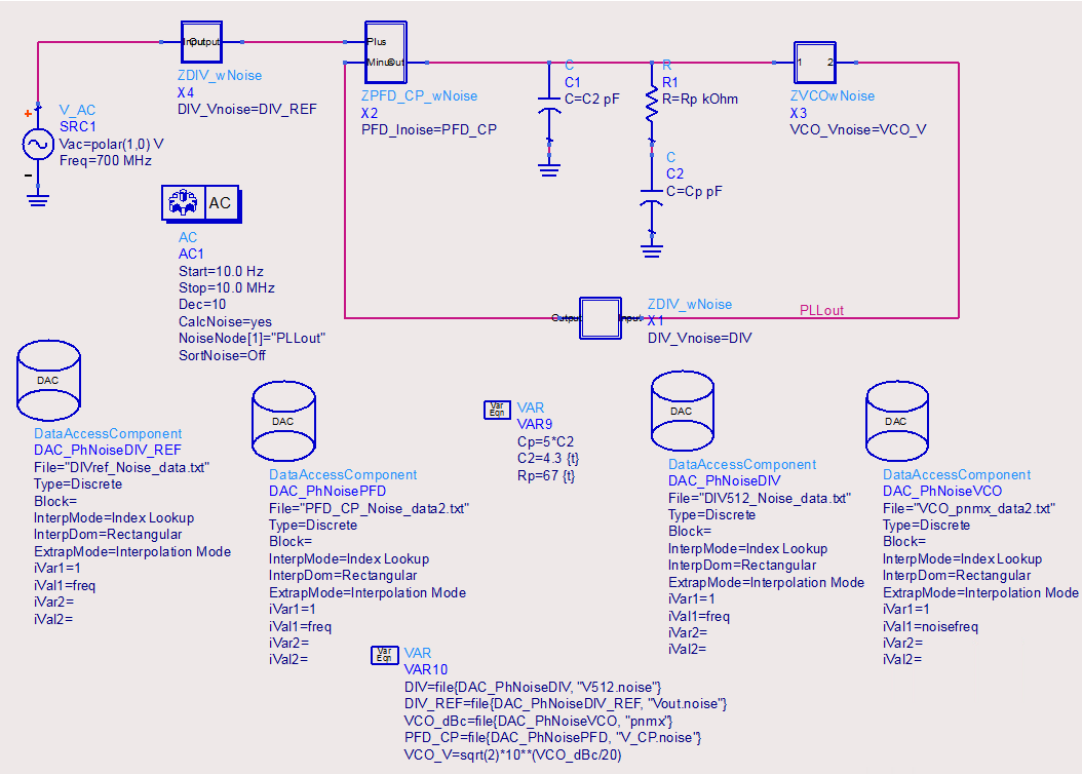


Figure 5.13: Noise analysis of the CPPLL considering the reference oscillator's noise.

In Figure 5.13, in addition to the internal frequency divider, that is placed in the feedback loop, the external frequency divider is also added. Therefore, for the added frequency divider an extra DAC, is also used. The same approach as the CPPLL noise analysis without the external oscillator noise contributor, is applied.

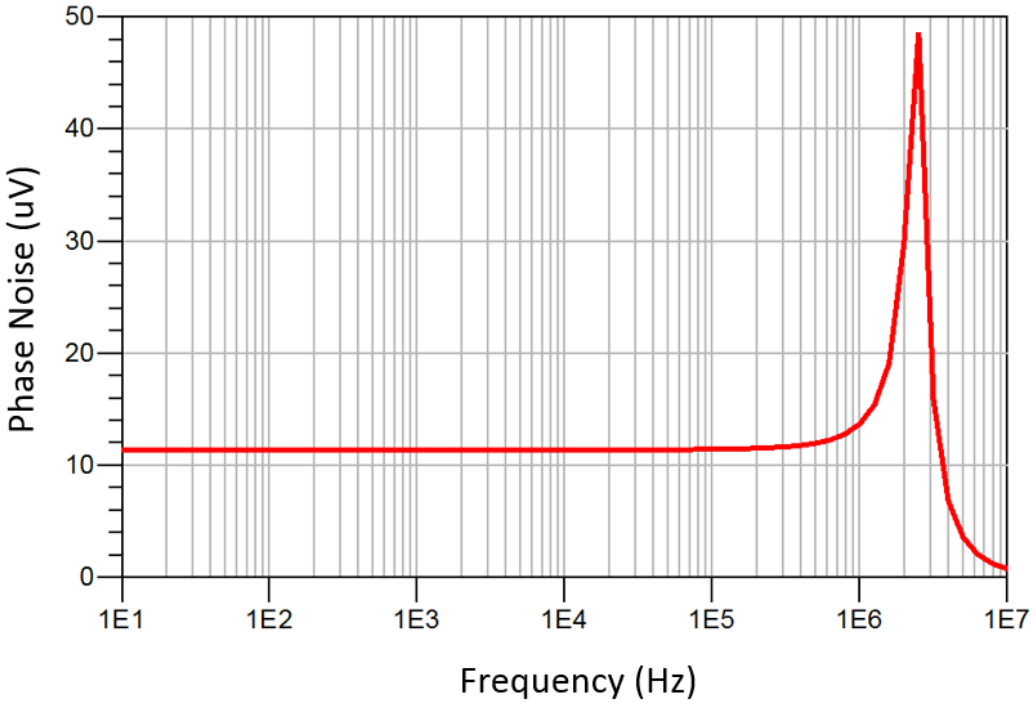


Figure 5.14: Simulation results for the CPPLL noise analysis.

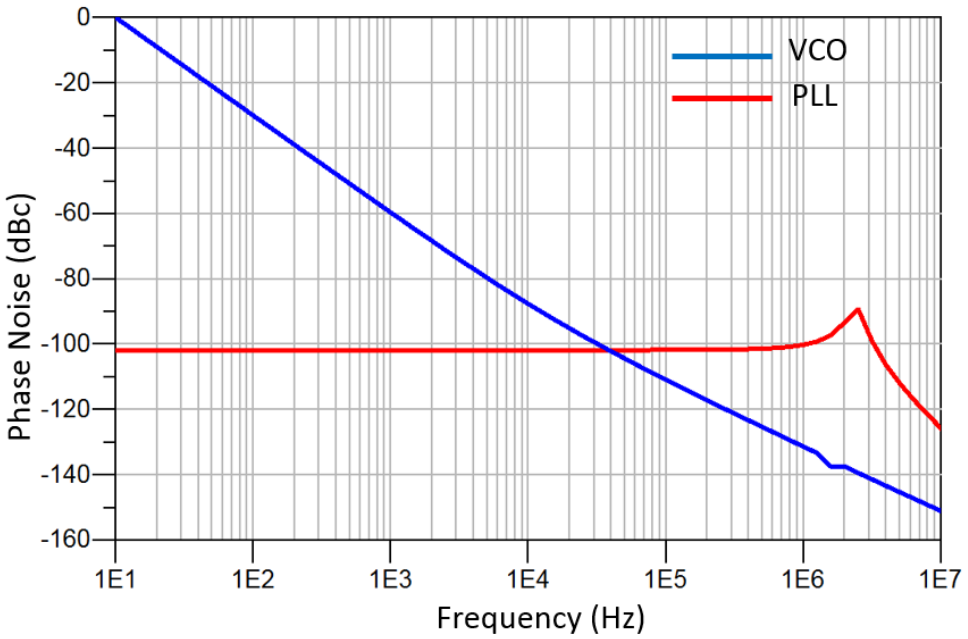


Figure 5.15: Simulation results for the CPPLL noise analysis. Phase noise comparison between the implemented VCO and the resultant PLL.

According to the phase noise analysis results, while the reference oscillator's noise is take into account, the PLL phase noise is increased about 20 dB. However, the behaviour of the PLL in reduction of the VCO phase noise is the same.

CHAPTER 6

CONCLUSION AND FUTURE WORK

In this thesis study, the design of a low phase noise CPPLL at 2.8 GHz for the microwave transmitter of the HMMDI, is presented. In HMMDI method, a microwave signal (a few GHz) is transmitted to the vibrating tissue (as a result of ultrasound excitation). The backscattered signal consists of a signal at the carrier frequency (operating microwave frequency) and a signal at vibration frequency (Doppler frequency). The vibration frequency is in the range of a few Hz. To realize this signal, the phase noise of the transmitter should be low.

A Phase locked Loop (PLL) as a circuit block to decrease the phase noise is selected. Different building blocks of the PLL including the VCO, frequency divider, PFD, CP and loop filter are designed using ADS. A gate grounding Colpittes VCO using HEMT transistor is designed. HEMT transistor is preferred because it has low noise figure and it can operate at high microwave frequencies. The Colpittes VCO is designed using capacitor and varactor. In the capacitor version, the capacitor is tuned manually but in the varactor version, the capacitance changes by varying the applied voltage. Using the capacitor, the obtained phase noise is -137.64 dBc/Hz at 1 MHz and using the varactor it is -131.434 dBc/Hz. The simulated VCO provides an oscillating frequency of around 2.7 GHz.

To bring the output frequency of the VCO to MHz frequency range provided by the external crystal oscillator (reference signal) a frequency divider is used. The frequency divider is simulated first using the D flip-flop blocks of the ADS and then by the analog D flip-flop designed by the CMOS transistors. The CMOS D flip-flops are preferred to simulate the phase noise of the PLL.

Commonly used PFD in PLL applications (basic PFD) was designed to detect the phase differences of the reference signal and the VCO output after passing through the frequency divider. Since HB simulation can not be run for phase noise analysis while using built-in blocks of ADS in the DSP library, the analog PFD is designed in transistor level using CMOS transistors. The phase noise of the PLL is simulated using this type of PFD.

To generate the control voltage for the VCO, a CP followed by a loop filter is considered. The output voltage of the CMOS CP fluctuates according to the phase error of the PFD and reaches to the steady-state when the error is nearly zero.

The PLL is simulated in ADS. In the designed PLL, the above mentioned VCO using HEMT transistor, the CMOS CP, the basic PFD, and the frequency divider using DFFs are used. The performance of the PFD and the CP are evaluated in a separate simulation. Other PLL components are also simulated individually.

Although the obtained control voltage of the VCO reached to the steady-state and the frequency of the obtained VCO signal was 3.5 GHz, the HB simulation could not be converged. HB simulation analyze the signals in the frequency domain. Since the output of the frequency divider is a rectangular signal, there exist a lot of harmonic components. Therefore, the HB simulation can not converge and hence the phase noise could not be obtained.

In order to analyze the phase noise. PLL is linearised and the parameters of each block were analytically calculated. For each block of the PLL loop the phase noise was simulated. The S-domain PLL model was generated. The loop was closed after adding the noise at specific points. Assuming noiseless crystal oscillator, the phase noise was -120 dBc/Hz at 100 Hz offset. The phase noise was decreased successfully 90 dBc compared to the VCO phase noise (-32 dBc/Hz at 100 Hz). While the noise of crystal oscillator is included, the phase noise at 100 Hz reached to -101 dBc/Hz.

The results show that the PLL loop method has a potential of decreasing the phase noise of the oscillator.

In the future work the following studies can be performed:

The phase noise of the designed VCO can be improved. Other VCO topologies using CMOS transistors can be designed. The resonator tank with high Q (Quality factor) can be used,

In frequency divider design the dual modulus dividers can be examined. The frequency divider can be designed programmable leading to fractional PLL frequency synthesizers,

Alternative PFDs including the latch based PFD, MPTPFD, and Falling-Edge PFD can be designed,

In the CP design, applying a differential CP can be useful. The CMFB circuitry will also be added to the loop filter in differential CP design,

All the implementations in this thesis are conducted in schematic level. The studied PLL is simulated using the CMOS transistor models in standard libraries of ADS except the VCO that is designed using a single HEMT transistor. In future the investigated PLL can be implemented in IBM 7RF SOI process.

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