A COMPREHENSIVE STUDY ON RF ENERGY HARVESTERS: MODELLING, DESIGN, AND IMPLEMENTATION

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2016

Approval of the thesis:

A COMPREHENSIVE STUDY ON RF ENERGY HARVESTERS: MODELLING, DESIGN, AND IMPLEMENTATION

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Name, Last name: Kaveh Gharehbaghi

Signature:

To ma

And memory of grandma

ABSTRACT

A COMPREHENSIVE STUDY ON RF ENERGY HARVESTERS: MODELLING, DESIGN, AND IMPLEMENTATION

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September 2016, **145** pages

The Dickson and the threshold self-compensated UHF rectifier architectures are investigated in detail. At first, the Dickson architecture is studied by aiming to find an accurate yet general input-output relationship. It is revealed that the ratio of peak forward current over the load current could be well approximated for broad range of incoming RF amplitudes. For threshold self-compensated UHF rectifiers, a behavioral model is presented for core unit of the structure to ease the analytical discussions. Then, a model is elaborated by noticing the steady-state waveforms at different nodes. Then the coherence between the dependence of the load current and power conversion efficiency over the variation of the generated DC voltage is used for finding the optimum design parameters of the structure.

In circuit design level, two novel architectures are introduced. The first one is threshold-compensated UHF rectifier with "self-calibration technique" which avoids the reduction of power conversion efficiency over the increment of the incoming RF signal. The idea is to separate the compensation-generator from the main rectifier by adding two auxiliary rectifiers. Second circuit for UHF rectifiers is "switched-gate" architecture [1] which increases the peak power conversion efficiency. The method is

based on adaptive threshold-compensation which establish different gate-source voltage for the diodes during the forward and reverse conduction phases.

Analysis of conjugate matching and passive Q-boosting methods for interfacing between antenna and rectifier is also conducted. At the end, a novel reference block is designed by reducing the power consumption of the voltage reference down to 89 nW while providing temperature/supply independent reference.

Keywords: RF Energy Harvesters, Analysis and modeling of UHF rectifiers, Design of UHF rectifiers, Antenna-Rectifier interface design, Ultra low power voltage reference circuit design.

ÖZ

RF ENERJİ DEPOLAMA DEVRELERIN TASARIM VE KAPSAMLI İNCELEMELERİ: MODELLEME, TASARLAMA, VE GERÇEKLEŞTİRMEK

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Eylül 2016, **145** sayfa

Dickson ve eşik değerini kendi dengeleyen UHF doğrultucu yapıları ayrıntılı bir biçimde araştırılmıştır. İlk olarak, Dickson yapısı doğru ama genel girdi-çıktı ilişkisinin bulunması amaçlanarak irdelenmiştir. İleriye tepe akımının yük akımına oranının geniş bir dizi halindeki gelen RF genlikleri için çok yaklaşık olacağı ortaya çıkarılmıştır. Eşik değerini kendi dengeleyen UHF doğrultuculara yönelik, yapının çekirdek biriminin çözümsel irdelenmesini kolaylaştıracak bir davranışsal model sunulmuştur. Model farklı düğümlerdeki kararlı dalga biçimleri önemsenerek detaylı olarak incelenmiştir. Daha sonra, yük akımının bağımlılığı ve güç dönüşüm verimliliği ile üretilen DC voltajın değişme miktarı arasındaki tutarlılık yapıya en uygun tasarım parametrelerinin bulunması için kullanılmıştır.

Devre tasarım düzeyinde iki yapı tanıtılmıştır. Bunlardan ilki gelen RF sinyalinin artışı üzerine güç dönüşüm verimliliğinin düşürülmesini önleyen, kendini ayarlayabilme özelliği ile eşik değerini dengeleyen UHF doğrultucusudur. Temel düşünce dengeleme-jeneratörünün ana doğrultucudan iki yardımcı doğrultucu eklenerek ayrılmasıdır. UHF doğrultucuları için ikinci devre tepe gücü dönüşüm verimliliğini arttıran "anahtarlamalı-kapı" yapılarıdır. Buradaki genel kavram ileri ve

ters iletim evreleri süresince diyotlar için farklı kapı-kaynak voltajını tesis eden "uyarlanabilir dengeleme"dir.

Anten ve doğrultucu arasındaki ara yüz için eşlenik eşleştirme ve pasif Q-artırma metotlarının analizleri de incelenmiştir. En sonunda, sıcaklıktan/beslemeden bağımsız referans sağlamakla birlikte 100 nW'nin altındaki voltaj referansının güç tüketimini azaltarak özgün bir referans bloğu tasarlanmıştır.

Anahtar Kelimeler: RF enerji hasatçı,UHF doğrultucu analiz ve modelleme, UHF doğrultucu tasarımi, Anten-doğrultucu arayüzey tasarımi, Ultra düşük güç referans Voltaj devre tasarımi.

ACKNOWLEDGEMENTS

I would like to thanks my family for their continuous support during my studies. All of my commitment to life and academic ethics are rooted by the lessons that I learned for years from them.

Then, I would like to thank my advisor Prof. Dr. Haluk Külah for his endless support during my times at the Middle East Technical University. He trusted me when I joined the university and always gave me opportunity to show my abilities. My largest desire at the end of my Ph.D. degree is to prove him right. Also, I am very grateful for enormous time and energy my co-advisor Dr. Fatih Koçer spent with me on my thesis. Also, his technical feedback has had great impact on improving my research.

I would also like to thank Dr. Ali Muhtaroglu, Prof. Tayfun Akın and Dr. Ozge Zorlu for their invaluable support for my research. Working with Dr. Muhtaroglu was one of the greatest chances I had in my life and I am so pleased to learn many things about IC design form him. The feedbacks I received from Prof. Akın in semi-annual thesis meetings helped me a lot to increase the impact of my research and identify the parts that require more investigation. Dr. Zorlu always motivated me toward doing better research and thinking positively. I will never forget the good moments of my collaboration with Dr. Zorlu. I would also like to express my greatest regards to Dr. Adnan Gundel for sharing his carrier experiences with me.

I would also like to specially thank my lab mates at METU. I specially thank Dr. Yekbun Adiguzel, Dr. Hatice Ceylan Koydemir, Dr. Dilek Işik, Aziz Koyuncuoğlu, Garsha Bahrieh, Levent Beker, Yağmur Demircan, Deniz Eroglu, Hasan Ulusan, Nasim Esmailzadeh, Parisa Naghinezhad, and finally METU orienteering group for all of their kindness and good memories.

My dear friends in Iran and Turkey makes my Ph.D. degree full of good memories and I am grateful to all of them. I take this opportunity to express my thanks to Dr. Gholamreza Zare Fatin, and Nabi Shiri for their support and helping me to be a better person.

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CHAPTER 1

1 INTRODUCTION

The demand for generating a sustainable supply chain to replace the batteries in portable electronic devices is growing steadily. Replacing batteries is especially important for emerging modern platforms such as wireless sensor networks (WSN), radio frequency identification (RFID), and internet of the thing (IoT) systems [2]. In these systems, there are many devices (sensors or tags), which should transmit data to the base station for further processing. Realizing battery-free operation of these devices drastically increase the feasibility of such systems thanks to reduced maintenance costs, widened application areas, and clean energy utilization. Battery-free operation may become possible by introducing energy harvesting devices in these systems. The key motivations behind substituting batteries with energy harvesting approaches are as follows:

i) Batteries require periodic replacement by human interference which may be troublesome specially when the sensors are located at inaccessible locations

ii) Physical volume of the sensors significantly increases by adding the battery, which is not desirable in many applications such as implantable healthcare devices [3] and tire pressure monitoring systems [4]

iii) The ingredients of typical batteries include heavy metals and toxic chemicals which are harmful for the environment.

Figure 1-1 shows the application of energy harvesting in a portable sensor system. The environmental energy is converted to electrical energy by means of a transducer. The required energy input to the transducer can be in many forms such as vibration [5], solar [6], thermal [7], and radio frequency (RF) [8]. In some cases, like solar and thermal energy harvesting, the electrical signal at the output of the transducer is in the DC form. However, for RF or vibration based energy harvesting, the generated electrical energy by the transducer comes in the AC form and should be converted to the DC form through a rectifier. Regardless of the type of the electrical energy provided by the transducer, a boosting circuitry is required to increase the DC voltage to the operable level of the electronic circuits. An energy storage component (supercapacitor or rechargeable battery) stores the harvested energy and delivers it to the load when power management network acknowledges the availability of sufficient energy, with which the microcontroller

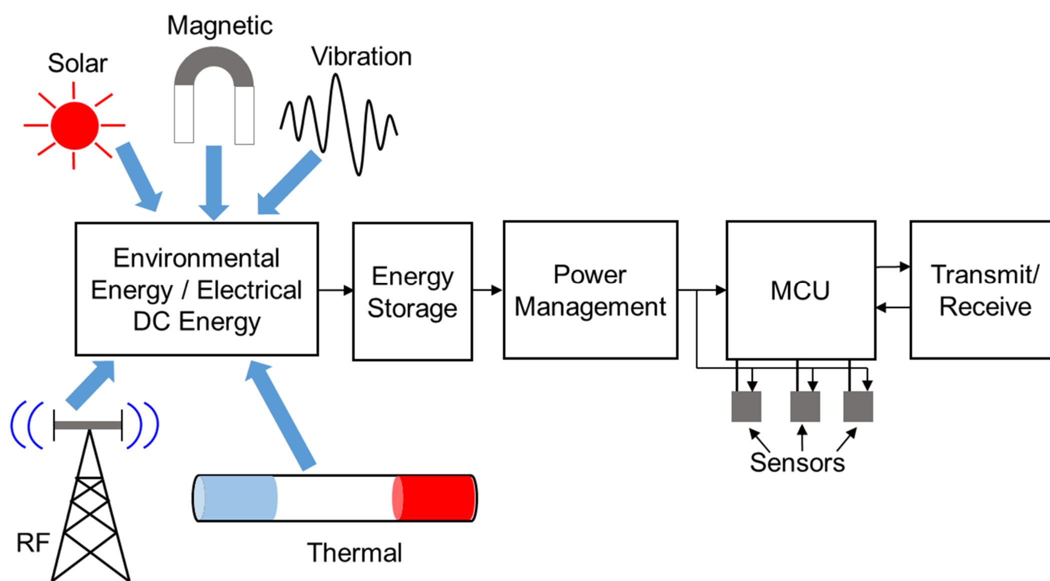


Figure 1-1: A typical energy harvesting WSN system for collecting the environmental data.

unit (MCU) performs required data processing assignment. The key motivations behind substituting batteries with energy harvesting approaches are as follows: *i)* Batteries require periodic replacement by human interference which may be troublesome specially when the sensors are located at inaccessible locations *ii)* Physical volume of the sensors significantly increases by adding the battery which is not desirable in many applications such as implantable healthcare devices [3] and tire

pressure monitoring systems [4] *iii)* The typical batteries contain heavy metals and toxic chemicals which are harmful for the environment.

There are many methods to alleviate the demand for battery in portable electronic devices by converting some of the environmental energy like vibration [5], solar [6], thermal [7], and radio frequency (RF) [8] into DC power. RF energy harvesting uses electromagnetic waves in ambient air as the energy source to provide DC power and is proved to be a promising solution for fully-autonomous (battery-free) infrastructures. Some key advantages of RF energy harvesting which makes it attractive for many modern applications can be summarized as below.

- **Ability to work at any time and any place:** Unlike the solar energy harvesting which could be used only during the daylight hours or vibration based energy harvesters which require some sort of mechanical stimulation, RF harvesting could be used at any time and could be employed in both indoor and outdoor applications.
- **Abundance of RF power in urban areas:** RF power is freely available in urban area since it is propagated by many resources like mobile and TV towers. Modern mobile communication systems operate at different standards such as GSM, WLAN, Wi-Fi, and Bluetooth, while their carrier frequency spans between 800 MHz and 2.5 GHz. These signals can be harvested to provide power in μW range, based on the availability of one [9] or more [10] of these aforementioned resources.
- **Robustness against variation of environmental parameters like motion, humidity and temperature:** RF energy harvesting systems mostly use isotropic antennas at the transmitter side [11] and the received RF power becomes independent of the relative phase of base station and the user node. Also, the performance of RF energy harvesting systems do not degrade over the variation of the environmental parameters like daylight and temperature while the system only requires sufficient electromagnetic power.

In contrast, proper operation of solar cells asks for accurate aligning of the cell with the sun at specific angle which could be destructed by possible motion of the harvesting module. While in periodic motion stimulates of vibration-based energy harvester (e.g. electromagnetic or piezoelectric), temperature variation could shift the natural frequency of the resonating structure which is not desirable.

In general, the RF power is fed to the antenna by using either deliberate (like insertion of a base station at the vicinity of the remote device) or ambient RF source (like mobile and TV stations). Typically, the transmitted power by the base station in addition to the power loss of the propagated electromagnetic waves through the air (path loss) determines whether the ambient energy harvesting would be sufficient for the application. Before discussing about the restrictions on transmitted power and path loss, it is worthwhile to stress that in RF domain, it is common to express the power levels in dBms, which is the abbreviation for the power in decibel (dB) with reference to 1 mW:

$$P_{dBm} = 10log\left(\frac{P}{1mW}\right) \tag{1-1}$$

Friss equation [12] is the principal relationship in communication systems which determines the amount of attenuation by electromagnetic waves propagated through the air:

$$P_r(dBm) = Pt(dBm) + G_t(dBm) + G_r(dBm) - 20log10(f_{MHz}d_{km}) - 32.4418 \tag{1-2}$$

where P_r is the collected power at the receiving antenna, P_t is the power input to the transmitting antenna, G_t and G_r are the gain of the transmitting and the receiving antenna, f is the signal frequency, and d is the distance of the power communication path (from the base station to the remote device). From (1.2), it can be seen that the amount of power incident on the receiver decreases by increasing the communication distance and the signal frequency. Hence, the reader may wrongly conclude that it would be better to decrease the frequency of signal as low as possible to minimize the path loss. However, it should also be noted that the radiation efficiency of the antenna (which propagates and collects the RF power) maximizes when the wavelength of the signal λ becomes comparable with the antenna dimensions. Hence, in order to limit the antenna size within several centimeters, the signal frequency should be in UHF band (between 300 MHz and 3 GHz, corresponding to λ of 100 and 10 cm, respectively).

1.1 Cycles of WSN Systems

Understanding the different operation modes of sensor nodes in WSN systems is necessary to gain insight for the design procedure of RF harvesters. In WSNs, having

multiple operation modes is inevitable since the amount of collected power by the RF harvester typically is not enough for continuous operation of the battery-free sensor. It is mostly due to the following reasons:

- **Considerable path loss:** As presented in (1.2), if the distance of the communication doubles, the received power reduces by a factor of four. In practice, it could be even worse due to multi path fading which is the arrival of several versions of the transmitted wave to the receiving side (which could be added or subtracted from the main signal due to their relative phase) by reflection from the adjacent objects. This problem is especially severe in indoor applications. The result is that the collected power could be decreased by $1/d^3$ due to multipath fading according to standard international telecommunication union (ITU) propagation model [13].
- **Limited propagated RF power:** The amount of the transmitted power is restricted to some extent since extreme RF powers could be harmful for humans. To be more specific, the amount of the transmitted RF power is limited to maximum permissible exposure (MPE) by federal communication commission (FCC) regulations [14], while higher powers could heat the body tissue [15]. For example, the amount of power transmitted at 900 MHz is limited to 4 W according to FCC regulations.

The outcome of the mentioned restrictions on the receiving and transmitting RF power is having the available RF power on the receiver side in μW-levels. This degree of input energy is not enough for continuous operation of the sensor devices which typically include data processing and transmission (with ASK [16], PSK [17], or FSK [18] modulation) functions. As a result, duty-cycled strategy should be devised. One of the well-known power management strategies is the charge and burst strategy in which the sensor waits until the stored voltage (on a super capacitor) reaches to a predefined value and then burst the power to accomplish the listen/transmit phase [18] (Figure 1-2).

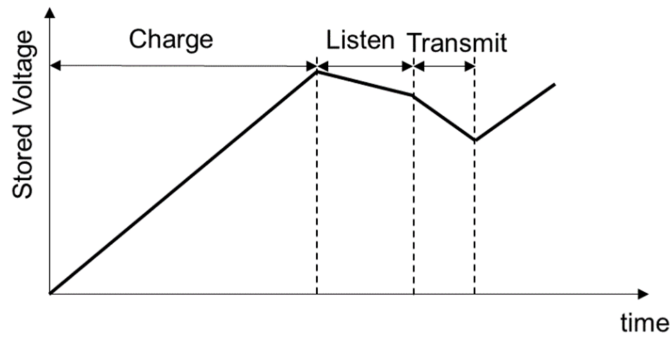


Figure 1-2: Different cycles of remote sensing device in a WSN system.

Understanding the different operation modes of the device, the designer could estimate the amount of the load that must be driven by the RF harvester during the charging phase. Typically, this current is defined by the over-voltage protection circuitry, the charging current of the storage capacitor and the current by the front-end power management circuitry. The power management units typically employ an ultra-low-power voltage reference [18] or a n-W voltage sensor [19] to be aware about the availability of the sufficient power during the charging phase. In general the dissipated power at the load side of the RF harvester during the charging phase is between 1 to 10 μA [20].

1.2 RF Energy Harvesting System

The general block diagram of an RF energy harvester system is shown in Figure 1-3. The incoming RF signals (transmitted by ambient or deliberately-inserted sources) are collected by the antenna. Then an impedance matching network, inserted between the antenna and the UHF rectifier, targets delivery of maximum power to the rectifier portion within certain frequency bandwidth. Ideally, the impedance seen by the antenna at its feeding port should be conjugate of the internal impedance of the antenna. In this way, no power is reflected from the load to the RF source and all collected power will be delivered to the load assuming that the impedance matching network is constructed with reactive components (with negligible loss).

Multistage UHF rectifier sub-circuit could be implemented with half or full wave rectifiers and has two functions: *i)* convert the AC signal into DC form and *ii)* boost up the DC level to attain the output voltage required by the device. Finally, power management block senses the DC voltage at the output of the UHF rectifier and sets

it to a predefined level. The UHF rectifier sub-block of the overall RF energy harvesting system is the major focus of this thesis, and will be further discussed in detail in the following chapters.

To better analyze the behavior of the system and gain insight about the functionality of it, the antenna and rectifier is modelled with passive components. As shown in Figure 1-3, antenna could be modeled by a voltage source in series with a complex impedance $R_{ant} + jX_{ant}$. The real part of the antenna impedance(R_{ant}), is composed of two components; the resistive loss of the antenna (R_S) and the radiation resistance (R_A) [21]. The reactive part of the antenna impedance (jX_{ant}) models the energy stored in the near field of the antenna and could be capacitive or inductive depending on the antenna type and operating frequency. The ideal voltage source represents the collected RF power using an ideal sinusoidal waveform with amplitude of V_{ant}, which can be calculated as:

$$V_{ant} = \sqrt{R_A G_A P_{EIRP}} \frac{\lambda}{2\pi d} cos\theta \tag{1-3}$$

where G_A is the gain of the antenna, P_{EIRP} is the equivalent isotropic radiated power, λ is the wavelength, d is the distance of communication, and θ is the misalignment angle between the electrical field of the antenna and the incoming wave.

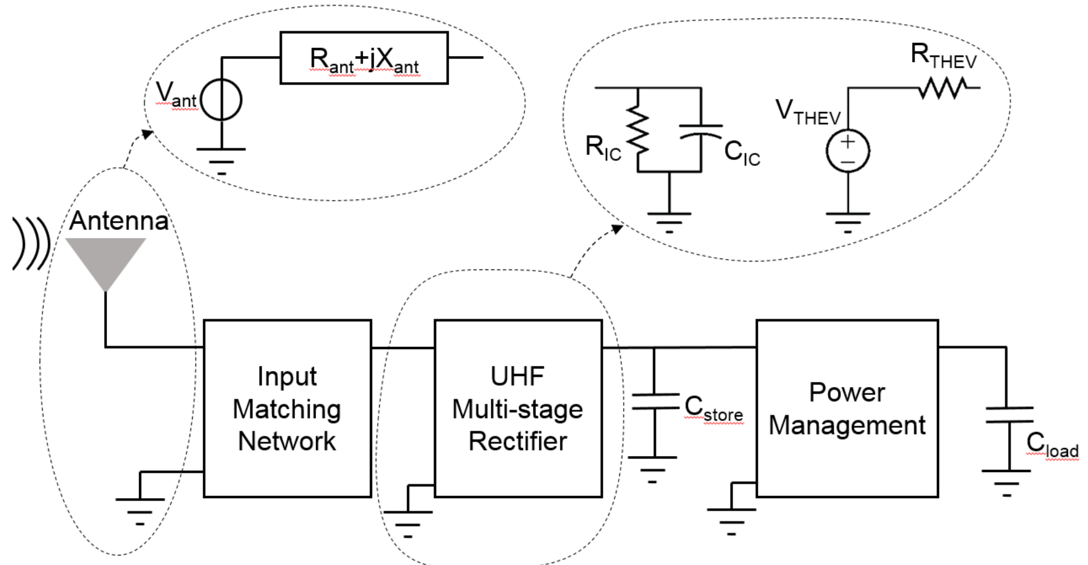


Figure 1-3: General block diagram of an RF energy harvesting system.

The model for the UHF rectifier is also presented in Figure 1-3. The internal components of the UHF rectifier are all resistive or capacitive. Also, the output voltage of UHF rectifier is a DC (by assuming that storage element is large enough to suppress the ripples).Hence, the input impedance of the rectifier is modeled by a shunt *R//C* network, while the output portion is modeled by a Thevenin equivalent circuit (to illustrate the generated DC voltage by the rectifier) to represent the output resistance and the output resistance [22]. As demonstrated in the following sections, accurate representation of the input impedance of the UHF rectifier is of paramount importance during the optimization procedure of the whole RF harvesting system. Output impedance of the rectifier is less important in the design procedure of the RF harvester interface, and gains significance in the design of power management unit. The output resistance of the rectifier is especially important during the calculation of the stability and response time of the low drop-out power management circuitry [23]. This subject is beyond the scope of this thesis and will not be detailed.

1.2.1 Antenna:

The electromagnetic waves emitted by the RF source are collected with an antenna and are used to generate µ-W level DC supply in the RF energy harvesting system. The primary goal of the antenna design for RF energy harvesting applications is to provide maximum RF amplitude for available power. Having higher RF amplitudes is desirable since, on one hand, it directly increases the amount of the DC voltage at the load side. On the other hand, the PCE of UHF rectifiers tends to decrease with decreasing input RF amplitude. From (1-3) it can be deducted that the antenna gain and the radiation resistance are the two design parameters that could be employed to increase the amplitude of the signal for a given RF power. The term G_A is the *power gain* and is defined as the ratio of radiation intensity of the antenna at a point to the radiation intensity of an antenna with uniform radiation with the same input power,

$$Gt = 4\pi \frac{radiation\ density}{total\ input\ power} \tag{1-5}$$

Dipole ([16], [24]), folded-dipole [25], and loop antennas [9] are the most common architectures employed in RF-to-DC converters. Antenna design is out of the scope

of this thesis and will not be detailed. Interested readers are encouraged to check [26] which provides a thorough discussion of antennas for UHF energy harvesting systems.

1.2.2 UHF Rectifiers: Survey and Comparison

This sub-section introduces the most common architectures used to convert the RF signal into the DC form. The structures selected here are used in short and long range power communication systems and are able to operate at UHF band. The architectures selected to be investigated are listed below:

I. Dickson and Villard rectifiers
II. Threshold compensated rectifiers
III. Differential-drive Bridge rectifiers

1.2.2.1 Dickson and Villard Rectifiers

Circuit diagram of the Dickson [27] and the Villard topologies [28] are shown in Figure 1-4. As can be seen, their circuit diagrams are very similar except for the configuration of the coupling capacitors. Peak PCE of both structures could reach 80% when RF power is about -5 dBm [29]. In the Dickson rectifier, the bottom plate of all coupling capacitors are connected to the input RF node while in the Villard topology, the bottom plate of the coupling capacitor is connected to the top plate of the coupling capacitor from the previous stage. This could modify the input impedance of the IC and the selection between the two could be done by noticing the requirements of the impedance matching network [29]. According to [30], the performance of both structures are very close to each other. Ideally, the generated DC voltage by each stage of the Dickson rectifier is equal to $2\times V_{RF}$ ($V_{DC}=4\times V_{RF}$ in Figure 1-13(a)). Thus, the Dickson rectifier is also referred to as "Doubler" rectifier, and it is mostly used in RFID tags [31]. The detailed analysis of the Dickson rectifier will be introduced in Section II.

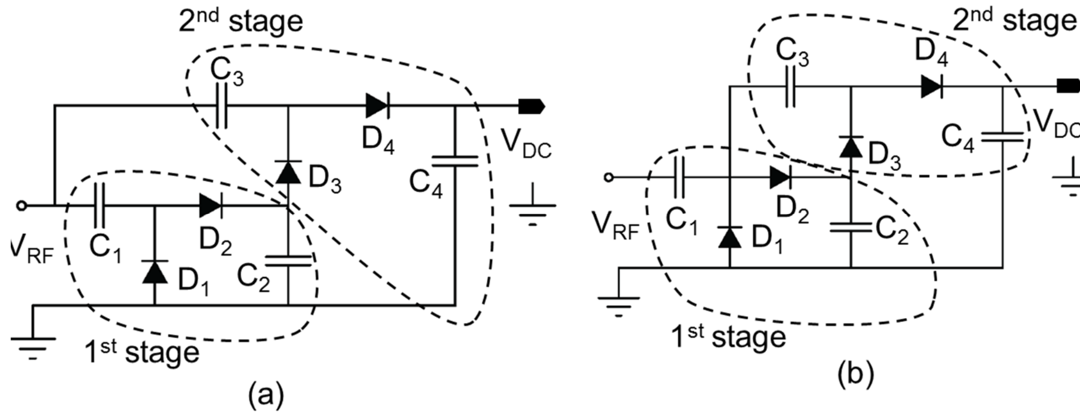


Figure 1-4: Circuit diagram of 2-stage a) Dickson and b) Villard rectifiers.

1.2.2.2 Threshold Self-Compensated Rectifier

Realizing the internal diodes with MOS transistors in Dickson topology (Figure 1.4), some part of the incoming RF signal should be consumed to overcome the intrinsic threshold voltage (V_{th}). Threshold self-compensated rectifier (shown in Figure 1-5) is firstly introduced in [32] to eliminate this problem by modifying the configuration of the gate connections. Unlike the Dickson topology in which the gate terminals are connected to the drain of the transistor itself, the gate terminals are connected to the source of the right-neighboring transistor, which leads to have a positive offset between the gate and the source terminals. The major advantage of the self-compensated topology compared to the Dickson architecture is its superior performance when the RF intensity is below -10 dBm. In [33], peak PCE of 17% is reported at -16 dBm while that of the Dickson architecture barely exceeds 10% at the same power. Similar to the Dickson topology, detailed analysis of the threshold self-compensated rectifier is provided in the Section II.

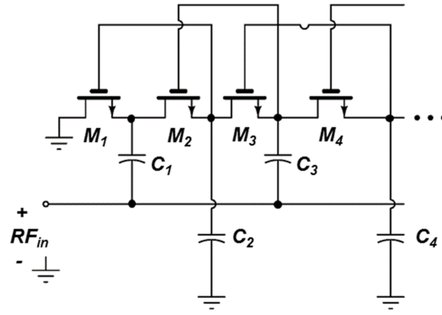


Figure 1-5: Circuit diagram of threshold self-compensated rectifier.

Even though the circuit diagram of the threshold self-compensated rectifier is simple, its design procedure is quite complex. In fact, the amount of the compensation voltage depends on many factors like the RF amplitude, the device aspect ratio and the amount of the connected load. The difficulty in adjusting the single optimum point in the threshold self-compensated structure motivate designers to offer new structures for compensation of the threshold voltage which are listed below.

- **V_{th}-compensation with bias distributer network:** Circuit diagram of the compensation with bias distributer [34] is shown in Figure 1.6. Compensation voltage is provided individually for each transistor through the V_{bth} distributer circuit, (V_{bth} is the gate-source voltage of an NMOS transistor biased with a reference current) which consists of pass transistors driven by a pulse waveform. The major advantage of the structure is that the V_{bth} can be equal to V_{th} regardless of the V_{th} deviation over process variations.

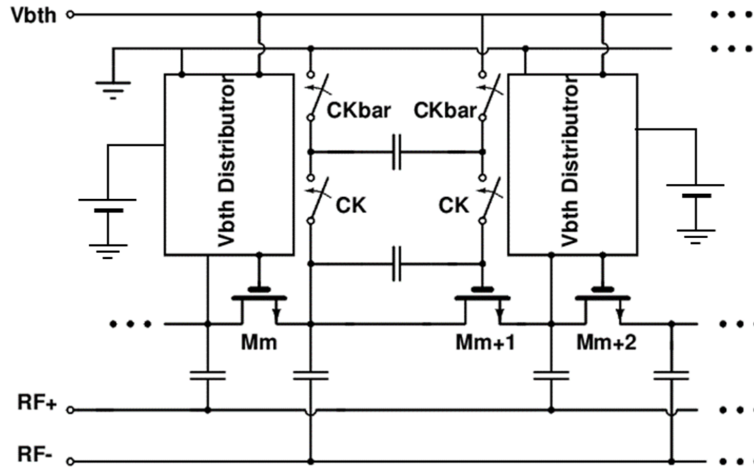


Figure 1-6: Circuit diagram of threshold compensated rectifier with bias voltage distributer [34].

The major drawback of the circuit is that the voltage distributer introduces additional parasitic capacitances (comes from switching transistors) at the top plate of the coupling capacitor which reduces the amplitude of the RF signal to be rectified by pumping transistors (M_m, M_{m+1}, M_{m+2}). Also, realization of the distributer network is hard in addition to the fact that the distributer asks for a secondary battery which prohibit its usage for passive applications.

- **V_{th}-compensation with Ferroelectric capacitor:** Circuit diagram of the UHF rectifier with passive V_{th}-cancellation [16] is shown in Figure 1-7. The technique uses two ferroelectric capacitors (C_{bn} and C_{bp}) to hold the threshold voltage of M_{p1} by replicating its threshold voltage with M_{p2}. The same scenario happens for M_{n1} and M_{n2}. By this technique, the internal V_{th} cancellation

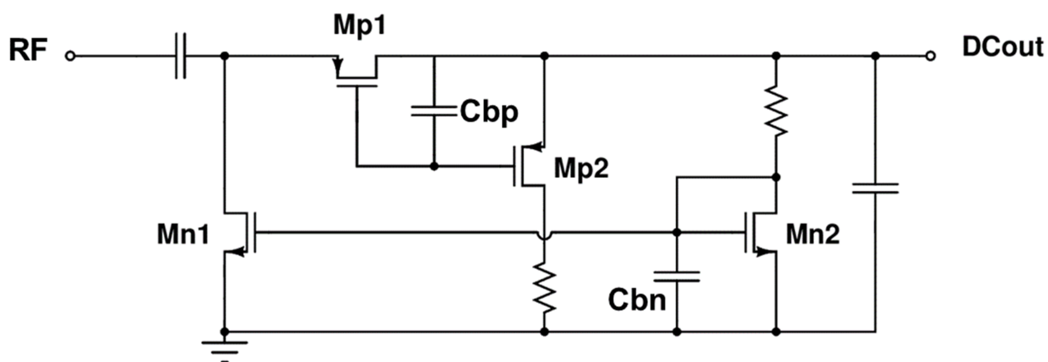


Figure 1-7: Circuit diagram of internal V_{th}-cancelation with ferroelectric capacitor [16].

circuit can precisely monitor the process and temperature variations and compensate the threshold voltage of M_{n1} and M_{p1} accordingly. On the other hand, the circuit has two considerable drawbacks: *i)* Bias resistors should be very large to minimize the leakage current of all diodes which asks for considerable extra area *ii)* Making ferroelectric capacitors asks for PZT ferroelectric layer which would be incompatible for CMOS processes.

Pseudo-floating-gate transistors for V_{th}-cancelation: Circuit diagram of the UHF rectifier implemented with pseudo-floating-gate transistors [11] is shown in Figure 1-8. In this architecture, the compensation voltage is generated by storing the pre-charged voltage in the floating gate transistors. Once the charge is trapped in the floating gates, it will retain for a long time due to floating gate's connection to the gate of the pumping transistors (M_m, M_{m+1}, …) which is the high impedance node. Even though the reported efficiency numbers suggest that the circuit can robustly cancel the threshold voltage at very low RF power intensities and increase the power sensitivity, the amount of the compensation voltage is prone to significant decrease by the gate leakage current. In addition, the residual charge trapped in the floating gate could change the V_{th} of the rectifier. To address this, the floating gate transistors must be programmed to remove the residual charge by F-N tunneling [35] using high-voltage pulse injected to the floating-gate transistors. As a conclusion, the circuit could offer very good power conversion efficiency numbers at very low RF powers and is able to improve the power sensitivity of the remote device. However, its battery-free life-span is not long and it is likely to require repeated human interference.

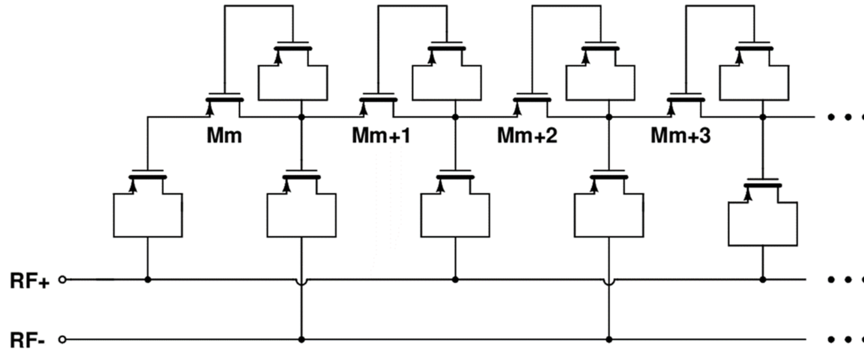


Figure 1-8: Circuit diagram of UHF rectifier with Vth-cancelation using pseudo-floating-gate transistors [11].

1.2.2.3 Differential-Drive Bridge Rectifier

In differential drive rectifiers, the MOS transistors are used as switches and turn ON and OFF at different phases of the RF signal. In general, two separate antennas are required to provide positive and negative RF signals. The reported efficiency numbers of differential drive rectifiers is high (compared to Dickson and threshold compensated rectifiers), but the current direction should be controlled during the overload cases. Depending on using N or P-type transistors, different architectures could be implemented as listed below:

- **Diode-Connected Differential-Drive Bridge Rectifier:** Schematic of the differential drive bridge rectifier is shown in Figure 1-9. The input RF voltage is applied differentially through the RF+ and RF- ports. This topology is widely used in high frequency HF contact-less smart cards. The minimum required input amplitude for starting the operation of the circuit is twice the V_{th} voltage of the NMOS transistors. In [36] it is shown that the power conversion efficiency of the bridge rectifier significantly decreases when the connected load becomes heavier (load resistance decreases) and the PCE will increase by increasing the amplitude of the input sinusoidal signal. The last remark about PCE of the bridge rectifier is that the major reason for efficiency reduction at small load current values (when R_L is high) is the power dissipation due to substrate leakage and channel resistance of the MOS transistors.

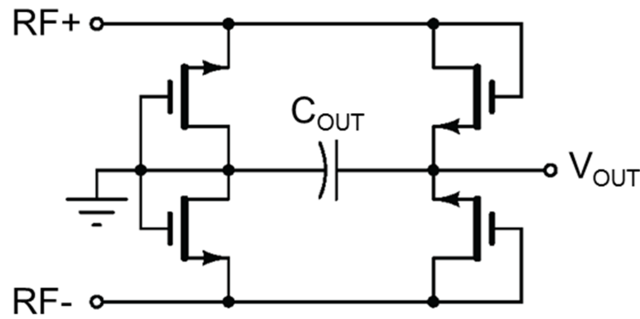


Figure 1-9: Circuit diagram of differential drive bridge rectifier [37].

- **NMOS gate cross-connected bridge rectifier:** As discussed above, the minimum required voltage for starting the operation of the differential drive bridge rectifier is twice the threshold voltage of the MOS transistors which makes its usage hard for UHF RF-to-DC converters. To relieve the minimum

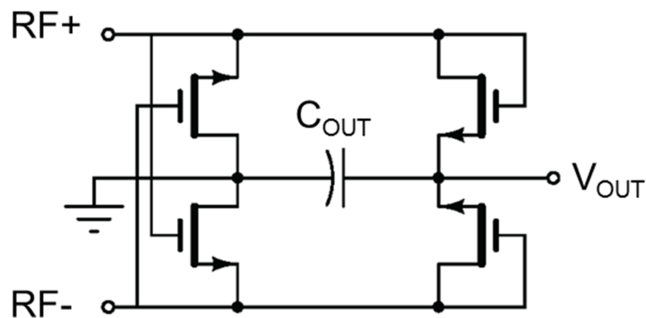


Figure 1-10: Circuit diagram of NMOS gate cross-connected bridge rectifier [36].

voltage requirement, NMOS gate cross-connected bridge rectifier could be used as shown in Figure 1.10 [36]. However, the PCE of this structure under the same load and input power is lower than the differential drive bridge rectifier. It also suffers from substrate leakage and switching losses.

- **NMOS-PMOS differential-drive gate cross-connected bridge rectifier:** Combining two complementary cross-connected branch leads to obtain the NMOS-PMOS differential drive bridge rectifier as shown in Figure 1-11. The minimum required RF amplitude of the structure is below 0.5 V, which is the major advantage over the two previously mentioned differential-drive architectures. All transistors operate as switches [37] (instead of diode). The principle of operation is as follows: at positive phase of the input RF (for which

RF+ is positive and RF- is negative), M_1 and M_4 turn ON while M_2 and M_3 turns OFF leading to direct the current from ground to V_{out}. At negative phase, M_2 and M_3 turns on (while the other transistors are OFF) with the current having the same direction as positive phase due to the special configuration of the transistors. The key issue is that the leakage current of this topology is higher than previous two topologies. Also, the structure requires extra circuitry to control the current direction when the output voltage gets higher than the amplitude of the incoming RF signal [36]. In general, efficiency of the differential drive architecture is good at heavy loads (R_L in kΩ range) while its performance at light loads (R_L in MΩ range) is questionable.

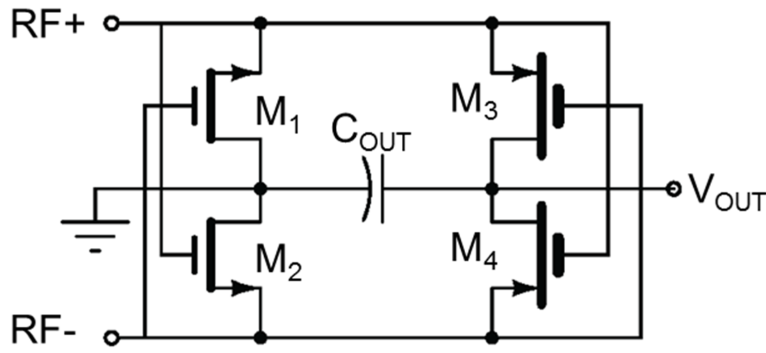


Figure 1-11: Circuit diagram of NMOS-PMOS differential-drive gate cross-connected bridge rectifier [37].

1.3 Modeling of RF Rectifiers

The modeling of UHF rectifiers is included in this work to provide a thorough understanding about their operation principle in addition to insight about the impact of each design parameter. Also, providing accurate models for UHF rectifiers could substitute time-consuming transient simulations. The structures studied in this thesis are the Dickson and the threshold self-compensated topologies. These structures are simple yet effective topologies which are very popular among the designers.

There are a number of publications in the literature modelling the behavior of UHF Dickson rectifiers in detail. In [20] a theoretical analysis of the UHF Dickson rectifier was presented by assuming the pumping device operates in the subthreshold region. However, this work does not introduce a relationship for finding the output voltage. In [38], the output voltage of the RF-to-DC converters was found by introducing a

Bessel function, which should be solved by iteration. Clearly, this is not a very easy task due to nonlinear nature of the Bessel functions. In [39], a methodology based on approximating the entering and exiting charge at steady-state is developed, which relates the output DC voltage to the amplitude of the RF signal, and physical properties of the diode-connected devices. This approach ignores the short channel effects and the channel length modulation by accepting the simple classical square law as the *I-V* characteristics of devices. Since most of the UHF band rectifiers are built in submicron CMOS technologies, this approach would not lead to precise prediction of the generated output voltage. Beside this, in [39], the input sinusoidal signal with a period T is approximated with a first-order Taylor series which is not accurate when the conduction time is more than $T/6$. In [22], an approach based on monitoring the ratio of the peak forward current over the load current, which is referred to as χ, over different DC voltages is developed. However, it is assumed that χ is constant for different load conditions. This assumption restricts the utilization of this technique to a very narrow range of load current values. Moreover, no easy-to-follow guideline is presented to find the value of χ, which should be calculated by several simulations. Finally, in [40], an analytical model is presented to predict the generated DC voltage and the input power of the charge pump structure usable over the broad range of frequencies without demanding any fitting parameter. Even though the model covers important nonlinearities like the I-V characteristic of the MOS device and the conduction angle of the transistors, it assumes that the reverse current is negligible when compared to the forward current. This assumption leads to inaccurate predictions in wireless charging and passive RFID applications where the standby current at the load is below 10 μA and the forward and reverse currents are in the same order.

For threshold self-compensated architecture, there is no study in the literature to address its optimization problem. Hence, one should run extensive and time consuming SPICE simulations to find the optimum device size and number of stages for maximizing the PCE for a given input RF power and output load. This research is the first detailed analysis of the threshold self-compensated rectifiers to the best of author's knowledge. The principle of this work is based on taking the advantage of the fact that the peaking point of PCE-V_{DC} and I_L-V_{DC} curves approximately

coincidence at different RF amplitudes. Proving the aforementioned coherence by both mathematical derivations and SPICE simulations, the optimum DC voltage which maximizes the power conversion efficiency is found. The formulated optimum voltage is used in charge conservation equations to find the optimum device dimension and the number of stages. The proposed method speeds up the design process considerably.

1.4 Design Criteria for RF Harvesting Section:

In an RF energy harvesting system, the minimum input RF power required to obtain a predefined DC voltage (typically 1 V) is referred as power sensitivity [9]. It is desirable to lower the power sensitivity as much as possible to increase separation between the RF source and the remote device. Another important design parameter is the power conversion efficiency (PCE), which defines the available DC power budget for the processing circuitry from the available RF power. This parameter is especially important when it is desirable to send data with high speed during the transmit phase of the remote device. For example, in radio frequency identification (RFID) systems, the input power level is between -14 dBm to -11 dBm, and the primary design goal is to increase the power conversion efficiency in this range of input RF power to add more freedom in the power consumption of the data processing circuitry.

In addition to the sensitivity and the power conversion efficiency, area and reliability of the designed RF harvester system are also critical parameters during mass production. The growing advances in the fabrication process of microelectronic systems in recent decades makes the integrated structures as the first and most common choice for producing low-cost industrial electronic devices in the market. Reducing the total area of the integrated circuit (IC) reduces the total cost which is severely on demand to reduce the total cost of the final product. Reliability of the designed circuit over temperature and process variations is also important to make sure that *i)* the yield of the fabricated prototypes will be high and *ii)* the micro-structure could be used globally (specially in adverse environments with atypical temperatures). Careful layout techniques like common-centroid [41], multi-finger components, and dummy diffusions [42] would be helpful to reduce the vulnerability of the integrated circuits over process variations. For example, the most common problem in recent CMOS fabrication technologies is the latch-up [41] phenomena in

which a parasitic lateral bipolar transistor is constructed inside the neighbor CMOS transistors which could harm the output driver circuits. However, this effect could be eliminated by several techniques, the most common one of which is using guard-rings around the neighbor n-type and p-type transistors to increase the isolation of the circuit from the possible impacts of the rest of the circuit.

1.5 Thesis Outline

The research presented in this thesis is classified into two categories: i) Analysis and modeling of the most common topologies for RF-to-DC converters. ii) Circuit design for RF-to-DC converter and power management units.

In the analysis and modeling part, the Dickson and the threshold self-compensated architectures are selected to be investigated in detail. Simplicity and effectiveness of these UHF rectifiers makes them the first option for front-end integrated section of RF-to-DC converters. For the Dickson topology, many works exist in the literature to model its behavior in UHF band, however, number of shortcomings exist in previous arts as discussed earlier. The first and foremost disadvantage of the previous works is that they are not compatible for modern CMOS processes. In most of them, the classical square I-V relationship ($I_D=k_n.(V_{gs}-V_{th})^2$) is accepted for MOS device, which is not accurate for submicron CMOS process. Also, none of the previous works are able to predict the output voltage of the multi-stage UHF rectifiers when the device operates in weak inversion region with the exponential I-V relationship. The aforementioned short comings should be alleviated by adapting the I-V characteristic of the submicron devices and providing a single formula for finding the output voltage of the device based on the amplitude of the incoming RF signal and process parameters. An implicit formula should be presented for the operation of the diodes implemented by MOS transistors in the weak inversion region.

Unlike the Dickson architecture, no detailed work on the modeling of the threshold self-compensated rectifiers. A mathematical based-framework for the optimization of the design parameters including the device aspect ratio and number of stages to maximize the power conversion efficiency should be presented. Also, the elaborated optimum design parameters should be transformable to power domain in order to make the model ease to use.

As discussed above, the Dickson and the threshold self-compensated architectures are very popular in the RF-to-DC conversion in the UHF band. However, each of them suffer from some disadvantages which prohibit their application in one way or another. For the Dickson rectifier, the amplitude of the incoming RF signal should be at least equal to the intrinsic threshold voltage of the device for its proper operation. As a result, both the power and the voltage conversion efficiency of the rectifier is very low while the input RF intensity is below -10 dBm. Threshold self-compensated rectifier circumvents the intrinsic threshold voltage problem but it suffers from extra leakage current which reduces the efficiency specially at light loads (large R_L). In chapter 3, a novel topology called the "switched-gate" architecture is presented to fill the gap between the Dickson and the self-compensated architectures. The major objective from the switched-gate topology is to compensate the intrinsic threshold voltage in the conduction phase when charge is delivered from the source to the load. In this way, leakage will be prevented since no positive offset exists during the reverse conduction phase.

In addition to the switched-gate rectifier, another novel circuit topology is proposed, called "self-calibrated UHF rectifier" to address the shortcomings of the standard architectures. The self-calibrated architecture is designed to maintain the compensation voltage at its optimum value. In the standard self-compensated architecture, the amount of compensation voltage depends on the intensity of the incoming RF power. This prohibits efficient power harvesting when the RF power gets too large. Thus, the power conversion efficiency reaches its maximum at a specific RF power (which offers the optimum compensation voltage) and abruptly reduces when the input power changes. It could be problematic in practice due to several reasons: First and foremost, several sources may exist at the vicinity of the mobile device, propagating EM waves at different RF powers. For successful energy harvesting, the PCE should be high for all available powers. Second, the intensity is unpredictable due to the insertion of unintended object between the source and the remote device or due to multipath fading. Self-calibrated architecture presented in section III isolates the compensation voltage from the generated DC voltage by the main rectifier and provides a compensation voltage which sets to its optimum value regardless of the intensity of the incoming RF power.

Chapter 4 briefly introduces the power management techniques for RF energy harvesters. The voltage reference block is investigated in more detail since it consumes most of the supply current during the charging phase. Realizing voltage reference circuit independent from temperature, and supply voltage is desirable during the design of the front-end power management unit for RF harvesters. Architectures presented in previous works either consume more than 100 nA from the supply or require special fabrication steps since multi-threshold or transistors with different oxide thickness are required. A novel ultra-low-power voltage reference architecture is presented to circumvent the aforementioned problems by providing the desired reference voltage while consuming 73 nA from the supply and eliminating the demand for extra fabrication process caused by multi-threshold transistors.

Aside from the analysis and the design of rectifier circuits, two most common approach for interface circuits between antenna and rectifiers are investigated: i) conjugate power matching and ii) passive Q-boosting networks. The advantage and disadvantage of each scheme is examined while providing a framework for selecting between the two for the reader.

CHAPTER 2

2 ANALYSIS AND MODELING OF UHF RECTIFIERS

This chapter studies the behavior of the well-known structures of RF-to-DC converters. It is intended to explain the principle of operation of the UHF rectifiers in detail and provide insight about the impact of different design parameters.

The primitive goal of any model created for UHF rectifiers is to estimate the output DC power based on the information from the available RF power and process parameters. From this point of view, the model should offer an accurate formula for the load voltage when the load current, amplitude of the incoming RF signal, and process parameters are known. The focus of this work is on the UHF rectifiers implemented with N-type metal oxide semiconductor (MOS) transistors connected as diodes. The major advantage of NMOS over PMOS device is its superior performance at RF frequencies [33].

Time domain behavior of any UHF rectifier includes transient phase in which the output voltage increases gradually and a steady state phase in which the output voltage reaches to its ultimate value and shows only small ripples.

In the analysis presented in this chapter, the value of the output voltage in which the structure is settled to its final value is intended to be found. Output voltage of the rectifiers is found by charge conservation principle which states that "the amount of the net charge (positive charge minus negative charge) for any passive device is equal to 0". The sinusoidal form of the RF signal in addition to the non-linear nature of the

diodes makes the steady-state current waveforms complex. However, fair approximations could be adapted to ease the relationships.

Aside from finding the output voltage, transforming data from voltage and current domain into power domain is important to make the analysis more suitable for practical applications. It is because, the path loss equation in (1-2) only gives the available RF power (not the RF amplitude). Hence, calculating the input RF power delivered to the rectifier is useful in determining the input impedance of the rectifier and consequently transforming the information from voltage domain to power domain. Calculating the power consumption of the rectifiers is also important for finding the power conversion efficiency of the rectifiers and consequently optimizing the design parameters.

Models presented for the Dickson and the self-compensated architectures are evaluated by comprehensive simulations and measurements. For the Dickson architecture, the predicted output voltage by the model is compared with measurements when the available RF power changes from -12 dBm to 0 dBm while connected to a load varying between 10 kΩ to 1 MΩ. For the threshold self-compensated rectifier, it is intended to find the optimum design parameters like device aspect ratio and number of stages to provide the maximum power conversion efficiency. The design parameters found by the model are compared with simulations, then the predicted output voltage is compared with simulations and measurements. The presented model for the self-compensated rectifier could precisely predict the optimum design parameters when the amplitude of the incoming RF signal is higher than 0.2 V. The predicted output voltage is compared by measured results when available RF power is between -10 dBm to 0 dBm and the connected load changes from 50 kΩ to 1 MΩ.

2.1 UHF Dickson Rectifiers

In most remotely powered systems, a form of Dickson charge pump [27], is used for the RF-to-DC conversion task [29]. The rectifying devices inside the Dickson charge pump can be Schottky diodes [23] or CMOS transistors [24]. Since Schottky diodes are usually not offered as a standard option in low cost processes, building the

converter with standard CMOS transistors is preferred to reduce cost and to make integration with the proceeding digital blocks possible.

The challenging part in the design of such RF-to-DC converters is to realize circuits that can handle very low amplitudes of incident RF waves. As can be deduced from Figure 2-1, in a CMOS implementation, the incident RF voltage should overcome the intrinsic threshold voltage of the diode-connected MOS devices for the converter to work. Using zero-threshold devices [43] is a method proposed to address the limitation. However, these devices are very sensitive to process variations and their leakage current is high. The threshold self-compensation architecture [32] is another method used regularly to overcome the threshold limitation of diode-connected devices. The technique is expanded in [33] by elongating the gate connections (to make the compensation voltage multiple times of the generated DC voltage per stage) for having higher compensation voltage at extremely low RF intensities. However, in any kind of self-compensated structure, extra compensation at high powers degrade the reverse isolation of the rectifying devices. Therefore, the technique should be used with caution and only be employed for applications where incident RF power is guaranteed to be very low. Robust blocking of the reverse current, makes Dickson architecture very attractive for near field applications where the input RF power is high. An analysis to accurately predict the output voltage and power conversion efficiency of the Dickson rectifier is, therefore, of paramount importance.

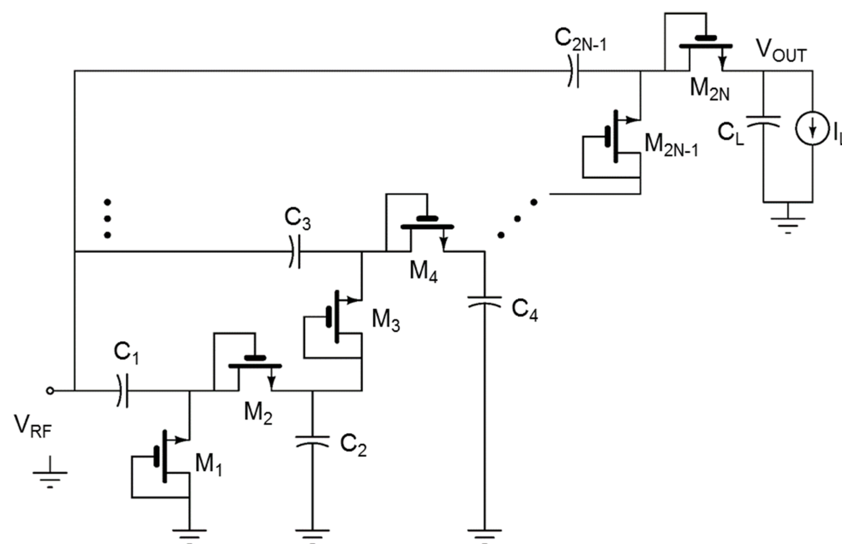


Figure 2-1: Diode-connected UHF multi-stage Dickson rectifier with MOS transistors.

In this sub-section, an analysis of the standard Dickson rectifier circuit is presented that provides a much better prediction of the generated DC voltage compared to the literature. An optimization procedure based on this analysis is presented which provides the required number of rectifying stages and device sizes, depending on the physical parameters of the diodes, to achieve maximum power efficiency for a given incident RF power and load current. The principle of this work is based on the accurate approximation of the ratio of the forward peak current (I_P) to the load current (I_L). The advantage of approximating the I_P/I_L ratio is several-fold: First, it eliminates the requirement of integrating the reverse current, which significantly reduces the complexity. Second, it makes the model suitable for broad range of the load currents (I_L) and RF amplitude values. Finally, the versatility of the approach allows finding a relationship for V_{DC} based on the RF voltage for any type of the diodes, including the ones with linear, square, or exponential *I-V* characteristics.

In the presented work, a mathematical analysis is developed based on the BSIM3v3.2 [44] model to determine the output DC voltage of the diode-connected rectifier, provided that the amplitude of the incoming RF signal and the load current are known. Finding the output DC voltage based on the proposed method is applicable for different types of diodes by plugging the *I-V* relationship of the device into the general formula. The analysis is followed by introducing a formula for maximizing the PCE. Unlike, [22], [39]and [45], which start the analysis of RF-to-DC converters by examining the rectifier diodes, this work focuses on the operation of the clamp diode and calculates the generated DC shifted voltage by the clamp circuit. In this way, the output voltage per stage can directly be calculated by considering the symmetry of the circuit. Thus, better accuracy is achieved by taking the generated DC voltage of the clamp into account without additional calculation. At the end, a simple, yet accurate equation is derived to express the input-to-output relationship of the diode-connected topology. The only requirement for directly calculating the output DC voltage in the proposed model is that the device operates in strong inversion inside the forward conduction time. Yet, finding the output DC voltage could be expanded to the cases that RF amplitude is lower than V_{TH} by employing a subthreshold *I-V* relationship for the MOS device leading to an implicit relationship.

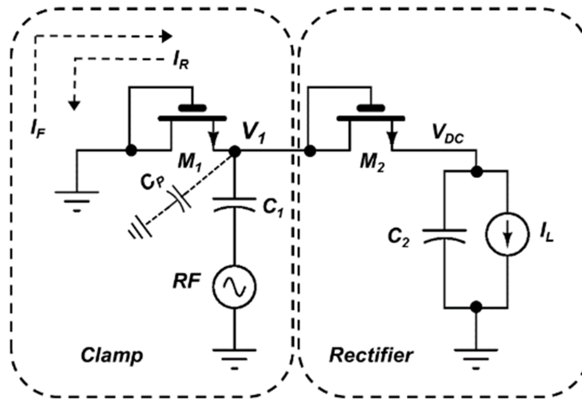


Figure 2-2: Basic cell of UHF Dickson rectifier with clamp and rectifier units.

2.1.1 Dickson RF-to-DC Architecture

This section finds the output DC voltage of the Dickson rectifier (V_{DC}) as a function of the peak value of the input RF voltage (V_P). In practice, the provided data from Friss equation is the power at the receiver (instead of RF voltage amplitude). However, after finding the output DC voltage as a function of the input RF voltage, the analysis is continued by finding the delivered power to the IC. Also, the available power from the RF source is found for given RF amplitude and elaborated V_{DC} values.

The structure of a Multistage UHF Dickson rectifier is shown in Figure 2-1. Each stage of the Dickson rectifier can be divided into two sub-blocks, as shown in Figure 2-2; a clamp circuit to increase the DC level of the incident RF, and a rectifier circuit

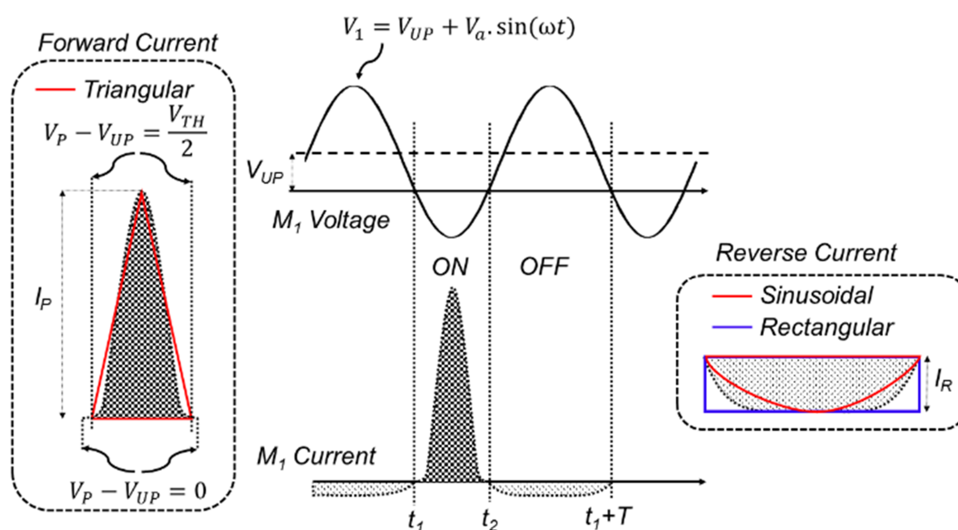


Figure 2-3: Steady-state waveforms of clamp transistor (M_1.in Figure 2-2).

to convert the RF into DC. Assuming a sinusoidal RF source with an angular frequency ω, the steady-state voltage at the top plate of C_1 is:

$$V_1 = V_{UP} + V_a \sin(\omega t),\ V_{UP} = \frac{V_{DC}}{2}, \qquad (2\text{-}1)$$

where V_{UP} is the up-shifting voltage created by the clamp circuit, and V_{DC} is the DC voltage generated by the single stage structure. Due to the symmetry of the structure, V_{UP} is equal to the half of the V_{DC}. V_a is the amplitude, of the incident RF waveform at the top plate of C_1 and is related to the amplitude of the incoming RF signal (V_P) by

$$V_a = V_P . \frac{C_1}{C_1 + C_P}, \qquad (2\text{-}2)$$

where C_1 is the coupling capacitor, and C_P is the total parasitic capacitance at node V_1 created by the parasitic components of the coupling capacitor and the overlap and junction capacitances of the two adjacent transistors.

Calculation of the V_{UP} (and consequently V_{DC}) is based on the charge conservation principle. At steady-state, the integral of the current passing through M_1 during forward conduction (I_f) is equal to the integral of the reverse current (I_r) during the discharging phase plus the load current (I_L):

$$\frac{1}{T}\int_{t_1}^{t_2} I_f dt = \frac{1}{T}\int_{t_2}^{t_1+T} I_r dt + I_L \qquad (2\text{-}3)$$

The steady-state waveform of the forward and reverse currents of M_1 is depicted in Figure 2-3. By noticing the specific shape of the device current at conduction (ON) and isolation (OFF) times, it can be seen that (2-3) could be simplified as below:

$$\frac{1}{2} I_P \Delta t_f - \frac{2}{\pi} I_R \Delta t_r = I_L . T \qquad (2\text{-}4)$$

where Δt_f and Δt_r are forward and reverse conduction durations, T is the period of the incoming signal, I_P and I_R are the peak currents inside the conduction and isolation times respectively. During the derivation of (2-4), the forward current is approximated by a triangular wave, and the special shape of the reverse current suggests that the value of its integral should be in between a sinusoidal waveform ($(1/\pi).\Delta t_r.I_R$) and a

rectangular waveform ($\Delta t_r.I_R$). Hence, 2/π is selected to approximate the integral of the reverse current. The I_P/I_L ratio could be rearranged as;

$$\frac{I_P}{I_L} = \frac{1 + \frac{2}{\pi}\left(\frac{I_R}{I_L}\right)\left(\frac{\Delta t_r}{T}\right)}{\frac{1}{2}\left(\frac{\Delta t_f}{T}\right)} \quad (2\text{-}5)$$

Figure 2-4 depicts the simulated I_P/I_L ratio of the clamp transistor for different RF levels as a function of the upshifting DC voltage (i.e. or half of the output DC voltage). The DC voltage is changed by connecting different resistive loads and monitoring the relevant I_P/I_L ratio for each DC voltage. The pattern of all curves is similar to each other suggesting that their estimation with a hyperbolic function would help to find a direct relationship for the output DC voltage ($2V_{UP}$) as a function of the input RF voltage (V_P). In all of these curves, for each V_P, there is an upper limit for V_{UP}, which is obviously obtained when the load current (I_L) is zero.

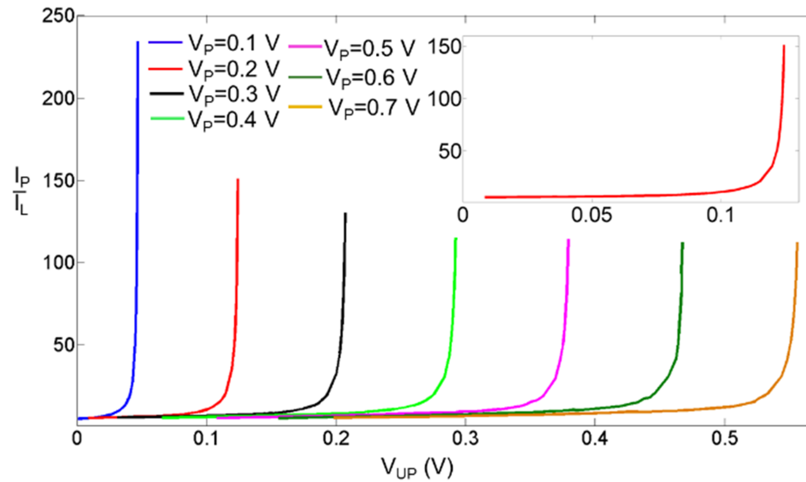


Figure 2-4: Simulated I_P/I_L for different RF voltages (f=900 MHz, V_{TH}=0.12 V, W/L=100).

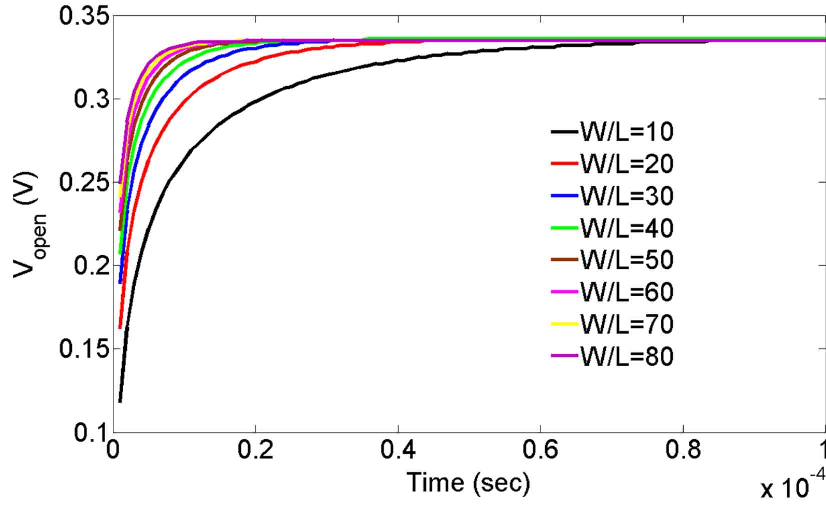


Figure 2-5: Simulated open load voltage for different device sizes. (V_P=0.25 V, f=900 MHz).

This work tries to represent the I_P/I_L ratio by a simple relationship while providing the utmost likeness with simulations. As Figure 2-4 suggests, this ratio is very close to the hyperbolic function and would be approximated as below:

$$\frac{I_P}{I_L} \approx m_1 + \frac{m_2}{V_a - \frac{1}{2}V_{open}} \tag{2-6}$$

where m_1 and m_2 are the coefficients whose derivation will be described later and V_{open} is the open load DC voltage of the single stage rectifier.

2.1.1.1 Finding the Open Load Voltage

Assuming a perfect rectification by both clamp and rectifier transistors, the generated DC voltage for each stage is two times the RF amplitude ($2V_P$). However, in practice, the resulted voltage is lower than its ideal value mostly due to nonzero conduction in isolation (OFF) times. In the literature (i.e. equation (22) in [39] and equation (1) in [22]), setting the I_L equal to zero will result to open load voltage of $2\times(V_P\text{-}V_{TH})$ for each stage. This expression is not accurate enough especially when V_P is close to or a bit higher than V_{TH}. For example, the predicted V_{DC} by previous works will be 0 when V_P is equal to V_{TH}, which is surely incorrect. The device operates in the subthreshold region when I_L is zero since the gate-source voltage is almost zero during the

conduction time and is exactly zero during the isolation time. The *I-V* relationship of the device at subthreshold region is equal to:

$$I=(n-1).I_S.\frac{W}{L}.e^{\frac{Vgs-Vth}{nVt}}.\left(1-e^{\frac{-Vds}{Vt}}\right) \quad (2\text{-}7)$$

where I_S is the specific current, n is the subthreshold slope of the device and V_T is the thermal voltage. This work finds V_{open} by solving (2-4) when its right hand side (I_L) is zero which leads to the implicit equation as below:

$$\frac{1}{2}e^{\frac{V_a-\frac{V_{open}}{2}}{nV_t}}.\left[1-e^{-\frac{V_a-\frac{V_{open}}{2}}{nV_t}}\right].\left[\frac{1}{2}-\frac{1}{\pi}sin^{-1}\left(\frac{V_{open}}{2V_a}\right)\right]-\frac{2}{\pi}\left[\frac{1}{2}+\frac{1}{\pi}sin^{-1}\left(\frac{V_{open}}{2V_a}\right)\right]=0 \quad (2\text{-}8)$$

During the derivation of this equation, the common terms of forward and reverse current, like the *W/L* ratio and the exponential dependence to the V_{TH} are cancelled. This equation suggests that the open load voltage is independent of the device size. Comprehensive simulations (Figure 2-5) show that changing the device size does not change V_{open} and it merely alters the rising time. Figure 2-6 shows the simulated open load voltage for different RF amplitudes and compares it with predicted open load voltage in (2-8) and previous works. It suggest that when RF amplitude is lower than or comparable to V_{TH}, equation (2-8) should be used to find V_{open}, but when V_P is more than two times of V_{TH}, it is safe to use $2(V_P\text{-}V_{TH})$ as the open load voltage as suggested in [39] and [22]. The deviation of the proposed formula with simulations over the growth of V_P is related to several non-idealities due to large voltage swing. Some key phenomena are listed here; *i)* Drain induced barrier lowering (DIBL): it refers to reduction in MOS threshold voltage due to high drain-source voltage. The result is that the gate loose its control on the current flow of the transistor. This effect is ignored in the model by assuming that the threshold voltage of the device is constant for all RF amplitudes. ii) Parasitic capacitance variation due to higher RF amplitude: This research assumes that the magnitude of the parasitic capacitance is constant for all RF amplitudes and takes a fixed capacitor division ratio in (2-2). However, amount of the junction capacitances depends on the reverse voltage across the P-N junction. Including the DIBL and parasitic capacitance variation by RF amplitude would result to better approximation of the open load voltage.

2.1.1.2 Finding m_1 and m_2

The unknown coefficients (m_1, m_2) are selected to make the approximated relationship for I_P/I_L in (2-6) close to the simulated results. Accurate estimation of V_{open} helps to resemble the simulated results when I_P/I_L ratio is high. Hence, the unknown coefficients are chosen to provide the similarity when the interested ratio is moderate or low. In these regions, the reverse current is negligible compared to the forward current and equation (2-5) could be simplified as below:

$$\frac{I_P}{I_L} = \frac{1}{\frac{1}{2}\left(\frac{\Delta t_f}{T}\right)} \cong \frac{2}{\frac{1}{2} - \frac{1}{\pi} sin^{-1}\left(\frac{V_{UP} + \frac{V_{th}}{2}}{V_a}\right)} \tag{2-9}$$

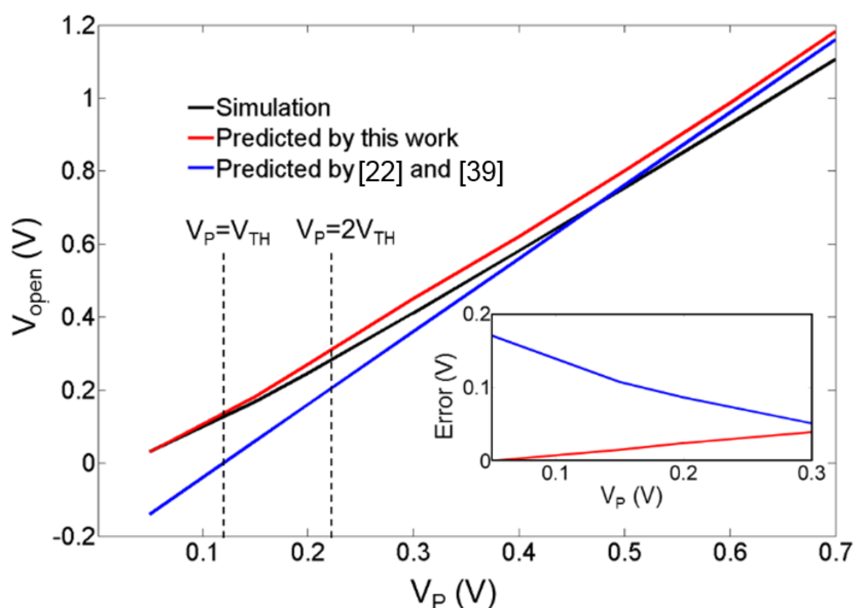


Figure 2-6: Simulated open-load voltage and its comparison with predicted result in (N=1, f=900 MHz, W/L=100, n=1.5, V_{TH}= 0.12 V) (the inset shows the error of two approaches with respect to the simulation result).

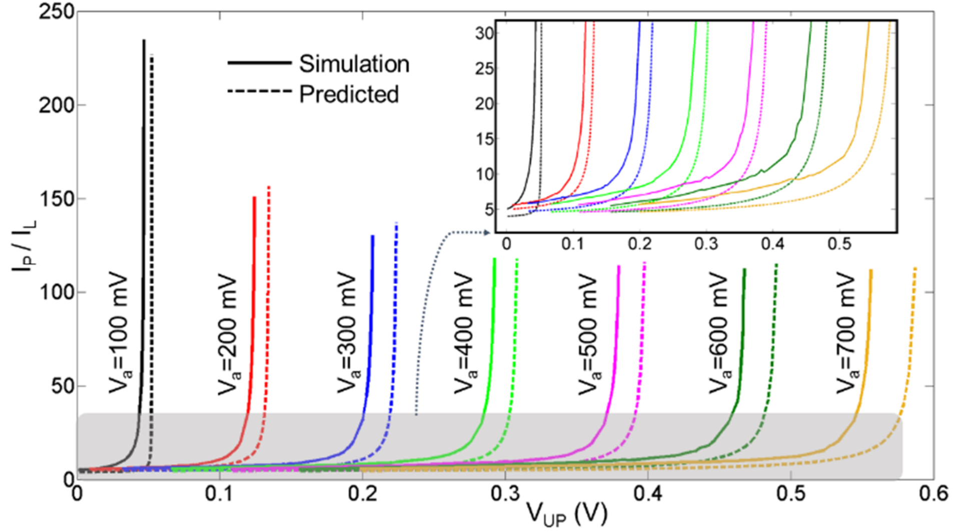


Figure 2-7: Simulated and estimated I_P/I_L for different RF amplitudes versus half of the DC voltage (V_{UP}).

During the elaboration of this equation, the forward conduction angle ($\Delta t_f /T$) is defined when the gate-source voltage of the device is higher than ($V_{TH}/2$). In practice, forward conduction time starts exactly when the gate-source voltage gets higher than zero. But, referring to Figure 2-3, it would be better to employ the compressed conduction angle to obtain better triangular approximation of the forward current integral.

Two arbitrary intercept points are chosen to match the right hand sides of (2-6) and (2-9) equal to each other. One of them is, the $V_{UP}=0$ which is the minimum possible upshifting voltage and the other point is $V_{UP}=0.9(1/2V_{open})$ which is very close to the upper boundary of V_{UP}. Then, the unknown coefficients are achieved as below:

$$m_1 = \frac{1}{9} \times \left[\frac{20}{\frac{1}{2} - \frac{1}{\pi}.sin^{-1}\left(\frac{V_{th}}{2V_a}\right)} - \frac{2}{\frac{1}{2} - \frac{1}{\pi}.sin - 1\left(\frac{0.45V_{open} + 0.5V_{th}}{V_a}\right)} \right]$$

$$m_2 = \frac{V_{open}}{2} \times \left[\frac{20}{\frac{1}{2} - \frac{1}{\pi}.sin^{-1}\left(\frac{V_{th}}{2V_a}\right)} - m_1 \right] \qquad (2\text{-}10)$$

Figure 2-7 compares the simulated I_P/I_L with the one obtained by approximated relationship in (2-6). Good agreement between the two is obtained at low, moderate, and high I_P/I_L ratios and also for different RF amplitudes. By replacing the dependence

of the drain current of the short channel MOS device to its gate-source and drain-source voltage as represented in [46], and also considering the fact that the gate-source voltage of M_1 at the maximum conduction instant (i.e. $I_{M1}=I_P$) is equal to V_a-V_{UP}, equation (2-6) becomes:

$$\frac{\frac{k_n(V_a - V_{UP} - V_{TH})^2}{1+\theta(V_a - V_{UP} - V_{TH})}.(1+\lambda(V_a - V_{UP}))}{I_L} = m_1 + \frac{m_2}{V_a - \frac{1}{2}V_{open}} \quad (2\text{-}11)$$

where K_n is $(1/2)\mu_n.C_{ox}$, θ is the mobility reduction factor of the subthreshold device, and λ is the channel length modulation coefficient. To simplify this equation and find a direct relationship between RF voltage and V_{UP}, it is assumed that V_P is high enough to approximate $1/2V_{open}$ with V_a -V_{UP}. However, when V_P is lower than $2V_{TH}$, it is better to find V_{open} by solving (2-8) to obtain better accuracy. By rearranging (2-11) the final form of RF-to-DC equation will be:

$$\begin{aligned} &a_1(V_a - V_{UP} - V_{TH})^4 + a_2(V_a - V_{UP} - V_{TH})^3 + a_3(V_a - V_{UP} - V_{TH})^2 + \\ &a_4(V_a - V_{UP} - V_{TH}) + a_5 = 0 \end{aligned} \quad (2\text{-}12)$$

With

$$a_1 = \frac{\lambda k_n}{I_L}, a_2 = \frac{(1+\lambda V_{TH})k_n}{I_L}, a_3 = -\theta m_1, a_4 = -(m_1 + m_2\theta), a_5 = -m_2 \quad (2\text{-}13)$$

The root of this equation is:

$$V_{UP} = V_a - V_{TH} - \left[-\frac{a_2}{4} + \frac{P_4}{2} + \frac{(P_5 + P_6)^2}{2} \right] \quad (2\text{-}14)$$

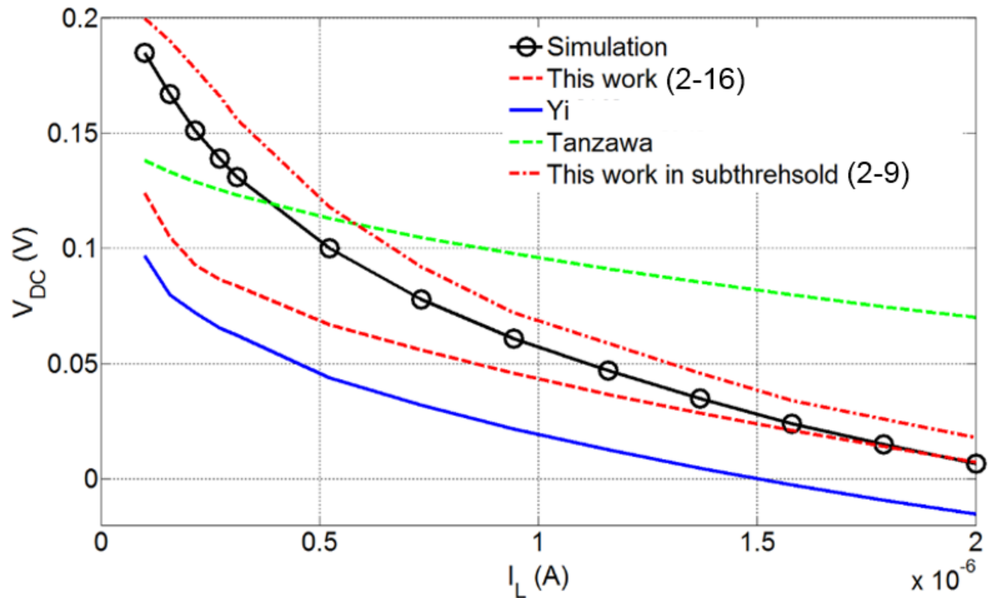
The unknown coefficients of this equation are:

$$P_1 = 2a_3^3 - 9a_2a_3a_4^2 + 27a_2^2a_5 - 72a_1a_3a_5,$$
$$P_2 = P_1 + \sqrt{-4\left(a_3^2 - 3a_2a_4 + 12a_1a_5\right)^3 + P_1^2}$$
$$P_3 = \frac{a_3^2 - 3a_2a_4 + 12a_1a_5}{3a_1\sqrt[3]{\frac{P_2}{2}}} + \frac{\sqrt[3]{\frac{P_2}{2}}}{3a_1},\ P_4 = \sqrt{\frac{a_2^2}{4a_1^2} - \frac{2a_3}{3a_1} + P_3}, \tag{2-15}$$
$$P_5 = \frac{a_2^2}{2a_1^2} + \frac{4a_3}{3a_1} - P_3,\ P_6 = \frac{-\frac{a_2^3}{a_1^3} + \frac{4a_2a_3}{a_1^2} - \frac{8a_4}{a_1}}{4P_4}$$

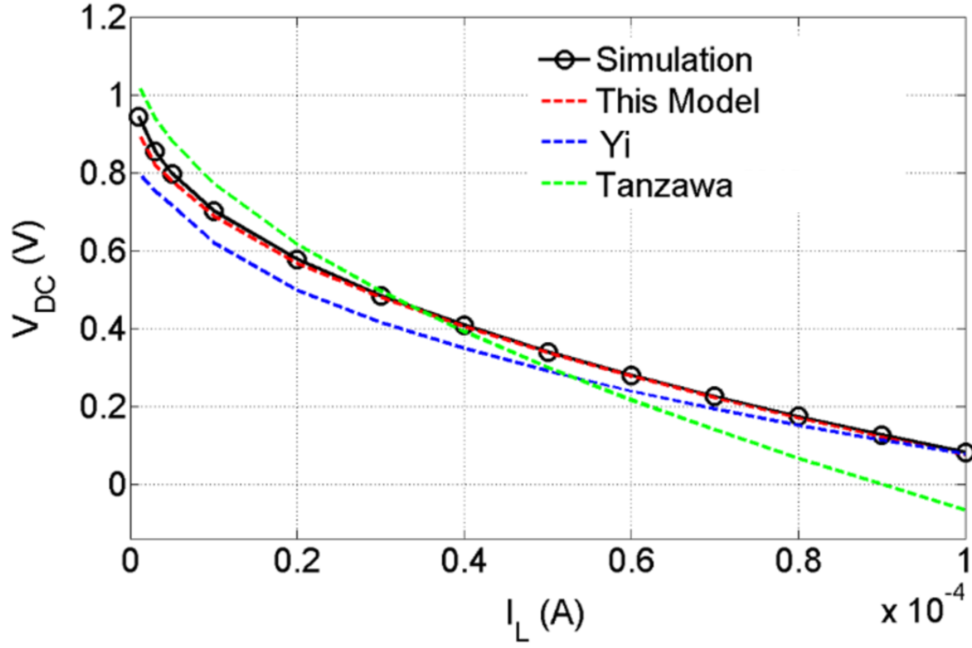
The DC voltage generated for an N stage UHF Dickson rectifier is found as below;

$$V_{DC} = 2N(V_{UP}) = 2N\left[V_a - V_{TH} - \left(-\frac{a_2}{4} + \frac{P_4}{2} + \frac{(P_5 + P_6)^2}{2}\right)\right] \tag{2-16}$$

Equation (2-16) suggest the generated output DC voltage is independent of the input RF frequency, but as explained in [25], generation of ripple-free voltage at top plate of storage capacitors requires that the time constant of the RC network constructed with the storage capacitors (C_2, C_4 in Figure 2-2) and the load current becomes much larger than the period of the incoming signal, $C_2 >> (I_L/V_{DC}2\pi f)$.



(a)



(b)

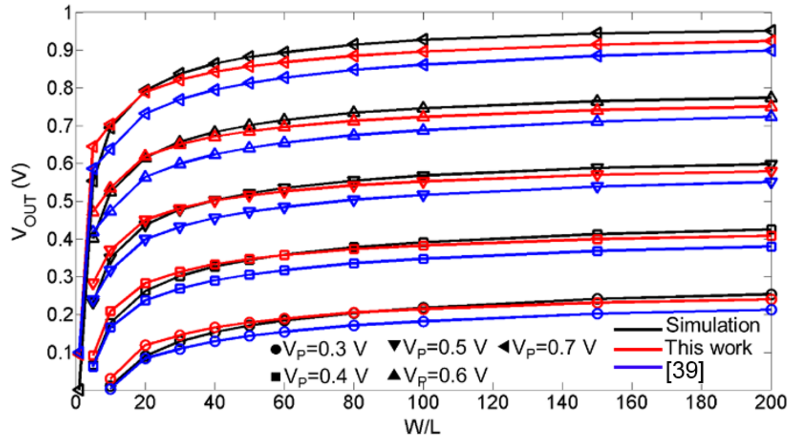
Figure 2-8: Comparison of simulated DC voltage with predicted results of this work and state of the art versus load current (a) V_P=0.7 V, W/L=2.4µm/0.24µm, C_1=3 pF, f=900 MHz (b) V_P=0.2 V, W/L=2.4µm/0.24µm, C_1=3 pF, f=900 MHz.

In previous studies, the number of diode-connected devices is considered as the number of stages. However, this work takes the combination of clamp and rectifier diode as a single stage due to the fact that generation of a ripple-free DC voltage from the RF signal asks for concurrent employment of both the clamp and the rectifier blocks. The exact expression for the output voltage including the variation of V_{TH} due to non-zero body voltage (in the N-well process) can be created by the same approach and is presented in Appendix A. Figure 2-8 compares the simulated DC voltage versus the load current with the one predicted by this work, [21], and [37] for two different RF amplitudes. It can be seen that the proposed method offers better approximation of the generated DC voltage compared to the literature due to the exact estimation of the I_P/I_L ratio and also including the dependence of the *I-V* relationship of the device to the channel length modulation effect. Both of the older approximation approaches deviates from the simulation results when $V_P=0.2\ V$ and I_L is very low. It is because of taking the strong inversion equation, which is not accurate when V_{gs} is close to V_{TH}. Better estimation of the DC voltage for $V_P=0.2\ V$ could be obtained (captured in Figure 2-8(b)) by using the subthreshold equation for I_P in (2-6). The cost for better

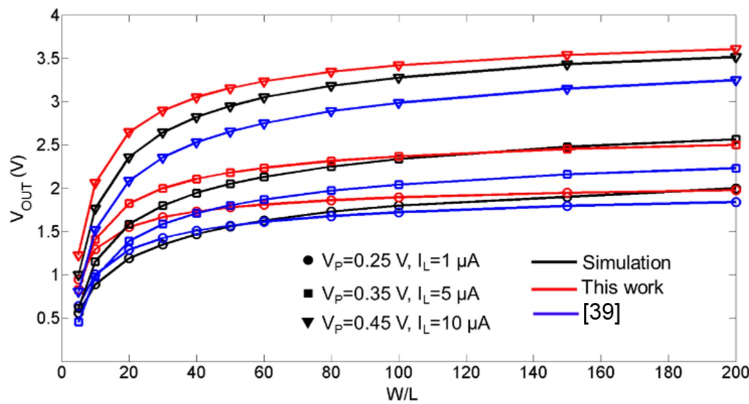
accuracy is to deal with an implicit equation which could be solved only by iteration. The design parameters used for plotting the estimated results are provided in Table I. Figure 2-9 compares the developed model with simulation results and previous work over different design parameters including the number of transistors, amplitude of the incoming RF, and the current drawn by the load. The *W/L* ratio is changed by keeping the channel width (W) to its minimum value (0.25 μm) and modifying the number of fingers of the transistors. It can be seen that good agreement exists between the simulation results and the proposed model. Using this very accurate model, a methodology to optimize the transistor sizes and the number of stages for a given load and incident RF condition will be developed in the next section.

Table 2-1: Design Parameters

Design Parameter	Value
V_{TH}	0.12 V
$\frac{\mu_n C_{ox}}{2}$	170 μA/V^2
Number of Diodes	16 (N=8)
Coupling capacitor	3 pF



(a)



(b)

Figure 2-9: Comparison of simulated DC voltage with predicted results by this work and the state of the art work versus device size (a) N=1, f=900 MHz, I_L=10 μA (b) N=10, f=900 MHz.

2.1.2 Optimization of Power Conversion Efficiency

This section presents a methodology to calculate the optimum W/L ratio of the diode-connected MOS devices based on the analysis presented in the previous section. The optimization procedure maximizes the PCE of the multi-stage rectifier without the need for extensive SPICE simulations. Using the simplified formula for calculating the power conversion efficiency as done in [47] will not lead to accurate result in UHF energy harvesters since the power consumption during the reverse isolation phase is not negligible. In [22], a formula is expressed for finding the power conversion efficiency. However, the dependence of the elaborated formula to the fundamental impedance of the IC leads to complexity. Instead, this work focuses on the steady-state waveform of the power consumption of the diodes. The dissipated power at the

clamp transistor (M_1 in Figure 2-2) is calculated as a start, and it multiplied by two to find the dissipated power of a single stage structure. Finally, the result is expanded for multi-stage structure with body effect in Appendix A.

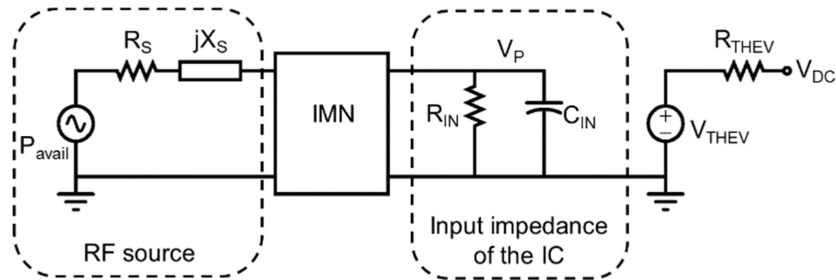


Figure 2-10: Behavioral model of the RF harvesting system for analysis of the delivered power to the rectifier.

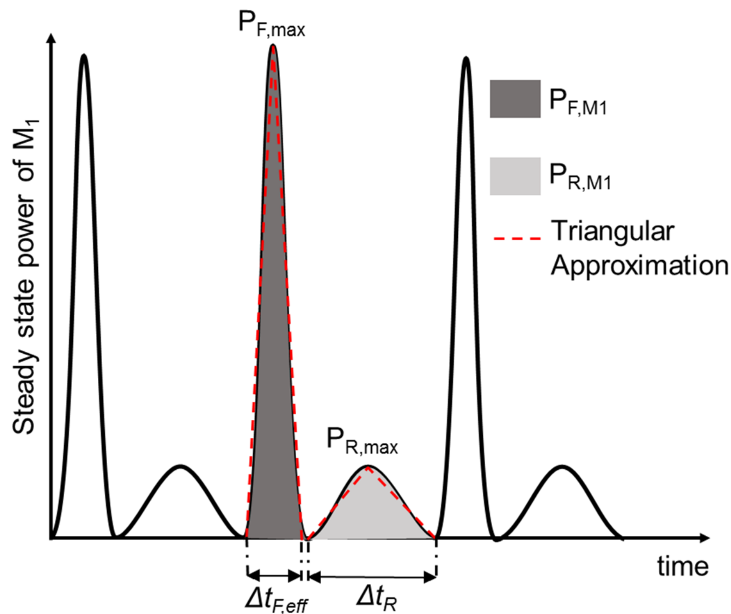


Figure 2-11: Steady-state power waveform of the clamp diode (M_1).

2.1.2.1 Rectifier Efficiency

Figure 2-10 models the antenna, impedance matching network (IMN), and the input impedance of the RF to DC converter IC [22]. Considering highly inductive nature of the typical antennas for RF harvesting and RFID applications, the RF source is represented with a power source (P_{avail}) while R_S and L_S are the input resistance and

inductance of the RF source. The power conversion efficiency of the rectifier is defined as below:

$$\eta_{rect} = \frac{V_{DC}.I_L}{P_{IC}} \tag{2-17}$$

where P_{IC} is the power delivered to the IC at the steady state. Figure 2-11 shows the steady state power waveform of M_1. The steady-state power can be divided into two parts: a) the power dissipated during the forward conduction, $P_{F,M1}$ and b) the dissipated power during the reverse conduction $P_{R,M1}$. Similar to the output voltage analysis, power optimization procedure takes the advantage of the fact that at steady-state, both $P_{F,M1}$ and $P_{R,M1}$ waveforms are very close to triangular shapes. Hence, the strategy is to calculate the instantaneous peak power of a single transistor during each mode and expand its results for multistage structure to approximate the steady-state power. The total input power of the M_1 in a single period is:

$$P_{IC,M1} = P_{F,M1} + P_{R,M1} \;, \tag{2-18}$$

while $P_{F,M1}$ and $P_{R,M1}$ could be found as below:

$$P_{F,M1} \cong \frac{1}{2T}\Delta t_f .P_{F,max} = \frac{1}{2T}\Delta t_f I_p (V_a - V_{UP}) \;, \tag{2-19}$$

$$P_{R,M1} \cong \frac{1}{2T}\Delta t_r .P_{R,max} = \frac{1}{2T}\Delta t_r I_R (V_a + V_{UP}) \;, \tag{2-20}$$

$\Delta t_f /T$ is represented in (2-9) and $\Delta t_r /T$ could be found as:

$$\frac{\Delta t_r}{T} = \frac{1}{2} + \frac{1}{\pi} sin^{-1}\left(\frac{V_{UP}}{V_a}\right) \tag{2-21}$$

and maximum reverse current (I_R) can be found using:

$$I_R = I_S\left(1 - e^{-\frac{V_a + V_{UP}}{V_t}}\right), \tag{2-22}$$

The total input power delivered to the IC for N-stage rectifier is given by:

$$P_{IC} = 2N(P_{F,M1} + P_{R,M1}) + I_L(2NV_{UP}), \tag{2-23}$$

Ignoring the body effect, the power conversion efficiency can be calculated as

$$\eta_{rect} = \frac{2NI_L V_{UP}}{2NP_{IC,M1} + 2NI_L V_{UP}} \tag{2-24}$$

by replacing $P_{IC,M1}$ with (2-18) - (2-22), we have

$$\eta_{rect} = \frac{I_L V_{UP}}{\frac{1}{T}\left[\frac{1}{2}\Delta t_f I_R (V_a - V_{UP}) + \frac{1}{2}\Delta t_r I_R (V_a + V_{UP})\right] + I_L V_{UP}} \tag{2-25}$$

For the sake of simplicity, body effect is ignored during the derivation of equation (2-25) in the main part of this paper. This equation can be used for isolated processes where body effect can be avoided. Detailed analysis including the body effect is given in Appendix A, which can be used in standard CMOS processes with body terminals connected to ground.

Figure 2-12 and Table II compare the simulated PCE of a single-stage Dickson rectifier with predicted results by this work and the one in [39]. The comparison is done at wide range of RF amplitudes to assess the ability of the model at different scenarios. Comparing with the previous work, the predicted optimum size and peak efficiency numbers in this work show better agreement with the simulated results. It should also be noted that both approaches accept the square relationship to model the I-V relationship of the MOS device. This relationship is valid in strong-inversion region. As a rule of thumb, the gate-source voltage should be at least 0.1 V [46] above the threshold voltage to completely operate in strong inversion region. Both this work and [39] accepts the square relationship and their accuracy of predictions in Figure 2-12 improves with increasing the V_P.

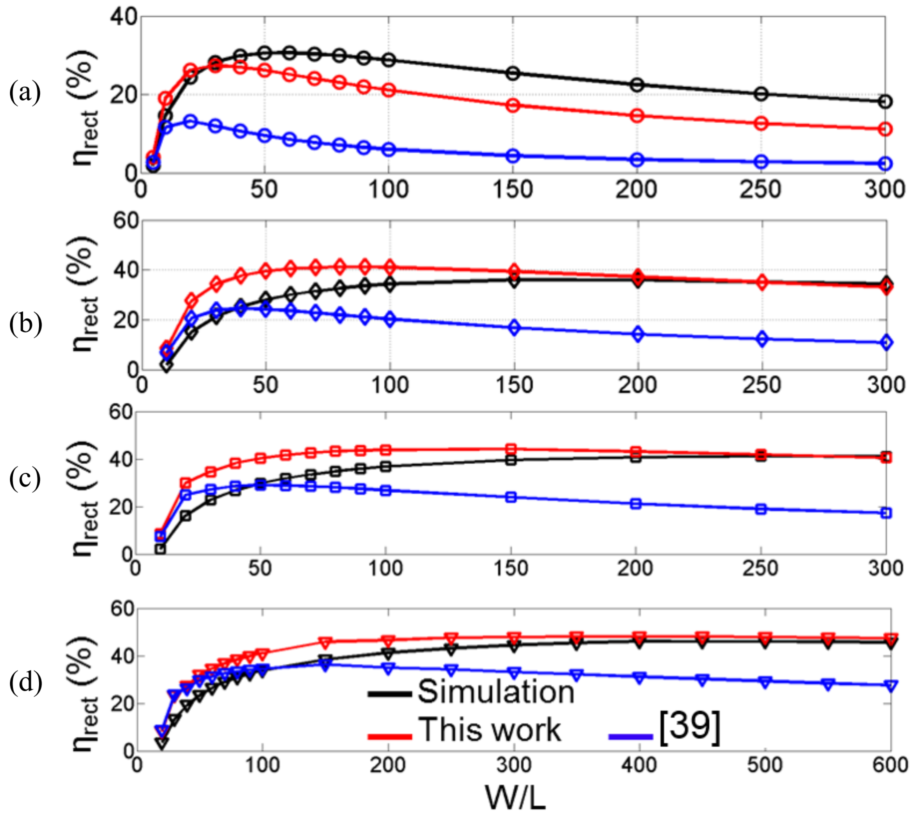


Figure 2-12: Comparison of simulated power conversion efficiency for a single stage rectifier with predicted results of the proposed model and [39] (a) V_P=0.2 V, I_{Load}=1 μA (b) V_P=0.25 V, I_{Load}=5 μA (c) V_P=0.3 V, I_{Load}=10 μA (d) V_P=0.4 V, I_{Load}=50 μA.

Table 2-2: Power Conversion Efficiency and Optimum Size Comparison.

V_P,I_L	Simulation	This work	[39]
V_P=0.2 V, I_L=1 μA	$(W/L)_{opt}$=60, Peak η_{rect}=32%	$(W/L)_{opt}$=30, Peak η_{rect} =23%	$(W/L)_{opt}$=20, Peak η_{rect} =12%
V_P=0.25 V, I_L=5 μA	$(W/L)_{opt}$=150, Peak η_{rect} =36%	$(W/L)_{opt}$=90, Peak η_{rect} =41%	$(W/L)_{opt}$=40, Peak η_{rect} =24%
V_P=0.3 V, I_L=10 μA	$(W/L)_{opt}$=250, Peak η_{rect} =41%	$(W/L)_{opt}$=150, Peak η_{rect} =44%	$(W/L)_{opt}$=50, Peak η_{rect} =29%
V_P=0.4 V, I_L=50 μA	$(W/L)_{opt}$=400, Peak η_{rect} =46%	$(W/L)_{opt}$=400, Peak η_{rect} =48%	$(W/L)_{opt}$=150, Peak η_{rect} =36%

2.1.2.2 Overall Efficiency

Figure 2-10 is used to find the overall efficiency from the RF source (P_{avail}) to the output. In order to find the available power coming from the RF source (P_{avail}), both the resistor R_{IN} and capacitor C_{IN}, of the input admittance should be calculated

beforehand. The power delivered to the IC (P_{IC}) is entirely due to the resistive part since the reactive component does not dissipate power. Hence, R_{IN} could be found as below:

$$R_{IN} = \frac{1}{2}\frac{V_P^2}{P_{IC}} \tag{2-26}$$

Total input capacitance of the IC for N-stage rectifier could be found as below [21]:

$$C_{IN} = N.\left(\frac{C_I.C_P}{C_I + C_P}\right) + N.(C_{cp}) + C_{FIX} \tag{2-27}$$

where C_{FIX} is the fix capacitance including the sum of the bondpad and ESD capacitances, C_I is the coupling capacitance, C_P is the sum of the parasitic capacitances at the top plate of C_I, and C_{CP} is the parasitic capacitance at the bottom plate of coupling capacitor. By having P_{IN} from (2-23) and calculating R_{IN} and C_{IN}, the available input power could be found by calculating the reflection coefficients for a given antenna and matching network [17]. The overall power conversion efficiency (η) from the source to the output could be calculated as below:

$$\eta = \frac{V_{out}.I_L}{P_{avail}} = \eta_{rect}.\frac{P_{IC}}{P_{avail}} \tag{2-28}$$

Due to the specific focus of this research on the rectifier unit, in the experimental results, it is assumed that no matching network is used and the impedance of the power source is equal to 50 Ω.

2.1.3 Experimental Results

To validate the proposed model with measurement results, a multi-stage rectifier has been implemented in the UMC 0.18 µm CMOS process. Figure 2-13 shows the die micrograph of the rectifier. The integrated circuit is tested by a custom PCB with minimum dimensions and traces. To access the integrated circuit, bondwires are connected to RF, ground, and output pads. The size of the coupling capacitors is 3 pF, assuring a ripple-free voltage for the internal even nodes at the operating frequency. The size of the diode-connected transistors is set to $W/L=80$ which is the predicted optimum number for $I_L=5\ \mu A$. All measurements are done at 900 MHz ISM band. The RF signal is fed to the system with a 50 Ω RF signal generator (Agilent N9310A). Due to the careful design of the PCB and RF traces, the measured path loss of the

connectors and wires at the operating frequency is negligible and the power generated by the signal generator is directly reported as the available power. Figure 2-14 and Figure 2-15 compares the measured output voltage of the fabricated Dickson rectifier with simulation results and the models proposed by this work and [39] as a function of P_{avail} at different loads[1]. The model is also validated by comparing it with the measurements, simulations, and the data presented in [39] in Figure 2-16 at different loads. Table III compares this work with the previous state of the art.

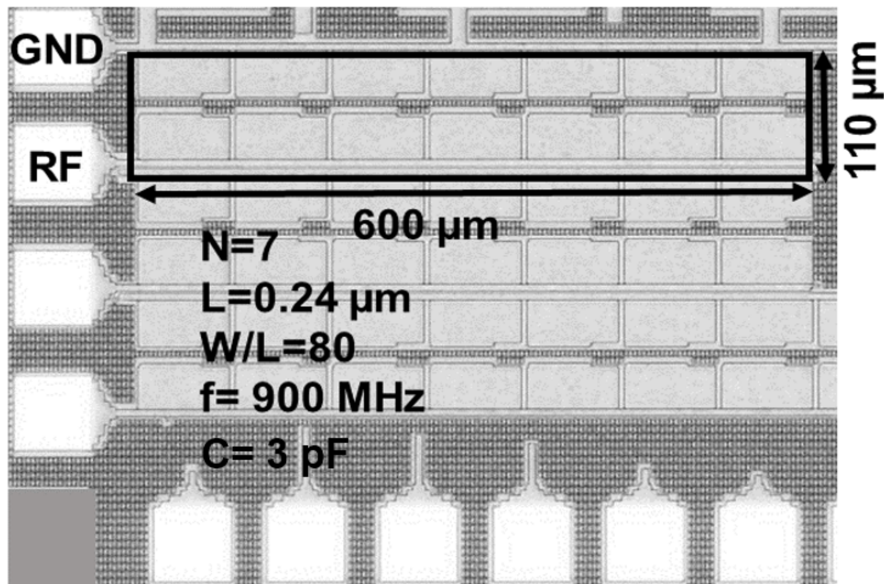


Figure 2-13: Die micrograph of multi-stage Dickson rectifier.

[1]In principle, this work finds the V_{OUT} as a function of I_L. Yet, when the given argument is R_L, V_{out} could be found by replacing the I_L with $(2NV_{UP})/R_L$ in (2-9). In this way, the generated voltage by each transistor will have a form similar to (2-14), but, the relevant coefficients in (2-15) will be modified. However, there is no straight forward approach for finding the output voltage in [10] as a function of the R_L. To compare the results with [10], this work sweeps the I_L for each RF amplitude and find the resulting input power and resistive load at the output.

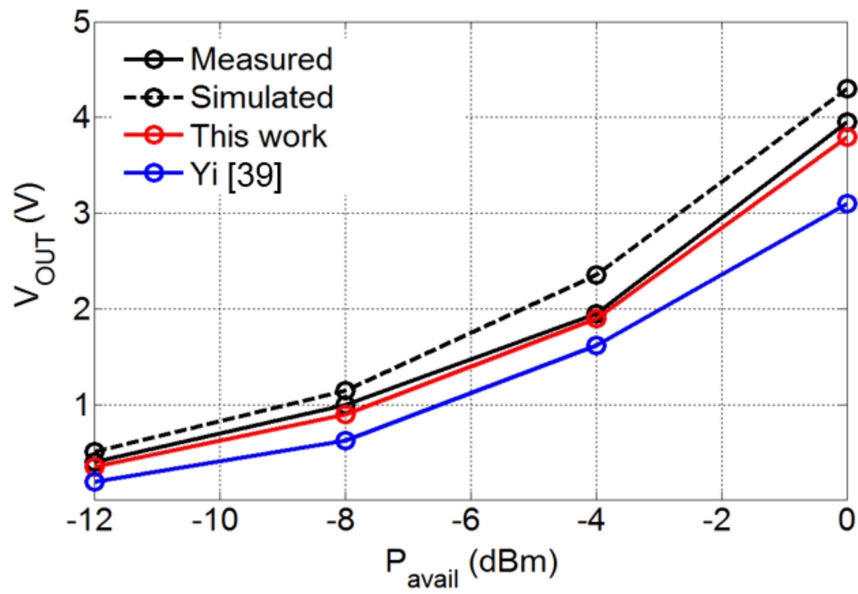


Figure 2-14: Simulation, modeling and measurement output voltage (R_L=1 MΩ).

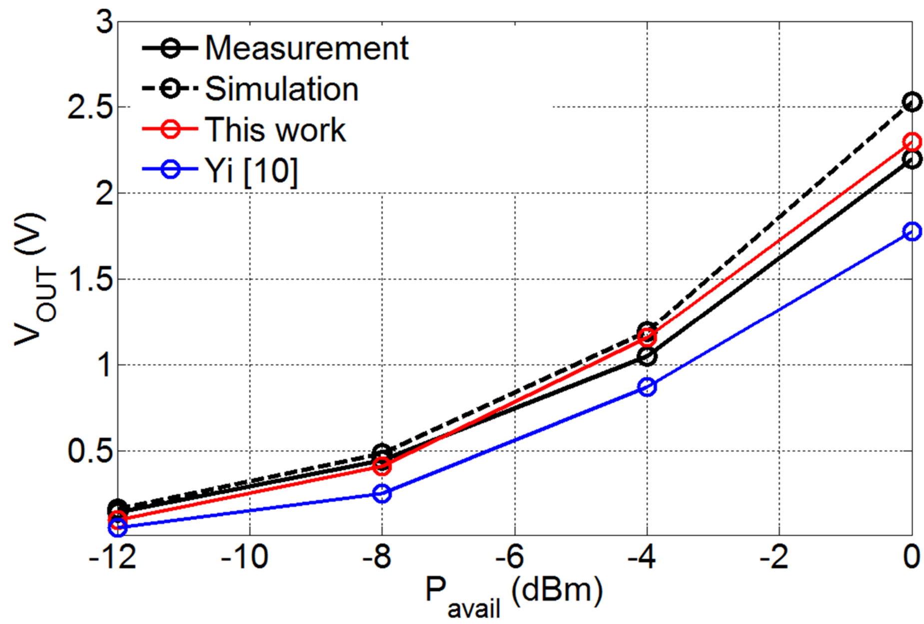


Figure 2-15: Simulation, modeling and measurement output voltage (R_L=50 kΩ).

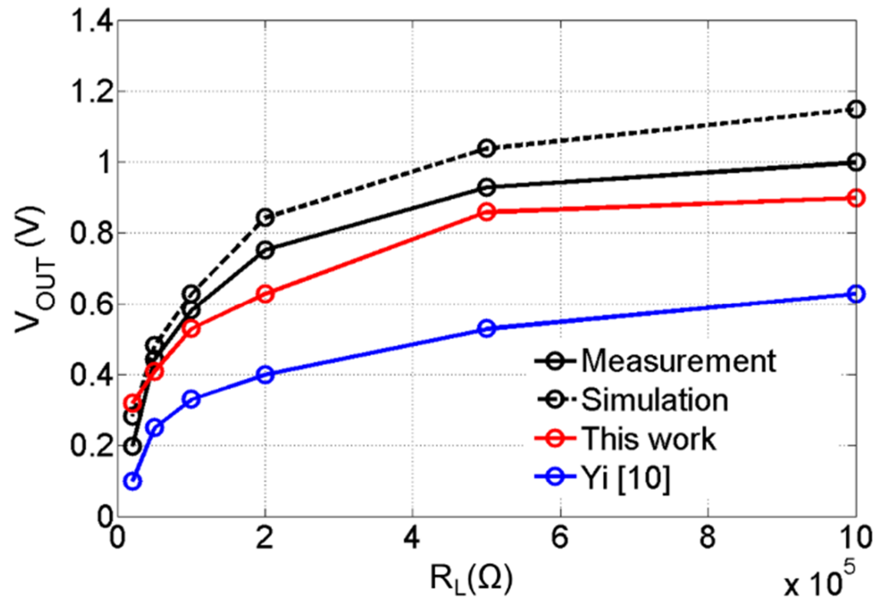


Figure 2-16: Output voltage for different load values (P_{avail}=-8 dBm).

Table 2-3: Comparison with State of The Art

Reference	J. Ye et al. 2007 [39]	R. E. Barnett et al. 2009 [22]	F. F. Dai et al. 2005 [48]	This work
Examination unit(s)	rectifier	rectifier	Clamp and Rectifier	Clamp
Methodology	Approximation of entering & exiting charge	Constant I_P/I_L assumption, calculation of Z_{IN}	Iteration	Approximate I_P/I_L, approximation of entering charge
Input/Output formula	Yes	Yes	Yes	Yes
Input power calculation and efficiency optimization	Yes	Yes	No	Yes
Compatible with different input RF and load currents	Yes	No	No	Yes
Process compatibility	No	No[2]	Yes	Yes[3]
Complexity	High[1]	Low	Low	Moderate
Technology/Frequency	CMOS/900 MHz	Schottky/900 MHz	CMOS/900 MHz	CMOS/900 MHz

1. Expression of the output voltage for even and odd number of stages is different.
2. The ratio of peak forward current to load current should be found by several SPICE simulations.
3. For different types of diodes employed in multi-stage charge pump, one can start with equation (7) and replace I_P with the relevant *I-V* relationship.

2.2 Threshold Self-Compensated UHF Rectifier

The threshold self-compensated architecture is an important circuit topology for converting RF signals with very low amplitude (less than 300 mV) and when the load current is limited to several µ-Amperes. It was firstly introduced in a patent [32] (and then expanded in [33]) to eliminate the intrinsic threshold voltage problem in wireless charging applications. Before starting to introduce the self-compensation architecture in detail, it would be helpful to investigate the intrinsic-V_{th} problem in detail.

Figure 2-17 shows the half-wave rectifier implemented with a diode-connected transistor. The forward charge delivery occurs when the drain voltage of the transistor gets higher than the source voltage. As can be seen from this figure, the diode-connected MOS transistor starts to conduct form the source to the load only when the

RF amplitude gets higher than V_{th}, meaning that considerable part of the incoming RF signal is wasted to overcome the intrinsic-V_{th} voltage. The most explicit drawback is that amount of the elaborated DC voltage at the load side becomes very low due to lack of sufficient stored charge on load capacitor (C_L). The problem is more severe in far-field applications where the amplitude of the incoming voltage is in the same order of the threshold voltage.

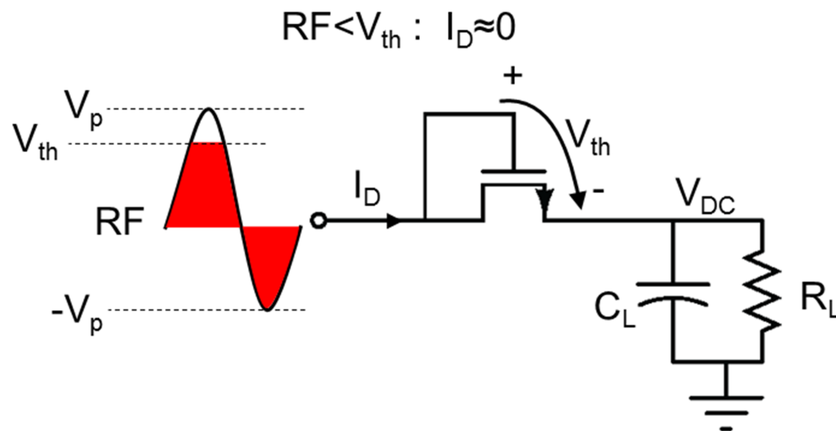


Figure 2-17: Intrinsic-V_{th} problem in half-wave RF-to-DC converter.

Circuit diagram of threshold self-compensated architecture is shown in Figure 2-18. The main motivation behind introducing the threshold self-compensation is to provide a positive offset between the gate and the source terminals without adding extra control circuitry. The technique uses the fact that for each stage of the rectifier chain, DC and RF voltages with an offset equal to the generated DC voltage per stage exist in the

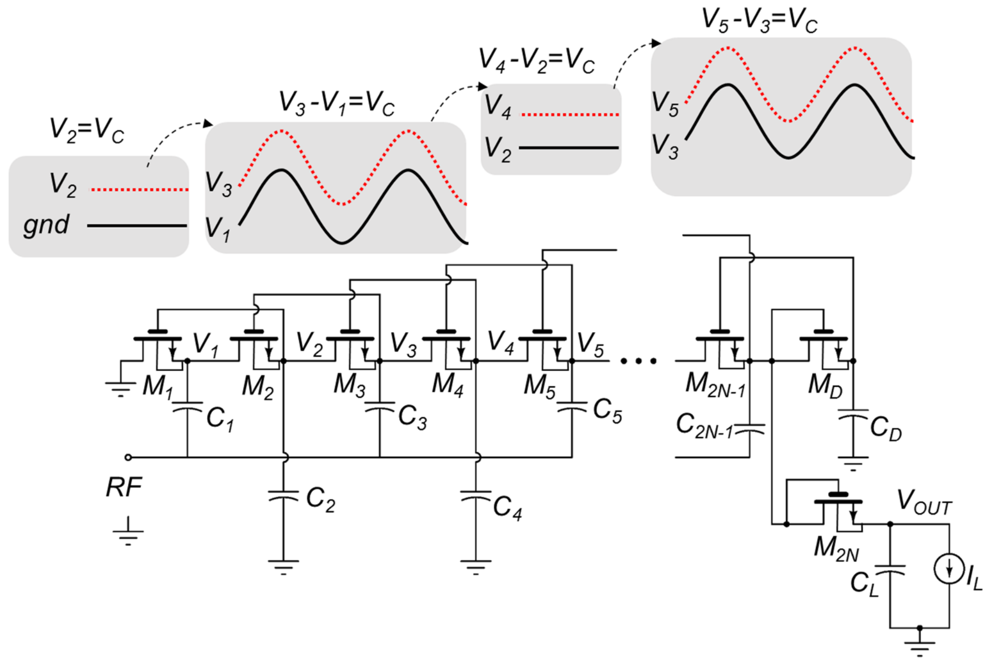


Figure 2-18: Schematic of threshold self-compensated UHF rectifier and steady state waveforms of each transistor.

right-neighbor stage. Hence, connecting the gate terminals to the source of the right neighbor transistors would be enough to provide the desired offset in order to cancel the intrinsic threshold voltage of the device.

The main benefit of the self-compensation technique is that, theoretically, the intrinsic V_{th} voltage could be completely canceled by simply adjusting the number of stages and device dimensions. However, this also brings the main limitation of this technique. A compensation voltage larger than the threshold voltage will get the rectifying devices conduct even under reverse swings, loosing this valuable energy, thus reducing the PCE. In order to achieve the maximum PCE, the rectifying device as well as the optimum number of stages must be carefully tuned with respect to the incident RF power and load power values. Hence, the incident power dynamic range over which the PCE of a given self-compensated rectifier is acceptable is very small. This highlights the importance of the careful selection of number of stages and device sizes for the given input and load power specifications early in the design phase.

Analysis of the PCE of the RF-to-DC converter employing standard Dickson topology has been done a number of times in the literature [49], [39], [22] , and in this thesis as detailed in the previous section. However, there is no study in the literature to address

the optimization problem of the self-compensated architecture. Hence, one should run extensive and time consuming SPICE simulations to find the optimum device size and number of stages for maximizing the PCE for given input RF power and output load. The principle of this work is based on using the similarity between dependence of PCE and load current (I_L) over the variation of the DC voltage (generated per stage). Proving the aforementioned similarity by both mathematical derivations and SPICE simulations, the optimum DC voltage which maximizes the power conversion efficiency is found. The formulated optimum voltage is used in charge conservation equations to find the optimum device dimension and stage number. The proposed method speeds up the design process considerably.

2.2.1 PCE and I_L Analysis in Single Stage Threshold Self-Compensated UHF Rectifier

The effect of the compensation voltage (V_C in Figure 2-18) on the performance of the rectifier could be best understood by comparing the power conversion efficiency of the self-compensated and the Dickson (with $V_C=0$) topologies using the same number of stages and diode dimensions as shown in Figure 2-19. In this plot, the simulated PCE is drawn versus the RF amplitude (V_{RF}). Starting from V_{RF}=0 up to V_{RF}=0.25 V, V_C in self-compensated rectifier helps to have higher output voltage for self-compensated architecture. However, as V_{RF} further increases, high discharge current

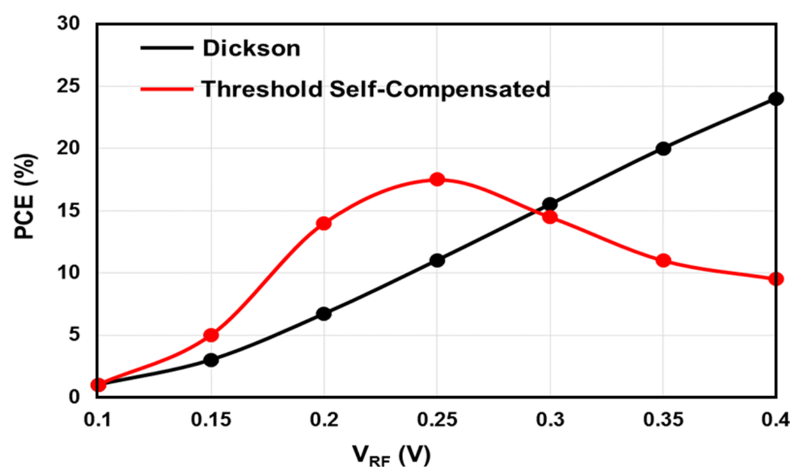


Figure 2-19: Comparison of power conversion efficiency in Dickson and self-compensated UHF rectifiers (f=900 MHz, N=5, W/L=100, R_L=10 kΩ).

from load to source nullify the forward charge yielding inferior performance of the self- compensated architecture. It is clear from the plot that if self-compensated architecture is used careful optimization of circuit parameters is required to achieve the peak PCE for a given set of operating conditions. The following sub-section discusses the dependence of PCE to V_C in more detail.

2.2.1.1 Power Conversion Efficiency of the Self-Compensated Rectifier

To ease the analysis of the basic building block of the multi-stage self-compensated structure (i.e. M_1, M_2, C_1, and C_2 in Figure 2-18), the unit cell is redrawn in Figure 2-20 by using ideal voltage controlled voltage sources to represent V_C. The body terminals in Figure 2-20 are connected to the source terminals (except the last stage) eliminating the V_{th} variation due to body effect. The analysis of the last stage will be provided in the content of this section. The power conversion efficiency of the rectifier is:

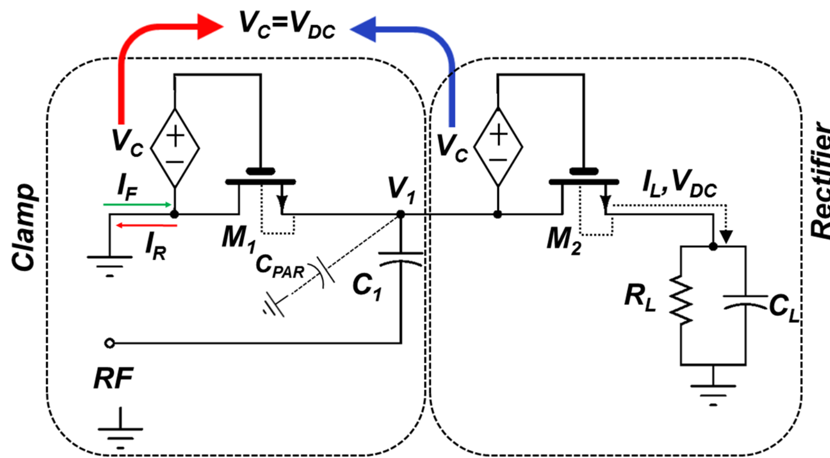


Figure 2-20: Unit cell of threshold self-compensated topology by representing the compensation voltages with voltage controlled voltage sources.

$$\eta_{rect} = \frac{P_{OUT}}{P_{IC}} = \frac{I_L.V_{DC}}{2P_{M1} + I_L.V_{DC}} = 1 - \frac{2P_{M1}}{2P_{M1} + I_L.V_{DC}} \qquad (2\text{-}29)$$

where P_{IC} is the average power delivered to the IC at steady state and P_{M1} is the power dissipated by M_1 [38]. By taking the derivative of η_{rect} with respect to V_{DC}, we have

$$\frac{\partial \eta_{rect}}{\partial V_{DC}} = -\frac{2\frac{\partial P_{M1}}{\partial V_{DC}}.(2P_{M1} + I_L V_{DC}) - \left(2\frac{\partial P_{M1}}{\partial V_{DC}} + \frac{\partial I_L}{\partial V_{DC}} V_{DC} + I_L\right).2P_{M1}}{(2P_{M1} + I_L.V_{DC})^2}. \tag{2-30}$$

Rearranging this equation yields to

$$\frac{\partial \eta_{rect}}{\partial V_{DC}} = \frac{\frac{\partial I_L}{\partial V_{DC}}.V_{DC} P_{M1} + I_L \cdot \left(P_{M1} - \frac{\partial P_{M1}}{\partial V_{DC}}.V_{DC}\right)}{(P_{M1} + I_L.V_{DC})^2} \tag{2-31}$$

Expressions of P_{M1} and I_L as a function of V_{DC} should be available to find the dependence of η_{rect} with respect to V_{DC}. The following subsections provide detailed analysis for P_{M1} and I_L and try to relate the interested terms to V_{DC} using single formulas. The principal approach of this work in elaborating the mathematical relationships is to approximate the steady-state waveforms with simple yet accurate well-known functions.

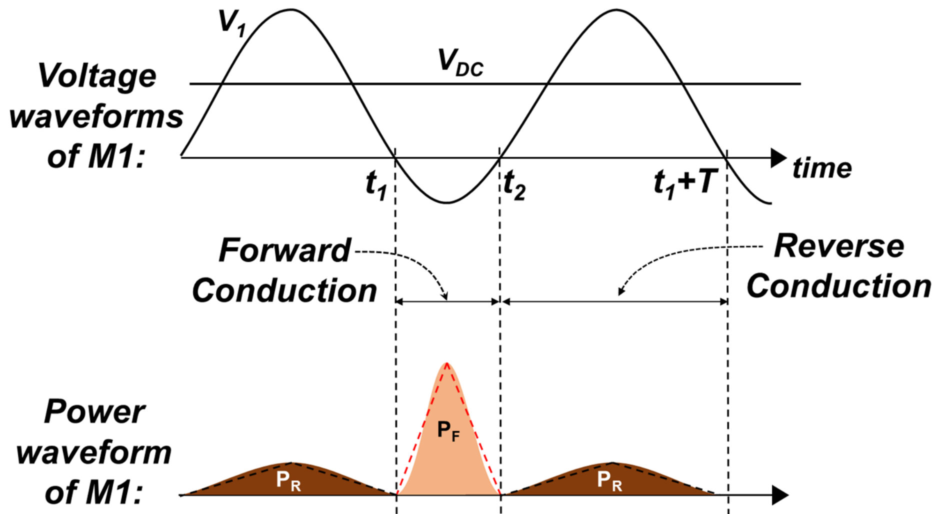


Figure 2-21: Steady state power waveform of a clamp transistor in .self-compensated architecture.

2.2.1.2 Dissipated Power at Steady State

Figure 2-21 draws the voltage and power waveforms of M_1 (in Figure 2-20) in the steady state. The total input power delivered to an N-stage self-compensated rectifier in steady-state is

$$P_{IC} = 2N.P_{M1} + I_L.V_{OUT} \qquad (2\text{-}32)$$

Basically, the power consumed by M1 (P_{M1}) consists of the dissipated power during the conduction phase (P_F) and the one during the isolation phase (P_R). Referring to Figure 2-21, both P_R and P_F areas can simply be approximated as below:

$$P_{M1} = \frac{1}{T}\left[\int_{t1}^{t2} P_F dt + \int_{t2}^{t1+T} P_R dt\right] \cong \frac{1}{T}\left[\frac{1}{2}\left(P_{F,max}.\Delta t_f\right) + \frac{1}{2}\left(P_{R,max}.\left(T - \Delta t_f\right)\right)\right] \qquad (2\text{-}33)$$

where $P_{F,max}$ and $P_{R,max}$ are the peak instantaneous powers at the middle of forward and reverse conduction time frames respectively, and $\Delta t_f/T$ is the conduction angle. Taking the incoming RF voltage in the form of $V_{RF}.sin(\omega t)$, the voltage at the top plate of the C_1 (V_1 in Figure 2-20) will be $V_{DC}/2+V_a.sin(\omega t)$ and conduction angle becomes

$$\frac{\Delta t_f}{T} = \frac{1}{2} - \frac{1}{\pi} sin^{-1}\left(\frac{V_{DC}}{2V_a}\right) \qquad (2\text{-}34)$$

where V_a is the RF amplitude at the top plate of C_1 and is related to input RF amplitude by

$$V_a = V_{RF} \cdot \frac{C_1}{C_1 + C_{PAR}} \qquad (2\text{-}35)$$

In the equation above, C_{PAR} is the sum of the parasitic capacitances at the top plate of C_1. Triangular approximation of the P_{M1} at steady state can be rewritten as

$$P_{M1} = \frac{1}{2} I_P \left(V_{DC} - \frac{1}{2}V_a\right)\frac{\Delta t_f}{T} + \frac{1}{2} I_R \left(V_{DC} + \frac{1}{2}V_a\right)\left(1 - \frac{\Delta t_f}{T}\right) \qquad (2\text{-}36)$$

where I_P and I_R denote the peak instantaneous currents at the middle of the forward and the reverse conduction phases respectively. The last step to obtain a formula to directly relate the P_{M1} to the V_{DC} is to substitute the I_P and I_R according to the *I-V* characteristic of the MOS transistor in strong and weak inversion regimes. It should be noted that the I-V relationship for the SOI devices are similar to the well-known formula for bulk CMOS technology [50]. The gate-to-source voltage of M_1 at the middle of the forward and the reverse conduction phases is V_{DC} and $V_{DC}+V_a/2$ respectively. Calculation of I_P and I_R based on BSIM model [44] for each V_{RF} asks for

noticing whether the device operates in weak or strong inversion region. However, the EKV model [51] offers a single relationship for the drain current of MOS transistors which is valid in weak, moderate and strong inversion regions:

$$I_D(V_G,V_S,V_D)=\frac{2\beta V_t^2}{\kappa}(i_f-i_r).(1+\lambda V_{DS}) \tag{2-37}$$

where V_G,V_S, V_D, and V_t are gate, source, drain and thermal voltages respectively. κ is the gate coupling coefficient, β is $\mu_n.C_{ox}$, and λ is the channel length modulation coefficient. The i_f and i_r have these definitions:

$$i_f=\left[ln\left(1+e^{\frac{\kappa(V_G-V_t)-V_S}{2V_t}}\right)\right]^2 \tag{2-38}$$

$$i_r=\left[ln\left(1+e^{\frac{\kappa(V_G-V_t)-V_D}{2V_t}}\right)\right]^2 \tag{2-39}$$

The final form of P_{M1} is:

$$\begin{aligned}P_{M1}=&\frac{1}{2}I_D\left(V_{DC},V_{DC}-\frac{1}{2}V_P,0\right)\left(V_{DC}-\frac{1}{2}V_a\right).\left(\frac{1}{2}-\frac{1}{\pi}sin^{-1}\left(\frac{V_{DC}}{2V_a}\right)\right)\\&+\frac{1}{2}I_D(V_{DC},0,)\left(V_{DC}+\frac{1}{2}V_a\right).\left(\frac{1}{2}+\frac{1}{\pi}sin^{-1}\left(\frac{V_{DC}}{2V_a}\right)\right)\end{aligned} \tag{2-40}$$

2.2.1.3 I_L-V_{DC} Relationship

Steady state voltage and current waveforms of the clamp transistor (M_1 in Figure 2-20) are shown in Figure 2-22. According to the charge conservation principle, the amount of net charge passes through the device should be equal to the charge delivered to the load. Referring to Figure 2-22, the basic form of the charge equality for M_1 becomes:

$$I_L\cong\frac{1}{2}\frac{\Delta t_f}{T}.I_P-\frac{2}{\pi}\left(1-\frac{\Delta t_f}{T}\right).I_R \tag{2-41}$$

Solving the direct integrals in (2-41) is complex due to the non-linear nature of the transistors and also sinusoidal form of the RF signal. The better approach would be to approximate the back and forth charges by noticing the special shape of the M_1 current inside the forward and the reverse conduction time frames.

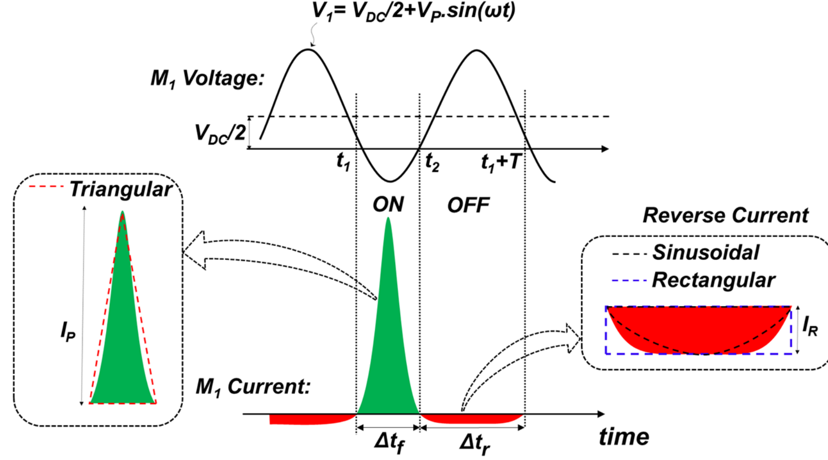


Figure 2-22: Steady state voltage and current waveforms of the clamp transistor.

In this way, the forward current could be well approximated by triangular approximation while the special form of the reverse current suggests its integral is between the rectangular ($\Delta t_r.I_{R,max}$) and sinusoidal ($1/\pi\Delta t_r.I_{R,max}$) waveforms. Hence, it would be the best to approximate it with $2/\pi\Delta t_r.I_{R,max}$. Using the above-mentioned approximations, (2-41) will be rewritten as below:

$$I_L \cong \frac{1}{2}\frac{\Delta t_f}{T}.I_P - \frac{2}{\pi}\left(1-\frac{\Delta t_f}{T}\right).I_R \tag{2-42}$$

where I_P, I_R , and $\Delta t_f/T$ have the same definitions as in (2-8).

Before interpreting (2-42), it should be noted that elaborating the I_L-V_{DC} relationship is based on the steady state current waveform of M_1 as depicted in Figure 2-22. However, simulated waveform of the device deviates from current waveform in Figure 2-22 due to the gate coupling current caused by the parasitic C_{gs} capacitance. The gate terminal of M_1 is V_{DC} and its source voltage is $V_{DC}/2+V_{RF}.sin(\omega t)$. The gate current due to parasitic coupling is $C_{gs}.\partial V_{gs}/\partial t$ and becomes non-negligible when the frequency of the incoming signal is high and the device operates in deep weak inversion. This observation is in agreement with the fact that as the RF amplitude is very low, its output voltage becomes independent from the threshold voltage and diode dimensions as noticed by [9], and [43]. According to simulations in the given process with V_{th}=0.29 V, and C_{gs}=10 fF (with W/L=10μm/0.24μm for M1 and M2), the current waveform in Fig. 7 is safe to use when V_{RF} is higher than 0.2 V.

Assuming the abundance of sufficient V_{RF}, (2-42) present a direct relationship between I_L and V_{DC} while using the device parameters and the V_{RF} as the input arguments.

Finding P_{M1} and I_L as a function of V_{DC} in (2-40) and (2-42), the η_{rect} in (2-29) could be drawn with respect to V_{DC}. The aim of this work is to take V_{RF}, I_L, and process parameters as the input arguments and find the optimum V_{DC} (denoted by $V_{DC(OPT)}$) for which the η_{rect} maximizes. Simplifying (2-40) and (2-42) while covering broad range of V_{RF} values is not possible since the natural logarithmic terms could not be expressed with single functions. Hence, the $V_{DC(OPT)}$ is found by solving $\partial\eta_{rect}/\partial V_{DC}=0$ using a CAD tool. Fig. 7 illustrates the optimum DC voltage for each RF amplitude while concurrently displays the V_{DC}, which results in the peak load current ($\partial\eta_{rect}/\partial V_{DC}=0$). The roots of both graphs are close to each other suggesting that finding the DC voltage for which the load current would be maximized could be used as an indicator for the point that η_{rect} have been maximized.

The major advantage of finding $V_{DC(OPT)}$ using $I_L(V_{DC})$ curve is that its peaking point could instantly be found by sweeping V_{DC} in (2-42) from 0 to $2V_{RF}$ using a CAD tool without needing to calculate the input power. Dividing V_{DC} to I_L at the peaking point of the I_L results the optimum load ($R_{L(OPT)}$). Figure 2-23 compares the $V_{DC(OPT)}$ and $R_{L(OPT)}$ predicted by (2-42) with simulation results. More details of the simulation results are presented in Figure 2-24 in which η_{rect} and I_L are drawn over the growth of the DC voltage for V_{RF}=0.3 V. Also, simulated I_L and η_{rect} and predicted I_L based on (2-42) is presented for further validation in Figure 2-25.

Aside from the fact that finding the $V_{DC(OPT)}$ form the charge conservation equation is straightforward and time-efficient, existence of W/L term in both back and forth charge terms in (2-42) makes the $V_{DC(OPT)}$ insensitive to the size variations. In other words, the calculated $V_{DC(OPT)}$ for each V_{RF} is unique and there is no need to run the optimization process for different diode dimensions. The insensitivity of the $V_{DC(OPT)}$ over the variation of diode dimension as predicted by the analysis is further validated by simulating the η_{rect} of unit cell for different diode dimensions in Figure 2-26. As a

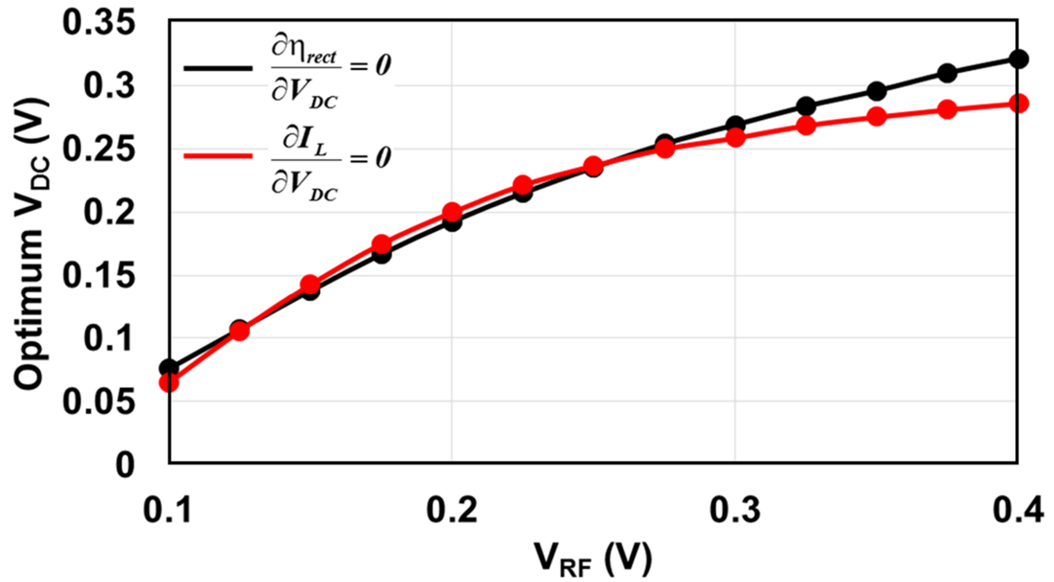


Figure 2-23: Comparison of the optimum DC voltage to maximize rectifier efficiency (using (3)) and load current (using (14))versus the RF amplitude.

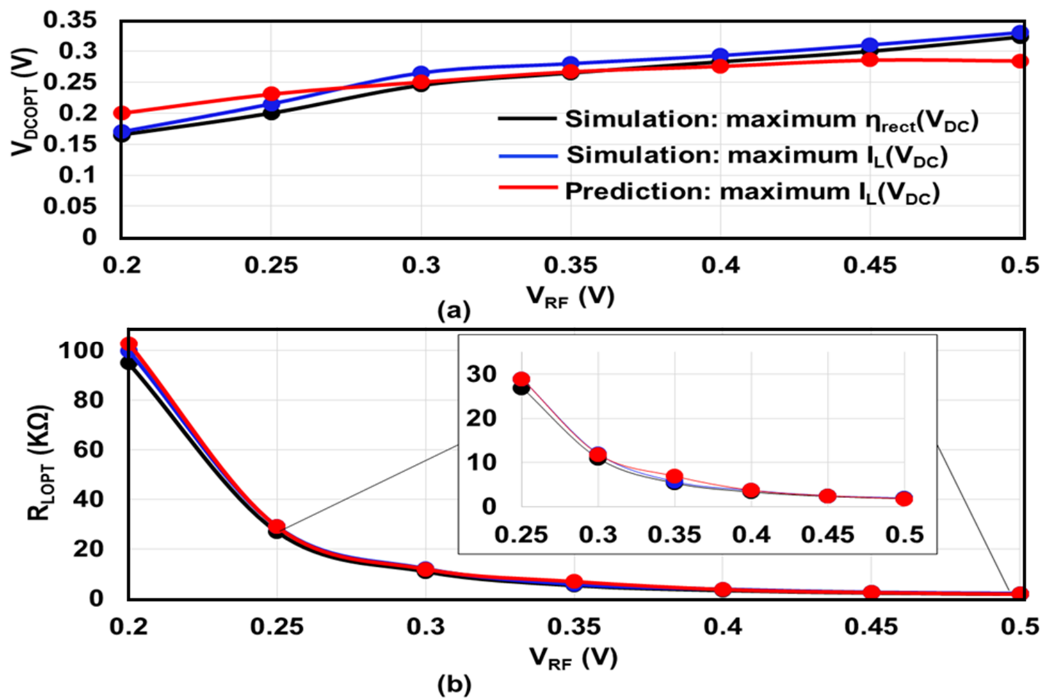


Figure 2-24: Comparison of simulated and predicted optimum parameters at the load side a) Optimum DC voltage b) Optimum resistance.

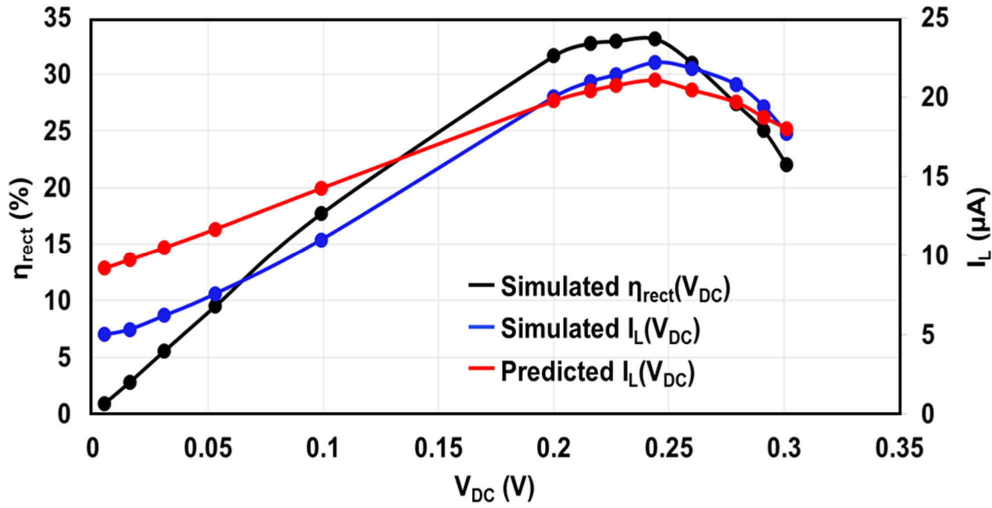


Figure 2-25: Comparison of simulated PCE, simulated I_L, predicted I_L over the growth of the V_{DC} (V_{RF}=300 mV, W/L=10μm/0.24μm, f=900 MHz).

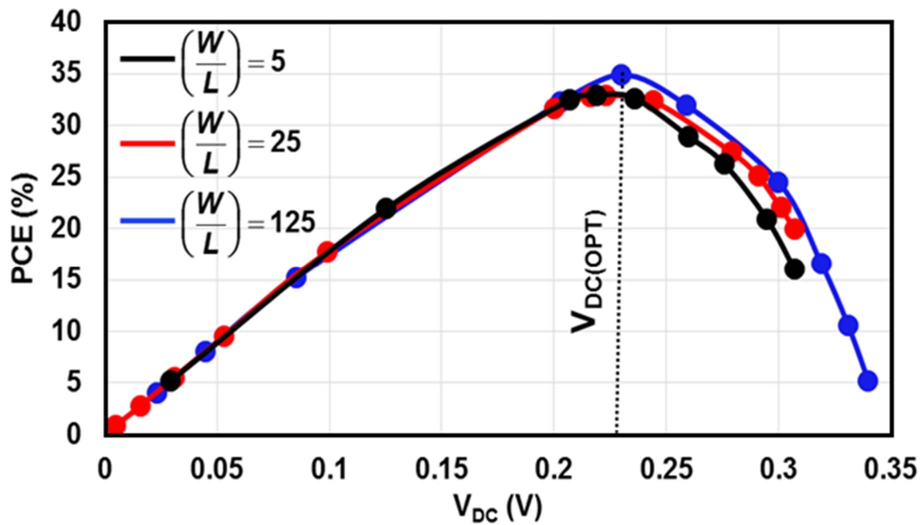


Figure 2-26: Simulation of efficiency versus the output DC voltage for different device sizes (f=900 MHz, N=5, V_{RF}=300 mV).

final remark, it should be noted that the most determining factor which affects both $V_{DC(OPT)}$ and $I_{L(OPT)}$ is the gate coupling coefficient (κ). By changing κ from 0.83 to 0.55 in (2-42), the peak load current and $V_{DC(OPT)}$ will reduce from 14 μA and 0.302 V to 5 μA and 0.247 V. The relevant parameters used for simulating the single stage self-compensated energy converter in 180 nm CMOS PD-SOI process are listed in Table 2-4. The following section will describe the procedure for selecting the

optimum diode dimensions and stages numbers of multi-stage threshold self-compensated rectifier based on elaborated $V_{DC(OPT)}$ and peak I_L values for the unit cell.

Table 2-4: Design Parameters

V_{th}	0.29 V
κ	0.83
$\mu_n C_{OX}$	290 μA/V^2
λ	0.85 V^{-1}
W/L	10 μm/0.4 μm

2.2.2 Analysis Extension to Multi-Stage Structure

Multi-stage self-compensated rectifier is constructed with cascading similar unit cells. Hence its symmetric nature helps to treat all stages equally except the last stage that has two key differences from the preceding stages: *i)* the compensation voltage for the last clamp transistor (M_{2N-1} in Figure 2-18) is generated by diode-connected dummy

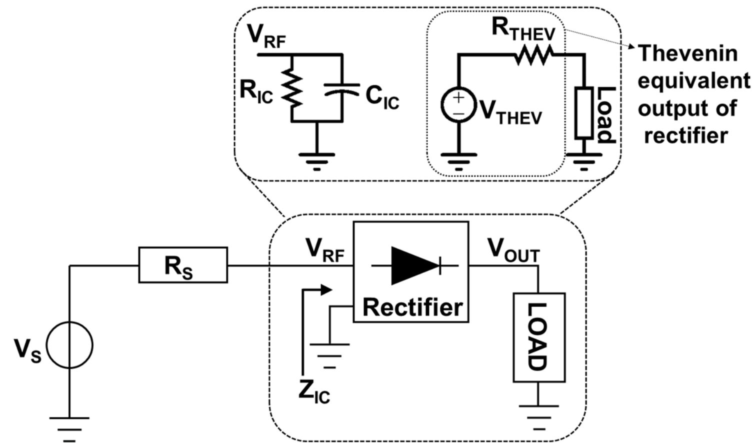


Figure 2-27: The model for analyzing the complete RF-to-DC conversion system.

transistor and *ii)* the last rectifier transistor (M_{2N} in Figure 2-18) is diode-connected transistor. Assuming that the stages from $i=1$ to $N-1$ generates $V_{DC(OPT)}$, the V_C in M_{2N-1} differs from $V_{DC(OPT)}$ and the compensation voltage for the M_{2N} in Figure 2-18 is zero. Since the load current flows from all stages is equal, the generated DC voltage from the last stage should be less than $V_{DC(OPT)}$ to pass the same I_L. To ease the calculations, this work assumes that, the last stage does not add any DC voltage to the

output. Then, by applying V_{RF} at the input, the optimum number of the stages, N_{OPT}, to provide the desired V_{OUT} is equal to:

$$N_{OPT} = 1 + \frac{V_{OUT}}{V_{DC(OPT)}} \tag{2-43}$$

As discussed above, the $V_{DC(OPT)}$ does not shift by changing W/L ratio, however, it adjusts the I_L. Thus, W/L ratio should be used to set the peak value of I_L in (2-40) to the desired value ($I_{L,OPT}$). The optimum diode dimension $(W/L)_{OPT}$ is

$$\left(\frac{W}{L}\right)_{OPT} = \frac{I_{L,OPT}}{I_{L,PEAK}} \cdot \left(\frac{W}{L}\right)_{M1} \tag{2-44}$$

where $I_{L,PEAK}$ is the peak number of I_L in (2-41) and (2-42) founded by substituting V_{DC} with $V_{DC(OPT)}$.

After determining N_{OPT} and $(W/L)_{OPT}$, the dissipated power of the optimally designed self-compensated structure would be found by (2-40). Calculating the available power from the RF source could be done by the help the model presented for RF-to-DC converter system in Figure 2-27 [22]. In this figure, the RF source is represented with an ideal voltage source in series with a resistance and due to special focus of this work on the rectifier part impedance matching network is eliminated. Having the input

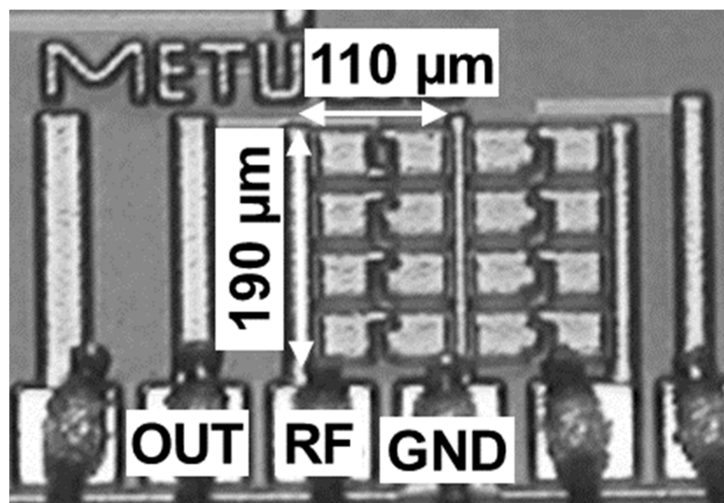


Figure 2-28: Die micrograph of the fabricated threshold self-compensated rectifier.

impedance of the rectifier, available RF power from the source (P_{avail}) could be calculated from P_{IC} and V_{RF}. The rectifier input impedance (Z_{IC}) is modeled by shunt

$R_{IC}//C_{IC}$ combination which is accurate when the input frequency is low enough to neglect the parasitic inductance [52]. The resistive part of the input impedance of the IC (R_{IC}) is:

$$R_{IC} = \frac{1}{2}\frac{V_{RF}^{2}}{P_{IC}} \tag{2-45}$$

Estimating the total input capacitance (C_{IC}) is too complex since the most contribution of the parasitic capacitances in PD-SOI transistors comes from floating body effect (FBE) [53] and predicting the junction capacitance from body to source/drain terminals is notoriously difficult. Hence, it would be the best to find C_{IC} by harmonic balance simulation.

2.2.3 Comparison of Model with Simulation and Measurement

This section verifies the analysis of the threshold self-compensated rectifiers by comparing it with simulation (in Cadence Spectre) and measurement using 1.5 V PD-SOI transistors of a 0.18-μm CMOS process. A 4-stage threshold self-compensated structure with W/L=10μm/0.4μm is fabricated and its microphotograph is shown in Figure 2-28. The aspect ratio of the fabricated transistors is equal to the one of transistors in unit cell (in Figure 2-20) to easily substitute the $V_{DC(OPT)}$ and $R_{L(OPT)}$ of the unit cell presented in Section III to the 4-stage structure. For testing each rectifier, three wirebonds are used: RF, ground, and output. The PCB is fabricated with minimum dimensions to minimize the loss. The RF signal is fed through a 50 Ω RF signal generator operating at 900 MHz. Due to high quality of the coaxial cable (connected between the RF source and PCB) and small dimensions of the PCB compared to the wavelength, the instrumental loss added by the test setup is negligible and the available power by the signal generator is reported as P_{avail}. At first, the integrity of (2-42) to predict the optimum W/L ratio and number of stages are verified by simulation. Table 2-5 lists the optimum diode size (to yield the maximum PCE) and number of stages found by simulation. The design parameters are selected to provide maximum PCE for each RF amplitude while connecting a specific load at the output. The connected load for the weak and the strong inversion regions is chosen differently to keep the stage numbers in a reasonable range. Good agreement between the transient simulations and the predicted optimum numbers is observed thanks to accuracy of the approximations utilized to elaborate load current and IC input power

in addition to robustness of the EKV model the I-V characteristic of device at different regions. Figure 2-29 provides more detail about the simulated PCE and V_{OUT} over the growth of the device size for two V_{RF} values. Closeness of the V_{OUT} to target output voltage 0.9 is a measure for verifying that the number of stages are selected correctly.

Table 2-5: Comparison of Simulated and Estimated Diode Dimension and Stage Number and Dissipated Power

Load	V_{RF}	Simulated $(W/L)_{OPT}$	Predicted $(W/L)_{OPT}$	Predicted N_{OPT}	Simulated V_{OUT} @ $(W/L)_{OPT}$
V_{OUT}= 0.9 V R_L=450 kΩ	200 mV	23	30	6	0.882
	250 mV	5	7	4	0.729
V_{OUT}= 0.9 V R_L=45 kΩ	300 mV	26	30	4	0.85
	350 mV	12	15	4	0.885
	400 mV	6	8	4	0.9
	450 mV	4	5	4	0.9

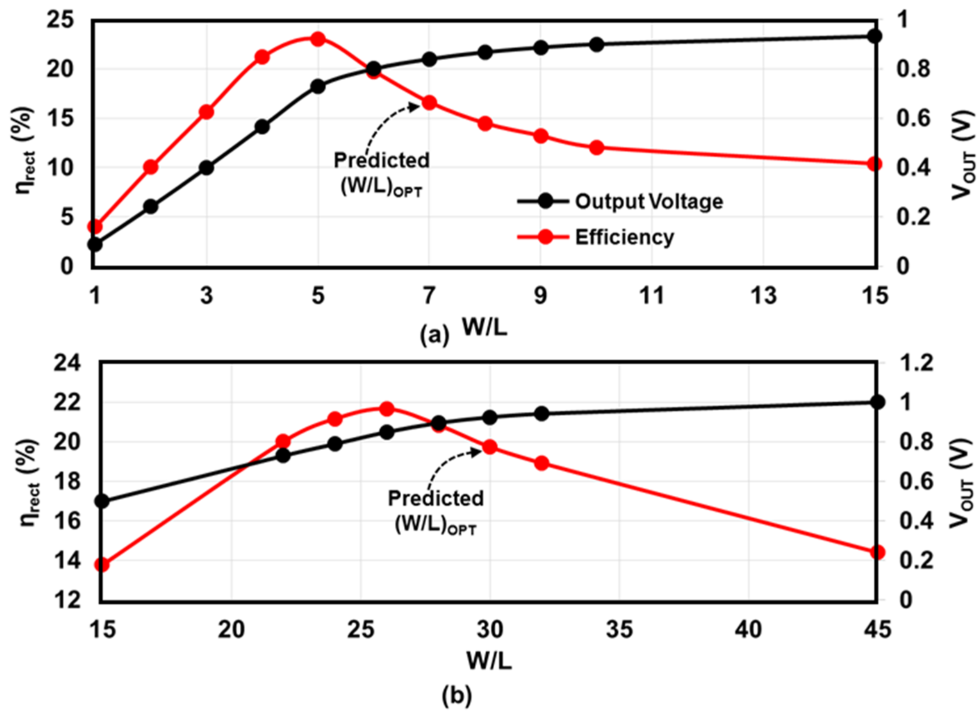


Figure 2-29: Comparison of simulated and predicted optimum W/L (L=0.25 µm) for a) V_{RF}=0.25 V and b) V_{RF}=0.3V.

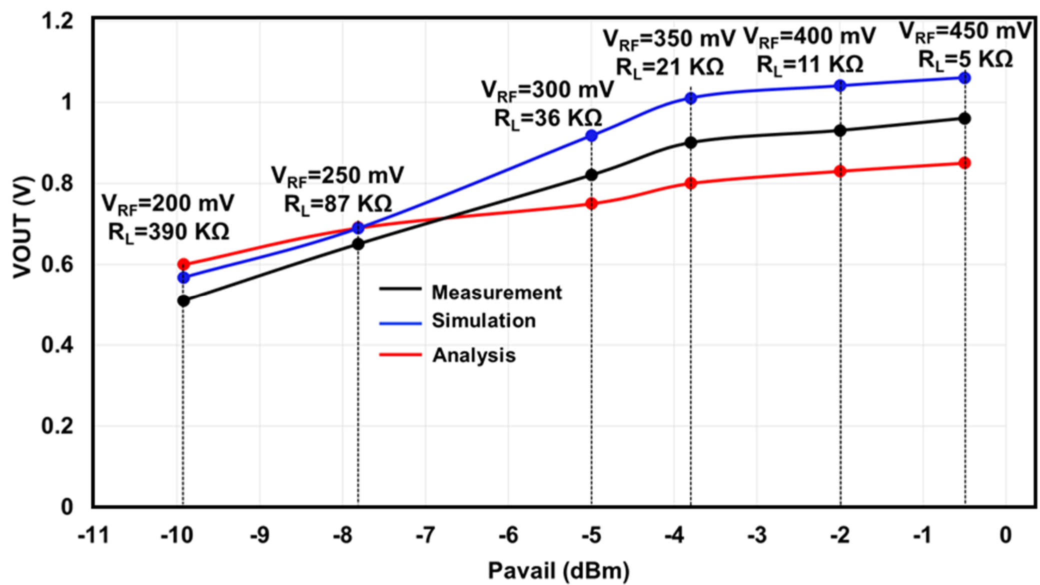


Figure 2-30: Comparison of predicted V_{OUT} with simulation and measurement results (R_L is the optimum load founded by analysis).

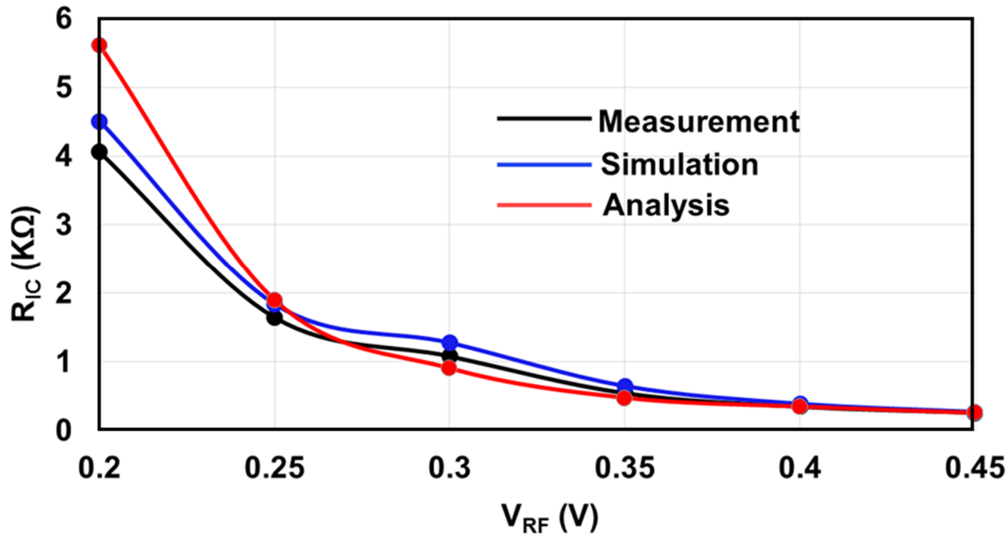


Figure 2-31: Comparison of the predicted IC input resistance with simulation and measurement while connecting optimum load for each RF amplitude.

The reliability of the mathematical equations is also confirmed by comparing the predicted V_{OUT} with simulation and measurement results. The connected load for each point for all graphs is R_{LOPT} which is found by (2-42) for a 4-stage rectifier with W/L=30. The imaginary part of the Z_{IC} is found by simulating the circuit while adding the parasitic effects of the RF pad, ESD circuitry according to the data provided by the foundry.

Aside from W/L and N, estimating the resistive part of the input impedance R_{IC} is helpful in the design of the interface circuit between antenna and rectifier. Figure 2-30 compares the estimated R_{IC} with simulated and measured (with network analyzer) at different RF powers. Similar to Figure 2-31, for each RF power the R_{LOPT} obtained from (2-41) is connected during the elaboration of all graphs.

As a conclusion to this chapter, the Dickon and the threshold self-compensated rectifiers are investigated in detail. A general formula is presented for the Dickson rectifier to find the DC voltage of the rectifier at a broad range of RF amplitudes. The novelty of the presented model for the Dickson rectifier is to use the ratio of the peak forward current over the load current and provide an effective method for its approximation. For the threshold self-compensated UHF rectifier, the optimum device

aspect ratio and the optimum number of stages are found by noticing the coherence between the dependence of the load current and power conversion efficiency on output DC voltage. Then, using charge conservation principle, the generated output DC voltage for the optimum self-compensated rectifier is found by a direct formula. Both models are verified with simulation and measurement results.

Dickson and threshold self-compensated rectifiers are widely used in industrial products (due to their simplicity) and their precise analysis is very helpful. However, there is significant room to apply circuit techniques and improve the performance of the basic UHF rectifiers. The following chapter introduces two novel circuit structures for UHF rectifiers.

CHAPTER 3

3 NEW UHF RECTIFIER ARCHITECTURES

Aside from the analysis and modeling of well-known UHF rectifiers used for RF-to-DC conversion, two novel architectures are also developed during this Ph.D. research. The fundamental idea of both structures are based on compensating the intrinsic threshold voltage to improve the power conversion efficiency of the rectifiers when the incoming RF amplitudes is very low (less than -10 dBm). As discussed in chapter 2, the major advantage of the self-compensation technique is its simplicity. However, its main drawback arises from the dependence of the compensation voltage on the generated DC voltage per stage. Recalling that the compensation voltage on one hand increases the forward conduction current and on the other hand leads to extra discharging current, it can be concluded that when the generated DC voltage per stage exceeds a predefined value, extra leakage current degrades the power conversion efficiency. The architectures introduced in this chapter aims to address the extra leakage problem by different circuit techniques.

The first circuit topology is the "Self-calibrated UHF rectifier" which is an improvement over the threshold-compensation technique specially developed for wireless charging applications. In these applications, having high power conversion efficiency for different RF power levels is required to scavenge the maximum RF power from all potential RF sources. Unfortunately, in threshold self-compensation technique, power efficiency shows a bell-shape response over the variation of the incoming RF amplitude suggesting that the PCE drops from its peak value when the incoming RF power changes from an optimum point. Self-calibrated rectifier on one

hand provides the required compensation voltage to overcome the intrinsic threshold voltage at weak RF signals and on the other hand avoids efficiency reduction due to the high compensation voltage when the RF amplitude is high.

Another rectifier architecture is the “Switched-gate” architecture which introduces new ***adaptive threshold cancelation*** scheme instead of commonly used constant compensation technique. It tries to increase the peak power conversion efficiency of the structure when the RF amplitude is low. Having higher peak power in the remote device allows increasing the complexity of the signal processing task in the wireless device. The principle of switched-gate technique is to separate the steady-state operation into forward and reverse conduction modes. It is essential due to the fact that the compensation voltage is desirable during the forward conduction mode and is not desirable during the reverse isolation. Hence, the technique tries to offer the compensation voltage during the forward conduction phase exclusively. The result is the enhancement of the charge delivery from the source to the load during the forward conduction phase while the reverse discharge current is blocked. Consequently, the power conversion efficiency is increased compared to the threshold self-compensated architecture which uses constant voltage to overcome the intrinsic-V_{th} voltage.

3.1 Self-Calibrated UHF Rectifier

A major concern in the design of RF harvesting system is the deviation of the intensity of the available RF power from the theoretically expected values (by Friss equation in (1.2)). Several factors such as multipath fading and insertion of an unintended object between the portable device and the RF source cause this discrepancy. Moreover, some materials lead to impedance changing in the receiver antenna that reduces the power coupled to the tag. For example, when the tag’s antenna is in contact with a metallic material, the electrical coupling between the two reduces the power of the tag. Water molecules may also impact the performance of the wireless tag. The antenna will lose energy in the vicinity of the water since the vibration of the H_2O molecules will form a low impedance path for absorbing the EM energy [54]. Hence, keeping the power conversion efficiency high for a broad range of RF power is of paramount importance to have the harvester work at different conditions and distances from the source.

As detailed in the previous chapter, the main idea of the threshold self-compensation [32] is to provide a positive offset between gate and source terminals of the clamp and rectifier transistors by connecting the gate terminals of each transistor to the source of the right neighboring transistor. The idea is further developed in [33] to increase the amount of compensation voltage by elongating the gate connection path. In principle, self-compensation technique uses the abundance of different voltage levels at the neighboring stages to generate the compensation voltage (V_C). However, this voltage is not well controlled and depends on several factors including the number of stages, size of the devices, load current, and more importantly the intensity of the incoming power. Deviation of the compensation voltage from its optimum value degrades the advantage of compensation technique by either preventing the generation of sufficient current during the forward conduction time or by degrading the blocking feature by allowing the flow of significant current in the reverse isolation time.

This sub-section presents a new self-calibrating technique for generating the compensation voltage. The compensation voltage is generated with passive rectifiers, making it independent form the intensity of the RF power and the value of the load to the output. The proposed self-calibrated rectifier circuit includes a simple stage-by-stage threshold compensation technique which keeps the compensation voltage very close to the intrinsic threshold voltage of the rectifying device itself, providing the best balance between the conduction and isolation features of the pumping devices. As a consequence, the power conversion efficiency (PCE) does not degrade with the variation of the incident RF power for a wide input power range. Moreover, with this technique, PCE reduction due to the variation of the output load and other design parameters of the rectifier structure (e.g. number of stages, device size, etc.) is avoided.

3.1.1 Optimum Compensation Voltage.

Figure 3-1(a) shows a UHF rectifier with ideal threshold compensation using batteries. This circuit is useful especially helpful for understanding the impact of the V_C over the voltage and power efficiency of the rectifier through the simulations. In Figure 3-1(b), V_C is swept together with the connected load. In Figure 3-1(c) and 3-2(d) compensation voltage is swept along with the RF amplitude and width (W) of the rectifying devices respectively. As can be seen from all three figures, the maximum

output voltage is obtained when the V_C is at the vicinity of the intrinsic threshold voltage of the device. Lower V_C will limit the forward conduction current while a higher value will lead to large reverse current. Hence a good compensation scheme

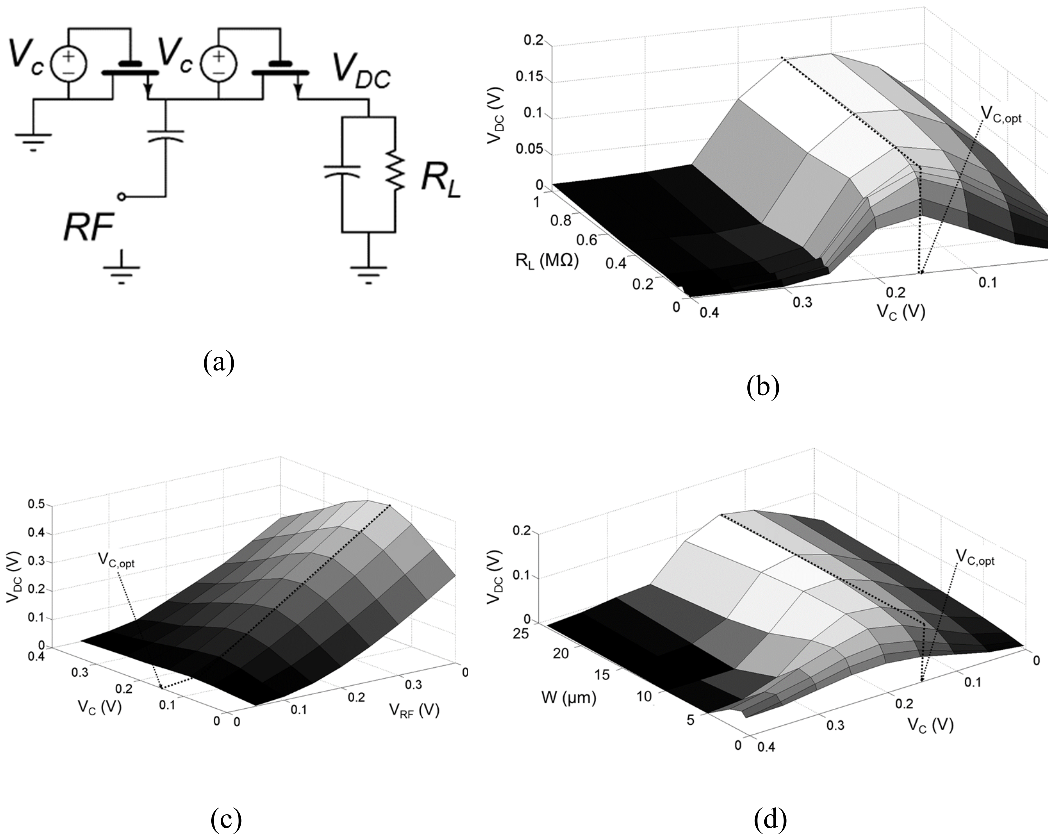


Figure 3-1: a) A single stage UHF rectifier with ideal threshold voltage compensation b) V_{DC} versus variation of compensation voltage and load (W/L=2.4μm/0.24μm, V_{RF}=150 mV) c) V_{DC} versus variation of compensation voltage and RF amplitude (W/L=24μm/0.24μm, RL=10 kΩ) d) V_{DC} versus variation of compensation voltage and device width (R_L=100 kΩ, V_{RF}=150 mV, L=0.24 μm).

must create a V_C value which is almost equal to V_{th} regardless of other parameters like the RF input power, operation frequency, and output load. Having this advantage with threshold compensation technique in that the compensation voltage depends on the generated DC voltage per stage was not possible. Keeping the compensation voltage at its optimum point independently from the other parameters within the whole possible input power range of the circuit is the primary goal of the proposed self-calibrated technique. The following part of this thesis represents the circuit realization of the self-calibration technique in details.

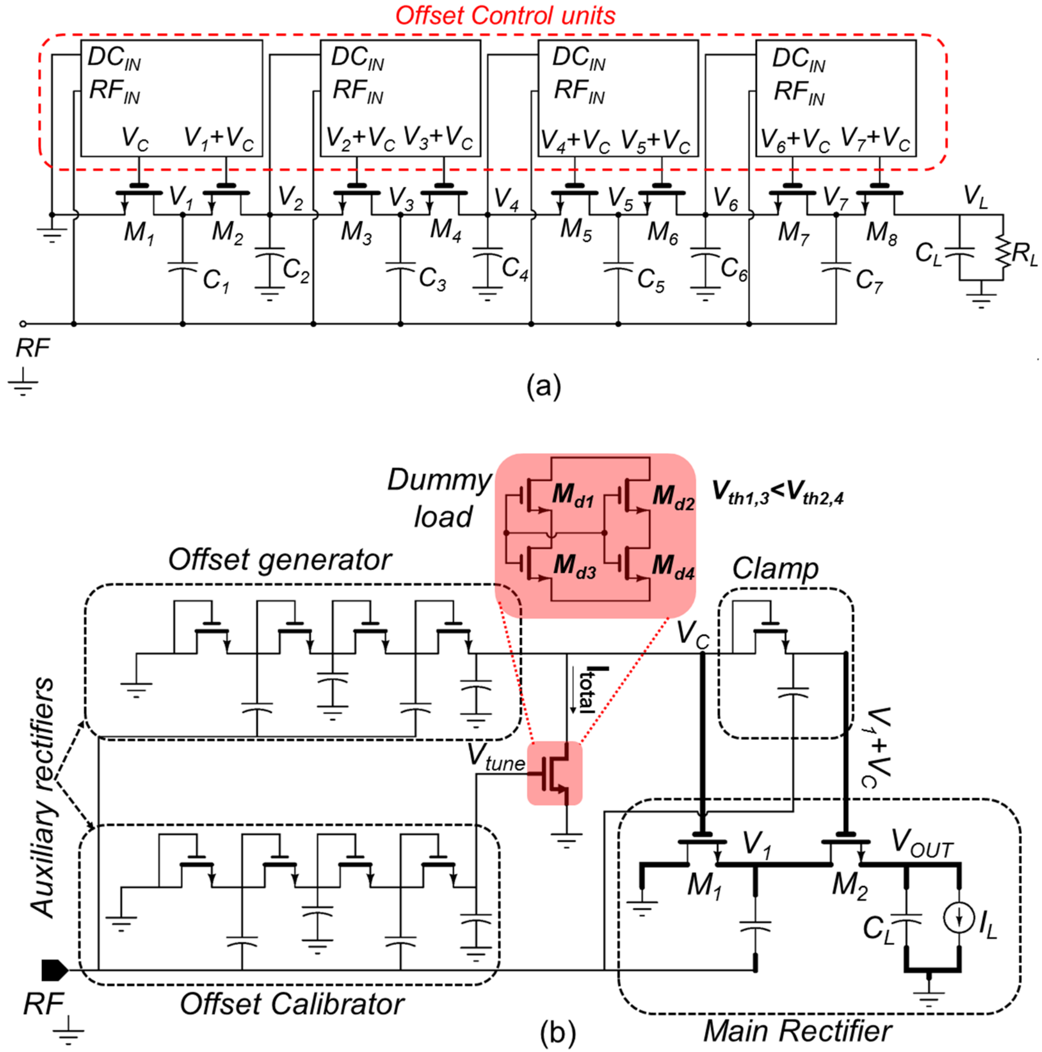


Figure 3-2: Self-calibrated UHF rectifier. a) Multi state block diagram b) single stage structure with detailed circuit realization.

3.1.2 Self-Calibrated Threshold Compensation

Figure 3-2 (a) shows the block diagram of the proposed UHF rectifier with self-calibration technique to keep the compensation voltage at the optimum value. The core of the structure is similar to Dickson architecture with the only difference in configuration of the gate terminals. They are controlled with offset control units, which provide a specific offset between the gate and the source terminals. Offset control unit senses the incoming RF voltage in addition to the generated DC voltage from the previous stage and tunes the gate voltage of the corresponding transistors to achieve the desired compensation voltage.

The circuit realization of the unit cell of the proposed RF-to-DC converter is presented in Figure 3-2(b). The structure includes a main rectifier (M_1, M_2, C_1, C_2), two auxiliary rectifiers, a dummy load, and a clamp circuit. Auxiliary rectifiers are two stage diode connected Dickson rectifiers. One of them is the offset generator rectifier, which converts the RF signal into DC form and generates the compensation voltage for M_1. This voltage will increase in proportion to the incident RF power. Another auxiliary rectifier (offset calibrator) is inserted to compress V_C with the aid of the dummy load. The principal of operation is as follows: As the incident RF power increases, the offset generator rectifier increases the compensation voltage. Meanwhile, the output voltage of the offset calibrator rectifier also increases getting the dummy load pulling more load current, counterbalancing the effect of higher input RF voltage. It should be noted that the Dickson structure is not an attractive option to generate the DC voltage at very low RF powers due to the intrinsic threshold voltage of its pumping devices. However, due to its negligible load current, its generated voltage will be sufficient even if its diodes are operating in the subthreshold regime. Furthermore, the number of stages would be used as a degree of freedom to increase the required DC voltage at a given input RF level. Both offset generator and calibrator rectifiers are implemented similarly while having W/L=0.24µm/10 µm for MOS diodes.

The aim of the dummy load circuit is to draw the desired current from the offset generator rectifier to keep V_C constant over a broad range of input power. Using the low threshold voltage (LVT) transistors in the main rectifier (M_1 and M_2 in Figure 3-2(b)) it is intended to fix the compensation voltage at 0.15 V in the given process. In order to ease the design procedure of the dummy load, the open-load voltage of the

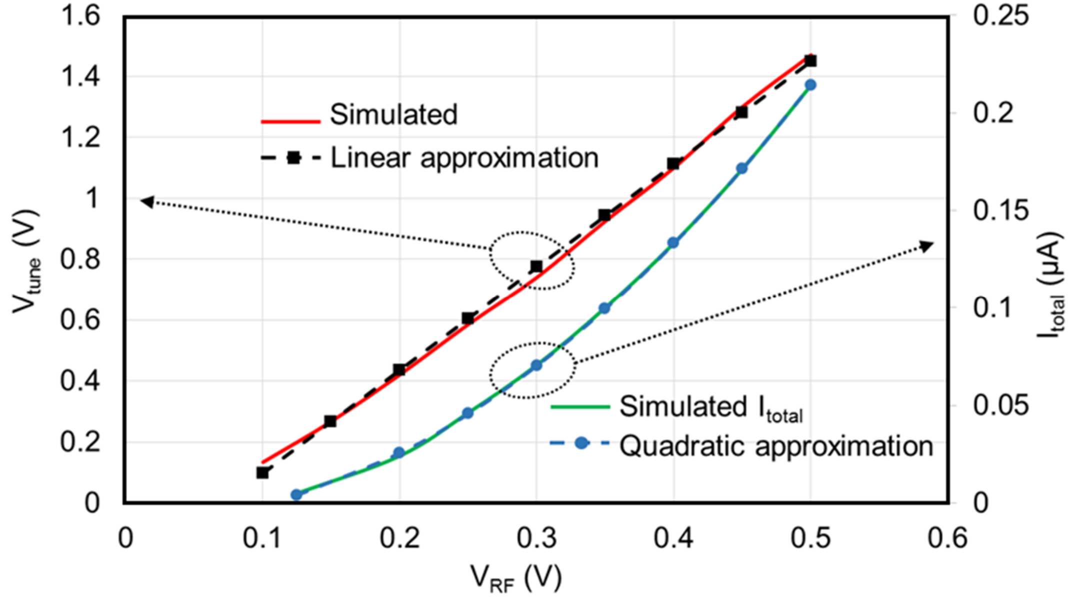


Figure 3-3: simulated V_{tune} and required I_{total} to set V_C=0.15 V with their linear and quadratic approximations.

auxiliary rectifiers (gate-source voltage of the dummy transistor) and the required drain current from the dummy load to fix the V_C should be investigated. Figure 3-3 shows the open-load voltage and the required dummy load current (I_{total}) over the growth of the input RF voltage. This figure suggests that the open load voltage of the rectifier (V_{tune}) can be well approximated by a linear relationship as

$$V_{tune} = b_1 + b_2 V_{RF} \tag{3-1}$$

where V_{RF} is the amplitude of the input RF voltage and b_1, and b_2 are the fitting parameters in the given process. Also, it can be understood that the desired load current which should be provided by the dummy load to fix the V_C at 0.15 V can be approximated with a square relationship:

$$I_L = a_1 V_{RF}^{\ 2} + a_2 V_{RF} + a_3 \tag{3-2}$$

where a_1, a_2, and a_3 are the fitting parameters. To fulfill the required I_L, dummy load is constructed with a combination of two parallel branches (Figure 3-2(b)). The sizes of the series transistors in each branch is same but threshold voltage of M_{d2} and M_{d4} is higher than that of M_{d1} and M_{d3}. By applying RF signals with amplitudes of higher

than 0.1 V, all dummy transistors will operate in the linear region. Equating the current passing through M_{d1} (I_{Md1}) and M_{d3} (I_{Md3}) in Figure 3-2(b) leads to:

$$k_{n1,3}\left[(V_{tune}-V_{th}).V_{DS3}-\frac{1}{2}V_{DS3}^{\ 2}\right]= \\ k_{n1,3}\left[(V_{tune}-V_{DS3}-V_{th}).(V_c-V_{DS3})-\frac{1}{2}(V_C-V_{DS3})^2\right] \quad (3\text{-}3)$$

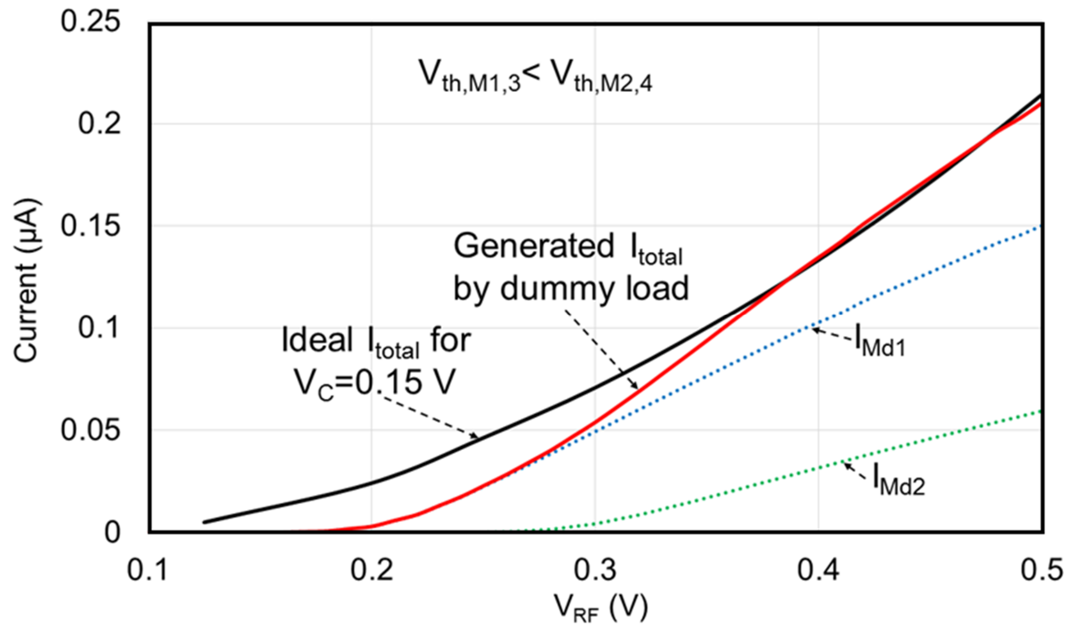
where $k_{n1,3}$ is $\mu_n C_{ox}(W/L)_{1,3}$ and V_{DS3} is the drain-source voltage of M_{d3}. V_{DS3} can be replaced as a function of V_{tune}, V_{th}, and V_C. Then, I_{d1} would be written as:

$$I_{d1}=k_{n1,3}\left[\frac{1}{2}V_c(V_{tune}-V_{th1,3})-\frac{1}{4}V_c^{\ 2}\right] \quad (3\text{-}4)$$

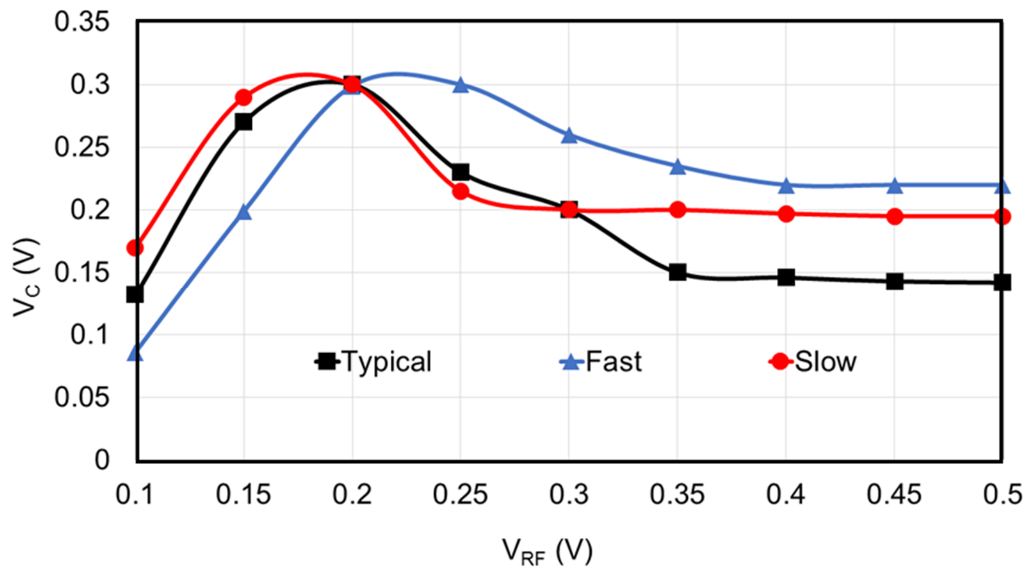
By replacing the V_{tune} from (3-1) the current passes from two parallel branch becomes:

$$I_{total}=k_{n1,3}\left[\frac{1}{2}V_c((b_1V_{RF}+b_2)-V_{th1,3})-\frac{1}{4}V_c^{\ 2}\right]+ \\ k_{n2,4}\left[\frac{1}{2}V_c((b_1V_{RF}+b_2)-V_{th2,4})-\frac{1}{4}V_c^{\ 2}\right] \quad (3\text{-}5)$$

Assuming the operation of M_{d1}-M_{d4} in linear region, V_C in (3-5) can be treated as a constant over the variation of V_{RF}. In this case, I_{total} (as a function of V_{RF}) becomes the sum of two linear current terms with different slopes and zero crossing points. This work makes the I_{total} close to the intended quadratic current in Figure 3-3 by proper sizing of $M_{d1\text{-}d4}$ which aids to fix the V_C to the predefined value (0.15 V). Figure 3-4(a) shows how the drawn current by the implemented dummy load resembles the desired total current while Figure 3-4(b) depicts the generated V_C versus V_{RF} for different process corners.



(a)



(b)

Figure 3-4: a) Simulated and estimated load current for setting the V_C to 0.15 V b) generated compensation voltage at different process corners.

3.1.3 Impedance Matching

A matching network is inserted between the RF source and the rectifier to deliver the maximum power to the load. The L-type matching network is mostly used in UHF RF-to-DC converters due to its simplicity and for its suitability for mass production [52]. Figure 3-5 shows the model for complete RF-to-DC conversion system [22] where the incident RF is modeled with a voltage source (V_S) and an internal resistance

(R_S). Using off-chip air core inductors the quality factor of the inductance becomes quite high (> 20) below 1 GHz, making it safe to ignore the series resistance of the inductance. L-match network is used to perform downward impedance transformation since the real part of the rectifier input impedance is several kΩs. The parallel combination of IC input capacitance (C_{IC}) and extra matching capacitor (C_{match}) should be selected to hold this equality:

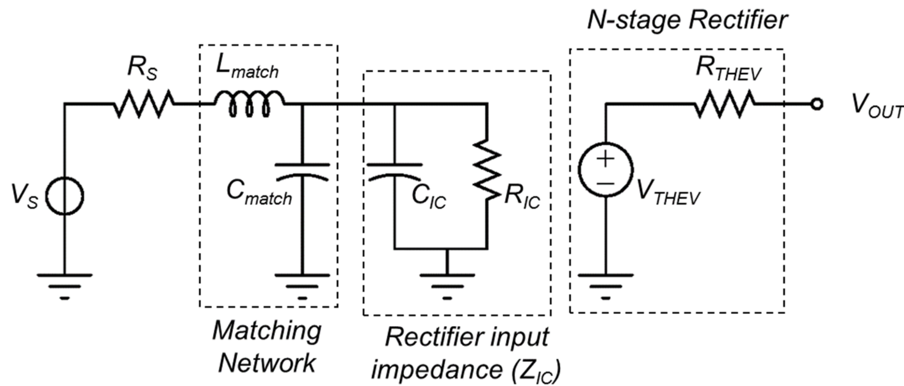


Figure 3-5: The model for RF source L-match network and UHF rectifier.

$$Re\left\{R_{IC} \,||\, \frac{1}{j\omega(C_{match}+C_{IC})}\right\} = R_S \tag{3-6}$$

Then, series inductance cancels the imaginary part of the impedance seen by the RF source:

$$Im\left\{jL_{match}\omega + R_{IC} \,||\, \frac{1}{j\omega(C_{match}+C_{IC})}\right\} = 0 \tag{3-7}$$

3.1.3.1 Multi-Stage Rectifier Design

The design procedures of the auxiliary and main rectifiers differ from each other. The key parameters for each rectifier are size and the number of stages. For auxiliary rectifiers, increasing the number of stages for offset generator rectifier improves the sensitivity but also leads to higher DC voltages at moderate and high RF powers which makes the design of the dummy load harder. Size of the dummy load transistors should be selected such that utmost similarity between the ideal load and combination of dummy load and offset-calibrator is provided. For main rectifiers, the number of

stages should be selected to provide the required output voltage. In this work, a 4-stage structure is selected, which can generate 1.2 V and 50 µA at the output with less than 0 dBm input power. Starting with minimum W/L ratio for the main rectifiers, power conversion efficiency increases with increasing size [39]. However, increasing the W/L ratio is beneficial to some extend as this also increases the parasitic components. As another point of view, the designer should also consider the effect of changing the W/L ratio of the main rectifier in variation of the input impedance of the IC. When the load current is in several micro amperes, the device size could be selected to concurrently provide good impedance matching at the input while showing good efficiency numbers. Table 3.1 summarizes the design parameters of the implemented RF rectifier.

Table 3-1: Design Parameters of the Fabricated Self-Calibrated Rectifier.

Design Parameter	**Main Rectifier**	**Auxiliary Rectifier**
W/L	15µm/0.24µm	0.24µm/10µm
Coupling capacitor	3 pF	200 fF
Type of transistors	LVT	SVT/HVT
Number of stages	4	2 per main stage

3.1.4 Experimental Results

The prototype of the implemented RF energy harvester is shown in Figure 3-6. The fabricated UHF rectifier is protected by on-chip ESD circuitry. The RF signal is generated by a 50 Ω RF signal generator. The integrated structure is connected to the PCB with 3 wire bonds which are connected to the ground, RF and output terminals. The PCB is designed with minimum dimensions to minimize losses. Due to the negligible loss of the connectors and PCB traces, the power generated by the signal generator is directly reported as the available RF power at the input of the chip. The measurements are performed in 433 MHz which is the ISM band for RFID applications in Europe and the USA. The structure is first evaluated with a network analyzer to measure the input impedance. The measured input capacitance of the structure is 4.5 pF. To match this input capacitance, a 30 nH inductor is used. Figure 3-7 shows the measured output voltage at 433 MHz while Figure 3-9 shows the power

conversion efficiency at the same frequency. By comparing the efficiency of this work with the state of the art, it can be seen that the proposed technique for calibrating the compensation voltage at different power levels successfully prevents the efficiency reduction over input power variation. Figure 3-9 and 3-10 show measurement of the system at frequency points. In Figure 3-9 a 100 kΩ resistance is connected as the load while the available RF power is -10 dBm. The frequency can be tuned between 410 MHz and 460 MHz without degrading the output voltage. The frequency response of the short circuit current of the fabricated module (Figure 3-10) is measured at two different input powers. The peak current at -17 dBm is 12 μA which is much higher than the measured result of the state of the art [33] at the same power (i.e. 1.25 μA). Transient response of the structure with different loads is presented in Table 3-2. Table 3-3 compares this work with previously reported similar works. The sensitivity of the proposed self-calibrated structure is comparable with the state of the art while its biggest advantage is that the power conversion efficiency does not reduce over the variation of the input power. Therefore, this approach is best suited for applications where the intensity of the available power is prone to change.

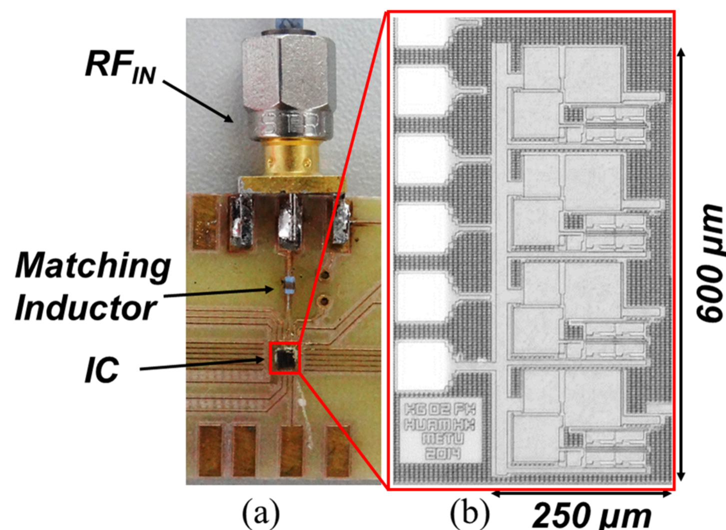


Figure 3-6: Prepared prototype for measuring the characteristics of the fabricated IC a) Test setup b) Die micrograph.

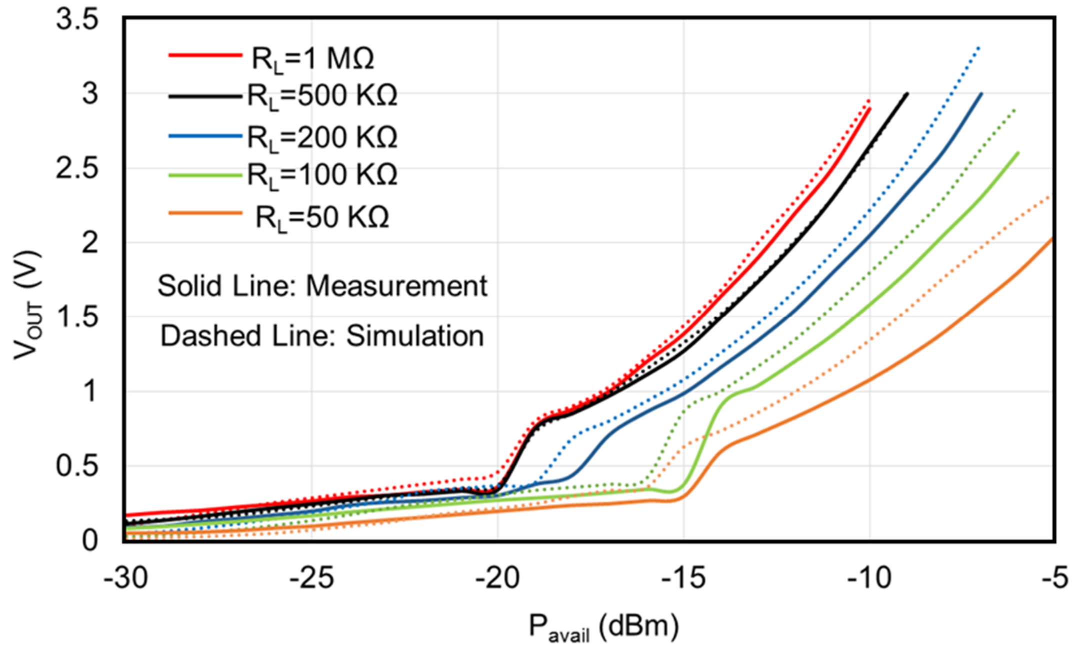


Figure 3-7: Measured output voltage versus available power at 433 MHz.

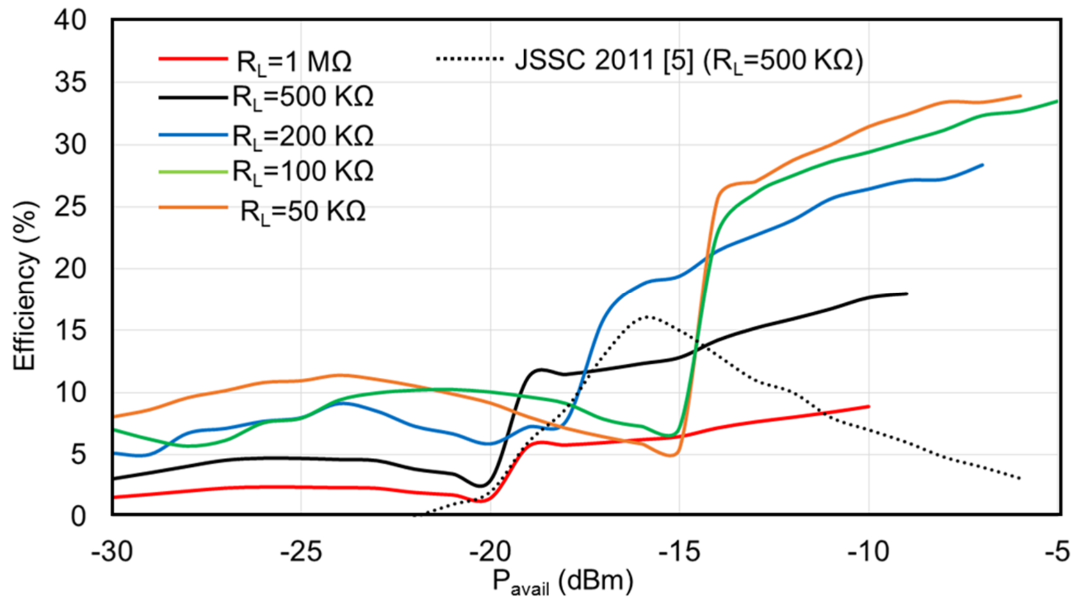


Figure 3-8: Measured power conversion efficiency at different loads and its comparison with other reported results.

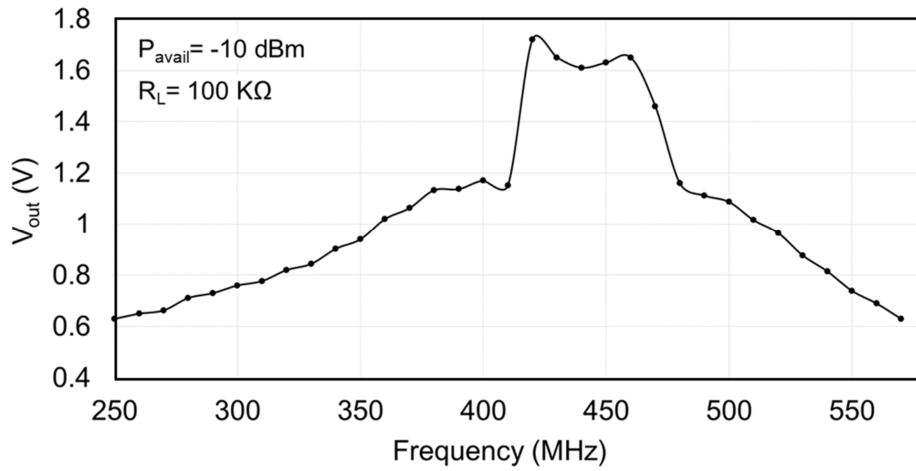


Figure 3-9: Measured frequency response of the 4-stage self-calibrated rectifier.

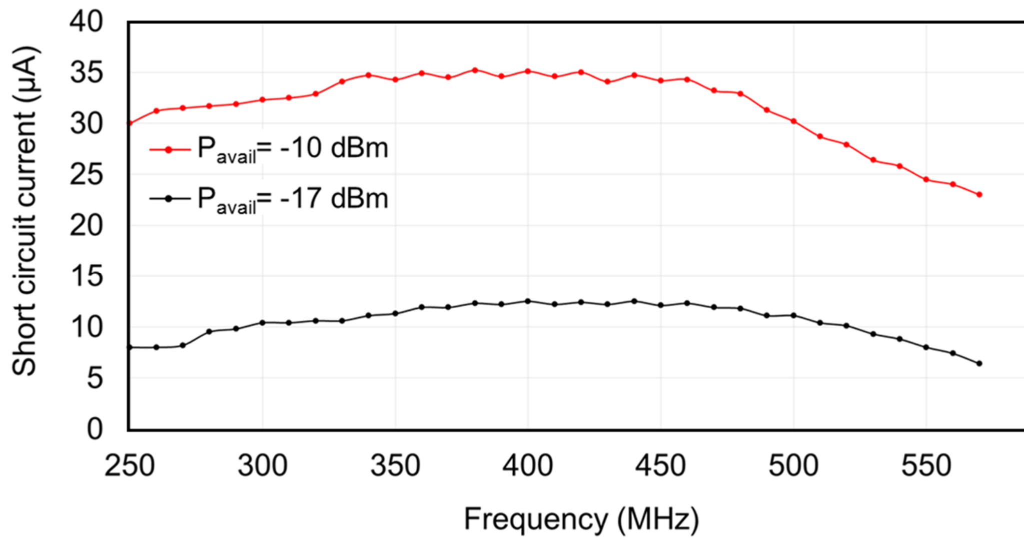


Figure 3-10: Measured short circuit current at two different RF powers.

Table 3-2: Comparison of the Measurement Results with State-of-the Art Works.

Parameter	This work	[55]	[33]	[34]	[11]
Number of stages	4	5	17	6	36
Technique	Vth self-calibratio n	Input capacitance tuning	Vth self compens ation	Dynamic gate biasing	Floating gate transistors
Requirement	Auxiliary Rectifiers & dummy load	Analog and Digital Control Circuitry	Deep n-well process	Bias distributer	Periodic charging
Efficiency variation from -20 dBm to -10 dBm @ 500 K	5%	23%	14%	-	35%
Sensitivity	-19 dBm @ 1 V, 433 MHz	-27dBm @ 1 V, 868 MHz	-24 dBm @ 1 V, 915 MHz	-14 dBm @1.5 V, 950 MHz	-22.6 dBm @ 2 V, 906 MHz
Maximum Efficiency	34% @ -7 dBm	40% @ -17 dBm	16.1% @ -15.1 Bm	11%@ -6 dBm	30%@ -8 dBm
Efficiency reduction with RF power variation	No	Yes	Yes	Yes	Yes
Process	180 nm	90 nm	90 nm	0.3 μm	0.25 μm

Table 3-3: Measured 10% Settling Time.

P_{avail}	R_L=1MΩ, C_L=47 nF	R_L=1MΩ, C_L=4.7 μF	R_L=200 kΩ, C_L=47 nF	R_L=200 kΩ, C_L=4.7 μF
-14 dBm	9.59 ms	923 ms	7 ms	796 ms
-13 dBm	8.38 ms	897 ms	6 ms	527 ms
-12 dBm	8.31 ms	839 ms	5.11 ms	513 ms
-11 dBm	8.00 ms	781 ms	4.8 ms	471 ms
-10 dBm	7.97 ms	735 ms	4.7 ms	460 ms

3.2 Switched-Gate UHF Rectifier

The second circuit topology proposed for UHF rectifiers is the "Switched-Gate" architecture which is based on adaptive threshold compensation. Adaptive threshold compensation is an alternative for constant compensation approach used in self-compensation based structures. As discussed in Section 2.2, high discharge current is

the most significant problem in threshold self-compensation approach especially when the offset between gate and source terminals (during the reverse isolation phase) exceeds the threshold voltage of the device itself. Proposed switched-gate technique is intended to address this problem by separating the forward and the reverse conduction phases and adjust the compensation voltage according to the operational phase of the pumping device. The operation mechanism of the adaptive technique during each operation phase is listed below:

- **Conduction phase:** The charge flows from the source to the load. It is desirable to ease the current conduction in this phase by having positive offset between gate and source terminals.
- **Isolation phase:** Discharging current flows from the load to source inside this phase. The offset between gate and source terminals should be zero to minimize the discharging current.

3.2.1 Concept and Circuit Implementation

Figure 3-11 shows the switched-gate UHF rectifier highlighting its operation at different phases. In Figure 3-11(a) the circuit configuration of the structure is depicted by separating each stage into two sub-blocks: *i)* Clamp circuit (M_1 and C_1 in the first stage) which upshifts the incoming RF signal *ii)* Rectifier circuit (M_2, C_2 in the first stage) which convert the upshifted RF signal by clamp circuit to the DC form. Gate connections for clamp transistors are connected to the source of the right-neighboring transistor (as done in self-compensated technique), but the gate terminals for rectifier transistors are controlled by means of two complementary switches (M_P, M_N). These switches are inserted to alter the gate connections between V_1 and V_3 according to the phase of the input RF signal. Assuming the ideal rectification by M_1 and M_2 and taking the RF signal as $V_{RF}sin(\omega t)$, the upshifted voltage (at top plate of C_1) and rectified voltage (at top plate of C_2) becomes $V_{RF}+V_{RF}sin(\omega t)$ and $2V_{RF}$ respectively. However, in practice both upshifted and rectified voltages drop from their ideal value due to leakage current and non- idealities (such as parasitic capacitances).

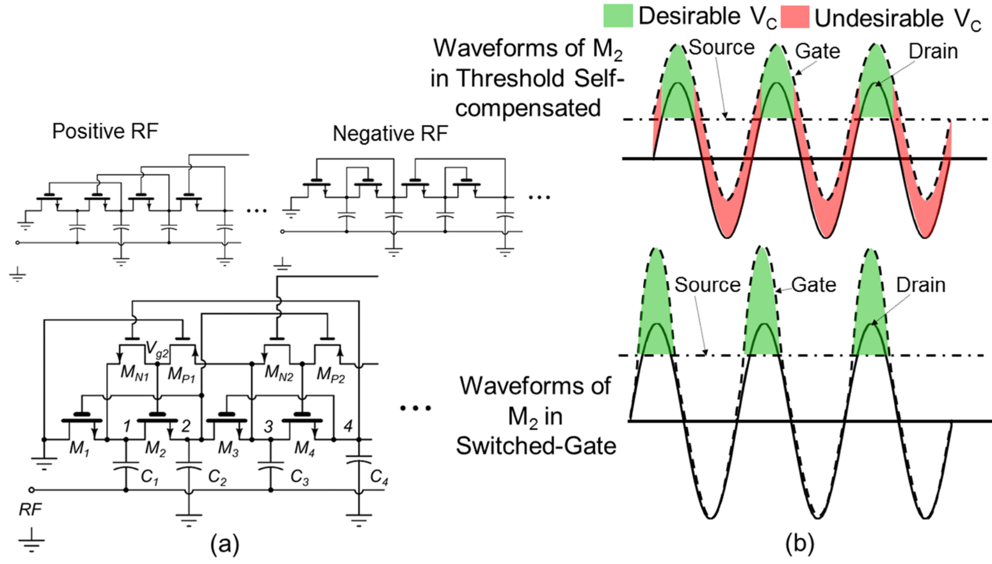


Figure 3-11: Proposed switched-gate UHF rectifier with adaptive Vth-cancelation a) Schematic b) Steady-state waveforms.

In fact, the amplitude of the RF signal at the top plate of the C_1 is less than V_{RF} due to the voltage division between C1 and augmented parasitic capacitance at its top plate (C_{par}) [22]. However, assuming that C_1/C_{par} is large enough, contribution of the parasitic capacitances becomes negligible. Also, by taking the rectified voltage by M_2 and C_2 as pure DC voltage V_{DC} (assuming that the C_2 is large enough to absorb ripples), the steady-state voltage at the top plate of C_1 becomes $\alpha V_{DC}+V_{RF}sin\omega t$. In this equality α is a constant and is equal to the ratio of the DC voltage generated by M_1 over the total V_{DC} voltage by the first stage. It should be noted that due to fundamental difference between the gate connection of M_1 and M_2, and noticing that the current passing through the transistors is equal to the load current, the augmented DC voltage by M_1 and M_2 would not be the same ($\alpha \neq 0.5$). The reason behind utilizing the adaptive threshold cancelation technique only for rectifier transistors is that proper operation of the complementary switches asks for generation of a minimum DC level by each stage for startup purpose. Otherwise, the input RF signal will have no impact on the complementary switches and the gate terminal of rectifier transistors would be floated, which is not desirable. Hence, implementing the offset voltage for clamp transistors without using extra switches assures the generation of the minimum DC voltage for internal transistor to start the switching by complementary switches. The gate-source voltage of the complementary switches (M_{N1} and M_{P1}) then becomes:

$$V_{gs(N1)} = (2-\alpha)V_{DC} - V_{RF}\sin(\omega t) \quad (3\text{-}8)$$

$$\left|V_{gs(P1)}\right| = (1+\alpha)V_{DC} + V_{RF}\sin(\omega t) \quad (3\text{-}9)$$

It can be understood from (3-1) and (3-2) that the RF term has opposite effect on M_{N1} and M_{P1}. During the positive RF phase within the forward conduction, sinusoidal term turns M_{N1} switch *OFF* and M_{P1} switch *ON*. The reverse scenario happens during the negative RF phase. Once M_{P1} is *ON* and M_{N1} is *OFF*, the gate terminal is connected to the top plate of the C_1 yielding a positive offset between the gate-to-source voltage of M_2 which helps to enhance the forward conduction current while turning M_{P1} *OFF* and M_{N1} *ON* reduces the gate-to-source offset voltage to zero leading to robust blocking of the reverse discharging current. Using the benefit of the compensation voltage just inside the conduction phase, the reader could intuitively conclude that passing similar current from M_1 and M_2, the generated voltage by M_2 should be higher than M_2. The following sub-section analyze the possible advantages of the adaptive compensation technique over the self-compensation approach.

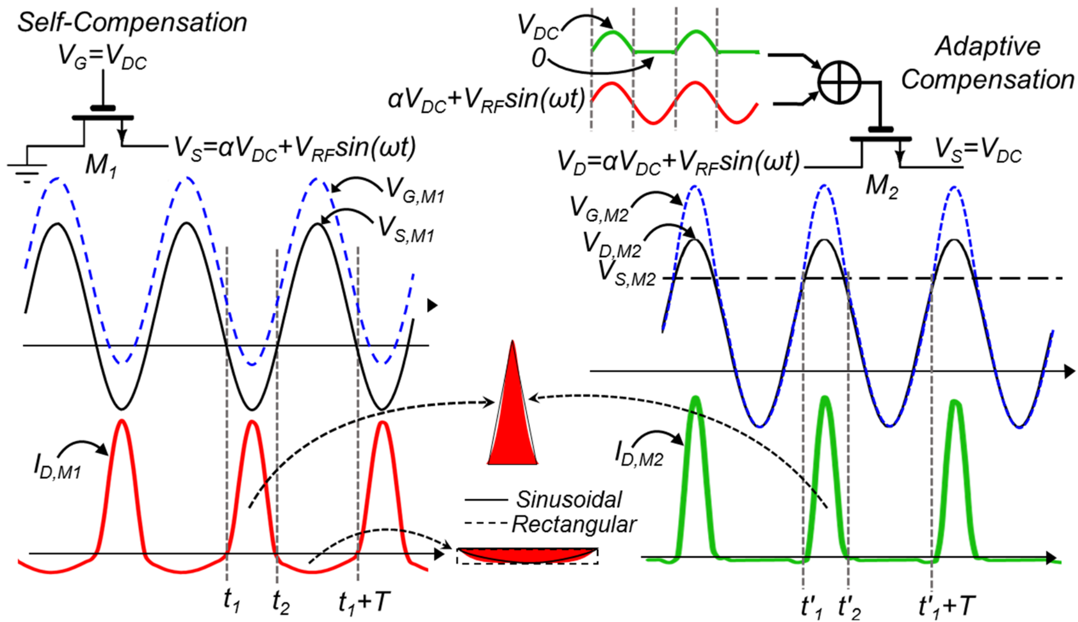


Figure 3-12: Comparison of the steady-state waveforms of the clamp and switched transistors.

3.2.2 Comparison of Constant and Adaptive Compensation

Figure 3-12 displays the steady-state waveforms of M_1 and M_2 of Figure 3-11 by supplying their terminals with ideal voltage sources. Steady-state waveforms of M_1 and M_2 in actual circuit (Figure 3-11) will be very close to the simulated waveforms with ideal batteries in the case of satisfying the following conditions: *i)* Both M_1 and M_2 completely pass their transient response and operate in steady state and *ii)* complementary switches in adaptive threshold compensation (M_P and M_N in Figure 3-11) push and pull the gate voltage of M_2 between right and left neighboring voltages. Analysis of the complementary switches will be explained in the following sub-section.

Here, the performance of M_1 (with self-compensation connections) and M_2 (with switched-gate connections) are compared by noticing the net current passing through each device. The higher net current is an indicator for robustly rectifying the incoming RF signal. Starting with M_1 the net current passing through the device is

$$I_{net(M1)} = \frac{1}{T}\left[\int_{t1}^{t2} I_{M1}dt - \int_{t2}^{t1+T} I_{M1}dt\right] \tag{3-10}$$

The terminal voltages of M1 are: $V_D=0$, $V_G=V_{DC}$, and $V_S=\alpha V_{DC}+V_{RF}\sin(\omega t)$. These voltages could be used for direct integral in (3-10) by replacing IM1 with I-V relationship of the MOS device. Direct calculation of $I_{net(M1)}$ is too complex [38] and gaining intuition about the elaborated results is difficult. To ease the calculations, the integrals could be solved by using the steady state waveforms and approximating the forward and backward charges with well-known waveforms. The instantaneous peak current at the middle of the forward and the reverse conduction phases are denoted by I_f and I_r accordingly. The current passing during the forward conduction phase ($t_1 < t < t_2$) could be well substituted by triangular approximation. Also, the current integral during the reverse conduction phase ($t_2 < t < t_1+T$) is in between the sinusoidal ($1/\pi.I_r.\Delta t_r$) and triangular ($I_r.\Delta t_r$) waveforms. Hence it is best to approximate it with $2/\pi.I_r.\Delta t_r$. Inserting the approximated charges during the forward and the reverse conduction, the net charge passing through the device at steady state becomes:

$$I_{net(M1)} = \frac{1}{2} I_f \left(\frac{\Delta t_f}{T} \right)_{M1} - \frac{2}{\pi} I_r \left(1 - \left(\frac{\Delta t_f}{T} \right)_{M1} \right) \tag{3-11}$$

where the conduction angle $(\Delta t_f/T)_{M1}$ is

$$\left(\frac{\Delta t_f}{T} \right)_{M1} = \frac{1}{2} - \frac{1}{\pi} sin^{-1} \left(\frac{\alpha V_{DC}}{V_{RF}} \right) \tag{3-12}$$

Assuming the operation of the device in strong inversion region, the current passing through the transistor becomes:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 . (1 + \lambda V_{DS}) \tag{3-13}$$

The process of computing the net charge passes through the switched transistor (M_2) is similar to the one taken for M_1. For M_2, the terminal voltages are: $V_S=\alpha V_{DC}+V_{RF}sin(\omega t)$, $V_G= \alpha V_{DC}+V_{RF}sin(\omega t)$ for $V_{RF} < 0$ and $(1+\alpha)V_{DC}+V_{RF}sin(\omega t)$ for $V_{RF} > 0$, and $V_S=V_{DC}$. Similar to M_1, the net current passing through the device is calculated by separating the forward and the backward currents and approximating them with well-known functions. Forward current has the same waveform as M_1 while the key difference is in reverse current which is negligible for M_2. Hence, the net current passes through the device would be expressed as:

$$I_{net(M2)} = \frac{1}{2} I_f \left(\frac{\Delta t_f}{T} \right)_{M2} \tag{3-14}$$

In (3-14), the integral of the forward current is approximated by triangular approximation and the discharge current is neglected. This approximation is validated by observing that the gate-to-source voltage of M_2 is zero inside the discharging phase assuring the operation of M_2 in the deep weak inversion region. The conduction angle for M_2 $(\Delta t_f/T)_{M2}$ is:

$$\left(\frac{\Delta t_f}{T} \right)_{M2} = \frac{1}{2} - \frac{1}{\pi} sin^{-1} \left(\frac{(1-\alpha)V_{DC}}{V_{RF}} \right) \tag{3-15}$$

Figure 3-13 draws the simulated and predicted (by (3-11) and (3-14))) net charge passing through M_1 and M_2 at different DC voltages. Comparing the net charge

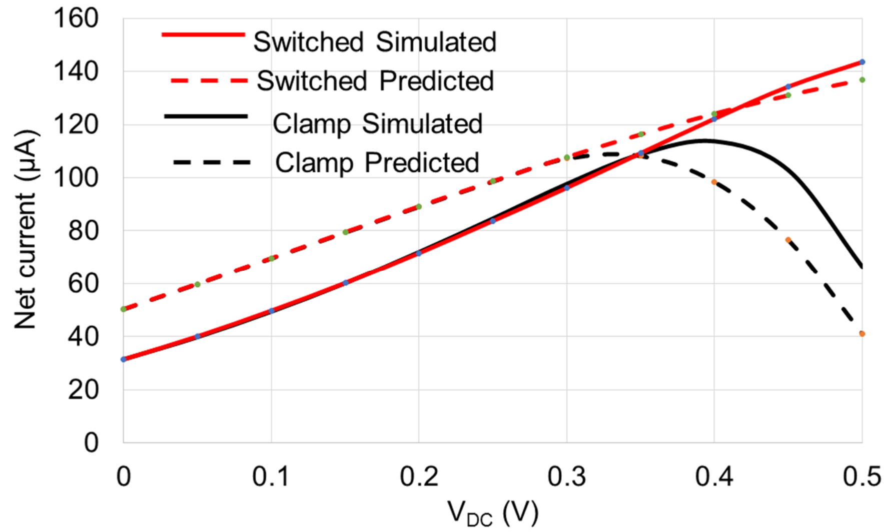


Figure 3-13: Simulated and estimated net charge of clamp and switched transistors (VRF=0.5 V).

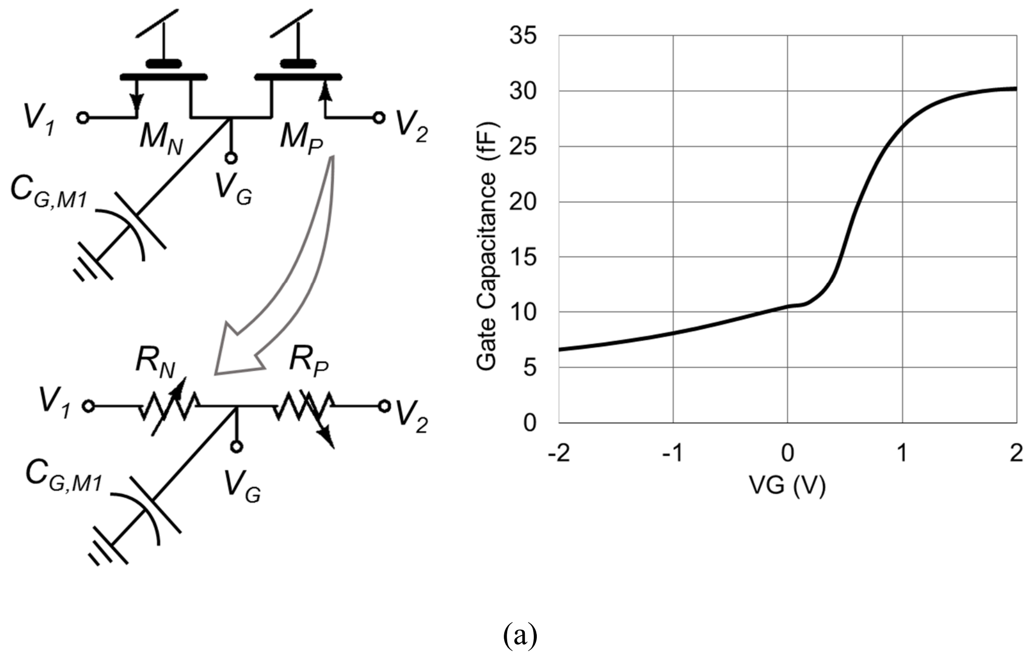
passing through the self-compensated and the adaptive compensated transistors in (3-11) and (3-14) in Figure 3-13 reveals the advantage of the adaptive cancelation technique by passing higher current when the V_{DC} is higher than the threshold voltage of the device. To have fair comparison, it is assumed that the conduction time of both M_1 and M_2 (in Figure 3-12) are the same (α=0.5). In practical realization of the switched-gate technique, the net charge of all transistors in a multi-stage UHF rectifier is the same ($I_{net(M1)} = I_{net(M2)}$) and is equal to the load current. However, lower discharge current of the switched transistor M2 in Figure 3-11 achieves better rectification of the current and reduces the required power from the RF source and consequently improves the power conversion efficiency.

As discussed above the switched-gate technique would be beneficial only if the complementary switches work well. Because, failure in completely pushing and pulling the gate terminal to the neighboring potentials causes the gate of M_2 to be floated. The floated transistor does not provide any difference between the forward and the backward charge and results in very negligible net charge. The following sub-section investigates the design considerations for complementary switches.

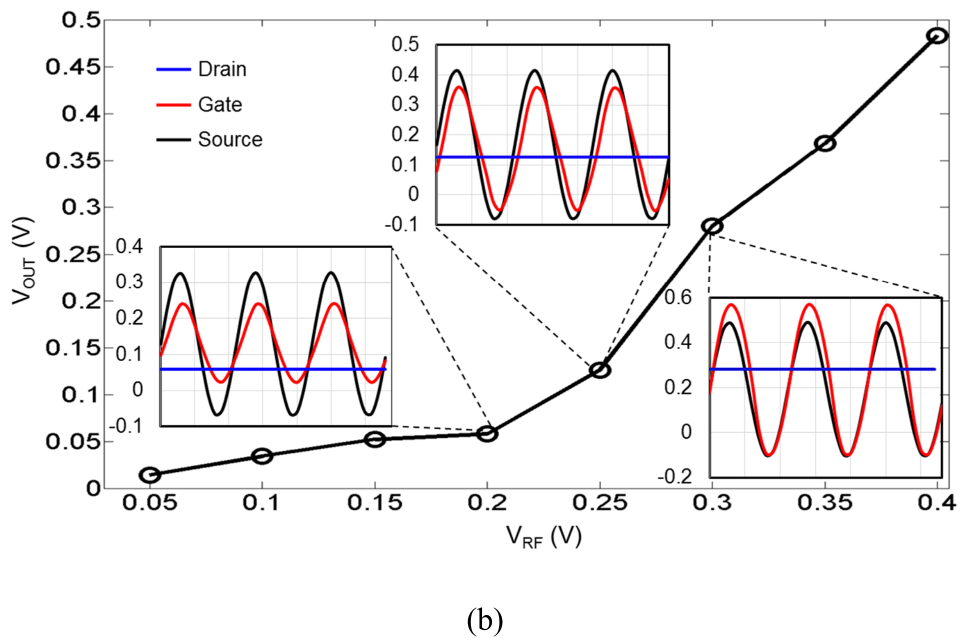
3.2.3 Complementary Switches

The complementary switches are responsible for shifting the gate voltage of M_2 in Figure 3-11 between the top plate of C_1 and C_3 according to the phase of the RF signal.

The major bottleneck in accomplishing successful switching is the loading effect of parasitic capacitance at the gate of M_2. To better understand the impact of parasitic components, Figure 3-14 redraws the complementary switches configuration (in Figure 3-11) with two oppositely varying resistors. Due to the large size of M_2 (compared to M_N and M_P), parasitic contribution of M_2 is dominant. Gate voltage equation is presented below by writing the KCL at node V_g in Figure 3-14 (a):



(a)



(b)

Figure 3-14: Replacing the transistors with resistors and simulated gate capacitance at different gate voltages.

$$V_g = V_1 \cdot \frac{1}{1 + \dfrac{R_n}{\left|\dfrac{1}{jC_{G,M2}\omega}\right| \| R_p}} + V_2 \cdot \frac{1}{1 + \dfrac{R_p}{\left|\dfrac{1}{jC_{G,M2}\omega}\right| \| R_n}} \tag{3-16}$$

where R_n and R_p are the channel resistance of M_N and M_P respectively, and C_{GM2} is the accumulated parasitic capacitance at the gate of M_2. Considering the ideal case, for which $C_{G,M2}$ is very small, the gate voltage is approximately equal to V_1 when $R_{nch} >> R_{pch}$ and to V_2 when $R_{pch} >> R_{nch}$. However, $C_{G,M2}$ tends to break the differential nature of the complementary switches and settle the gate voltage at the middle point which is not desirable. Simulated gate capacitance over the variation of the gate voltage (using LVT transistors in IBM *0.18-μm* PD-SOI CMOS process) is also depicted in Figure 3-14(a). Deviation of the capacitor characteristic from the valley-shape graph presented in classical handbooks is due to the fact that at applying high frequency to SOI transistors, neither minority nor majority carriers follow the variation of the applied potential [56]. Given that the gate capacitance scales with device size (∝W.L) [57], M_2 should have minimum dimensions in order to minimize the parasitic effects for complementary switches.

Solving the power-speed trade-off is the most critical task during the sizing of complementary switches. Choosing high aspect ratio for the switches assures their sufficient speed while causes high power consumption penalty which would counteract the advantages obtained by the switched-gate technique. On the other hand, lowering the device size (aspect ratio) may result in M_N and M_P not being able to push and pull V_G between V_1 and V_2 at the given frequency.

In digital applications, the speed of MOS switch is gauged by the intrinsic process characteristic time constant [41] which is defined as $\tau_n = R_n.C_{ox}$. It is the decaying time constant of MOS transistor when the drain is charged to V_{DC} and the input changes from to 0 to V_{DD}. Even though the application here does not have a supply voltage and could not be considered as a digital circuit, the speed concept (defined by τ_n) is helpful in order to gain intuition about the important design parameters. Replacing R_n with device parameters in τ_n results in:

$$\tau_n = R_n.C_{ox} = \frac{2C_{ox}.V_{DD}.L^2}{k_n.(V_{DD} - V_{th})^2} \quad (3\text{-}16)$$

From (3-16), it can be seen that the gate-to-source voltage of the device (which is V_{DD} in (3-16)) should be much higher than V_{th}. Otherwise, the denominator becomes close to zero causing very low switching speed. Also, the switching speed inversely increases by the square of the channel length suggesting that the length of the MOS switch should be kept at a minimum value. Finally, noticing that the peak gate-source voltage for both M_N and M_P is the same, the transconductance of NMOS and PMOS transistors should be equal to each other in order to maintain identical switching speed (and have symmetric gate waveform for M_2). In this work, the W/L ratio of M_P is selected twice the one of M_N to provide equal weight for switches.

As a conclusion, two criteria should be fulfilled together to achieve the proper operation of complementary switches. First and foremost, sufficient gate-source voltage should exist for both M_N and M_P. Second, the size of the complementary switches should be as small as possible to minimize the switching loss while their aspect ratio should be high enough to completely alter V_G between V_1 and V_2 even with the loading effects of parasitic $C_{G,M1}$ capacitance.

Figure 3-14(b) shows the simulated DC voltage of the single stage switched-gate structure while drawing the steady-state waveforms of the M_2. The output voltage changes by the increasing the RF amplitude, and it can be seen that when the RF amplitude is 0.2 V, the gate voltage cannot swing as well as the source terminal and the gate voltage operate like floating gate. When the RF amplitude is 0.25 V, the swing of the gate terminal is equal to the one of the source terminal and the structure behaves like the Dickson topology wherein the source terminal is connected to the gate terminal. Finally, when the RF amplitude is 0.3 V, the gate terminals swing higher than the drain terminal and the desired offset between the gate and source terminals exist during the forward conduction while it is removed by the connection of the gate terminal to V_1 during the negative phase of the RF swing. Our simulations show that in order to guarantee the proper operation of the switches, the amplitude of the incoming RF voltage should be at least equal to the threshold voltage of the complementary switches.

3.2.4 First Design in Bulk-CMOS

The first design was implemented in the UMC *0.18-µm* CMOS process, to evaluate the robustness of the proposed switched-gate technique in comparison with constant compensation based architectures. Figure 3-15 shows the die micrograph of the fabricated rectifiers. It includes 7-stage Switched-gate, threshold self-compensated and, the Dickson rectifiers together on the same die. Sizes of all transistors are the same. For switched gate structure,

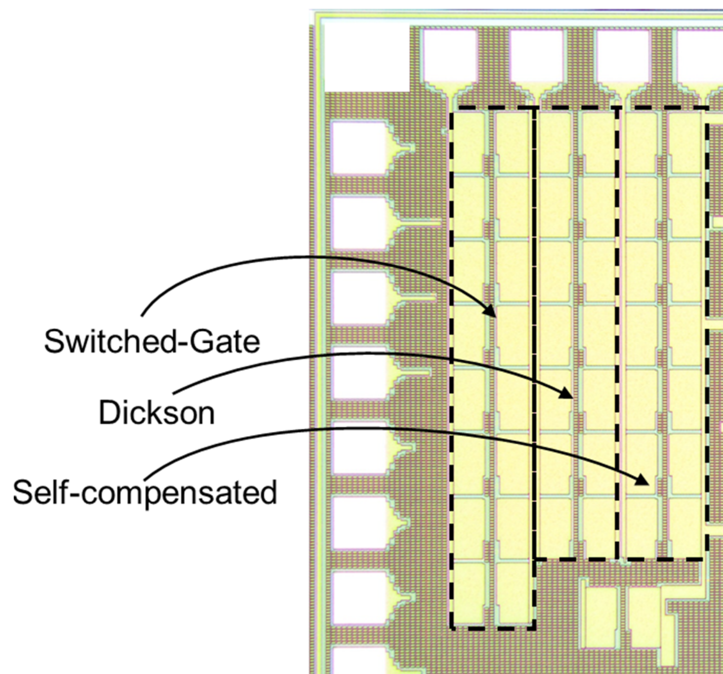


Figure 3-15: Die micrograph of the fabricated rectifiers in UMC *0.18-µm* CMOS process (N=7, W/L=8µm / 0.25µm).

the W/L ratio of the NMOS switch and PMOS switch are set to1µm/0.25 µm and 2µm/0.25µm respectively. Figure 3-16 compares the measured power conversion efficiency at different RF amplitudes and frequencies. The results at 100 MHz reveals that the switched-gate technique could increase the peak PCE at low RF amplitudes compared to the threshold compensation and the Dickson architectures. However, as the frequency increases to 500 MHz, two undesirable phenomena happen: First, the peak power conversion efficiency of the switched-gate rectifier decreases. And second, the minimum required RF amplitude that the structure starts to work increases. Both of these problematic effects arises from poor performance of the complementary switches at high frequencies. For each cycle of the RF signal, the gate

terminal of the switched transistor should completely shift from the lower potential to the higher potential and come back afterwards. The speed constraint on the PMOS switch is more severe since the conduction time frame is the short portion of the hole cycle and the PMOS switch should be very fast to instantly push and pull the gate potential. As discussed above, assuming that the sufficient RF voltage exists, the parasitic components impose the most severe restriction on the switches.

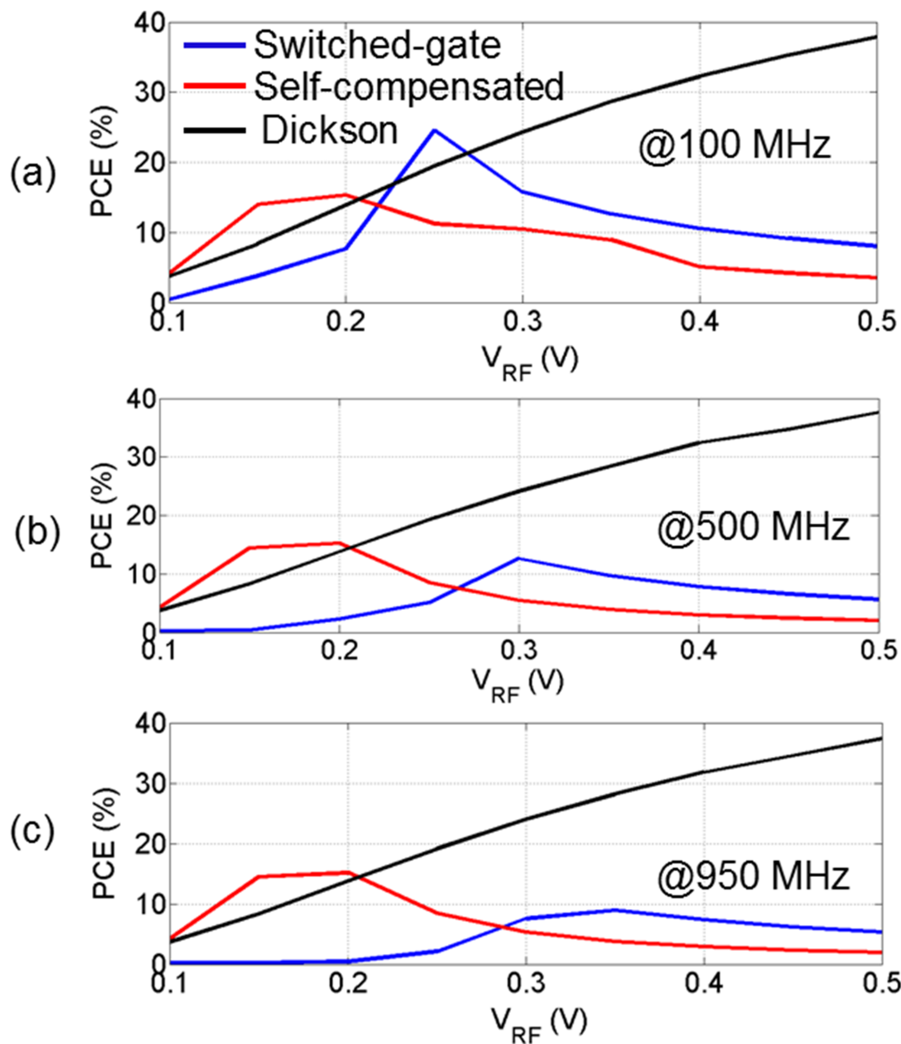


Figure 3-16: Performance comparison of switched-gate, self-compensated and Dickson architectures at different frequencies a) f=100 MHz. b) f=500 MHz. c) f=950 MHz.

3.2.5 Second Design in SOI-CMOS

To improve the frequency performance of the structure, a second prototype is designed and fabricated on an SOI process. A 4-stage switched-gate structure is

designed and implemented in IBM *0.18-μm* CMOS process. Figure 3-17 illustrates the designed 4-stage UHF rectifier and its die micrograph of the fabricated silicon.

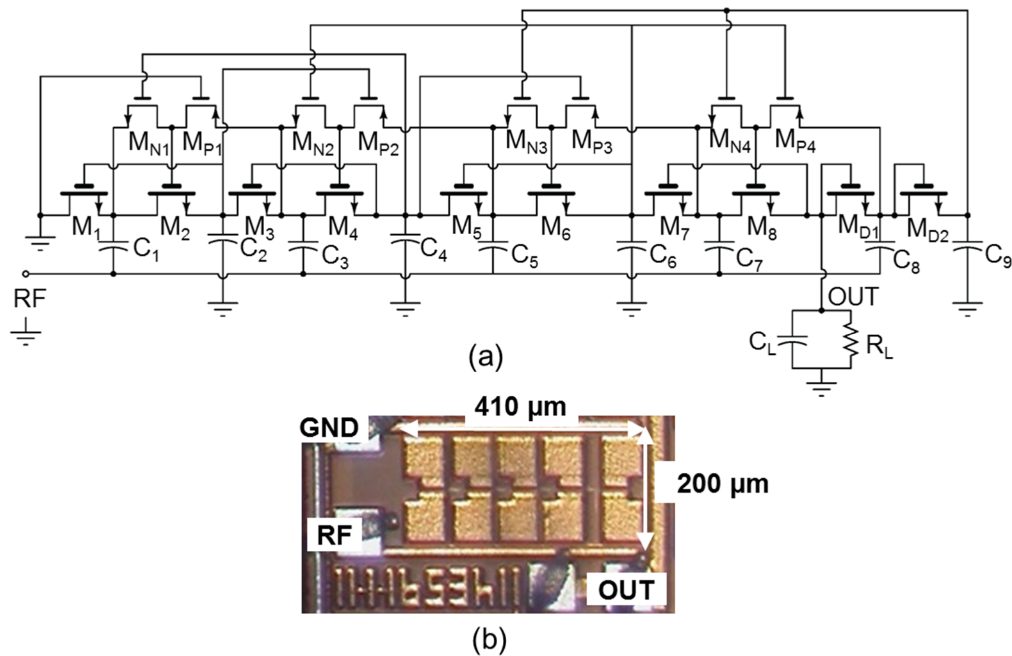


Figure 3-17: 4-Stage switched-gate UHF rectifier designed for *0.18-μm* SOI process a) Circuit diagram. b) Die micrograph.

The primary objective of the designed structure in SOI process was to increase the operating frequency up to 950 MHz. Figure 3-21 shows the simulated and measured results at interested frequency. The abrupt increase in the power conversion efficiency demonstrates that the required voltage for proper operation of the complementary switches is provided for the given voltage. The minimum required voltage increases by connecting heavier loads (with decreasing R_L). That is because decreasing R_L leads to a drop in the generated DC voltage per stage. As can be understood from (3-9), the gate-source voltage of the PMOS switch (M_{P1},M_{P2},…) at the conduction angle is directly proportional to the DC voltage generated by the rectifier. Hence, when R_L decreases, the PMOS switch could not connect the gate of rectifying transistor (M_2, M_4, …) to the source of the right-neighbor transistor. Hence, the RF amplitude should be increased to compensate the lower V_{DC} due to the heavier load.

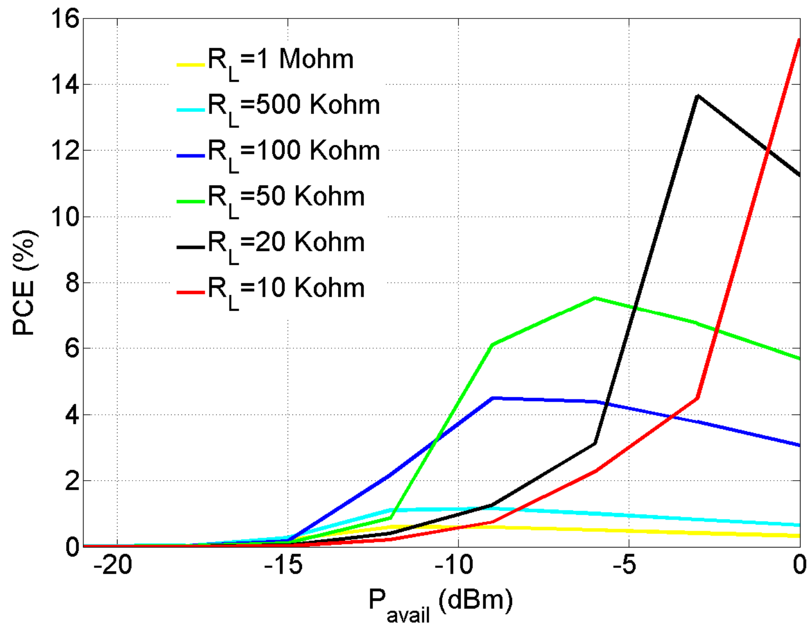


Figure 3-18: Measured power conversion efficiency of 4-stage switched-gate UHF rectifier fabricated at 950 MHz.

Even though realizing the switched-gate technique in the given PD-SOI process helps to increase the input frequency up to 950 MHz, the efficiency numbers could not surpass the state of the art works (like 20% PCE at -12 dBm reported in [37]) due to the following difficulties:

- **No low threshold transistor exists for PMOS transistors:** Figure 3-19 displays the simulated threshold voltage of the "pfet" transistor which owns the lowest threshold voltage among all P-type devices in the process. Even with employing pfet transistors as the switches, their threshold voltage is 0.33 V, which is quite large to handle the power amplitudes below -10 dBm. Also, as mentioned previously, the slow switching speed of the PMOS transistor is more dominant than the NMOS counterpart in switched-gate configuration due to the limited forward conduction time frame in a single cycle.

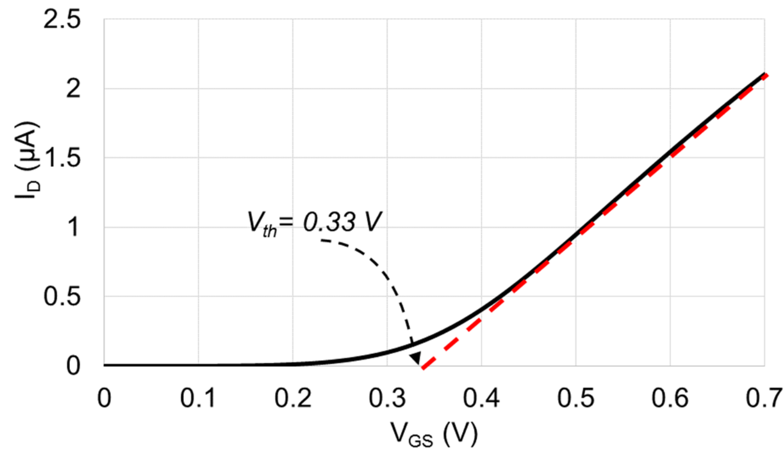


Figure 3-19: Simulated I-V characteristic of P-type transistor with lowest threshold voltage in PD-SOI process.

- **History effect in NMOS switches**: In the given process, the low-leakage transistors "nfet_ll" has the lowest threshold voltage among the N-type MOSFETs. However, these types do not have body contacts and considerable history effect is expected during their real time operation. History effects leads to variation in threshold voltage of the SOI device when it is used as a switch [58]. The variation in the threshold voltage depends on the history of the switching activity of the device. Figure 3-20 shows the cross section of the NMOS transistor fabricated in the PD-SOI process while highlighting the dominant mechanisms which contribute to variation of the threshold voltage: Impact ionization due to high energy carriers (ii in Figure 3-20) and, leakage body current due to drain/source-to-body junction (D_{sb} and D_{db} in Figure 3-20).

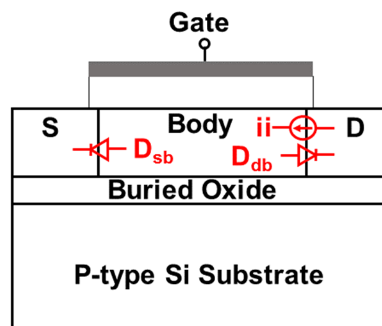


Figure 3-20: Cross section of PD-SOI transistor with highlighting the history effect due to variation in the body potential [58].

The simulated drain current of the NMOS transistor without body-contact is shown in Figure 3-21. The simulation setup is also depicted in this figure. The drain and gate terminals have DC voltages while the sinusoidal signal is applied to the source terminal. If the device has time invariant behavior, it is expected to observe steady-state current waveform since the applied voltages are in steady state. However, due to the dependence of the body potential to the history of the switching, the threshold voltage changes over time and the device shows a transient response.

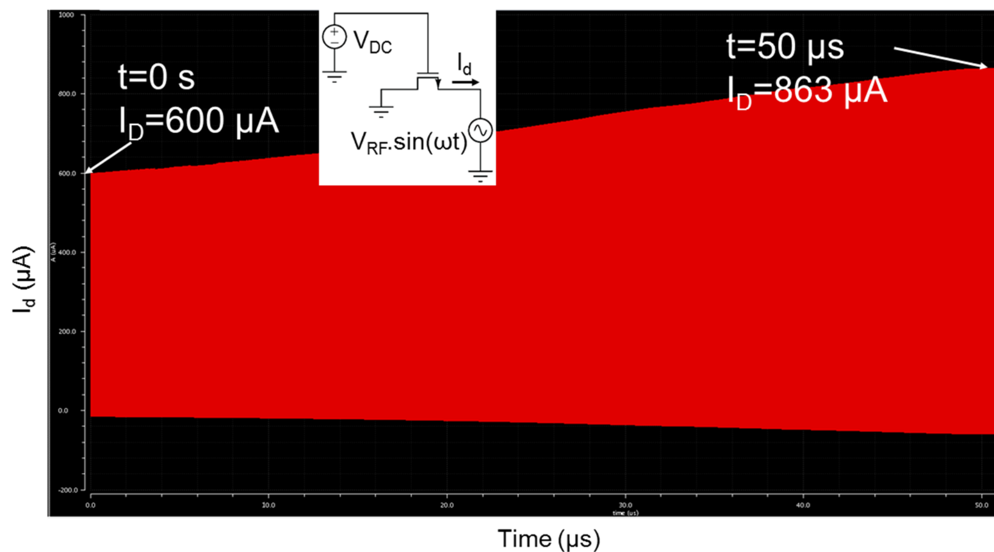


Figure 3-21: Simulated transient response of body-contact-less NMOS transistor.

Presented circuit architectures in this chapter aim to improve the performance of self-compensated rectifier with different approaches. The simplicity of the self-calibrated rectifier is its biggest advantage since the extra circuitries include only simple rectifier. It successfully addresses the efficiency drop due to large discharging current by controlling the compensation voltage.

Superior performance of the switched-gate architecture is also demonstrated by both simulation and measurement but the demand for fast switching of complementary switches put some difficulties in the practical realization. In the bulk-CMOS realization of the switched-gate technique, loading of parasitic components at high frequencies is the major problem limiting the operating frequency at 100 MHz. When

the circuit is designed and implemented in SOI-CMOS process, lack of low-threshold transistors increases the minimum operable RF voltage and consequently increases the minimum RF power to -6 dBm. In order to really appreciate the benefits of the switched-gate technique, a low-power FD-SOI process merging both requirements (low parasitic capacitors and low threshold) should be used to concurrently meet the frequency (900 MHz) and minimum power (-12 dBm) requirements.

Aside from the rectifier part, an RF-to-DC conversion system includes the RF source (typically antenna), matching network and storage element. Design of the antenna is out of the scope of this VLSI research, however, antenna-rectifier interface design is investigated in detail in the following chapter. It is intended to introduce the popular interface design approaches and compare the advantages and disadvantages of each approach.

CHAPTER 4

4 ANALYSIS OF THE MATCHED AND MISMATCHED ANTENNA-RECTIFIER INTERFACE NETWORKS

This chapter investigates two common methods for the antenna-rectifier interface design: i) matched network and *ii)* mismatched networks. The motivation behind this part of the research is to determine advantages and disadvantages of each method and provide insight for the reader during the design of the interface network between the RF source and the rectifier. In literature, authors only mention the matching network without providing extra information about the reasons behind the chosen approach. The importance of selecting appropriate approach for the matching network arises from the non-linear nature of the rectifier input impedance. In the steady state, input impedance of the rectifier could be represented by shunt $R||C$ network. Both real and imaginary parts of the IC input impedance depends on the amplitude of the incoming RF signal. Also, the IC input impedance depends on the current drawn at the load side causing broad variations for both the real (from hundreds on Ωs to several kΩs) and the imaginary (from hundreds of fF to several pFs) parts.

The interface networks are studied from two different standpoints: first the amount of passive boosting obtained by the interface circuit and second the practical limitations imposed by the interface network. The first criterion is important because UHF rectifiers tends to have large RF signals at their input. As the amplitude of the incoming RF signal decreases, MOS transistors fail to conduct the current from the

load to the source and most of the incoming RF power dissipates by charging and discharging parasitic capacitances. On the other hand, comparison of the physical values of reactive components is worthwhile to evaluate the feasibility of the solution and also bandwidth restrictions imposed by the matching network.

4.1 Impedance Matching Network

As discussed at the beginning of this section, the aim of any matching network is to deliver the maximum power from the source side (antenna) to the load side (rectifier). Hence, the impedance matching is an important part during the co-design of the antenna and rectifier.

4.1.1 Conjugate Matching

Typically, in RF engineering the designers would like to offer the conjugate impedance of the source impedance to deliver the maximum power to the load. This approach is known as the conjugate matching and guarantees the maximum power delivery to the load.

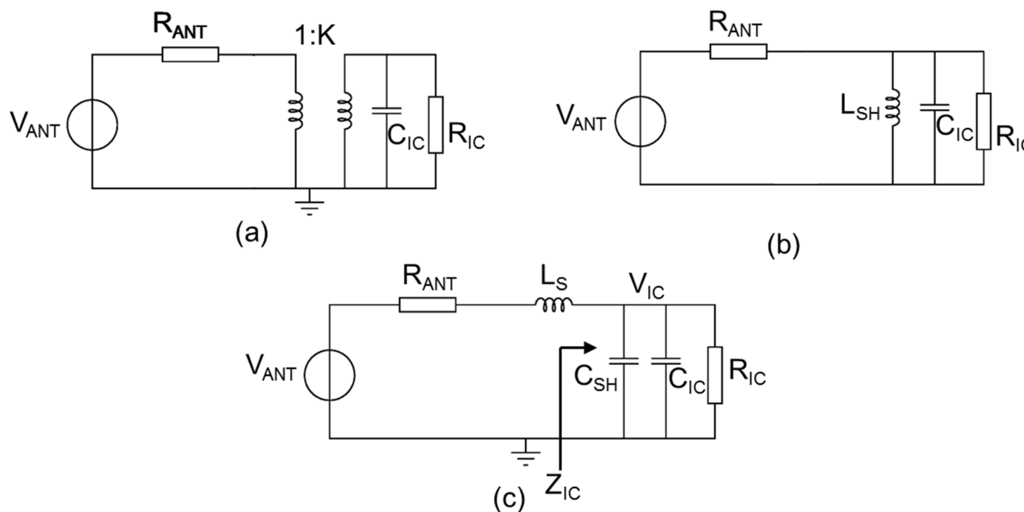


Figure 4-1: Different strategies for conjugate matching a) by transformer b) by shunt inductance c) by series inductance [22].

Figure 4-1 shows the common methods used in RF-to-DC converter structures to match the impedance of the antenna and the rectifier. They include matching with a transformer (Figure 4-1(a)) and, shunt (Figure 4-1(b)) and series (Figure 4-1(c)) inductance matching networks. Implementing transformers requires large silicon area

and is not cost-effective in mass production. Selecting between shunt and series inductance depends on the designed input resistance of the UHF rectifier (R_{IC}). Using shunt inductance for matching, two condition should be fulfilled to have matched load: a) the resistive part of the IC input impedance (R_{IC}) is equal to radiation resistance of the antenna (R_{ant}) b) the shunt inductance and capacitive part of the IC cancel their impedance at resonance frequency. On the other hand, using series inductance would be useful when the input impedance of the IC is larger than the antenna impedance. The recent case is more common in RF energy harvesting applications since the antenna impedance is limited to several hundred ohms but R_{IC} typically ranges from 1 kΩ to 10 kΩ given that the load current is less than 100 µA (which is the case for most of the practical applications). Impedance matching using series inductance could be better understood by writing the complex input impedance of the IC:

$$Z_{IC} = \frac{R_{IC}}{1 + jR_{IC}C_{IC}\omega} = \frac{R_{IC}}{1 + \left(R_{IC}\left(C_{IC} + C_{SH}\right)\omega\right)^2} - j\frac{R_{IC}{}^2\left(C_{IC} + C_{SH}\right)\omega}{1 + \left(R_{IC}\left(C_{IC} + C_{SH}\right)\omega\right)^2} \quad (4.1)$$

The shunt capacitance C_{SH} should be selected such that the real part of the Z_{IC} be equal to R_{ANT}. Then, the L_{SH} is responsible to cancel the imaginary part of the IC input impedance at the operating frequency and to equate the load seen by the antenna to R_{ANT}. At the end, the voltage gain obtained by conjugate matching could be found by noticing that using reactive components in the interface network all generated power by the source will be delivered to the rectifier. Then the voltage gain becomes equal to:

$$G = \frac{1}{2}\sqrt{\frac{R_{IC}}{R_{ANT}}} \quad (4.2)$$

4.1.2 Passive Voltage Boosting

The circuit diagram of the voltage boosting matching network (shown in Figure 4-2) is similar to conjugate matching except that no shunt inductance is added in parallel with the IC input impedance. Aside from the absence of the shunt capacitor in voltage boosting network, the more important difference with the conjugate matching counterpart is in the design procedure. The passive voltage amplification from the

antenna feed to the input of the UHF rectifier using voltage boosting network requires the ratio of R_{IC}/R_{ANT} to be very high [9]. The voltage gain from the antenna to the rectifier input is:

$$G = \left|\frac{V_{IC}}{V_{ANT}}\right| = \frac{R_{IC}}{\sqrt{\left(R_S + R_L(1-\omega^2 L_{SQ}C_{IC}\right)^2 + \omega^2\left(L_S + R_L R_S C_L\right)^2}} \quad (4.3)$$

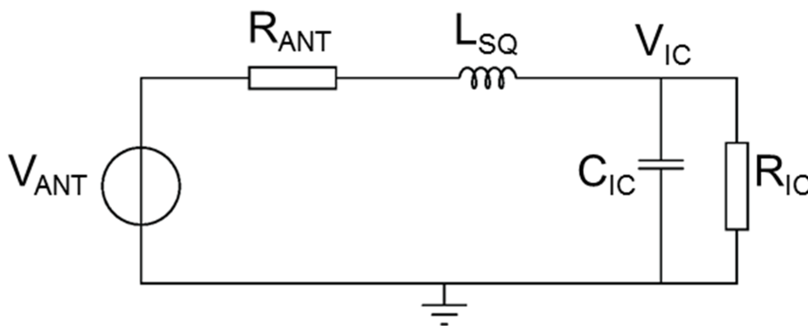


Figure 4-2: Passive voltage amplification using series inductance.

The value of the series inductance should set to have the peak voltage gain at the desired frequency (ω_o):

$$\left.\frac{\partial G}{\partial \omega}\right|_{\omega_o} = 0 \quad (4.4)$$

Hence, the L_{SQ} should be set to satisfy the following equation:

$$\omega^2 = \frac{1}{L_{SQ}C_{IC}} . \left[1 + \frac{R_{ANT}}{R_{IC}} - \frac{\left(L_{SQ} + R_{IC}R_{ANT}C_{IC}\right)^2}{2}\right] \quad (4.5)$$

4.1.3 Comparison of Matched and Mismatched Networks

The voltage gain of V_{IC}/V_{ANT} is the primary merit during the selection between the conjugate matching and the voltage boosting approaches. The comparison should be done under the same condition including equal C_{IC}, R_{IC}, R_{ANT}, and V_S while L_S and L_{SQ} are selected based on the design procedure explained for conjugate matching and voltage boosting accordingly. Figure 4-3 compares the simulated voltage gain for conjugate matching and voltage boosting approaches. By comparing the elaborated

voltage gain for each approach, it could be seen that the voltage gain of the conjugate matching is always higher than the voltage boosting network. It can be accepted intuitively by

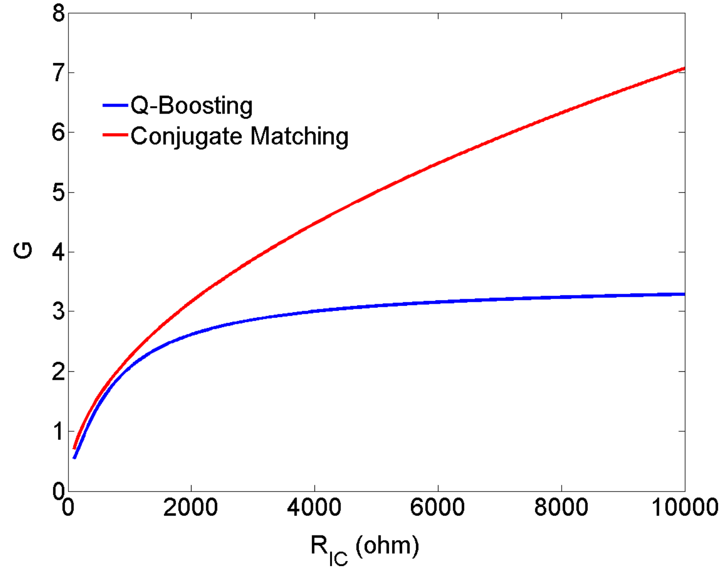


Figure 4-3: Comparison of the voltage gain from the antenna to the rectifier in voltage boosting and conjugate matching networks (C_{IC}=1 pF, f=900 MHz).

writing the steady-state dissipated power of a shunt RC network as below:

$$V_{IC} = \sqrt{2P_{IC}R_{IC}} \tag{4.6}$$

Connecting equal R_{IC}, for both topologies, the amount of V_{IC} will depend on the amount of P_{IC} delivered to the IC and recalling from circuit theory, providing conjugate matching assures the delivery of the maximum power to the load (rectifier in our case).

Although the conjugate matching provides higher voltage gain compared to the voltage boosting under equal R_{IC}, the practical restrictions of the conjugate matching should also be considered while selecting between the two. In conjugate matching, it is assumed that the amount of the C_{IC} should be selected accordingly to pull-down the real part of the Z_{IC} equal to R_{ANT}. As R_{IC} gets higher, the amount of the required C_{IC} gets lower. Figure 4-4 draws the required $C_{IC}//C_{SH}$ to pull the real part of the Z_{IC} to 73 Ω (which is the typical radiation resistance for a dipole antenna) over different R_{IC} values. For example, assuming that no C_{SH} exists, when R_{IC}=10 kΩ and f=900 MHz,

the required C_{IC} is about 0.2 pF which is very low. Recalling the approximation of the C_{IC} as discussed in chapter 2, it should be noted that C_{IC} comes from RF pad, ESD protection circuitry, parasitic bottom plate of the coupling capacitors, and finally parasitic capacitance of the pumping diodes. In bulk-CMOS process, and having the stage numbers more than three, the C_{IC} is more than 1 pF. When the C_{IC} is higher than the intended value (to pull the real part downward enough), the C_{SH} in Figure 4-1 should be replaced with shunt inductance L_{SH}. The cost should be paid is the lower bandwidth for the matching network.

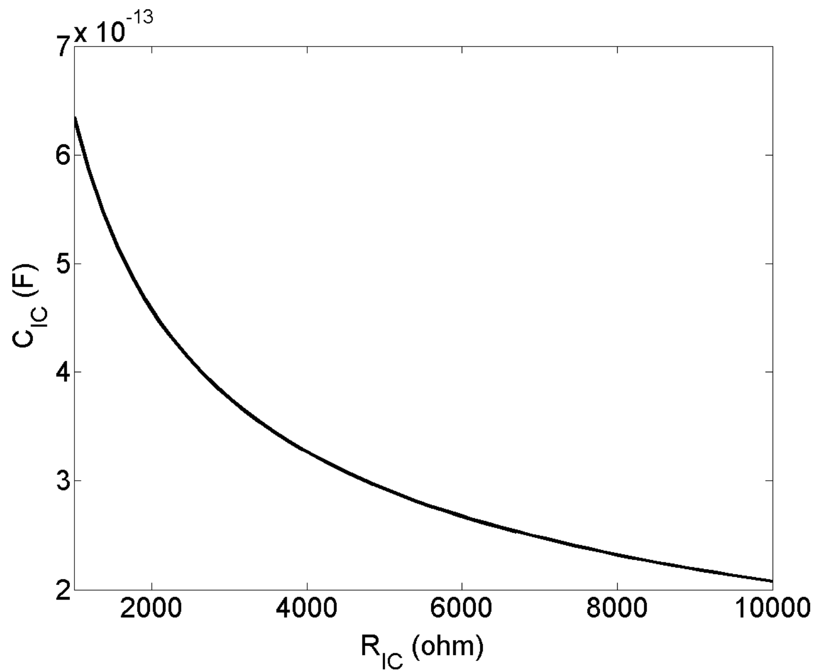


Figure 4-4: Required C_{IC} to make the real part of the Z_{IC} equal to 73Ω at 900 MHz.

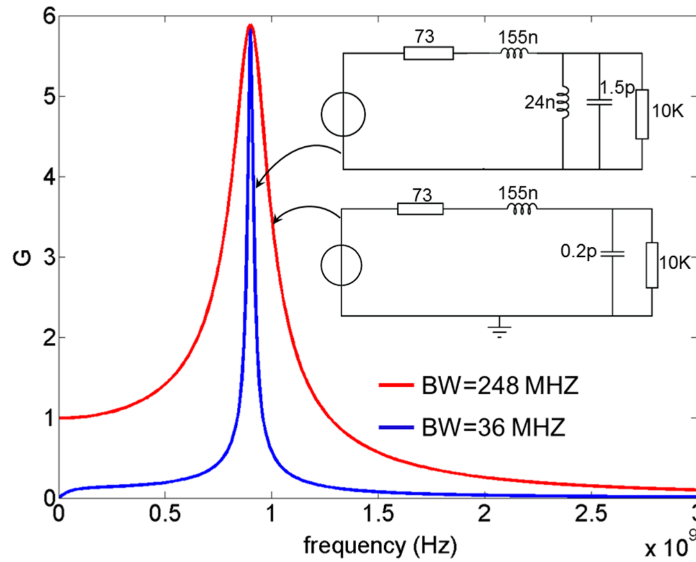


Figure 4-5: Comparison of the bandwidth of conjugate matching network when C_{IC} is higher and equal to the desired value.

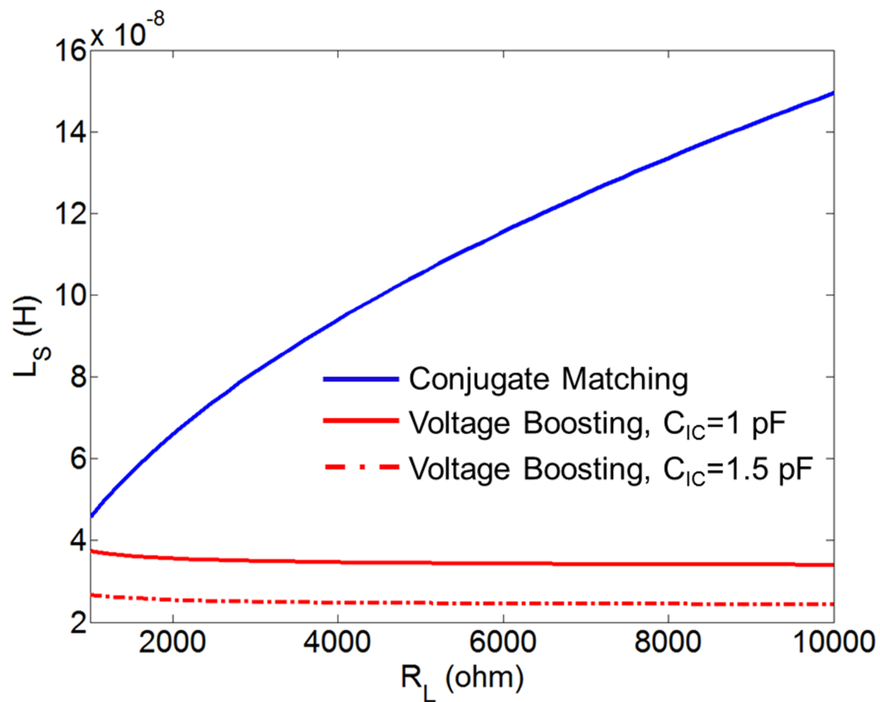


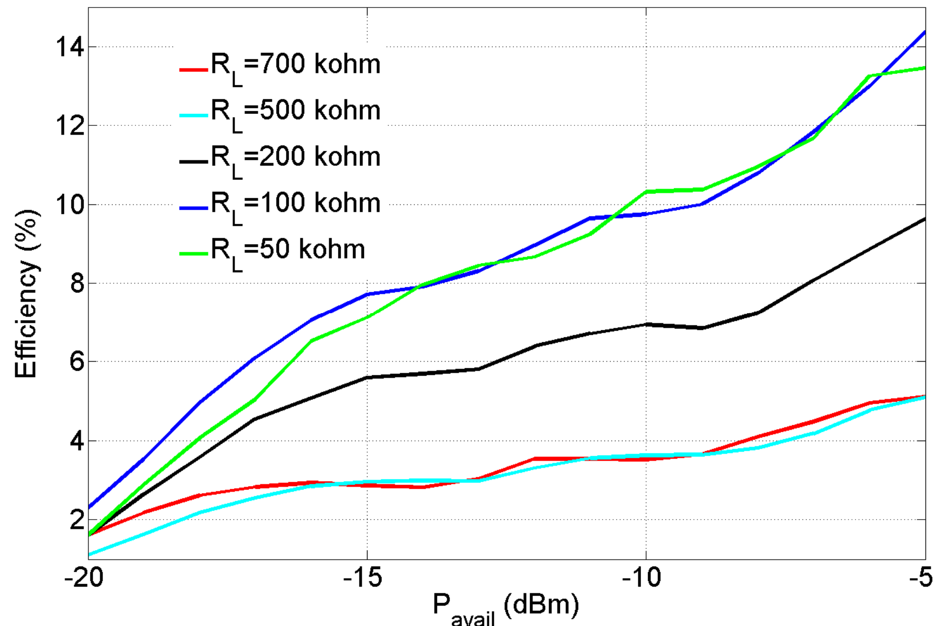
Figure 4-6: Comparison of the series inductance required in conjugate matching and voltage boosting method with two different C_{IC} value (R_{ANT}=73 Ω, f=900 MHz).

The second drawback of the conjugate matching is that the inductance required to accomplish the matching is higher than the voltage boosting method. Figure 4-6

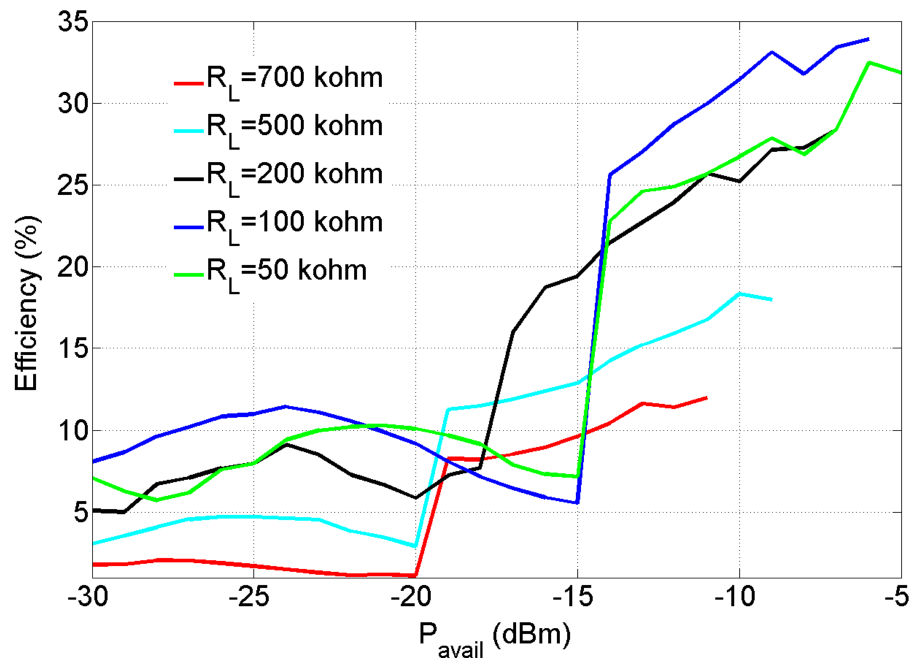
compares the required series inductance by the voltage boosting and the conjugate matching networks. The key conclusions worth to drawn from Figure 4-6 are: *i)* the required inductance by the conjugate matching network increases as the R_{IC}/R_{ANT} ratio increases *ii)* The required series inductance value by conjugate matching network is definitely higher than the voltage boosting and the gap between the two increases as R_{IC} increases *iii)* the required inductance by the voltage boosting method shows little variation over the growth of the R_{IC} proving its robustness against the deliberate variations of the load current (due to shifting in operation mode of the sensor) or undeliberate changes due to process and temperature variations.

As a general conclusion, when R_{IC} is close to R_{ANT}, it would be better to use the conjugate matching. But, as the R_{IC}/R_{ANT} ratio increases, more severe restrictions should be imposed on both the minimum input shunt capacitance and the series inductance to complete the matching. In this case, it would be better to consider the voltage boosting network to provide a passive gain form the antenna to the rectifier without imposing undesirable condition on the value of the reactive components.

In summary, the discussions presented here, reveals the importance of the rectifier complex input impedance during the interface design between RF source and the rectifier. The challenge arises from the fact that both the real and the imaginary parts of the rectifier have a non-linear dependence over the variation of the input RF voltage and the load current. Also, it is demonstrated that comparative values of the real and the imaginary parts of the rectifier input impedance has great impact on the interface design procedure. The consideration of the required voltage gain, bandwidth, and the size of the reactive components are the trade-offs in the interface design procedure. In comparison to the Q-boosting method, conjugate matching offers higher voltage gain but narrows the bandwidth and also ask for larger reactive components. The results of this section is used in the design of the matching network for the self-calibrated rectifier. A series inductance (70 nH) matching network is used a Q-boosting matching to have 50 MHz bandwidth and provide a voltage gain of 3 (from RF source to rectifier input impedance). Figure 4-7 compares the overall efficiency of the RF harvesting system with and without the series matching inductance for self-calibrated RF harvester. It can be seen that adding series inductance based on the analytical procedure presented in this chapter significantly improve the PCE for different loads.



(a)



(b)

Figure 4-7: Comparison of the measured overall power conversion efficiency a) without and b) with series matching inductance in self-calibrated RF harvester.

After investigating the RF-to-DC converting systems, it is intended to investigate the ultra-low-power voltage reference circuits which are an important part of the power management circuits in the RF-powered portable devices. The typical bandgap reference structures could not be used due to their higher power consumption. New

sub-bandgap structures should be employed to meet the challenging requirements of power-starved applications. The next chapter proposes a circuit for this task.

CHAPTER 5

5 AN ULTRA-LOW POWER REFERENCE VOLTAGE GENERATOR FOR RF-POWERED PORTABLE DEVICES

This chapter expands the scope of this Ph.D. research from energy generator circuits to low power signal processing circuits. A novel ultra-low-power (ULP) voltage reference circuit is designed and implemented to be used in the front-end power management unit of wirelessly-powered portable devices. The objective of the design of a new architecture for the ULP voltage reference is to generate accurate, temperature/supply independent reference voltage while reducing the power consumption of the structure to below 100 nW. Also, it is intended to avoid utilizing multiple threshold transistors to reduce the fabrication cost.

The most important part of this section is to mathematically prove that the output voltage of the proposed circuit would be able to provide a reliable standing point for the whole structure. In this sense, a technical foundation will be provided for the circuit in addition to giving a guideline for the reader to realize the reference voltage in other fabrication processes.

Another critical criterion for the ULP voltage references is to evaluate the integrity of the results by conducting measurements through several fabricated samples. This is important due to significant impact of the process variations on the performance of the circuit. Although most foundries provide models to run Monte Carlo simulations

to assess circuit operation under process variations, measurement results should be done for several samples to assure that the output fluctuations are within the expected range.

5.1 Objective and Previous Arts

The demand for ultra-low-power reference voltage circuits in portable devices is growing increasingly by emerging internet-based platforms like wireless sensor network (WSN) and internet-of-things (IoT). Hardware implementation of these products in scale of billions put severe challenges to come up with ULP solutions while meeting the wireless standards [59]. Voltage references are essential parts of analog and digital modules and developing low-power reference voltages is critical for power-hungry LSIs [60].

Traditionally, bandgap voltage reference (BGR) [61] circuits are the common approach to generate temperature and supply-independent reference voltage. In such references, two voltages are summed to cancel the temperature coefficient of each other; *i)* the forward bias voltage of PN junction and *ii)* difference in forward voltage of two diode-connected bipolar transistor biased at different currents [46]. A Scaling factor is provided by division ratio of resistors to completely cancel the temperature dependence of the reference voltage. Stability, easy design procedure, and insensitivity over process variations are the advantages of the BGR. However, its current consumption is usually in the order of several milliamps. Reducing the supply current in BGRs asks for increasing the resistance up to hundred megaohms (i.e., with large silicon area).

In literature, many sub-bandgap references are reported in CMOS process while their supply current is in nanoamp range. Two techniques are used in CMOS-based voltage references to cancel the temperature dependence of the output. The first technique takes the advantage of the fact that the temperature coefficient of the threshold voltage of the MOSFET devices is negative and generate the reference voltage by subtracting threshold voltages of two transistors that have different threshold voltages to cancel the temperature coefficient of each other [62], [63]. The major drawback of this method is the requirement for multiple threshold devices. Also, careful process control is required (during the ion implementation) to adjust the threshold voltages.

Generating reference voltage which is equal to the threshold voltage of the MOSFETs at 0˚K is another approach to establish a temperature-insensitive reference. Although this method addresses the demand for extra fabrication mask by employing monolithic transistors, its design complexity is high. Hence, the number of transistors increases which on one hand asks for large the silicon area and on the other hand increases the power consumption. As an example of extracting the threshold voltage at absolute zero, in [64] the reference is generated by using MOS transistors operate in subthreshold region. However, several stages are cascaded for circuit realization which leads to 300 nW power consumption and minimum supply voltage of 1.5 V. Both of these values are high for many applications.

Here, the details of the design of a ULP sub-bandgap voltage reference circuit in *.GF 0.18-μm* SOI CMOS process is presented. The principle of this work is based on forcing the current passing through the transistors operating in weak inversion and strong inversion to be equal. In this way, the reference voltage becomes equal to the threshold voltage of the MOSFET at 0 ˚K. The primary approach to reduce the power consumption is to keep the number of transistors small. From fabrication cost standpoint, the design does not add any overhead due to using monolithic transistors. Also, the minimum supply voltage is maintained to 1.2 V by lowering the number of transistors cascade between supply and ground. Finally, the systematic gain error of the current mirrors arises from unequal V_{DS} of the pairs is eliminated by a stabilizer path.

5.2 Principle

Figure 5-1 illustrates the simplified circuit schematic of the proposed sub-bandgap voltage reference. It includes two asymmetric branches while gate terminals of N-type MOSFETs are tied together and the current passing through all of them is forced to be equal by current mirror. M_1 and M_4, operate in the saturation region. By appropriately setting the aspect ratios, operation of M_1 in saturation forces M_2 to operate in triode region [65]. M_3 is set to operate in the weak inversion region by setting an appropriate W/L ratio. The following subsection describes how the specific configuration

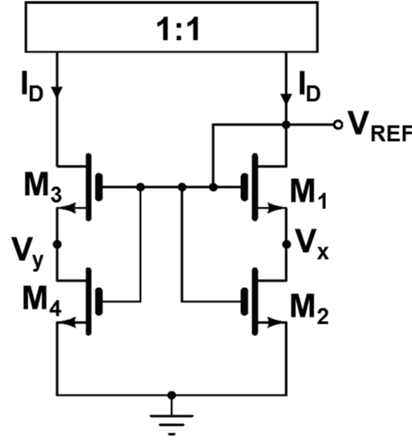


Figure 5-1: Basic schematic of the proposed reference voltage generator.

of M_1-M_4 with aforementioned operation regions leads to temperature-insensitive reference voltage.

5.2.1 Temperature Sensitivity

For M_1, and M_4, the *I-V* characteristic of the MOS device is:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{5-1}$$

where μ_n is the electron mobility in silicon and C_{OX} is the gate oxide capacitance. Slight increment of drain current due to channel length modulation effect is ignored in (5-1) since both M_1 and M_4 are long length making it possible to ignore the effect [46]. Reference voltage (V_{REF}) is equal to $V_{GS1}+V_X$ and by replacing V_{GS} with I_D in (5-1), it becomes:

$$V_{REF} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}} + V_x \tag{5-2}$$

The Drain-source voltage of M_2 (V_x) is trapped by the gate source loop composed by M_1 and M_4 (V_x=V_{gs4}-V_{gs1} =(V_{GS4}-V_{TH}) − (V_{GS1}-V_{TH})) and again using (5-1), V_x becomes:

$$V_X = \sqrt{\frac{I_D}{\mu_n C_{OX}}}\left(\sqrt{\frac{2}{\left(\frac{W}{L}\right)_4}} - \sqrt{\frac{2}{\left(\frac{W}{L}\right)_1}}\right) \tag{5-3}$$

Replacing the second term in right hand side of (5-2) with V_x according to (5-3) yields to:

$$V_{REF} = V_{TH} + \frac{\sqrt{\left(\frac{W}{L}\right)_1}}{\sqrt{\left(\frac{W}{L}\right)_1} - \sqrt{\left(\frac{W}{L}\right)_4}} V_x \tag{5-4}$$

The temperature dependence of the threshold voltage is

$$V_{TH} = V_{TH0} - \gamma T \tag{5-5}$$

while V_{TH0} is the threshold voltage at 0 K and γ is the temperature coefficient of the threshold voltage [66]. The aim of the designed circuit is to provide V_X in proportional to temperature to cancel the temperature dependence of the V_{TH} and makes the reference voltage equal to V_{TH0}. In the given process, threshold voltage at absolute zero and temperature coefficient of the threshold voltage are V_{TH0}=0.53 V, and γ=0.78 mV/°C respectively. By operation of M_3 in weak inversion region, its drain current could expressed as [46]:

$$I_D = (n-1)\mu_n C_{ox}\left(\frac{W}{L}\right)_3 V_t^2 e^{\frac{V_{REF} - V_y - V_{th}}{nV_t}}, \tag{5-6}$$

where n is the subthreshold slope, V_t $(=K_BT/q)$ is the thermal voltage, K_B is the Boltzmann constant, T is the absolute temperature and q is the elementary charge. Equating the current passes from M_3 and M_4 results to:

$$\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_4 (V_{REF} - V_{TH})^2 = (n-1)\mu_n C_{ox}\left(\frac{W}{L}\right)_3 V_t^2 e^{\frac{V_{REF} - V_y - V_{TH}}{nV_t}} \tag{5-7}$$

Assuming V_{REF} to be equal to V_{TH0} (which will be proven shortly), V_y becomes:

$$Vy = \left(\gamma + n\frac{K}{q} ln \frac{2(n-1).K^2}{A\gamma^2 q^2} \right) T \tag{5-8}$$

with $A=(W/L)_3/(W/L)_4$ which illustrates the linear dependence of V_y to the absolute temperature. Noticing that M_2 and M_3 currents are also equal, it can be written that:

$$\mu_n C_{OX} \left(\frac{W}{L} \right)_2 \left[(V_{REF} - V_{TH})V_x - \frac{1}{2} V_x^2 \right] = (n-1)\mu_n C_{ox} \left(\frac{W}{L} \right)_3 V_t^2 e^{\frac{V_{REF} - V_y - V_{th}}{nV_t}} \tag{5-9}$$

By replacing V_{REF}-V_{TH} according to (5-4), V_x becomes

$$V_x = \sqrt{\frac{1}{B-0.5}(n-1)\frac{\left(\frac{W}{L} \right)_3}{\left(\frac{W}{L} \right)_2} e^{\frac{-C-\gamma}{n\frac{K}{q}}}} V_t \tag{5-10}$$

where undefined terms have these definitions: $B=\sqrt{(W/L)_1}/(\sqrt{(W/L)_1}-\sqrt{(W/L)_4})$, $C = \gamma + n\frac{K}{q} ln \frac{2(n-1)K^2}{A\gamma^2 q^2}$. The temperature coefficient (TC) of V_{REF} from (5-4) and (5-10) is written as below:

$$\frac{\partial V_{REF}}{\partial T} = -\gamma + \sqrt{(n-1)\frac{\left(\frac{W}{L} \right)_3}{\left(\frac{W}{L} \right)_2} .e^{\frac{-C-\gamma}{n\frac{K}{q}}}} \frac{K_B}{q} \tag{5-11}$$

And zero coefficient would be obtained when the following equality holds:

$$\sqrt{(n-1)\frac{\left(\frac{W}{L} \right)_3}{\left(\frac{W}{L} \right)_2} e^{\frac{-C-\gamma}{n\frac{K}{q}}}} \frac{K_B}{q} = \gamma \tag{5-12}$$

Which yields to Zero TC for V_{REF}:

$$V_{REF} = V_{TH0} \tag{5-13}$$

This also makes the assumption taken after (5-7) valid. The final equation of the drain current of M_1-M_4 could be found by substituting V_x in (5-3) with (5-10):

$$I_D = \frac{1}{D^2}\mu_n C_{OX}\left(\frac{1}{B-0.5}(n-1)\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_2}e^{\frac{-C-\gamma}{n\frac{K}{q}}}\right)V_T^{\,2} \qquad (5\text{-}14)$$

where $D=\sqrt{(2/(W/L)_4)}-\sqrt{(2/(W/L)_1)}$. Obviously, I_D is independent from the threshold voltage which makes the supply current robust against the process variations [64].

5.3 Circuit Design and Considerations

Entire circuit schematic of the reference voltage generator is shown in Figure 5-2. It includes the core loop, the stabilizer path (M_5, M_{P3}), and the start-up circuit. Details of the core loop is provided in previous section. Stabilizer path sets the high impedance node at drain of M_3 equal to the V_{GS} of M_5.

The M_{P2}-M_3-M_4 trio which is a high impedance path, is stabilized by negative feedback including M_5 and M_{P3}. It is intended to make the voltage at node *C* equal to the reference voltage to completely eliminate the systematic error between M_{P1} and M_{P2}. In theory, it could be done by setting the aspect ratio of M_5 exactly equal to M_4. However, $(W/L)_5$ is selected lower than $(W/L)_4$ to avoid operation of M_3 and M_4 in the linear region due to mismatch. Another reason behind selecting lower $(W/L)_5$ compared with $(W/L)_4$ is that MOS transistors display slow transition from triode to active region [65]. As a result, the V_{GS} of M_5 is set 100 mV higher than V_{REF} to sufficiently suppress the dependence of M_3 current over drain-source voltage. Start-

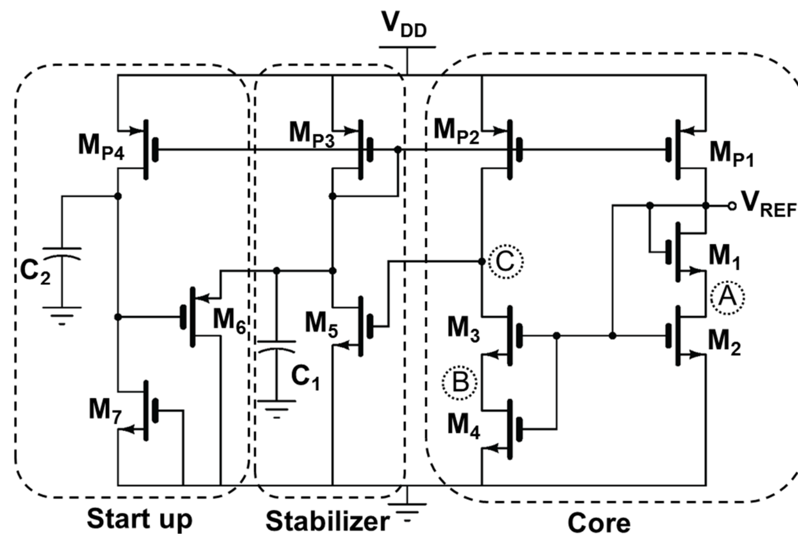
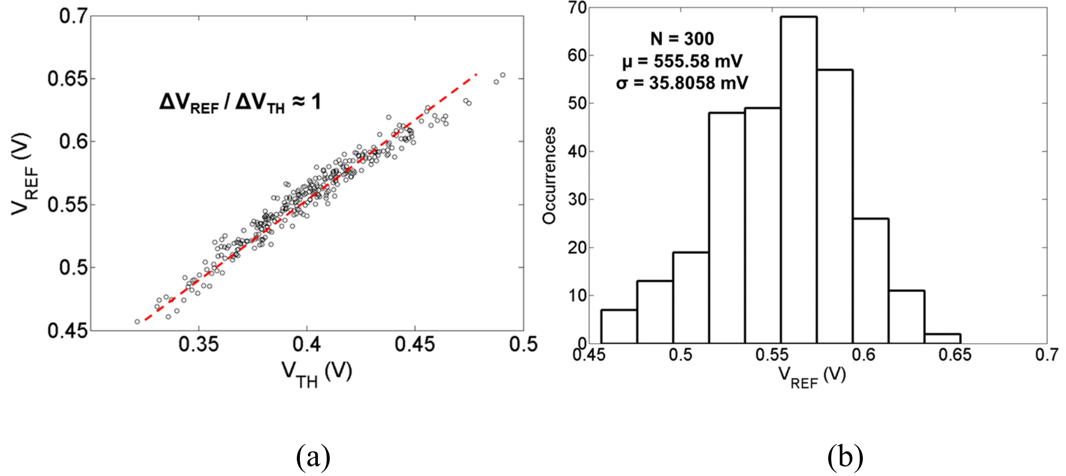


Figure 5-2: Complete circuit diagram of the proposed reference generator.

up circuit is a continuous conduction type structure [67] that drives the reference generator circuit out of the zero-current state. The current in the core loop is sampled by M_{P4} and compared with the leakage current of M_7. Then, M_6 forces M_{P3} to drive more current when zero-current state happens. The start-up network does not turn off in the normal operation of circuit but its current consumption is below 1 nA which is acceptable. Capacitors C_1 and C_2 are inserted to alleviate the susceptibility of start-up network over the injected noise from the supply. All transistors are implemented with 2.5 V body-connected transistors of *GF 0.18-μm* SOI-CMOS process. The body terminals of all transistors are connected to their source terminal. Size of all transistors is listed in Table 5-1. The longest channel length is for M5 (500μm) which may cause some random errors due to no-idealities in fabrication process. However, M5 does not contribute in setting the reference voltage and it is only responsible to keep the voltage at node C slightly above the V_{REF}. Hence, the process non-idealities of M5 have negligible destructive effect on the insensitivity of the output over temperature and supply variations.

Table 5-1: Aspect ratio of the transistors in proposed ULP reference generator circuit.

M_1	5 μm/50 μm
M_2	1 μm /100 μm
M_3	30 μm /1 μm
M_4	2 μm /186 μm
M_5	1 μm /500 μm



(a) (b)

Figure 5-3: a) Simulated Monte Carlo results of reference voltage versus threshold voltage variation (N=300). b) Monte Carlo simulation of reference voltage in (N=300).

This work selects $(W/L)_1$ = 5µm/50µm and $(W/L)_4$ = 2µm/186µm which results supply current of 78 nA at room temperature. As a final comment for transistor sizing, it should be noted that size of M_1, M_2, and M_4 are considered concurrently to fulfill the operation region requirement of the both. Noticing that the current passes through M_2 and M_4 is equal, the following relationship should be satisfied:

$$\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_4 (V_{REF}-V_{TH})^2 = \mu_n C_{OX}\left(\frac{W}{L}\right)_2 \left((V_{REF}-V_{TH})V_X - \frac{1}{2}V_X^{\,2}\right) \quad (5\text{-}15)$$

5.3.1 Process Mismatch

Dependence of the reference voltage to the threshold voltage at absolute zero reveals the importance of the mismatch analysis on the reference voltage. Mismatch in MOSFETs comes from fluctuations in the threshold voltage, and transconductance parameter ($\mu_n C_{ox}$) [68]. Assuming that variations in device dimensions is alleviated using layout techniques (i.e. making transistor areas large and adding dummy diffusions), threshold voltage fluctuations has the most significant effect on the reference voltage. Recalling the theoretical discussions provided in the previous section, some key conclusions could be drawn to lessen the mismatch variations:

i) According to (5-13), the reference voltage is directly proportional to the threshold voltage of N-type MOSFETS suggesting that its threshold deviation due to process

mismatch should be minimized. Standard deviation of the threshold variations is inversely proportional to effective area of transistor [68]:

$$\sigma_{V_{TH}} \propto \frac{1}{\sqrt{W_{eff}.L_{eff}}} \tag{5-16}$$

suggesting that to improve the threshold insensitivity one should selects the transistor physical size large enough.

ii) During the temperature sensitivity analysis of the reference voltage in (5-9), it is assumed that the threshold voltage of M_3 and M_4 are exactly equal. Hence, Drawing the M_3 and M_4 layout in close proximity makes the reference voltage less sensitive to device parameter mismatch.

iii) Current matching in P-type current mirrors could be improved by increasing the gate-source voltage of the transistors. However, it would be obtained at the cost of lower *(W/L)* ratio for a given current which degrades line sensitivity and power supply rejection ratio.

Monte Carlo simulation of 300 run is shown in Figure 5-3. As expected form (5-13) the reference voltage is directly proportional to the threshold value of transistors. The simulated mean value of reference voltage is 555 mV and standard deviation of the simulated voltages is 35.8 mV.

5.3.2 Supply Sensitivity

Analysis of the reference sensitivity over the large and small signal variations of the supply voltage is surveyed in this subsection. Effect of large signal and small signal variations is gauged by Line sensitivity (LS) and power supply rejection ratio (PSRR) respectively.

In general, the major approach to improve LS is to increase the impedance from V_{REF} to V_{DD}. In this work, the impedance seen by V_{DD} gets large enough by increasing the channel length of the current mirror transistors (M_{P1}-M_{P4}). The penalty for long channel P-type transistors is increasing their effective voltage (V_{eff}=V_{gs}-V_{th}) and consequently requiring larger minimum supply voltage. Also, total silicon area will be increased.

From small signal perspective, the noise from supply mainly couples to V_{REF} through M_{P1} and M_{P2} (Figure 5-4). The reason for that is the incoming noise form M_{P3} is negligible due to large attenuation from drain to gate of M_5. However, as depicted in Fig. 4, the active load nature of the M_1-M_4 helps to improve the rejection from the supply noise. The total small signal gain from supply to the output is:

$$\frac{V_{ref}}{V_{dd}} = \frac{V_{refa}}{V_{dd}} + \frac{V_{refb}}{V_{dd}} \tag{5-17}$$

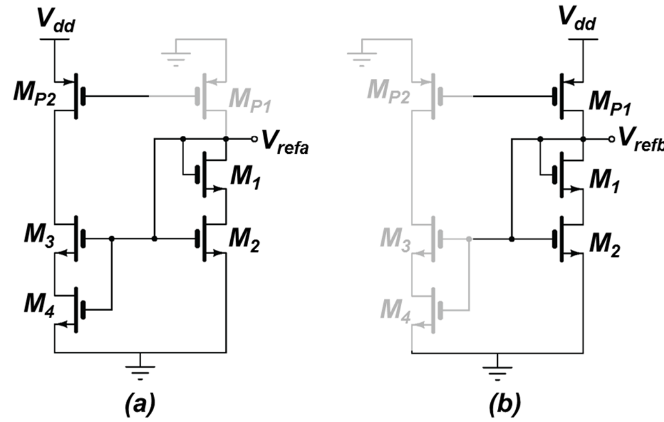


Figure 5-4: Small signal analysis of V_{REF} due to V_{dd} noise a) Coupled by M_{P2} b) Coupled by M_{P1}.

Derivation of the exact relationship for V_{ref}/V_{dd} is straightforward but tedious. However, to gain insight, it is sufficient to say that the sign of the first term in the right hand side of (5-17) is positive while the ones of the second term is negative. In other words, most of the signal coupled by M_{P1} is cancelled by M_{P2}.

5.3.3 Supply Voltage Range

Recalling the equations used to elaborate the temperature independent reference voltage in Section 5.2.1 may suggest that V_{REF} does not depend on the supply voltage. However, it is assumed that the supply voltage is large enough for proper operation of the M_1-M_5 inside the intended regions. The minimum supply voltage is limited by the M_{P3} and M_5 path. Drain-source voltage of M_3 should be higher than $4V_T$. As mentioned before, the voltage at node C is selected slightly (100 mV) above the reference voltage to provide some margin against possible mismatches and also to assure negligible dependence of the drain current of M_3 on its drain-source voltage variations. In this sense, the minimum supply voltage becomes

$$V_{DD,min} = V_C(at\ T_{max}) + 4V_T + 100\ mV - V_{TH5} + V_{GS3} \tag{5-18}$$

Which is 1.2 V in the given *GF 0.18-µm* process. On the other hand, maximum allowable supply voltage is determined by breakdown voltage of transistors.

5.3.4 Channel Length Modulation

Non-zero drain-source voltage increases M_3 and M_4 current due to channel length modulation (CLM) effect. M_1 is diode-connected and M_2 operates in linear region meaning that CLM could be ignored for them. Rewriting the drain current by equating M_3 and M_4 currents in (5-7) results in the following equality:

$$\begin{aligned}&\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_4 (V_{REF} - V_{TH})^2 (1+\lambda V_{DS4}) = \\ &(n-1).\mu_n C_{ox}\cdot\left(\frac{W}{L}\right)_3 .V_t^2 .e^{\frac{V_{REF}-V_y-V_{TH}}{nV_t}} (1+\lambda V_{DS3})\end{aligned} \tag{5-19}$$

In (5-19), the CLM terms $(1+\lambda V_{DS})$ at the right and left hand side of (5-16) nullify each other since the V_{DS} voltage of M_3 and M_4 are comparable to each other. The effect of the channel length modulation in M_5 on the amount of the output voltage is trivial since it is simply inserted to stabilize the high-gain path and has little impact on the operation of the transistors in the core loop. Finally, any mismatch between V_{DS3} and V_{DS4} could be suppressed by using long channel lengths for M_3 and M_4.

5.3.5 Body Effect

Noticing that the proposed voltage reference circuit is implemented in SOI process which allows tying the body terminals to source terminals, threshold variation due to the body effect could completely be eliminated. The same scenario, happens in deep N-well process and isolated transistors fabricated in CMOS process.

In the case of realizing the proposed circuit in standard Bulk-CMOS process, body effect will appear due to the non-zero source-body voltage of M_1 and M_3. Then (5-2) and (5-7) should be rewritten by modifying V_{TH} term including the body-source voltage. When the device operates in strong inversion region, the threshold voltage including the body effect (V_{THb}) is given as below:

$$V_{THb} = V_{TH} + K_1\left(\sqrt{\varphi_s + V_{SB}} - \sqrt{\varphi_s}\right) + K_2 V_{SB} \tag{5-20}$$

where V_{TH} is given by (5-5), φ_s is the surface potential, and K_1 and K_2 are model parameters. However, the effect of non-zero source-body voltage on the current equation of M_1 is negligible since its source voltage is connected to the drain voltage of M_2 (V_x), which operates in deep-triode region.

M_3 operates in the weak inversion region and the non-zero source-body voltage (V_{SB}) modify the drain current as below:

$$I_D = (n-1).\mu_n C_{ox}.\left(\frac{W}{L}\right)_3 .V_t^2.e^{\frac{\frac{1}{n}.(V_{GB}-V_{TH})-V_{SB}}{V_t}} \quad (5\text{-}21)$$

Noticing that the source-body voltage of M_3 is equal to Vy, (5-7) will be modified as below:

$$\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_4 (V_{REF}-V_{TH})^2 = (n-1).\mu_n C_{ox}.\left(\frac{W}{L}\right)_3 .V_t^2.e^{\frac{\frac{1}{n}.(V_{REF}-V_{TH})-V_y}{V_t}} \quad (5\text{-}22)$$

In this sense, following the same procedure by starting with the assumption that reference voltage is equal to V_{TH0}, V_y would be found as a linear function of temperature while the coefficient of dependence should be modified slightly. Afterward, the validity of V_{REF}=V_{TH} could be proved similar to Section 5.2.1. Therefore, even with implementing the reference voltage in standard CMOS process, the output voltage could be independent from temperature by only adjusting the size of the transistors.

5.3.6 Kink Effect and History Effect in PD-SOI Process

Realizing analog circuits in SOI process causes lower parasitic components compared to Bulk-CMOS counterpart but have some drawbacks. Kink effect and History effect are the most important ones. Kink effect is the excess current in the MOSFET induced by excess carrier accumulation and approximately scales with the inverse square of the channel length. Hence, higher channel lengths (as done in this work) should be used to eliminate it. More importantly, transistors with body-contact should be used to suppress the kink effect. Body connection also helps to eliminate the history effect which causes unwanted variation in the body voltage over the time due to different

currents leaked into the body. Using body-connected transistors (as done in this research) helps to establish a well-defined value for the bulk potential.

5.4 Measurement Results

To evaluate the characteristics of the reference circuit, the design is fabricated in *GF 0.18-µm* SOI CMOS process. Figure 5-5 shows the die micrograph and the layout of the designed ULP reference voltage. The chip area is 0.0207 mm^2 (74µm×280µm). The reference voltage is protected by ESD circuitry. Three bondwires connect the GND, V_{DD}, and V_{REF} nodes to the test setup. To measure the temperature sensitivity of the fabricated dies samples are placed in a furnace. The

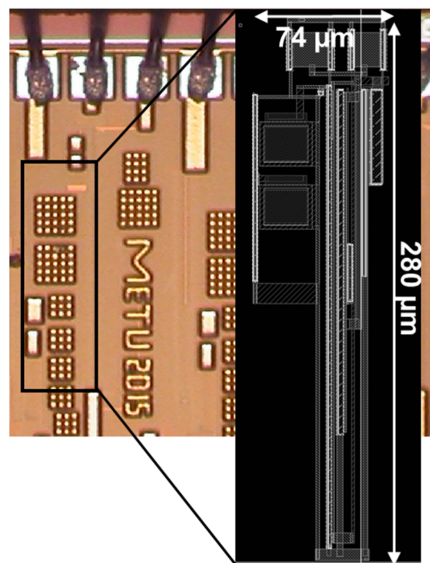
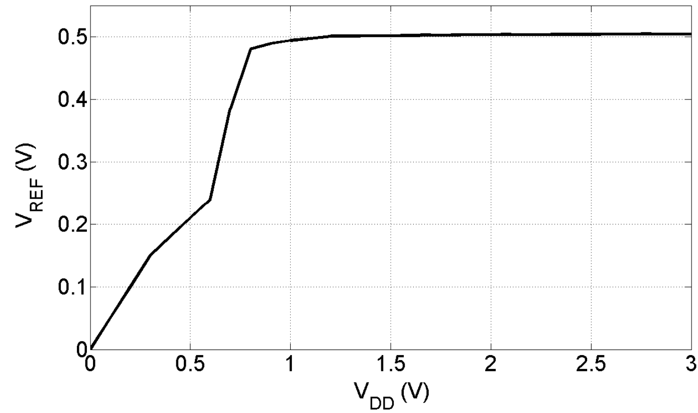
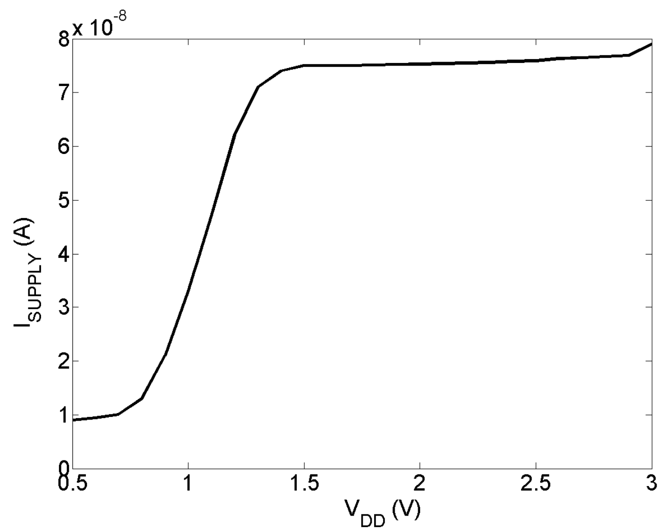


Figure 5-5: Die micrograph and layout diagram of the fabricated chip.

temperature of the samples is swept between 0 ˚C to 100 ˚C. Although the temperature inside the furnace could be monitored, the temperature distribution at different places of the furnace could change drastically. Hence, to report accurate results, a temperature sensor is located in close vicinity of the sample to determine the accurate temperature of the sample. High impedance multi-meter is used to measure the output voltage of the reference generator circuit. The current consumption is measured by connecting a 100 kΩ resistance between the DC voltage source and V_{DD} terminal of the circuit. Then the supply current is measured by probing the voltage across the resistance. As mentioned above, the current consumption of the device is below 100 nA. Hence, the voltage across the resistor is lower than 10 mV.



(a)



(b)

Figure 5-6: Measured results versus variation of the supply voltage a) Reference voltage. b) Supply current.

Figure 5-6 (a) and (b) draw the measured reference voltage and supply current of the reference voltage over the variation of the supply voltage. The reference voltage shows 0.36 %/V line sensitivity which is very good when compared with the state of the art. Also, the current consumption when sufficient supply voltage exists (V_{DD}>1.2 V) is 78 nA meaning that the power consumption would be 90 nW. Further details of the measured samples are presented in the histogram diagram of 22 different samples in Figure 5-7 and Figure 5-8.

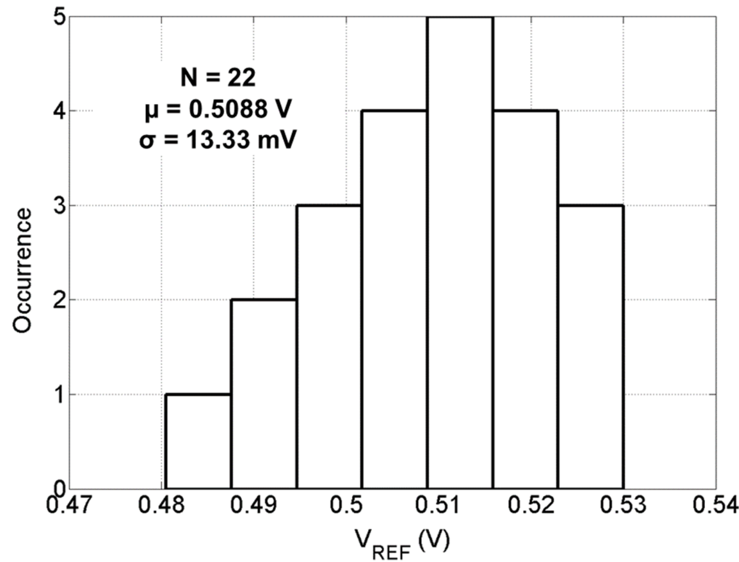


Figure 5-7: Measured reference voltage of 22 samples.

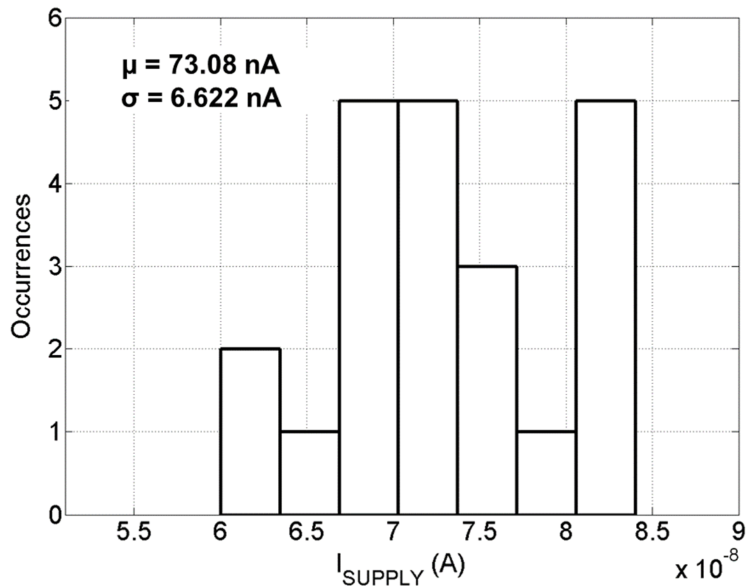


Figure 5-8: Measured supply current of 22 samples.

The standard deviation of the reference voltage is 13 mV which is lower than the standard deviation of simulated results (35 mV). That is because in simulations both lot-to-loy and within-lot mismatch effect are considered but the measured samples are fabricated in a single wafer meaning that the lot-to-lot variations are negligible in measured results. The measured voltage and currents are measured at room temperature (27 ˚C) when the supply voltage is set to 1.2 V.

Figure 5-9 shows the measured reference voltage over the variation of the temperature. The temperature range of the circuit is from 10 ˚C to 100 ˚C. The

temperature coefficient is almost equal for different supply voltages and is 188 ppm/˚C at minimum supply. Simulated TC at 1.5 V supply voltage is 40 ppm/˚C. The exact reason for considerable gap between simulated and measured TC is unknown at the time of the writing, and currently being investigated.

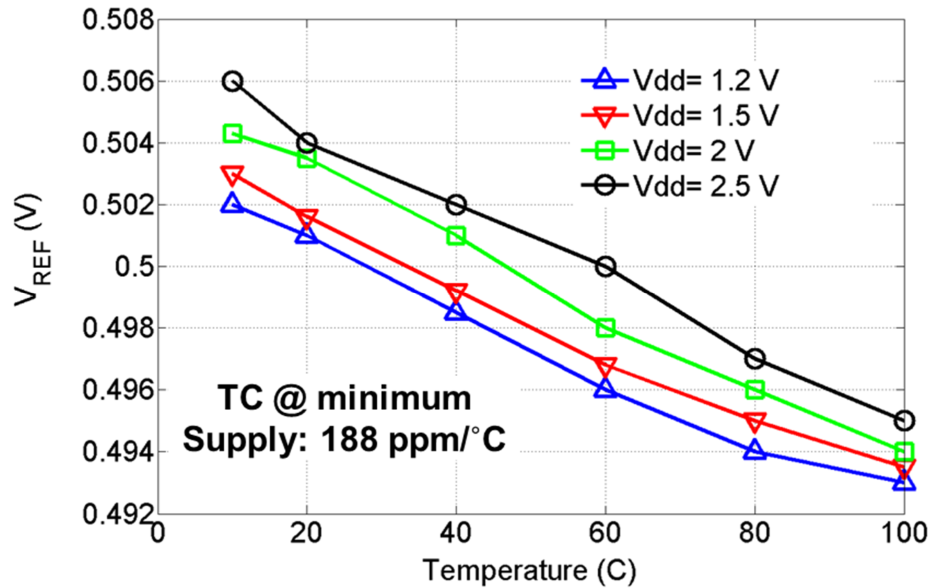


Figure 5-9: Measured reference voltage versus temperature variation at different supply voltages.

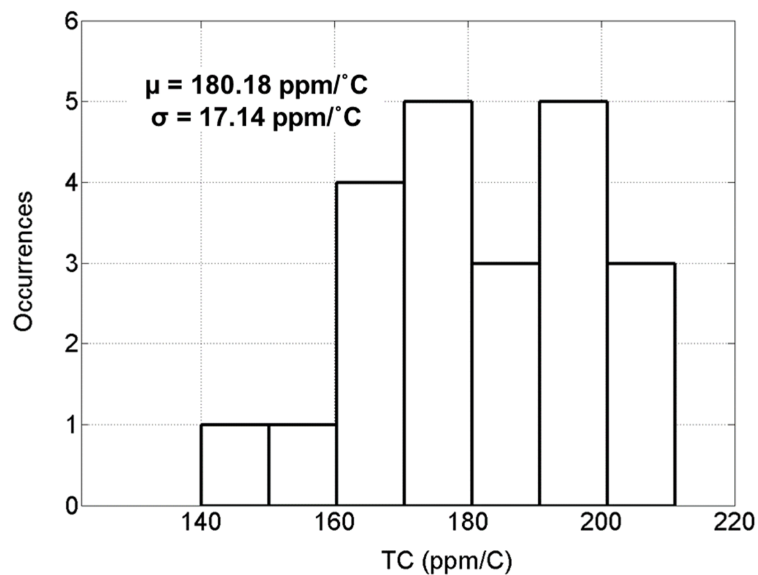


Figure 5-10: Histogram diagram of measured temperature coefficient for 22 samples (V_{DD}=1.2 V).

Table III. Comparison of the results with state of the art works.

	This work	**JSSC 2011, Magnelli** [69]	**JSSC 2009 Ueno** [64]	**JSSC 2007 De Vita** [63]	**TCAS II- 2006 Huang** [70]	**El. Lett. 2009** [71]
Temperature range	10-100˚C	0-125˚C	-20-80˚C	0-80˚C	-20-120˚C	-20-80˚C
V_{DD}	1.2 – 3 V	0.45– 2 V	1.4 – 3 V	0.9 – 4 V	0.85 – 2.5 V	1.1 – 4 V
V_{REF}	501 mV	263.5 mV	745 mV	670 mV	221 mV	96.6 mV
Power Dissipation	87.6 nW @ (V_{DD}=1.2 V)	3 nW @(V_{DD}=0.45 V)	0.3 µW @ (V_{DD}=1.2 V)	36 nW @(V_{DD}=0.9 V)	3.299 µW @(V_{DD}=0.85 V)	23 nW @(V_{DD}=1.1 V)
TC	188 ppm/˚C	142 ppm/˚C	7 ppm/˚C	10 ppm/˚C	194 ppm/˚C	11 ppm/˚C
Line sensitivity	0.369%/V	0.44%/V	0.002%/V	0.27%/V	0.905%/V	0.09%/V
PSRR	-36.47 dB (@ 100 Hz) (Simulation)	-45 dB (@ 100 Hz)	-45 dB (@ 100 Hz)	-47 dB (@ 100 Hz)	-	-60 dB (@ 100 Hz)
Chip Area	0.01344 mm^2	0.043 mm^2	0.055 mm^2	0.045 mm^2	0.0238 mm^2	0.0189 mm^2
Extra Requirement	-	High-V_{th} and Standard-V_{th}	-	High-V_{th} and Standard-V_{th}	High value resistors	Thick-oxide and Thin oxide transistors

As can be seen from Figure 5-9, the temperature coefficient of different samples is between 140 ppm/˚C and 211 ppm/˚C with mean value of 180 ppm/˚C. The comparison of the experimental results with the state of the art is presented in Table 5-2. From this table it can be seen that the power consumption of this work is comparable with the other reported works. The lower power consumption in [69], [63], and [71] is achieved at the cost of extra fabrication steps. For example, [63] and [69] requires high-V_{th} transistors (with V_{th}=0.7 V) which is hard to found in low-power foundry design kits. Also, [71] demands availability of thick and thin oxide layers which may not feasible to implant in most of the fabrication process. The measured average temperature coefficient is acceptable for ULP power management networks. That is because, the ULP reference voltages are directly connected to the output of energy harvesting circuitry and are used to detect whether sufficient power exist or not. Fine tuning of the DC voltage used as supply for sensitive signal processing blocks is done by another accurate reference voltage with a power consumption in the µ-watt range. Thanks to the efficient reduction of supply variations by selecting long-channel P-type transistors and the active load nature of the structure, the line sensitivity and the power supply rejection ratios are comparable with the previous arts.

In circuit design perspective, the biggest advantage of the proposed circuit is its simple design procedure due to straightforward sizing techniques and few number of transistors. The simplicity of the topology helps to reduce the power consumption down to 86 nW and reduces the silicon area compared to previous works. Finally, the structure is realized with monolithic transistors which is advantageous for cost reduction in mass production.

CHAPTER 6

6 CONCLUSION AND FUTURE WORKS

As the structure of thesis suggests, the outlook of this Ph.D. research should be inspected in four different frameworks: *i)* Analysis of UHF rectifiers *ii)* Design of UHF rectifiers *iii)* Analysis of antenna-rectifier interfaces and *iv)* Design of ULP reference generator for power management unit. The achievements of most sections in comparison with previous arts was thoroughly discussed in the content of this thesis. However, some research topics (Analysis of threshold self-compensated rectifiers, Analysis of matched and mismatched antenna-rectifier interfaces) are completely unique and no similar works exist in the literature (to the best of the authors knowledge) to conduct a fair comparison. Overviewing the general approaches, the achievements of each part of this research is briefly discussed. At the end, the parts of this research which are prone to further improvement are highlighted as future works.

6.1 Thesis at a Glance

Analysis and modeling of UHF rectifiers are important part of this thesis. UHF Dickson and the threshold self-compensated architectures are selected to be inspected in detail. Choosing these architectures are mainly because of their wide use in both academic works and industrial prototypes. Specially, the Dickson architecture is the most well-known topology used for converting the RF signals into DC form. Simplicity of these architectures is another reason for their popularity.

UHF Dickson rectifier is inspected to provide more accurate formula when compared to the previous studies for predicting the output voltage when the design is fabricated in advanced CMOS process. Unlike the previous works which ignore the secondary effects (like velocity saturation and channel length modulation) this work improves the accuracy of the predicted output voltage by taking these non-linarites into account. Yet, a single formula is presented at the end which gives the output voltage by simply plugging the process parameters and the RF amplitude data to the formula. Another advantage of the proposed approach is that it is possible to expand the predicted output voltage when the amplitude of the incoming RF voltage is very low such that the device operates in the weak inversion region. Finally, an optimization approach is presented for maximizing the power conversion efficiency of the Dickson rectifier which instantly gives the optimum device aspect ratio and the number of stages. The predicted input power ranges from -12 dBm to 0 dBm while the connected load could change from 20 kΩ to 1 MΩ.

The analysis of the threshold self-compensated rectifiers is also conducted in this research. The main difficulty during the inspection of the self-compensated architectures is attributed to its gate connection configuration. The structure by its nature ties the gate terminals to the source of the right-neighboring transistors to provide the required compensation voltage without adding extra cost on complexity and silicon area. However, it makes the study of single transistors difficult, since its operation depends on the neighboring transistors. To ease the analysis of the single-stage self-compensated structure, a simple behavioral model is presented. Then, dependence of the load current and the input RF power on the output DC voltage is investigated in the same manner that was done for the Dickson rectifiers. At the end, by taking the output DC voltage as the input argument, close coherence between the load current and power efficiency curves is observed. This similarity is very useful since elaborating the dependence of the load current to the output voltage (for each RF amplitude) is straightforward while the one of power conversion efficiency is complex. As a conclusion, using the charge conservation principle, the peaking point of load current versus output DC voltage is found and is used for determining the optimum device aspect ratios and number of stages for multi-stage structures in order to maximize the power conversion efficiency. Although the optimization formula is

an implicit equation which should be solved in a mathematical program, its independence from (W/L) ratio of transistors makes a single run sufficient enough to find the optimum design parameters in the given process. The presented model could accurately predict the optimum aspect ratio and number of stages when the RF amplitude changes from 200 mV to 500 mV. Connected loads also could change from 10 kΩ to 1 MΩ. The predicted output voltage of 4-stage rectifier is validated by simulation and measurement results when the input RF power changes from -10 dBm to 0 dBm.

From the circuit design standpoint, a novel method, which author calls the self-calibration technique, for compensating the intrinsic threshold voltage of the transistors is presented in this thesis. The objective of this technique is to address the extra compensation voltage problem in self-compensated rectifiers under large RF power incident on the rectifier. This problem leads to the flow of high discharging current and consequently reduces the power conversion efficiency of the structure. The principle of the proposed self-calibration technique is to make the compensation voltage independent from the intensity of the incoming RF signal and also the load current. The idea is realized by adding two auxiliary rectifiers for each stage. Both rectifiers are simple 2-stage Dickson rectifiers while their power consumption is negligible due to their low (W/L) ratio. One auxiliary rectifier converts the incoming RF signal to DC form in order to generate the compensation voltage and the other auxiliary rectifier calibrates the compensation voltage to the desired value. The calibration is performed by tuning the current drawn from the output of the compensation-generator auxiliary rectifier. The design procedure is formulized by mathematical relationships in order to provide more insight for the reader. Characterization of the self-calibration technique is performed both by simulation and measurement results. It is shown that unlike the previous compensation techniques where extra leakage current degrades the power conversion efficiency, this work provides high PCE within the broad range of incoming RF power intensities. The technique is suitable for wireless charging applications where several base stations may transmit RF signals with different intensities and having high PCE for different RF powers is desirable. The sensitivity of the measured self-calibrated structure is -19 dBm with a peak efficiency of 34% at -7 dBm. Thanks to the lack of extra

discharging current, the efficiency variation is kept below 5% within 10 dBm variation of the input RF power.

Another circuit proposed in this thesis is the switched-gate UHF rectifier. It is designed to increase the peak power conversion efficiency of the rectifier compared to the self-compensated rectifiers. The switched-gate architecture accepts adaptive threshold compensation instead of constant compensation which is used in self-compensated rectifiers. It is noticed that providing a constant compensation voltage have two opposing aspects: On one hand it improves the charging current from source to the load during the conduction phase which is desirable. On the other hand, it eases the flow of discharging current during the reverse isolation phase which is not desirable. To overcome this difficulty, adaptive threshold compensation technique is proposed which alter the gate terminal between right and left neighboring voltages according to the phase of the incoming RF signal. Altering the gate terminal is done using two complementary switches. The advantage of the adaptive cancelation technique comes at the cost of the demand for high speed switching. Two multi-stage switched-gate rectifier is designed and fabricated. The first design had been fabricated in UMC *0.18-μm* CMOS process and the speed of the transistors was not high enough for 900 MHz operation. The second design has been fabricated in *GF 0.18-μm* PD-SOI process and the availability of low-voltage transistors only in body-less structure causes problems stemming from the history effect. The consequence was that even with the operation of the device at 900 MHz, the minimum required input RF power was -6 dBm which is higher than the expected input RF power (-12 dBm). It was concluded that, the proposed technique showed some promise. However, if the circuit was designed in FD-SOI process with body contacts, the circuit would show its best potential.

Aside from the analysis and the design of UHF rectifiers, design of antenna-rectifier interface circuits is investigated in this thesis. It is intended to evaluate the matched and mismatched networks and compare their pros and cons. It is shown that by assuming equal load for both topologies, the voltage gain of the matched network (from input of the RF source to the input port of the rectifier) is always higher than the gain of the mismatched network. However, it is also revealed that the matched interfaces put more severe restrictions on the physical size of the matching reactive

components. For example, size of the required inductance for the matched network is significantly higher than the required inductance for the mismatched network. Obviously, it makes on-chip solutions hard to realize. Also, the matched network requires the value of the input capacitance of the IC to be lower than a specific value to make the resistive part of the rectifier equal to the one of RF source. But, the mismatched network does not impose any restriction on the input capacitance of the IC. However, their voltage gain is lower than the matched network. It is concluded that when the input impedance of the IC is several kΩs (by assuming that resistive part of the RF source is below 100 Ω), mismatched interfaces are better option. Otherwise, when the resistive part of the IC input impedance is lower than 1 kΩ, using matched interface is feasible without imposing harsh restriction on the value of reactive matching components.

As a last part of this Ph.D. study, a custom topology for ULP voltage reference circuit is presented. The reason for targeting the reference generator is that the power consumption of the front-end power management section in portable autonomous devices is mostly determined by this block. It is intended to reduce the power consumption below 100 nW. Although, some transistors operate in strong inversion region, the supply current consumption is reduced by realizing the structure with only three paths from positive rail to ground. Insensitivity of the designed voltage reference over temperature variation is proved both by mathematical relationships and simulations. The symmetric active-load (by current mirrors) nature of the structure makes the output voltage immune against small and large signal supply variations. Averaged reference voltage and power consumption of 22 samples are 501 mV and 87.6 nW respectively. The measured line sensitivity is 0.369%/V. Finally, realizing the reference voltage only with single-threshold transistors alleviates the demand for extra fabrication mask (for multi-threshold devices) and consequently reduces the fabrication cost.

In summary, the major contributions of this thesis are:

- Proposing a new modeling approach for UHF Dickson rectifiers suitable for deep-submicron implementations.

- Proposing a new method for the analysis and the optimization of threshold self-compensated rectifiers.
- Proposing a new self-calibrated UHF rectifier to avoid efficiency drop in self-compensated rectifiers.
- Proposing a new switched-gate UHF rectifier to increase the peak power conversion efficiency of the self-compensated rectifier.
- Providing insights about the analysis and design of antenna-rectifier interfaces.
- Proposing a new ULP sub-bandgap reference voltage circuit suitable for the power management unit of RF-powered portable devices.

6.2 Possible Topics for Future Research

The presented results of the designed circuits (except switched-gate technique) and proposed analytical methodologies are all comparable with the state of the art works. Yet, further studies could be done to improve some aspects.

Analysis of UHF rectifiers is essential to understand the operation of the RF-to-DC converting systems. Aside from the Dickson and the threshold self-compensated architectures, interest toward the differential drive UHF rectifiers is growing. Their analysis and modeling would be very beneficial for instantly finding their output voltage and also providing the optimum device sizes and number of stages. Although they show good power conversion efficiency numbers at low RF powers, differential drive rectifiers suffer from overload problem and requires some control circuitry to direct their load current. Careful analysis to set safe RF boundaries for alleviating the demand for protection circuitry is also worthy to investigate. Co-design of antenna and rectifier is another hot topic which still needs some improvement. Finally, analysis of the output impedance of the UHF rectifier during the transient phase could not be found in the literature and could be very useful during the design of low drop out regulator (LDO) circuit in the power management unit.

In the circuit design level, many architectures are proposed in the literature for UHF rectifiers and little room exist for novel architectures. However, the attempts could be shifted from rectifier to the impedance matching section. Designing an adaptive impedance matching networks is done before in literature [9]. But there are still a lot

to be done. For example, aside from tuning the capacitor bank in matching network, inductor tuning could be considered to deliver maximum power to the rectifier even with the variation of the RF or the load power.

As mentioned above, a ULP voltage reference is proposed in the content of this thesis. Although the dependence of the output voltage to temperature and supply variations could be addressed by sizing techniques, the output voltage still depends on the threshold voltage of the device. A single trim calibration scheme could be applied to the proposed circuit to suppress the process variations and minimize die-to-die variations. From another perspective, the linear dependence of the output voltage in the ULP voltage reference to the threshold voltage could be used to calibrate other sensitive signal processing circuits. As an example, when the current consumptions of low noise amplifiers (LNA) and mixers are reduced from μ-ampere to n-ampere for very low power applications, their performance becomes more likely to deviate from ideal due to process variations. In this case, the output of the ULP reference voltage could be used as an indicator of the threshold voltage for each sample and its output could be used to calibrate the characteristics of other sensitive processing blocks.

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APENDICES

A. Output Voltage of Dickson Rectifier with Body Effect

Appendix section modifies equations (2-16) and (2-25) by including the variation of V_{TH} due to the body effect. This work employs the N-well process in which the body terminals should be connected to the lowest potential (ground). The principal equation which is used for finding the output voltage is equation (2-9) which is rewritten here:

$$\frac{I_P}{I_L} = \frac{1}{\frac{1}{2}\left(\frac{\Delta t_f}{T}\right)} \cong \frac{2}{\frac{1}{2} - \frac{1}{\pi} sin^{-1}\left(\frac{V_{UP} + \frac{V_{th}}{2}}{V_a}\right)} \tag{2-9}$$

In this equation, I_P, and V_{TH} show variation due to the body effect. The dependence of the threshold voltage to the body-source voltage can be expressed as:

$$V_{TH} = V_{TH0} - K_1\left(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s} - K_2 V_{bs}\right) \tag{A-1}$$

where V_{TH0} is the threshold voltage of the device when the body-source voltage (V_{bs}) is zero, K_1 and K_2 are technology parameters, and φ_s is the surface potential. Due to importance of accurate estimation of I_P the body source voltage will be taken into account at the middle of the conduction time for which the maximum forward current will be flow. The body-source voltage of the clamp transistor at i^{th} stage (M_{2i-1} in Figure 2-1) is:

$$V_{bs,2i-1} = -\left(V_{2i-2} + V_{up,2i-1} - V_a\right) \tag{A-2}$$

Where V_{2i-2} is the generated DC voltage from previous stage. For the sake of simplicity, it can be assumed that the body-source voltage of the first stage is equal to zero and the generated DC voltage by each clamp transistor ($V_{UP,2i-1}$) is equal to the one generated by the previous stage ($V_{UP,2i-3}$).

Using (A-2) as the bulk-source voltage for the calculation of both I_P and V_{TH} in the conduction time, the output voltage for each stage can be written as:

$$V_{DC,i} = 2\left[V_a - V_{TH,2i-1} - \left(-\frac{a_2}{4} + \frac{P_4}{2} + \frac{(P_5 + P_6)^2}{2}\right)\right] \quad \text{(A-3)}$$

where $V_{TH,2i-1}$ can be calculated by inserting (A-2) into (A-1). The total output voltage can be found by calculating the generated voltage in each stage and using it for determining the boy-source voltage of the preceding stage. Augmenting the generated voltage by each stage, the total output voltage becomes:

$$V_{OUT} = \sum_{i=1}^{N} V_{DC,i} \quad \text{(A-4)}$$

The same procedure is followed for finding the impact of body-source voltage on the elaborated formula for PCE in (2-25). By replacing the constant V_{TH} with the modified expression in (A-1) and (A-2), and updating I_P, Δt_f, Δt_r and I_R values for the clamp transistor at i^{th} stage, the rectifier PCE becomes:

$$\eta_{rect} = \frac{I_L V_{OUT}}{\frac{2}{T}\cdot\left(\sum_{i=1}^{N}\left(\frac{1}{2}\Delta t_{f,2i-1} I_{p,2i-1}\left(V_a - \frac{1}{2}V_{DC,i}\right) + \frac{1}{2}\Delta t_{r,2i-1} I_{R,2i} - 1\left(V_a + \frac{1}{2}V_{DC,i}\right)\right)\right)} \quad \text{(A-5)}$$

VITA

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