COLUMN LEVEL TWO-STEP MULTI-SLOPE ANALOG TO DIGITAL CONVERTER FOR CMOS IMAGE SENSORS

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ABSTRACT

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In the past few years, CMOS image sensors has performed an enormous growth in technology and their market is broadened with the integration cameras on the cell phones. The advancement trend continues as the pixel sizes getting smaller and the array formats getting larger. With pixels decreasing in size and growing in numbers, faster row read-out speed requirements have emerged to keep frame rates constant. Column parallel ADC architectures meet these demands as they utilize large numbers of parallel conversion channels.

This thesis presents the design of a 12-bit column parallel Two-Step Multi-Slope (TSMS) analog to digital converter for low power CMOS image sensors. TSMS ADC architecture enables larger conversion speeds compared to widely implemented Single Slope architecture on its Two-Step Single-Slope (TSSS) mode. Proposed design can achieve even larger readout speeds in the TSMS mode, where it exploits the relaxed quantization noise requirements for larger shot noise, introduced to the circuitry by

pixels subject to a large photon flux, by reducing the conversion resolution and increasing the conversion speed.

The design is realized for pixel pitch of 6.7μm. Power consumption per column ADC is 88 μW and sampling speeds larger than 50kS/s is supported. The prototype IC generates timing and biasing signals on its own. Using SPI interface, bias voltages can be trimmed with the help of DACs and timing signals can be programmed to adapt different operation modes and speeds. Layout of the design is drawn using 180nm process and 3.15 mm × 3.15 mm sized prototype IC is sent to multi-project-wafer MPW run for fabrication.

Keywords: CMOS image sensor, Shot Noise, Analog to Digital Converter, Column-Parallel ADC, Two-Step Single-Slope ADC

ÖZ

CMOS GÖRÜNTÜ SENSÖRLERİ İÇİN KOLON SEVİYESİ İKİ ADIMLI VE DEĞİŞKEN RAMPA EĞİMLİ ANALOG/SAYISAL ÇEVİRİCİ

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Geçtiğimiz yıllarda CMOS görüntü algılayıcı teknolojisi ciddi bir ilerleme katetmiş ve pazar payı kameraların cep telefonlarına entegrasyonu ile beraber oldukça büyüme göstermiştir. İlerleme eğilimi piksel boyutlarının küçülmesi ve piksel dizininin büyümesi yönünde devam etmektedir. Küçülen pikseller ve dizindeki piksel sayısındaki artış, resim hızını sabit tutma amacıyla satır okuma hızında artış ihtiyacını doğurmuştur. Kolon seviyesi için tasarımı gerçekleştirilen ve paralel olarak yüksek sayılarda yerleştirilen Analog/Sayısal Çeviriciler bu ihtiyaçlara cevap verebilmektedir.

Bu tezde düşük güç tüketimli CMOS görüntü algılayıcıları için tasarlanmış 12-bit, kolon seviyesi, İki Adımlı-Değişken Rampa Eğimli Analog/Sayısal Çevirici mimarisi sunulmaktadır. İki Adımlı-Değişken Rampa Eğimli Analog/Sayısal Çevirici mimarisi, İki Adımlı-Sabit Eğimli Çevirici modunda CMOS görüntü algılayıcı uygulamalarında genel olarak tercih edilen Sabit Eğimli Analog/Sayısal Çevirici mimarisine kıyasla daha kısa süreli çevrimlere olanak sağlayabilmektedir. Öne sürülen tasarım İki Adımlı-

Değişken Rampa Eğimli Analog/Sayısal Çevirici modunda ise yüksek miktarda foton akısına mağruz kalan piksellerin yüksek miktarda atım gürültüsü üretmesinden dolayı niceleme gürültüsününün düşük tutulmasına gerek olmadığı için çevrim çözünürlüğünü düşürerek çevrim hızını daha da arttırabilmektedir.

Tasarım 6.7 μm piksel adımı için gerçekleştirilmiştir. Her kolon çeviricisin güç tüketimi 88 μW seviyesindedir ve 50kS/s örnekleme hızı sağlanabilmektedir. Örnek tümleşik devre ihtiyacı olan kutuplama ve zamanlama sinyallerini kendi içerisinde üretmektedir. Seri Programlama Arayüzü kullanılarak kutuplama gerilimleri DAClar yardımıyla farklı değerlere ayarlanabilmekte, zamanlama sinyalleri farklı çalışma modlarına ve hızlarına uyum sağlayacak şekilde programlanabilmektedir. Devrenin serimi 180 nm süreci ile çizilmiş ve 3.15 mm × 3.15 mm boyutlarındaki örnek tümleşik devre üretime yollanmıştır

Anahtar kelimeler: CMOS Görüntü Algılayıcı, Atım Gürültüsü, Analog/Sayısal Çevirici, Kolon Seviyesi Analog/Sayısal Çevirici, İki Adımlı-Sabit Eğimli Analog/Sayısal Çevirici

To My Family

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

Noteworthy improvements on optics and solid state electronic technologies have enabled image sensors to experience an immense advancement. Consequently, image sensors found themselves widespread areas of usage and an ever-demanding market. Mobile imaging, digital still and video cameras, camcorders, biometrics, and surveillance systems can be count among them [1].

The invention of the first transistor stimulated the semiconductor industry, which in turn allowed process of substitution of analog film based cameras with the solid-state image sensors. Charge Coupled Devices (CCD) and Complementary Metal Oxide Semiconductor (CMOS) image sensors have been the dominant classes of semiconductor based image sensor devices.

These two types of image sensors have both their advantages and disadvantages, but in the 1970's, the picture was not this blurry. CCD's, from their invention at 1971, has outweighed CMOS image sensors owing to their higher light sensitivity, larger dynamic range, smaller pixel pitch, and lower spatial variation. However, the continuous improvement on the CMOS technology has created number of advantages for the CMOS image sensors and starting from the early 1990's, they have been started to be considered as a possible choice along with the CCD's [2]. From that time until today, CMOS image sensors has gained a large share of the market but was not able eliminate CCD completely because of the reasons that are listed on Table 1.1.

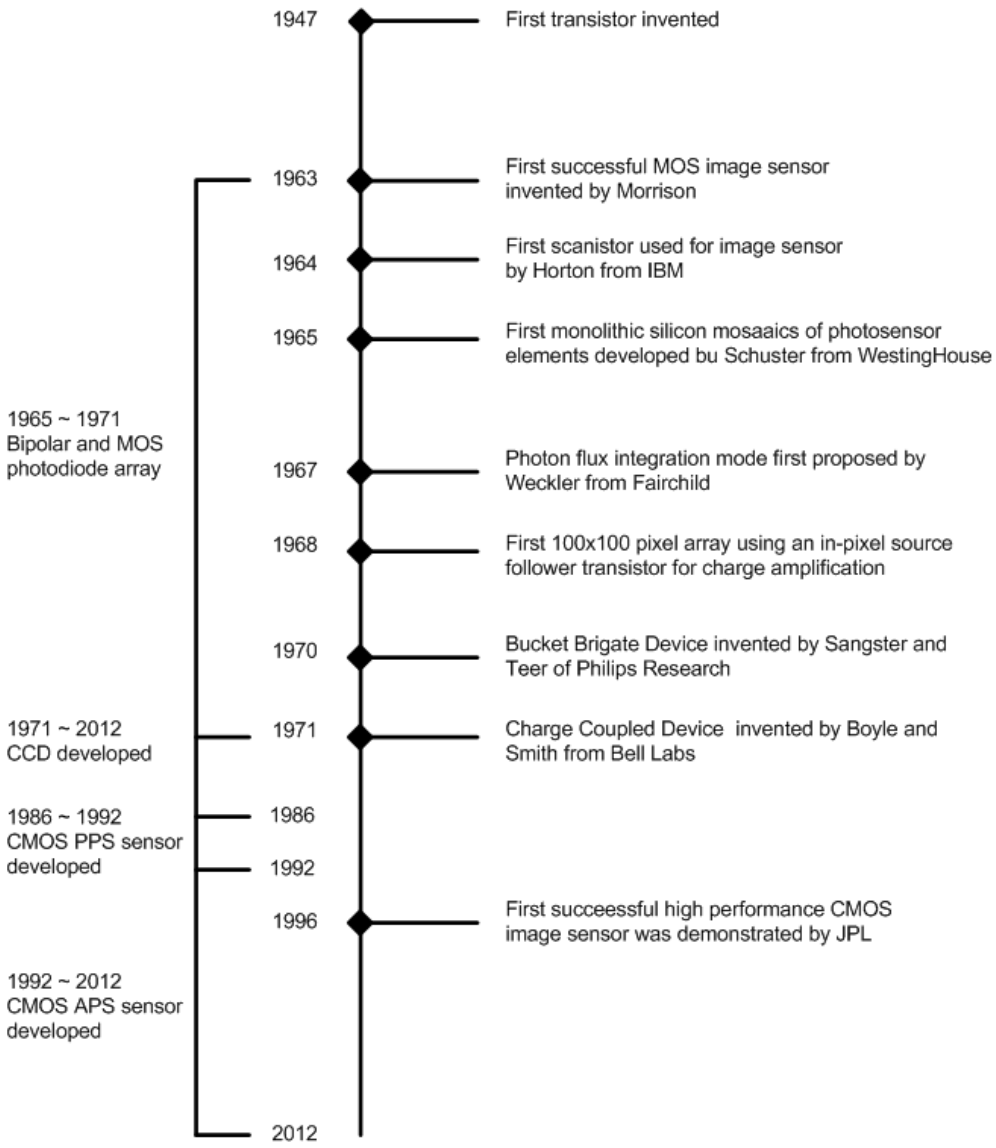

Figure 1.1 Development of Semiconductor Based Image Sensors [3].

Figure 1.1 lays out the achievements during the development process of image sensors over years. From the invention of transistor on 1947, continuous progress including the invention CCD's and simple CMOS image sensors led to today's high quality cameras.

Table 1.1 Advantages of CCD and CMOS image sensors [2].

Advantages of CMOS Imagers	**Advantages of CDD's**
Low Power Consumption	Lower Noise and Dark Current
Low Cost	Smaller Pixel Size
Integration Capability and Compatibility with Standard CMOS Technology	%100 Fill Factor
High Frame Rates	Higher Sensitivity

In order to improve the advantages and reduce the effects of disadvantages of the CMOS image sensors, continuous research have been going on. One of the challenges encountered during this development process is keeping frame rates constant or, in some cases, even faster while the array sizes getting larger. Conventional serial readout schemes, in which each pixel is read one by one in a sequential manner, became burdensome to design and fell short of achieving desired speed. Employing column parallel analog to digital converters, in which readout of each column in the array is made simultaneously, made it possible to overcome speed limitations. In these implementations, among various alternatives offered in the literature, two-step single-slope ADC architecture stands as a suitable choice with its low power consumption, small silicon area requirement, moderate conversion speed, and resolution.

1.1 Scope and Motivation of This Thesis

In the opening of this section, historical background and status of the CMOS image sensors has been depicted. Research on the pixel part of the imager is focused on shrinking the pixel size, reducing the pixel noise, boosting the dynamic range, and increasing the fill factor and the light sensitivity. Alongside these, numerous other development on the peripherals of the CMOS imagers are in progress.

Performing analog to digital conversion on chip can be considered as one of the main exploration areas for the improvement of the performance of the CMOS image sensor. The reasons for converting image sensor output (which is analog in nature) in to digital domain on the same die are plenty. Firstly, digital outputs are less sensitive to noise in the peripheral domain. Secondly, an image sensor with a digital output can be directly

combined with the rest of the system blocks in a camera. Another appealing trait of having digital output on the image sensor is increased output bandwidth of the sensor chip [4].

In this thesis, various data converter architectures that can be utilized on a CMOS image sensor for a column-parallel readout scheme are investigated, in order to choose the best possible architecture. A new design based on this selection is presented and implemented. The phases of the development presented here can be listed as follows:

- The literature review to determine the preference among various alternatives and set preliminary requirements
- Exploring the strengths and weaknesses of the chosen architecture and work on improving them
- Design of a prototype analog to digital converter circuitry alongside with the communication interface, biasing, and timing control signal generation blocks.

1.2 Design Overview

In this work, design of a column level Two-Step Multi-Slope analog to digital converter is presented. Prototype design is carried out using 0.18 μm process node and the fabrication is still in progress.

As will be detailed later in this text, column parallel analog to digital conversion scheme makes it possible to reach high frame rates for imager arrays with sizes reaching to megapixels and beyond, without drastically increasing the sampling rate of the analog to digital conversion. Therefore, analog to digital conversion is handled in the column level.

Popular analog to digital converter architectures employed in CMOS image sensors are listed on Table 1.2 with their advantages and drawbacks. Detailed descriptions of these ADC structures are provided on Section 2.4.

Table 1.2 Different ADC Architectures and Their Features.

ADC Architecture	Conversion Speed	Layout Area	Resolution	Power	Implementation Level
Integrating	Low	Low	Medium	Low	Pixel – Column
SAR	High	High	Medium	Low	Column – Chip
Σ-Δ	Medium	Medium	High	Medium	Chip
Cyclic	High	Medium	Medium	Medium	Column
Pipeline	High	High	High	High	Chip

Among the alternative architectures for the column-level analog to digital conversion listed in Table 1.2, Successive Approximation Register ADC has a large capacitive DAC to provide a reference voltage for the comparison. This DAC structure contains extensive number of unit-cell capacitances and an amplifier alongside with a comparator and a memory structure. Placing these elements within a column elongates the column height considerably. Cyclic ADC is another analog to digital conversion architecture suitable for implementation in column level. Instead of employing a DAC structure as it was the case for SAR ADCs, this architecture contains an accurate multiplier to multiply the residual voltage between the fixed reference voltage and the analog input by 2. This accuracy on the multiplier structure calls for high gain for amplifier used in multiplier. Required high gain comes with the increased power consumption and layout area for the amplifier. Integrating ADC on the other hand, has the smallest area occupation since it has only a comparator and a memory block within a column. Power consumption is also smaller compared to other architectures as the adoption of other mentioned blocks used in SAR and cyclic ADCs are omitted.

However, as it can be inferred from Table 1.2 conversion speed of the Integrating ADC is slower compared to other architectures. In order to improve the sampling rate of the Integrating ADC, a new variant which is referred as Two- Step Single-Slope ADC structure is used. This method speeds up the conversion of the Integrating ADCs by dividing the conversion into coarse and fine conversion phases. Detailed explanation of the Two-Step Integrating ADC is provided within Chapter 3.

Moreover, to decrease the conversion rate and the power consumption of the Two-Step Integrating ADCs further, companding method suggested in [5] is introduced into Two-Step Integrating ADC and Two-Step Multi-Slope ADC is obtained. This method includes decreasing the resolution of the conversion for highly illuminated pixel outputs, since the quantization noise of the ADC is considerably small, compared to the short noise generated by those pixels. Multi-Slope feature is obtained with generation of fine ramps with varying slopes, corresponding to decreasing resolutions offered for increasing illumination levels of CMOS image sensor pixels.

1.3 Thesis Organization

The content of this thesis is divided into 7 chapters. Next chapter (Chapter 2) focuses on the literature review for the CMOS image sensors and the peripheral electronic on the imager chips. Within this chapter, starting with the background for the CMOS image sensors, readout methods, noise sources, and analog to digital converter (ADC) structures are presented. Finally, ADC performance evaluation parameters and requirements for the ADC presented in this work are explained.

On Chapter 3, information on the operation of Two-Step Multi-Slope (TSMS) ADC is presented, alongside with the alternative design approaches of the functional blocks required for the implementation of TSMS ADC.

Chapter 4 presents the detailed design and block level simulation results of the functional blocks employed in the designed ADC.

Physical implementation of the designed ADC is illustrated on Chapter 5.

On Chapter 6, various top-level simulation results for the evaluation of the designed ADC is presented.

On the 7th and last chapter, conclusions are drawn and future work is laid out.

CHAPTER II

LITERATURE REVIEW

This chapter is concentrated on providing the necessary background about CMOS image sensors, readout architectures, and analog to digital converters. In section 2.1, photo detection operation is explained and several essential pixel architectures are presented. Section 2.2 compares analog and digital ROIC architectures. In section 2.3 different ADC placement topologies are evaluated. Section 2.4 provides information about ADC architectures that can be used as column parallel and their comparison.

2.1 CMOS Image Sensors Background

2.1.1 Optical Absorption and Photo Conversion

Energy of a photon is described by the Plank's law which is provided below.

$$E_{photon} = hv = \frac{hc}{\lambda}, \tag{2.1}$$

where h is the Planck's constant, c is the speed of light, and λ is wavelength of light.

When a photon is incident on a semiconductor, if the photons energy is larger than the semiconductor's bandgap energy, it is absorbed by the semiconductor and electron hole pairs are created. Elsewise that semiconductor is transparent to that photon.

Focusing on the silicon, the substrate material for the CMOS image sensors, photons with energy larger than the silicon's bandgap energy of 1.1 eV are absorbed within a vicinity of dx, which is proportional to the intensity of the photon flux Φ(x) and α is the silicon's absorption coefficient.

$$\frac{d\phi(x)}{dx} = -\alpha\Phi(x). \tag{2.2}$$

When solved with the boundary condition $\Phi(x = 0) = \Phi_0$, this equation yields the result provided below:

$$\Phi(x) = \Phi_0 \exp(-\alpha x). \tag{2.3}$$

So, the intensity of the photon flux lessens exponentially as the distance from the surface gets larger. Silicon absorbs the photons with the wavelength shorter than 1100 nm and transparent to those with wavelengths larger than 1100 nm [6].

In the CMOS image sensors, widely employed photodetector type is the reverse biased photodiode illustrated in Figure 2.1, where n-type region is initially reset to a positive supply voltage then left floating, and p-type region is constantly driven to the ground voltage. While the reverse bias conditions still apply, photo generated electrons are accumulated on the n-type region whereas the holes are drawn to the p- type grounded region. Accumulation of electrons of the n-type region reduces the potential of that node. At the end of the exposure time, the voltage of the n-type region is read out and that node is reset to a positive supply voltage again.

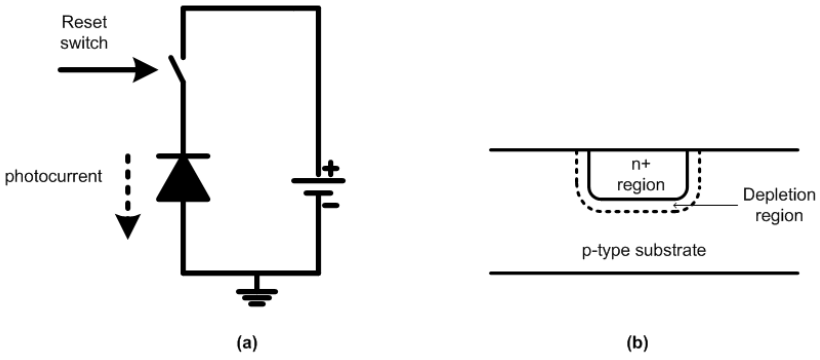

Figure 2.1 Reverse Biased Photodiode (a) Simple Schematic Diagram (b) Cross Sectional View of Photodiode.

2.1.2 Pixel Structures

It is beneficial to be familiar with the pixel structures employed in image sensors, as the work presented here will be used alongside CMOS image sensors. This section aims to present the basics of several prevalent pixel architectures.

A CMOS image sensor pixel can be considered as a circuitry composed of a photodiode, reset switch, and other optional elements, such as amplifiers and output stages. These pixel architectures can be classified based on the following criteria:

- Photodiode type: n-well or n+ diode, buried photodiode, photogate, and pinned photodiode
- Accumulation capacitance type: junction capacitance of the photodiode in the 3-transistor pixels, feedback capacitor in the capacitive trans-impedance amplifier pixels, and floating diffusion in the pinned photodiode pixels[7]
- Active or passive pixels [8].

Before delving into the pixel architectures, important pixel design specifications and parameters are presented below, as they are used for the evaluation of the performance.

- **The fill factor (FF)** can be defined as the ratio of the photosensitive area to the overall pixel area.

$$FF = \frac{A_{ps}}{A_{pix}} \times 100 \ [\%], \tag{2.4}$$

  where A_{ps} and the A_{pix} are the photosensitive area and pixel area respectively. It should be noted that, as circuit elements (e.g. transistors) and wiring is added to the pixel to improve performance, fill factor drops because of the limited remaining area to implement the photodiode.

- **The full well capacity (FWC)** can be described as the maximum amount of charge that can be stored in the pixel in terms of electrons. The equation governing the value of full well capacity can be given as follows.

$$FWC = \frac{1}{q}\int_{V_{RST}}^{V_{PD(min)}} C_{PD}(V_{PD})dV \ \ [e^{-}], \tag{2.5}$$

  where q is the charge of a single electron, V_{RST} is the reset voltage of the photodiode, $V_{PD(min)}$ is the photo diode voltage at its full swing, and C_{PD} is the capacitance of the photodiode.

- **The quantum efficiency (QE)** is the ratio of the number of photo generated electron hole pairs to the total number of incident photons. This can be expressed with the equation below.

$$QE(\lambda) = \frac{N_{sig}(\lambda)}{N_{ph}(\lambda)}, \tag{2.6}$$

where $N_{sig}(\lambda)$ and $N_{ph}(\lambda)$ are the signal charge and the number of incident photons respectively. It should be noted that these parameters have spectral dependence and change with the wavelength of the incoming photons.

- **The dynamic range (DR)** is expressed as the ratio of the maximum achievable signal and the total read noise in terms of decibels. It is represented by

$$DR = 20\ log \frac{N_{sat}}{n_{read}}\ [dB], \tag{2.7}$$

where N_{sat} is the full well capacity and n_{read} is the pixel noise without illumination.

- **The signal to noise ratio (SNR)** is described as a ratio between the RMS input signal (N_{sig}) and the RMS noise (n), at a specific input level. SNR is expressed as follows:

$$SNR = 20\ log \frac{N_{sig}}{n}\ [dB]. \tag{2.8}$$

As indicated in Figure 2.2, the SNR value increases linearly with increasing signal amplitude at low signal levels, where the total pixel noise is dominated by the reset and the readout noise components. However, as the signal magnitude gets larger, shot noise dominates the overall noise and the SNR equation acquires square root relation form.

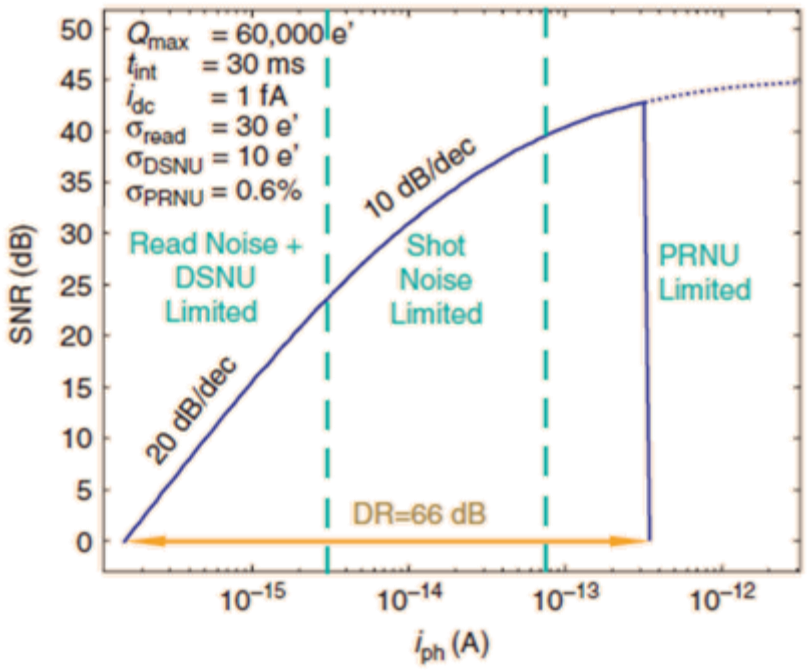

Figure 2.2 SNR versus Photo-Generated Current [1].

- **The conversion gain** is the property that determines how much potential difference will be obtained per accumulated electron.

$$CG = \frac{q}{C_{PD}} \left[\frac{\mu V}{e^-}\right], \tag{2.9}$$

where q is the charge of a single electron (1.602 x 10^{-19} Coulombs) and C_{PD} is the pixel charge storage capacitance [3],[6],[7].

In the following part of this section, several pixel types are explained.

2.1.2.1 Passive Pixel Architecture (PPS)

Passive pixels are the most primal pixel architecture, existing since the invention of the first CMOS image sensors. They involve a photodiode and a select transistor acting as a switch, as illustrated in Figure 2.3. Operation of the passive pixel sensors can be described as follows:

- The select transistor is activated at the beginning of the read-out cycle and photodiode is reverse biased to a high voltage through the column bus.

- Then the select transistor is disabled and the n+ node of the photodiode is left floating. Accumulation of charges in the n+ node pulls the potential of this node to a lower value.
- Following step is to measure the potential on the n+ node and calculate the difference from the original value.
- The last step is to reset the photodiode to start the next exposure cycle [8],[9].

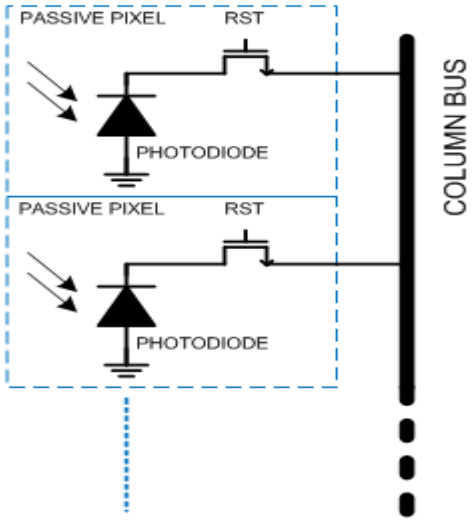

Figure 2.3 Schematic Diagram of Passive Pixel.

Passive pixel structure offers the highest fill factor for any pixel size. On the other hand, it suffers from large readout noise. Another drawback of this architecture is the lack of ability to achieve fast frame rates and support for large array sizes, since the column bus capacitance distorts the signal accumulated on the pixel capacitance [8], [9].

2.1.2.2 3-Transistor Active Pixel Architecture (3T-APS)

A possible improvement for the passive pixel architecture is to insert a buffer amplifier to improve the operational parameters. A source-follower amplifier with its gate connected to the n-side of the photodiode, as seen in Figure 2.4, can act as a buffer. This way the accumulation node is isolated from the large bus capacitance, solving the destructive readout and noise issues [3], [9].

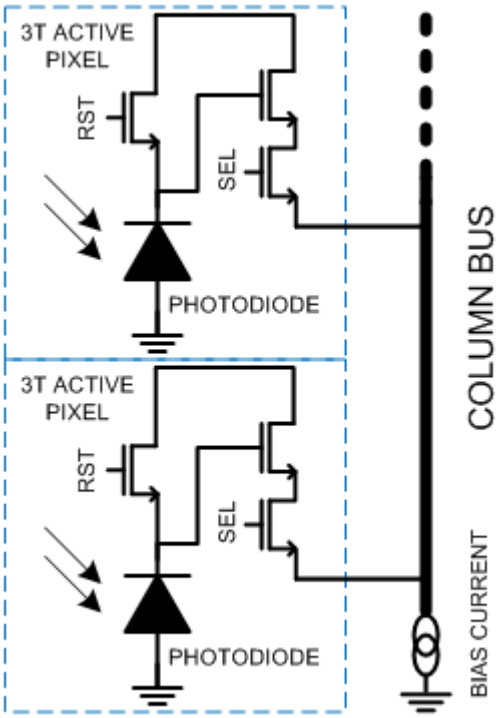

Figure 2.4 Schematic Diagram of 3-T Active Pixel.

The working principle of the Transistor Active Pixel Architecture (also known as the 3-T active pixel sensor due to employing three transistors) is very similar with the PPS and can be described as follows:

- The photodiode is reset to a high voltage at the beginning of the exposure cycle.
- As it was the case for PPS, photo-generated electrons pull the voltage of the n+ node to a lower value.
- When it is time to read the accumulated signal, the pixel is selected and the photodiode voltage is read-out via the source-follower transistor.
- The last step is to reset the photodiode to start the next exposure cycle [8], [9].

This type of pixel architecture solves numerous noise issues. However, it is still prone to kT/C noise and Fixed Pattern Noise caused by the threshold variations of source follower transistors due to manufacturing mismatches. Moreover, the fill factor and consequently the quantum efficiency is decreased because of the limited area to implement the photodetector after the placement of additional transistors and routing [7]–[9].

2.1.2.3 Photogate and Pinned Photodiode APS (4T-APS)

Photogate and Pinned Photodiode Active Pixel Sensors, also referred as the four transistor active pixel sensors (4T-APS), exploit the CCD's appealing traits (integration and transport of charges). As it can be seen from Figure 2.5, the circuitry managing the reset and read-out operations are identical to the 3T-APS. Photo conversion takes place at the photodiode or under the photogate.

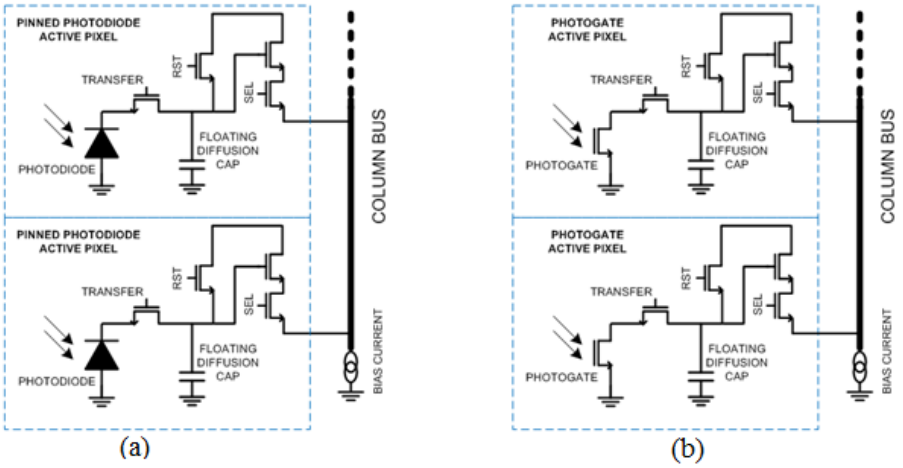

Figure 2.5 Schematic Diagrams of Pinned Photodiode Pixel (a) and Photogate Pixel (b)

Operation steps of 4T-APS is provided below:

- At the start of the exposure cycle, readout node (floating diffusion capacitance) is reset and a measurement is made.
- Then the photo conversion is done and the charge is transferred to the readout node through the transfer gate.
- Voltage at the readout node is read again and Correlated Double Sampling is performed by subtracting the measurements from each other.

There are very appealing qualities of this type of pixel architecture, such as suitability to implement Correlated Double Sampling to reduce threshold variations and low frequency and kT/C noise components. 4-T APS also provides larger full well capacity and improved light sensitivity [7]–[9].

2.2 Readout Architectures and Methods

This section is intended to provide a brief information about the readout architectures of the CMOS image sensors, as the selection of the architecture plays a crucial role on the metrics of the Analog to Digital Converter to be designed. The issues that will be covered in this section are shutter modes, timing of the CMOS image sensors, and the readout parallelism.

2.2.1 Shutter Modes

As mentioned during the introduction of the basic pixel architectures, image is acquired in a time interval, which is called exposure or integration time. The photo-generated electrons accumulated in this time window are read out using a method appropriate to the pixel type employed. Moreover, all CMOS image sensors uses either one of the two main types of shutter modes to control their exposure time, rolling or global (or snapshot) shutter. Following subsections present timing diagrams and basic information about these two shutter modes.

2.2.1.1 Rolling Shutter

When operating in the rolling shutter mode, pixels belonging to one row are reset at the same time. After a delay time, known as the exposure time, read-out phase of the pixels begins. Consecutive rows follow the same pattern with a constant predefined time lag, as demonstrated in Figure 2.6.

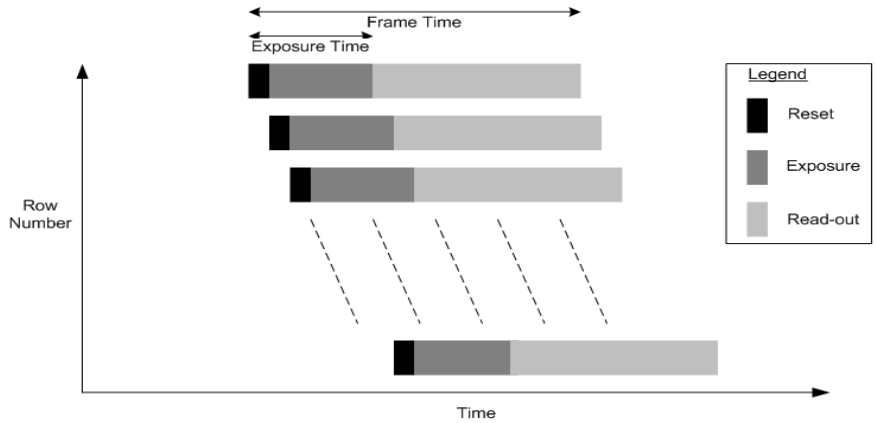

Figure 2.6 Timing Diagram of Rolling Shutter Mode [3]

Rolling shutter timing scheme is very easy to implement and very high frame rates are obtainable. However, since charges are integrated during different time intervals for different rows, image can be distorted if the imager or the object is moving fast (a speed comparable to the shutter speed).

Figure 2.7 Illustration of Moving Effect While Using Rolling Shutter [10]

Figure 2.7 is a picture taken from a fast-moving vehicle using a digital camera employing rolling shutter mode. As can be seen from the figure, the rails, which are supposed to be straight, appear to be inclined from top-left to the bottom-right. This indicates that, readout of pixels begins from the top row to the bottom for this specific imager.

2.2.1.2 Snapshot (Global) Shutter

In the global shutter mode, all pixels in the array are reset at the same time and they accumulate charges simultaneously. After the end of exposure time, generated signal in the pixel photodiodes are sampled and hold and read out sequentially row-by-row. Global shutter helps to remove undesired effects caused by the rolling shutter in the expense of frame speed. Timing diagram presented in Figure 2.8 represents readout phases for different rows included in a CMOS image sensor employing Global Shutter.

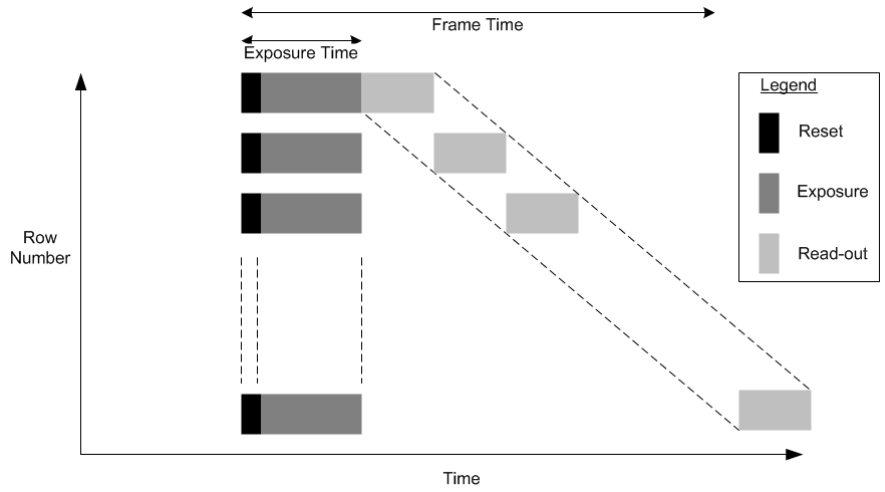

Figure 2.8 Timing Diagram of Global Shutter Mode [3]

2.2.2 Chip Architectures

Alongside with the imaging core composed of pixels, digital CMOS image sensors contain numerous peripheral electronic circuitries that handle on-chip signal processing. These peripheral blocks include:

- Bias generators
- Row decoders and column multiplexers
- Column amplifiers
- Analog to digital converters
- External communication interfaces (e.g. Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C), etc.)
- Serial output interfaces (e.g. Low Voltage Differential Signaling (LVDS)).

Figure 2.9 depicts possible placements of the above-mentioned CMOS image sensor blocks on a chip. Note that column-parallel analog to digital conversion is employed in the architecture shown in Figure 2.9.

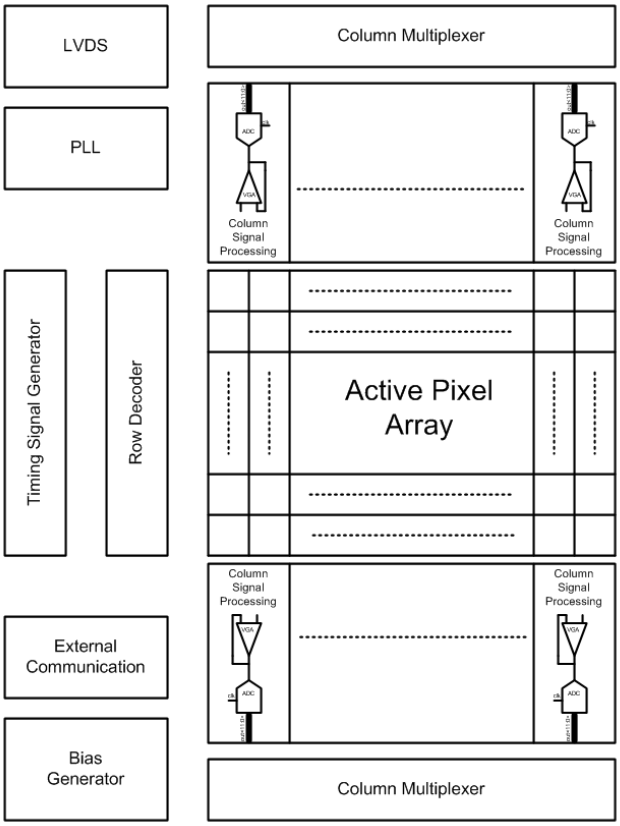

Figure 2.9 Image Sensor Chip Architecture Diagram.

After the image data is generated at the pixels, regardless of the type of the shutter mode employed, a row is addressed and the pixel outputs belonging to that specific row is fed to the column signal processing circuits. In the following step, assuming that analog to digital converters are placed in the columns, the signal processed in the column amplifiers are fed to the ADCs and converted into the digital domain. Next, the ADC outputs at the parallel columns are selected one-by-one by the column multiplexers and fed to the LVDS blocks. LVDS blocks transfer the data out of the chip. This architecture requires individual ADCs connected to each column in the imager.

In the serial analog to digital conversion scheme, the analog data at the output of the column amplifiers will be multiplexed and fed to a single serial analog to digital converter. Then digital ADC output will be transferred off-chip by the LVDS drivers.

Upcoming sub-section presents a discussion about the read-out parallelism, (i.e. at which stage to implement the analog to digital converters) and investigates this topic in terms of power and data rate.

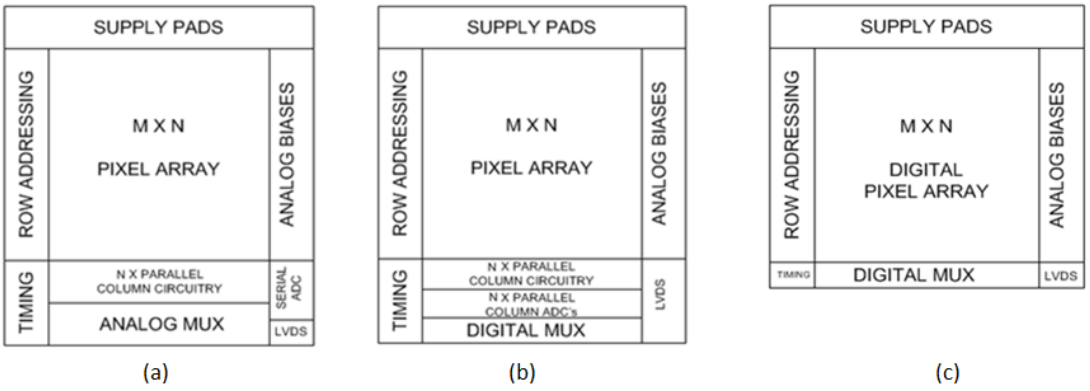

Figure 2.10 Serial (a), Column-Parallel (b), and Pixel-Parallel (c) Conversion Architectures [4].

2.2.2.1 Serial Analog to Digital Conversion

Serial ADC architecture incorporates the usage of single chip-level ADC, as shown in Figure 2.10(a), where outputs of all the pixels in the array are converted into the digital domain by this single ADC in a frame time. This architecture requires fastest speed ADC architectures where the sample rate of the ADC should be:

$$SR_{ADC} = f_{frame} \times N_{row} \times N_{column}, \quad (2.10)$$

where f_{frame} is the frame read-out speed, and N_{row} and N_{column} are the number of rows and columns in the array respectively [6],[11].

Employing serial analog to digital conversion can be beneficial in several ways. Firstly, ability to place converter circuitry away from the pixel array can reduce the substrate injected noise affecting the pixels. Another asset worth mentioning is that implementing serial conversion scheme allows the developer to use third party silicon intellectual properties of ADC's which in turn reduces the time spent for overall design. On the other hand, extreme data-rate required for this approach is a serious drawback. With today's standards on array sizes, which is usually in the order of tens of megapixels, it is nearly impossible to employ this method and still meet speed requirements [4],[12].

2.2.2.2 Column-Parallel Analog to Digital Conversion

Column-parallel analog to digital conversion scheme uses a dedicated ADC for column. An implementation example of column parallel ADCs is demonstrated in Figure 2.10(b). This approach has medium amount of simultaneity and thousands of ADC's working at the same time in parallel relaxes the data rate requirements. Sampling rate requirements of this analog to digital conversion method is given as:

$$SR_{ADC} = f_{frame} \times N_{row}, \tag{2.11}$$

where the frame read-out speed and number of rows terms are represented by f_{frame} and N_{row}. This conversion scheme is widely used due to its lower power consumption and moderate data rate requirements. One of the major handicap of using the column parallel ADCs is the area limitation imposed on the ADC designs. It is obvious that, the layout of the ADC should fit perfectly with the column width, preventing the usage of ADC architectures are with large area requirements. An improvement over this is achieved by placing ADCs both on the bottom and the top of the array in the two-pixel pitch. This structure is also advised in order to evenly distribute the heat generation to avoid current shading [11]. Another problem to be addressed in these architectures is the possible cross-talk between the columns. However there are ways to address these and perfectly operating designs are available in the literature [4].

2.2.2.3 Pixel-Parallel Analog to Digital Conversion

Pixel parallel conversion method involves placement of an ADC per pixel, as depicted in Figure 2.10 (c). This scheme relieves the constraints on conversion rate by employing very large amount of parallel signal processing. Sampling rate regulation for this design type is provided by the equation (2.12) and equivalent with the frame rate.

$$SR_{ADC} = f_{frame}. \tag{2.12}$$

This conversion method has become popular in recent years, however, power consumption values being considerably large compared to column-parallel counterpart and area restrictions affecting both the architecture selection and devices sizes, make this design less preferable.

2.3 Noise Sources in CMOS Image Sensors

Noise is a principal issue when designing both the image sensor pixels and peripheral signal processing blocks, as it is closely related to the quality of the output image. It degrades the system performance and limits the signal to noise ratio, i.e. the sensitivity.

Noise in the image sensor circuitry can be divided into 2 main categories, which are temporal and spatial noise sources. Temporal noise is caused by the arbitrary movements of the carriers inside the semiconductor and dependent on time, i.e. may vary from frame to frame. Spatial noise represents itself as the offset and gain variations from pixel to pixel and originates from the mismatches during production. This type of non-ideality is time independent and present even under no illumination [1].

Following part of this section aims to demonstrate the types of both the temporal and the spatial noise sources.

2.3.1 Types of Temporal Noise Sources

2.3.1.1 Thermal (Johnson) Noise

The thermal noise is caused by the random motion of the electrons inside a resistor or a conducting medium due to thermal effects. The power spectral density equation of the thermal noise is provided below:

$$V_{n_{th}}^2(f) = 4kTR \ \left[{V^2}/{Hz}\right], \tag{2.13}$$

where k is the Boltzmann's constant = 13.8 x 10^{-24} Joules/Kelvin, T is temperature in Kelvin, and R is the resistance in Ohms. Notice that there is no spectral dependence of thermal noise, i.e. it is constant for all frequencies. Thermal noise is generally modeled as a voltage source in series with an ideal resistor or a current source in parallel with an ideal resistor as demonstrated in Figure 2.11.

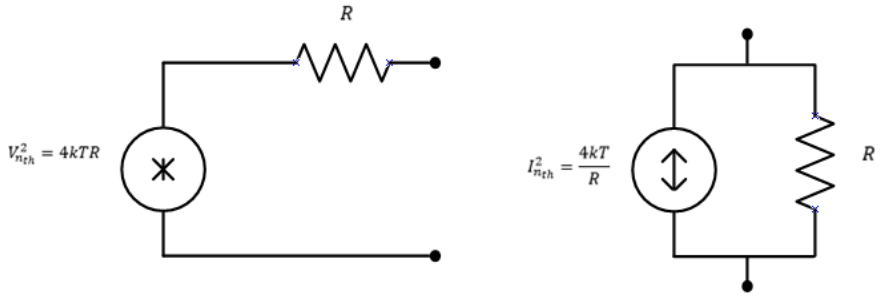

Figure 2.11 Equivalent Thermal Noise Model Circuit.

2.3.1.2 Flicker (1/f) Noise

Flicker noise is a low frequency noise component and as its name suggests, its power spectral density decreases with increasing frequency. The source of this noise is not completely understood, but its approximation for its PSD is given as

$$V_{n_{fl}}^2(f) = \frac{k_v^2}{f} \quad \left[V^2/_{Hz}\right], \tag{2.14}$$

where k_v is a constant. This noise can be significantly reduced by using Correlated Double Sampling [13].

2.3.1.3 Shot Noise

Shot noise is a dominating degrading factor for the performance of most CMOS image sensors. It is generated during the passage of carriers over the potential barriers build by p-n junctions. This is an unavoidable non-ideality for CMOS image sensors, as the core of the imaging is built on the p-n junction photodiodes. Photon shot noise can be described by the following equation:

$$n_{n_{sh}} = \sqrt{N_e} \ [e^-], \tag{2.15}$$

where N_e is the total number of accumulated electrons. Photon shot noise is the determining factor for the Signal-to Noise Ratio of the CMOS image sensors over a certain signal value [9]. In the shot noise dominated regime, maximum achievable SNR can be expressed as:

$$SNR_{MAX} = \frac{N_e}{n_n} = \frac{N_e}{\sqrt{N_e}} = \sqrt{N_e}. \tag{2.16}$$

As mentioned in the introductory chapter, pixel sizes are continuously getting smaller imposing a limiting factor on the full well capacity of the sensor. Provided in the numerous articles [14]–[16],maximum number of electrons that can be integrated on a single pixel is in the order of several tens of thousands. Assuming an exaggerated number of 100.000, the SNR is limited to 50 dB, much lower than the maximum attainable SNR of a 12-bit ADC (which is approximately 74 dB). In the light of this fact, it can be said that ADC resolution can be reduced to a lower value and the signal will not be degraded. Thus the conversion speed and power consumption can be improved in the cost of the resolution [5], [17]. This point will be revisited on the design related chapter of this thesis.

2.3.1.4 kT/C (Reset) Noise

Ideally, capacitors do not introduce any noise source to the circuitry. However, when used in the Switched-Capacitor circuits (i.e. driven via a MOS switch), they integrate the noise created by the other circuit elements. As mentioned in Section 2.1.2, pixel operation yields a step where the pixel capacitance is reset via a MOS switch, thus the reset noise is a serious limiting factor for CMOS image sensor pixels.

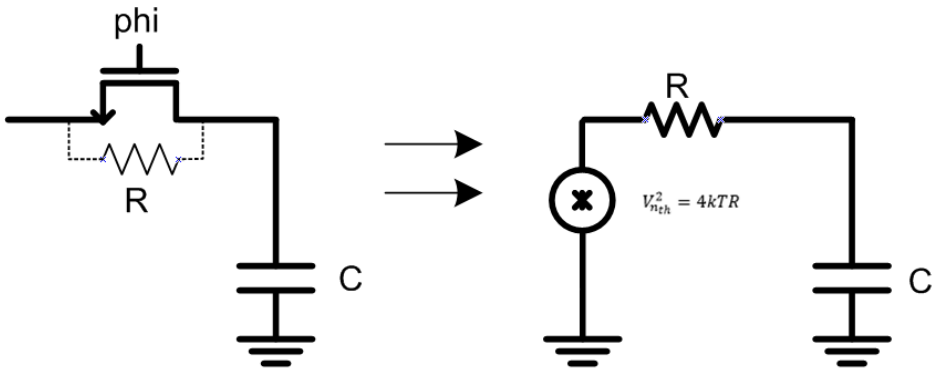

Figure 2.12 Equivalent kT/C Noise Model Circuit.

Figure 2.12 shows the Switched-Capacitor circuit mentioned above. Even though the capacitor is a noise-free element, it integrates the thermal noise generated at the channel of the MOS switch. kT/C term arises from the integration of the thermal noise generated at the channel of the switch transistor, on the capacitor, to a bandwidth determined by the resistance value of the transistor channel and the capacitance value.

$$V_{n_{rst}}^2 = \int_0^\infty 4kT \frac{R}{1+(2\pi fRC)^2} df = \frac{kT}{C} \quad [V^2], \tag{2.17}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin, and the C is the capacitance in Farads.

2.3.2 Types of Spatial Noise

2.3.2.1 Dark Signal Non-Uniformity (DSNU)

Caused by the dark current variations on the photodiodes and the threshold voltage differences of source follower amplifiers, this type of non-uniformity represents itself on the long exposure times and under low illumination. This type of non-uniformity cannot be cancelled using Correlated Double sampling, however external image processing algorithms may reduce the visible effects of this non-ideality.

2.3.2.2 Photo-Response Non-Uniformity (PRNU)

This spatial noise type is related with the gain variations among the pixels or the column readout channels. Applying non-uniformity correction (2 point or above) to the output image on the computer environment can eliminate the effects of photo-response non-uniformity.

2.4 ADC Architectures for CMOS Image Sensors

This section provides the basic information regarding several ADC architectures used in the CMOS image sensors. Each of the analog to digital conversion methods provided below have their desirable traits and drawbacks. These attributes make the ADC architectures mentioned below form an alternative solution for implementation in either pixel or column or chip level (serial).

2.4.1 Flash ADC

Flash ADC is the fastest method of analog to digital conversion and very straightforward to implement. It takes only 1 conversion cycle to convert the analog data into the digital domain. This rapid response comes with a large area and power requirement. Flash analog to digital conversion uses a resistive DAC consisting of 2^N unit resistors placed between high and low reference voltage levels and 2^{N-1}

comparators for making comparison at each reference level, as illustrated in Figure 2.13. Output is provided in the thermometer code form, with comparators having larger ladder voltage than the input voltage giving LOGIC 0 output and the other ones showing LOGIC 1. This thermometer code output is then converted into the binary form using a decoder. Fast conversion speed, large area occupation, and high power requirement of this architecture makes this ADC type an alternative for serial conversion [4].

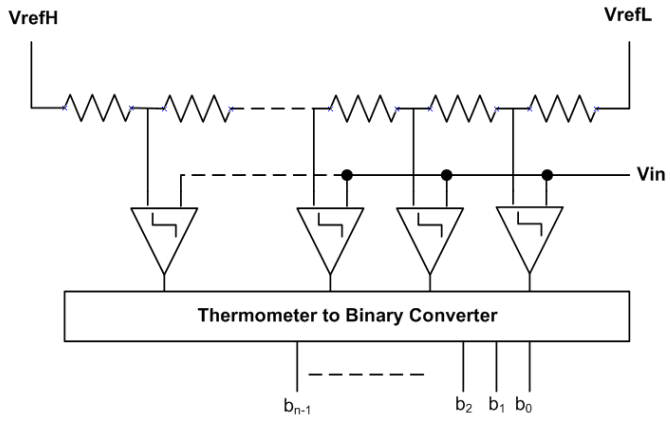

Figure 2.13 Generic Flash ADC Diagram.

2.4.2 Successive Approximation ADC

Successive approximation (SAR) analog to digital conversion method is based on using the previous conversion's result to generate the next step's reference voltage. An example SAR ADC operation is illustrated in Figure 2.14(b) for 4-bit. First conversion is performed by comparing mid–scale reference voltage, V_{ref_mid} to the input voltage. If the input signal is larger than V_{ref_mid}, next conversion step is restricted with the upper half of the full-scale conversion range. Otherwise conversion is performed in the lower half. Second conversion is executed by using the mid voltage of either the upper or the lower half scale and this trend continues until the result is achieved. This method typically requires 1 clock cycle to sample the input data and N clock cycles to perform the N-bit conversion.

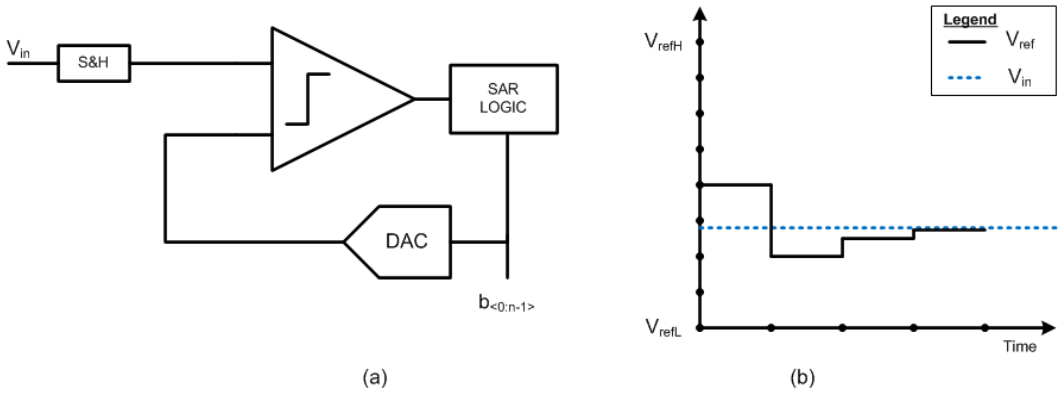

Figure 2.14 Successive Approximation ADC Block Diagram (a) and Example 4-bit Conversion Algorithm [4].

Successive approximation method is a very high-speed ADC suitable for both column parallel or serial conversion, however it requires the design of very precise charge redistribution DACs, shown in Figure 2.14(a), which is hard to implement in column level and consumes significantly high power [18], [19].

2.4.3 Pipeline ADC

Another alternative to realize analog to digital conversion for CMOS image sensors is using a pipeline ADC. This architecture consists of N-sub ranging stages to perform the N-bit conversion and can be considered as having a separate hardware for each iteration of successive approximation method. Figure 2.15(a) shows N-stages of conversion for pipeline ADCs. Operation algorithm can be briefly explained as a comparator determining if the input voltage is lower or higher than the reference voltage, followed by feeding the residual voltage between the input and the reference voltages to the next stage as demonstrated in Figure 2.15(b) [18], [20].

Complexity and fast conversion rate of this architecture, which is comparable to SAR ADCs, makes it a suitable candidate for the serial conversion. However, increasing array sizes demands higher data rates and there are examples on the literature showing successful implementation of pipelining method on column stage [21], [22].

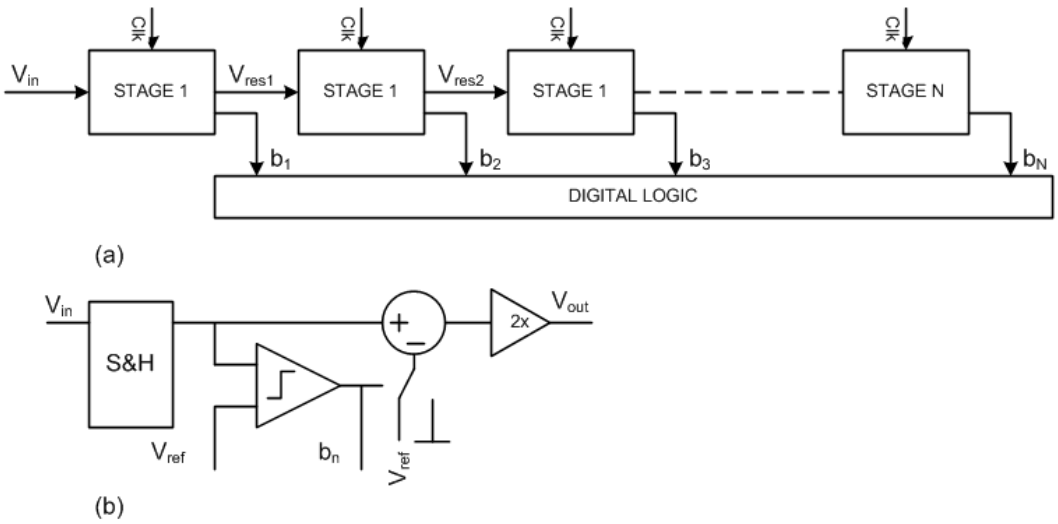

Figure 2.15 Pipeline Architecture (a) and Block Diagram of a Single Pipeline Stage (b) [18], [20].

2.4.4 Cyclic (Algorithmic) ADC

Cyclic ADC's can be interpreted as pipeline ADC's with its stages reduced to only one and feeding the output residual voltage to itself. Because of the large silicon area requirements of charge redistribution DAC inside the SAR ADC's, this architecture keeps the analog reference voltage constant and makes capacitive manipulation of the input voltage.

Figure 2.16 depicts the simplified diagram of the cyclic converter. The input voltage is compared to the mid-voltage of the full-scale range. If the conversion yields the result that input voltage is larger than the reference voltage, the difference between the reference and the input voltages are multiplied by 2 and fed back to the input of the sample- hold stage.

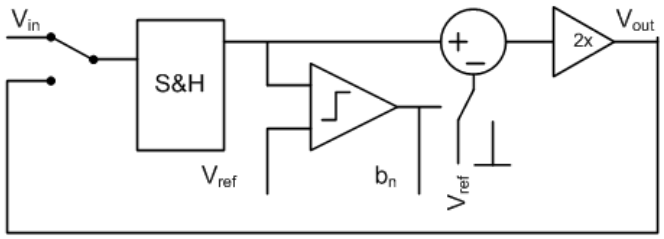

Figure 2.16 Cyclic ADC Block Diagram.

Reduced complexity and lower power requirement of the cyclic conversion method compared to pipeline method makes this architecture attractive solution for column-parallel high frame rate applications.

2.4.5 Sigma-Delta (Σ-Δ) ADC

Sigma Delta ADC's employ oversampling to achieve high signal to noise ratio values, which in turn, enables this architecture to reach high resolutions. Usage of analog functional blocks is limited in this architecture, however, realizing digital signal processing circuitries like digital low pass filters and decimations circuits still demand large silicon area. Furthermore, high speed clock necessity due to high oversampling rates limits the use of this architecture to serial conversion. The literature shows the research progress for implementation on column and pixel level by reducing the power conversion and the circuit complexity [16], [23].

2.4.6 Integrating ADC

Integrating ADC, also called as Single slope ADC's, may be considered as the most compact alternative for CMOS image sensors and thus, it is commonly used. Small area requirement of this architecture makes the implementation possible on both the column-level and the pixel-level. Single Slope ADCs incorporate a global ramp and a counter bus, which is common to all column-parallel ADC's as well as comparators and memory blocks per column, as shown in Figure 2.17. Operating principle of the single slope ADC can be described as follows:

As the analog ramp voltage increases by the amount of 1 LSB per clock cycle simultaneously with the incrementing counter value, ramp voltage is compared with the input in the column level ADCs. When the ramp voltage crosses the input voltage, a decision is made and the counter value is latched on the column memory blocks.

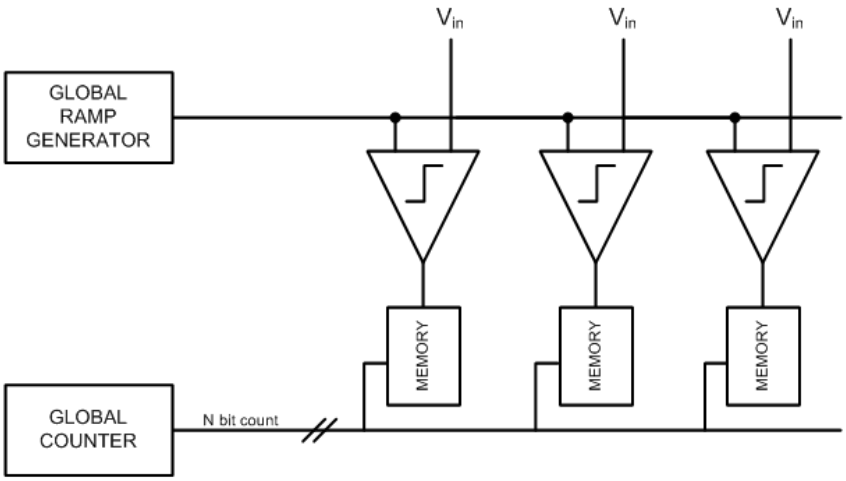

Figure 2.17 Integrating ADC Block Diagram.

Simplicity of design, very low power consumption, and excellent linearity makes this architecture a popular choice. On the other hand, a single slope ADC requires 2^N clock cycles to perform a single conversion, limiting the use of the Integrating ADC to the low frame rate applications.

2.5 ADC Evaluation Parameters

This section presents ADC performance evaluation parameters. Area occupation, power consumption, and sampling rate are important specifications, determining the architecture's feasibility to the application. In addition to these metrics, there are several generic parameters that are used to grade the ADC's performance, no matter what the application area would be. These criteria can be split into two as static and dynamic parameters, representing the converter's linearity and frequency dependent distortive effects.

The Integral Non-Linearity (INL) is a static non-ideality, which represents the deviation of the ADC output from the ideal conversion result. INL value for any possible step of the full range can be described as

$$INL = \frac{A(i) - i \times LSB}{LSB} \; for \; i = 0 : 2^{n-1}, \tag{2.18}$$

where A(i) is the analog signal value for output code moving from i to i+1 and LSB is the quantization step size. Generally INL value is presented as plot in literature,

however there are cases INL is described by a signal number which corresponds to the maximum value on the INL plot [20].

$$INL = max\left|\frac{A(i) - i * LSB}{LSB}\right| \; for\; i = 0{:}\, 2^{n-1}. \tag{2.19}$$

INL causes smooth shading artifacts on the output image. As long as the INL value does not exceed %7 of the full scale range, INL errors can be tolerated by the human eye [4], [12], [20].

The Differential Non-Linearity (DNL) is a static non-ideality, which can be described as the deviation of a quantization stop from the ideal LSB size. The equation for any output value on the full-scale range is given as:

$$DNL = \frac{A(i+1) - A(i)}{LSB} \; for\; i = 0{:}\, 2^{n-1}, \tag{2.20}$$

where A(i+1)-A(i) term represent the amount of increase in the analog input voltage for the output code to increment from i to i+1 and the LSB is the ideal quantization step size. As in INL, DNL can also be given as plot or a single maximum value, which is provided on equation (2.21) [20].

$$DNL = max\left|\frac{A(i+1) - A(i)}{LSB}\right| \; for\; i = 0{:}\, 2^{n-1}. \tag{2.21}$$

A differential non-linearity larger than 1 LSB causes generation of missing codes. DNL directly affects the image quality and considered as more critical compared to INL. Missing codes causes instantaneous jumps in the reconstructed image, which represent itself as sharp transitions.

The Signal to Noise and Distortion Ratio (SNDR) is the ratio of signal power to the RMS of the harmonics components and the noise power. When a time varying input is fed to the ADC, distortive artifact caused from the nonlinearity of the transfer function of the ADC alter the output image performance.

The Effective Number of Bits (ENOB) is the modified representation of the SNDR and shows ADC's non-ideality performance on the resolution level. Mathematical representation of the ENOB value is given as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \ bits. \quad (2.22)$$

The out of range recovery is required for the ADCs used image sensors to recover from the input signals that are above or below the predefined full scale range. Blooming or dead pixels can generate such output values. ADC is expected have out of range recovery circuits and provide an output code corresponding to the inputs outside the conversion limits.

2.6 ADC Design Specifications

On this last section, the ADC performance parameters and design specifications aimed in the work presented in this thesis are given. Table 2.1 lists the design requirements that are set for the design of ADC.

Table 2.1 ADC Design Specifications.

PARAMETER	VALUE	UNIT
Resolution	12	bits
Column Pitch	13.4	μm
Sampling Rate	>50	kS/s
Clock Frequency	10	MHz
Power Consumption	<150	μW
Supply Voltage	3.3 & 1.8	V
Conversion Range	2.9-0.9	V
Process	0.18	μm

Analog to digital converter design within the scope of this study adopts a variation of the Integrating ADCs, the Two-Step Multi Slope ADC architecture, which will be cleared in Chapter 3. Column-level ADC implementation method is followed in order to have a moderate conversion speed. The sampling rate is determined to abide by a readout speed of 50 frames per second on a CMOS image sensor with 1080p vertical resolution. 10 MHz clock speed is sufficient to satisfy this speed requirement. Column-level comparators are designed to be placed both top and bottom sides of the CMOS image sensor array, as demonstrated in Figure 2.9. Therefore, width of each column-level comparator is determined as 13.4 μm.

CHAPTER III

TWO-STEP MULTI-SLOPE ADC

Two –Step Integrating ADCs can be considered as a mid-point between the widely used Single-Slope and SAR architectures. When implementing Single-Slope ADCs, a serious trade-off is made between the conversion speed versus linearity, circuit simplicity, and power consumption. Recalling the sampling speed equation of the Single-Slope ADC from the previous section, conversion time increases exponentially with the ADC resolution. Literature shows several examples that uses very high speed clocks. However, this requires design of complex clock generation circuits with high power consumption [24], [25]. On the other hand, integrating SAR ADC to a column would require a serious area to implement charge redistribution DAC. A hybrid of these architectures, two-step integrating ramp architecture, has been proposed and several application examples are available in the literature [5], [17],[26],[27].

Performing the Two-Step Integrating analog to digital conversion depends on dividing the conversion into two steps: coarse and fine conversion. K-bit coarse and L-bit fine conversion steps provide the result of N=K+L bit ADC. The outline of the operation of the Two-Step Integrating ADC is explained below and an example conversion sequence is illustrated in Figure 3.1.

- In the first step, K-bit coarse conversion is performed using a ladder shaped ramp. When the decision is made, the ramp value is latched into a memory capacitor. Furthermore, the global counter value latched in the digital coarse memory block.

- Secondly the residue between the latched ramp value and the input voltage is compared to the fine ramp in the L-bit fine conversion phase. Likewise, when the decision is made global counter value is latched into the digital fine memory block.
- On the final step, coarse and fine conversion results are superimposed and fed to the output stage.

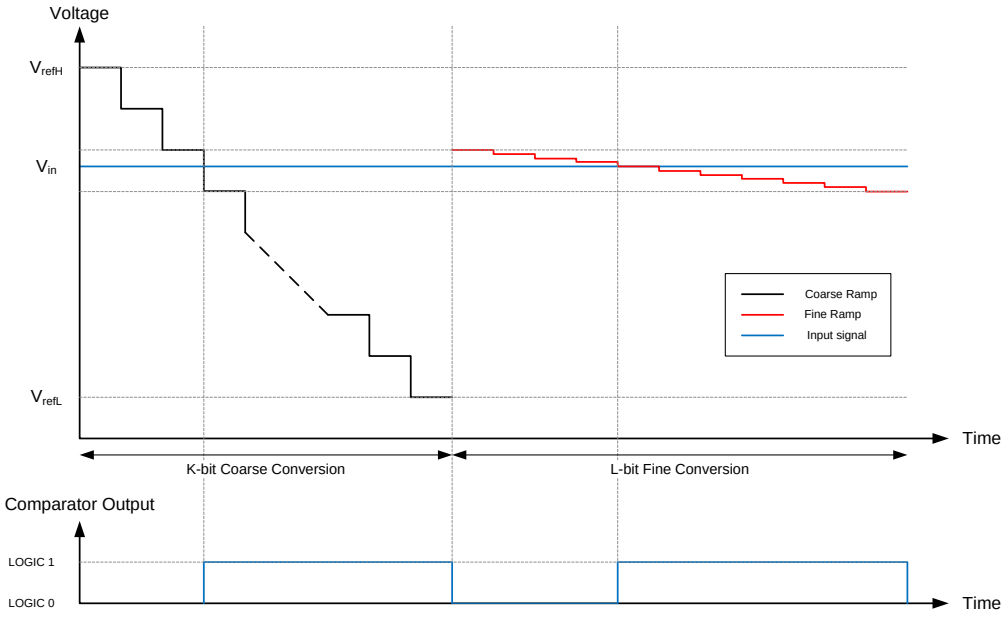

Figure 3.1 Example Ramp Waveforms Depicting the Conversion Algorithm for Two Step Integrating ADCs.

Duration of the Two-Step Integrating analog to digital conversion is only $2^K + 2^L$ steps for N-bit resolution (N=K+L), whereas the conventional Integrating ADC's conversion time for N-bit resolution is 2^N. For 12-bit resolution, up to 32 times faster conversion is achieved using the Two-Step Integrating ADC compared to the Single Slope ADC with K=6 and L=6.

The simplified circuit diagram for the conventional Two-Step Integrating ADC is shown in Figure 3.2. It includes a comparator to compare the pixel generated input signal with the ramp signal, switches for alternating between the coarse and the fine phases, and a hold capacitor to store the final settled coarse ramp voltage belonging to the step at which the toggling at the comparator occur. However, this architecture is problematic due to the parasitic capacitance at the input of the comparator. In the fine

conversion phase, when the bottom plate of the hold capacitor is driven by the fine ramp (Φ_{coarse} = LOGIC 0, Φ_{fine} = LOGIC 1), ramp and the slope of the fine ramp is distorted by the parasitic capacitance present at the input of the comparator. Figure 3.3 portrays the variation of the slope due to the input parasitic capacitor of the comparator.

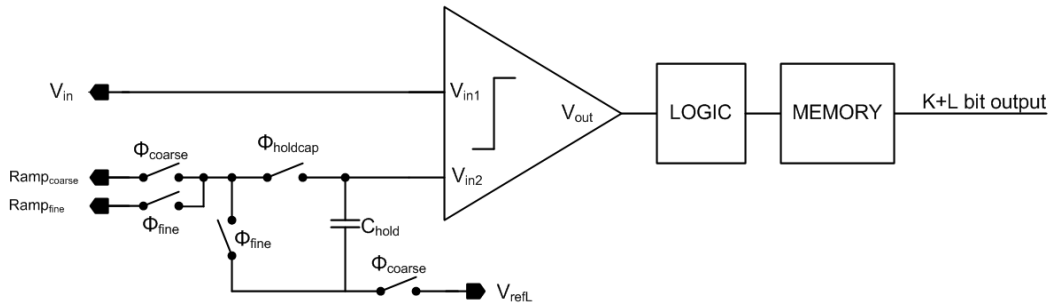

Figure 3.2 Schematic Diagram for Column-Parallel Part of Two-Step Integrating ADC.

Input voltage of the comparator during the fine conversion phase can be given by:

$$V_{in\_comparator} = \frac{C_{hold}}{C_{hold} + C_{par}} \times V_{fine\_ramp}. \quad (3.1)$$

As can be seen from equation (3.1), in order to have the comparator input voltage ($V_{in\_comparator}$) to converge to the fine ramp voltage (V_{fine_ramp}), hold capacitor value (C_{hold}) should be considerably larger than the value of the parasitic capacitance (C_{par}) at that node. However, increasing hold capacitance value makes it harder to drive the coarse ramp voltage.

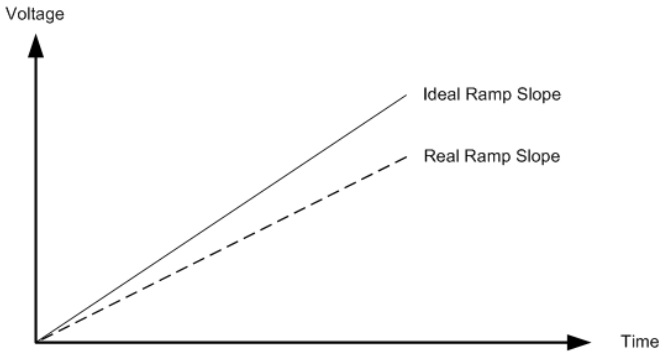

Figure 3.3 Distortion on Fine Ramp by Parasitic Capacitance.

In pursuance of decreasing the non-idealities due to the parasitic capacitances at the input of the comparator, different comparator structures proposed in the literature are explored. In [28], [29] a 4-input comparator is used to reduce the effects of parasitics. As it can be seen from Figure 3.2, bottom plate of the hold capacitor is connected to 0.9 V reference voltage (V_{refL}) and this connection switches to fine ramp signal in the fine conversion phase. It is suggested in [28] that instead of performing this switching, fine ramp and V_{refL} should be connected to their dedicated input terminals on the 4-input comparator. Another approach presented in [29] involves removing the hold capacitance and instead of generating a staircase shaped coarse ramp, feeds outputs of 4-bit resistive ladder to columns. Columns switch between 16 reference voltages created by resistive ladder and instead of storing analog voltage, it uses the latched coarse conversion result to add offset to the fine ramp voltage. This approach is useful as it eliminates the hold capacitance. However, it limits the speed of the conversion.

The ADC designed in this thesis incorporates 4-input comparator scheme incorporating the hold capacitor in order to not to compromise speed. The circuit diagram for the column-parallel implemented part of the Two-Step Multi-Slope ADC is shown in Figure 3.4. 4-input comparator has analog input signal, coarse ramp, reference voltage, and fine ramp input terminals as wells as a logic block that governs the timing of switches implemented on signal paths.

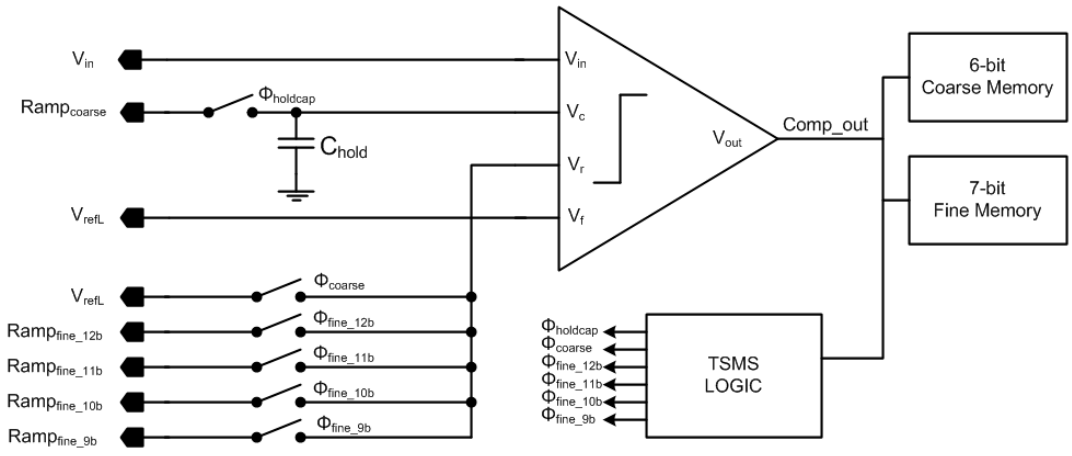

Figure 3.4 Implemented TSMS ADC Schematic Diagram.

At this point, before digging into the block details, it would be beneficial to mention the multi-slope function of the ADC. As mentioned while describing the CMOS image

sensor basics in Section 2.3.1 , sensor's output level increases with the incident light intensity and exposure time, as the full well capacity of the pixel allows. Alongside with the light generated signal of the pixels, there are various noise components associated with the nature of the electronic devices. Except for the shot noise component, other remaining noise sources has no relation with the amount of the incoming light and can be considered constant. Shot noise on the other hand, has a square root relation with the photo-generated electrons in the well and can be described as follows:

$$n_{n_{sh}} = \sqrt{N_e} \ \ [e^-], \tag{3.2}$$

where N_e is the total number of accumulated electrons. As one can deduce, the shot noise component at the pixel output gets very large as the pixel output level increases and poses as the dominating factor on noise.

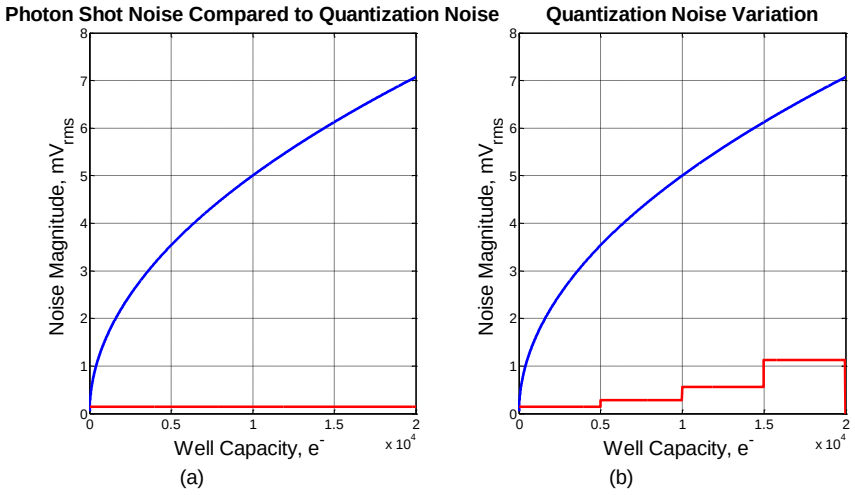

Figure 3.5 Comparison of Quantization Noise of ADC with the Shot Noise Existing at the Pixel Output

Shot noise component for 20.0000 e^- full-well capacity and 50 μv/e^- conversion factor is calculated. Excluding the other noise components, the relation of the shot noise for given parameters and quantization noise can be seen in Figure 3.5. Quantization noise of the designed ADC can be given as:

$$n_q = \frac{V_{LSB}}{\sqrt{12}} = \frac{2/_{2^{12}}}{\sqrt{12}} = 140.95\ \mu V, \tag{3.3}$$

where V_{LSB} is the LSB size of the ADC. As can be understood from the figure on the left, quantization noise is considerably small compared to the shot noise, as it can be seen from Figure 3.5(a). This means that ADC has a better performance than needed, thus quantization noise can be increased by decreasing the resolution and increasing the LSB size, as illustrated in Figure 3.5(b), without affecting the overall system performance. This method known as companding and can be used to reduce the power consumption of the ADC and increase the conversion speed [5], [17].

Companding method is exploited on several works present in the literature as piecewise linear ramps with increasing slopes for Single-Slope ADCs [30], [31]. Another approach was to divide the conversion range of the ADC to 4 or 8, and generate ramps with increasing slopes as the mean value of the divided portion increases. The work presented in this thesis aims to combine the latter approach with the Two-Step Single-Slope ADCs presented in [26]–[28], obtaining higher conversion speed in terms of clock cycles and reduce the power dissipated in one conversion cycle.

To integrate the companding method into the Two-Step Single-Slope ADC architecture, 4 fine conversion ramps is needed instead of only 1. This way, ramps with larger slope will be used to compare the input voltages belonging to higher regimes in the conversion range. The information of the region at which V_{in} belong is going to be excerpted from the most significant 2-bits of the coarse conversion results. Using this data, selection between 4 fine ramps present at the fine ramp input terminal of the comparator is made and fine conversion is performed. In Figure 3.6, selection of fine ramp voltages according to the coarse conversion results can be seen.

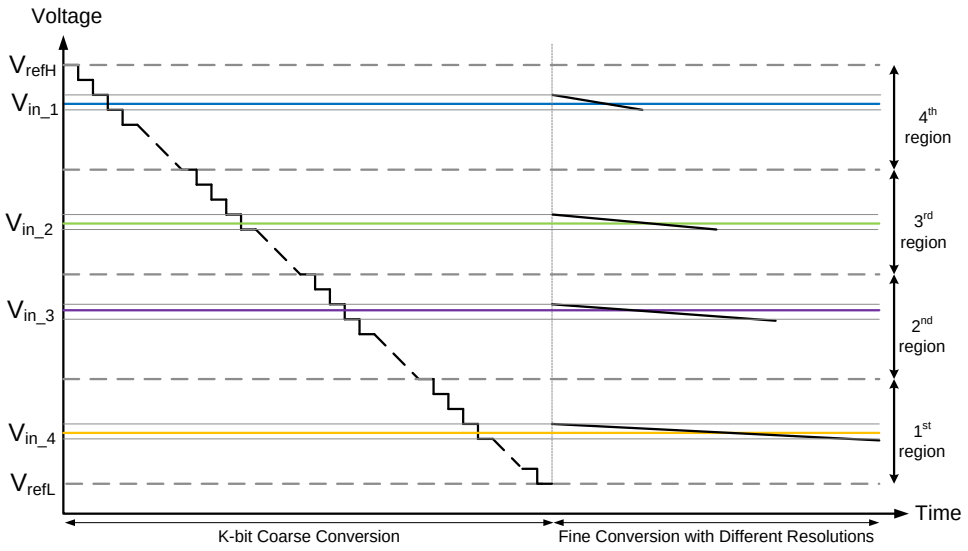

Figure 3.6 Example Ramp Waveforms Depicting the Conversion Algorithm for Two Step Multi-Slope ADCs.

3.1 Error Correction

Due to some undesired effects, such as the comparator offset and the charge injection of the sampling switch, the operation of the structure introduced above may be adversely effected. As an example, in the fine conversion phase, fine ramp voltage and the input voltage may not cross each other because of the effects mentioned above.

To overcome this problem, swing range of the fine ramp is increased to the 1.5 LSB of the coarse conversion. This way the fine ramp starts to decrease from the lower quarter of the upper LSB band and stops at the upper quarter of the lower LSB band that it should scan. Modified fine ramp signal for error correction can be seen in Figure 3.7. By taking this precaution against errors, fine ramp resolution is increased to 7-bits and conversion duration is increased by 32 clock cycles, making a total of 96 clock cycles. for fine conversion time. Conversion durations for different modes and resolutions are provided on Table 3.1. Even though fine conversion duration increase because of error correction, employing error correction method for the Two-Step ADC is obligatory. Otherwise dead bands and missing codes would decrease the ADC linearity. In [26], fine ramp swing corresponds to 2 LSBs of the coarse conversation, starting to decrease from the half of the upper LSB band and stopping at half of the lower LSB band. However, that much of non-ideality is not expected.

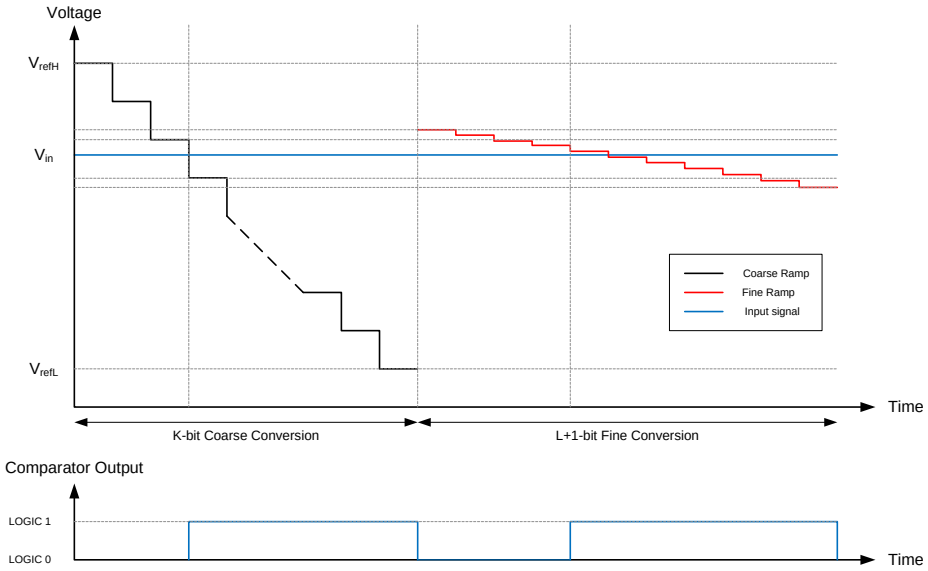

Figure 3.7 Proposed Fine Ramp Signal for Error Correction.

Following the end of conversion, output data is rescaled in the computer environment. If the fine conversion output yields a result that correspond to the upper or lower LSB band, the coarse conversion result is incremented or decremented by 1 respectively and the fine conversion result is re-calculated and reduced to 6-bit. Otherwise if the fine conversion result show that output belongs to the central band, the coarse conversion is not changed and the fine conversion result is re-calculated to give the 6-bit output. Figure 3.8 below shows the output re-calculation algorithm for the 6-bit coarse and the 7-bit fine conversion results. For the 12-bit regime, after the coarse conversion is completed, the global counter starts counting down from 95 to 0, whilst the fine ramp covers the 1.5 LSB band starting from the lower quarter of the upper LSB band to the upper quarter of the lower LSB band. Thus, the fine conversion outputs between 95 and 80 belongs to the upper LSB band, whereas outputs between 79-16 belong to the base band and results between 16-0 belong to the lower LSB band. While this algorithm is for a 12-bit conversion, it can easily be scaled for lower resolutions of conversion.

Table 3.1 Conversion Durations for Different Resolutions of ADC.

ADC Operation Mode	Resolution (bits)	Coarse Conversion Resolution (bits)	Fine Conversion Resolution (bits)	Coarse Conversion Duration for 10 MHz clk (µs)	Fine Conversion Duration for 10 MHz clk (µs)
Two-Step Single-Slope	12	6	7	6.4	1.6 + 6.4 + 1.6 = 9.6
Two Step Multi-Slope	12	6	7	6.4	1.6 + 6.4 + 1.6 = 9.6
	11	6	6	6.4	0.8 + 3.2+ 0.8= 4.8
	10	6	5	6.4	0.4 + 1.6 + 0.4 = 2.4
	9	6	4	6.4	0.2 + 0.8 + 0.2 = 1.2

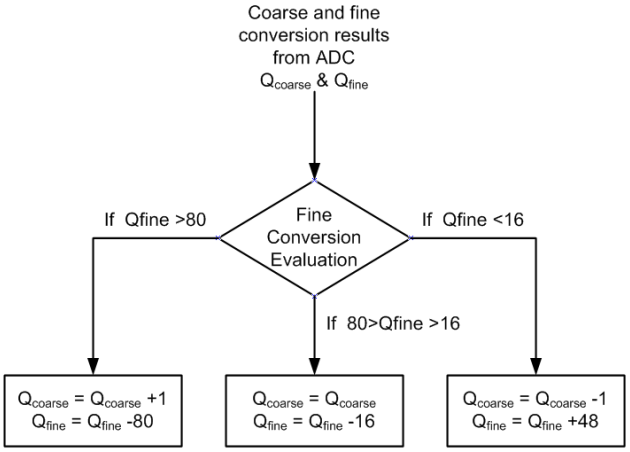

Figure 3.8 Fine Conversion Output Re-Calculation Algorithm.

Up to this point on this chapter proposed Two-Step Single-Slope ADC architecture is clarified. Henceforth, the alternative implementation methods for the required circuit blocks will be investigated and a selection for each functional block will be made.

3.2 Common Shared Circuitry

Common shared circuitry is implemented only once, serving all the column-parallel ADCs inside the prototype chip. This block includes a coarse ramp generator, fine ramp generators, and counters.

3.2.1 Ramp Generators

Ramp generators are critical blocks for integrating image sensors. They are a determinant factor on the linearity and noise performance of column-parallel ADCs. As the generated ramp signal is distributed to all columns, ramp generators should have low output noise and must be immune to the kickback noise caused by the instantaneous state change of numerous comparators.

3.2.1.1 DAC based Ramp generators

One way to implement a ramp generator is to use a digital to analog converter. By continuously increasing or decreasing the digital input, a staircase shaped ramp output signal is generated at the output of the DAC. Various types of DAC architectures such as, conversion on the voltage domain, the current domain or the charge domain can be implemented for ramp generators [32] Figure 3.9, example circuit diagrams for ramp generators implemented as DACs are provided.

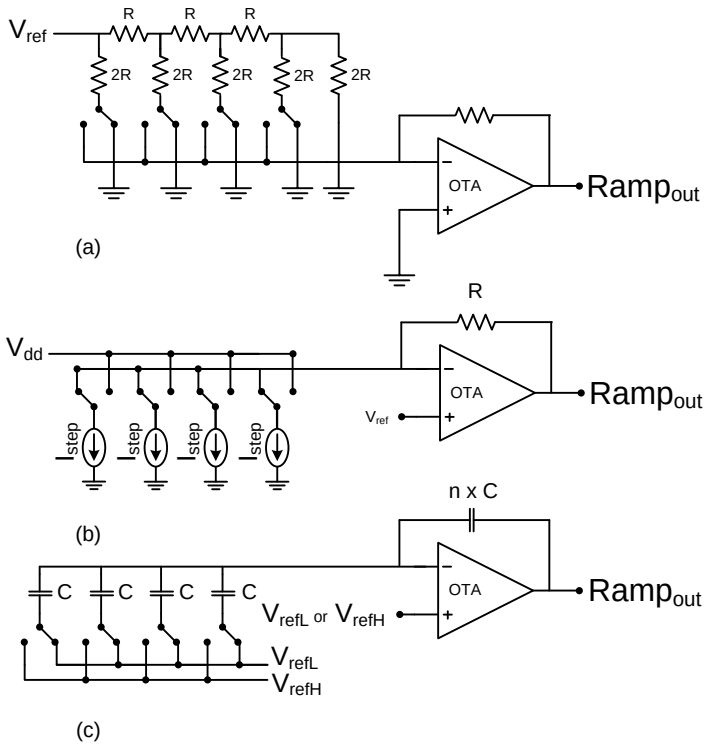

Figure 3.9 Simplified Schematic Diagrams for R-2R DAC (a), Current-Steering DAC (b), and Charge Redistribution DAC (c).

R-2R DAC presented in Figure 3.9(a) generates ramp shaped output waveform by switching binary-weighted currents flowing over 2R resistors placed on vertical branches from ground to resistor on the feedback loop. Current switching DAC represented in Figure 3.9(b) works with the same principle with R-2R DAC. However, currents are provided from the current mirror structures implemented with MOS transistors. Charge redistribution DAC shown in Figure 3.9(c), works with the principle of transferring charge packets to the capacitor on the feedback loop.

3.2.1.2 Integrator Based Ramp Generators

Ramp generation using current integrator is portrayed in Figure 3.10. The virtual ground is kept at V_{ref} voltage by the amplifier and the current supplied by the current source causes a decrease on the output as it is integrated over the feedback capacitor.

Unlike the DAC based ramp generator architectures mentioned above, integrator based ramp generator has current as the input, instead of the digital code, and the output shape is a saw tooth wave. Another distinguishing trait of the integrating ramp generator is that, step size of the ramp generator depends on the clock frequency, whereas for the DAC based ramp generators step size is independent.

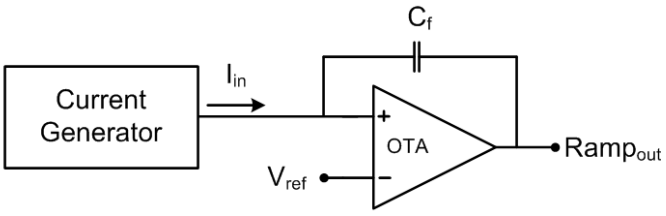

Figure 3.10 Block Diagram for Integrator Based Ramp Generator.

Obtained output swing also depends on the accumulation capacitor on the feedback loop of an OTA and the input current. It is described by the relation below:

$$dV = \frac{dt * i}{C} \ [V], \tag{3.4}$$

where dV is the output swing in Volts, dt is the integration period in seconds, i is the current to be integrated in Amperes, and C is the integration capacitance in Farads. One thing to be noted here is that, the input current is very prone to the process, temperature, and voltage variations. The value of the integration current has great

impact on the ramp signal's linearity and slope. Thus, a calibration scheme should be implemented. There are various calibration methods present in the literature [33], [34].

3.2.2 Shared Counter

Utilization of a shared counter is necessary to implement integrating ADCs on column parallel approach to feed digital data to the decision circuitries placed inside each column. Parallel loadable synchronous sequential up-down counter is a good alternative to generate the required digital data simultaneously with the ramp generators. Synchronous counters utilize a clock signal that triggers all flip flops inside the counter block concurrently. An example of parallel loadable counter is given in Figure 3.11. Selection of counting direction and being able to load the counter starting point in the parallel fashion, creates a flexibility of supporting different ADC resolutions and error correction algorithms as it will be explained below. Since the counter output is shared by a large number of column memory circuits, buffering by strong drivers is needed to not to latch the wrong code on the decision instant.

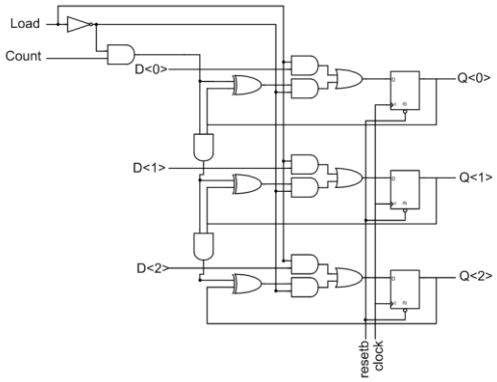

Figure 3.11 Example Schematic for 3-bit Parallel Loadable Synchronous Sequential Counter

3.3 Column Circuitry

Column-parallel implemented portion of the two-step integrating ADC is responsible for comparing the analog input signal to the ramp voltage, and toggles the output signal when the ramp and the input signals are crossed. At this toggling moment, counter outputs are latched to the memory.

Column-parallel circuitry consists of a comparator, an N-bit memory, and additional logic control blocks. Among these, comparator performance is the most crucial factor on the ADC operation. Kickback, offset, noise, power consumption, bandwidth, hysteresis, and area occupation are the main critical characteristics of comparators, thus mentioned parameters need to be considered carefully for optimum efficiency. Kickback can be described as the charge transfer at the instant of toggling, into or out of input terminals of the comparator, causing glitches on the previous stages like ramp generators or sample-hold. Offset in ADCs is one of the main contributors of the fixed pattern noise and causes strip artifacts on the image. Input referred noise of the comparator is another pivotal parameter, as it directly affects the signal to noise ratio of the ADC, hence the resolution. Power consumption should be kept as low as possible, elsewise the large number of comparators placed on the image sensor array would create excessive power drain. Bandwidth of the comparator influences the decision time, where low bandwidth may cause delay in toggling, which in turn may result in latching the wrong counter value. Hysteresis can be defined as the memory of the comparator, caused by the stored charge in the internal capacitances, and should be minimized by periodically resetting the comparator. Considering the fact that column parallel circuitries will be laid out on a single or double pixel pitch, large area requirement of a comparator will cause the chip dimensions to get larger in a single dimension and this conflicts with the efforts on manufacturing CMOS image sensors with smaller proportions.

3.3.1 Comparator

Different design approaches for column-parallel ADC comparators are present in the literature. The following subsection investigates several comparator architectures.

3.3.1.1 High Gain Amplifier

A simplistic approach for implementing comparators is using a high gain amplifier. An amplifier in the open loop configuration functions as a comparator, as shown in Figure 3.12, toggles its output to the positive supply voltage if the signal on the non-inverting terminal is larger than the inverting terminal and vice-versa [35]. Low bandwidth (slow decision time) is the major drawback of this approach. Larger current

dissipation may resolve the bandwidth issue however low power dissipation is a must for column parallel comparators.

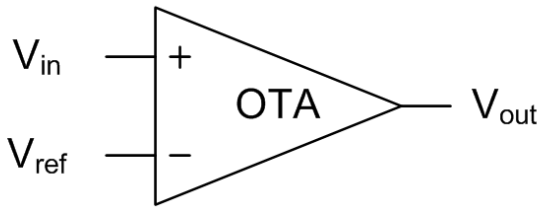

Figure 3.12 Comparator Implementation with High Gain Amplifier.

3.3.1.2 Multistage Comparator

Employing several single stage amplifiers in the cascaded form is another approach for high gain in comparators. Example of a three-stage comparator comprising low-gain amplifiers is illustrated in Figure 3.13. This architecture can operate very fast since the individual single stage amplifiers can operate fast as they do not need compensation [35]. Offset is a serious issue on this method and offset cancellation should be performed on successive gain stages.

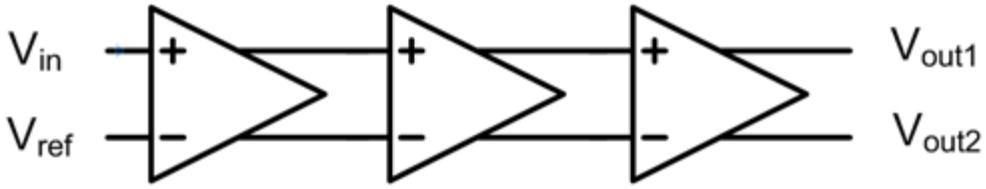

Figure 3.13 Comprator Implementation with Succesive Gain Stages.

3.3.1.3 Latched Comparator

Another generally used comparator type is latched comparator which is essentially a pre-amplification followed by a positive feedback latching circuit, as depicted in Figure 3.14. Preamplifier is used to provide gain, thus increasing resolution and alleviating kickback effects. The latch state further amplifies the preamplifier outputs by the help of regenerative feedback and provides a complementary full scale digital output [36].

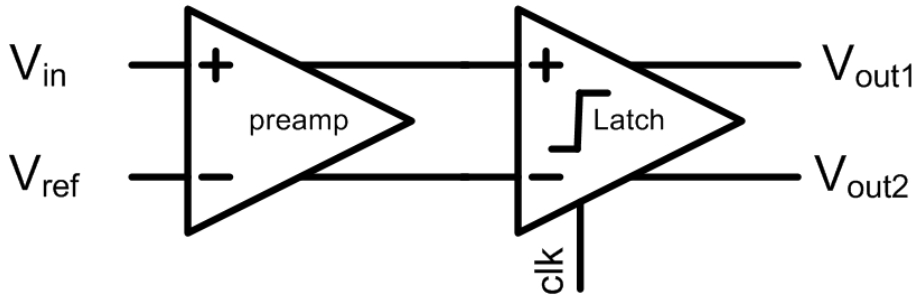

Figure 3.14 Comparator Implementation with Dynamic Latch Preceded by a Preamplifier.

Gain of the preamplifier is generally in the order of several 10 V/V. By keeping the preamplifier gain low, large bandwidth and smaller decision time is ensured. Preamplifiers used in latched comparators are generally implemented as one or two stages of cascaded differential pairs loaded with either resistive or diode connected MOS devices. To reduce the nonlinearities caused by the offset and noise, auto zeroing is also involved in high resolution applications.

One eminent point to be mentioned here is that the positive feedback latch circuitry is immune to the memory effect mentioned above as hysteresis since the internal nodes are reset at one phase of the input clock signal and the decision is made during the transition of the clock from one state to another.

3.3.2 Memory

As discussed while describing the operation flow of two step integrating ADC, shared counter's output stage should be latched onto a memory. A very straightforward memory block design can be realized by using D Flip-Flops. Even though the design may seem simple layout should be drawn carefully not to enlarge the layout footprint. Another alternative for the memory block can be the implementation of SRAMs for narrow pixel pitch applications. However, usage of SRAMs requires additional labor and experience, for the design of CMOS SRAM cells and sense amplifiers.

3.4 Design Methodology for Two-Step Multi-Slope ADC

So far on this chapter, different design approaches have been investigated for the functional blocks of Two-Step-Multi Slope ADC. In pursuance of meeting the

predefined design requirements for the Two-Step-Multi Slope ADC, the best fit among the alternatives presented above is picked and implemented. Following part of this subsection presents a discussion about the selection about the suitable alternatives.

3.4.1 Design of the Coarse Ramp Generator

As depicted in the Figure 3.1, a ladder shaped ramp generation is required for coarse phase, to latch the final value of the decision step on the analog memory capacitor. This requirement rules out the integrator based ramp generators. Resistive DACs are limited in their performance by the matching of the resistors and large thermal noise generated on the resistive ladder. Current steering DACs offer high speed in expense of drawing continuous current from the supply. Among the DAC based ramp generators capacitive charge sharing DAC seems to be an appropriate alternative with its speed and resistance to the kickback noise due to its large output capacitance.

3.4.2 Design of the Fine Ramp Generator

The fine ramp generator block is realized with the integrating ramp generator. The reasoning behind this decision is mainly due to its capability to scale for different resolutions easily without dramatically increasing the occupied area. Ensuring the ramp output to swing between the predefined range is a challenge due to process, voltage, and temperature variations. However, this complication can be overcome by introducing calibration circuits.

3.4.3 Design of the Comparator

For the design of the comparator, dynamic comparator approach is employed. High gain amplifier and multistage amplifiers are out of scope for this thesis as they reach high bandwidth with excessive consumption of power. Positive feedback latch comparator offers high gain, low power, and fast decision when preceded with a moderate gain providing preamplifier. Special care is taken for minimizing the input referred offset and noise for the comparator.

3.4.4 Design of the Counter

Synchronous sequential counter with the ability of up-down counting and parallel loading is implemented. There are several different alternatives which offer lower

power consumption, such as ripple counter and gray counter. However, the shared nature of the counter is an advantage in terms of power, as the overall consumed power is divided between the columns when calculating power.

3.4.5 Design of the Memory

Flip-flop based registers are selected for their simplicity.

CHAPTER IV

IMPLEMENTATION

This chapter summarizes the design of the Two-Step Multi Slope ADC by means of facts, requirements, and decisions covered in the previous parts of this text. Design of the prototype ADC IC is handled with block level top to bottom design methodology. Employed functional blocks in ADC prototype IC can be listed as:

- Common Shared Ramp Generators
- Column-parallel ADC block
- Common Shared Counter
- Bias Generators
- Digital Controller
- Column Multiplexer
- Output Serializer

Each of the blocks listed above will be examined thoroughly in different sections of this chapter. First section will focus on the implementation of the coarse and fine ramp generators. In the following part, comparator design for column parallel ADC will be described. Succeeding two sections aims to describe the design of column multiplexer and output serializer, which are used for readout of the binary data. Finally, implementations of bias generators block and digital controller are presented.

4.1 Common Shared Ramp Generators

Recalling from the introductory text of Chapter 3, operation of the Two-Step Multi-Slope ADC is divided into the coarse and the fine conversion phases. During both phases, the analog input signal of the ADC is compared to the ramp signals. Following section demonstrates the design of the coarse and the fine ramp generator blocks.

4.1.1 Coarse Ramp Generator

Generation of the coarse ramp signal is handled using a capacitive, charge-sharing DAC. The logic behind the implementation of a Charge-Redistribution DAC is replacing the input capacitance of a switched capacitor amplifier with a programmable capacitor array. Figure 4.1 depicts the schematic of the designed Charge-Redistribution DAC to be used as coarse ramp generator. Top plates of the capacitor array are shorted and driven to the 2.9 V reference voltage (V_{refH}). By switching the bottom plate voltages sequentially from V_{refH} to 0.9 V reference voltage (V_{refL}) to V_{refH}, decrementing output ramp is obtained [37].

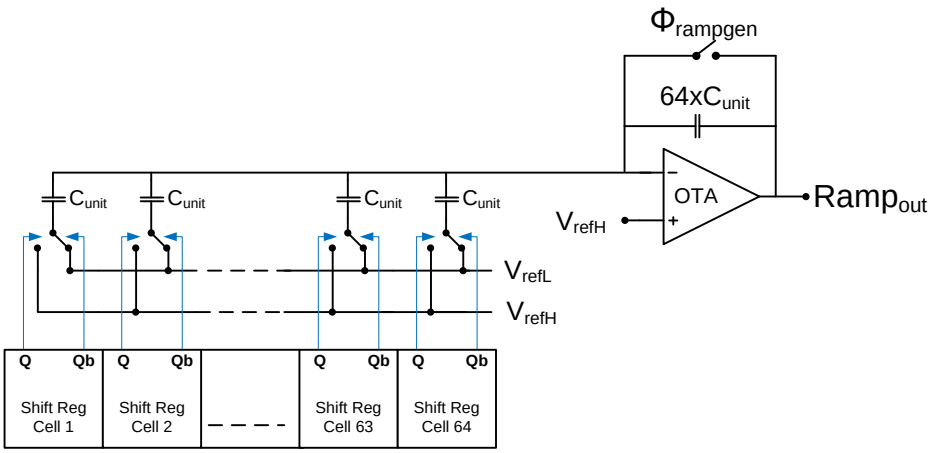

Figure 4.1 Schematic Diagram of Charge-Redistribution DAC.

As it can be seen from Figure 4.1, switching of capacitor bottom plates reference voltage is achieved through the use of a shift register, with every bit of the shift register in control of a single unit cell in the capacitor array.

There are two alternative methods known as unary weighted and binary weighted approaches, for realizing the capacitor array. Unary weighted capacitor method uses 2^K capacitors having equal values. This approach is beneficial as it guarantees the

monotonicity, i.e. no increase is possible for a decreasing ramp. Binary weighted capacitor method on the other hand, employs capacitors having values increasing exponentially. Even though this concept offers low area occupation and power consumption, code transitions may generate non-monotonicity, if a capacitor having higher exponential order is smaller than the sum of lower weighted capacitors. As mentioned in Section 3.2.1, relaxed area specifications for common ramp generators tilt the scales from power and area concerns to better linearity, thus usage of unary weighted unit-cell capacitors is employed when designing capacitor DAC.

The ramp generator operates on a sequential principle where every count is evaluated successively. Ramp generation starts with the closing of the feedback switch, disabling the unity gain buffer configuration. At the instant of breaking feedback loop, all the capacitors in the array have their both top and bottom plates connected to the V_{refL} voltage. As the shift register outputs change states sequentially, bottom plates of the capacitors are switched to V_{refL}, drawing a charge of:

$$Q = C \times \left(V_{refH} - V_{refL}\right) [Coulombs]. \tag{4.1}$$

The equation (4.1) above implies that the unit cell capacitance is charged between the ADC's full scale voltage and the required charge is drawn from the feedback capacitance. As illustrated in Figure 4.1, the feedback capacitance is 64 times larger compared to the unit cell capacitances in the array. Therefore, the charge stored on the unit cell capacitance corresponds to the 1/64 of the charge if the feedback capacitor was to be biased between V_{refH} and V_{refL}. In the light of this information it is safe to say that the charge drawn by the unit cell capacitance in the moment of switching creates a voltage drop at the OTA output corresponding to the 1/64 of the ADC's conversion range. The equation (4.2) describes the output ramp voltage per step number.

$$V_{ramp}(i) = V_{ramp}(i-1) - \frac{\left(V_{refH} - V_{refL}\right) \times C_{unit}}{C_{feedback}} [V], \tag{4.2}$$

where i =1:64 stands for the step number and V_{ramp} (0) equals to the V_{refH} voltage just before making the unity gain buffer connection OFF. Considering the fact that feedback capacitance is 64 times larger than the unit cell capacitance, (4.2) reduces to

$$V_{ramp}(i) = V_{ramp}(i-1) - \frac{\left(V_{refH} - V_{refL}\right)}{64}\ [V]. \quad (4.3)$$

As pointed out in Table 2.1, ADC's conversion range is 2 V, so each step on the coarse ramp voltage corresponds to 31.25 mV.

4.1.1.1 Design of the OTA

A typical folded-cascode amplifier is preferred to use as the buffer for the coarse ramp generator due to its high DC gain, large output swing range, and ability to drive large capacitances. Though there are other amplifier architectures offering lower power consumption, it is not a primary concern in the design as the coarse ramp generator is common to the all column-parallel ADCs.

DC gain value of the OTA is settled according to the monotonicity requirements of the ADC, such that the output of the OTA should settle within ½ LSB proximity of the desired value [12]. If the OTA is considered in a closed-loop negative feedback configuration, transfer function can be given as follows.

$$H(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1 + A(s)\beta}. \quad (4.4)$$

The gain of the OTA would be infinite in the ideal case, therefore, (4.4) would reduce to

$$H(s) = \frac{1}{\beta}. \quad (4.5)$$

The error on the condition where the amplifiers gain is non-ideal can be expressed as

$$\varepsilon = \frac{H(s)_{ideal} - H(s)_{real}}{H(s)_{ideal}} = \frac{\frac{1}{\beta} - \frac{A(s)}{1 + A(s)\beta}}{\frac{1}{\beta}}. \quad (4.6)$$

When the equation (4.6) is solved for A, the result gives us the gain requirement in terms of the specified error rate.

$$A = \frac{1 - \varepsilon}{\beta\varepsilon}. \quad (4.7)$$

On the unity gain configuration (β=1) and for ½ LSB error rate of 12-bit resolution on 2 V scale, the result yields minimum of 78 dB gain.

Another major requirement of the OTA is that it should settle for 12-bit accuracy within a half clock cycle time, leaving a safe time window for the preamplifier to process the input signals before the regenerative latch makes the decision corresponding to that cycle.

The coarse ramp signal was decided to have a decrementing nature thus the positive input should be connected to the V_{refH} voltage, which is 2.9 V. As V_{refH} voltage is within a threshold voltage proximity of the 3.3 V supply, usage of NMOS input pair is preferred. Allocated current dissipation value for this amplifier is approximately 1 mA and devices are sized to meet the specifications mentioned above. The rest of the design is straightforward and the schematic of the designed OTA can be seen in Figure 4.2. Device sizes of the amplifier are provided on Table 4.1

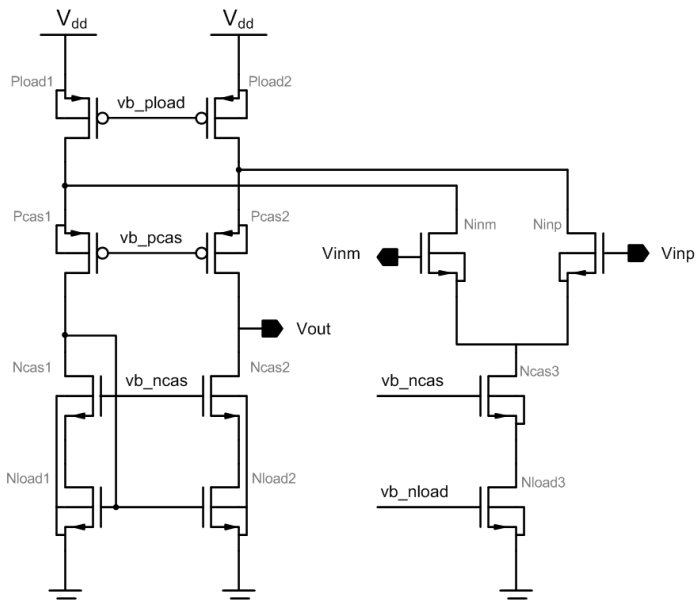

Figure 4.2 Schematic of the Coarse Ramp Generator OTA.

Table 4.1 Coarse Ramp Generator OTA Device Sizes

Device Name	**Dimensions (µm/µm)**	**Device Name**	**Dimensions (µm/µm)**
Ninm-Nimp	960 / 2	Ncas1-Ncas2	96 / 0.5
Ncas3	288 / 0.5	Nload1-Nload2	200 / 2
Nload3	300 / 2	Pcas1-Pcas2	400 / 0.5
-	-	Pload1-Pload2	800 / 2

4.1.1.2 Design of the Capacitor Array

The Two Step Multi-Slope ADC is designed to perform 6-bit conversion in the coarse phase, whose results correspond the most significant 6-bits of the overall result. To perform 6-bit conversion with unary weighted capacitors, 2^6=64 equal sized capacitors were employed. For each capacitance in the array, 64-bit shift register was also implemented, whose outputs act as the enable signals for the switches connected to the bottom plates of the capacitors. The schematic of the unit cell of capacitor array block, containing a unit capacitance, 2 MOS switches, and a D-Flip Flop of the shift register is depicted below in Figure 4.3.

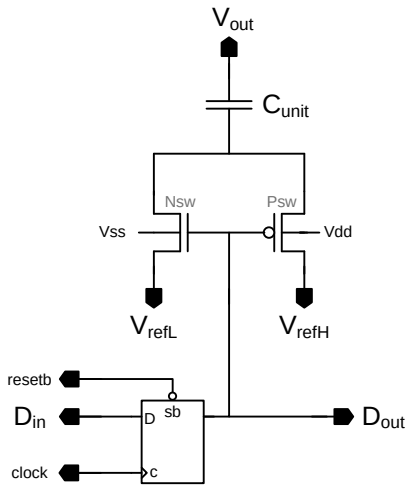

Figure 4.3 Schematic of a Unit-cell of Capacitive Array

64 of these unit-cell are connected in cascaded form, with their V_{out} terminals shorted and a cell's D Flip-Flop output connected to the succeeding unit-cell's input. Also, note that the data input of the first D Flip-Flop of the shift register is connected to a standard LOGIC 0 cell. When the OTA is in unity gain buffer configuration with the CMOS switch on the feedback loop ON, all the flip-flops are set and their outputs are at LOGIC 1 level. This output enables NMOS switch and unit cell capacitance's bottom plate gets biased with V_{refL}. When the unity gain connection of the OTA gets broken, D Flip-Flops on the array changes state one by one with each rising edge of the clock signal to the LOGIC 0 level. This output state enables the PMOS switch and unit-cell's bottom plate gets biased with V_{refH}. As both plates of the unit capacitor get

biased by same voltage, V_{refH}, stored charge leaves the unit capacitor and causes a voltage drop corresponding to 64 LSBs of the 12-bit conversion.

The capacitor size is determined so as the matching of the capacitors do not affect the linearity of the ADC adversely. For a 12-bit resolution, the capacitor value standard deviation should be:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{1}{2^{12}} = 0{,}024\ \%. \tag{4.8}$$

The process device specification document of the CMOS manufacturer describes the capacitor mismatch by the formula below:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC\_MIMH}{\sqrt{W_{eff} \times L_{eff}}}, \tag{4.9}$$

where W_{eff} - L_{eff} are the device width - length respectively and AC_MIMH is the Pelgrom coefficient for capacitor mismatch, 0.43 %µm. Using these values, device sizes are obtained such that W_{eff} =L_{eff} = 20 µm. A capacitor having these dimensions has 902.5fF capacitance. However, having 64x902fF capacitance on the feedback loop, creates glitches on the coarse ramp with very large glitch impulse areas, due to the capacitive coupling mechanisms. Thus, by reducing the capacitor dimensions and sacrificing from matching, glitch energies are reduced. Final dimensions of array capacitors are W_{eff} =L_{eff} = 10 µm and the corresponding capacitance value is 232 fF. With these dimensions on unit-cell capacitors, matching over 11-bits is achievable.

4.1.1.3 Simulation Results for the Coarse Ramp Generator

Simulation results and performance parameters for the coarse ramp generator block is provided within this section. Stability performance of the OTA is evaluated at –40 °C, 27 °C, and 85 °C.

Stability simulation results for the OTA is given in Figure 4.4. DC gain and unity gain frequency values for temperature corners, extracted from Figure 4.4 and stability simulations run at different temperatures, are provided in Table 4.2.

Table 4.2 Stability Simulation Results for Temperature Corners of Coarse Ramp Generator OTA.

Temperature [°C]	**DC Gain [dB]**	**Phase Margin [Deg]**	**Unity Gain Bandwidth [MHz]**
-40	80.79	60.33	45.91
27	83.27	60.5	38.43
85	84.96	60.72	34

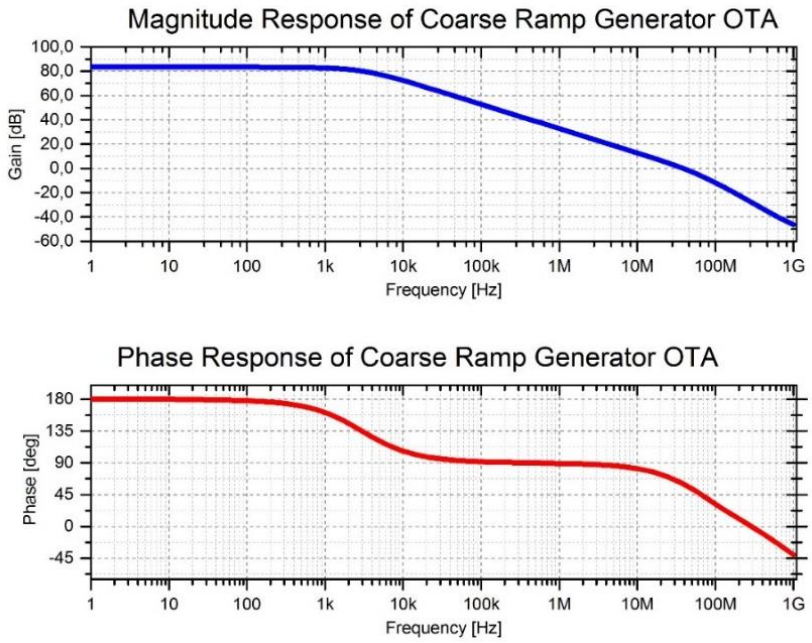

Figure 4.4 Frequency Response of the Coarse Ramp Generator OTA at 27 C

As the simulation results show, requirements set on Section 4.1.1.1 are well met, following transient simulation results in Figure 4.5 agree with the stability simulation results in terms of settling proximity and required settling time. While the ramp generation enable signal is in the LOGIC 1 state, ramp signal is 208 µV below the V_{refH} voltage, satisfying the ½ LSB error rate requirement which is 244 µV for 1 LSB being 488 µV. Transition time of ramp signal from n^{th} state to $(n+1)^{th}$ state is around 35 nS.

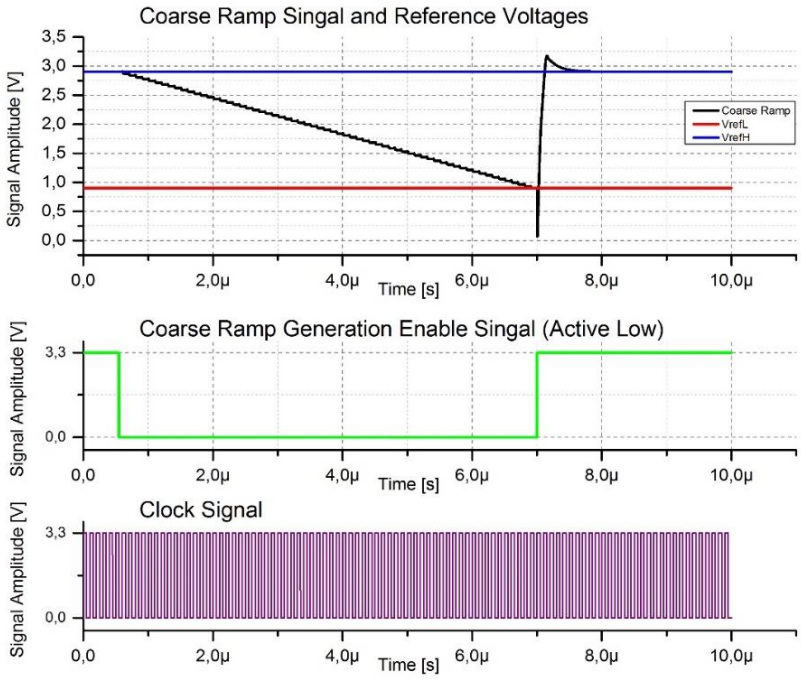

Figure 4.5 Transient Simulation Results for Coarse Ramp Generation

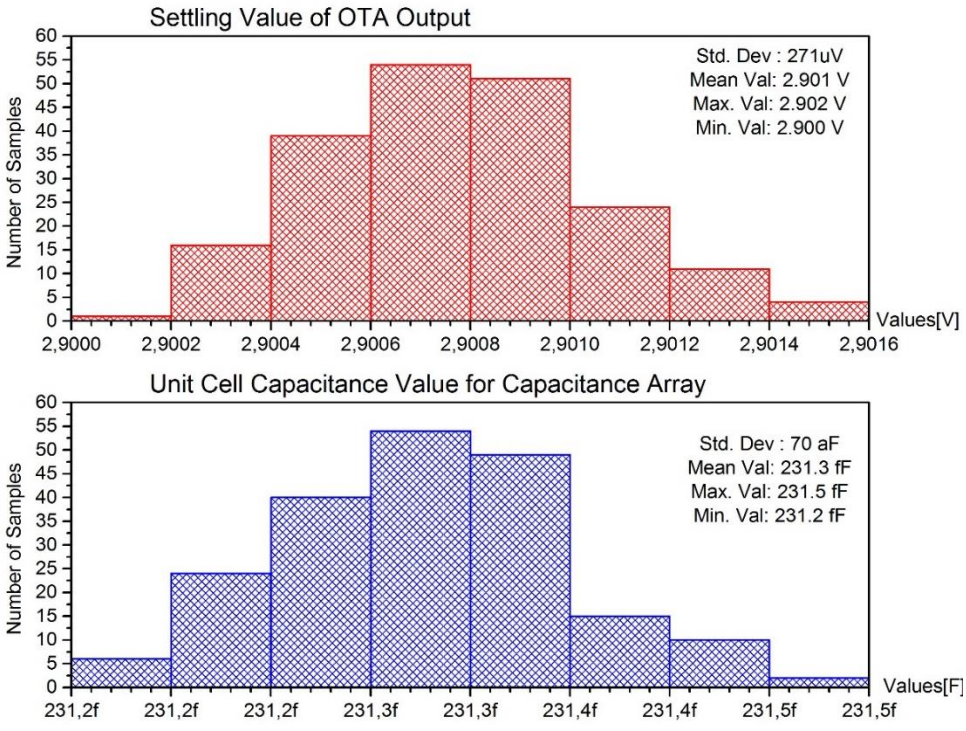

Figure 4.6 Mismatch Variations for OTA Offset and Unit-Cell Capacitance.

Monte – Carlo simulation results are provided in Figure 4.6. OTA input referred offset variation value is 270 µV. This value can be considered adequate, since it is smaller

than the LSB size of 12-bit conversion. Variation of the capacitance value on the capacitor array is 70 aF, which provides matching at 0.03 % level. This value is also satisfactory as it is very close to 12-bit matching requirement.

4.1.2 Fine Ramp Generator

The fine ramp is generated by means of an integrator based approach, as shown in Figure 4.7. Current from a trimmable source flows onto the feedback capacitor of the OTA and alters the output voltage in a decreasing manner. Slope of the fine ramp signal depends on the integration capacitor and input current. Output ramp waveform with respect to time can be expressed as:

$$V_o(t) = V_0(0) - \frac{1}{C}\int_0^t i(t)dt, \tag{4.10}$$

where V_o (0) is the start voltage of the ramp generator, which is equal to the input reference voltage the input referred offset of the OTA, C is the integration capacitance and i(t) is the input current. Furthermore, slope of the ramp is described as follows:

$$Slope = \frac{dV_o(t)}{dt} = \frac{i(t)}{C}. \tag{4.11}$$

Before the start of the fine ramp generation, a CMOS switch is kept at the ON state and OTA is in unity gain buffer configuration. Thus, the output is driven to input reference voltage, which is $1.25\times V_{LSB\_COARSE}$ higher than V_{refL} due to the error correction algorithm explained above. When the ADC steps into the fine conversion phase, enable signal for fine ramp generation changes state and the unity gain buffer connection is broken by making the switch OFF. From that point on, current from the current source is integrated on the feedback capacitance, causing decrease on the output signal. One thing to be noted here is, as mentioned in Section 3.2.1.2, input current generated at the current source is prone to process and mismatch variations, thus, it may create slope variations that would lead to linearity errors if calibration is not implemented. Using *ctl_rampslope <8:0>* control bit bus, integration current I_{framp} is programmed to achieve the desired ramp slope.

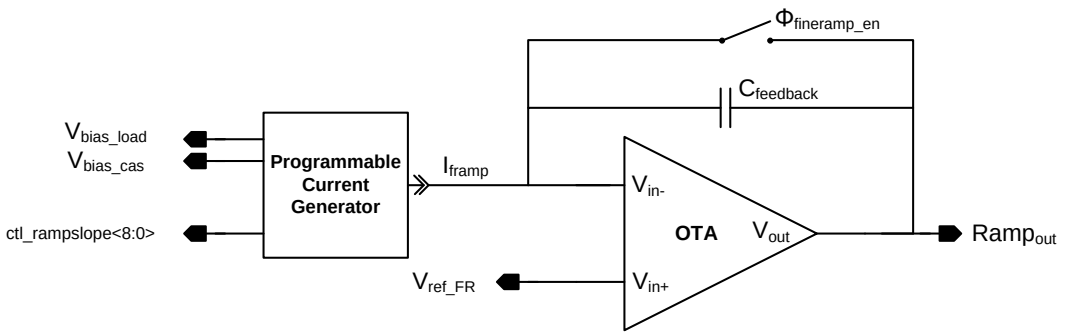

Figure 4.7 Fine Ramp Generator Circuit Topology

As mentioned in Chapter 3, allocated time span for the fine conversion phase is 96 clock cycles, corresponding to 9.6μs for a 12-bit resolution. If the ADC operates in the TSMS mode, fine ramp resolution decreases, thus the allocated time for fine ramps for 11, 10, and 9 bit resolutions downscale. To comply with the increased slope requirements of lower conversion resolutions, capacitor value is reduced.

Capacitor and input current values are determined considering the required slope, feasibility, and area occupation. Ramp slope is conditioned per allocated time and the swing of the fine ramp. It has been cleared that the fine ramp covers a 1.5 LSB region of the coarse conversion in 9.6 μs time duration.

$$\frac{dV}{dt} = \frac{1.5\ LSB_{coarse}}{9.6\ \mu s} = \frac{1.5\times\frac{2}{2^{12}}\ V}{9.6\ \mu s} = \frac{46.875mV}{9.6\mu s} = 4{,}8828\ {}^{kV}/_{s}. \quad (4.12)$$

To achieve this slope, if the amount input current is decided as 1 μA, a 204 pF capacitor is required. Implementing a capacitor of that value would occupy very large area and thus, the order of the input current is reduced to hundreds of nA. For a 100 nA current, required capacitance is reduced to 20.4 pF which is appropriate. Reducing the current further would be burdensome since the device sizes of the current mirror used in current generator gets very large. Final decision is made on 20.4 pF capacitance and 100nA integration current.

4.1.2.1 Design of the OTA

Like the OTA designed for coarse ramp generation, a folded-cascode amplifier is adopted to act as a buffer due to its well-known qualities like, large swing range and high DC gain.

Condition on the DC gain of the amplifier is similar to the OTA designed for the coarse ramp generation. For achieving a settling behavior within ½ LSB of the desired value, 78 dB gain is required as derived in Section 4.1.1.1.

Bandwidth requirement for this amplifier is relaxed as the swing within one clock cycle is reduced from 31.25 mV to 488 µV. However, care need to be taken as there is a large capacitive load present due to the input capacitances of the comparators placed in columns.

The fine ramp voltage is generated in the lower regimes of the conversion range so that it crosses the V_{refL} voltage after completing ¾ of its duration. Knowing that V_{refL} voltage is 0.9V, implementing an amplifier having NMOS input pairs may be risky, so PMOS input pairs will be employed as its input range spans from one threshold voltage below the positive supply to the ground. Schematic of the designed folded-cascode amplifier having PMOS input pair can be seen in Figure 4.8 and device sizes are provided on Table 4.3.

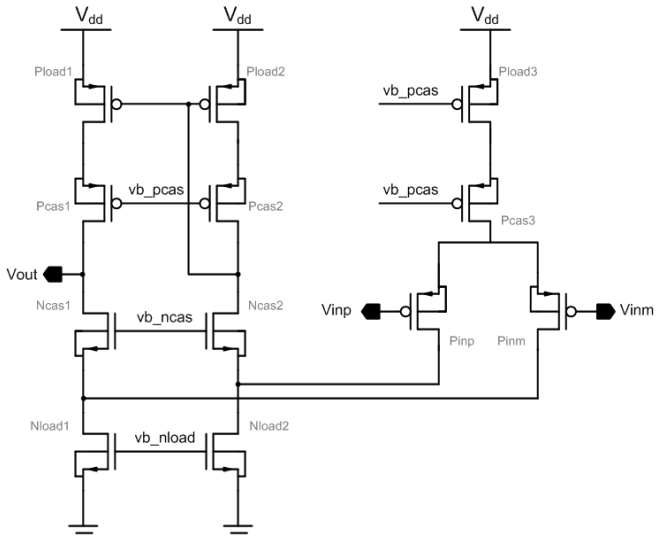

Figure 4.8 Schematic of Fine Ramp Generator OTA.

Table 4.3 Fine Ramp Generator OTA Device sizes.

Device Name	Dimensions (µm/µm)	Device Name	Dimensions (µm/µm)
Pinp-Pinm	720 / 0.4	Pcas1-Pcas2	200 / 1
Pcas3	200 / 0.5	Pload1-Pload2	400 / 1
Pload3	400 / 1	Ncas1-Ncas2	144 / 2
-	-	Nload1-Nload2	200 /2

4.1.2.2 Design of the Current Source

In order to produce the integration current, a reference current needs to be generated in the first place. Reference current generation is possible using a constant bandgap voltage, a trimmable resistor, and an operational amplifier.

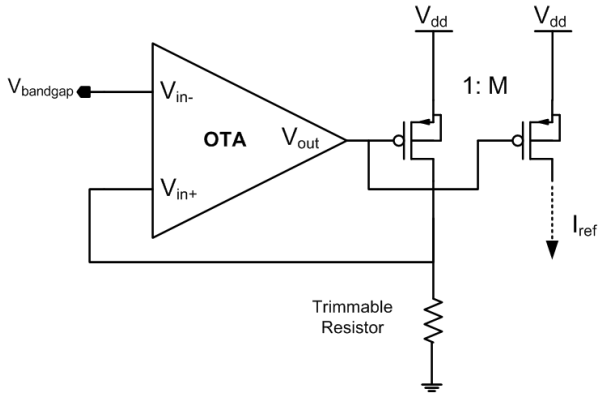

Figure 4.9 Generic Reference Current Generator.

Basic architecture to obtain reference current is depicted in Figure 4.9. Using the feedback loop, a voltage drop equal to the bandgap reference voltage over the resistor is created. Resulting gate voltage on the PMOS transistor is used to generate copies of the current flowing over the resistor on other transistors [35].

Generated reference current can be calculated as follows:

$$I_{ref} = M \times \frac{V_{bandgap}}{R} \ [A]. \tag{4.13}$$

Using the current generator scheme shown in Figure 4.9, a 10 µA reference current is generated inside the bias generator blocks of the chip. Then this reference current is further scaled down using down-scaling current mirror architecture shown in

Figure 4.10, to generate bias voltages for mirror and cascode PMOS devices that is going to source 100 nA current. Referred bias voltages are created from PMOS devices sourcing 100 nA and 1 nA currents, since the aimed resolution for current generation is 250 pA and current mirroring ratios below 10:1 is impractical for accuracy.

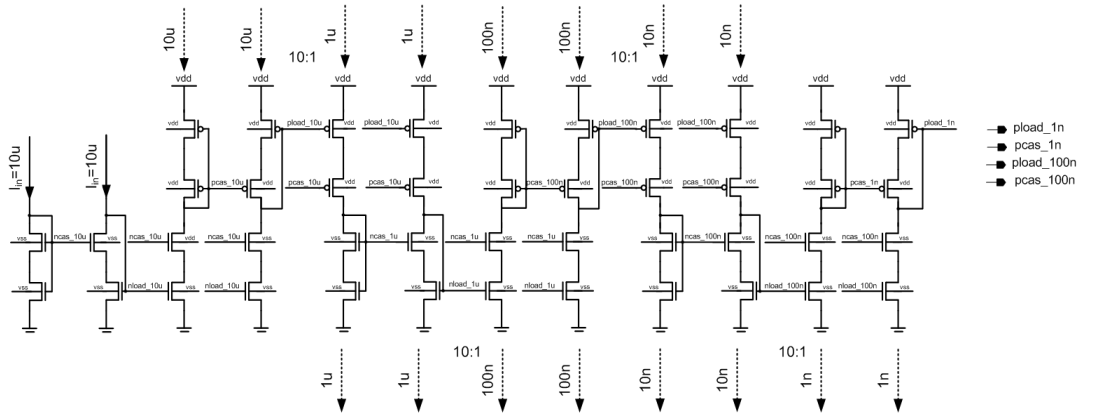

Figure 4.10 Down-Scaling Current Mirror.

Generated bias voltages from the down-scaling current mirror is used in current DACs for integration current generation. Using a 9-bit programming word, current values from 32 nA to 159.75 nA are obtainable with 250 pA resolution. Selection between currents is made possible with PMOS switches placed following each current sourcing cascode branch.

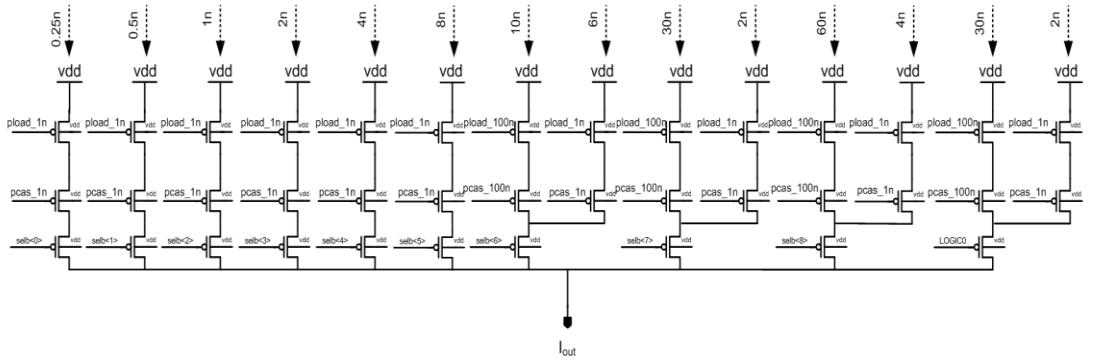

Figure 4.11 Current DAC for Generating Integration Current.

As pointed out earlier, 100 nA current is needed for the fine ramp signal to swing 46.875 mV using 20.4 pF capacitance. According to the DAC schematic provided above in Figure 4.11, 9-bit programming word should be:

$$ctl\_rampslope < 8:0 >= 100010000. \quad (4.14)$$

This value provides 100 nA current at the output terminal of the current DAC. However, due to process and mismatch variations both on the integration capacitor and the current sourcing PMOS devices, the programming word may need to be changed, which is handled via the SPI interface.

4.1.2.3 Simulation Results for the Fine Ramp Generator

The frequency response simulation results for the OTA employed in fine ramp generator, is presented below in Figure 4.12. 85.6 dB gain, approximately 60 Degrees of phase margin, and 55 MHz unity gain frequency is obtained under 15 pF capacitive load at 27 °C.

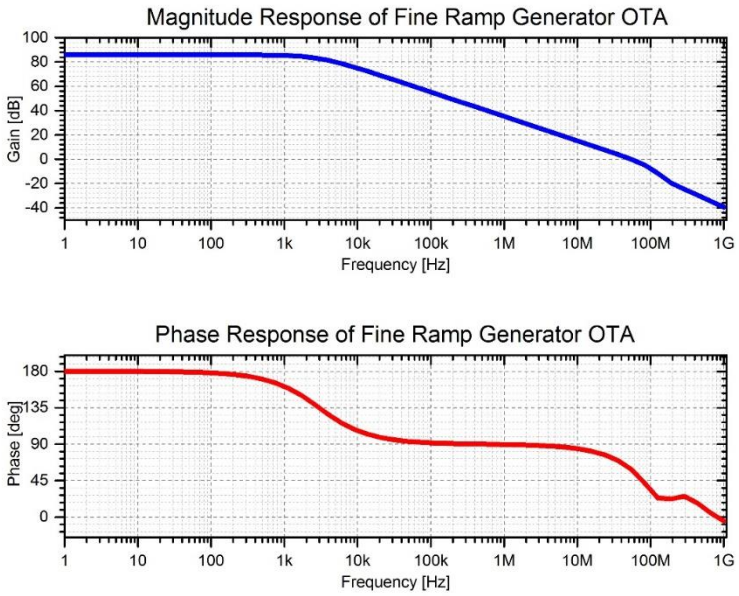

Figure 4.12 Stability Simulation Results for Fine Ramp Generator OTA at 27 °C.

Gain, phase margin, and unity gain frequency parameters for temperature corners are provided on Table 4.4. Results indicate that stability is not risked at any temperature value between -40 °C and 85 °C.

Table 4.4 Stability Simulation Results for Temperature Corners of Fine Ramp Generator OTA.

Temperature [°C]	DC Gain [dB]	Phase Margin [Deg]	Unity Gain Bandwidth [MHz]
-40	89.16	60.08	63.05
27	85.83	58.92	54.49
85	83.96	57.86	49.76

The transient simulation results for the fine ramp generator are given in Figure 4.13. The output of the fine ramp block is held at the reference value during the time interval where the enable fine ramp generation signal is at LOGIC 0 state. When the enable signal toggles to LOGIC 1 state, the fine ramp signal starts to decrease from the reference voltage value with the slope determined by the integration current and feedback capacitance over the OTA. Also, pay attention that the current value remains constant during the whole operation (except for the glitches at the beginning and the end of the ramp generation phase), due to the high output impedance characteristic of the cascode current source architecture.

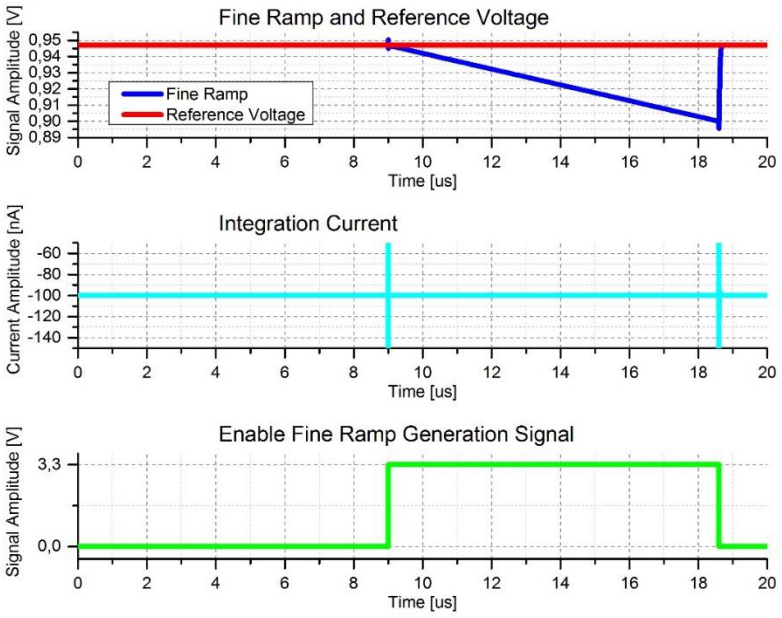

Figure 4.13 Transient Simulation Results for Fine Ramp Generator.

There are four different fine ramp generator blocks, implemented with four different capacitance values, to produce four fine ramp signals with varying slopes to be used in the Two-Step Multi-Slope mode of the designed ADC. These ramp generator blocks have their own separate programming words and digital enable signals, to trim the integration current individually and indicate the duration of the integration respectively. Operation of these ramp generators are illustrated in Figure 4.14.

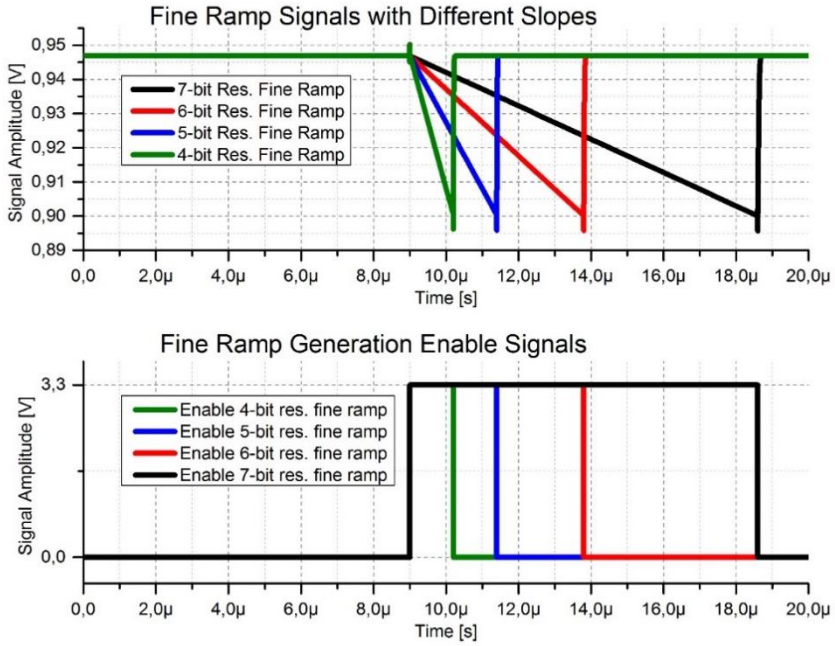

Figure 4.14 Simultaneous Operation of 4 Different Fine Ramp Generators.

The effect of process and mismatch variations on the integrating current and the feedback capacitance is investigated with Monte-Carlo Simulations. It is of utmost importance that the current generator to supply required current to match the determined slope for the maximum and the minimum values of the feedback capacitance. If these worst corners are within the range of current generation, any other capacitance value between these do not pose any threat on the slope of the fine ramp generator and the linearity of the designed ADC.

The maximum and the minimum values are provided in Figure 4.15 alongside with the mean and the standard deviation for both the integration current and the feedback capacitance. According to the maximum and the minimum capacitance values

obtained from the Monte-Carlo simulation results, required current values to match the slope requirement are calculated below.

$$Required\ Slope = 4.88\,{}^{kV}/_{s} = \frac{I}{C_{min}} = \frac{I}{18.01\ pF}. \qquad (4.15)$$

Solving the above equation for I yields 87.93 nA current requirement, which indicates that required current for the minimum capacitance value is well within the programmability range of the current DAC.

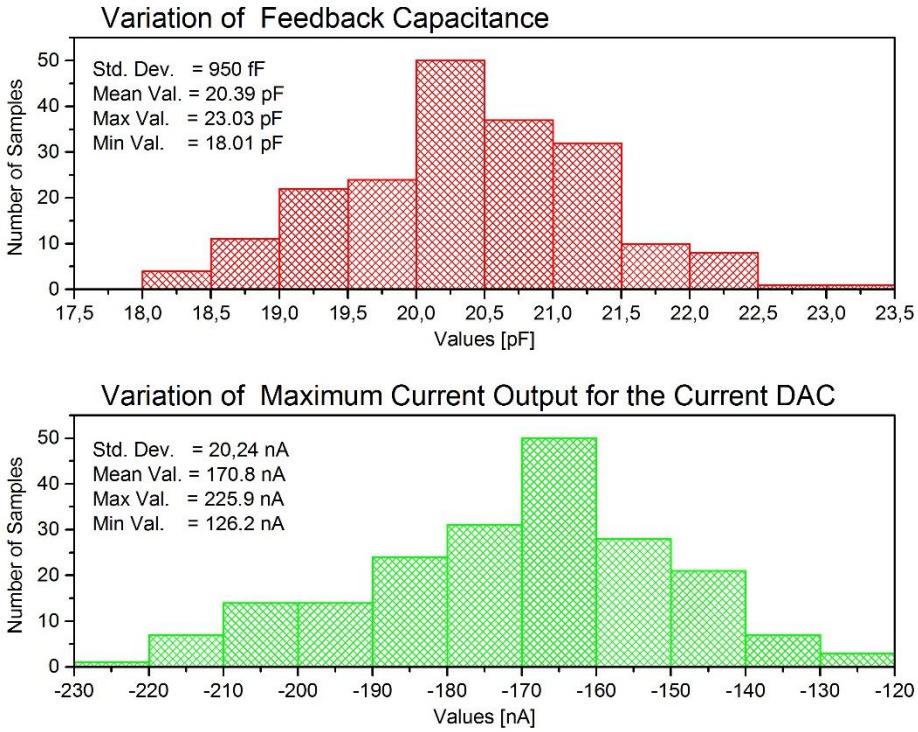

Figure 4.15 Process and Mismatch Variations for Feedback Capacitance and Maximum Output of Current DAC.

For the maximum value of the feedback capacitance,

$$Required\ Slope = 4.88\,{}^{kV}/_{s} = \frac{I}{C_{min}} = \frac{I}{23.03\ pF}, \qquad (4.16)$$

112 nA integration current is required if the equation above is solved for I. This value also, can be supplied by the current DAC even in the worst corners.

4.2 Column-Parallel Comparators

This section of the thesis focuses on the column parallel comparators designed as a part of the ADC. The column-parallel comparators are implemented using the approach at which a low gain pre-amplifier is followed by a positive feedback dynamic latch. Power consumption, input referred offset, and noise are parameters of utmost importance for mentioned blocks. Another important point to be mentioned of is that, the memory effect should be minimized by periodically resetting the comparator before every comparison [35]. Design of pre-amplifier, dynamic latch, memory, and column logic blocks will be investigated thoroughly within this section.

4.2.1 Pre-Amplifier

The pre-amplifier is designed to have more resolution from the comparator by diminishing some of the negative effects caused by the dynamic latch such as, the kickback noise and the input referred offset. It provides a gain in the order of 10 V/V. The reason for keeping the gain of the pre-amplifier low is to not to compromise bandwidth, i.e. keeping the decision speed high.

Pre-amplifiers are generally implemented as single or two stages of differential pairs with diode connected loads. Variations of this structure to increase the gain, noise performance, and bandwidth is present in the literature [38], [39]. For this design, diode connected loads are utilized for its simplicity, moderate gain, and large bandwidth.

Recalling the discussion on the input parasitic capacitance of the comparator circuits and its negative effects on the ADC architecture on Chapter 3, a 4-input comparator architecture is chosen for this design. Since the pre-amplifier is the input stage of the dynamic latched comparator structure, a pre-amplifier having 4 inputs is needed. For this purpose, a two-stage pre-amplifier is designed with its first stage incorporating a Gilbert Cell. Differential pairs' current steering property [40] is exploited during the design of this 4-input pre-amplifier.

In [40], the difference of drain currents of an NMOS input pair of a differential amplifier is described with the equation below:

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}, \quad (4.17)$$

where I_{D1} and I_{D2} are drain currents of the NMOS input transistors, μ_n is mobility, C_{ox} is the gate-oxide capacitance, W/L is the aspect ratio of input transistors, and I_{SS} is the tail current of the differential pair. Under the light of the (4.17), the operation of the pre-amplifier can be examined clearly.

Four inputs of the pre-amplifier are used for the coarse ramp, the analog input voltage, the fine ramp, and V_{refL}. These inputs are paired and connected to two differential pairs as illustrated in Figure 4.16. To determine the output state at the beginning of the conversion, initial conditions of inputs should be known. They can be listed as follows:

- The coarse ramp signal remains fixed at the V_{refH} voltage before the ramp generation enable signal is received.
- The analog input voltage is at an arbitrary level between V_{refH} and V_{refL}.
- V_{refL} input is fixed at the bottom of the full-scale range.
- The fine ramp input is also connected to V_{refL} before and during the coarse conversion phase.

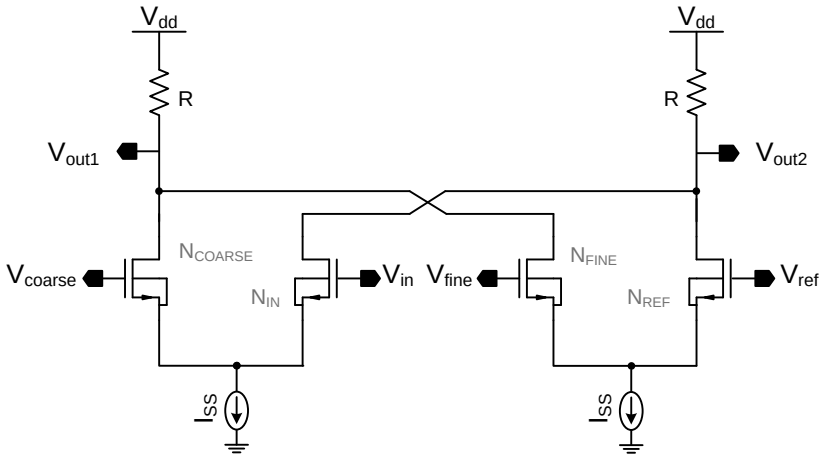

Figure 4.16 Conceptual Drawing of 4-Input Pre-Amplifier.

From the information on the initial states of the inputs, it can be concluded that:

- The coarse ramp input voltage is larger than the analog input voltage and following inequity on the drain currents of the transistors of the first differential pair is present.

$$I_{D_{COARSE}} > I_{D_{IN}}. \quad (4.18)$$

- The fine ramp input voltage is equal to the V_{refL} input and the drain currents of the transistors of the second differential pair are equal.

$$I_{D_{FINE}} = I_{D_{VREFL}} = \frac{I_{SS}}{2}. \quad (4.19)$$

It can be seen from Figure 4.16 that drain currents of the coarse ramp input device and the fine ramp input device are summed and the resulting sum of currents flows over the resistor connected to V_{out1}, whereas drain currents of the analog input device and V_{refL} input device are summed and the resulting sum of currents flows over the resistor connected to V_{out2}. Therefore, since the current flowing from the resistor connected to the V_{out1} branch is larger than the one from V_{out2} branch, the value of V_{out2} is higher compared to V_{out1} at the beginning of the conversion.

As described in the Chapter 3, the coarse ramp signal stays at V_{refH} voltage for a definite duration and starts to decrease in a ladder shape waveform, with every step corresponding to

$$V_{LSB\_COARSE} = {}^{2\,V}/_{64} = 31.25\,mV. \quad (4.20)$$

When the coarse ramp crosses the input signal, the value of the coarse ramp signal becomes smaller than the input voltage and is stored on the memory capacitor at the input of the preamplifier, after it settles on a value before decreasing another step. Assuming the bandwidth of the preamplifier is sufficient, stored value on the memory capacitor corresponds to the bottom value of the step where the crossing between the coarse ramp signal and the input signal occur. This condition can be interpreted as the potential difference between the coarse ramp input terminal and the analog input terminal is equal or less than V_{LSB_COARSE}, if the errors caused by the charge injection errors and offset are neglected. So, a difference on the drain currents corresponding to a voltage difference around V_{LSB_COARSE} is present on one of the differential pairs, after the coarse comparison phase. It should also be noted that, since the amplitude of the coarse ramp is now below the analog input signal value, $I_{DCOARSE}$ is smaller than the I_{DIN} and V_{out1} is larger compared to V_{out2}.

In Figure 3.4, it is depicted that the fine ramp input of the 4-input comparator has 5 inputs and V_{refL} being one of them, is connected to the fine ramp input terminal via a switch, which is ON during coarse conversion phase. Hence, second differential pair with its both inputs at V_{refL} voltage, has no difference between drain currents of input pair devices during the coarse phase. When the ADC enters in the fine conversion phase, one of the four fine ramp signals is connected to the fine ramp input terminal of the comparator. Fine ramp signal, as shown in Figure 4.13, starts from its reference voltage and decreases by $1.5\times V_{LSB\_COARSE}$ during the fine conversion phase. Therefore, at the start of the fine conversion phase, $1.25\times V_{LSB\_COARSE}$ voltage difference is present between the input terminals of the second differential pair and the drain current values differ for the input pair devices by an amount corresponding to this voltage difference.

Knowing that the voltage difference between the input terminals of the second differential pair is larger than the first differential pair, it can be stated that the difference between the drain currents of the second differential pair is also larger than first differential pair.

$$\left(I_{D_{IN}} - I_{D_{COARSE}}\right) < \left(I_{D_{FINE}} - I_{D_{REF}}\right). \tag{4.21}$$

Looking at Figure 4.16, it can be seen that drain currents of N_{COARSE} - N_{FINE} and N_{IN} - N_{REF} input transistors are summed. The inequality above can be manipulated to express the sum of the drain currents of N_{coarse} - N_{fne} and N_{in} - N_{ref} pairs. The result yields,

$$\left(I_{D_{IN}} + I_{D_{REF}}\right) < \left(I_{D_{FINE}} + I_{D_{COARSE}}\right), \tag{4.22}$$

which in turn causes V_{out1} to become larger than V_{out2}, thus the outputs return to their original state. Then during the fine phase, simultaneously with the decrease of the fine ramp signal, the difference between the drain currents of the second differential pair gets smaller. When the difference between the fine ramp signal and V_{refL} becomes smaller than the residue between the analog input voltage and the stored coarse ramp voltage, the inequity between the currents reverse and take the following form.

$$\left(I_{D_{IN}} + I_{D_{REF}}\right) > \left(I_{D_{FINE}} + I_{D_{COARSE}}\right). \tag{4.23}$$

This condition on currents causes V_{out1} value to get higher compared to V_{out2} value and the conversion is complete with this crossing.

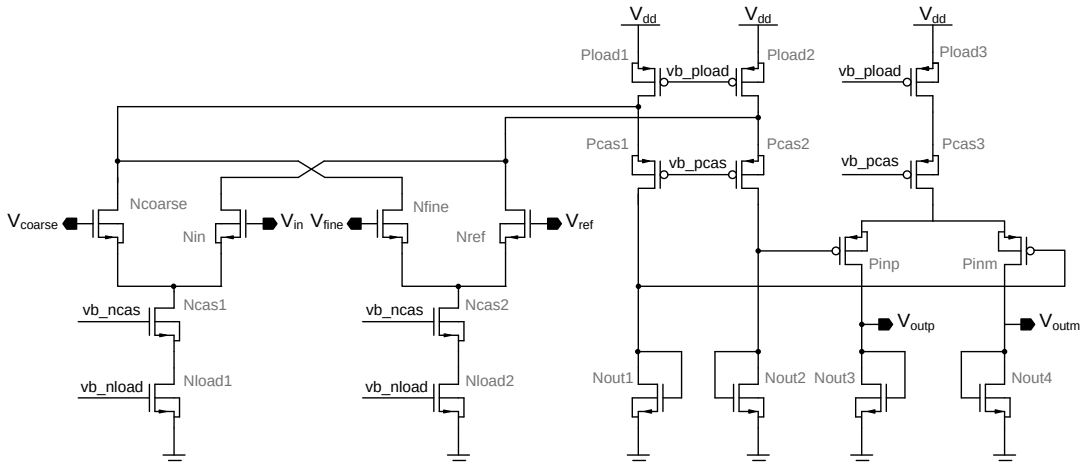

Figure 4.17 Schematic of the Designed Pre-Amplifier

Schematic of the designed pre-amplifier is illustrated in Figure 4.17. The reason for employing folded cascode architecture on the first stage is to keep the voltage swing as large as possible. If the telescopic architecture was to be employed, diode connected PMOS devices would consume a great voltage headroom, limiting both gain and voltage swing. The second stage is realized as a simple differential pair with diode connected loads. Device sizes for the designed pre-amplifier are given on Table 4.5.

Table 4.5 Device Sizes for Designed Pre-Amplifier.

Device Name	**Dimensions (µm/µm)**	**Device Name**	**Dimensions (µm/µm)**
Ncoarse-Nin-Nfine-Nref	80 / 1	Nout1-2-3-4	1 / 5
Ncas1-Ncas2	24 / 0.5	Pinp-Pinm	40 / 0.5
Nload1-Nload2	20 /3	Pcas3	40 / 0.5
Pcas1-Pcas2	50 / 0.5	Pload3	18 / 2
Pload1-Pload2	24 / 2	-	-

The total current dissipation of the pre-amplifier block is 40 µA. Tail currents for two differential pairs at the input is 10 µA. Pload1 and Pload2 devices sources 15 µA current each and remaining 5 µA current flows over the output transistors of the first stage. Second stage is also biased with 10 µA tail current.

Gain of the pre-amplifier is expressed by the equation below:

$$A = \frac{g_{m_{Ncoarse}}}{g_{m_{Nout1}}} \times \frac{g_{m_{Pinp}}}{g_{m_{Nout3}}}, \tag{4.24}$$

where g_m is the transconductance of the respective transistor.

4.2.1.1 Offset Cancellation

As mentioned in Section 2.3, noise sources (both temporal and spatial) can seriously degrade the image sensor performance. Since the comparator is the key element determining the performance of the analog to digital converter, offset reduction should be performed to reduce the spatial noise components. These non-idealities can be reduced by means of sampling the undesired quantities on a capacitor and subtracting the sampled value from the signal to be cleared [13].

Using this method, non-idealities that are fixed with respect to time is completely cancelled and low frequency noise source are high pass filtered, thus greatly reduced. However, alongside with these positive effects, auto zeroing increases the high frequency noise components. Therefore, special care should be taken to minimize the noise floor of the designed comparator.

Implementing the offset cancellation requires division of the comparator's operation into two phases. In the first phase, offset voltages are sampled and hold in sampling capacitors. Then, in the second phase, analog to digital conversion is performed. Hence, to employ offset cancellation, conversion time of the designed analog to digital converter is increased by a certain time interval.

Offset cancellation is generally performed using two approaches. First method is storing the offset voltage at the input of the comparator, forming a closed feedback loop between the input and the output of the comparator. Second method, output offset storage, encompasses feeding the same voltage reference to all the input terminals and sampling the offset voltage at the output [41]. Input offset storage method increases the input capacitance of the comparator and large gain is required to cancel out the offset, thus output offset storage method is employed in this work.

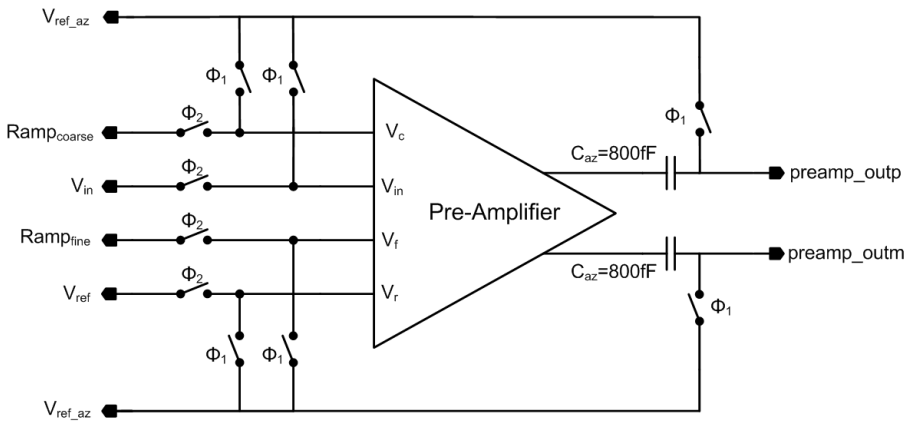

Figure 4.18 Implementation of Offset Cancellation.

Employed offset-cancellation scheme is illustrated in Figure 4.18 and explained hereon. During the first phase, switches controlled by Φ_1 are ON, therefore all four inputs and the bottom plates of the sampling capacitors are shorted to the V_{ref_az} reference voltage, which can be equal to the V_{refL} voltage or a higher value. During this phase, preamplifier offset voltage is sampled on the top plate of the capacitors. On the second phase, Φ_1 and Φ_2 signals change state and branches that have the switches controlled by Φ_1 are open-circuited. The pre-amplifier has its real inputs and the analog to digital conversion is performed.

The residual input referred offset voltage of the pre-amplifier after performing offset-cancellation is described as:

$$V_{OS} = \frac{\Delta Q}{A_0 C_{az}} + \frac{V_{OSL}}{A_0}\ [V], \tag{4.25}$$

where ΔQ is the difference of injected charge due to mismatch on sampling switches, A_0 is the gain of the preamplifier, C_{az} is the auto-zero sampling capacitance, and V_{OSL} is the input referred offset of the dynamic latch [41].

4.2.1.2 Simulation Results for the Pre-Amplifier

DC simulations are performed for the pre-amplifier to check the bias points of transistors and calculate the gain. Gain of the pre-amplifier is described by the equation (4.24). The g_m values of NMOS input transistors in the Gilbert-Cell and the PMOS input transistors in the second stage amplifier are 114.4 $\mu\Omega^{-1}$ and 107.4 $\mu\Omega^{-1}$, whereas

the g_m values for both of the diode connected NMOS load devices are 19.78 $\mu\Omega^{-1}$. Having these values, gain of the pre-amplifier stage can be calculated as:

$$A = \frac{g_{m_{Ncoarse}}}{g_{m_{Nout1}}} \times \frac{g_{m_{Pinp}}}{g_{m_{Nout3}}} = \frac{114.4\mu S}{19.78\ \mu S} \times \frac{107.4\mu S}{19.78\ \mu S} = 31.4\ [V/V]. \quad (4.26)$$

To check the calculated gain value and obtain frequency response of the pre-amplifier, stability simulations were performed. Magnitude response of the pre-amplifier for -40°C, 27°C, and 85°C temperatures are given on the Figure 4.19. Gain and cut-off frequency values extracted from Figure 4.19 are provided on Table 4.6.

Table 4.6 Frequency Response and Noise Parameters of Pre-Amplifier on Temperature Corners.

Temperature [°C]	**DC Gain [V/V]**	**Cut-off Frequency [MHz]**	**Input Referred Noise [µV]**
-40	30.22	4	54.13
27	35.2	4.7	63.32
85	39.7	5.9	73.12

By looking at the DC gain values provided on Table 4.6, it can be said that the gain calculations were accurate. Using the cut-off frequency values provided on the same table, integrated input-referred noise values were calculated and presented on the rightmost column. Acquired noise values are sufficient to obtain an ENOB performance over 11-bit.

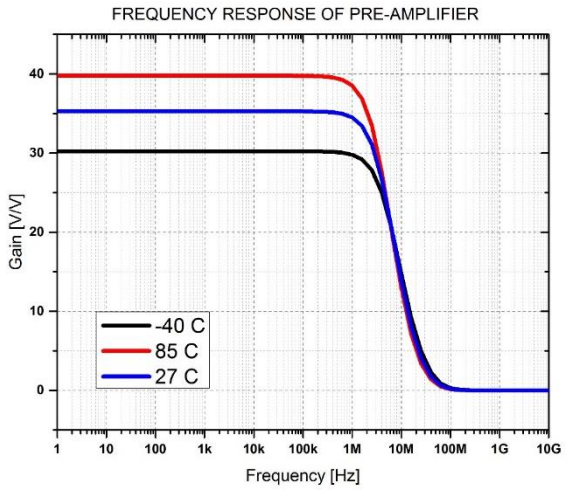

Figure 4.19 Frequency Response of the Pre-Amplifier.

A transient simulation for the pre-amplifier block is performed for an analog input voltage at 2.83 V level and results are demonstrated in Figure 4.20. As it can be seen from the figure, while coarse ramp signal is higher compared to the analog input voltage, I_{COARSE} current value is also higher than I_{IN}. When the coarse ramp signal and analog input voltage crosses each other, inequity between I_{COARSE} and I_{IN} changes direction. Simultaneously, outputs of the pre-amplifier crosses each other and they remain such until the start of the fine conversion phase. Also, note that the coarse ramp signal value is stored on the memory capacitor at the end of the step wherein the crossing occurs. With the beginning of the fine conversion phase, the actual fine ramp is connected to the fine ramp input of the pre-amplifier and the outputs of the pre-amplifier toggle again. As the fine ramp voltage gets smaller, agreeing with the logic explained above in section 4.2.1, I_{FINE} decreases and I_{REF} increases, consecutively, where the sum of I_{IN} and I_{REF} becomes larger than the sum of I_{COARSE} and I_{FINE}, pre-amplifier outputs crosses each other again and conversion is completed.

The decision delay value obtained from this simulation is around 35 nS, which is adequate for 100 nS decision cycles.

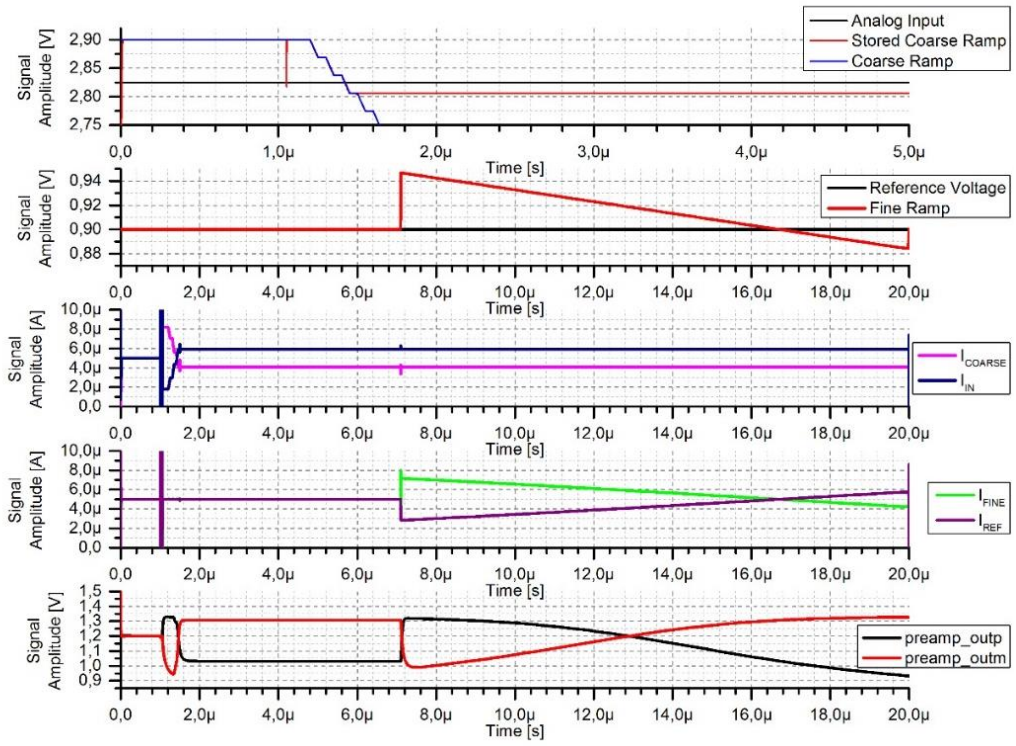

Figure 4.20 Transient Simulation Results of the Pre-Amplfier.

To check the efficiency of the offset cancellation architecture, 500-point Monte-Carlo simulations are run. The input referred offset values for the pre-amplifier architecture both with and without offset-cancellation, as well as the gain and tail current variations are shown in Figure 4.21. By comparing the input referred offset results for pre-amplifier structures with and without offset-cancellation, accuracy of the method can be grasped. The standard deviation value of the input referred offset for the pre-amplifier with the offset-cancellation is 1.1 μV, whereas it is 1.6 mV for the pre-amplifier without the offset-cancellation, corresponding to approximately 3.3 LSBs. Gain variation is 1.14 V/V.

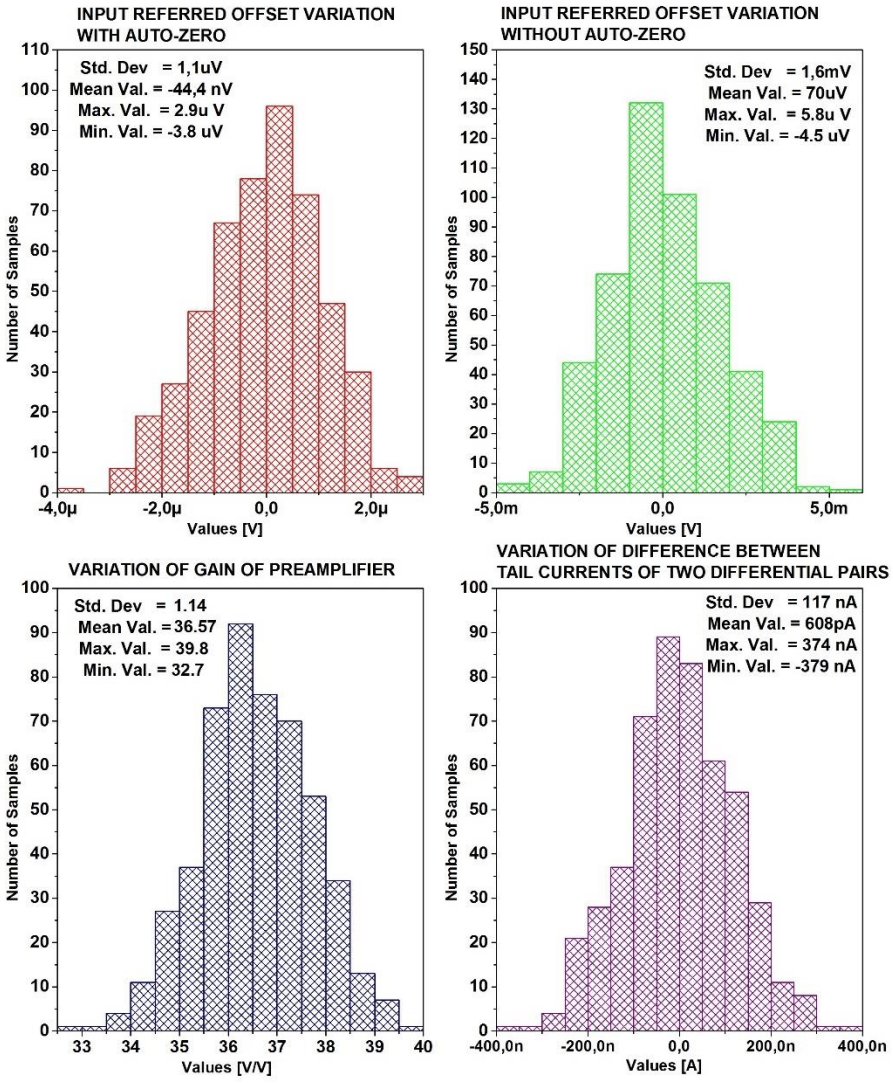

Figure 4.21 Monte-Carlo Simulation Results for Pre-Amplifier.

The tail currents biasing the Gilbert-Cell differential pairs should be matched for high-accuracy. However, the simulation results for the difference of these tail currents yields an undesired result, despite the usage of MOS devices with long length in the current sinking structure. The standard deviation for the difference between two tail currents is 117 nA which is quite high and will limit the yield of the manufactured samples. To address this issue on the future designs, transistors with larger dimensions should be employed on current mirrors.

4.2.2 Dynamic Latch

Dynamic latches can be considered as cross-coupled inverters, similar to the sense amplifiers employed in SRAM designs, whose decision cycles are controlled by a clock signal. Dynamic latches are widely employed for comparator designs in the ADCs due to their appealing traits such as no static power consumption, fast decision due to positive-feedback, reduction of memory effect, and small area.

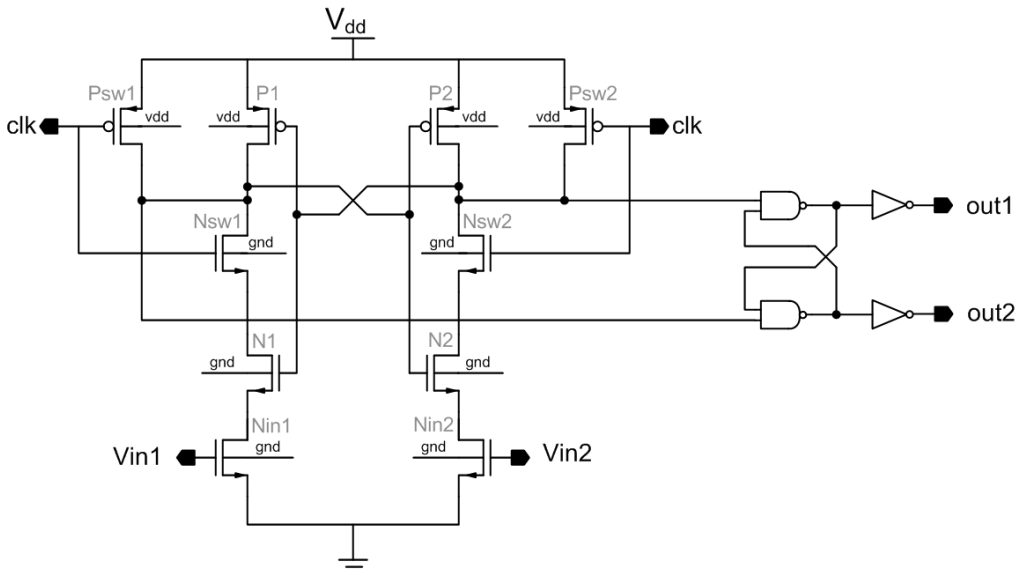

Figure 4.22 Schematic of Implemented Dynamic Latch.

In Figure 4.22, schematic of the dynamic latch design is illustrated. Back-to-back connected inverters are formed with N1-P1 and N2-P2 pairs. Psw1 and Psw2 transistors are used for clocking and reduction of memory due to the previous comparison. Nsw1 and Nsw2 transistors are used to ensure that no DC path is present from the positive supply to the ground. Nin1 and Nin2 transistors are employed to

create an imbalance using input voltages at the sources of the N1 and N2 transistors. Device sizes of the dynamic latch design is provided on Table 4.7. Dimensions are considerably small compared to the other blocks. Furthermore, Nsw1 and Nsw2 transistor sizes are kept large to prevent the sensing circuit to suffer from meta-stability on low input voltage differences.

Table 4.7 Device Sizes for Dynamic Latch.

Device Name	**Dimensions (µm/µm)**	**Device Name**	**Dimensions (µm/µm)**
Nin1-Nin2	5 / 0.5	P1-P2	5 / 0.18
N1-N2	5 / 0.18	Psw1-Psw2	0.4 / 0.18
Nsw1-Nsw2	8 / 0.18	-	-

Operation of the dynamic latch circuitry is described below:

- During the time interval where the input clock signal is LOW, Psw1-Psw2 switch transistors are ON. Sources of P1 and P2 transistors are actively driven to the positive supply during this phase. The gate voltages of N1 and N2 are also connected to the positive supply, therefore their drains are connected to the ground, assuming the input voltages Vin1 and Vin2 are higher than threshold voltage of NMOS transistors. Hence it can be said that all active nodes are actively driven to a known voltage to erase memory. Low clock signal at the gate of Nsw1 and Nsw2 transistors forces these devices to the cut-off mode, thus the connection path from positive supply to ground is broken.
- At the rising edge of the clock signal, Psw1 and Psw2 switch transistors turn OFF and Nsw1 and Nsw2 transistors turn ON. The input devices and the NMOS transistors employed in the inverters, quickly recovers from the triode state. Assuming that Vin1 is higher than Vin2, the output node of the inverter on the left is discharged faster compared to the output of the inverter on the right. The regenerative effect of the positive feedback fastens this discharging and the output of the inverter on the left quickly falls to ground level while the output of the inverter on the right does not change state and remain at the positive supply level.

To prevent latch outputs to change at every clock cycle, an SR latch with NAND gates is implemented on the output. Function table of the SR latch using NAND gates is given on Table 4.8. Before the inputs of the dynamic latch crosses each other, the sensing circuit always produces the same S-R values at the rising edge of the clock. Assuming the S input is 1 and R is 0 at the initial state, sensing circuit outputs continuously change between SR=10 and SR=11 with every clock cycle. From Table 4.8, it can be inferred that output of the SR latch does not change for these input combinations. Only when the inequity between the inputs change direction, sensing circuit reverses its outputs as SR=01 and SR=11 and the SR latch outputs toggle their logical values [42].

Table 4.8 SR Latch Function Table.

S	R	Q	Qn
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	-	-

4.2.2.1 Simulation Results for the Dynamic Latch

Transient simulation result for the dynamic latch block, using a 10MHz clock and two-dynamic changing inputs is provided in Figure 4.23. As it can be seen, outputs of the sensing circuitry are periodically drawn to 1.8 V positive supply level, where the clock signal is low. On the rising edge of the clock, a decision is performed and one of the sensing circuit outputs toggle to the ground. This trend continues until two inputs cross each other. From that point on, the output that is remaining on the positive supply level starts to toggle down to the ground level with every rising edge of the clock and the second output remains at the positive supply level. Also, notice that final outputs of dynamic latch do not change until the inputs cross each other, thanks to the SR latch implementation. The simulated transition time of outputs is around 320 pS.

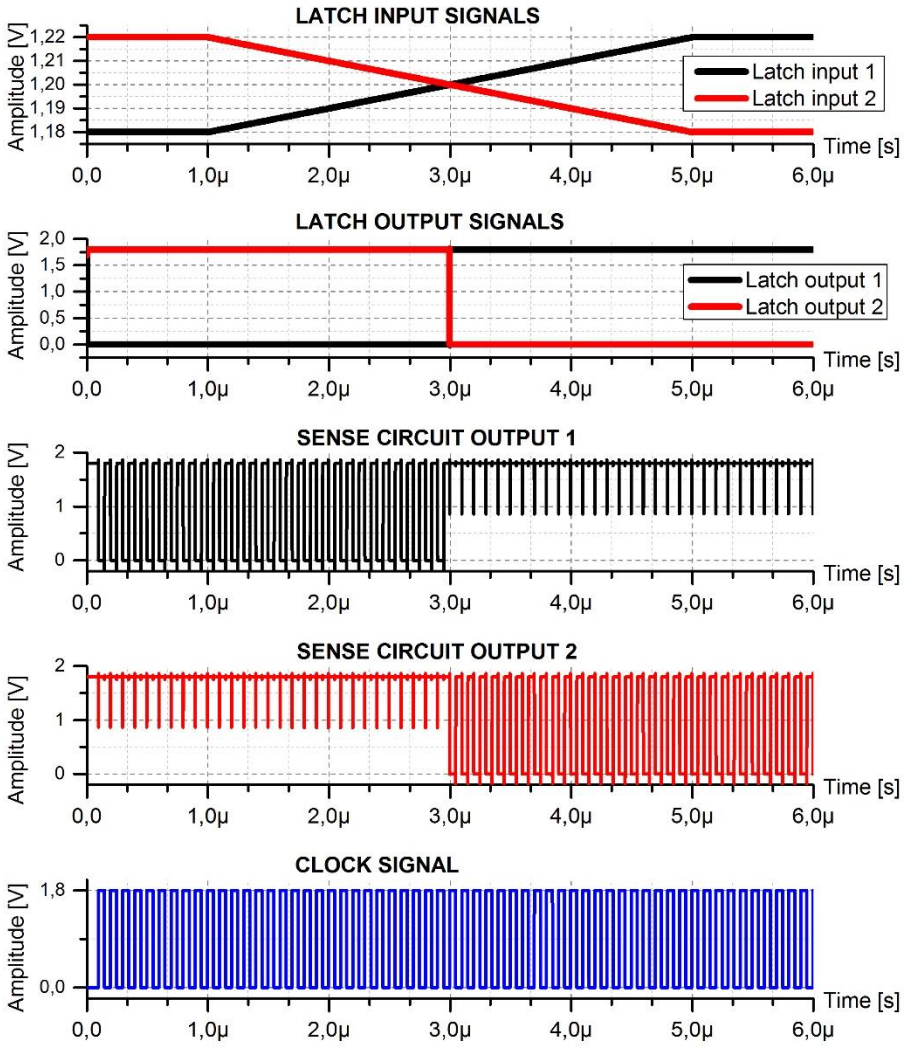

Figure 4.23 Transient Simulation Results for Dynamic Latch.

4.2.3 Memory

Storage capacity requirement for the Two-Step Multi-Slope ADC is 13-bits per column; 6-bits for the coarse and 7-bits for the fine conversion results. The counter output data at the instant of the toggling of comparator output is parallel-loaded onto the memory block with the rising edge of the comparator outputs. Stored data is set to LOGIC 1 for all bits, after the outputs are read-out via the column multiplexer and the output serializer blocks.

The memory circuit is implemented using rising-edge triggered D Flip-Flops. Each of the flip-flops shown in Figure 4.24 are connected to a different bit of the counter output

bus. Their clock input is connected to the comparator output and the active-low set signal is generated by the timing block.

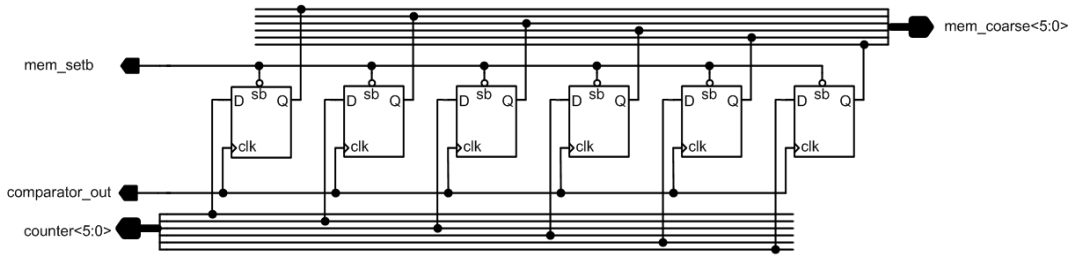

Figure 4.24 6-bit Memory for Coarse Conversion Result Storage.

4.2.3.1 Simulation Results for the Memory Block

Figure 4.25 exemplifies the storage of the coarse conversion result, where the output to be latched is 25 in the decimal form. Before the start of the conversion, *mem_setb* signal is received and all the D Flip-Flip outputs are set to LOGIC 1, corresponding to decimal 63. The counter output decrements from 63 one-by-one in each clock cycle, and at the point where the latch output toggles from LOGIC 0 to LOGIC 1, the counter output, which points to decimal 25 at that instant, is stored on the coarse memory block.

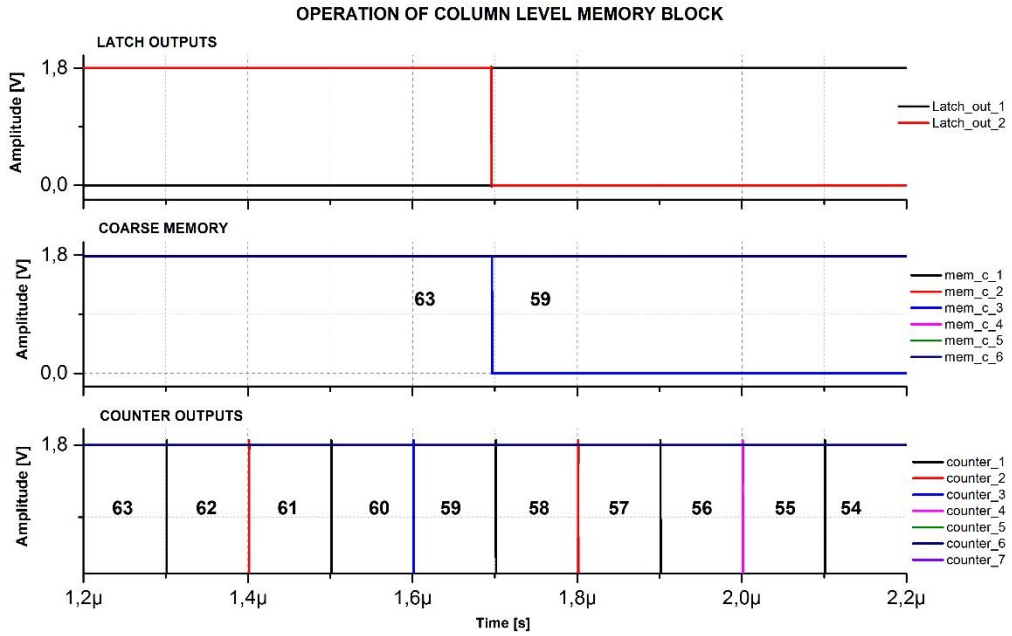

Figure 4.25 Simulation Results for Coarse Memory Block.

4.2.4 Logic Block

Column logic block is designed to assist the operation of the comparator by generating switch control signals, and to enable alternating between different modes and resolutions. This block is designed with standard cells provided by the CMOS foundry.

Output signals generated by this block are:

- *ctl_holdcap:* Hold capacitor control signal. Starts the conversion on LOGIC 1 state and toggles to LOGIC 0 when the comparator output toggles during coarse phase. Using this signal, coarse ramp value is stored on the hold capacitor.
- *ctl_rfine_sw<3:0>:* Generation of this signal requires MSB 2-bits of the coarse conversion result, which mark the region that the analog input resides. Using these two bits, selection between fine ramps with different slopes is made and the Two-Step Multi-Slope ADC operation is performed. These signals can also be overridden by the programming inputs fed by the SPI interface, allowing the user to select resolution and forcing the ADC to operate in the Two-Step Single-Slope mode.

The out of range recovery function is also embedded within this block. If the analog input voltage is outside the conversion range of the designed ADC, 13-bit binary output composed of LOGIC 1s is kept on the memory block, which is also an invalid output value. This function is realized by checking if the coarse ramp can cross the input signal or not. If the coarse conversion was performed successfully, a D Flip-Flop which has the comparator output as the clock input raises its output to LOGIC 1 state, enabling the loading of the counter outputs on the fine conversion phase. Elsewise, if the coarse ramp does not cross the analog input voltage in the coarse phase, that D Flip-Flop's output remains at LOGIC 0 level, disabling the parallel loading of the data. Recall from Section 4.2.3, before the conversion, all the bits in the memory are set to LOGIC 1. Therefore, as no parallel-loading is carried-out, the conversion output for an analog input voltage out of conversion range is given as 13-bit LOGIC 1s.

$$memory\ output = 111111 - 1111111. \tag{4.27}$$

Another function of the logic block is to disable the pre-amplifier and the dynamic latch blocks, after the fine conversion decision is achieved. Using this function, a significant improvement on the power consumption value is achieved. Assuming an even distribution of the analog input voltage on the conversion range, average power consumption can be conserved up to 41 % while operating in the Two-Step Multi-Slope Mode.

4.2.4.1 Simulation Results for the Logic Block

The fine ramp selection function of logic block while the ADC is operating on the TSMS mode is illustrated in Figure 4.26.

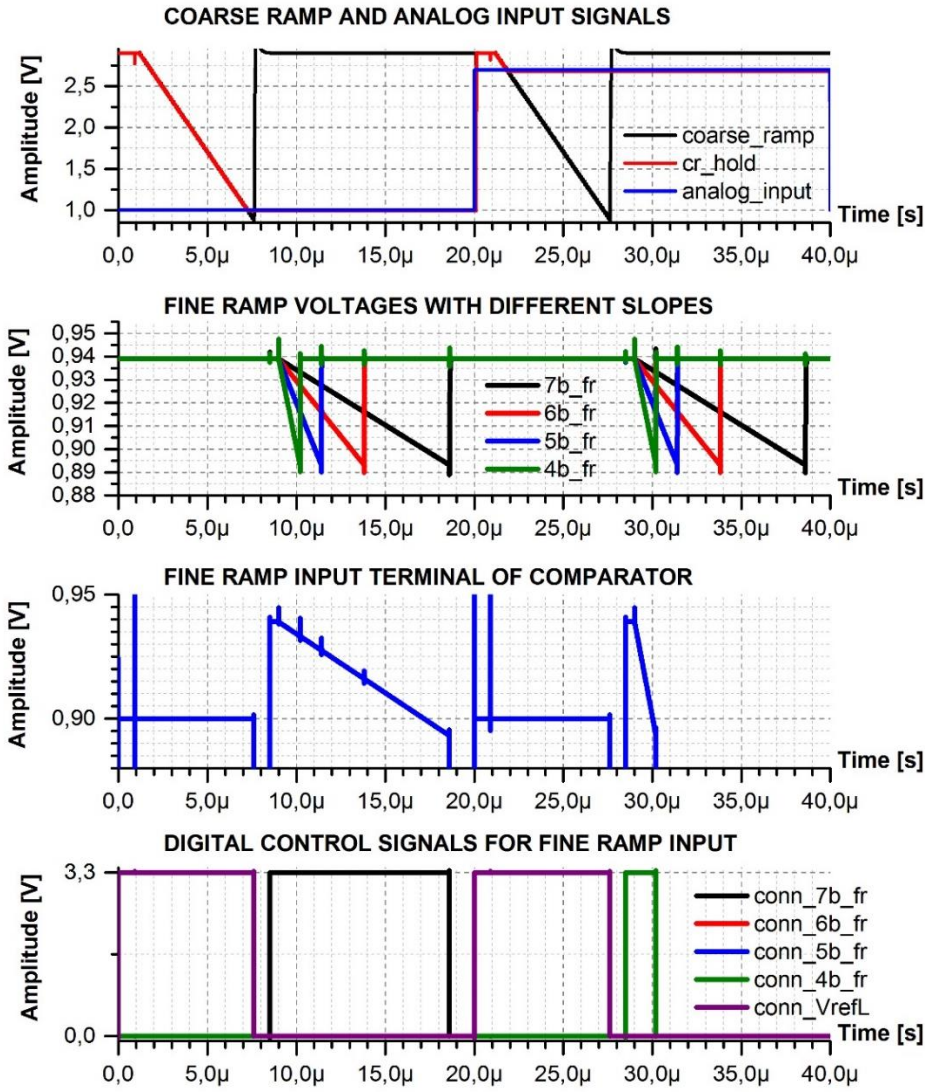

Figure 4.26 Column Logic Block Transient Simulation Result.

During the first conversion cycle, 1 V analog input is given to the ADC. This level of analog input requires the use of the fine ramp voltage with 7-bit resolution. Thus the 7-bit fine ramp voltage is connected to the fine ramp input terminal of the comparator. On the second decision cycle, the analog input voltage is increased to 2.7 V. The analog inputs at this regime is polluted with the shot noise and 12-bit conversion is not necessary, as explained in Chapter 3. Therefore, fine ramp with a resolution of 4-bits is selected for the comparator and the conversion is completed.

4.3 Readout Blocks

Following the conversion of the analog signal to the digital domain, generated 13-bit data needs to be transferred to the peripherals of the IC. To handle this operation, 13-bit data packages provided by the numerous columns needs to be reduced to a single 13-bit word and then fed to the output terminal in a serial scheme. Following sections present the column multiplexer and the output serializer blocks that serve for the abovementioned purpose.

4.3.1 Column Multiplexer

Design of the column multiplexer block is realized with the use of standard 4x1 and 2x1 multiplexers. A 24x1 multiplexer is formed as shown in Figure 4.27. 13 of these multiplexers work in parallel to reduce 24x13-bit data to single 13-bit word.

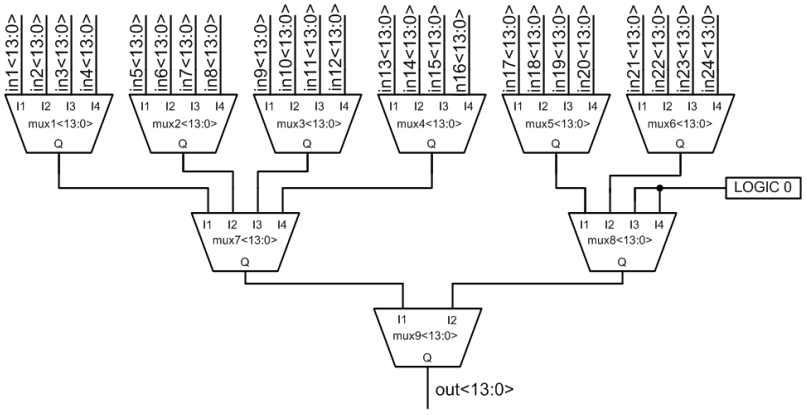

Figure 4.27 Schematic of Column Multiplexer.

4.3.2 Output Serializer

Transferring 13-bit data to outside of the IC via 13 parallel ports is inconvenient as it increases the number of pads and consequently the package size. To reduce the number of data output terminals, a shift register is designed. Design of the shift register incorporates 4x1 multiplexers, D Flip-Flops, and an output buffer. Operation of the output shift register is controlled by 3 digital control signals; clock, pd_*load* and *data_valid*.

Design of the output serializer is illustrated in Figure 4.28. Using two digital control signals, hold, parallel data load, and shift operations are performed. If both signals are at LOGIC 0 state, hold operation is performed. Using *pd_load* signal, 13-bit digital data provided by the column multiplexer is loaded onto the D Flip-Flops. When the *data_valid* signal is at LOGIC 1 state for 13 clock cycles duration, data is shifted from LSB side to the MSB side of the shift register. MSB bit is buffered and fed to the output terminal alongside with the *data_valid* signal. LOGIC 0 signal is fed to the LSB side as the serial data input.

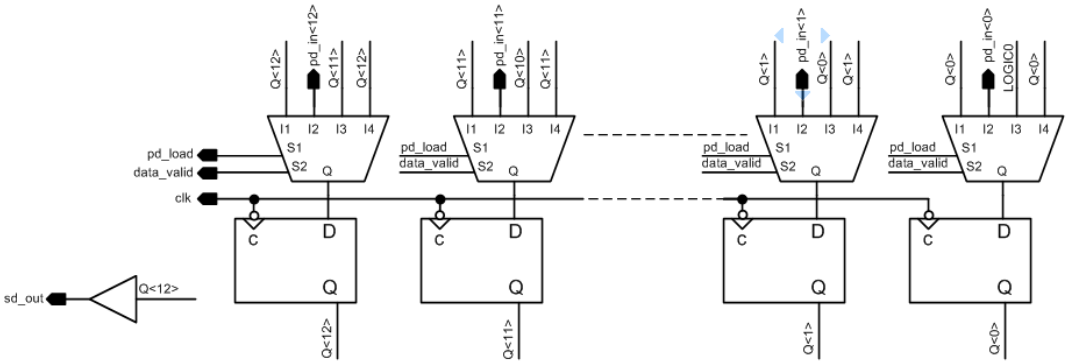

Figure 4.28 Schematic of Output Serializer.

4.3.2.1 Simulation Results for the Output Serializer

In Figure 4.29 a transient simulation result for the output serializer block is shown. 13-bit binary data of 1100011010100 is fed and parallel load occurs with the *pd_load* signal. During the time interval where the *data_valid* signal is at LOGIC 1 state, data it fed out with MSB bit being the first. Data transition occur at each falling edge of the clock signal.

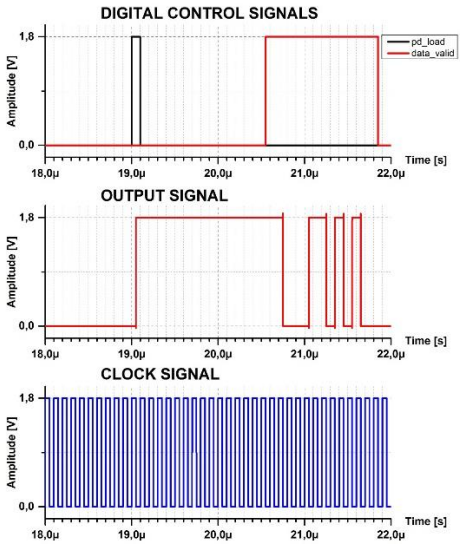

Figure 4.29 Simulation Result for Output Serializer.

4.4 Peripheral Blocks

Blocks that are explained throughout this section is designed to assist the comparators and ramp generators, by generating necessary bias voltages and digital control signals. Both blocks have programmability feature to select the bias voltages accurately and adjust the length of the time interval for any particular operation.

4.4.1 Bias Generator

The bias voltages and currents required for the operation of the designed ADC is supplied by the bias generator block. Bias generator is illustrated in Figure 4.30 on block level. It incorporates a bandgap voltage generator and feeds bandgap voltage as a reference voltage to various digital-to analog converters to obtain biasing voltages and currents.

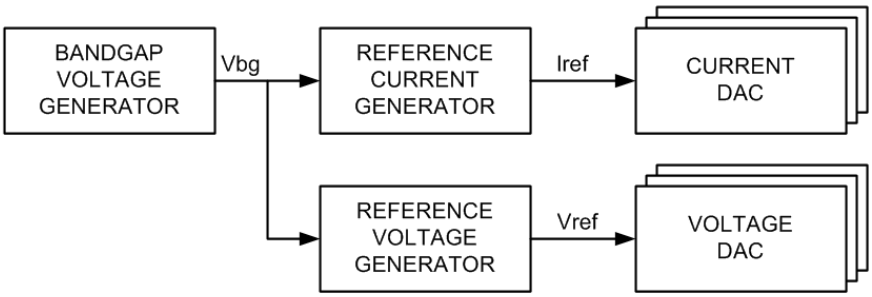

Figure 4.30 Bias Generator Block Diagram.

The biasing currents are generated with the structure shown in Figure 4.9. By transferring the gate voltage of the PMOS device at the output of the amplifier to other PMOS devices with different W/L ratios, a programmable current DAC is realized.

The bias voltages for the amplifiers are produced by the means of voltage DACs. Using a resistive DAC structure and a bandgap originated reference voltage, biasing voltage is generated and buffered to be connected to the required node.

4.4.2 Digital Controller

Digital Controller is designed to provide the necessary timing signals for the designed ADC. The global counter block, whose outputs are shared by all the column-parallel comparator, is also included within this block.

An internal counter, whose counting cycles are controlled by an external pulse, is implemented within digital control block to aid the generation of the timing signals. Digital equality-checker blocks for each timing signal uses this counter output to compare with the programing data and generates the output signal. In order to receive the programming data, digital controller block includes a 4-wire Serial Peripheral Interface protocol. Received data is stored in digital memory structure. Note that SPI and memory structures also serves to provide the trimming data for the voltage and the current DACs as mentioned in previous section.

The schematic of a single signal generation block is given on the Figure 4.31. The details of the digital control signal generation can be given as follows:

- An external pulse resets the counter and triggers the counting process with its falling edge. The frequency of this pulse also determines the sampling rate of the designed ADC.
- For any digital signal to be generated, the start and the end coordinate values with respect to the counter output is received from the SPI.
- By using digital equality checkers, active high rise and active low fall pulses for each control signal is generated. These rise and fall pulses are fed to the clock and the reset inputs of a D Flip-Flop respectively. Using these pulses, required signal is generated.

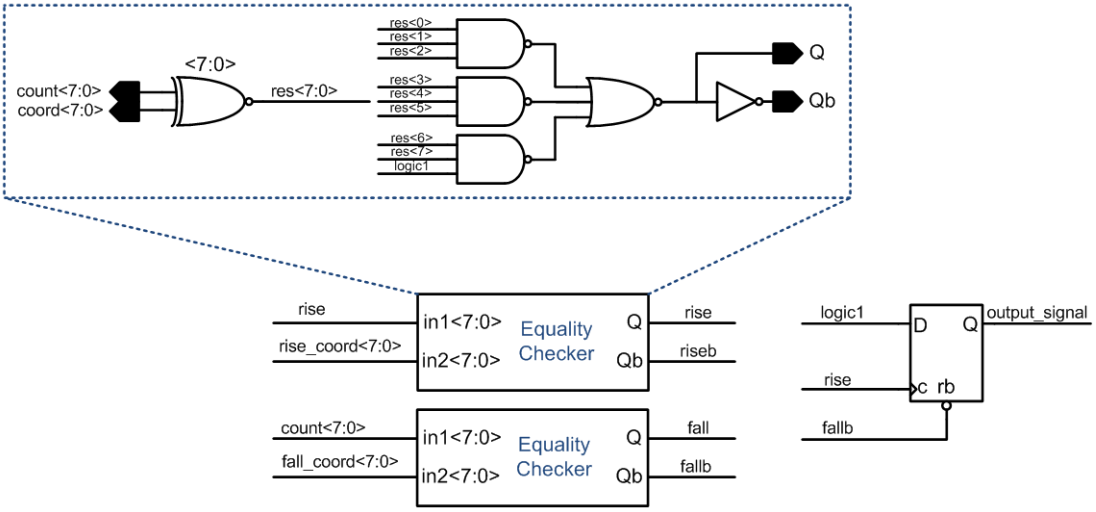

Figure 4.31 Digital Signal Generation Block.

The global shared counter is also implemented within this block. The counter needs to count down from 63 to 0 in the coarse conversion phase, and from 95 to 0 in the fine conversion phase, therefore a 7-bit, parallel loadable, up-down counter is designed. Before the start of the coarse and the fine conversion phases, the binary data corresponding to 63 and 95 is loaded onto the counter and with a count enable signal, generated with the above-mentioned method, counting is performed. The counter output is driven with strong buffers in order not to suffer from the long rise and fall times due to the parasitic capacitance of the conduction paths. Schematic of the designed counter block is given in Figure 4.32.

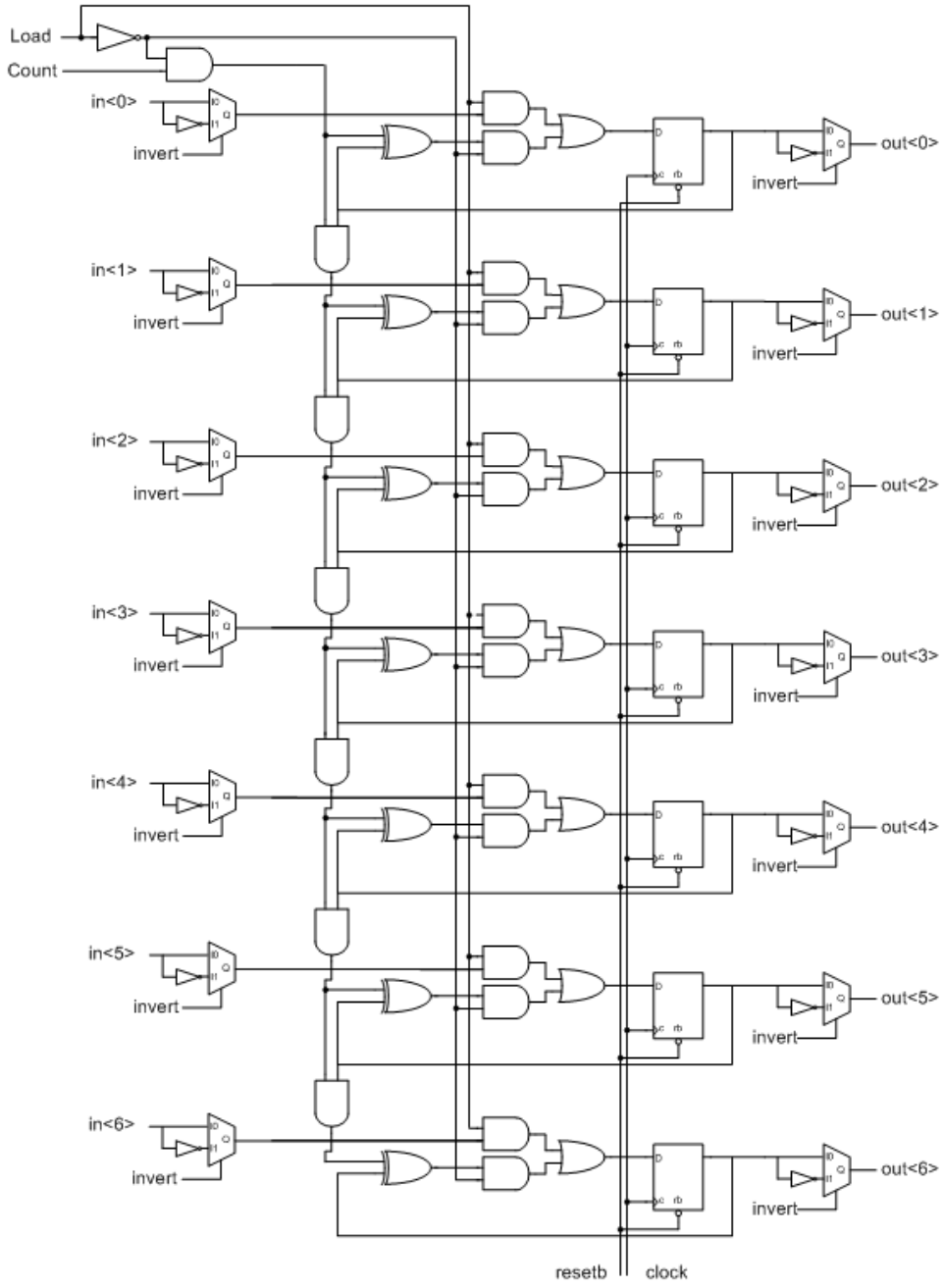

Figure 4.32 Global Counter Schematic.

4.4.2.1 Serial Peripheral Interface

The communication with external electronics of the IC is dealt with the usage of a standard 4-wire Serial Peripheral Interface. 4 signals used in SPI is provided on Table 4.9. Data transfer of 24-bits with 1-bit Read/Write option, 7-bit address, and 16- bit data is implemented.

Table 4.9 SPI Communication Signals.

Signal Name	Direction	Polarity	Purpose
sclk	input	-	Clock signal for synchronization
sdatain	input	-	Serial data input
senb	input	active low	Communication enable signal
sdataout	output	-	Serial data output

For data transfer, MSB first approach is employed. First bit of the received 24-bit data denotes the purpose of the operation, whether the data is sent to write on or read from a specific register. The succeeding 7-bits are address bits, pointing the address of the register and the remaining 16-bits are the data to be sent. If it is a read operation, received 16-bit data is discarded. Data transfer scheme is illustrated in Figure 4.33. *senb* toggles to LOGIC 0 level to initiate the start of the operation. At each rising edge of the *sclk*, a new bit is send via *sdatain* terminal and the present data is shifted into the input shift register at the falling edge of the *sclk.* At the end of the data transfer, if a write command is received, the 16-bit data on the input shift register is loaded onto the specific register marked by the 7-bit address word. Elsewise, the content of the register pointed by the 7-bit address word is loaded onto the shift register and transferred to the master device of the SPI communication (e.g. a microcontroller or a Field Programmable Gate Array).

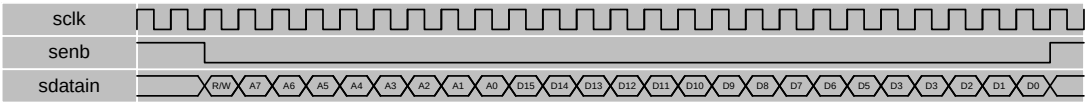

Figure 4.33 General SPI Timing Diagram.

64 registers with the storage capability of 16 bits are implemented for memory. 19 registers are dedicated for the digital signal generator block, whereas 32 registers serve analog circuitries and 13 of registers are left idle.

CHAPTER V

LAYOUT OF THE DESIGN

The final step of the physical implementation of the designed prototype is the layout of the blocks detailed in Chapter 4, the pad-frame and the top-level layout of the full structure. This part starts with a of discussion on the top-level planning of the full layout followed by the details of the block level layouts. The top-level layout will be demonstrated at the end.

A commercial 180nm CMOS process is used to draw the layout of the design. Except for the pads and standard digital cells, all layouts are custom made.

5.1 Planning of Block Placement

The pad-frame is divided into two by power-cut cells, to isolate the analog signals and the power supplies from the digitals signals and the power supplies. The top and the right parts of the pad-frame serve the analog signal paths, whereas the left and the bottom parts of the pad-frame, is responsible for the conduction of digital signals and power supplies. Blocks are placed to keep the power supply and signal routing distance at a minimum. In Figure 5.1, top-level block placement plan can be seen.

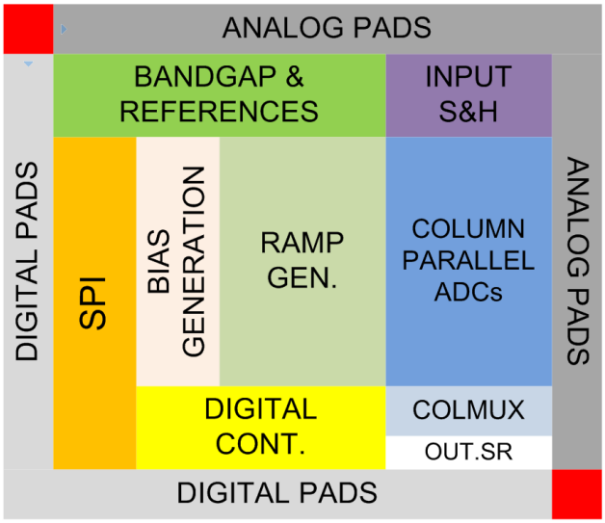

Figure 5.1 Layout Floorplan of the Designed IC.

5.2 Block Layouts

5.2.1 Coarse Ramp Generator

Layout of the coarse ramp generator is shown in Figure 5.2. Matching of the capacitors on the capacitor array and the feedback capacitor is very crucial for the linearity of the ADC. Therefore, layout of these capacitors is handled with using the same unit cell capacitors and exactly same distances between the devices. Dummy capacitors, whose both plates are connected to the ground voltage, are placed on the perimeter of the capacitor array. Connections for feedback loop is done so that it introduces the minimum parasitic capacitance to the circuitry.

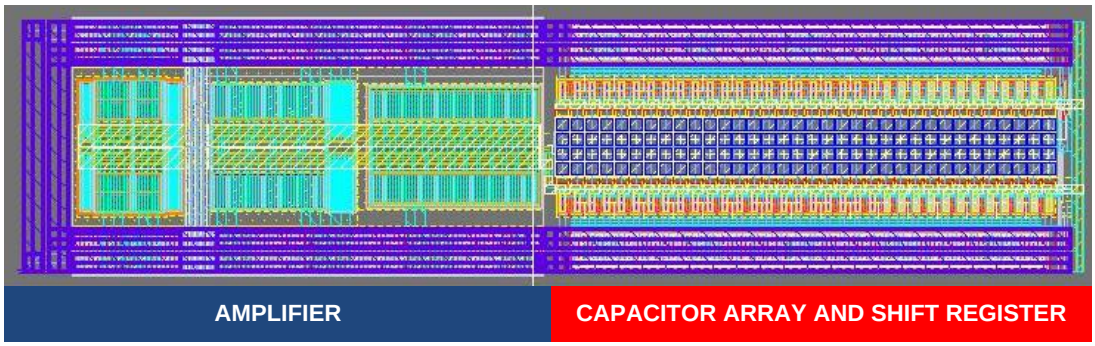

Figure 5.2 Layout of Coarse Ramp Generator.

Layout of the coarse ramp generator occupies an area of 835µm ×199 µm.

5.2.2 Fine Ramp Generator

Physical implementation of the 7-bit fine ramp generator is shown in Figure 5.3.

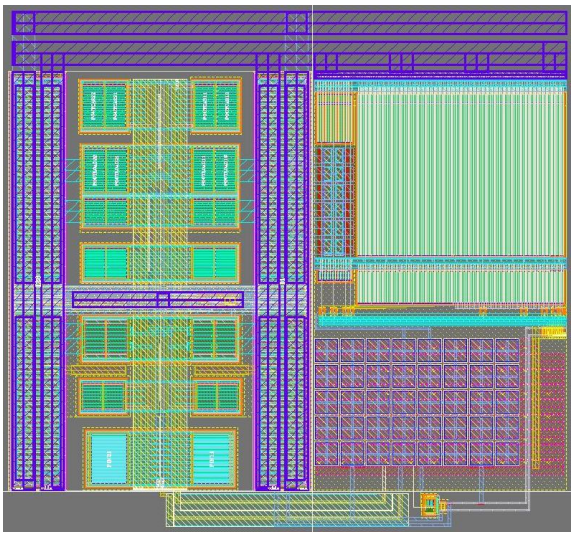

Figure 5.3 Layout of the Fine Ramp Generator.

The amplifier is placed on the left side of the layout. On the top-right, the 9-bit current DAC is implemented. The integration capacitor is positioned on the bottom right with the use of 40 unit-cell capacitors. For the fine ramp generators with 6-bit, 5-bit, and 4-bit resolutions, the number of unit cell capacitors are reduced to 20, 10, and 5, respectively. Dimensions of fine ramp generator are 340µm ×360 µm.

5.2.3 Column-Parallel Comparator Layout

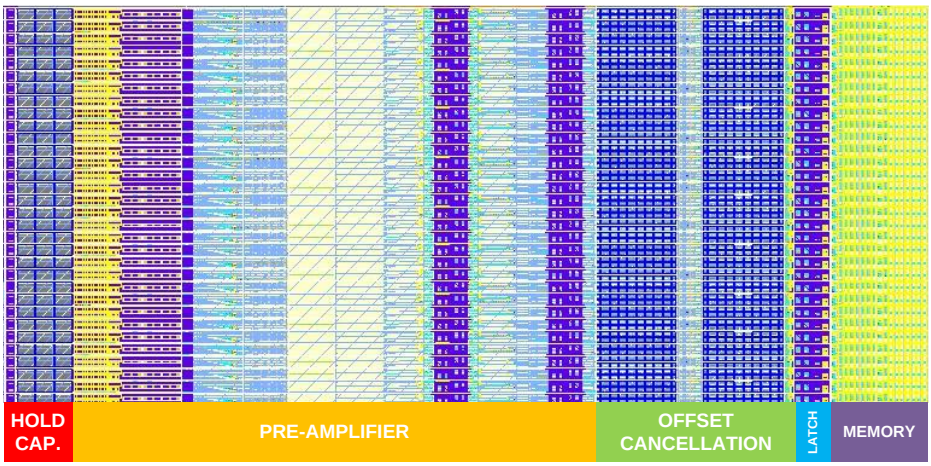

Figure 5.4 Layout of Column-Parallel Comparators including Pre-Amplifiers, Latches, Memory Circuits, and Logic Blocks

Layout of the column-parallel comparator is the most challenging part, due to the narrow column pitch, which is 13.4 µm, as provided in Table 2.1. Figure 5.4 demonstrates sixteen columns that are placed right next-to each other. The 4-input pre-amplifier is the block that occupies the most of the area. Height of a single column is 1mm.

5.2.4 Digital Controller Layout

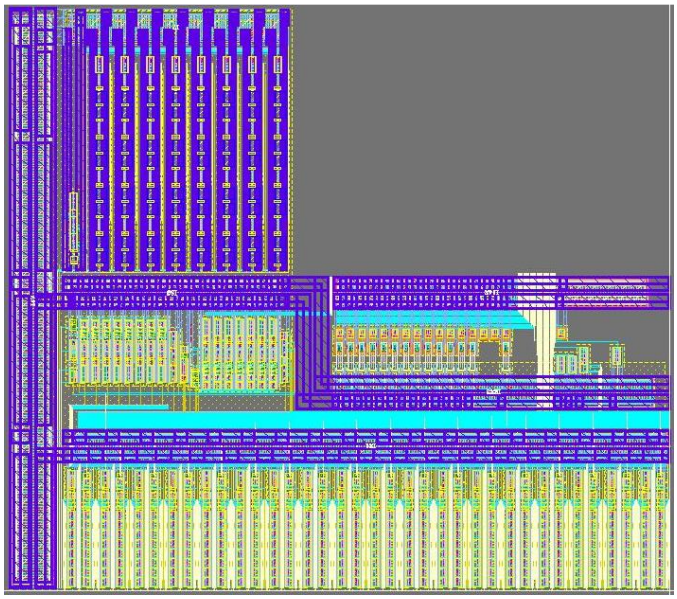

Figure 5.5 Layout of the Digital Controller

In Figure 5.5, digital controller block layout is shown. Digital programming bit inputs are fed from the bottom side. This block also includes 1.8 V to 3.3 V level shifters, since all the digital circuitry works with the 1.8 V supply and the digital signals on the 3.3 V regime is required for the analog circuitries. The layout size of the digital controller block is 480 µm × 420 µm.

5.2.5 Column Multiplexer Layout

The column multiplexer layout is drawn with the 13.4 µm pitch, as the column-comparator outputs are provided with this step size. Since a lot of digital activities happen on this block, decoupling capacitances are placed beneath the supply routings, as can be seen from Figure 5.6. Layout of the column multiplexer has 200 µm height.

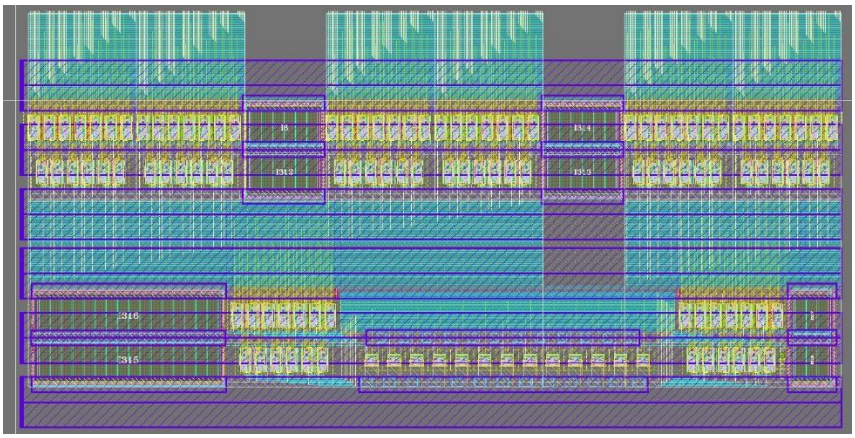

Figure 5.6 Layout of the Column Multiplexer.

5.2.6 Output Serializer Layout

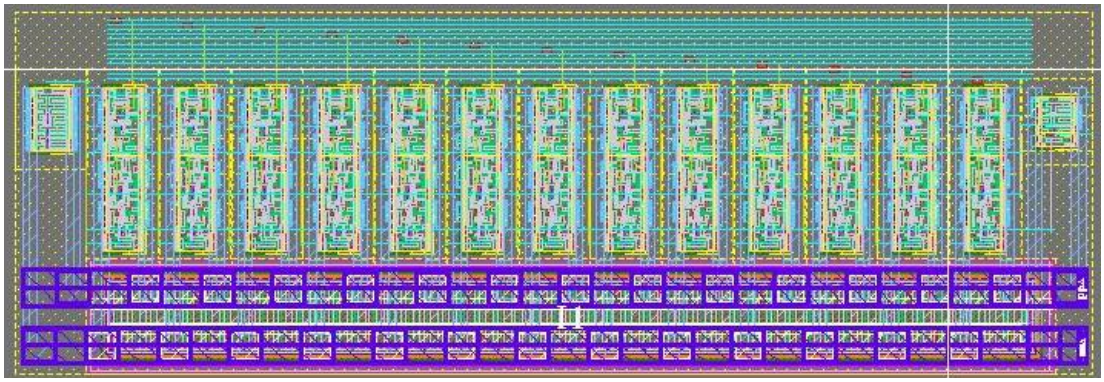

Figure 5.7 Layout of the Output Serializer.

The output serializer layout is demonstrated in Figure 5.7. Thirteen identical digital blocks on the middle are the 4x1 multiplexers and the D Flip-Flops. On the left and right sides, the output and the clock buffers are placed respectively. The area occupied by the output serializer block is 150 µm × 50 µm.

5.3 Top-Level Layout

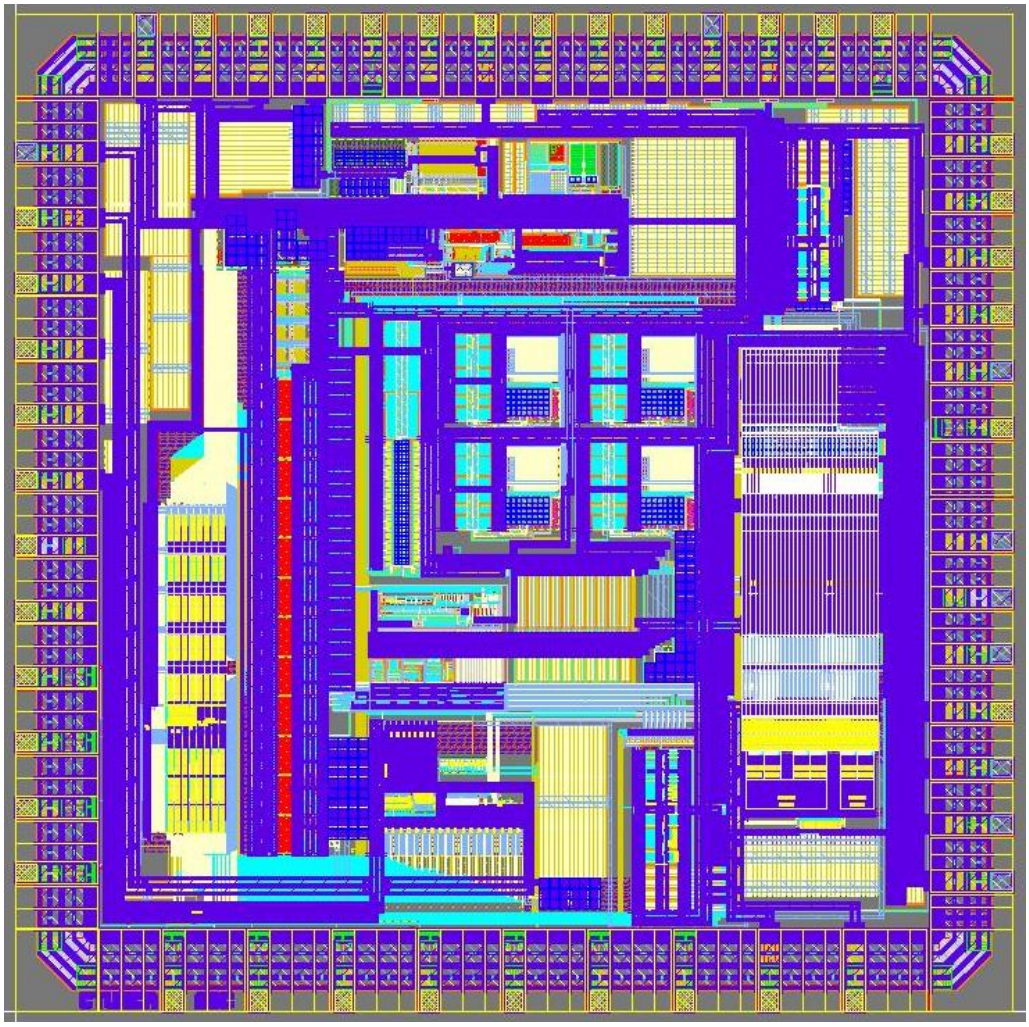

Figure 5.8 Layout of the Prototype IC.

The top-level layout involving all the major functional blocks described in Chapter 4, alongside with the pad-frame and the inter-block routings is shown in Figure 5.8.

The size of the prototype IC is 3.15 mm by 3.15 mm, however, height of the pad-frame comprised of the pad-limited cells is around 250 μm. Therefore, the core area of the prototype IC is approximately 2.6 mm by 2.6 mm.

CHAPTER VI

TOP LEVEL SIMULATION RESULTS

Designed ADC is simulated in detail, in order to verify the performance. In these simulations, all the functional blocks mentioned in Chapter 4 is employed. Simulations are run in SPICE environment.

6.1 Top-Level Transient Simulations

The purpose of these simulations is to check if the ADC produces the accurate outputs at the end of the conversion. Two conversion cycles are simulated for both the Two-Step Single-Slope and the Two-Step Multi-Slope modes of operation, for two different analog input levels. Desired digital output is calculated and compared with the conversion results.

6.1.1 Two-Step Single-Slope Mode Simulation

The ADC outputs for two sampled analog input voltages are shown in this section. Input voltage for the first and second conversion cycles are $V_{in1} = 1.04\,V$ and $V_{in2} = 2.76\,V$ respectively.

Expected conversion results in the decimal form can be calculated by using equation (6.1),

$$Output = \frac{V_{in} - V_{refL}}{V_{refH} - V_{refL}} \times 2^N, \tag{6.1}$$

where N is the aimed resolution for conversion.

Hence, the expected digital output values for V_{in1} and V_{in2} are calculated as follows:

$$Output_{V_{in1}} = \frac{1.04 - 0.9}{2.9 - 0.9} \times 2^{12} = (286{,}72)_{10}, \tag{6.2}$$

$$Output_{V_{in2}} = \frac{2.76 - 0.9}{2.9 - 0.9} \times 2^{12} = (3809{,}28)_{10}. \tag{6.3}$$

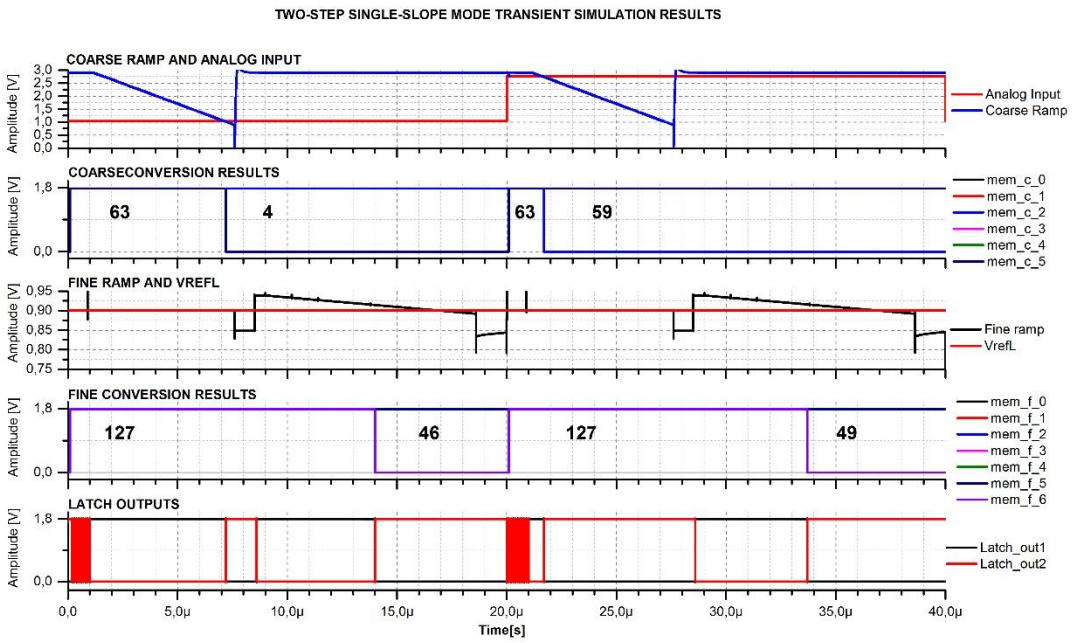

Figure 6.1 Transient Simulation Results for Two-Step Single-Slope Mode.

Figure 6.1 illustrates the transient simulation results for the Two-Step Single-Slope mode of the designed ADC. The conversion results are shown on the figure and binary-to-decimal converted values are annotated on the plots. Acquired values are for V_{in1} and V_{in2} are:

$$Out\_coarse_{V_{in1}} = (4)_{10}, Out\_fine_{V_{in1}} = (46)_{10}\,, \tag{6.4}$$

$$Out\_coarse_{V_{in2}} = (59)_{10}, Out\_fine_{V_{in2}} = (49)_{10}. \tag{6.5}$$

Outputs for the coarse and the fine conversion results are re-calculated using the algorithm presented in Figure 3.8. As the fine conversion results for both outputs are in the mid-band of fine conversion, no alteration is done on coarse conversion results.

Fine conversion results are re-calculated to yield the result in the mid-band, by subtracting 16 from the results. Achieved results are;

$$Output_{V_{in1}} = 4 * 64 + (46 - 16) = (286)_{10}, \quad (6.6)$$

$$Output_{V_{in2}} = 59 * 64 + (49 - 16) = (3809)_{10}, \quad (6.7)$$

Acquired results are within 1 LSB proximity for the both inputs and very satisfactory.

6.1.2 Two-Step Multi-Slope Mode Simulation

Similar to the Section 6.1.1, the ADC outputs for two sampled analog input voltages, which are $V_{in1} = 1.04\ V$ and $V_{in2} = 2.76\ V$, are demonstrated in this part.

Note that on this simulation, conversion results have different resolutions. As V_{in1} and V_{in2} reside in 1st and 4th bands of conversion range respectively, obtained resolutions will be 12-bits for V_{in1} and 9-bits for V_{in2}.

Expected outputs for two successive conversions are calculated using equation (6.1) and given as follows:

$$Output_{V_{in1}} = \frac{1.04 - 0.9}{2.9 - 0.9} \times 2^{12} = (286{,}72)_{10}, \quad (6.8)$$

$$Output_{V_{in2}} = \frac{2.76 - 0.9}{2.9 - 0.9} \times 2^{9} = (476{,}16)_{10}. \quad (6.9)$$

Figure 6.2 depicts the transient simulation results for the Two-Step Single-Slope mode of the designed ADC. Alongside with the conversion results, binary-to-decimal converted values are annotated on the plots. Acquired values are for V_{in1} and V_{in2} are:

$$Out\_coarse_{V_{in1}} = (4)_{10}, Out\_fine_{V_{in1}} = (46)_{10}\ , \quad (6.10)$$

$$Out\_coarse_{V_{in2}} = (59)_{10}, Out\_fine_{V_{in2}} = (90)_{10}. \quad (6.11)$$

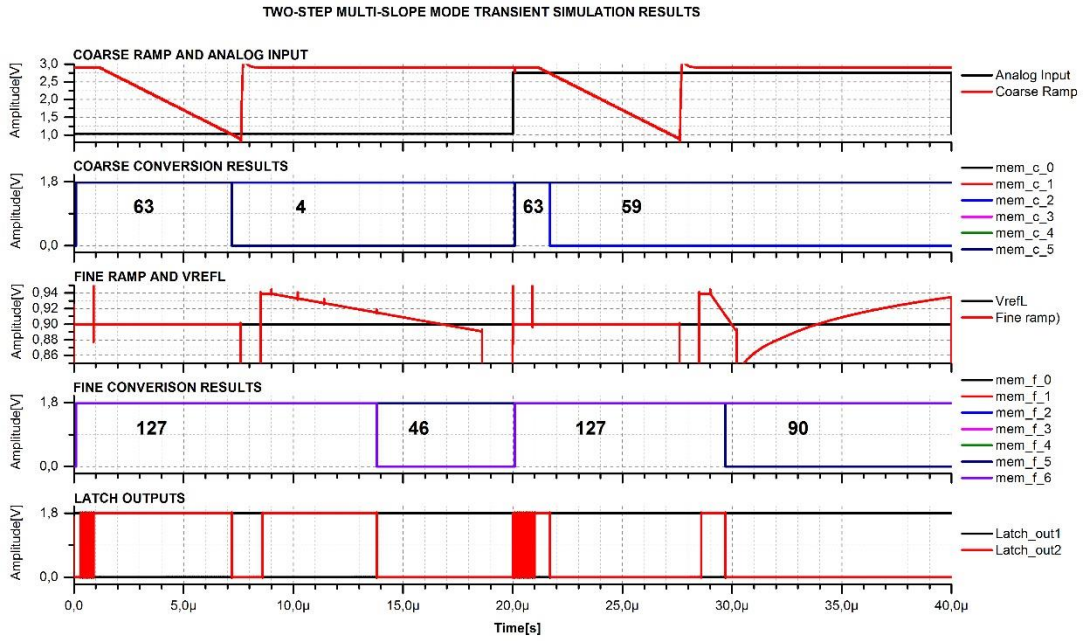

Figure 6.2 Transient Simulation Results for Two-Step Multi-Slope Mode.

The reason of increase on the fine conversion result of V_{in2} compared to the TSSS mode results is due to the increased slope of the fine ramp. Fine conversion is completed within 12 clock cycles for V_{in2} in TSMS mode, whereas it took 96 clock cycles in the TSSS mode. Since separate counters are not implemented for different regimes for TSMS mode, output value is provided over 96 clock cycles.

For obtaining the final outputs, steps on the output re-calculation algorithm is performed again. For TSMS mode, algorithm demonstrated in Figure 3.8 needs to be re-scaled for different bands. According to the re-scaled algorithm, acquired results are given as follows:

$$Output_{V_{in1}} = 4 * 64 + (46 - 16) = (286)_{10}, \quad (6.12)$$

$$Output_{V_{in2}} = 59 * 8 + \big((90 - 84) - 2\big) = (476)_{10}. \quad (6.13)$$

Note that the weight of the coarse conversion is reduced from 64 to 8 and the number of counts separated for regimes above and below the main band decreased from 16 to 2. Simulation results for the TSMS mode are also within 1 LSB proximity of the desired result.

6.2 Out of Range Recovery Simulation

In order to check the behavior of the ADC for analog inputs that are outside its conversion range, the out-of-range simulation is performed. As described in Section 4.2.4, if no decision is performed on the coarse conversion, ADC prohibits the fine conversion phase, since the fine ramp reaches outside the conversion range. Thus 13-bit output of all LOGIC 1s are provided at the output.

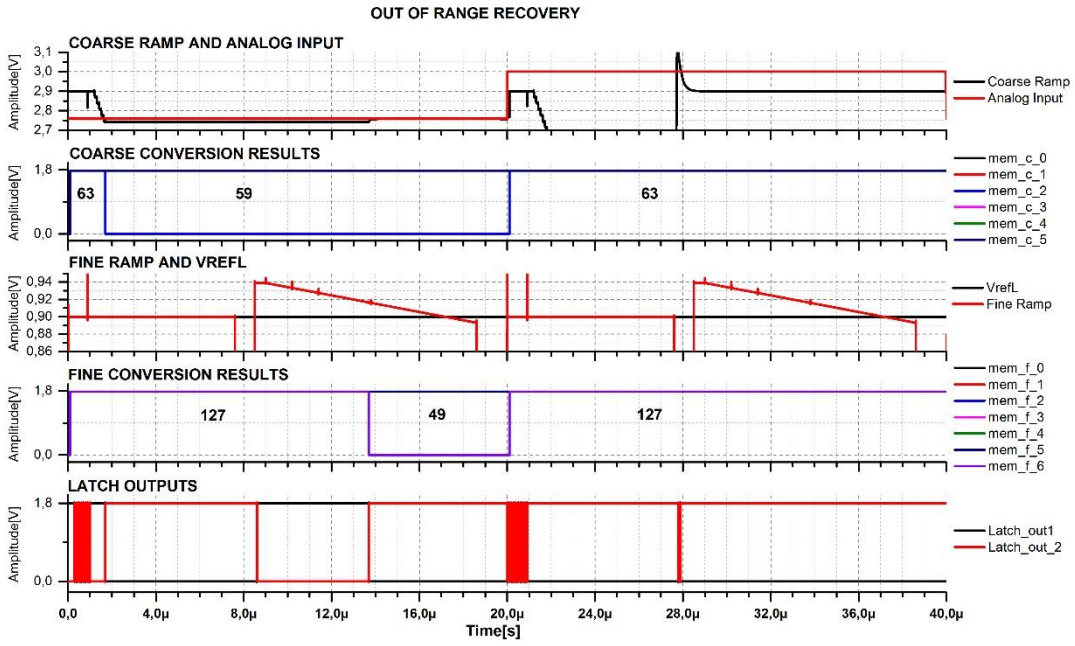

Figure 6.3 Out of Range Simulation Results.

Figure 6.3 depicts the analog to digital conversion of two inputs, where the second input is 3V, an out of range value. ADC performs the conversion successfully on the first step, however, no decision is performed on the second step and the coarse and the fine conversion results of $(63)_{10}$ and $(127)_{10}$ is given to the output. This way, the user/tester is informed that the second analog input voltage is out-of-range.

6.3 Power-Cut Function Simulation

The power-cut function is implemented to reduce the power consumption, by disabling the column level pre-amplifiers and dynamic latches after the fine conversion is completed. This function is governed by the logic blocks employed in column-parallel comparators. Figure 6.4 illustrates the effect of power-cut function on the current dissipated by the pre-amplifier inside the column-parallel comparators. The current

drawn from the positive supply is at 40 µA level while the pre-amplifier is enabled. After being disabled, current value dissipated by the pre-amplifier reduces to few nAs. By exploiting power-cut function, power consumption can be reduced up to 30% for the Two-Step Single-Slope mode. Moreover, while operating in the Two-Step Multi-Slope mode, power can be conserved up to 41%, which is the main reason of integrating multi-slope function to the designed ADC.

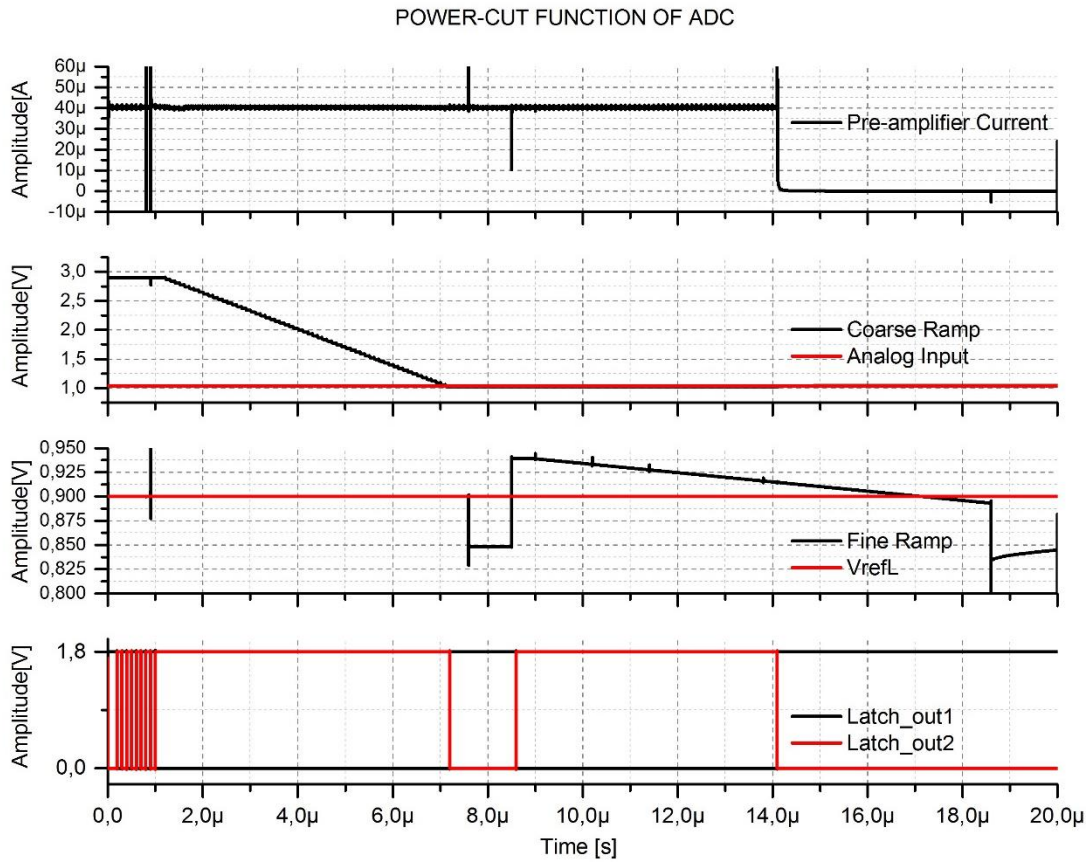

Figure 6.4 Simulation of Power-Cut Function.

6.4 Readout Simulation

The co-operability of the column-parallel analog to digital converters, the column multiplexer, and the output serializer blocks are simulated and results are provided in Figure 6.5. The resultant binary data belonging to analog input of $V_{in} = 1.75\ V$ is read out after the end of the first conversion. Expected output from $V_{in} = 1.75\ V$ is calculated on equation (6.14).

$$Output_{V_{in}} = \frac{1.04 - 0.9}{2.9 - 0.9} \times 2^{12} = (1740{,}8)_{10}. \quad (6.14)$$

Acquired data from the simulation gives the result provided on equation (6.15).

$$Output_{V_{in1}} = 27 * 64 + (30 - 16) = (1742)_{10}, \quad (6.15)$$

An error equal to 1.2 LSB is present on the outputs, which is reasonable due to the non-idealities on coarse ramp and charge injection of the hold switch driving the hold capacitor at the input of the pre-amplifier. These errors can be corrected by adjusting the VrefL and VrefH voltages to get ideal swing on the coarse ramp.

On the other hand, conversion results are successfully read-out via output shift register as Figure 6.5 shows. Binary equivalent values of the coarse and the fine conversion outputs are provided on equations (6.16) and (6.17).

$$Out_{coarse} = (27)_{10} = (011011)_2 \quad (6.16)$$

$$Out_{fine} = (30)_{10} = (0011110)_2 \quad (6.17)$$

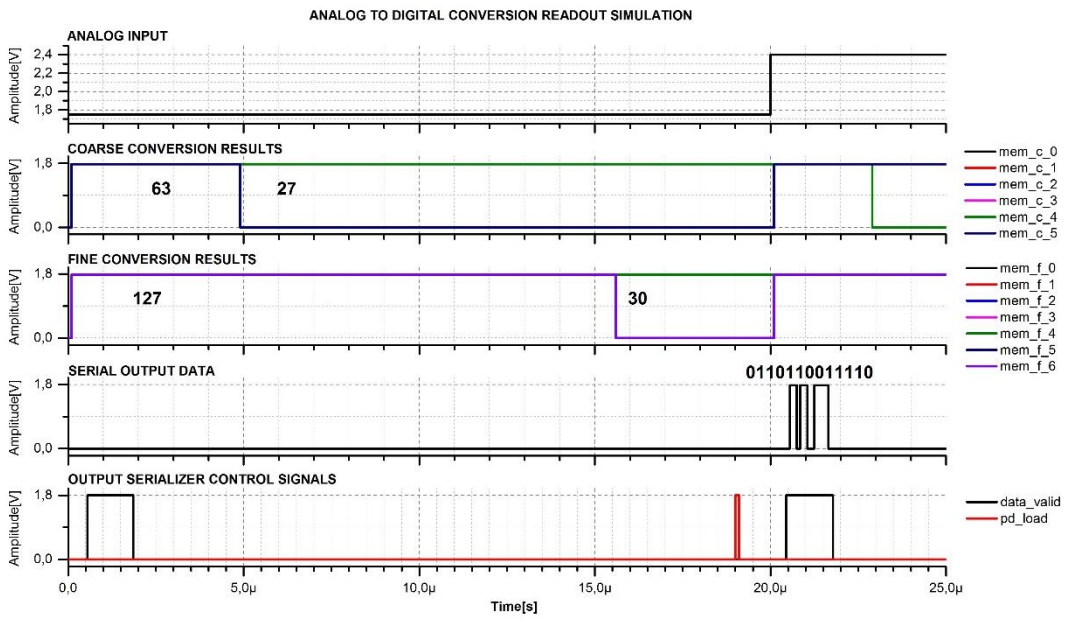

Figure 6.5 Digital Data Read-out Simulation

With *pd_load* pulse, resultant binary data on column-parallel ADCs are multiplexed down to a single 13-bit data and transferred out of the chip with the MSB first approach.

6.5 Fast Fourier Transform Simulations

Signal to Noise and Distortion Ratio is a good indicator of ADC's dynamic performance as it includes the disturbances due to noise, harmonics and non-linearity sources. SNDR is generally converted into Effective Number of Bits to represent the ADC's performance in terms of resolution. The relationship between the SNDR and ENOB is provided in equation (2.22).

A popular method to calculate the SNDR and ENOB values of an ADC is the Fast-Fourier Transform spectral analysis. Fast Fourier Transform is an algorithm to calculate the Discrete Fourier Transform, in which a sampled periodic time domain signal is dissolved into sinusoids with different frequencies. To perform FFT analysis, a single tone sinusoidal input is sampled with the sampling frequency f_s and $M = 2^K$ point conversion is performed by the ADC. In order to prevent the spectral leakage and folding back of harmonics, a certain restriction is present between the sampling frequency, input sine wave frequency, and the number of conversions, i.e. M. Relationship between these parameters can be described as follows:

$$f_{in} = f_s \times \frac{M_c}{M} \text{ [Hz]}, \tag{6.18}$$

where M_c is the integer number of periods of sine input contained within M-point time window. Decision of M_c is advised to be a prime number to prevent the folding back of early harmonic components into Nyquist region [43], [44]. Elsewise, usage of windowing functions would be necessary to suppress the effect of harmonics. Another point to be mentioned here is that, with M getting larger, improved frequency resolution and noise floor values can be obtained. However, larger number of samples drastically increases the simulation time on the SPICE environment.

Under the light of these information, an FFT analysis is performed with 50 kHz sampling frequency, 128 data points, and M_c being 7. Using these values, frequency of the input sine voltage is calculated as:

$$f_{in} = 50\ kHz \times \frac{7}{128} = 2.734375\ kHz. \tag{6.19}$$

A full-scale sine wave, with the frequency value provided on equation (6.19) is generated and sampled with f_s on the MATLAB software. Then, these sampled values are written into a text file and fed to the transient simulation as the ADC input data. Note that the simulation includes noise components up to 100MHz. Using a Verilog-A script, the simulation output generated by the ADC is written into a text file and this text file is fed back to the MATLAB software. Employing the FFT algorithm provided in [45], following results are obtained.

In Figure 6.6, FFT analysis of the designed ADC at 27 °C temperature is presented. Obtained 70.38 dB SNDR corresponds to 11.398-bit ENOB value, which is comparable to the literature standards on the Two-Step Integrating ADCs.

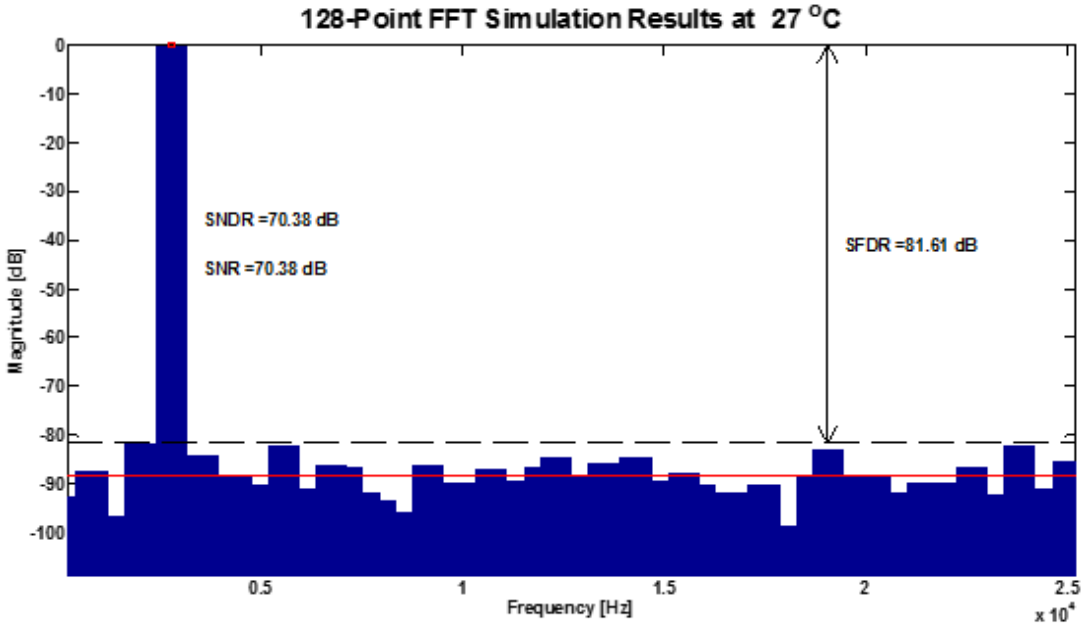

Figure 6.6 FFT Analysis Results by 128 Points at 27 °C

Figure 6.7 demonstrates the FFT Analysis results at 85 °C temperature corner. A slight decrease on the SNDR value is expected at 85 °C, due to the nature of the thermal noise sources. On this simulation, 70.12 dB SNDR value is achieved, which equals to 11.35-bit ENOB performance.

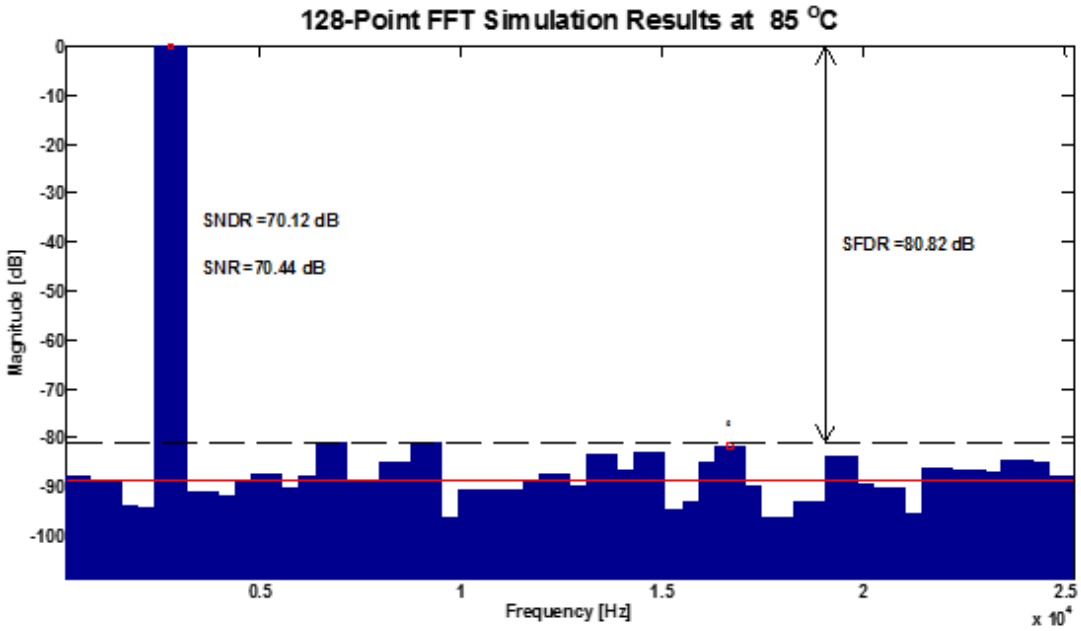

Figure 6.7 FFT Analysis Results by 128 Points at 85 °C

FFT Analysis results on -40 °C temperature is depicted in Figure 6.8. Noise generation within circuitries is reduced at this temperature, however, increased MOS threshold voltage introduces additional non-linearity and limits the SNDR to 68.78 dB. This SNDR value corresponds to 11.13 bit ENOB performance.

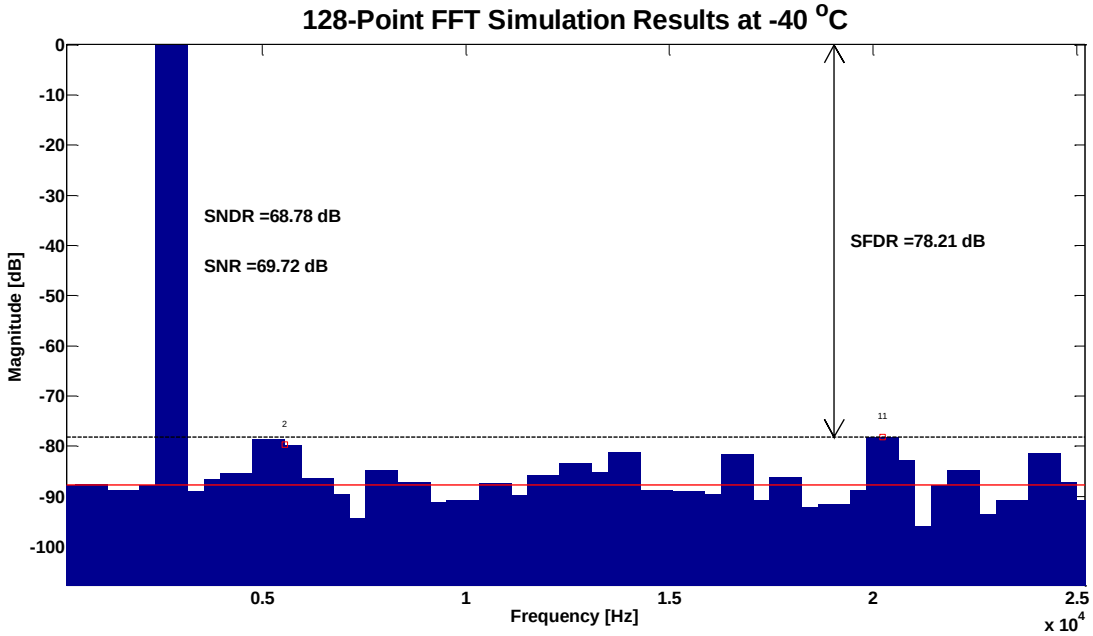

Figure 6.8 FFT Analysis Results by 128 Points at -40 °C

The ADC outputs are fed to an ideal DAC formed in MATLAB software and sampled sine wave is reconstructed. Comparison of the input sine wave and the ADC output is overlaid as shown in Figure 6.9. No apparent distortion is observable on this plot.

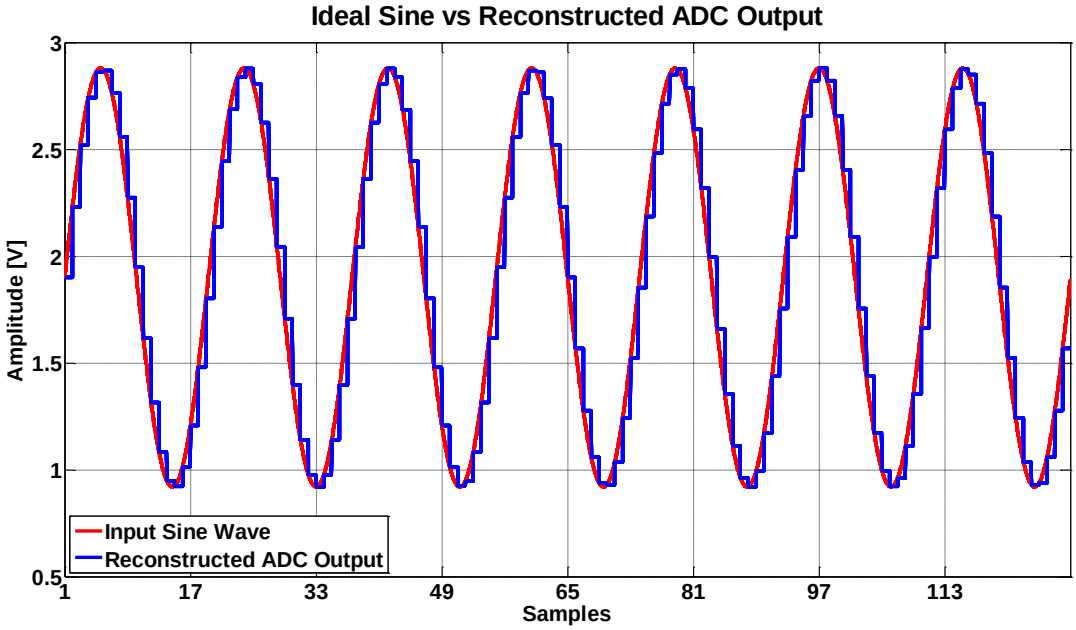

Figure 6.9 Comparison of Input Sine Wave with Reconstructed ADC Output

6.6 Summarized Results

In order to provide an overview of the performance of the designed ADC, several evaluation metrics are provided on **Error! Not a valid bookmark self-reference.**.

Table 6.1 Performance Summary of the Designed ADC.

Parameter	**Description**
Technology	0.18 µm
Power Supply	3.3 V (Analog) & 1.8V (Digital)
Column Pitch	13.4 µm
Sample Rate	>50 ks/s
ADC Resolution	12-bit
ADC Clock	10 MHz
ENOB	11.4-bit
ADC Input Range	2 V
Column ADC Average Power Consumption	88 µW

Presented values are obtained in the simulation environment. Integrated Non-Linearity, Differential Non-Linearity, and histogram measurements of the ADC will be completed after the manufactured samples are acquired.

CHAPTER VII

CONCLUSION AND FUTURE WORK

The research conducted within this thesis is focused on the design of a column-parallel Two-Step Multi-Slope ADC for CMOS image sensors. Since the pixel type and array format is not specified, the effort is spent on developing an ADC with the optimum performance. The summary of the work carried on in this thesis is listed below:

1. A column- parallel ADC with Two-Step Multi-Slope architecture is designed for a 6.7 μm pixel pitch. Columns are designed such that designed ADC will be placed both on the top and the bottom sides of the array, and will have two pixels' width.
2. By virtue of the Two-Step Multi-Slope mode and the power down functionality on the designed ADC, average power consumption is reduced up to 41 % by disabling the column level pre-amplifiers and the dynamic latches upon the completion of the conversion.
3. A digital controller is implemented in order to communicate with the external electronics on the test board.
4. Digital control signals and biasing voltages are generated internally and can be programmed by the implemented serial programming interface. Thanks to this programmability feature, digital control signals' start coordinates and widths can be programmed with 1 clock cycle resolution. Furthermore, internal bias voltages and currents have 12-bit and 8-bit programmability feature respectively.

5. In order to not to suffer from process, temperature, and voltage mismatches, fine ramp generators are implemented with a 9-bit calibration capability.
6. Design is carried out in a 0.18 μm CMOS process. Layout of the prototype IC has dimensions of 3.14 mm × 3.14 mm and fabrication is on progress.
7. Thorough sub-block and top level simulations are performed to validate the functionality.

A comparison of the designed ADC with the other examples on the literature can be found on Table 7.1. Designed ADC stands on a good position in terms of power consumption and effective resolution. Conversion time can be decreased down to 15 μs, by increasing the clock frequency up to 12 MHz and removing the dead time between the coarse and the fine conversion phases. This would create no problem as the settling time of the coarse ramp generator and the response time of the column pre-amplifiers are shorter than ½ clock cycle duration of the 12 MHz clock.

Table 7.1 ADC Performance Comparison

Reference	[27]	[5]	[46]	[47]	**This Work**
Technology	0.18 μm	0.25 μm	0.25 μm	0.35 μm	0.18 μm
Architecture	Two-Step Single Slope	Multi-Ramp Multi-Slope	Two-Step Single Slope	Two-Step Single Slope	Two-Step Multi-Slope
Column Pitch	30 μm	7.4 μm	-	5.6 μm	13.4 μm
Conversion Time	36 μs	12.8 μs	2 μs	4 μs	<20 μs
ADC Clock	20 MHz	20 MHz	-	25 MHz	10 MHz
ADC Resolution	12-bit	10-bit	11-bit	10-bit	12-bit
ENOB	11.67-bit	-	10.3-bit	-	11.4-bit
ADC Input Range	-	1 V	1 V	-	2 V
Column ADC Power Consumption	128 μW	95 μW	170 μW	150 μW	88 μW

Design of the ADC and the verification of the system through SPICE simulations was an important step, however, there is some work remaining, waiting for the delivery of the manufactured samples. Moreover, to integrate the designed ADC to a full-functioning CMOS image sensor, several alterations need to be done on several sub-blocks. Planned work is detailed on the list below:

1. A Printed Circuit Board for the electrical tests of the designed ADC should be implemented.
2. Block level and the system level measurements should be done on the manufactured chips to check if the ADC meets the specifications of the design.
3. For integrating the ADC on a CMOS image chip, auto-calibration for fine ramp generators should be implemented. Furthermore, due to the large capacitive load that will be introduced at the output of the coarse ramp generator, an operational amplifier with the capability to drive large capacitive loads or column-level low-power voltage buffers should be designed.

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