FABRICATION OF THIN CRYSTALLINE SILICON SOLAR CELLS WITH ADVANCED LIGHT TRAPPING

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ABSTRACT

FABRICATION OF THIN CRYSTALLINE SILICON SOLAR CELLS WITH ADVANCED LIGHT TRAPPING

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Thin crystalline silicon (c-Si) solar cells with thickness in the order of few tens of microns offer many attractive applications, such as, electronic wearables, space probes and satellites thanks to their flexibility and light-weight character. However, reducing the thickness of active layer of silicon solar cells leads to poor light absorption within the silicon layer, especially in the near infrared region of the solar spectrum. The poor absorption becomes problematic for thin c-Si solar cells as it causes substantial photocurrent loss. One method to curtail the absorption loss is to incorporate light trapping structures into thin silicon. Light trapping structure of random upright pyramids has been proved efficient for conventional silicon solar cells allowing for easy and inexpensive method of texturization by alkaline-based solution. However, the average size of the randomized pyramids ranges from 4 - 10 μm which is not suitable geometry for thin silicon with thicknesses less than 20 μm. Recently, periodic submicron inverted pyramids have been shown to enhance absorption in thin c-Si solar cells. In this work, we fabricated flexible thin c-Si solar cells with advanced

light trapping of periodic inverted pyramids using relatively low-cost wet etching process as well as optimized random upright pyramids with maximum size of 2 μm for thin silicon. Efficiencies of 10.01% and 13.6% have been achieved for planar and textured silicon solar cells with a thickness of 30 μm, respectively. Thin c-Si solar cells were successfully attached to a polymer and removed from the initial wafer. In this thesis, we will discuss the fabrication process of flexible thin c-Si solar cells along with the fabrication of the advanced light trapping structures.

Keywords: Thin Silicon Solar Cells, Light Trapping, Random Upright Pyramid, Periodic Inverted Pyramids, Flexible Solar Cells

ÖZ

FABRICATION OF THIN CRYSTALLINE SILICON SOLAR CELLS WITH ADVANCED LIGHT TRAPPING

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Birkaç on mikrometre kalınlığa sahip ince kristal silisyum (k-Si) güneş gözeleri, esnekliği ve hafifliği sayesinde kıyafet, uzay aracı ve uydu gibi birçok ilgi çeken uygulama alanı sunmaktadır. Fakat silisyum güneş gözelerinin aktif tabakasının kalınlığının düşürülmesi, özellikle de güneş tayfının yakın kızıl ötesi bölgesinde, ışığın silisyum içerisinde zayıf soğrulmasına (absorpsiyonuna) sebep olmaktadır. Zayıf soğrulma ciddi bir foto akım kaybına sebep olacağından ince k–Si güneş gözeleri için problem olmaktadır. Soğrulma kaybını azaltmanın bir yöntemi silisyum içine ışık kapanlama yapılarını eklemektir. Alkali tabanlı solusyonda kolay ve ucuz dokulama yöntemi ile oluşturulan gelişigüzel dik piramit ışık kapanlama yapılarının konvansiyonel silisyum güneş gözeleri için verimi kanıtlandı. Fakat gelişigüzel piramitlerin ortalama boyutu 5-15 μm arasında değişmektedir ve bu 20 μm'den daha az kalınlıktaki ince silisyum için uygun değildir. Yakın zamanda, periyodik mikron altı ters piramitlerin ince k-Si güneş gözelerinin soğurmasını geliştirdiği gösterilmiştir. Bu çalışmada, göreceli olarak ucuz maliyetli ıslak aşındırma işlemini kullanarak

periyodik ters piramitlerle geliştirilmiş ışık kapanlamalı esnek ince k-Si güneş gözeleri ürettik ve maksimum 2 μm boyutundaki gelişigüzel ters piramitleri optimize ettik. Düzlemsel silisyum ve dokulu silisyum güneş gözeleri için sırasıyla 10.01% ve 13.6% verimleri elde edildi. İnce k-Si başarıyla polimer malzemeye tutturuldu ve başlangıç silisyumdan ayrıldı. Bu tezde, geliştirilmiş ışık kapanlama yapılarıyla birlikte esnek ince k-Si güneş gözelerini tartışacağız.

Anahtar Kelimeler: İnce Silisyum Güneş Gözeleri, Işık Kapanlama, Gelişigüzel Dik Piramit, Periyodik Altı Ters Piramit, Esnek Güneş Gözeleri

To my family

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NOMENCLATURE

Ag	Silver
Al	Aluminum
ARC	Antireflection coating
a-Si	Amorphous silicon
BSF	Back surface field
CdTe	Cadmium telluride
CIGS	Copper indium gallium sulfide
c-Si	Crystalline silicon
EQE	External quantum efficiency
FF	Fill factor
H2O2	Hydrogen peroxide
H2SO4	Sulfuric acid
HCl	Hydrochloric acid
HF	Hydroflouric acid
HNO3	Nitric acid
IPA	Isopropyl alcohol
Jsc	Short circuit current
JV	Current density-Voltage
KOH	Potassum hydroxide
MAE	Metal assisted etching
NH4F	Ammonium flouride
PECVD	Plasma enhanced chemical vapor deposition
PERC	Passivated emitter rear contact
PV	Photovoltaics
RCA	Radio Corporation of America
Si	Silicon
SiNx	Silicon nitride
SiO2	Silicon dioxide
UV	Ultraviolet

Voc	Open circuit voltage

CHAPTER 1

INTRODUCTION

Interest in harvesting energy from alternative sustainable resources other than natural gas and oil is steadily growing following the ever-increasing worldwide demand for energy consumption. These alternatives include nuclear, hydroelectric, wind, solar, tidal source, geothermal, just to name a few. Photovoltaics (PV), in particular, are promising technology for its direct conversion of energy from the Sun with its massive potentials. Ever since the first proposal of PV cells to be used as large-scale sustainable energy source, the industry has grown in a fascinating rate of more than 30% per year over the last decade [1]. In 2015 alone, 59 gigawatts for solar PV have been installed globally, which corresponds to an increase of 34% over the previous year. By the end of 2016, it is expected that 321 gigawatts will be installed in total [2]. In the United States, 2015 marks the year where solar exceeds energy addition of natural gas resource for the first time ever [3]. To say that solar PV is booming is really an understatement.

Until the last decade, however, PV was not considered as serious contender for energy source alternative owing to the fact that the technology was far more expensive than the others were, especially when compared to conventional fossil fuels. The applications of solar cells were limited to space application where power-per-weight ratio was crucial and cost was not of significance. Thanks to heavy investment in PV research, which led to advancement in the efficiency, the price continued to drop dramatically. Today, PV is regarded as one of the more efficient energy sources, in particular for those who need power in remote areas where there is no electrical grid.

The trend of price decline for solar module in the past 20 years can be observed from Figure 1.1, which indicates the learning rate of solar modules. Learning rate implies that for each time the cumulative production double, there is a decrease of

~20% in the price. Starting from early 2000, the price for solar module had decreased from around $5.50/Wp to just about $0.55/Wp in December 2015 [4]. The dramatic decline in the price is the result of improved module efficiency, reduction in raw material cost, simpler processing steps and up scaling in production plant.

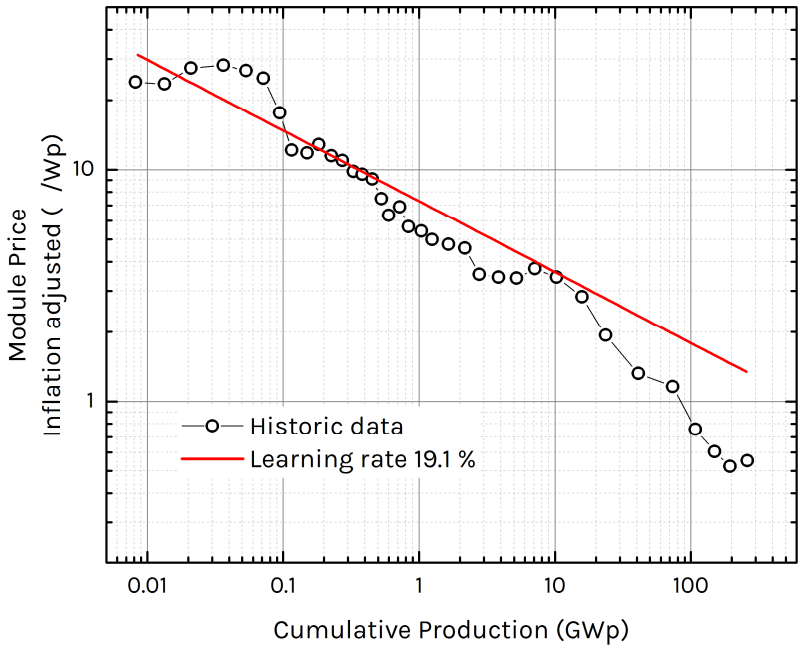

Figure 1.1 Learning curve of photovoltaics for the last 20 years [4].

Among PV technologies, silicon based solar cells have been dominating the market for a long time. Despite intense development over the last couple of decades in the second generation solar materials such as CIGS (Copper Indium Gallium Selenide), CdTe (Cadmium Telluride) and a-Si (Amorphous Silicon), the share in the market for these solar cell remains low and is expected to diminish even more in the upcoming years [5]. CdTe, for instance, is facing obstacles because Cadmium and Telluride are harvested as byproduct of zin and copper. It raises the question of availability of the material to fulfill the demand for mass production within a given year. The issue of Cadmium toxicity is also needed to be addressed for when CdTe to be used as mass-produced alternative energy source. CIGS, on the other hands, is relatively complex material and requires complicated process, which often involve toxic gases (e.g., H_2Se) for the selenization step. Obtaining reproducible large area CIGS modules has also proved to be problematic. This hinders the potential of CIGS being cost-competitive PV technologies [6]. The usage of In and Te which are rare

element might also pose long-term availability issues if CIGS and CdTe are to be chosen as main alternative for PV.

1.1 Thin Crystalline Silicon Solar Cells

Silicon solar cells, by far, have been dominating photovoltaics market with over 90% of the market share (Figure 1.2) [4]. This is mainly because silicon is very abundant on the earth crust and non-toxic material. These two factors are considered to be de-facto requirements of mass produced energy source. The other important factor that has fueled the emergence of silicon as solar cell material is the vast knowledge transferred from integrated circuit (IC) industry that preceded PV industry. Silicon solar cells share many common technologies with IC. This means that the developments of silicon solar cells need few adjustments from the already existing multibillion-dollar infrastructure and experience of IC.

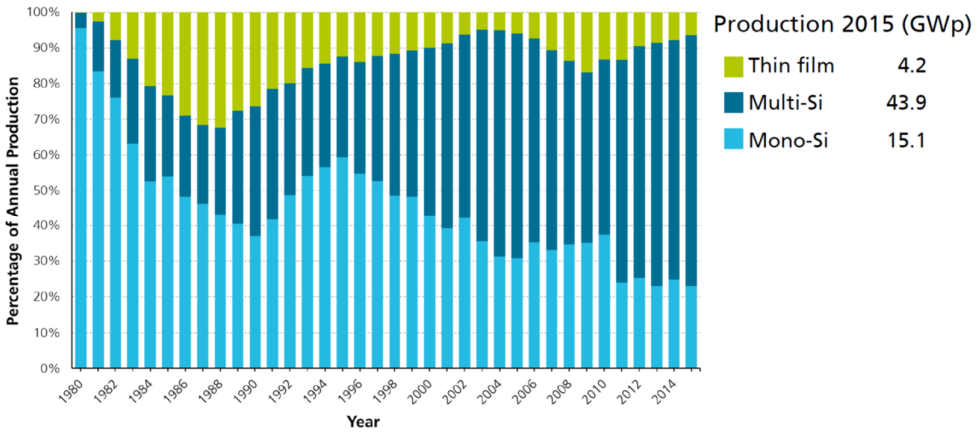

Figure 1.2 PV annual production in the last two decades [4].

Since its first realization of solar cell from silicon in Bell lab in 1954 with an 6% efficiency [7], continuous improvement in the efficiency has been observed over the last decades. The current record efficiency of silicon solar cell sits at 26.3% which is just slightly below the theoretical efficiency limit of 29% [8]. While in commercial silicon wafer based solar modules, the efficiency range from 12% up to 17% [4].

In order to achieve high efficiency silicon solar cells, high purity single crystal silicon wafer with thickness around 180-300 μm is needed. Among all other

requirements, this thickness is necessary to ensure adequate light absorption within the silicon wafer. This might not seem too much at first glance. However, to achieve such high quality silicon wafer, multi-step purifications are necessary. In addition to this, silicon wafers are obtained through a process of wire sawing in which 25 - 45% of the initial silicon ingot is lost in the process. The loss is named as called Kerf-loss. Including the silicon kerf, SiC abrasive slurry and metallic wire, the total loss in the wafer slicing process accounts for more than 65% of the total wafering cost. All these add up to account for more than 40% of the total cost of the final silicon solar cells [9].

There are several routes to decrease the cost of silicon solar cells. One way is to use much lower quality silicon such as multicystalline silicon and metallurgical grade silicon [10–12]. The other promising way is to fabricate thin film amorphous silicon solar cells [13]. However, with lower material quality it is difficult to achieve similarly high efficiency silicon solar cells. In particular, a-Si solar cells' efficiency only hovers around 10% efficiency [14]. In addition to this, a-Si solar cells suffer from light induced degradation reducing the efficiency of the initial solar cells by 30% within only couple of years of deployment into the field [15].

To alleviate this issue, an attractive way at reducing the cost is using thin single crystal silicon. This way, the high efficiency can still be maintained while at the same time less material is being used. Indeed, Solexel recently has recently announced efficiency of 21.6% while only using 35 μm thick silicon [16]. Several other research groups and companies have also been reporting highly efficient thin silicon solar cells over the last couple of years. Figure 1.3 summarizes the efficiency of thin silicon reported by various groups.

Not only that thin silicon is an effective way to reduce cost, it also is lightweight and flexible allowing easy integration for solar cells into many different surface morphologies. This opens up variety of exciting applications such as solar tent and lightweight portable electronics.

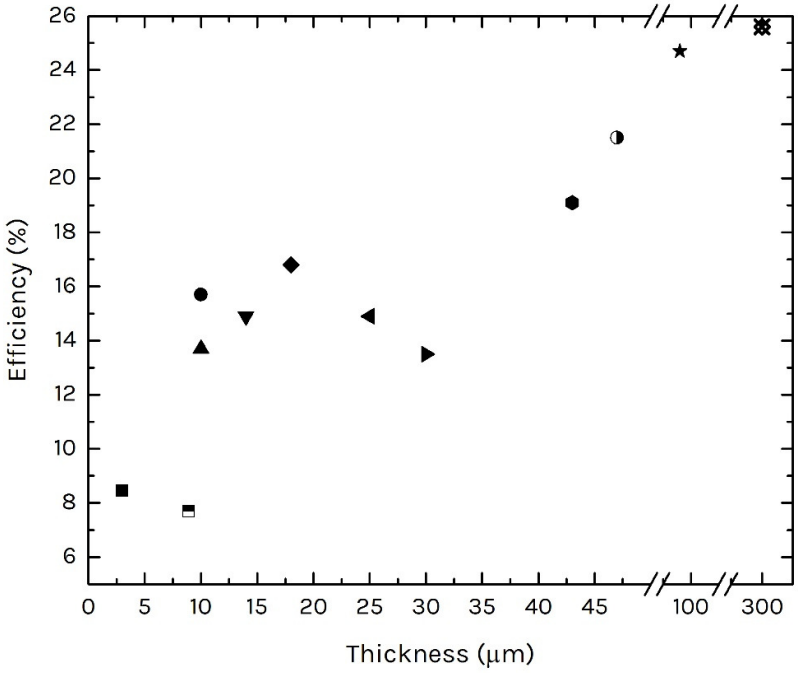

Figure 1.3 Efficiency of various thin silicon with different thicknesses. ■ K. J. Yu et al. (3 μm) [17], ⬒ S. Wang et al. (8.9 μm) [18], ▲ S. Jeong et al. (10 μm) [19], ● M. S. Branham et al. (10 μm) [20] ▼ J. L. Cruz et al. (14 μm) [21], ◆ L. Wang et al. (18 μm) [22], ◀ S. Saha et al. (25 μm) [23], ▶ F. Hasse et al. (30 μm)[24], ⬢ J. H. Petterman et al. (43 μm) [16], ◑ Solexel (47 μm) [25], ★ M. Taguchi et al. (98 μm) [26], ※ Panasonic [27].

Figure 1.4 shows the ratio of generated power to the weight of the solar cells. Power-per-weight ratio can be defined as the ratio of the output power to the weight of the solar cell per unit area under standard solar irradiation of AM1.5 Global. As expected, CIGS has very low number considering that most of the weight is distributed to the glass substrates. Commercial crystalline silicon with thickness of about 180 μm exhibits ratio of 0.3 W/g, which is much lower than ultrathin perovskite with power-per-weight of more than 10 W/g. Nevertheless, if the thickness of silicon is reduced to only 30 μm, the ratio increases to 1.3 W/g. The calculation was based on final device fabricated in this study. This makes silicon competitive to other alternatives such as GaAs and ultra-thin CdTe. Among others, silicon has the advantage of having more reliability with proven long lifetime of more than 25 years [28].

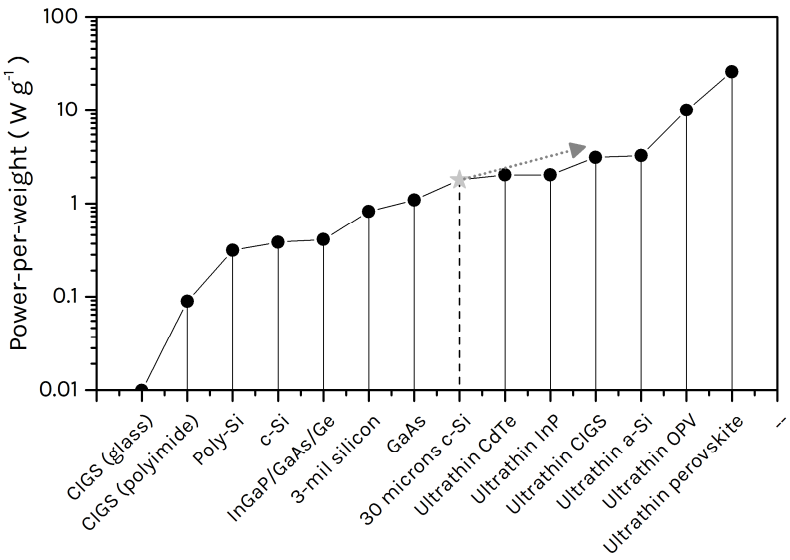

Figure 1.4 Power per weight ratio of different photovoltaics technologies. Adapted from [29]

1.2 Light Absorption

One of the many foundations in solar cell is light absorption. In principle, upon light absorption, regardless of its energy, electron and hole pairs are generated which are then to be collected to contribute for photo-generated current. However, for light to be absorbed within a material, the energy has to be larger than the bandgap of the material. Silicon has a bandgap 1.12 eV (1120 nm) which means that all light with an energy more than this will be readily converted into electron and hole pairs. Figure 1.5 shows the photon flux of the sun (AM1.5G) with dotted line at silicon bandgap. To the left, the light is readily to be absorbed while to the right, all the light is lost to transmission and do not contribute to current at all.

While thin silicon may solve the problem of cost reduction, it suffers from poor light absorption especially in the infrared part of the solar spectrum. As consequence, the power conversion efficiency is also reduced. Because of the nature of silicon, which is an indirect semiconductor, the absorption coefficient for wavelength close to its bandgap is relatively small. This translates to relatively long absorption depth within silicon. At these wavelengths, light needs long distance before it is completely

absorbed. Silicon with thickness of several hundreds of micrometer is therefore necessary to efficiently absorb almost all the incoming light. This is part of the reasons why current silicon solar cells' thickness range from 150 to 300 μm, to ensure adequate absorption of light.

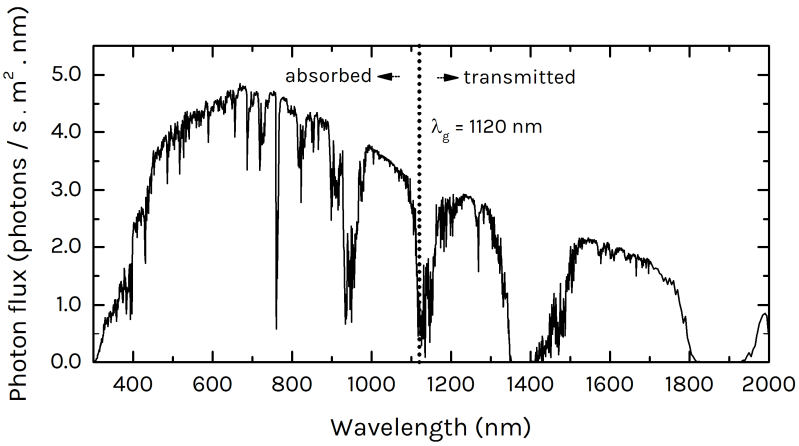

Figure 1.5 Photon flux of the Sun (AM1.5G). The dotted line showing the optical bandgap of silicon at room temperature (1120 nm).

When the thickness of silicon is reduced, more and more long wavelength light is transmitted. This will lead to loss in photogenerated current. To illustrate this, Figure 1.6 shows the amount of light being absorbed by a 30 μm and 300 μm-thick silicon. From the figure, it is clear that even for the case of silicon with thickness of 300 μm, part of the light after 800 nm is not fully absorbed well and even less toward the bandgap of silicon. This issue is even more severe for 30 μm thick silicon where light after 550 nm is mostly wasted not being converted into useful electrical power.

The abovementioned absorption loss analysis neglects the reflection loss, which plays another important role in silicon solar cells. Silicon with refractive index of ~ 3.5 reflects most of the light incoming onto it. The typical reflection loss from planar silicon is about 30 - 50% depending on the wavelength. Overall, both optical losses from both transmission and reflection need to be eliminated to allow for high efficiency silicon solar cells.

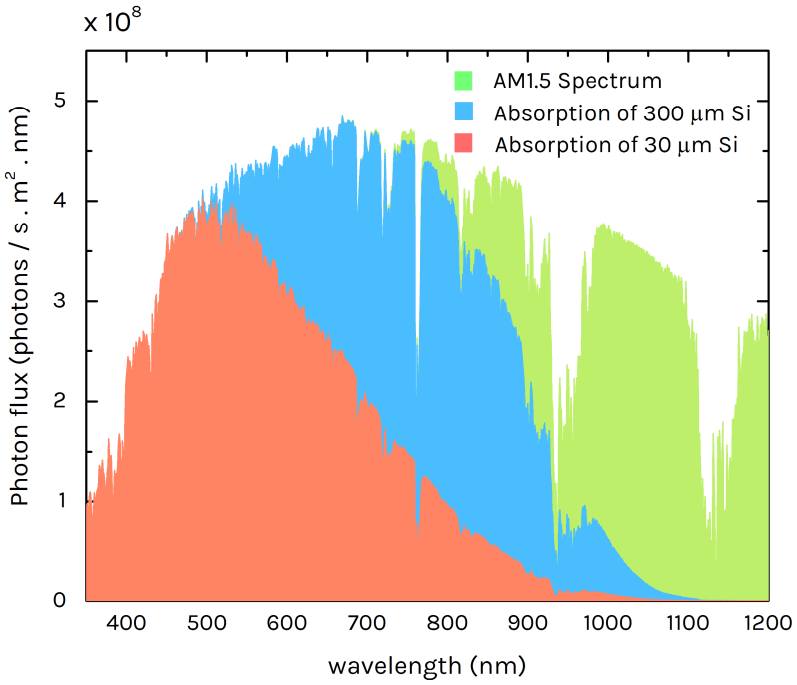

Figure 1.6 Absorption spectra of silicon with thickness of 300 µm (blue) and 30 µm (red).

The transmission and reflection loss can be suppressed by allowing incoming light to bounce multiple times inside the solar cell. This concept is known as light trapping. By implementing light trapping, the optical path of the light can be enhanced and therefore the probability of light being absorbed within the solar cells is increased. In general, surface texturing is widely accepted as an efficient way of achieving light trapping. Three benefits of surface texturing are: a) reduction in the reflected light, b) enhancement of light path length within absorber layer by means of diffraction and c) reduction of escaping light through enhanced total internal reflection.

In industrial single crystalline silicon solar cells, random upright pyramids have become de facto standard for achieving absorption enhancement. While it is very efficient for the current state of art c-Si solar cells, it is not suitable for thin silicon whose thickness is only few tens of microns. This is mainly because the size of the upright pyramids ranges from 5-15 µm, which already makes up for bigger portion of total effective absorber layer. Over the last decades, new paradigms in the light trapping mechanism have been introduced by means of nanophotonics light trapping

structure. The size of the structures is designed in such a way that the it is comparable to the incident wavelength and thus moves the regime from ray optics to wave optics.

There is a great deal of interest in the literature for nanophotonic light trapping structures including nanocones [30] nanodomes [31], nanonholes and nanocylinders [32], nanowires [33], inverted pyramids [34], honeycombs [35]. Despite the intense research on these nanophotonics light trapping structures, only some of the concepts have already been implemented and reported to increase the absorption and improve the efficiency at the same time. One major drawback for most of the structures is the increased surface area, which leads to severe surface recombination that is limiting the efficiency. Nevertheless, the importance of light trapping, in particular for thin silicon should not be undermined and will be highlighted in this thesis.

1.3 Thesis Overview

In this thesis, thin single crystal silicon solar cells with thickness of about 30 μm are fabricated. Two different suitable light trapping structures for thin silicon geometry are investigated; random upright pyramids and periodic inverted pyramids. Maximum efficiency of 13.6% with short circuit current of 32.96 mA/cm^2 and open circuit voltage of 564 mV of has been achieved for random upright pyramids textured thin silicon solar cell.

Chapter 2 provides a brief overview of the importance of light trapping in thin silicon solar cells. Chapter 3 presents descriptions of general parameters being used in solar cell technology and ways of obtaining thin silicon solar cells. Chapter 4 describes the fabrication of two different light trapping structures, random upright pyramids and periodic inverted pyramids. Surface morphology and optical properties of the light trapping structures are also covered in this chapter. Chapter 5 presents details of device fabrication of thin single crystal silicon solar cells. Lastly, Chapter 6 provides the fabricated devices' optical and electrical properties.

CHAPTER 2

LIGHT TRAPPING

When light is incident on a material, several outcomes are possible. A fraction of the light is reflected and never to be seen again by the material. Some part of the light is transmitted through the material. While the rest of the light that is neither reflected nor transmitted gets absorbed or scattered within the material. The complete analysis of the light-matter is out of scope of this thesis and can be found elsewhere [36].

Assuming that the incoming light is normalized to unity, the interaction of light and semiconductor can be simplified to

$$1 = R + T + A \tag{1}$$

where R is reflectance representing the portion of light being reflected, T is transmittance corresponding for the amount of transmitted light and lastly, A is absorbance representing the amount of light being absorbed within the semiconductor.

As the light pass through the absorber layer, its intensity decreases exponentially and is governed by a law, which is known as Beer Lambert's law

$$I(\lambda) = I_0 e^{-\alpha(\lambda)x} \tag{2}$$

where α is the absorption coefficient which is intrinsic for different materials. Absorption coefficient dictates how far the light can travel before finally being absorbed within the absorber layer. The magnitude of absorption coefficient is wavelength dependent. x represents the length of the absorber layer that the light has travelled. Based on this simple equation, one expects solar material to have very high absorption coefficient to absorb most of the incoming light.

Light absorption itself is fundamentally a quantum mechanical process where photons, electrons, and in some cases, phonons interact. In a direct bandgap semiconductor, where valence band maxima and conduction band minima occurs at the same k - plane, light absorption occurs when a photon transfers their energy to electron in valence band. The absorbed energy by electrons promotes them to available energy states in the conduction band. In an indirect bandgap semiconductor, light absorption process is slightly different. Owing to the requirement of energy and momentum conservation, extra momentum has to be included in the process. This is because the maxima of valence band and minima of conduction band are at different k-plane. An indirect semiconductor, in general, is a very poor absorber as in the case for silicon.

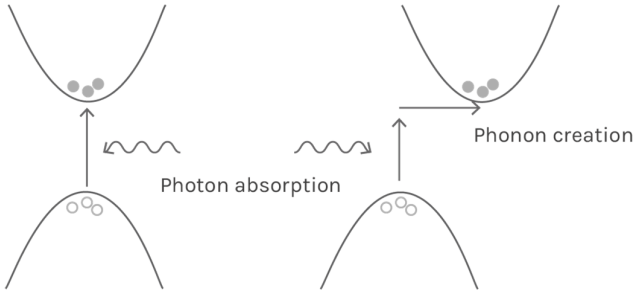

Figure 2.1 Schematics of photon and phonon interaction in direct (left) and indirect (right) bandgap semiconductor.

As a consequence of being an indirect bandgap semiconductor, silicon has relatively small absorption coefficient, especially in the near infrared regime toward the bandgap. To efficiently absorb all light, silicon needs to be significantly thicker when compared to direct bandgap semiconductor such as GaAs, CdTe and amorphous Si (a-Si). Certainly, this comes as a disadvantage for when silicon is used as a solar cell material. To ensure adequate light absorption, silicon with thickness larger than 150 μm is being used in commercial silicon solar cells. It is then evident that the insufficient absorption will become more severe when the thickness of the silicon is reduced to only few tens of micrometers.

One very common way being used to curtail the absorption issue is to increase the path length of the light inside the active region so that the light gets fully absorbed before escaping the device. This is achieved by texturing the device as to let the light

bounce several times within the absorber and hence the optical path length. This phenomenon is often called as path length enhancement. Not only does it increase absorption probability but also the surface textures force the light to bounce more than once on the front surface and gives multiple chance for light to enter the absorber. Consequently, the reflection on the front side is greatly reduced.

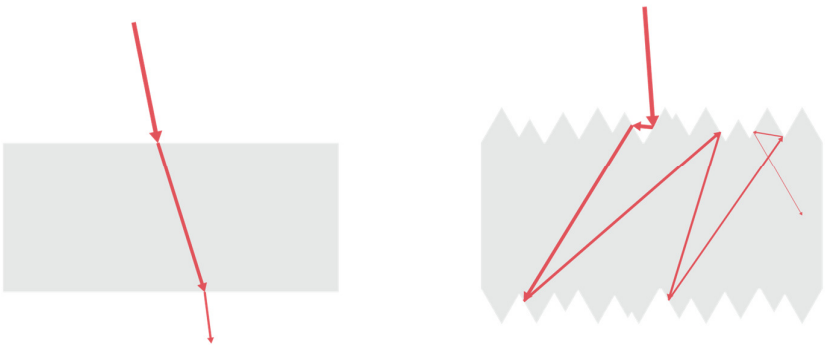

Figure 2.2 Schematics of light travel path within planar (left) and textured (right) absorber layer.

2.1 Lambertian Limit

An upper limit that has long been the benchmark for evaluating the light trapping performance is Lambertian limit which was derived by Yablonovitch and Cody [37]. The derivation was based under three assumptions

- The structure shall have Lambertian surface. On the front side, the surface acts as Lambertian scatterer and the rear surface act as Lambertian reflector. On both cases, light is either transmitted or reflected randomly at every possible angle.

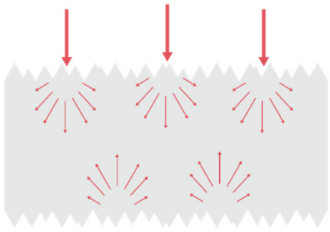

Figure 2.3 Schematic of light interaction with Lambertian surface.

- The absorption within the active material should be in *weak absorption regime* in which

$$4n^2\alpha l \ll 1 \tag{3}$$

where n is the refractve index of the material, α is the absorption coefficient and l is the thickness of the absorber layer.

- The thickness of the absorber layer should be larger than the wavelength inside it, which is calculated as λ/n. This assumption is necessary to ensure that geometrical optics arguments are valid.

Under these three assumptions, the average optical path length is enhanced by factor of $4n^2/\sin^2\theta$, with 2θ as acceptance angle of light. In the case for a device with isotopically incident radiation ($\theta = \pi/2$), the path length enhancement factor becomes $4n^2$. For silicon with refractive index of about ~ 3.5, this corresponds to enhancement of ~ 50 compared to the planar case. This means that thinner silicon can be utilized to absorbs almost as much as thick counterpart. The current thickness of c-Si solar cells of 180-300 µm can be reduced to only 4-25 µm, further reducing material cost.

2.2 Light Trapping for Different Material Thickness

To understand better the effect of light trapping on the thickness of solar material, consider an incident light experiencing only one single pass through the device. The total absorption within the device can be written as

$$A(\lambda) = 1 - e^{-\alpha(\lambda)d} \tag{4}$$

The relation is derived from equation (2) while considering zero reflection loss. Following the derivation by Green [38], the enhanced absorption for Lambertian surface equipped material becomes

$$A(\lambda) = 1 - \frac{1}{1 + 4n^2\alpha(\lambda)d} \tag{5}$$

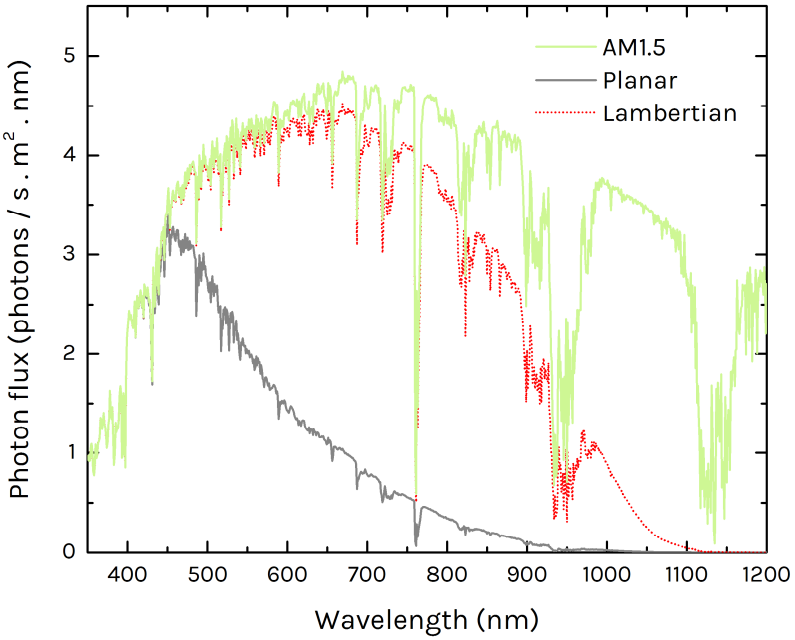

Figure 2.4 Absorption spectra of 10 μm-thick silicon without and with Lambertian light trapping surface together with AM1.5 solar spectrum.

Figure 2.4 shows the calculated absorption spectra of 10 μm thick silicon for the case when it is planar and decorated with Lambertian surface. It is obvious that for planar case most of the light starting from 500 nm towards near infrared regime is mostly lost and not absorbed by silicon. However, with efficient light trapping, the absorption value is enhanced tremendously. Up to 700 nm, almost all incoming light is absorbed within the device. The absorption value eventually drops at wavelength close to the optical band gap of silicon.

By integrating the absorption spectrum over the whole wavelength of interest, maximum attainable short-circuit current can be calculated

$$J_{sc} = q \int_{\lambda_{min}}^{\lambda_{max}} S(\lambda) d\lambda \tag{6}$$

where q is elementary charge and S is photon flux as shown in Figure 2.4 on the absorption spectra. The integration takes an assumption that for every photon absorbed, electron hole pair is generated and collected by metal electrode (i.e. an internal quantum efficiency of 1). From the calculation, the maximum attainable current if all the light up to 1120 nm (bandgap of silicon) is absorbed with zero loss is 43.78 mA/cm^2. In the case of 10 μm thick planar silicon, a mere 11.77 mA/cm^2 of current can only be obtained, whereas for the same thickness of silicon with Lambertian light trapping surface, a current density of 32.47 mA/cm^2 can be obtained. That is almost three-fold enhancement in the photogenerated current. This also emphasizes the importance of light trapping. With a simple act of adding light trapping into thin silicon, efficiency of the solar cell can be drastically enhanced.

Figure 2.5 shows the J_{sc} as a function of thickness for common solar material such as GaAs, CdTe and silicon, with either no light trapping or Lambertian light trapping. The value of J_{sc} is calculated by combining equation (4) and (6) for planar case and (5) and (6) for Lambertian light trapping. The optical properties of both GaAs and CdTe was obtained from [39].

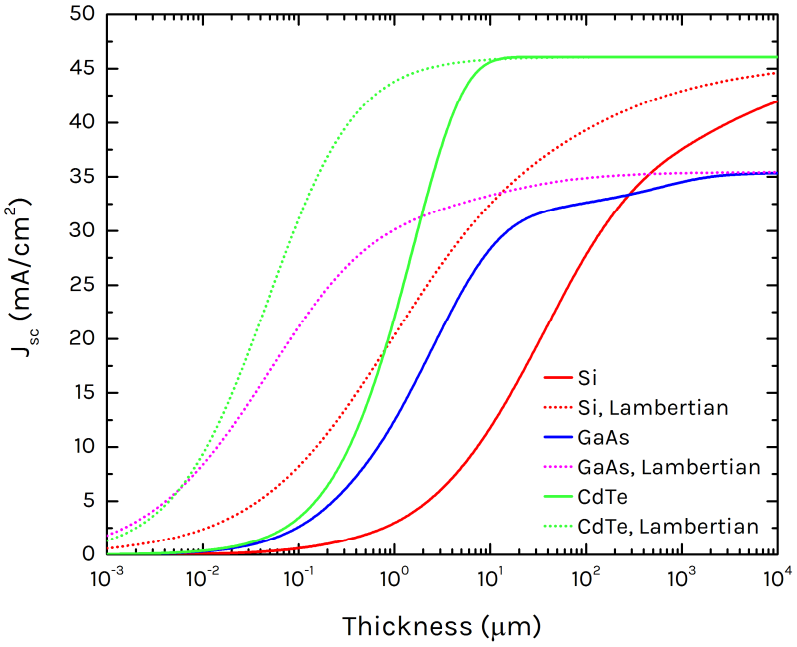

Figure 2.5 Short circuit current (J_{sc}) as function of thickness for Silicon, GaAs and CdTe. Solid line represents the J_{sc} for planar films while dotted line indicating the J_{sc} for films with the Lambertian light trapping.

From Figure 2.5, it is evident that silicon requires much thicker absorber layer to absorb as much light compared to CdTe and GaAs. One clear example is for the case of 10 μm thick CdTe and Si, without any light trapping structure, CdTe already absorbs as much as light that silicon can absorb with Lambertian light trapping. To obtain maximum achievable J_{sc} at least 10 mm thick of silicon is necessary.

2.3 Light Trapping Schemes

To achieve light trapping mechanism on silicon solar cells, several methods are available. These include anti-reflection coating, back reflector and surface texturing. These will be briefly explained in the following sections.

2.3.1 Anti Reflection Coating (ARC)

While anti-reflection coating coatings do not necessarily act as light trapping mechanism, throughout this thesis the ARC will be referred and therefore it will be useful to discuss the principle behind it.

Due to highly mismatch refractive index between air ($n \sim 1$) and silicon ($n \sim 3.5$), most of the light is reflected from the front surface of silicon. The ratio of the reflected light can be calculated with the Fresnel equation

$$R = \left|\frac{\tilde{n} - 1}{\tilde{n} - 1}\right|^2 \tag{7}$$

where $\tilde{n}$ represents the complex refractive index of silicon. On the interface of air and silicon, the amount of reflected light is about 35% in average over the whole wavelengths of interest. To minimize reflection loss, one simple way is to put an intermediate layer between the interface of silicon and air whose refractive index value is between air and silicon. Upon putting additional layer on the absorber layer, the equation of reflection becomes (complete derivation of the formula can be obtained in [40])

$$R = \frac{r_{12}^2 + r_{23}^2 + 2r_{12}r_{23}\cos(2\beta)}{1 + r_{12}^2 r_{23}^2 + 2r_{12}r_{23}\cos(2\beta)} \tag{8}$$

In the above equation, r_{12} represents the reflectance from phase 1 to phase 2 material and likewise for r_{23}. The relation for β is described via $\beta = \frac{2\pi}{\lambda} n_2 d cos(\theta)$ where d is the thickness of the ARC layer and θ is the refracted angle on the interface between phase 1 and phase 2 material as shown in Figure 2.6.

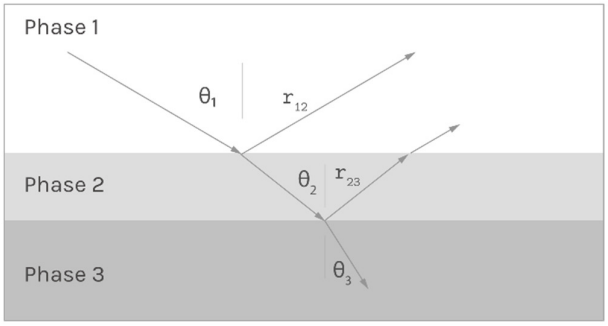

Figure 2.6 Schematic of light travel path for antireflection coating.

The simplest type of ARC is a quarter-wave transformer. The situation is satisfied when the thickness of the layer equals to quarter of the wavelength inside the layer ($d = \lambda/4n_2$). Putting this relation into the equation (8) requires that

$$r_{12} = r_{23} \tag{9}$$

Assuming that the light is at normal incidence, equation (9) becomes

$$\frac{n_2 - n_1}{n_2 + n_1} = \frac{n_3 - n_2}{n_3 + n_2} \tag{10}$$

Solving the equation for n_2 gives

$$n_2 = \sqrt{n_1 n_3} \tag{11}$$

In order to maximize the photo-generated current, reflection at which solar irradiance is maximum needs to be at minimum. Solar irradiance is maximum at around 550 nm at which gives silicon refractive index of about ~ 3.5. A simple math concludes that the optimum refractive index of the ARC layer must be around ~ 1.87. There are plenty of choices of material that satisfy this condition. One particular material that stands out is silicon nitride (SiN_x). At its stoichiometry, SiN_x:H has refractive index of about ~1.8 and can be tuned by adjusting the ratio between silicon and nitrogen. Besides acting as excellent ARC, SiN_x also acts as good surface passivation layer for n-type silicon [41–43]. Other choices of materials to be used for ARC are SiO_2 and TiO_2. SiO_2 can also acts as excellent passivation layer for both n-type and p-type silicon. However, the refractive index of SiO_2 is smaller than to SiN_x and therefore provides less effective ARC performance. TiO_2, on the other hand, may give great ARC performance but does not provide sufficient passivation function [44].

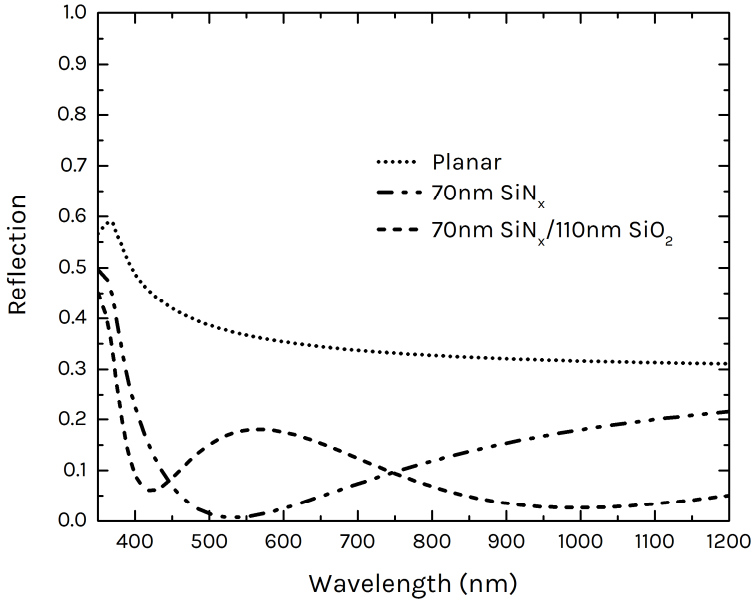

Figure 2.7 Reflection spectra of ARC layer on silicon with semi-infinite thickness. The dash-dot line represents the spectrum for single layer ARC of SiN_x. The dashed line represents spectrum for double layer ARC of SiN_x/SiO_2.

Figure 2.7 shows typical reflection spectrum for planar silicon with anti-reflection coating. For a single layer ARC, a minimum in the spectrum is observed at around 550 nm. This was achieved by depositing 70 nm of SiN_x with refractive index of about 1.82. Single layer ARC does not work over the whole wavelength. As depicted in figure, single ARC only minimizes reflection at around wavelength of interest. However, by adding another layer on the already existing ARC layer, further reflection can be suppressed. Several combination of double ARC have been studied in literature such as MgF_2/SiN_x [45], SiO_2/TiO_2 [46] and Al_2O_3/TiO_2 [47] and others. The concept of tri-layer of ARC has also been investigated with combination of SiO_2/SiO_2-TiO_2/TiO_2 [48]. Figure 2.7 also shows simple analytical solution to double layer of ARC with SiN_x and SiO_2. Upon adding second ARC layer, another reflection minimum is observed on the reflection spectrum and the position of initial minima is shifted. Overall, greater performance at minimizing reflection can be obtained.

2.3.2 Back Reflector

The simplest way of elongating optical path within an active absorber is by putting a "mirror" or back reflector on the rear side of the material. In this way, light will travel at least twice of the original path length. Back reflector is especially beneficial for long wavelength light since most of short wavelengths light are already absorbed within the top layer of absorber in the first pass. The mirror in this context can be a metal layer. Most of metal reflect more than 90% of the incoming light. Metal can serve two purposes in solar cell; a) as metal electrode to collect photo-generated carrier, b) as back reflector to avoid transmitted light. Another possible way of providing the mirror-like properties is by adding Bragg reflector layer in which stacks of two or more dielectrics layers are deposited consequently [49, 50]. Other interesting concept of back reflector also includes multi-layer of porous silicon on the rear side [51].

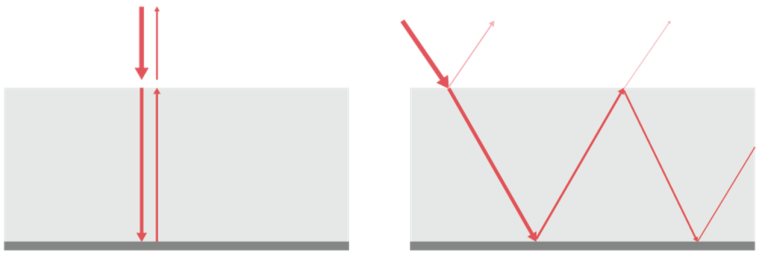

Figure 2.8 Schematic of silicon slab with metal back reflector.

Ideally, the reflectance of the metal should be unity ($R = 1$) and the front surface reflection should be zero ($R = 0$) to minimize any losses. This can be achieved by assuming that a perfect ARC layer is present on the surface. In the event that both the conditions are met, path length enhancement factor of 2 at normal incidence is obtained. The path length can further be enhanced by tilting the incoming light in such a way that the light reflected from the metal comes back at angle in which it is sufficient for internal reflection condition. This way, the light will be reflected multiple times inside the absorber layer further increasing absorption probability.

In practice, common metals for silicon solar cells are aluminum and silver. Aluminum is usually used to make contact with p-type silicon and cover the whole rear side of p-type base silicon solar cells. One disadvantage of aluminum is that it also

acts as parasitic absorber especially toward infrared range. For optical purpose, ideally silver is preferred for back reflector thanks to its lower parasitic absorption.

2.3.3 Surface Texturing

Surface texturing or surface roughening mainly serves the purpose of scattering the incident light to an oblique angle and therefore increase the path length of light. The graphical representation of surface texturing is depicted in Figure 2.2. By roughening the surface, the dwelling time of light inside the absorber increases and thus increases the probability of light to be absorbed before escaping the layer. Strictly speaking, these assumptions are only valid in the regime of geometrical optics where the feature sizes are larger than wavelength of light. Fundamentally, light trapping in textured absorber layer is accomplished by coupling incident light into available guided optical modes within the layer. Optical mode, in other words, is a spatial distribution of optical energy in one or more dimensions that remains constant in time.

2.3.3.1 Random Pyramids

Common practice of surface texturing for silicon solar cells is to form random upright pyramids on the surface. This is easily achieved by alkaline solution anisotropic etching of silicon wafer. The most frequently used solution is potassium hydroxide (KOH). The process takes advantage of crystallography of silicon. Silicon plane of (111) is etched much slower when compared to (100) plane. As consequence, pyramids are formed on (100) silicon with faces of (111) planes being exposed on all sides of the pyramids. The angle formed between (100) silicon plane and (111) plane is approximately 54.7° degree.

The complete chemical reaction of surface texturing of KOH has been subject of discussion for long time. Generally, the following equation is agreed upon by many

$$Si + H_2O + 2KOH \rightarrow K_2SiO_3 + 2H_2 \quad (12)$$

In the reaction, potassium sulfate and hydrogen gas are byproducts of the reaction [52, 53].

Solution of KOH by itself does not usually provide desired pyramids structures on silicon. The etch rate of the solution is too fast to allow pyramids formation. To

reduce the etch rate and therefore increasing the selectivity of etch rate along (111) plane and (100) silicon, additive such as isopropyl alcohol (IPA) is typically included in the solution. IPA also acts as a wetting agent to prevent the H_2 bubbles adhering on the silicon surface which would otherwise lead to non-uniform pyramids formation [54].

While random upright pyramids structure has proved to be excellent for conventional silicon solar cells, the applicability of it towards thin silicon is rather suitable. The average size of the pyramids ranges from 5-15 μm, as can be seen on Figure 2.9. Such geometry is not suitable for thin silicon since it already makes up for most of the absorber layer. The other less obvious reason why conventional texturing route is not suitable for thin silicon is that during the process of etching, at least 10 μm of silicon from each side of the wafer is being etched. This is certainly disadvantageous for when the starting wafer is very thin (less than 30 μm). Indeed, this was one of the main driving forces behind the intense research of nanophotonics light trapping structures.

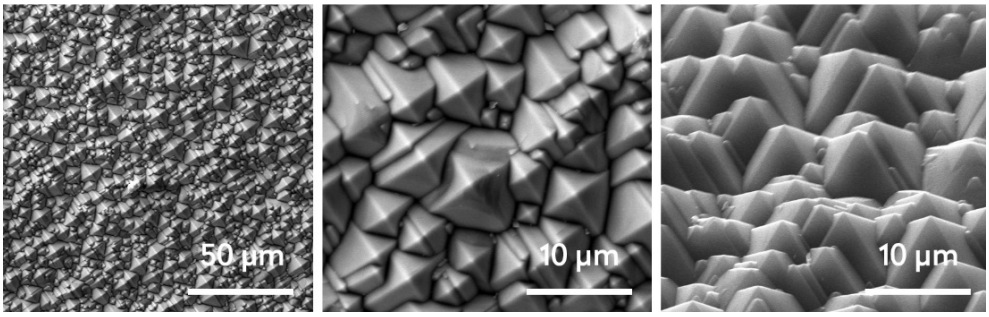

Figure 2.9 Top view of surface morphology of standard random upright pyramids texture on silicon surface with different magnifications.

2.3.3.2 Periodic Inverted Pyramids

The logical step to achieve suitable and efficient light trapping in thin silicon is to form small textures while at the same time minimizing material loss. Another promising alternative of light trapping structure to random upright pyramids is periodic structures. Periodic structures can come in forms of 1D grating, 2D grating. Notable example includes periodic inverted pyramids, nanocones, nanodomes. Periodic

structures may offer two different advantages; a) reducing reflection and b) better light management inside active absorber material. Periodic structures can couple incident incoming light to guided optical modes inside the absorber layer. In turn, this will reduce reflection from the surface as well as improve the absorption within the absorber layer.

Periodic inverted pyramids, in particular, have been used in many highly efficient silicon solar cells. Adopting the same principle of anisotropy in etching of different planes in silicon, inverted pyramids can be formed as shown in Figure 2.10. For this reason, the same etchant of KOH solution can still be used. Within geometrical optics assumption, the shape of inverted pyramids gives light two chances of entering the absorber. In addition, it increases the chances of internal reflection from the rear surface. The well-known application of the inverted pyramids was realized in one of the early world-record silicon solar cell [55]. In this report, however, the size of the inverted pyramids is several microns and still not suitable for thin silicon. Recently, nanopyramids structures have been shown to be an efficient light trapping structure for thin silicon [34, 56]. An efficiency of 15.7% has also been obtained from 10 µm-thick thin silicon with sub-micron inverted pyramids [20]. Inverted pyramids has also the advantage of low surface area enlargement in when compared to other light trapping structures which might lead to an enhanced surface recombination loss [34].

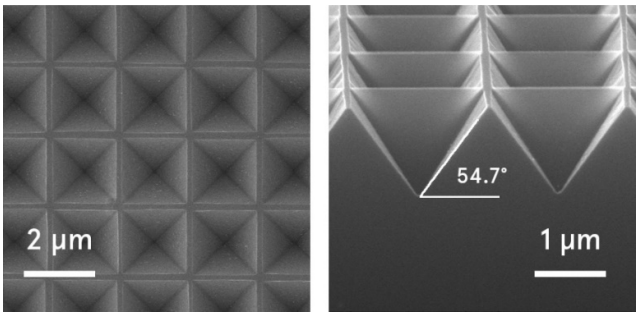

Figure 2.10 Inverted pyramids texture on silicon. An angle of 54.7° is observed on the inverted pyramid between (100) and (111) planes of silicon.

Similar to the fabrication of random upright pyramids, the fabrication of inverted pyramids can also take advantage of silicon crystallinity. Anisotropic etchant such as KOH and tetramethylaamonium hydroxide (TMAH) can be used to form

inverted pyramids with precise angle of 54.7°. One big disadvantage of periodic inverted pyramids compared to random upright pyramids is the need of extra step to create masking layer, which is typically achieved by photolithography process.

CHAPTER 3

OTHER RELEVANT CONCEPTS

In this chapter, solar cells parameter definitions to be used throughout the thesis will be explained. In addition, loss mechanisms in a solar cell via recombination will be explained. Lastly, methods of obtaining thin silicon will be introduced.

3.1 Solar Cells Parameters

Most of the parameters of a finished solar cell device can be extracted from current-voltage (JV) curve. A typical JV curve is given in the Figure 3.1. Since a solar cell is just a semiconductor diode, the shape of the curve is governed by Shockley's ideal diode law

$$J = J_o \left[e^{\frac{qV}{k_B T}} - 1 \right] - J_L \tag{13}$$

where J_L is the photo-generated current, J_o is the reverse saturation current density, q is electron charge, V is voltage being applied onto the cell, k_B is the Boltzmann constant and T is temperature in Kelvin. J_o is determined by the sum of recombination loss in the emitter and base region of a solar cell. It generally takes into account the recombination via Shockley-Read Hall, radiative and Auger.

From the JV curve, the parameters such as fill factor (FF), open circuit voltage (V_{oc}) and short circuit current (J_{sc}) are to be extracted. V_{oc} is the measured voltage of a solar cell when there is no current flowing thorugh it. Meanwhile, J_{sc} represents the maximum attainable current from a solar cell at zero bias. The power conversion efficiency (η) which consists of these parameters can also be determined. Power conversion efficiency η can be defined as the ratio between the maximum generated

electrical power p_{max} from the cell to the total power of incident light J_L. The relation of the efficiency can be written as

$$\eta = \frac{p_{max}}{I_L} = \frac{V_{oc}.J_{sc}.FF}{J_L} \tag{14}$$

Generally, the efficiency is measured under light intensity of 1000 W/m^2 which corresponds to the area underneath of spectrum of AM 1.5G and temperature of 25 °C. The efficiecy is identified by following the curve of product of current and voltage. The ratio between the maximum point on this curve (maximum power point) to the product of J_{sc} and V_{oc} gives us the fill factor (FF) of a given solar cell. In a good solar cell, the value of fill factor ranges from 75% to 85%.

$$FF = \frac{J_{PP}.V_{PP}}{J_{sc}.V_{oc}} \tag{15}$$

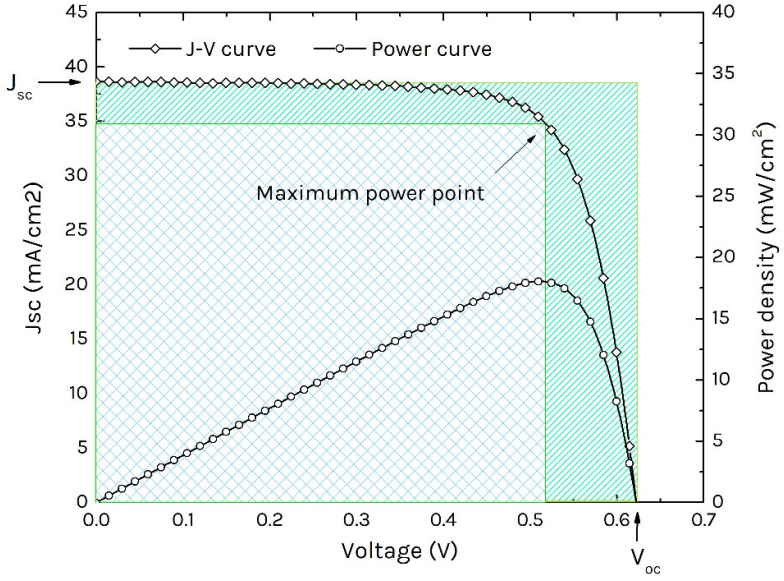

Figure 3.1 Typical JV curve and power density-voltage of a solar cell.

Setting V in the equation (13) to zero, we can see that J_{sc} also corresponds to J_L which is the maximum photo-generated current. Setting the left-hand term in the equation (13) to zero, it can be clearly seen that V_{oc} can approximately be calculated as

$$V_{oc} = \frac{k_B T}{q} \ln \left[\frac{J_L}{J_o} + 1 \right] \tag{16}$$

The magnitude of V_{oc} is greatly affected by the quality of the solar cell material. For silicon solar with bandgap of 1.12 eV, the maximum practical V_{oc} of 753 mV has been obtanied [57].

The shape of JV can be distorted by the presense of resistance loss and hence the value of fill factor. Two resistance losses in a solar cell include series resistance R_s and shunt resistance R_{sh}. The series resistane account for the resistance encountered by carries within the bulk material, the emitter as well as the metal contacts. The value of series resistance can be approximately calculated by the slope of IV curve at the V_{oc}

$$R_s = \left[\frac{1}{\frac{dI}{dV}} \right]_{V=V_{oc}} \tag{17}$$

Shunt resistance may occur due to prensence of alternative path for the photo-generated current to flow instead of the junction. Therefore, the value of V_{oc} is reduced in the presence of low shunt resistance. Estimation of the value of shunt resistance can be obtained by determining the slope of the curve at short circuit point the IV curve

$$R_{sh} = \left[\frac{1}{\frac{dI}{dV}} \right]_{V=0} \tag{18}$$

Quantum efficiency

Spectral response of a solar cell can be defined as the ratio between the photo-generated current to the power of light incident on it. It can be mathematically expressed as

$$SR(\lambda) = \frac{J_{sc}(\lambda)}{I(\lambda)} \tag{19}$$

The unit of spectral response is in A/W and the quantity is wavelength-dependant. Another useful quantity based on the spectral response is external quantum efficiency

(EQE). It is the ratio between the numbers of collected carriers to the incoming photons onto the cells.

$$EQE(\lambda) = \frac{J_{sc}}{q}\frac{hc}{\lambda I(\lambda)} = \frac{hc}{q\lambda}SR(\lambda) \tag{20}$$

By considering the transmission and reflection loss, internal quantum efficiency (IQE) can also be calculated from EQE

$$IQE(\lambda) = \frac{EQE(\lambda)}{(1-R-T)} \tag{21}$$

IQE represents the ratio of carriers that are collected by metal electrodes to the photons absorbed within the solar cells.

3.2 Recombination losses

Recombination refers to the process where carrier of holes and electrons annihilate each other. This is the exact reverse of carrier generations. In a solar cell, recombination processes need to be suppressed to eliminate losses since they affect both current and voltage of the cell. Generally, there are two types of recombination processes, radiative and non-radiative recombination.

Within radiative recombination, electrons and holes react to release. Therefore, the rate of radiative recombination is proportional to the photogeneration. The process is more prevalent in direct bandgap semiconductor. Silicon is an indirect bandgap semiconductor, and thus radiative recombination play a minor role in the recombination losses.

In non-radiative recombination process, the extra released energy from the recombination process must be transferred to other particles such as other electrons or holes and phonons. Auger and Shockley-Read-Hall (SRH) recombination are example of non-radiative recombination process. In Auger recombination, the energy released during recombination process is transferred to other electrons or holes, which is then excited to higher energy states. The excited electron or hole eventually thermalizes down while losing its energy via collisions with electrons or holes. SRH recombinations occur due to the presence of impurities within the semiconductor. The

presence of impurities results in discrete energy levels in the bandgap. Carriers can be trapped within these discrete energy levels and recombine. It can be said that less defective material is necessary to have a good solar cell.

Referring back to the equation (16), it is understood that the value of V_{oc} is dependent on the reverse saturation current Jo. The saturation current is dictated by the density of recombination within the cell. The saturation current increases with recombination rate, which in turn will reduce the V_{oc}.

3.3 Obtaining Thin Silicon

Over the past couple of years, driven by the motivation of cost reduction, several methods have been proposed to obtain thin silicon. Notable ones include kerf-less methods such as thin silicon on porous silicon [58], stress induced peel-off [59], Polymax™ by SiGen [60].

The process of obtaining thin silicon on porous silicon starts with forming layer of porous silicon by electrochemical etching of HF based solution. After porous silicon etching, the wafer is annealed at high temperature of more than 1100 °C in a hydrogen ambient. During the annealing process, the pores within silicon coalesce and form bigger voids, which then form a thin smooth silicon layer on top. Silicon layer is then epitaxially grown on the wafers until desired thickness. The crystallinity of the epitaxially grown layer follows the initial silicon layer. After obtaining the desired silicon thickness, the silicon can easily be detached from the parent substrates mechanically.

Another promising way to obtain thin silicon is by method of stress induced silicon peel-off. In this process, a thin layer with different thermal expansion coefficient (CTE) to that of silicon is deposited on top of silicon wafer. The layer can be metal such as aluminum or epoxy polymers. In the example from Niepelt et.al, aluminum layer is evaporated on bulk silicon while the wafer is heated which will results in stressed aluminum layer upon cooling to room temperature [61]. Then the sample is exposed to temperature gradient in which due to the difference in CTE both layer expands separately. High amount stress is then induced on the silicon layer. Upon cooling, the top layer induced a thermal stress that is large enough to create a crack

starting from the edge and continue to propagate parallel to the substrate surface. In the end of the process, thin silicon is exfoliated. The thickness of the exfoliated thin silicon can be adjusted by changing stressor material.

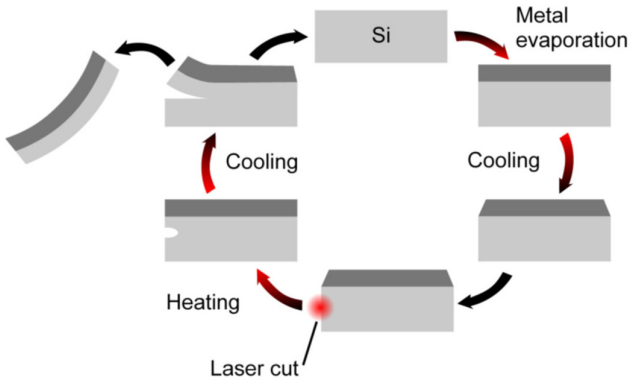

Figure 3.2 Schematic of metal-assisted stress-induced exfoliation of thin silicon [61].

Other promising method of obtaining thin silicon that has received heavy investment from Silicon Genesis (SiGen) company is dubbed as Polymax^{TM}. The process involves two main steps, which are implant and cleave. Highly energetic proton beam is directed onto silicon ingot and implanted at desired depth. This process weakens the silicon along the implanted region. Then, the silicon is induced to cleave along the already weakened region defined by implanted ions. Finally, thin silicon wafer of controlled thickness with high quality is obtained. The substrate underneath can be then recycled to be used for the same process.

For demonstration purpose, obtaining thin silicon can also be done by chemical etching of thick silicon wafer. While this method eliminates the purpose of reducing the cost, it is often useful to prove experimentally that highly efficient thin silicon solar cells can be attained. Indeed, an efficiency of 21.5% using 47 μm silicon obtained by this method has been realized [62]. This remains the highest efficiency of sub-50 μm-thick silicon solar cells. Other than the abovementioned methods, several others have also been proposed to fabricate thin silicon such as ribbon silicon [63], laser wafer cutting [64], electrochemical cutting [65] and direct film transfer [66].

CHAPTER 4

FABRICATION OF LIGHT TRAPPING STRUCTURES

In this chapter, the fabrication of two light trapping structures, random upright pyramids and periodic inverted pyramids, will be explained in detail. Their structural properties will be discussed through SEM images. Moreover, light trapping performance of these two structures will be explained and compared by means of reflection measurements.

4.1 Random Upright Pyramids

As it was mentioned in Chapter 2, conventional texturing process for obtaining random upright pyramids is not suitable for thin silicon. During the standard process, tens of microns of silicon are etched from both sides and the average size of the pyramids is well above 5 μm. In the following sections, a modified etching process which result in random upright pyramids with a maximum pyramid size of 3 μm while maintaining minimal material loss will be explained.

4.1.1 Random Upright Pyramids by KOH + IPA Solution

The texturing process with solution of KOH and additive of IPA is still the most frequently used method for single crystalline silicon solar cells. By changing the parameters of texturing process, smaller or larger pyramids can be obtained.

4.1.1.1 Fabrication

Surface texturing of random upright pyramids with IPA additive was carried out on (100) p-type double side polished silicon wafers. Prior to texturing process, wafers were cleaned in a piranha solution consisting of sulfuric acid and hydrogen

peroxide to remove organic contaminants. Surface cleaning affects uniformity of pyramids sizes across the whole wafer [67, 68]. After cleaning process, the wafers were then dipped into a diluted HF solution to remove thin oxide layer grown during the previous cleaning process. Shortly afterwards, the wafers were immersed into solution containing KOH (4 wt%) and IPA (2%). From here on, the recipe will be called as "IPA recipe". The temperature of the solutions was kept constant at 70 °C. An ultrasonic agitation was also provided during the etching process to remove hydrogen bubbles from the silicon surface. After texturing process, the wafers were rinsed in DI water and dried out with blowing nitrogen.

4.1.1.2 Surface Morphology

Surface morphology of the textured wafers was imaged using SEM (Scanning Electron Microscopy). Upright pyramids with near complete coverage of the surface were achieved in the first 10 minutes as shown in Figure 4.1. The size of the pyramids was smaller after 20 minutes etching. However, after 30 minutes of etching, distinct large pyramids were observed on the surface surrounded by much smaller pyramids and relatively large planar regions. Appearance of planar regions can be attributed to the fact that after 30 minutes, most of the IPA inside the solution was evaporated. This increases the etch rate of the solution and most of the pyramids collapse and are planarized. In short, pyramids with average size less than 2 μm were obtained with the abovementioned solution parameters and conditions.

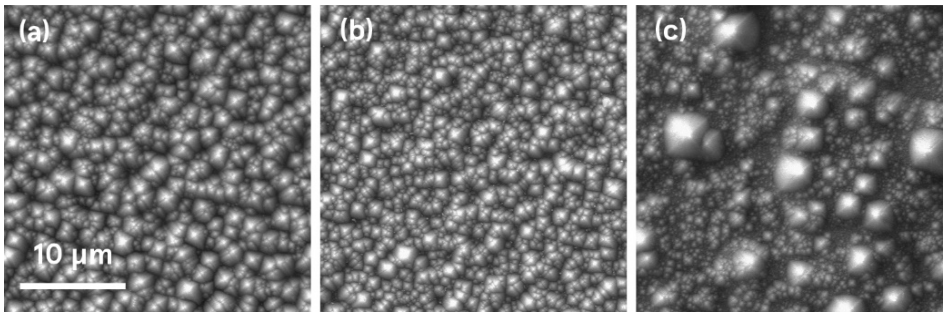

Figure 4.1 SEM images of fabricated random upright pyramids by IPA recipe with a) 10 minutes, b) 20 minutes and c) 30 minutes of etching time.

4.1.1.3 Optical Properties

The reflectivity spectra of textured wafer with different etching times are plotted in Figure 4.2. The details of reflection measurement methods can be found in the appendix. It is evident that surface texturing greatly reduces the reflection of the silicon surface when compared to planar silicon. The reflection of silicon wafers textured with the proposed recipe is also compared with the ones textured with the standard recipe being used for high-efficiency silicon solar cells at GUNAM and with the planar silicon wafer with no texturing. The recipe for the standard process is (3.3 wt% KOH + 5.4% IPA at 70 °C for 35 minutes). The reflection spectra for silicon wafer with various texturing resemble each other's. Average reflection of textured silicon wafers is always smaller than the planar silicon.

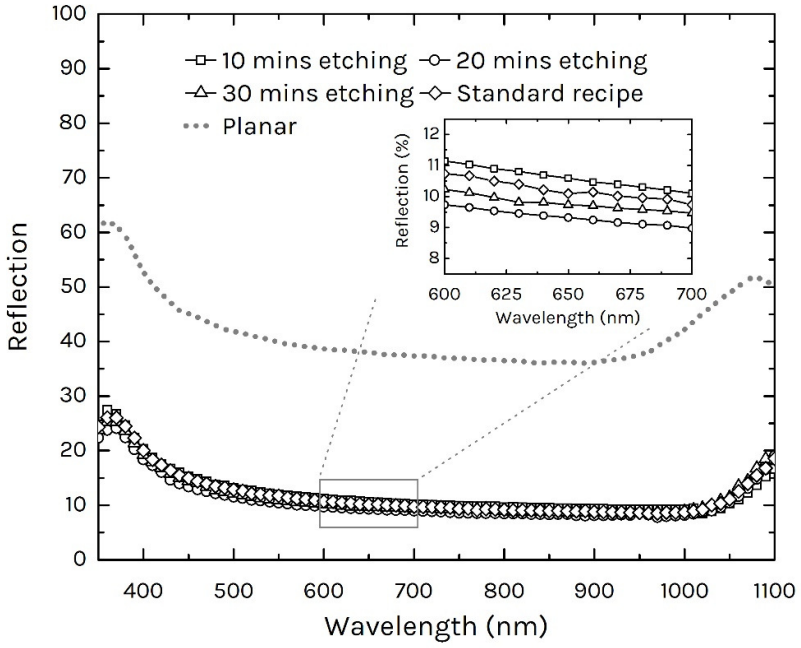

Figure 4.2 Reflection spectra of a silicon wafer textured with random upright pyramids obtained by IPA recipe solution at etching times of 10, 20 and 30 minutes in comparison with random upright pyramids obtained by GUNAM standard recipe. Reflection of planar silicon is given for comparison.

It is rather difficult to compare the reflection value over broad range of wavelength. Another figure of merit, the weighted average reflectance, can be used to

directly compare the performance over the whole wavelength range. The weighted average reflectance (R_w) can be calculated as

$$R_w = \frac{\int_{\lambda_{min}}^{\lambda_{max}} S(\lambda)R(\lambda)d\lambda}{\int_{\lambda_{min}}^{\lambda_{max}} S(\lambda)d\lambda} x100 \quad (22)$$

where $S(\lambda)$ corresponds to the AM1.5 solar spectrum and $R(\lambda)$ is the measured reflectance spectrum.

As shown in Figure 4.3, the weighted reflection of a silicon wafer etched for 10 minutes with the proposed recipe is slightly higher than that etched with the standard recipe. The reason might be due to the presence of planar region on the silicon surface in the case of 10 min etching, which might have resulted from the incomplete formation of pyramids. As the etching time increases, the planar regions form into pyramids and therefore reduce the reflection as evidently shown by the lower weighted reflection. However, due to the collapse of pyramids, reflection increases for the sample with 30 minutes of etching time but its weighted reflection is still slightly lower than the standard recipe.

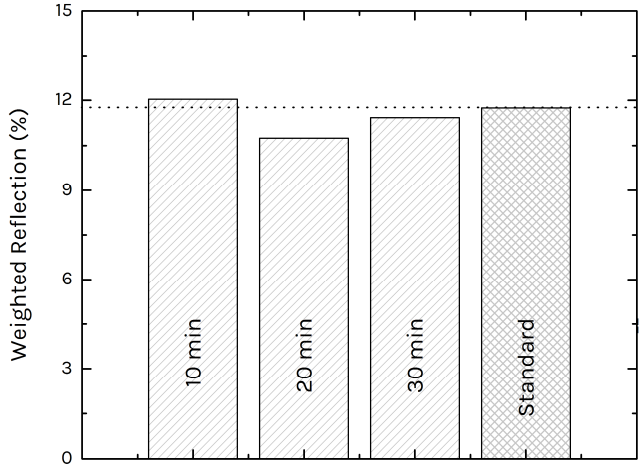

Figure 4.3 Weighted reflection for a silicon wafer with random upright pyramids textured using IPA recipe solution at 10, 20, and 30 minutes in comparison with that textured using GUNAM standard recipe. The dotted line is shown to guide the eye.

4.1.2 Random Upright Pyramids by KOH + Alka-tex Solution

IPA has been widely used as additive for surface texturing by KOH etching. The typical etching process temperature is 70-80 °C, which is just below the boiling point of IPA (82.4 °C). As consequence, IPA evaporates quickly overtime and its concentration alters during the texturing, therefore reduces the stability of the solution. It is rather difficult to reproduce uniform pyramid morphologies. Another concern regarding the usage of IPA is that it is a health hazard and explosive substance [69].

In place of IPA, Alka-tex from GP Solar is used as additive for etching solution of texturing process. Alka-tex provides relatively much lower additive consumption, longer solution lifetime and most importantly less organic contaminants from the additive. Unlike IPA, the issue of fast replenishment of additive can be eliminated. Therefore, the texturing process is much easier to control.

4.1.2.1 Fabrication

Similar to the texturing process of IPA recipe, surface texturing of random upright pyramids was carried out on a (100) p-type double side polished silicon wafer. All fabrication steps using this method are identical with the KOH + IPA texturing, except the wafers are immersed into a solution containing KOH (4 wt%) with addition of 0.6% of Alka-tex. From here on, the recipe will be called as “Alka-tex recipe”. It is clear that the usage of the additive is much less than IPA that might help in cost reduction.

4.1.2.2 Surface Morphology

Figure 4.4 shows the surface morphology of pyramid textured silicon with Alkatex additive. It is seen for the figure that the size of the pyamids is much less than 10 μm. Starting from the etching time of 5 minutes, clusters of smaller pyramids around relatively larger pyramids are seen on the surface. Increasing the etching time to 10 minutes, the size distribution of the pyramids gets even better. At 15 and 20 minutes etching time, relatively larger pyramids are formed. The average size of the pyramids is still much smaller than 10 μm.

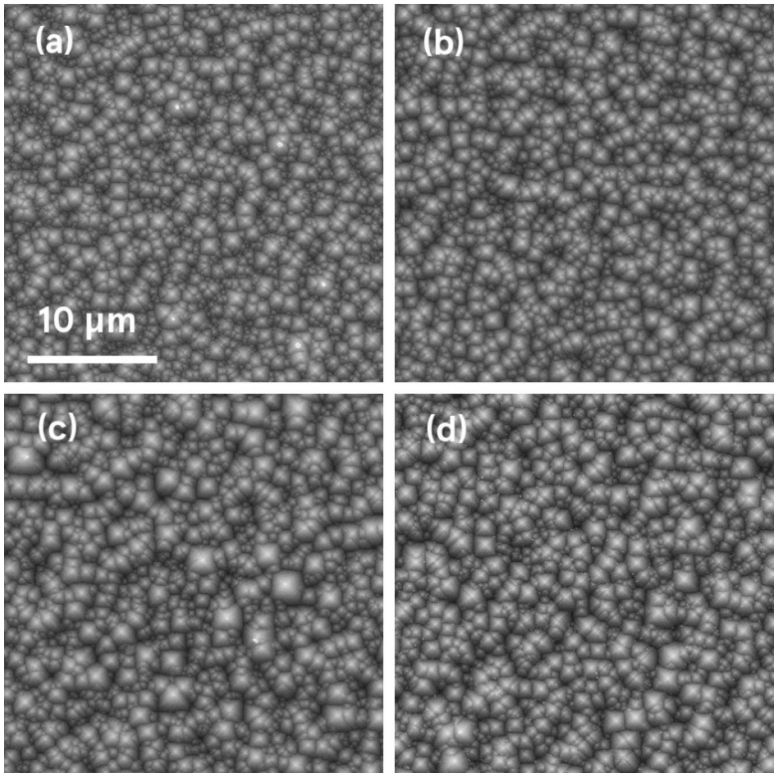

Figure 4.4 SEM images of fabricated random upright pyramids by Alka-tex recipe with a) 5 minutes, b) 10 minutes, c) 15 minutes, d) 20 minutes of etching time.

4.1.2.3 Optical Properties

The reflectance data from textured surface with Alka-tex additive are plotted in Figure 4.5. Similar as in the case of IPA, reflection from the surface is greatly reduced compared to planar silicon.

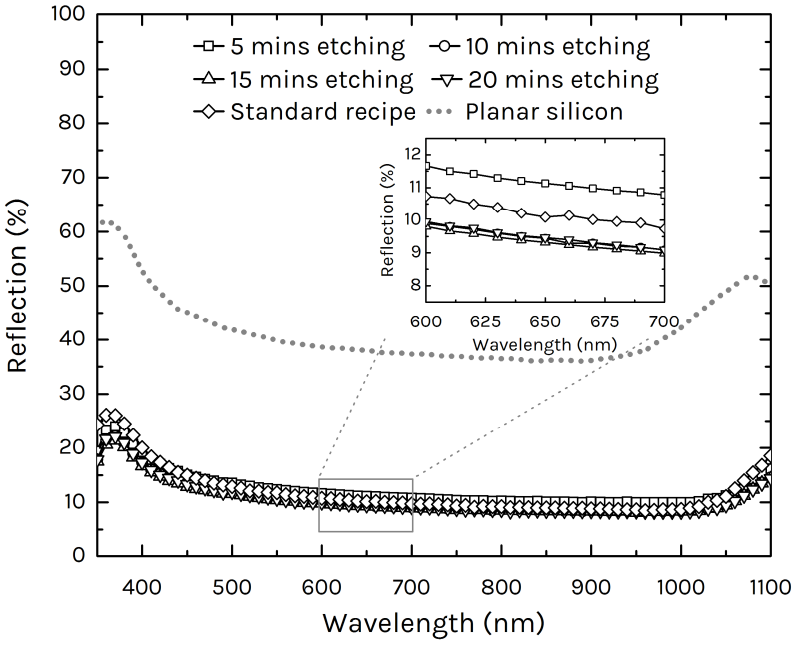

Figure 4.5 Reflection spectra for random upright pyramids texture obtained by Alka-tex recipe at etching times of 5, 10, 15 and 20 minutes in comparison with random upright pyramids obtained by GUNAM standard recipe. Reflection of planar silicon is given for comparison.

Silicon with random pyramids fabricated by Alka-tex recipe etching in 5 minutes possess the highest reflection as shown in Figure 4.5 due to incomplete pyramid formation. Increasing the etching time to 10 minutes reduces the reflection quite significantly. The lowest reflection was achieved for the sample with etching time of 15 minutes. It is also worth noting that the weighted reflection of samples with etching time more than 10 minutes is lower than the standard recipe, which results in relatively larger pyramids.

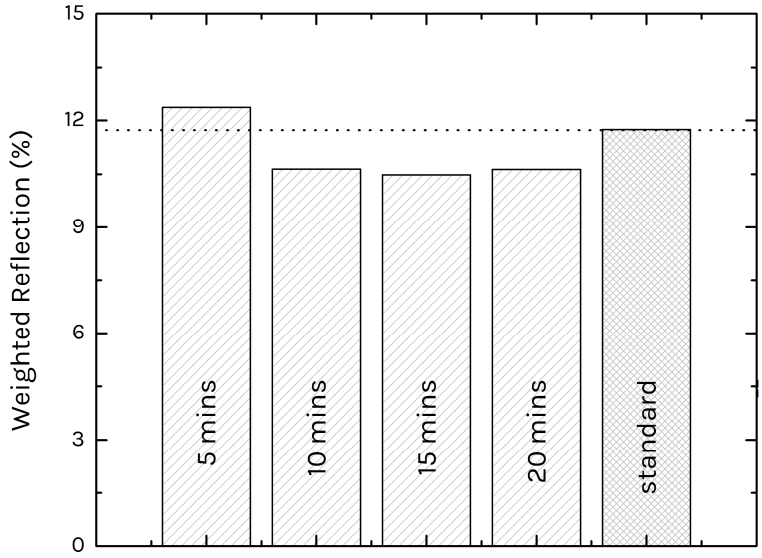

Figure 4.6 Weighted reflection for thick silicon textured with random upright pyramids obtained by Alka-tex recipe solution at 5, 10, 15 and 20 minutes, in comparison with that of thick silicon textured by GUNAM standard recipe. The dotted line is shown to guide the eye.

4.2 Comparison between IPA and Alka-tex as additive

In this part, the best performing samples of IPA and Alka-tex recipes are compared in terms of surface morphology and optical reflection. Figure 4.7 shows surface morphology of pyramids textures obtained by different etching recipes. The smallest pyramids size (< 2 μm) was observed for pyramids obtained with Alka-tex additives. Pyramid size for silicon wafers textured using Alka-tex additive is slightly smaller compared to the one textured using IPA additive. In fact, the average size from both sample seems to be very similar. On the other hand, it is clear that standard recipe resulted in very large pyramid size of more than 10 μm in size. For the purpose of light trapping in thin silicon, smallest pyramids are highly preferred. Therefore, for final thin silicon solar cell device, standard recipe was omitted.

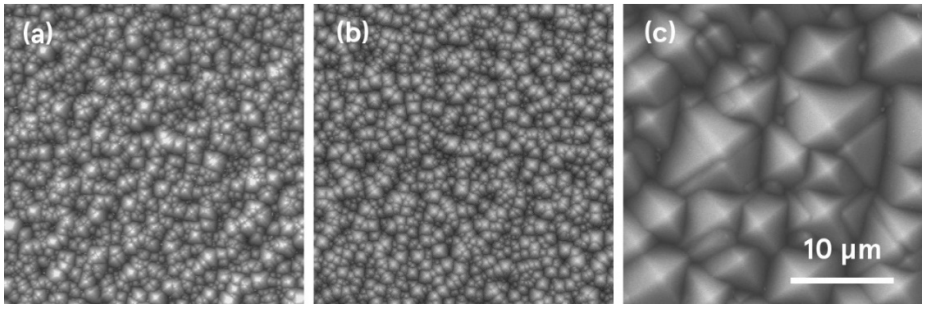

Figure 4.7 Surface morphology of random upright pyramids textured silicon using a) IPA, b) Alka-tex and c) GUNAM recipe.

Figure 4.8 shows the reflection spectra of silicon textured with IPA and Alka-tex recipes, both of which yield reflection that is lower than the standard recipe. Silicon textured with Alka-tex additive shows slightly lower reflection for wavelength below 400 nm and those longer than 1050 nm. Therefore, we concluded that the lowest reflection of silicon is obtained by texturing using the Alka-tex recipe.

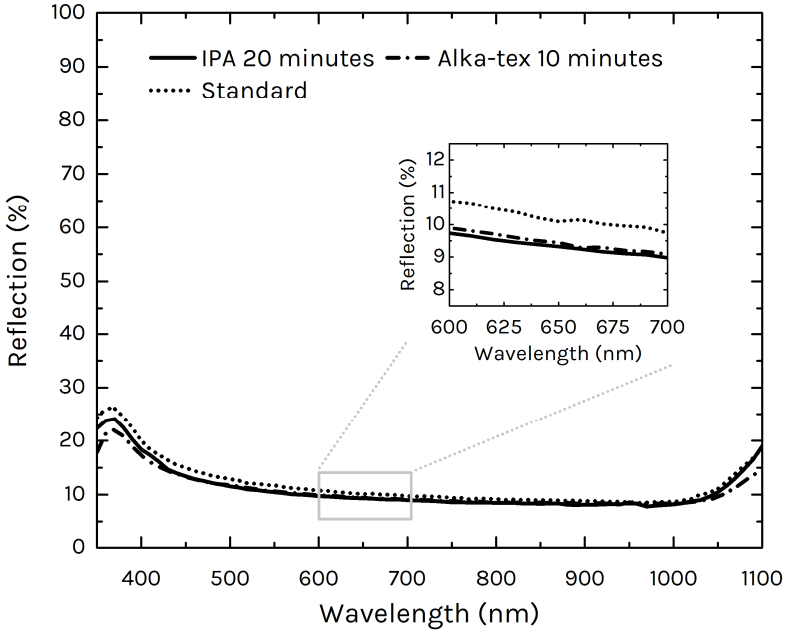

Figure 4.8 Reflection spectra for silicon wafers textured with random upright pyramids obtained by IPA recipe at an etching time of 20 minutes, Alka-tex recipe at etching time of 10 minutes in comparison

with random upright pyramids obtained by GUNAM standard recipe. Reflection of planar silicon is given for comparison.

4.3 Periodic Inverted Pyramids

Other than random upright pyramids, a light trapping structure based on periodic inverted pyramids has also been fabricated. The process naturally allows for minimal material loss since the geometry is already predefined by the photolithography mask.

4.3.1 Fabrication

The process of fabrication of inverted pyramids started with deposition of a 70 nm-thick SiN_x layer on pre-cleaned silicon wafers by PECVD (Plasma Enhanced Chemical Vapor Deposition). SiN_x acts as masking layer for KOH etching process. Photoresist was then coated on the SiN_x-coated silicon wafer. Then a UV exposure step with predefined mask was performed. The mask was a 2D grating with 1 μm hole opening and periodicity of 2 μm. After photoresist development process, a buffered oxide etch was performed to etch uncovered SiN_x layer. Then the photoresist was stripped off in acetone. The patterned wafer was then immersed in a KOH solution with concentration of 3%. The solution was kept at 70 °C. KOH only etches the area where there is no masking layer. Note that the initial opening in the mask layer was circles. However, due to the anisotropy of the etchant, the final structure resulted in square openings. Part of silicon was etched under the masking layer following the (111) plane of silicon. The hanging SiN_x masking layer depicted in Figure 4.9 f can also be seen in the Figure 4.10 c.

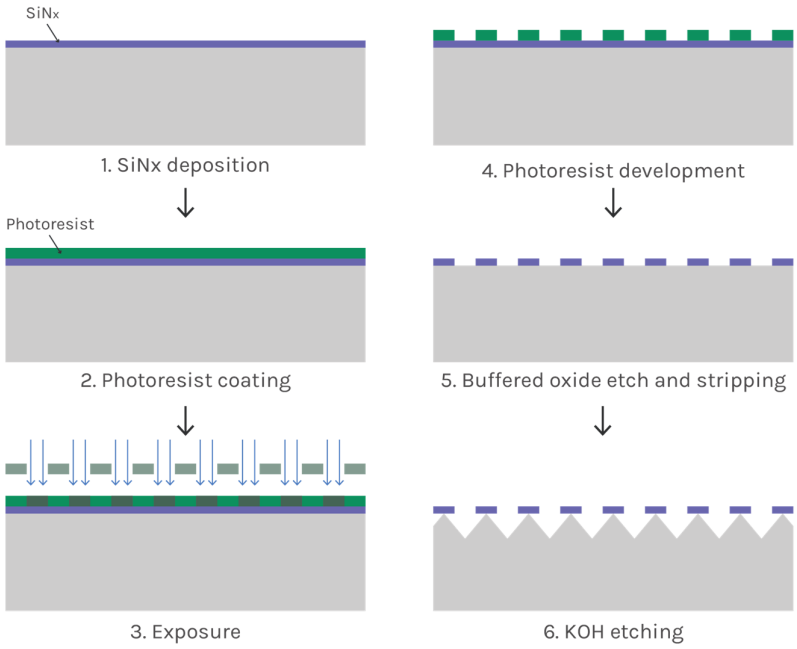

Figure 4.9 Process flow of fabrication of periodic inverted pyramids.

4.3.2 Surface Morphology

The surface morphology of fabricated periodic inverted pyramids is provided in Figure 4.10. By adjusting the initial nitride mask opening size and etching time, the size of the inverted pyramids can also be adjusted. For a small initial opening, an etching time of 3 minutes' results in pyramids with base of 1.6 μm shown in Figure 4.10. By creating larger opening, which can be obtained by intentionally over exposing the photoresist, inverted pyramids with base length of 1.9 μm can also be obtained. As seen on the Figure 4.10, with increasing the base length, the depth of the pyramids also increase. This follows the fact that the angle of the inverted pyramid's side is always 54.7° to the base.

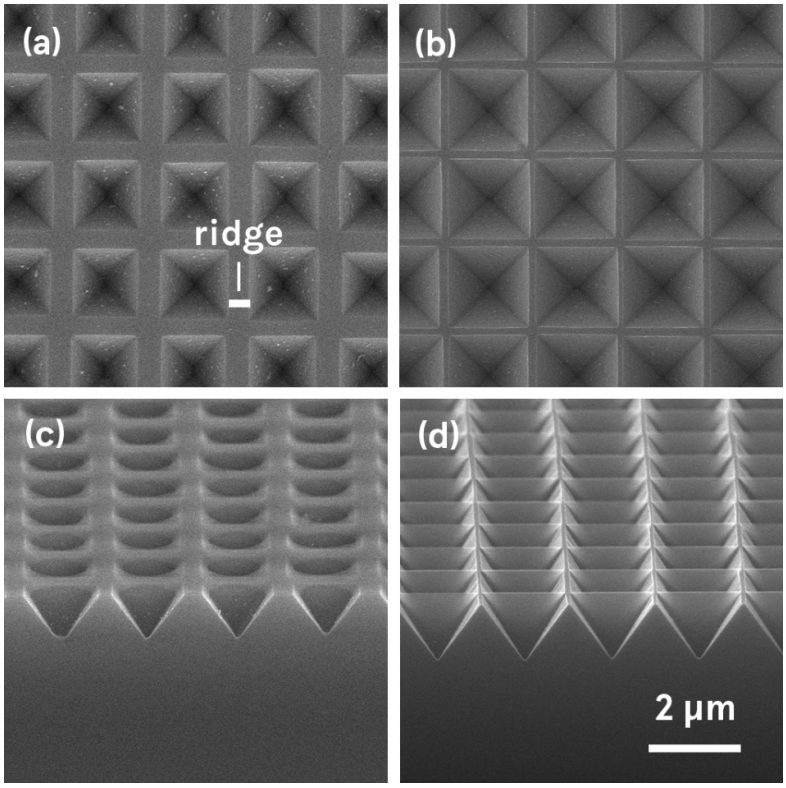

Figure 4.10 Top view of fabricated periodic inverted pyramids with period of 2 µm and ridge separation of a) 400 nm and b) 100 nm. Side view of fabricated periodic inverted pyramids with period of 2 µm and ridge separation of a) 400 nm and b) 100 nm.

4.3.3 Optical Properties

The reflectance spectra of Si wafers with periodic inverted pyramids are plotted in Figure 4.11. The highest reflection value was obtained for inverted pyramids with ridge separation of 400 nm. This can be readily understood, as more planar surface is present on the wafer and therefore reflects more of the incoming light. Decreasing the ridge separation to 250 nm slightly reduces the reflection because of less planar surface coverage. By decreasing the ridge separation to only 100 nm, the reflection value is greatly reduced. It is interesting to note that the reflection in the infrared regime is greatly reduced for all samples when compared to planar silicon.

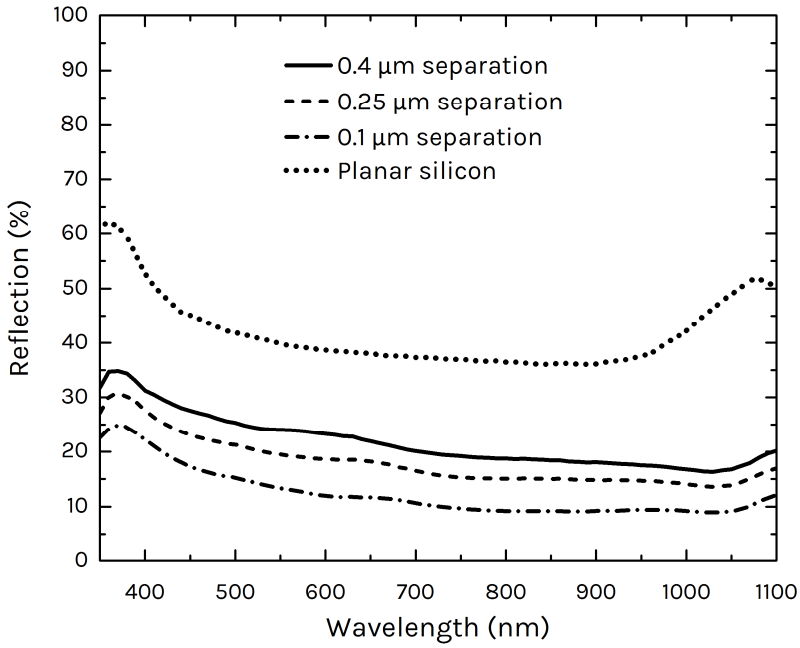

Figure 4.11 Reflection spectra of fabricated periodic inverted pyramids with ridge separation of 0.1, 0.25 and 0.4 µm. The reflection spectrum of planar silicon is also provided for comparison.

4.4 Comparison of Silicon Surface Texturing of Random and Periodic Stuctures

One important aspect other than the optical perforance of surface texturing is material loss during the etching process. Periodic inverted pyramids with periodicity of 2 µm translates to 1.41 µm of material loss in vertical direction. This takes an assumption that there is little to no separation between consecutive pyramids. Therefore, they are very suitable for thin silicon solar cells where minimial material loss is necessary.

Recurring concern regarding standard random upright pyramids is that the etching process removes tens of microns of silicon from the initial wafer. However, with the proposed recipe within this thesis, only ~ 1.7 µm of silicon can be etched to achieve uniform surface coverage of upright pyramids (Figure 4.12). This is based on the best performing random upright pyramids texture obtained by Alka-tex recipe etching of 10 minutes. Meanwhile, up to only ~ 3.3 µm of silicon is etched to result in best performing texture for IPA recipe with etching time of 20 minutes. In comparison, as much as ~8 µm of silicon is etched using GUNAM standard solution for ething time

of 35 minutes (*Courtesy of Sedat Bilgen*). Side view of both random upright pyramids and periodic inverted pyramids are shown in Figure 4.13.

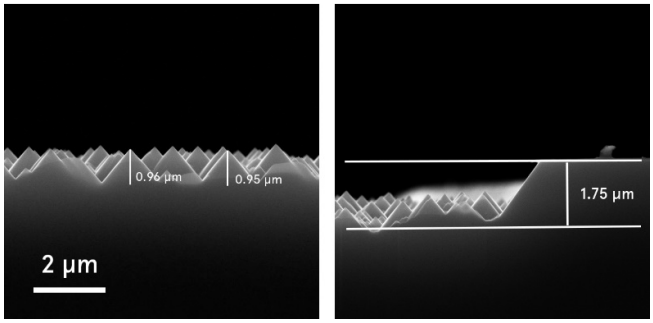

Figure 4.12 Side view SEM images of fabricated random upright pyramids structure by Alka-tex recipe (left) and material loss of silicon for the etching time of 10 minutes (right).

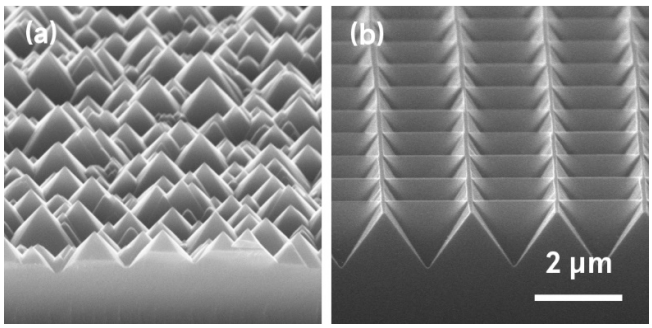

Figure 4.13 Tilted (60 degree) SEM images of a) random upright pyramids and b) periodic inverted pyramids.

For comparison purpose, a sample with periodic inverted pyramids having a ridge separation of 100 nm and random upright pyramids obtained by a 20 minutes etching of IPA recipe solution are used. The reflection spectra of both textures are shown in Figure 4.14. While comparing the reflection value of the random upright pyramids and periodic inverted pyramids, generally, small difference is observed. For the case where the wafers are bare without anti reflection coating, most differences are seen in the range of UV light. At the range of 350 nm to 400 nm, reflection is slightly lower for periodic inverted pyramids. Note that the photon flux at these wavelengths is very small; thus, the reflection difference does not contribute much to the overall reflection performance. From 400 nm to 1000 nm, very little difference in the reflection value is observed. In the infrared range after 1000 nm, periodic inverted

pyramids exhibit less reflection. Again, at this wavelength regime, the photon flux is very little and thus does not contribute much to the overall performance. With that said, comparing the weighted reflection over the whole wavelength range, periodic inverted pyramids indeed perform better than upright pyramids but not by great difference (Figure 4.15).

Upon deposition of anti-reflection coating, as expected, the reflection for both textures is greatly reduced. Similar trend of reflection value is also observed with periodic inverted pyramids having lower reflection at the UV regime. This is partly because the discrepancy in ARC thickness in both sample. Thinner ARC for random upright pyramids texture yields in slightly higher reflection in the UV region. This can also be understood from the minima of the spectrum. The minima for random upright pyramids is present at around 525 nm, meanwhile the minima for periodic inverted pyramid occurs at 600 nm, further confirming the discrepancy in ARC thickness.

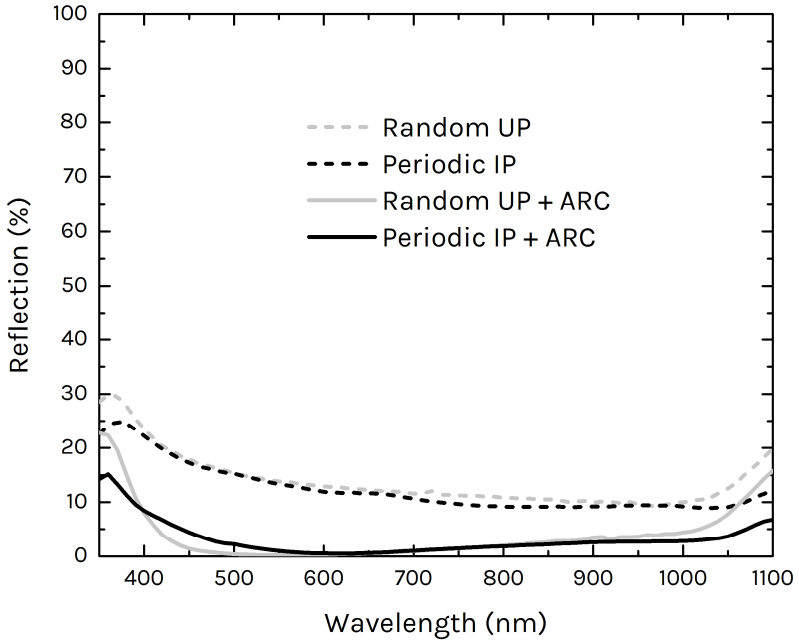

Figure 4.14 Reflection spectra for random upright and periodic inverted pyramids with and without anti-reflection coating.

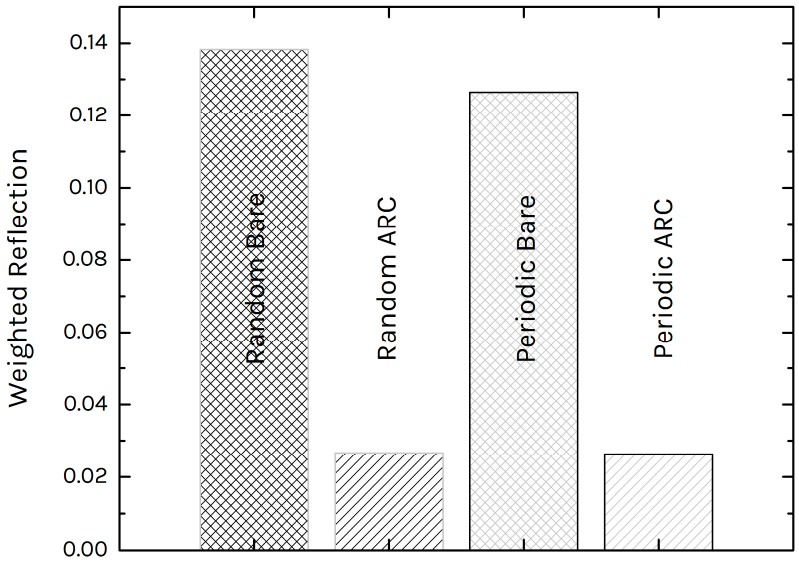

Figure 4.15 Weighted reflection for random upright and periodic inverted pyramids with and without anti-reflection coating

CHAPTER 5

DEVICE FABRICATION

The fabrication process of flexible thin crystalline silicon solar cells is discussed in this chapter. The overall fabrication process flow, depicted in Figure 5.1, includes (1) window opening through a mask, (2) thinning down silicon, (3) texturization, (4) removal of the mask, (5) phosphor doping, (6) ARC deposition, (7) Al deposition, (8) BSF formation by annealing, (9) Ag front contact deposition, (10) Al back contact deposition, (11) SU-8 coating and (12) releasing of thin silicon from the supporting sides.

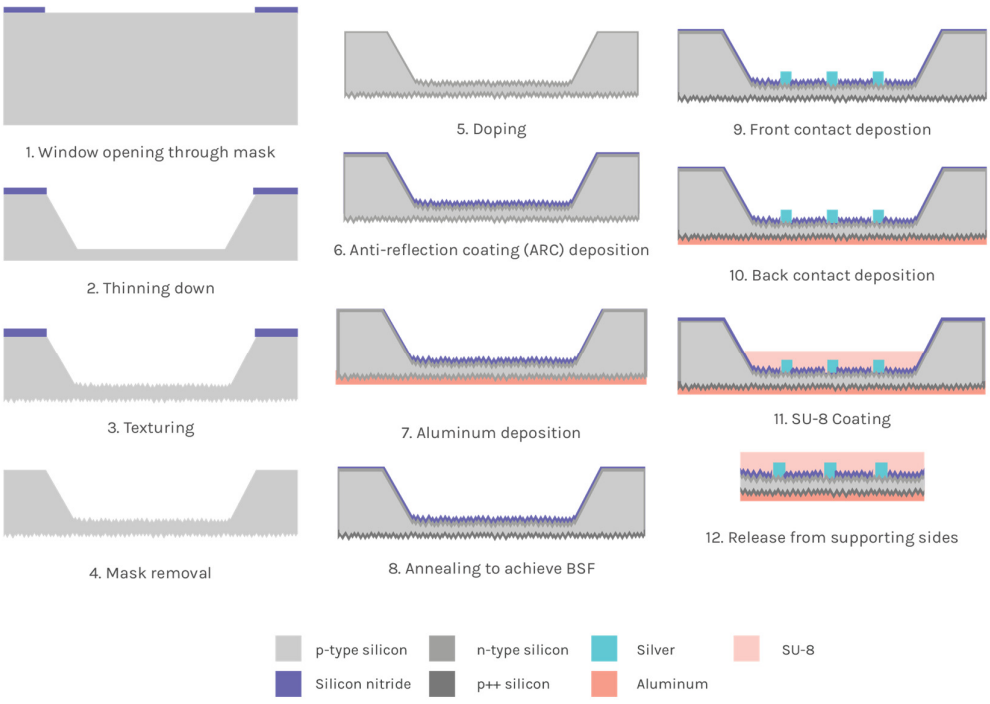

Figure 5.1 Schematic of thin silicon solar cell fabrication process flow.

5.1 Thin Silicon

The process of obtaining thin silicon started with deposition of silicon nitride as masking layer for the proceeding chemical etching process. Prior to deposition of silicon nitride, a 4-inch silicon wafer with orientation of (100) was cleaned in an RCA-1 solution consisting of 6:1:1 of H_2O:NH_4OH:H_2O_2. RCA-1 cleaning was carried out to clean any residues left on the fresh wafers taken out of the container. RCA-1 particularly cleans organic contaminants. Immediately after RCA-1 cleaning, the wafers were immersed in a diluted HF solution with ratio of 100:1 of H_2O:HF to remove oxide layer grown during the cleaning process.

The next step was to put the wafers into a PECVD (Plasma Enhanced Chemical Vapor Deposition) furnace (SEMCO) for silicon nitride deposition. Silicon nitride layer with thickness of around 100 nm was deposited by providing ammonia and silane gas (more details will be explained in the later section).

Following the deposition of silicon nitride, a standard photolithography process was performed to create die pattern on the wafers. A short cleaning step of acetone and IPA was performed to clean any organic remnants on the wafers. Photoresist (S1813) was then spun onto the silicon wafers at 2000 RPM (Figure 5.2 1). Then, the coated wafer was baked on a hotplate at 120 °C for 60 seconds. The process was followed by exposure step on OAI 500 mask aligner. The exposure time was chosen to be 15 seconds with UV lamp power at 13 mW/cm^2. An intermediate post baking process was done on a hotplate at 120° C for 60 seconds, followed by development of photoresist using MF319 solution. During this process, the exposed photoresist area was dissolved in the developer solution leaving the silicon nitride underneath (Figure 5.1 2). Lastly, the wafer was put on hot plate for hard baking at 120 °C for 3 minutes.

Shortly after photolithography process, a chemical etch was performed to remove the exposed silicon nitride layer. Buffered oxide etch (BOE) solution was used for the purpose. The BOE solution consists of H_2O:HF:NH_4F with ratio of approximately 7:1:1. BOE solution selectively etches silicon nitride without creating substantial damage to photoresist (Figure 5.2 3). Next, the photoresist was stripped off in acetone for complete removal. Another short cleaning step in fresh acetone and IPA was performed to clean the photoresist residues.

At this point, a die pattern of silicon nitride opening was formed on silicon wafer (Figure 5.2 4). In order to thin down the silicon, the wafer was immersed in KOH solution prepared with concentration of 50% (by weight) at 90 °C. At this concentration, the etch rate of silicon is approximately 1.2 μm/min (Figure 5.3). It is important to note that with this concentration, a smooth silicon surface finish can be obtained which is beneficial for the proceeding texturing process.

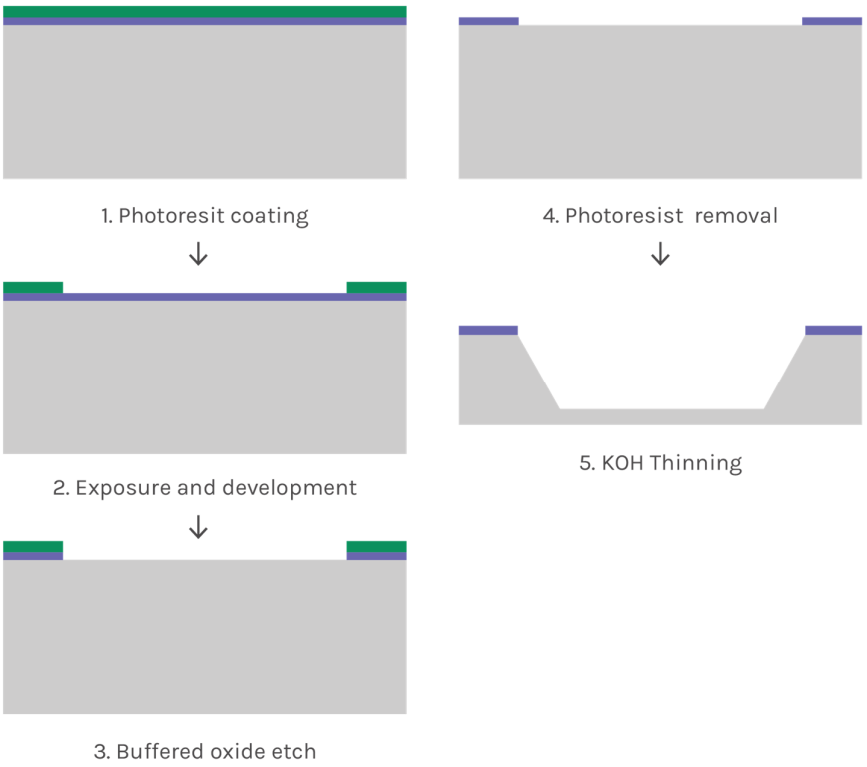

Figure 5.2 Schematic of fabrication sequence for obtaining thin silicon.

Since the etching process was carried out at 90 °C, which is just slightly below boiling point of water, overtime some of the solution KOH evaporates and the concentration of the solution changes accordingly. As a result, etching rate of silicon varies. To minimize the change in the etching rate, the volume of the solution was kept constant by compensating the evaporated water. This was done by feeding the solution with drops of water provided by a setup of IV (intravenous) drop as shown in Figure 5.4. Depending on the surface area of the solution container, the rate of evaporation may also vary. At average about 200 mL of the solution was evaporated in an hour.

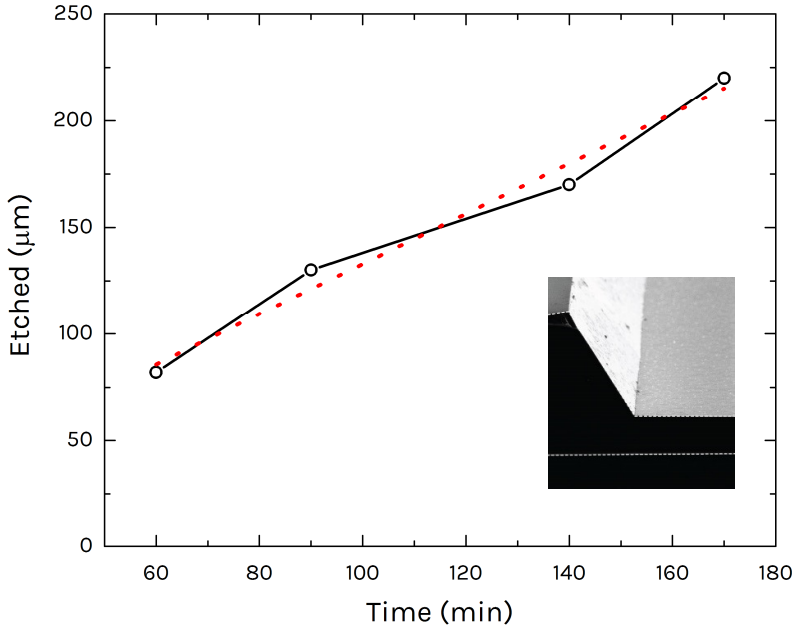

Figure 5.3 Etching rate of KOH solution with concentration of 50 wt% at 90 °C. Dotted line shows the linear fit of the etching rate. The inset figure shows the thinned silicon with thicker side.

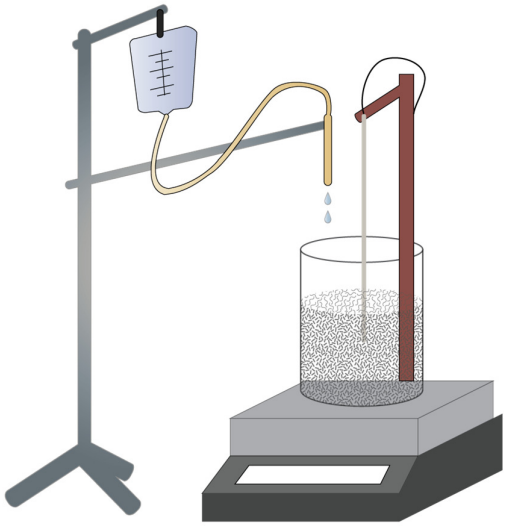

Figure 5.4 Depiction of experimental setup for silicon thinning process by KOH etching.

It should be noted that the rear side of the wafer was also exposed to KOH solution without any masking layer. This way, the etching was taking place from both

sides of the wafer. This served mainly two purposes; a). Reducing the time of etching and b) Elimination of possible pinhole through the wafer. By doing the etching from both sides of the wafers, the time of etching can be drastically decreased into half. The quality of the PECVD deposited nitride was often not perfect in that some pinholes may be present on the layer. Upon immersion into KOH solution, these pinholes allow the solution to go through the holes and etch the silicon underneath. This is especially not desired if the goal was to obtain flat silicon layer.

The starting wafer is a 1-10 Ω.cm p-type silicon wafer with thickness of 525 ± 5 μm. Based on a simple calculation, the required time to obtain 30-μm thick silicon layer is around 180 minutes. The inset of Figure 5.3 shows the thinned down silicon. It can be seen that thicker silicon layer is present next to the thinned silicon. These particular thick sides are important to assist handling. With the thicker sides, it is much easier to handle the thin silicon considering that silicon with thickness of only 30 μm is flexible and at the same time very fragile.

5.2 Texturing

The sequence after obtaining thin silicon was texturization to form random upright pyramids on silicon as shown in Figure 5.5. Taking consideration that random upright pyramids achieved by both IPA and Alka-tex recipe perform comparably well to periodic inverted pyramids and the fact that fabrication process of random upright pyramids requires less complicated and much easier steps, random upright pyramids structure was chosen as the light trapping mechanism for final thin silicon solar cell device. The flexibility of textured thin silicon is seen in Figure 5.6.

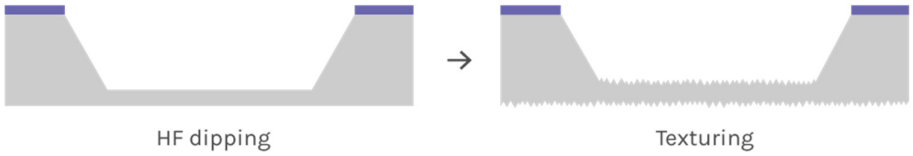

Figure 5.5 Schematic of texturing process via KOH etching.

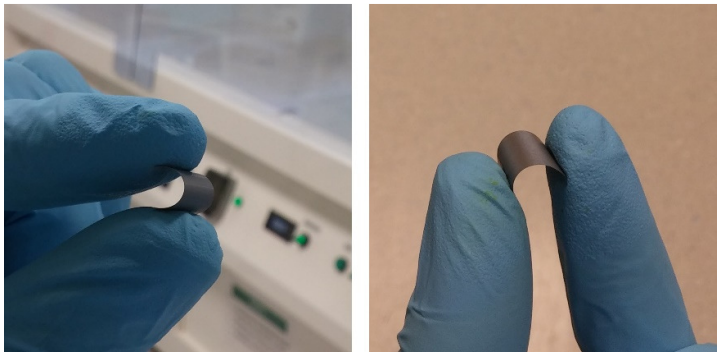

Figure 5.6 Flexible random upright pyramids textured silicon with thickness of ~ 30 μm.

Immediately after the texturization process, the samples were immersed in a diluted HCl (Hydrochloric acid) to neutralize the wafers from potassium ions. It also helps to remove metal ions contaminant that may have deposited on the wafer. Note that at this point, silicon nitride layer was still present on the sides of silicon wafer. To further clean the wafer, RCA-2 cleaning consisting of H_2O:HCl:H_2O_2 with ratio of 6:1:1 was performed. Prior to putting the wafer into RCA-2 solution, the wafers were immersed into a dilute HF solution for 10 minutes to remove native oxide as well as the masking layer of silicon nitride.

5.3 Doping

In order to create a p-n junction within the already textured silicon wafer, a diffusion process of phosphorus atoms is required. Note that the initial silicon wafer was a p-type silicon. Phosphors atoms act as n-type dopant for silicon. Several considerations need to be taken into account while forming the thin n-type silicon layer. Most of the short wavelength photons get absorbed within the topmost layer, which is the n-type layer. This necessitates the n-type layer to be slightly lowly doped as to reduce losses via Auger recombination of minority carriers, which will decrease the open circuit voltage. However, to provide good lateral carrier transport, highly doped n-type layer is needed. This ensures the layer to have low series resistance. Therefore, a good balance between the two inflicting requirements needs to be satisfied.

The process started with immersion of the wafer into dilute HF solution to remove native oxide on the silicon. After drying the wafer in a hot nitrogen blower, the wafers were sent into a diffusion furnace (SEMCO Engineering Incorporation MINILAB Series). The process is depicted in Figure 5.7.

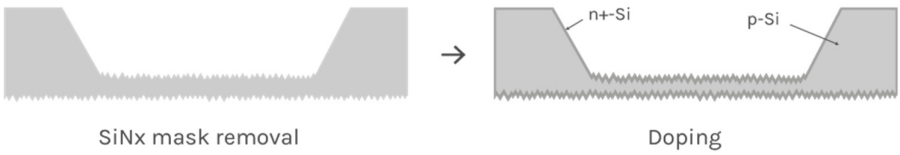

Figure 5.7 Schematic of phosphorus doping step which results in p-n junction both at the front and rear surface.

The doping process was carried out at around 830 °C. The sources for doping were liquid phosphorus oxychloride ($POCl_3$) and oxygen (O_2) carried to the furnace by nitrogen (N_2) gas. The process mainly consisted of two steps, 'pre-deposition' of the dopant in the form of glass to the surface and 'drive-in' for diffusion of dopant from glass to the silicon bulk. The reaction of the process can be simplified and written as following

$$4POCl_3 + 3O_2 \rightarrow P_2O_5 + 6Cl_2 \tag{23}$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \tag{24}$$

It is understood from the reaction (24), after the diffusion process, defective thin layer of glass (SiO_2) is present on the surface (phosphosilicate glass). In order to remove this layer, the wafers were immersed in dilute HF solution until the wafers were free from the defective layer, which was indicated by hydrophobicity of the wafers. To clean the wafer further from contaminants, RCA-2 cleaning was performed for the wafers followed by a short dip in a diluted HF solution. This marks the end of doping process.

5.4 ARC Deposition

The sequence after doping process was anti-reflection coating deposition. ARC layer of SiN_x was coated inside PECVD chamber of SEMCO Engineering Incorporation MINILAB Series. To obtain SiN_x, gas of silane (SiH_4) and ammonia

(NH3) were fed into the system at 380 °C degree and at pressure of 1 Torr. Dissociation of inlet gases to their reactive radicals was provided by means of an RF generator operating at 375 W with a frequency of 50 kHz.

With the help of plasma, the reactive radicals went into reaction expressed as

$$3SiH_{4(g)} + 4NH_{3(g)} \rightarrow Si_3N_{4(s)} + 12H_{2(g)} \quad (25)$$

The product of the reaction was a solid stoichiometric Si_3N_4, which was directly deposited on the silicon wafers as shown in Figure 5.8. By changing the ratio of SiH_4 and NH_3 gas, the ratio of silicon to nitrogen (x) can also be adjusted. As consequence, both optical and surface passivation properties can be tuned. Depending on the value of x, the refractive index of silicon nitride may vary between 1.8 and 2.3. The more silicon content in the SiN_x the higher the value of refractive index [70, 71]. The determination of optical properties of the deposited SiN_x layer was performed using spectroscopic ellipsometry (SEMILAB).

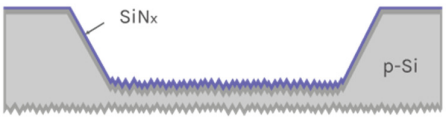

Figure 5.8 Schematic of thin silicon solar cell with SiN_x as ARC layer deposited using PECVD.

5.5 Back Surface Field Formation

The concept of back surface field within silicon solar cells is implemented to reduce current loss due to recombination at the rear side as well as increase collection probability for minority carriers in the n-p layer of silicon. Additional p+-silicon layer is present at the rear side of the existing n-p junction. The presence of p-p+ junction at the back creates an electric field in the same direction of electric field within n-p junction. In that sense, the electric field drives minority carriers within p-silicon layer back to n-p junction at the front. This way, recombination of carriers at silicon-metal interface can be reduced and carrier collection probability is increased.

To form back surface field silicon-aluminum alloying at elevated temperature was performed. Layer of aluminum was evaporated onto the rear side of silicon. The

sample was then annealed at high temperature of 800 °C under nitrogen ambient. The temperature is much higher than silicon and aluminum eutectic temperature of 577 °C. Note that before annealing, the structure of the device is n-p-n with thin n-layer at the backside as well. Upon annealing, aluminum layer alloys with silicon and aluminum atoms diffuse into silicon as shown in Figure 5.9. Aluminum is also p-dopant atoms for silicon and hence p+ layer is formed after the annealing process. The amount of doping can be determined by the amount of initial evaporated aluminum and the thickness of p+-layer can be adjusted by the temperature and time of annealing [72].

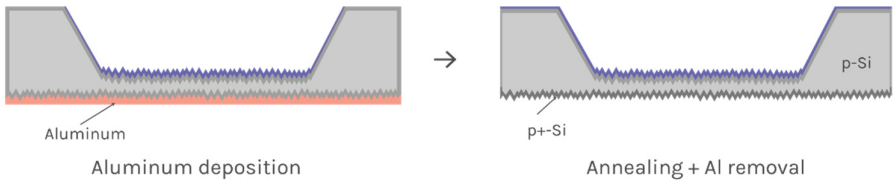

Figure 5.9 Schematic of back surface field (BSF) formation via aluminum alloying.

A strong HCl etch was performed overnight to remove residual aluminum silicon alloy from the wafer. This was done to ensure that all the residues were well cleaned. HCl solution does not attack SiN_x significantly and the ARC layer stayed intact after the long etch process. For further cleaning, RCA-2 cleaning was also carried out right after HCl etch.

5.6 Front Contact Deposition

The next sequence in the process line was to put metal electrodes for collection of photo-generated carriers. Since there was a step height of more than 250 μm from the thin silicon layer to the supporting sides, lift-off process was considered problematic. Firstly, because of the step height, any photolithography mask put on the sample will create gap between the mask and the sample. This may result in distortion of the transferred features. Most important of all, due to the presence of the gap, photoresist sidewalls will not be well defined and thus making it difficult to perform

lift-off process. Because of these reasons, a modified way of depositing metal on the sample was developed.

The sequence started with coating of photoresist on the wafer (Figure 5.10). Positive photoresist of S1813 was spin-coated on the wafers at 2000 RPM for 45 seconds. The choice of the photoresist and spinning speed will be explained later on. The sample was then baked on a hotplate at 120° C for 60 seconds, followed by exposure with features of busbar and finger structures for 15 seconds on a 13 mW/cm^2 power lamp. Another baking step at 120 °C was performed for 60 seconds. Finally, the sample was submerged into developer to remove exposed photoresist. At the end of photolithography process, a hard baking at 120 °C for 3 minutes was done to harden the photoresist so that it was more resistant to the proceeding buffered oxide etch process.

After the photolithography process, a buffered oxide etch was performed to remove SiN_x layer on the photoresist-uncovered region. This was to allow soon to be deposited metal to make direct contact with silicon. It was important at this point that all the pyramids textures on silicon were covered with photoresist. Otherwise, SiN_x layer on them will be etched away. This will reduce the anti-reflection performance. For this reason, a thick photoresist (S1813) was chosen. Slower spinning speed of the spin coater also ensured that the photoresist will be thick enough to cover all the pyramids whose average height is 750 nm.

Shortly after buffered oxide etch process, photoresist was stripped off the sample using acetone. The samples were then cleaned with fresh acetone and isopropyl alcohol. After the samples were cleaned, evaporation of front silver metal was done inside thermal evaporation chamber. To form busbar and fingers shape on the samples, a shadow mask with feature following the one on the previous photomask was created. The shadow mask was created out of silicon wafer with opening formed by marking laser. The shadow mask was aligned onto the sample in a way that the openings align perfectly to the opening on SiN_x layer. The base pressure of the chamber was kept at around $2x10^{-5}$ Torr.

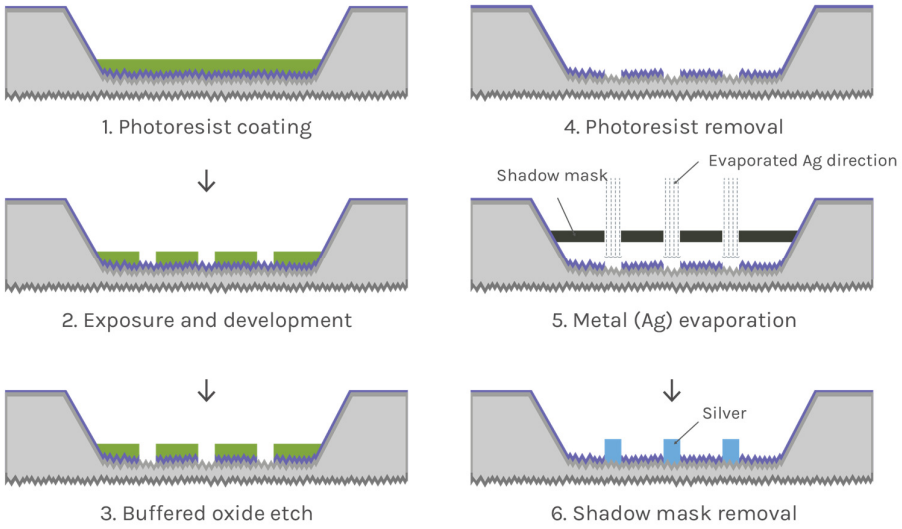

Figure 5.10 Schematic of front contact (Ag) deposition process.

5.7 Rear Contact Deposition

The next sequence in the process was deposition of rear contact of aluminum. After releasing the shadow mask, the sample was flipped so that the rear side was on top. Aluminum evaporation was done inside the same thermal evaporation chamber. The base pressure of $2x10^{-5}$ was maintained for the deposition of aluminum. The deposited aluminum covers the whole rear side of the cell as shown in Figure 5.11.

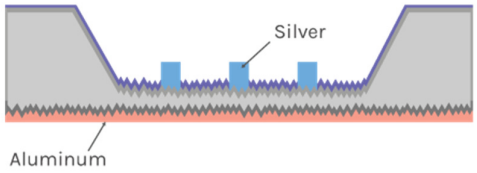

Figure 5.11 Schematic of thin silicon solar cell with rear metal (Al).

5.8 Polymer Coating

The last step of the whole fabrication process was to coat the final working device with a polymer to serve as supporting layer to afford flexibility in the thin silicon. Several considerations have to be taken for the polymer layers. First, if the layer is to be put on the front surface, the polymer has to be transparent over the usable solar spectrum for silicon solar cells. Therefore, a layer with the least parasitic

absorption is preferred. Secondly, the layer has to be flexible and exhibit great mechanical properties. Finally, the layer has to form a good adhesion to the silicon since the layer will be in direct contact. Several different types of polymers have been investigated such as epoxy, PDMS, and SU-8. Among those three, SU-8 proved to satisfy almost all the requirement for good supporting layer.

SU-8 has been shown to exhibit good mechanical properties with great flexibility [73, 74]. As it is seen on Figure 5.12, SU-8 is mostly transparent from 375 nm up to infrared region. SU-8 also proves to exhibit very low parasitic absorption. This makes SU-8 very suitable to be put on top of silicon layer.

A spin coating process was performed to coat the polymer layer. SU-8 100 was spun onto the sample at 3000 RPM, which resulted in a layer with thickness of around 100 μm. Then, the sample was baked with gradual change of temperature. It is important to note that SU-8 is very sensitive to temperature change during baking process. Careful thermal treatment of SU-8 is therefore necessary. The baking step started with 50 °C for 10 minutes, then 65 °C for 20 minutes and finally 90 °C for 45 minutes. Since SU-8 is a negative photoresist, a flood exposure of UV light is necessary to crosslink it. An exposure step of 60 seconds with lamp power of 13.5 mW/cm^2 was done afterwards. Another post bake of SU-8 was done after exposure. The baking process was 50 °C for 10 minutes, then 65 °C for another 10 minutes and 75 °C for 30 minutes. The resulting layer from this process was a stress-free SU-8 with good mechanical properties as well as good flexibility as shown on the Figure 5.13.

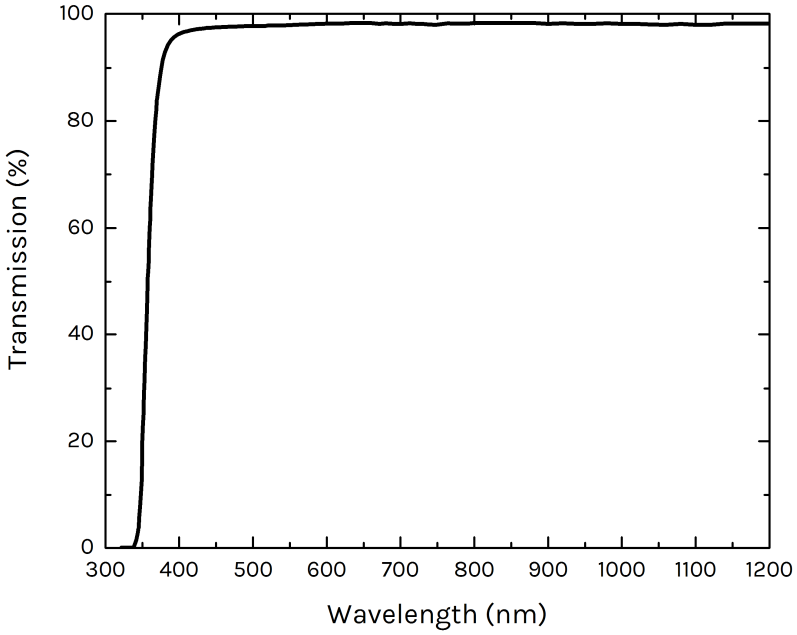

Figure 5.12 Transmission spectrum of SU-8 over wavelength of interest.

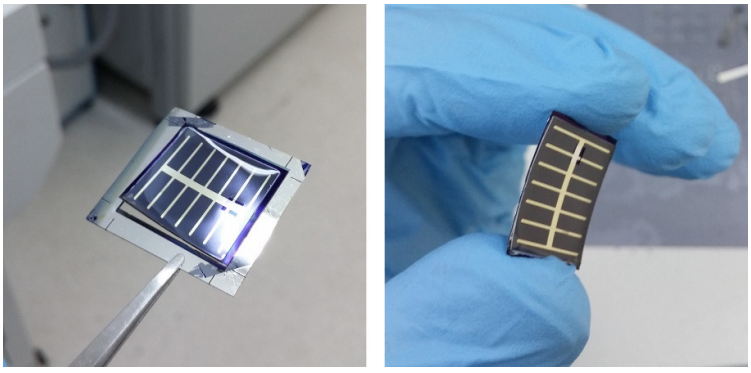

Figure 5.13 Thin silicon solar cell with SU-8 polymer layer deposited on top. Flexibility property is also shown on the right figure.

CHAPTER 6

DEVICE CHARACTERIZATION

In this chapter, optical and electrical characterization of fabricated thin silicon solar cells will be explored. In addition, a loss analysis of the fabricated devices will be provided.

6.1 Optical Characterization

Thin silicon with thickness of 30 μm with a good thickness uniformity was fabricated as shown in the Figure 6.1. In addition, texturing of random upright pyramids with sizes less than 2 μm was performed onto the thin silicon. Reflectivity of the textured thin silicon is plotted in Figure 6.2. The reflectivity is similar to the case where the pyramids sizes are larger than 5 μm (discussed in Chapter 4). Upon addition of anti-reflection coating, the reflectivity is further reduced over the whole wavelength range. This is easier to see in the shorter wavelength regime where reflection is greatly reduced.

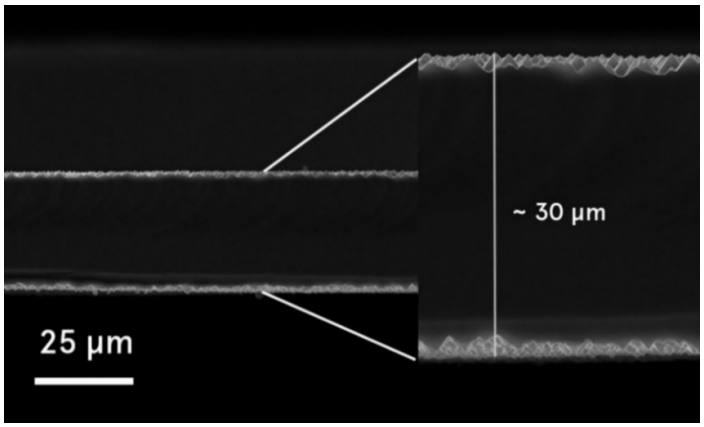

Figure 6.1 Cross section SEM view of 30 μm-thick textured silicon.

The reflectivity is even further reduced in the infrared regime upon deposition of back reflector of aluminum. However, it is important to note that parasitic absorption in rear Al metal layer has to be considered. Parasitic absorption, especially in the infrared regime, is due to excitation of surface plasmon polaritons [75].

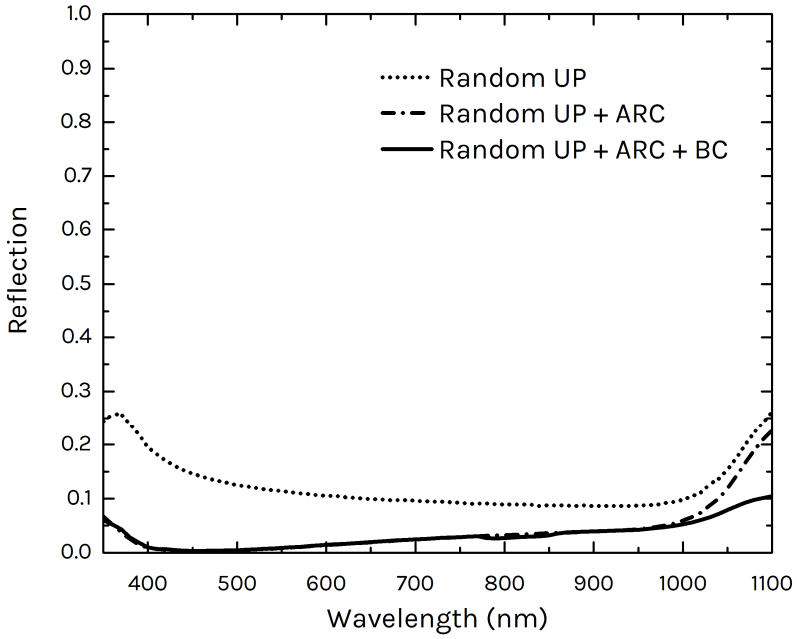

Figure 6.2 Reflection spectra of textured thin silicon without, with antireflection coating and with both antireflection coating and rear metal reflector.

The result of transmission measurement of textured thin silicon is shown in Figure 6.3. For the case where there is only ARC, it can clearly be seen that some of the light in infrared transmitted. Upon deposition of rear Al metal layer, no light is transmitted through the rear side.

By considering the measured value for reflection and transmission, absorption is calculated using equation (1). The absorption spectrum is plotted in the Figure 6.3. The optical absorption of thin silicon with small (< 2 μm) random upright pyramids is also compared to thick silicon with large (>7.5 μm) random upright pyramids texture. In the UV regime, thin silicon with small pyramids absorbs slightly higher amount of light. This may be attributed to the fact that the size of the pyramids is much smaller and thus better light coupling in the UV regime. Over the visible spectrum, the

absorption spectra for both textured thin and thick silicon are almost identical. However, towards the infrared region, it is clear that the absorption of thin silicon is lower than thick silicon, but not by a large margin. In fact, considering that the thickness is one fifth of the thick silicon, it performs very well. It absorbs light almost as much as thick silicon with large pyramids does.

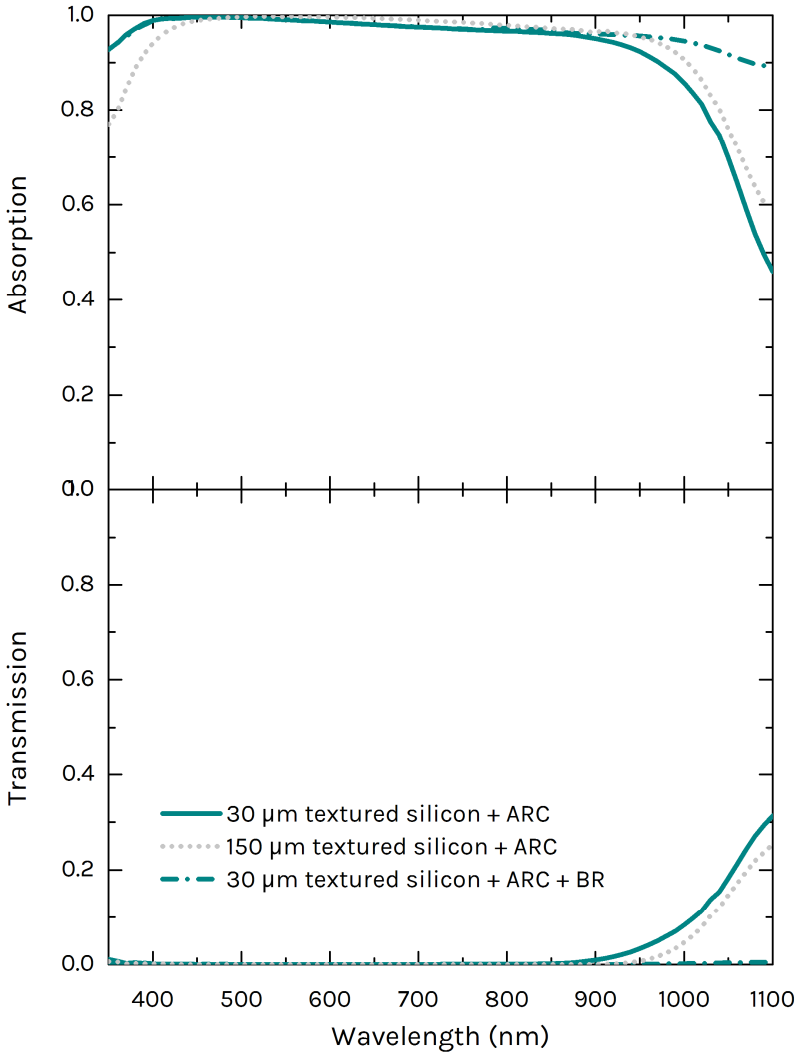

Figure 6.3 Transmission and absorption spectra of ARC coated textured thin silicon with and without metal back reflector (BR) in comparison to textured thick silicon with antireflection coating.

6.2 Electrical Characterization

Both planar and textured thin silicon cells with thickness of ~30 μm have been fabricated. JV characteristics of the cells were measured by an AM1.5G calibrated class 3A flash solar simulator (QUICKSUN 120CA-XL). The results of JV measurements are given on Figure 6.4. It is apparent from the JV curve that the planar cell produces a lower short-circuit current of 27.12 mA/cm^2 in comparison to textured cell with value of 32.96 mA/cm^2. An improvement of nearly 30% in the short-circuit current has been obtained by the textured cell. The obtained J_{sc} of the textured cell is still far below maximum attainable current calculated via Lambertian limit of 36.26 mA/cm^2 for 30 μm-thick silicon. The current loss will be discussed in the later section. However, it is clear that there is indeed still ample room for improvement.

Two textured samples with different amount of Al in BSF formation were fabricated. Textured 1 sample with more Al amount is expected to have higher BSF doping concentration compared to textured 2 sample. Distinct JV characteristics were observed for the two cells. Textured 1 sample exhibits higher fill factor of 73.39% compared to 69.71% for textured 2 sample. The lower value of fill factor of textured 2 cell mainly comes from poor series resistance of the contacts. It was also observed that V_{oc} is slightly improved with increasing BSF doping. Overall, higher efficiency is achieved for textured 1 sample. Nevertheless, both V_{oc} values for textured devices are still higher than the V_{oc} of planar device. This is expected as more light is being absorbed within the cell and following equation 16, higher V_{oc} value is expected.

Device characteristics of the planar and textured sample are tabulated in table 6.1. Texture 1 sample exhibits the highest efficiency with 13.6% efficiency. An efficiency increase of more than 3% (absolute) has been obtained for textured thin silicon solar cell with thickness of 30 μm compared to planar cell.

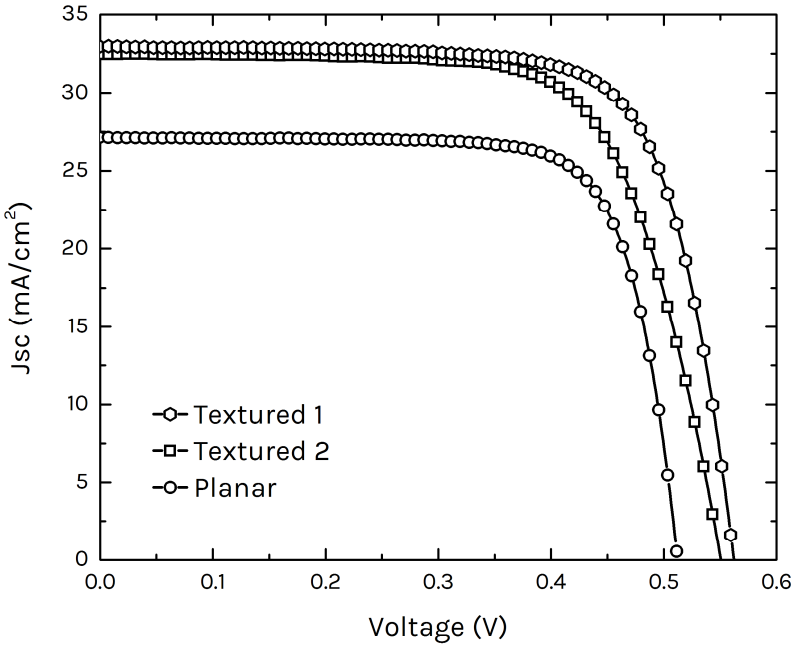

Figure 6.4 Current density-voltage curves of planar and textured thin silicon solar cells.

Table 6.1 Current density-voltage characteristics for planar and textured cells.

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
Planar	0.512	27.12	75.86	10.54
Textured 1	0.562	32.96	73.39	13.6
Textured 2	0.55	32.46	69.71	12.45

The result of external quantum efficiency measurement is provided on Figure 6.5. Form the figure, it is clearly seen that improvement in the external quantum efficiency is observed over the whole range of wavelength when comparing planar and textured cells. The improvement is even more evident in the wavelength larger than 800 nm.

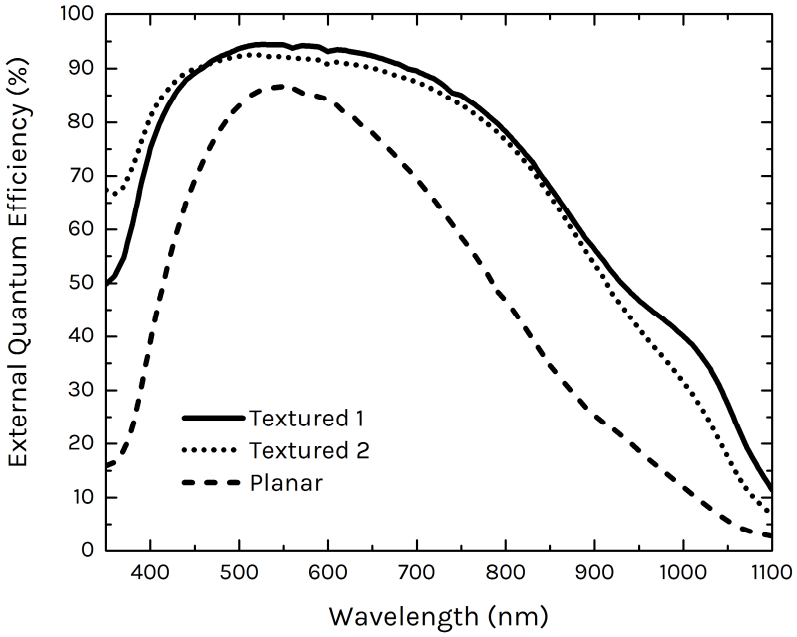

Figure 6.5 External quantum efficiency spectra for planar and textured cells.

Looking at EQE spectra of textured device, over the range of 400 nm to 800 nm, the EQE is well above 80%. However, poor response has been observed for UV regime and infrared regime. Above 800 nm, the EQE starts to drop significantly. The poor UV response may arise due to loss from surface and Auger recombination. Most of the short wavelength light is absorbed within the top most layer where the highly n-dope layer is present. With the higher doping, more Auger recombination loss is expected. The fact that no excellent surface passivation is present on the emitter may also contribute to most of the losses in the UV regime. The loss above 800 nm may be attributed to the parasitic absorption within rear Al metal layer. It is well known that aluminum absorbs some amount of light in the infrared. The device structure of Al-BSF also suffers from poor rear surface passivation as the whole rear side is covered with highly recombinative silicon-metal interface. As results, carriers that are generated at the rear region recombine before being collected by the metal electrode decreasing the quantum efficiency.

6.3 Loss Analysis

Despite the excellent absorption value over the entire spectrum, Figure 6.6 shows that most absorbed photons are lost especially in the UV and infrared regime. Within UV region, the reason for the low quantum efficiency can be broken down to surface recombination and parasitic absorption in SiN_x layer. In the range of 350 nm $< \lambda <$ 450 nm, the loss contributes to 0.68 mA/cm^2. At these wavelengths range, the photon flux is relatively lower and therefore the loss is not significant. In the range of 450 nm to 800 nm where photon flux is at its maximum, as much as 1.87 mA/cm^2 of current density is lost. At this region, most photogenerated carriers might be lost due to recombination within the bulk by means of Shockley Read Hall recombination. By far, the current loss is greater for wavelengths above 800 nm. In this wavelength regime, 7.50 mA/cm^2 of current density is wasted. Considering that long wavelength lights are mostly absorbed after more than single pass and at the rear side of the solar cells, most of the loss may be attributed to the poor rear surface passivation. Bulk recombination via SRH recombination also plays another great role to the loss at long wavelength since most of the light absorbed within the bulk of the cell. In addition, parasitic absorption in rear metal aluminum layer adds to the loss in the long wavelength.

In total, out of possible 41.86 mA/cm^2, only 31.78 mA/cm^2 of current density can be obtained from the final thin silicon solar cell device. A slight discrepancy between J_{sc} obtained from EQE and JV measurement may arise because the EQE measurement does not cover the whole spectrum of the Sun, unlike the JV measurement setup. Poor response of silicon photodetector used in EQE setup may have also resulted in slight change of values obtained.

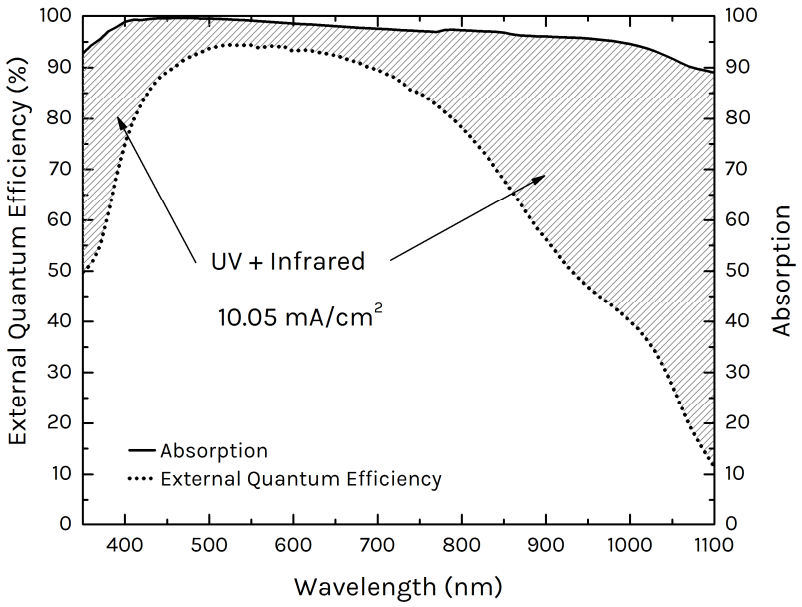

Figure 6.6 Internal quantum efficiency and absorption spectra for best textured cell. Shaded region shows the current loss within the cell.

Thin silicon is less dependent on the bulk recombination loss or in other words the quality of the wafer. However, thin silicon is very sensitive to surface recombination loss. With this consideration, a high value of V_{oc} is to be expected [76]. However, looking back at the JV curve on Figure 6.4, only 563 mV of open circuit current is obtained. One possible explanation to this might be due to the absence of perfect surface passivation on the device. Only SiN_x layer on the front surface acts as passivation layer. This increases the recombination loss significantly and hence reduces the value of V_{oc}. To improve the front surface passivation, addition of thin layer of SiO_2 can be implemented. Indeed, most highly efficient silicon solar cells include thin layer of SiO_2 grown by either dry or wet oxidation [42].

The fact that the final device adopts Al-BSF device structure also plays important role to the loss of J_{sc} and V_{oc}. The rear interface between highly doped p+-silicon layer and metal exhibit very high surface recombination velocities. Carriers that are generated near the interface are likely to recombine and not contribute to current. Not only does it decrease the short-circuit current; it also reduces open circuit voltage. Note that the final device of textured cell also has the rear side textured. What this means is that the surface area is greatly enhanced and therefore will lead to even

more severe surface recombination loss. In addition, larger surface area leads to more excitation of surface plasmon polariton, increasing parasitic absorption in the real Al metal layer. With this in mind, rear planar surface is expected to reduce the loss in the rear side if the Al-BSF structure is maintained.

The best performing thin silicon solar cell device exhibits only modest 73.39% of fill factor. The main loss mechanism for the fill factor may have come from the fact that the evaporated metal contacts are considerably thin both for rear aluminum and from silver contacts. Thin metal lines increase the contact resistance significantly. To further improve the fill factor, more complex contacting scheme can be utilized such as titanium/palladium/silver contact for the front side. Indeed, this contact scheme has been used for many record breaking silicon solar cells [55]. The common problem for all silver contact on silicon is that the adherence of silver to silicon is very poor and unreliable. Titanium layer acts as adhesion layer to silicon and in addition, the band structure of titanium match well with silicon to form Ohmic contact. The thin palladium layer serves as diffusion barrier layer for silver. It is well known that silver tends to penetrate into titanium where electrochemical reaction may occur [77].

6.4 Flexible Thin Silicon Solar Cells

As previously mentioned, to obtain flexible device, thin SU-8 layer is deposited on top of the working thin silicon solar cells. The final cell with thickness of 30 μm includes 100 μm thick SU-8. The result is a very flexible thin silicon solar cell as can be seen on Figure 6.7. The device can be bent with radius of curvature of 1 cm without any mechanical failure. The device also exhibits good twistable characteristics. Not only that SU-8 acts as supporting layer, it also serves the purpose of lamination layer to protect the metal contact from oxidation over long term. Further mechanical test needs to be performed to assess the stability.

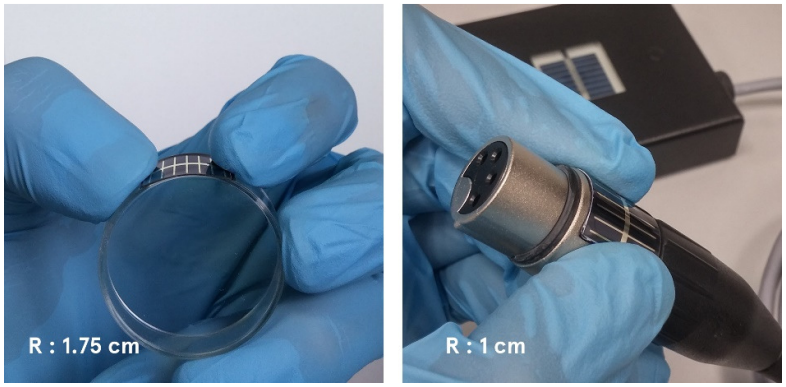

Figure 6.7 Flexible thin silicon solar cell with great flexibility at radius of curvature of 1.75 cm (left) and 1 cm (right).

CHAPTER 7

CONCLUSION AND OUTLOOK

Photovoltaic checks all the marks when it comes to satisfy world demand for environmentally friendly alternative energy source. In particular, silicon solar cells offer tremendous possibility. With its great abundance as well as the maturity of the technology, silicon solar cells are still the primary choice among all other PV technologies. One prominent challenge that still surrounds silicon solar cell technology is the cost. One of the many routes to reduce the cost of the cells is to use thinner silicon wafers.

Silicon is an indirect semiconductor and a poor material for applications where plenty of light absorption is essential, as such in the case for solar cells. Owing to its very low absorption coefficient towards its optical bandgap, silicon wafers as thick as 10 mm are necessary to fully absorbs all the incoming light. Most commonly used thickness for state-of-the-art silicon solar cells is about 180-250 μm. Even at this thickness, silicon wafer itself accounts for more than 40% of the total cost of the solar cell. It is clear that reducing the thickness of the silicon will bring about potential cost reduction. However, common problem at reducing the silicon wafer is the absorption loss which in turn reduces the photo-generated current and hence the efficiency. The proven way at increasing the absorption in silicon is to incorporate light trapping structures. In other words, it is the act of elongating the light path inside the absorber layer. Theoretical calculation has shown up enhancement up to 50 folds can be achieved for silicon.

For conventional single c-Si solar cells, the way at achieving light trapping is to form random upright pyramids with sizes around 5-15 μm on the surface by alkaline etching process. It has proved to be an efficient way at enhancing the absorption within silicon. While this is an efficient way for silicon with thickness of more than 150 μm,

it is not suitable for thin silicon with thickness of only 20-30 μm. Alternative ways of achieving light trapping schemes on thin silicon is therefore necessary.

In this thesis, two different routes of light trapping structure fabrication for thin silicon were explored. The first one was to fabricate random upright pyramids with maximum size of 2 μm while at the same time minimizing material loss. The second method was to fabricate periodic inverted pyramids with sizes less than 2 μm. To fabricate small random upright pyramids, two KOH containing solutions; one with IPA and another one with Alka-tex additive were used. Meanwhile, to fabricate periodic inverted pyramids, a photolithography step with initial mask of 2 μm periodicity was carried out. A chemical etching with KOH was performed after the photolithography process to form inverted pyramids on (100) silicon wafers.

Random upright pyramids with a maximum size of 2 μm were fabricated with both IPA and Alka-tex recipe. At the same time, periodic upright pyramids structure with periodicity of 2 μm, which translates to a depth of 1.47 μm, was fabricated. Comparison of the optical performance of both random upright pyramids and periodic inverted pyramids showed that the two structures exhibit similar properties. Upon anti-reflection coating deposition, random upright pyramids showed lower reflection in short wavelengths over the inverted pyramids. Taking into consideration that both structures perform comparably well and the fabrication of inverted pyramids requires more complicated processes, random upright pyramids structure was chosen for the light trapping scheme of thin silicon solar cells fabricated in this study.

To obtain thin silicon, a chemical etching of bulk silicon was performed using highly concentrated KOH solution. Thin silicon with thickness of ~30 μm was fabricated. In addition, a good thickness uniformity of the thin silicon was achieved. With small random upright pyramids, 30 μm-thick silicon can absorb almost as much of light of 150 μm-thick silicon textured with large pyramids. It further shows the possibility of achieving high-efficiency silicon solar cell in spite of the reduced thickness. Finally, thin planar and textured thin silicon solar cells were fabricated via conventional silicon solar cells fabrication processes.

It was clear from the results that surface texture of random upright pyramids greatly enhances the short circuit current of the device. The enhancement of more than

30% in the short circuit current was achieved in the textured cell when compared to the planar cell. The open circuit of the textured device was increased as a consequence of short circuit improvement. However, despite the excellent optical performance of the textured device, only about 32 mA/cm^2 of J_{sc} was collected. This is far lower than the maximum calculated J_{sc} of 37 mA/cm^2. This is mainly due to the poor carrier collection efficiency, especially in the infrared region.

The obvious reason for the low carrier collection performance was that the device adopted Al-BSF structure, which is well-known for poor backside carrier collection. Carriers generated near the rear Al metal contact can easily recombine and therefore do not contribute to the photocurrent. To some extent, the recombination can be suppressed by local Al doping to create a back surface field. Additionally, the presence of full Al coverage on the rear size adds parasitic absorption in the infrared region further reducing the light absorption within the solar cells. The evidence of poor carrier collection was observed through internal quantum efficiency measurement. Nevertheless, efficiency of 13.6% is achieved for textured thin silicon solar cells. This is a sizable improvement over planar silicon solar cell with an efficiency of only 10.01 %.

In the end, it is apparent that one of the prominent limiting factors for achieving highly efficient thin silicon solar cells is the poor carrier collection and parasitic absorption in the real metal layer. One clear pathway to improve these is to adopt Passivated Emitter and Rear Cell (PERC). Within PERC cells, an additional dielectric layer is present at the rear side just between Al metal contact and silicon. The dielectric layers can be silicon dioxide, silicon nitride or aluminum oxide. To create contact with silicon, local contact openings are opened through the dielectric layer. The presence of the dielectric serves the purpose of passivating the rear side. In this way, silicon-metal interface is minimized, hence minimizing the recombination of carriers in the rear side. By suppressing the carrier recombination, an improvement in the open circuit voltage is also expected. Not only that it helps at improving V_{oc}, the dielectric layer also increases the rear reflectivity of light, especially in the infrared regime on the rear side. It can also reduce parasitic absorption in the real metal layer. As a result, the optical absorption within the silicon absorber layer is improved. Therefore, adopting

PERC structure to thin silicon will not only bring about the improvement in V_{oc} but also J_{sc} at the same time.

Another possible route to increase the efficiency of the thin cells is to improve the front surface passivation if the Al-BSF structure is maintained. The effect of the absence of perfect surface passivation has been clearly shown in the quantum efficiency measurement. It is most apparent in the UV range where light absorption occurs near the un-passivated surface, which acts as recombination center. In fact, the front surface passivation will help not only limited to Al-BSF but also PERC structure.

Alternative Light Trapping Structure

Random nanostructures enabled by simple chemical etching processes can also provide alternative methods for light trapping structures in ultrathin Si. One candidate for such simple chemical etching processes is metal assisted etching (MAE). MAE is a highly flexible technique for fabricating various structures on Si, ranging from nanometers to micrometers in size [78–80]. Weighted reflection of less than 3% over full commercial size of Si solar cells was previously achieved [81, 82].

In brief, the MAE process can be explained as accelerated oxidation and etching of Si by HF near metal nanoparticles formed on the surface by electroless deposition. A schematic of MAE process and an example of Si surface achieved by MAE are shown in Figure 7.1. The mechanism of reactions is as follows. In the cathode, reduction of Ag ions and HNO_3 at the surface occurs via the following reactions:

$$Ag^+ \rightarrow Ag(s) + h^+ \tag{26}$$

$$HNO_3 + 3H^+ \rightarrow NO + 2H_2O + 3h^+ \tag{27}$$

While at the anode, oxidation and etching of Si takes place via the following reactions:

$$2Si + 12HF + 6h^+ \rightarrow \ 2H_2SiF_6 + 6H^+ + H_2 \tag{28}$$

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \tag{29}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{30}$$

Holes generated by reaction (26) and are transferred to the metal-silicon interface through metal dendrites. Etching of Si occurs in hole-rich regions. The reaction repeats until all the chemical species are consumed. After the MAE process, the residual silver dendrites are removed with HNO_3 and subsequent RCA cleaning.

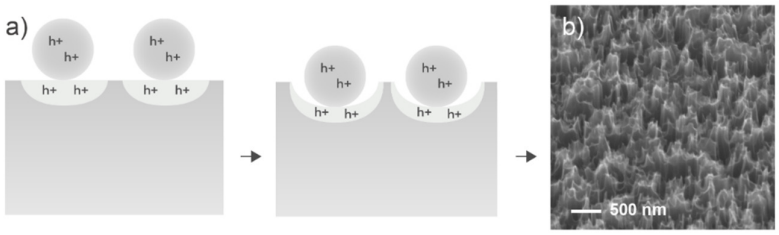

Figure 7.1 a) Schematic of metal assisted etching process. b) Side view of nanostructure texture on silicon surface

The MAE process yields in a dense high aspect ratio structures whose average height is about 500 nm. The structures provide graded refractive index from air to silicon and acts similarly to antireflection coating, which helps reduce front side reflection substantially. Figure 7.2 shows comparison of reflection spectra of random upright pyramids and nanostructures textured silicon with an additional ARC layer of SiN_x. For small wavelength up to 400 nm, nanostructures seem to exhibit smaller reflection. This is likely because the size of the structure is in the order of the incoming wavelength and provide better light coupling. Throughout the visible spectrum, random upright pyramids provide less reflection thanks to its optimized ARC thickness. For the rest of the spectrum towards infrared, lower reflection is observed for nanostructures textured sample exhibits lower reflection. Overall, both structures provide similarly great optical properties. Low weighted reflections of 2.33% and 2.53% have been achieved by both nanostructures and random upright pyramids textures, respectively.

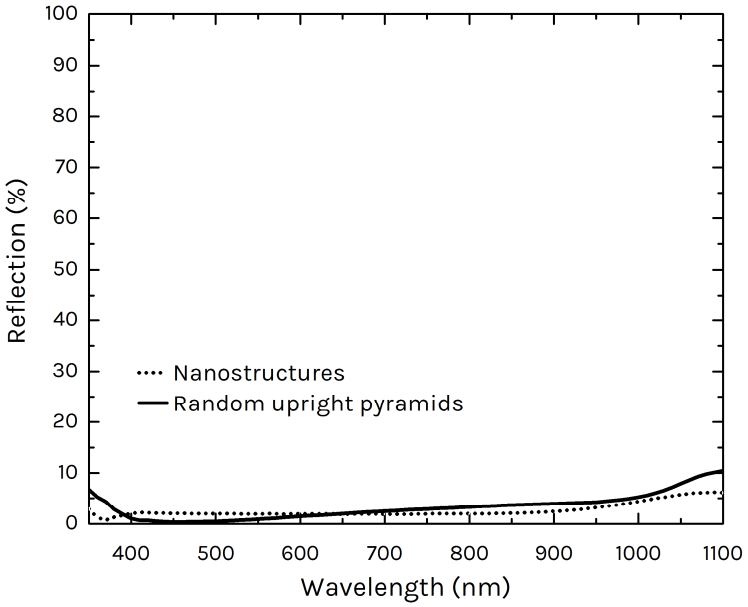

Figure 7.2 Reflection spectra of random upright pyramids and nanostructures with antireflection coating of SiN_x.

Similar device fabrication process was performed for final thin nanostructures silicon solar cell. Despite having very low reflection (<10%) in the measured wavelength range, the fabricated nanostructure textured solar cell only collected a J_{sc} of 26.24 mA/cm^2, 6 mA/cm^2 less than the best performing random upright pyramid textured cell (Figure 7.3). This is ascribed to the fact that the surface area of the nanostructures is greatly enhanced, which increases surface recombination losses. In addition, due to the high aspect ratio geometry of the structures, the same doping conditions result in relatively deeper junction in the emitter. With the increase in junction depth, Auger recombination loss in the emitter is also enhanced. From EQE spectra in Figure 7.4, it is clear that losses in carrier collection are predominantly occurring in the UV region. Light at relatively short wavelengths (<500 nm) is mostly absorbed within the uppermost layer of Si owing to its high absorption coefficient. Most carriers in the upper region of the cell are susceptible to surface and Auger recombination. Nevertheless, with improved surface passivation, an increase in the carrier collection efficiency is expected. Indeed, an efficiency of 22.6% has been achieved for similarly textured thick silicon solar cells [83]. The passivation scheme can achieved by means of atomic layer deposition, which provides excellent coverage of film growth.

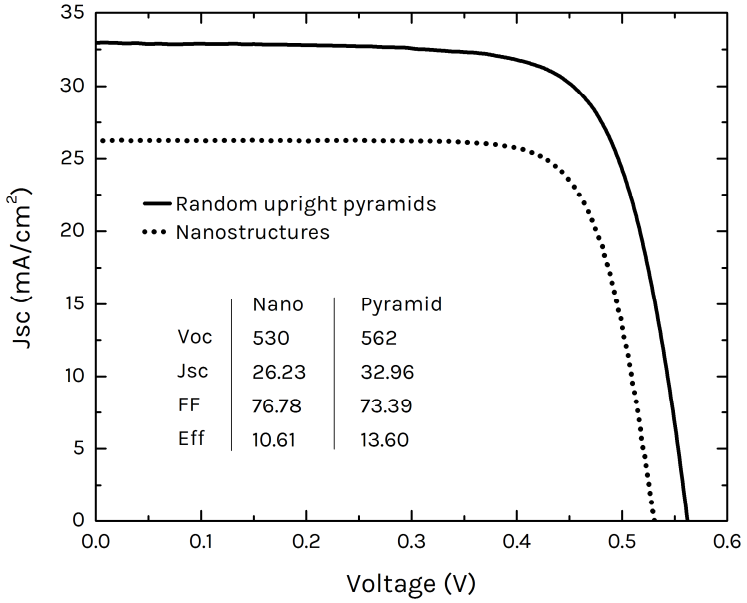

Figure 7.3 Current density-voltage curve for both 30 μm thick nanostructures and random upright pyramids textured silicon solar cells.

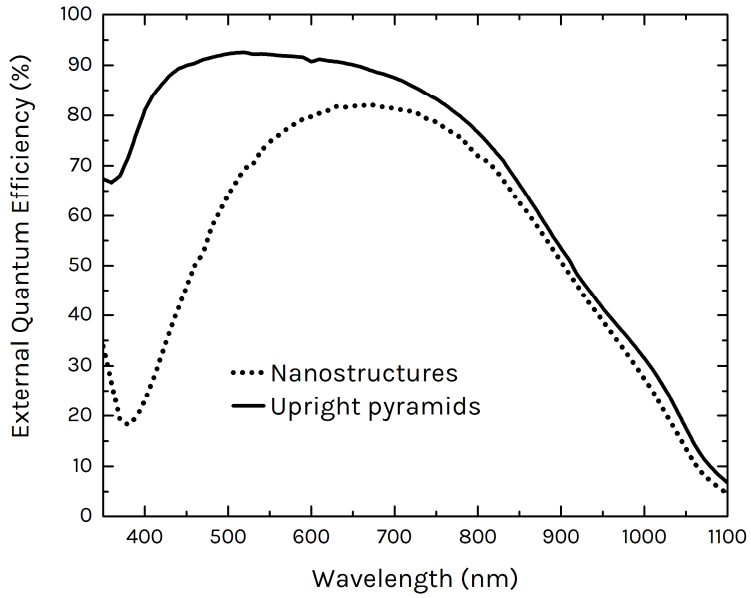

Figure 7.4 External quantum efficiency spectra for both 30 μm-thick nanostructures and random upright pyramids textured silicon solar cells.

Overall, it is clear that with proper surface passivation engineering and device optimization, both random upright pyramids and nanostructures textures may provide high efficiency for relatively thin absorber.

APPENDIX

Characterization techniques

Current-voltage measurement was performed in a calibrated QuickSUN (WCT) under AM1.5 illumination. Surface morphology was obtained using scanning electron microscopy (ZEISS HD EVO 15).

Optical spectroscopy

Optical measurements were performed in an optical setup equipped with a 5-port integrating sphere with a diameter of 8 inch (Oriel, Model no. 70679NS), a monochromator (Oriel Model no: 74100), a thermal light source, and a UV enhanced silicon photodiode detector (Oriel, Model no. 70356). Light originating from the thermal light source is directed in a direction pointing from input port at one end toward the output port at the other end of the integrating sphere. The incoming light is chopped right before entering the integrating sphere with a chopper and collimated through a lens. The frequency of the chopper is chosen in a way that the frequency does not interfere with the surrounding electrical components. The frequency is regulated by a chopper controller. The interior of the integrating sphere is coated with a diffusive layer to further minimize unwanted reflection. The incoming signal from silicon photodetector is read by a lock-in which is then collected in the computer.

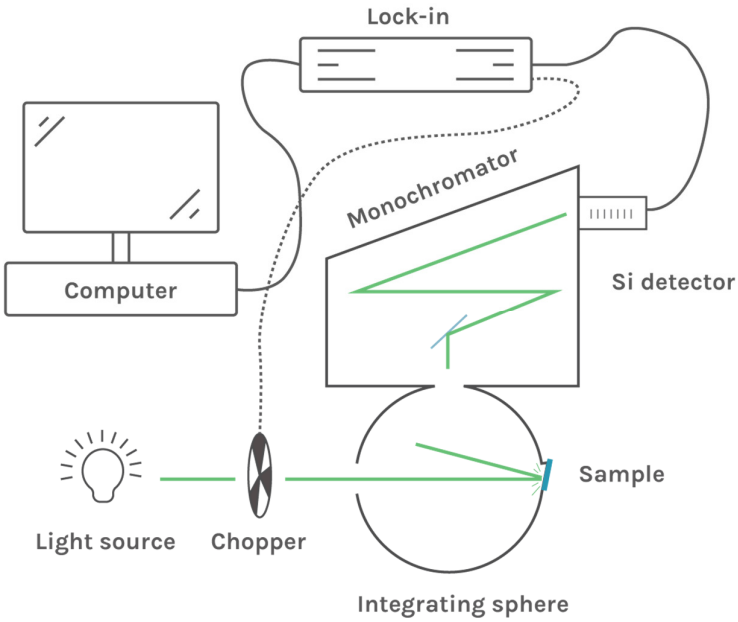

Figure A.1 Optical measurement setup at reflection mode.

In a reflection mode, the input port is left open to let the light pass though while the sample is put on the output port which is at angle of 8 degrees normal to the input port. The reflection is calculated via

$$R = \frac{R_{sample} - Dark}{\frac{Ref}{R_{BaSo_4}} - Dark} \tag{31}$$

In the above relation, $Dark$ represents the measurement while both the input and output port are left open. R_{ref} is the measurement result when the output port is closed with $BaSO_4$ coated material (calibration disc), the exact same material covering the integrating sphere. Meanwhile, R_{BaSO_4} is the reflectance from the calibration disc.

In the transmission mode, the sample is mounted on the input port while the calibration disc id placed on the output port. The measured transmission can be calculated via

$$R = \frac{T_{sample}}{Ref} \tag{32}$$

External Quantum Efficiency

The measurement of external quantum efficiency is carried out in the similar optical setup as reflection measurement with a slight modification. In front the exit port of the monochromator, the sample is placed in such a way that light in infringing on it. Firstly, the photon flux is calculated using silicon photodetector. Photo-generated current from the device is then measured at each wavelength interval. To measure the current, the sample is probed and connected to current to voltage amplifier.

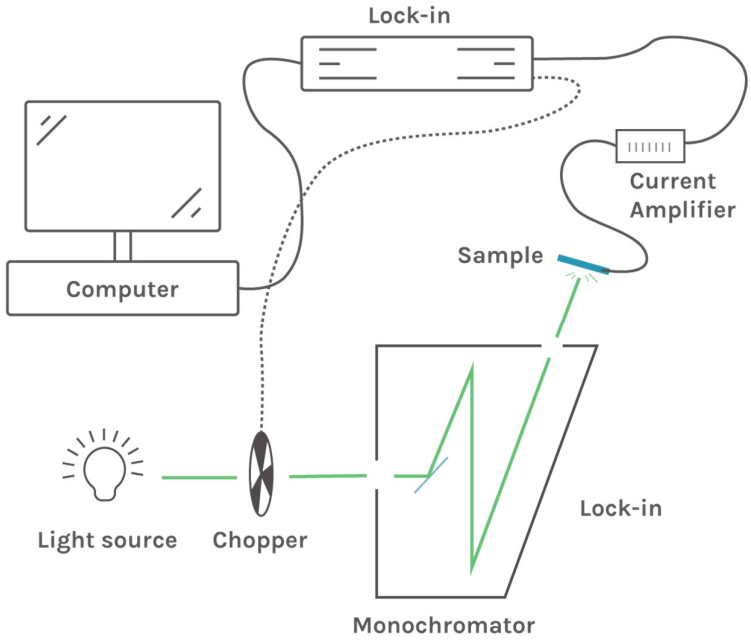

Figure A.2 External quantum efficiency measurement setup.

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