DEVELOPMENT OF A LARGE AREA GERMANIUM ON INSULATOR PLATFORM BY LIQUID PHASE EPITAXY

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ABSTRACT

DEVELOPMENT OF A LARGE AREA GERMANIUM ON INSULATOR PLATFORM BY LIQUID PHASE EPITAXY

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Germanium is a group IV element compatible with CMOS (Complementary metal oxide semiconductor) fabrication technology and advantageous over silicon by having smaller band gap and higher carrier mobility, which provide infrared photodetectors and high-speed transistors respectively. In addition, by having direct band gap, strained-Ge enables fabrication of infrared lasers. Finally, thanks to lattice-matching, Ge layers on Si can also be used as virtual substrates for the growth of III-V compounds on Si. In order to enable these technological developments, single crystalline Ge (c-Ge) needs to be grown on a low cost CMOS material, preferably Si. Within this scope, Ge films were grown on SiO_2 layers using liquid phase epitaxy enabled by crystalline Si (c-Si) seed window and rapid melting method. Effects of insulator, Ge film and capping layer thicknesses, temperature and cooling rate were probed by electron backscatter diffraction (EBSD) and Raman measurements. We demonstrated that while insulator thickness decreases the crystal quality, Ge film and capping layer thicknesses typically have a positive effect on crystal structure. Additionally, we observed that there is an optimum temperature around the melting point of Ge. Finally, we showed that lower cooling rates contributes to single crystal formation. The results of this research can offer a material platform for fabrication of infrared photodetectors, high-speed transistors and infrared lasers as well as low-cost high-efficiency solar cells providing economic and industrial benefits for photovoltaics.

Keywords: liquid-phase epitaxy, rapid melting growth, germanium, germanium-on-insulator

ÖZ

SIVI FAZ EPİTAKSİ İLE YALITKAN ÜZERİNE GENİŞ ALAN GERMANYUM PLATFORMU GELİŞTİRİLMESİ

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Germanyum bir grup IV elementi olup CMOS (tümleşik metal oksit yarıiletken) üretim teknolojisi ile uyumludur ve silisyuma göre daha küçük bant aralığı ile daha yüksek yük taşıyıcı mobilitesine sahip olduğundan kızılötesi detektör ve yüksek-hızlı transistor üretimini sağlar. Buna ek olarak, gerinimli Ge direk bant aralığına sahip olması sayesinde kızılötesi lazer üretimine olanak sağlar. Son olarak, örgü aralığı uyuştuğundan, Si üzerinde Ge tabakası III-V bileşiklerinin silisyum üzerinde büyütülmesi için alttaş olarak kullanılabilir. Germanyumun sunduğu bu avantajlardan faydalanabilmek için tek kristal germanyumun (k-Ge) silisyum gibi düşük maliyetli bir CMOS malzemesi üzerine büyütülebilmesi gerekmektedir. Bu kapsamda, SiO_2 yalıtkan tabakaları üzerine, kristal silisyum (k-Si) tohum ve hızlı eritme metodu ile desteklenmiş sıvı faz epitaksi yöntemi kullanılarak Ge filmleri büyütülmüştür. Elektron geri saçılım kırılma (EBSD) ve Raman ölçüm yöntemleri ile yalıtkan, Ge film ve kaplama tabakası kalınlıkları ile tavlama sıcaklığı ve soğutma hızı etkileri incelenmiştir. Yalıtkan tabaka kalınlığının kristal kalitesini düşürdüğünü, Ge film ve kaplama tabakaları kalınlıklarının kristal yapısında olumlu etki yaptığını gösterdik. Bunun yanısıra, Ge erime sıcaklığı civarında bir optimum tavlama sıcaklığı olduğunu gözlemledik. Son olarak, düşük soğutma hızlarının tek kristal yapı oluşumunu desteklediğini gösterdik. Bu araştırmanın sonuçlarının kızılötesi fotodetektörler,

yüksek-hızlı transistörler, kızılötesi lazerler ve düşük maliyetli yüksek kalitede güneş gözeleri için malzeme platformu sunarak fotovoltaik alanına ekonomik ve endüstriyel anlamda katkı sağlaması öngörülmektedir.

Anahtar kelimeler: sıvı-faz epitaksi, hızlı ısıl tavlama, germanyum, yalıtkan üzerinde germanyum

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NOMENCLATURE

GeOI	Germanium-on-insulator
Ge	Germanium
Si	Silicon
IC	Integrated circuit
FET	Field-effect transistor
CMOS	Complimentary metal-oxide semiconductor
I_{on}	Saturation drive current
GaAs	Gallium-arsenide
PVD	Physical vapor deposition
CVD	Chemical vapor deposition
TDD	Threading dislocation density
MBE	Molecular beam epitaxy
SiGe	Silicon-germanium
RMG	Rapid-melting growth
UHV	Ultra-high vacuum
RHEED	Reflected high-energy electron diffraction
LEED	Low energy electron diffraction
AES	Auger electron spectroscopy
MBMS	Modulated beam mass spectrometry
LPE	Liquid-phase epitaxy
RTA	Rapid-thermal annealing
TEM	Transmission electron microscopy
SK	Stranski-Krastanov
DC	Direct current
AC	Alternating current
RF	Radio frequency
UV	Ultra-violet
PR	Photoresist
RPM	Round per minute

SEM	Scanning electron microscopy
EBSD	Electron back scattering diffraction
CCD	Charge-coupled device
CW	Continuous laser
IPA	Isopropyl alcohol
BOE	Buffered oxide etch
FWHM	Full-width half-maximum

CHAPTER 1

INTRODUCTION

1.1. Motivation for germanium on insulator (GeOI) platform

Germanium (Ge) was used for the first transistor built in Bell Laboratories, in 1947, and since then played a crucial role in the development of semiconductor electronics. But due to the need of stable insulators it soon gave way to silicon industry, which had a great success owing to scalability and integration of microelectronics. Until 2005, silicon integrated circuits (ICs) had rapidly developed following Moore's law, which states that roughly in every eighteen months the number of transistors in an integrated circuit doubles [1].

Over the last decades, due to further scaling issues in integrated silicon technology, the demand for new channeling materials in field-effect-transistors (FETs) with high carrier mobility has increased. In this regard, germanium regained interest as an alternative to solve performance challenges in electronics-photonics integrated devices. Not only is it compatible with complimentary metal-oxide semiconductor (CMOS) techniques but also it precedes silicon in some areas. Ge offers higher carrier mobility, which leads to the increase in saturation drive current (I_{on}) in FET devices [2-4]. With its higher optical absorption in 1.3–1.55 µm wavelength range it provides near-infrared photodetectors in Si photonics [5-7]. Also in its strained form it acts as a direct band-gap material and can be used in the fabrication of infrared lasers [8] [9]. It is also considered as a virtual substrate for growing III-V materials such as GaAs for multi-junction solar cells [10].

Having such outstanding properties as a promising material for Si-CMOS technology, germanium has brought about the challenge of its integration on silicon substrates. The lattice mismatch of approximately 4% between germanium and silicon allows growing a critical thickness of only 2-3nm pure Ge crystal, above which many dislocations form causing recombination of electron-hole pairs and reducing the electrical performance dramatically [11].

In order to overcome the negative outcomes of Ge epitaxy on Si, many methods have been proposed. In the following sections the most outstanding methods will be explained and compared in terms of advantages/disadvantages briefly.

1.2. Epitaxial growth of germanium on silicon: Methods

There are two broad types of deposition techniques for growing semiconductors epitaxially, namely physical vapor deposition (PVD) and chemical vapor deposition (CVD). In PVD, the semiconductor to be grown, referred as the target, is in the elemental form and evaporated by a high energy source such as electron or ion beams in a high-vacuum chamber. The evaporated atoms or clusters then travel to the substrate conditions to grow thin films. CVD, on the other hand is chemical and the semiconductors are in the form of precursor gases flowing over hot substrates. Chemical reactions occur on these hot surfaces and as thin films grow over the surfaces some by-product gases also form and are exhausted out of the chamber.

Epitaxial growth of germanium on silicon is constrained by the lattice mismatch between the two (lattice constant of Si is 0.543nm whereas that of Ge is 0.566nm.) since above the critical film thickness (~2nm) threading dislocation density (TDD) highly increases (Fig. 1.1) [12]. In order to reduce the dislocations and obtain a defect free crystal many epitaxial growth methods have been studied. Molecular beam epitaxy (MBE) was the first method used for obtaining pure germanium films with good quality in the 1970s [13]. Due to the low yield that prevents mass production, however, MBE gave its way to CVD techniques readily having been used for silicon

production since 1960s. SiGe buffer layers are also investigated for matching the lattice constant and reducing the dislocations. Besides direct epitaxy, an alternative way to grow germanium on dielectrics, namely rapid melting growth (RMG) was proposed by Liu [14]. In the following these methods will be discussed in detail.

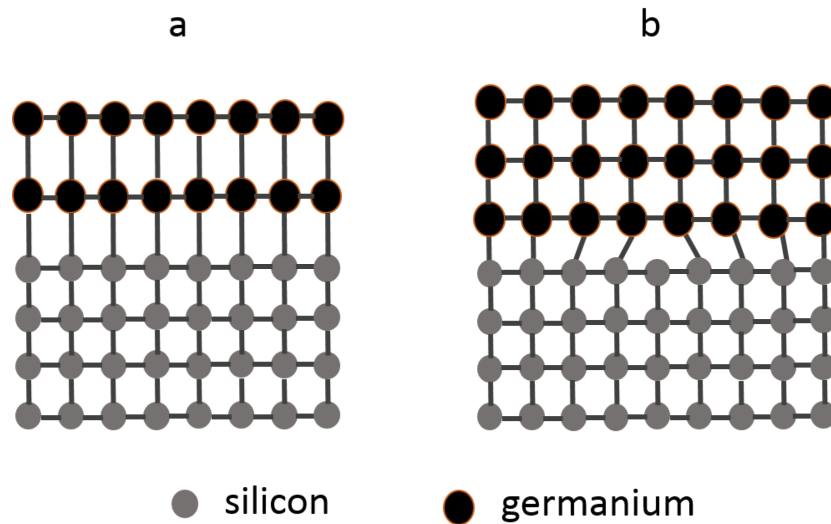


Figure 1.1. (a) strained growth of germanium on silicon. (b) misfit dislocation caused by larger germanium thickness.

MBE is a type of PVD method in which atoms or molecules are evaporated from a solid source of material and deposited on a heated substrate in a high vacuum chamber. The schematics of an MBE chamber is shown in Figure 1.2. There is a substrate with holder on the top which can be heated at a controlled temperature for providing source atoms with sufficient thermal energy to bond to lattice sites, and beneath there are effusion cells that contain pure sources (targets) of the material to be deposited. The effusion cells contain crucibles with the source material in them and the source is heated either by a filament or an electron beam. There are shutters on effusion cells to control the deposition. Ultra-high vacuum (UHV) (~10^{-10} Torr) in the chamber minimizes contamination and also provides atomic/molecular beams with nearly collision-free mean paths. Also for monitoring growth, reflected high-energy electron

diffraction (RHEED), low energy electron diffraction (LEED), auger electron spectroscopy (AES), modulated beam mass spectrometry (MBMS) methods can be used in the chamber [15] [16].

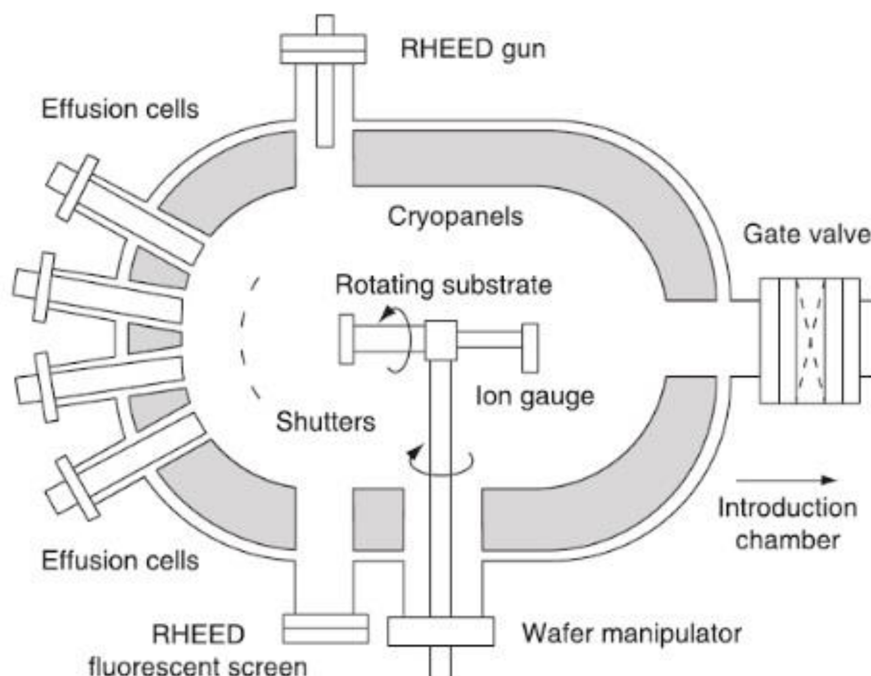


Figure 1.2. Schematics of MBE system [16].

One of the advantages of MBE in depositing semiconductor films is the precise control of thickness due to very slow rate (~Å/sec) and along with that good surface morphology. Also, ultra-high vacuum environment provides clean films with high crystal quality. It can be done at low temperatures and is safer than CVD methods in terms of byproducts. However, it is not suitable for growing thicker films ~100s of nanometers since it is very slow and costly to maintain [17].

CVD is another common method in the deposition of good quality semiconductor films. In CVD, the source is in the form of precursor gases that flow over heated substrates. As seen in Figure 1.3 the film production occurs by the chemical reactions

that take place over these heated surfaces of substrates and the byproducts and unreacted precursors in the gaseous form are exhausted out safely. It can be done in wide temperature and pressure ranges (200-1800ºC, tens of Torrs to atmospheric pressures) [18] [19].

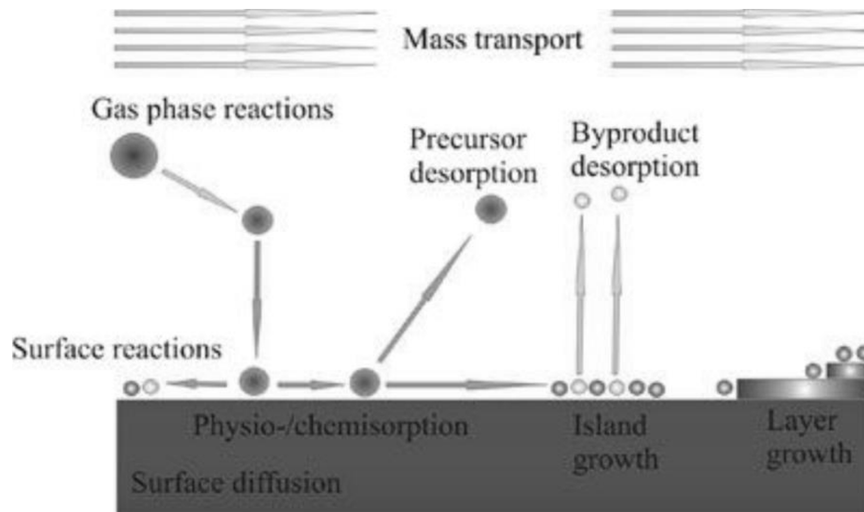


Figure 1.3. CVD process principle [17].

The main advantage of CVD is it allows mass production due to its high growth rate. Since it is a chemical method the deposited film can cover all the surfaces; i.e. it is highly conformal unlike physical methods. It does not have much complexity as MBE and such low pressures are not needed. On the other hand, there are disadvantages such as hazardous byproducts like CO, H_2, HF, etc., toxic precursors and high temperatures which lead to thermal stress in the films.

Silicon-germanium (SiGe) heterostructures have gained importance in the fabrication of heterojunction bipolar transistors due to increased carrier mobility and lower power consumption [20]. Although the lattice mismatch between silicon and germanium is relatively large (4.2%), a good heterojunction between Si and Ge can be obtained with low (30%) content of germanium and low film thickness (~15nm) [21]. Different types

of heteroepitaxy structures are shown in Figure 1.4. Below the critical thickness, the SiGe layer will compensate the lattice mismatch with a vertical tensile strain, whereas if the film gets thicker misfit dislocations form at the interface inevitably.

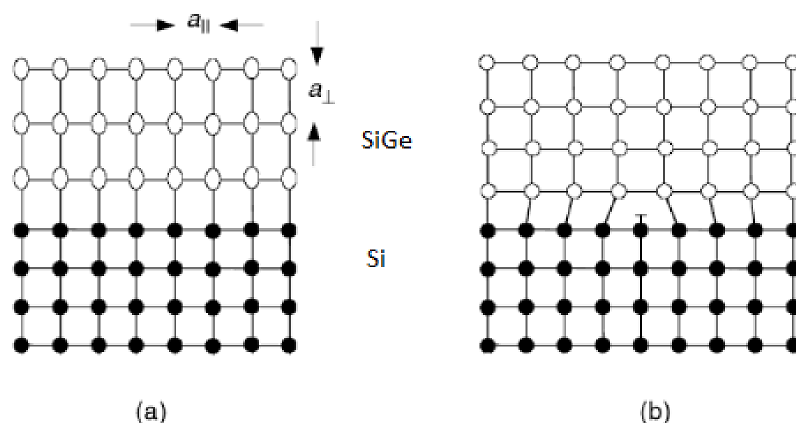


Figure 1.4. (a) pseudomorphic growth and (b) mismatch dislocation in SiGe heteroepitaxial structures [22].

For growing pure germanium crystals on silicon, graded SiGe buffer layers can be used as virtual substrates. In order to obtain fully relaxed SiGe layer with increasing Ge content, the buffer layer should be thick, reaching micrometer order. This will create some drawbacks such as higher cost due to material usage and increased surface roughness that causes difficulties in integration.

In wafer-bonding method, two mirror-polished wafers of same/different materials are brought together without any external force in room temperature. Bonding occurs between two materials through Van der Waals force, which is relatively weak compared to ionic or metallic forces, thus after the bonding process wafers are heat-treated to increase the bond strength. Furthermore, Van der Waals is a rather short-range force so that hydrogen bonds are usually introduced through oxidizing the surface to increase the bonding range. Upon heat treatment, the hydrogen bonds break and leave stronger covalent bonds instead, at temperatures around 800-1200°C. For

lowering the temperatures plasma treatment is an effective way since it activates the surface. Since many applications require thin layers, the transfered wafer generally needs to be thinned. The best technique up to now for thinning is known as smart-cut, which is based on hydrogen implantation before bonding process [23]. The implanted hydrogen layer goes deep in the material and forms a cracking site upon heat treatment. The upper wafer is then splitted from the handling wafer and a thin layer of desired material remains and it is polished to decrease surface roughness.

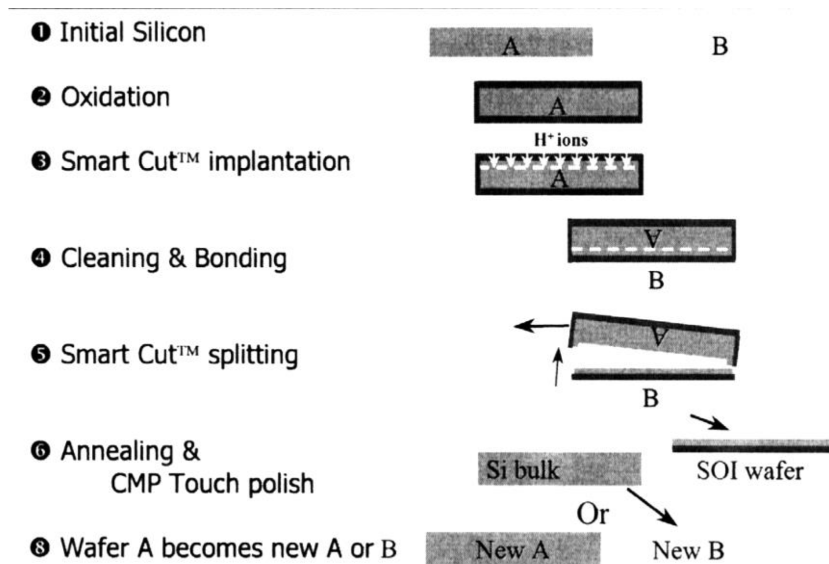


Figure 1.5. Wafer bonding process with Smart-cut technology [24].

Wafer bonding method is also used for obtaining germanium-on-insulator (GeOI) and SiGe structures on silicon wafers. GeOI substrates are formed by the basic steps used in smart-cut technique; (1) cleave layer is formed in germanium wafer by hydrogen implantation, (2) silicon handle wafer is oxidized for bonding, (3) Ge and Si wafers are bonded by plasma activation, (4) wafers are separated from the cleave plane, and (5) additional processes like polishing are performed to reduce surface roughness and other damages.

Obtaining Ge films on silicon with a buried oxide layer using wafer bonding technique has advantages over some methods such as using SiGe buffer layer in terms of lower dislocation density and lower budget. However, it also brings about several issues concerning; macroscopic defect densities caused by temperature treatment and mechanical stress, surface contamination in bonding step, and high surface roughness (~20nm) preventing the fabrication of thin layers [25].

Liquid-phase epitaxy (LPE) is a technique invented in 1963 for growing thin films of compounds of II to VI elements to form heterostructures for electronic and photonic devices like GaAs/GaAlAs and InP/In GaAs [26]. It is mainly based on epitaxy from a metallic solution on a crystal substrate at temperatures about 400-1200°C. The solution is heated up to liquid phase, brought in contact with the solid substrate and system is cooled down below the liquid-solid equilibrium, which is the driving force in the epitaxial growth.

There are three cooling profiles used commonly (Fig. 1.6). In step-cooling, the solution is supersaturated at a temperature T_s above melting point, cooled down to the growth temperature T_a with constant ΔT and kept constant at this temperature during growth. In equilibrium-cooling, growth starts at a supersaturation temperature T_s and system is cooled down with a constant rate α. Supercooling is a combination of step-cooling and equilibrium cooling, in which the solution is cooled down to T_a with constant ΔT and then cooled down further linearly [27].

LPE makes it possible to grow high-purity crystalline structures owing to its basis of being a near-equilibrium process, which is one of its most unique properties. The control of liquid-solid phase diagram makes it possible to minimize the defects. Also thin layers in the range of a few nanometers can be produced and the growth rates can be high to allow much thicker films. LPE is advantageous over other epitaxy methods in many ways. Compared to vapor phase methods it is less hazardous, because the byproducts are safer and since it does not require air conditioning or gas supply systems it is less expensive. Furthermore, it allows doping profiles of either n-type or p-type during growth.

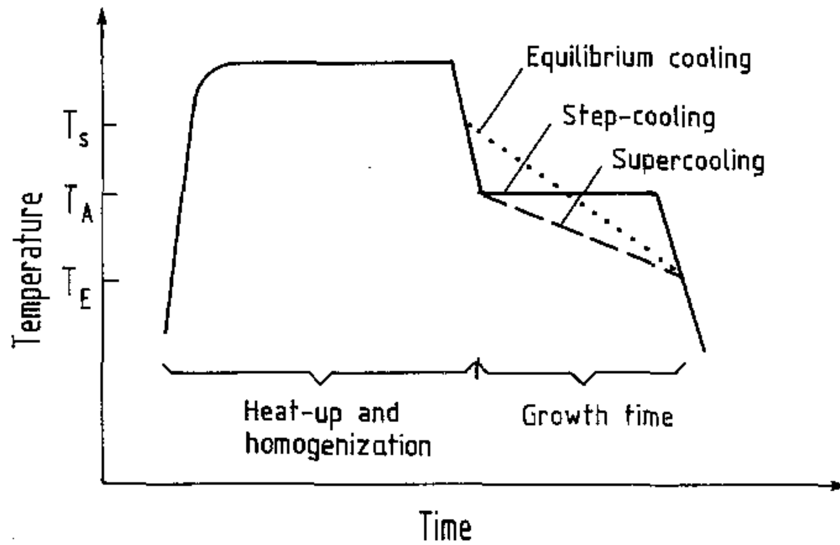


Figure 1.6. Main cooling profiles used in LPE [27].

Along with these advantages, LPE also has some weaknesses to be considered. The most apparent one is the difficulty in controlling the growth rate, which prevents accurate sized very thin layers to be produced. The growth rate can be lowered by decreasing saturation temperature, however it will cost the decrease in interface sharpness [28].

1.3. Organization of this dissertation

Chapter 1 is a brief introduction for the motivation of growing germanium epitaxially on silicon. Along with the advantages that germanium offers for CMOS technology, the common methods having been used so far are explained in order to provide a preliminary for the next chapter.

In Chapter 2 the motivation behind choosing liquid-phase epitaxy (LPE) for the growth of Ge films on Si is given. For this purpose, the rapid-melting growth (RMG) method proposed in 2004 by Liu et. al. is explained in mechanism. Further, studies concerning

the Ge growth using this method were mentioned and how they contributed to obtaining high quality crystal films in terms of various factors are discussed.

In Chapter 3 the fabrication techniques and characterization methods used in this study are explained conceptually. For the fabrication three techniques; reactive magnetron sputtering, photolithography and chemical etching are mentioned. For the characterization part SEM, EBSD and Raman spectroscopy are defined.

Chapter 4 covers the fabrication process and results of this study. Fabrication steps are explained in detail with optimized parameters. Results are given in terms of SEM, EBSD and Raman measurements. Discussions are made in terms of the effects of insulator, germanium, capping layer thicknesses and temperature and cooling rates.

Chapter 5 is the conclusion part covering the results of this study and also further possible studies are mentioned.

1.4. Contributions

The fabrication part of this study was carried on in GÜNAM clean rooms. Masks were prepared and the research was initiated by Wisnu Hadibrata. SEM and EBSD measurements were conducted by Sedat Canlı and Seçkin Öztürk in METU Central Laboratory. Raman measurements were conducted by Elif Ünsal in METU Central Laboratory.

CHAPTER 2

LIQUID-PHASE EPITAXY FOR GeOI PLATFORM

2.1. Motivation

The outstanding properties and advantages of germanium in CMOS technology and the importance of integrating it into electronic and photonic devices were mentioned in Chapter 1. Besides, the challenges related to its epitaxy on silicon and the common methods proposed were discussed separately. The main challenge of growing germanium crystal over silicon is the formation of threading dislocations due to the lattice mismatch between silicon and germanium. The solution requires using a method for both eliminating the dislocation formation and also exceeding the critical thickness to grow 100s of nm films.

Among the most common methods, SiGe buffer layers have been used effectively to form pure germanium layers directly on Si [29]. However, in order to reduce the threading dislocations down to ~10^7 cm^{-2}, post annealing process at high temperature (>800^oC) is needed, which is harmful to other components in the CMOS process [30]. As mentioned in Chapter 1, liquid-phase epitaxy method is advantageous in the sense that it provides high crystallinity and high purity in grown films. It also allows obtaining thicker films without the need of buffer layers. Recently, a method called rapid-melting-growth (RMG) has been proposed by Liu et. al. that uses the advantages of liquid-phase epitaxy process [14].

Rapid-melting-growth method is based on necking technique as in Czochralski growth of crystals from melt to eliminate the defects during the growth [31]. Seed and microcrucible regions are defined on insulator in which germanium is deposited as material form as in Figure 2.1. Based on liquid-phase epitaxy, germanium is heated over its melting point (938°C) and cooled down to initiate crystal growth. Since melting point of Si is much higher (1414°C), cooling starts from the seed region where Ge and Si are in contact and the film orientation follows that of silicon. The necking mechanism allows terminating the dislocations forming at an angle of 54.7^{o} at the upper edge of Ge, thus high-quality single-crystal structure can be obtained on insulator [32] [33].

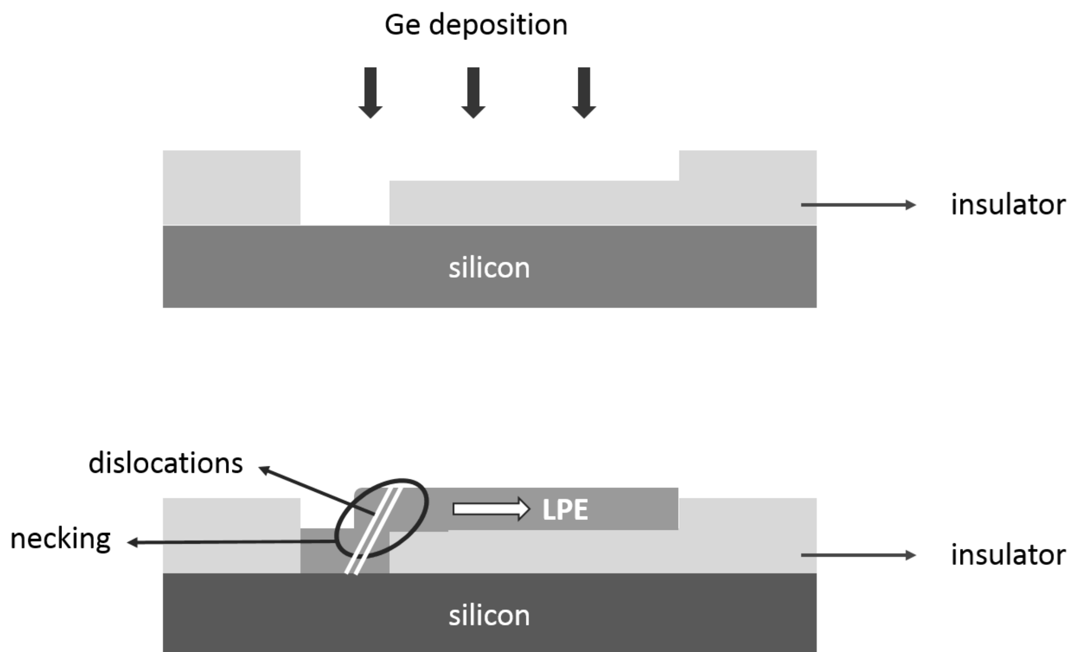


Figure 2.1. Cross-sectional schematics of rapid-melting growth method. Dislocations terminate at the upper edge of germanium crystal with necking mechanism.

Consequently, RMG method provides the fabrication of GeOI structures especially for high performance field-effect transistors using a relatively simple process. Besides being CMOS compatible, the cost of using germanium is highly reduced since it

requires films with small areas. Due to confining the dislocations into the seed window and thus obtaining high-quality crystal structure, carrier mobility increases significantly. In order to get full benefit from this method important factors such as crucible size, insulator, annealing temperature, etc. should be extensively studied. In the following section a detailed survey of recent works taking these variables into consideration will be given.

2.2. Literature Survey for GeOI platform with Rapid-Melting Growth

Rapid-melting growth method proposed by Liu et. al. (2004) uses the advantages of both necking mechanism and liquid-phase epitaxy to provide the fabrication of low-defect crystal germanium on insulator. The method is much simpler than zone-melting method used for fabrication of Si-on-insulators in the aspect that RMG requires only rapid-thermal annealing (RTA) furnace to heat up the whole sample [34]. In their earliest studies in RMG, Liu et. al. observed the lateral crystal growth of Ge and the defect mechanism [14] [35]. In these works transmission electron microscopy (TEM) results showed that the threading dislocations formed along <110> directions on <111> planes due to the diamond structures of silicon and germanium. These dislocations were observed to make an angle of 54.7° with (100) plane of silicon and terminate at the top surface of Ge film as expected [32]. The defect density in the seed region was high due to the lattice mismatch between Si and Ge, whereas far from the seeding region no dislocations were found.

One of the challenges in obtaining defect-free germanium crystal with RMG is Stranski-Krastanov (SK) growth [36] [37]. This type of growth mode occurs due to random nucleation of Ge atoms in the cooling phase of annealing and causes island formations (agglomerations) to reduce the surface energy. Moreover, the grown film will be polycrystalline. In order to suppress these island formations lateral crystal growth rate should be higher than random nucleation rate. Liu et. al. proposed that there is a temperature range below melting point of Ge that lateral growth rate exceeds random nucleation based on thermodynamical calculations [35]. Also it was stated the

crystal growth and nucleation rates increase with undercooling down to certain temperatures then decrease due to slow motion of atoms. Thus, when the Ge is heated over its melting point and cooled down, close to the melting point growth rate can exceed nucleation. In their study Ge is heated up to 940°C over its melting point with a ramp up rate of 100°C/s and held at the same temperature for 1s before cooled down with the same rate of heating. No agglommerations were observed and the crystal quality was high showing that random nucleations were suppressed. In 2006, Balakumar et. al. also studied the concept of Stranski-Krastanov growth and they compared the effect of different temperatures and soaking times on agglomeration [37]. They annealed the samples at three different temperatures 940°C (above melting point), 932°C and 925°C, and tried different soaking times of 2, 3, 5 and 10s. Ge balling up was observed the most in annealings above the melting point. Below melting point the agglomerations decreased and at the lowest temperature 925°C they obtained a continuous crystal. Soaking time was also found to affect Stranski-Krastanov growth. When the soaking time increased segregation is observed in Ge crystal (Fig. 2.2).

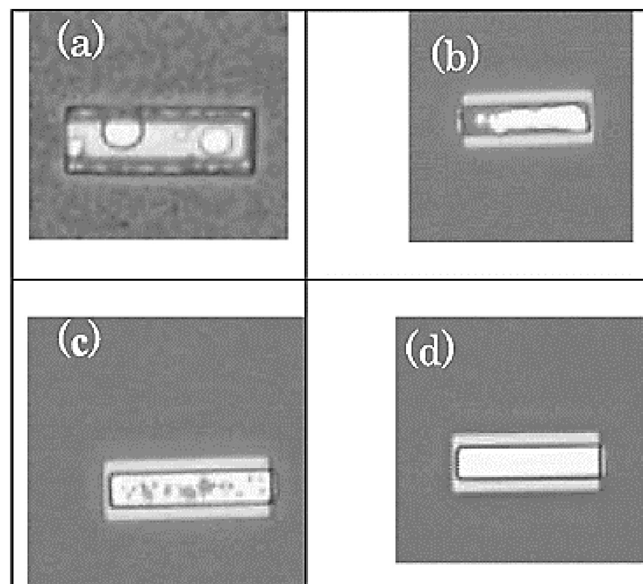


Figure 2.2. Optical micrograph of 10 μm pad (a) 940°C at 2 s, (b) 932°C at 3 s, (c) 925°C at 10 s, (d) 925°C at 5 s [37].

Choosing the right materials is an important factor in RMG, especially for the insulator layer. Growth mechanisms of crystals are highly affected by the material that the crystal is grown upon since the interface energy between the insulator and the crystal determines the shape and orientation of the crystal. As the interface energy rises, the crystal tends to form more spherical shapes which have lower area/volume ratio for reducing the energy. In the first studies of RMG of GeOI oxide and nitride layers were used, however, no observation on the effect of insulator were done [14] [35] [37]. In 2009, Hashimoto conducted a study on the effect of insulator and compared three different layers; SiO_2, HfO_2 and La_2O_3 in terms of interface energy with liquid Ge [38]. The insulators had thicknesses of 60nm, 50nm and 17nm, respectively. They observed that SiO_2 and HfO_2 showed no significant difference in affecting agglomeration, whereas La_2O_3 suppressed the polycrystal grains with its lower interface energy value, which also provides better bond strength between the two materials.

There are two proposed mechanisms behind the lateral growth from the seed in RMG method. First mechanism is the increase in the melting point in seed area due to silicon-germanium interface. Since the melting point of silicon (1414°C) is much higher than that of germanium (938°C), when the whole GeOI on silicon system is annealed, liquid in the seed region will move to solid phase first due to Si-Ge mixing. The second mechanism of lateral growth is the temperature gradient between liquid and solid phases in the melt. Si-Ge mixing in the seed and stripe regions can be determined by Raman spectroscopy, comparing the peak intensities of Ge-Ge (at ~300 cm^{-1}) and Si-Ge (~380 cm^{-1}) bonds. Recent studies involving Raman measurements for RMG of Ge indicate that above melting point Si-Ge mixing increases and it provides an increase in lateral growth rate [39-42]. Furthermore, in 2010, Toko et. al. conducted a study by using quartz substrates as insulator layer [43]. They studied three different variations with samples having poly-Si, poly-Ge seeds and also samples with no seed. The samples with poly seeds eventually formed single crystal structure, whereas the samples with no seed turned to be polycrystalline. This result indicated the importance of seed region for lateral growth. In addition to this perspective of Si-Ge mixing-triggered growth, Mizushima et. al. introduced a different approach [44]. They

proposed that while in the seed region Si diffusion into Ge liquid can initiate solidification, the Si fraction is lost in the far regions of the stripe. Thus in the regions where there is only liquid Ge, the latent heat of solidification is the key factor to explain growth phenomena. Since liquid Ge will tend to maintain the melting point, a thermal gradient will be formed in the liquid-solid interface (Fig. 2.3).

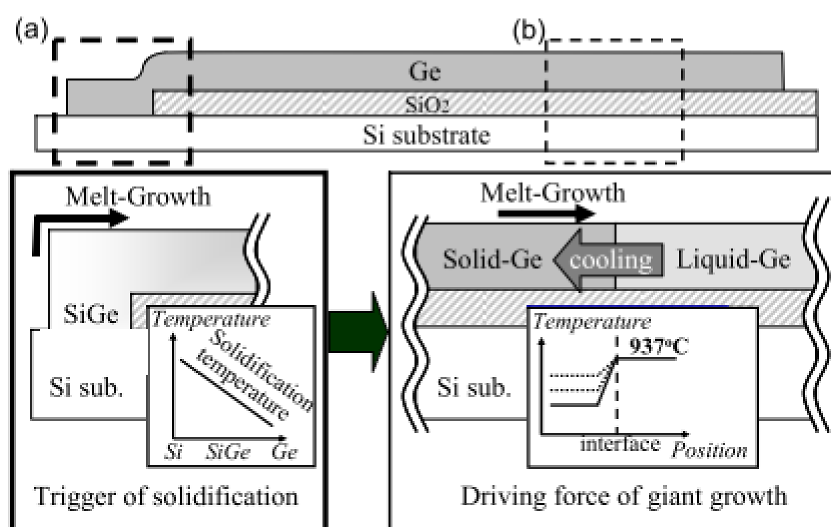


Figure 2.3. Model for SiGe mixing-triggered rapid melting growth in seeding area (a), and the region far from seeding area (b) [44].

Other studies related to Ge crystallization with RMG method include the effect of factors such as temperature and cooling rate on crystal quality, grain size and lattice rotation. Moreover, the tensile strain induced in the grown Ge films have been inspected via Raman measurements. Some of these studies will be mentioned in Chapter 4 related to the results of this study.

CHAPTER 3

EXPERIMENTAL TECHNIQUES USED IN THIS STUDY

3.1. Fabrication Methods

3.1.1. Reactive Magnetron Sputtering

Sputtering, in general, is a type of physical vapor deposition (PVD) technique which uses plasma environment for the deposition of desired material from a target. It provides film growth without the need of using hazardous gas mixtures or applying high temperatures as in the chemical deposition processes. Plasma is created on the target by applying voltage (DC or AC) and high speed particles (electrons and ions) are created in this environment. These accelerated particles collide with the surface and with momentum and energy transfer they eject the surface atoms/clusters. Then the ejected atoms/clusters use their gained energy for traveling to the substrate and form the desired film structure on the substrate (Fig. 3.1).

In magnetron sputtering there are magnets placed under the targets and they create a strong magnetic field used for trapping the unbound electrons in the plasma region. When the voltage is applied to the target electrons pile up on the surface and create an electric field. At the same time an inert gas (usually argon) is sent into the system with a predefined gas pressure, which collide with the traveling electrons, and upon these collisions heavy positive ions are created. This plasma is called glow discharge since light is emitted upon ion creation. As the electrons travel in the bound region of magnetic field, more and more collisions take place between the inert gas and electrons. Consequently, the efficiency of plasma creation is highly increased with the introduction of magnetron.

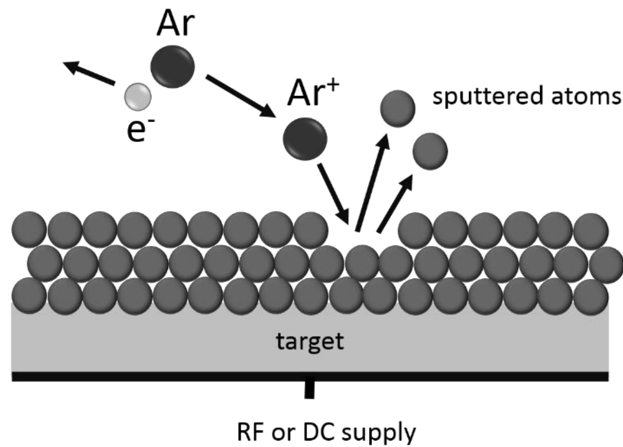


Figure 3.1. The basic scheme of sputtering process.

Two different voltage supplies can be used in sputtering according to the target material. DC voltage can be applied to the conducting targets due to enough electron mobility. However, for semiconductor or insulator targets it is not applicable since the voltage bias can cause breakdown of the material eventually. Thus for non-conducting materials RF power supplies are generally used. For the industrial and research purposes 13.56MHz is allocated as the commonly used frequency. Applying RF voltage to the target provides the heavy ions with sufficient energy for sputtering the atoms from the surface, and also electrons can travel fast enough and return to the surface which prevents charging. Using RF power supply instead of DC makes it possible to apply higher voltage difference and thus higher sputter and deposition rates.

Insulator layers can be deposited using RF supplies and stoichiometric insulator targets, however, the sputtering yield will be low compared to semiconductor targets. For the insulator layers, especially when thick layers of micron size are needed, sputtering with insulator targets is not preferred. For growing insulator films with higher sputter rates reactive sputtering can be used. In reactive sputtering, along with the desired metallic or semiconductor target a reactive gas is sent with the inert gas. The flow rate of the reactive gas is determined due to the desired stoichiometry of the film.

One drawback of reactive sputtering is the "poisoning" of the target which occurs when the reactive gas forms compound on the target faster than sputtering process. When this happens sputtering rate is highly reduced. According to the hysteresis curve provided by Westwood, upon increasing the reactive gas flow the deposition rate remains constant at a certain point where the sputtering rate equals to the compound formation on the target [45]. Beyond this point of poisoning deposition rate suddenly decreases due to the compound layer on the target and in order to reverse this phenomenon all of the compound layer should be removed by decreasing the reactive flow rate to a value lower than the poisoning point (Fig. 3.2). The poisoning of the target can be prevented by optimizing and monitoring the reactive gas flow.

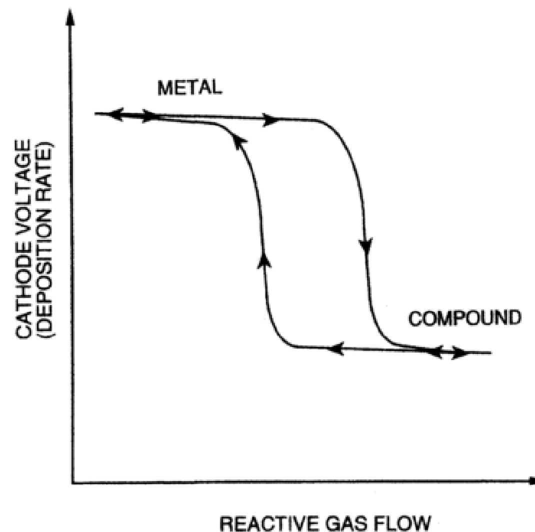


Figure 3.2. Hysteresis curve for reactive magnetron sputtering system [46].

The main parameters in reactive magnetron RF sputtering deposition are base pressure, RF power, gas flow and deposition gas pressure. Base pressure in the deposition chamber can reach down to ~10^{-7} Torr. High vacuum level provides less contamination from the walls of the chamber and longer mean free path values for sputtered species. High sputter yield can be achieved by increasing RF power, and also poisoning can be prevented at high voltages applied to the target. Gas flow of inert and reactive gases

can be adjusted and monitored separately, which allows maintaining a desired stoichiometry in grown films. Partial gas pressure during deposition is generally applied between 1-10 mTorr. Increasing the deposition pressure will create more ions and sputtered species, however it also increases scattering of atoms. Thus, for the best coverage, directionality and quality of the films the partial gas pressure should be optimized.

3.1.2. Photolithography

Lithography in IC fabrication is the patterning of a surface by transferring a shape from a predefined mask. In photolithography, UV light is used for transfering the patterns. A polymer that is sensitive to UV light, called photoresist (PR), is used for coating the surface where the pattern will be formed. Upon light exposure the structure of the polymer changes and becomes soluble in developer solution. For positive photoresist the exposed areas will be solved, whereas for negative photoresist they remain. After creating the pattern, the open areas can be etched or films can be deposited in them.

The sequence of the process steps are shown in Figure 3.3. The first step in photolithography is the covering of the desired surface with photoresist after cleaning the surface (b). Sample is placed in a spin coated and photoresist solution is dropped onto the surface and coated at a defined RPM for a defined time. In the prebake (soft-bake) step the sample is heated on a hot plate to evaporate the coating solvent and densify the polymer.

Second step is the exposure of photoresist to UV light (c). Sample is placed on a mask aligner system and the mask is aligned on the desired area of the surface. Different operating modes can be used for aligning; in contact mode mask touches the photoresist during exposure, in proximity mode there is a space between mask and sample causing poorer images, and in projection mode the is another optical system between mask and the sample for imaging.

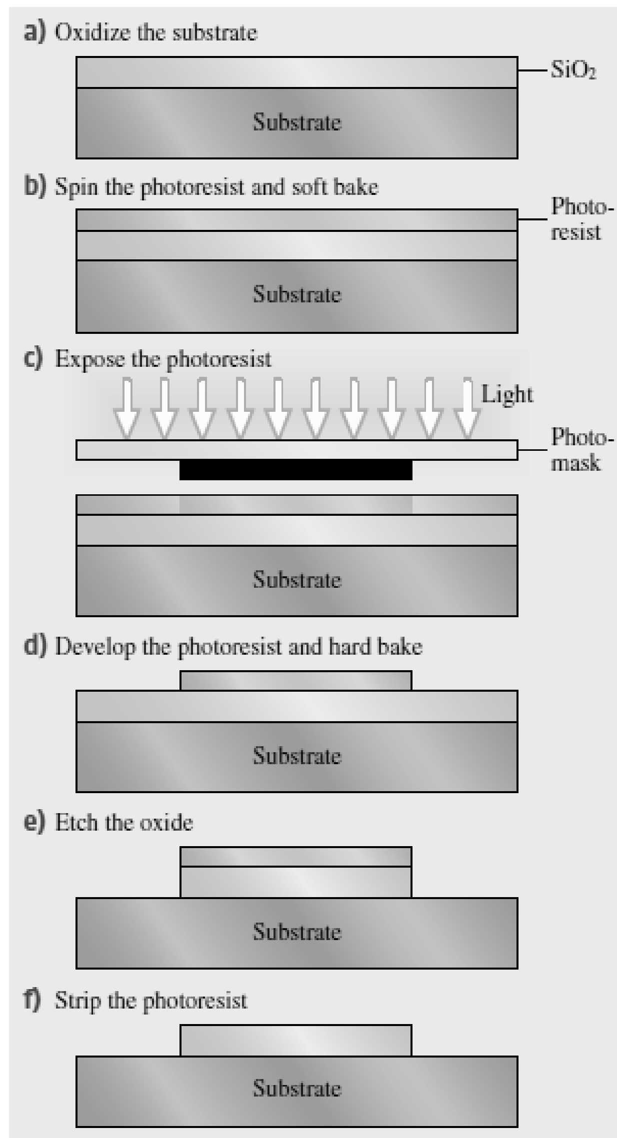


Figure 3.3. Schematic drawing of photolithography steps with a positive PR [47].

After the exposure step the sample is again heated on hot plate (postbake or hard bake) optionally and developed in a solution optimized for the photoresist type (d). As a last step photoresist can be heated further for chemical etching purposes (e) and can be removed with acetone (f).

3.1.3. Chemical Etching

Chemical etching is used to remove material by a chemical reaction and usually applied along with a lithography step to define the areas to be etched. Photoresist, insulator layers or other hard materials can be used as a protective mask to cover the rest of the sample that will remain. If the etching is selective, i.e. the etchant is specific to one material, process can be done without a protective layer. There are two types of etching profiles (Figure 3.4). For isotropic etch, the rate is equal in every direction of the material structure. On the other hand, in anisotropic etch the etch rate is higher in one direction than the others. Most chemical etching processes are isotropic. Within the scope of this study, etching of SiO_2, and germanium layers were performed.

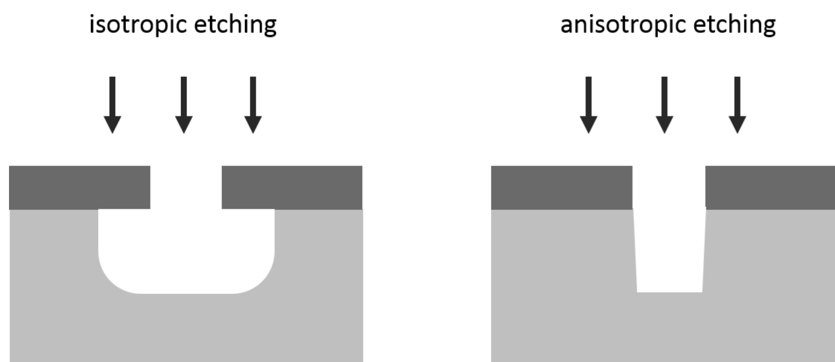
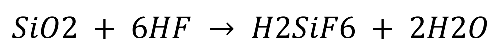


Fig. 3.4. Isotropic and anisotropic etching profiles.

Silicon-dioxide layers are mainly etched with hydrofluoric-acid (HF) based solutions. For pure HF, the overall reaction of etching is as follows [48];



$$SiO2 + 6HF \rightarrow H2SiF6 + 2H2O$$

Hydrofluoric-acid is commercially produced as its concentrated solution (49% by weight). It etches oxide very rapidly and also can strip photoresist layers, thus for sensitive processes that need slow etch rates its buffered solution is preferred. HF is buffered with NH_4F in order to keep pH constant and stabilize the etching rate. Different concentrations of NH_4F were studied for oxide etching and the etch rates were observed to have a maximum range around 10-15 w/o (weight per cent) of NH_4F (Fig.3.5) [49].

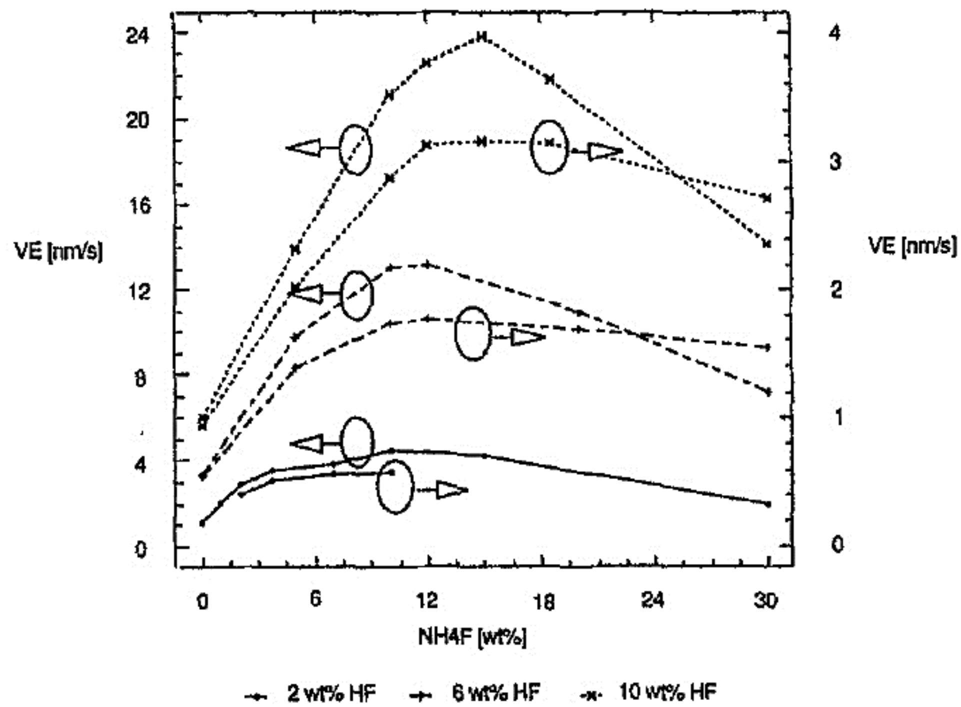


Figure 3.5. Etch rates (nm/s) vs. ammonium fluoride concentration (w/o) for thermal oxide (arrows indicate the right scale) and undensified oxide (arrows indicate the left scale) layers for different to HF concentrations [49].

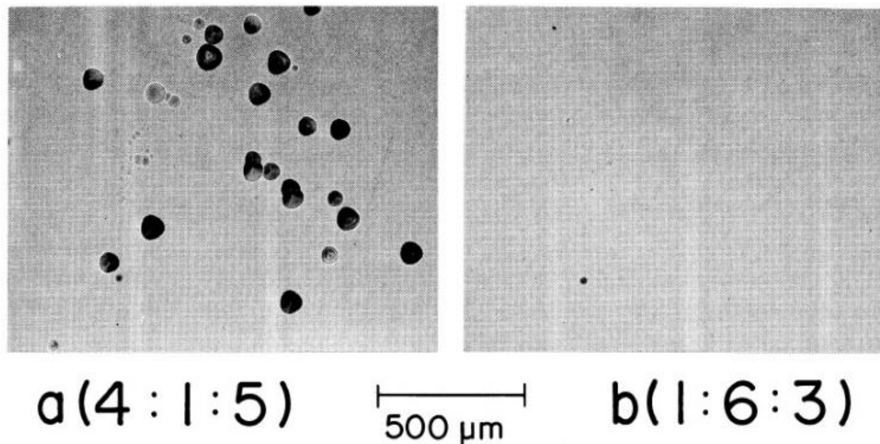


Figure 3. 6. Photographs of etched surfaces using H_3PO_4-H_2O_2-H_2O solution from regions a and b for 15 min [50].

Different solutions for etching germanium layers have been reported [51-53]. However, most of these contain HF, which also etches oxide and also photoresist if not buffered, and the etching rates are too high to be controlled. A solution of phosphoric acid (H_3PO_4), hydrogen peroxide (H_2O_2) and water (H_2O) was introduced for improving germanium etching process [50]. In this solution, H_2O_2 oxidizes the germanium surface and H_3PO_4 etches the oxide layer. H_2O_2 can be used alone for etching germanium but the etching will be too slow. In the study, the oxidation process with peroxide was observed to be slower than dissolving the oxide layer by the acid, so the reaction depends on the peroxide to acid concentration. For a low H_2O_2:H_3PO_4 ratio (1:4) etch pits were observed on the surface, whereas for a higher ratio of 6:1 the surface was much smoother (Fig. 3.6). Since peroxide to phosphoric acid is higher in the second case, surface is continuously covered with oxide and etched in a controlled way. This solution can be used for etching germanium layers with SiO_2 and photoresist masks.

3.2. Characterization Methods

3.2.1. Scanning Electron Microscopy (SEM)

Surfaces can be analyzed in nanometer scale by using scanning electron microscopy, in which electron beams are used for imaging instead of light. The high energy electrons interact with the sample surface and properties such as morphology, composition and crystal structure can be obtained with the collected signals. The electron-sample interactions are shown in Figure 3. 7. In scanning electron microscopy image of the surface is obtained by using the information from secondary and backscattered electrons.

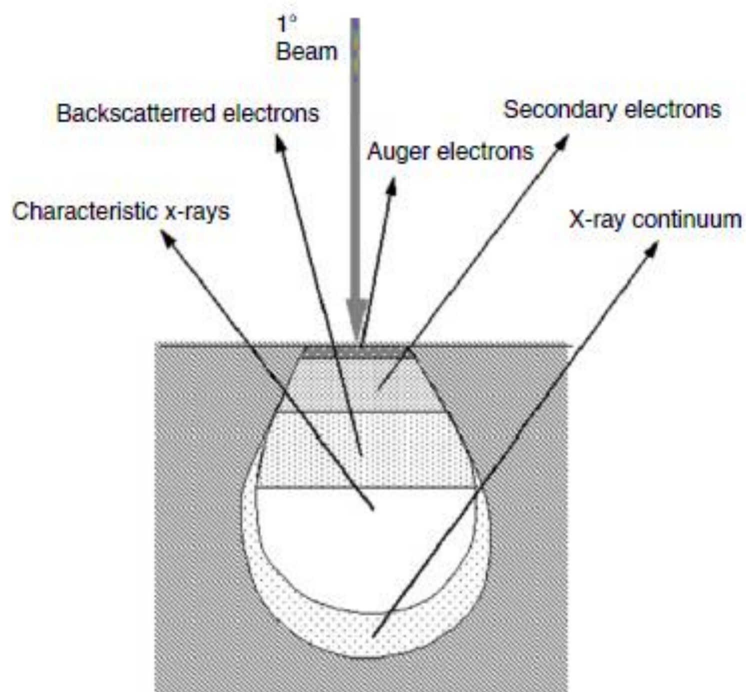


Fig 3.7. Signals generated by the electron beam-specimen interactions in SEM and the regions from which the signals can be detected [54].

Secondary electrons come from the inelastic collisions and scatterings of the incident electron with the sample and they have energies <50eV. They are collected from a region of a few nanometers from the surface and give information about the topography of the surface. Thus by secondary electrons surface texture and roughness can be visualized with high resolution, down to an order of 10nm. Tilting the detector will increase the topographical contrast since not all the secondary electrons will reach to the detector and this will cause shadow formation on the image [54].

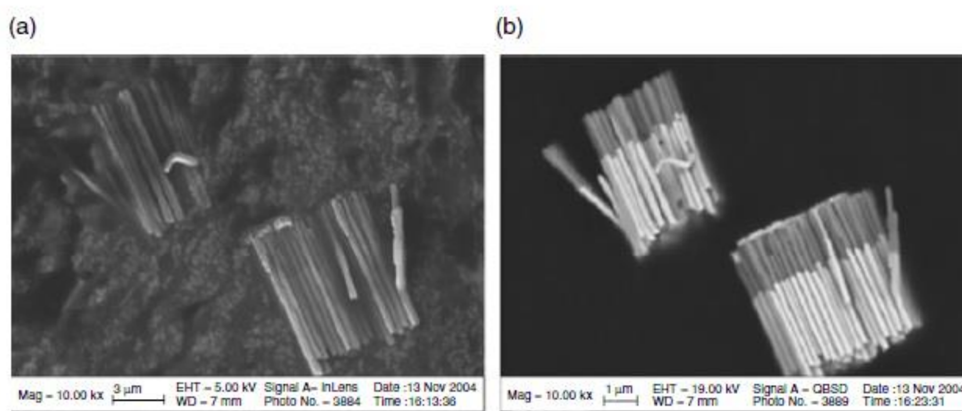


Figure 3.8. Ni/Au nanorods images formed by (a) secondary electron signal and (b) backscattering electron signal [54].

Backscattered electrons are obtained from single or multiple scatterings and elastic collisions between the incident electron beam and atoms of the surface. Since the energy loss is negligible they have energies greater than 50eV. They give information about composition of the sample as well as topography. Elements with higher atomic number will scatter the incoming electrons more so that the signal will be higher, resulting brighter regions on the image. A comparison of images taken with secondary electron signal and backscattering electron signal is depicted in Figure 3.8.

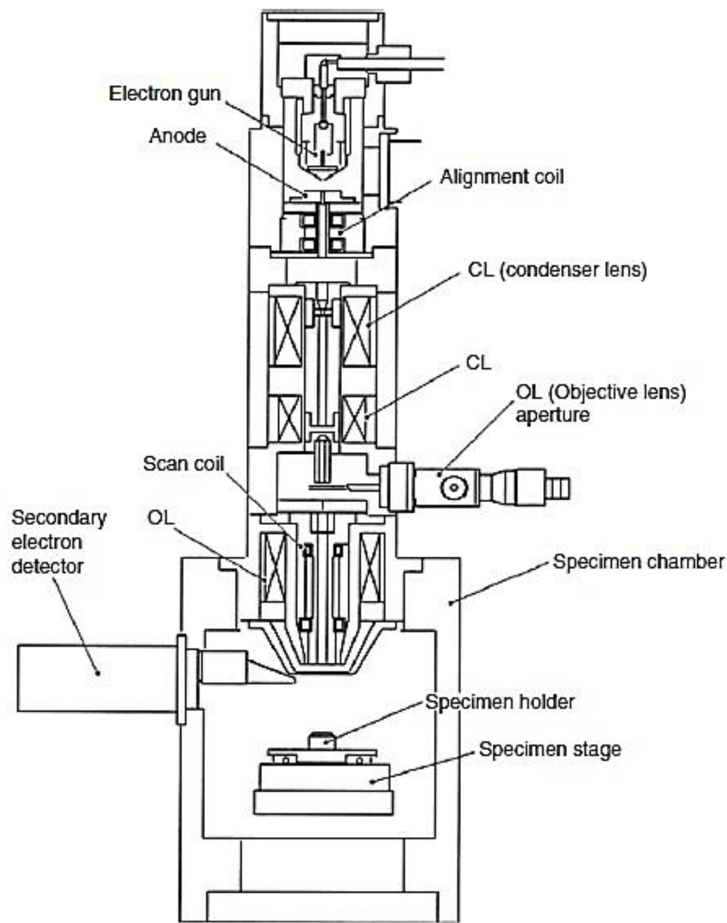


Figure 3.9. Schematic diagram of a scanning electron microscope [54].

Scanning electron microscope is mainly composed of an electron gun, condenser lenses, a scanning system, specimen chamber, vacuum system, and detector and display system (Fig.3.9). Electrons are generated by the electron guns either from a filament or crystal. They are accelerated within a magnetic field and sent through condenser lenses where the beam is focused down to 10^3 times of initial size. The beam goes through other apertures where the spot size is adjusted. Scanning of the sample is carried out by scanning coils which control the direction of electron beams. The collected signal is amplified and displayed as an image on a monitor [55].

3.2.2. Electron Back Scattering Diffraction (EBSD)

Electron back-scattering diffraction (EBSD) method is used for determining the crystallographic information of samples. The technique is carried out in SEM system with an EBSD detector. In order to get a proper signal the surface should be flat or polished. The electron beam is sent at a low angle ~20° to the sample and the backscattered electrons form constructive and destructive interference patterns on a fluorescent screen. The phosphor on the screen interacts with the electrons and light is emitted to a CCD camera. The patterns on the obtained image refers to the crystallographic planes and carries information of the lattice structure.

The electron beam interacts with the sample according to Bragg's law (Fig. 3.10);

$$n\lambda = 2d \sin\theta$$

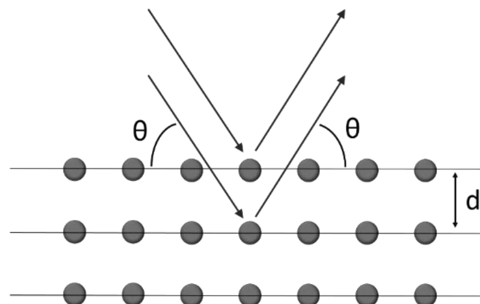


Figure 3.10. Diffraction of electrons in a crystal lattice according to Bragg's law.

Due to different diffraction angles from different planes of the crystal, bands corresponding to these planes will appear on the image, which are called Kikuchi bands (Fig. 3.11). The width of the bands is related to lattice spacing and the angles between the bands correspond to the angles between the crystal planes. These Kikuchi bands are transformed to points with Hough Transform. The width of the lines and the

angle between them are compared to a database of Miller indices. After determining the planes, a sequence of rotations are applied to the sample frame to match with a reference frame and the crystal orientation is determined [54] [56].

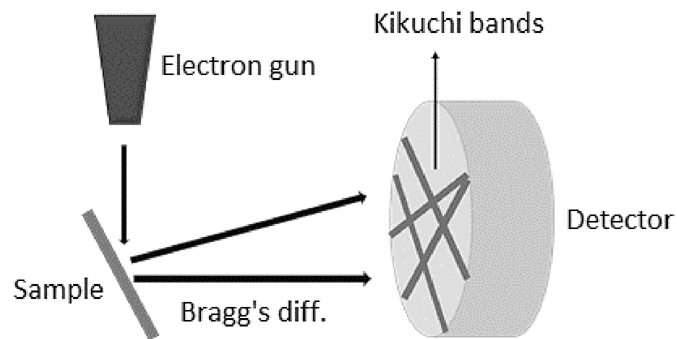


Figure 3.11. Electron-sample interaction in EBSD and formation of Kikuchi bands.

Crystallographic orientation data can be used to construct 2D maps and analyzing the grain structure of the sample. These maps show grain morphology, size and boundaries. Also the crystal structure and orientation of the sample are determined. An example of EBSD colored map is shown in Figure 3.12.

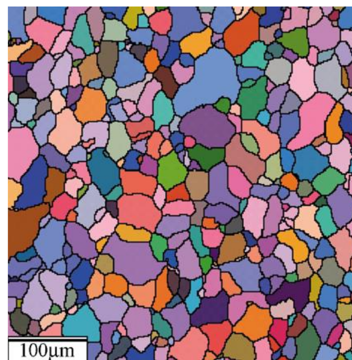


Figure 3.12. EBSD map of a recrystallized specimen of a commercial Al-Mg alloy (AA5182) with a weak texture [57].

3.2.4. Raman Spectroscopy

“Raman Effect”, a type of light scattering from molecules, was discovered by Prof. Chandrashekhara Venkata Raman in 1928, which brought him the Nobel Prize for Physics in 1930 [58]. Light scattering from molecules occur in two ways; mostly Rayleigh scattering, which is elastic; i.e. there is no frequency shift in the scattered photon and Raman scattering, which is inelastic where the frequency of scattered photon changes. The oscillating electric field of incident photon induces a dipole moment on the molecule. If there is a polarizability of the electron cloud around the molecule, the light will be scattered according to Raman Effect. The induced dipole moment (μ) is linearly dependent on the polarizability (α) and the electric field (E) [59];

$$\mu = \alpha E$$

In Raman spectroscopy, the sample is irradiated with monochromatic light (usually laser) and upon scattering, the shift in energy is measured in terms of wavenumbers (cm^{-1}) specific to the vibrations of the molecules. Some photons are scattered with less energy and a phonon is created. This energy shift appear as Stokes lines is the spectrum. On the other hand some photons gain energy from a molecule which is in excited state and a phonon will be annihilated. This type of shift appears as anti-Stokes lines (Fig. 3.13).

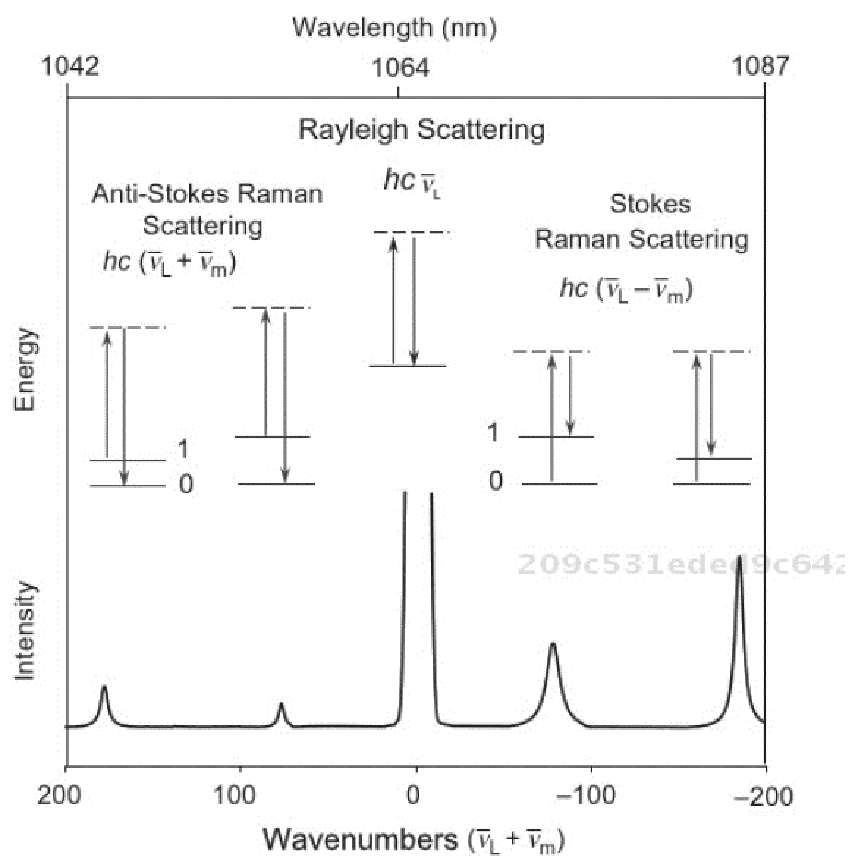


Figure 3.13. Schematic illustration of Rayleigh scattering as well as Stokes and anti-Stokes Raman scattering. Dashed lines indicate "virtual state" [59].

The main components of a Raman spectrometer are; excitation source (usually a CW laser), sample illumination system and optics for collecting light, wavelength selector (spectrophotometer) and detector. For excitation using pulsed lasers are advantageous for focusing the beam to a specific area, having monochromatic light and increased intensities [60]. According to the shape, size and shifts of the peaks in the Raman spectrum, properties like crystallinity, particle size or applied stress on the material can be determined.

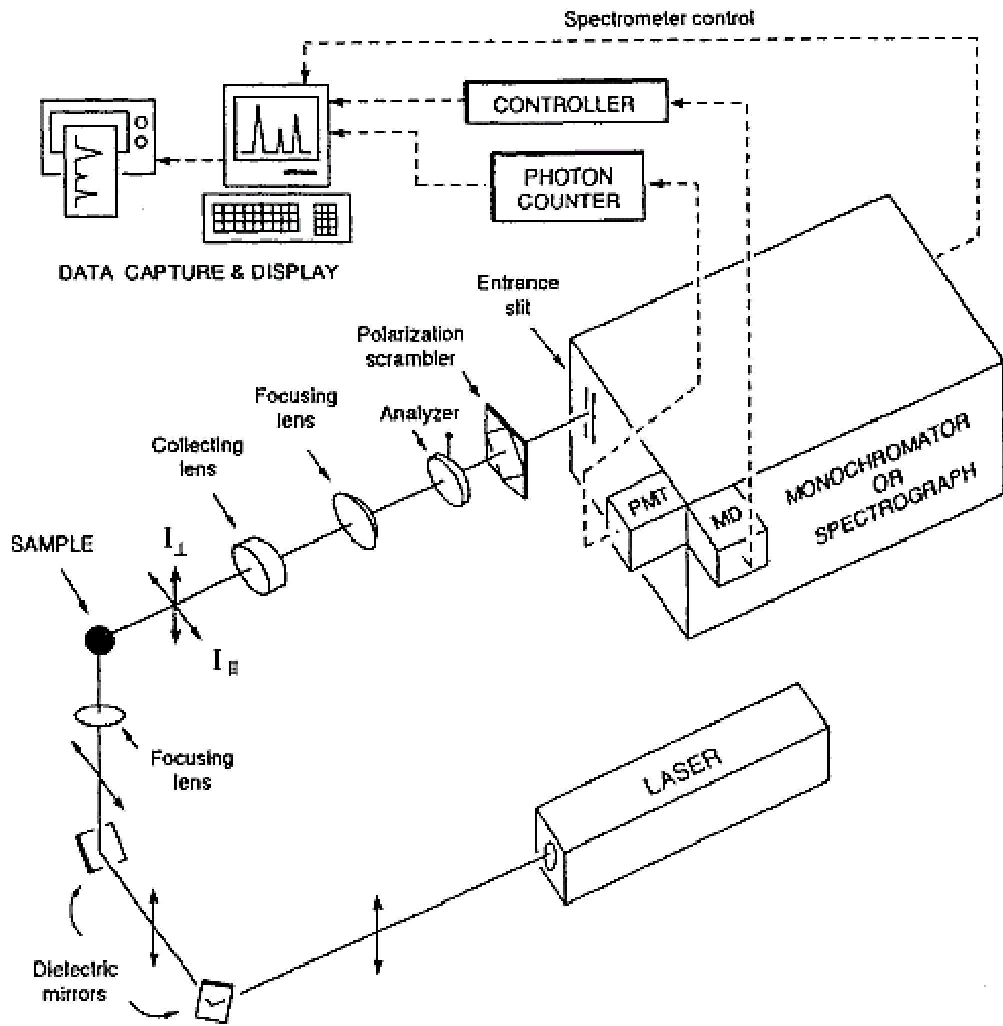


Figure 3.14. Schematic diagram of a Raman spectrometer [60].

CHAPTER 4

FABRICATION AND CHARACTERIZATION OF GeOI PLATFORM

4.1. Fabrication

Fabrication of germanium-on-insulator (GeOI) platform mainly consists of two photolithography and chemical etching steps to define seed and crucible parts and three sputtering deposition steps to grow oxide and germanium films on the silicon substrates. Before all the fabrication procedures, the silicon wafer substrates were cleaned using RCA1 procedure. The schematic representation of process flow is shown in Figure 4.1.

First step in the fabrication of GeOI is the growth of oxide films on silicon wafers using reactive RF sputtering technique. Power applied to Si target was 300 W, base pressure of the chamber was kept between $3 \times 10^{-7} - 7 \times 10^{-7}$ Torr, total gas flow (argon + oxygen) was kept at 20 sccm and the deposition pressure was 3 mTorr in all oxide depositions. The stoichiometry and thickness of oxide films were determined using spectroscopic ellipsometry. By this way, three different thicknesses of 40, 50 and 85 nm oxide films were fabricated.

On the oxide films 2µmx2µm seed layers were defined using a photolithography procedure. The samples were cleaned with acetone, isopropyl alcohol (IPA) and water, and dried with nitrogen gun before the procedure. Samples were then heated for 5 mins for proper dehydration. They were coated with S1805 photoresist and preheated at

120°C for 60 sec. For the lithography step a positive mask was used to define seed regions. Exposure time was 10 sec and post-heating was done at 120°C for 60 sec.

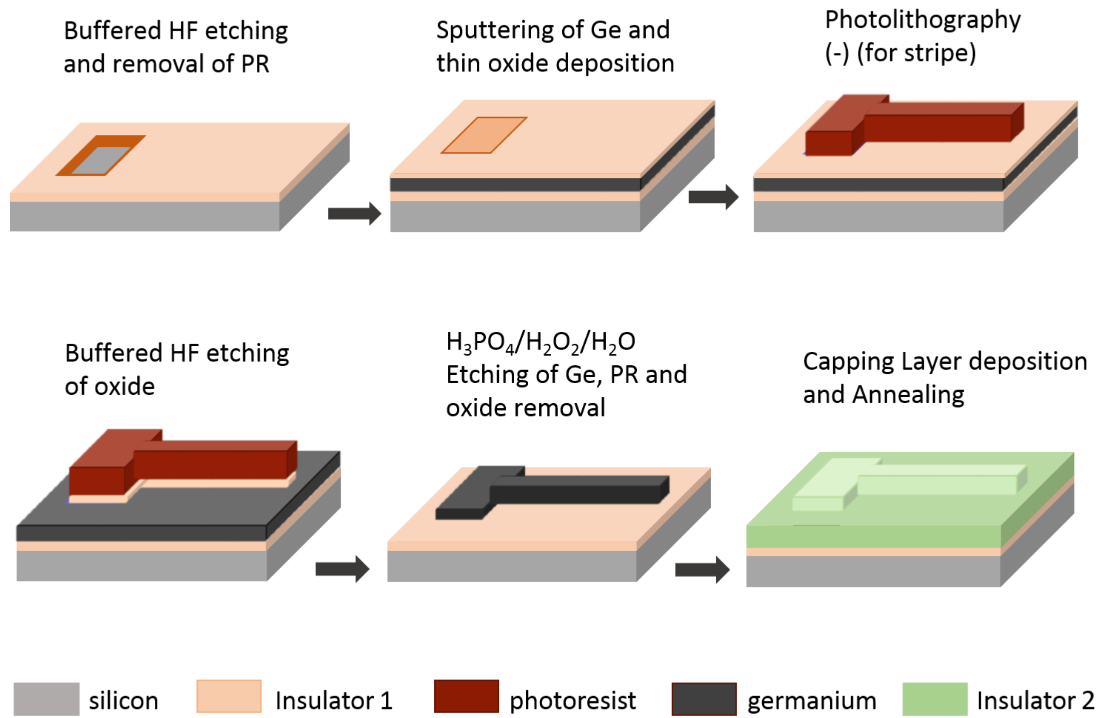


Figure 4.1. Fabrication steps of GeOI platform.

Samples were developed using MF319 developer for 30 sec. The seed profiles were observed under the microscope and samples were heated for 3 min before the etching step. Seed windows were etched down to silicon surface using BOE solution. After etching, photoresist was removed in acetone and samples were cleaned in IPA.

Until Ge deposition, the samples were kept in alcohol in order to keep the silicon surface in seed windows clean from oxidation. Samples were placed into load-lock chamber with alcohol. Ge target was pre-sputtered before loading the samples into the main chamber. Power applied to Ge target was 200W, Ar flow was kept at 20 sccm, base pressure of the chamber was kept between $2x10^{-7}$ – $3x10^{-7}$ Torr and deposition

pressure was 2 mTorr during deposition. Ge films with three different thicknesses of 150, 300 and 500nm were produced. Following Ge deposition a thin layer of oxide (~20nm) was deposited on the samples.

Stripe layers were defined on the germanium and oxide deposited samples with another photolithography procedure. In this step negative photoresist AZ5214 was used. Before the procedure samples were cleaned with acetone, IPA and water. They were dried with nitrogen gun and heated for further dehydration. Samples were spin coated with AZ5214. Before 5 sec exposure samples were heated for 50sec at 125°C, post-annealing was done at the same temperature for 2 min. Flood exposure was applied to the samples and they were developed in AZ726 developer solution for 20 sec. Stripe profiles were observed under light microscope and samples were heated for 3 min before BOE treatment. First the thin oxide layer was removed with BOE, then germanium layers were etched using 6:3:1 H_2O_2:H_2O:H_3PO_4 solution. After etching the photoresist was removed with acetone and samples were cleaned with IPA.

Deposition of capping oxide layer was again carried on with RF magnetron sputtering technique. Before sputtering the samples were dried with nitrogen gun. All the conditions were kept same as in the first oxide deposition step. Capping layers with four different thicknesses (150 nm, 500 nm, 1 μm and 2 μm) were produced on the samples.

As the last step samples were annealed with different profiles using rapid thermal anneal (RTA) system. In all the annealing profiles samples were heated up to 800°C with a rate of 100°C/sec, held at the same temperature for 1 min, heated again up to temperatures above the melting point of germanium (938°C) with the same rate. Different cooling rates were applied from 5°C/sec to 50°C/sec.

4.2. SEM Results

Microcrucible and surface profiles of germanium film were investigated after second photolithography and etching step at GÜNAM, METU (Fig. 4.2). The roughness at the edges of stripes and on the surface of deposited Ge film were negligible. Cross-section of the sample after capping layer deposition was also observed. Thickness of the capping layer was increased for suppressing agglomerations observed with thin (~150 nm) oxide capping. Ge film was well adhered to the underlying oxide layer and capping layer was also well distributed on Ge film (Fig. 4.4).

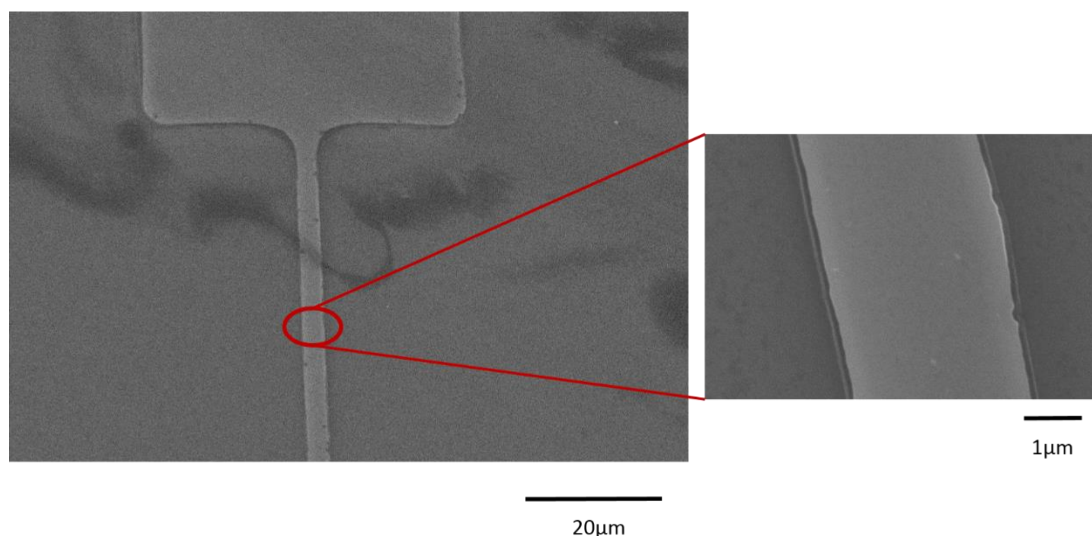


Figure 4.2. Ge microcrucible and surface profiles after H_2O_2:H_2O:H_3PO_4 etching.

The main challenge in the fabrication of GeOI films was Stranski-Krastanov growth, as mentioned in Chapter 2. In order to observe the random nucleation in Ge film, samples were annealed at different temperatures above melting point of Ge and cross-sections of microcrucible profiles were observed with SEM at GÜNAM, METU. As seen in Figure 4.3 germanium islands begin to form upon increasing temperature. The reason of this island formation is the surface energy difference between Ge and

underlying SiO_2 films. Ge film tends to decrease surface area in order to reduce its surface energy. This phenomena is supported by the work of Yam et. al., where the interfacial energy between Ge and SiO_2 was derived as 5.67 eV/nm^2 [61].

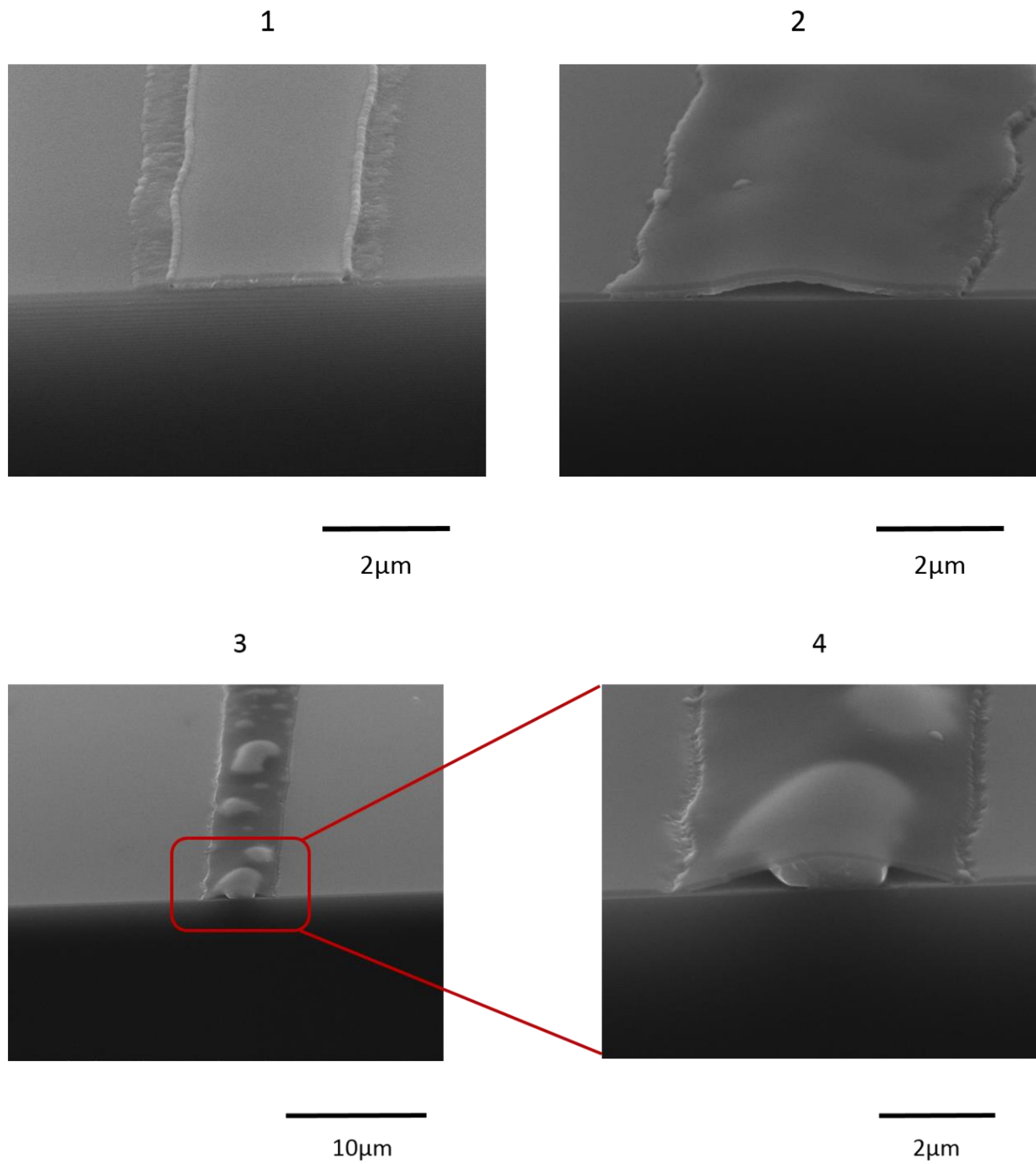


Figure 4.3. Formation of Ge islands under thin capping layer (150 nm) for annealing temperatures; (1) 1050°C, (2) 1075°C, (3) 1090°C. (4) is a closer look to (3).

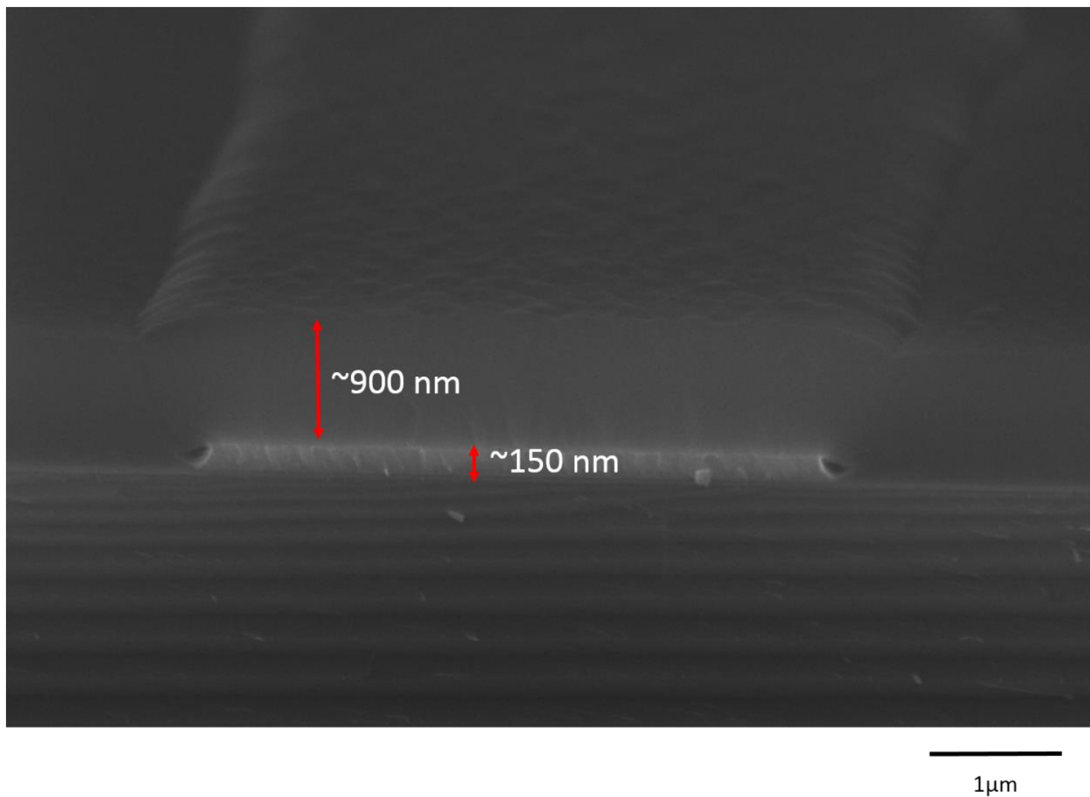


Figure 4.4. Cross-section image of GeOI structure before annealing with thick capping layer (~900 nm).

The sample with thick (~900 nm) capping layer annealed at $1075^{o}C$ was treated with 7:1 BOE solution to remove the oxide and top-view image was taken at GÜNAM, METU. No agglomeration is observed for this sample, indicating that increasing the capping layer thickness suppresses Ge balling up and provides a smooth film (Fig. 4.5).

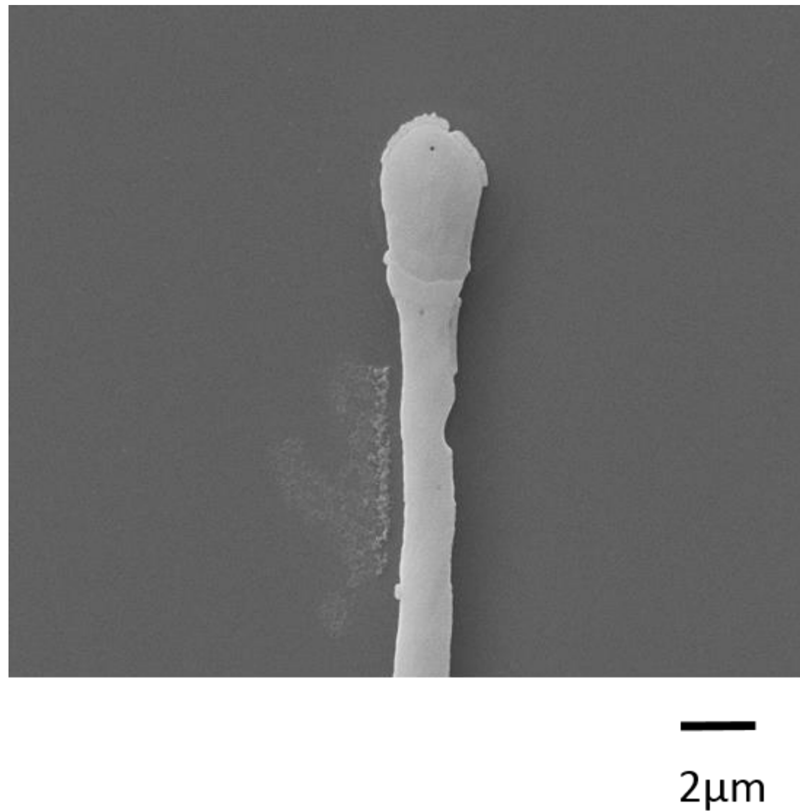


Figure 4.5. GeOI profile after annealing at 1075ºC and removing capping layer (~900 nm). No agglomeration is observed.

4.3. EBSD Results

Crystal formation (single or poly), orientation and grain size were investigated in five different aspects; insulator thickness, Ge film thickness, capping layer thickness, temperature and cooling rate. The measurements were carried out in the Central Lab., METU. The thickness parameters are shown in Figure 4.6.

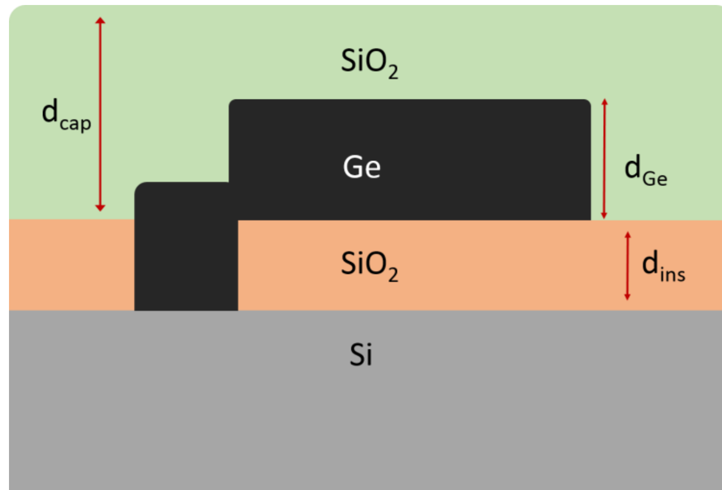


Figure 4.6. Cross section schematics of samples.

4.3.1. Effect of Insulator Thickness

Three different insulator thicknesses were compared in order to study the effect of insulator layer thickness on crystal formation. The fabrication parameters of the samples are shown in Table 4.1. Sample with 85 nm oxide is observed to be polycrystal both in the seed and stripe regions, whereas the other samples were close to single crystal form. Sample with 40 nm oxide had the same orientation (100) in the seed region and was closer to the same orientation in the stripe region with a lattice rotation. The sample with 50 nm had a different orientation in the stripe showing that there is a random nucleation which does not follow crystal orientation of Si substrate.

Table 4.1. Fabrication parameters of samples for different insulator thicknesses.

Sample #	d_{ins} **(nm)**	d_{Ge} **(nm)**	d_{cap} **(nm)**	**Annealing Temp. (°C)**	**Cooling (°C/s)**
1	40	150	900	1075	10
2	50	150	900	1075	10
3	85	150	900	1075	10

Figure 4.7. Crystallization for different insulator thicknesses according to Table 4.1.

Polycrystal formation in the case of thick insulator layer can be explained by the change in the cooling rate. Since oxide is a poor thermal conductor, as the thickness increases cooling rate will decrease to the point where lateral crystal growth cannot exceed random nucleation rate, as in the study of Miyao's group, in 2011 [62]. Thus thin insulator layers are more efficient in obtaining single crystal Ge growth.

4.3.2. Effect of Ge and Capping Layer Thicknesses

Nine samples with different Ge and capping oxide thicknesses were fabricated according to parameters in Table 4.2. Three Ge film thicknesses of 150, 300 and 500 nm, and three capping layer thicknesses of 500, 1000, and 2000 nm were compared in terms of crystal formation. Samples with 150 nm Ge films (1, 2 and 3 in Figure 4.8) were all polycrystal in the seed region and got closer to single form in the stripe region as the capping layer thickness increased. Also voids were observed after BOE treatment. On the other hand, samples with thicker Ge (300 and 500 nm) were observed to be more intact structurally, seed and stripe regions were close to Si orientation (100) (4,5,6,7,8 and 9 in Figure 4.8).

Table 4.2. Fabrication parameters of samples for different Ge and capping layer thicknesses.

Sample #	**d_{ins} (nm)**	**d_{Ge} (nm)**	**d_{cap} (nm)**	**Annealing Temp. (^oC)**
1	40	150	500	1075
2	40	150	1000	1075
3	40	150	2000	1075
4	40	300	500	1075
5	40	300	1000	1075
6	40	300	2000	1075
7	40	500	500	1075
8	40	500	1000	1075
9	40	500	2000	1075

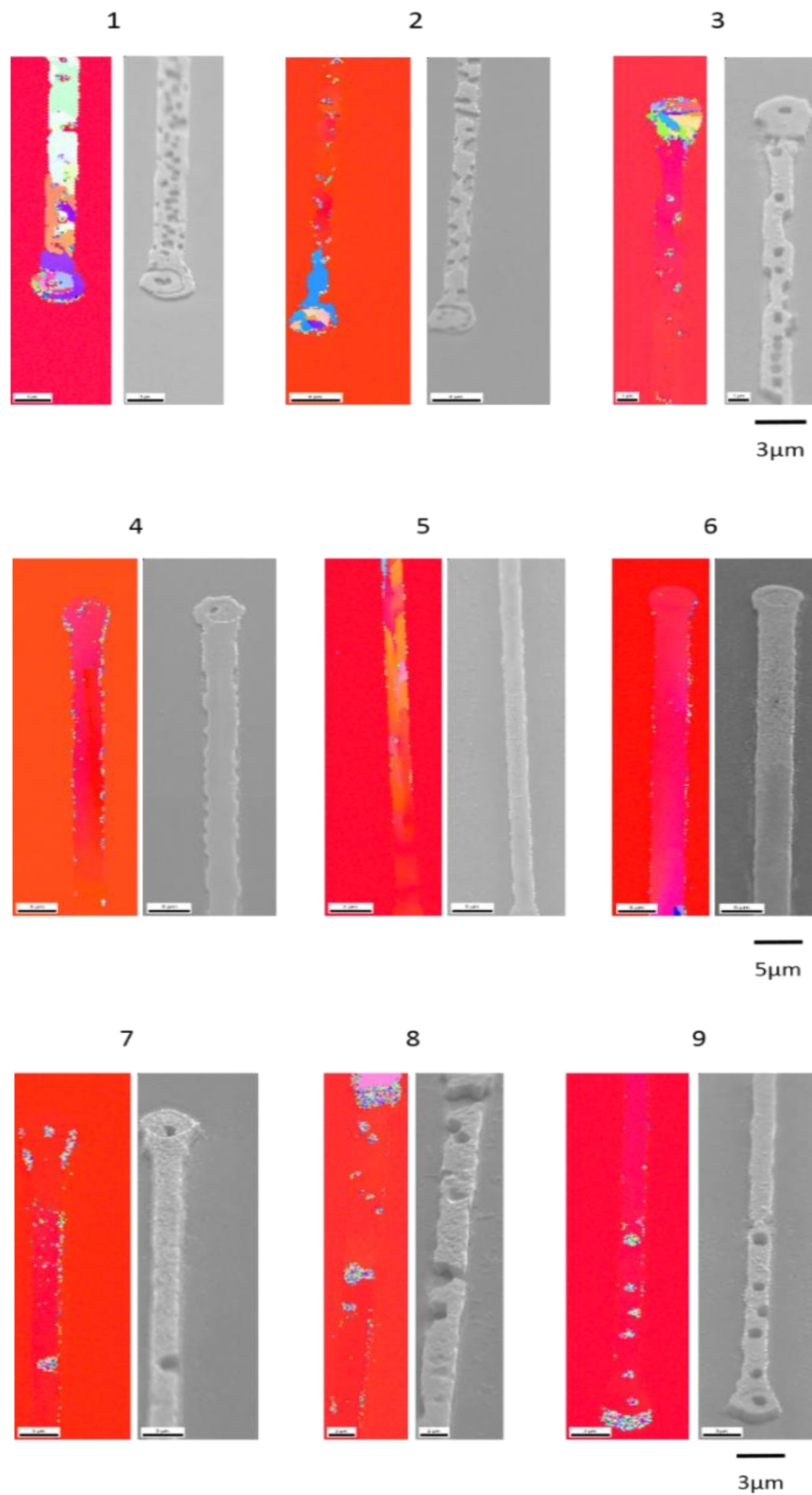


Figure 4.8. Crystal formation for different Ge and capping layer thicknesses according to Table 4.2.

Capping layer thickness plays a crucial role in suppressing agglomerations and preventing the evaporation of Ge film. As mentioned in SEM results a thin (~150 nm) capping layer does not prevent Ge agglomeration since the stress on the film is not enough [62]. On the other hand, capping thickness above 500 nm was observed to have a slight effect on Ge with large crystallites. For thin Ge film (150 nm) lateral growth followed the (100) orientation for 1000 and 2000 nm capping oxides, whereas polycrystal Ge is formed for 500 nm capping. Since polycrystalline structure is related to random nucleation rate, it can be deduced that thicker capping layer suppresses random nucleation and provides larger crystallite sizes.

It was observed that increase in Ge thickness affected crystal formation positively. While the seeds of the samples with 150 nm Ge layer were polycrystal, crystal orientation in the 300 nm and 500 nm samples followed that of the silicon from seed areas. Increasing the Ge thickness will reduce the surface/volume ratio and this may help to reduce the interface energy, decreasing the random nucleation rate. Moreover, increased Ge volume will result in a slower heat dissipation and melting point can be stable in the liquid during growth. Ge thickness also affected the lattice rotation in the stripe regions. If we look at the contrast difference in the stripe regions for 300 nm and 500 nm Ge films (Fig. 4.8, 4, 5, 6 vs. 7, 8, 9), less contrast change was seen for higher Ge thickness. Douglas et. al. found that increasing Ge film thickness reduces the twist formations in stripe, which also supports our findings [63].

4.3.3. Effect of Temperature and Cooling Rate

Effect of annealing was studied among four different temperatures, 1065, 1070, 1075 and 1090°C. Fabrication parameters of the samples are shown in Table 4.3. Samples annealed at 1065°C were totally polycrystal with very small grains. As the temperature increased much larger grains were observed for 1070°C. At 1075°C the seed was totally single crystal with Si (100) orientation and the stripe was close to single form with lattice rotation. At the annealing temperature 1090°C the whole structure again

became polycrystal with large grains and the Ge film was observed to spread under capping oxide.

Table 4.3. Fabrication parameters of samples for different annealing temperatures.

Sample #	d_{ins} (nm)	d_{Ge} (nm)	d_{cap} (nm)	Annealing Temp. (°C)	Cooling (°C/s)
1	40	150	900	1065	10
2	40	150	900	1070	10
3	40	150	900	1075	10
4	40	150	900	1090	10

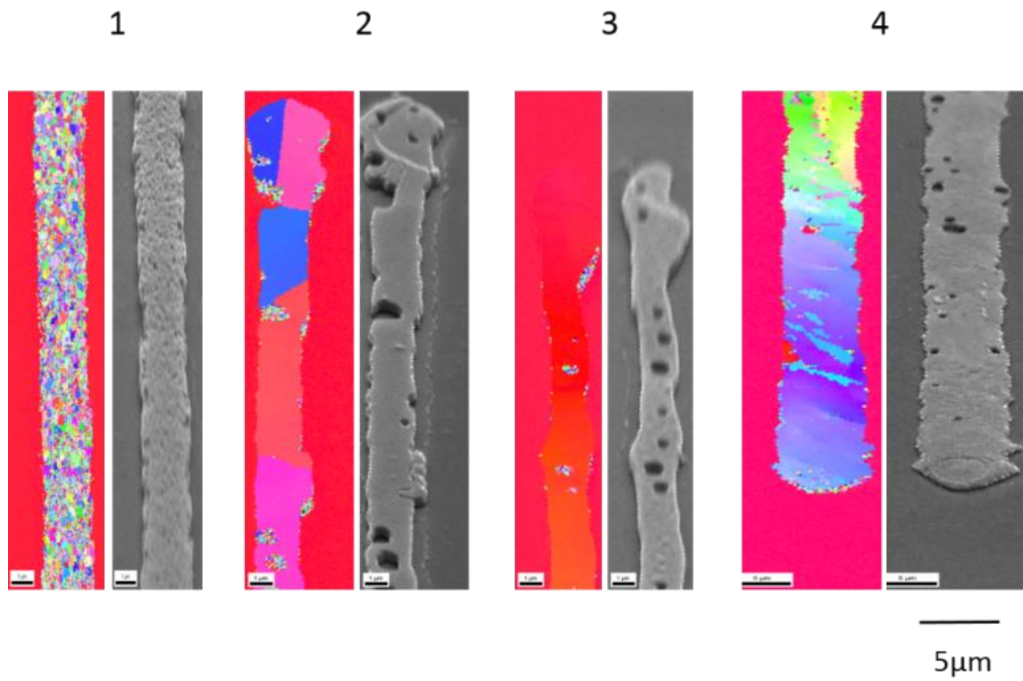


Figure 4.9. Crystal formation for different annealing temperatures according to Table 4.3.

According to a study by Liu et. al., grain size increases with increasing the annealing temperature [64]. They studied the crystal formation under and above the melting point of Ge. The films were polycrystal for low annealing temperatures, whereas for the temperatures above melting point grains size increased and the crystal became single. Below melting point the film is not fully liquid so that upon cooling many nuclei will form as centers for spontaneous nucleation. However, above melting point all the Ge will be in liquid form and nucleation rate will be reduced due to equilibrium. Bai et. al. also suggested that for reducing the Si diffusion into the Ge film, the anneal temperature should be just above the melting point [65].

In SEM results, on the other hand, we have shown that upon increasing anneal temperature Ge islands form in order to reduce surface energy. Thus with increasing temperature random nucleation rate also rises. In order to maintain higher lateral growth rate than spontaneous nucleation, the annealing temperature should be optimized. It should also be noted that the annealing temperature was measured with pyrometer, which collects infrared signals from the RTA chamber, and can be much higher than the temperature of Ge films during the process.

Table 4.4. Fabrication parameters of samples for different cooling rates.

Sample #	**d_{ins} (nm)**	**d_{Ge} (nm)**	**d_{cap} (nm)**	**Annealing Temp. (^oC)**	**Cooling ($^oC/s$)**
1	40	150	900	1075	5
2	40	150	900	1075	10
3	40	150	900	1075	15
4	40	150	900	1075	20
5	40	150	900	1075	25
6	40	150	900	1075	30
7	40	150	900	1075	40
8	40	150	900	1075	50

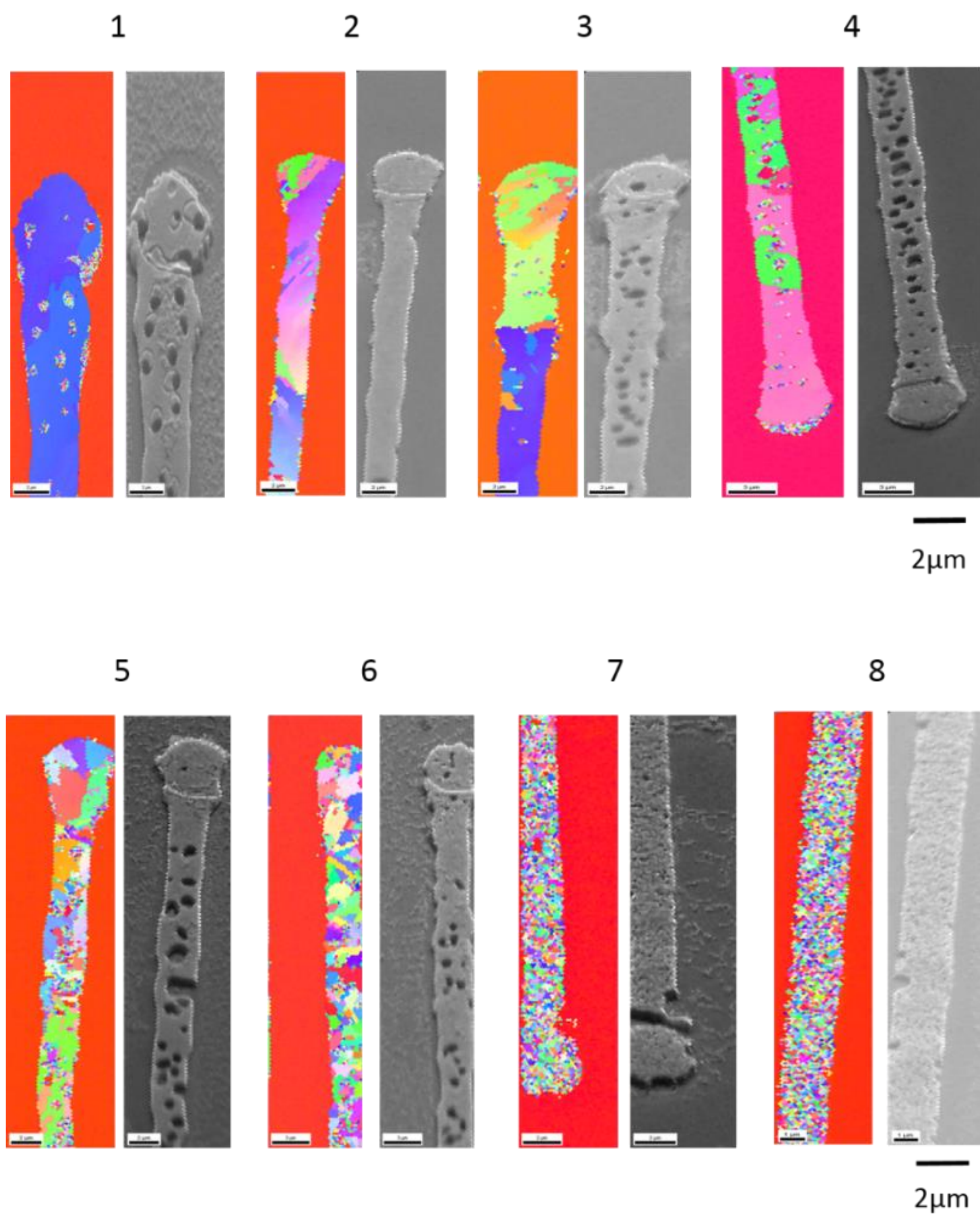


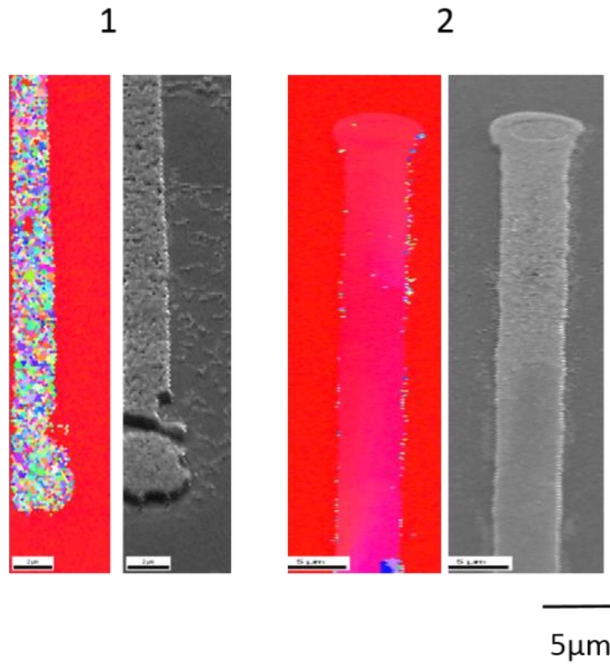
Figure 4.10. Crystal formation for different cooling rates according to Table 4.4. Annealing temperature is 1075ºC.

Eight samples with different cooling rates were fabricated according to parameters in Table 4.4 and compared. For cooling rates up to 20°C very large grains (~10 µm) were observed, however as the rate increases the grains were smaller and caused polycrystalline Ge films.

The cooling effect can be explained by follows. If the temperature is above the liquidus curve for germanium, the nuclei number is low in the melt. Thus, slow cooling will initiate nucleation from less sites and random nucleation will not dominate. However, upon supercooling the nuclei number will rise and initiate spontaneous nucleation, which will result in polycrystal formation [66]. Also, Miyao's group have studied this effect on SiGe crystal profiles and they have applied cooling rates between 10-19°C/sec [67]. They have found that low cooling rate (10°C/sec) provides a uniform profile in the film, whereas high rates cause abrupt changes in the SiGe profile. Consequently, low cooling rates can provide a controlled growth mechanism.

4.4. Raman Results

The quality of the crystal and the strain in the film is determined by Raman measurement. For this purpose two samples are chosen for the comparison of single and polycrystalline structures in terms of peak shifts and FWHM (full-width half-maximum) values in the spectra. In Figure 4.11, EBSD images of the two samples and fabrication parameters are shown. First sample was chosen among the study of cooling rate and the second was chosen from the study of Ge and capping layer thickness. As seen from the EBSD figure, the first sample is polycrystal as a whole, whereas the second one is nearly single in crystal form. The polycrystal structure of the first sample can be attributed to thin Ge layer and high cooling rate. As the Ge thickness increase and with a low cooling rate nearly single crystal was obtained as mentioned in EBSD results.



Sample	d_{ins} (nm)	d_{Ge} (nm)	d_{cap} (nm)	Anneal temp (°C)	Cooling rate (°C/sec)
1	40	150	900	1075	40
2	40	300	2000	1075	7

Figure 4.11. EBSD images and fabrication parameters of (1) polycrystal and (2) single crystal Ge samples for Raman measurement.

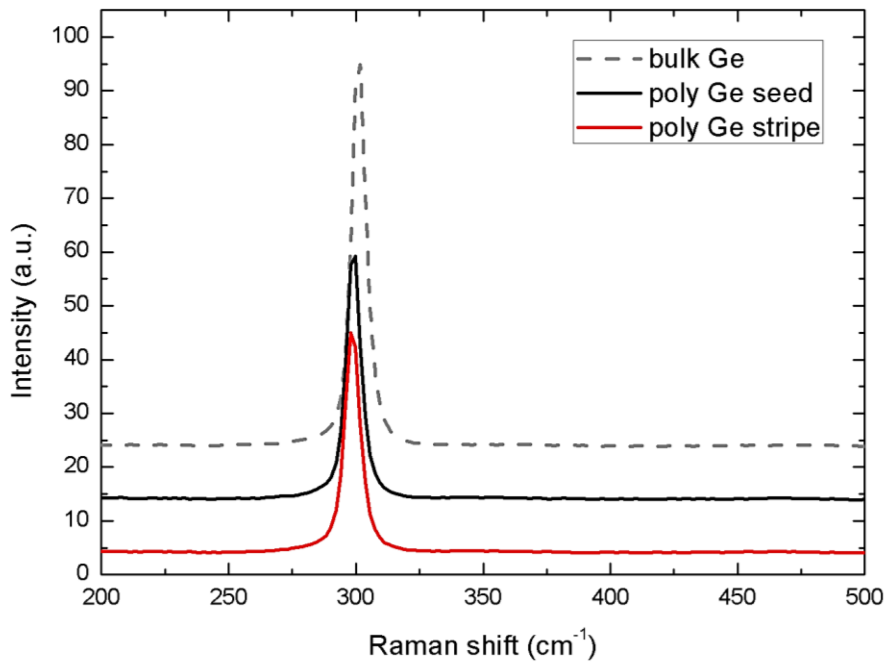


Figure 4.12. Raman shift of bulk Ge and poly crystal Ge (1).

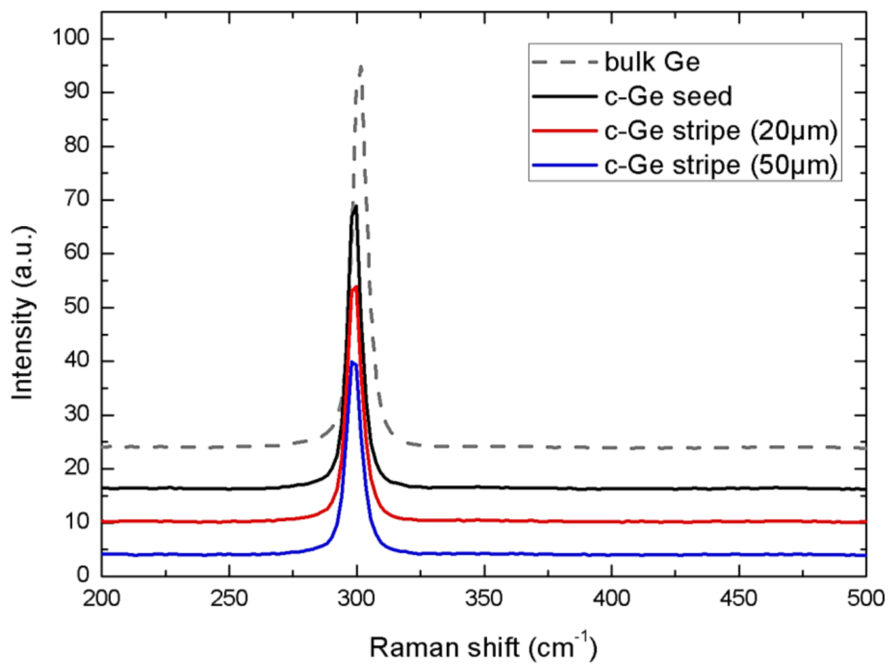


Figure 4.13. Raman shift of bulk Ge and nearly single crystal Ge (2).

FWHM and peak center values obtained from Raman spectrums of two samples (Fig. 4.12 and 4.13) show the crystal quality and tensile strain in the film, respectively (Table 4.5). The FWHM value taken from the seed region of crystal structure (2) is very close to that of bulk Ge, which means the crystal quality is high. In the stripe regions, this value increases probably due to twisting and crystal quality decreases as we go further from the seed. On the other hand, the FWHM of polycrystal seed and stripe regions are higher than the bulk Ge as expected. In the study of Liu et. al., in 2015, FWHM values of bulk Ge and crystal films were found to be 5.45 and 5.8, respectively [64]. In their study the FWHM value in the seed region was also higher than in the stripe (5.51 to 5.85). They suggested that this increase is due to different nucleation processes taking place in the seed and stripe regions.

Peak center of bulk Ge is found to be at 301.1 cm^{-1}. As seen in Table 4.5, the peak centers shift towards lower wavenumbers. This indicates a tensile strain in the annealed Ge films as expected. The strain in the film is explained by the thermal expansion coefficient difference between Ge and SiO_2 layer. Above the melting point, all the Ge film will be in liquid form and the interaction with underlying insulator will be decreased. As the film is cooled down, the liquid will turn to semi-solid state which increases the interaction of the two layers and strain will be induced in this state [37] [68].

Table 4.5. Peak center and FWHM values for bulk Ge, polycrystal Ge (1) and single crystal Ge (2) samples.

Sample Name	**Peak Center (cm^{-1})**	**FWHM (cm^{-1})**
Bulk Ge	301.1	5.5
(1) poly-Ge seed	299.1	6.3
(1) poly-Ge stripe (20µm)	298.7	6.5
(2) c-Ge seed	299.1	5.6
(2) c-Ge stripe (20µm)	299.1	5.9
(2) c-Ge stripe (50µm)	298.9	6.1

CHAPTER 5

CONCLUSIONS AND FUTURE STUDIES

Germanium is a promising material for CMOS and photovoltaic technology with its advantages of high carrier mobility, lower band gap compared to silicon, direct band gap property in strained form and lattice match with III-V compounds. These advantages carry germanium one step forward as an alternative in the production of high-speed transistors, infrared photodetectors and lasers, and also photovoltaic cells which use III-V compounds like GaAs. GeOI (germanium-on insulator) platform offers the epitaxy of germanium on silicon substrates, which is still the most abundant material in CMOS technology. In this study, crystal Ge films were grown on insulator layers using rapid melting growth method and the effects of different parameters were examined. The defect density and Si-Ge mixing were aimed to be reduced by introducing a seed area, and large area single crystal Ge films were aimed to be obtained on insulator.

In this study effects of insulator, germanium and capping layer thicknesses, temperature and cooling on the crystal quality and orientation of Ge films were examined. Increasing insulator layer thickness was found to decrease the crystal quality. For thin insulators (40, 50 nm) crystal formation was close to single, whereas thicker insulator layer (85 nm) caused polycrystalline structure. Germanium and capping layer thicknesses both affected the crystal quality positively. Increasing the germanium thickness provided lateral growth to exceed spontaneous nucleation, while capping layer was observed to suppress agglomerations. Higher annealing temperature enabled larger grains up to some point where the integrity of the microcrucibles start to break down and again polycrystal was observed. Faster cooling typically reduced the crystallite sizes. Low cooling rates (5-15ºC/sec) provided larger grains in the crystal. The crystal quality was also compared for poly and single crystal structures with Raman measurements. FWHM values were found to be 5.6 cm^{-1} for a single

crystal sample and 6.3 cm^{-1} for a polycrystal structure. Compared to FWHM of bulk Ge (5.5 cm^{-1}) these results confirm that crystal quality increases with thin insulator, thicker Ge and capping layers, an optimized annealing temperature and low cooling rates.

Further studies can be carried on with different insulator materials such as HfO_2 in order to observe the effect of interface energy difference between Ge and insulator. Moreover, TEM measurements are important in determining the Si-Ge mixing and defect density in the seed regions and will show the importance of Si diffusion into Ge liquid during growth. Finally, the most crucial part of growing Ge films is to make sure that the Si interface is clean before the deposition. Therefore, TEM results can also tell whether the interface has any impurities like oxygen.

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