

THERMAL EFFECTS OF GATE CONNECTED FIELD-PLATES AND SURFACE
PASSIVATION ON ALGAN/GAN HEMTS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
MECHANICAL ENGINEERING

MAY 2018

Approval of thesis:

**THERMAL EFFECTS OF GATE CONNECTED FIELD-PLATES AND SURFACE
PASSIVATION ON ALGAN/GAN HEMTS**

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ABSTRACT

THERMAL EFFECTS OF GATE CONNECTED FIELD-PLATES AND SURFACE PASSIVATION ON ALGAN/GAN HEMTS

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May 2018, 75 pages

AlGaN/GaN high electron mobility transistors (HEMTs) are widely preferred in automotive, space, and military applications due to their superior electrical and thermal properties. However, when operated in full capacity, their electrical reliability drops significantly due to electron collapse, device degradation, concentrated heating, and mechanical stresses. To increase the reliability and maximum performance of GaN HEMTs, field-plate and surface passivation technologies are used frequently. Although significant research has been done to understand the electrical effects of these structures, their true effect on thermal performance of devices is still missing in the literature. For this purpose, thermal simulations with and without gate field-plates having different thicknesses of SiO₂ and Si₃N₄ surface passivation layers are performed. These simulations, performed using realistic Joule heating data obtained from device electrical simulations, proves that up to 6% reduction in hotspot temperature along with increased breakdown voltage can be obtained by using gate field-plate technology in GaN HEMTs operated around 4 W/mm. Since the percentage of temperature reduction is the same for devices operated at similar power densities, net temperature reduction will be higher in devices with more localized heating with higher maximum temperatures, as in the case for devices biased with more negative gate bias. Optimization studies performed as a part of this study suggests that while thick surface passivation (>200nm for Si₃N₄) eliminates the thermal advantages of field plate technology, thin passivation layers (<25 nm) decrease the breakdown voltage significantly and promote electron leakage. Similar results suggesting the importance of passivation thickness optimization are

obtained for devices with thinner SiO₂ passivation layers. Thus, significant thermal advantages are observed when gate field-plates are introduced to the device if field-plate length, passivation material and thickness are optimized based on the device operation condition.

Keywords: AlGaN, GaN, HEMT, Thermal Modelling, Electro-Thermal Simulations, Field-Plate, Passivation

ÖZ

ALGAN/GAN HEMT AYGITLARINDA KAPI BAĞLANTILI ALAN LEVHASININ VE YÜZEY PASİVASYONUNUN ISIL ETKİLERİ

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Mayıs 2018, 75 sayfa

AlGaN/GaN HEMT cihazları üstün ısıl ve elektriksel özellikleri sebebiyle otomotiv, uzay, ve savunma sanayi uygulamalarında yaygınca tercih edilmektedir. Ancak tam kapasitede çalıştırıldıklarında elektriksel dayanıklılıkları cihaz degradasyonu, yoğun ısınma etkisi, ve mekanik streslerden ötürü belirgin bir şekilde düşüş yaşanmaktadır. Cihaz dayanıklılığını ve performansını arttırmak amacıyla alan levhası ve yüzey pasivasyonu teknolojileri yaygınlaşmakta ve literatürde bu teknolojilerin elektriksel etkilerine dair birçok araştırma bulunmasına rağmen, gerçek ısıl etkileri hala yeteri kadar bilinmemektedir. Bu amaçla, alan levhalı ve levhasız farklı SiO₂ ve Si₃N₄ yüzey pasivasyonuna sahip cihazların ısıl simülasyonu gerçekleştirildi. Bu simülasyonlarda, elektriksel simülasyonlardan elde edilen gerçekçi Joule ısınma verileri kullanılarak alan levhası kullanılan cihazlarda 4 W/mm güç yoğunluğu seviyesinde maksimum sıcaklıkta %6 düşüş ile çökme voltajında artış gözlemlendi. Yüzde olarak bu düşüşün benzer güç seviyeleri için aynı olmasından dolayı, daha yüksek electron kapı voltajında çalıştırılan ve daha yoğun ısınma dağılımı ile birlikte yüksek sıcaklıklara sahip olan cihazların net sıcaklık değerlerinde daha yüksek düşüş elde edildi. Öte yandan, bu çalışmada gerçekleştirilen optimizasyon çalışmalarına göre kalın yüzey pasivasyonu (>200nm Si₃N₄ için) uygulandığı zaman alan levhasının ısıl avantajları elimine olurken, fazla ince uygulandığında (<25 nm) çökme voltajında düşüş ve kanaldan elektron kaçağı gözlemlenmiştir. Pasivasyon kalınlığı optimizasyonunun önemini gösteren benzer sonuçlar daha ince SiO₂ pasivasyon katmanı için de elde edilmiştir. Alan levhası uzunluğu, pasivasyon malzemesi ve kalınlığı optimize

edildiđi taktirde, GaN HEMT cihazlarda alan levhası kullanımı ile kayda deđer ısıl avantajlar sađlanmıřtır.

Anahtar Kelimeler: AlGaN, GaN, HEMT, Sıcaklık, Isıl modelleme, Elektro-termal Simulasyon, Alan Levhası, Pasivasyon

To My Dear Mom, Dad and Sister

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisor Dr. F. Nazlı Dönmezer Akgün for the continuous support and mentorship throughout my Master study and related research. This work would not have been materialized without her valuable guidance, profound belief and extensive knowledge. This work would not be possible. I could not have imagined having a better advisor and mentor. I would also like to express my appreciation to my committee, for reviewing my work, giving helpful advice, and sharing their constructive criticism.

I cannot begin to express my gratitude to my parents and sister for raising me to become the person I am today. Without their support, guidance and love I wouldn't reach to my potential and learn how to succeed. All the support they have provided me over the years was the greatest gift anyone has ever given me.

This research was supported by the METU-BAP (Grant no: BAP-08-11-2015-028) and the TUBITAK (Grant no: 115E756), without either of which this work would not have been possible. Also, valuable data and fabricated devices are provided by Bilkent University NANOTAM research center in order to enhance the capability of this research.

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LIST OF ABBREVIATIONS

ABBREVIATIONS

1D: One Dimensional

2D: Two Dimensional

2DEG: Two Dimensional Electron Gas

3D: Three Dimensional

AlGa_N: Aluminum Gallium Nitride

AlGaAs: Aluminum Gallium Arsenide

AlN: Aluminum Nitride

GaAs: Gallium Arsenide

GaN: Gallium Nitride

HEMT: High Electron Mobility Transistors

IR: Infrared

LDMOS: Laterally Diffused Metal Oxide Transistor

MOCVD: Metal Oxide Chemical Vapor Deposition

MTTF: Mean Time-to-Failure

PEALD: Plasma Enhanced Atomic Layer Deposition

PECVD: Plasma Enhanced Chemical Vapor Deposition

RF: Radio-frequency

Si: Silicon

SiC: Silicon Carbide

Si_3N_4 : Silicon Nitride

SiO_2 : Silicon Dioxide

TBR: Thermal Boundary Resistance

TTF: Time-to-Failure

CHAPTER 1

INTRODUCTION

1.1 AlGaN/GaN HEMTs

In late 1970s, improvements in molecular beam epitaxy growth technique and modulation doping along with a strong interest in quantum well structure led to the production of depletion type MOSFETs [1]. This introduced the idea to control the electron movement in a multi-layer device. Later, Schottky gate contact is added to the overall design creating the high-electron-mobility transistor (HEMT) layout [2]. At the beginning, HEMTs were based on AlGaAs and GaAs semiconductor layers to create an electron depletion region, many research laboratories started to develop new structures to improve their designs [2], [3]. As a results of those efforts, HEMTs were introduced to military and space industries by 1990s and entered consumer market in satellite receivers and emerging mobile phone systems [4], [5].

In 2000s, with the improvement of deposition methods such as metal organic chemical vapor deposition (MOCVD), growing GaN on different substrates became possible and first AlGaN/GaN HEMT is developed [6]. Shortly, AlGaN/GaN HEMTs became one of the most investigated solid-state electronic devices in power electronics industry due to their high radio frequency (RF) power densities, high electron mobility and breakdown fields, and wide bandgaps [7]–[11]. Breakdown voltage is the minimum voltage value required for a semiconductor to become conductive and bandgap is an energy range where electron states cannot exist, which is the energy state between the top of the valence band and bottom of the conduction band for semiconductor materials. Both of these properties are critical in designing power electronics. Table 1 gives the material property comparison between GaN, GaAs, Si and SiC. Compared to GaAs, Si, and SiC; GaN had higher thermal conductivity, higher critical breakdown field, and wider

bandgap; making it more durable against breakdown and burnout even at high power operation conditions[12]–[14]. Due to their such capabilities, AlGaIn/GaN HEMTs replaced silicon LDMOSs and GaAs pHEMTs in RF applications and became popular in automotive, defense, and space industries in recent years [15], [16].

Table 1.1 Material properties of GaN, GaAs, Si and SiC. [7]-[11]

	Thermal Conductivity [W/mK]	Breakdown Field [MV/cm]	Bandgap [eV]
GaN	180	3	3.49
GaAs	50	0.4	1.1
Si	150	0.3	1.42
SiC	450	4.5	3.26

GaN electronic devices market reached to \$0.87 b in 2016 and is expected to grow with a compound annual growth rate of 17.0% to reach \$3.43 b in 2024 according to Transparency Market Research. With the increasing market share, AlGaIn/GaN HEMT performance also increased dramatically reaching 41.4 W/mm continuous-wave power density [17], 10400 V breakdown voltage [18], 65% power-added efficiencies at 10 GHz frequency [19] and maximum operation frequency of 100 GHz [20] in recent years.

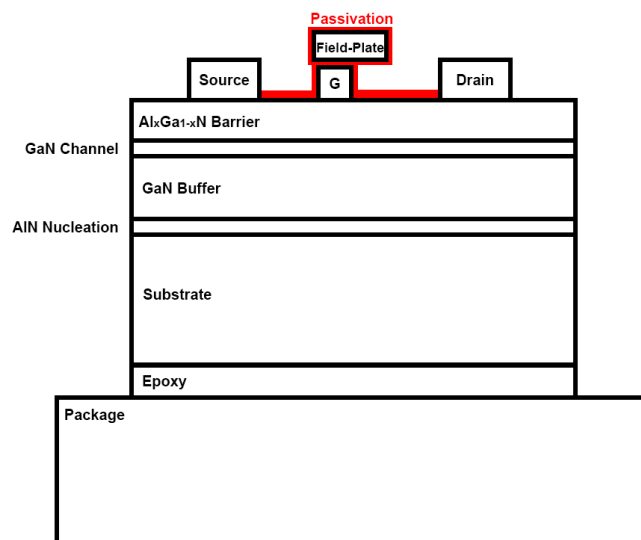


Figure 1.1. Cross-section representation of a gate field-plated AlGaIn/GaN HEMT multilayer structure.

High power density capabilities of AlGaN/GaN HEMTs arise from multi-layer, vertical stacked structure of the device. Figure 1.1 shows the cross section representation of a gate field-plated AlGaN/GaN HEMT multi-layer structure. Barrier ($\text{Al}_x\text{Ga}_{1-x}\text{N}$), GaN channel and GaN buffer layers are grown on AlN using high pressure and temperature MOCVD technique. AlN thin layer is used as a nucleation layer between substrate and GaN buffer. Beneath this multi-layer semiconductor and nucleation layer stack, a thick substrate layer is used and bonded to device package by using epoxy. SiC, sapphire, or diamond can be used as substrate material depending on the application and necessities. In high power and high temperature applications, expensive diamond related materials are preferred to thermally manage the device and increase reliability due to high thermal conductivity of diamond. On the other hand, SiC substrate materials can be used where cost efficiency is the priority instead of operation capability under extreme thermal conditions [21]–[23]. Barrier ($\text{Al}_x\text{Ga}_{1-x}\text{N}$) layer isolates metal contacts from electron channel, creating a barrier against electron leakage. Opposite electrical charges of AlGaN and GaN semiconductor layers in the device generates a region inside GaN channel where electrons accumulate between these two layers creating a charge density [24]. In general, crystal structure of GaN channel layer has less defects compared to GaN buffer layer. GaN channel region crystalline structure quality is critical since electron transport takes place in this layer. During deposition process, GaN crystal structure above AlN layer has lower quality due to fabrication technique on material interface and the quality of crystal structure increases with increased thickness of GaN. GaN layer thickness may vary around 0.5 - 4 μm depending on the device design [25]–[27]. Materials with high electron conductivity such as Gold, Titanium, Nickel, Copper and Aluminum are used to deposit metal contacts. Source and drain contacts are deposited on top of the barrier layer by high temperature annealing to decrease electrical resistance of the contacts by increasing the absorption rate of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ during process, creating the Ohmic contacts. Gate contact is deposited by low temperature annealing to prevent absorption through barrier layer to increase resistance to create Schottky barrier. Generally gold is preferred as contact material to improve device performance [28]. A nitride or oxide passivation layer is deposited on barrier layer to prevent electron leakage during operation.

GaN and AlGaN layers are grown with a certain spontaneous polarity as given in Fig. 1.2. Growth of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ on GaN creates a compressive strain leading to a piezoelectric polarization. This polarity dominates device behavior and results in a net positive charge at AlGaN/GaN interface inside GaN channel as shown in Fig. 1.1. Any applied voltage difference between drain and source metal contacts generates an electron flow at the material interface inside this electron accumulated region, which is also called two-dimensional electron gas (2DEG) region.

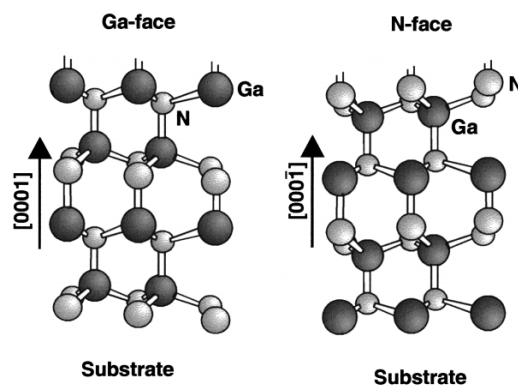


Figure 1.2. Schematic representation of Ga-face and N-face GaN crystal structure [29].

Formation of 2DEG can also be understood by investigating the energy band diagram of AlGaN/GaN HEMTs. As seen in Fig. 1.3, AlGaN and GaN layers form a unique junction due to their bandgap difference and polarizations, creating a quantum well at GaN side of the heterojunction. This difference of conduction band and Fermi level traps electrons moving from doped AlGaN into the GaN layer due to conduction energy band difference, causing 2DEG formation.

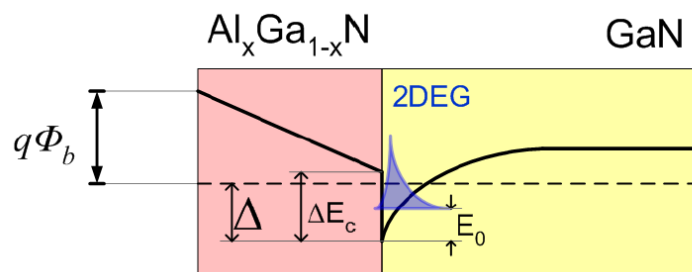


Figure 1.3. 2DEG formation due to energy band differences in AlGaN and GaN heterostructure. ϕ_b is barrier height, Δ is penetration of the conduction band below Fermi level and ΔE_c is conduction band offset. [30]

With an applied voltage difference between drain and source contacts (V_D), electrons in 2DEG region moves with almost no restriction. This condition, where no voltage difference between gate and source contacts (V_G) is applied, is considered as open channel condition. To manage the electron flow through the 2DEG, gate voltage can be adjusted independently from V_D . Applying a negative gate voltage ($V_G < 0$ V) decreases the energy difference between conduction band and Fermi level, creating a depletion region in the channel and leading to a decreased current in 2DEG. If the gate voltage is decreased further, electron flow can be restricted completely; putting the device into a “pinch-off” state. Thus, channel current is dependent both on V_D and V_G .

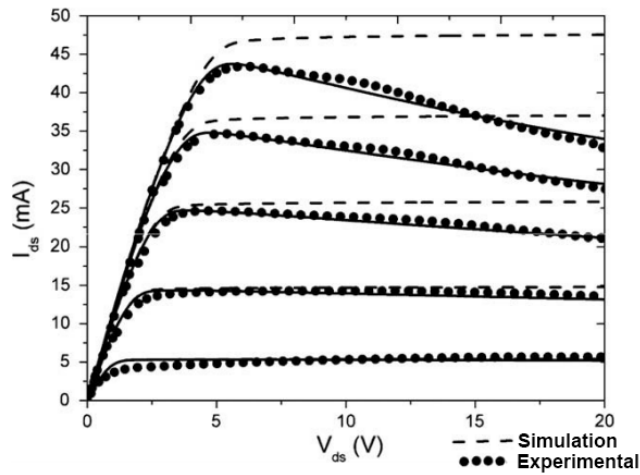


Figure 1.4. Device current and drain voltage (I_D - V_D) graph for different gate voltage values [31].

In Fig. 1.4, a device current vs. drain voltage (I_D - V_D) graph is given. Two main characteristics of I_D - V_D graph can be observed from this figure. First, device current decreases with decreasing gate voltage. As device reaches to pinch-off state, channel current decreases and after a certain threshold it completely shuts down. This decreases power output of the device since power is directly proportional to device current. Second, for constant gate voltage value, a linear behavior between device current and drain voltage can be observed until a certain drain voltage value. This region is regarded as linear region. If the drain voltage is further increased, device current saturates. Thus, this region is regarded as saturation region. The voltage required for saturation is called knee voltage, V_{knee} .

High power densities obtained from AlGaN/GaN HEMTs comes from the high rates of channel current during operation. Due to its wide bandgap, 3.49 eV, GaN can withstand high rates of applied electric field as the energy difference between valence and conduction bands are high, meaning the energy required to promote a valence electron to become a freely moving conduction electron is higher compared to other semiconductors. Moreover, due to their high electron mobility, electrons inside GaN channel layer can reach to high velocities under a strong electric field as shown in Fig. 1.5. High velocities combined with the high breakdown field results in a high saturation velocity, making AlGaN/GaN HEMTs more resistant against higher power outputs compared to other semiconductors as shown in Fig. 1.5.

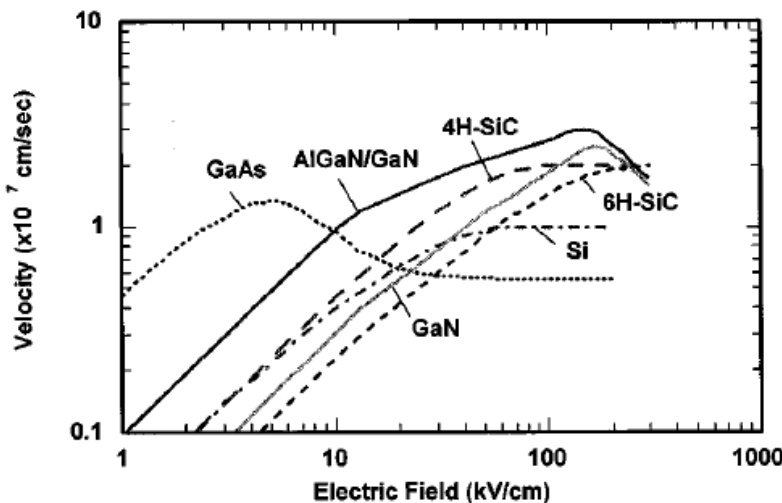


Figure 1.5. Carrier velocity according to electric field for AlGaN/GaN, GaAs, Si, 4H-SiC and 6H-SiC [32].

The saturation velocity strongly depends on temperature as shown in Fig. 1.6. Even though GaN has low electron scattering, increasing temperature increases electron scattering and decreases saturation velocity. During device operation, heat generation inside device channel occurs due to Joule heating. The amount of heat generation increases with increasing device power, leading to a decrease in device current and performance due to decreased carrier mobility. Thus, preventing temperature increase is

the key element to obtain high power density and efficiency. Carrier mobility behavior with increasing temperature is given in Fig. 1.6.

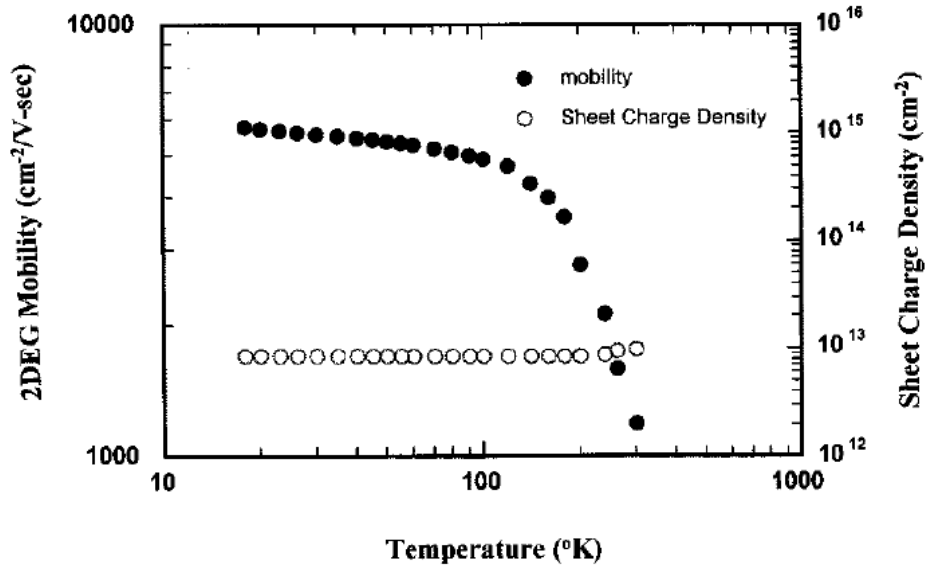


Figure 1.6. Carrier mobility dependency of AlGaIn/GaN on temperature [32].

1.2 Electrical and Thermal Degradation

Even though AlGaIn/GaN HEMTs provide promising outputs; electrical, mechanical, and thermal degradation mechanisms that define the reliability and mean-time-to-failure (MTTF) of such devices are still being investigated. As mentioned previously, one of the most important features of AlGaIn/GaN HEMTs is 2DEG formed by the electrons trapped at the interface of the AlGaIn/GaN heterostructure [24]. Electrons flowing through 2DEG are restricted by the applied gate voltage (V_G), that is responsible for the abrupt change of electrical field at the gate edge of 2DEG that can cause permanent current reduction due to strong piezoelectric effects and current collapse.

Permanent current reduction is caused by the electric field formed during the device operation which generates high rates of piezoelectric strain inside the device causing irreversible damage in long term usage [33]. High rates of piezoelectric stress defects the lattice structure of the device, creating new trap states. New trap states induced to the device reduces channel current by trapping electrons in a permanent way. Piezoelectric

stress is related to the applied gate voltage, hence for different gate-biasing conditions reliability of the device may change significantly. AlGaN/GaN HEMTs have a threshold gate voltage value where time-to-failure (TFF) is lowest compared to other gate-bias conditions. In Fig. 1.7, a typical graph for gate voltage dependence of time-to-failure is given for various drain voltages. At open channel condition, electrons accelerated by the strong electric field are injected towards AlGaN/GaN interface, in either AlGaN or SiN passivation layer to be trapped permanently in the generated trap states. Moreover, with increasing power output, energy of hot electrons in the channel increases; resulting in an increase in electron injection rate. Therefore, taking biasing condition into account while analyzing AlGaN/GaN HEMT reliability has a great importance to improve HEMT designs. Their reliability is highly dependent on operating conditions throughout their lifespan.

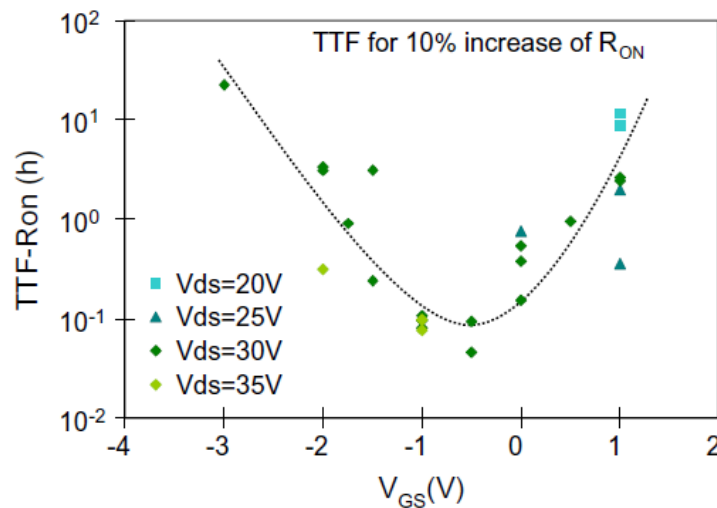


Figure 1.7. Gate voltage, V_G , dependency of time-to-failure (TFF) for AlGaN/GaN HEMTs [34].

On the other side, current collapse causes a temporary reduction in the electron flow caused by the trapped electrons inside the already existing traps [30]. Even though it is not permanent, current collapse can affect the device up to several weeks and cause major power loss inside the device by decreasing saturation current and increasing knee voltage [35]. Already existing material defects act as trap states inside crystalline structure resulting in current collapse. Another mechanism effecting device performance is

electron leakage, which is the unintended flow of electrons from 2DEG to electrical contacts. Since electrons escape from device channel during leakage, device current and power output decreases significantly if electron leakage is not prevented. Deposition of a passivation layer can both reduce current collapse and electron leakage.

In Fig. 1.8, a summary of device failure mechanisms for AlGa_N/Ga_N HEMTs is given. Different areas inside the device are prone to different failure mechanisms as explained previously. Each of these mechanism are created by either electrical or thermal effects. Electrical failure mechanism consists of current collapse and permanent device degradation, which are both trap related effects. In both phenomena, degradation is caused by the trap states, either created from the deformation of the device due to piezoelectric strains or already existing traps.

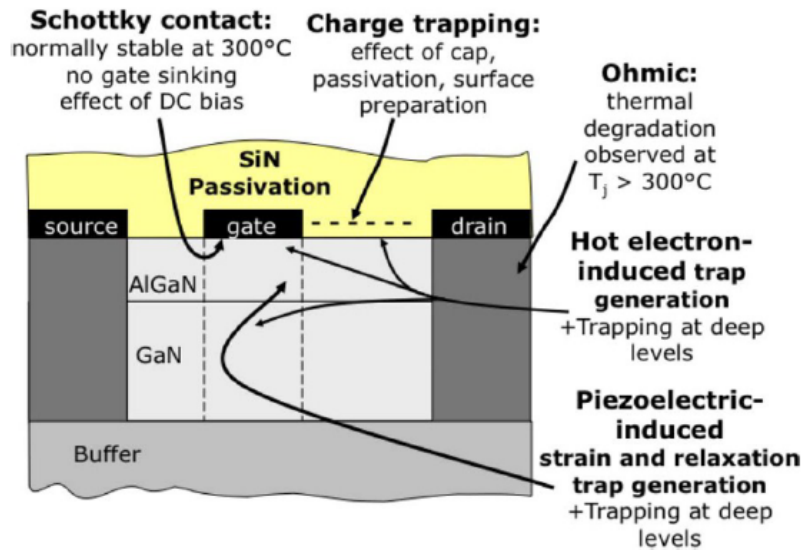


Figure 1.8. Summary of device failure mechanisms in AlGa_N/Ga_N HEMTs. [25]

While permanent device degradation and current collapse are major factors that affect reliability, they are strongly affected by device temperature. Thus, thermal management of Ga_N HEMTs does not only effect the reliability of the device, but also its performance. As a gate voltage is applied to the device, electron flow inside 2DEG becomes restricted creating a local high resistance region. This resistance causes sudden changes of the electrical field, thus high and localized Joule heating in the same region. Joule heating is

caused by the energy dissipated from carriers to the lattice, increasing lattice temperature. This localized region is called the “hotspot” and can be treated as a highly localized heat generation region [36], [37]. Hotspot formation is considered as one of the main reasons for reduction of device performance and failure for GaN HEMTs since it effects mechanical stresses, chemical reactions, and electron transport properties [38], [39].

Hotspot is located in 2DEG, where electron flow occurs, at the drain side of the gate contact as seen in Fig. 1.9. High rates of change in electrical field is generated at depletion region, depending on the gate voltage. Hot electrons flowing through channel gets accelerated by the applied drain and gate voltage, generating localized Joule heating inside the device. As the operation frequency of AlGaN/GaN HEMTs are low, device reliability problems significantly decrease by reduced hotspot temperature. Mean time-to-failure (MTTF) is obtained to be 10^6 and 10^7 hours for 450 K and 500 K operation

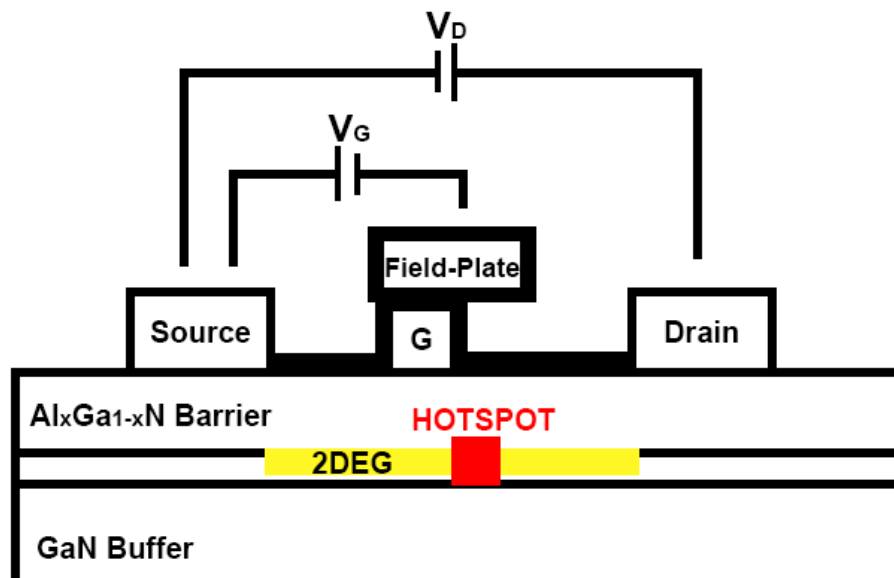


Figure 1.9. AlGaN/GaN HEMT schematic showing 2DEG region and hotspot formation.

temperature. However, with increased hotspot temperature during space and military applications, MTTF decreases significantly.

1.3 Current Technology & Reliability

Different techniques have been analyzed over last decade to overcome these failure mechanisms and increase overall device reliability. The main solution to reliability problems was to regulate non-uniform distribution of the electric field in 2DEG region, which is triggering many degradation mechanisms and limiting the voltage performance of AlGaIn/GaN HEMTs. Two main technologies to increase reliability by decreasing electron leakage, current collapse, and device degradation are field-plate and passivation layer.

1.3.1 Field-Plate

By the implementation of the field-plate technology, higher breakdown voltage performance is obtained [8]. Source and gate connected field plates with different sizes [8] and shapes [7], [15] are examined to reduce and spread the electric field in the 2DEG region [40]. Both in source and gate connected field-plate applications, field-plate introduces an additional metallization contact layer to the device allowing the modification of some electrical properties of HEMT, such as electric field distribution, electron leakage from channel, and breakdown voltage.

Electrical effects of the field-plates and passivation on the performance of AlGaIn/GaN HEMTs have been significantly investigated in the past [41]. Y. F. Wu et al. [35] used and optimized field-plates to enhance radio frequency (RF) current-voltage swings by reducing trapping effects and increasing breakdown voltage. 32.2 W/mm continuous wave output power density is achieved by implementing field-plate to the device compared to 12 W/mm obtained by conventional gate GaN HEMT. C. Y. Chiang et al. [40] obtained an improved 160 V breakdown voltage by using field-plate compared to 90 V with conventional gate structure. All those improvements are obtained with an acceptable compromise in device gain due to regulated electric field. V. Palankovski et al. [8] simulated AlGaIn/GaN HEMTs with different gate and field-plate lengths to

optimize electrical performance and reliability of the device. A two-dimensional model, is used to obtain the effect of field-plate on electric field distribution and the research is only focused on electrical effects.

Even though significant improvements have been made in electrical enhancement of field-plates, an analytical study on their thermal effects, regarding a combined electro-thermal study, are still missing in the literature. As explained in previous section, device failure mechanisms are highly dependent on device temperature, hence analyzing the thermal effects of field-plates are critical to improve performance and reliability.

1.3.2 Passivation

On the other hand, electron leakage from channel is reduced by creating high density shallow traps at the device surface and minimizing the formation of virtual gate, hence eliminating gate-lag. Variety of different nitride and oxide passivation materials are tested, to minimize electron leakage and improve device performance by preventing device degradation and current collapse.

Similar to the research on field-plates, electrical effects of passivation layer are also broadly studied in literature. S. Huang et al. [42] prevented significant current collapse occurring inside AlGa_N/Ga_N HEMT by using AlN thin film passivation grown by plasma-enhanced atomic layer deposition (PEALD). Fig. 1.11 shows the effect of applied passivation layer where in Fig. 1.11(a) the output current is significantly lower for high gate-biasing conditions indicating current collapse. After the application of AlN passivation layer shown in Fig 1.11(b), current collapse is prevented by reducing electron leakage from channel. V. Tilak et al. [43] obtained 1 W/mm power density increase in AlGa_N/Ga_N HEMT operating at 4 GHz, 20 V bias condition, from 1.3 W/mm to 2.3 W/mm, by deposition of a thin layer of SiN using plasma enhanced chemical vapor deposition (PECVD). M. Gassoumi et al. [44] reported significant enhancement from DC measurements in AlGa_N/Ga_N HEMT performance by using SiN/SiO₂ passivation layers along with some minor disadvantages as decreased electron mobility and saturation current for high drain voltages. In their study, improvement obtained in device

performance is related to the surface states as explained in the previous section. N. Ramanan et al. [45] investigated the effect of SiO₂ passivation layer on virtual gate phenomena and gate lag in AlGa_N/Ga_N HEMTs. A simple simulation framework is generated to observe these effects and a decrease in virtual gate formation and gate-lag is observed. In another study, Y. Pei et al. [26] proposed a model to observe the effect of SiN_x passivation layer thickness to prove DC-RF dispersion dependency not only on surface passivation, but also on SiN_x passivation thickness. W. S. Tan et al. [46] compared Si₃N₄, SiO₂, SiO, and unpassivated devices to obtain their effects on electron leakage. They demonstrated that SiO₂ is a good alternative as surface passivation even though Si₃N₄ gives the best performance in device current as seen in Fig 1.10.

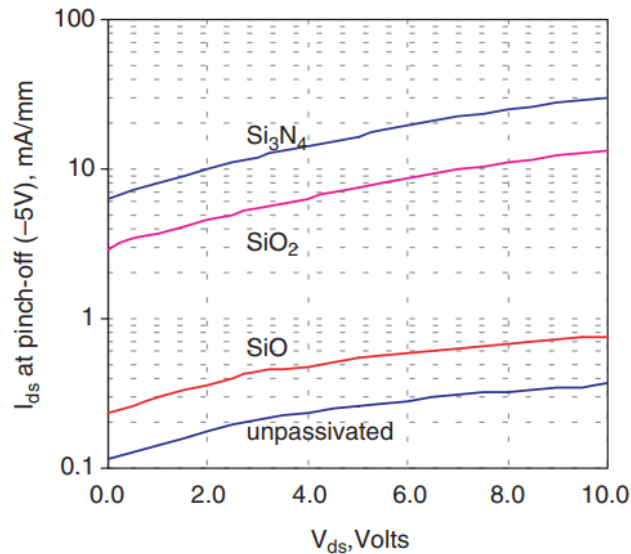


Figure 1.10. Device current versus drain voltage under pinch-off conditions ($V_G = -5$ V) for devices with Si₃N₄, SiO₂, SiO passivation layers and unpassivated device obtained by W. S. Tan et al. [46]

Type and thickness of the passivation layer also has an importance on field-plate utilization for AlGa_N/Ga_N HEMTs. Material properties and thickness of passivation layer should be analyzed considering the field-plate effect inside device channel to obtain optimal device performance and reliability. As thermal studies on passivation layer, a research to analyze combined passivation and field-plate effects on AlGa_N/Ga_N HEMTs are also lacking in literature.

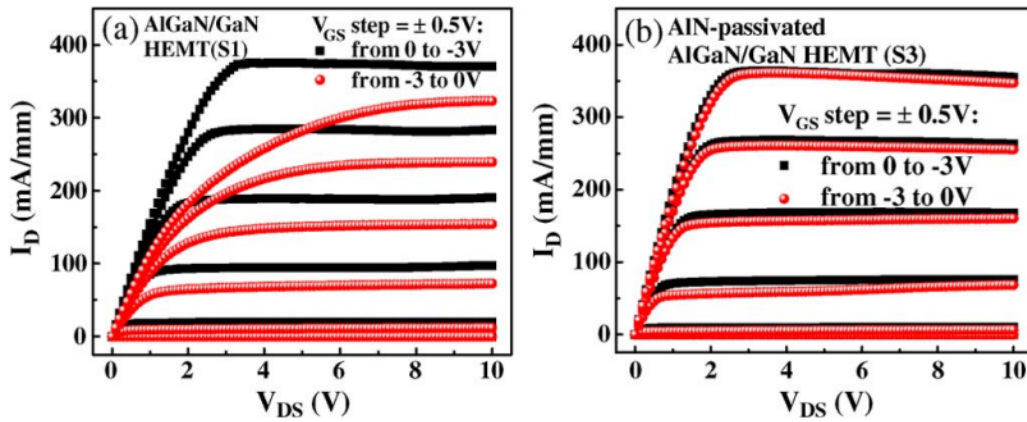


Figure 1.11. I_d - V_d characteristics of AlGaIn/GaN HEMTs representing (a) current drop indicating current collapse without AlN passivation applied, (b) reduced electron leakage with AlN passivation applied [42].

1.4 Thermal Studies of Field-Plates & Passivation

As discussed previously, reliability and performance of the devices are not only dependent on electrical effects but also the thermal side effects, so such structures should be analyzed in detail with a combined electro-thermal perspective. Although significant effort has been made to characterize their effects on device electric field distribution, breakdown voltage, and current-voltage characteristics; little has been done to understand their combined thermo-electric effects. Since any change in electrical field will also alter the Joule heating distribution in the device that is expected to affect the device temperatures.

Another issue about analysis of AlGaIn/GaN HEMTs is the lack of case variety and combined effect for these reliability solutions. Less experimental results can be obtained on maximum temperature of GaN HEMTs due to high cost and time requirements; whereas by conducting precise simulations, different outputs of devices with various geometrical and biasing conditions can be obtained and analyzed in a much more efficient way. Today even the most advanced thermal imaging techniques have low spatial resolutions compared to the hotspot size, thus experimental techniques may not be adequate to measure true maximum temperature of GaN HEMTs. Even widely preferred

experimental techniques such as infrared cameras, micro-Raman thermography, transient thermo-reflectance, liquid crystal thermography and photoluminescence are limited in spatial and/or temperature resolution while being budget and time consuming. A thermal imaging example for thermo-reflectance and infrared techniques are given in Fig 1.12. Although experimentation is critical to validate numerical and analytical methods, a well optimized and validated model can simulate various devices with different biasing conditions, material properties and geometrical dimensions in a much more cost and time efficient way. Moreover, especially in the case of AlGaIn/GaN HEMTs, more detailed and precise outputs about device performance can be obtained using analytical methods compared to relatively low resolution experimentation techniques. In addition, with increasing computational power, solving more complicated simulations with complex boundary conditions are getting easier and faster each day.

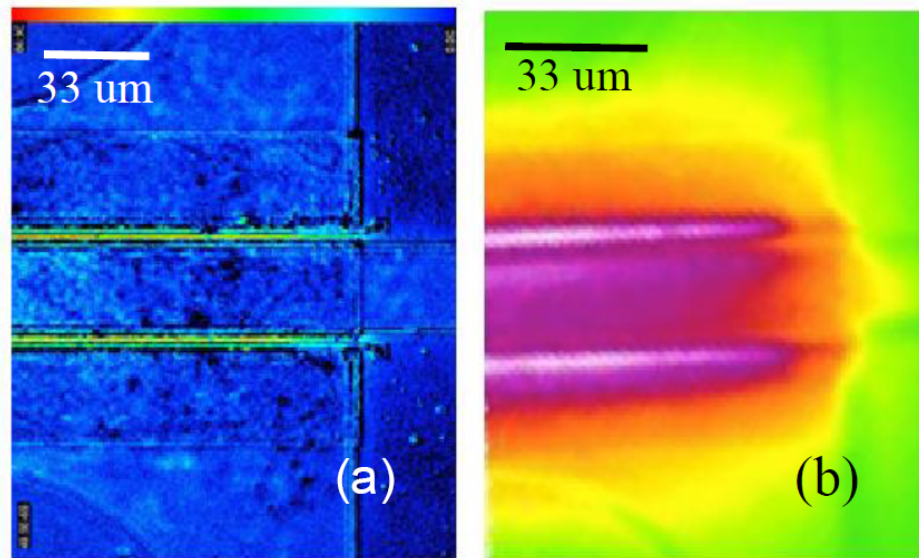


Figure 1.12. Color scale thermal image of (a) thermo-reflectance and (b) infrared techniques.

Several numerical and analytical models exist in literature, M. Darwish et al. [47] presented an analytical model to calculate thermal resistance of AlGaIn/GaN on SiC substrate. In this study, analytical model was validated using a numerical simulation conducted in ANSYS and comparing the results with experimentation data obtained from Kubal et al. [48]. Nearly 200 cases with varying substrate thickness, gate pitch, gate width

and gate length are analyzed proving the time and cost efficiency of validated numerical and analytical simulations. However, effect of gate-biasing condition on heat generation is neglected and model is generated solely in thermal perspective. D. P. Wang et al. [24] created a numerical simulation to observe the effects of temperature on polarization and conduction band offset in heterojunction and validated their findings with experimental data, but focused only on electrical outcomes.

To solve the reliability problem, similar studies are conducted for different field-plate technologies and passivation applications. A. Prejis et al. [49] showed the effects of non-linear thermal resistance modelling to simulate self-heating of field-plated GaN HEMT on SiC substrate systems by coupling the model with IR spectroscopy measurements as shown in Fig. 1.13. A more recent analytical study that investigates the thermal side effects of a source connected field plate on a device operating at different biasing conditions [50]. Experimentally calibrated combined electrical and thermal model predicts that DC and RF operations acts similar under 50 V of drain voltage. For higher drain voltage values, such as 100 V, 9% temperature difference between two conditions is obtained. Even though both of the simulated devices in these researches are field-plated, the effect of field plate was not the focus of the study and its effects are not analyzed. A combined electro-thermal study to investigate the effects of gate connected field plates with varying geometrical properties and bias conditions is still missing in literature.

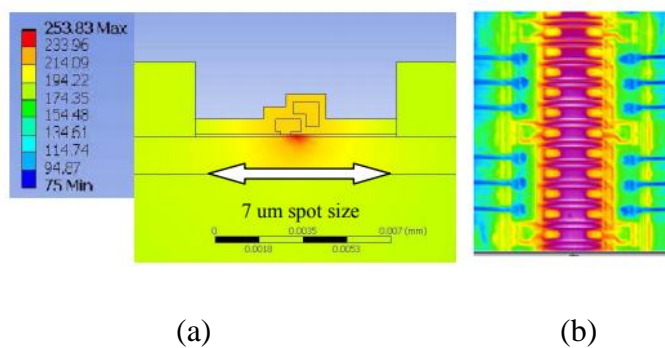


Figure 1.13. (a) Thermal profile obtained by simulations near device channel and (b) IR measurement image from GaN HEMT obtained by A. Prejis et al. [49]

For passivation layers very limited amount of thermal analysis are studied in literature. A. Haghshenas et al. [51] used an analytical method to model the effect of SiO₂ and Si₃N₄ surface passivation on self-heating of AlGaIn/GaN HEMTs. They analyzed the thermal resistance effect of surface passivation layer for a single device operating under single biasing condition. A. Prakash et al. [52] used a combined electro-thermal-mechanical simulation to observe the effects of SiO₂ surface passivation on GaN HEMTs. Even though thermal effects are included in this study, they are used to obtain electrical outputs of surface passivation without explaining its effect on self-heating characteristics.

These researches focus either only on electrical outcomes of surface passivation while neglecting thermal effects or doesn't focus on the effects of field-plate and passivation on thermal characteristics. A study that contains both electrical and thermal perspectives is essential to observe the effects of passivation layer in a broad sense. Moreover, the combined effect of field-plate and passivation should also be analyzed since they will both induce different electrical and thermal resistances on each other.

1.5 Motivation

As stated in previous section, a variety of research on different technologies were investigated to increase AlGaIn/GaN HEMT reliability. Increasing AlGaIn/GaN reliability is the key element in improving device performance for automotive, military and space applications. However, wide range of these studies were either focused on electrical performance or thermal optimization of the devices. Many research in literature either neglect the effect of biasing condition on heat generation and assume uniform heating while observing the thermal effects of field-plate and passivation layer, or focus on the electrical outcomes of devices with different biasing conditions without taking the thermal effects into account. Moreover, experimental studies are not sufficient to present large amounts of data about AlGaIn/GaN HEMT performance due to their high cost and time requirements while obtaining true hotspot temperature inside device channel is not possible with current experimental technology due to low resolution. Thus, a combined electro-thermal analytical and numerical approach to analyze inter-dynamics of field-plate and passivation technologies is much required to observe the true effects and

optimize devices to obtain reliable devices with high power density and efficiency. For this reason, validated analytical and numerical simulations are need to be used in order to be time and cost efficient. In this study electrical and thermal simulations are conducted to analyze separate effects of field-plate and passivation layer, as well as combined effects to optimize device performance and increase reliability.

1.6 Outline of Thesis

This thesis consists of three main parts. Chapter 2 explains the methodology used to create electrical and thermal simulations in two sections. Device geometry and boundary conditions are defined in this chapter. Electrical simulation section covers the electron transport model used to simulate carrier physics along with used parameters and boundary conditions. Furthermore, obtaining device power density output, electric field distribution and Joule heating inside channel is discussed in this part. Secondly in thermal simulation section, boundary conditions used to define thermal parameters and numerical analysis details are discussed.

Chapter 3 covers the combined electro-thermal effects of gate field-plates, in three sections. Effects of biasing condition for field-plated and I-gate devices are analyzed in section one, in which devices with and without field-plate are simulated to obtain electrical and thermal results. Field-plate effect on breakdown voltage, power output, electric field distribution and Joule heating is obtained in this section. In second section, similar analysis are done on same power output devices to obtain hotspot temperature and temperature distribution along with power density, electric field distribution, and breakdown voltage of the devices. Same study is also conducted for various field-plate lengths to acquire more information about field-plate length optimization in last section.

In chapter 4, electro-thermal effects of passivation layer is investigated. Different passivation materials are analyzed in various thicknesses to obtain its effect on breakdown voltage, electron leakage, power output, and electric field and heat generation distributions. Moreover, passivation thickness optimization in order to decrease thermal

resistance and increase the electro-thermal effects of field-plate is discussed in this chapter.

Final part of this thesis, Chapter 5, concludes the findings obtained throughout this research and discusses future research directions.

CHAPTER 2

METHODOLOGY

As explained in chapter 1, analytical and numerical methods are needed to study and optimize device performance to increase reliability. By using such methods, large number of outputs can be obtained and analyzed. This is neither practical, nor cheap with experimental techniques. Furthermore, obtaining precise information about inner device phenomenon such as true hotspot temperature is not possible due to limitations of current experimentation technologies. Yet, with a validated electro-thermal model, any precise information about device physics can be attained for various biasing conditions, geometrical dimensions and material properties.

To prepare a complete model, drawbacks of previous analytical and numerical solutions should be well analyzed. In the past, while some researchers assumed constant temperature through the device channel to obtain electrical performance, some conducted thermal simulations without considering the effect of biasing conditions. Yet, it is known that channel heat generation distribution is dependent on biasing condition. Electron transport inside the channel and any related phenomena has a significant impact on Joule heating. Coupled electrical and thermal simulations should be employed to imitate real operating conditions. For this purpose, 2D and 3D models are generated respectively for

electrical and thermal simulations in this study, which will be explained in detail through following sections.

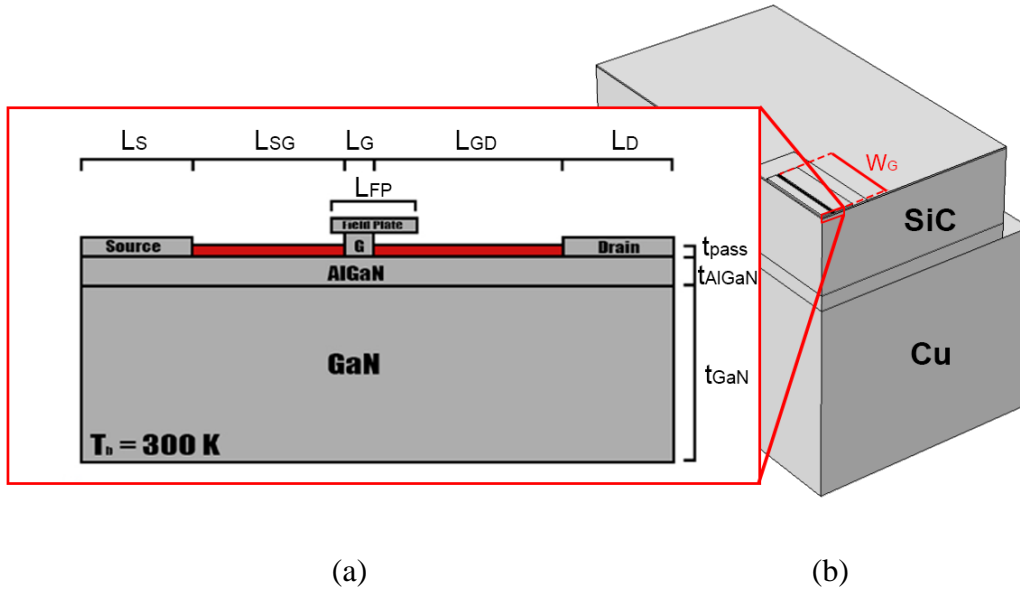


Figure 2.1. Model schematic used in (a) 2D electrical simulations and (b) 3D thermal simulations for 2 finger devices.

AlGaIn/GaN HEMT investigated in this research is illustrated in Fig. 2.1. Fig. 2.1(b) shows the 3D quarter model of the two finger device used in thermal simulations and the zoomed-in inset represented in Fig. 2.1(a) illustrates the 2D model used for the electrical simulations. 3D models are preferred in thermal simulations to include the effect of spreading thermal resistance and obtain the true hotspot temperature compared to experimental results with fairly low resolutions. On the other hand, 2D model is used for electrical simulations with the assumption of infinite gate, since channel length ($L_{SG}+L_G+L_{GD} = 4 \mu\text{m}$) is small compared to gate width ($W_G = 100 \mu\text{m}$), to avoid high computational requirements.

In these simulations; AlGaIn thickness of $t_{\text{AlGaIn}} = 20 \text{ nm}$, GaN thickness of $t_{\text{GaN}} = 2 \mu\text{m}$, AlN interlayer thickness of $t_{\text{AlN}} = 200 \text{ nm}$ and SiC substrate layer thickness of $t_{\text{SiC}} = 98 \mu\text{m}$ is used. To bond the die with packaging, $20 \mu\text{m}$ thick epoxy is modelled and CuW is

selected as the packaging material. Drain and source contact lengths of $L_D = L_S = 34 \mu\text{m}$ and gate length of $L_G = 600 \text{ nm}$ is defined and metal contacts are selected to be Gold. Source gate separation of $L_{SG} = 1 \mu\text{m}$, gate drain separation of $L_{GD} = 2.4 \mu\text{m}$ and total die length of $L_{\text{device}} = 520 \mu\text{m}$ is used. While in electrical simulations only the single finger of the device is modeled under the assumption that the electrical effects of neighboring fingers are negligible, in thermal simulations devices with 2 to 6 fingers are simulated to mimic commercial AlGaIn/GaN HEMTs. In 6 finger device configuration, HEMTs with 6 gate contacts are used on a single die as shown in Fig. 2.2.

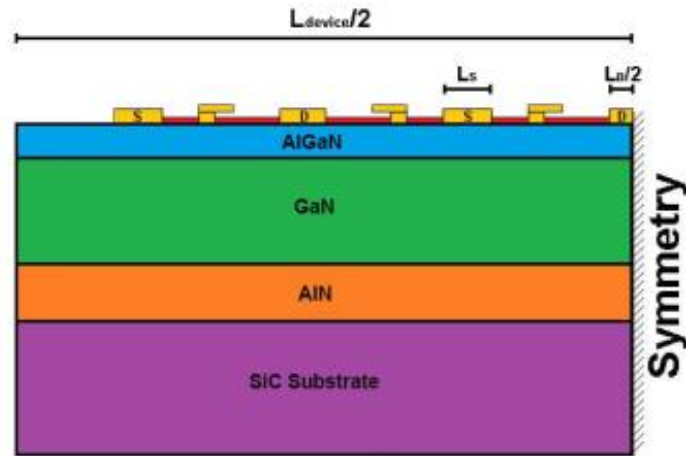


Figure 2.2. 2D schematic of half model used to simulate 6-finger AlGaIn/GaN HEMTs.

Power output, electrical field distributions and Joule heating data are going to be acquired from electrical simulations and Joule heating data obtained is going to be used as input function to thermal simulation in order to obtain temperature distribution and maximum temperature inside the device. In the following sections electrical and thermal simulations are explained in detail.

2.1 Electrical Simulations

Detailed electrical simulations are performed using Sentaurus TCAD; a commercial computer simulation program used to develop and optimize the semiconductor processing technologies and devices. In these simulations, a hydrodynamic transport model is generated to simulate electron transport and applied as system physics. While scale of state-of-art semiconductor technologies getting smaller every day, internal and external characteristics of devices cannot be analyzed truly by using drift-diffusion transport model. Velocity overshoot cannot be taken into account while using drift-diffusion equations and impact ionization generation is generally overestimated. On the other hand, using the Monte Carlo method to solve Boltzmann Kinetic equations may be the ideal approach, however; it cannot be used for cases where large numbers of simulations are needed to be conducted due to high time and computational requirements.

Hydrodynamic transport model is preferred when more complex solutions are required compared to drift-diffusion equations and there is a time constraint to obtain large amounts of data. This transport model is the simultaneous solution of six partial differential equations (PDEs). These equations are Poisson equation, continuity equations for electrons and holes, and the energy conservation equations for electrons, holes and lattice.

The Poisson equation is:

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap} \quad (2.1)$$

where ε is electrical permittivity, q is elementary electron charge, n and p are electron charge densities, N_D and N_A are concentration of ionized donor and acceptors respectively, and ρ_{trap} is fixed charge and trap charge density.

Electron and hole continuity equations are:

$$\nabla \cdot \vec{J}_n = qR_{net} + q \frac{\delta n}{\delta t} \quad - \nabla \cdot \vec{J}_p = qR_{net} + q \frac{\delta p}{\delta t} \quad (2.2)$$

where \vec{J}_n and \vec{J}_p are electron and hole current densities respectively, and R_{net} is the net electron-hole recombination rate.

In drift-diffusion transport model, current densities of electrons and holes are:

$$\nabla \cdot \vec{J}_n = -nq\mu_n \nabla \Phi_n \quad (2.3)$$

$$\nabla \cdot \vec{J}_p = -nq\mu_p \nabla \Phi_p \quad (2.4)$$

where μ_n and μ_p are mobility values, Φ_n and Φ_p are quasi-Fermi potentials of electrons and holes respectively. However in hydrodynamic transport model, carrier temperatures for electrons T_n and holes T_p are taken into account independent of lattice temperature T . So in hydrodynamic transport model, electron and hole current densities are defined as:

$$\vec{J}_n = q\mu_n(n\nabla E_C + kT_n \nabla n + f_n^{td} kn \nabla T_n - 1.5nkT_n \nabla \ln m_n) \quad (2.5)$$

$$\vec{J}_p = q\mu_p(p\nabla E_V + kT_p \nabla p + f_p^{td} kp \nabla T_p - 1.5pkT_p \nabla \ln m_p) \quad (2.6)$$

where $q\mu_n n \nabla E_C$ and $q\mu_p p \nabla E_V$ terms are contributions of spatial variations of bandgap, electrostatic potential and electron affinity. Remaining terms are related to gradient of concentration, carrier temperature gradient and spatial variations of effective electron and hole masses m_n and m_p . E_C and E_V are conduction and valence band energies and terms f_n^{td} and f_p^{td} are parameter variables to optimize simulation performance. Parameter variables can be adjusted to fit numerical results with experimental data by effecting velocity distribution inside semiconductor device.

Three remaining equations solved in hydrodynamic transport model are energy balance equations for electrons, holes and lattice:

$$\frac{\delta W_n}{\delta t} + \nabla \cdot \vec{S}_n = \vec{J}_n \cdot \nabla E_C + \frac{dW_n}{dt}_{col} \quad (2.7)$$

$$\frac{\delta W_p}{\delta t} + \nabla \vec{S}_p = \vec{J}_p \cdot \nabla E_V + \frac{dW_p}{dt}_{col} \quad (2.8)$$

$$\frac{\delta W_L}{\delta t} + \nabla \vec{S}_L = \frac{dW_L}{dt}_{col} \quad (2.9)$$

where the following energy fluxes are:

$$\vec{S}_n = -\frac{5r_n}{2} \left(\frac{kT_n}{q} \vec{J}_n + f_n^{hf} \left(\frac{k^2}{q} n\mu_n T_n \right) \nabla T_n \right) \quad (2.10)$$

$$\vec{S}_p = -\frac{5r_p}{2} \left(\frac{kT_p}{q} \vec{J}_p + f_p^{hf} \left(\frac{k^2}{q} n\mu_p T_p \right) \nabla T_p \right) \quad (2.11)$$

$$\vec{S}_L = -\kappa_L \nabla T_L \quad (2.12)$$

Terms r_n , r_p , f_n^{hf} and f_p^{hf} are parametric variables and can be adjusted to change convective and diffusive contributions inside the transport model. In eq. 2.12, κ_L represents lattice diffusive thermal conductivity. The diffusive thermal conductivity terms for electrons and holes are $\left(\frac{k^2}{q} n\mu_n T_n \right)$ and $\left(\frac{k^2}{q} n\mu_p T_p \right)$ respectively.

Thermal and electrical boundary conditions defined in hydrodynamic model are crucial to obtain accurate results from simulations. Boundary conditions of metal contacts such as source, drain and gate are priority in defining electrical boundary conditions. Gate contact is defined as a Schottky contact. This electrical boundary condition is dependent on three equations as:

$$\phi = \phi_F - \Phi_B + \frac{kT}{q} \ln \left(\frac{N_C}{n_{i,eff}} \right) \quad (2.13)$$

$$\vec{J}_n \cdot \hat{n} = qv_n(n - n_0^B) \quad \vec{J}_p \cdot \hat{n} = -qv_p(p - p_0^B) \quad (2.14)$$

$$n_0^B = N_C \exp \left(\frac{-q\Phi_B}{kt} \right) \quad p_0^B = N_V \exp \left(\frac{-E_{g,eff} + q\Phi_B}{kt} \right) \quad (2.15)$$

where ϕ_F is the Fermi potential, Φ_B is the barrier height, v_n and v_p are thermionic emission velocities, and n_0^B and p_0^B are equilibrium densities. In this study, $\Phi_B = 1.48$ eV, $v_n = 2.573 \times 10^6$ cm/s $v_p = 1.93 \times 10^6$ cm/s are used to define gate contact with initial voltage value of $V_{ini} = 0$ V. Whereas, source and drain are defined as resistive contacts and resistivity $R = 4 \Omega\mu\text{m}$ is defined in order to conduct 2D simulations. Acceptor and donor type traps are defined for materials and interfaces.

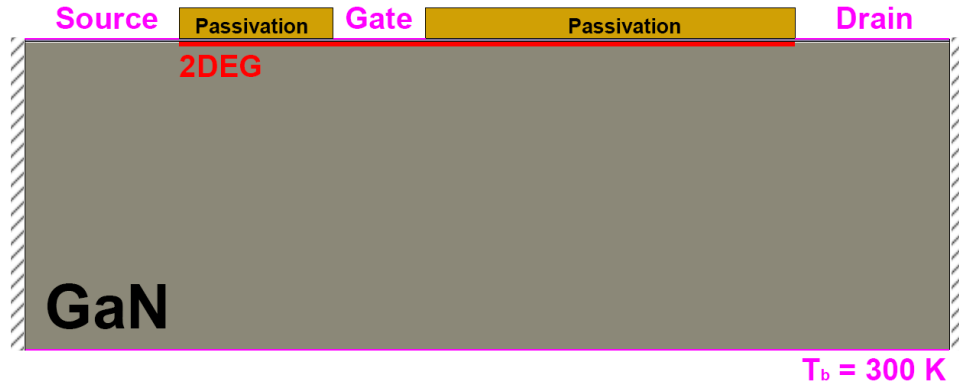


Figure 2.3. Device geometry used in electrical simulations.

As material properties; temperature dependent dielectric constant, lattice heat capacity, thermal conductivity, energy relaxation time, thermal diffusion factor, avalanche factors, bandgap, mobility, doping dependence, recombination and generation models are defined for AlGaN and GaN to support hydrodynamic transport model. DC operating conditions are preferred for electrical simulations. Although when V_D is higher than 50 V, such as 100 V, temperature differences around 6-10% for DC and RF simulations are expected,

for drain voltages used in our case which are lower than 50 V, DC simulations predict similar channel temperatures with RF results as given in Fig 2.4 [50].

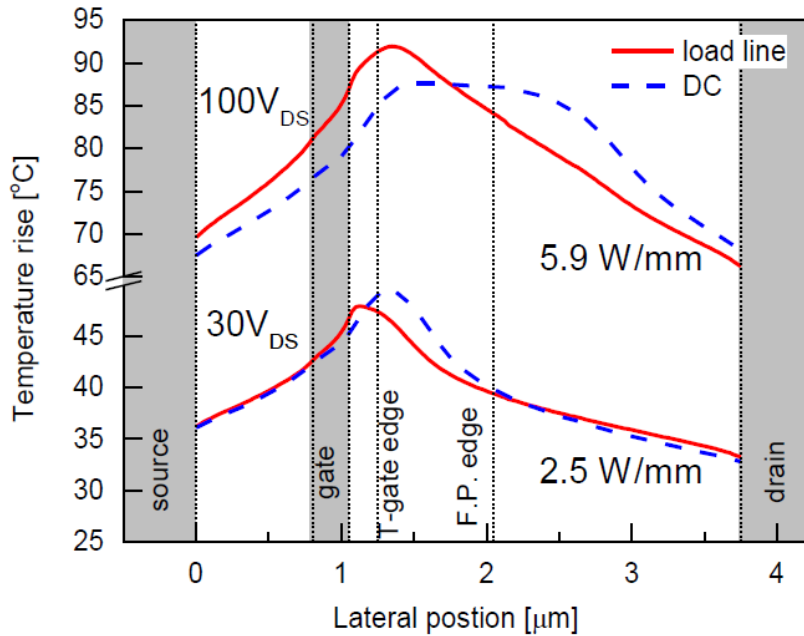


Figure 2.4. DC analysis comparison for devices operating at $V_D = 30$ and 100 V with power density 2.5 W/mm and 5.9 W/mm respectively. [50]

Device geometry is created by using dimensions given in the previous section as shown in Fig 2.3. Meshing has a great importance to obtain accurate results. However, if the model is meshed too fine computational requirements increases dramatically. So meshing

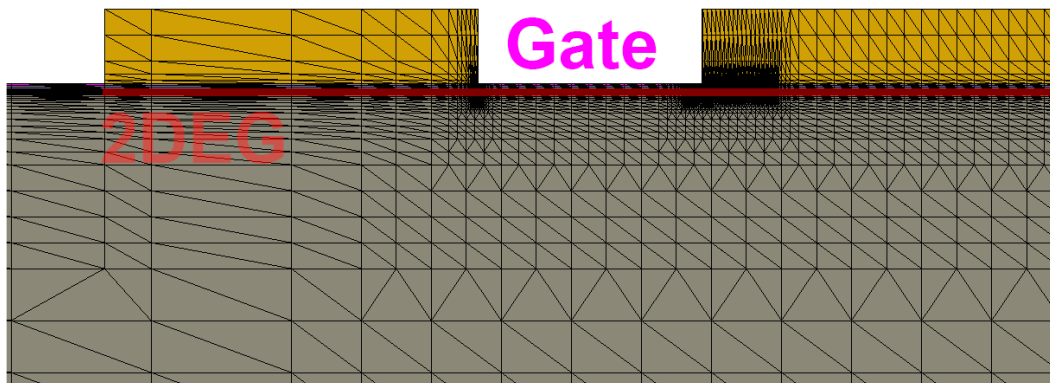


Figure 2.5. Close-up meshing of the electrical simulation model.

should be localized in critical regions such as 2DEG, gate, and field-plate edge where electron transport and heat generation due to resistance occurs. A close-up figure showing the meshing used in electrical simulations is given in Fig 2.5.

After the geometry is created, material properties are defined and device physics are set; device simulation is operated by first ramping gate voltage to the desired bias condition and then increasing drain voltage step-by-step to increase channel current. After the simulation is complete, various outputs can be obtained such as operation current, power density, electric field distribution, electron velocity, potential, Joule heating, and heat flux distribution.

In Fig. 2.6, I_D - V_D graph obtained from simulation and experimentation at partially pinched-off ($V_G = -2.5$ V) condition is given. Experimental data is obtained from AlGaIn/GaN HEMTs fabricated in NANOTAM research center. Dimensions of fabricated device are identical to model geometry. Power density, knee voltage, and breakdown voltage of simulation results should be fitted to experimental data in order to

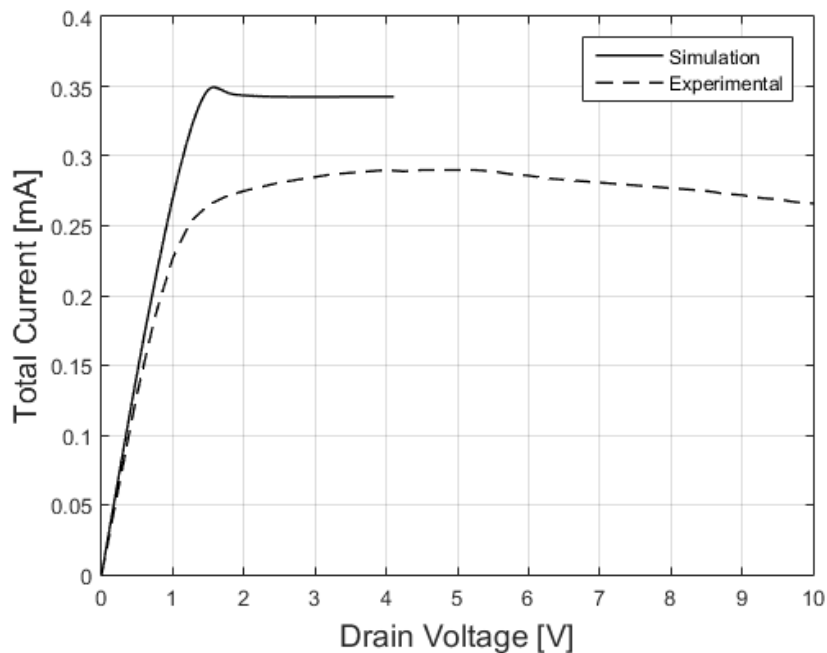


Figure 2.6. I_D - V_D comparison of simulation result with experimental data for AlGaIn/GaN HEMTs operating at $V_G = -2.5$ V and $V_D = 10$ V.

obtain accurate outputs imitating real device operation. Electron mobility, saturation velocity, trap distribution and concentration directly affect power density, knee voltage, and breakdown voltage, hence, can be altered to fit simulation results. Decreasing the electron mobility decreases velocity of electrons inside semiconductors and leads to a decreased slope in linear region of I_D - V_D graph. Changing the saturation velocity effects saturation current of the device. Power density of the simulation can be fit to the experimental results by decreasing the saturation velocity, hence, decreasing power density of the simulation. Lastly, doped semiconductors have impurities inside their crystal structure. These impurities may be implemented intentionally to increase the number of free carriers and adjust channel current and power output of the device. By changing trap density, concentration of impurities can be changed to increase or decrease channel current. By adjusting these three parameters, simulation is adjusted to give similar results with fabricated AlGaIn/GaN HEMT. In Fig. 2.7(a) effect of electron mobility and saturation velocity on channel current is given in an I_D - V_D graph. Decreasing the saturation velocity decreased saturation current inside the device to fit power density level and decreasing the electron mobility increased knee voltage of the device. In Fig. 2.7(b) a comparison of fitted simulation I_D - V_D result with experimental data for $V_G = -2.5$ V and $V_D = 10$ V is given.

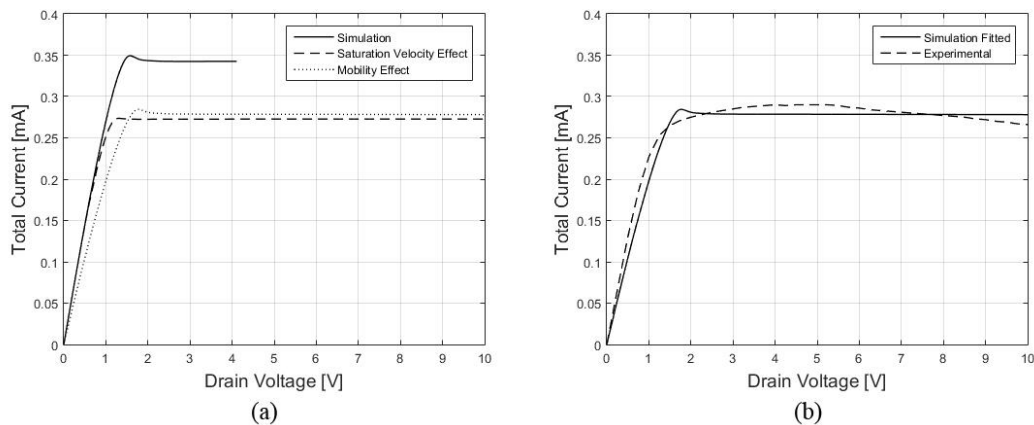


Figure 2.7. I_D - V_D graph showing (a) effect of electron mobility and saturation velocity on device current and (b) fitted simulation result compared to experimental graph.

To fit the simulation results, electron mobility equations are adjusted to:

$$\mu_e = 1375 \left(\frac{T}{300} \right)^{-1} \quad (2.16)$$

$$\mu_h = 170 \left(\frac{T}{300} \right)^{-2.1} \text{ W/mK} \quad (2.17)$$

for electrons and holes respectively in GaN layer. Similarly, saturation velocities of 1×10^7 and 1.6×10^7 are used for electrons and holes. Once the fitting process is completed, no other adjustment is necessary since results obtained for different biasing conditions are accurate in general.

After the simulation results are fitted and model is validated, electrical field distribution and Joule heating data are extracted in 2D from electrical simulation by using a Linux script. Electric field distribution inside the device is analyzed to observe the electrical effects of used technology.

On the other hand, extracted 2D heat generation data is post-processed to be used as surface heat flux in thermal simulations. Obtained 2D heat generation is given as contour in Fig. 2.8 (b), by integrating this data along its thickness using MATLAB, linear heat generation function can be obtained as given in Fig. 2.9 (b). Using a 1D heat generation distribution as surface heat flux at channel is an acceptable assumption since the thickness of heat generation (~ 4 nm) is much smaller compared to channel length ($4 \mu\text{m}$).

I_D - V_D graph and electrical field distribution inside the device should be analyzed carefully along with channel temperature to improve overall reliability of AlGaIn/GaN

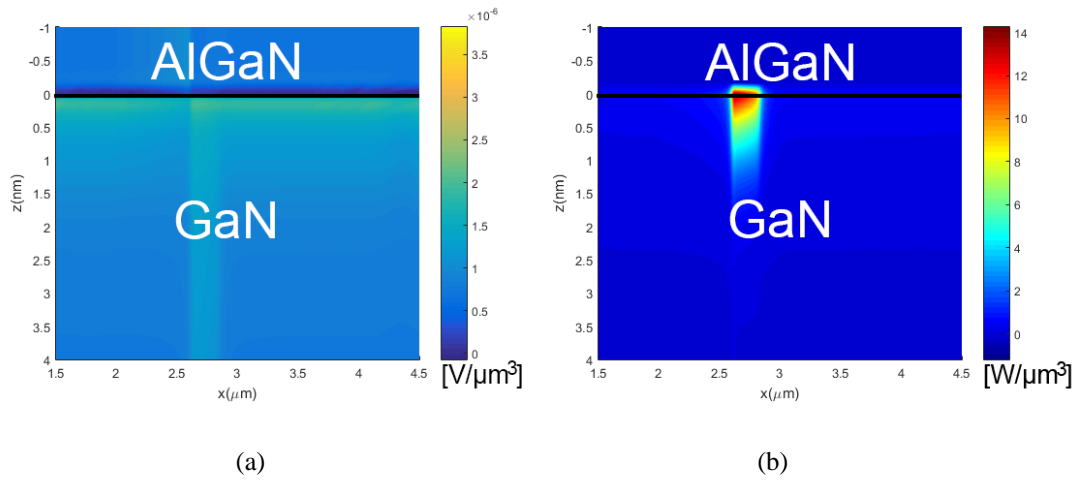


Figure 2.8. Obtained heat generation data as (a) 2D contour plot and (b) linearized heat generation graph obtained by integrating 2D plot along thickness.

HEMTs. Even though the effects of field-plate and passivation layer on power density, breakdown voltage, electron leakage are obtained from electrical simulations; thermal simulations should be performed using the Joule heating output of electrical simulations to understand their effects on temperature distribution and combined electro-thermal effects.

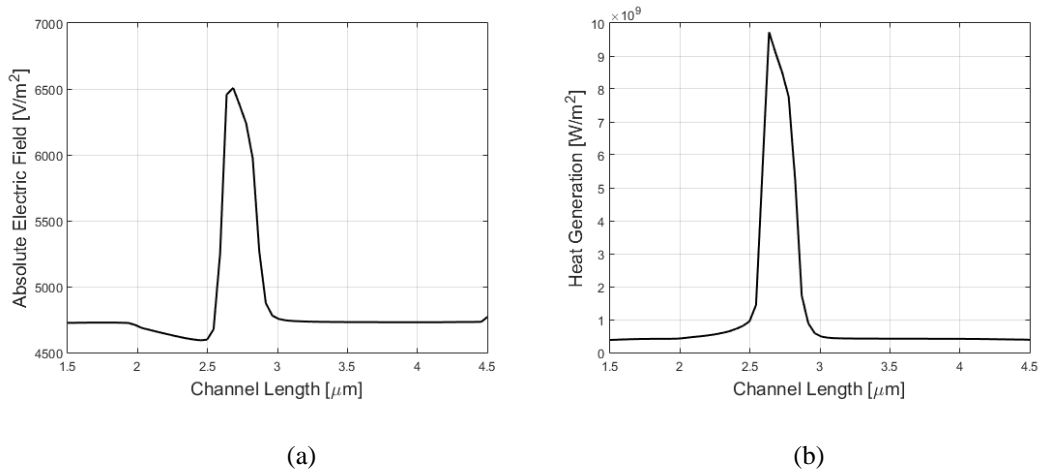


Figure 2.9. 1D linearized data obtained by integrating (a) 2D electric field distribution and (b) 2D Joule heating data along their thickness.

2.2 Thermal Simulations

Thermal simulations are conducted using COMSOL Multiphysics, which is a finite element analysis simulation program. For thermal simulations, realistic 3D model of AlGa_N/Ga_N HEMTs are generated in order to observe heat spreading effects through the die. Due to symmetry condition, quarter model assumption is used to ease computational

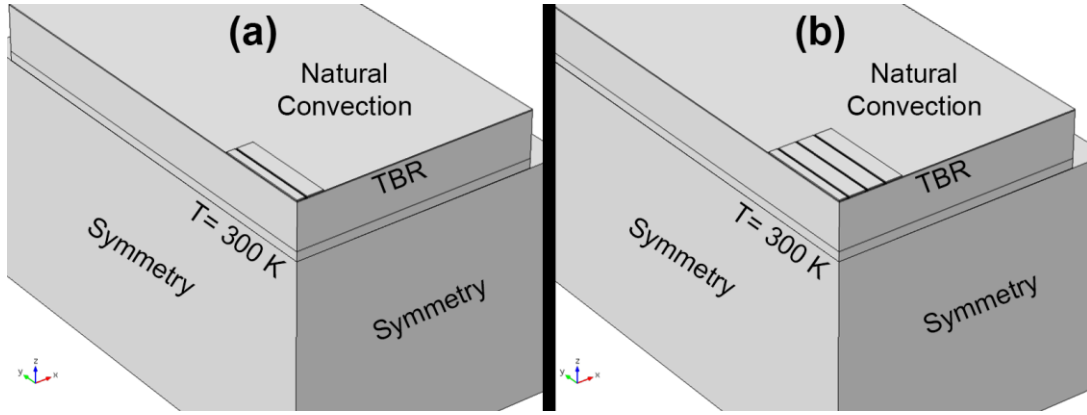


Figure 2.10. Quarter model geometry used to simulate (a) the 2 finger and (b) 6 finger device with boundary conditions.

requirements. Fig. 2.10 (a) and (b) shows the quarter model geometry used to simulate a two finger and six finger device respectively. Since only the quarter of the model is used, only one finger is represented in Fig 2.8 (a). A similar quarter model is built to represent a 6 finger device. Actual device dimensions are used to create the device geometry.

Thermal conductivities of AlGa_N, Ga_N and SiC are defined as temperature dependent to obtain precise hotspot temperature results [16]:

$$k_{AlGaN, GaN} = 100 \left(\frac{T}{300} \right)^{-0.5} \text{ W/mK} \quad (2.16)$$

$$k_{SiC} = 395 \left(\frac{T}{293} \right)^{-1.29} \text{ W/mK} \quad (2.17)$$

and thermal conductivities of gold, AlN, epoxy and copper are assumed as constants; $k_{Au} = 318 \text{ W/mK}$, $k_{AlN} = 174 \text{ W/mK}$, $k_{epoxy} = 60 \text{ W/mK}$ and $k_{Cu} = 374 \text{ W/mK}$.

In all integration processes, acoustic mismatch between the materials form impurities near the bonding regions, and the presence of a nucleation layer [53] builds a thermal barrier, known as TBR, between GaN and the substrate. These defects start from the bonding surface and decrease towards increasing material thickness. Some experiments of GaN-on-SiC HEMTs report a $TBR = 2 \cdot 10^{-8} m^2K/W$ in the latest commercial devices [54], [55]. However, by the utilization of epitaxial growth on GaN-on-SiC technology results in significantly lower $TBR = 0.45 \cdot 10^{-8} m^2K/W$ [56]. This resistance is critical in simulating high power and temperature HEMTs since it increases heat spreading along die instead of dissipating the heat through packaging of the device. To obtain a realistic temperature distribution for the majority of GaN HEMTs fabricated, $TBR = 2 \cdot 10^{-8} m^2K/W$ is used in thermal model. Maximum temperature inside device channel increases significantly with TBR introduced to the simulation and more accurate thermal results are obtained in the analysis. Thermal boundary conditions for this device are defined as natural convection over the top, right and back boundaries of the device at $T_\infty = 300$ K, $P = 1$ atm, insulation condition at the front and left boundary due to quarter model assumption and temperature boundary condition at the bottom of SiC substrate as $T_b = 300$ K.

As explained in the previous section, linearized heat generation obtained from Joule heating data is defined as boundary heat generation along each channel through the gate width. This includes the effect of bias condition, field-plate and passivation layer on heat generation distribution, unlike many thermal simulations with uniform heat generation assumption.

As in electrical simulations, proper mesh selection has a great importance in thermal simulations. Since thermal simulations are conducted in 3D, mesh should be generated carefully to minimize computation requirements without neglecting any critical. Figure 2.11 (a) and (b) shows the mesh distribution of 2-finger and 6-finger devices, respectively. Channel is the most critical region to mesh in thermal model due to heat generation. For this reason finer mesh is used between AlGa_N and GaN layers localized especially under the gate contact. About 2 and 3 million tetrahedral elements are used to mesh 2 finger and 6 finger devices, respectively.

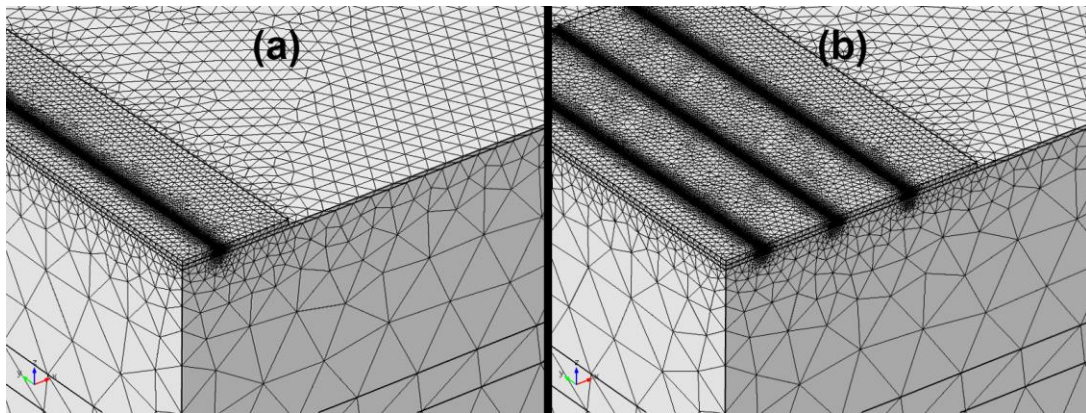


Figure 2.11. Mesh distribution of (a) 2 finger and (b) 6 finger thermal model.

Temperature distribution and hotspot temperature are obtained from thermal simulations. Since high device temperature is an important factor affecting AlGa_N/GaN HEMT reliability, conducting accurate thermal simulations are crucial to solve this problem. Thermal effects of field-plate and passivation layer along with effects of different cooling techniques can be analyzed using these simulations. Besides, more detailed results compared to experimental techniques can be obtained since spatial resolutions of experimental techniques are not sufficient enough to measure true hotspot temperature of the device. Thus, conducting accurate thermal simulations are necessary to improve device performance along with reliability.

CHAPTER 3

FIELD-PLATE

In order to investigate combined electro-thermal effects of gate connected field-plate on AlGaIn/GaN HEMT reliability, devices with $L_{FP} = 700$ nm, 1200 nm and 2000 nm field-plates are compared with a non field-plated (I-gate) device operating under open gate and partially pinched-off conditions. As open gate condition, $V_G = 0$ V and $V_D = 7$ V is used to simulate free electron flow inside the channel. For partially pinched-off condition gate voltage is decreased to $V_G = -3$ V to restrict electron flow, which will create high rates of electric field gradient near gate contact due to resistance and with the accelerating electrons at gate region, localized Joule heating will be generated. With this setup, effect of field-plate for extreme conditions as well as standard operating conditions will be examined.

Passivation thickness has a great impact on field-plate effect as well, which will be analyzed in the following chapter, so a widely used thickness of 200 nm for Si_3N_4 passivation layer is used in field-plate analysis. Field-plate material is also selected to be

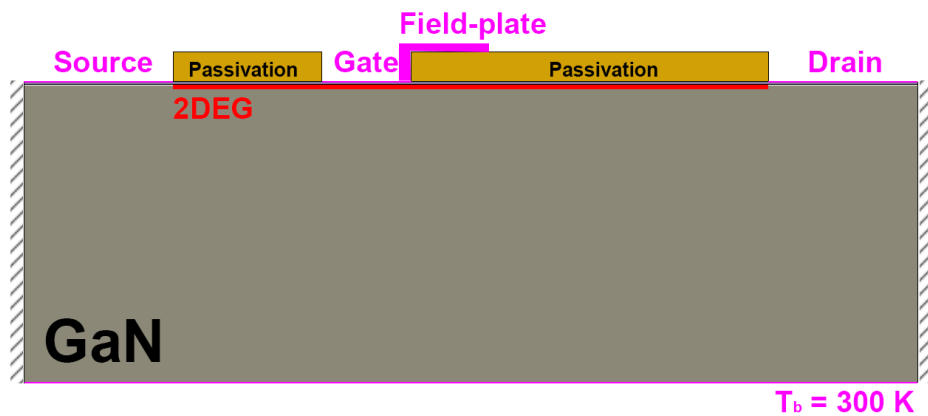


Figure 3.1. Field-plated device electrical simulation geometry.

Gold, and an additional metal contact region is defined to the device as given in Fig. 3.1 in electrical simulations.

3.1 Effect of Gate Bias

3.1.1 Same Drain Bias

As mentioned in previous chapter, biasing condition is an important factor to analyze device performance and reliability. According to the operating conditions, Joule heating amount as well as heat generation characteristics inside device channel vary creating different temperature distribution profiles for different operating conditions. To analyze this phenomena, AlGaIn/GaN HEMTs with I-gate and field-plate are operated under standard and extreme biasing conditions. Figure 3.2 shows the I_D - V_D graph obtained for equal drain voltage, $V_D = 7$ V; open channel condition, (a) $V_G = 0$ V, and partially pinched-off condition, (b) $V_G = -3$ V for I-gate and 1200 nm field-plated devices. While open channel devices are operating at 4.3 W/mm power density, devices with field-plate

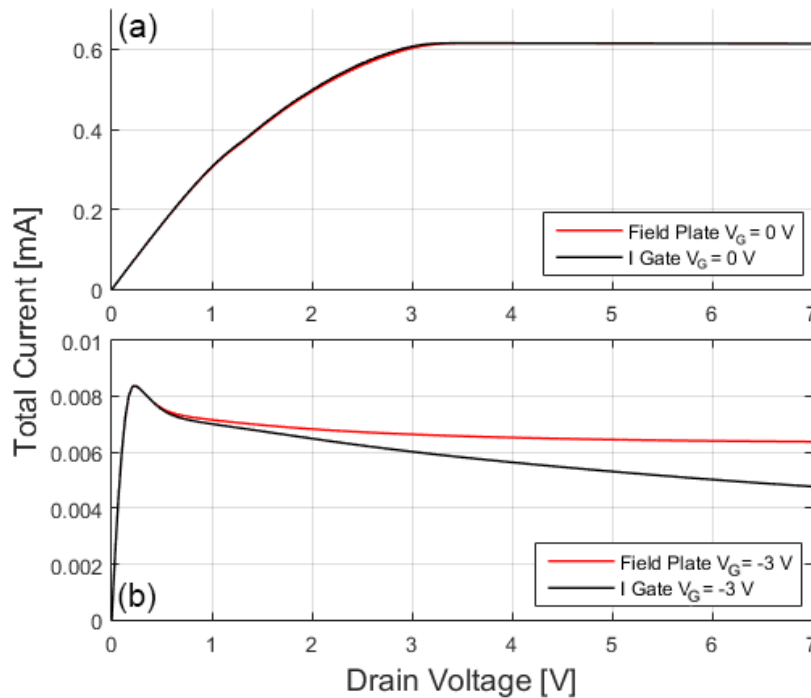


Figure 3.2. I_D - V_D graph obtained from I-gate and field-plated devices operating at open channel condition, (a) $V_G = 0$ V & $V_D = 7$ V, and near pinch-off condition, (b) $V_G = -3$ V & $V_D = 7$ V.

and I-gate operate at 0.045 and 0.03 W/mm respectively under partially pinched-off condition. If the gate voltage is further reduced under -3 V, device completely turns to OFF state where no channel current can be obtained. Effect of field-plate on electric field distribution is more crucial for partially pinched-off state due to more extreme operating conditions.

For partially pinched-off condition, I-gate device current decreases with increasing drain voltage, due to increased electron leakage and the device eventually reaches to breakdown voltage. When a 1200 nm field-plate is used in the same device, this decrease in channel current cannot be observed because of the increased stability and decreased electron leakage under extreme operation conditions. Same phenomena is not observed in open channel condition since I-gate device can easily reach to 4.3 W/mm power density level without reaching close to its breakdown voltage. Without the extreme operating condition, electron leakage is not a major issue around 4 W/mm power density

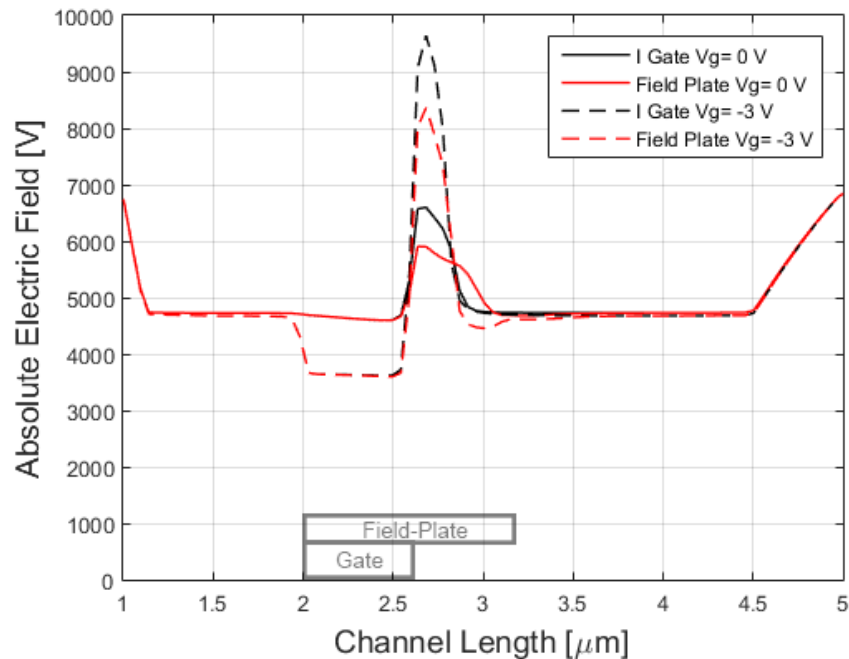
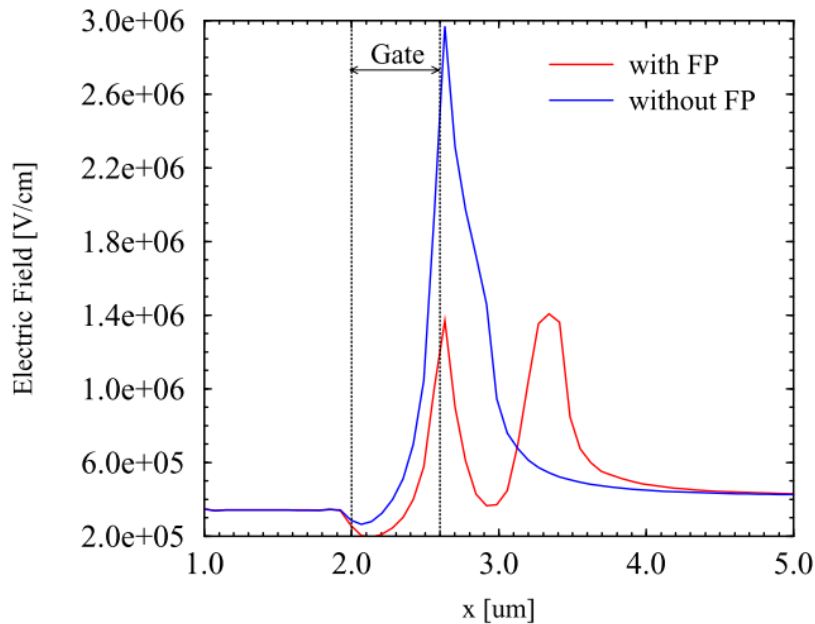


Figure 3.3. Absolute electrical field distribution inside 2DEG region for I-gate and field-plated devices operating at $V_G = 0 \text{ V}$ & $V_D = 7 \text{ V}$ and $V_G = -3 \text{ V}$ & $V_D = 7 \text{ V}$.

level. 50% increase in device power output is obtained by utilizing field-plate under extreme conditions and preventing electron leakage leading to an increased breakdown voltage.

Figure 3.3 represents the corresponding absolute electrical field distribution inside 2DEG, operating at $V_G = 0 \text{ V}$ & $V_D = 7 \text{ V}$ and $V_G = -3 \text{ V}$ & $V_D = 7 \text{ V}$. Sharp changes in the electric field within channel are eliminated and around 40% reduction in peak electrical field is obtained by the use of field-plates for both conditions. For open channel condition, electric field localized at the drain side of gate is dissipated through field-plate leading to a regulated electric field distribution inside channel. On the other hand for partially pinched-off state, an overall decrease in absolute electric field under gate contact is obtained, hence a more controlled electron transport occurs. This leads to a decrease in electron leakage and an increase in breakdown voltage by using field-plate in the device operating at near pinch-off condition. Similar outputs are reported in literature proving the breakdown voltage and electrical reliability enhancement of field-plate by



regulating electric field inside the channel as seen in Fig. 3.4 [8].

Figure 3.4. Simulated electrical field distribution inside 2DEG region for I-gate and field-plated devices operating at $V_G = 0 \text{ V}$ & $V_D = 7 \text{ V}$ obtained by V. Palankovski et al. [8].

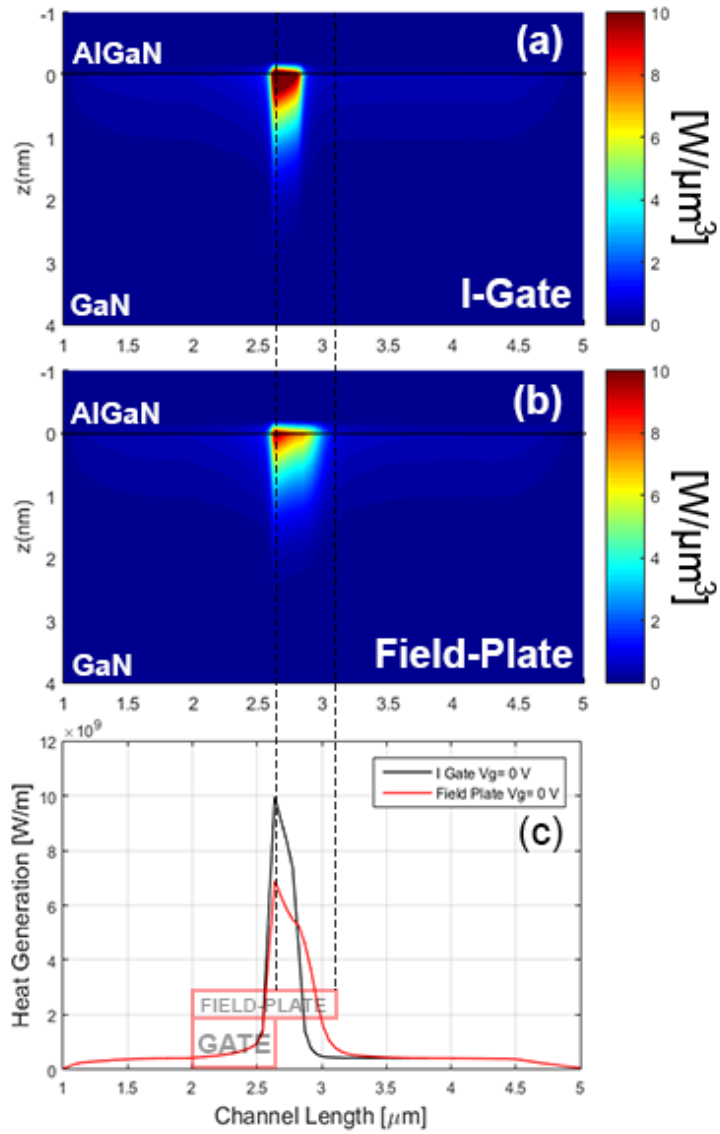


Figure 3.5. Heat generation plots for (a) I-Gate device 2D heat generation contour, (b) field-plated device 2D heat generation contour and (c) 1D integral projections of heat generations operating at $V_G = 0 \text{ V}$ and $V_D = 7 \text{ V}$.

For open channel condition, even though heat generation is denser at the drain side of gate contact, a generation throughout the channel can be observed in Fig. 3.5. As electrical field distribution suggest, heat generation is more distributed for field-plated device. However for partially pinched-off condition, a highly localized heat generation region is present only at the edge of gate. Fig. 3.5 (c) and Fig. 3.6 (c) shows the integral

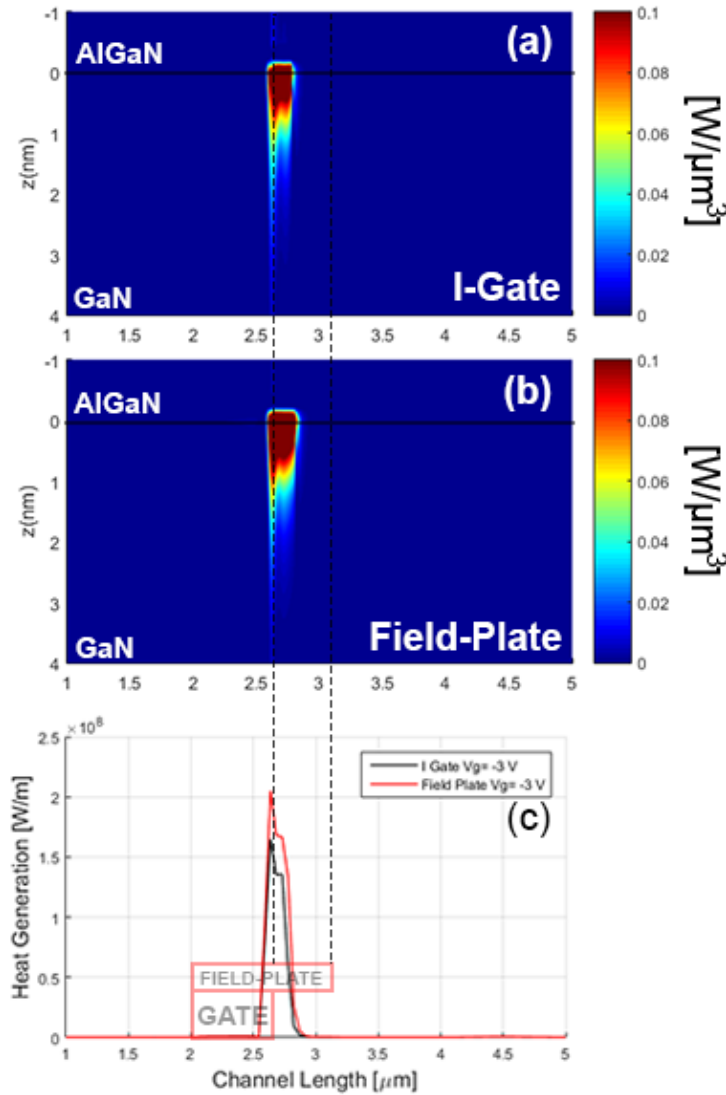


Figure 3.6. Heat generation plots for (a) I-Gate device 2D heat generation contour, (b) field-plated device 2D heat generation contour and (c) 1D integral projections of heat generations operating at $V_G = -3 \text{ V}$ and $V_D = 7 \text{ V}$.

projection of 2-dimensional Joule heating data to the AlGaN and GaN interface for comparison purposes. The projected data is later used in thermal simulations as surface heat flux. The thickness of the heat generation region do not exceed 4 nm as shown in Fig. 3.5 and Fig. 3.6; thus, this assumption can be made without major accuracy loss. Heat generation thickness is much smaller (4 nm) compared to channel length (4 μm) of the device.

Since the change in electrical field directly effects heat generation inside the device, Joule heating data is also obtained for corresponding devices using electrical simulations. Joule heating distributions of devices are given in Fig. 3.5 and Fig. 3.6 for different biasing conditions. As observed in these figures, heat generation occurs at AlGaN and GaN interface as expected since electron flow occurs in 2DEG.

For open channel condition, where $V_G = 0$ V, same power output ($P = I_D \cdot V_D$) can be obtained from devices with I-gate and field-plate as there is no difference in their I_D - V_D characteristics represented in Fig. 3.2 (a). Therefore, the total (integrated) heat generation in these devices are also the same. On the other hand, Joule heating of the device with field-plate, shown in Fig. 3.5, is distributed to a wider region compared to the I-gate device. This difference in Joule heating distribution can be obtained from the gradient of the electrical field shown in Fig. 3.3.

For partially pinched-off state, where $V_G = -3$ V, Fig. 3.6 shows the higher and slightly more distributed heat generation characteristic of the field-plated device. This contradicts with the results obtained for open channel condition. The reason behind this contradiction can be explained by careful analysis of Fig. 3.2 (b). According to this figure, the power output ($P = I_D \cdot V_D$) of the device without field-plate is significantly lower compared to the device with the field-plate due to increase in I_D under same biasing conditions. As explained previously, under extreme operating conditions device with I-gate suffers from instability due to high electric field gradient. This instability increases electron leakage, decreases breakdown voltage and power output of the device leading to a decreased channel current under high drain voltages. Reduced power output is also responsible for decreased total heat generation inside the device. Thus, these analysis should be conducted for devices with same power outputs, hence same total heat generations, to observe true effect of field-plate.

3.1.2 Same Power

Two biasing conditions with similar power outputs are simulated to analyze biasing condition effect under equal heat generation. Gate voltages of $V_G = 0$ V and $V_G = -1.5$ V

are chosen to be simulated since the device under partially pinched-off condition, $V_G = -3$ V, cannot reach to high power density levels due to low breakdown voltage, 7.2 V, under extreme conditions. Figure 3.7 shows the I_D - V_D characteristics of field-plated and I-gate devices. According to this graph when the power output density is chosen to be 4.3 W/mm, field-plate and I-gate devices with $V_G = -1.5$ V biasing condition are operated at $V_D = 15.9$ V and $V_D = 16.1$ V, respectively.

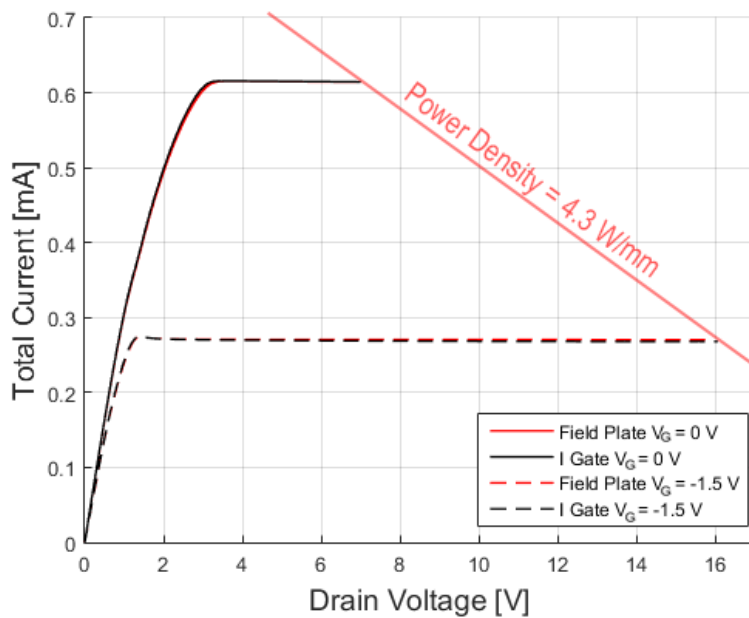


Figure 3.7. The I_D - V_D characteristics of I-gate and field-plated devices operating at gate voltages $V_G = 0$ and -1.5 V and power density of 4.3 W/mm.

Similar to the first study, 2-dimensional Joule heating data, for these devices at above biasing conditions, is obtained using electrical simulations. This data is integral projected to AlGaIn/GaN interface and plotted as in Fig. 3.8. Devices with field-plates have more widely distributed heat generation profiles and lower peak heat generation values. Although the total heat generation amount inside the channel is equal for devices operated at similar power outputs, heat generation in the field-plated devices spreads to a wider area where electric field is dissipated towards field-plate edge. While for open channel condition, $V_G = 0$ V, 35% drop in maximum heat generation is obtained by using field-plate, its value drops to 25% for $V_G = -1.5$ V. This drop may appear as controversial to

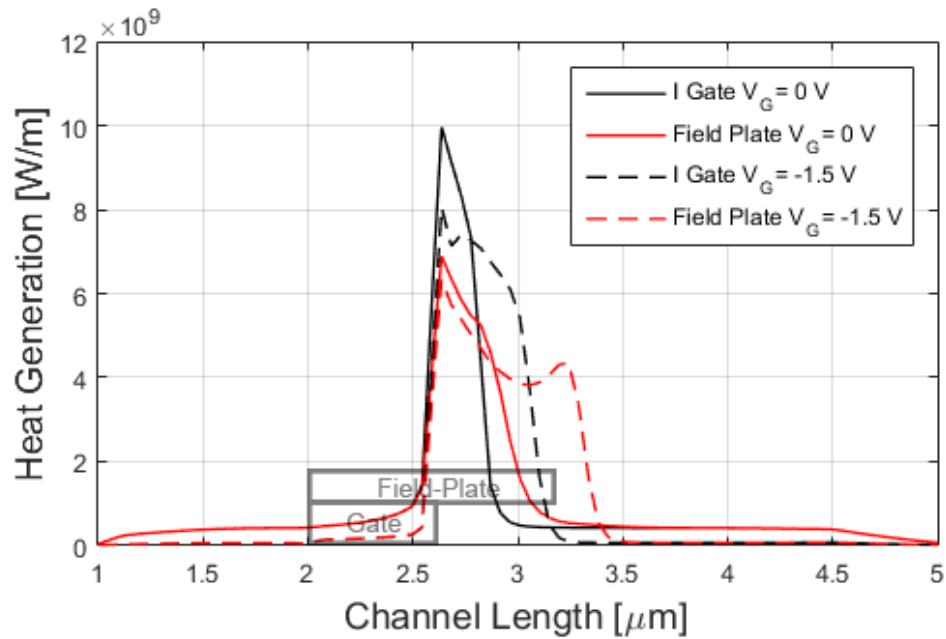


Figure 3.8. Integral projection of 2D heat generation data into linearized heat generation distribution for devices operating at 4.3 W/mm.

previously stated data. However for open gate condition, 35% drop is obtained for a single point in heat generation distribution. On the other hand, when the overall decrease between 2.5 – 3.5 μm into the channel is analyzed, effect of field-plate appears to be more significant for AlGaIn/GaN HEMT operated at $V_G = -1.5$ V.

To observe the effect of heat generation distribution obtained from electrical simulations, on maximum temperature in devices; thermal simulations are performed. Obtained linearized heat generation data is used as boundary heat flux input to thermal simulations as explained before. Temperature distribution of devices with 1200 nm field-plate and I-gate device are simulated to obtain hotspot temperatures of corresponding devices and to analyze the impact of field-plate on AlGaIn/GaN reliability.

In order to compare 1200 nm field-plated device with I-gate device, projected Joule heating distributions in Fig. 3.8 are used as surface heat flux in the previously explained thermal model. By integrating 2D Joule heating data along its thickness, linearized heat generation data through device channel is obtained to be used as surface heat flux to obtain temperature distribution given in Fig. 3.9. This figure shows the 3-dimensional temperature distribution and Fig. 3.10 shows the temperature distribution inside the 2DEG regions in devices obtained from these thermal simulations. Devices with $V_G = 0$ V bias condition have lower maximum temperatures despite of having higher peak heat generation values due to heat generation distributions spread to entire channel, as shown in Fig. 3.8. At equal power outputs, generated heat in open channel devices is more distributed compared to devices with relatively closed channels. Increased gate voltage restricts the flow of electrons causing higher electrical field gradients and more localized heat generation in such devices.

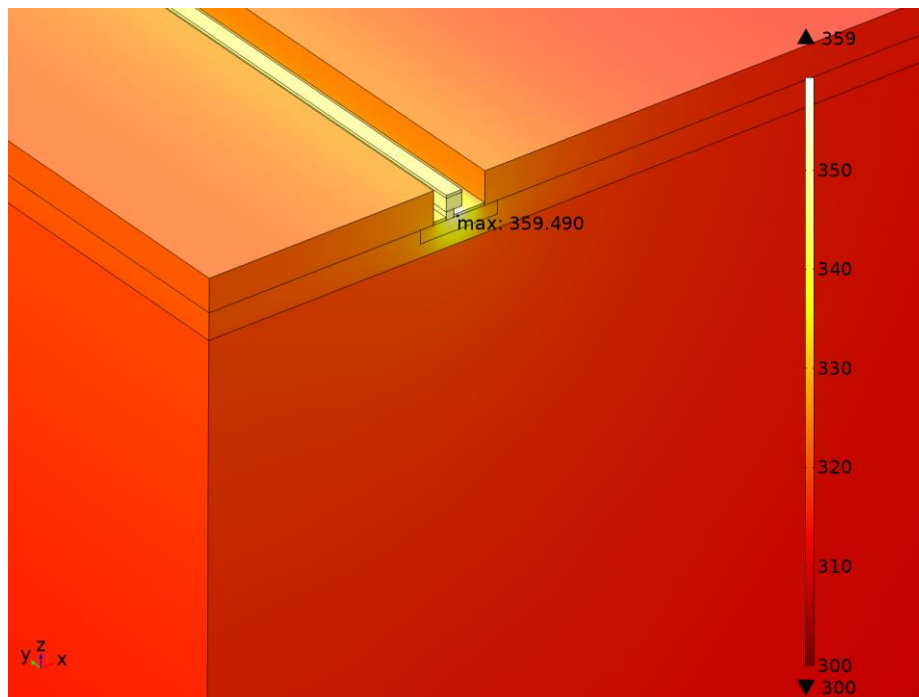


Figure 3.9. 3D temperature distribution obtained for field-plated AlGaIn/GaN HEMT operating at $V_G = -1.5$ V and $V_D = 15.9$ V.

In Fig. 3.10, I-gate device operating under $V_G = -1.5$ V has the highest maximum temperature with 362.5 K. When field-plate is used for same device, maximum temperature is decreased to 359 K, meaning a 6% reduction in hotspot temperature difference ($\Delta T = T_{\text{hotspot}} - T_b$) is obtained. However; for fully open channel condition, $V_G = 0$ V, only 1 K reduction is obtained by using field-plate. These results show that even though using field-plate is beneficial to reduce maximum temperature, its effect decreases for open channel condition, as in the case of $V_G = 0$ V. When a similar analysis is done on $V_G = -3$ V device before reaching to its breakdown voltage, 7.2 V; maximum temperature is obtained to be much lower due to very limited power output of device. Power density outputs of 0.045 W/mm and 0.03 W/mm for field-plated and I-gate devices respectively generated lower heat rates compared to devices operating under 4.3 W/mm as seen previously on Fig. 3.6.

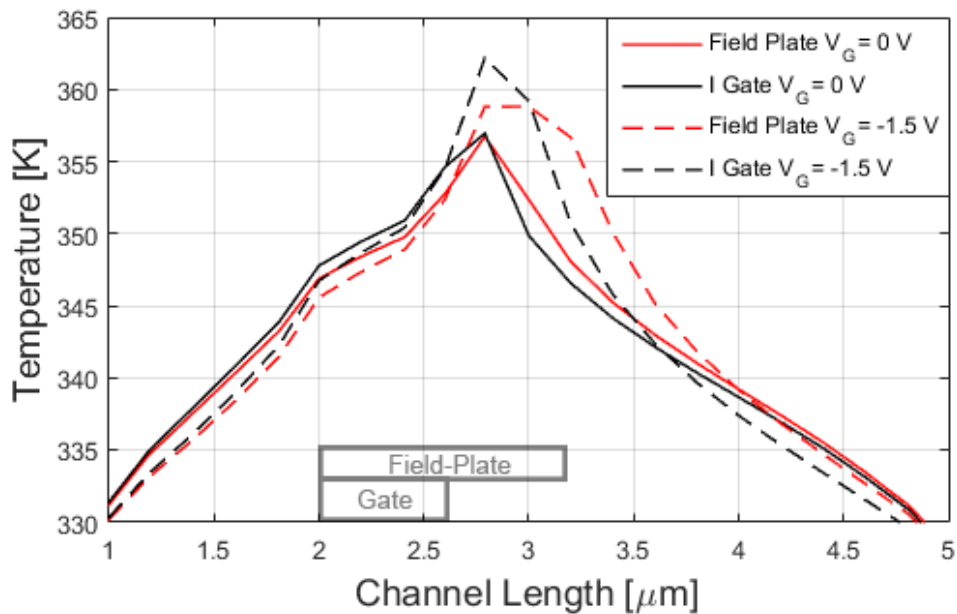


Figure 3.10. Temperature distribution inside the channel for I-gate and field-plated AlGaIn/GaN HEMTs operating at $V_G = 0$ and -1.5 V with power density 4.3 W/mm.

All the previous analysis are done for 2 finger configuration. To analyze the multi finger effect, 6 finger configuration is used with same device dimensions. Biasing condition of $V_G = -1.5$ V from equal power output analysis is selected, since hotspot temperature is higher compared to open channel condition, to simulate the maximum temperature condition for both field-plated and I-gate devices. Field-plate length of 1200 nm is used to simulate field-plated device. Maximum temperature of I-gate device is obtained as 389 K when 6 finger configuration is used, instead of 362.5 K in 2 finger configuration of the same device. For field-plated device with 6 fingers, maximum temperature is obtained as 384 K. Temperature reduction (ΔT) by using field plated design is 6% which is equal to the one obtained by using a 2 finger configuration shown in Fig. 3.10. Thus, although the maximum temperature reduction percentages are the same, usage of field-plate is more critical for multifinger devices since the operating temperatures are much higher due to thermal influences of neighboring fingers on each other.

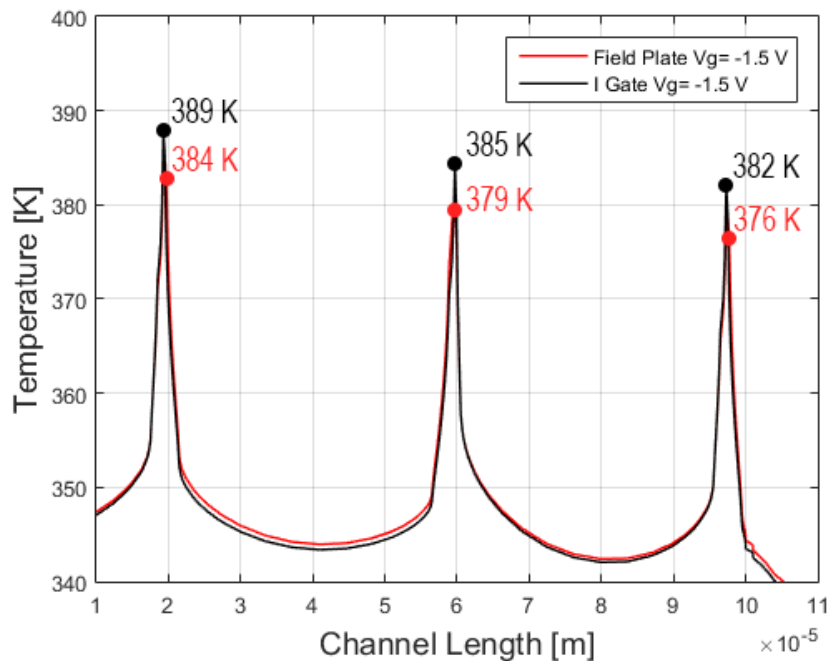


Figure 3.11. Temperature distributions and maximum temperatures of 6-finger I-gate and field-plated AlGaN/GaN HEMTs operating at $V_G = -1.5$ V with power density of 4.3 W/mm.

In multifinger configurations, maximum temperatures are observed at innermost fingers. Figure 3.11 shows that while the maximum temperature of outermost finger for field-plated device is 376 K, innermost finger is heated 10.5% more in ΔT to 384 K due to heat spreading. Also, even though peak temperatures of I-gate device is higher than field-plated one, the remaining regions have lower temperatures. In field-plated device same amount of total heat is generated, only the heat generation distribution is more scattered. This decreases the peak temperatures by dissipating heat generation throughout the channel and the die. This effect also can be observed when temperature distribution inside single finger is analyzed. Figure 3.12 shows the temperature distribution along innermost finger channels of field-plated and I-gate devices. Even though the maximum temperature of I-gate device is higher, temperature distribution between gate and drain contact is lower than field-plated device.

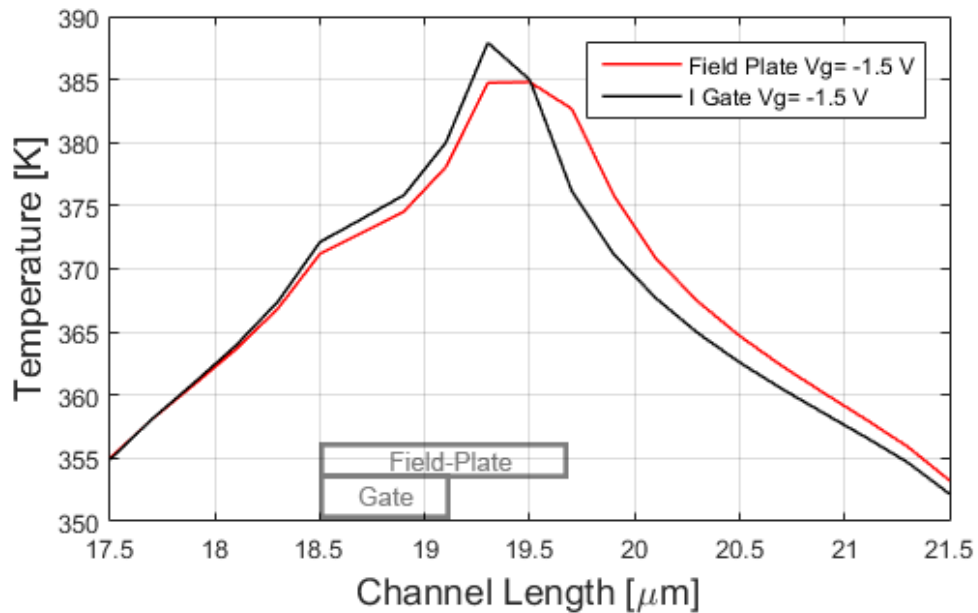


Figure 3.12. Temperature distribution of innermost fingers for 6-finger I-gate and field-plated AlGaIn/GaN HEMTs operating at $V_G = -1.5$ V with power density of 4.3 W/mm.

On the other hand, when temperature distribution around maximum temperature of the device is measured in 1 μm region, between 19 -20 μm , an average of 378 K is obtained for the I-gate device under $V_G = -1.5$ V and $V_D = 16.1$ V condition. A deviation of 12% is obtained from true hotspot temperature, proving that the low spatial resolution of

experimental techniques are not sufficient to measure maximum temperature inside AlGaIn/GaN HEMTs. Moreover, maximum temperature occurs inside the device, between AlGaIn and GaN layers, hence; a measurement taken from the surface of the device would lead to a larger deviation from real maximum temperature.

In our previous research, same thermal model is used to estimate hotspot temperature of a different AlGaIn/GaN HEMT design operating at 8.4 W/mm power density and the results were compared with the experimental data obtained from infrared (IR) and thermo-reflectance (TR) measurements in order to validate our thermal model [57]. Temperature surface average values from 0.3 μm and 5 μm wide regions are taken from thermal model in order to compare the results since spatial resolutions of TR and IR methods are 0.3 μm and 5 μm respectively. Figure 3.13 shows that, the model and experimental results fit well within 2% error margin at the corresponding spatial averaging of the simulation output. Channel temperature values obtained from TR analysis are significantly higher compared to the IR results due to better spatial resolution. However, by even using TR measurements, 18% deviation in measured temperature is observed compared to the true hotspot temperature.

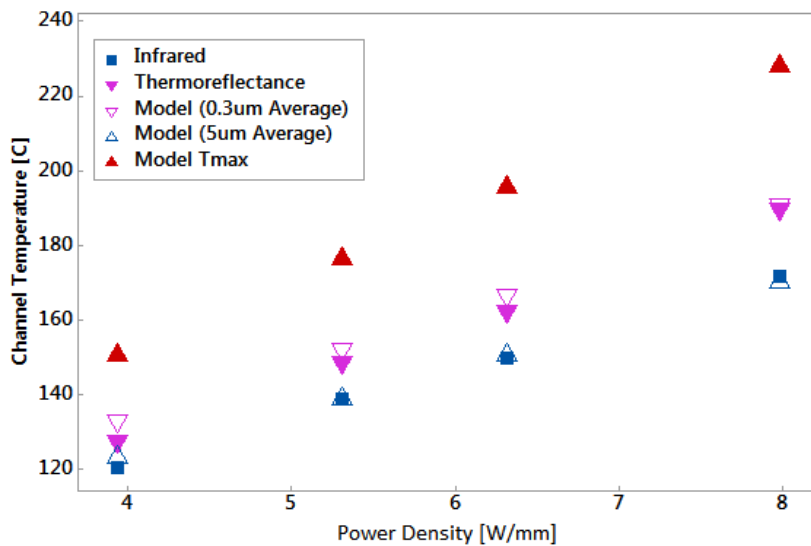


Figure 3.13. Comparison of the simulation results and experimental data obtained from IR and TR experimental methods. [57]

By the utilization of field-plate, a reduction in hotspot temperature is obtained for varying gate-biasing conditions. This thermal effect arise from electrical impacts of gate connected field-plate such as regulating electric field distribution and increasing breakdown voltage. If the field-plate length is selected to be shorter, heat generation localization increases. On the other hand, if it is longer, electron leakage increases from channel decreasing current and power output of the device, which will be explained in detail in the following section.

3.2 Effect of Field-Plate Length

Power density, electric field distribution, heat generation, and temperature distribution are obtained for devices with and without field-plate by using 1200 nm field-plate. Electric field distribution is regulated and an increase in breakdown voltage, especially under extreme operating conditions, is achieved by decreasing current leakage from channel. However, the length of field-plate also has a significant effect on these properties. To analyze the effect of field-plate length, same device is simulated with 700

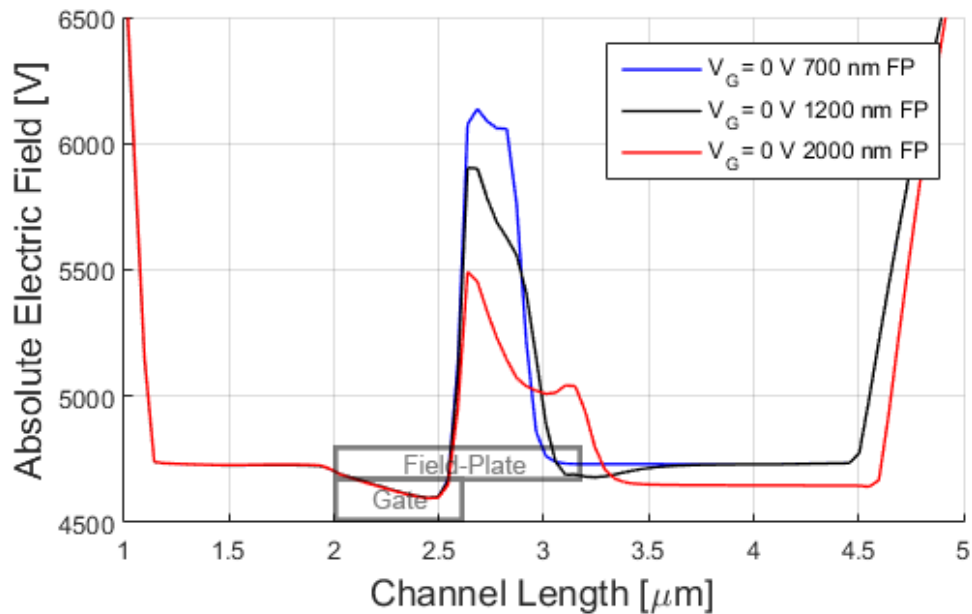


Figure 3.14. Electric field distributions of devices with $L_{FP} = 700, 1200$ and 2000 nm operating under open channel condition, $V_G = 0V$ and $V_D = 7V$.

nm and 2000 nm long gate connected field-plates, and compared with 1200 nm field-plated device.

Fig. 3.14 represents the electric field distribution along device channel for three different field-plate lengths. When a shorter, $L_{fp} = 700$ nm, field-plate is used; a significant increase in electric field gradient is observed and compared to 1200 nm field-plate device, regulation effect of field-plate on electric field is decreased. If field-plate length is further decreased, electrical field distribution characteristic converges to I-gate device. On the other hand, when field-plate length is increased, electron leakage from the channel also increases. Field-plate contact approaches to drain metal contact leading to electron leakage and power loss inside the device [8]. As seen in Fig. 3.14, 2000 nm field-plate device has reduced overall electrical field due to power loss, which decreases power density output from $P = 4.3$ W/mm to 3.9 W/mm.

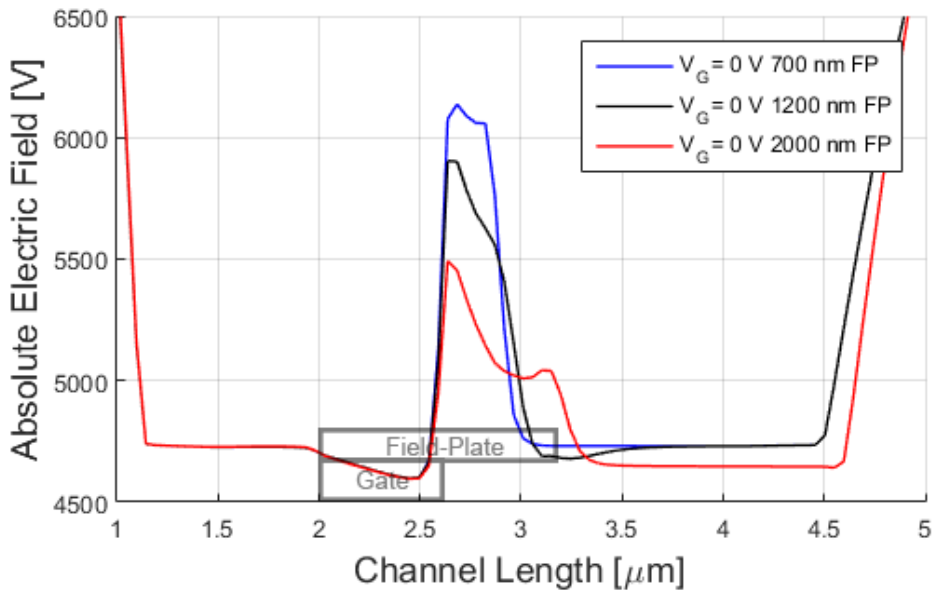


Figure 3.15. Linearized heat generation distributions of devices with $L_{FP} = 700, 1200$ and 2000 nm operating under open channel condition, $V_G = 0V$ and $V_D = 7V$.

Heat generation distribution of devices with varying field plate lengths output along channel is given in Fig. 3.15. Device with 700 nm field-plate has more localized heat generation even though total heat generations of 1200 nm field-plate and 700 nm filed-

plate devices are equal. This dissipation further increases for device with 2000 nm field-plate but total heat generation of this device is also lower than devices with 700 nm field-plate and 1200 nm field-plate due to power loss. Thus, field-plate length should be optimized before fabrication process since longer field-plates increases electron leakage and decreases power output, and shorter field-plates are responsible for localized heating and increased maximum temperatures of the devices.

CHAPTER 4

PASSIVATION AND OPTIMIZATION

In literature, reduction of current collapse and device degradation by application of a dielectric layer as surface passivation is proven in many studies. This reduction indicates the effect of passivation layer on surface properties to prevent electrical failure mechanisms. Even though many dielectric materials can be used as passivation layer such as AlN, MgO, Al₂O₃, HfO₂ and Sc₂O₃; SiO₂ and SiN based passivation layers are widely used to improve AlGaIn/GaN HEMT performance [42], [44], [58], [59]. Since passivation layer increases device performance by reducing surface trap density, in order to increase AlGaIn/GaN HEMT reliability and performance, application of a passivation layer in right thickness has a great importance. If the passivation layer thickness is smaller than a certain threshold, devices operate at lower breakdown voltage with increased electron leakage from channel. On the other hand, if the passivation thickness is too large in a field-plated device, electro-thermal effects of field-plate may be hindered, thermal management of the device may become more difficult and deviation of experimental results from true hotspot temperature increases due to increased thermal resistance. For this reason, passivation layer should be applied as thin as possible, but thick enough to prevent electron leakage from the channel by reducing surface trap density. Especially for field-plated devices, passivation layer optimization is crucial to obtain best thermal performance from AlGaIn/GaN HEMTs.

To analyze the passivation effect, AlGaIn/GaN HEMTs are simulated with two widely used passivation materials, SiO₂ and Si₃N₄. When materials with different dielectric properties are used as passivation layers, threshold thickness varies significantly.

4.1 SiO₂ Passivation

For SiO₂ passivation, thicknesses of $t_{\text{SiO}_2} = 5, 10, 35$ and 50 nm are simulated for both I-gate and field-plated devices under gate voltage $V_G = -1$ V and $V_D = 7$ V to observe the effect of passivation material. On the other hand, same device with Si₃N₄ passivation with passivation thicknesses of $t_{\text{Si}_3\text{N}_4} = 25, 100$ and 200 nm thick are simulated under both open channel and partially pinched-off operating conditions to compare results obtained in previous chapter with smaller passivation thicknesses in the following section.

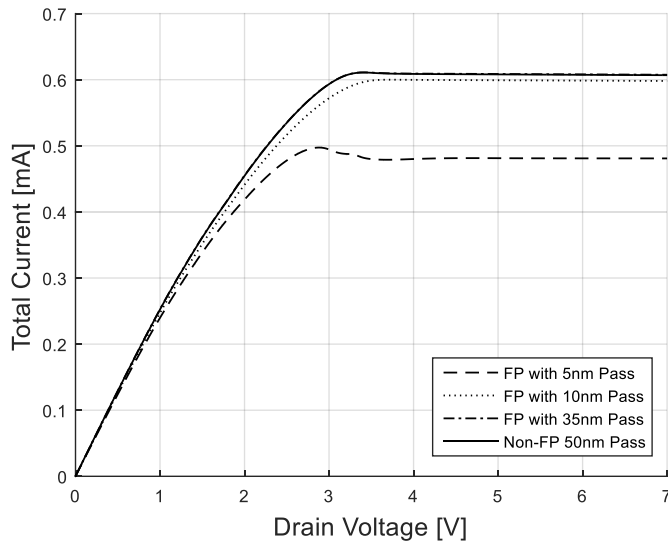


Figure 4.1. I_D - V_D graphs obtained for I-gate device with $t_{\text{SiO}_2} = 50$ nm and field-plated devices with $t_{\text{SiO}_2} = 5, 10, 35,$ and 50 nm operating at $V_G = -1$ V and $V_D = 7$ V.

The I_D - V_D graphs obtained for I-gate device with $t_{\text{SiO}_2} = 50$ nm and field-plated devices with $t_{\text{SiO}_2} = 5, 10, 35,$ and 50 nm operating at $V_G = -1$ V and $V_D = 7$ V are given in Fig. 4.1. Device with 5 nm SiO₂ passivation layer has lower power density output compared to other devices at any given drain voltage. Using a very thin SiO₂ passivation layer caused electron leakage from channel through the passivation. Electrons tend to escape from AlGaN/GaN interface and flow to the gate metal contact when passivation layer thickness is not sufficient. A reduction in electron leakage can be obtained by increasing passivation thickness. On the other hand, increasing passivation thickness too much

decreases the effect of field-plate, which is used to regulate electrical field and increase breakdown voltage inside device channel. Field-plate is introduced to devices as an additional electrical contact to apply voltage difference. This additional contact acts as an extension of gate metal contact and reduces electric field gradient inside the channel. When $t_{\text{SiO}_2} = 35$ nm passivation thickness is reached, the effect of field-plate on power output disappears. Both $t_{\text{SiO}_2} = 35$ nm field-plated, I-gate and $t_{\text{SiO}_2} = 50$ nm field-plated, I-gate devices have $P = 4.35$ W/mm power density output, meaning electron leakage can be prevented and power output reaches to a saturation level at $t_{\text{SiO}_2} = 35$ nm SiO₂ passivation for this device.

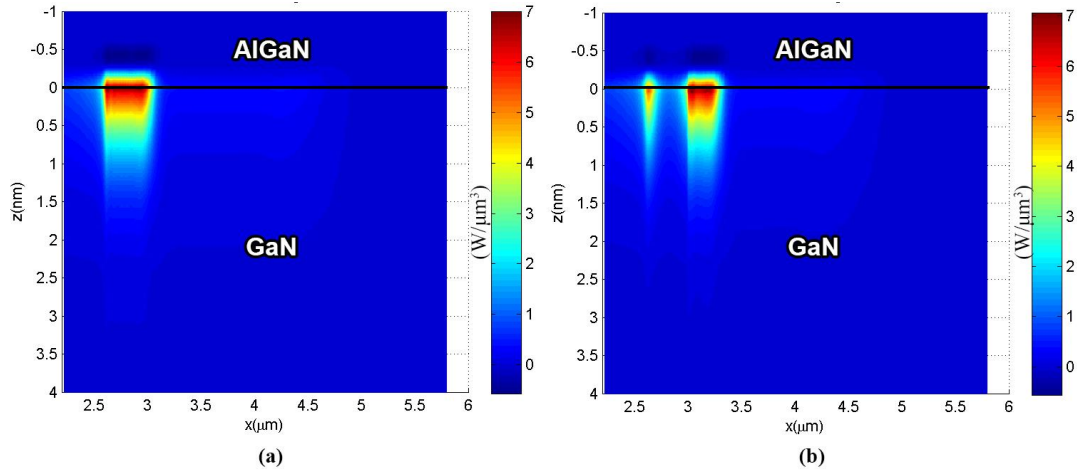


Figure 4.2. 2D heat generation contour plots obtained for (a) I-gate and (b) field-plated AlGaIn/GaN HEMTs with SiO₂ passivation thickness of $t_{\text{SiO}_2} = 10$ nm operating at $V_G = -1$ and $V_D = 10$ V.

Power densities, electrical field distributions, and Joule heating data of devices are obtained as a result of the electrical simulations. In Fig. 4.2, 2D contour plots obtained from the Joule heating data for I-gate and field-plated devices with $t_{\text{SiO}_2} = 10$ nm are given. In Fig. 4.2(a), localized heat generation region is observed at the drain edge of the gate. With the introduction of a field-plate to the device, localized heating spreads along the field plate as shown in Fig. 4.2(b). Applied gate voltage to control the current flow generates a resistance leading to high electric field gradients at the drain side of the edge. Since electrical field gradient and Joule heating are related, localized heat generation occurs as shown in Fig. 4.2(a). However; the addition of field-plate to the device

introduces an additional electrical contact to that edge, reducing the effects of sharp electric field gradients. With such regulation of the electric field distribution, a spreading effect in heat generation to a wider area is obtained as shown in Fig. 4.2(b).

Although Fig. 4.2 shows the effects of field-plate on heat distribution, a better comparison can be made by using the 1D heating characteristic along the channel length. Integration of the 2D heat generation data along its thickness in Matlab gives lateral heat generation distribution along the device channel as explained in previous chapter. Fig. 4.3, obtained with this method, shows the effect of field-plate on the heat generation for the devices with $t_{\text{SiO}_2} = 5 \text{ nm}$.

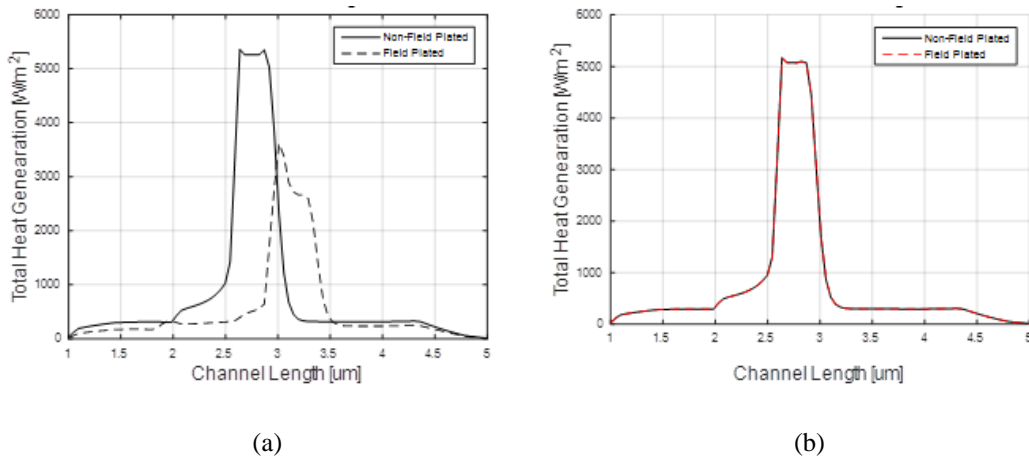


Figure 4.3. Linearized heat generation distribution graphs for I-gate and field-plated AlGaIn/GaN HEMTs with SiO₂ passivation thickness of (a) $t_{\text{SiO}_2} = 10 \text{ nm}$ and (b) $t_{\text{SiO}_2} = 50 \text{ nm}$ operating at $V_G = -1$ and $V_D = 10\text{V}$.

As shown in Fig. 4.3 (a), total heat generation, (area under the curves given in figure) inside the device is decreased when field-plate is added to the device. This is a result of the lower power density output of field-plated device with $t_{\text{SiO}_2} = 5 \text{ nm}$ that suffers from the electron leakage. Since very thin passivation layer is used, the additional electrical contact introduced by the field-plate causes electrons to escape from 2DEG to the metal contacts on the surface, where voltage differences are applied. Hence; for the devices with $t_{\text{SiO}_2} = 5 \text{ nm}$, the reduction in heat generation, thus device temperatures, are caused by the decreased power output of the device due to electron leakage. This is not desired

for reliable and efficient device performance and causes a similar problem as using too long field-plates as explained previously. On the other hand, the effects of field-plate vanish when passivation thickness of $t_{\text{SiO}_2} = 50$ nm is reached as given in Fig. 4.3 (b). Both the field-plated and I-gate devices with $t_{\text{SiO}_2} = 50$ nm thick SiO_2 layers have the same heat generation characteristics.

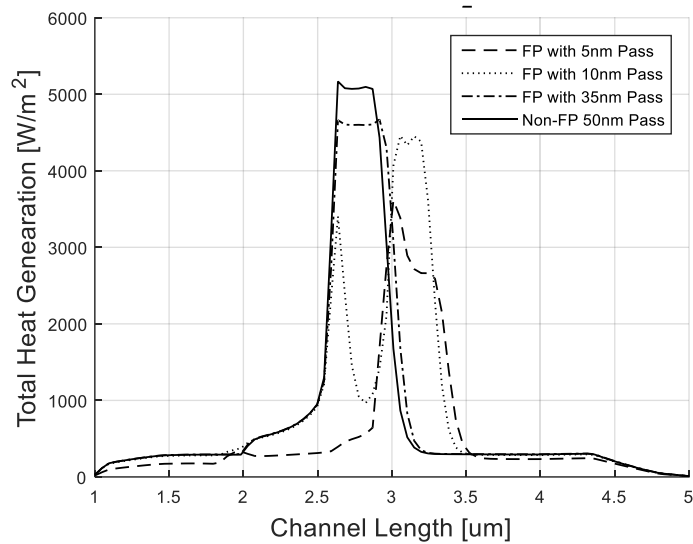


Figure 4.4. Linearized heat generation distribution graphs for I-gate AlGaN/GaN HEMTs with SiO_2 passivation thickness of $t_{\text{SiO}_2} = 50$ nm and field-plated AlGaN/GaN HEMTs with SiO_2 passivation thickness of $t_{\text{SiO}_2} = 5, 10, 35$ and 50 nm operating at $V_G = -1$ and $V_D = 10\text{V}$.

To observe the overall effect, heat generation distributions along device channel are plotted for SiO_2 passivation thicknesses of $t_{\text{SiO}_2} = 5, 10, 35,$ and 50 nm for field-plated and $t_{\text{SiO}_2} = 50$ nm for I-gate device in Fig. 4.4, since field-plate effect can only be seen for thicknesses lower than $t_{\text{SiO}_2} = 50$ nm. When the passivation thickness is selected to be $t_{\text{SiO}_2} = 35$ nm, a spreading in localized heat distribution is obtained towards field-plate in the channel without any decrease in the power output of the device. Even though the amount of heat generated are equal for both devices with field-plated $t_{\text{SiO}_2} = 35$ nm and $t_{\text{SiO}_2} = 50$ nm passivation layers, heat generation along channel are different.

Table 4.1 lists the variations in the power output and maximum temperature of field-plated and I-gate devices when different passivation thicknesses are used. For a field-plated device with $t_{\text{SiO}_2} = 5$ nm passivation thickness, 12.66% decrease in maximum device temperature is obtained, however power density of device is decreased from $P = 4.25$ W/mm to $P = 3.36$ W/mm corresponding to 20.94% power loss. When passivation thickness is increased to $t_{\text{SiO}_2} = 10$ nm for the same field-plated device, about 6% drop in maximum temperature is observed with minimal 1.85% power loss. The drop in hotspot temperature is 2.55% for a field-plated device with $t_{\text{SiO}_2} = 35$ nm without any decrease in power density. This reduction in maximum temperature is caused by the spreading effect of field-plate on heat generation distribution, rather than a decrease in the total amount of heat generated. If the passivation thickness is increased further, field-plate effect on the hotspot temperature cannot be seen. Finally, as observed in Table 4.1 significant improvement of the power output and thermal performance of the devices cannot be achieved solely by introducing passivation on devices without the field-plates.

Passivation Thickness [nm]	Power Density Output [W/mm]		Percentage Change of Power Density [%]	$\Delta T = T_{\text{max}} - T_{\text{b}}$ [K]		Percentage Change in ΔT [%]
	without	with		without	with	
	Field Plate	Field Plate		Field Plate	Field Plate	
5	4.25	3.36	20.94	15.8	13.8	12.66
10	4.33	4.25	1.85	15.4	14.5	5.84
35	4.35	4.35	0.00	15.7	15.3	2.55
50	4.35	4.35	0.00	15.8	15.8	0.00

Table 4.1. Power density output, change in power density by field-plate effect and decrease in maximum temperature for I-gate and field-plated AlGaIn/GaN HEMTs with SiO₂ passivation thicknesses of $t_{\text{SiO}_2} = 5, 10, 35,$ and 50 nm.

4.2 Si₃N₄ Passivation

A similar study is conducted to observe the effect of Si₃N₄ applied as a passivation material. The current fitting process, as explained in chapter 2, between simulation and experimental results were conducted on this device configuration. Also, field-plate analysis in chapter 3 was based on device with Si₃N₄ passivation. Devices with $t_{\text{Si}_3\text{N}_4} = 25$ nm, 100 nm, and 200 nm thick passivation layers are analyzed. Six different electrical and thermal simulations are conducted for bias conditions of $V_G = 0$ and $V_G = -3$ V at $V_D = 7$ V. From Fig. 4.5 it can be seen that, using thinner Si₃N₄ layer as passivation increases the effect of field-plate significantly. Absolute electric field distribution is more regulated for 100 nm passivation device, compared to 200 nm passivation case where the effect of field-plate slightly fades away, as explained previously. However, when the passivation layer is selected too thin, it cannot fulfill its purpose to prevent electron leakage from the

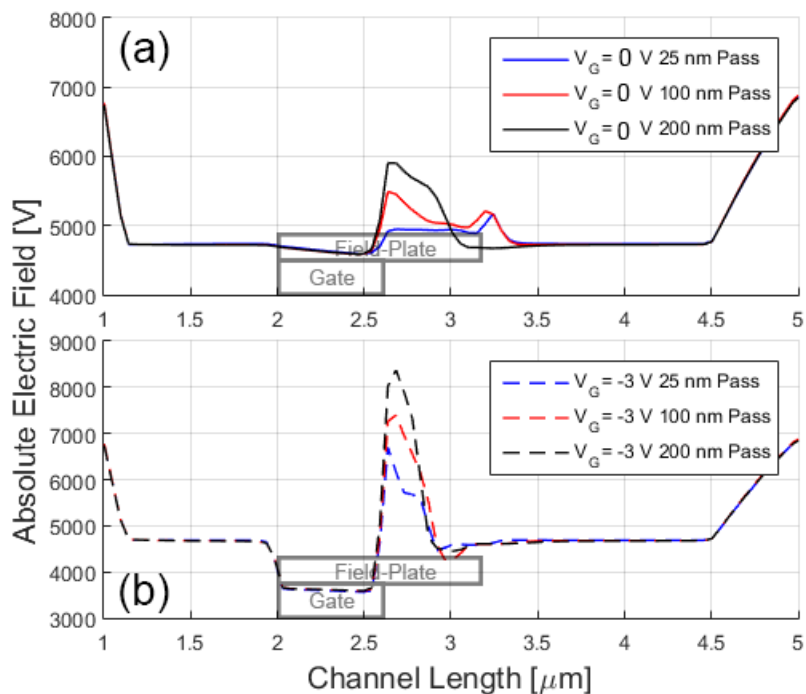


Figure 4.5. Electric field distribution along channel for 1200 nm field-plated AlGaIn/GaN HEMTs with $t_{\text{Si}_3\text{N}_4} = 25, 100,$ and 200 nm operating at (a) $V_G = 0$ V & $V_D = 7$ V and (b) $V_G = -3$ V & $V_D = 7$ V.

device and degradation occurs [60]. For example, when 25 nm Si_3N_4 passivation is applied to the device, major power loss and breakdown problems occur due to electron leakage from channel. For $V_G = 0$ V; device fails to achieve drain voltages more than 5.63 V, limiting the device to 3.1 W/mm power density level. Moreover; when $V_G = -3$ V is applied, drain voltage limit drops to 5.05 V. This major problem can be clearly seen in Fig. 4.6; where due to electron leakage, absolute electric field inside the channel have dropped significantly for 25 nm passivation device.

Heat generation distribution graphs are also given in Fig. 4.6 for 100 nm and 200 nm Si_3N_4 passivation layer devices. For open channel condition, $V_G = 0$ V, heat generation is more distributed along device channel for 100 nm passivation thickness. Increased effect of field-plate dissipated localized heat generation even more compared to 200 nm passivation field-plated device. This is evident from Fig. 4.6, where absolute electric field

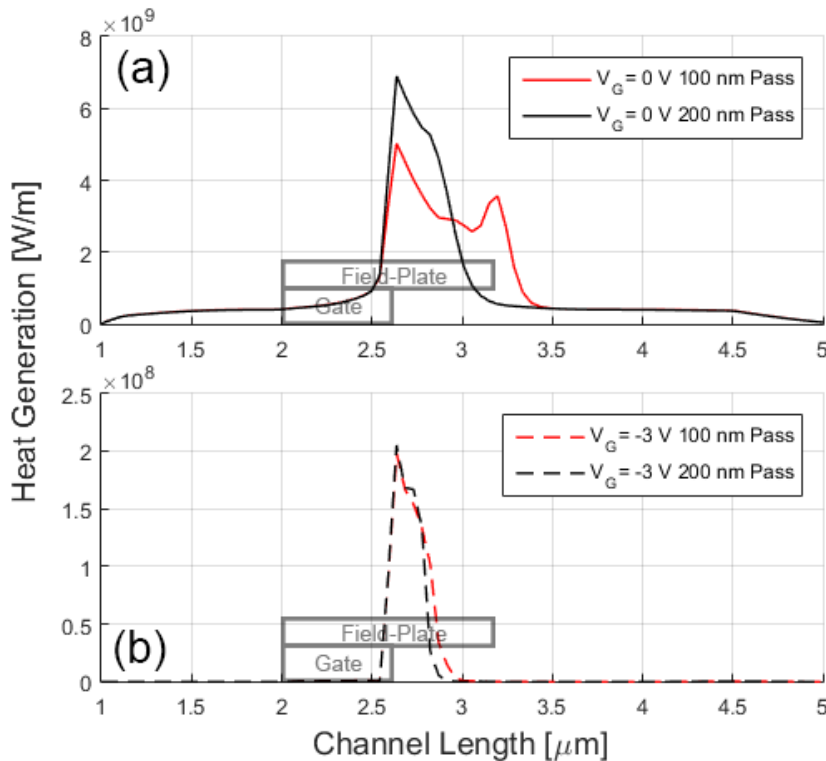


Figure 4.6. Linearized heat generation distribution along channel for 1200 nm field-plated AlGaIn/GaN HEMTs with $t_{\text{Si}_3\text{N}_4} = 100$, and 200 nm operating at (a) $V_G = 0$ V & $V_D = 7$ V and (b) $V_G = -3$ V & $V_D = 7$ V.

distribution of 100 nm passivation device is more uniform. However, the spreading effect on heat generation is not that significant compared to regulated electric field distribution for near pinch-off state. As explained in previous chapter, field-plate effect on power output is more crucial for extreme conditions such as $V_G = -3$ V since it increases breakdown voltage. However, it is not significantly effective on heat generation characteristic due to decreased power density and Joule heating at near pinch-off condition. When the passivation thickness is increased further than 200 nm, effect of field plate completely fades away and device starts to act as an I-gate device as observed in SiO₂ passivation device.

Below a certain threshold passivation layer thickness, electron leakage from device channel occurs decreasing power density output and breakdown voltage of the device. This thickness depends on layer material and properties. In this study, when a thickness of $t_{\text{Si}_3\text{N}_4} = 25$ nm is applied to AlGa_N/Ga_N HEMT, breakdown voltage and power density output decreased significantly. For SiO₂ simulations, similar outcome is obtained for $t_{\text{SiO}_2} = 5$ thickness.

On the other hand, increasing passivation layer thickness hinders electro-thermal effects of gate connected field-plate, thus have a negative impact both on electrical field distribution and heat generation along channel. For SiO₂ passivation layer, after the thickness of $t_{\text{SiO}_2} = 50$ nm field-plate effect completely vanished. Similar trend has been also observed when Si₃N₄ passivation layer is used. When a thickness of 200 nm is simulated, more localized heat generation is obtained compared to 100 nm passivation AlGa_N/Ga_N HEMT. Both electrical and thermal effects of field-plate are improved when passivation thickness is decreased to 100 nm.

For this reason, passivation thickness should be optimized for each AlGa_N/Ga_N HEMT design depending on the passivation material, field-plate type and length, and biasing conditions. Application of passivation as thin as possible without going below the threshold thickness is the key to design best performing AlGa_N/Ga_N HEMTs.

CHAPTER 5

CONCLUSION AND FUTURE RESEARCH

In power electronics industry, new semiconductor technologies are constantly researched to improve the capability of power devices. As the necessity of power increases every day, importance of innovative solutions becomes more remarkable. AlGa_N/Ga_N HEMTs revealed new possibilities with their high RF power densities, wide bandgaps and high breakdown voltages. They possess very high potential to lead the way to the future for power electronics. However, their low reliability prevents that potential to be fully used.

To increase AlGa_N/Ga_N HEMT reliability, many researchers work on analytical and numerical methods to find out new solutions on major electrical and thermal problems. Resolutions of experimental techniques may remain incapable to obtain true outputs of AlGa_N/Ga_N HEMTs. Moreover, cost and time requirements of experimental techniques also remain as a drawback for them. For this reason, effects of field-plate and passivation layer are widely analyzed individually either just from a thermal or electrical perspective. However, this study presents a combined electro-thermal approach to observe field-plate and passivation effect interconnected with each other.

In this thesis, first an electrical model is presented to simulate field-plate and passivation layer on AlGa_N/Ga_N HEMTs. The inputs, boundary conditions, parameters and the equations used to solve complex electron transport physics are explained in detail. The connection of electrical and thermal model is presented to observe combined electro-thermal effects. These simulations are used later to simulate different field-plates and passivation layers to maximize device reliability. I_D - V_D characteristics of the simulation are compared with experimental electrical data in order to validate the model and obtain realistic results.

A comprehensive study on electro-thermal effects of field-plate is conducted. Power density output, breakdown voltage, electric field distribution as well as Joule heating data are obtained from electrical simulations. To analyze self-heating effect on hotspot, Joule heating is used as an input function to thermal simulation maximum temperature dependent on biasing condition, field-plate, and its length are obtained. Electrical and thermal outcomes of field-plate utilization are discussed in detail. A comparison between thermal model and experimental infrared (IR) and thermo-reflectance (TR) is analyzed from one of our previous researches to validate thermal findings.

A similar approach is used to study passivation effect. SiO₂ and Si₃N₄ passivation layers with different thicknesses are analyzed to obtain electron leakage, breakdown voltage and power density of the AlGaN/GaN HEMTs. Electric field distributions and Joule heating data is also obtained both for I-gate and field-plated devices. By using an interconnected method, passivation effect on field-plate is also analyzed and passivation thickness adjustment according to field-plate is done to optimize AlGaN/GaN HEMT performance and increase device reliability.

Significant improvements and key features on AlGaN/GaN HEMTs are achieved such as:

- 6% decrease in hotspot temperature is obtained by utilizing 1200 nm field-plate for a device operating with 4.3 W/mm power density.
- Effect of field-plate for partially pinched-off condition, $V_G = -3$ V, is more crucial since it improves power density output and breakdown voltage of the device by preventing electron leakage from channel.
- Effect of field-plate decays if SiO₂ and Si₃N₄ passivation layers are applied thicker than 50 and 200 nm, respectively.
- Due to increased electron leakage, breakdown voltage and power density output of devices significantly decrease when SiO₂ and Si₃N₄ passivation layers are applied thinner than 10 and 25 nm, respectively.

- Our thermal model is obtained to be accurate up to 2% error margin from comparison with IR and TR measurements.
- Experimental methods, such as thermo-reflectance measurements, deviates around 18% from real hotspot temperature. Without using analytical and/or numerical methods, real hotspot temperature cannot be obtained.

There are still many other ways to improve analytical and numerical simulations to obtain more accurate results. If the necessary improvements can be made, combined electro-thermal models can be used more in HEMT designing process. These improvements may be:

- Further validation of electro-thermal model by fitting obtained simulation temperature with a thermo-reflectance experimental result. By calculating the average temperature on the top of the simulated device for an area of 300 nm x 300 nm, simulation finding can be compared to an experimental data to validate numerical model.
- Different field-plate types, such as source connected field-plate, can be analyzed.
- Effect of gate length, source-gate separation, drain-gate separation can be analyzed since all of these dimension effect device performance significantly. By conducting these analyses and further validating the model, a guide to fabricate AlGaIn/GaN HEMTs with maximized performance and reliability can be created.
- Finally, different cooling techniques to decrease hotspot temperature for different biasing conditions can be easily tried with a validated electro-thermal model.

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