GAN-BASED ROBUST LOW-NOISE AMPLIFIER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

OĞUZ KAZAN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

JULY 2018

Approval of the thesis:

GAN-BASED ROBUST LOW-NOISE AMPLIFIER

submitted by **OĞUZ KAZAN** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Tolga Çiloğlu
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Hatice Özlem Aydın Çivi
Supervisor, **Electrical and Electronics Engineering Dept., METU** _____

Dr. Fatih Koçer
Co-Supervisor, **Analog Devices Inc., Chelmsford, MA, USA** _____

Examining Committee Members:

Prof. Dr. Sencer Koç
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Hatice Özlem Aydın Çivi
Electrical and Electronics Engineering Dept., METU _____

Assist. Prof. Dr. Serdar Kocaman
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Ekmel Özbay
Electrical and Electronics Engineering Dept., Bilkent University _____

Date: 10.07.2018

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Oğuz Kazan

Signature:

ABSTRACT

GAN-BASED ROBUST LOW-NOISE AMPLIFIER

Kazan, Oğuz

M.S., Department of Electrical and Electronics Engineering

Supervisor: Prof. Dr. Hatice Özlem Aydın Çivi

Co-Supervisor: Dr. Fatih Koçer

July 2018, 92 pages

This thesis presents the theory, design and evaluation of low-noise amplifiers (LNAs) with high input power immunity, built on GaN/SiC substrate. Two separate X-band (8-12 GHz) LNAs are designed and sent out for production. After the manufactured samples are received, they are measured and evaluated. Measurement results show that both LNAs have a gain of more than 20 dB. One LNA achieves a noise figure of less than 2 dB, while the second one has a noise figure of less than 2.5 dB. Using three-stage topology, high linearity is achieved with an OIP_3 of 29 dBm at 0.6 W power dissipation for one of the LNAs, and an OIP_3 of 28.3 dBm is achieved at 0.36 W power dissipation for the other LNA. The robustness tests show that the circuits survive 2.5 W (34 dBm) input power. This survivability performance enables the use of presented LNAs in electronic warfare systems without a need of a diode limiter. With a size of just 2.8×1.3 mm^2 (3.6 mm^2) the presented LNAs are compact when compared to the state of the art. The circuits are realized using the 0.25 μm Power GaN/SiC HEMT process by WIN Semiconductor.

Keywords: Gallium Nitride, HEMT, Low-Noise Amplifiers, MMIC, Noise Figure, Scattering Parameters.

ÖZ

GAN TABANLI DAYANIKLI ALÇAK GÜRÜLTÜLÜ YÜKSELTEÇ

Kazan, Oğuz

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Prof. Dr. Hatice Özlem Aydın Çivi

Ortak Tez Yöneticisi: Dr. Fatih Koçer

Temmuz 2018, 92 sayfa

Bu tezde düşük gürültülü yükselteçlerin teori, tasarım ve değerlendirilmesi açıklanmıştır. X-bandında (8-12 GHz) çalışan ve yüksek giriş gücüne dayanıklı iki düşük gürültülü yükselteç bir GaN/SiC tabanda tasarlanmış ve bu tasarımlar üretime gönderilmiştir. Tasarımlar üretimden geldikten sonra bunların ölçümleri yapılmış ve çıkan ölçüm sonuçları değerlendirilmiştir. Ölçüm sonuçlarına göre iki tasarım da 20 dB'den fazla kazanca sahiptir. Tasarımlardan ilkinin gürültü figürü 2 dB'den az ve ikincinin gürültü figürü 2,5 dB'den az olarak ölçülmüştür. Tasarımda, üç katlı topoloji kullanarak yüksek doğrusallık sağlanmıştır. Bu sayede, tasarlanan düşük gürültülü yükselteçlerden ilkinin güç tüketimi 0,6 W ve OIP_3'ü 29 dBm'dir. Diğer düşük gürültülü yükseltecin güç tüketimi 0,36 W ve OIP_3'ü 28,3 dBm'dir. Dayanırlık testleri iki tasarımın da 2,5 W'lık (34 dBm) girdi gücüne dayanabildiğini göstermiştir. Bu dayanırlık değerleri sunulan bu yükselteçlerin herhangi bir sınırlandırıcıya ihtiyaç duyulmadan elektronik savaş sistemlerinde kullanılabileceğini göstermektedir. 2.8 × 1.3 mm^2 (3.6 mm^2) boyutuyla tasarımlar günümüz literatürdeki tasarımlara göre küçüktür. Tasarımlar yapılırken WIN Semiconductor'un 0,25 μm Power GaN/SiC HEMT teknolojisi kullanılmıştır.

Anahtar kelimeler: Galyum Nitrat, HEMT, Alçak Gürültülü Yükselteçler, MMIC, Gürültü Figürü, Saçılma Parametreleri.

To my family

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to Prof. Dr. Hatice Özlem Aydın Çivi, my current supervisor at METU, and to Dr. Fatih Koçer, my former supervisor (now my co-supervisor) at METU, for their continuous support and valuable guidance during my thesis.

I am indebted to the rest of my thesis committee, namely Prof. Dr. Sencer Koç, Prof. Dr. Şimşek Demir, Assist. Prof. Dr. Serdar Kocaman and Prof. Dr. Ekmel Özbay for their insightful comments that contributed to my thesis.

I would like to acknowledge The Scientific and Technological Research Council of Turkey (TÜBİTAK-EEEAG-115E750) for funding the project. I would like to thank ASELSAN for fabricating the PCBs and helping us with the measurements. I would like to acknowledge Hakan Coşkun for the fabrication of PCBs, and I would also like to thank Enis Kobal, Onur Memioğlu and Çağdaş Yağbasan for their help in the measurements.

In addition, I would like to acknowledge Dr. Adnan Gündel from Mikro-Tasarım A.Ş. and my fellow lab-mates from RFIC Research Group at METU, Işınsu Turan and Ömer Fevzi Güngör for their valuable support during implementation of the work presented in this thesis.

Last but not the least, my very profound gratitude is given to my beloved family for their unfailing support throughout my life. This accomplishment would not have been possible without them. Thank you.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

A low-noise amplifier (LNA) generally resides as the first stage in a radio-frequency (RF) receiver system. The purpose of an LNA is to amplify the desired small-powered signal from the antenna with as minimum degradation of the signal-to-noise ratio as possible. Thus, an LNA is very crucial since its noise performance directly dominates in a cascaded RF receiver system as will be explained in Section 2.1.5. The primary performance metrics of an LNA are a high gain and a slight noise performance degradation (noise figure). An example of an RF receiver block diagram is given in Figure 1.1.

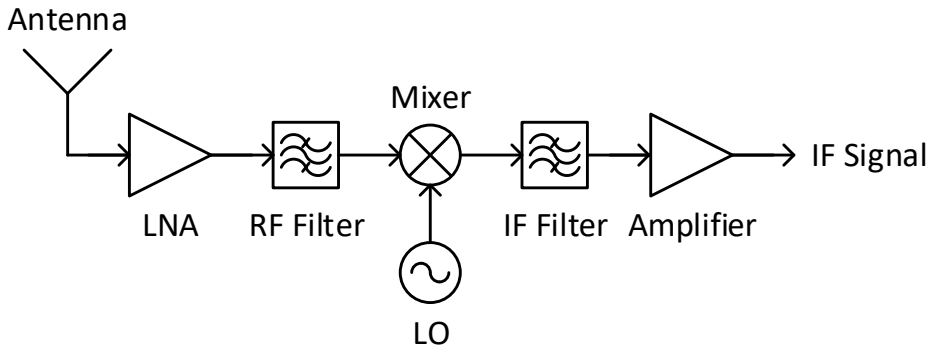


Figure 1.1 An example of an RF receiver block diagram [1]

This thesis presents the theory, design and evaluation of two monolithic microwave integrated circuit (MMIC) LNAs which are built on gallium nitride (GaN) on silicon carbide (SiC) substrate. The presented designs are fabricated using a 0.25 μm Power GaN/SiC HEMT process from WIN Semiconductor.

The LNAs presented in this work are designed to operate in the X-band (8-12 GHz). As can be seen in the literature and in the industry [2]–[6], a vast number of LNAs built on gallium arsenide (GaAs) substrates that offer excellent noise figure values (with lower noise figure than reported in this thesis) which can be as low as 0.5 dB over the X-band have been reported. Therefore, the decision to build LNAs on an arguably inferior process like GaN might seem counter-intuitive. In order to explain the motivation behind this decision, one particular and very common use of the X-band frequencies needs to be detailed; Electronic-warfare.

Transmitter and receiver (T/R) frontend modules are key components to active phased array antennas for electronic warfare applications. Inside a T/R module, there are two main components, namely a power amplifier (PA) and a low-noise amplifier. Typical block diagrams for T/R systems implemented built on GaAs and GaN/SiC substrates are given in Figure 1.2.

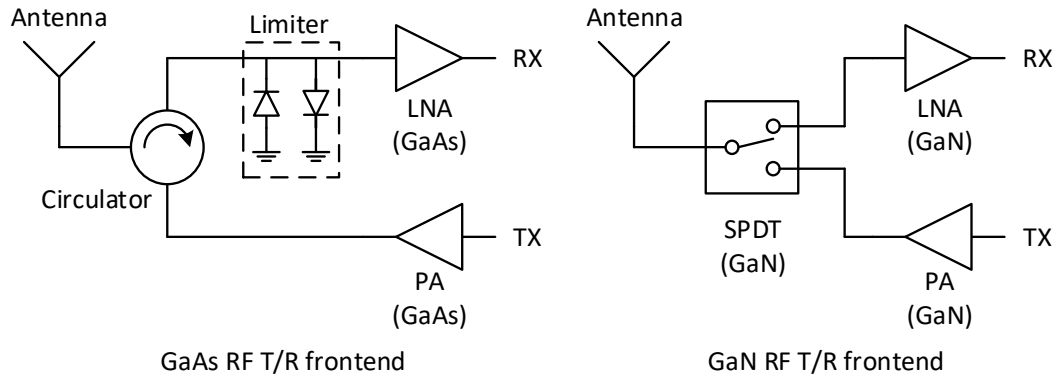


Figure 1.2 Typical block diagrams for T/R systems implemented built on GaAs and GaN/SiC substrates (SPDT: Single-pole double-throw switch) [7]

Most of today's GaAs MMIC PAs in T/R modules may have output power levels in the range of 5 W to 10 W. To meet future requirements, higher output power levels and increased power added efficiency (PAE) values are advantages for performance improvement. Higher breakdown voltage of GaN compared to GaAs enables GaN devices to handle very high powers and makes GaN devices very promising for these applications [8]. Another important consideration for these transceivers is input power survivability for the LNA. The receiver of a radar may be subject to high-power input signals (1-5 W), and these aggressive high-power input signals may permanently

damage the LNA and the full receiver chain if not protected adequately. A common method to protect against these aggressors is to use high-power limiter PIN diodes in front of the GaAs LNA, which has inherently good noise properties. However, these limiters generally can not be integrated into the same substrate as the LNA itself, which increases the system size and cost. Moreover, these extra diodes in front of the LNA increases the system noise. Furthermore, the spike leakage of limiter circuits due to the PIN diodes is another consideration for the protection of the LNA. GaN devices, on the other hand, are intrinsically robust to high powers, thanks to the high bandgap of GaN, which eliminates the need for the input limiter circuitry [9]–[11]. These are the reasons why GaN high-electron mobility transistor (HEMT) technology is chosen for this work.

1.1 Literature Survey

In the last two decades, there have been considerable amount of efforts spent on GaN LNAs in the literature. The LNAs are designed in various topologies covering various frequencies. The S-, C- and X-bands are particularly targeted due to their use in radar, telecommunications and electronic warfare [12]. There are many GaN LNAs recently reported in both monolithic and hybrid technologies. Generally, the topology used in the designs are cascaded single- or multiple-transistor amplifier stages. These amplifier stages are, namely, common-source, common-gate, cascode and common-drain amplifier. Before discussing the recently reported LNAs in detail. The use of these amplifier stages should be made clearer.

The most commonly used amplifier stage is common-source (CS) amplifier. As one might remember from analog electronics courses, it is a good voltage-amplifier. A schematic for a common-source amplifier is shown in Figure 1.3.

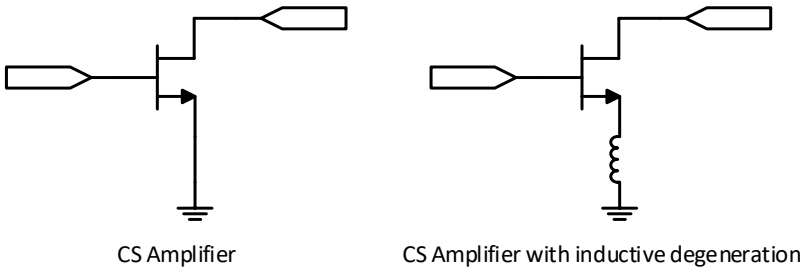


Figure 1.3 A schematic for a common-source amplifier

This stage is generally used for the power gain. Although it has poor isolation, this stage has good low-noise and good linearity properties [13]. Also, due to Miller effect, a CS amplifier has a narrow band operation [14]. It should also be mentioned that in order to improve its noise properties, a degeneration inductor to the common-source amplifier can be added [15]. On the other hand, the common-gate (CG) amplifier has a good isolation [13]. It is generally used with a CS stage to create a cascode topology. Schematics for a CG and cascode amplifiers are given in Figure 1.4.

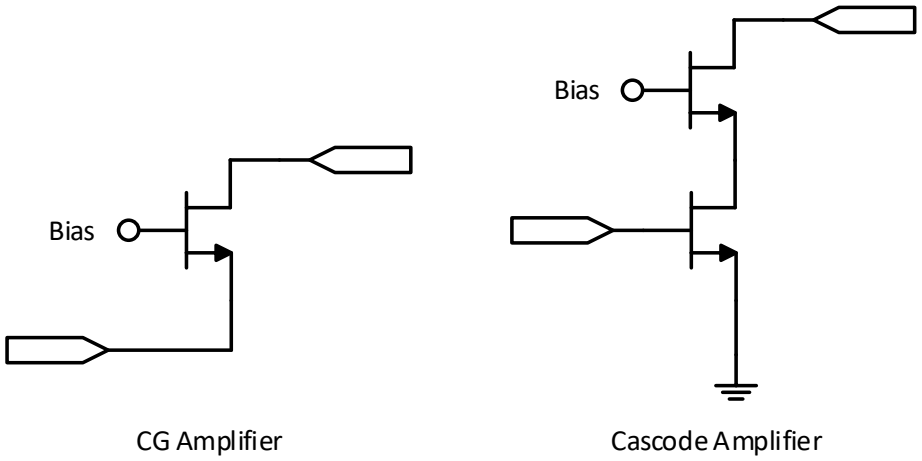


Figure 1.4 Schematics for common-gate and cascode amplifiers

The cascode topology has a very good isolation and a good linearity. Thanks to its isolation, matching circuits for that topology can easily be designed [13]. The most noticeable advantage of a cascode amplifier is the suppression of Miller effect. This helps the stage to have a wider operation band than a common-source stage. One drawback is the higher power dissipation due to the doubled supply voltage. Moreover, the cascode amplifier has slightly worse noise properties than a CS stage [11][13]. When the design library does not include non-linear transistor models but only the linear models, this topology as it is shown in Figure 1.4 can not be implemented. To overcome this problem, bias circuitry of the CS and CG stages of a cascode amplifier can be separated as shown in Figure 1.5.

However, due to the extra periphery for the bias circuitry, the circuit occupies more area than a CS stage. Also, this extra periphery may result in noise performance degradation and bandwidth reduction.

Common-drain (CD) topology is rarely used in the literature. As one again can remember from analog electronics courses, the topology is used for the amplifier to have low output impedance. In the work of [17], CD topology is used at the output stage as an impedance transformer in order to increase the operation bandwidth. A schematic for a CD topology is illustrated in Figure 1.6.

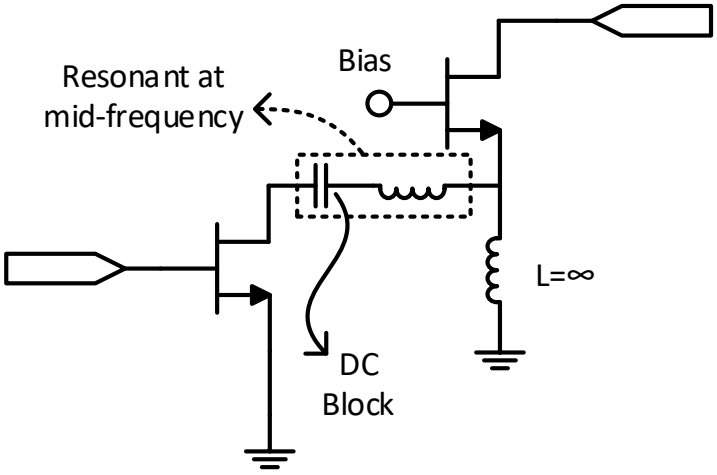


Figure 1.5 A schematic for a simple cascode amplifier with separated stages

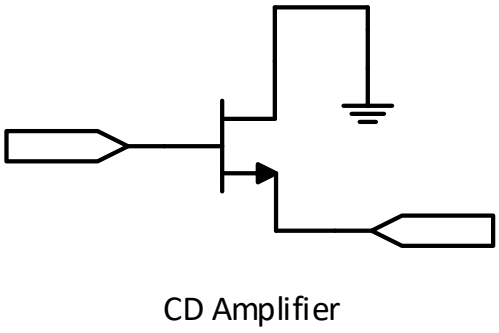


Figure 1.6 A schematic for a common-drain amplifier

It should be noted than in none of Figure 1.3, Figure 1.4, Figure 1.5 and Figure 1.6, the complete bias circuitry is shown. After these explanations, the discussion for the recently reported GaN LNAs can be discussed.

In the literature, particularly, there are some GaN LNAs in hybrid technology (composed of multiple integrated circuits -ICs- mounted on a printed circuit

board -PCB-). The bandwidth of these designs are up to 3 GHz and these LNAs operate at low frequencies compared to MMIC counterparts [18]–[21]. In the design of [18], an extremely high linearity of 54 dBm OIP_3 (which is discussed in Section 2.2.2) at 2 GHz is reported. Also, the noise figure (which is discussed in Section 2.1) of that design is 2 dB. The work in [19] achieves a noise figure of 1.7 dB while having a gain of 22 dB. Moreover, in the work of [20], a noise figure of less than 2 dB between 1.7 and 2.3 GHz is reported. The design in [21] achieves a noise figure of between 0.5 and 1.6 dB, and the design operates up to 3 GHz. Therefore, the recently reported hybrid GaN LNAs can be said to have noise figures in the range of 0.5-2.0 dB.

Moving to MMIC technology, there is a vast number of LNAs operating over various frequency ranges. For example, in the work of [22], a noise figure of 2.9 dB reported while achieving a power gain of 17.2 dB over the S-Band (2-4 GHz). The work utilizes a cascode topology as the first stage and a CS topology as the second stage. For the C-band (4-8 GHz), a noise figure of less than 1.85 dB is achieved in [23]. This design utilizes only a single CS stage. For higher frequencies, the work of [24] achieves a minimum noise figure of 2 dB for the Ku-band (12-18 GHz). Also, a minimum noise figure of 1 dB is achieved in the design of [25] for the Ka-Band (27-40 GHz).

Moving to the targeted X-band for this thesis, in the work of [17], a wideband two-stage LNA is designed. The first stage has a CS topology to provide a high gain, and the second stage has a CD topology to act as an impedance transformer. Although this design has very wide operation band (4-16 GHz), it has the low gain of about 11 dB over most of the operating frequencies. Also, even though it is not reported, the die seems to consume a large area compared to the other GaN LNAs in the literature. In order to increase the gain, another CS stage can be added as the second or the third stage. However, this might shrink the bandwidth and will increase the noise and the die area. In the work of [26], a two-stage LNA is designed. Although the design is composed of only two stages, the die occupies significantly large area of 5 mm^2, which will be given in Section 4.7. Also, the noise figure of the that design can be considered to be high (2.5 dB). In the work of [7], the designs seem to have high performances in many aspects. However, the designs occupy large areas (6 mm^2). Finally, in the work

of [27], there are two designs and both design have quite good performances. However, neither of the designs can cover the whole X-band.

A brief summary of some recently reported GaN LNA MMICs is given in Table 1.1.

Table 1.1 A brief summary of some recently reported GaN LNA MMICs

Reference	**Operating Frequency (GHz)**	**Noise Figure (dB)**	**Gain (dB)**	**Topology**
[22] 2013	2-4.5 (for S-Band)	2.9	17.2	Cascode-CS
[23] 2004	4-8 (C-Band)	<1.85	10.9 (at 6 GHz)	CS
[24] 2013	12.8-14.8 (for Ku-Band)	>2.0	>20	CS-CS-CS
[25] 2016	30-39.2 (for Ka-Band)	>1.0	~25	CS-CS-CS
[17] 2007	4-16	1.45 min	11-14.5	CS-CD
[26] 2012	7-12	2.5	14	CS-CS
[7] 2013	8-12	<1.8	>14	CS-CS
[7] 2013	7-11	>2.0	>18	CS-CS
[27] 2016	8-10	1.3 max	24.27	CS-CS-CS
[27] 2016	10-12	1.3-1.75	24.425.2	CS-CS-CS

It should be mentioned again that the introduction of GaN LNA generally aims to eliminate the need of GaAs LNA used with a limiter in the front. In Table 1.1, the noise figures of the LNAs are in the range of between 1.3 and 2.5 dB. These low noise figure values prove that the GaN technology indeed can replace the chipsets composed of GaAs LNA and a limiter. One such commercial chipset is TGM2543-SM by Qorvo [28]. The noise figure of the product is around 2 dB, and the product has a gain of 17 dB. The operating frequency is between 4 and 20 GHz. Hence, the GaN LNA designs in the literature have better noise figure than some of such products.

Considering the most important considerations for an LNA, namely the gain and the noise figure, some goals are set for the designs in this work. The goals for the LNA design for this work is given in Table 1.2.

Table 1.2 The goals for the LNA design

Operating Frequency (GHz)	8-12 (X-band)
Noise Figure (dB)	<2
Gain (dB)	>20
Return Losses (dB)	>10
Output P1dB (dBm)	>15
Input Power Survivability (W)	>2

1.2 Organization of the Thesis

The thesis is organized as follows. Firstly, most of the basic concepts for LNAs are given in Chapter 2. In that chapter, it is assumed that the reader is familiar with the concepts given in the related undergraduate courses, such as analog electronics, microwave engineering, feedback/control theory, semiconductor devices, random processes etc. Then, the design methodology of the circuits is presented and the corresponding electromagnetic (EM) simulation results are given in Chapter 3, along with the complete schematics and layouts of the circuits. In Chapter 4, the measurement methodology and the measurement results along with their comparison with the simulation results are presented. The chapter also includes a discussion on the back-fitting efforts done to reduce the discrepancy between the simulated and measured results. The thesis is completed with a conclusion section, summarizing the work done, and a discussion about the future work.

CHAPTER 2

BASIC CONCEPTS IN LNA DESIGN

RF design requires knowledge on various fields, including microwave, telecommunications, and electronics. The theories in RF design also have different analysis tools. For example, when modelling noise, one uses random processes, whereas to analyze stability, transfer functions of s-domain can be used. When deriving gain equations, scattering parameters are used. On the other hand, the derivations of equations regarding linearity require the usage of power series.

In this chapter, the basic concepts regarding LNA design are discussed. For many of the equations, the derivations are available. The concepts introduced are general concepts that may also be applied to RF designs other than LNA.

2.1 Noise

Noise limits the performance of the RF systems as it determines the sensitivity of the receiver in the system. If noise did not exist in nature, RF receivers would detect arbitrarily small signals from arbitrarily far distances. In broadest sense, it is defined as “any signals except the desired signals”. For instance, a sine wave generator which carries no data at the input of a receiver amplifier can be considered as a noise source. In this section, however, the noise sources presented have only physical basis (occur as nature dictates), or at least they are considered to only have physical basis. These noise sources can not simply be filtered out, but at least their undesired effects can be minimized.

2.1.1 Thermal Noise

Johnson was the first to report measurements of noise in resistors. In the measurements reported, a vacuum tube amplifier with a resistor connected at the input was used [29]. Nyquist explained thermal noise using the principles in thermodynamics and statistical mechanics [30]. Mean-squared value (or variance) of the noise voltage across a resistor (or an element which has a frequency dependent complex impedance) is given by

$$\overline{v_t{}^2} = 4Rk_BT\Delta f, \tag{2.1}$$

where R is the real part of the impedance (in ohms) of the element under observation, which can be replaced by $R(f)$ if it is frequency dependent, k_B is the Boltzmann's constant (which is about 1.38065×10^{-23} J/K), T is the resistor's temperature (in kelvins), and Δf is the measurement bandwidth (in Hertz). The model of noisy resistor is shown in Figure 2.1.

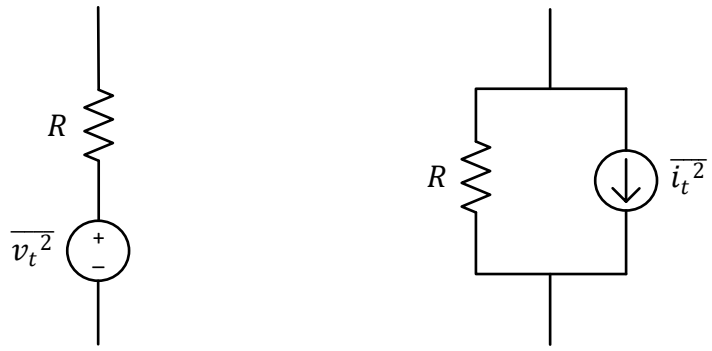


Figure 2.1 Representations of noisy resistor (G: conductance of the resistor)

As can be seen in Figure 2.1, a noisy resistor can be represented as a noiseless resistor in series with a noise voltage source (Thevenin equivalent), or as a noiseless resistor in parallel with a noise current source (Norton equivalent).

A simple circuit containing a noisy resistor and a matched load is given in Figure 2.2. For that circuit, the maximum noise power delivered to the load by the source resistor can be calculated as

$$P_{n,max} = \frac{\overline{v_t{}^2}}{2 \times 2R} = \frac{4Rk_BT\Delta f}{4R} = k_BT\Delta f. \quad (2.2)$$

For $T = 290\,K$ and $\Delta f = 1\,Hz$, the maximum delivered noise power is -174 dBm. This value sets the noise power delivered to an RF receiver at $T = 290\,K$ when the source impedance is matched to the input of the receiver, and directly affects the sensitivity of the system. Of course, one might argue that the inputs of most RF receivers are not connected to a source resistor of $50\ \Omega$ but an antenna. Indeed, noise contributed by the antenna is from back-ground noise, but in RF design, the calculation in (2.2) is assumed to be valid [31]. Also, it is reasonable to think these assumptions are for the noise measurement equipment but not for the application.

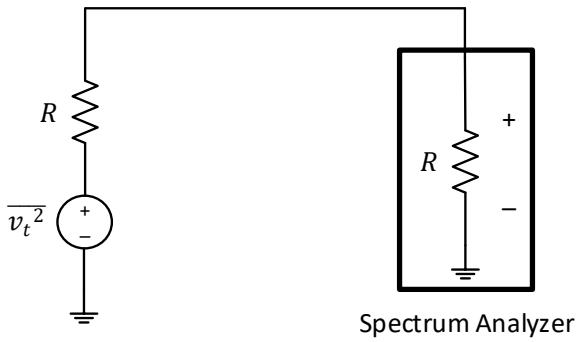


Figure 2.2 A noisy resistor connected to the input of a spectrum analyzer

Thermal noise spectrum is flat up to around 1 THz, and since it is almost not frequency-dependent in microwave frequencies (300 MHz – 300 GHz), it can be considered as white noise. As a more general case, Nyquist also showed that the mean-squared value of the noise power of a resistor is

$$\overline{v_t{}^2} = 4R\frac{hf}{e^{\frac{hf}{k_BT}} - 1}\Delta f, \quad (2.3)$$

where h is the Planck constant (which is about 6.62607×10^{-34} J/Hz), f is the frequency (in Hertz) and the rest of the variables are as in (2.1). At very high frequencies and/or at very low temperatures, the equation (2.1) can not be used, and for those cases, the equation (2.3) can be used instead.

For the sake of completeness, the plots of the power (dBm/Hz) delivered to the load in the circuit considering (2.1) and (2.3) are shown in Figure 2.3.

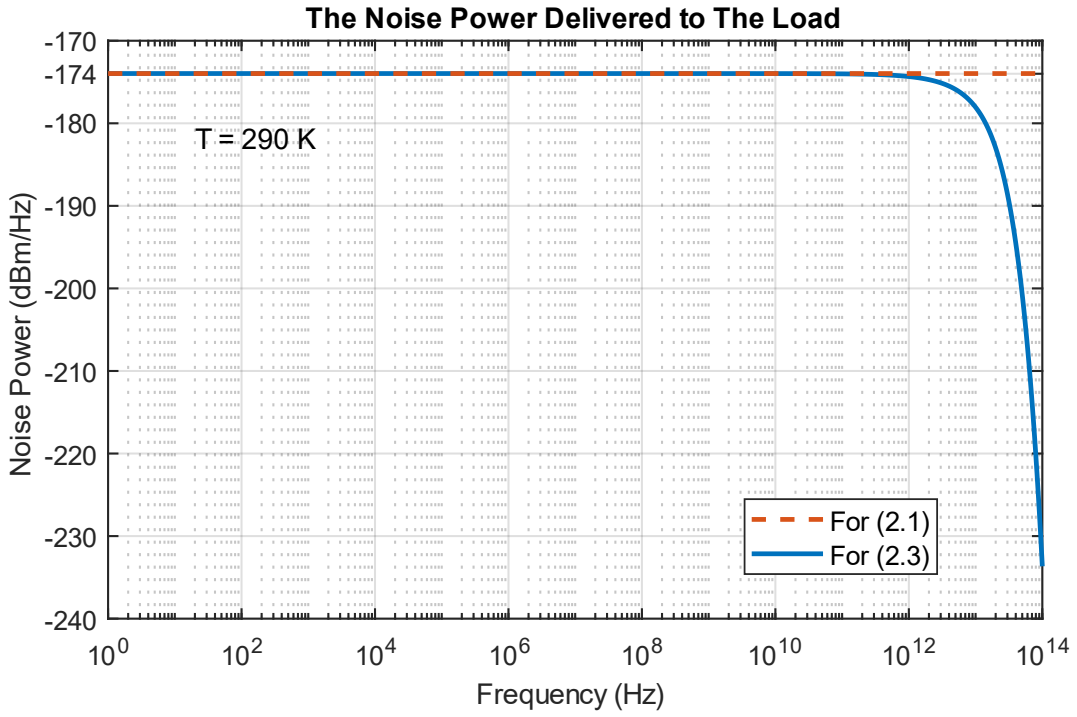


Figure 2.3 The noise power delivered to the load versus frequency

As can be seen the delivered noise power for (2.1) is indistinguishable from that for (2.3) up to around 1 THz. Of course, as f in (2.3) approaches zero Hertz, the equation (2.1) can be obtained.

2.1.2 Shot Noise

Shot noise comes from the discrete nature of the charge carriers. These carriers create a current, I, on average. The randomness of the arrival times causes the current to deviate from its average value, I, and the arrival times obey Poisson's statistics. The mean-squared value of the deviation from the current, I, can be expressed as

$$\overline{i_{shot}{}^2} = 2qI\Delta f, \tag{2.4}$$

where q is the elementary charge (which is about 1.60218 $\times 10^{-19}$ coulombs), I is the average current (in Amperes), and Δf is the measurement bandwidth (in Hertz). As can be seen from (2.4), the shot noise exhibits white noise characteristics. Shot noise requires there be a direct current flow, I, or there is no shot noise.

Shot noise can be suppressed if the transmission events are correlated [32][33]. For example, in a metallic conductor, there are correlations between charge carriers

[34]. On the other hand, in a *pn* junction, since the passage of the charge carriers are random and independent in the depletion region, and the energy barrier inside permits the current flow only in one direction, this process can be described by Poisson statistics [35].

2.1.3 Flicker Noise

At low frequencies of the noise spectrum, flicker noise is dominant. Flicker noise is also called 1/f noise as its power spectrum is nearly proportional to the inverse of the frequency. Its mechanisms have not been fully discovered yet. Interestingly, in addition to electronics, it can be observed in geology, biology, musical systems, etc. Moreover, it seems that its origins at different devices are quite different [36].

There are two competing models in the literature explaining flicker noise. These are McWhorter's number fluctuation theory and Hooge's mobility fluctuation theory. According to McWhorter, flicker noise is mainly a surface phenomenon and is generated by fluctuations in the number of charge carriers in the charge trapping surface states [37]. On the other hand, according to Hooge, flicker noise is a bulk phenomenon and it occurs due to the fluctuations in the mobility [38]. Also, there are combined models to fit as much published data as possible. There is no single model completely explaining all the phenomena, but at least it seems Flicker noise is partially explained.

In addition to those models, there are also empirical models. These models do not exactly reflect the models mentioned above. They are generally the simplified forms. According to Tsividis [39], for a common bulk CMOS process, one may find the input-referred voltage relation due to flicker noise as

$$\overline{v_{flicker}}^{\,2} = \frac{K}{{C_{ox}}'^{2}} \frac{1}{WL} \frac{1}{f^{c}} \Delta f, \tag{2.5}$$

where K is constant depending on the process, ${C_{ox}}'$ is the gate capacitance per area, W and L are the gate width and length, respectively, c is the process dependent constant (generally between 0.7 and 1.2), f is the frequency, and Δf is the measurement bandwidth.

2.1.4 Noise Theory for Linear Two-Ports

To quantify its quality, signal-to-noise ratio (SNR) of a signal is determined. It is defined as the ratio of the desired signal power divided by the noise power measured in a certain bandwidth (1 Hz for our case) and expressed as

$$SNR \triangleq \frac{P_{sig}}{N_s}, \tag{2.6}$$

where P_{sig} is the signal power, and N_s is the noise power.

As a useful measure for the two ports, noise factor (F) is used. It is defined as

$$F \triangleq \frac{total\ output\ noise\ power}{output\ noise\ power\ due\ to\ noise\ at\ the\ input}. \tag{2.7}$$

Sometimes, the equation (2.7) is not practical, and some manipulation may be needed. If the power gain of the two-port is G, the noise power at the input is N_s, the noise power added by the two-port to the output is $N_{amp,o}$, and the input signal power is P_{sig}, then

$$F = \frac{GN_s + N_{amp,o}}{GN_s}$$

$$F = \frac{\frac{1}{N_s}}{\frac{G}{GN_s + N_{amp,o}}}$$

$$F = \frac{\frac{P_{sig}}{N_s}}{\frac{GP_{sig}}{GN_s + N_{amp,o}}}$$

$$F = \frac{SNR_{in}}{SNR_{out}}, \tag{2.8}$$

where SNR_{in} is the signal-to-noise ratio of the signal at the input of the two port, and SNR_{out} is the signal-to-noise ratio of the signal at the output.

In practice, it is generally converted into decibels, and it is called noise figure (NF). It is defined as

$$NF \triangleq 10 \log_{10} F. \tag{2.9}$$

In fact, in different text books (or in simulators), these two terms might be used interchangeably, but in this text, these terms are used as defined in (2.7) and (2.9).

If one is concerned only with the input-output relation of a two port, it is undesired to deal with internal noise sources. Fortunately, a pair of noise sources referred to the input of the two-port can represent these internal noise sources, as shown in Figure 2.8.

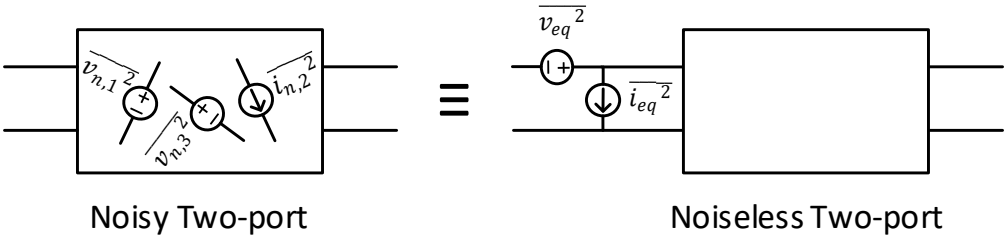


Figure 2.4 A noisy two-port and its equivalent representation

For Figure 2.1, the noise factor can be expressed as

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s v_n|^2}}{\overline{i_s^2}}, \tag{2.10}$$

where i_s is the noise due to the source, Y_s is the source admittance, and i_n and v_n are the input referred noise sources of the two-port. Since each internal noise source is possibly represented by the two input referred noise sources, these noise sources are correlated. It can be expressed that

$$i_n = i_c + i_u, \tag{2.11}$$

where i_c and i_u are the correlated and the uncorrelated components, respectively. The correlated component can be treated as proportional to v_n:

$$i_c = Y_c v_n, \tag{2.12}$$

where Y_c is the correlation admittance. Using (2.11) and (2.12), (2.10) can be modified as

$$F = \frac{\overline{i_s^2} + \overline{|i_u + (Y_c + Y_s)v_n|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2\overline{v_n^2}}{\overline{i_s^2}}. \tag{2.13}$$

Now, in (2.13), the noise sources are uncorrelated. We can convert these noise sources into hypothetical noise resistances and conductances;

$$R_n \triangleq \frac{\overline{v_n}^2}{4k_B T\Delta f}, \tag{2.14}$$

$$G_u \triangleq \frac{\overline{i_u}^2}{4k_B T\Delta f}, \tag{2.15}$$

$$G_s \triangleq \frac{\overline{i_s}^2}{4k_B T\Delta f}. \tag{2.16}$$

Using these equivalences, the noise factor equation can be modified as

$$\begin{aligned} F &= 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} \\ &= 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s}, \end{aligned} \tag{2.17}$$

where Y_c and Y_s are decomposed into their reactance and susceptance components. Integrating the equation with respect to the source admittance and setting it equal to zero, (2.18) and (2.19) can be obtained.

$$B_s = -B_c = B_{opt}, \tag{2.18}$$

$$G_s = \sqrt{\frac{G_u}{R_n} + {G_c}^2} = G_{opt}. \tag{2.19}$$

Therefore, modifying the impedance seen by the input of the two-port, the noise factor can be minimized. Z_{opt} $(1/Y_{opt})$ is thus the impedance the two-port need to see to minimize its noise factor. Since the source admittance for the minimum noise factor are expressed in terms of resistances and conductances, it may now be appreciated why the noise sources are converted.

Combining the equations, the minimum noise factor equation can be obtained as

$$F_{min} = 1 + 2R_n\left[G_{opt} + G_c\right] = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + {G_c}^2} + G_c\right]. \tag{2.20}$$

F_{min} is the minimum noise factor the two-port can achieve if it was terminated with Z_{opt} at its input. The noise factor can also be expressed in terms of F_{min} and the source admittance [15][40] as

$$F = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right]. \quad (2.21)$$

Moreover, the noise factor (2.21) can also represented in terms of optimum source reflection coefficient, Γ_{opt}, and source reflection coefficient, Γ_s, [40] as

$$F = F_{min} + \frac{4R_n}{Z_o}\left[\frac{\left|\Gamma_{opt} - \Gamma_s\right|^2}{\left|1 + \Gamma_{opt}\right|^2\left(1 - |\Gamma_s|^2\right)}\right], \quad (2.22)$$

where Z_o is the characteristic impedance of the system, which is $50\ \Omega$ in general. According to (2.22), source impedance contours for a constant noise factor can be plotted on a Smith chart. These contours appear to be non-overlapping circles (see Figure 2.5). Constant noise figure circles are an important and useful tool when designing an LNA. For the LNA design, the linear models of transistors (touchstone file) generally include data for F_{min}, R_n/Z_o and Γ_{opt} in addition to its S-parameters.

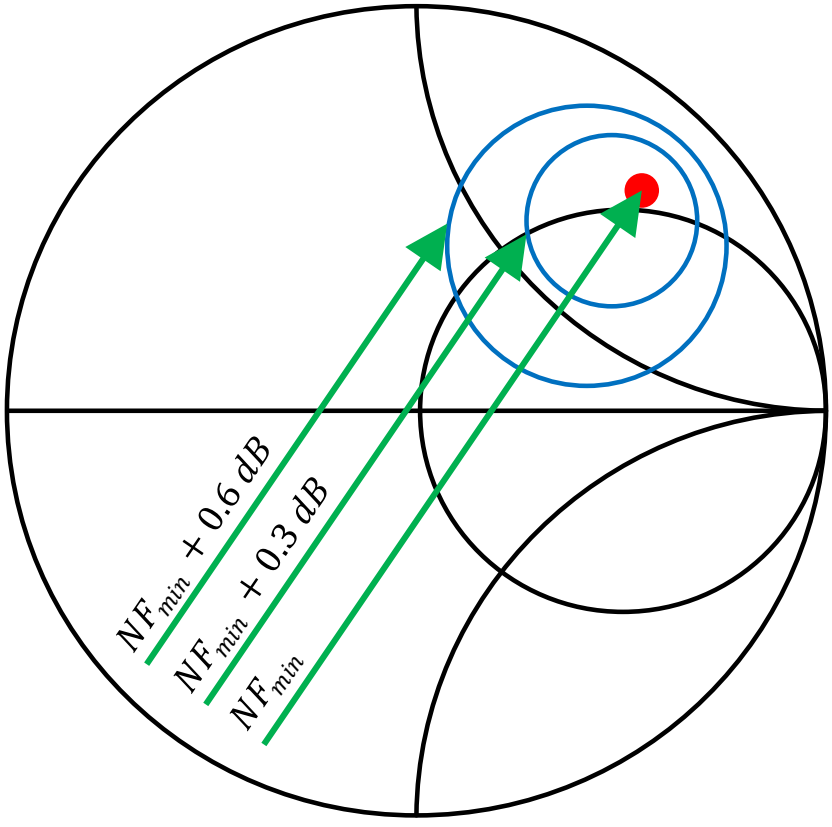


Figure 2.5 Noise figure circles (blue) and the optimum impedance point (red) on a source plane

2.1.5 The Friis' Formula for Noise

Since an LNA may be composed of multiple cascaded stages, the effect of each stage on the overall noise performance may need to be known. A simple two-stage amplifier is given in Figure 2.6.

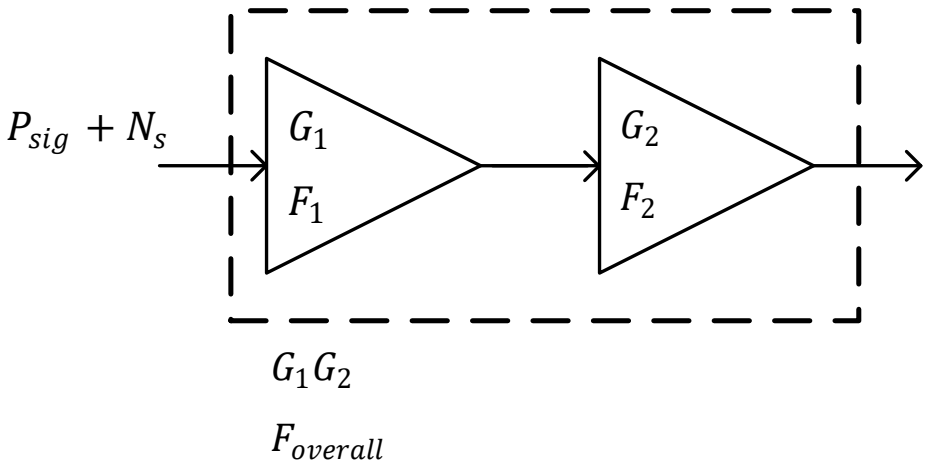


Figure 2.6 A two-stage amplifier

The noise factor for an amplifier block can be expressed as

$$F_i = \frac{G_i N_s + N_{out,i}}{G_i N_s} = 1 + \frac{N_{in,i}}{N_s}, \tag{2.23}$$

where $N_{in,i}$ is the noise contribution by a stage referred to the input. Then, input-referred noise for each stage is found as

$$N_{in,i} = N_s(F_i - 1). \tag{2.24}$$

For the overall amplifier, the input referred noise is

$$N_{in,overall} = N_{in,1} + \frac{N_{in,2}}{G_1} = N_s(F_1 - 1) + \frac{N_s(F_2 - 1)}{G_1}. \tag{2.25}$$

Hence, using (2.23), the overall noise factor can be obtained as

$$F_{overall} = F_1 + \frac{F_2 - 1}{G_1}. \tag{2.26}$$

The general formula for a multiple stage amplifier is

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \ldots \tag{2.27}$$

This equation is known as Friis' formula for noise. By inspecting this formula, it can be concluded that the first stage of an amplifier must have the lowest noise factor and the highest power gain for the amplifier to have a better noise performance. It should be noted that this formula is valid when every stage is conjugately matched, which is usually the case when each stage is designed to match a characteristic system impedance (e.g. 50 Ω). Also, this formula explains why an LNA is generally the very first stage of an RF receiver.

2.1.6 Noise Factor of a Passive Two-Port

The calculations and formulas for the minimum noise factor in the previous sections are used for the two-ports containing at least one active element. There might be cases when we need to know how to determine the noise factor of a two-port containing only passive elements. For instance, in Figure 2.7, there is an amplifier whose noise factor needs to be determined. However, when taking measurements regarding noise, the effects of the passive networks (e.g. microstrip lines -MS- for PCB measurements or coaxial cables for probe station measurements) connected to the input and output of the amplifier must be accounted for since they can not simply be discarded when measuring.

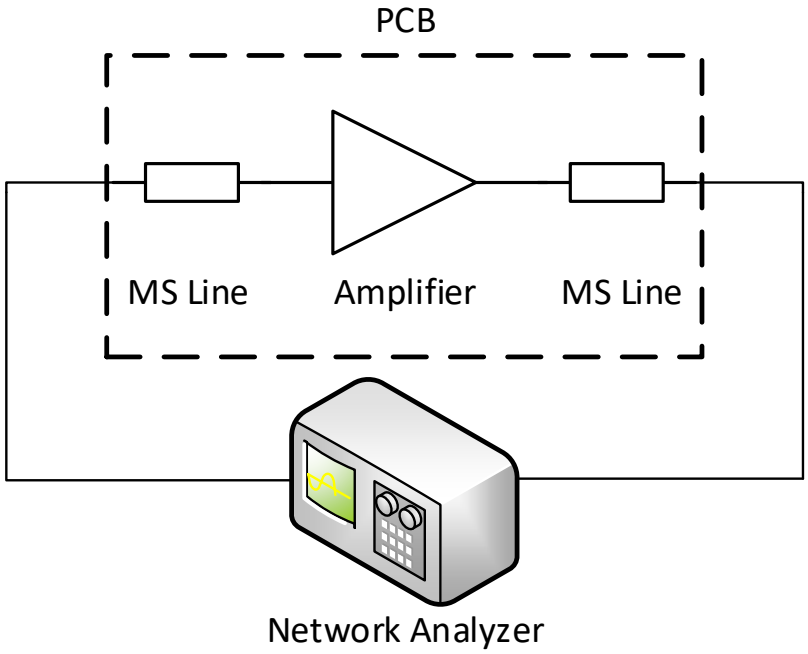


Figure 2.7 An example of noise factor (noise figure) measurement setup

In Figure 2.8, a passive network is given (e.g. an attenuator). The network is conjugately matched in the frequency band of interest.

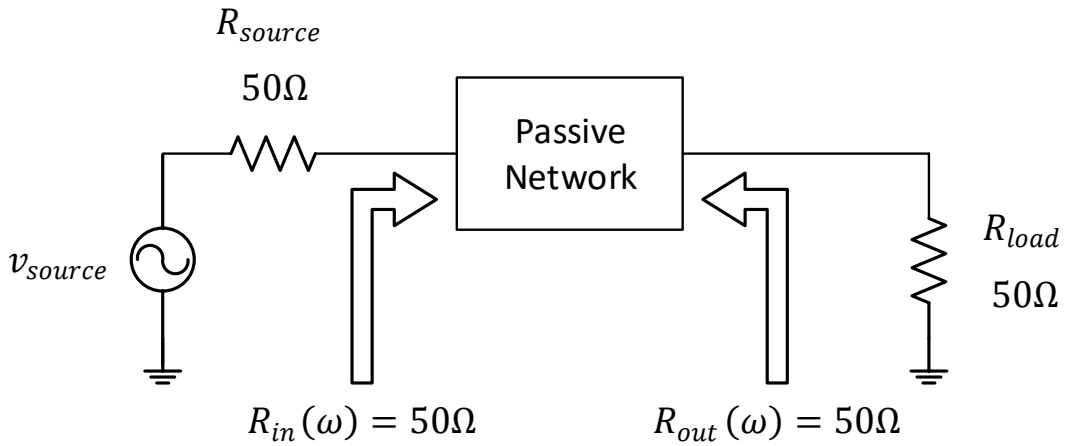


Figure 2.8 A passive network connected to a source and a load

Similar to the discussion for the thermal noise, the amount of noise introduced to the load is identical to that introduced to the input of the two-port;

$$N_s = \left(4R_{source}k_BT\Delta f \times R_{in}(\omega)\right)/\left(R_{source} + R_{in}(\omega)\right)^2 \quad (2.28)$$

$$N_{two-port,o} = (4R_{out}(\omega)k_BT\Delta f \times R_{load})/\left(R_{load} + R_{out}(\omega)\right)^2 = N_s \quad (2.29)$$

$$R_{source} = R_{load} = R_{in}(\omega) = R_{out}(\omega) = 50\ \Omega \text{ and } \Delta f = 1\ Hz \quad (2.30)$$

If the power attenuation of the two port is A $(1/G)$, the output signal is

$$P_{sig,o} = \frac{P_{sig,i}}{A}. \quad (2.31)$$

Using Figure 2.9, the noise factor of a passive two port is

$$F = \frac{\frac{P_{sig,i}}{N_s}}{\frac{P_{sig,o}}{N_{two-port,o}}} = \frac{\frac{P_{sig,i}}{N_s}}{\frac{P_{sig,i}/A}{N_s}} = A. \quad (2.32)$$

Therefore, using Friis' formula, the noise factor of the amplifier can be found if the gain of the amplifier, the overall noise factor and the attenuations of the networks at the input and the output are known.

2.2 Linearity

Linearity affects the performance of RF systems, and it sets the upper limit of the dynamic range. These effects can not be predicted by the small-signal models of the components in the circuit.

This section discusses the effects of non-linearity for memoryless systems, whose output at a time depends on the input only at that time. The output is represented using power series, and it is assumed that at the input signal levels of interest, the effects of the forth order or higher terms will be insignificant. Such a system can be approximated by

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t). \quad (2.33)$$

The examples of non-linearity effects are gain compression, intermodulation, cross modulation and harmonic distortion. Since gain compression and intermodulation concepts are used in the dynamic range discussion, only these concepts are explained.

From this discussion, one might infer that non-linearity is always an undesirable effect. However, it should be stated in advance that this is certainly not true as these effects can be used in a useful way. For example, when designing a mixer, the effects of non-linearity must be used. Another example is, a non-linearity effect of harmonic distortion enables the design of THz radiation sources even when the maximum oscillation frequencies (f_{max}) of the transistors are lower than the frequency of the desired signal [41][42].

2.2.1 Gain Compression

In analog and RF circuit analyses, the signals of interest are generally assumed to be small-signal. In fact, the signals may be high, and its non-linear effects must be considered. If a sinusoidal signal of a frequency, ω, and an amplitude, U, as

$$v_i(t) = U\cos(\omega t) \quad (2.34)$$

is applied to a circuit, then the output voltage, according to (2.33), can be modelled as

$$v_o(t) = a_1 U\cos(\omega t) + a_2[U\cos(\omega t)]^2 + a_3[U\cos(\omega t)]^3. \quad (2.35)$$

Using trigonometric identities, the equation (2.35) can be rearranged as

$$
\begin{aligned}
v_o(t) &= \left[\frac{1}{2}a_2U^2\right] \\
&+ \left[a_1U + \frac{3}{4}a_3U^3\right]\cos(\omega t) \\
&+ \left[\frac{1}{2}a_2U^2\right]\cos(2\omega t) \\
&+ \left[\frac{1}{4}a_3U^3\right]\cos(3\omega t).
\end{aligned}
\tag{2.36}
$$

As can be seen, the cubic term in (2.35) creates an undesired third harmonic and modifies the gain as

$$\left[a_1 + \frac{3}{4}a_3U^2\right]. \tag{2.37}$$

If $a_1a_3 < 0$, then the gain is compressive, which is typical in most RF systems. Here, the gain expression gives the relation between the input and the output amplitudes. When the gain is converted into decibels, it gives the input and the output power relation. Typically, the input and output power relations are similar to the one shown in Figure 2.9.

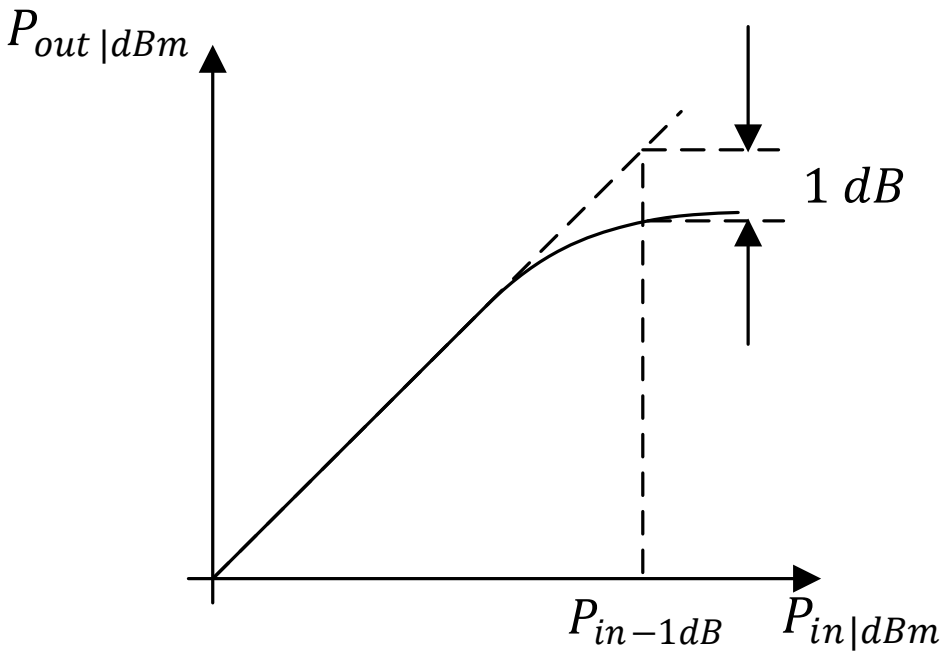


Figure 2.9 A typical input-output power relation

In general, as a performance metric, the point where the power gain is reduced by 1 dB is used and is called the "1-dB compression point". It can be expressed as either input

amplitude (or power) or output amplitude (or power). To calculate the input 1-dB compression point, the compressed gain can be equated to 1 dB less the ideal gain as

$$20\log\left[a_1 + \frac{3}{4}a_3 {U_{in-P1dB}}^2\right] = 20\log a_1 - 1\ dB. \tag{2.38}$$

After making several manipulations, the input amplitude for 1-dB compression point can be obtained as

$$20\log\left[a_1 + \frac{3}{4}a_3 {U_{in-P1dB}}^2\right] - 20\log a_1 = -1\ dB$$

$$20\log\left[\frac{a_1 + \frac{3}{4}a_3 {U_{in-P1dB}}^2}{a_1}\right] = -1\ dB$$

$$1 + \frac{3}{4}\frac{a_3}{a_1}{U_{in-P1dB}}^2 = 10^{(-1/20)}$$

$$U_{in-P1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|}. \tag{2.39}$$

1-dB compression point is important where the amplitude of the signal carries information (e.g. AM modulation). When the device operates in its compression region, some data may be lost as depicted in Figure 2.10.

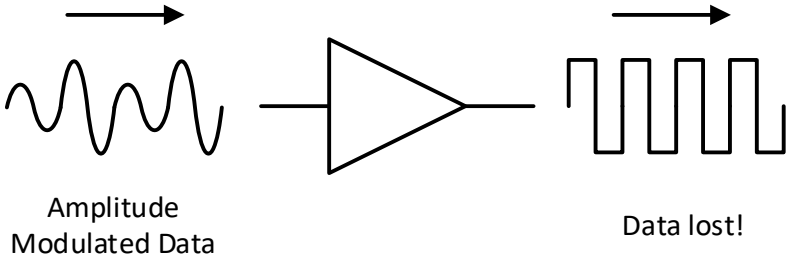


Figure 2.10 The effect of compression on amplitude modulated data [31]

Therefore, the 1-dB compression point is an important metric, and for these amplitude modulation schemes, the device must operate at the input signals below a certain compression point.

2.2.2 Intermodulation

Another problem arising due to non-linearity is intermodulation. This effect can not manifest itself when only a single tone signal is considered. However, when a two-tone

signal is introduced to the system (as typically the case for all communication systems where multiple channels exist) as

$$v_i(t) = U\cos(\omega_1 t) + U\cos(\omega_2 t), \tag{2.40}$$

the output can be calculated by

$$\begin{aligned} v_o(t) &= a_1[U\cos(\omega_1 t) + U\cos(\omega_2 t)] \\ &+ a_2[U\cos(\omega_1 t) + U\cos(\omega_2 t)]^2 \\ &+ a_3[U\cos(\omega_1 t) + U\cos(\omega_2 t)]^3. \end{aligned} \tag{2.41}$$

If the right-hand side of (2.41) is expanded, one can obtain the following "intermodulation products"

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3a_3U^3}{4}\cos(2\omega_1 + \omega_2)t + \frac{3a_3U^3}{4}\cos(2\omega_1 - \omega_2)t \tag{2.42}$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3a_3U^3}{4}\cos(2\omega_2 + \omega_1)t + \frac{3a_3U^3}{4}\cos(2\omega_2 - \omega_1)t \tag{2.43}$$

and the following fundamental components

$$\omega = \omega_{1,2} : \left(a_1U + \frac{9}{4}a_3U^3\right)\cos\omega_{1,2}t \tag{2.44}$$

If these intermodulation products are at the operating frequencies, they virtually behave as noise, and hence, reduce the sensitivity of the system as depicted in Figure 2.11.

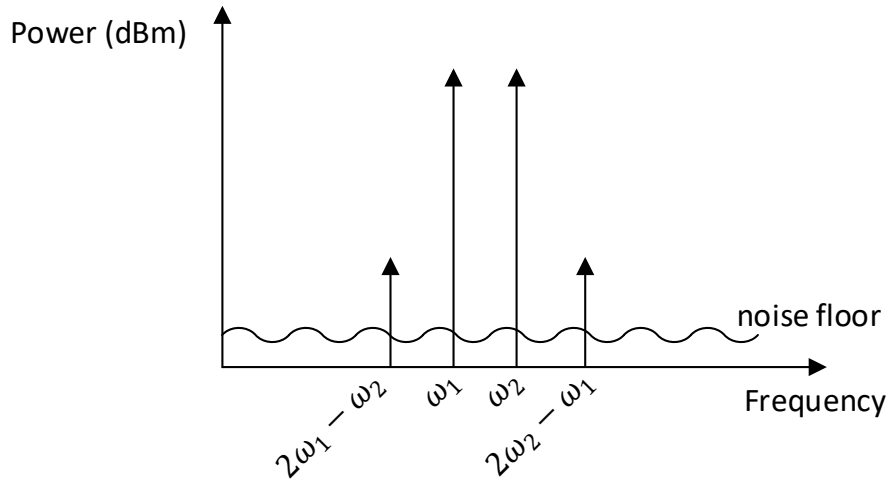


Figure 2.11 The output spectrum referred to the input in a two-tone test

Therefore, as well as gain compression, intermodulation also sets the upper limit of the dynamic range from another point of view.

One of the performance metrics for intermodulation is the "third intercept point". When the input signal is low enough, U^3 term in the fundamental component can be neglected, as depicted in (2.45).

$$\omega = \omega_{1,2}: a_1 U \cos \omega_{1,2} t \tag{2.45}$$

The fundamental terms are proportional to U, whereas the intermodulation terms are proportional to U^3. If the compression is ignored, as the input signal level increases, the fundamental level and the intermodulation level meet at a hypothetical point (see Figure 2.12). This point is called the "third intercept point" (IP_3).

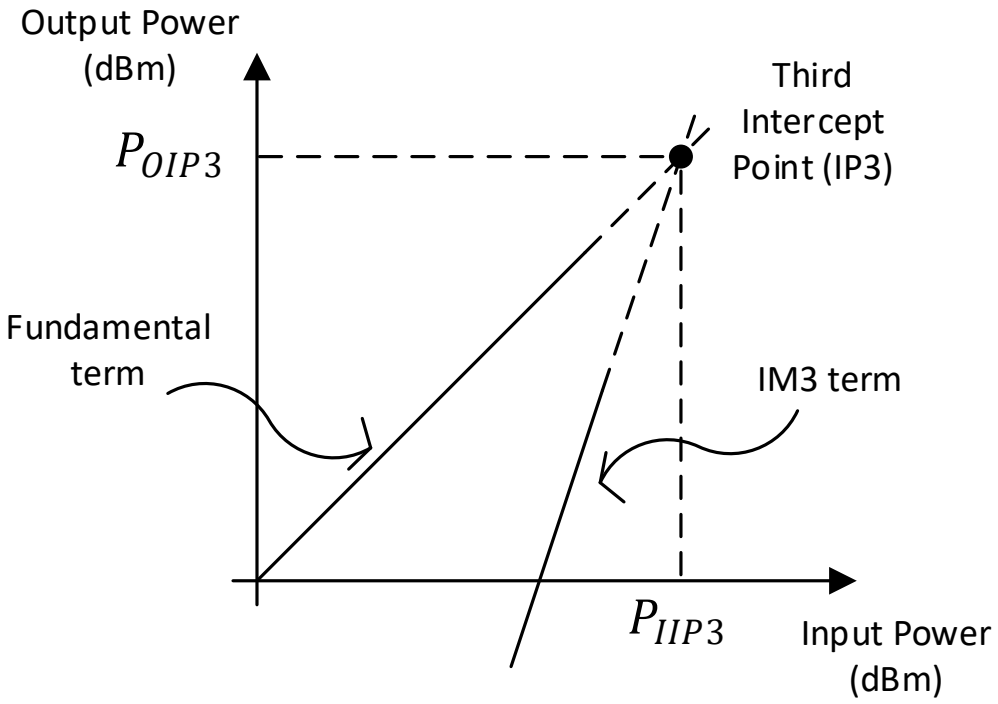


Figure 2.12 The definition of IP_3

As can be seen from Figure 2.12, IP_3 can be represented by the input amplitude (or power) at which this intercept occurs (IIP_3). Also, it can be represented by the output level (OIP_3). To find the expression for the amplitude of IIP_3, the fundamental amplitude can be equated to the intermodulation amplitude:

$$|a_1 U_{IIP3}| = \left|\frac{3}{4} a_3 {U_{IIP3}}^3\right| \tag{2.46}$$

$$U_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.47}$$

A relationship between the input 1-dB compression point and IIP_3 can be derived by

$$\frac{U_{IIP3}}{U_{in-P1dB}} = \frac{\sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}}{\sqrt{0.145\left|\frac{a_1}{a_3}\right|}} = \sqrt{\frac{4}{0.435}} = 9.64\ dB. \tag{2.48}$$

Of course, this relation is not valid if higher than third order terms manifest themselves.

Measuring IP_3 by increasing the input amplitude and plotting a graph similar to Figure 2.12 would be cumbersome. Fortunately, there is another measurement method using the output spectrum. If one divides the fundamental amplitude by the intermodulation amplitude, it is obtained that

$$\frac{U_{fund}}{U_{IM3}} = \frac{|a_1 U|}{\left|\frac{3}{4} a_3 U^3\right|} = \frac{4}{3}\left|\frac{a_1}{a_3}\right| \frac{1}{U^2} = \frac{{U_{IIP3}}^2}{U^2},$$

$$20\log\left(U_{fund}\right) - 20\log(U_{IM3}) = 20\log\left({U_{IIP3}}^2\right) - 20\log(U^2),$$

$$20\log\left(U_{fund}\right) - 20\log(U_{IM3}) = 2 \times \{20\log(U_{IIP3}) - 20\log(U)\},$$

$$20\log(U_{IIP3}) = \frac{1}{2}\left\{20\log\left(U_{fund}\right) - 20\log(U_{IM3})\right\} + 20\log(U). \tag{2.49}$$

If the gain is added to the both sides of (2.49), the output power (dBm) for IP_3 can be obtained as

$$20\log(U_{IIP3}) + G_{dB} = \frac{\Delta P}{2} + 20\log(U) + G_{dB}$$

$$P_{OIP3} = \frac{\Delta P}{2} + P_{out-fund}. \tag{2.50}$$

Therefore, OIP_3 can be calculated simply by using the data in the output spectrum, as shown in Figure 2.13.

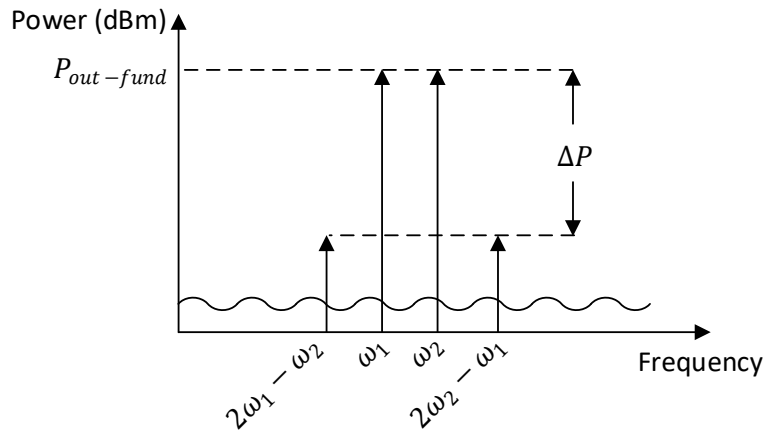


Figure 2.13 The output spectrum for the determination of IP_3

As a final discussion for intermodulation, cascaded amplifier stages, as shown in Figure 2.14, are considered.

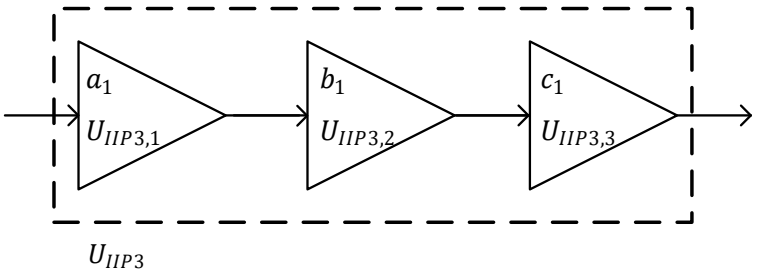


Figure 2.14 A three-stage amplifier

The overall IIP_3 can be approximated by

$$\frac{1}{{U_{IIP3}}^2} \approx \frac{1}{{U_{IIP3,1}}^2} + \frac{{a_1}^2}{{U_{IIP3,2}}^2} + \frac{{a_1}^2{b_1}^2}{{U_{IIP3,3}}^2}, \tag{2.51}$$

whose derivation is given in [31]. According to (2.51), for the overall linearity of an amplifier, the latter stages become increasingly more critical.

2.3 Sensitivity and Dynamic Range

Thus far, two limits for the input signal of an amplifier have been discussed. Noise defines the lower bound as it sets the sensitivity of the system, and linearity defines the upper bound. Another performance metric is dynamic range, which prevents the designer from making mistake of improving one parameter (e.g. noise figure) while accidentally destroying the other.

2.3.1 Sensitivity

Sensitivity for an RF system can be defined as a minimum input signal level (P_{sens}) which yields an acceptable SNR required by the RF system. Typically, the minimum SNR required is in the range of 6 dB to 25 dB [31].

In order to calculate sensitivity, similar to the discussion in the noise section, the equation (2.8) can be rewritten as

$$F = \frac{SNR_{in}}{SNR_{out}},$$
$$F = \frac{P_{sig}/N_s}{SNR_{out}}.$$

Then, it follows that

$$P_{sig} = N_s \cdot F \cdot SNR_{out}. \tag{2.52}$$

Since the power quantities here are in terms of W/Hz, to find the total power, one must multiply the both sides of (2.52) by a certain bandwidth:

$$P_{sig,tot} = N_s \cdot F \cdot SNR_{out} \cdot \Delta f \tag{2.53}$$

If the minimum SNR required is denoted by SNR_{min}, after converting both sides to dB or dBm, one can obtain the sensitivity as

$$10\log\left(\frac{P_{sens}}{1mW}\right) = 10\log\left(\frac{N_s}{1mW} \cdot F \cdot SNR_{min} \cdot \Delta f\right),$$
$$P_{sens|dBm} = 10\log\left(\frac{N_s}{1mW} \cdot F \cdot SNR_{min} \cdot \Delta f\right),$$
$$P_{sens|dBm} = -174\frac{dBm}{Hz} + NF + 10\log(\Delta f) + SNR_{min|dBm}. \tag{2.54}$$

The unit of the first term in the right-hand side might be misleading as it is dBm divided by Hertz. In order to obtain the power in dBm, one must add the dB form of the bandwidth to that quantity. The noise power (-174 dBm/Hz) is calculated using the discussion in the section regarding noise, as in (2.2).

The first three terms in the right-hand side of (2.54). represent the overall output noise of the system referred to the input, which might also be called the “noise floor”.

2.3.2 Dynamic Range

Dynamic range is loosely defined as the maximum input signal the RF system tolerates divided by the minimum meaningful input signal (sensitivity). The maximum input signal is somewhat unclear. It may mean an input signal level at which the gain of the RF system is compressed by 1 dB. The value, 1 dB, may (of course) vary and depends on the system and the application. If one takes the upper limit as the 1-dB compression point, the dynamic range (DR) can be calculated as

$$DR = P_{in-P1dB|dBm} - P_{sens|dBm}. \tag{2.55}$$

On the other hand, when the data are not carried by the amplitude of the input signal, what sets the upper limit of the allowable signal needs to be defined. There is another type of dynamic range called the "spurious-free dynamic range" ($SFDR$). For $SFDR$, when the maximum allowable input signals are applied in a two-tone test, the power of the third-order IM product becomes equal to that of the noise floor. To calculate the upper limit, the equation (2.49) can be rewritten as

$$P_{OIP3} = \frac{\Delta P}{2} + P_{out-fund}.$$

Then, it can be modified as

$$P_{IIP3} + G_{dB} = \frac{P_{out-fund} - P_{out-IM3}}{2} + P_{in} + G_{dB}$$

$$P_{IIP3} = \frac{P_{in} + G_{dB} - P_{in-IM3} - G_{dB}}{2} + P_{in}$$

$$P_{IIP3} = \frac{3P_{in} + P_{in-IM3}}{2},$$

and hence

$$P_{in|dBm} = \frac{2P_{IIP3} + P_{in-IM3}}{3}.$$

If the input referred third order intermodulation product is set to the noise floor, one can find

$$P_{in,max} = \frac{2P_{IIP3} + (-174\ dBm + NF + 10\log(\Delta f))}{3}. \tag{2.56}$$

Therefore, $SFDR$ can be found as

$$SFDR = P_{in,max|dBm} - P_{sens|dBm} = \frac{2(P_{IIP3} + 174\ dBm - NF - 10\log(\Delta f))}{3} - SNR_{min|dBm}. \quad (2.57)$$

2.4 Stability

Another important consideration for an amplifier is its stability. Stability can be defined as "the resistance of the system to oscillations". For example, in the circuit shown in Figure 2.15, a signal (e.g. noise) coming from the passive network may reflect when it encounters the other network containing an active device with a greater power at a certain frequency.

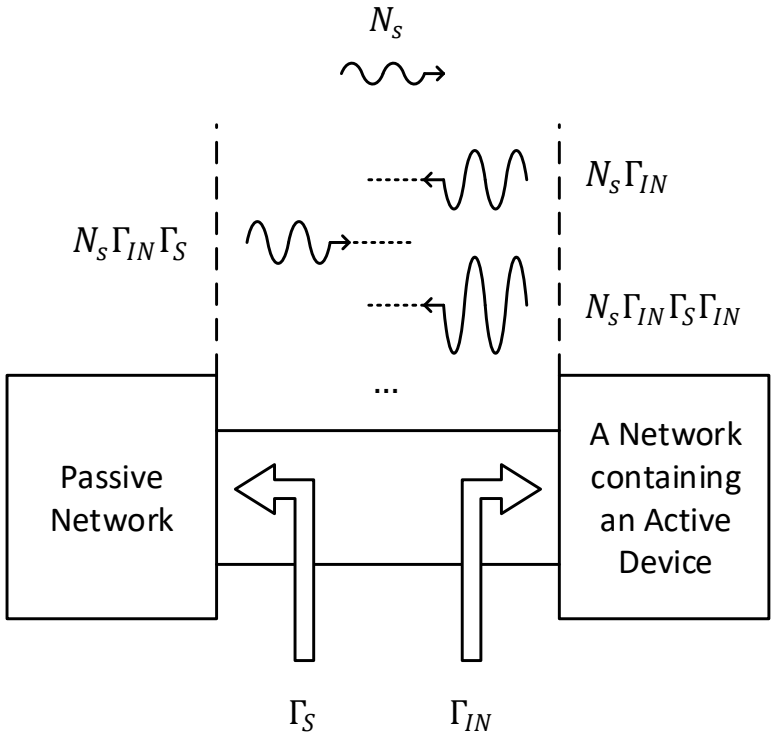


Figure 2.15 A simplified oscillation situation for a circuit

If the reflected signal again reflects from the passive network with a power greater than the initial signal power, the signal goes back and forth, and its power increases indefinitely. Of course, in a real situation, the increase in the power of the signal is limited, and it is probably due to the non-linearity of the active device.

Oscillations disturb the intended usage of some RF designs. Fortunately, there are some ways to determine the stability.

2.4.1 Barkhausen Stability Criterion

The Barkhausen stability criterion is a mathematical condition to determine when a linear feedback circuit *might* create steady-state oscillations.

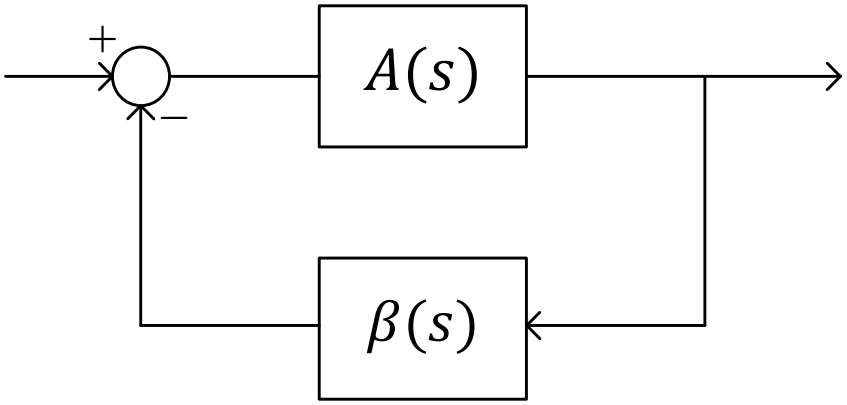


Figure 2.16 A simple feedback circuit

For the feedback circuit shown in Figure 2.16, the closed-loop transfer function can be written as

$$H(s) = \frac{A(s)}{1 + A(s)\beta(s)}. \tag{2.58}$$

When the magnitude of the loop gain, $A(s)\beta(s)$, is less than unity for $\angle A(\omega_{180^\circ})\beta(\omega_{180^\circ}) = 180°$, the magnitude of the closed-loop transfer function is greater than that of the open-loop transfer function, $A(s)$, but the system is stable. On the other hand, when $|A(\omega_{180^\circ})\beta(\omega_{180^\circ})| = 1$, the magnitude of the closed loop transfer function becomes infinity, meaning that there is a steady-state oscillation when there is no input. Moreover, it should be remembered from circuit and feedback courses that when a transfer function has conjugate right half-plane (RHP) poles, the output has a growing oscillation component.

For the steady-state oscillation to occur, the Barkhausen criterion states that

$$|A(\omega_{180^\circ})\beta(\omega_{180^\circ})| = 1, \tag{2.59}$$

where ω_{180° is the angular frequency at which the phase of the loop gain is equal to 180°.

However, it should be indicated that the Barkhausen criterion is *necessary*, but *not sufficient* for the steady-state oscillation [43].

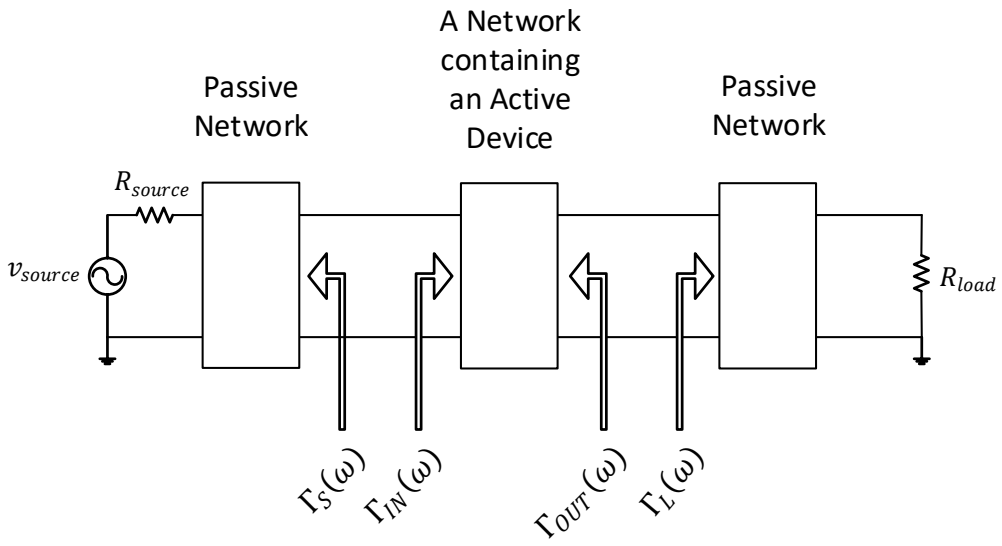


Figure 2.17 A simple RF amplifier block diagram

After this discussion, why this criterion is important in RF amplifier design should be explained. To understand this, a simple RF amplifier block diagram (see Figure 2.17) and its corresponding signal flow graph for the input side (see Figure 2.18) can be considered.

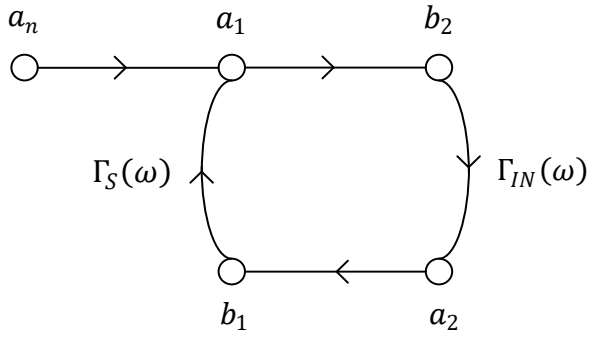


Figure 2.18 Signal flow graph for the input side of the circuit in Figure 2.17

From the flow graph in Figure 2.18, the following relation (2.60) can be obtained.

$$\frac{a_2}{a_n} = \frac{\Gamma_{IN}(\omega)}{1 - \Gamma_S(\omega)\Gamma_{IN}(\omega)} \tag{2.60}$$

With a loop gain of $-\Gamma_S(\omega)\Gamma_{IN}(\omega)$, the equation (2.60) indeed resembles (2.58), and its stability analysis must be performed.

From (2.60), it can be inferred that to ensure the stability, all loop gain values must be less than unity when their phase are $180°$, which is indeed the commonly used method among RF engineers to ensure stability. Moreover, the transfer functions like (2.60) must not have RHP poles.

2.4.2 Stability Circles

Using the S-parameter techniques, the magnitudes of Γ_{IN} and Γ_{OUT} for the circuit in Figure 2.17 can be calculated as

$$|\Gamma_{IN}| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right|, \tag{2.61}$$

$$|\Gamma_{OUT}| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right|. \tag{2.62}$$

As expected, the magnitudes of Γ_{IN} and Γ_{OUT} depend on the networks connected to the input and output. If these networks are passive ($R_S > 1$ and $R_L > 1$), then it can be said that $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$. For this condition, it is sufficient that $|\Gamma_{IN}| < 1$ and $|\Gamma_{OUT}| < 1$ for the loop gains to be less than unity.

A stability circle is a circle drawn on a Γ_L (or Γ_S) plane for which $|\Gamma_{IN}| = 1$ (or $|\Gamma_{OUT}| = 1$). When designing an amplifier, it must be ensured that Γ_L and Γ_S lie within the stable side, i.e. either inside or outside of the stability circles. The stable side can simply be determined by setting Γ_L (or Γ_S) to zero and checking if $|\Gamma_{IN}| < 1$ (or $|\Gamma_{OUT}| < 1$).

After this discussion, two definitions can be made:

An *unconditionally stable* amplifier has $|\Gamma_{IN}| < 1$ and $|\Gamma_{OUT}| < 1$ for every passive source and load impedances ($|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).

A *potentially unstable* amplifier has $|\Gamma_{IN}| > 1$ and $|\Gamma_{OUT}| > 1$ for some passive source and load impedances ($|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).

For the sake of completeness, the equations for these stability circles can be derived by setting $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$. For the output stability circle, the equations are

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \text{ (center)}, \tag{2.63}$$

$$R_L = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \text{ (radius)}, \tag{2.64}$$

and similarly, for the input stability circle, the equations are

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \text{ (center)}, \tag{2.65}$$

$$R_S = \left|\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2}\right| \text{ (radius)}, \tag{2.66}$$

where Δ is the determinant of the scattering matrix which is equal to $S_{11}S_{22} - S_{12}S_{21}$.

2.4.3 Tests for Unconditional Stability

Instead of the stability circles, there are simpler methods to test unconditional stability. It is known that a linear two-port circuit is unconditionally stable if the Rollet's condition

$$K \triangleq \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1, \tag{2.67}$$

along with *any one* of the auxiliary conditions below are satisfied.

$$B_1 \triangleq 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \tag{2.68}$$

$$B_2 \triangleq 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta|^2 > 0 \tag{2.69}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.70}$$

$$1 - |S_{11}|^2 > |S_{12}S_{21}| \tag{2.71}$$

$$1 - |S_{22}|^2 > |S_{12}S_{21}| \tag{2.72}$$

This condition is *necessary* and *sufficient* for unconditional stability.

There is another commonly used test for unconditional stability, which is the μ-factor [44]. The condition below is again necessary and sufficient for unconditional stability.

$$\mu \triangleq \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{21}S_{12}|} > 1 \tag{2.73}$$

The μ-factor has several advantages over the Rollet's condition. One advantage is that a single parameter is sufficient to test unconditional stability unlike the Rollet's condition, which require an extra auxiliary condition. Another advantage is that it is possible to say "the greater the value of μ is, the more stable the circuit is." [45]. The reason is that μ gives the distance between the center of the Smith chart and the closest unstable point of the load stability circle (see Figure 2.19). No such inference can be made from the Rollet's factor.

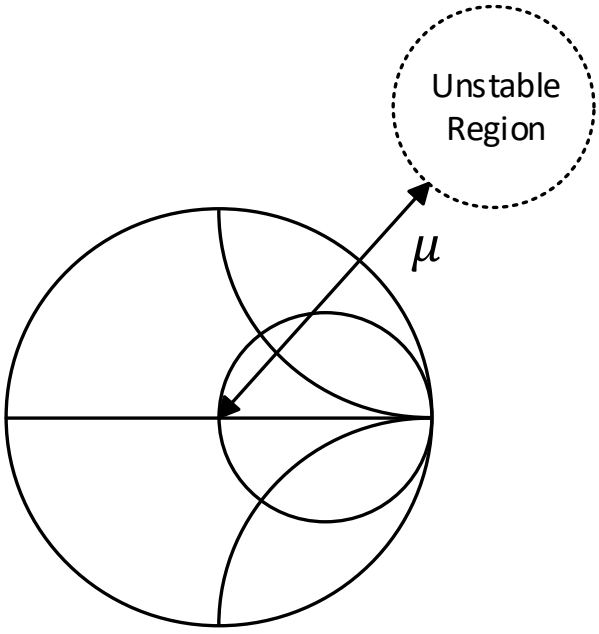


Figure 2.19 The load plane and the corresponding stability circle [45]

There is also a companion factor, μ', which gives the distance between the center of the Smith chart and the closest unstable point of the source stability circle. This μ'-factor can also be used to test unconditional stability.

$$\mu' \triangleq \frac{1-|S_{22}|^2}{|S_{11}-S_{22}^*\Delta|+|S_{21}S_{12}|} > 1 \tag{2.74}$$

As a final remark, it must be pointed out that these tests can be used for a network containing *only one* active element as they do not ensure that there is no oscillation between active elements. Therefore, for a multistage amplifier, each stage requires its own stability test. However, one might claim that since these tests indicate unconditional stability only when they are connected to passive networks and one stage can introduce negative resistance to the other, the overall circuit may not be

unconditionally stable even when each stage passes the stability test. This is not true. The reason is that when each stage passes stability test, there is no possibility that any stage seeing a positive resistance from one side can introduce a negative resistance to other side as illustrated in Figure 2.20.

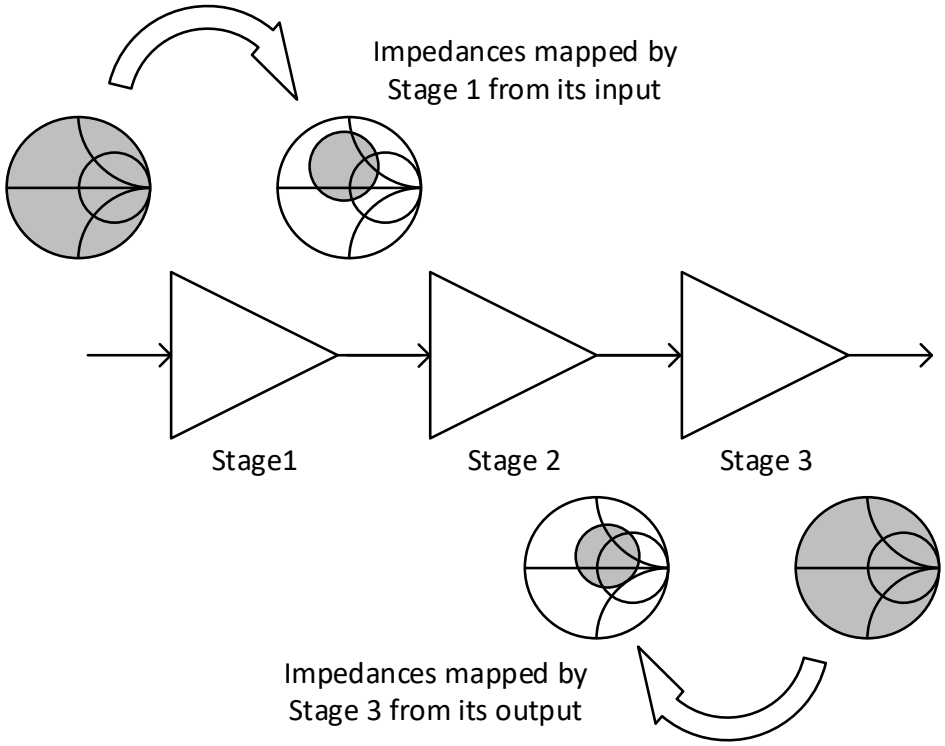


Figure 2.20 An amplifier with unconditionally stable three stages and the impedance mappings by Stage 1 and Stage 3

2.4.4 Nyquist Stability Criterion

For a multistage amplifier, there are several drawbacks for the stability tests in the previous section. One of them is that any possible (electromagnetical) couplings between amplifier stages are not taken into account. Another drawback is that one stage maps all the different passive loads it may see to the other port as a smaller portion in the Smith chart as can be seen from Figure 2.20. For example, although Stage 2 in Figure 2.20 is designed as it can see all the passive impedances from one port, it only sees a small portion of the Smith chart. Therefore, the stages of the amplifier might be over stabilized, possibly causing some performance loss. Finally,

these stability tests can not be used for some topologies. For example, for a cascode amplifier as in Figure 2.21, unconditional stability of the first (common-source) stage can probably not be ensured and even if the second (common-gate) stage is unconditionally stable, the first stage may introduce a negative resistance to the second stage. Therefore, these previously mentioned stability analyses are not applied to a cascode amplifier.

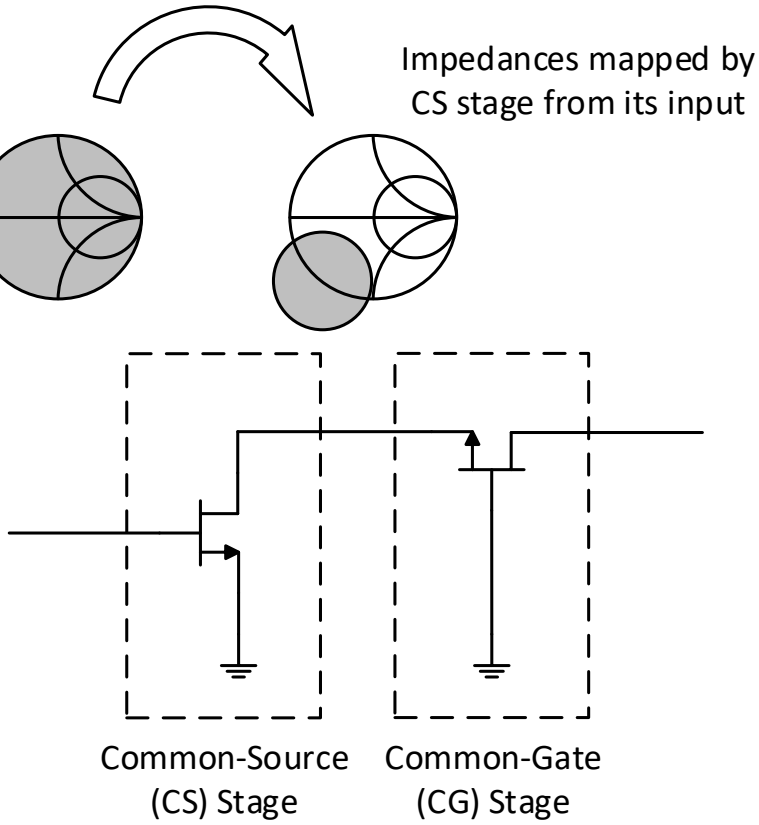


Figure 2.21 A cascode amplifier with matching, biasing and stabilizing element neglected

Fortunately, for such cases, Nyquist stability criterion can be employed. According to Nyquist test, loop gains (e.q. $-\Gamma_S(\omega)\Gamma_{IN}(\omega)$) can be analyzed to determine if the transfer functions have RHP poles.

The Nyquist analysis is performed by plotting the outputs of the loop gain as ω goes from zero to infinity on a complex plane. If the number of the clockwise encirclement of the point, -1, is N, then

$$Z = N + P, \tag{2.75}$$

where Z is the number of zeros, P is the number of poles for the denominator of the transfer function. Therefore, if the number of the clockwise encirclement of the point, -1, is non-zero, then the overall transfer function has RHP poles. One interesting case would be when $Z = P$ in which case the instability would not be detected.

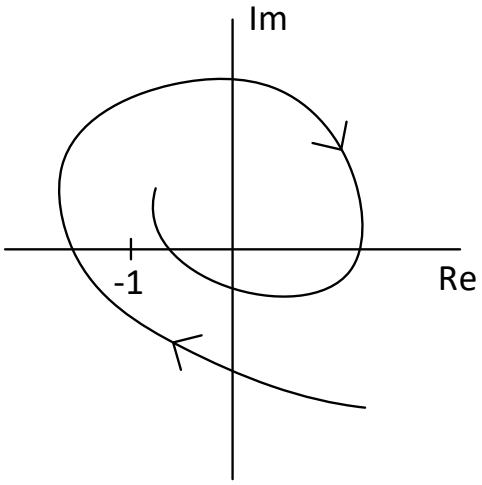


Figure 2.22 A Nyquist plot showing clockwise encirclement of the -1 point

To ensure stability, for each terminal of the active devices, this test must be employed. Also, these tests should be performed for each combination of passive source and load impedances as each analysis is valid for a single pair of source and load impedances.

2.5 Impedance Matching and Gain

Impedance matching is yet another important issue in RF design. It enables not only the maximum power transfer but also the maximum gain possible. In this section, impedance matching and gain are discussed together as they are interrelated.

2.5.1 Simultaneously Conjugate Matching for Two-Ports

From undergraduate microwave courses, one might remember how to perform conjugate matching for one-ports. For example, if the matching circuits are designed for the circuit in Figure 2.23 so that the one-port sees the conjugate of its input impedance at its port, the one-port is conjugately matched.

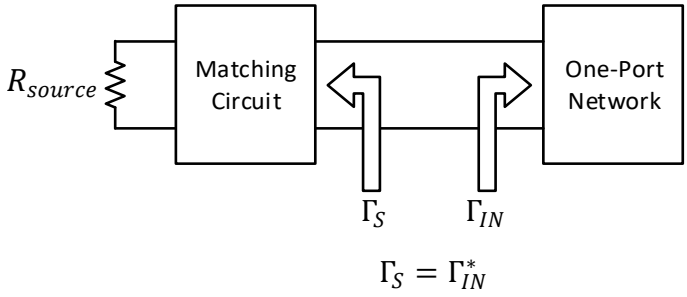


Figure 2.23 A conjugately matched one-port

For two-ports, on the other hand, the problem of impedance matching becomes more complicated. In Figure 2.24, a two-port circuit together with its matching networks are drawn. To calculate Γ_{IN} and Γ_{OUT}, the more general forms of (2.61) and (2.62) can be rewritten as

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \tag{2.76}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{2.77}$$

Initially, if it is assumed that there is no matching network, the values of Γ_{IN} and Γ_{OUT} are that of S_{11} and S_{22}, respectively. If the matching circuit is made for the output, Γ_L becomes S_{22}^*, so the value of the Γ_{IN} is modified as it depends on Γ_L. If Γ_S is set to Γ_{IN}^*, then the value of Γ_{OUT} is changed and the output is not matched anymore. Therefore, the two-port can probably not be matched by doing this.

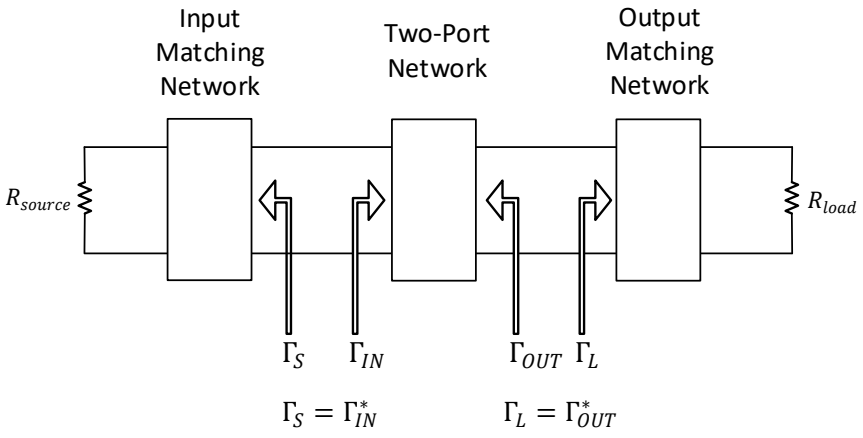


Figure 2.24 A conjugately matched two-port

Another approach must be developed to match a two-port. The conditions required for simultaneously conjugate matching are

$$\Gamma_S = \Gamma_{IN}^* \tag{2.78}$$

and

$$\Gamma_L = \Gamma_{OUT}^*. \tag{2.79}$$

From (2.76), (2.77), (2.78), and (2.79), it can be written that

$$\Gamma_S^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.80}$$

and

$$\Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{2.81}$$

Simultaneously solving (2.80) and (2.81) gives Γ_S and Γ_L values required for simultaneous conjugate match [46]. Calling these values Γ_{MS} and Γ_{ML}, one can obtain

$$\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}, \tag{2.82}$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}, \tag{2.83}$$

$$B_1 \triangleq 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2, \tag{2.84}$$

$$B_2 \triangleq 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta|^2, \tag{2.85}$$

$$C_1 \triangleq S_{11} - \Delta S_{22}^*, \tag{2.86}$$

$$C_2 \triangleq S_{22} - \Delta S_{11}^*. \tag{2.87}$$

For an unconditionally stable two-port, the solutions with minus signs are the useful ones.

2.5.2 Maximum Transducer Power Gain

There are several gain equations found in the literature. One of them is the transducer power gain, G_T. It is defined as

$$G_T \triangleq \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source}. \tag{2.88}$$

Under simultaneous matching condition, the maximum transducer power gain can be obtained as

$$G_{T,max} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right), \tag{2.89}$$

where K is the Rollet's stability factor.

Therefore, if an unconditionally stable ($K > 1$) two-port is conjugately matched, a power gain of $G_{T,max}$ is obtained. Of course, the matching circuits must not include any resistors for this condition to hold.

Finally, for potentially unstable two-ports, there is a figure of merit called the maximum stable gain, and it is defined as the value of $G_{T,max}$ when $K = 1$, as depicted in (2.90).

$$G_{MSG} = \frac{|S_{21}|}{|S_{12}|} \tag{2.90}$$

2.6 Conclusion

In this chapter, basic concepts for LNA design are given. The concepts and the methods presented are employed for the design and evaluation of the LNA in Chapter 3 and Chapter 4. In Section 2.1 regarding noise, it is concluded that the input side of the receiver has a great impact on the overall system noise performance (Friis' formula for noise). At the input side of the LNA, no resistor is used so that the noise performance of the LNA can not significantly be damaged by the noise of the resistor. Also, the first stage is designed for its possibly maximum gain over the band of interest (X-band). The concepts in Section 2.2 regarding linearity are used for the transistor size selection. When determining OIP_3 performance, similar to the discussion in the

linearity section, the output spectrum is used with only single power level of input signals, speeding up the measurements. For the stability, the gains of the stages reduced by using resistors, degeneration inductances and series feedback as can be concluded from Section 2.4. Also, each stage is initially conjugately matched so that any internal reflections can not occur. Moreover, considering the possible couplings between the stages, Nyquist criterion is used for the stability. Using the discussions in Section 2.5, the cores of the stages are designed by the help of the maximum transducer gain. Since each stage has a common-source topology, they have poor isolation between their input and output ports, making matching circuits more difficult to construct. To overcome this, the discussions for conjugate matching are used.

CHAPTER 3

DESIGN AND SIMULATION

Two LNA designs are presented in this thesis. Both are composed of three common-source stages. The designs are simulated and optimized using AWR MWO. The operating band is the X-band (8-12 GHz). The gain is targeted to be higher than 20 dB and the return losses are targeted to be higher than 10 dB. For convenience, the goals for the LNA design for this work is re-given in Table 3.1.

Table 3.1 The goals for the LNA design

Operating Frequency (GHz)	8-12 (X-band)
Noise Figure (dB)	<2
Gain (dB)	>20
Return Losses (dB)	>10
Output P1dB (dBm)	>15
Input Power Survivability (W)	>2

The circuits are realized using the 0.25 μm Power GaN/SiC HEMT process by WIN Semiconductor. Since the circuits described here are designed for possible integration of a complete TX/RX chain for military applications, access to the factories in the United States is highly restricted due to U.S. International Traffic in Arms Regulations (ITAR) restrictions. The WIN Semiconductor fab is located in Taiwan and is not subject to United States' International Traffic in Arms Regulations restrictions. However, the process is still under development and the transistor models in the process design kit (PDK) are incomplete. Due to this, two LNA designs go through two revision cycles to hit target performance values. The first LNA is designed using the PDK 1.1.2. After the layout for the LNA is sent to the manufacturer, a newer

PDK (1.2.1) version is received. Then, the samples from the first tapeout are received. The samples are measured, and the measurement results are compared with the simulated results using the PDK 1.1.2. It is seen that the measured results are not consistent with the simulated ones. However, when the measured results are compared with the simulation results using the new PDK (1.2.1), there is a good agreement between the result, indicating that the old PDK version is not valid anymore. The discrepancy is due to the transistor models only since the simulation results of a circuit composed only of passive elements are consistent with the corresponding simulation results. In order to hit the targets, another LNA is designed using the PDK 1.2.1, and the design is sent for production. In the meeting with WIN Semiconductor's representative, it is explained that they replace one of the reactors which is used in the manufacturing. Therefore, the transistor models from the PDK 1.2.1 are considered to be invalid for the future tapeouts. To solve this, new transistor models are created using back-fitting method, which will be explained in Section 4.6. The problems encountered during the work are summarized in Figure 3.1.

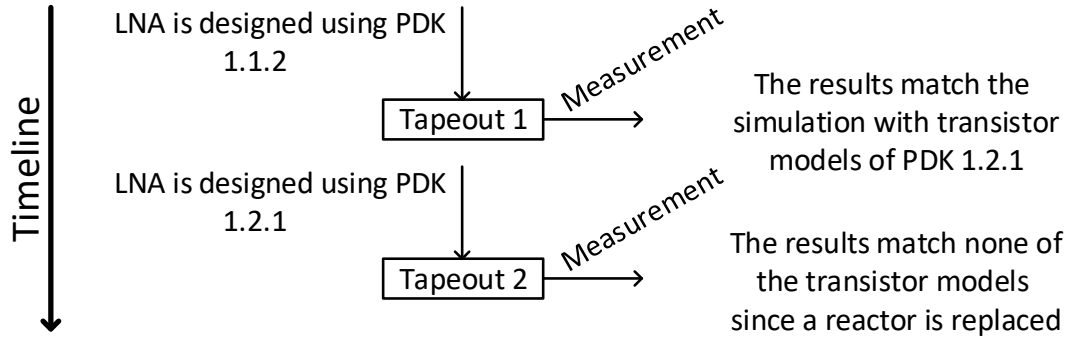


Figure 3.1 The summary of the problems encountered during the work

This chapter briefly explains how these LNAs are designed and gives their simulation results. Since there are no non-linear models of transistors in the PDKs supplied by the fab, linearity simulations, such as P_{1dB} and IP_3, are not available. However, the transistor sizes and quiescent points were determined by referring to the designs done on similar processes and with the goal of achieving more than 15 dBm of output P_{1dB} [47].

3.1 Design Procedure and Environment

The design flow for the RF integrated circuit (IC) design is as follows. Firstly, a circuit composed mostly of ideal elements is constructed. If the simulation results meet the expectations, this step is done. Then, the ideal elements are replaced by the corresponding models in the PDK and the layout is created. After that, the circuit is simulated again, and the results are compared with the specifications. Since the passive components in the PDK may couple to each other in a real situation, an electromagnetic (EM) structure is created combining the passive models in the circuit and this structure is electromagnetically simulated. Again, the results must meet the specifications. After that, it should be checked that the layout really represents the components in the schematic (Layout Versus Schematic -LVS- check) and that the layout can be manufactured obeying the manufacturing rules (Design Rule Check -DRC-). Also, the components should be checked for their current handling capability. Next, the layout is sent for production, which is called "tapeout". After the manufactured samples are received, they must be evaluated by measurements, and it must be decided whether the measured results meet the expectations or not. If the measured results meet the specifications, the design is complete. If not, the design error must be detected, and to fix that, some of the previous steps are re-applied. This design flow of a radio-frequency integrated circuit (RFIC) is summarized in Figure 3.2.

In this thesis, the circuits are designed and simulated using AWR Microwave Office (MWO) software. Electromagnetic simulations are performed using AXIEM, which is the 2D planar electromagnetic (EM) analysis software supplied within AWR MWO [48]. Figure 3.3 shows the 3D view of a layout of one of the LNAs, which is divided into meshes and distinctively colored for the DC paths.

It should be noted that all the simulation results in this thesis are coming from the EM simulations of the layouts of the designs.

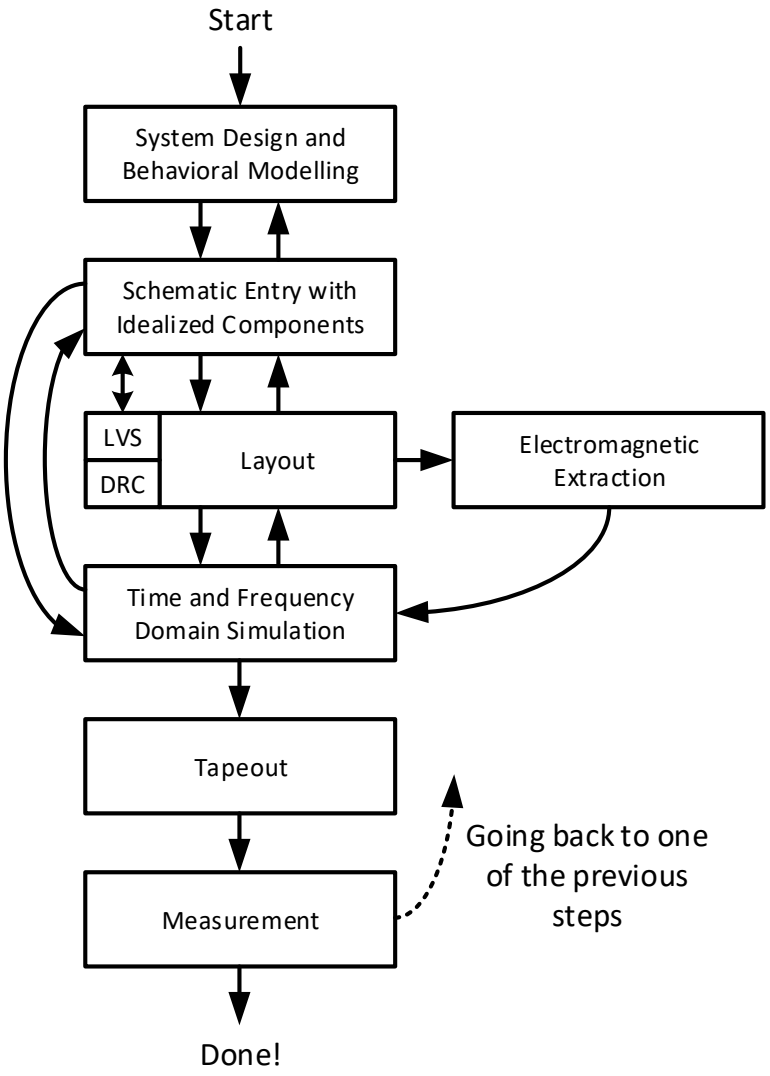


Figure 3.2 Summary of the RFIC design flow

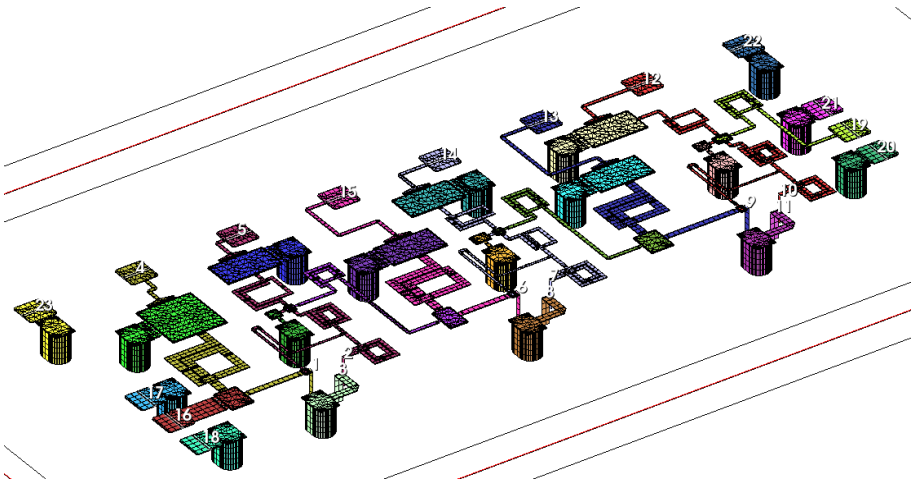


Figure 3.3 The 3D view of the EM structure for the first LNA (tapeout 1)

3.2 Topology

A broad-band circuit may easily be designed with a cascode stage due to the suppression of the Miller effect. However, it has higher noise figure than a common-source stage (for the same size and bias of transistors) [11][13]. Moreover, a cascode topology should be implemented separating its stages in this process, as only the linear models of transistor are available in the PDKs, and this separated cascode topology occupies more area and consumes more power than a common-source stage as explained in Section 1.1. By investigating the LNAs in the literature and considering the properties of different topologies (CS, cascode etc.), the circuit is designed as three cascaded common-source stages in order to meet the project specifications and to make the circuit have a small size.

3.3 Core Circuit

This section discusses the design of the core circuits. The term “core circuit” is used to refer to a circuit including elements (e.g. transistor, resistor, and degeneration inductor), indicating the topology of the circuit. However, this circuit excludes the matching circuit elements and possibly the bias circuit elements.

Since the available models of transistor are only S-parameters (2-26 GHz), the bias points of the transistors are not determined by tuning gate voltages. Instead, these S-parameters with pre-defined biases are put into the circuit, and then the periphery is designed. For the sake of completeness, how bias point selection can be performed is also discussed.

The bias point selection may need to be performed both on single-transistor topologies, and on multiple-transistor topologies (e.g. cascode). The philosophy is that when adding ideal sources to bias the transistors, these sources must not affect the small-signal operation as they are shorted in small-signal circuits. Also, any DC currents should not flow into the ports. To achieve this, a bias-tee similar to the one in Figure 3.4 can be used.

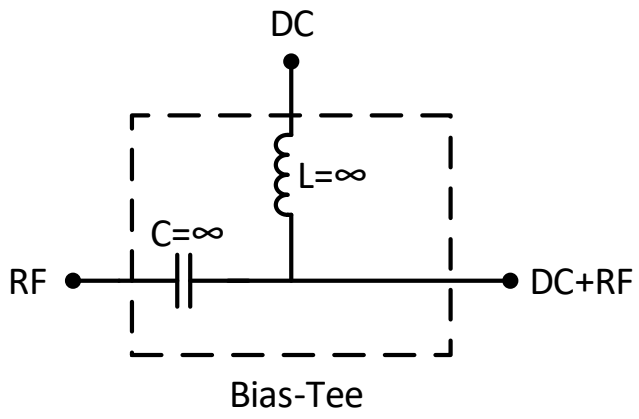


Figure 3.4 An ideal bias-tee structure

After biasing is complete, some parameters (e.g. noise figure and maximum stable gain) can be checked to determine if the transistors and the bias points are useful for the design goal.

A sample bias point determination circuit for a single-transistor topology (common-source for this case) is shown in Figure 3.5.

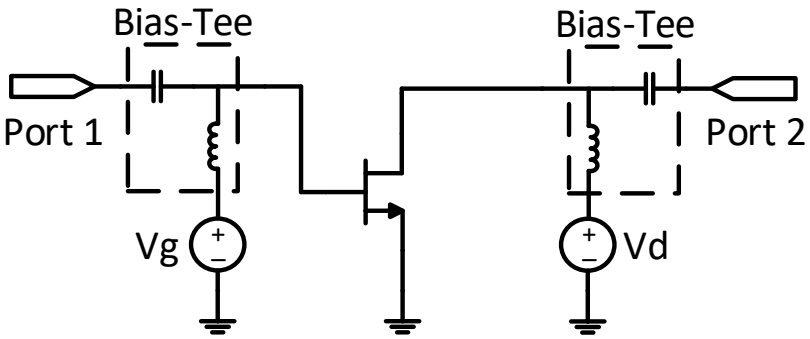


Figure 3.5 A bias point determination circuit for a common-source stage

As mentioned before, the designed LNAs are composed of three single transistor common-source stages. Each stage has a 4×50 μm transistor, and their drain currents are 20 mA. To increase linearity, the transistor sizes can be increased for the latter stages with the same current density. Since the manufacturing process is under development and the transistor models are not complete, the same size and the same bias current are used for each stage to facilitate the back-fitting of the transistor models which is discussed in the next sections.

A simplified schematic of one of the core circuits is shown in Figure 3.6.

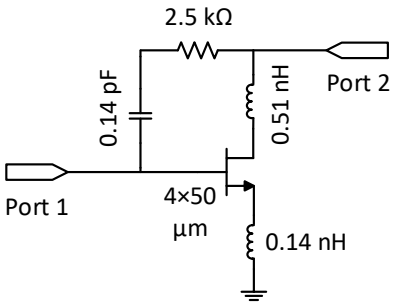


Figure 3.6 The core circuit for the first stage (for the LNA from the first tapeout)

In Figure 3.6, the degeneration inductor (below the transistor) is added in order to facilitate both noise and conjugate matchings simultaneously. The shunt-feedback resistor is added to increase bandwidth. The capacitor is put to isolate DC voltages and currents. The degeneration inductor and the resistor also increase the stability of the circuit.

The minimum noise figure (NF_{min}) simulation for this circuit is presented in Figure 3.7.

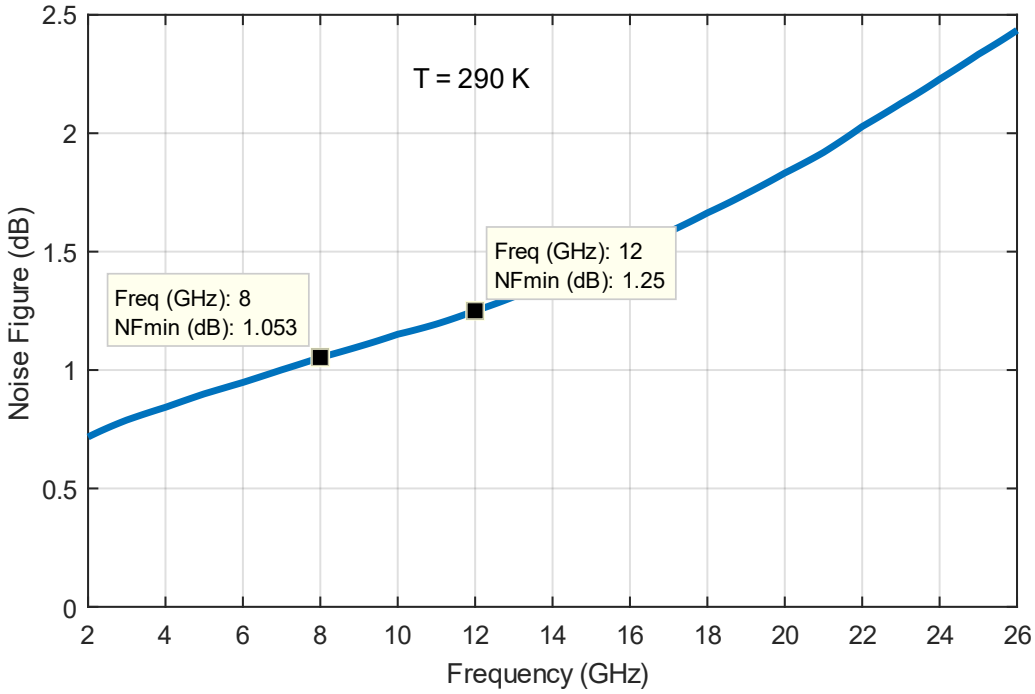


Figure 3.7 The NFmin simulation of the core circuit

As can deducted from Figure 3.7, the circuit can have a minimum noise figure of less than around 1.25 dB at operating frequencies when the input of the circuit sees the impedance for the minimum noise figure.

Simulation results for the maximum transducer gain ($G_{T,max}$) and the maximum stable gain (G_{MSG}) are shown in Figure 3.8.

The circuit has a gain of more than around 9 dB over the frequency band of interest when the circuit is conjugately matched.

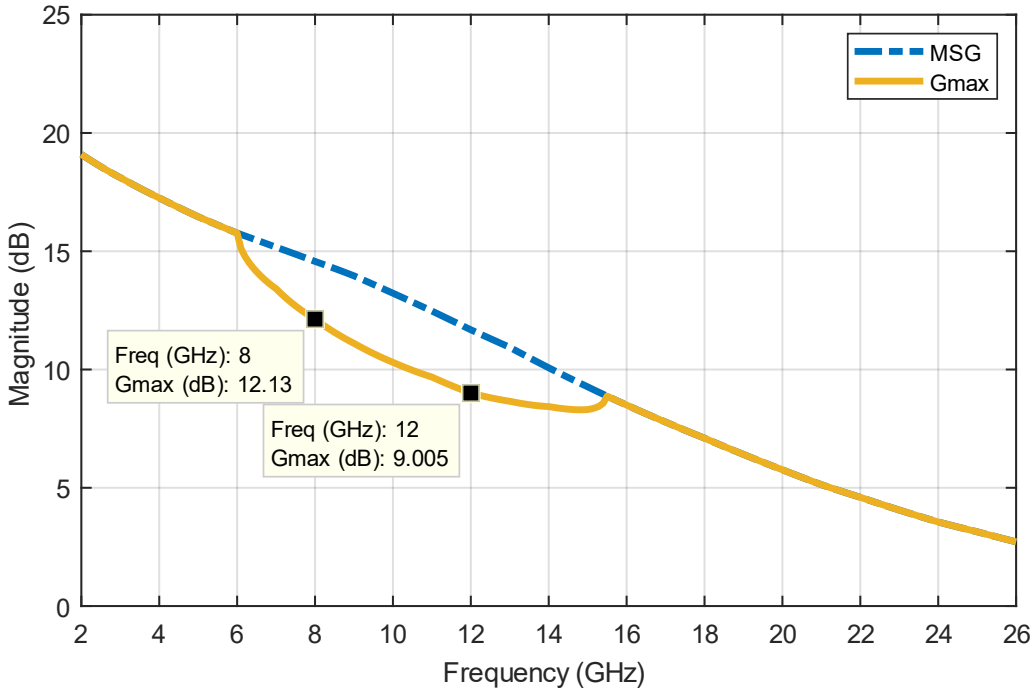


Figure 3.8 The Gmax and MSG simulation of the core circuit

It should be added that in the first design, the core circuits of the stages are identical to each other. This results in a sloped gain over the band of interest. To solve this, in the second design, each core circuit is modified. In the core circuits of the latter stages, $G_{T,max}$ is higher at the high-end of the X-band (10-12 GHz) so as to compensate the lower gain of the first stage at those frequencies.

3.4 Impedance Matching Circuit

Impedance matching circuits are an important part of an overall RF design. When designing a multistage amplifier, one can start to design matching circuits from either the output or the input, and successively continue to the other side using gain circles and possibly load-pull contours which are discussed in [17][19]. Another method would be to design conjugately matched stages separately, and then to connect them in series. The latter method may have the disadvantage of the use of more elements than the former one. The use of more elements means more chip area and more performance loss due to the lossy elements. Another problem would be the increased coupling among elements possibly causing the circuit to oscillate. To solve this problem, after the stages are connected, one may eliminate some of the elements by combining them or tuning the values of the other elements. In this work, the second method is used. Also, in the design, biasing networks as in Figure 3.4 are not used, but the biasing is included in the matching circuits, instead. In this section, first of all, the schematic of the input matching network and its simulation results are given. After that, those for the output matching network are given. Finally, the schematic of the overall stage and the corresponding simulation results are given.

The schematic of the input matching circuit for the first stage is shown in Figure 3.9.

The element values are chosen so that the Γ_S is in the vicinity of Γ_{MS} and Γ_{opt} on the Smith chart moving Γ_S from 50 Ω to the corresponding place over the operation band.

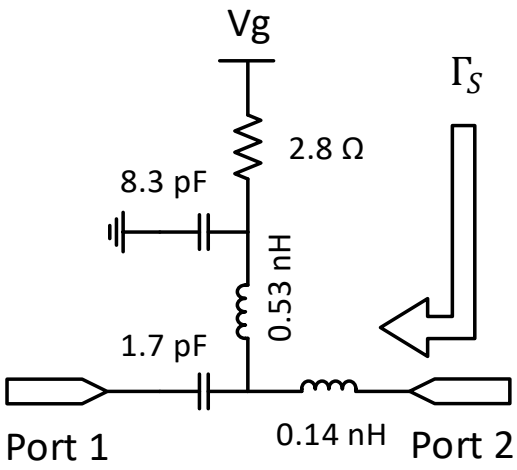


Figure 3.9 The schematic of the input matching circuit for the first stage

The simulation results of GammaMS (Γ_{MS}) and GammaOpt (Γ_{opt}) together with GammaS (Γ_S), which is seen by the input, are shown in Figure 3.10.

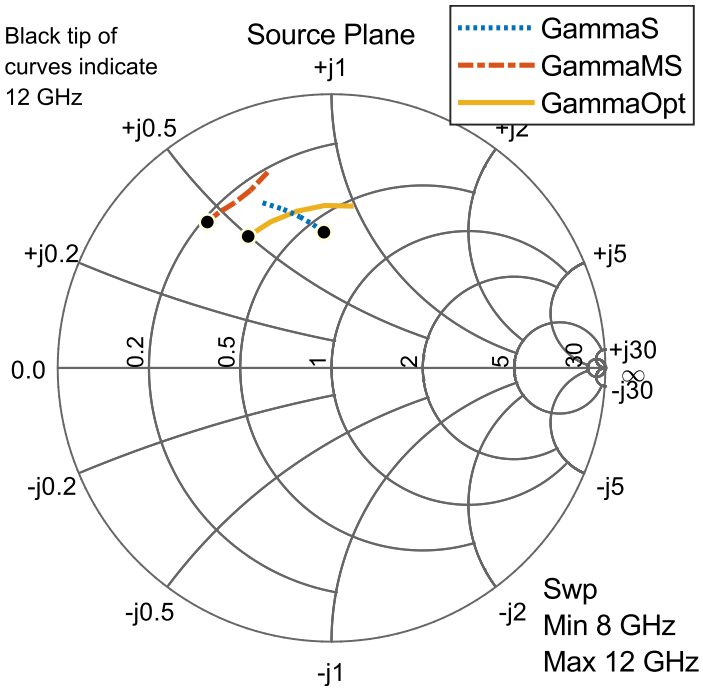


Figure 3.10 The simulation results of GammaMS, GammaOpt and GammaS

The output matching schematic is demonstrated in Figure 3.11.

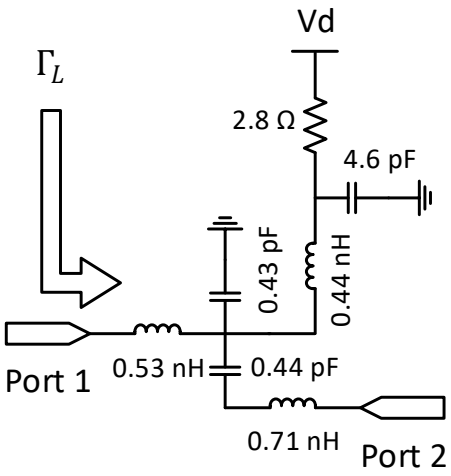


Figure 3.11 The schematic of the output matching circuit for the first stage

Similarly, the element values are chosen so that the Γ_L is in the vicinity of Γ_{ML} on the Smith chart moving Γ_L from 50 Ω to the corresponding place over the operation band.

The simulation results of GammaML (Γ_{ML}) together with GammaL (Γ_L), which is seen by the output, are shown in Figure 3.12.

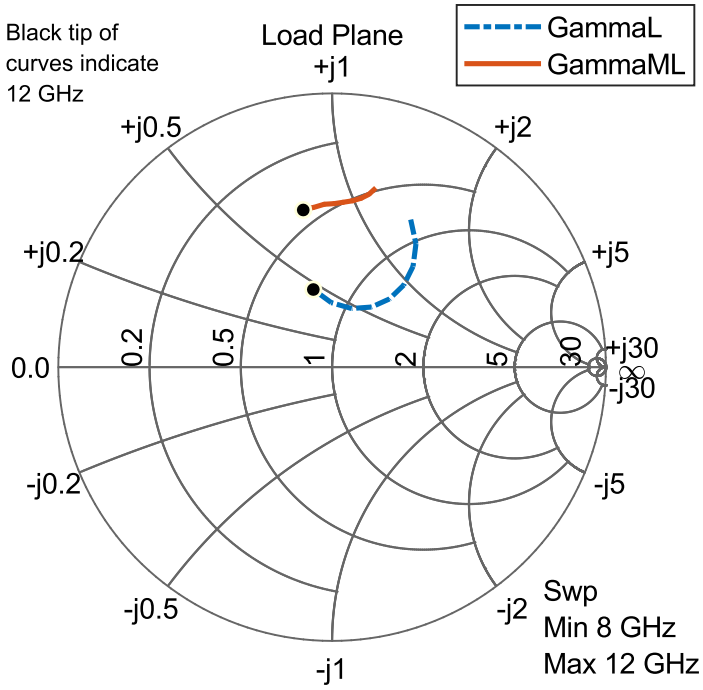


Figure 3.12 The simulation results of GammaML and GammaL

After the matching circuits are constructed, they are connected to the core circuit. The schematic is given in Figure 3.13.

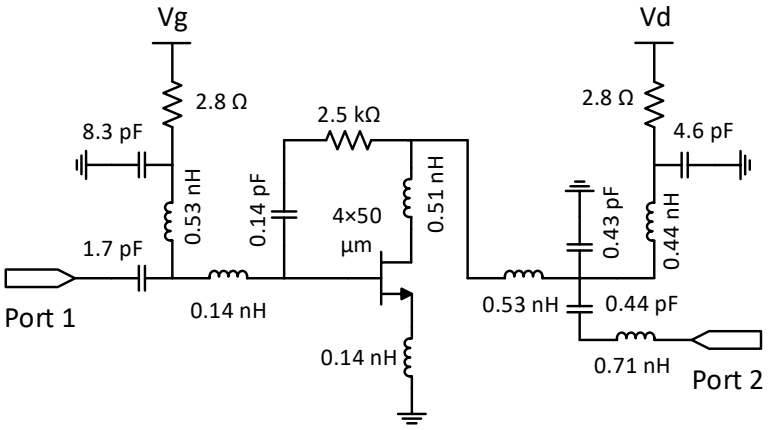


Figure 3.13 The schematic of the whole stage

The simulation results of the S-parameters for the overall first stage are given in Figure 3.14.

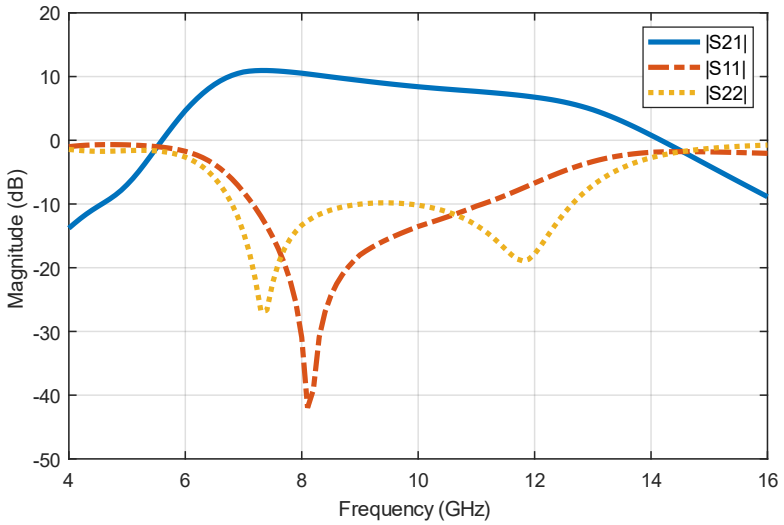


Figure 3.14 The simulation results of the S-parameters

From Figure 3.14, considering the lossy nature of the real elements, it can be concluded that the circuit is conjugately matched as the gain (S_{21}) is similar to the maximum transducer gain as shown in Figure 3.8.

The simulation results of the noise figure are shown in Figure 3.15. The noise figure is below about 1.75 dB over the operating frequencies. According to the Friis's formula for noise, which is given in Section 2.1.5, when three stages identical to this designed one are cascaded, the overall noise figure will not exceed 2 dB over the X-band, achieving the design goal.

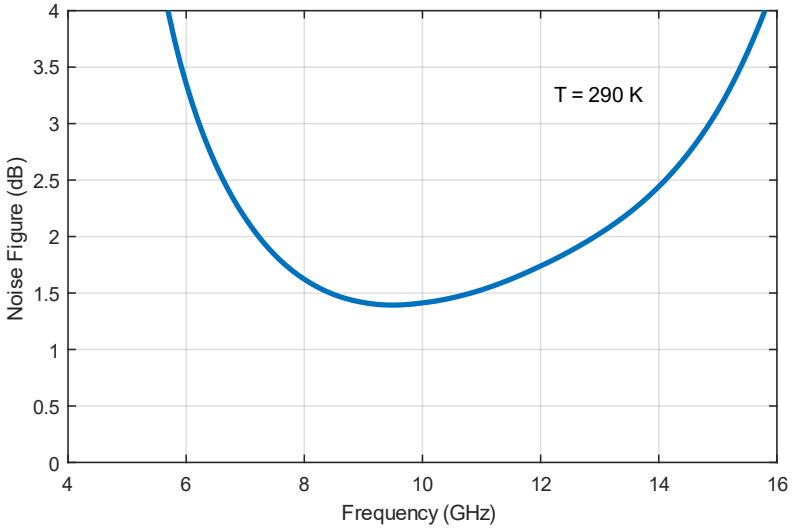


Figure 3.15 The simulation results of the noise figure

Finally, the stability simulations are given in Figure 3.16 and in Figure 3.17. Since $K > 1$ and $B_1 > 0$ ($\mu > 1$ or $\mu' > 1$) at all frequencies, the circuit can be said to be unconditionally stable.

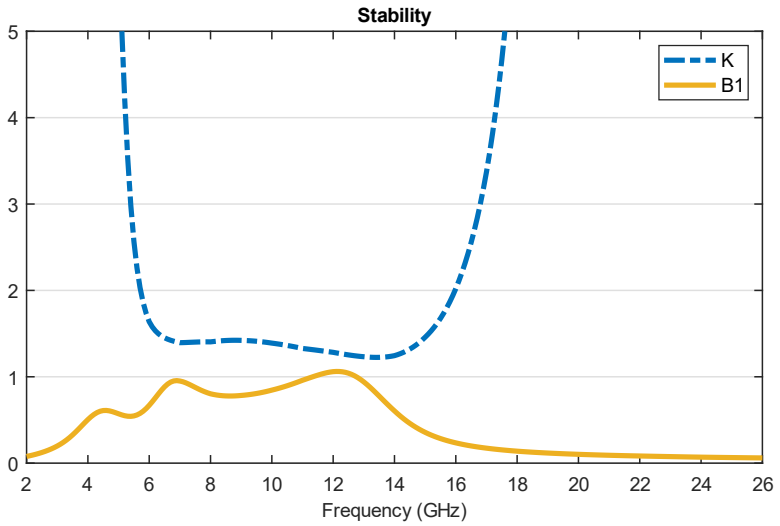


Figure 3.16 Rollet's stability simulation results

Since the circuit is unconditionally stable, it is ready to be combined with the other stages.

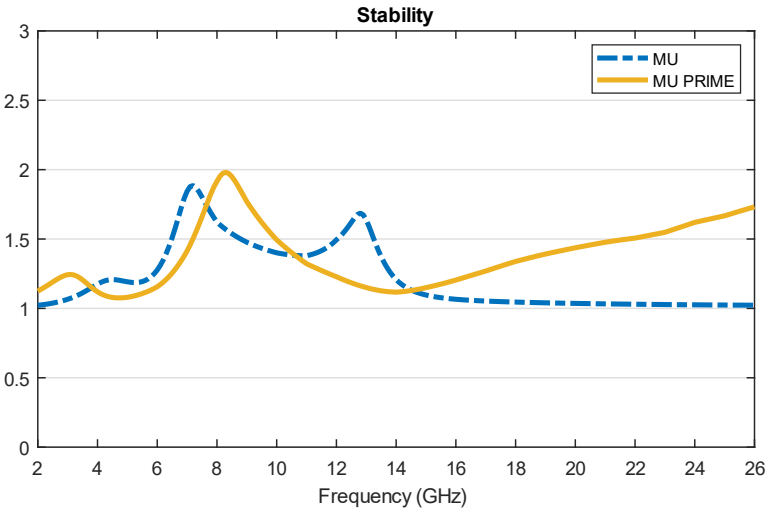
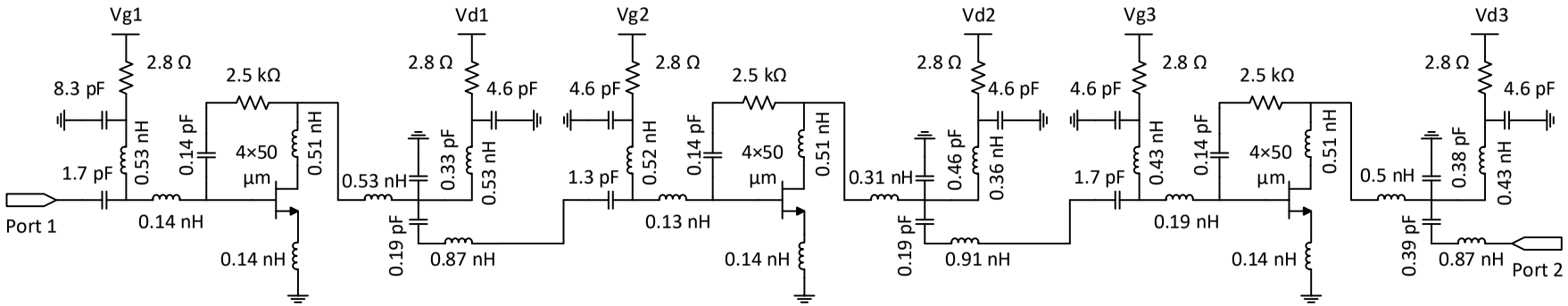
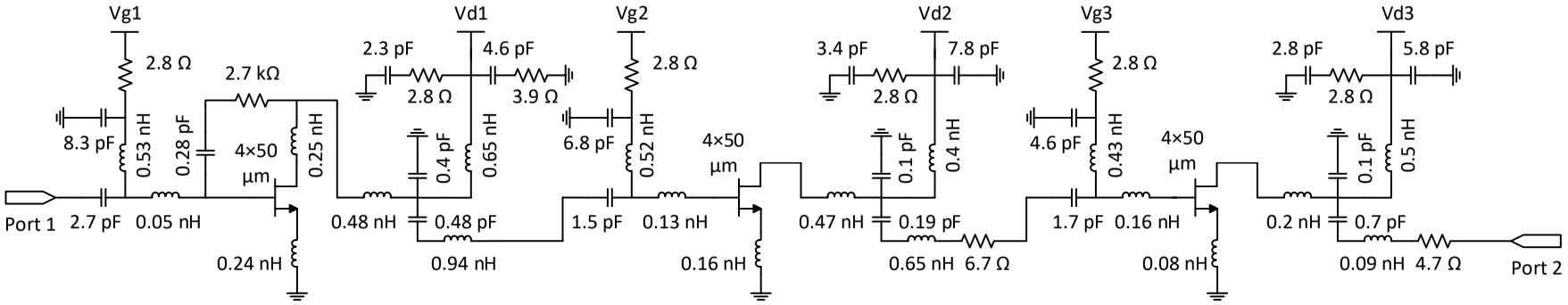


Figure 3.17 μ-factor stability simulation results

Finally, the other stages are designed similarly. After they are combined, the values of the matching elements are optimized to achieve the design goal. Then, the modified stages are re-checked for the stability.



TAPEOUT 1



TAPEOUT 2

Figure 3.18 The schematics of the LNA versions

The schematics of the LNA versions are given in Figure 3.18. Also, the layouts of the first and the second LNAs are given in Figure 3.19 and in Figure 3.20, respectively.

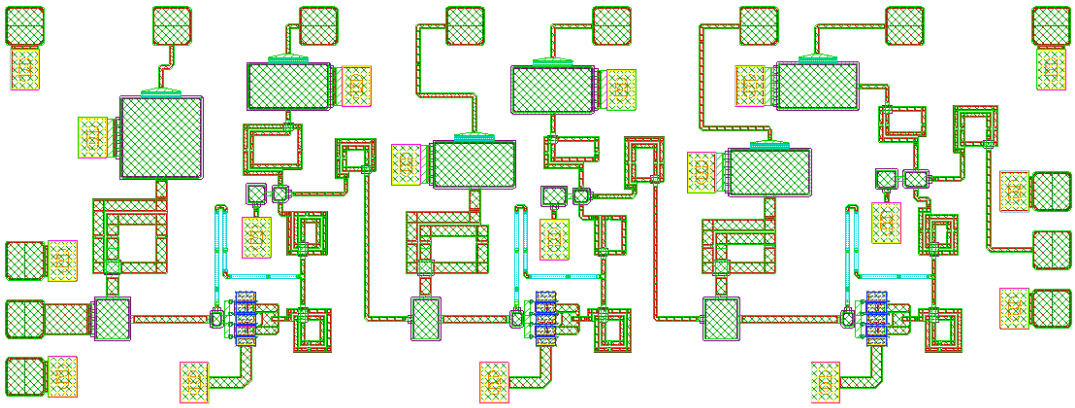


Figure 3.19 The layout of the first LNA (tapeout 1)

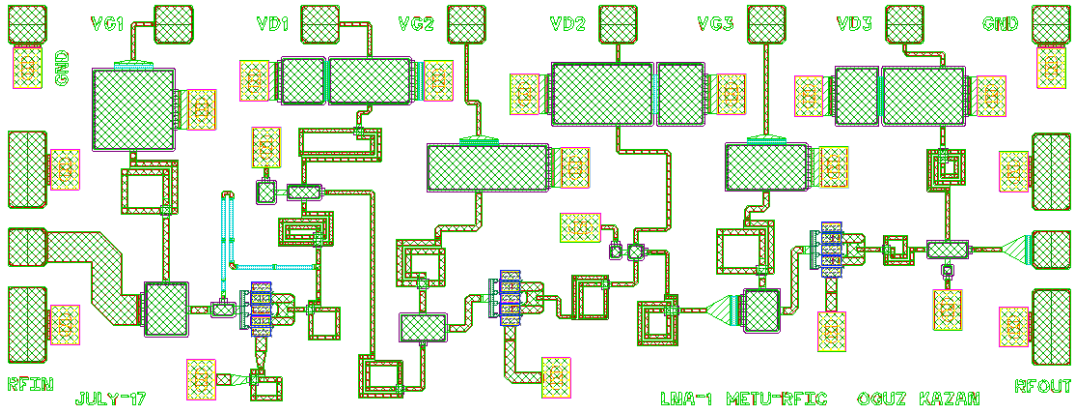


Figure 3.20 The layout of the second LNA (tapeout 2)

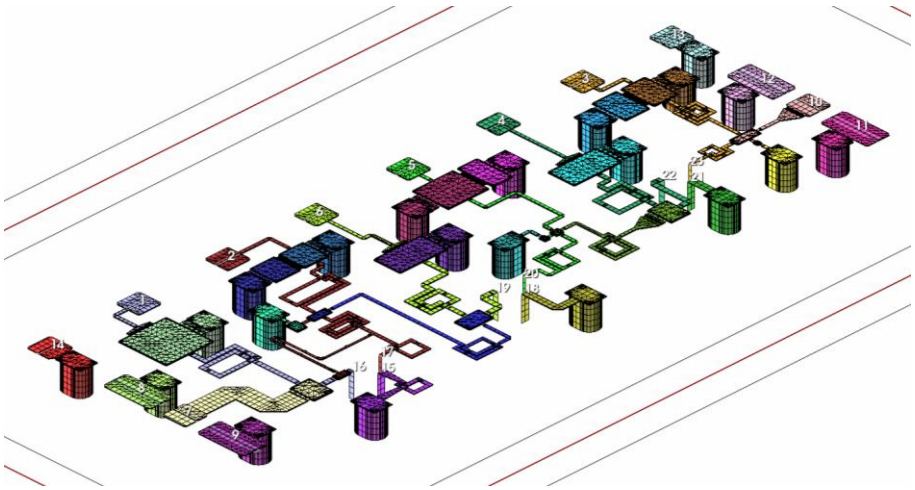


Figure 3.21 The 3D view of the EM structure for the second LNA (tapeout 2)

The layouts in Figure 3.19 and in Figure 3.20 are electromagnetically simulated. The 3D view of the EM structure for the first design is already given in Figure 3.3. For the sake of completeness, the 3D view of the EM structure for the second design is demonstrated in Figure 3.21.

3.5 Simulation Results

In this section, the EM simulation results of two LNA versions are given. One version is from the first tapeout, and the other version is from the second tapeout.

The S-parameter simulation results of the two LNA designs are presented in Figure 3.22 and in Figure 3.23. As can be seen, both designs have more than 20 dB gain over the operating frequencies, achieving the design goal. Both designs in the simulation have an input return loss of better than almost 10 dB at operating frequencies. However, as mentioned previously, the transistor models in the PDK used for the first tapeout are not valid, and the measurement results show that the input return loss fails to be better than 10 dB at frequencies higher than 11 GHz. In order to fix this problem, the second circuit is designed. It should be noted that in the second design, a better gain flatness is achieved over the X-band than the first design.

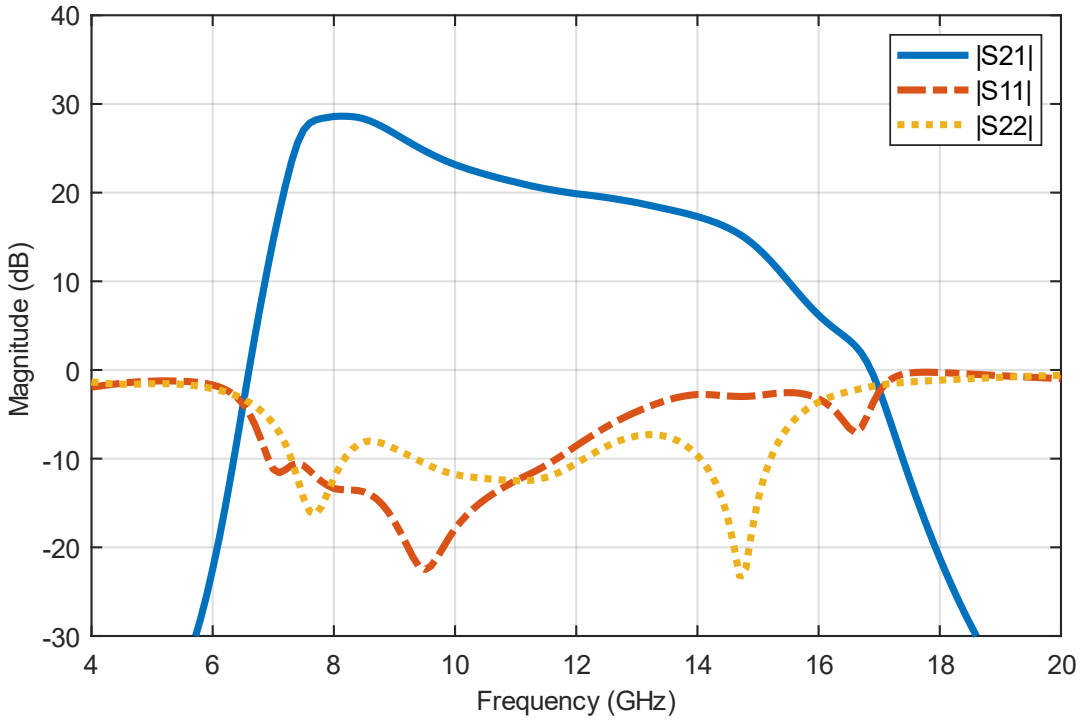


Figure 3.22 S-parameter simulation of the LNA from tapeout 1

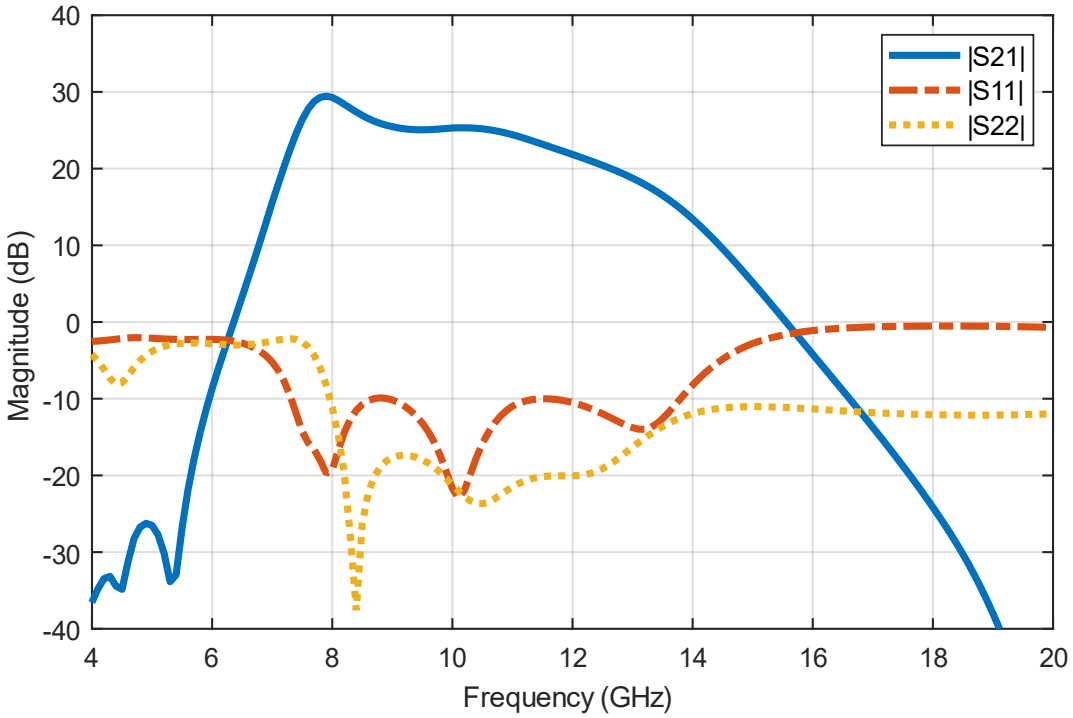


Figure 3.23 S-parameter simulation of the LNA from tapeout 2

The noise figure simulation results are shown in Figure 3.24 and in Figure 3.25.

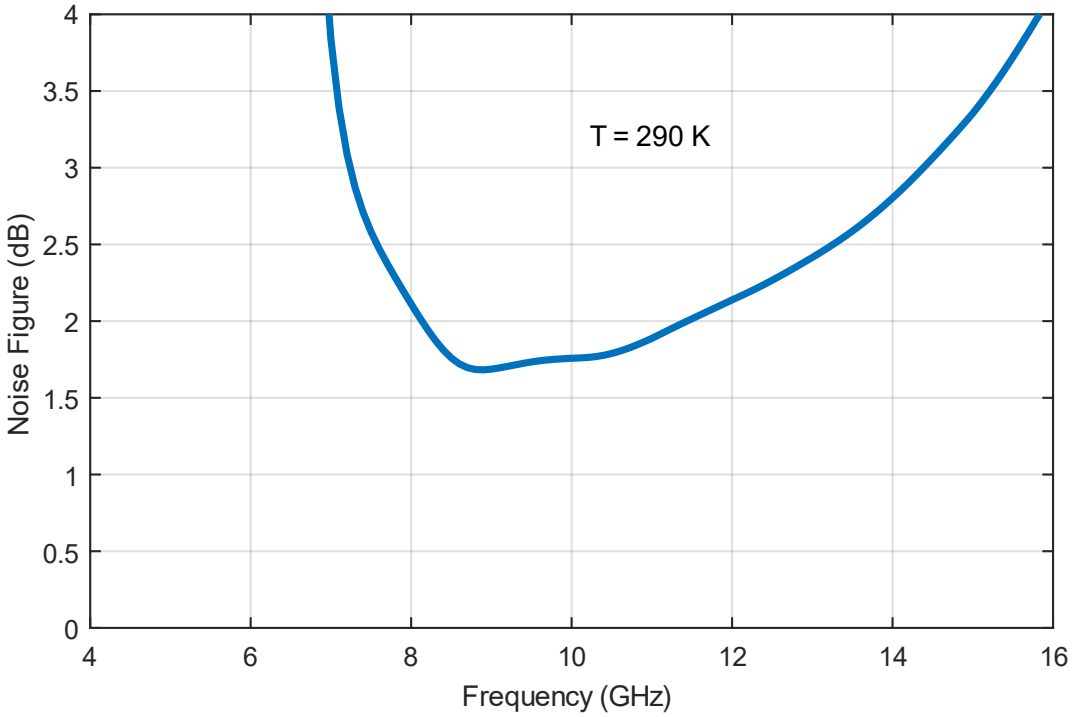


Figure 3.24 Noise figure simulation of the LNA from tapeout 1

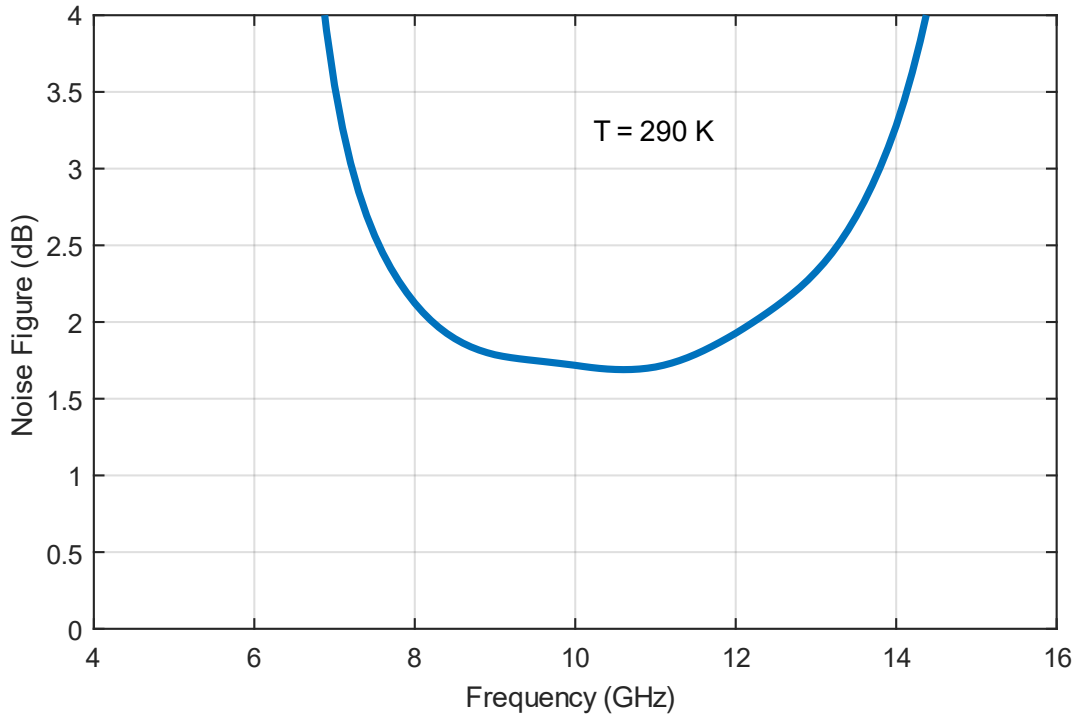


Figure 3.25 Noise figure simulation of the LNA from tapeout 2

The Rollet's stability simulation results are given in Figure 3.26 and in Figure 3.27.

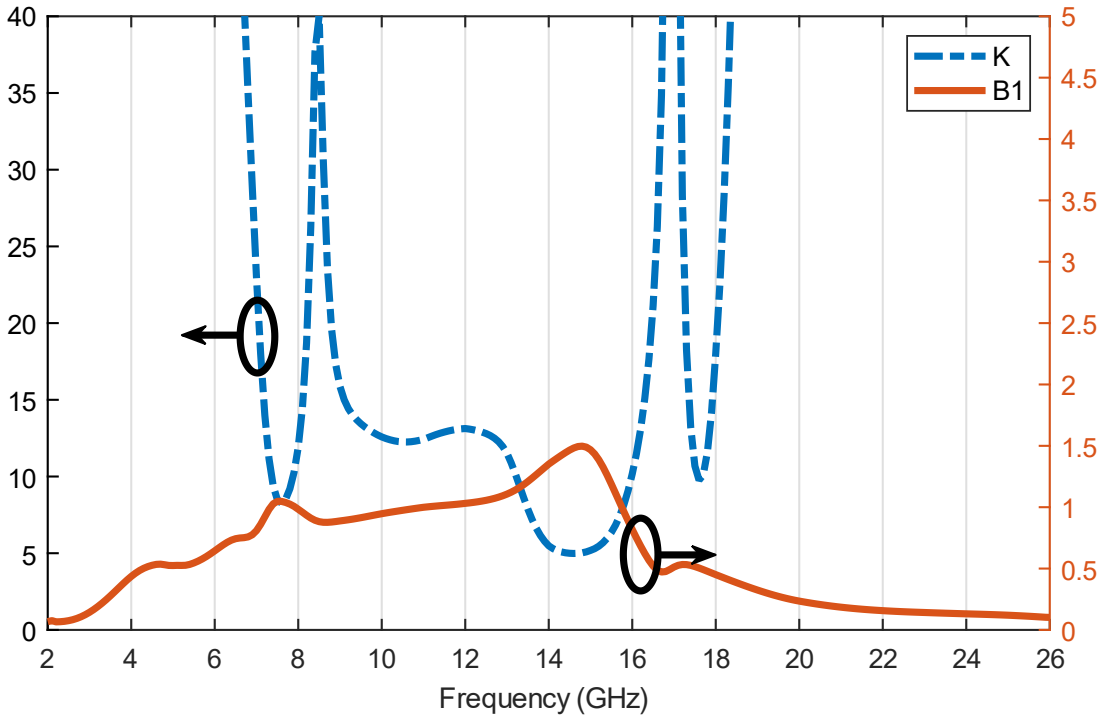


Figure 3.26 Stability simulation of the LNA from tapeout 1

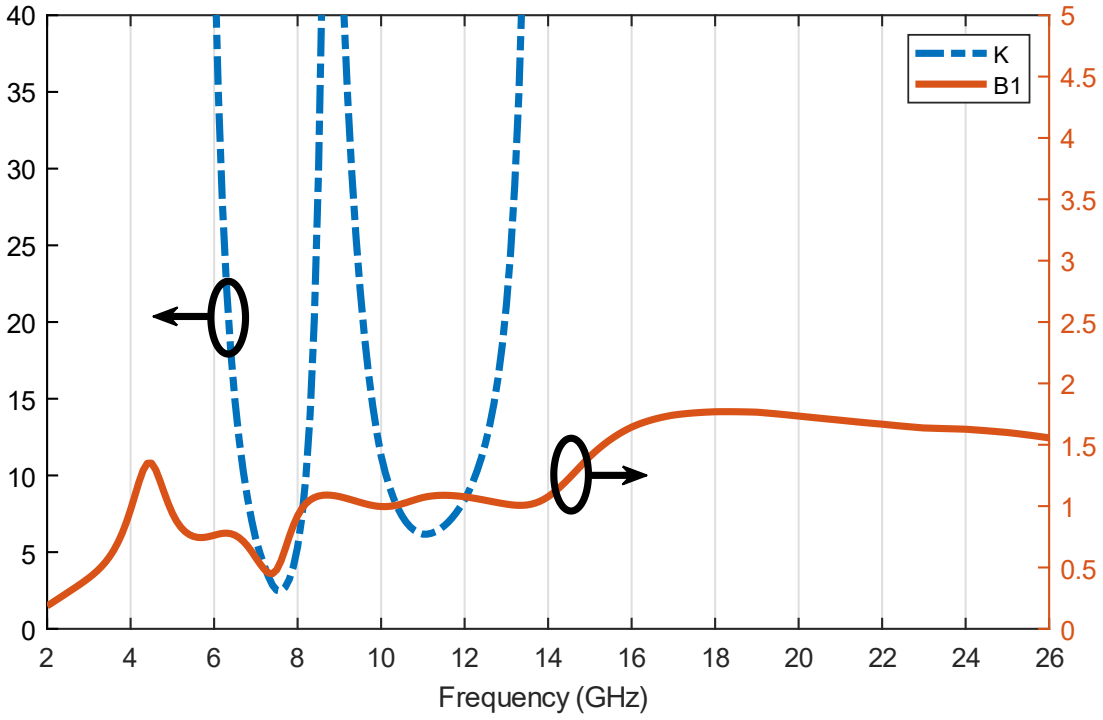


Figure 3.27 Stability simulation of the LNA from tapeout 2

From the noise figure simulations, it is inferred that the manufactured designs will have a measured noise figure of less than 2 dB achieving the design goal.

As one might remember, these simulation results only mean that any passive impedance introduced to one port is mapped to only passive impedance to the other port. This does not ensure stability, even if every stage is unconditionally stable as there might be coupling between stages. To test stability, S-probe technique is also used [50], which is based on the Nyquist criterion. To sample reflections, gamma probes are put into the schematic (see Figure 3.28).

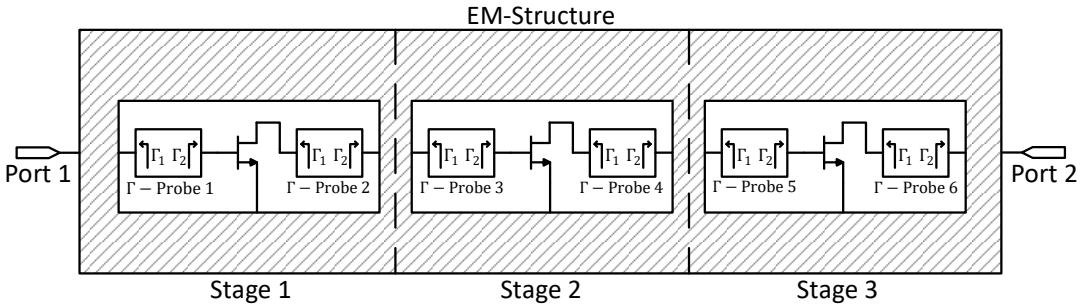


Figure 3.28 The placement of the gamma probes in the LNA schematic

These gamma probes do not affect the operation of the circuit at all. The Nyquist plots are given in Figure 3.29 and Figure 3.30.

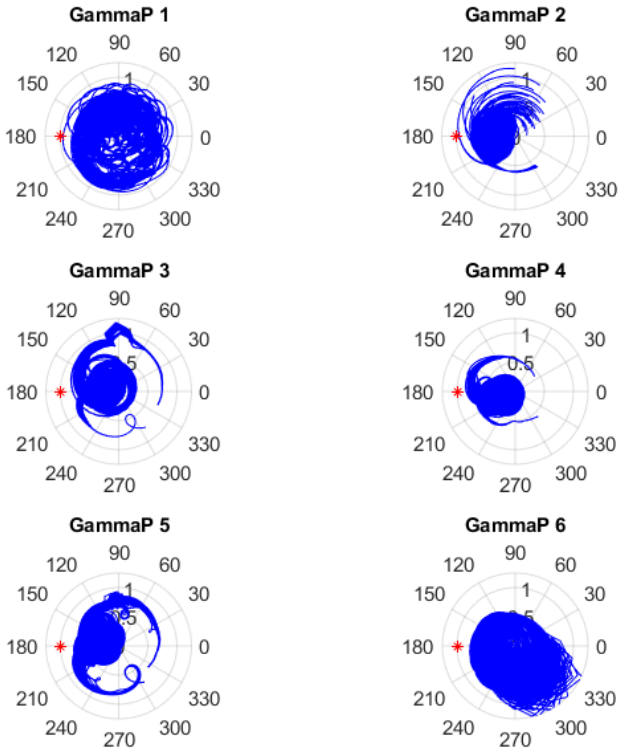


Figure 3.29 S-probe simulation of the LNA from tapeout 1 (the -1 point is red)

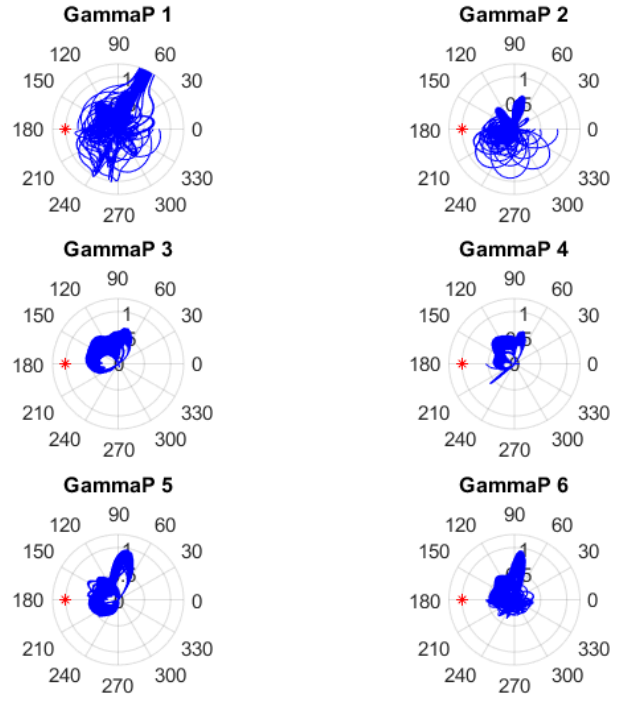


Figure 3.30 S-probe simulation of the LNA from tapeout 2 (the -1 point is red)

As can be seen from the figures, there is no clockwise encirclement of the -1 point. The reason for the multiple contours in the plots is that since each Nyquist plot is for a single pair of source and load impedances, many passive impedance combinations are employed in an effort to cover all passive source and load impedances for unconditional stability. The source and load impedances used in Nyquist plots are shown in Figure 3.31. In fact, more points at the outer edge of the Smith Chart should also be covered.

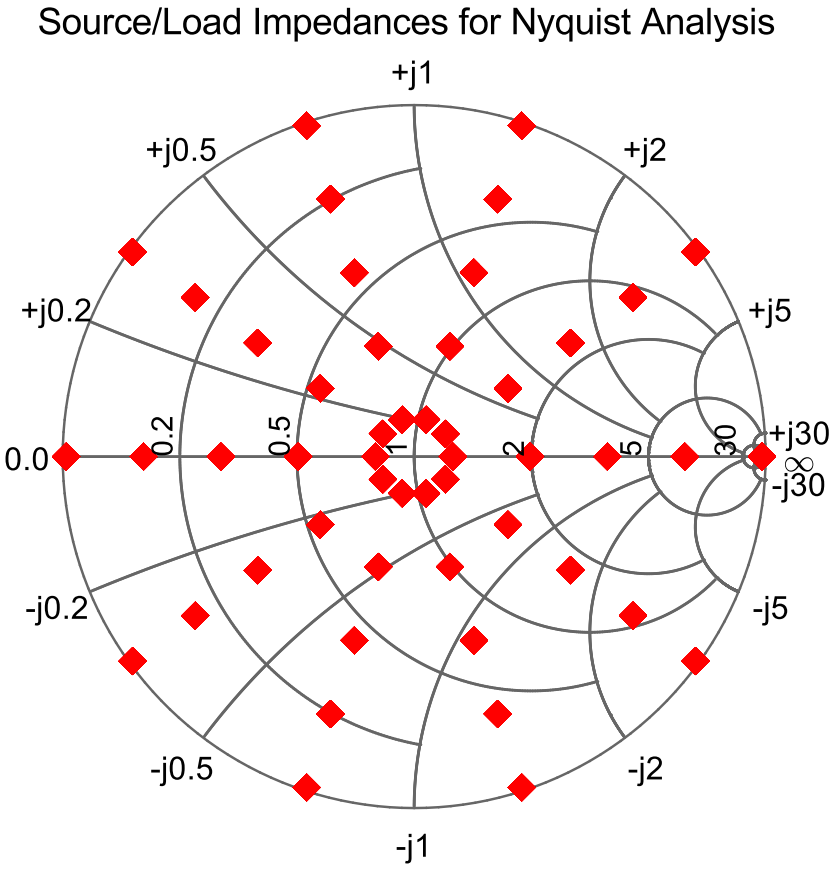


Figure 3.31 Source and load impedances used for Nyquist analysis

3.6 Summary

In this chapter, the design procedure of the LNAs is explained. Each successive design step is discussed consecutively. Also, the complete schematics and the simulation results are given. In the first design, each core circuit used is identical resulting in a sloped gain. To fix this, in the second design, the core circuits of the second and the third stages are modified so that they have higher $G_{T,max}$ at the high-end of the X-band (10-12 GHz).

In Figure 3.32, the summary of the design procedure used in this work is given.

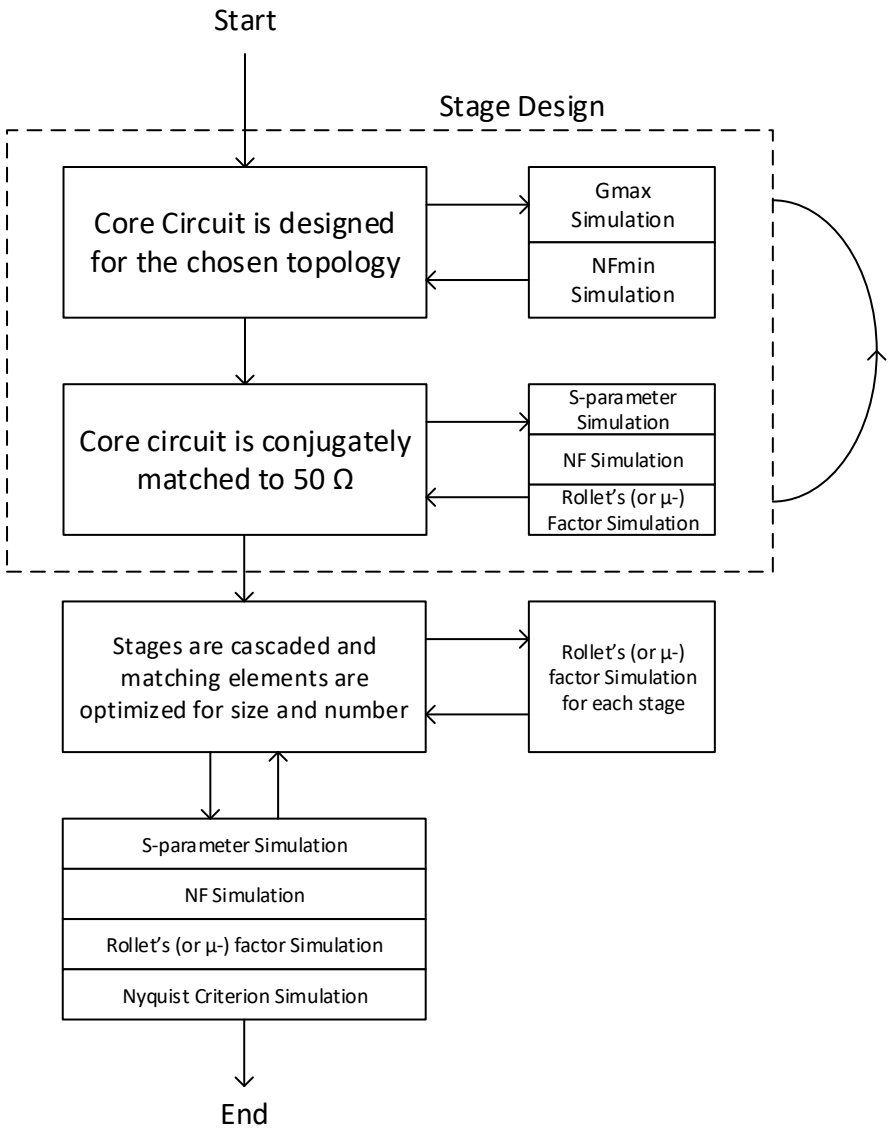


Figure 3.32 The block diagram of the LNA design procedure used in this work

CHAPTER 4

MEASUREMENT AND EVALUATION

Both designs presented in Chapter 3 are sent out for production. After the manufactured samples are received, they are measured and evaluated. The micro-photographs of the fabricated LNAs, with dimensions 2.8 × 1.3 mm^2 (including pads), are shown in Figure 4.1 and Figure 4.2.

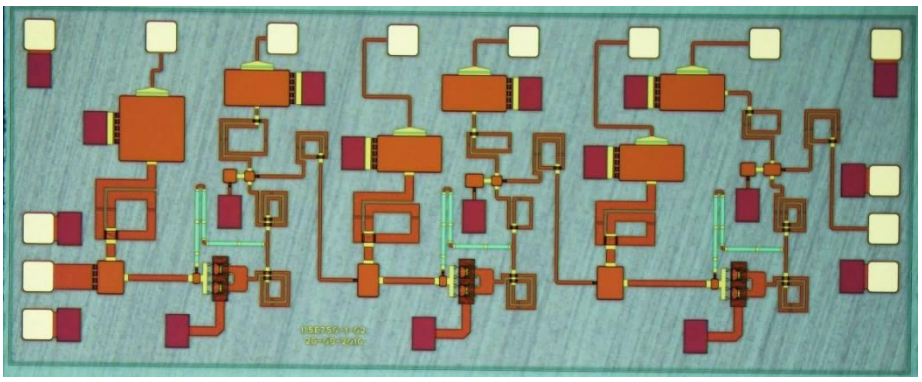


Figure 4.1 The micro-photograph of the fabricated LNA from tapeout 1

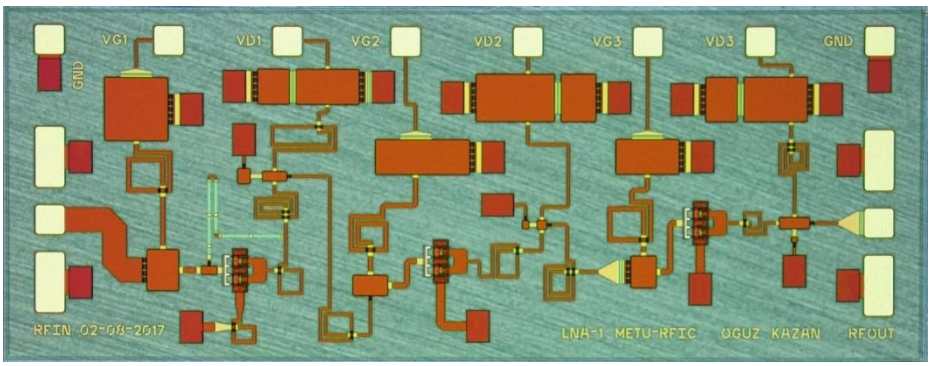


Figure 4.2 The micro-photograph of the fabricated LNA from tapeout 2

The drain voltages of transistors for the first LNA version are 10 V, and their drain currents are 20 mA. Therefore, the power dissipation of the first LNA is 0.6 W. On the other hand, although the drain voltages of 10 V are supposed to be applied, they are 6 V for the second LNA version with the drain currents of 20 mA (0.36 W). The reason is that simulation results for the second tapeout do not match the measurement results with the drain voltages of 10 V applied.

This chapter presents measurement results and their comparisons with the simulation results. The inconsistency between the simulation and measurement results is also explained, and then a possible solution to overcome this problem is given.

4.1 Measurement Tools

In this section, some of the instruments used in the measurement of the LNAs are briefly explained for the unfamiliar reader.

4.1.1 Network Analyzer

A network analyzer is used to determine the network parameters of an electrical circuit. In general, they measure S-parameters as network parameters. Some of the network analyzer types also measure the noise figure of a two-port. A network analyzer needs calibrating before using it. What a network analyzer basically does is, it sends a signal from one port and measures the response from all its ports at a certain frequency, and it repeats this step for each frequency in the measurement range. Also, it sends a signal from the other port and repeats the previous steps. In S-parameter and noise figure measurements, a network analyzer is used.

4.1.2 Signal Generator

A signal generator is used to send a signal power at a certain frequency. It allows us to change the power of the signal and the frequency of the signal. When the maximum power it can deliver is not sufficient, an external amplifier can be used. For the OIP_3 measurements where two-tone signals are needed, two signal generators are used since signal generators used can supply only a one-tone signal.

4.1.3 Spectrum Analyzer

A spectrum analyzer is used to determine the power of input signal at full range of frequencies of the instrument. It can also measure the noise figure of a system. Since it does not have a port to send a signal, the measurement generally needs a signal generator. For the linearity measurements, a spectrum analyzer together with signal generators is used.

4.1.4 Probe Station

Most of the measurements are performed using a calibrated probe station. The probe station utilizes precisely positioned needles (probes) to make contact to the pads, and it allows us to directly measure the dies. Since a printed circuit board is not used, the effects of wirebonds and the microstrip lines are eliminated as shown in Figure 4.3. The responses of the dies are monitored using a network analyzer or a spectrum analyzer.

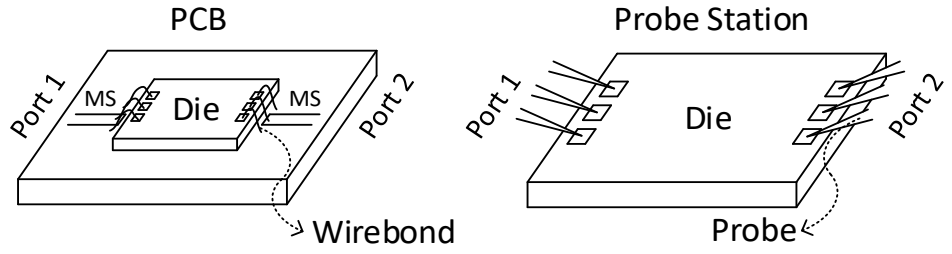


Figure 4.3 A schematic showing the difference between PCB and probe station measurement

4.2 S-Parameter Measurement and Simulation Comparison

The S-parameters of the dies are measured on wafer using an Agilent Network Analyzer (E8361A). Five samples are measured for the first LNA, and four samples are measured for the second LNA. The schematic of the S-parameters measurement setup is shown in Figure 4.4.

The S-parameter comparisons between the simulation and the measurement results for the LNA from the tapeout 1 are separately given in Figure 4.5, Figure 4.6 and Figure 4.7. The simulation results shown in Figure 4.5, Figure 4.6 and Figure 4.7 are different than those of Figure 3.22.The reason for the difference between the simulation results

in this chapter and that in Chapter 3 is that after the design is sent for production, the fab updates the PDK and the measurement results are closer to the results for the updated PDK. In this section, only the simulation results of the updated PDK is given.

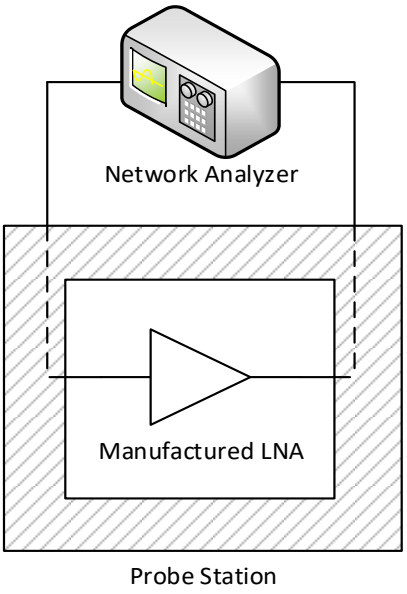


Figure 4.4 The schematic of the S-parameter measurement setup

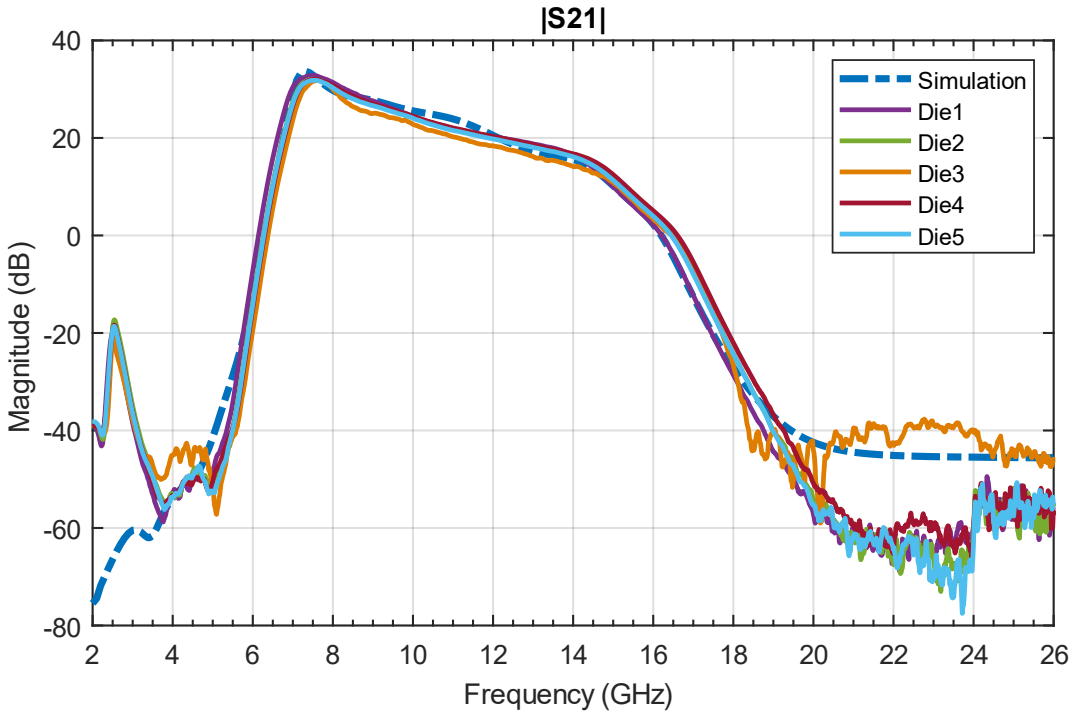


Figure 4.5 The comparison of the simulation and measurement results for the magnitude of S_{21} (tapeout 1)

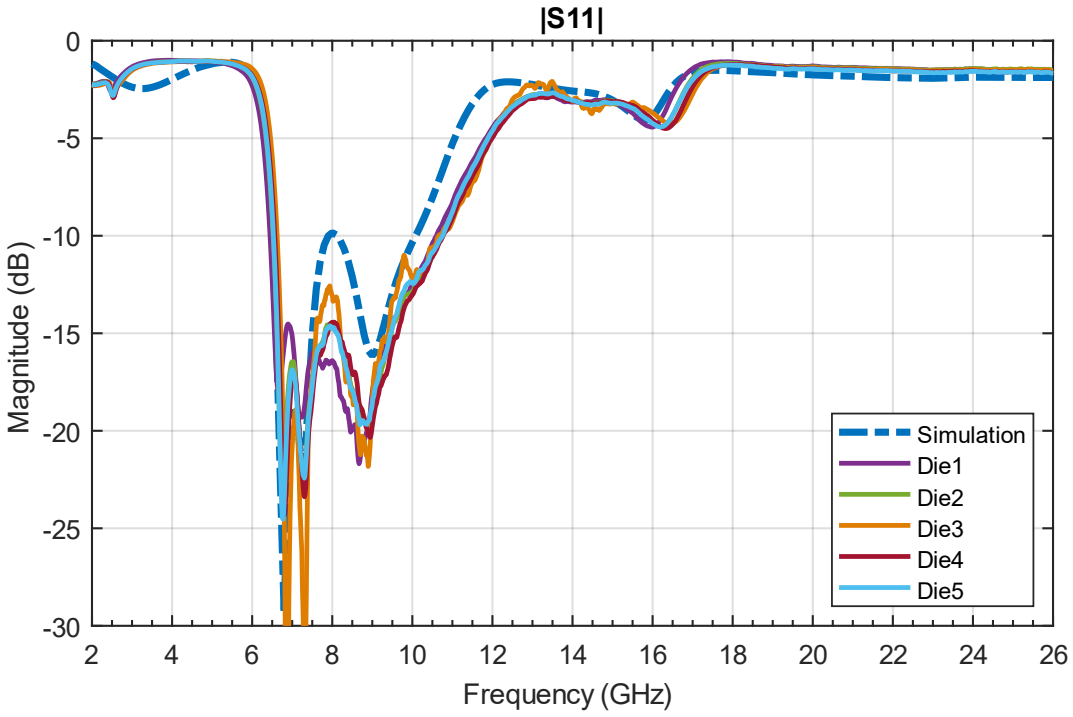


Figure 4.6 The comparison of the simulation and measurement results for the magnitude of S_{11} (tapeout 1)

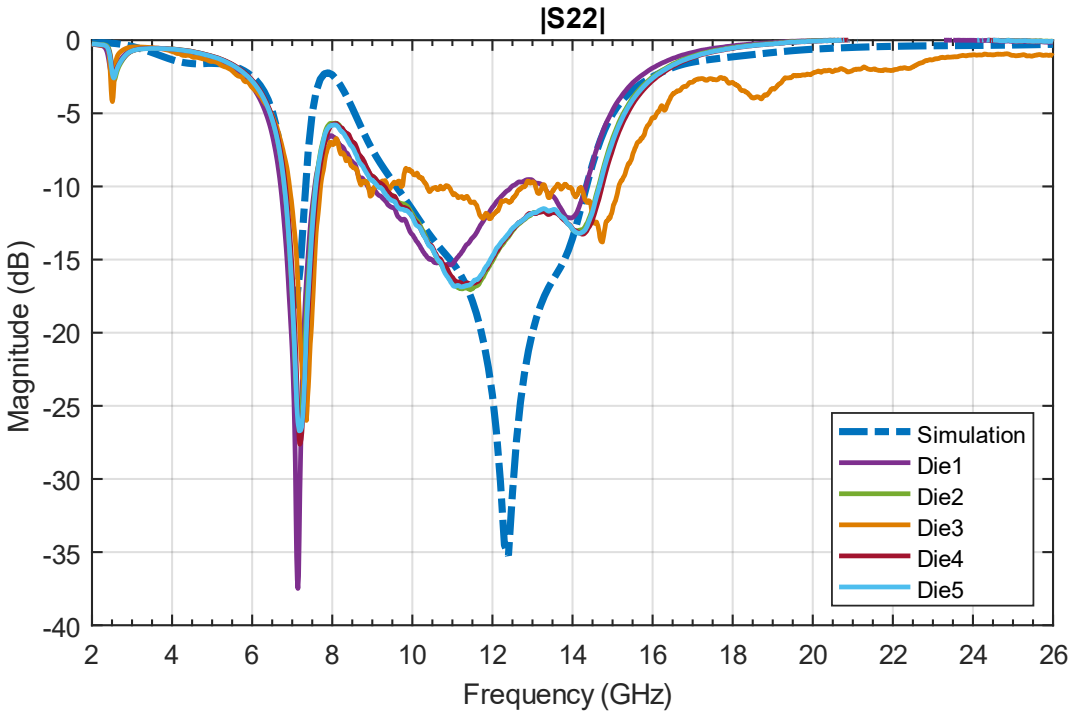


Figure 4.7 The comparison of the simulation and measurement results for the magnitude of S_{22} (tapeout 1)

As can be seen from Figure 4.5, the LNA has a gain of more than 20 dB over the operating frequencies, meeting the design goal of a gain of minimum 20 dB at the X-band. Also, the return losses are better than 10 dB covering most of the operating frequencies, as depicted in Figure 4.6 and Figure 4.7.

The S-parameter comparisons between the simulation and the measurement results for the LNA from the tapeout 2 are separately given in Figure 4.8, Figure 4.9 and Figure 4.10.

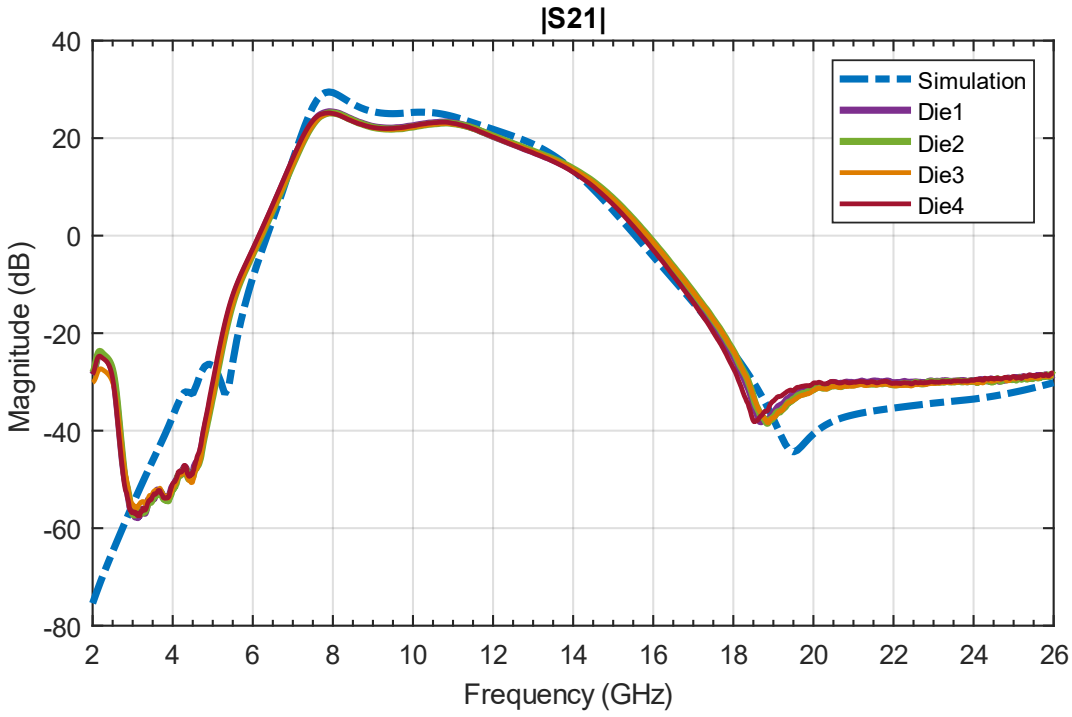


Figure 4.8 The comparison of the simulation and measurement results for the magnitude of S_{21} (tapeout 2)

Again, as can be seen from Figure 4.8, the LNA has a gain of more than 20 dB over the operating frequencies. Also, the return losses (see Figure 4.9 and Figure 4.10) are better than 10 dB covering the operating frequencies.

The models are expected to be valid for the drain voltages of 10 V, but not 6V. When this amount is applied, the measurement results do not match the simulated ones at all. In one of the meetings with the fab representative, it is explained that they replace one of the reactors which is used in the manufacturing. It is now considered that those transistor model used for the second tapeout are not valid anymore.

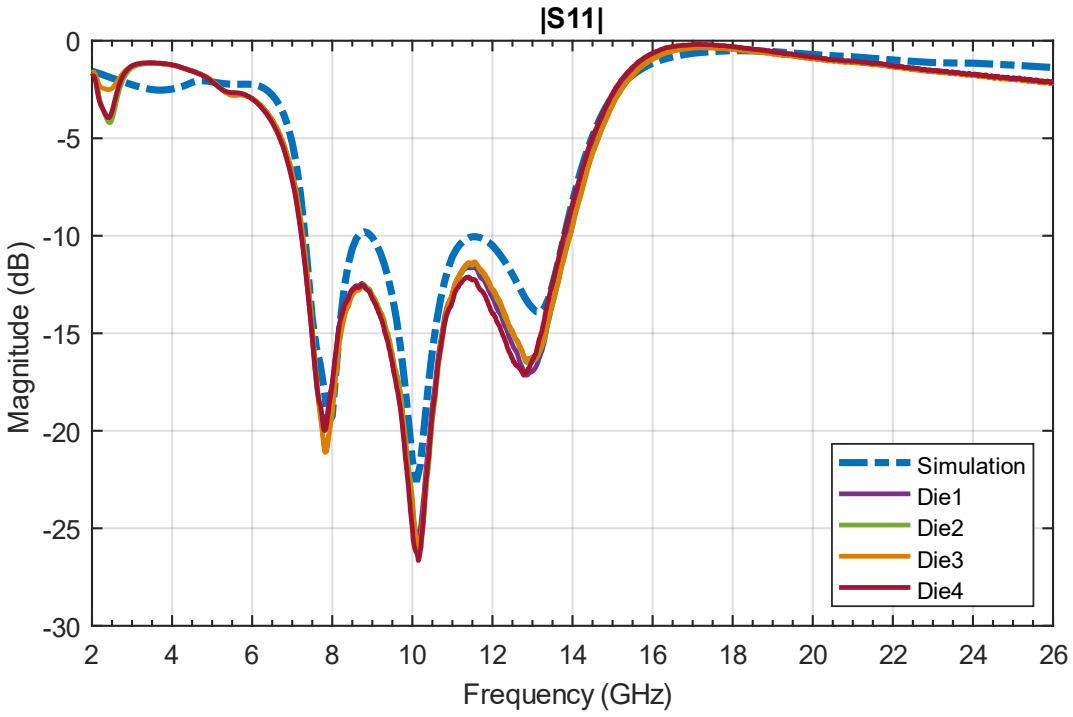


Figure 4.9 The comparison of the simulation and measurement results for the magnitude of S_{11} (tapeout 2)

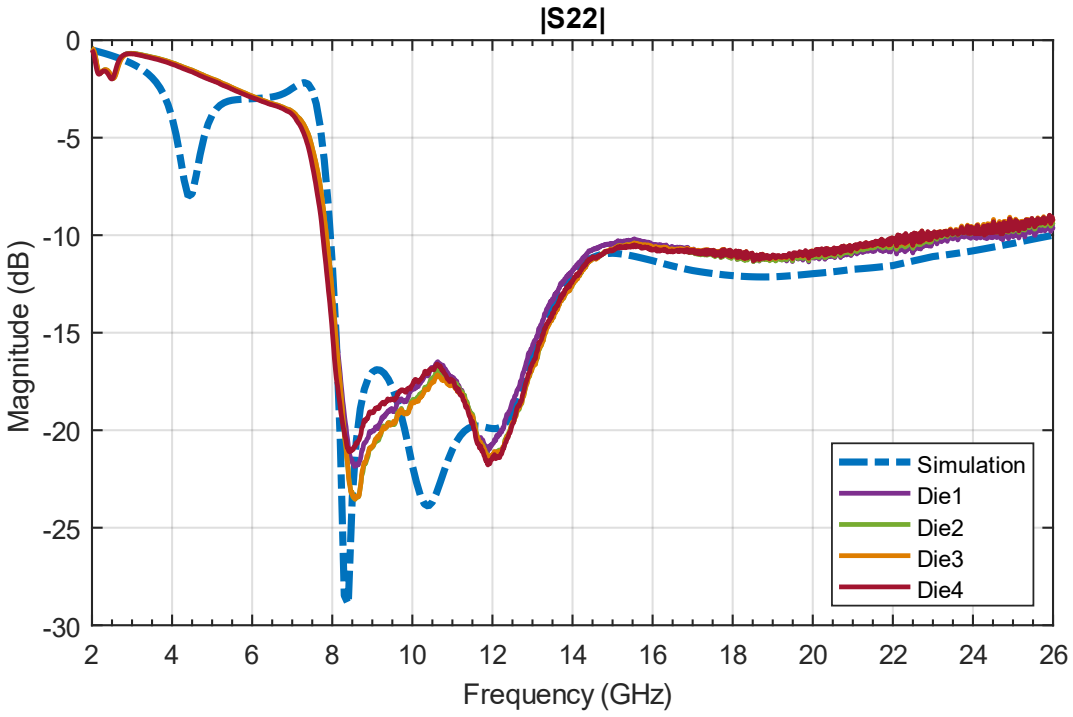


Figure 4.10 The comparison of the simulation and measurement results for the magnitude of S_{22} (tapeout 2)

4.3 Noise Measurement and Simulation Comparison

In the beginning, the noise measurements are performed on wafer using an Agilent Spectrum Analyzer (E4446A). After measuring the whole system's noise, the effects of the probe cables are eliminated using the method in Section 2.1.6. However, to increase the measurement precision, the noise measurements are re-performed on wafer using another setup with an Agilent Network Analyzer (N5242A, option 029). The schematic of the noise measurement setup is shown in Figure 4.11. Also, it should be indicated that five samples are measured for the first LNA, and three samples are measured for the second LNA.

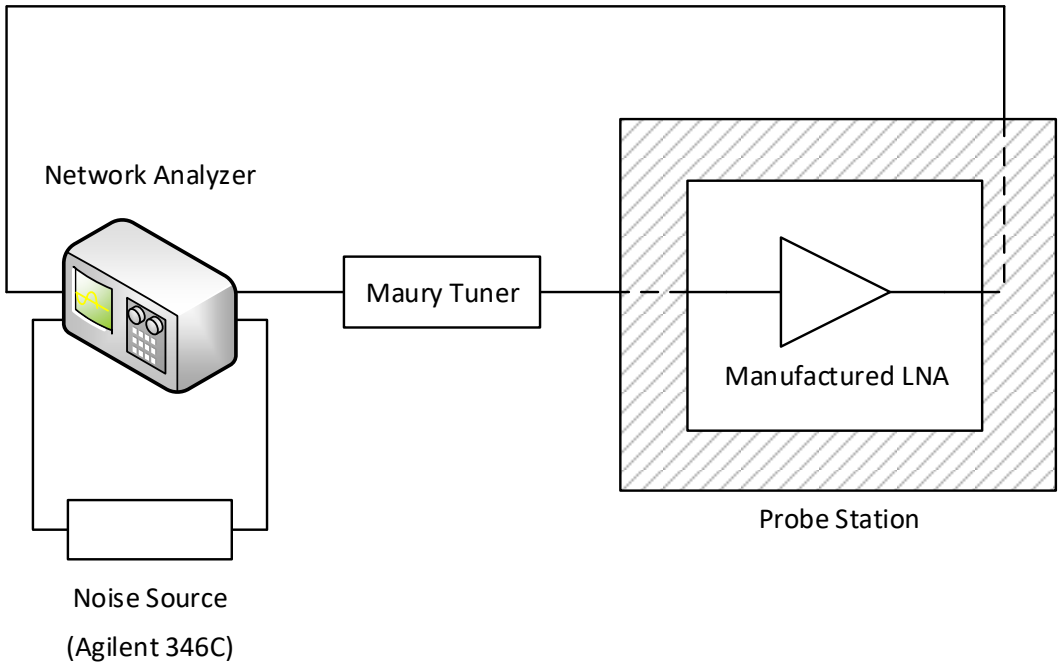


Figure 4.11 The schematic of the noise figure measurement setup

The noise figure comparison between the simulation and the measurement results for the LNA from the tapeout 1 is given in Figure 4.12. As can be seen from Figure 4.12, samples have a noise figure of less than 2 dB at the X-band, meeting the design goal.

The noise figure comparison between the simulation and the measurement results for the LNA from the tapeout 2 is given in Figure 4.13. Unfortunately, as can be seen from Figure 4.13, samples have a noise figure of more than 2 dB over operating frequencies.

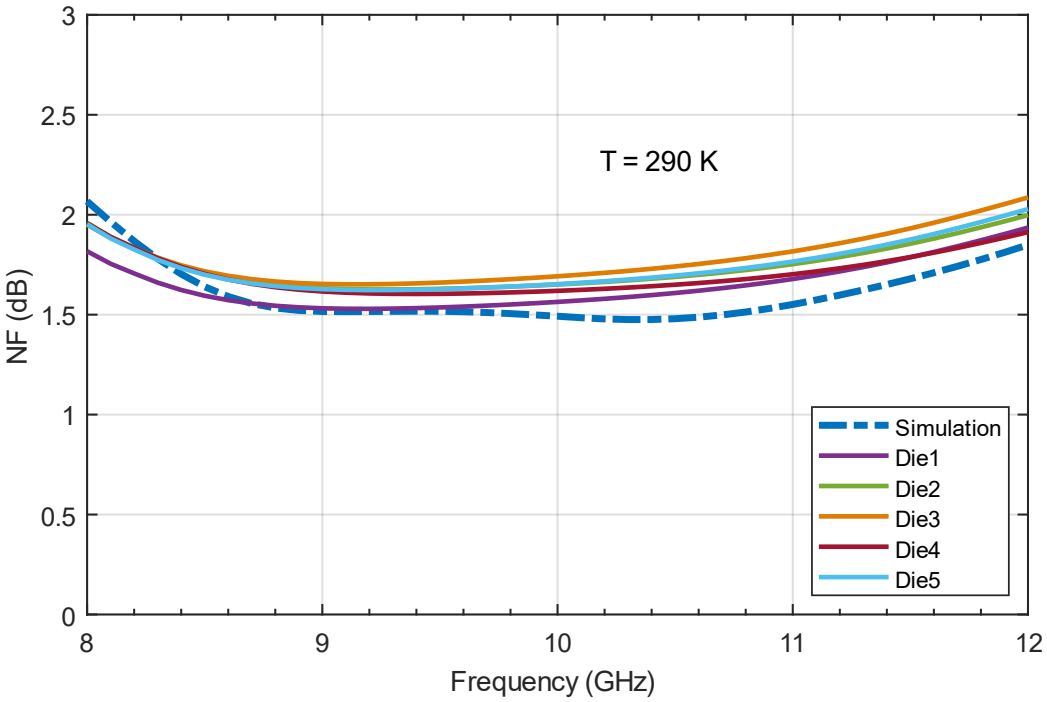


Figure 4.12 The comparison of the simulation and measurement results for the noise figure (tapeout 1)

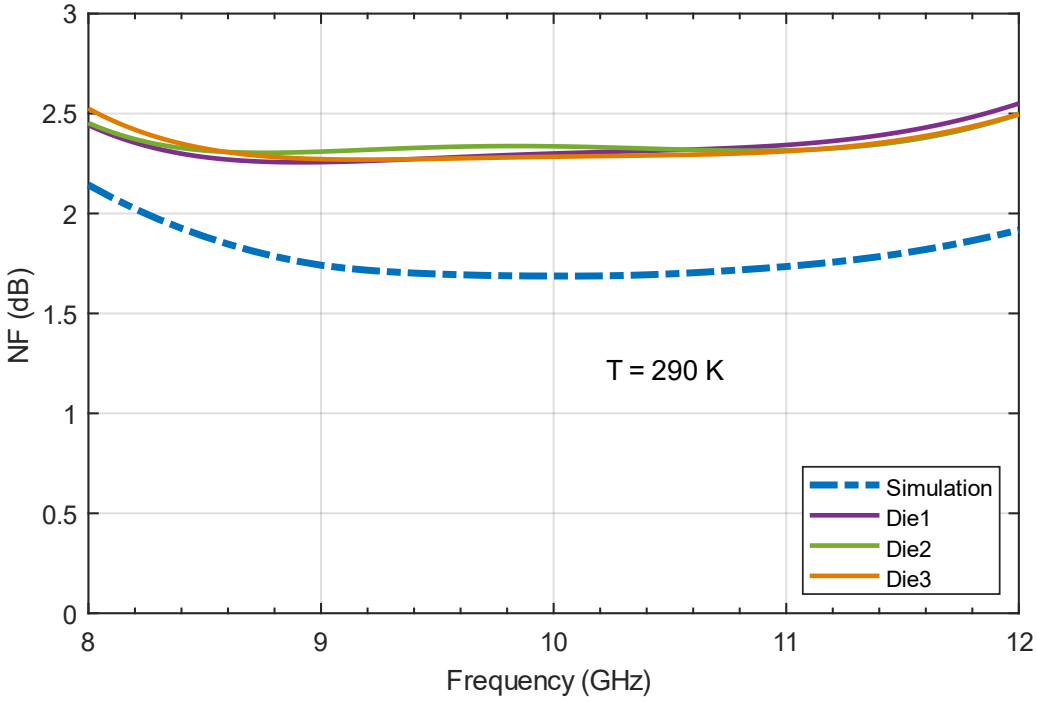


Figure 4.13 The comparison of the simulation and measurement results for the noise figure (tapeout 2)

The noise measurement results for the first design are close to the simulation results, indicating that the simulation error is negligible and that the transistor models used in the simulation is valid. On the other hand, for the second design, the noise figure results are higher than the simulated results. This is not unexpected. One of the reasons for this is that the models are not valid for this tapeout. Another reason is that the bias of the transistors in the measurements is different from the bias of the transistor models used in the simulation.

4.4 Linearity Measurement Results

The linearity measurements are performed on wafer using an Agilent Spectrum Analyzer (E4446A) and Agilent Signal Generators (E8257C and E8257D). The schematic of the OIP_3 measurement setup is shown in Figure 4.14, and that of the P_{1dB} measurement setup is given in Figure 4.15.

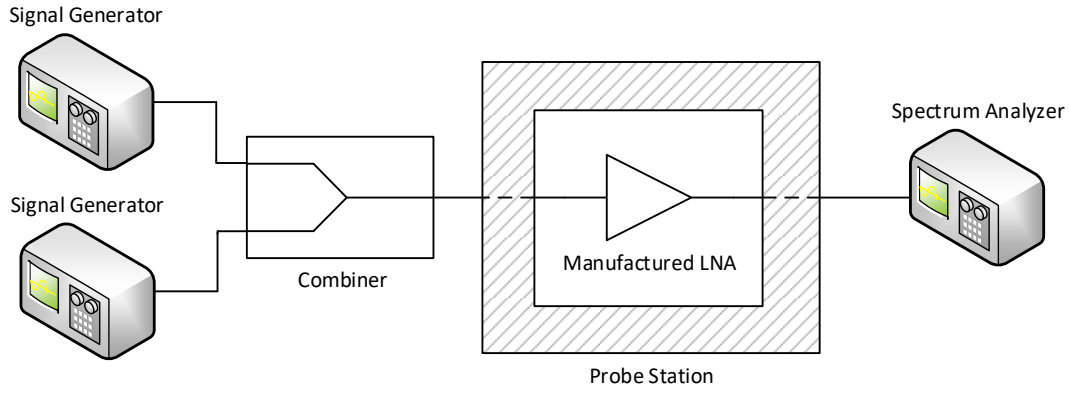


Figure 4.14 The schematic of the OIP_3 measurement setup

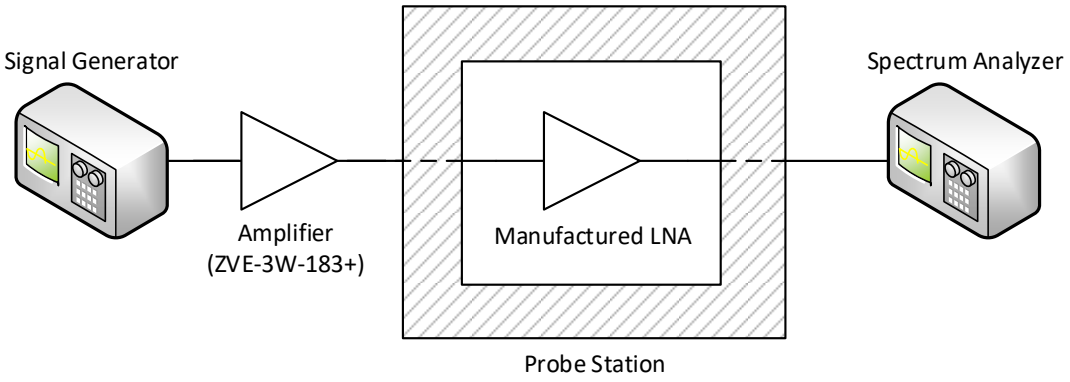


Figure 4.15 The schematic of the P_{1dB} measurement setup

As mentioned previously, since there are no non-linear transistor models in the PDK used for the tapeouts, non-linear simulations are not available.

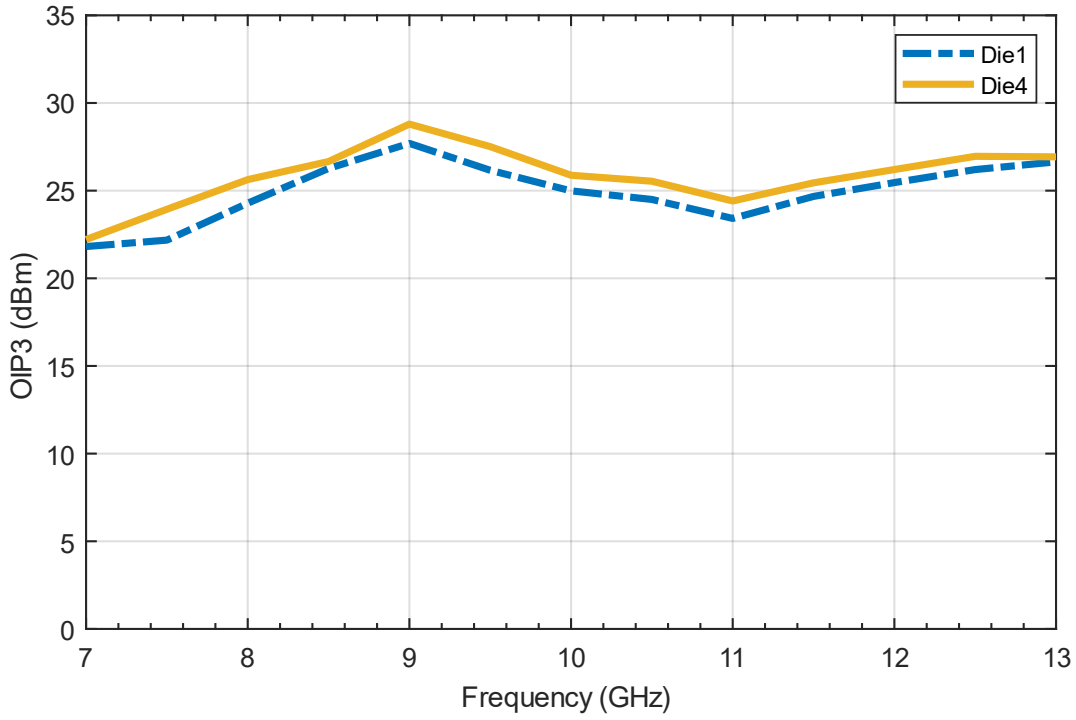


Figure 4.16 The measurement results for OIP_3 (tapeout 1)

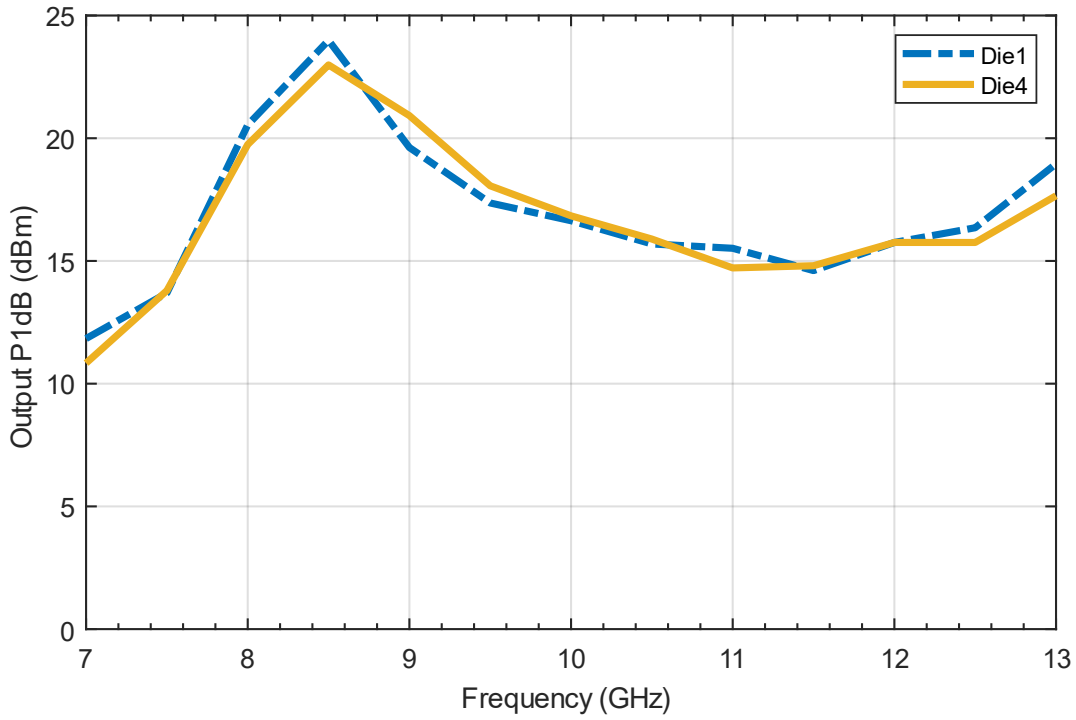


Figure 4.17 The measurement results for P_{1dB} (tapeout 1)

The OIP_3 measurement results of the tapeout-1 LNA are given in Figure 4.16, and the output P_{1dB} measurement results of the tapeout-1 LNA are shown in Figure 4.17.

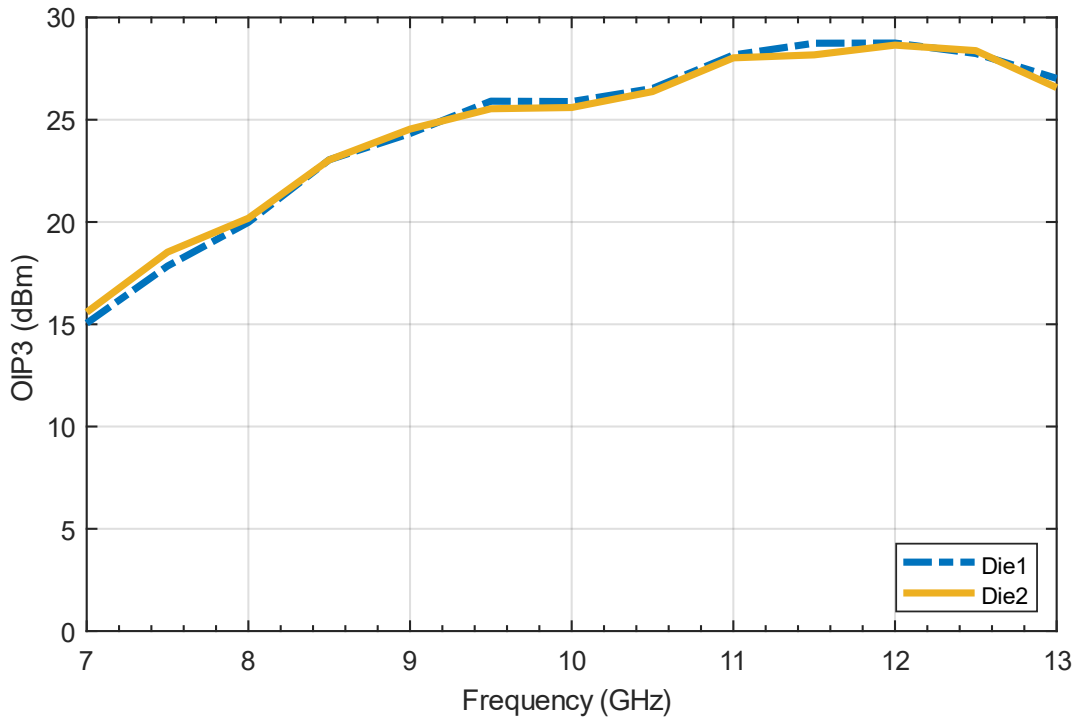


Figure 4.18 The measurement results for OIP_3 (tapeout 2)

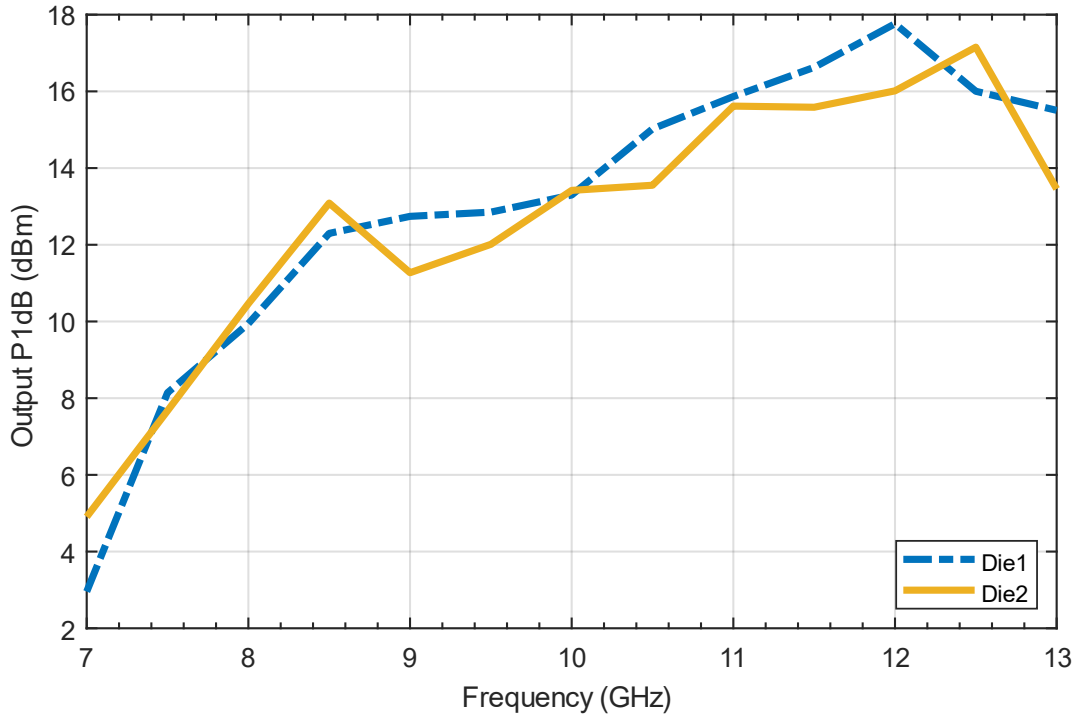


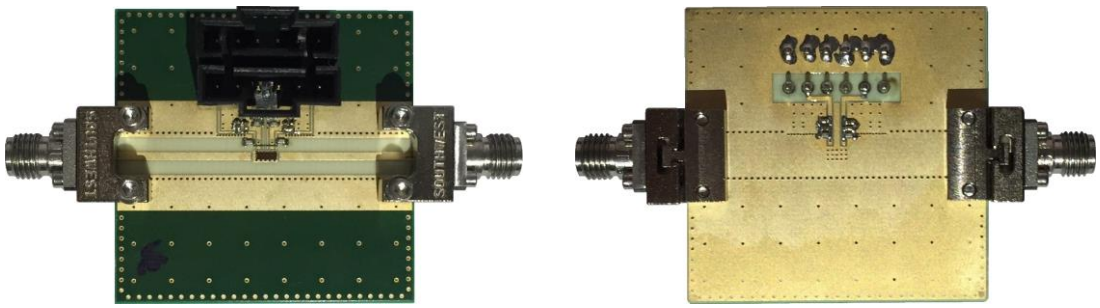
Figure 4.19 The measurement results for P_{1dB} (tapeout 2)

The OIP_3 measurement results of the tapeout-2 LNA are given in Figure 4.18, and the output P_{1dB} measurement results of the tapeout-2 LNA are shown in Figure 4.19.

The first LNA has an output P_{1dB} of more than 15 dB as expected over the X-band. However, since the drain voltages of the second LNA is lower than that of the first LNA, the output P_{1dB} is lower for that design. Moreover, the offset between OIP_3 between output P_{1dB} can be observed from Figure 4.16, Figure 4.17, Figure 4.18 and Figure 4.19. The value of this offset is supposed to be around 9.64 dB as expected from (2.48). The offset deviation from 9.64 dB is probably due to the measurement error.

4.5 Robustness Tests

The input cable of the probe station limits the maximum power that can be delivered to the input of the LNA as the long cables are quite lossy. In order to perform robustness tests, a PCB is designed in an effort to overcome the limitations introduced by the lossy probe station cables. The manufactured PCB with one of the LNAs on it is demonstrated in Figure 4.20.



Top view of the PCB Bottom view of the PCB

Figure 4.20 The manufactured PCB with one of the LNAs on it

The robustness tests are performed using an Agilent Spectrum Analyzer (E4446A) and an Agilent Signal Generator (E8257C). The test setup for the input power stress test is shown in Figure 4.21. In this setup, the power delivered by the amplifier connected at the input of the LNA is limited. Even if the losses introduced by the microstrip lines are much less than that by the probe station cables, input powers (at 8 GHz and at 10 GHz) of only up to 2.5 W are applied to the LNA.

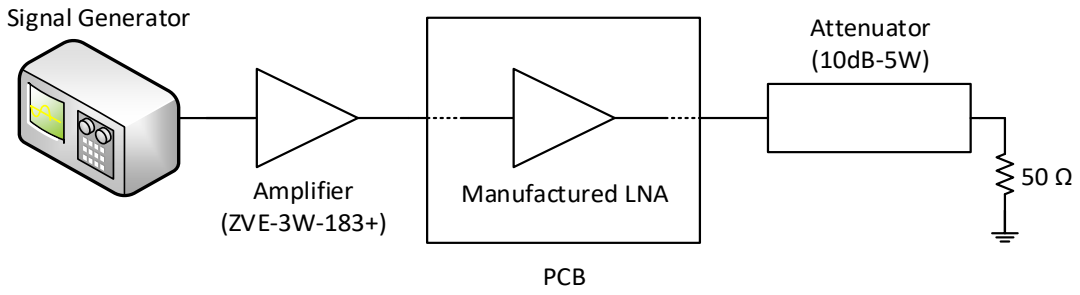


Figure 4.21 The setup for the input power stress test

The noise figure measurement setup for the robustness test is shown in Figure 4.22.

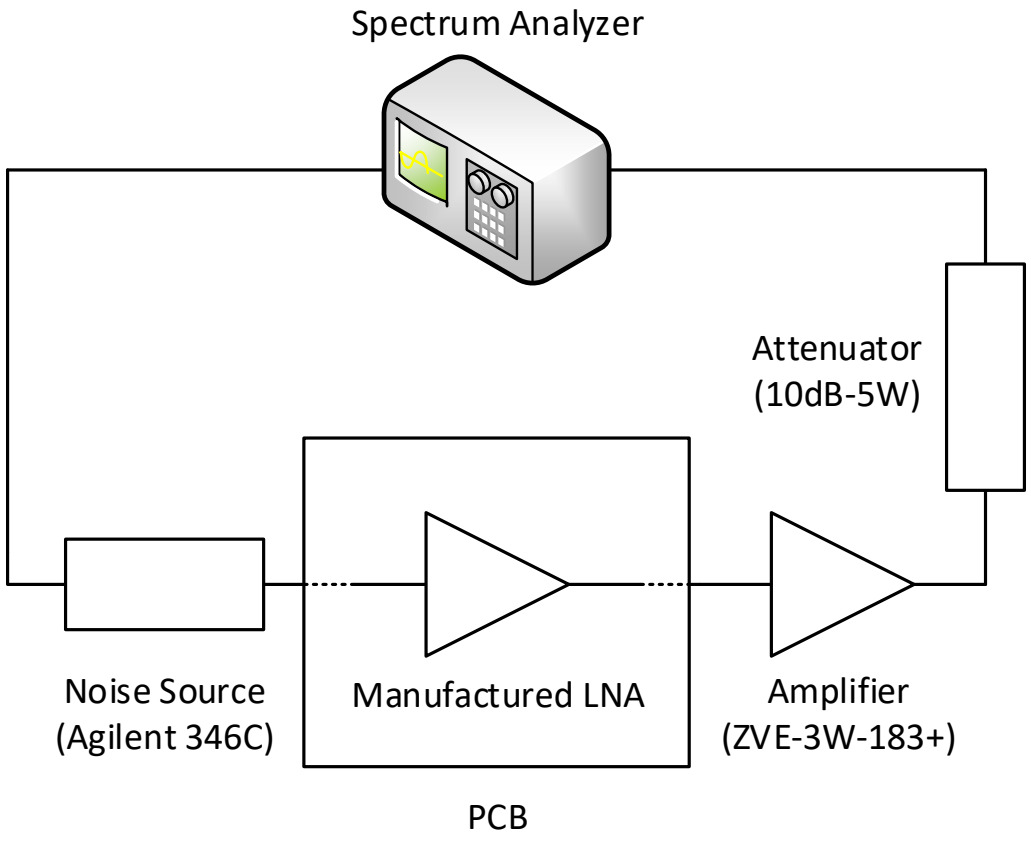


Figure 4.22 The noise figure measurement setup for the robustness test

Noise figure measurement results before and after input power stresses are given in Figure 4.23 and Figure 4.24. In the results of Figure 4.23 and Figure 4.24, the effects of connectors, microstrip lines and wirebonds are not de-embedded.

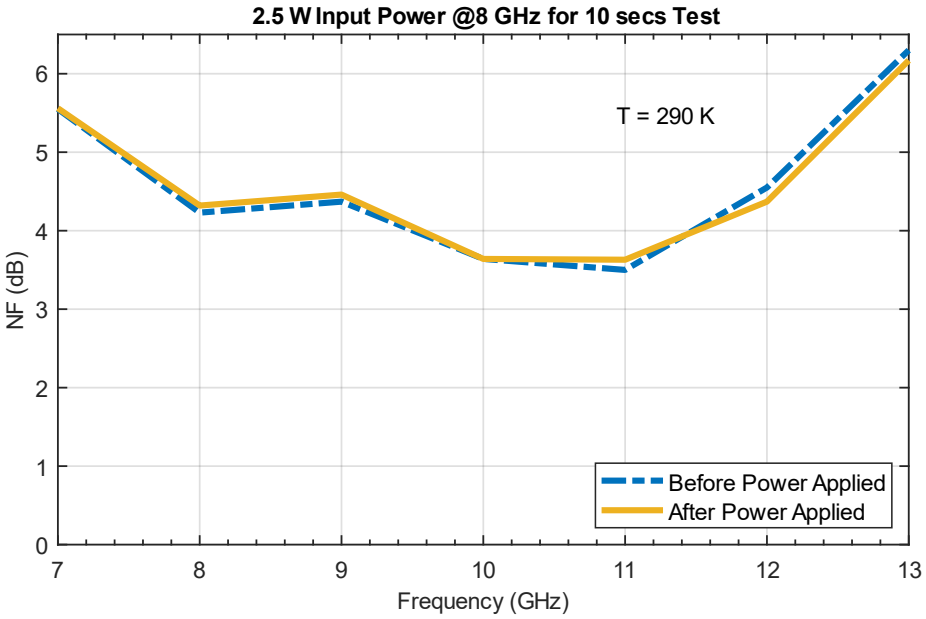


Figure 4.23 The noise figure results before and after input power applied at 8 GHz

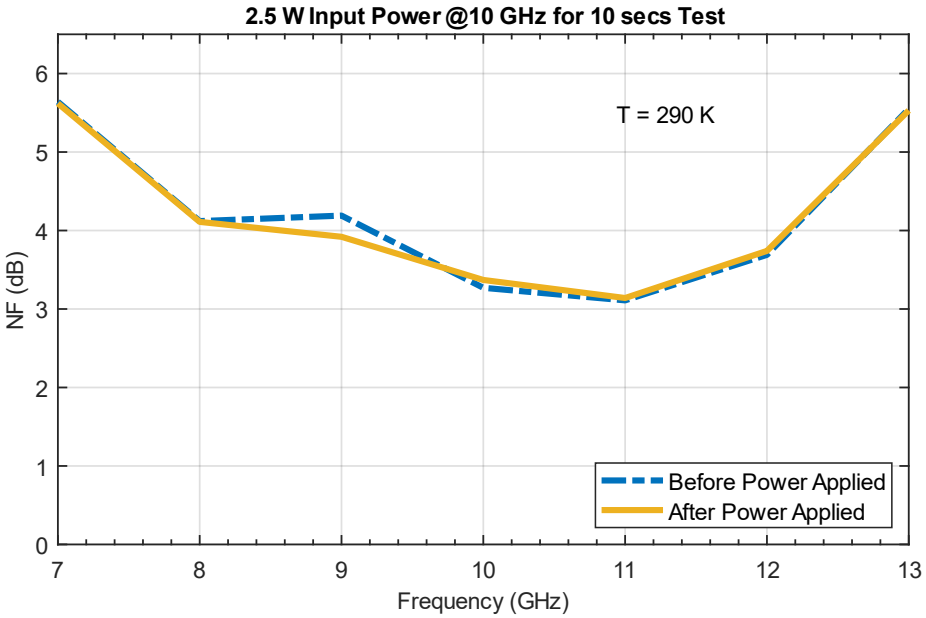


Figure 4.24 The noise figure results before and after input power applied at 10 GHz

As can be seen from Figure 4.23 and Figure 4.24, the noise figure change is negligible after 10 secs of input power stress tests. Therefore, it can be said that the LNAs can survive up to 2.5 W input power. It is, however, expected that the designed LNAs will survive input levels of more than 4 W since GaN LNAs with similar circuit topologies in the literature survives the input power of at least 4 W [21][22].

4.6 Back-fitting

The unavailability of the complete transistor models lead to the deviation of the measured results from the simulated ones, as can be seen in Section 4.2 and Section 4.3. One way to solve this problem is back-fitting. Since transistors of only one type are used in the LNA designs, a valid transistor model can be attempted to be created, by adding some elements to the periphery of the transistor model and trying to create similar simulated results to the measured ones.

The transistor models for the PDK used in the second tapeout are valid when the drain voltages are 10 V. However, when these drain voltages are applied, the measurement results do not match the simulation results for the LNA from tapeout 2 at all. A new transistor model is created for possible future tapeouts. The schematic of the created model is given in Figure 4.25.

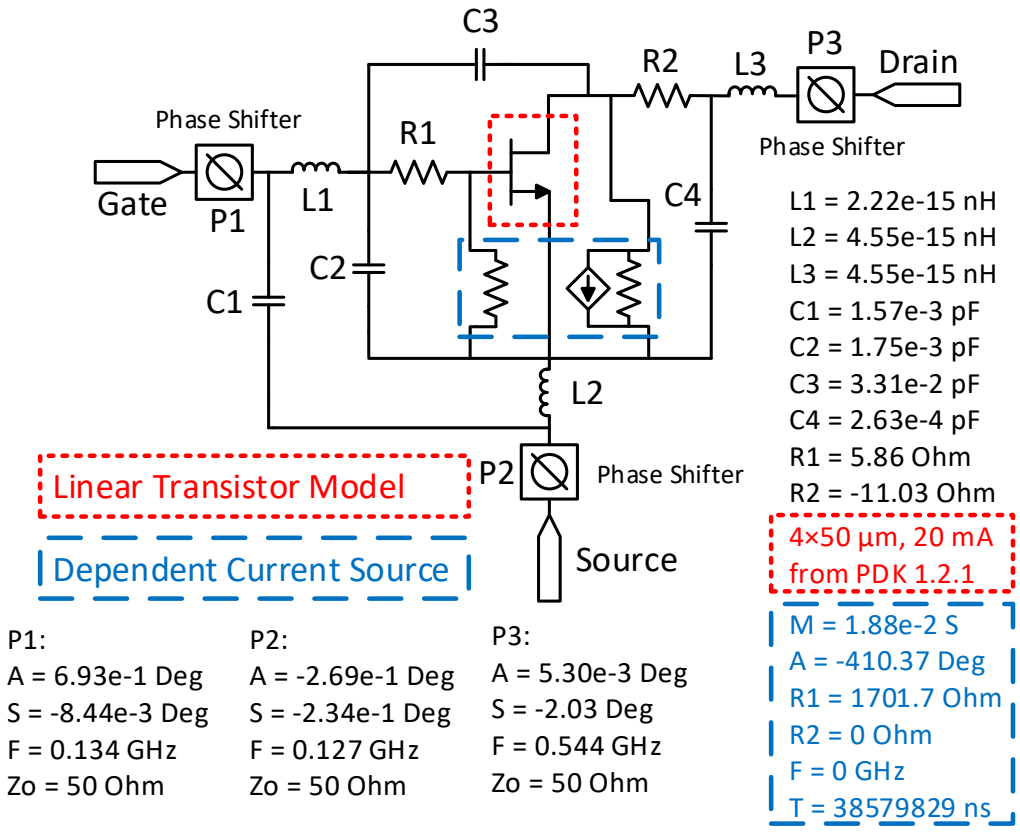


Figure 4.25 The schematic of the created linear model

The values of the peripheral elements are optimized using the tools in AWR MWO. The function used in the simulator is SModel, which is used to compute the weighted difference (error function) between two sets of S-parameters [51]. The equation (2.1) shows this error function.

$$Error = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\left|S_{ijA} - S_{ijB}\right|\right)^2}{N^2}, \tag{4.1}$$

where S_A and S_B are the two $N \times N$ S-parameter matrices.

The value of this error function is tried to be minimized by optimizing the element values. Since the magnitude of S_{21} is greater (has larger weight) than that of the other S-parameters over operating frequencies, in the optimization process the values of $|S_{21}|$ are intentionally reduced by adding identical ideal negative gain (dB) amplifiers at the output of the measured LNA and the optimized LNA, as can be seen in Figure 4.26.

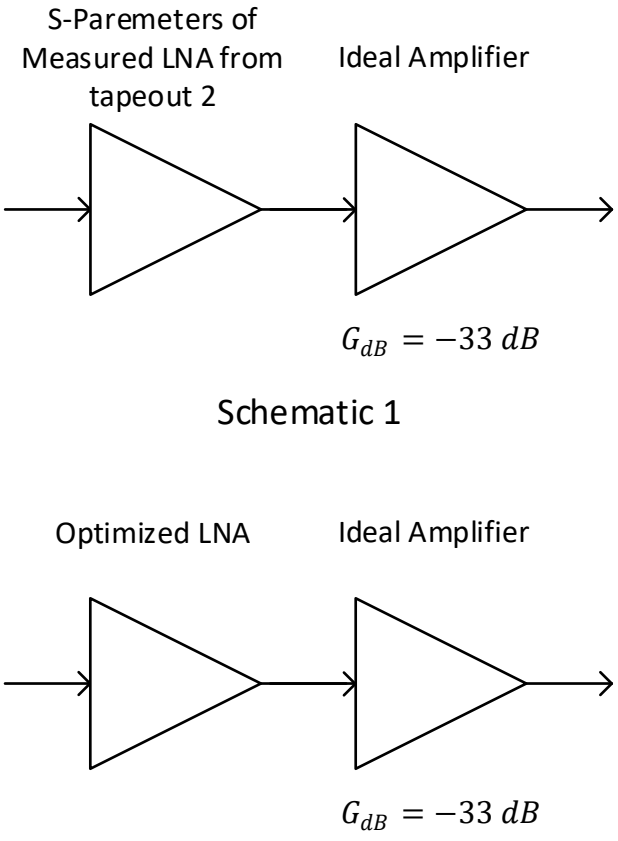


Figure 4.26 The circuits used for the creation of the optimized model

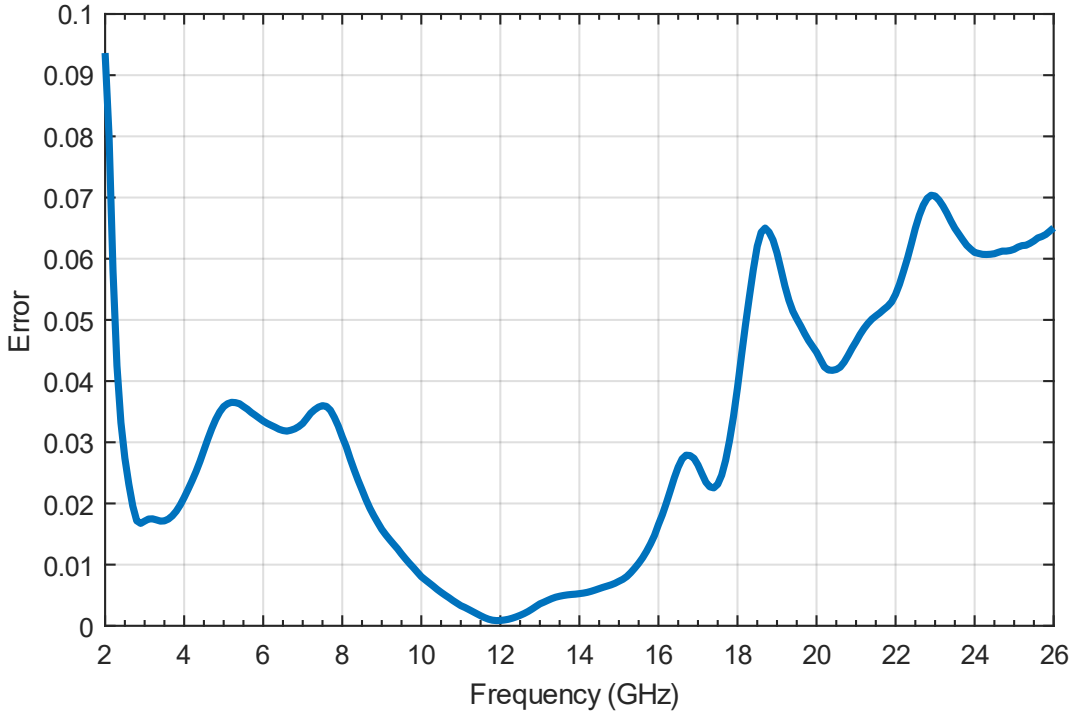


Figure 4.27 The error function simulation of the LNA with optimized model

They are intentionally not called "attenuators" since they only alter the gains (S_{21}), but not the return loss (S_{22} in this case). After optimization, error function results in Figure 4.27 are obtained.

The S-parameter comparisons between the measured results (for the LNA from the tapeout 2 with the drain voltages of 10 V) and the simulation of the LNA with optimized transistor models are shown in Figure 4.28, Figure 4.29, and Figure 4.30.

As can be seen from Figure 4.28, Figure 4.29, and Figure 4.30, the LNA with optimized transistor model yields simulations results which are very close to the actual measurement result especially over operating frequencies (8-12 GHz).

Unfortunately, this optimized transistor model lacks the proper noise data even if the noiseless resistors are used in the periphery. To (at least partially) overcome this, the created transistor model is converted into a touchstone file with noise data. Then, the noise data of this model are swapped with that of the PDK's transistor model. The comparison between the simulation and measurement results for the noise figure is given in Figure 4.31.

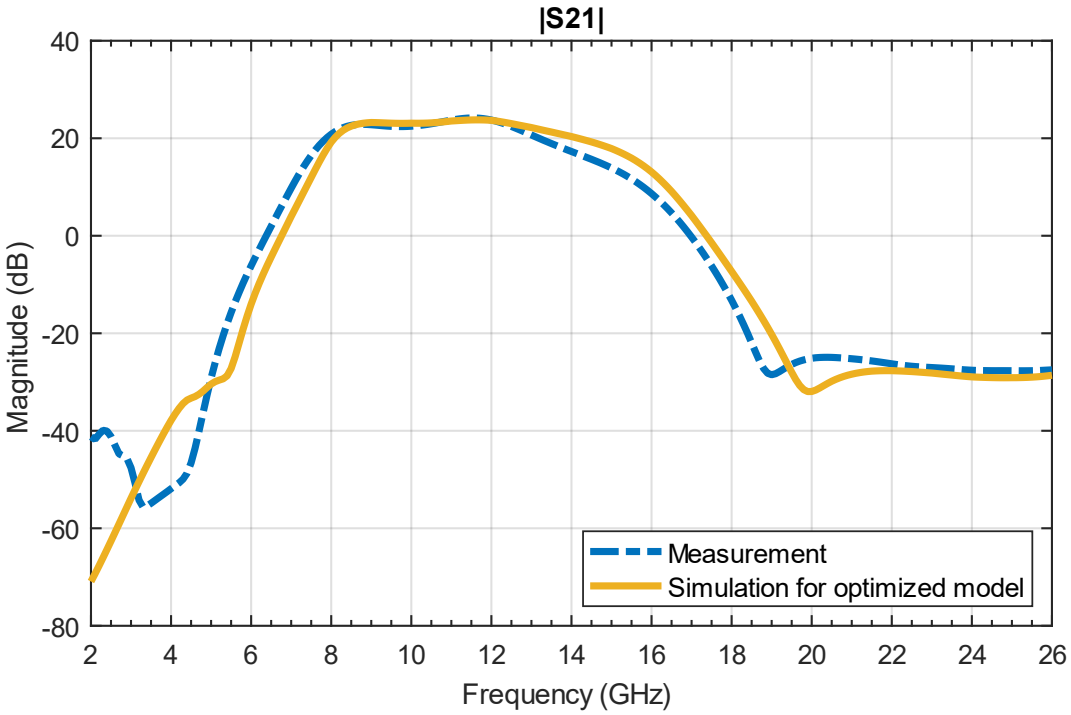


Figure 4.28 The comparison of the simulation and measurement results for the magnitude of S_{21}

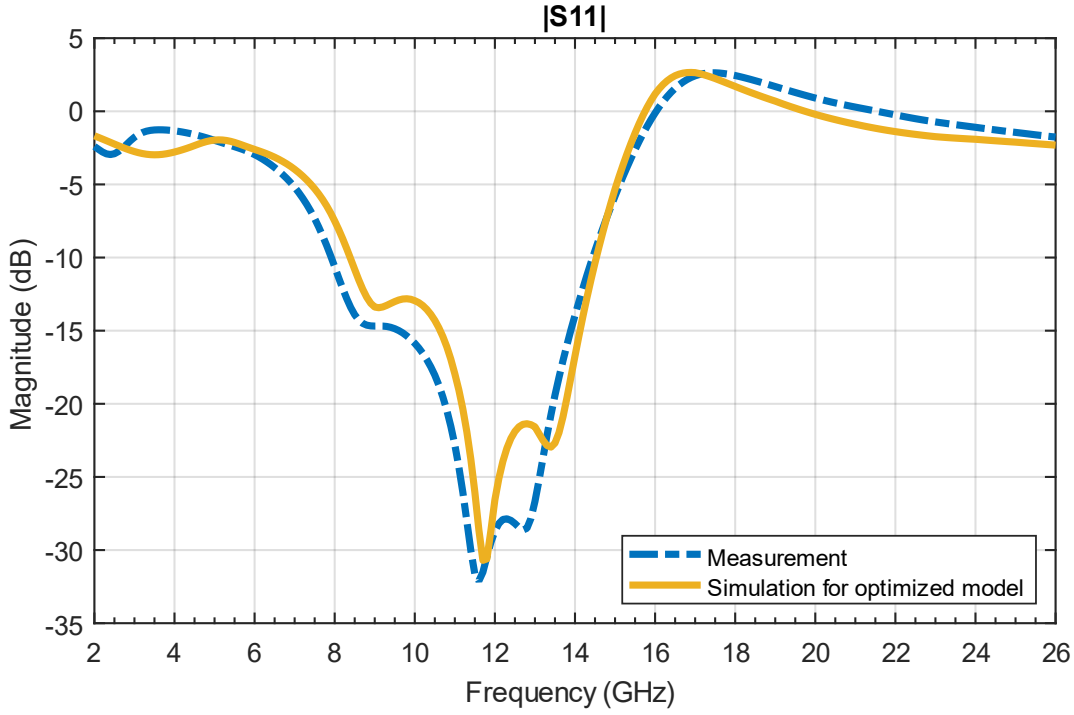


Figure 4.29 The comparison of the simulation and measurement results for the magnitude of S_{11}

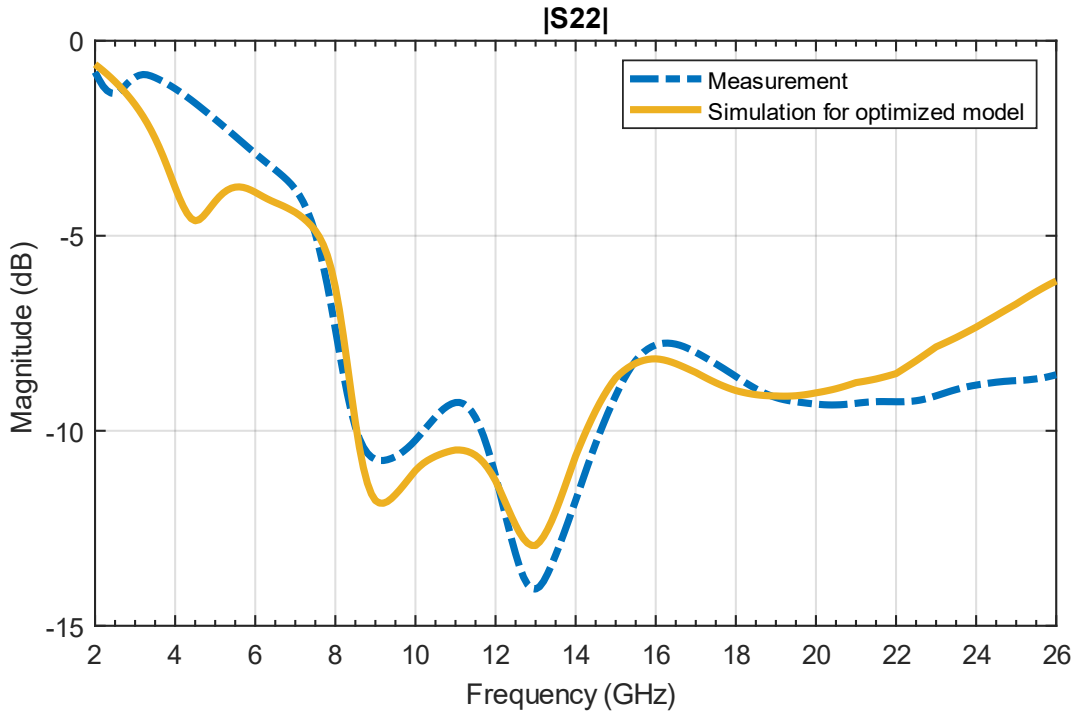


Figure 4.30 The comparison of the simulation and measurement results for the magnitude of S_{22}

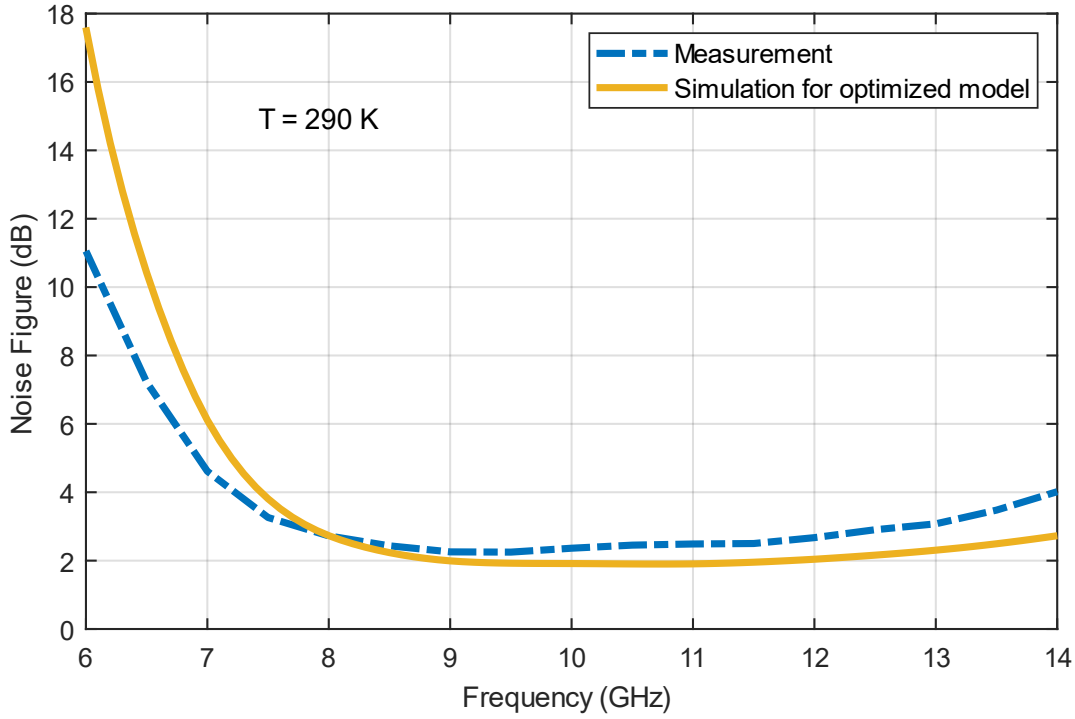


Figure 4.31 The comparison of the simulation and measurement results for the noise figure

4.7 Conclusion

Table 4.1 compares the performance of the LNA designs in the thesis with other LNAs recently reported in the literature. As can be seen from Table 4.1, the designed LNAs are superior to other LNAs recently reported in the literature at almost every aspect. The commercial product, TGA2612 by Qorvo, on the other hand, is better in many aspects except the power dissipation and return losses. The supply voltage of this product is also 10 V. Therefore, it has higher current dissipation, and possibly higher current density, meaning that each transistor of the stages might have higher gains. They might have added more lossy elements to stabilize circuit and to increase the bandwidth. In the work of this thesis, since the process is still under development and there is a lack of non-linear transistor models, it has been not possible to work with higher current densities. Even so, with this power dissipation, the LNAs in this thesis are successful and superior to the commercial product in other aspects like power dissipation and return losses. Moreover, it is not known whether 0.25 μm feature size technology used for the commercial product or not. Therefore, it not very easy to compare the product with the work in this thesis. When the process has complete transistor models, circuits with even better performances are considered to be designed with the design procedure presented in this thesis.

Table 4.1 Comparison with previously reported GaN LNAs

Reference	**Operating Frequency (GHz)**	**Noise Figure (dB)**	**Gain (dB)**	**Input Return Loss (dB)**	**Chip Size (mm^2)**	**OIP3 (dBm)**	**Output P1dB (dBm)**	**Power Dissipation (W)**
[17] 2007	4-16	1.45 min	11-14.5	10-14.5	-	24	-	-
[26] 2012	7-12	2.5	14	10	5	28	20	-
[7] 2013	8-12	<1.8	>14	-	6	-	-	0.21
[7] 2013	7-11	>2.0	>18	-	6	-	-	0.35
[27] 2016	8-10	1.3 max	24-27	2-20	4.5	33.8	-	0.9
[27] 2016	10-12	1.3-1.75	24.4-25.2	>10	4.5	32.8	-	0.9
[52] TGA2612 Qorvo	6-12	1.5-1.8	22-28	>7	3.15	29	20	1.0
Tapeout-1 LNA	8-11	1.60-1.95	22.0-30.8	9.1-20.6	3.6	29	23	0.6
Tapeout-2 LNA	8-12	2.22-2.58	20.4-25.0	11.5-25.7	3.6	28.6	17.8	0.36

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this thesis, two LNA MMICs are designed and evaluated. The circuits are realized using the 0.25 μm Power GaN/SiC HEMT process by WIN Semiconductor, whose fabs are located in Taiwan. The LNAs are designed and simulated using AWR MWO, and the electromagnetic simulations are performed using AXIEM in AWR MWO.

The circuits are composed of three cascaded common-source stages. When designing the circuits, firstly, the stages are conjugately matched to the characteristic impedance of the system. After that, the stages are combined and optimized for the design goals. It should be added that when designing the circuits, S-probe stability analysis has enabled the design of compact circuit layouts.

The measurements are performed mostly using calibrated probe station. After the evaluations, it is concluded that the designed LNAs are superior in many aspects to the GaN LNAs recently reported in the literature as demonstrated in Section 4.7. The first LNA achieves the targeted noise figure of less than 2 dB. Its input return loss has a very good performance between 8 and 11 GHz. However, in this tapeout, the simulation and the measurement results are not consistent. The reason is that the transistor models used in the first tapeout are not valid. The second LNA is designed to have better input return loss performance. This time, however, the circuit does not meet the noise figure goal since some tools in the fabrication process are replaced, invalidating the transistor models used in the design. Despite this, the second LNA also has good noise figure performance of less than 2.5 dB. Also, both designs have

gains of more than 20 dB over the targeted X-band. Moreover, LNAs are tested up to 2.5 W input power, and no degradation in the noise performance has been observed.

To solve the problem of transistor models, new transistor models are developed using the method of back-fitting. Using these models, LNA designs can be modified and improved. Also, since the need for an input limiter is eliminated, a fully integrated GaN RF transceiver frontend operating at the X-band can be designed as a future work. The simple schematic for such a transceiver is re-demonstrated in Figure 5.1.

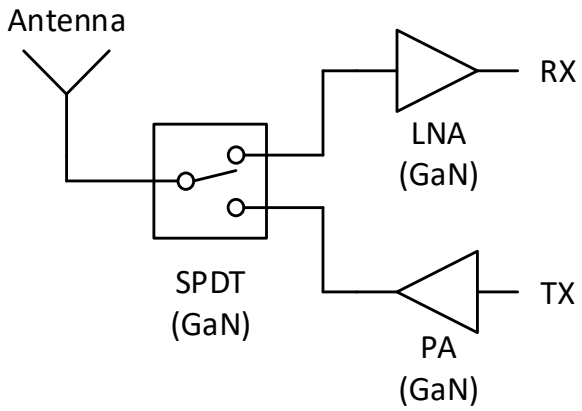


Figure 5.1 A simple schematic showing a GaN RF transceiver module

REFERENCES

[1] "Low-Cost Front End Receives 9 GHz," *Microwaves & Radio Frequency*, 13-Mar-2014. [Online]. Available: http://www.mwrf.com/mixed-signal-semiconductors/low-cost-front-end-receives-9-ghz. [Accessed: 29-Jun-2018].

[2] S. Bhaumik and D. Kettle, "Broadband X-band low noise amplifier based on 70 nm GaAs metamorphic high electron mobility transistor technology for deep space and satellite communication networks and oscillation issues," *Antennas Propagation IET Microwaves*, vol. 4, no. 9, pp. 1208–1215, Sep. 2010.

[3] "HMC-ALH444-DIE Datasheet and Product Info | Analog Devices." [Online]. Available: http://www.analog.com/en/products/amplifiers/rf-amplifiers/low-noise-amplifiers/hmc-alh444-die.html#product-overview. [Accessed: 30-Jun-2018].

[4] "HMC772 Datasheet and Product Info | Analog Devices." [Online]. Available: http://www.analog.com/en/products/amplifiers/rf-amplifiers/low-noise-amplifiers/hmc772.html#product-overview. [Accessed: 30-Jun-2018].

[5] "QPA2609 - Qorvo." [Online]. Available: https://www.qorvo.com/products/p/QPA2609. [Accessed: 30-Jun-2018].

[6] M. S. Heins, J. M. Carroll, M. Kao, J. Delaney, and C. F. Campbell, "X-band GaAs mHEMT LNAs with 0.5 dB noise figure," in *2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535)*, 2004, vol. 1, pp. 149-152 Vol.1.

[7] P. Schuh and R. Reber, "Robust X-band low noise limiting amplifiers," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013, pp. 1–4.

[8] P. Schuh *et al.*, "T/R-module technologies today and possible evolutions," in *2009 International Radar Conference "Surveillance for a Safer World" (RADAR 2009)*, 2009, pp. 1–5.

[9] "Low Noise GaN Amplifiers with Inherent Overdrive Protection | 2015-12-16 | Microwave Journal." [Online]. Available: http://www.microwavejournal.com/articles/25638-low-noise-gan-amplifiers-with-inherent-overdrive-protection. [Accessed: 29-Jun-2018].

[10] P. Parikh *et al.*, "High linearity, robust, AlGaN-GaN HEMTs for LNA and receiver ICs," in *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 2002, pp. 415–421.

[11] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-Based RF Power Devices and Amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[12] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, "GaN-Based Robust Low-Noise Amplifiers," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013.

[13] "HFIC_chapter_7_low-noise_amplifier_design.pdf." [Online]. Available: http://www.cambridge.org/us/files/8113/6698/2364/HFIC_chapter_7_low-noise_amplifier_design.pdf. [Accessed: 01-Jul-2018].

[14] "lect14.pdf." [Online]. Available: http://rfic.eecs.berkeley.edu/~niknejad/ee142_fa05lects/pdf/lect14.pdf. [Accessed: 01-Jul-2018].

[15] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2003.

[16] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2000.

[17] M. Micovic *et al.*, "Robust Broadband (4 GHz - 16 GHz) GaN MMIC LNA," in *2007 IEEE Compound Semiconductor Integrated Circuits Symposium*, 2007, pp. 1–4.

[18] I. Khalil, A. Liero, M. Rudolph, R. Lossy, and W. Heinrich, "GaN HEMT Potential for Low-Noise Highly Linear RF Applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 9, pp. 605–607, Sep. 2008.

[19] S. Piotrowicz *et al.*, "Broadband AlGaN/GaN high power amplifiers, robust LNAs, and power switches in L-band," in *2009 European Microwave Conference (EuMC)*, 2009, pp. 1784–1787.

[20] C. Andrei, A. Liero, R. Lossy, W. Heinrich, and M. Rudolph, "Highly linear broadband GaN-based low-noise amplifier," in *German Microwave Conference Digest of Papers*, 2010, pp. 36–38.

[21] P. Chehrenegar, M. Abbasi, J. Grahn, and K. Andersson, "Highly linear 1-3 GHz GaN HEMT low-noise amplifier," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, 2012, pp. 1–3.

[22] H. L. Kao *et al.*, "Design of an S-band 0.35 μm AlGaN/GaN LNA using cascode topology," in *2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, 2013, pp. 250–253.

[23] H. Xu, C. Sanabria, A. Chini, S. Keller, U. K. Mishra, and R. A. York, "A C-band high-dynamic range GaN HEMT low-noise amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 6, pp. 262–264, Jun. 2004.

[24] D. Resca *et al.*, "A robust Ku-band low noise amplifier using an industrial 0.25-μm AlGaN/GaN on SiC process," in *2013 European Microwave Conference*, 2013, pp. 1467–1470.

[25] M. Micovic *et al.*, “Ka-Band LNA MMIC’s Realized in Fmax > 580 GHz GaN HEMT Technology,” in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2016, pp. 1–4.

[26] C. Andrei, R. Doerner, O. Bengtsson, S. A. Chevtchenko, W. Heinrich, and M. Rudolph, “Highly linear X-band GaN-based low-noise amplifier,” in *2012 International Symposium on Signals, Systems, and Electronics (ISSSE)*, 2012, pp. 1–4.

[27] M. Vittori, S. Colangeli, W. Ciccognani, A. Salvucci, G. Polli, and E. Limiti, “High performance X-band LNAs using a 0.25 μm GaN technology,” in *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2017, pp. 157–160.

[28] “TGM2543-SM - Qorvo.” [Online]. Available: https://www.qorvo.com/products/p/TGM2543-SM#documents. [Accessed: 01-Jul-2018].

[29] J. B. Johnson, “Thermal Agitation of Electricity in Conductors,” *Phys. Rev.*, vol. 32, no. 1, pp. 97–109, Jul. 1928.

[30] H. Nyquist, “Thermal Agitation of Electric Charge in Conductors,” *Phys. Rev.*, vol. 32, no. 1, pp. 110–113, Jul. 1928.

[31] B. Razavi, *RF Microelectronics*. Prentice Hall, 2012.

[32] H. Birk, M. J. M. de Jong, and C. Schönenberger, “Shot-Noise Suppression in the Single-Electron Tunneling Regime,” *Phys. Rev. Lett.*, vol. 75, no. 8, pp. 1610–1613, Aug. 1995.

[33] “Microsoft PowerPoint - Noise in Electronics.ppt.” [Online]. Available: http://www.fen.bilkent.edu.tr/~aykutlu/msn/hw/HO2_NoiseinElectronics.pdf. [Accessed: 09-Jun-2018].

[34] P. Horowitz and W. Hill, *The Art of Electronics*. Cambridge University Press, 2015.

[35] “ShotNoise.dvi.” [Online]. Available: http://123.physics.ucdavis.edu/shot_files/ShotNoise.pdf. [Accessed: 09-Jun-2018].

[36] “Noise Sources in Bulk CMOS.” [Online]. Available: http://web.mit.edu/klund/www/papers/UNP_noise.pdf. [Accessed: 09-Jun-2018].

[37] A. L. McWhorter, “1/f noise and related surface effects in germanium.,” Thesis (Sc. D.), Massachusetts Institute of Technology, 1955.

[38] F. N. Hooge, “$1/f$; noise is no surface effect,” *Physics Letters A*, vol. 29, no. 3, p. 139, Apr. 1969.

[39] Y. Tsividis and C. McAndrew, *Operation and modeling of the MOS transistor*, 3rd ed. New York, NY: Oxford Univ. Press, 2011.

[40] “eecs242_lect8_twoportnoise.pdf.” [Online]. Available: http://rfic.eecs.berkeley.edu/~niknejad/ee242/pdf/eecs242_lect8_twoportnoise.pdf. [Accessed: 21-Jul-2018].

[41] K. Sengupta and A. Hajimiri, “A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[42] Z. Hu and R. Han, “Fully-scalable 2D THz radiating array: A 42-element source in 130-nm SiGe with 80-µW total radiated power at 1.01 THz,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 372–375.

[43] E. Lindberg, “The Barkhausen Criterion (Observation ?),” *Proceedings of Ndes 2010*, pp. 15–18, 2010.

[44] M. L. Edwards and J. H. Sinsky, “A new criterion for linear 2-port stability using a single geometrically derived parameter,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 12, pp. 2303–2311, Dec. 1992.

[45] R. Gilmore and L. Besser, *Practical RF Circuit Design for Modern Wireless Systems: Active Circuits and Systems, Volume 2*. Artech House, 2003.

[46] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Prentice Hall, 1997.

[47] B. Kim and W. Gao, “X-Band Robust Current-Shared GaN Low Noise Amplifier for Receiver Applications,” in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2016, pp. 1–4.

[48] “AXIEM - 3D Planar Electromagnetic (EM) Analysis. | NI AWR Design Environment.” [Online]. Available: http://www.awrcorp.com/products/ni-awr-design-environment/axiem. [Accessed: 19-Jun-2018].

[49] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House, 2006.

[50] K. Wang, M. Jones, and S. Nelson, “The S-probe-a new, cost-effective, 4-gamma method for evaluating multi-stage amplifier stability,” in *1992 IEEE MTT-S Microwave Symposium Digest*, 1992, pp. 829–832 vol.2.

[51] “Microwave Office Measurement Catalog: Error Between S-parameters: SModel.” [Online]. Available: https://awrcorp.com/download/faq/english/docs/Measurements/smodel.htm. [Accessed: 10-Jun-2018].

[52] “TGA2612 - Qorvo.” [Online]. Available: https://www.qorvo.com/products/p/TGA2612. [Accessed: 19-Jun-2018].