# DESIGN AND IMPLEMENTION OF A THREE PHASE GRID CONNECTED SIC SOLAR INVERTER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MEHMET CANVER

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2018

Approval of the thesis:

**DESIGN AND IMPLEMENTATION OF A THREE PHASE GRID CONNECTED SIC SOLAR INVERTER**

submitted by **MEHMET CANVER** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Tolga Çiloğlu
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Muammer Ermiş
Supervisor, **Electrical and Electronics Engineering Dept., METU** _____

**Examining Committee Members:**

Assist. Prof. Dr. Ozan Keysan
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Muammer Ermiş
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Işık Çadırcı
Electrical and Electronics Engineering Dept., Hacettepe University _____

Assist. Prof. Dr. Murat Göl
Electrical and Electronics Engineering Dept., METU _____

Assist. Prof. Dr. Emine Bostancı
Electrical and Electronics Engineering Dept., METU _____

**Date:** 06.09.2018

**I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.**

Name, Last Name : Mehmet Canver

Signature :

## ABSTRACT

### DESIGN AND IMPLEMENTION OF A THREE PHASE GRID CONNECTED SIC SOLAR INVERTER

Canver, Mehmet

M.S., Department of Electrical and Electronics Engineering

Supervisor: Prof. Dr. Muammer Ermiş

September 2018, 111 pages

In this research work a 30 kW grid connected voltage source three-phase inverter with SiC MOSFET module has been designed and implemented, in order to work with a phase-shifted full bridge (PSFB) maximum power point tracker (MPPT) converter, in such a way that these two converters compose a full system solution. The emergence of commercial SiC based power MOSFETs, which have short turn-on and turn-off times, has enabled to increase switching frequency as compared to traditional Si based switching components. This circumstance was one the main motives of this thesis in the scopes of increasing the switching frequency, in order to reduce passive component volumes of inverter such as LCL filter and DC link capacitor volume, decreasing losses which leads to reduce the heat sink volume and having better efficiency. Designed and implemented inverter had been operated in the field with PSFB MPPT converter, energized by 23.75 kW total installed capacity solar arrays. Output characteristics had been investigated, and in the grid connected close loop mode various powers up to 22.32 kW had been transferred into grid. Inverter switching characteristics, drain-source voltage, unfiltered line current and zero voltage switching phenomenon were examined with the change of dead time

and output line current. Total harmonic distortion had been recorded at various output powers, and a minimum THD value of 3.84% had been obtained at maximum output power of 22.32 kW. Experimental efficiency values was calculated from various recorded input and output powers. 98.55% peak efficiency at half of rated output power and 98% efficiency at peak output power had been obtained.

Keywords: Three-Phase Grid Connected Inverter, Silicon Carbide, Voltage Source Inverter (VSI), Photovoltaic.

# ÖZ

## ÜÇ FAZ ŞEBEKE BAĞLANTILI SiC GÜNEŞ EVİRİCİSİ TASARIMI VE UYGULAMASI

Canver, Mehmet
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Prof. Dr. Muammer Ermiş

Eylül 2018, 111 sayfa

Bu tez çalışmasında 30 kW anma gücüne sahip üç-faz şebeke bağlantılı Gerilim Kaynaklı Evirici (GKE), SiC MOSFET modülü kullanılarak, bir faz-kaydırmalı tam köprü (FKTK) maksimum güç noktası izleyici (MGNİ) dönüştürücü ile birlikte çalışıp, tam bir sistem çözümü oluşturacak şekilde tasarlanmış ve uygulanmıştır. Kısa açılma ve kapanma süresine sahip ticari SiC tabanlı güç MOSFET'lerinin ortaya çıkması ile birlikte geleneksel Si tabanlı anahtarlama elamanlarına göre anahtarlama frekanslarının artması mümkün hale gelmiştir. Bu durum, anahtarlama frekansının arttırılarak LCL filtre, DA bağ kondansatör hacmi, kayıpların azalmasına bağlı olarak soğutucu hacminin küçültülmesi ve daha iyi verim elde edilmesi bakımından bu tezin ana amaçlarından birisidir. Tasarlanan ve uygulanan üç-faz evirici sahada bir FKTK MGNİ dönüştürücü ile birlikte 23.75 kW toplam kurulu güce sahip güneş dizileri ile enerjilendirilerek çalıştırılmıştır. Üç-faz evirici çıkış karakteristiği incelenmiş olup şebeke bağlantılı kapalı döngü modunda 22.32 kW gücüne kadar çeşitli güçler şebekeye aktarılmıştır. Evirici anahtarlama karakteristiği, "drain-source" gerilimi, filtrelenmemiş hat akımı ve sıfır gerilim anahtarlama olgusu, ölü zaman süresinin ve çıkış hat akımının değişimi ile birlikte incelenmiştir. Üç-faz evirici toplam harmonik bozulumu (THB) çeşitli çıkış güç

değerleri için kaydedilmiş ve en yüksek 22.32 kW çıkış gücünde, minimum THB değeri 3.84% olarak elde edilmiştir. Deneysel verim değerleri çeşitli giriş ve çıkış güç değerleri üzerinden hesaplanmıştır. Çıkış anma güç değerinin yarısında, 98.55% tepe verim değeri ve tepe çıkış güç değerinde 98% verim değeri elde edilmiştir.

Anahtar Kelimeler: Üç-Faz Şebeke Bağlantılı Evirici, Silisyum Karbür, Gerilim Kaynaklı Evirici (GKE), Fotovoltaik.

To my wife

To my family

## ACKNOWLEDGMENTS

I would like to express my deepest gratitude to my supervisor Prof. Dr. Muammer Ermiş not only for his guidance, criticism, encouragements and insight throughout this research but also for his continuous confidence in me.

I would like to show my gratitude to Prof. Dr. Işık Çadırcı and Assist. Prof. Dr. Ozan Keysan for their guidance, criticism, encouragements and insight throughout this research.

I would like to thank ARTI INDUSTRIAL ELECTRONICS Inc. and TÜBITAK Marmara Research Center Ankara Branch for its valuable support throughout my graduate studies. Outstanding laboratory equipment and component resources have benefited my work greatly.

I would also like to thank my technical director M. Volkan Utalay and my colleague in METU İlker Şahin and my friends Serkan Öztürk and Ö. Şahin Alemdar for their enduring support and encouragement.

I express my deepest gratitude to my family Mevlüt, Müjgan and Mert Canver for their patience and support throughout my life.

And lastly I would like to thank to my wife Burcu Yüksek Canver for her never ending support, help and patience through the time of work and my entire life. No word can express my gratitude.

## TABLE OF CONTENTS

## LIST OF TABLES

TABLES

## LIST OF FIGURES

FIGURES

## LIST OF SYMBOLS

| | |
|---|---|
| $\theta_s$ | dq-frame reference angle. |
| $\eta$ | efficiency |
| $\omega$ | dq-frame angular speed |
| d | subscript indicating d-axis component |
| q | subscript indicating q-axis component |
| $C_{dc}$ | capacitance of the DC-link capacitor |
| $C_f$ | capacitance of the output filter capacitor |
| $C_{oss}$ | output capacitance of the MOSFET |
| $f_{sw}$ | switching frequency of the semiconductors |
| $I_{a,b,c}$ | output phase a, b, c currents |
| $I_{dc}$ | mean DC-link current |
| $I_d$ | d-axis component output current |
| $I_d^*$ | reference d-axis component output current |
| $I_q$ | q-axis component output current |
| $I_q^*$ | reference q-axis component output current |
| $L_c$ | converter side filter inductance |
| $L_g$ | grid side filter inductance |
| m | modulation index |
| $P_{in}$ | input power of the inverter |
| $P_{loss}$ | inverter losses |
| $P_{out}$ | output power of the inverter |
| $R_d$ | damping resistance |
| $R_g$ | external gate drive resistance |
| $T_c$ | case temperature |

| | |
|---|---|
| $T_j$ | junction temperature |
| $V_{GS}$ | gate-source voltage of MOSFET |
| $V_{dc}$ | DC-side voltage of the VSI |

## LIST OF ABBREVIATIONS

| | |
|---|---|
| AC | Alternating Current |
| CSI | Current Source Inverter |
| DC | Direct Current |
| ESL | Equivalent Series Resistance |
| ESR | Equivalent Series Inductance |
| DSP | Digital Signal Processor |
| GaN | Gallium Nitride |
| IGBT | Insulated-Gate Bipolar Transistor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MPP | Maximum Power Point |
| MPPT | Maximum Power Point Tracking |
| PCB | Printed Circuit Board |
| PFSB | Phase-Shifted Full Bridge |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| PLL | Phase Locked Loop |
| Si | Silicon |
| SiC | Silicon Carbide |
| SPWM | Sinusoidal PWM |
| SVPWM | Space Vector PWM |
| TDD | Total Demand Distortion |
| THD | Total Harmonic Distortion |
| ZVS | Zero Voltage Switching |
| VSI | Voltage Source Inverter |

# CHAPTER 1

# INTRODUCTION

## 1.1. Background and Motivation

Beginning with 1970s researches about utilization from solar energy started to increase so that technological advances in solar panel and power semiconductors technology leaded a significant decrease in the cost of solar power plants. Also inevitable depletion of fossil fuels and increases in prices due to lack of increase in supply proportional to demand to fossil fuels, caused establishing of solar power plant feasible. So that with the incremental increase in established solar power plants, total solar PV global capacity has reached to 303 gigawatts by the end of 2016 as can be seen in Fig. 1-1.

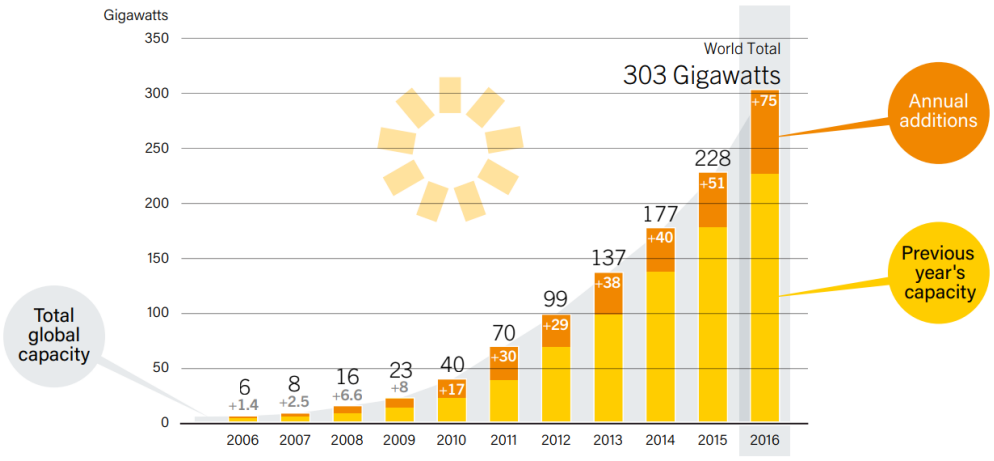



Figure 1-1: Global Solar PV Capacity and Annual Additions, 2006-2016 [1]

The decrease in PV module prices per watt can be seen in Fig. 1-2. According to that factory gate module prices dropped to $0.35/W in March 2017. Such reduction in the costs of PV module is expected to continue so that more solar power plants are foreseen to be established in near future.

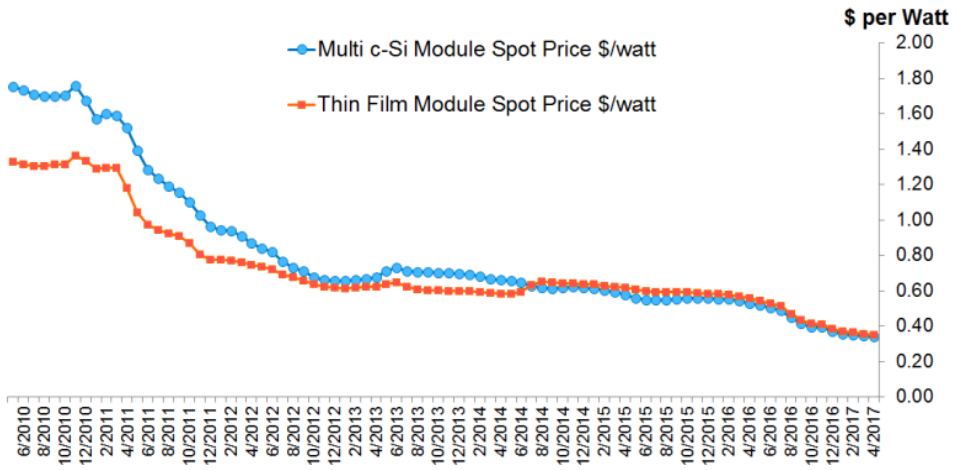



Figure 1-2: Ex-factory price for U.S crystalline-silicon and thin-film PV modules [2]

PV inverters is one of the key components in a PV power plant. PV inverter is responsible for transferring PV energy to grid in a highly efficient and robust way, grid synchronization, anti-islanding, voltage and current protections to protect PV installation, maximum power extraction from PV modules and etc. Among the various types of the PV system configuration concepts, multi-string inverter is relatively a new configuration which contains more than one DC-DC converters for PV strings so that eliminating negative effects of partial shading and one inverter to transfer PV energy to grid which makes it a hybrid solution for intermediate power level between residential and utility scale PV plants by containing advantageous parts of string inverter and central inverter.

By utilizing new generation power semiconductors, inverter efficiencies have reached very high efficiencies up to 98.2% for ABB TRIO-27.6-TL transformerless multistring inverter with new generation IGBT power semiconductors [3]. In addition to existing power semiconductor technology, SiC based power MOSFETs have been commercialized in recent years. Lower $t_{on}$ and $t_{off}$ time of SiC MOSFETs

lead lower switching loss so that higher efficiency up to 99.5% [4] and reduction of heatsink volumes, also enables utilization higher switching frequency so that reduction passive component size. Based on these features, SiC power MOSFETs can dominate the power semiconductor market with the price reduction in next years.

### 1.2. Objectives of the Thesis

The main objective of this thesis is to design and implement a three-phase grid connected 30 kVA voltage source inverter (VSI) by using SiC based MOSFETs in the power stage and examine the outputs. In order to find maximum power point and prevent common mode currents a maximum power point tracking (MPPT) converter designed and implemented by Hacettepe University with SiC power semiconductors, and this converter has been added between three-phase two-level voltage source inverter and PV strings. All SiC three-phase grid-connected PV supply experimental set-up configuration can be seen in Fig. 1-3.

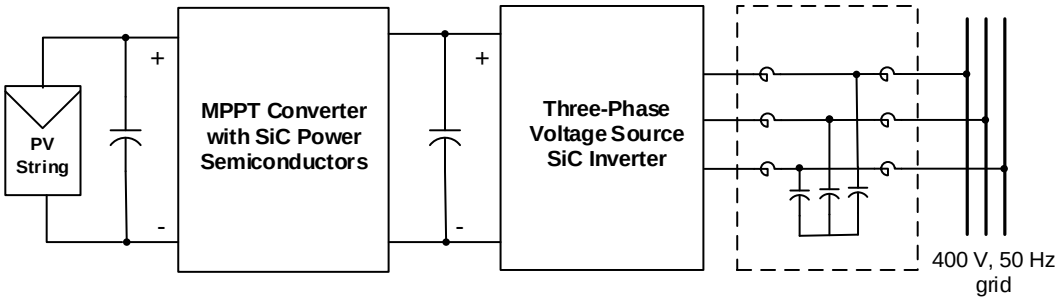



Figure 1-3: All SiC three-phase grid-connected PV supply string inverter system configuration [5]

Designed inverter can be also used in multistring applications as can be seen in Fig. 1-4. With the emergency of higher rating SiC power MOSFETs, power rating of three-phase, two-level voltage source inverter can reach 175-400 kVA for transformerless connection to 400 V l-to-l, 50 Hz utility grid. For this high power

rating inverters which will be used in multistring applications, multi MPPT converters with DC/AC/DC link can be used to process 15-25 kW PV power. The inverter rating in the application described in this thesis is limited to 25 kVA due to the 23.75 kW peak capacity solar modules installation.

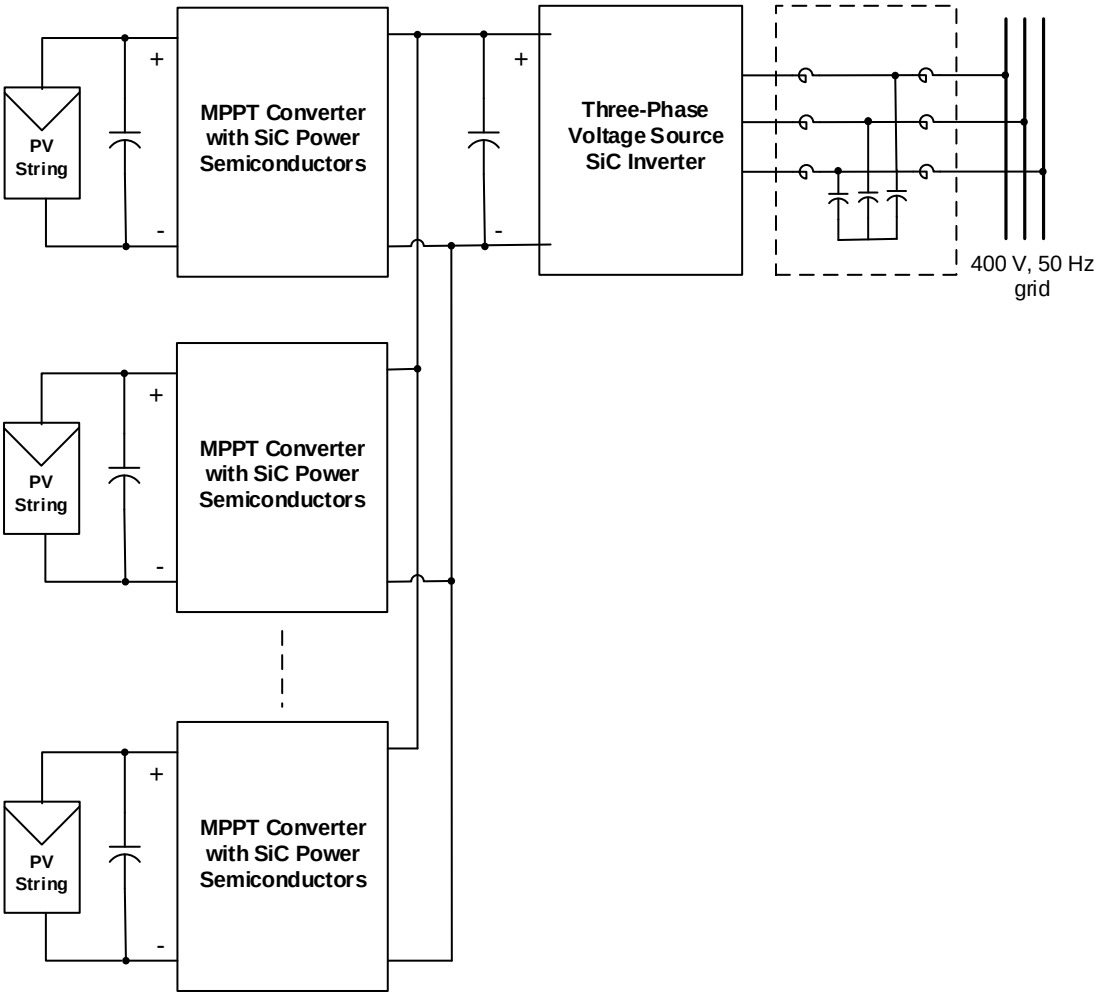



Figure 1-4: All SiC three-phase grid-connected PV supply, multi-string PV inverter system configuration [5]

The implemented VSI inverter has been investigated via performance criteria such as overall efficiency, peak efficiency, total harmonic distortion (THD), power factor, step response reaction, switching performance and etc.

### 1.3. Thesis Outline

The main purpose of this thesis is to design and implement a 30 kVA rated output power three-phase grid connected voltage source inverter using SiC based MOSFET switches and verify the design through field tests. The performance criteria for three-phase inverter consist of efficiency, robustness, total harmonic distortion and some other specifications which will be shown. The outline of this thesis is represented as follows:

In Chapter 2, an overview of photovoltaic systems and photovoltaic three phase inverters are explained briefly. Basic elements of PV system, PV system configuration types, current situation of photovoltaic technology, PV inverter types for each type of PV configuration, advantages and specifications of SiC MOSFETs are given in this chapter.

In Chapter 3, operating principles, analysis and control of grid connected three-phase inverters are explained. Control techniques, PWM methods used in three-phase voltage sources inverters are explained and compared. State of the art of three-phase grid connected voltage source inverters is presented in this section.

In Chapter 4, step by step design procedure of a grid connected three-phase inverter is presented. In this section optimum switching frequency, DC link voltage and capacitance selection, output LCL filter design, control loop implementation, loss and efficiency calculations are stated.

In Chapter 5, field test results of three-phase inverter are given and examined in depth with the use of recorded data, tables and figures. In this chapter switching characteristics of inverter, ZVS conditions depending on output current and dead time, current and voltage waveforms of inverter at grid connection for various output powers, total harmonic distortion, efficiency plot, and step response characteristics are presented and explained.

In Chapter 6, general conclusions about three-phase inverter design, implementation and test results are presented. Also some suggestions for future work in order to enhance system performance are given.

# CHAPTER 2

# OVERVIEW OF PHOTOVOLTAIC SYSTEMS AND THREE PHASE INVERTERS

## 2.1. Photovoltaic System

Photovoltaic system consists of some various components such as photovoltaic modules, junction box, solar inverters, mounting, cabling and in some installations battery system, battery charger, solar tracker, maximum power point tracker (MPPT), transformer station and so on.

Photovoltaic modules are used in order to transform solar power to electricity, and the serial connections of modules constitutes a PV string. Most of modules consist of generally 60-72 cells and generate a DC voltage of 30-40 V with a power range of 160-300W. With the serial connection of PV modules, PV string generate a DC voltage between 400 V to 950V in most applications. A number of PV strings are paralleled depending to the inverter power rating. Those PV string cables goes to a combining box named as junction box which includes connection cables of PV strings, fuses for each string, DC disconnector, surge arrestor for lightning protection. PV inverter is responsible for transferring the combined power of PV strings into grid in an efficient, robust way. There are some regulations indicated in international standards for PV inverters which will be explained in this thesis. Also in some installations especially where solar power station is not connected to grid infrastructure, battery system and battery chargers are used in order to maintain providing electricity to loads. In addition, those power stations with battery system can be used to support active power to grid in cloudy weather and at the night hours when the interconnected system is in need of active power.

Photovoltaic energy has a wide range of applications starting from a few hundreds of watts for a small system to more than a gigawatt (Tengger Desert Solar Park China, 1.547 megawatts installed capacity) for large utility scale PV plants. Because of this wide power range different PV system configurations is used for different power levels of PV installations. Each PV configuration concept has its own advantageous and disadvantageous features which will be discussed in this thesis.

## 2.2. Photovoltaic Module Characteristics

Photovoltaic panel characteristics change with conditions such as solar irradiance and ambient temperature. An electrical circuit of multi-string PV system based on static model is given in Fig. 2-1. Multi-string PV system is composed of individual PV modules so that it can be observed as electrical circuit of a PV module.

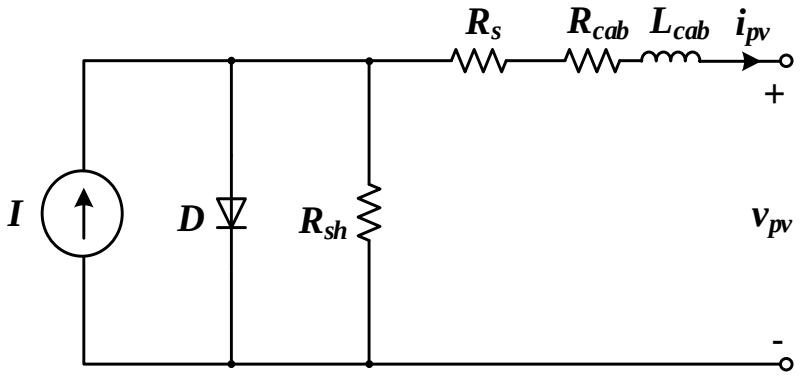



Figure 2-1: Equivalent circuit of multi-string PV system for static model

As can be seen in Fig. 2-1 PV module is represented as a photo-current source where $R_s$ and $R_{sh}$ are equivalent series and shunt resistance of PV string. Also due to cabling $R_{cab}$ and $L_{cab}$ serial resistance and inductance values are added to static model. Although static model can lead sufficient resemblance with real case for steady state DC loading applications, for transient stages and pulsed current loading applications an alternative model named in literature as dynamic model which is shown in Fig. 2-2 is used. This dynamic model gives much accurate results compared to static model therefore for simulations of MPPT converter dynamic model should be used.

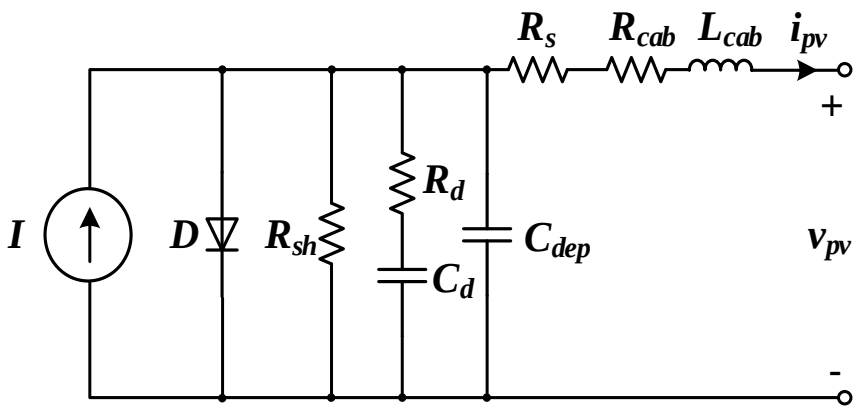



Figure 2-2: Equivalent circuit of multi-string PV system for dynamic model

As stated earlier PV module output power is significantly dependent on ambient temperature and solar irradiance. As it can be foreseen, increasing solar irradiance results in increase of output power and ambient temperature increase effects output power negatively. I-V curve of a photovoltaic panel is given in Fig. 2-3 for different values of solar irradiance.

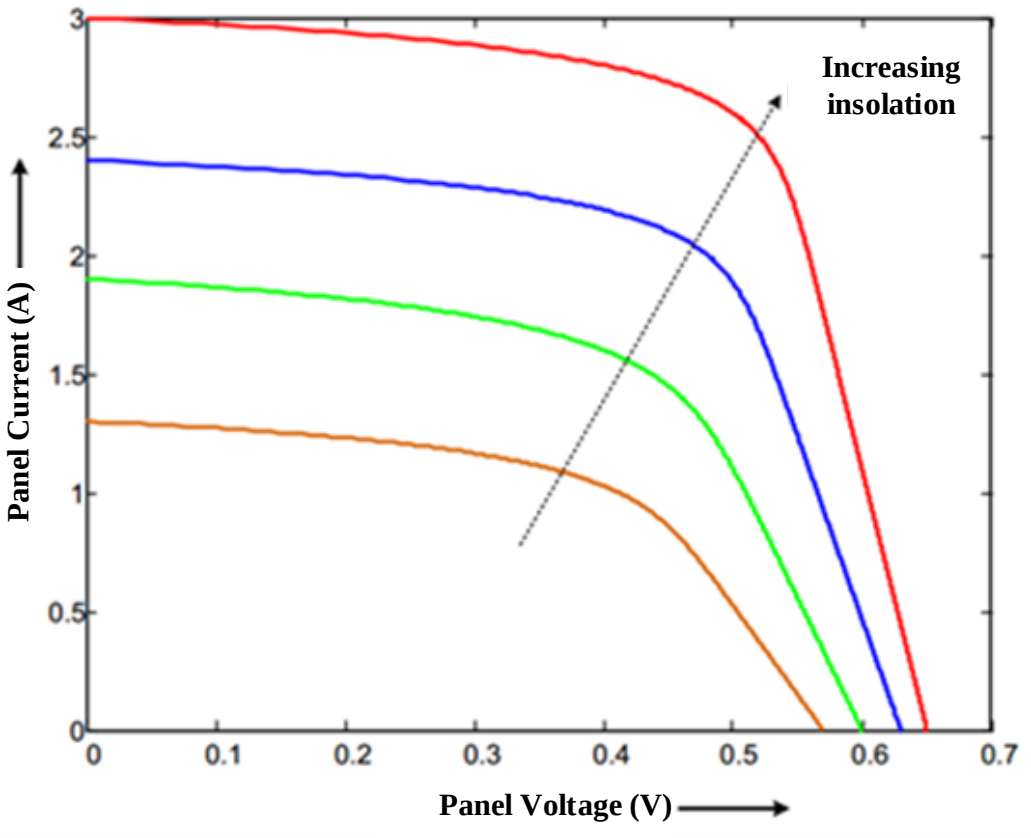



Figure 2-3: I-V curve of PV panel for different solar irradiance

As can be seen in Fig. 2-3 PV panel output voltage is maximum at open circuit condition. As the PV panel output current increases, PV panel output voltage decreases non-linearly. Also with the increasing solar irradiance for curves from brown to red, open circuit panel voltage and short circuit panel current hence maximum output power increases. Because of the non-linear change of PV panel output current and voltage, change of PV panel output power curve is expected to be a hill form with change of loading conditions which is shown in Fig. 2-4.

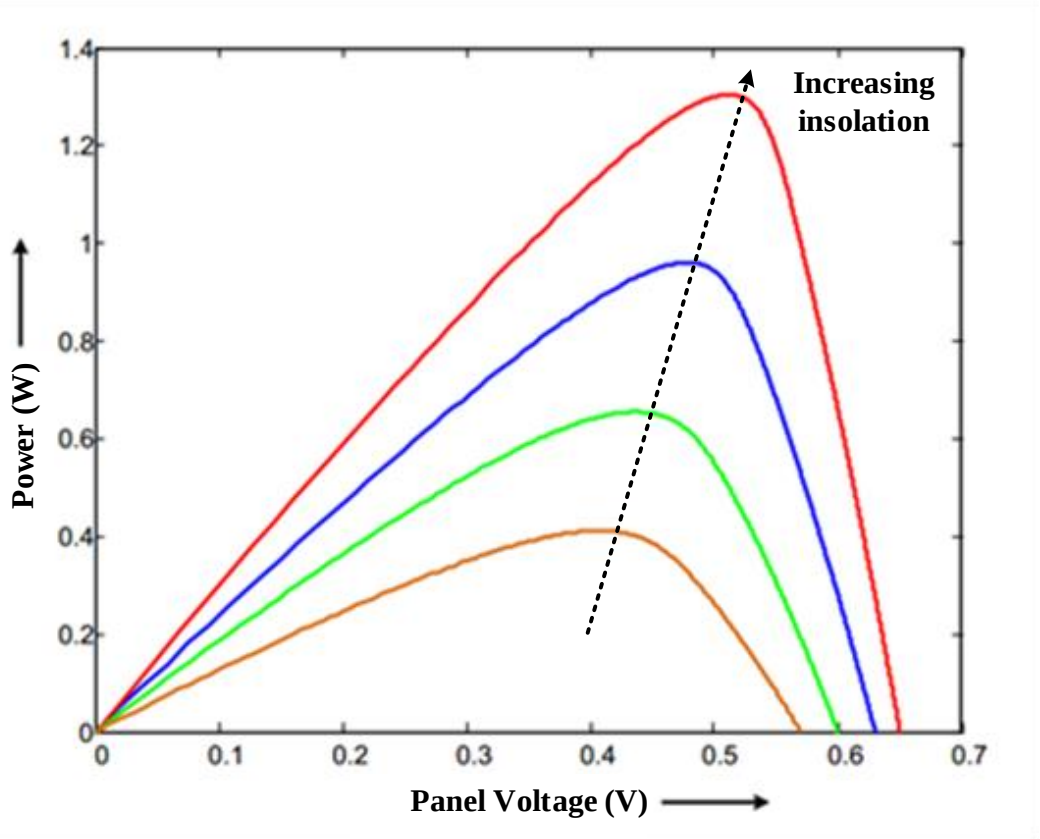



Figure 2-4: P-V curve of PV panel for different solar irradiance

As it can be seen in Fig. 2-4 panel output power reaches a maximum power point which occurs at a fixed loading condition and this loading point changes with solar irradiance and ambient temperature. Maximum power point tracking duty which can be done by a separate DC-DC converter or by inverter itself, aims to extract the maximum power from PV string, by changing the loading conditions. For maximum power point tracking, different algorithms exist such as perturb-observe, incremental conductance methods and some hybrid forms [6] [7]. Due to the fact that a separately designed MPPT converter is used in this research work, maximum power point tracking subject will not be detailed.

## 2.3. Photovoltaic System Requirements

In order to establish a photovoltaic system in an efficient and robust way and to keep power quality of transferred energy at desired standards, there are some expected requirements for PV systems.

To be able to get maximum use of installed PV strings, maximum power point tracking systems are used. According to the mission profile and rated power of the PV system, various PV configuration types can be used as well as inverter types and MPPT control algorithms. Apart from that, there are some regulations for the grid side requirements such as total harmonic distortion value of a lower level of 5% [8]. For high power rating PV systems, such as larger than hundreds kW, it is expected from PV system to support grid by providing or consuming reactive power and other necessary precautions for stabilizing grid voltage.

In addition to these general requirements, there are some more requirements changing by countries. Since the PV technology is more expensive compared to other energy sources such as wind energy there is a strong urge to increase the efficiency of PV system. In order to increase the efficiency, transformerless PV inverters are allowed and gain popularity in the European market [9]. On the other hand absence of galvanic isolation can cause a leakage current which can result in safety issues, so that reduction of leakage current is required in most cases [10].

Lastly reliability of PV system is also important for energy production to be not interrupted, since a possible failure can cause repairing costs as well as money loss due to idle system. Temperature intolerance is one of the most crucial factors that affects reliability of the system, due to the fact that exposure to sun and small inverter housings. High temperature results in degradation of some components of inverter. In order for prevention of failure due to temperature, inverter cooling mechanism must be well-designed and components with high temperature grade must be selected.

## 2.4. Photovoltaic System Configuration Types

Installed power of PV system installations changes from a couple of hundred W's to MW's. Because of this large range of variety, for different power levels, different system structures are used. These system structures can be composed under four main configuration types [11] [12]. As it is shown in Fig. 2-5 for small system use, power level up to 300 W which is the average power of a PV panel, module inverter is used. For residential use, power level between 1 kW and 10 kW string inverter, for commercial and residential uses, power between 10 kW and 30kW multi-string inverter, for commercial-utility scale uses, power level larger than 30 kW central inverter is used. These power levels which define the system configuration types are vague numbers and these configuration types can be used for different power levels, by considering advantages and disadvantages of each configuration type and system needs, in terms of efficiency, price, robustness and partial shading conditions.

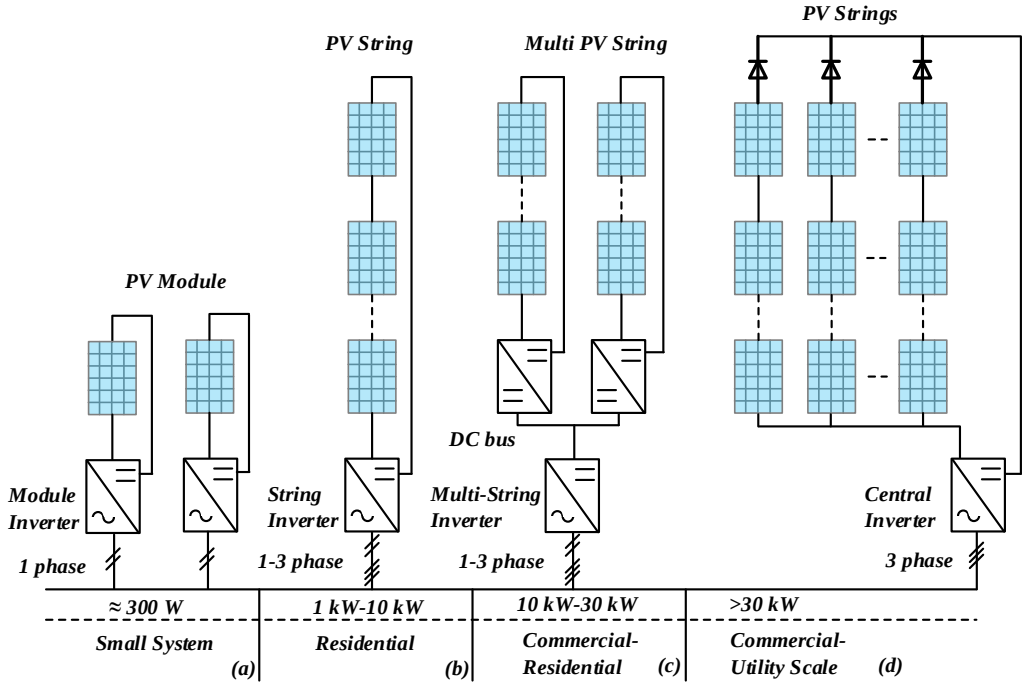



Figure 2-5: Different PV system configuration types based on demanded power for (a) small system/ (b) residential/ (c) commercial-residential/ (d) commercial-utility scale [13]

Module inverters are generally used for small PV installations. Since for each PV module a separate inverter is used in this configuration type, maximum power point tracking for this type of configuration is optimized and in the case of a malfunction, missing power is minimum during the maintenance and repair time. The disadvantages of this configuration type are mainly price and efficiency. Price/Watt for this type of inverter is higher compared to other types of inverters and efficiency values are lower compared to higher power rating inverters. Because of these listed disadvantages, those type of inverters are generally used in small systems.

String inverters are used as connected to a single PV string, so that each string maximum power point is tracked individually and this results in better MPPT. String inverters can be connected to single or three phase grid. For the case of PV string voltage is not enough, a DC-DC converter is used to increase the DC link voltage. This DC-DC converter could be a boost type or a HF-link transformer based converter. If the PV string voltage is enough and there is no need for galvanic isolation, PV inverter can be single stage, by taking necessary precautions for common mode currents. Also there is no need for string diodes, so that string diode losses can be eliminated. By taking into consideration these conditions, string inverters are advantageous in many ways especially in partial shading conditions.

Multi string inverter is a hybrid solution which combines the advantages of central inverters, in terms of low cost and string inverter, in terms of individual MPP tracking for each string. For each PV string there is a separate DC-DC converter in order to increase the voltage level and fulfill MPPT duty. Outputs of DC-DC converters are paralleled and transferred to grid by a single inverter. Also like in the string inverter case, a transformerless type can be adapted.

Central inverters are generally used in large scale utility systems by combining PV strings through string diodes. Central inverters are single stage inverters without a DC-DC converter. Since all of the PV strings are paralleled, strings do not operate in the exact maximum power point. Also due to string diodes and very long cabling, additional losses occur. Because of the absence of DC-DC converter, PV modules must be connected such that, output voltage of PV string reaches enough voltage for DC link mostly between 550-850 V. Another disadvantage of central inverter is that

a very large power source is dependent on a single inverter, and in the case of a malfunction, money loss is huge during the repair time. Despite of these disadvantages, central inverters have a very high efficiency value up to 99% and very low Price/Watt.

### 2.5. SiC Based MOSFETs

The occurrence of wide bandgap switching devices, namely as SiC and GaN base material MOSFETs, enabled higher efficiency and higher power density in many power electronic devices. In the recent years, SiC technology in switching devices has been commercialized. SiC switching devices have lower turn-on and turn-off times compared to traditional Si based switching elements. Also, on-state resistance for the fixed semiconductor area is relatively smaller in SiC devices. These conditions have resulted in better efficiency, increase of switching frequency, hence increase of power density in the area of power electronics application. Although switching frequency increase is not needed in all applications such as low voltage motor drives, since the motor inductance does enough filtering, higher efficiency for the same switching frequency is the advantage of SiC MOSFET use.

The radar chart comparison of traditional Si based switching devices and newly developed SiC based switching devices is given Fig. 2-6, in terms of junction temperature $T_j$/°C, Area/$, dv/dt, breakdown voltage and conductivity.

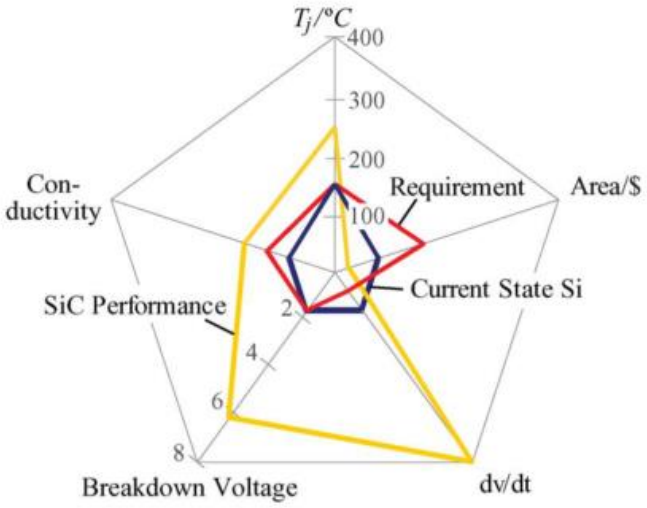



Figure 2-6: Radar chart comparison of Si and SiC based switching devices in terms of $T_j$/°C, Area/$, dv/dt, breakdown voltage and conductivity [14]

As it can be seen in Fig. 2-6 SiC MOSFETs show better performance, in terms of every aspect, except the price which is expected to drop in the next years. Apart from the efficiency and power density due to switching frequency increase, junction temperature limitation of SiC MOSFETs is larger than 175°C, which is around 125°C for Si based semiconductors for the same voltage and current rating. This rise in the limitation of junction temperature, results in shrinking of heat-sink volume independent from efficiency value.

Market share of wide bandgap devices of SiC and GaN based semiconductors is shown in Fig. 2-7, by power rating and operation frequency.

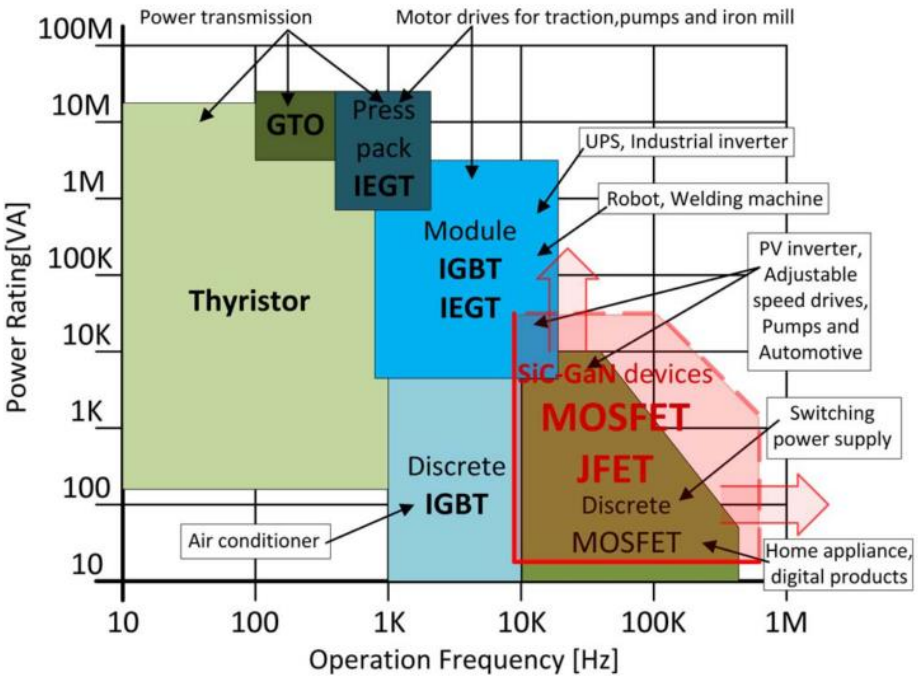



Figure 2-7: Market share of switching devices [15]

As it can be seen in Fig. 2-7, use of SiC based switching devices starts from 10 kHz operation frequency and power ratings up to 100 kVA, mainly in the applications of PV inverter, small pumps, adjustable speed drives and automotive. In addition, with the newly developed commercial SiC devices, upper limit of power rating tends to increase.

# CHAPTER 3

# OPERATING PRINCIPLES, ANALYSIS AND CONTROL OF GRID CONNECTED THREE-PHASE INVERTERS

## 3.1. Voltage Source Three-Phase Inverter

Three-phase voltage source inverter consists of three half bridge switches and each half bridge switch is used to generate sinusoidal voltage waveform for each phase. Power bridge of three-phase voltage source inverter can be seen in Fig. 3-1.

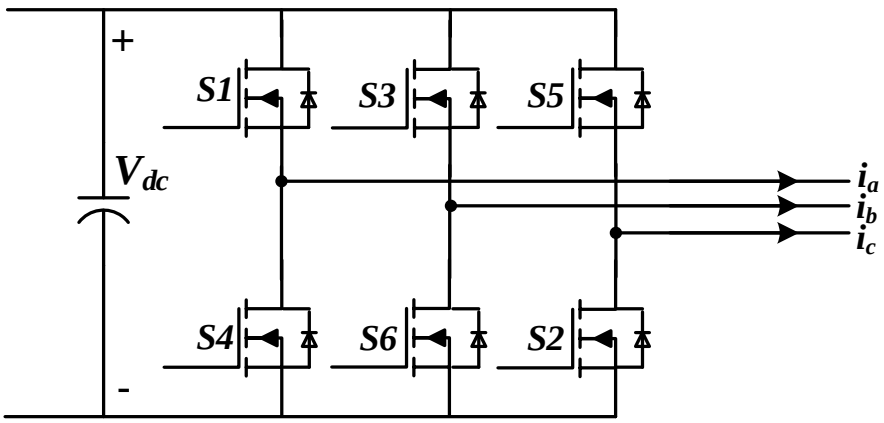



Figure 3-1: Three-phase voltage source inverter power bridge

When each half bridge is switched according to the selected PWM method, unfiltered output of power bridge occurs as a pulse width modulated voltage waveform. In order to generate sinusoidal voltage waveform and to be able to

transfer power to grid in a controlled way, a filter is needed. Single line diagram with an LCL filter is presented in Fig. 3-2.

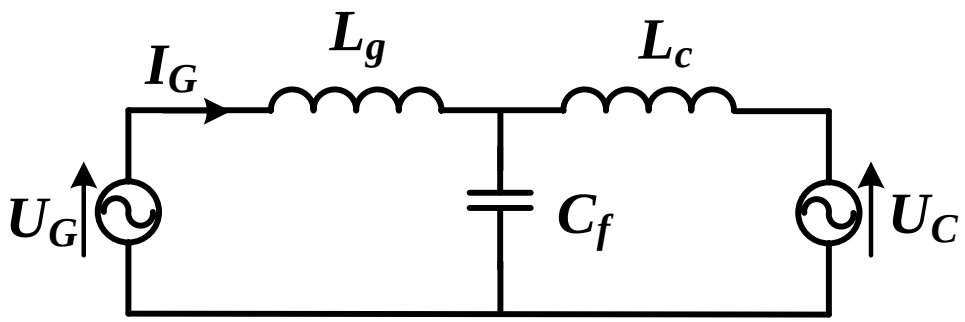



Figure 3-2: Simplified single line diagram of three-phase inverter

In order to transfer power to grid in a stable way, line impedance is needed since power transfer is done by changing phase and magnitude difference between inverter output voltage and grid voltage. So that this line impedance limits the current flowing from inverter to grid or vice versa. According to the signal line diagram of the inverter phasor diagram of three-phase voltage source inverter for different operating conditions is given in Fig. 3-3.

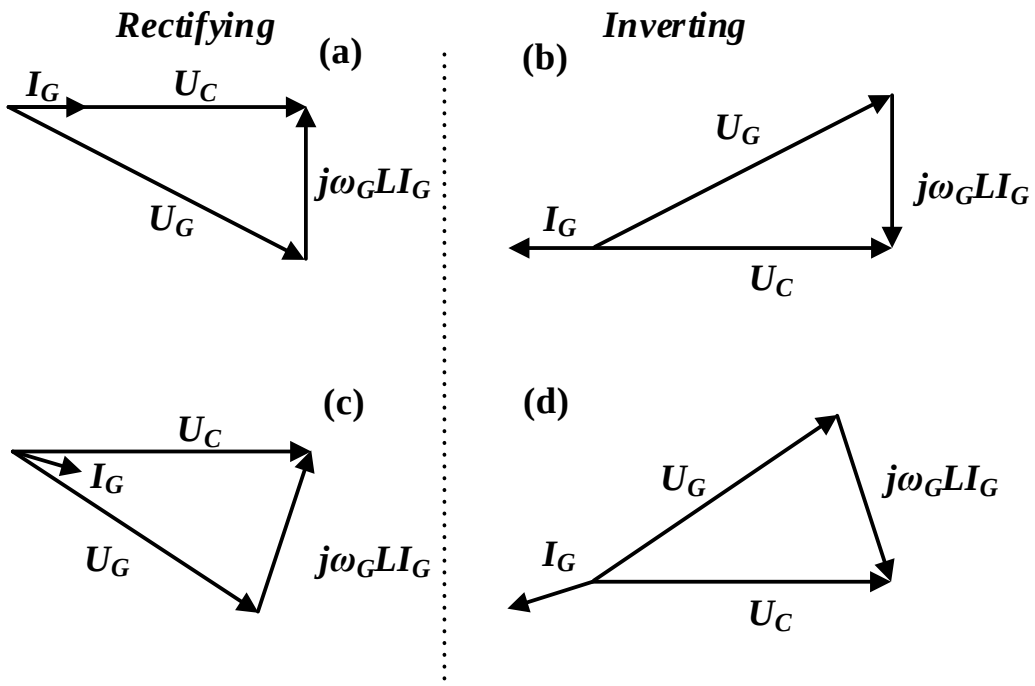



Figure 3-3: Phasor diagram according to operation mode of inverter (a) Unity power factor rectifying, (b) Unity power factor inverting, (c) Non-unity power factor rectifying, and (d) Non-unity power factor inverting.

As it can be seen in Fig. 3-3, $U_C$ defines the inverter output voltage while $U_G$ defines grid voltage. Inverter output line current is defined by the voltage and phase difference between inverter output and grid, also the line impedance between inverter output and grid. Since $U_C$ value is controllable with the change of switching state, in order to regulate the line current, control system modifies inverter output voltage. Besides, line impedance is necessary for the control loop to work in a stable way and to control line current. If the filter impedance is too small excessive current flows can occur, even if there is a minor phase and voltage difference between inverter output and grid.

When the phasor diagrams are examined, it can be seen that in inverting mode inverter output voltage waveform is leading compared to grid voltage waveform. And reactive power flow mostly occurs due to magnitude difference between inverter output voltage and grid voltage. In this phasor diagram, resistance between inverter output and grid is ignored and it can be included, when the filter resistance should be taken into consideration.

## 3.2. Control Strategy of Three-Phase Inverter

### 3.2.1. Control Methods

There are various control methods for three-phase grid connected voltage source inverters. Although the control algorithms for these control methods are different, main purposes are the same.

One of these main purposes is stabilizing DC-link voltage at the desired value. For single stage inverters, which does not contain a DC-DC converter for MPPT function, desired DC-link voltage value of inverter changes to track MPP value. Due to the fact that there is a DC-DC converter to track maximum power point and increase the voltage level, control loop is used to stabilize the DC-link at a fixed value by regulating the active power transfer to grid, in order to accomplish the power balance between the power generated from PV strings and power transferred into the grid.

Another main purpose of control method is to maintain the power factor at the desired value. Most of the time inverter is wanted to work at unity power factor, which is the case of zero reactive power. However, in some cases the grid infrastructure can be in the need of reactive power sources or reactive power loads. In those cases, inverter can extract or inject from/to grid in order to support grid. Also, control loop is responsible from harmonic content of line currents injected to grid. There are various control methods and modifications in order to keep total harmonic distortion of line currents at minimum.

The control methods for three-phase grid connected voltage source inverter can be listed as synchronous rotating (dq) reference frame control, stationary ($\alpha\beta$) reference frame control and natural (abc) reference frame control.

Synchronously rotated reference frame control, also named as DQ control, is one of the very popular algorithms in three-phase inverter control. Grid angle, $\theta$ value is obtained from phase locked loop algorithm applied to line to neutral phase voltages $v_{a\text{-}n,\ b\text{-}n,\ c\text{-}n}$. And by applying park transformation to measured line currents $i_{a,b,c}$, PI controllable DC quantities of line currents, which are $i_d$ and $i_q$, are obtained. These

two quantities are the main two main controllable variables to control the whole system in a stable way.

The transformation phasor diagram of line currents, $i_{a,b,c}$ to DC quantities of $i_d$ and $i_q$ is given in Fig.3-4.

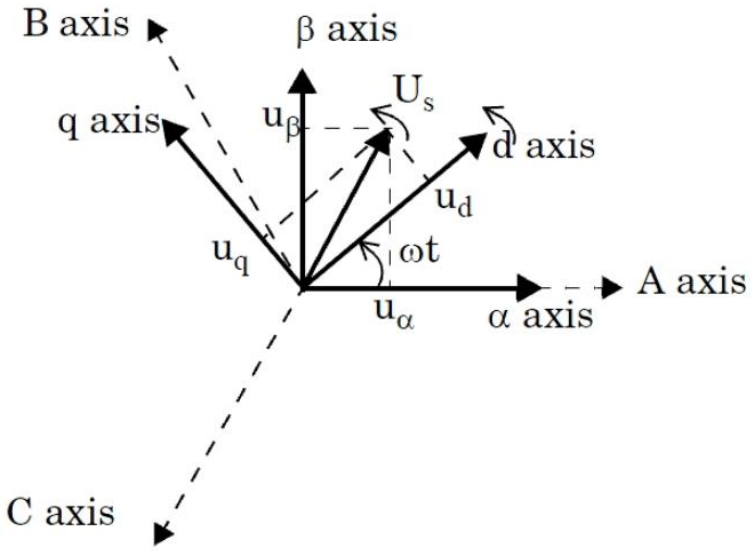



Figure 3-4: Synchronous reference frame of phase currents

DQ transformation is done according to the following equation below.

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3\text{-}1)$$

The error value between the measured DC link voltage and the reference value of DC link voltage, is implemented by PI controller to generate referenced active

current component value which is $i_d^*$. This referenced $i_d^*$ value specifies how much active current is needed in order to keep the DC link voltage at the desired value. After this PI controller, in order to control current, a second inner current control loop takes part. The measured $i_d$ value is subtracted from referenced $i_d^*$ value and goes into a PI controller, in order to generate voltage referenced signal which is $v_d^*$. Although in ideal conditions, which is line currents are pure sin wave at fundamental frequency, and unbalance does not exist, $i_d$ and $i_q$ values are pure DC, but this is not the actual case. In real conditions, due to line current unbalance and low order current harmonics, there will be oscillations on $i_d$ and $i_q$ values, and this inner current control loop tries to fixate these oscillations and equalize them to referenced $i_d^*$ and $i_q^*$ value.

As the same logic with active current control loop, there is another control loop for reactive power. In order to regulate the reactive power at the desired value, a PI controller named as Q controller generates the referenced $i_q^*$ value, by subtracting measured Q value from referenced Q value. This system can change reactive power according to the grid needs. However most of the cases, system is desired to work at unity power factor conditions, so that this first PI controller named as Q controller is not needed and $i_q^*$ value is set as zero. Similarly, in the inner $i_d$ current control loop, in order to generate referenced $v_q$ value, there is a PI controller, which is implemented to the subtraction of $i_q^*$ and $i_q$. This PI controller makes the necessary changes at $v_q^*$ value in order to keep $i_q$ value at zero and regulate the oscillations. Also $v_d$ and $v_q$ values, achieved from DQ transformation of measured line to neutral voltage values, are feed-forwarded in order to reduce low order harmonics, which are also exist in grid, and also to improve the step response characteristics of three-phase inverter at voltage oscillation case at the grid.

The referenced D and Q axis reference waveforms are then transformed to abc axis reference waveforms, by implementing the following equation.

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \times \begin{bmatrix} d \\ q \\ 0 \end{bmatrix} \quad (3\text{-}2)$$

The main disadvantage of this control strategy is the poor attenuation of low order current harmonics. Even if, grid voltage and cross-coupling terms are adapted and feed-forwarded, still the compensation capacity is poor. In order to improve that compensation, current compensators, which are specified for fixed low order harmonics especially $5^{th}$ and $7^{th}$, can be adapted. The synchronously rotating reference frame control structure is presented in Fig. 3-5.

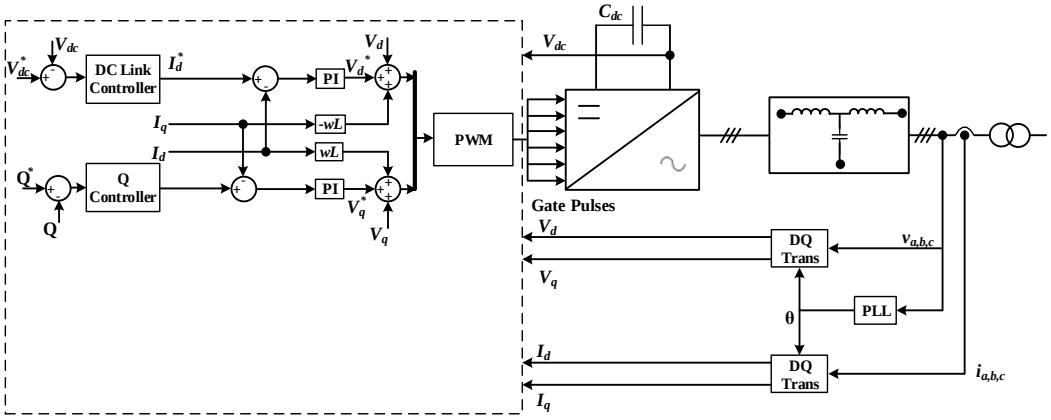



Figure 3-5: Synchronous rotating frame control (dq-control) structure of three-phase inverter

Another control method is stationary referenced frame control, also known as αβ-control structure, is shown in Fig. 3-6.

In this control method, instead of transforming line current values to DC quantities of DQ components, line currents are transformed to αβ values, which are sinusoidal according to the following equation.

$$\begin{bmatrix}\alpha\\ \beta\\ o\end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix}1 & \cos\left(\frac{2\pi}{3}\right) & \cos\left(-\frac{2\pi}{3}\right)\\ 1 & \sin\left(\frac{2\pi}{3}\right) & \sin\left(-\frac{2\pi}{3}\right)\\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}\end{bmatrix} \times \begin{bmatrix}a\\ b\\ c\end{bmatrix} \quad (3\text{-}3)$$

The PI controllers, used in synchronously rotating reference frame control, does not remove steady state error completely, when the error signal is time-varying. On the other hand, proportional resonant, PR, controllers eliminate the steady state error when the error signal is sinusoidal, which is the case in stationary referenced frame control, due to αβ values. Because of this reason PR controller has become very popular in control of three-phase grid connected inverters. Although PR controller low order harmonic current compensation capability is good, in order to further improve this capability harmonic compensation, HC, blocks tuned to 3rd, 5th and 7th harmonics, which are the most dominant low order harmonics, can be adapted. Besides PR controller shows good dynamic response characteristics [16].

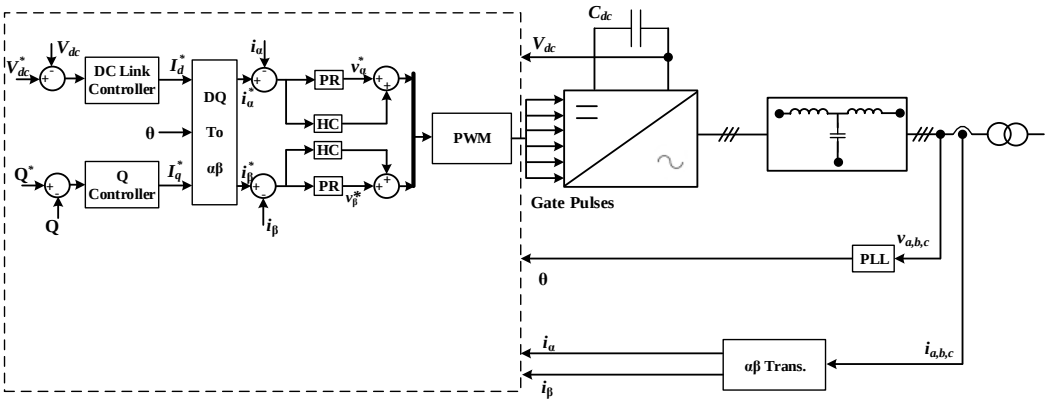



Figure 3-6: Stationary frame control (αβ-control) structure of three-phase inverter

According to natural referenced frame control method, each line current is controlled by a different current controller. By implementing PI controllers in DC link controller and Q controller stage, based on the parameters of value of referenced

DC link voltage subtracted by measured DC link voltage and value of referenced reactive power subtracted by measured reactive power, referenced $i_d^*$ and referenced $i_q^*$ values are obtained. Then these referenced DC quantity current values are transformed to referenced AC quantity line current values $i_a^*$, $i_b^*$ and $i_c^*$ by implementing inverse DQ transformation. Those referenced current values are subtracted by measured line currents and then this error signal goes into current controller, so that reference PWM signals are obtained. These current controller blocks are achieved by using proportional resonant, PR controller, since the controlled variable is a time varying sinusoidal wave, so that PI controller cannot be used. The structure of natural referenced frame control method also known as abc-control is given in Fig. 3-7.

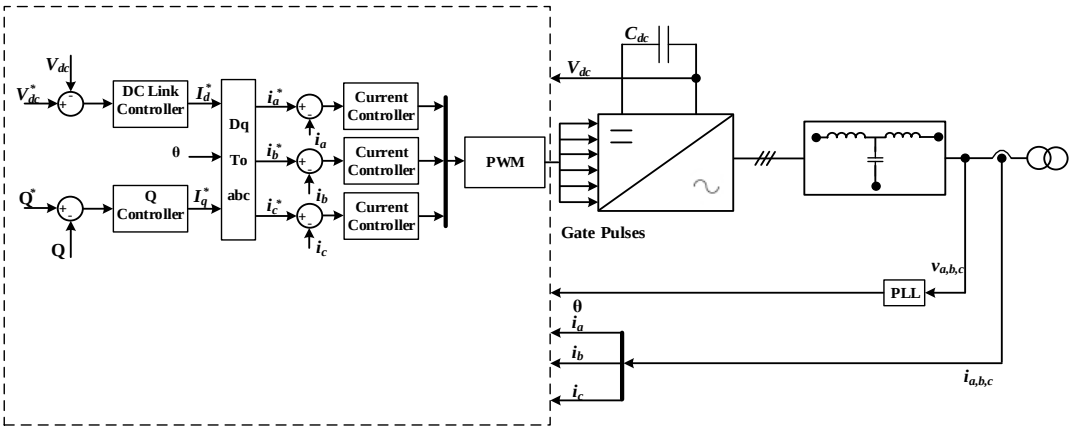



Figure 3-7: Natural frame control (abc-control) structure of three-phase inverter

The rotational angle, θ, which is needed to implement DQ transformation, is obtained via using phase locked loop block. Despite the fact that rotational angle can be obtained by zero cross detection of line to neutral voltage measurement, due to oscillations, this method can result in wrong calculations of rotational angle. Instead of zero cross detection method, synchronous reference frame method [17] can be used among various PLL algorithms [18]. In this method, line to neutral voltage measurements are transformed via DQ transformation, by using the rotational angle obtained from PLL block. If the rotational angle is correct, the

resulting quadrature axis component should be zero. So that, this quadrature axis component of voltage goes into a PI controller to obtain angular velocity. And integral of this angular velocity occurs as the rotational angle, which is the rotational angle used in DQ transformation of the PLL block. When the closed loop control of the PLL block is stabilized, quadrature axis component resulted from DQ transformation occurs as zero, since the rotational angle is set to correct value. Synchronous reference frame phase locked loop block diagram is given in Fig. 3-8.

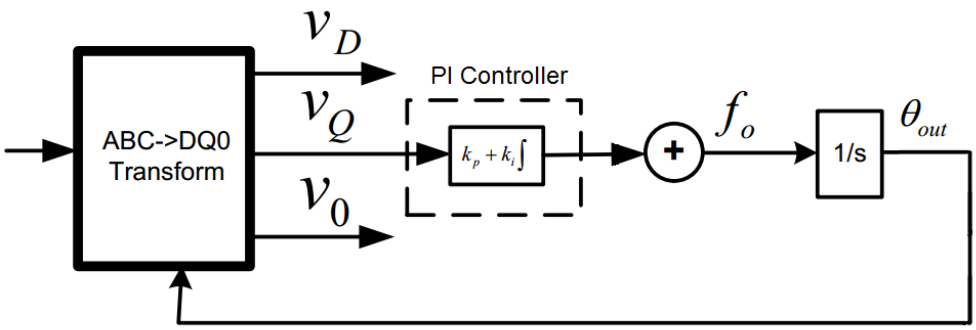



Figure 3-8: Synchronous reference frame phase locked loop block diagram

## 3.3. Pulse Width Modulation Techniques

### 3.3.1. Sinusoidal Pulse Width Modulation

Sinusoidal pulse width modulation is one of the many pulse width modulation methods, which is also simplest and widely used. Basically in sinusoidal pulse width modulation technique, a reference signal for each phase is generated and compared with a triangle signal, whose frequency is set to switching frequency. Switches are turned on when the reference signal becomes higher than triangular waveform and turned off when the reference signal becomes lower than triangular waveform. MOSFETs in half bridge are in the inverse state with the other MOSFETs in the half bridge, in order to prevent a short-through event by settig an appropriate dead time between turn on instant of a MOSFET and turn off instant of other MOSFET in the half bridge. According to the frequency of triangular waveform, switching frequency of inverter is defined. Each reference waveform has a phase difference of 120° between one and another, as shown in illustration of sinusoidal pulse width

modulation technique in Fig. 3-9. According to the frequency of triangular waveform, high frequency switching harmonic occurs at the line currents.

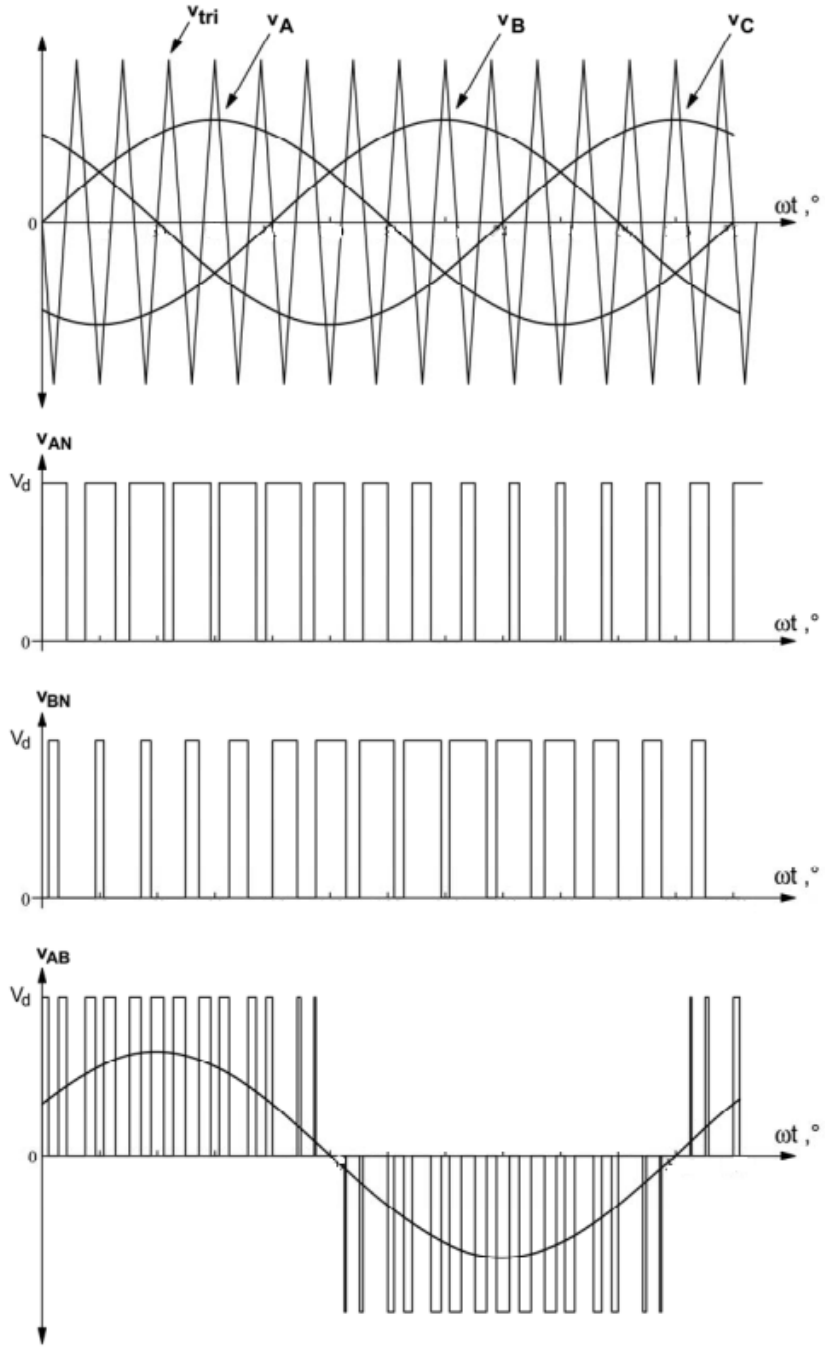



Figure 3-9: Illustration of sinusoidal pulse width modulation technique [19]

According to the turn-on rising time and turn off falling time of semiconductor switch, an appropriate dead time should be used. Implementation type of dead time is presented in Fig. 3-10. When the active high complementary switching is used, high side MOSFET will be turned on, when the reference signal is larger than triangular signal. During turn on and turn off instants, rising edge delay time and falling edge delay times are applied respectively.

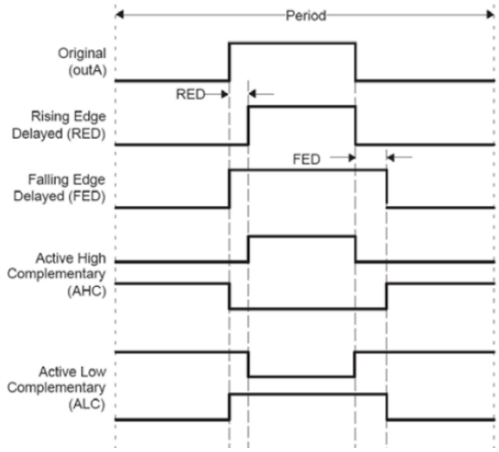



Figure 3-10: Dead-time implementation types [20]

Modulation index is defined via division of peak to peak magnitude of reference signal by peak to peak magnitude of triangular voltage waveform, which is the carrying signal. Three-phase inverter line-to-line RMS voltage/DC link voltage value as a function of modulating index is given in Fig. 3-11.

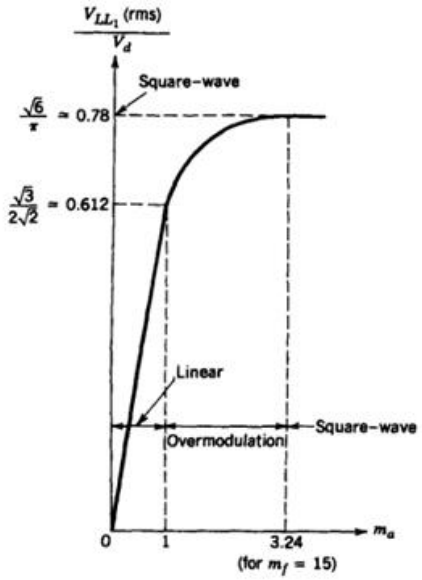



Figure 3-11: Three-phase inverter line-to-line RMS voltage/DC link voltage, $V_{LL(rms)}/V_d$ as a function of modulation index [19]

As presented in Fig. 3-11, during linear modulation in which modulating index, $m_a$ is smaller than 1, inverter line-to-line RMS voltage/DC link voltage is 0.612. As the modulating index increases this value is saturated to 0.78, even if inverter is modulated by square-wave operation. However, when $m_a$ is larger than 1, which is the over-modulation case, low order harmonics start to occur in inverter output voltage and hence inverter output current. Because of that, over-modulation is not preferred in SPWM. In order to prevent this, DC link voltage should be selected by considering line to line grid voltage and liner modulation conditions.

### 3.3.2. Space Vector Pulse Width Modulation

Space vector pulse width modulation, SVPWM is a special pulse width modulation technique that uses a switching sequence of three high side semiconductor device of three phase voltage source inverter, in applications of motor drives and PV inverters. This switching sequence for semiconductor devices establish three sinusoidal currents at the inverter output flowing to the grid.

Compared to sinusoidal pulse width modulation technique, SVPWM shows less harmonic distortion in the line currents and inverter output voltages. Also with SVPWM DC link voltage is used more efficiently, which means less DC link voltage is needed without generating low order harmonics.

According to the diagram of three phase inverter power bridge, which consists of three half bridges, there exists eight possible switching states of high side power semiconductor switches, since the low side semiconductor switches are at the inverse state of the high side semiconductor switch states. Device switching patterns and instantaneous voltage values of three-phase inverter are presented in Table 3-1.

Table 3-1: Device switching patterns and instantaneous voltage values of three-phase inverter

| **c** | **b** | **a** | $\mathbf{V_{AN}}$ | $\mathbf{V_{BN}}$ | $\mathbf{V_{CN}}$ | $\mathbf{V_{AB}}$ | $\mathbf{V_{BC}}$ | $\mathbf{V_{CA}}$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | $2V_{DC}/3$ | $-V_{DC}/3$ | $-V_{DC}/3$ | $V_{DC}$ | 0 | $-V_{DC}$ |
| 0 | 1 | 0 | $-V_{DC}/3$ | $2V_{DC}/3$ | $-V_{DC}/3$ | $-V_{DC}$ | $V_{DC}$ | 0 |
| 0 | 1 | 1 | $V_{DC}/3$ | $V_{DC}/3$ | $-2V_{DC}/3$ | 0 | $V_{DC}$ | $-V_{DC}$ |
| 1 | 0 | 0 | $-V_{DC}/3$ | $-V_{DC}/3$ | $2V_{DC}/3$ | 0 | $-V_{DC}$ | $V_{DC}$ |
| 1 | 0 | 1 | $V_{DC}/3$ | $-2V_{DC}/3$ | $V_{DC}/3$ | $V_{DC}$ | $-V_{DC}$ | 0 |
| 1 | 1 | 0 | $-2V_{DC}/3$ | $V_{DC}/3$ | $V_{DC}/3$ | $-V_{DC}$ | 0 | $V_{DC}$ |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The space vector projections of these eight switching combinations are called as basic space vectors, and reference voltage vector projection are given in Fig. 3-12. Note that the combination of every high side MOSFET switching state on and off conditions, are called as zero vectors and does not generate an output voltage.

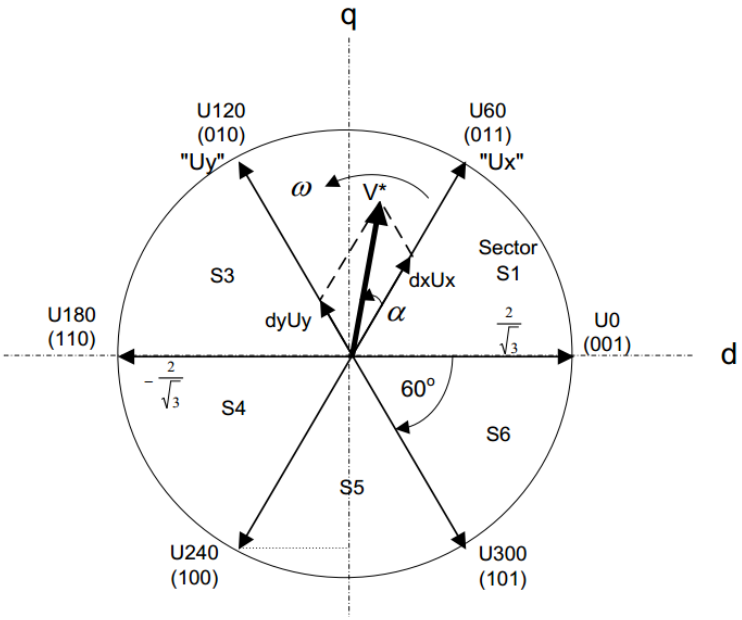



Figure 3-12: Reference voltage and basic space vectors projection for SVPWM

As shown in Fig. 3-12, reference voltage vector, $V^*$ is the voltage reference generated by the control loop to transfer desired current to grid. In order to generate this reference voltage vector, a time average combination of relevant basic vectors that are adjacent to the reference voltage vector at the instantaneous state and zero vectors should be used in a PWM switching period with respective time averages.

# CHAPTER 4

# DESIGN AND IMPLEMENTATION OF THREE PHASE GRID CONNECTED INVERTER

## 4.1. Introduction

Within the scope of this thesis a 30 kW two-level 3-phase grid connected SiC inverter has been designed and implemented. The main focus of this design is to transfer solar energy to 3-phase 50 Hz 400 V l-l grid in an efficient, robust way and minimize the passive components, in other words input DC capacitor and output LCL filter volume, as far as possible. Another goal is to keep the current harmonics, which are injected to grid, within maximum harmonic current distortion limit according to IEEE STD 519-2014.

The implemented system configuration, which can be seen in Fig. 4-1, is consisting of multi-string PV system, high-frequency link phase shifted full bridge SiC MPPT converter, which is designed and implemented by Hacettepe University, and 3-phase two-level grid connected SiC inverter. While maximum power tracking duty is accomplished by the MPPT converter, VSI inverter is responsible of grid synchronization, grid connection, power transfer and DC-link voltage stabilization. Utilization of high frequency AC link transformer in the MPPT converter enables the use of a conventional two level VSI with 6-pack MOSFET module, since HF-link transformer limits common mode currents, which flows from utilization grid ground to PV modules through earth and PV modules stray capacitance.

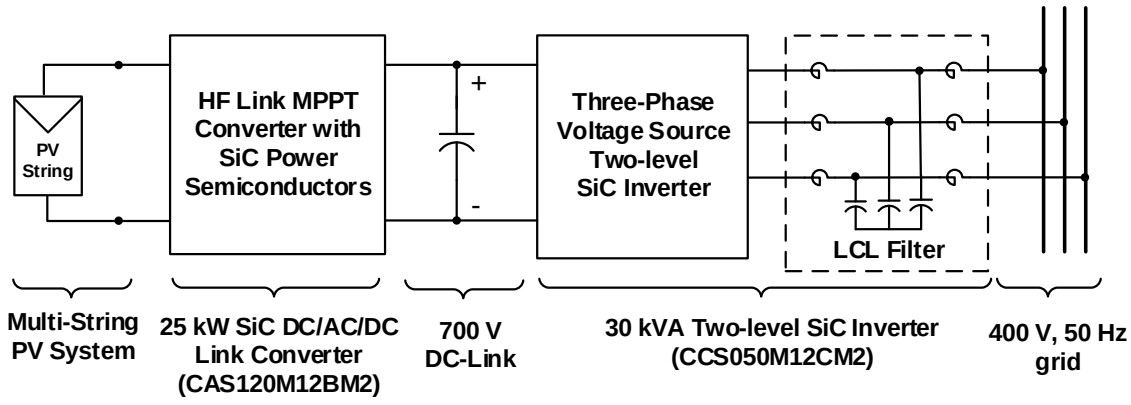



Figure 4-1: Experimental setup system configuration of high frequency link MPPT converter and two-level VSI [5]

During the implementation of multi-string PV system, in order to meet MPPT converter design parameter specifications, CSUN 255-60P PV modules are used as 19 series and 5 parallel strings configuration, so that PV system open voltage occurs as 712 V and MPPT voltage occurs as 572 V, at the ambient conditions of 20°C ambient temperature, 800 W/m$^2$ solar irradiance, according to the electrical characteristics of CSUN 255-60P photovoltaic module, which is shown in Fig. 4-2.

**Electrical characteristics at Standard Test Conditions(STC)**

| Module type | CSUN 255-60P | CSUN 250-60P | CSUN 245-60P | CSUN 240-60P | CSUN 235-60P |
|---|---|---|---|---|---|
| Pmpp [W] | 255 | 250 | 245 | 240 | 235 |
| Voc [V] | 37.5 | 37.3 | 37.1 | 36.9 | 36.8 |
| Isc [A] | 8.88 | 8.81 | 8.74 | 8.67 | 8.59 |
| Vmpp [V] | 30.1 | 29.9 | 29.7 | 29.6 | 29.5 |
| Impp [A] | 8.47 | 8.36 | 8.25 | 8.11 | 7.97 |
| Module efficiency | 15.70% | 15.40% | 15.09% | 14.78% | 14.47% |

Standard Test Conditions(STC):irradiance 1000W/m$^2$; AM 1.5G; module temperature 25 ℃.Measuring uncertainty of power is within ±3%. Tolerance of Pmpp:0~+3%. Certified in accordance with IEC61215,IEC61730-1/2 and UL1703.

**Electrical characteristics at Nominal Operating Cell Temperature(NOCT)**

| Module type | CSUN 300-72P | CSUN 295-72P | CSUN 290-72P | CSUN 285-75P | CSUN 280-72P |
|---|---|---|---|---|---|
| Maximum Power-Pmax | 188 | 185 | 181 | 178 | 175 |
| Open Circuit Voltage(V)-Voc(V) | 34.6 | 34.5 | 34.2 | 34.0 | 33.8 |
| Short Circuit Current(A)-Isc(A) | 7.16 | 7.10 | 7.02 | 6.95 | 6.90 |
| Maximum Power Voltage-Vmp(V) | 28.0 | 27.9 | 27.5 | 27.2 | 27.0 |
| Maximum Power Current-Impp(A) | 6.72 | 6.64 | 6.58 | 6.54 | 6.48 |

Nominal Operating Module Temperature(NOCT): irradiance 800W/m$^2$; wind speed 1m/s; module temperature 45 ℃;ambient temperature 20 ℃. Measuring uncertainty of power is within ±3%.Certified in accordance with IEC61215, IEC61730-1/2 and UL1703.

**Temperature Characteristics**

| | |
|---|---|
| Voltage Temperature Coefficient | -0.292%/ ℃ |
| Current Temperature Coefficient | +0.045%/ ℃ |
| Power Temperature Coefficient | -0.408%/ ℃ |

**Maximum Ratings**

| | |
|---|---|
| Maximum system voltage(V) | 1000 |
| Series fuse rating(A) | 20 |
| Reverse current overload(A) | 27 |

Figure 4-2: Electrical characteristics of CSUN 255-60P photovoltaic module [21]

## 4.2. Optimum DC Link Voltage

Value of DC link voltage, which is MPPT converter output, and VSI input is kept constant by the inverter in the entire range of operation, no matter the amount of PV power. VSI is supposed to transfer all the power from MPPT converter, into grid and by keeping the value of the DC link constant, this duty is accomplished. As the solar power increases, power output of the MPPT converter increases, and this condition results in the increase of the DC link voltage, if voltage control does not exist. But, the control circuitry of the VSI is going to react to keep the DC link voltage constant, by increasing the active power transfer to grid by changing VSI inverter output voltage magnitude and phase with respect to grid voltage magnitude and phase. DC link voltage may vary in some applications, such as single-stage solar voltage source inverter systems in mostly central inverter configurations [22]. In those applications DC/DC converter stages, which are mostly boost converter serves as MPPT converters, are removed, due to prevent losses occurring in the DC/DC conversion. Maximum power point tracking duty is done by the inverter by varying DC link voltage, such as decreasing or increasing DC link voltage to increase or decrease the current drawn from solar array in a specific manner, to track maximum power point with the various conditions of solar irradiation, ambient temperature and so on. Since in the implemented grid connected PV inverter, MPP tracking is done by the MPPT converter, DC link voltage is constant.

DC link voltage, $V_{dc}$ has effects on some features of the inverter, such as efficiency and high frequency current ripple on the filter inductor. For the same output filter inductance value, higher DC link voltage results in increase of the switching frequency current ripple, which increase magnetic losses in the inductor and current harmonic distortion at the switching frequency. Another adverse outcome is the increase of the RMS value of the current through semiconductor switches for the same fundamental output current component, which also results in increase of conduction and switching losses on semiconductor switches. As the $V_{dc}$ increases, M, which is the modulation index, decreases when the output voltage value is constant.

$$M = \frac{2\sqrt{2}}{\sqrt{3}} \times \frac{V}{V_{dc}} \qquad (4\text{-}1)$$

Where V is the l-to-l RMS value of the inverter output voltage value and $V_{dc}$ is the DC link voltage value of the inverter.

In IEC 60038 2002-07 Standard Voltages [23], 50 Hz l-to-l voltage variation ranges are specified. According to this standard, maximum voltage variations in the grid voltages are specified as between +6% and -10%. At the consumer connection points this variation band is increased 4% more and becomes +10% and -14%. These variations in the grid voltage determines variation range of modulation index, M for fixed DC bus voltage under SPWM. Calculated and simulated variation range of M, according to grid voltage disturbances are as shown in Fig. 4-3 and Fig. 4-4.

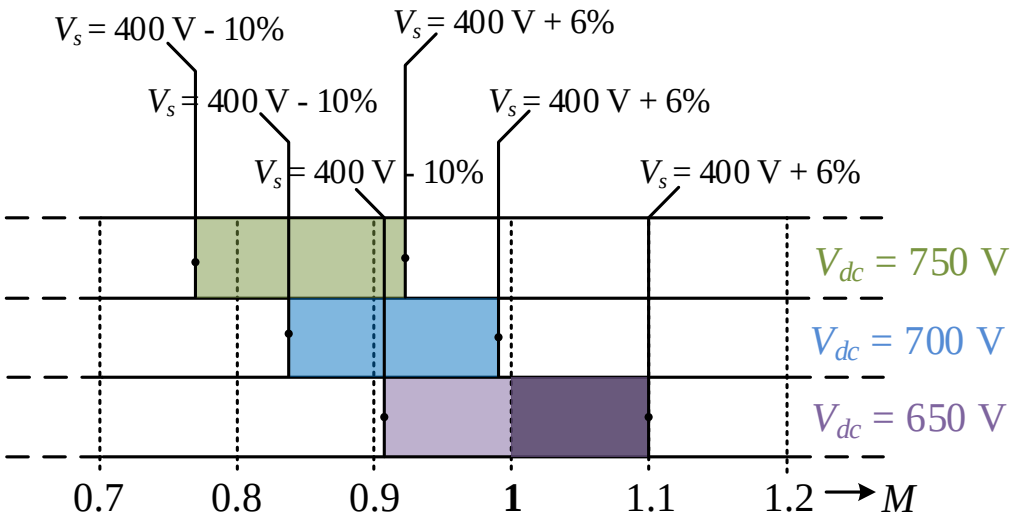



Figure 4-3: Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +6% -10% as specified in IEC 60038 2002-07 Standard Voltages for the supply side voltage range

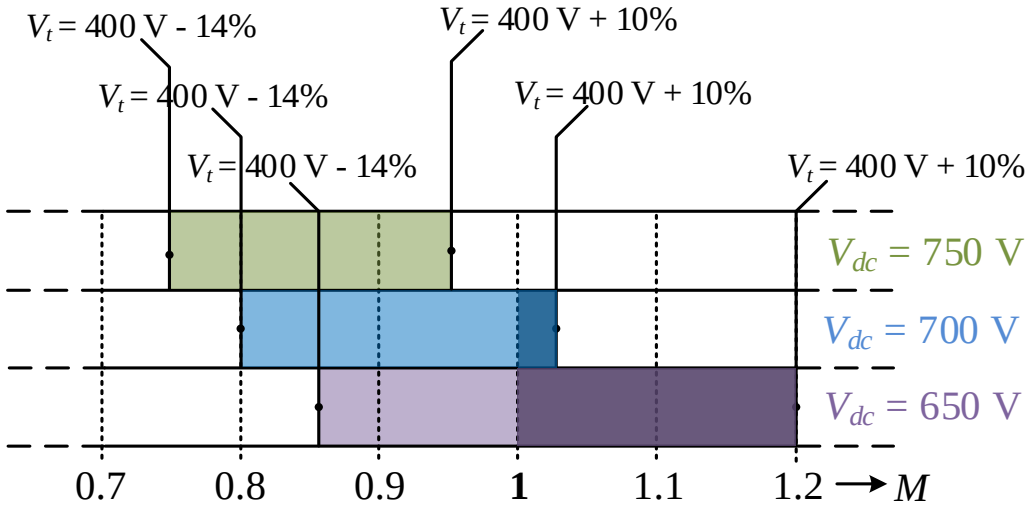



Figure 4-4: Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +10% -14% as specified in IEC 60038 2002-07 Standard Voltages for the utilization voltage range

According to these plots, which are shown in Fig. 4-3 and Fig. 4-4, it can be understood that optimum value for DC link voltage is around 700 V. For the supply side voltage upper and lower band limits, inverter does not goes into over-modulation, which causes low order harmonics. For the utilization voltage range, inverter works in slightly over-modulated at the upper band limit, which is acceptable. For 650 V DC bus voltage, inverter works highly over-modulated at the upper band limits of both supply side voltage and utilization voltage, which is unacceptable since low order harmonics grow dramatically. In the case of 750 V DC link voltage, inverter does not does into over-modulation in any case for both supply side and utilization side voltage limits, but modulation index M, is too low, which increases losses for the same switching frequency and same output filter. By considering these reasons listed above. DC link voltage is designated as 700 V.

Alternative design approaches, such as third harmonic injection [24], [25], enables to reduce DC link voltage to nearly 600 V without causing low order harmonics. So third harmonic injection method could be used to reduce switching and conduction losses by reducing DC link voltage in future works.

### 4.3. Optimum Switching Frequency

For many modulation techniques, such as SPWM and SVPWM, as the switching frequency increases, frequency of high order harmonics, which are also known as side-band harmonics occurring both sides of switching frequency and its' multiplies, also increases [26].So that, output filter corner frequency, in other words resonant frequency of LCL filter, can be set to a higher value in order to reduce the volume of passive components. However, increasing switching frequency has a drawback in terms of losses. As the switching frequency increases, switching loss occurring in power semiconductors proportionally increases with the frequency. Traditional Si based power semiconductors, such as IGBT, has significantly larger turn-on, turn-off times with respect to SiC based power semiconductor. So that, with the emergence of SiC power MOSFETs, switching frequency can be increased more, in comparison to IGBT switching frequency, for the same power rating of the inverter and for the same switching loss. But, benefits of increasing switching frequency, in terms of lowering the size of passive components, start to saturate at one point in the view point of control stability. Reducing inductor component of output filter causes stability problems, since voltage and phase difference between inverter output voltage and grid voltage is necessary to control power flow to grid. Output filter inductor is the component which compose the phase and voltage difference, and current flow occurs according to this difference between inverter output and grid voltage according to impedance between them, as can be understood from single line diagram of three phase inverter. Reducing impedance too much, between inverter output and grid voltage causes massive current flows, even with a slight voltage difference. This condition is also a problem, in terms of low order harmonics which exist in grid voltage. Low order voltage harmonics in the grid cause low order current flows, despite control circuitry current loop attenuation. Because of this reasons, output filter inductance has a minimum value which has shown in output filter design section, so that increasing switching frequency too much has no advantage after one point.

In order to find optimum switching frequency, loss calculations has been done for SiC MOSFETs conduction loss, switching loss, SiC body diode conduction loss,

output LCL filter copper loss and LCL filter core loss. These calculations are made for different switching frequencies such as 10, 20 and 30 kHz, which are seen to be feasible for inverter power rating and output LCL filter specifications. Loss analysis has been verified analytically, in addition to manufacturer loss analysis tool [27]. Detailed analytical loss calculation of power semiconductor losses and LCL output filter loss are also investigated in power loss calculation section. Loss components, such as the wiring from power source to inverter, inverter to grid and between discrete components of the inverter are ignored in the calculations. Also, only fundamental frequency current component, which is 50 Hz, has been taken into account during calculation of losses in SiC MOSFETs, even if there are switching current ripples about 25% of fundamental current superimposed on main current component, due to ease calculation. So, in fact, the real semiconductor and wiring loss before filtering is slightly higher than calculated value. When calculating the loss of LCL output filter losses, LCL filter is modified for the switching frequency, so that switching current ripple is the 25% of the fundamental 50 Hz current, due to consistency of switching frequency selection. Total power loss and distribution of loss components can be seen in Fig. 4-5. These calculations are made for output power of the inverter, $P_o$ = 22.3 kW which is the maximum achievable power from the installed PV system.

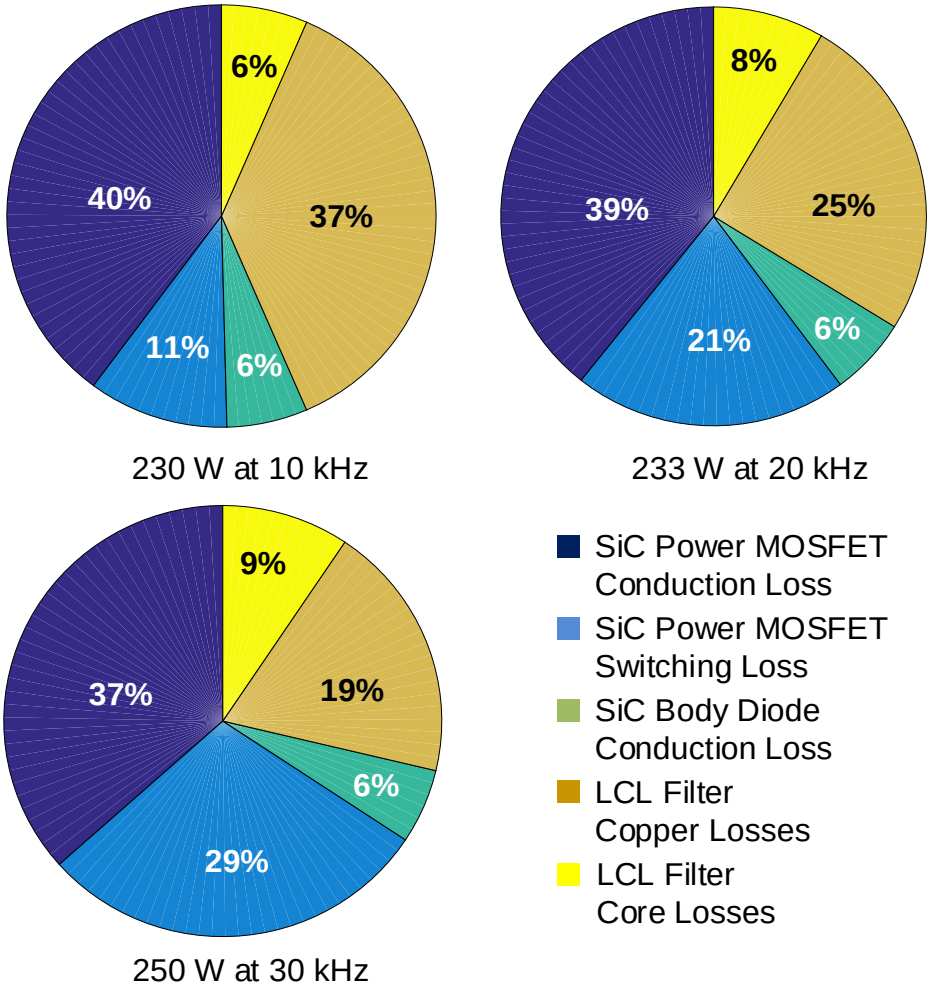



Figure 4-5: Total loss and distribution of loss components at $P_o$=22.3 kW for $f_{sw}$=10, 20 and 30 kHz

According to these results, switching frequency has been selected as 20 kHz, due to following reasons. 10 kHz switching frequency has almost no advantage in terms of losses and LCL filter size needs to be increased significantly. LCL filter copper loss increases dramatically, in order to have the same switching current ripple. In the case of 30 kHz switching frequency, LCL filter volume reduction according to 20 kHz switching frequency is not very remarkable, in addition, switching loss of SiC MOSFETs starts to be a considerable amount. Also, because of mentioned control loop stability problems, due to insufficient impedance between inverter output and grid voltage, 30 kHz switching frequency is not considered as advantageous. So that switching frequency is selected as 20 kHz.

### 4.4. DC Bus Capacitance Calculation and Capacitor Selection

When choosing DC link capacitor of the three-phase grid connected inverter, some parameters such as DC link capacitance, rated DC link voltage, capacitor ripple current and life time of capacitor need to be considered. Capacitance of DC link is a key feature, that affects DC link high frequency voltage ripple due to switching current ripple, and DC link capacitance is typically selected as to meet the design criteria of 1 or 2% ripple voltage on the DC link voltage [28]. Maximum power transfer from DC bus to grid in a single switching period, is given in the following formula.

$$\Delta W = T \times P_{max} \tag{4-2}$$

According to maximum power transfer, DC link capacitance, DC link voltage and ripple voltage on the DC link are given as;

$$\Delta V_{dc} = \frac{\Delta W}{V_{dc} \times C_{min}} \tag{4-3}$$

Minimum DC link capacitance can be calculated, in order to meet the required ripple at the maximum power transferring to grid as;

$$C_{min} = \frac{T \times P_{max}}{V_{dc} \times \Delta V_{dc}} \tag{4-4}$$

Even though installed PV array power rating is 23.750 W, inverter is designed to transfer 30 kW power to grid. Because of that, calculations made for 30 kW maximum power. For 30 kW $P_{max}$, 20 kHz switching frequency, 700 V DC link voltage and 1% $\Delta V_{dc}$, $C_{min}$ is calculated as 306 uF.

Other criteria to select DC bus capacitor, are equivalent series inductor, ESL, and equivalent series resistance, ESR, value of the capacitor. ESR value is critical in a way that determining ripple current capacity of the capacitor. Lower ESR means higher ripple current capacity, so less thermal stress on the capacitor, in order to increase the life time of the capacitor. ESL value of capacitor is important, in terms of voltage spikes on SiC MOSFETs, during turn off. ESL value of the capacitor and parasitic inductance of the power plane are get charged during on state of MOSFET, and during turn off state this charge results in a voltage spike on the parasitic

capacitance $C_{oss}$ on MOSFETs. This spike may cause hazardous effects, such as burning of the MOSFET, if the voltage spike exceeds maximum drain source voltage $V_{DS}$ of the MOSFET.

By considering all the reasons listed above, MKP1848C64010JY5 part number 1000 V 40uF metal film capacitor is selected, due to 5 mΩ low ESR, low ESL value, 17 A RMS ripple current capacity and 100.000 h very long useful life time. In order to be safe side considering voltage ripple, 12 piece capacitors, a total capacitance of 480 uF capacitor is used as DC link capacitor.

### 4.5. Output Filter Design

In order to attenuate high order harmonics, which resulting from switching at sidebands of the switching frequency, a low pass filter, mostly L or LCL type, is placed between output of the VSI and grid. LCL filter harmonic attenuation is considerably larger than L filter, due to the fact that LCL filter is a second order low pass filter, while L filter is a first order filter. Because of this reason, LCL filter needed inductance value is much lower compared to L filter, for the same harmonic attenuation, and this condition enables volume reduction of filter, lower filter loss and better current filtering. As can be seen in Fig. 4-6, LCL filter is composed of four components, $L_c$ as inverter side inductor, $L_g$ as grid side inductor, $C_f$ as filtering capacitor and $R_d$ as damping resistor. Although for this design damping resistor, $R_d$ is placed in series with the filtering capacitor $C_f$, there are several other methods for damping resistor placement, such as placing ramping resistor $R_d$ in parallel with filtering capacitor, in series with inverter side inductor $L_c$ or in parallel with inverter side inductor. All of this design type has some advantages and disadvantages.

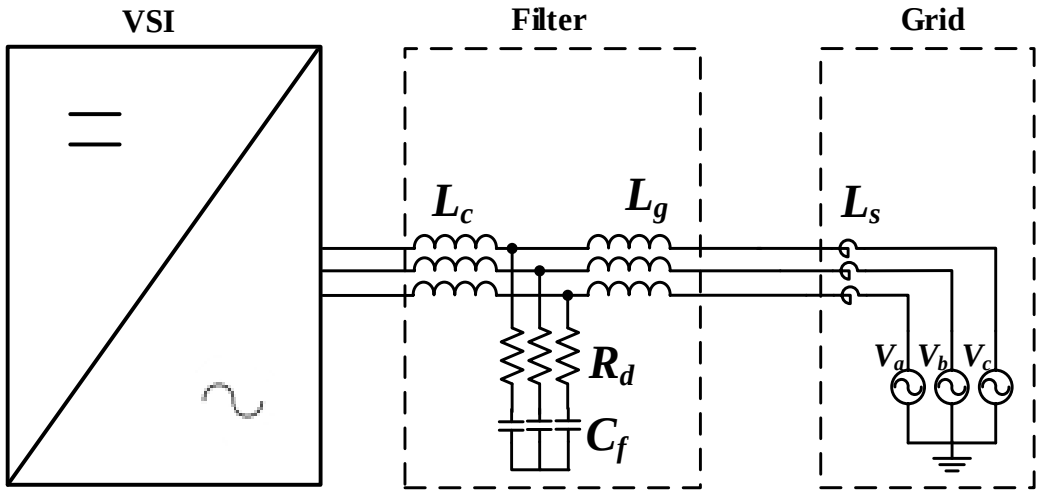



Figure 4-6: LCL filter based filtering circuit diagram of three-phase VSI

As design methodology of LCL filter, there are several design methods [29], [30] and for all of them the main design purpose is to maximize the high order harmonic filtration, caused from switching, with minimum reactive power consumption and filter volume. According to step by step design methodology [31] of LCL filter, LCL filter component values have been calculated in the following procedure.

Firstly, base parameters of impedance, capacitance and inductance have been given as;

$$Z_B = \frac{U_N{}^2}{P_N} \tag{4-5}$$

$$L_B = \frac{Z_B}{w_N} \tag{4-6}$$

$$C_B = \frac{1}{w_n Z_B} \tag{4-7}$$

Where $U_N$ is the l-to-l RMS voltage, which is $230\sqrt{3}$, $P_N$ is three-phase inverter power rating, which is 30 kW, and $w_n$ is the angular velocity, which is $2\pi 50$, in this

design. According to these formulas, base parameter values are calculated as $Z_B$=5,29, $L_B$=0,0168 and $C_B$= 0.0006

RMS value of line currents of VSI at rated power can be calculated as;

$$I_N = \frac{P_N}{\sqrt{3}U_N} \tag{4-8}$$

Where $I_N$ is found as 43,47 at full load.

In order to calculate inverter side inductor, $L_c$, the maximum ripple current flowing through $L_c$ must be defined. Maximum ripple current $I_{maxrip}$ can be defined between the values of 10% and 30% of the line current, $I_N$, at full load. Maximum ripple current on $L_c$ can be calculated as following;

$$I_{maxrip} = \sqrt{2}I_{maxripref} \times I_N \tag{4-9}$$

Where $I_{maxripref}$ is the percentage of ripple current according to nominal line current. According to calculated maximum ripple current, $I_{maxrip}$, inverter side inductor, $L_c$ can be calculated as;

$$L_c \geq \frac{V_{DC}}{6f_{sw}I_{maxrip}} \tag{4-10}$$

Where $f_{sw}$ is the switching frequency and $V_{DC}$ is the DC bus voltage.

According to given equations, for 30% switching ripple current, $I_{maxrip}$ is calculated as 18.44 A, and for 700 V DC bus voltage and 20 kHz switching frequency, $L_c$ is calculated as 316 uH.

Filtering capacitor, $C_f$ should be calculated according to base capacitance value, $C_b$. $C_f$, filtering capacitor value should be less than 5% of the base capacitance. In order to calculate filtering capacitor, the following equation is given.

$$C_f = C_{Fref}C_B = C_{Fref}\frac{P_N}{w_n{U_N}^2} \tag{4-11}$$

Where $C_{Fref}$ is the per unit capacitance. For selection of $C_{Fref}$ as 2.5%, filtering capacitor $C_f$ value is calculated as 15 uF.

Grid side inductor $L_g$ can be calculated as;

$$L_g = r_a L_c \tag{4-12}$$

Where $r_a$ is the ratio factor of inverter side inductance, and grid side inductance can be calculated as;

$$r_a = \left| \frac{1 - HA}{HA(1 - L_c C_f {w_{sw}}^2)} \right| \tag{4-13}$$

Where $w_{sw}$ is the switching frequency angular velocity, and HA is the harmonic attenuation percentage of the switching harmonics. Ratio factor, $r_a$ is calculated as 0.2, for the selection of HA as 0.16, so that $L_g$ is found as 62 uH. Transfer function of LCL filter from inverter to grid is given as;

$$\frac{I_G}{U_C} = H_{LCL(inv-to-grid)}(s) = \frac{1 + R_d C_f s}{L_c L_g C_f s^3 + L_c R_d C_f s^2 + L_g R_d C_f s^2 + L_c s + L_g s} \tag{4-14}$$

Transfer function of LCL filter from grid to inverter is given as;

$$\frac{I_G}{U_G} = H_{LCL(grid-to-inv)}(s) = \frac{1 + R_d C_f s + L_c C_f s^2}{L_c L_g C_f s^3 + L_c R_d C_f s^2 + L_g R_d C_f s^2 + L_c s + L_g s} \tag{4-15}$$

As it can be seen in above function, transfer functions, from inverter to grid and from grid to inverter are different. For an un-damped LCL filter, resonance frequency which is viewed from inverter side, $f_{ri}$ and resonance frequency which is viewed from grid side, $f_{rg}$ can be calculated as;

$$f_{ri} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_c}{L_g L_c C_f}}, \qquad f_{rg} = \frac{1}{2\pi}\sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \tag{4-16}$$

As it can be seen in above equation, $f_{ri}$ and $f_{rg}$ are the same.

Apart from that, there is another phenomenon in grid to inverter LCL filter transfer characteristics. At some frequency, which is called in this thesis as LCL filter grid to inverter attenuation resonance frequency, attenuation of LCL filter boosts, since

LCL filter impedance increases dramatically at this frequency. Grid attenuation resonance frequency can be calculated as;

$$f_{arg} = \frac{1}{2\pi}\sqrt{\frac{1}{L_c C_f}} \tag{4-17}$$

Where $f_{arg}$ is the grid to inverter attenuation resonance frequency.

Resonance phenomenon should be taken into consideration carefully when using LCL filter. For an LCL filter, at the resonance frequency harmonics, whose frequency is close to resonance frequency, are highly boosted. So that, resonance phenomenon causes very high harmonic distortion in line currents, stability issues even loss of synchronization of inverter with grid, if no precautions are taken. Firstly, resonance frequency should be selected according that resonance frequency should not be close to harmonic distortion sources in order to avoid boosting harmonics.

Resonance frequency should be in the limits which given as;

$$10f_G \leq f_{ri} \leq \frac{f_{sw}}{2} \tag{4-18}$$

Where $f_G$ is the grid fundamental frequency, which is 50 Hz in this case.

In order to damp the boosting effect at the resonance frequency, active damping or passive damping should be utilized [32], [33]. In this research work, passive damping is used by utilizing series damping resistor, $R_d$ in series with filtering capacitor. $R_d$ value affects the loss value on damping resistor, damping factor at resonance frequency and attenuation of switching frequency, so that resistance value must be carefully selected.

Apart from calculations of LCL filter components values, some modifications should be made with these components, in order to reduce volume of the filter, in the manner of providing enough attenuation at the switching frequency. By optimizing filter parameters, resulting components values are found as $L_c$=250uH,

$C_f$=15uF, $L_g$=50uH and $R_d$=0.22Ω. For these values, resonance frequency viewed from inverter side, is found as 6.66 kHz, which is $f_{sw}/3$, and provides enough attenuation of switching harmonics. For various set of filter components, without damping resistor, transfer characteristics of LCL filters is given in Fig.4-7.

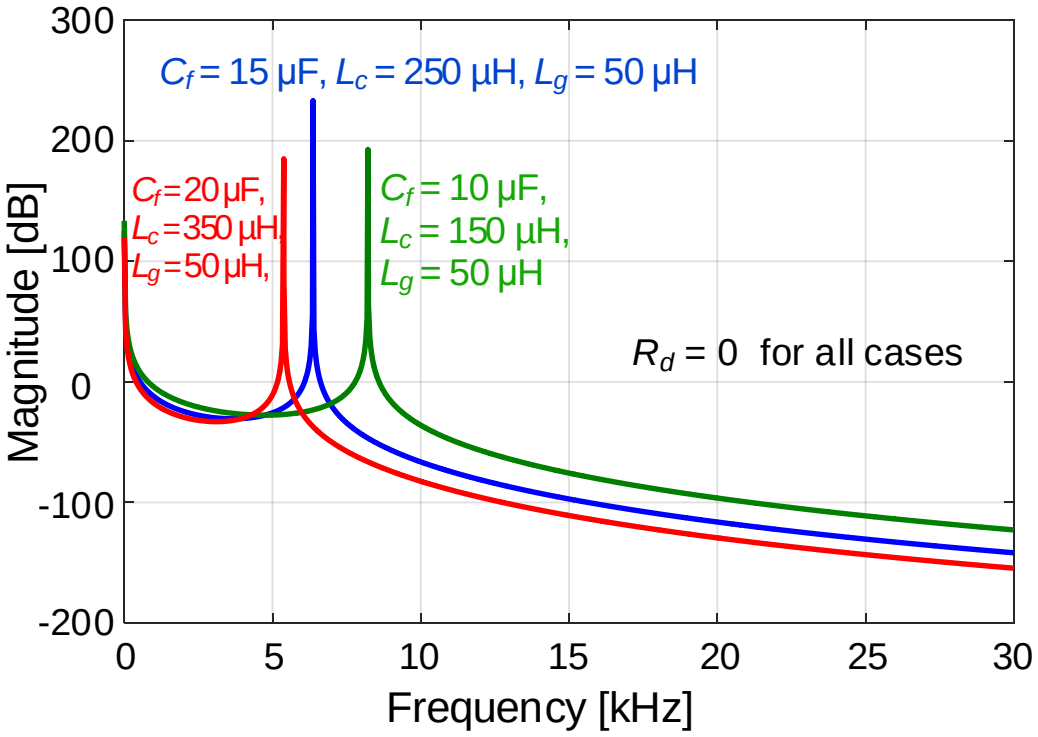



Figure 4-7: From inverter to grid transfer characteristics of various set of components values of LCL filters

As can be seen in Fig. 4-7, all LCL filter sets provide enough attenuation at switching frequency about -100dB. Red colored filter ($L_c$=350uH, $C_f$=20uF, $L_g$=50uH) is not chosen, since converter side inductor, $L_c$ increases volume of filter almost 40%, and that much attenuation is not needed. For the green colored filter ($L_c$=150uH, $C_f$=10uF, $L_g$=50uH), although it provides enough attenuation at switching frequency, and it has the minimum LCL filter volume, it is not chosen either, because of stability issues resulting from narrow control range of voltage and phase shift angle, causing output power oscillations and instability, since $L_c$ is too low. Field work experience has shown that, larger $L_c$ value enables to increase

proportional and integral term of PI current control and reduce of low order harmonics through current control. Boosting effect of harmonics, at resonant frequency, also can be seen in Fig. 4-7. In order to reduce and attenuate magnitude of amplification under 0 dB for several values of damping resistors $R_d$, change of transfer characteristics plotted, as can be seen in Fig. 4-8, for the selected LCL filter (($L_c$=250uH, $C_f$=15uF, $L_g$=50uH)).

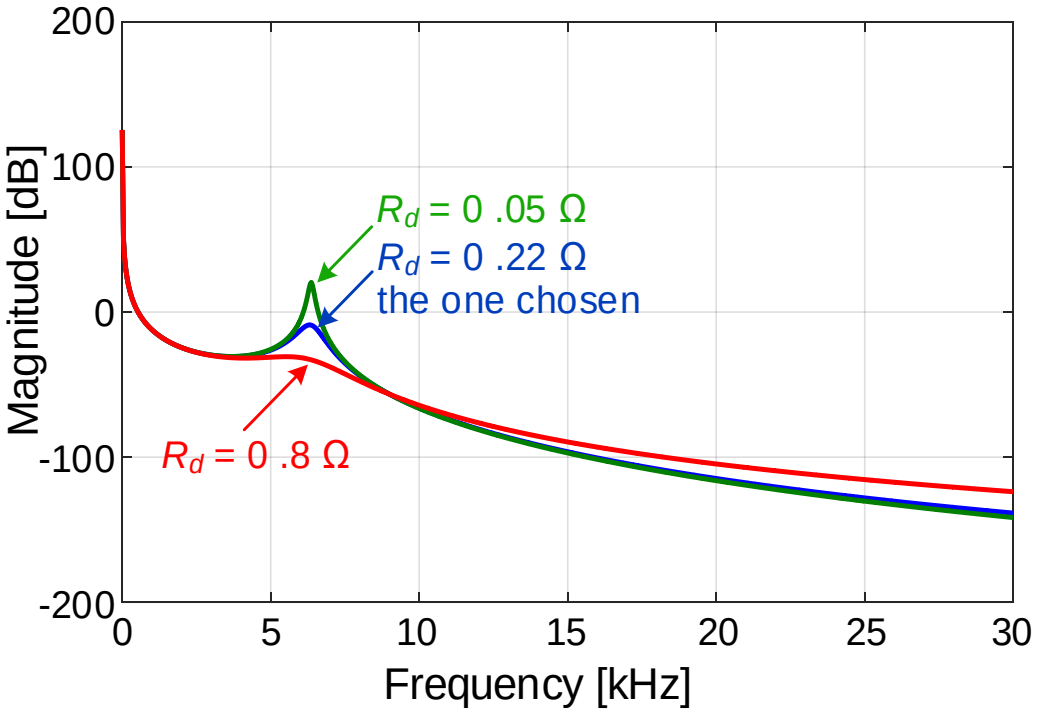



Figure 4-8: From inverter to grid transfer characteristics of selected LCL filter for various damping resistor values

For the colored line which $R_d$ is 0.8Ω, filter resonance frequency amplification is properly damped, but filter attenuation value is reduced because of excessive damping of filter. Because of this, further increase of damping resistor value makes switching harmonics significant. Also, loss of damping resistor is relatively high for this value. In the case of selecting damping resistor value as 0.05Ω, transfer characteristics of LCL filter is as green colored line. Attenuation of high order harmonics is almost the same with the un-damped filter, but at resonance frequency, damping of amplification is not enough. For $R_d$= 0.22Ω, damping of amplification

at resonance frequency is enough, since magnitude is under 0 dB, also attenuation at the switching frequency does not change significantly. So that value of damping resistor, $R_d$ selected as 0.22Ω.

In order to compare designed LCL filter transfer characteristics, in terms of inverter to grid and grid to inverter, for both transfer functions, LCL filter transfer characteristic are plotted as is can be seen in Fig. 4-9.

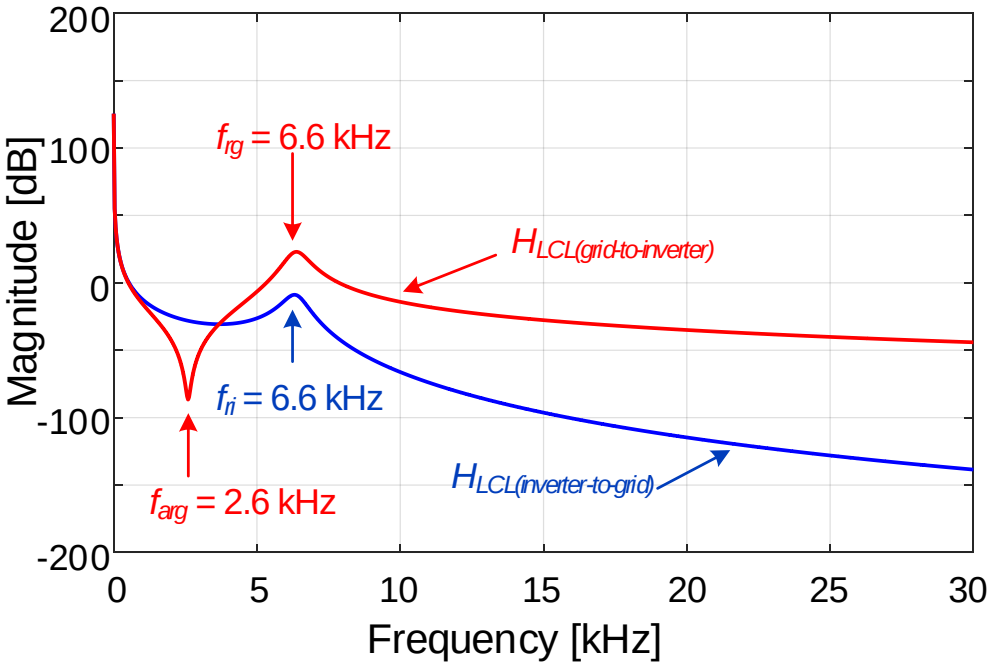



Figure 4-9: From inverter to grid (blue) and from grid to inverter (red) transfer characteristics of designed LCL

As it can be seen in Fig. 4-8, for grid to inverter transfer characteristic of LCL filter, line forms a dip and a peak as stated earlier and resonance frequency of boosting is the same resonance frequency with inverter to grid transfer function resonance frequency.

### 4.6. Power Loss Calculation of Three Phase inverter

As switching power semiconductor, Cree CCS050M12CM2 part numbered, six-pack SiC MOSFET module, which can be seen in Fig. 4-10, is used in the power circuitry of three-phase grid connected inverter [34].


Figure 4-10: Cree CCS050M12CM2 six-pack SiC MOSFET module

Features of MOSFET module, such as 0.025 Ω low $R_{DS(on)}$, zero reverse recovery current, ease of cooling and low turn-on/off losses have been effective in selection of switching component.

In order to find inverter losses, whose large portion is composed of semiconductor conduction loss, switching loss, LCL filter copper losses and LCL filter core losses, loss calculations made in this section is done according to manufacturer application notes [35] and verified with calculation tools such as Wolfspeed SpeedFit design simulation software [36].

Since the maximum power harvesting from PV installation is limited and maximum reached output power of the inverter is 22.3 kW, theoretical loss calculations made up to 22.3 kW output power, in order to compare theoretical and experimental efficiencies.

### 4.6.1. Conduction Loss Calculation

Instantaneous conduction loss of MOSFET is calculated by the multiplication of instantaneous current flowing through MOSFET and voltage drop on MOSFET according to the MOSFET on state resistance and current value. Although on state resistance of the CCS050M12CM2 MOSFET module is given as 0.025 Ω, according to the amount of current flowing through and junction temperature, minor changes can occur. Because of that in conduction loss calculations $I_{DS}$ vs. $V_{DS}$ curve will be used as given in Fig. 4-11.

Since the current flowing through MOSFET is accepted as sinusoidal, conduction loss of MOSFET, $P_{Mcond}$ can be derived as;

$$P_{Mcond} = I_{Npeak} \times V_{DS} \times \frac{1}{2\pi}\int_{0}^{\pi} (\sin X)^2 \times \frac{1 + \sin(X + \theta) \times M}{2} dx$$
$$= I_{Npeak} \times V_{DS} \times \left(\frac{1}{8} + \frac{M}{3\pi}\cos\theta\right) \quad (4\text{-}19)$$

Where $I_{Npeak}$ is the peak value of current flowing through MOSFET, $V_{DS}$ is drain-source voltage at the peak current, M is the modulation index and cos θ is power factor value.

Since inverter cooling is efficient enough, junction temperature value is predicted as 100 °C at maximum. According to given conditions $P_{Mcond}$ per MOSFET is found as 15.24 W at 22 kW output power, for 45 A peak value of current, 1.5 V drain-source voltage $V_{DS}$ unity power factor, 0.934 modulation index and 20 V gate-source voltage, $V_{GS}$ .

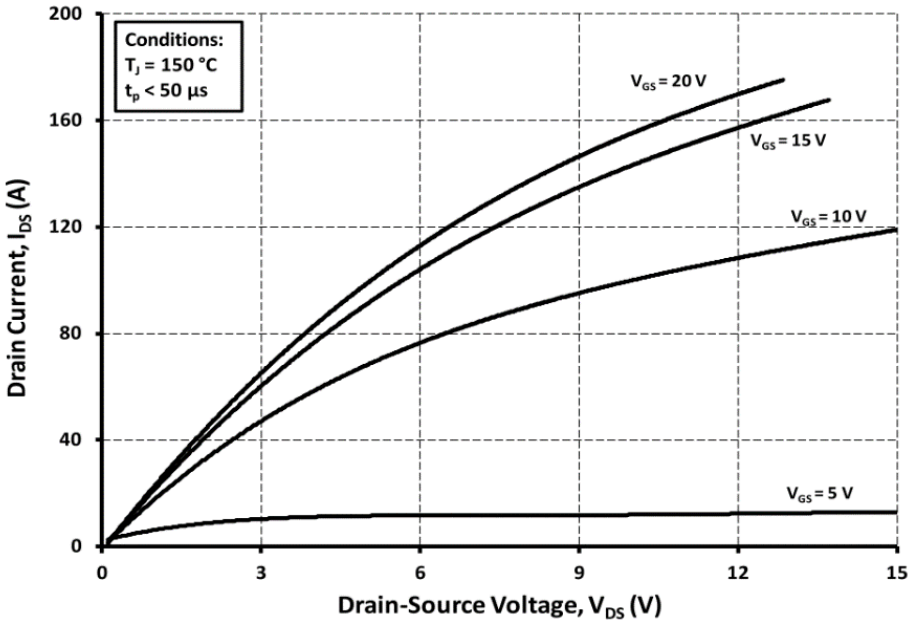



Figure 4-11: Drain current, IDS, versus drain-source voltage, VDS curve of CCS050M12CM2 [34]

Body diode conduction losses can be calculated as;

$$P_{Dcond} = I_{Npeak} \times V_{AC} \times \left(\frac{1}{8} - \frac{M}{3\pi}\cos\theta\right) \quad (4\text{-}20)$$

Where $V_{AC}$ is the diode forward voltage drop, anode-cathode voltage, and $I_{Npeak}$ is the maximum current value flowing through body diode.

Body diode conduction loss, $P_{Dcond}$ is calculated as 2.33 W per diode according to conditions for 22 kW output power, 45 A peak value of current, 2 V anode-cathode voltage, $V_{AC}$ as unity power factor, 0.934 modulation index.

MOSFET and body diode conduction loss calculations are made for output powers at 2, 3.5, 5, 7, 10, 15 and 22 kW, which will be shown in total theoretical efficiency section.

### 4.6.2. Switching Loss Calculation

Switching loss occurs during turn-on and turn-off transitions of the MOSFET, as shown Fig. 4-12. In order to get for low switching loss, rise and fall times during transition should be low. For 20/-2 V gate-source voltage, 3.8 Ω gate resistance rise time and fall time are 30 and 18 ns respectively, which is far quicker with respect to commercial IGBTs at the same power rating.

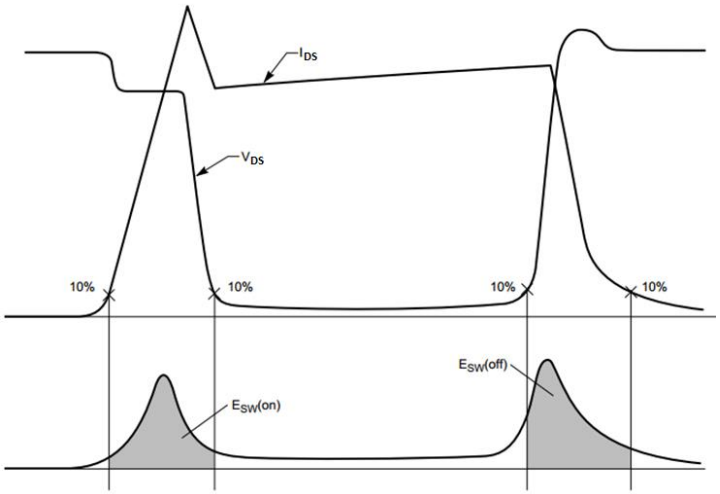



Figure 4-12: Switching loss during turn-on and turn-off transitions of MOSFET [19]

Change of turn-on and turn-off switching energy with respect to drain-source current given in Fig. 4-13, in conditions of gate resistance, $R_G$ is 20 Ω, gate-source voltage, $V_{GS}$ +20/-5 V and DC link voltage is 600 V.

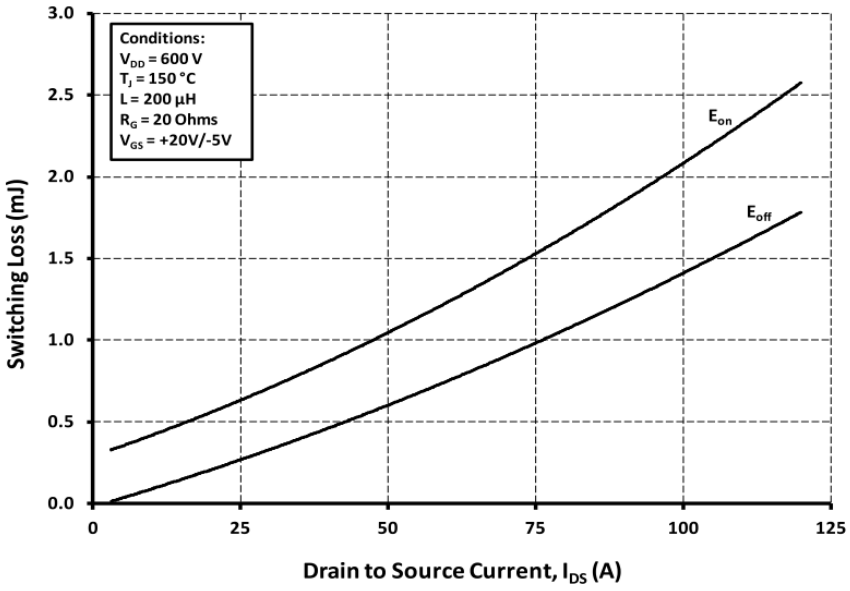



Figure 4-13: Change of turn-on and turn-off switching energy with respect to drain-source current [34]

In order to calculate switching losses, necessary equation given as;

$$P_{SW} = (E_{SW(ON)} + E_{SW(OFF)}) \times f_{SW} \frac{1}{2\pi} \int_0^{\pi} \sin x \, dx = (E_{SW(ON)} + E_{SW(OFF)}) \times f_{SW} \frac{1}{\pi} \quad (4\text{-}21)$$

Where $E_{SW(ON)}$ is the turn-on switching energy, $E_{SW(OFF)}$ is the turn-off switching energy and $f_{SW}$ is the switching frequency.

For 600 V $V_{DS}$, 50 A $I_{DS}$, 20/-5 V gate-source voltage, and 20 Ω gate resistor, $E_{SW(ON)}$ and $E_{SW(OFF)}$ are given 1.1 mJ and 0.6 mJ respectively. Since gate resistor used in design is 10 Ω, turn-on and turn-off transitions are quicker, so that switching energies are lower. According to the used gate resistance, 700 V DC link voltage and 45 A drain-source current, $E_{SW(ON)}$ and $E_{SW(OFF)}$ values are recalculated and found as 0.82 and 0.45 respectively. According to these values, $P_{SW}$ calculated as 8.08 W per MOSFET for 22 kW output power. For output power of 2, 3.5, 5, 7, 10, 15 and 22 kW, switching power losses calculated which will be shown in efficiency section.

### 4.6.3. Output Filter Implementation and Loss Calculation

In order to construct converter side inductor, $L_c$, 0078337A7 part numbered Magnetics brand X-Flux family powder toroid core is used [37]. Number of turns of the core, to reach desired value of inductance which is 250 uH, can be calculated as;

$$L_c = A_L \times N^2 \quad (4\text{-}22)$$

Where $L_c$ is inductance of converter side inductor, $A_L$ is the inductance factor per square-turn and N is the number of turns.

For a given $A_L$ value of 68 nH/$N^2$, number of turns is calculated as 61 turns for 250 uH inductance. By using 6 $mm^2$ cross-section cable, at maximum output power of 22 kW, copper losses, $P_{copp}$ calculated as 9.66 W per inductor. For 10 A peak-to-peak switching current ripple superimposed on 31 A RMS fundamental frequency

current at 22 kW output power, core loss, $P_{core}$ calculated as 6.55 W per inductor, using and Magnetics Inductor Design Tool [38]. Copper loss calculations are made for power outputs from 2 kW to 22 kW, but core loss for the inductor is almost constant for all power ranges since switching current ripple is constant and fundamental current contribution on core loss is negligible.

For grid side inductor T225-40 part numbered Micrometals brand iron powder toroid core is used [39]. For a given $A_L$ value of 87 nH/N$^2$, necessary number of turns is calculated as 24 turn for 50 uH inductance. Since number of turns is not many and core outer diameter is 58 mm, copper loss in winding is negligible. Also, due to the attenuation of switching ripple current on converter side inductance and filtering capacitor, switching ripple current on $L_g$ is too low either. So that, loss component resulting from grid side inductor, $L_g$ is not taken into consideration.

For the filtering capacitor, $C_f$, MKP1848S61510JY5F part numbered, VISHAY brand, metal film capacitors used, due to high ripple current capacity and long life time. Implemented LCL filter can be seen in Fig. 4-14.

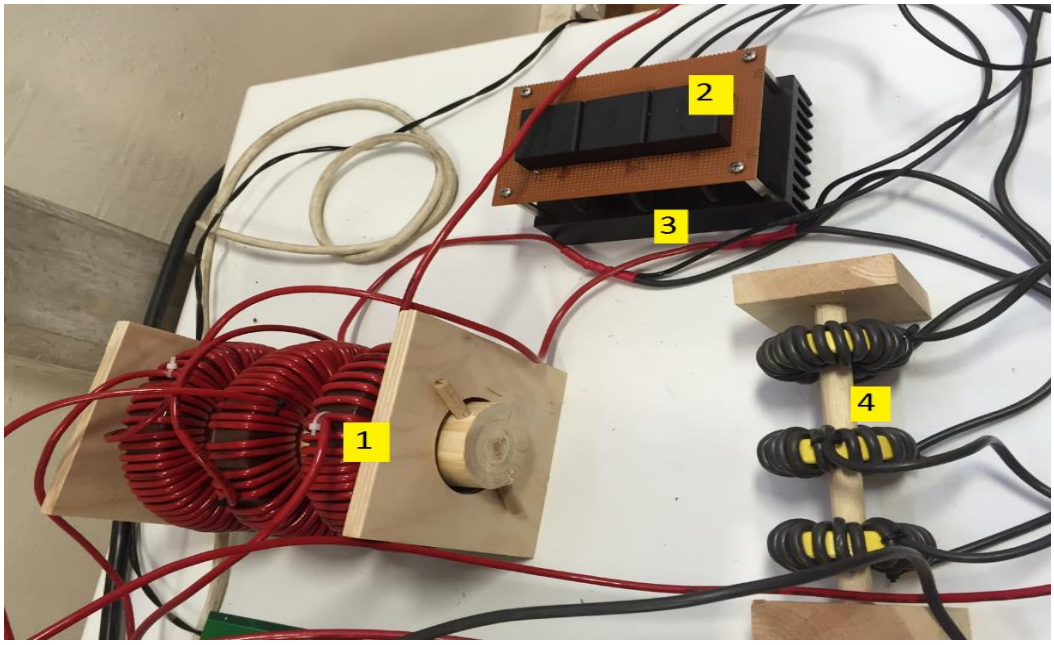



Figure 4-14 Implemented LCL filter 1: $L_c$=250 uH 2: $C_f$=10 uF 3: $R_d$=0.22Ω mounted on heatsink 4: $L_g$=50 uH

### 4.6.4. Total Theoretical Efficiency

According to calculation methods, which are explained in the previous sections, MOSFET switching losses, $P_{SW}$, MOSFET conduction losses, $P_{Mcond}$, body diode conduction losses, $P_{Dcond}$, filter copper losses, $P_{copp}$, filter core losses, $P_{core}$, total loss, $P_{total}$, and efficiency values are calculated for output powers, $P_o$ from 2 kW to 22 kW as can be seen in Table 4-1.

Table 4-1: Change of losses and efficiency for output power from 2 kW to 22 kW

| $P_o$, kW | $P_{SW}$, W | $P_{Mcond}$, W | $P_{Dcond}$, W | $P_{copp}$, W | $P_{core}$, W | $P_{total}$, W | Efficiency, η-100,% |
|---|---|---|---|---|---|---|---|
| 2 | 4.41 | 0.75 | 1.27 | 0.49 | 19.65 | 26.57 | 0.987 |
| 3,5 | 7.72 | 2.31 | 2.22 | 1.49 | 19.65 | 33.40 | 0.991 |
| 5 | 11.03 | 4.72 | 3.18 | 3.05 | 19.65 | 41.63 | 0.992 |
| 7 | 15.44 | 9.25 | 4.45 | 5.98 | 19.65 | 54.77 | 0.992 |
| 10 | 22.06 | 18.89 | 6.35 | 12.20 | 19.65 | 79.15 | 0.992 |
| 15 | 33.09 | 42.51 | 9.53 | 27.45 | 19.65 | 132.23 | 0.991 |
| 22 | 48.53 | 91.45 | 13.98 | 59.04 | 19.65 | 232.65 | 0.990 |

According to these results, change of theoretical efficiency for different output powers can be seen in Fig. 4-15.

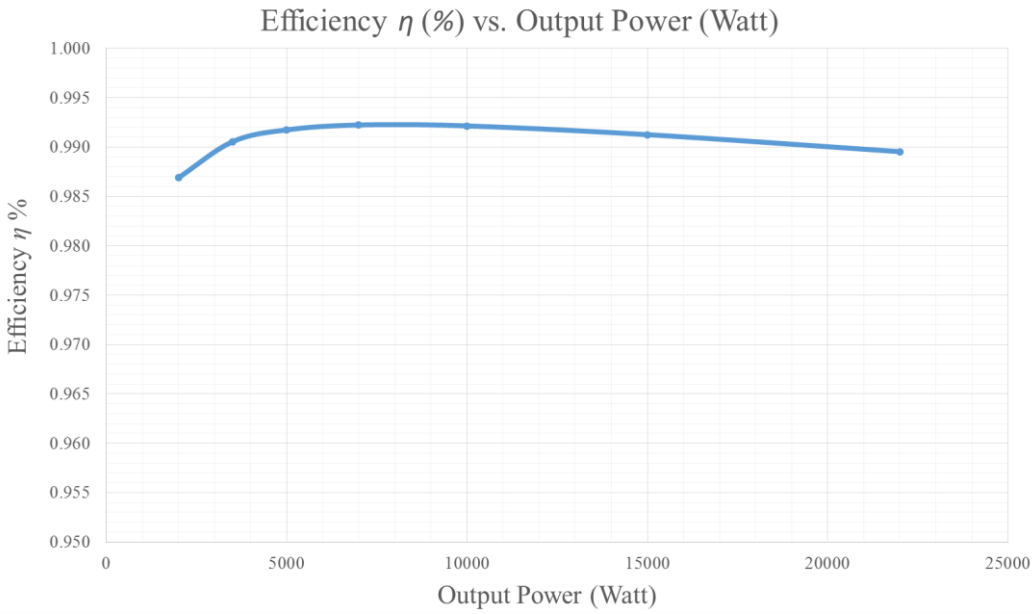



Figure 4-15: Plot of theoretical Efficiency (%) vs. Output Power (Watt) curve

By considering these calculations and design outputs, it is observable that inverter efficiency is 99.2% at its peak value at half load, which is 10 kW. Change of efficiency is very smooth from 5 kW output power to 22 kW output power and above 99% efficiency value, and from half load to full load decrease in the efficiency is about 0.1%.

### 4.7. Design of Controller, Interface Board, and Power Plane

For the three-phase inverter implementation, two PCB has been designed and implemented, which are interface board and power plane board. Interface board is consisting of voltage and current measurement circuits, buffers and voltage regulators, while power plane board contains gate drivers, DC bus capacitors and SiC MOSFET module. As for the microcontroller and its necessary peripherals TMDSDOCK28335 part numbered Texas Instruments Experimenter kit used. Details of designed boards and controller design are elaborated in the related sections. Power stage and control circuitry of all SiC three-phase grid connected voltage source two level inverter is given in Fig. 4-16.

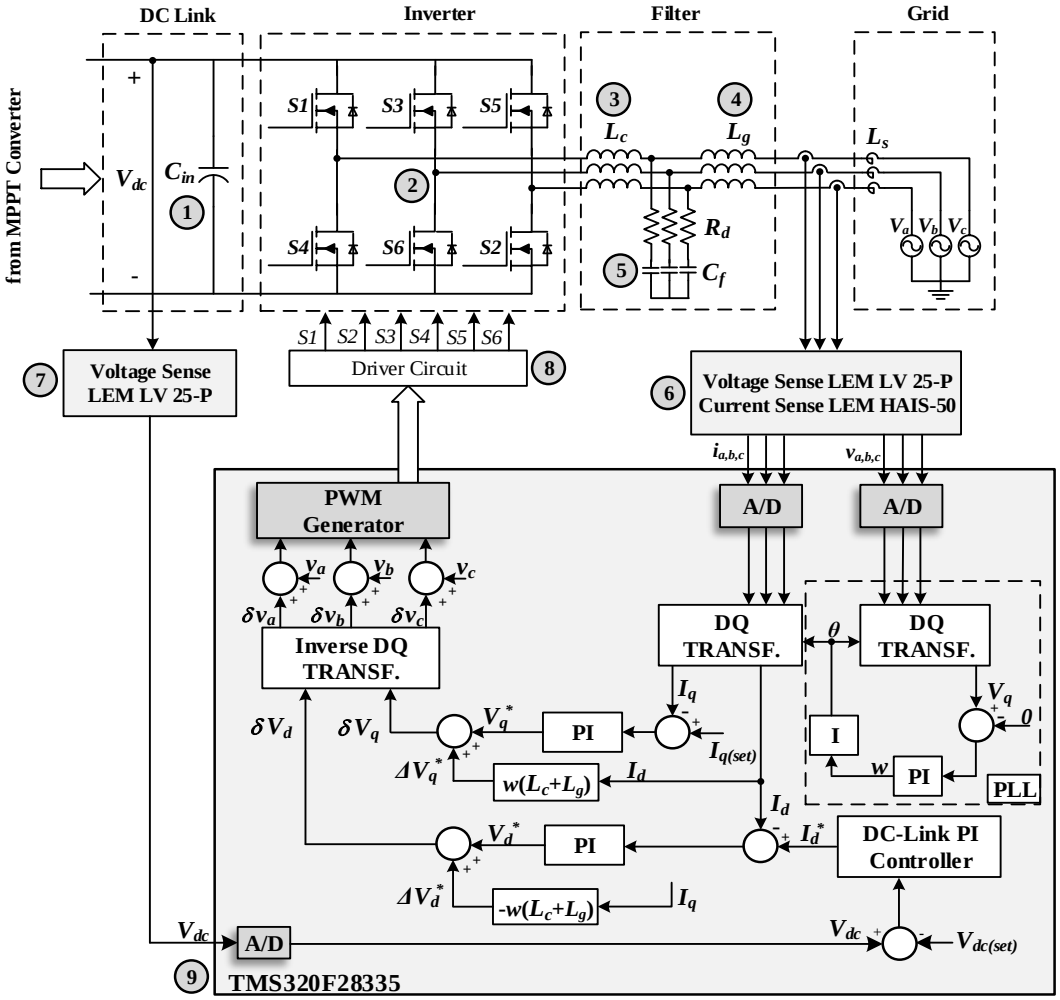



Figure 4-16: Power stage and control circuitry of all SiC three-phase grid connected voltage source two-level inverter [5]

Numbered notifications in Fig 4-15 can be elaborated respectively as 1: Metal Film 12x40 µF Input Capacitor Bank (VISHAY MKP1848640094Y), 2: All-SiC Six-Pack Three-Phase Module (CREE CCS050M12CM2), 3-4: Lc=250 µH (Magnetics 0078337A7) and Lg = 50 µH Filter Inductor (Micrometals T225-40), 5: Metal Film 15 µF Filter Capacitor (VISHAY MKP1848S61510JY5F), 6: Hall-Effect Current Transducer (LEM HAIS 50-P), 7: Voltage Transducer (LEM LV25-P), 8: Single Channel SiC MOSFET Driver (CREE CRD-001), 9: Experimenter Kit (TI TMDSDOCK28335)

### 4.7.1. Controller Design

A slightly modified version Synchronously Rotating Reference Frame control [40], [41] is used as the control technique of three-phase grid connected voltage source inverter to control active power flow to grid, DC bus voltage regulation and other controlled parameters. Input parameters of the control software are $v_{a,b,c}$, line-to-neutral voltage measurements, $i_{a,b,c}$, line currents after LCL filter and $V_{dc}$, DC bus voltage. These input parameters are measured with hall-effect sensors and sampled at a rate of 10 kS per second by the DSP. $I_{q(set)}$ and $V_{dc(set)}$ are the reference control parameters of reactive current and DC link reference voltage respectively. Reference value of output reactive current component is set to 0 A in order to fulfil unity power factor requirement, and reference value of DC bus voltage, $V_{dc(set)}$ is set to 700 V.

In order to obtain phase angle, $\theta$ which is necessary to perform DQ transformation to line currents, synchronous reference frame PLL is used as can be seen in Fig. 4-16. DQ transformation is performed on line currents with the help of generated phase angle, $\theta$. $I_d$ and $I_q$, which are outputs of DQ transformation of line currents, are controllable DC quantities and active and reactive components of output current respectively.

Subtraction of reference DC bus voltage, $V_{dc(set)}$ from measured DC bus voltage, $V_{dc}$, goes into DC-link PI controller as error signal. Output of DC-link PI controller is the reference d-axis current component $I_d^*$, and subtraction of measured $I_d$ from $I_d^*$ gives the current error, which goes into PI controller for current loop control. Output of this PI controller is the d-axis voltage reference, $V_d^*$. The inverse DQ transformation of d-axis voltage reference output is in the same phase with the $v_{a,b,c}$, phase-to-neutral voltages. So that, increase in the $V_d^*$ reference voltage means increase in the output voltage waveform magnitude. According to that, to set an example, if power of PV installation increases, to increase output power MPPT output voltage increases, hence, DC bus voltage increases. In order to keep DC bus voltage at the reference value, which is 700 V DC, $I_d$ current reference value increases too to transfer more active power to grid. With positive error signal, $V_d^*$ reference increases, but, only output voltage magnitude increases and this situation almost only changes reactive power flow to grid according to single line diagram of

three-phase inverter. As the reactive power increases, measured reactive component of the output current, $I_q$ will become non-zero and system starts to work in non-unity power factor mode. $I_q$ is subtracted from reference q-axis current component, $I_q^*$, which is 0, and goes into PI controller. Output of the PI controller is the q-axis voltage reference, $V_q^*$, and increase of $V_q^*$ results in phase change in the leading direction. So that, with the change of phase degree, active power increases and inverter output becomes unity power factor. As it can be understood, inverter control loop controls output active power indirectly.

Current loop control also enables attenuation low order harmonics. Since DQ transformation of 50 Hz fundamental current component are DC quantities, and DQ transformation of low order harmonics, such as $5^{th}$ and $7^{th}$, occurs as AC oscillations on $I_d$ and $I_q$, current control loop compensates and attenuates these AC oscillations to some point, and tries to keep $I_d$ and $I_q$ as the same as reference $I_d^*$ and $I_q^*$ DC quantities.

In literature, measured voltage d-axis component, $V_d$, measured voltage axis component, $V_q$ and cross-coupling terms, which are obtained from the voltage drop on LCL filter inductors, are used as to increase the compensation capability of low order harmonics and inverter stability, during step changes of grid voltage and PV installation output voltage [42]. Grid voltage contains low order harmonics mainly $3^{rd}$, $5^{th}$ and $7^{th}$, and according to single line diagram of three phase inverter, just like 50 Hz fundamental diagram, these voltage harmonics results in current flow for the specified voltage harmonics according to LCL filter impedance and voltage difference between inverter output voltage and grid voltage. In order to prevent low order current harmonics, voltage difference between inverter output voltage and grid voltage for the specified harmonic order, must be kept minimum if possible zero. In order to do that, measured grid voltage is superimposed to switching reference voltage as inversely proportional to DC bus voltage, aimed to generate the same grid voltage at the inverter output voltage, except necessary changes to control active and reactive power flow. Another advantage of this implementation is that in the case of a step change or distortion in the grid voltage, inverter output voltage directly

responds this change, even without the need for PI controller's outputs to change, since grid voltage is feed-forwarded.

In this design, instead of feed-forwarding the components of $V_d$ and $V_q$ feed-forwarding terms of $v_a$, $v_b$ and $v_c$ are used, due to the following advantages. When feed-forwarding terms of $V_d$ and $V_q$ are used, during DQ transformation zero sequence term is lost, and grid voltage cannot be generated at the inverter output completely. Also during DQ and inverse DQ transformation, data can be corrupted slightly. In addition to that, there is no need to generate grid voltage through DQ and inverse DQ transformation once again since grid voltages already measured. It is nothing but extra processing time for the micro-controller.

Whole control algorithm has been implemented on TMS320F28335 DSP Texas Instruments Experimenter Kit in Code Composer Studio, using C based programming software. Used micro-controller board can be seen in Fig. 4-17.

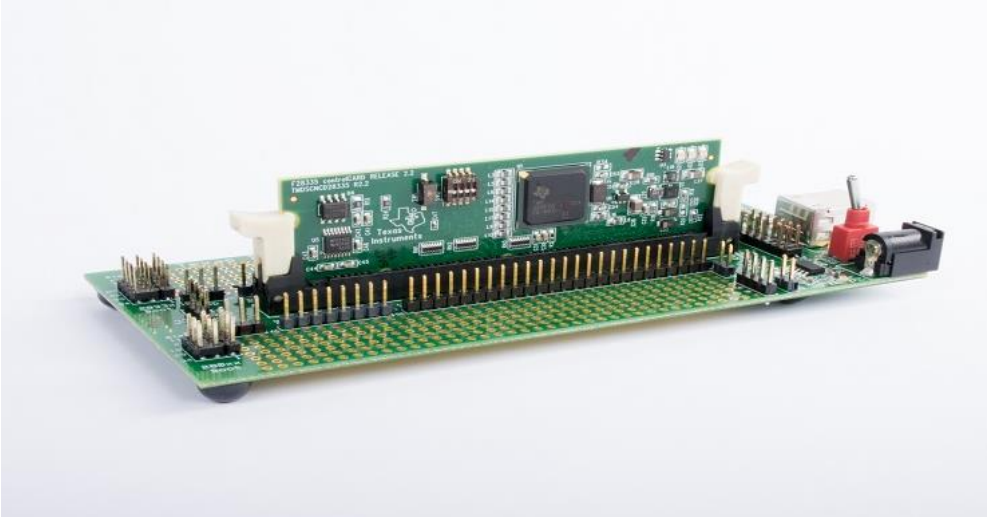


Figure 4-17: TMS320F28335 Experimenter Kit

Control loop start and PWM cycle update time instance in synchronization with PWM switching time period is given in Fig. 4-18. Start of ADC sampling of voltage and current measurements and control loop calculation is at the time that carrier signal reaches its maximum value, in order to use the newly calculated PWM duty

cycles at the next PWM switching period. This method results in better performance, since phase delay between implementation time and calculation time of PWM duty cycle is minimized.

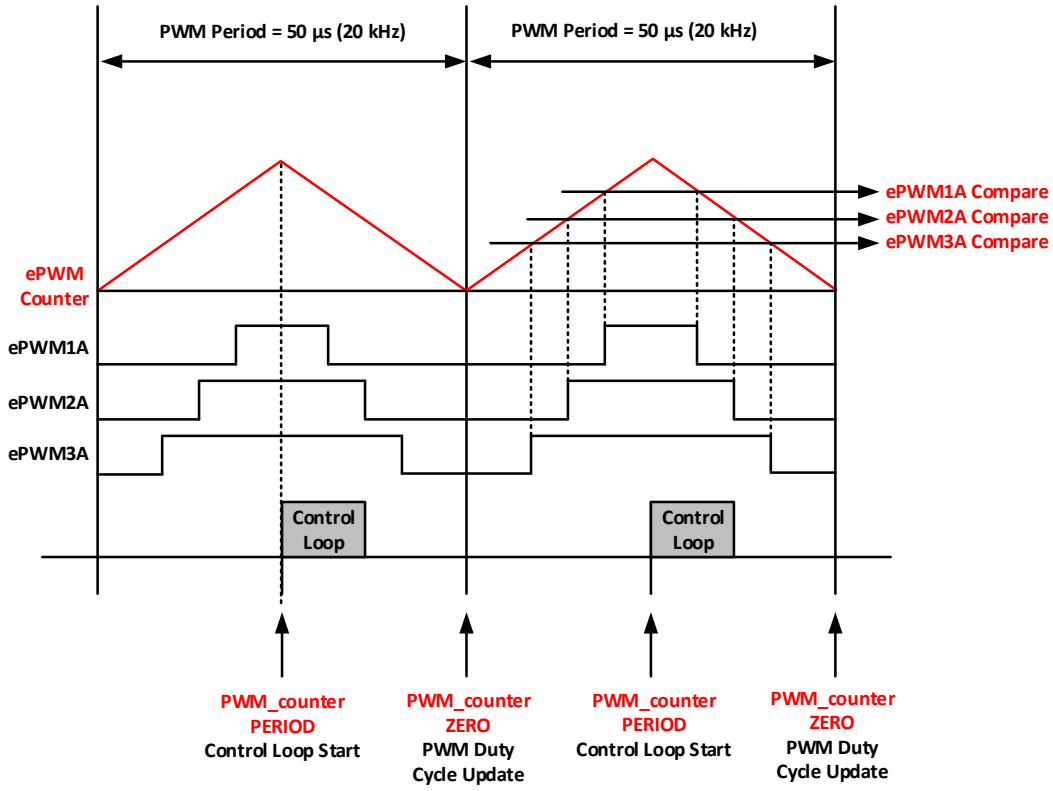



Figure 4-18: Control loop, PWM duty cycle update synchronization in PWM period

### 4.7.2. Interface Board Design

In order to perform measurements, such as DC bus voltage, $V_{dc}$, line currents $i_{a,b,c}$, and line-to-neutral voltages $v_{a,b,c}$, which are necessary for control software, interface board has been implemented. These measurements are scaled to the limits between 0-3V, which is microcontroller ADC measurement interval, and connected with TMS320F28335 Experimenter Kit jumper cables. For all measurements, isolated hall-effect sensors are used to perform. In addition to measurement circuitry, interface board is responsible for delivering gate drive signals to gate drivers through buffers, since TMS320F28335 PWM output signals are not capable of delivering

enough current necessary for gate drivers. For current measurements, hall-effect sensors LEM HAIS 50-P are used with inner voltage reference. These current measurements are then scaled, according to DSP analog-to-digital converter, ADC interface, which accepts 0-3 V. So that, AC signal measurement circuitry outputs are 1.5 V at zero current flowing, in order to utilize maximum range of ADC interface. A total of four-piece hall-effect sensors are used, three of them are for line currents and one of them is for DC bus current, in order to do MPP tracking if the MPPT is done by inverter in future work. For voltage measurements, LEM LV 25-P hall-effect voltage measurement sensors are used, as a total of four pieces again. Three of them are used for line-to-neutral voltage measurements and one of them is used for DC bus voltage measurement. Designed PCB of interface board can be seen in Fig. 4-19.

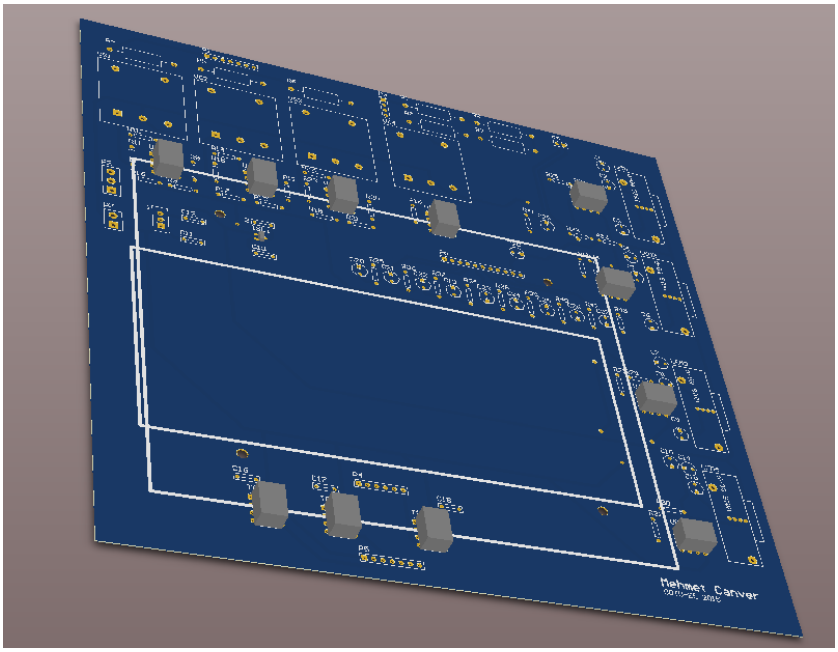


Figure 4-19: Designed PCB of interface board

Interface board has been implemented on a 2-layer PCB with a 1 oz of copper. For both of PCBs, which are the interface board and power plane board, Altium Designer (14.3) PCB design software environment is used.

### 4.7.3. Power Plane Board Design

For mounting of SiC module, DC bus capacitors and gate drivers of SiC MOSFET module, a power plane PCB board has been designed. As stated earlier a total 12 pieces of 40 uF metal film capacitors are used as DC bus capacitor of the three-phase inverter. Inductance resulting from capacitors' ESL value and power plane parasitic inductance must be as low as possible, in order to prevent voltage spikes caused from switching. Because of that, low ESL value metal film capacitors are used. Since CCS050M12CM2 has two DC bus voltage entrance, and MOSFET half-bridges are distributed in the module, DC bus capacitors are spited in two parts as it can be seen in Fig. 4-20. So that, each MOSFET in the module encounters almost the same parasitic inductance.

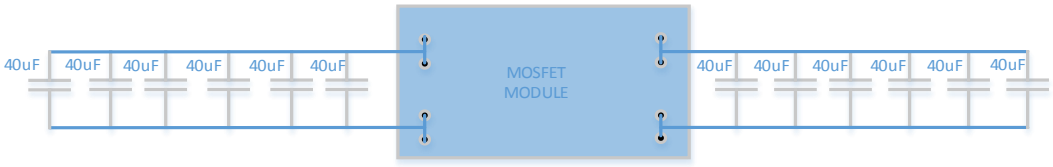



Figure 4-20: Placement of DC bus capacitors around the SiC MOSFET module

Also, in order to reduce the parasitic inductance in the power plane, VDC+ and VDC- power planes are poured at the same size and at the same place of the board, as VDC+ is the bottom layer with blue color and VDC- is the top layer with red layer color, as it can be seen in Fig. 4-21. Thereby, there is no loop between VDC+ and VDC- planes to create parasitic inductance, except the distance between top layer and bottom layer which is too small. Field experiments showed that power plane design is successful, in terms of voltage spikes and parasitic inductance.

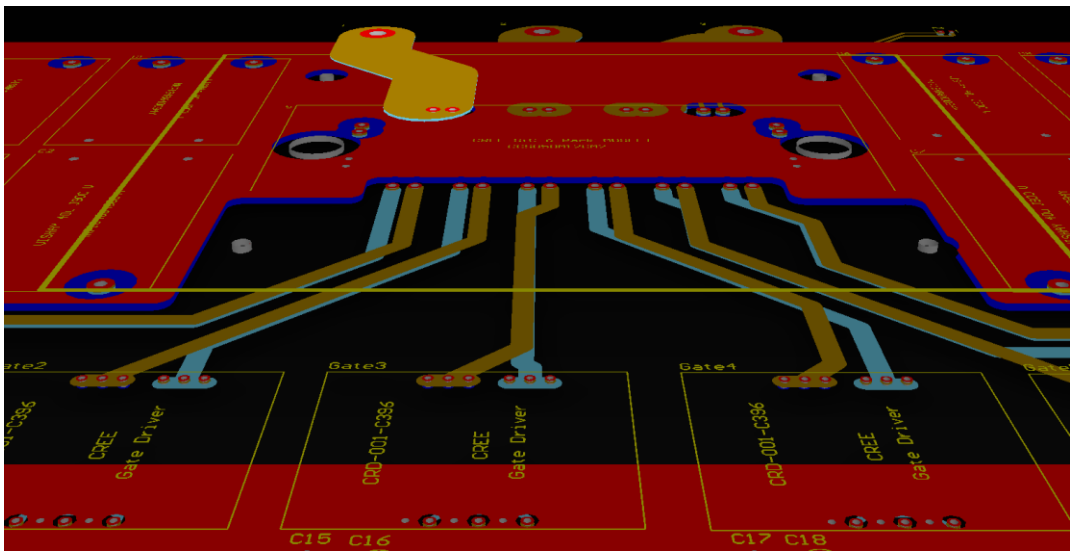



Figure 4-21: Power plane board routing view in 3-D color by layer

For gate driver of SiC MOSFET module, CRD-001 isolated SiC MOSFET gate drivers are used, as it can be seen in Fig. 4-22. There are two isolated unregulated 1 W DC/DC converter on each of them, and in the case of 10 V supply voltage for gate drivers, MOSFETs are driven by +20V/-5 V turn on and off voltages, which are selected for gate drive voltages, in order to get minimum on state resistance for MOSFETs. Gate driver output resistance is selected as 10 Ω.

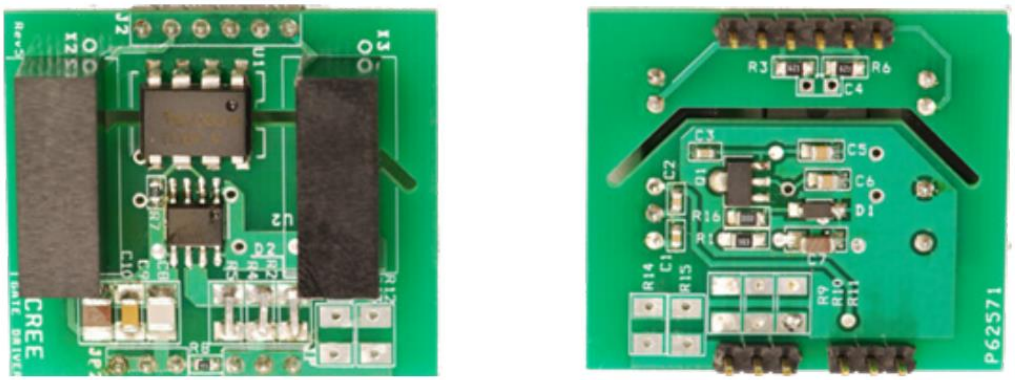



Figure 4-22: CRD-001 isolated SiC MOSFET gate driver

Gate source connection of SiC module must be also carefully implemented. Parasitic inductance of gate-source loop should be kept minimum, since gate-source capacitance of MOSFET and parasitic inductance of gate source loop, form a LC circuit, and according to L and C values voltage spikes occur on gate-source voltage. As it can be seen in Fig. 4-21, routing of gate-source terminals is done according to minimize the loop. Also parasitic capacitance, caused from routing, must be minimized. Larger capacitance means larger turn on and off times of MOSFET for the same values of gate driver parameters, and causes larger switching losses. In addition to that, larger capacitance increases the load for gate drivers for the same switching frequency. Since gate driver routing goes bottom-top layers to reduce parasitic inductance, routing width must not be large, in order not to increase parasitic capacitance. 3-D view of power plane board can be seen in Fig. 4-23. Power plane board has been implemented on a 4-layer board with 3 oz copper, to reduce the power dissipation on board. While bottom and top layers are used for VDC+ and VDC- lines, mid-layers are used for three phase outputs of inverter.

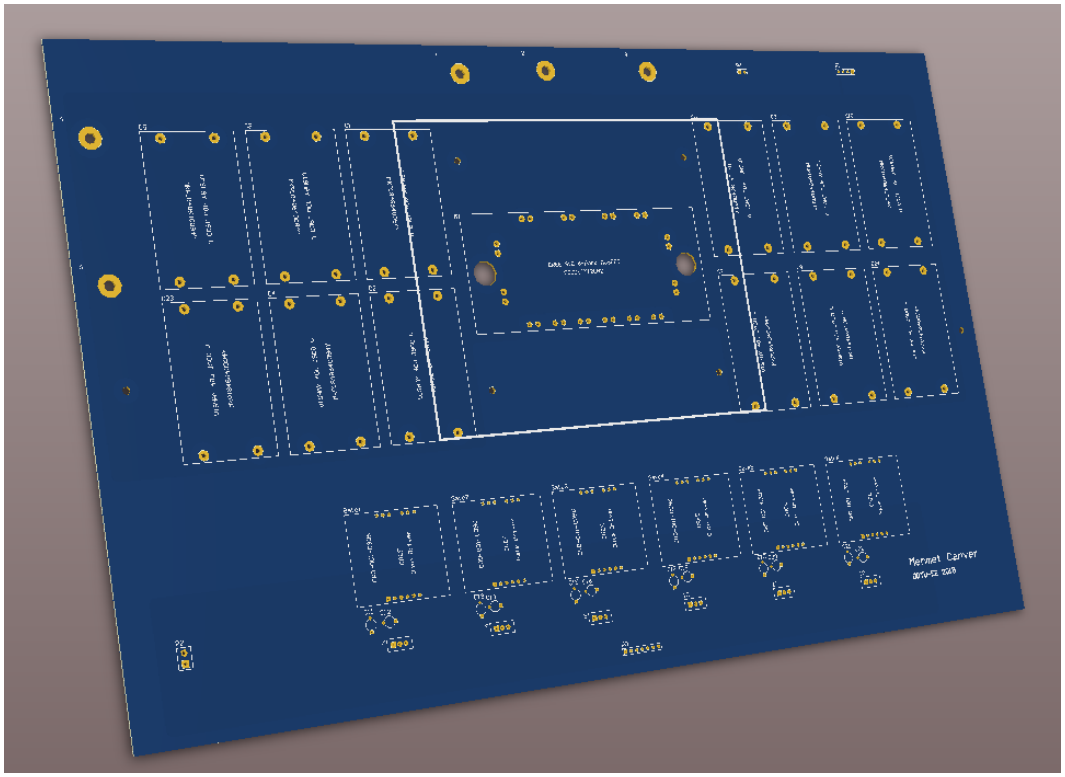


Figure 4-23: Power plane board in 3-D view

### 4.8. Heat Transfer and Heat-Sink Selection

For the SiC MOSFET module, heat transfer circuitry is given as in Fig. 4-24. Junction of SiC MOSFET can withstand temperatures up to 150°C. According to heat transfer circuitry, MOSFET losses and module total loss, the necessary heatsink parameters are found.

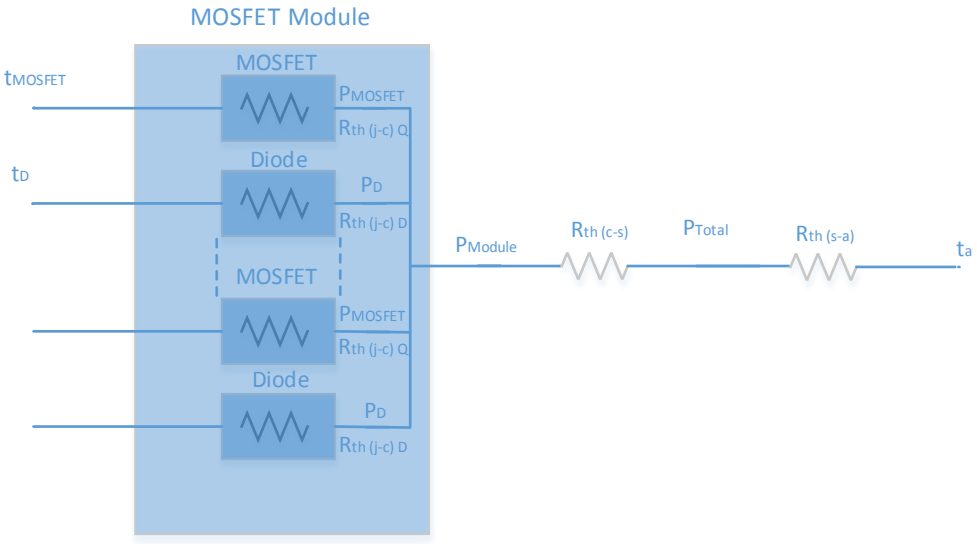



Figure 4-24: Heat transfer circuitry of SiC MOSFET module

Junction temperature of SiC MOSFET module can be found according to the following equation.

$$t_{MOSFET} = P_{MOSFET} \times R_{th\,(j-c)Q} + P_{TOTAL} \times R_{th\,(c-s)} + P_{Total} \times R_{th\,(s-a)} + t_a \quad (4\text{-}23)$$

Where $t_{MOSFET}$ is the junction temperature of SiC MOSFET module, $P_{MOSFET}$ is the individual MOSFET loss, $R_{th(j-c)Q}$ is the junction-to-case thermal resistance of MOSFET, $P_{TOTAL}$ is total loss of SiC MOSFET module, $R_{th(c-s)}$ is the thermal resistance between module enclosure and heatsink, $t_a$ is the ambient temperature, $R_{th(s-a)}$ is the thermal resistance between heatsink and ambient and finally $P_{Total}$ is the total power loss of components mounted on heatsink, which is in this case equal to $P_{TOTAL}$, since MOSFET module is the only component mounted on heatsink.

As the junction temperature increases, on state resistance of MOSFETs increases too, and this condition results in increase of conduction losses. So junction temperature should be as low as possible. For maximum output power of 22 kW, $P_{MOSFET}$= 23.3W, $P_{TOTAL}$= 154 W, $t_{MOSFET}$=100°C, $t_a$=45°C, $R_{th(j-c)Q}$= 0.37 K/W, $R_{th(c-s)}$= 0.025 K/W and $R_{th(s-a)}$ is calculated as 0.27 K/W. But to be in the safe side, LA17 FISHER brand heatsink with 150 mm heatsink length and 230 V AC fan has been selected. Thermal resistance vs. heatsink length graph of LA17 is given in Fig. 4-25. According to this graph for 1500 mm length heatsink thermal resistance is given as 0.1 K/W and this results in 73°C junction temperature.

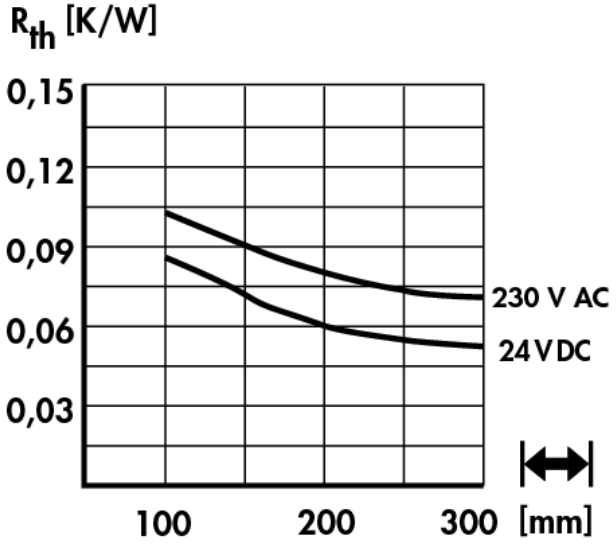



Figure 4-25: LA17 230 V AC heatsink thermal resistance vs. heatsink length graph [43]

# CHAPTER 5

# EXPERIMENTAL RESULTS OF THREE PHASE GRID CONNECTED INVERTER

## 5.1. Introduction

In this chapter experimental results of 3-phase 400 V line-to-line RMS grid connected SiC MOSFET PV inverter, whose design procedure is shown in the previous chapters, is examined. For the experimental setup and grid connection, infrastructure of Middle East Technical University Electrical and Electronics Department, Electromechanical Energy Conversion (EMEC) Laboratory is used. PV module installation on the rooftop of EMEC Laboratory is used as power source of the inverter. A total of 95 CSUN255-60P modules with five parallel strings consisting of 19 series modules, constituting 23.75 kW at 1000 W/m$^2$ solar irradiation and 25°C, are used. PV module installation can be seen in Fig. 5-1.

Figure 5-1: PV module installation as power source

For the protection precautions and other necessary cabling, a junction box is used as it can be seen in Fig. 5-2. DC+ and DC- cables for each string goes through 10 A fuses for over current protection. In order prevent current flowing from one string to another string, diodes are used for each string. For the lightning protection of PV modules, a voltage surge arrestor has been used. And to connect and disconnect PV array, 80 A rated current capacity DC disconnecter is used.

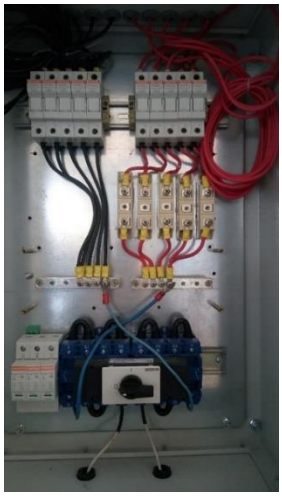


Figure 5-2: Junction box for PV strings

In this chapter active and reactive power transferring to grid, current and voltage waveforms, individual current harmonics and total harmonic distortion at various powers will be shown. For these purposes HIOKI PW3198 Power Quality Analyzer is used with current probes 9661 clamp on sensors which has current measurement range up to 500 A AC. For high frequency current waveforms, such as the switching current transitions through SiC MOSFETs, CWT06 ultra mini Rogowski coils, which has a 120 A peak current measurement capability and 34 Hz-30 MHz frequency bandwidth, are used. Since DC current measurements cannot be taken with Rogowski coils, Tektronix TCP404XL current probe and Tektronix TCPA300 current probe amplifier is used. In order to measure voltages on switching device and other voltages, Tektronix P5205A high voltage differential probes are used, and to record all current and voltage measurement waveforms Tektronix MSO3034

oscilloscope, 4-channel 300 MHz bandwith with a sampling rate of 2.5 GSPS, is used.

For efficiency measurements and to energize the PV inverter without PV array, MAGNA Power TS series, which has 0-800 V DC voltage output range and up to 24 A current output capability, programmable DC supply is used. For the efficiency measurements, input power is measured from DC supply, while output power is measured from HIOKI power analyzer.

List of measurement devices used in this research work is given in Table 5-1.

Table 5-1: Devices used in experimental results

| |
|---|
| HIOKI PW3198 Power Quality Analyzer |
| Tektronix MSO3034 Oscilloscope |
| Tektronix TCPA300 Current Probe Amplifier |
| Tektronix TCP404XL Current Probe |
| Tektronix P5205A High Voltage Differential Probe |
| HIOKI 9661 Clamp On Sensors |
| MAGNA Power Programmable DC Supply (20 kW) |

## 5.2. Experimental Setup

Experimental setup and implemented three-phase grid connected inverter is shown in this section. MPPT converter, which is needed to increase the voltage level of the PV array to necessary DC bus voltage of the three phase inverter and to track maximum power point, is given in Fig. 5-3. MPPT converter is also necessary in order to reduce the common mode currents and galvanic isolation.

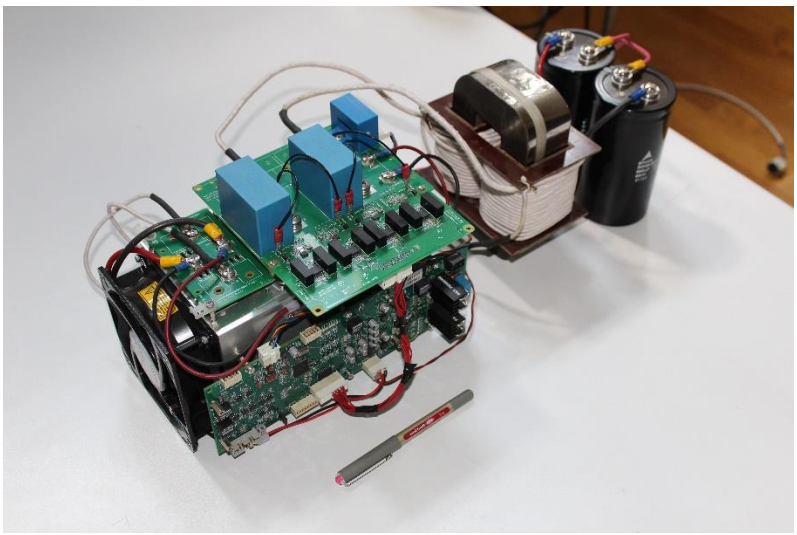
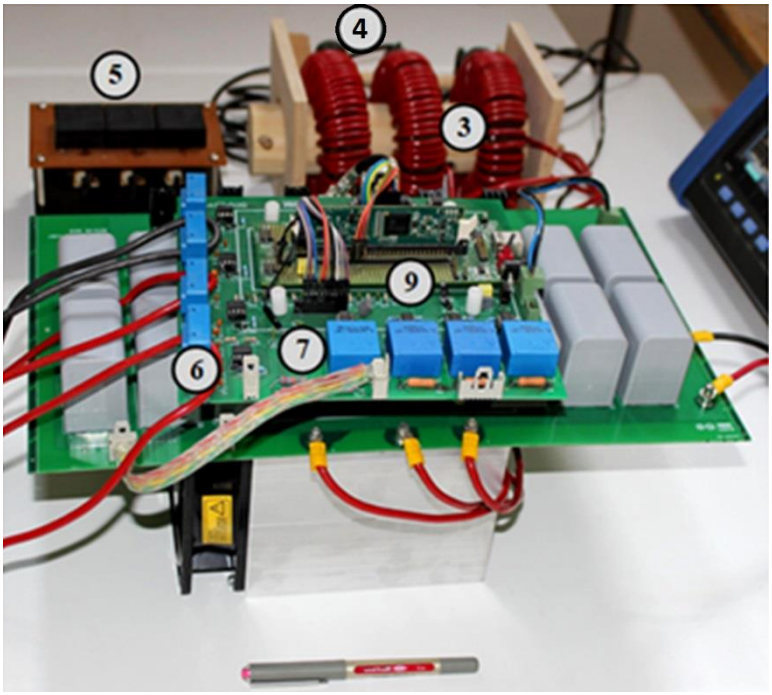


Figure 5-3: Phase-shifted full bridge MPPT converter

In all of the field tests, when transferring energy from solar arrays to three-phase grid, SiC inverter and phase-shifted full-bridge MPPT converter worked together, since three-phase inverter cannot work as single stage inverter, due to excessive common mode current occurrence when MPPT converter is not used. Implemented three-phase grid connected voltage-source inverter is given in Fig. 5-4.


(a)




(b)

Figure 5-4: (a) side and (b) top view of implemented three-phase inverter

Numbered notifications in Fig. 5-4 can be elaborated respectively as 1: Metal Film 12x40 µF Input Capacitor Bank (VISHAY MKP1848640094Y), 2: All-SiC Six-Pack Three-Phase Module (CREE CCS050M12CM2), 3-4: Lc=250 µH (Magnetics 0078337A7) and Lg = 50 µH Filter Inductor (Micrometals T225-40), 5: Metal Film 15 µF Filter Capacitor (VISHAY MKP1848S61510JY5F), 6: Hall-Effect Current Transducer (LEM HAIS 50-P), 7: Voltage Transducer (LEM LV25-P), 8: Single Channel SiC MOSFET Driver (CREE CRD-001), 9: Experimenter Kit (TI TMDSDOCK28335)

### 5.3. Grid Connection Procedure

As the first step of grid connection procedure, phase locked loop is implemented. After connecting phase voltages to phase-to-neutral voltage measurement circuitry in the correct order, phase locked loop software activated. Waveform of voltage measurement of phase-A phase-to-neutral voltage and waveform of phase angle, $\theta$ can be viewed in Fig. 5-5.

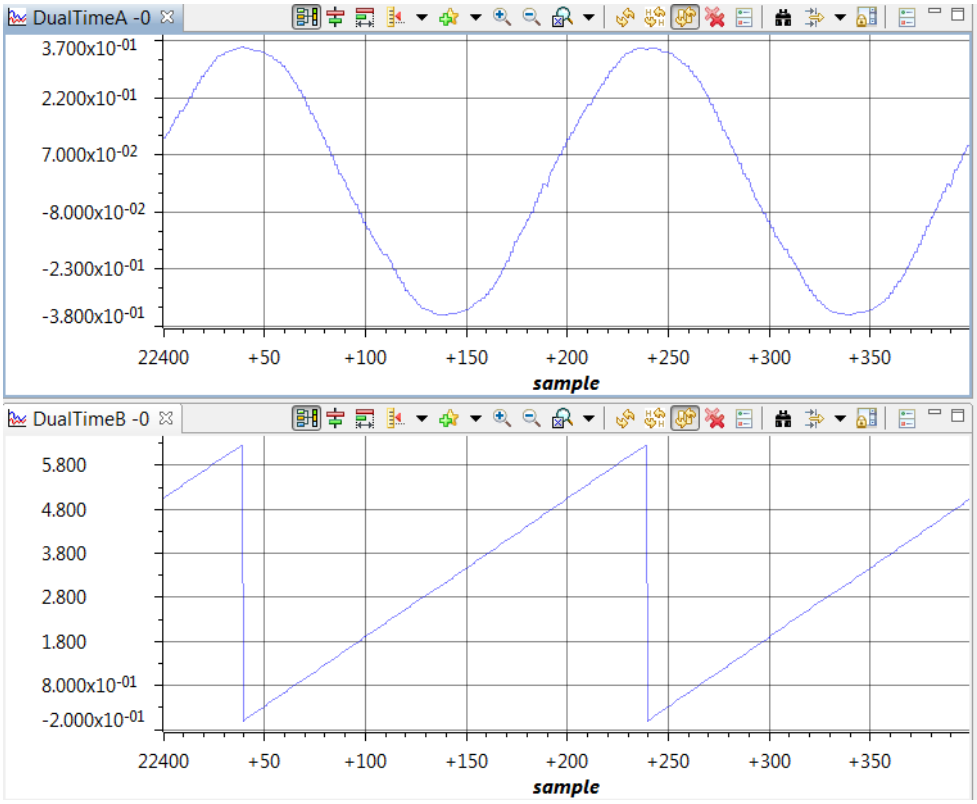
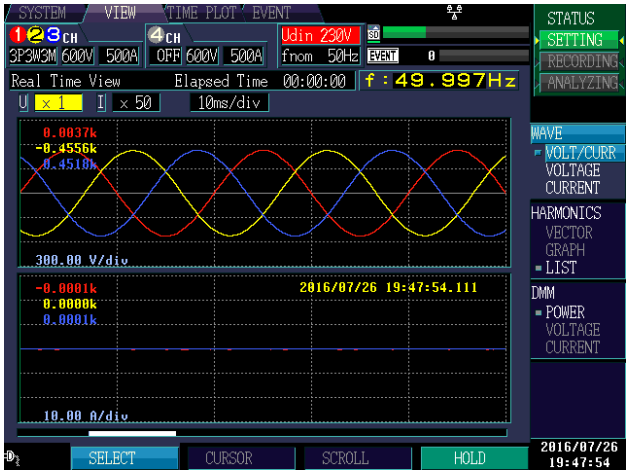



Figure 5-5: Waveform of phase-A phase-to-neutral voltage (top) and phase angle, θ (bottom)

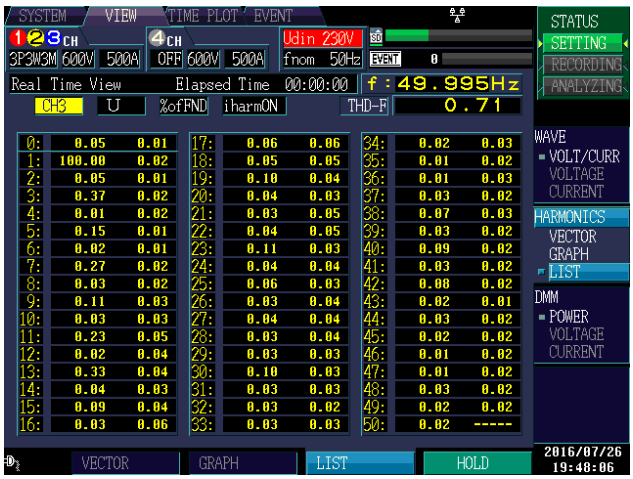
The corresponding voltage and phase angle, θ waveform is obtained using Code Composer Studio graph tool from real data. As it can be seen, phase-to-neutral voltage is directly proportional with cos(θ). Peak phase to neutral voltage measurement $V_{peak}$ cos(θ) is equal to 324cos(θ) for a 230 V AC RMS line-to-neutral voltage.

For connecting three-phase voltage source inverter to grid, a unique grid connection procedure is used in this research work. In order to reduce the excessive and uncontrolled current flow to grid at the instance of grid connection, some precautions are taken. Grid connection procedure starts with the energizing the MPPT converter by turning on the DC disconnecter between PV arrays and MPPT converter manually. If PV voltage at the input of MPPT converter is larger than 400 V DC, MPPT converter starts switching in charging mode from zero duty cycle and

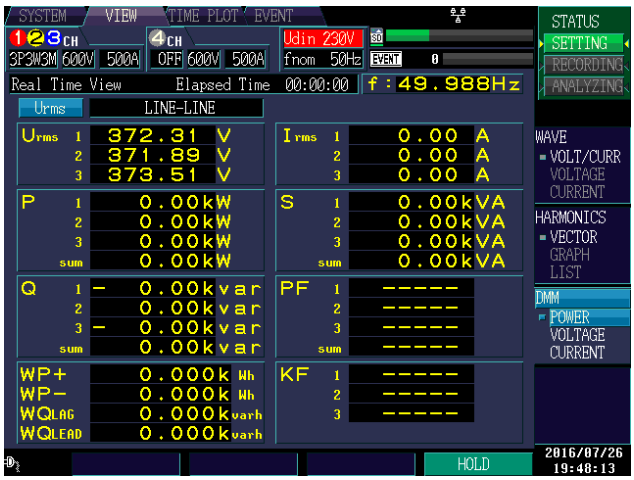
slowly increases the duty cycle, in order to rise the DC link voltage of the three phase inverter to 700 V DC, which is the fixed DC link voltage regulated by the three-phase inverter in steady state grid connected operation. Voltage source inverter starts in open loop switching mode just after DC link voltage reaches 50 V DC. Until the grid connection, three-phase inverter is in open loop mode, according to grid line-to neutral voltages. Modulation reference signal for phase-A is as $v_a/(700/2)$ for phase B is as $v_b/(700/2)$ and for phase C is as $v_c/(700/2)$, where $v_{a,b,c}$ are the instantaneous voltage measurements of line-to-neutral voltages. The purpose of this work mode is to imitate the line voltages, and when the DC link voltage reaches to 700 V DC, output line-to-neutral voltages of three phase inverter are almost the same as the grid line-to-neutral voltages including all impurities, such as voltage harmonics and unbalanced line voltages. At the open loop mode, when the DC link voltage is equal to 700 V DC, output voltage waveform, voltage harmonics, total harmonic distortion of line voltage and line-to-line voltage RMS values of three-phase inverter can be seen in Fig. 5-6. These snapshots are taken with Hioki Power Analyzer PW3138.




(a)




(b)




(c)

Figure 5-6: Snapshots of inverter output electrical quantities at open loop operation mode (a) Line-to-line voltage and line current waveforms, (b) Harmonic content of line current waveforms, and (c) Output powers.

In Fig. 5-6 (a) three-phase line-to-line voltage waveforms, which are generated at point that DC link voltage is equal to 700 V DC, are given. These waveforms are generated to imitate the grid voltage, and as it can be seen in Fig. 5-6 (b) and (c). Inverter output voltage waveforms contain impurities, which grid voltages has too, so that they contain $3^{th}$, $5^{th}$ and $7^{th}$ dominant voltage harmonics, and also line-to-line voltages are not equal as in the case of grid voltage.

Continuing with the grid connection procedure, when the DC link voltage reaches to 700 V DC, grid connection is made by three-phase switch manually. Line currents are measured constantly as 10 k samples per second, and if the one of the line

currents exceeds 5 A peak, closed loop control becomes active. But since current flow at the instant of grid connection is so low and three phase inverter does not acquire the knowledge of grid connection, closed loop control does not become active just after grid connection and DC link voltage continues to increase. This condition shows how successive is the grid connection procedure, in terms of excessive current flow at the instance of grid connection. Closed loop control can become active at the instant of grid connection, if grid connection is made by a signal controlled relay, driven by the inverter. This development can be made in future work. But since grid connection is made manually and closed loop control becomes active when current reaches 5 A peak value, DC link voltage increases due to lack of regulation. As the DC link voltage increases, inverter output voltage increases too, and at some point line current reaches to 5 A peak, when DC link voltage is equal approximately to 730 V DC. After closed loop control becomes active, DC link voltage is regulated to 700 V DC, which is a fixed value, by the three phase inverter. MPPT converter also change its mode from charging mode to MPPT mode by measuring its output current, since there is no communication interface between converters, which can be added in future. If the output current MPPT converter exceed a fixed value, MPPT converter start to operate in MPPT mode, and system operates in steady state operation mode.

### 5.4. Switching Waveforms

In this section change of MOSFET drain-source voltage and change unfiltered line current during switching will be investigated. Since six-pack MOSFET module is used as switching component, MOSFET drain-source current cannot be recorded and instead of that line current waveforms are recorded. For measuring switching transients of drain-source voltage and line current, first half-bridge leg of SiC module is used as it can be seen in Fig. 5-7.

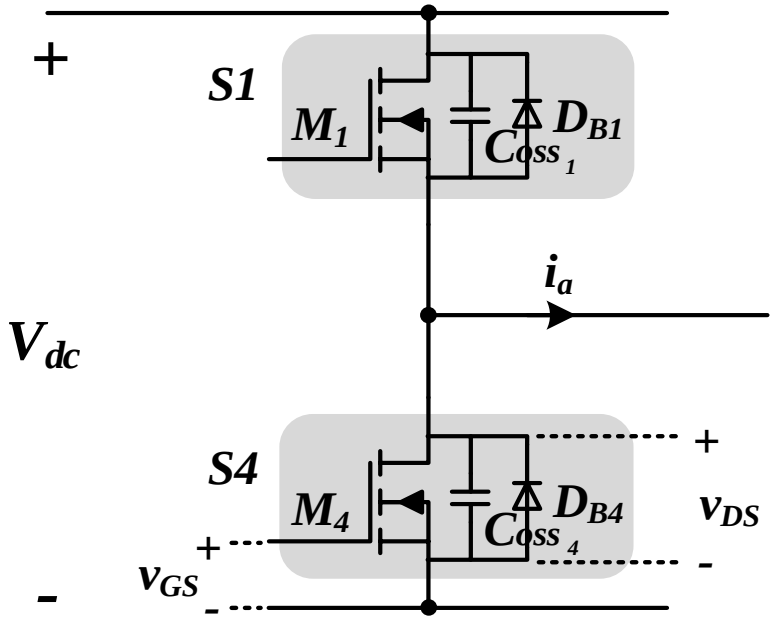



Figure 5-7: First half-bridge leg of SiC module and parasitic elements

As it can be seen in Fig. 5-7, each MOSFET in SiC MOSFET module has an output parasitic capacitance, $C_{oss}$, between drain and source terminals. During switching $C_{oss}$ charges and discharges to 700 V DC link voltage, so that when $M_1$ is on and $M_4$ is off $C_{oss4}$ is charged to 700 V DC and $C_{oss1}$ is zero volt, and when $M_1$ is off and $M_4$ is on their voltages are vice versa. Sum of voltages of $C_{oss1}$ and $C_{oss4}$ is equal to DC link voltage, which is 700 V. Effects of dead time and instantaneous load current on turn-on and turn-off characteristic are investigated in this section, for different instantaneous load currents and different dead times. Drain source voltage of $M_4$, $v_{ds4}$ and unfiltered phase-A current are recorded, during time interval between $M_4$ is turning-off and $M_1$ is turning-on, as it can be seen in Fig. 5-8. Data is recorded by MSO3034 Tektronix oscilloscope, using P5205A Tektronix high voltage differential probe, TCP404XL Tektronix current probe and TCPA300 Tektronix current probe amplifier.

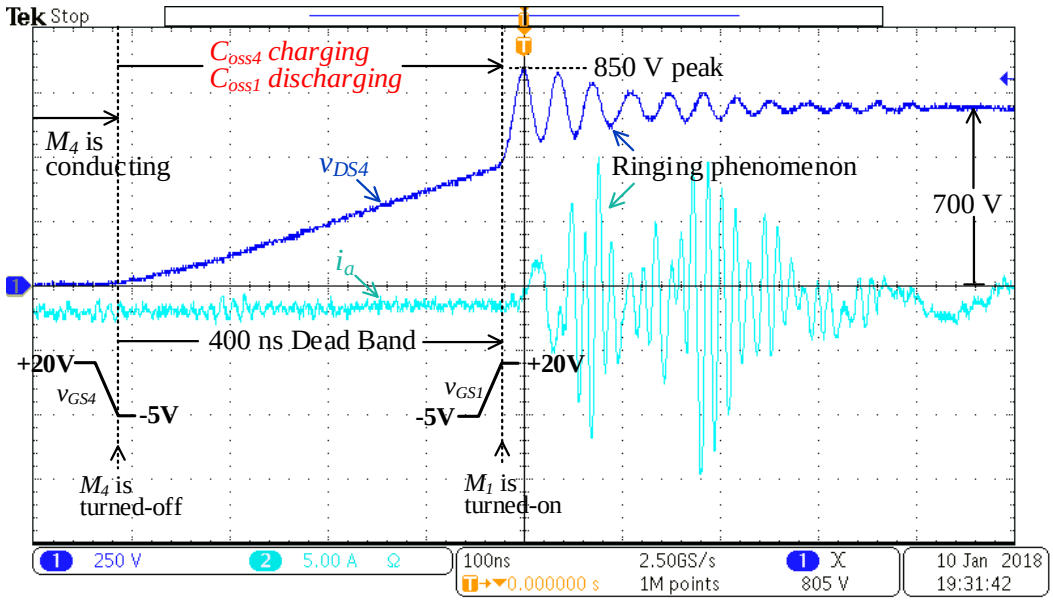



Figure 5-8:Drain-source voltage of $M_4$ and unfiltered negative phase-A line current waveform at switching transient of $M_4$ turning-off $M_1$ turning-on for 2 A phase current and 400 ns dead time

If the switching waveforms in Fig. 5-8 should be explained, until the instant of gate-source voltage of $M_4$, $v_{GS4}$ goes from +20 V to -5V, line current $i_a$ goes through $M_4$. As it can be understood from waveforms, instantaneous line current is negative, which means current flows from grid to three-phase inverter. After $v_{GS4}$ become -5V, $M_4$ stops conducting, but since the line current flows through the filter inductance and filter inductance has a stored energy on it, current flow tries to preserve its present amount and direction. Because of the stored energy on filter inductance, $i_a$ continues to flow and start to charge the parasitic capacitance of $M_4$, $C_{oss4}$, and discharge the parasitic capacitance of $M_1$, $C_{oss1}$. This charging and discharging state, resulting from stored energy on filter inductance, continues until end of dead time, or voltage on parasitic capacitance reaches to DC link voltage, or stored energy on inductance finishes and $i_a$ becomes zero. Since the sum of voltages on parasitic capacitances $C_{oss1}$ and $C_{oss4}$ is equal to DC link voltage, when the voltage of $C_{oss4}$ becomes 700 V, $C_{oss1}$ becomes full discharged. If this condition becomes before dead time ends, $i_a$ current flows through the body diode of discharged MOSFET, which is $M_4$ in this case. If $i_a$ cannot charge $M_4$ parasitic capacitance,

$C_{oss4}$ to DC link voltage, before $M_1$ opens, at the instance when $M_1$ opens, sum of leakage inductance of DC link capacitances and inductance of power plane forms a resonant circuitry with parasitic capacitances of $M_1$ and $M_4$. If the difference between charging capacitor voltage and DC link voltage is a large amount, the voltage oscillation becomes larger, since the leakage inductance will be charged to a higher current and hence it charges parasitic capacitance to a higher voltage value. As it can be seen in Fig. 5-8, parasitic capacitance, $C_{oss4}$ cannot be charged to 700 V DC link voltage, and as a result at the instance when $v_{GS1}$ voltage goes from -5V to +20 V and $M_1$ opens, $C_{oss4}$ charged through DC link leakage inductance and ringing occurs.

Since sum of voltages of parasitic capacitances on the same half-bridge is equal to DC link voltage, if ringing occurs on one of the MOSFET, ringing occur on the other MOSFET either. So that, if the voltage on the parasitic capacitance of MOSFET which is going to be turned-on, is not completely discharged to zero volt, ringing occurs at the instant when MOSFET is turned-on. For positive $i_a$ current switching transition and change of $v_{DS4}$ is given in Fig. 5-9.

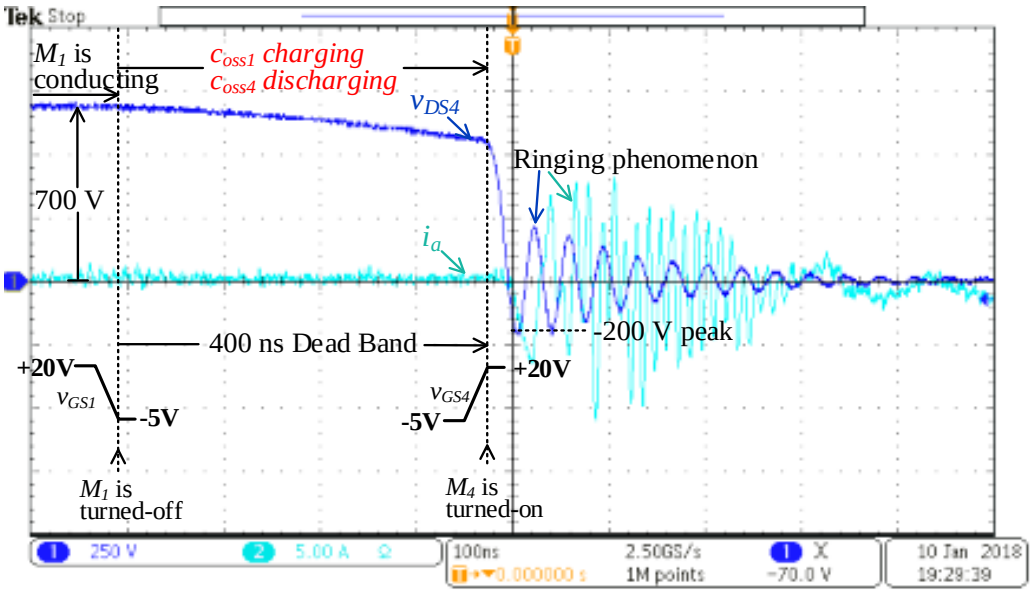



Figure 5-9: Drain-source voltage of $M_1$ and unfiltered positive phase-A line current waveform at switching transient of $M_4$ turning-off $M_1$ turning-on for 1 A phase current and 400 ns dead time

As it can be seen in Fig. 5-9, $i_a$ is positive in this case, flowing from three-phase inverter to grid. Until the instant of $v_{GS1}$ going from +20 V to -5 V, $i_a$ current flows through $M_1$ and $v_{DS1}$ is equal to zero volt, while $M_4$ is in the off state and $v_{DS4}$ is equal to 700 V DC link voltage. After $M_1$ is turned-off, $i_a$ current continues to flow in the same direction and start to discharge $C_{oss4}$ and charge $C_{oss1}$ until the end of dead time and turn-on instant of $M_4$. Since $C_{oss4}$ is not fully discharged at the end of dead time, with turn-on of $M_1$, parasitic capacitance $C_{oss4}$ is discharged through leakage inductance of DC link and ringing occurs. Phase current $i_a$ is lower than the case in Fig. 5-8 so capacitor charge and discharge current is lower during dead time and as a result ringing is higher in Fig. 5-9. Since minimum voltage due the ringing is -200 V on $M_4$, peak voltage on $M_1$ can be deduced as 900 V at the ringing instant.

For higher phase currents charge and discharge process of parasitic capacitances can be completed in dead time as can be seen in Fig. 5-10. For 400 ns dead time and for current $i_a$ in Fig. 5-10, voltage of parasitic output capacitance of $M_4$ reaches to DC link voltage value, before end of dead time. Since $i_a$ is a negative quantity current flowing from grid to three phase inverter, after $C_{oss4}$ charges to 700 V and $C_{oss1}$ discharges completely, $i_a$ flows through body diode of $M_1$, $D_{B1}$, due to the fact that both MOSFETs in the half-bridge are closed. On time of $D_{B1}$ continues until the turn-on instant of $M_1$.

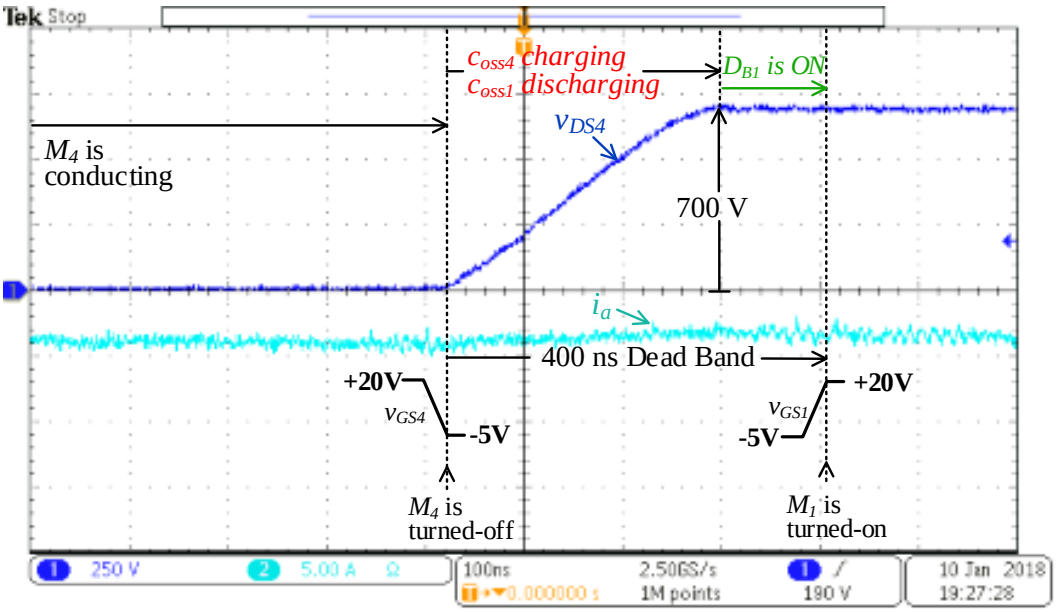



Figure 5-10: Drain-source voltage of $M_4$ and unfiltered negative phase-A line current waveform at switching transient of $M_4$ turning-off $M_1$ turning-on for 4 A phase current and 400 ns dead time

For the cases of which $C_{oss4}$ is fully discharged at the instant of turning-on of $M_1$, no switching losses occurs during turning-on of $M_1$. This situation is also called as zero voltage switching, ZVS. ZVS is a desirable phenomenon since it lowers the switching losses and increases efficiency. As it can be seen in previous figures, ZVS condition is depended upon phase current quantity and dead time. If the phase current is high, output parasitic capacitance charge and discharge process is quicker and conditions can fulfil ZVS requirements before the end of dead time. But phase current quantity is dependent to power flow to grid, so that it is not modifiable. For the same phase current, ZVS conditions can be fulfilled by increasing the dead time, hence that gives more time for the process of charging and discharging. By increasing dead time from 400 ns to 700 ns, switching waveform are recorded as can be seen in Fig. 5-11 and Fig. 5-12. In Fig 5-11, for 1 A instantaneous phase current ZVS condition is almost fulfilled and peak voltage due to ringing is 780 V while for the case in Fig. 5-8 peak voltage is 850 V, even if the phase current is 2 A.

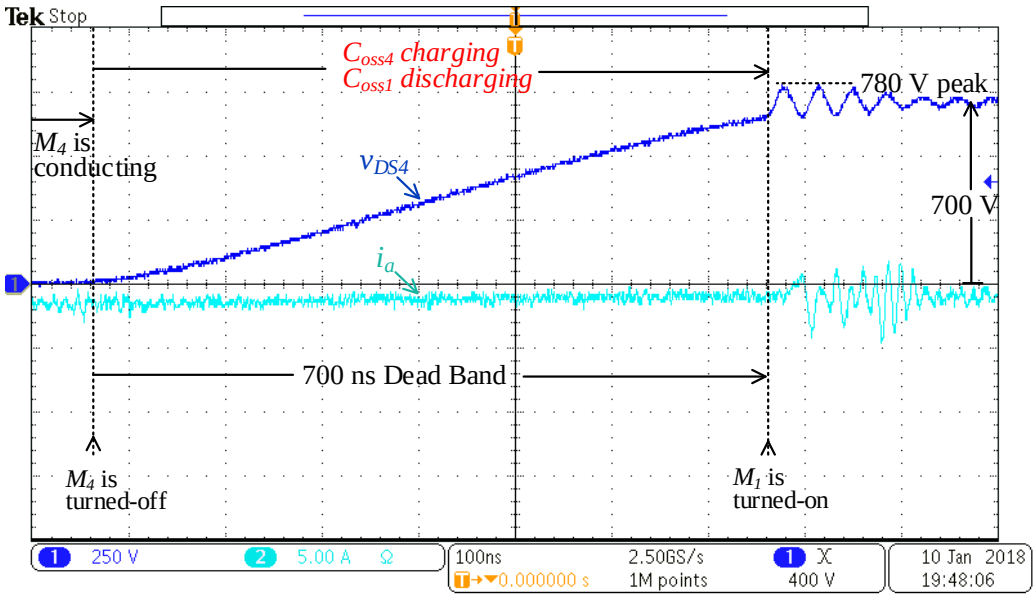



Figure 5-11: Drain-source voltage of $M_4$ and unfiltered negative phase-A line current waveform at switching transient of $M_4$ turning-off $M_1$ turning-on for 1 A phase current and 700 ns dead time

For 2 A instantaneous phase current like the same current quantity in Fig 5.8, $C_{oss4}$ is charged to 700 V and $C_{oss1}$ is fully discharged, and zero voltage switching occurs for turning-on of $M_1$ as it can be seen in Fig. 5-12, since dead time is increased to 700 ns. Increasing dead time may be useful in terms of switching losses, but high dead time has unfavorable effects on current harmonic content of phase current, such as increase of low order harmonics [44].

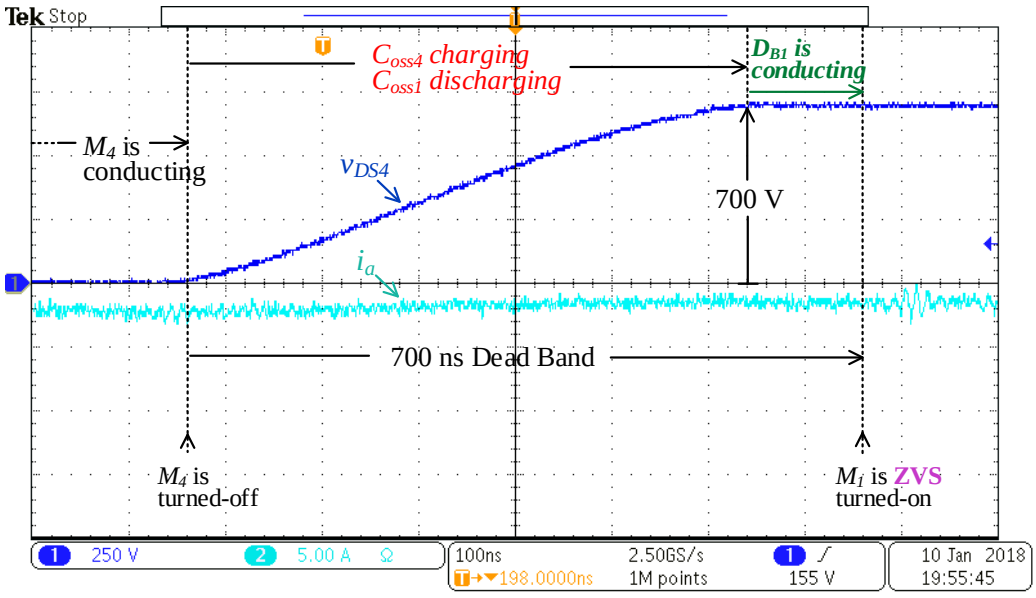



Figure 5-12: Drain-source voltage of $M_4$ and unfiltered negative phase-A line current waveform at switching transient of $M_4$ turning-off $M_1$ turning-on for 2 A phase current and 700 ns dead time

### 5.5. Harmonic Analysis

For grid connected operation of three-phase voltage source inverter, several current waveforms recorded at different output powers. During field tests, a maximum of 22.3 kW output power has been reached. Total voltage harmonic distortion, THDv of connected grid is recorded as ≅ 1.4%, according to harmonic measurement method IEC61000-4-7:2002 [45]. Especially $5^{th}$ and $7^{th}$ harmonics are dominant in the harmonic spectrum, and this condition also creates current harmonics at the same harmonic order. For total harmonic distortion measurements, active and reactive power measurements, power factor measurements and voltage and current waveform records, HIOKI Power Analyzer PW3198 is used, which can measure harmonic spectrum up to $50^{th}$ harmonic. But since three-phase inverter switching frequency is 20 kHz, in order to record switching current ripple Tektronix TCP404XL current probe is used with Tektronix TCPA300 current probe amplifier. Current waveform recording is done with Tektronix MSO3034 oscilloscope. For 22.3 kW peak output power, phase current waveforms on the inverter side inductor and on the grid side inductor can be seen in Fig. 5-13.

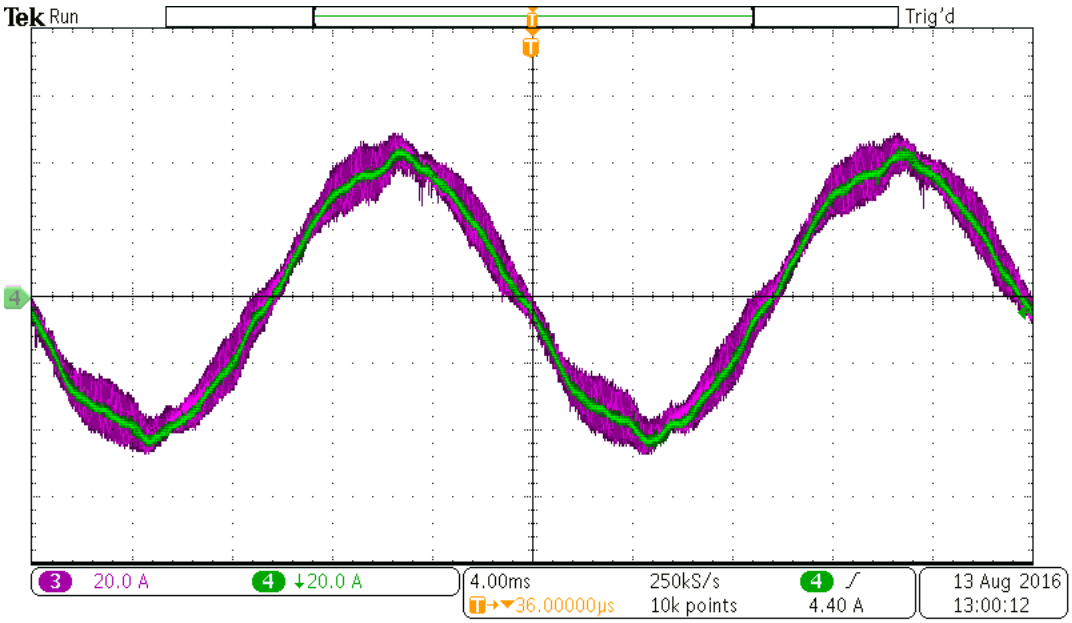



Figure 5-13: Phase current waveforms on the inverter side inductor (purple) and on the grid side inductor (green) at 22.3 kW output power

A detailed view of phase current waveforms at 22.3 kW output power is also given in Fig. 5-14. As it can be seen in Fig. 5-13 peak to peak current ripple on the inverter side inductor, at switching frequency is about 25% of fundamental frequency current component as intended. For the current waveform on the grid side inductor, switching frequency current harmonic is almost completely filtered with the designed LCL filter parameters.

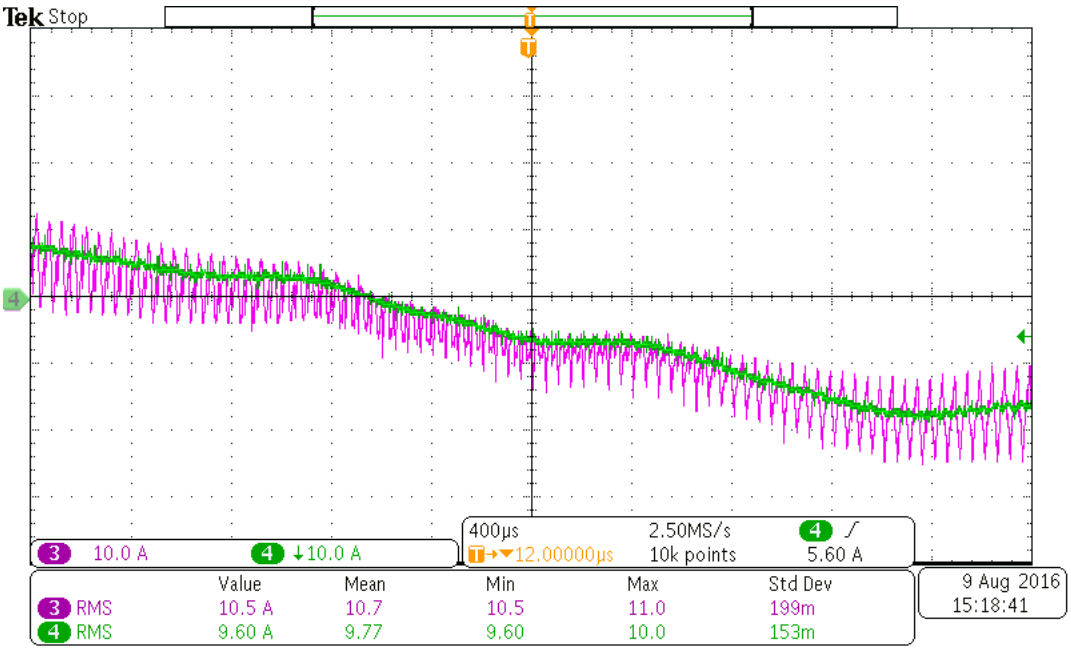



Figure 5-14: Detailed view of phase current waveforms on the inverter side inductor (purple) and on the grid side inductor (green) at 22.3 kW output power

In order to find the magnitude of switching frequency current harmonic as a percentage of fundamental frequency current component, output current waveform data in Fig 5-13 has been recorded and processed in MATLAB. As it can be seen in Fig. 5-15 switching frequency harmonics magnitude is 0.6% of fundamental frequency current component.

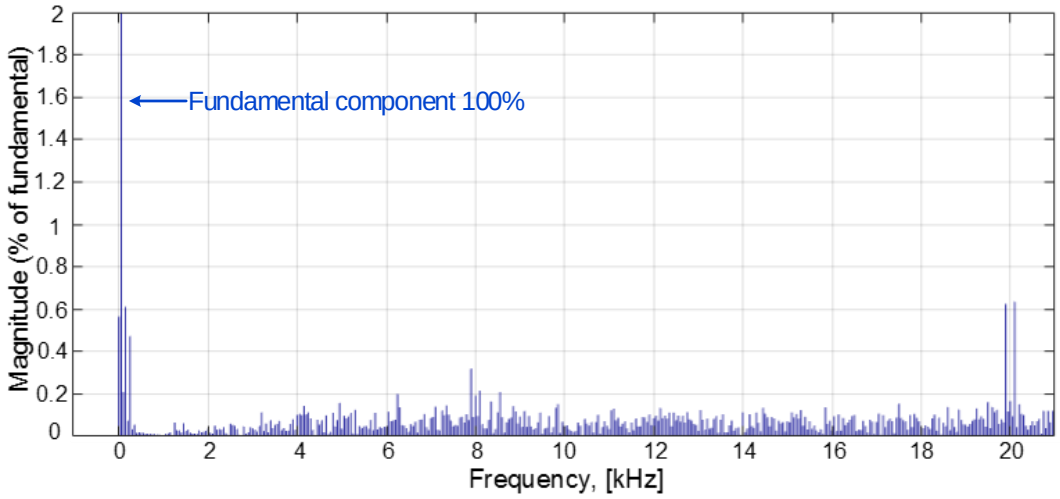
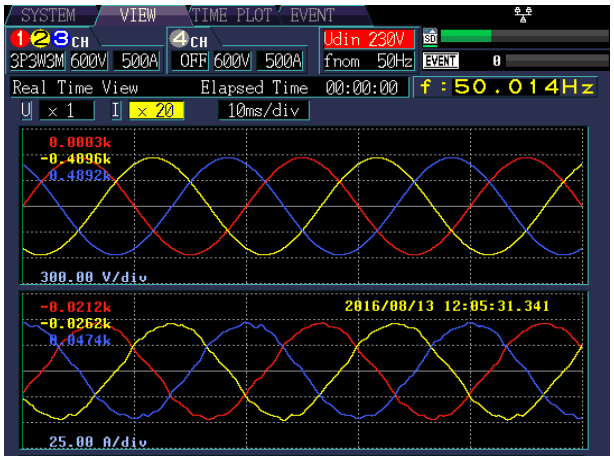
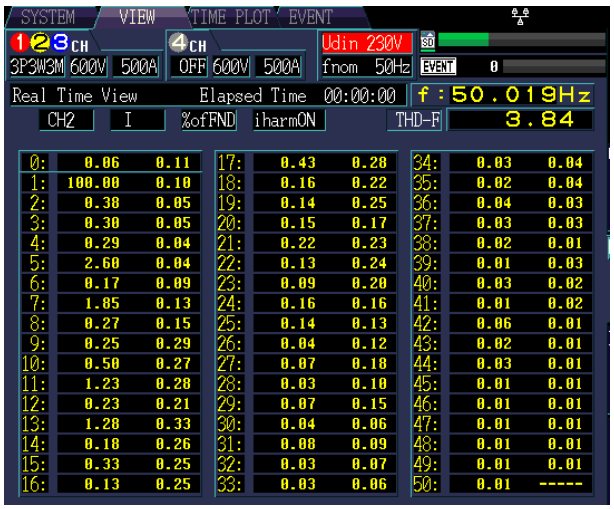



Figure 5-15: Magnitude (% of fundamental) of current harmonics up to 25 kHz

At 22.3 kW output power, inverter output electrical characteristics are recorded by Hioki Power Analyzer PW3198, as it can be seen in Fig. 5-16. In Fig 5-16(a) three-phase line-to-line voltage and line current waveforms are given. Individual current harmonic components including interharmonics as a percentage of fundamental current component and total harmonic distortion, THD is given in Fig. 5-16(b) measured with IEC61000-4-7:2002 measurement method. Since 5$^{th}$ and 7$^{th}$ voltage harmonics is dominant in grid voltage, 5$^{th}$ and 7$^{th}$ current harmonics is the most two dominant current harmonic in the harmonic spectrum. Total harmonic distortion, THD value is recorded as 3.84%, which is the lowest THD value obtained in the field tests.




(a)



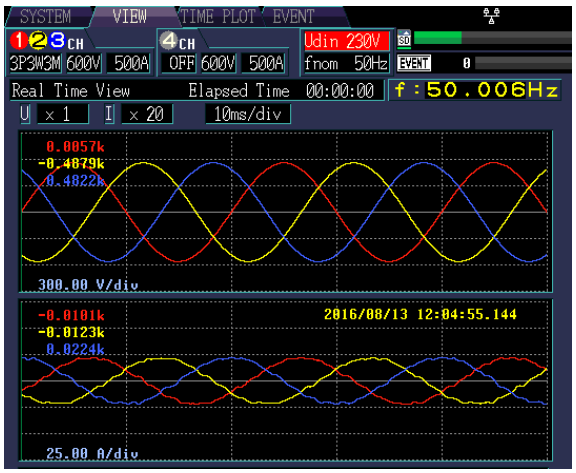

(b)


(c)

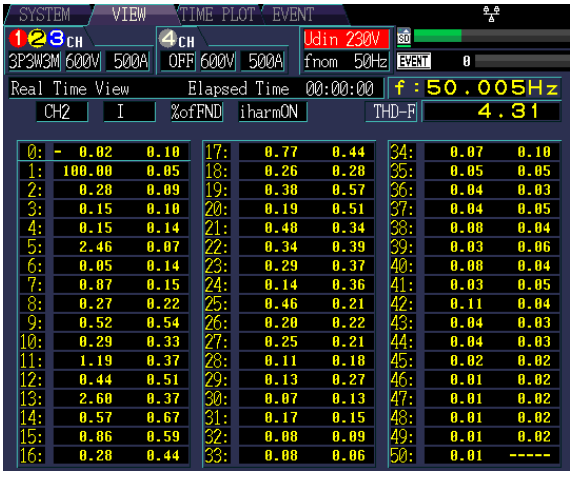
Figure 5-16: Snapshots of inverter output electrical quantities at 22.3 kW output power (a) Line-to-line voltage and line current waveforms, (b) Harmonic content of line current waveforms, and (c) Output powers.

As it can be seen in Fig 5-16(c), inverter operates almost at unity power factor with a power factor, PF > 0.999, according to the preset reactive current reference value which is equal to zero.

At 10.77 kW half-load output power, inverter output electrical characteristics are recorded as it can be seen in Fig. 5-17. In Fig 5-17(a) three-phase line-to-line voltage and line current waveforms at 10.77 kW output power are given. In Fig. 5-17(b) total harmonic distortion, THD value can be seen as 4.31%. Inverter also operates almost at unity power factor at 10.77 kW output power, as it can be seen in Fig. 5-17(c).




(a)




(b)


(c)

Figure 5-17: Snapshots of inverter output electrical quantities at 10.77 kW output power (a) Line-to-line voltage and line current waveforms, (b) Harmonic content of line current waveforms, and (c) Output powers.

At 22.34 kW output power, each individual harmonic current magnitude as a percentage of fundamental current magnitude is compared with the individual harmonic limits defined in IEEE Std. 519-2014 for $I_{SC}/I_L<20$. Comparison plot can be seen in Fig. 5-18. As it can be seen, each measured current harmonic is within individual harmonic limits defined in standard, except 24$^{th}$ harmonic which is almost equal to the harmonic limit. Phase current TDD is equal to 3.43% ,if the rated output power of the three-phase inverter is accepted as 25 kW.

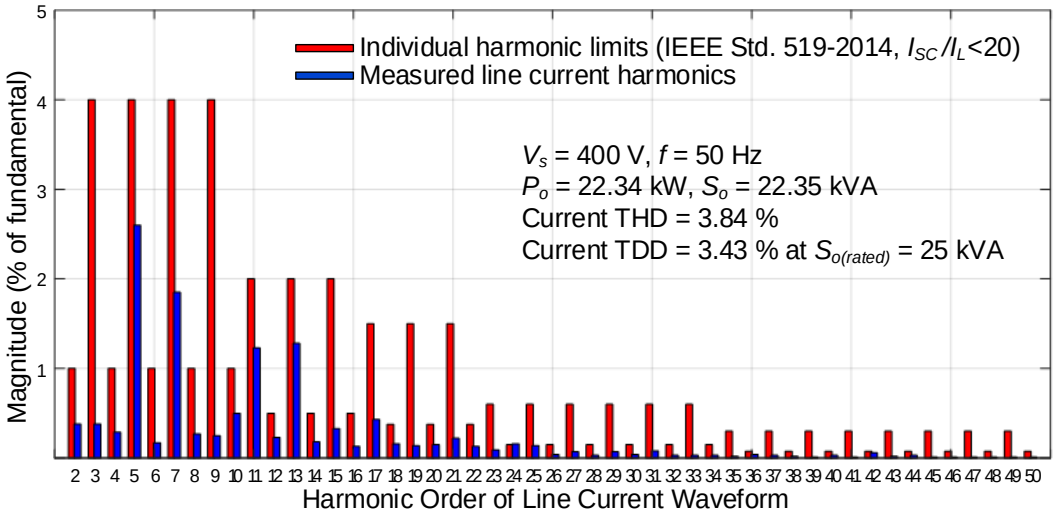



Figure 5-18: Comparison plot of measured individual current harmonics at 22.34 kW output power and individual harmonics limits in IEEE Std. 519-2014 ($I_{SC}/I_L<20$)

Change of phase current THD for different output powers up to 22.34 kW is given in Fig. 5-19. As it can be seen in the figure, as the output power and hence output current fundamental frequency component increases, phase current THD level decreases, since magnitude of low level current harmonic components is almost fixed, and their percentage decreases as the output power increases.

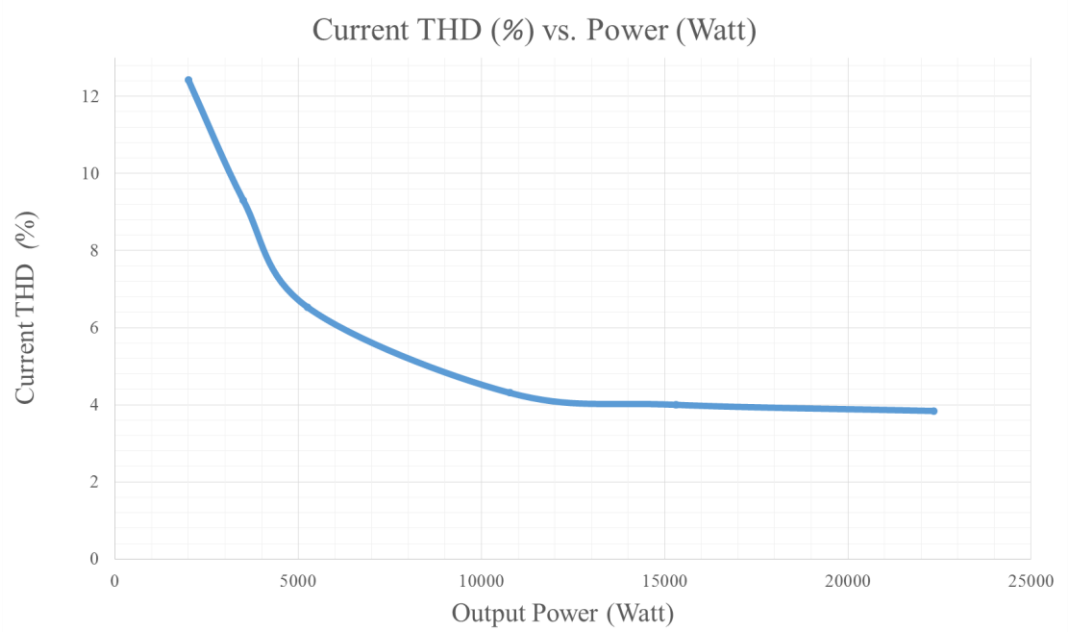
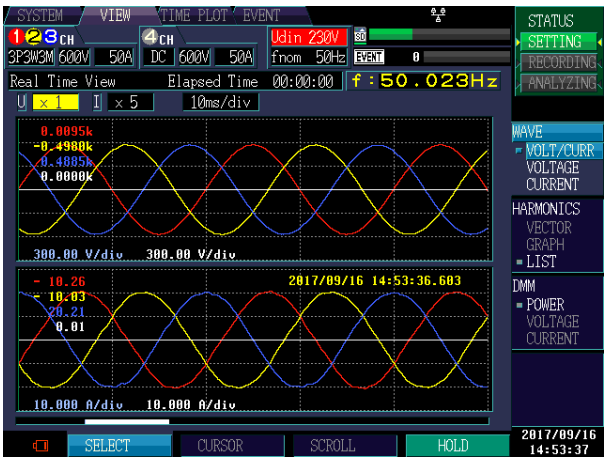
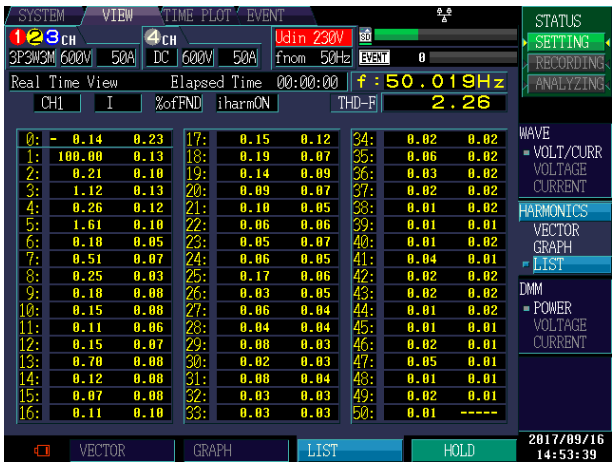



Figure 5-19: Change of experimental phase current THD (%) for output powers up to 22.34 kW

In the design of LCL filter, main focus is to design a LCL filter of minimum volume which is enough to fulfil the requirements in individual harmonic limits defined in IEEE Std. 519-2014 and to obtain a THD value lower than 5% at peak output power. By considering the field test results, main design purpose of LCL filter is achieved. On the other hand, increase of filter inductance has positive effect on THD. Although designed LCL filter has more than enough attenuation at switching frequency, higher filter inductance is advantageous in terms of attenuating low level harmonics. As stated earlier in the design section, increase of filter inductance enables to increase the parameters of PI controller, so that inverter current control loop has better control on low order harmonics to increase the attenuation at low frequencies. In order to show the effects of high inductance on total harmonic distortion of line current, instead of 50 uH grid side inductor, $L_g$ 1.5 mH grid side inductor is used. During 5.6 kW active power transferring to grid with 1.5 mH grid side inductance, recorded electrical quantities of three-phase inverter can be seen in Fig. 5-20.




(a)




(b)


(c)

Figure 5-20: Snapshots of inverter output electrical quantities at 5.61 kW output power using 1.5 mH grid side inductance, $L_g$ (a) Line-to-line voltage and line current waveforms, (b) Harmonic content of line current waveforms, and (c) Output powers.

As it can be seen in Fig 5-20(b), total harmonic distortion of line current reduced to 2.26% at 5.6 kW output power, which is even smaller from the THD at the rated output power. For the same output power THD value is 6.8% when grid side inductance is 50uH. By considering the decrease in the THD value of output current, using a large value of filter inductance can be thought as preferable. However larger inductance value means larger filter volume, increased cost and some other disadvantages stated in the design section, so that, since the designed filter fulfils IEEE Std. 519-2014 current harmonic distortion standards with a much smaller filter volume, there is no need for higher inductor.

### 5.6. Transient Performance of the System

In order to investigate the three-phase inverter performance and stability in the case of that solar power changes dramatically, solar power is disconnected suddenly when three-phase inverter is transferring nearly 11 kW power to grid. During PV array disconnection, output line current, $i_a$ waveform and DC bus voltage, $v_{dc}$ waveform is recorded, as it can be seen in Fig. 5-21 by Tektronix MSO3034 oscilloscope.

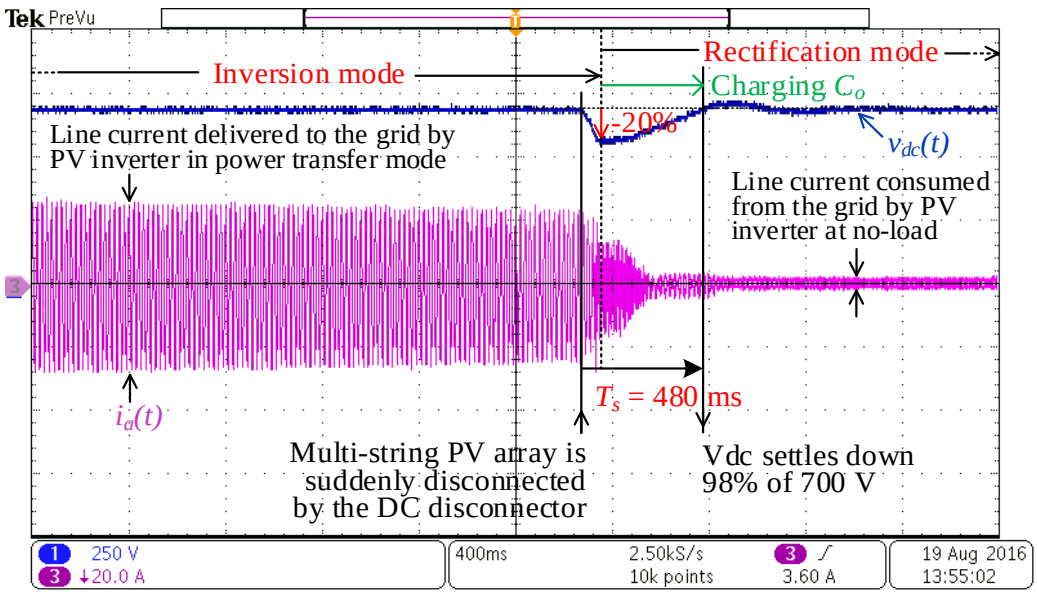



Figure 5-21: Change of output line current, $i_a$ and DC bus voltage, $v_{dc}$ at the instant of sudden disconnection of PV power

As it can be seen in Fig. 5-21, three-phase inverter transfers nearly 11 kW to grid in steady state operation until the instant of PV array disconnection. Output current and DC link voltage is stable during operation at steady PV power. PV power is disconnected at the time where $T_s$ is equal to zero. Right after the disconnection of PV power, DC link voltage drops nearly 20%, due to the fact that three-phase inverter endeavors to proceed active power transfer to grid. After DC link voltage reaches to 560 V DC, inverter operation mode changes and starts to work as a three-phase PWM rectifier. As demonstrated in Fig. 5-21, after inverter start to work in rectification mode in order to keep DC link voltage at the reference value, three-phase inverter charges DC link capacitor to the reference DC link voltage. DC link voltage reaches to 98% of referenced DC link voltage value which is 700 V, 480 ms later than PV power disconnection. Three-phase inverter continues its operation at rectification mode, drawing active power from grid necessary for the losses occurs from switching and other inverter losses, in order to keep DC link voltage stable at 700 V. The reason of the long settling time, which is 480 ms, can be explained as follows. In order to protect the three-phase inverter from excessive DC link voltage, output of DC link PI controller which controls the reference value of $I_d$ is limited for negative values. When the output of DC link PI controller, in other words reference d-axis current, becomes negative inverter works in rectification mode. High active power drawing after PV power is disconnected can result in excessive DC link voltage overshoot. With the limitation of reference d-axis current in the negative region by software, active power drawing from grid is also limited. So that, after DC link voltage undershoots, three-phase inverter charges DC link capacitor with a limited current. As it can be seen in Fig. 5-21, after inverter starts to work in rectification mode, rise of DC link voltage slope is stable until it reaches to referenced DC link voltage, due to constant active power drawing from grid. This is one of the reasons why settling time of DC link voltage is that much long. Another reason of long settling time is because of the high output filter capacitance of PSFB MPPT converter. Since the capacitor value, that is needed to be charged, is high and charging current is limited, settling time, $T_s$ is around 480 ms. Settling time value may become shorter with the smaller capacitance value at the DC link and also with increased negative band limitation of DC link voltage PI controller output value.

## 5.7. Efficiency

At different values of output power, efficiency of grid connected three-phase voltage-source inverter is calculated. In order to calculate the efficiency, input power of three-phase inverter, which is also output power of MPPT converter, can be calculated by the recorded values of DC link current, $i_{dc}$ and DC link voltage, $v_{dc}$. DC link current and DC link voltage waveforms is recorded by Tektronix MSO3034 oscilloscope as can be seen in Fig. 5-22.

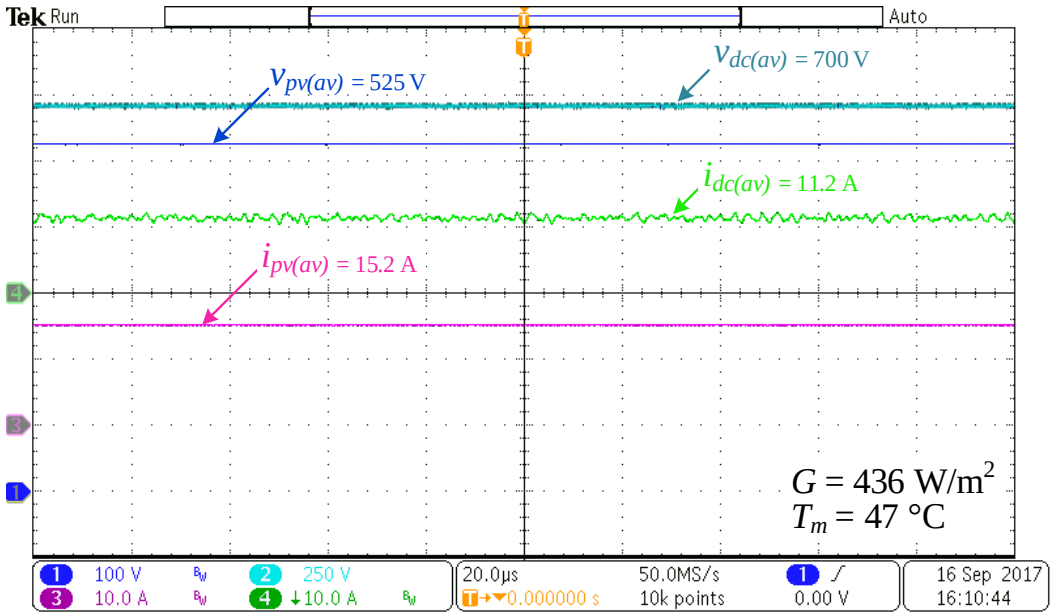



Figure 5-22: PV array average voltage, $v_{pv(av)}$ (blue), PV array average current, $i_{pv(av)}$ (magenta), DC link voltage $v_{dc(av)}$ (cyan) and DC link current, $i_{dc(av)}$ (green) waveforms at 436 W/m$^2$ solar irradiation and 47 °C ambient temperature

In order to calculate overall system efficiency, including MPPT converter and three-phase inverter, PV array voltage and PV array current is also recorded. Since the original current and voltage waveforms are oscillating because of switching, current and voltage waveforms are averaged. Input power of three-phase inverter is calculated by multiplying average values of DC link voltage and current. Output power of three-phase inverter is recorded by HIOKI 3198 Power Analyzer. For different experimental values of three-phase inverter input power, which is also the output power of MPPT converter, theoretical three-phase inverter output power and efficiency values are calculated. Also output power of three-phase inverter is

recorded by HIOKI 3198 Power Analyzer for each input power value. Recorded and calculated values of input power, output power and efficiency can be seen in Table 5-2.

Table 5-2: Comparison of experimental and theoretical values of output power and efficiency for different input power levels

| $P_{in}$, kW | $P_o$, kW | | Efficiency, $\eta = [P_o / P_{o(MPPT)}]$ 100, % | |
|---|---|---|---|---|
| Experimental* | Experimental* | Theoretical† | Experimental | Theoretical |
| 3.08 | 2.99 | 3.05 | 97.05 | 99.00 |
| 4.31 | 4.21 | 4.27 | 97.54 | 99.05 |
| 8.69 | 8.57 | 8.61 | 98.55 | 99.10 |
| 10.37 | 10.21 | 10.27 | 98.46 | 99.10 |
| 15.13 | 14.88 | 14.98 | 98.32 | 99.05 |
| 19.58 | 19.21 | 19.38 | 98.09 | 99.00 |

Theoretical and experimental efficiency values are plotted for various output power values, based on calculated and recorded efficiency values, as it can be seen in Fig. 5-23.

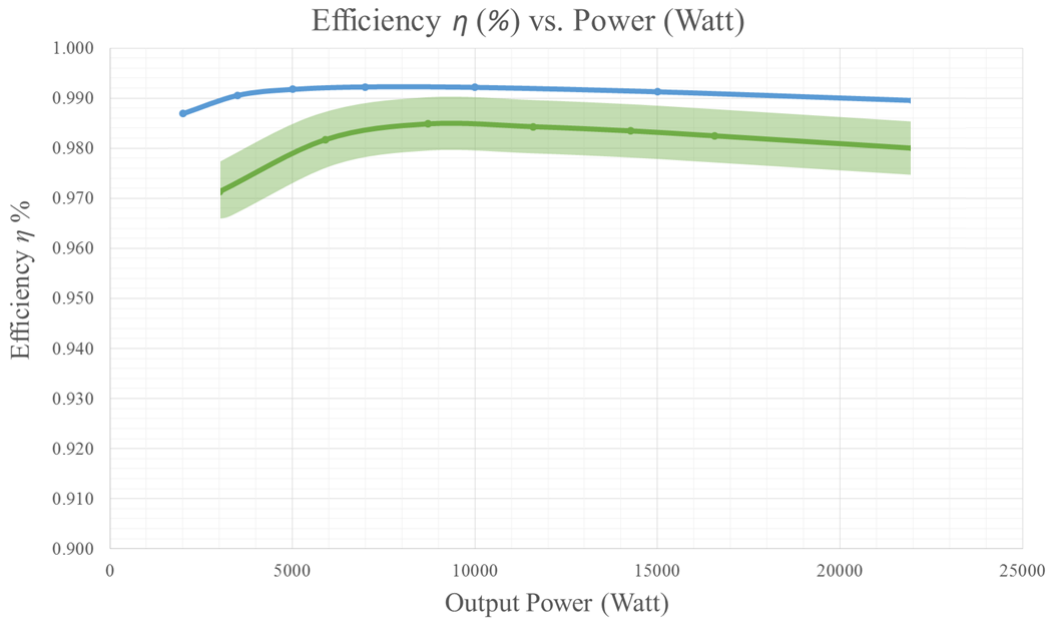



Figure 5-23: Change of theoretical efficiency (blue line), experimental efficiency (dark green line) and experimental efficiency error tolerance (light green band) with respect to output power

As it can be seen in Table 5-2 and Fig. 5-23 three-phase inverter peak efficiency is around 98.5%, occurs at half of rated output power and drops to 98 % at maximum output power, while theoretical efficiency is 99% at 3 kW output power and continues to be above of 99% up to maximum output power. Due to the measurement devices error tolerance, which is ±0.5%, a light green band, that illustrates the experimental efficiency error tolerance, is shown in Fig. 5-23. From half load to full load the difference between theoretical and experimental values changes between 0.5% and 1%. Also at low output power, such as 3 kW, difference between theoretical and experimental values is 2%. One of the reason behind the difference between theoretical and experimental efficiency values is the usage of assumption in the calculation of theoretical efficiency. The used assumption is that current flowing through SiC MOSFETs is 50 Hz fundamental frequency current. Switching and conduction losses of SiC MOSFETs are calculated based on this assumption. In reality, current flowing through SiC MOSFETs is not completely filtered. In addition to 50 Hz fundamental output current, there is switching frequency current ripple of a magnitude which is nearly 25% of rated output current, superimposed on fundamental output current. This high frequency current ripple increases both switching losses and conduction losses, since RMS value of current flowing through SiC MOSFETs increases. In addition to that phenomenon, during calculation of theoretical efficiency some loss sources, such as cabling between three-phase inverter components and LCL filter damping resistor losses are ignored. These reasons can be listed as why theoretical and experimental efficiencies are not completely consistent.

Thermal image of inverter power stage and interface board is given in Fig. 5-24. Maximum temperature of power MOSFET module is measured as 41.4°C from top of the power plane board.

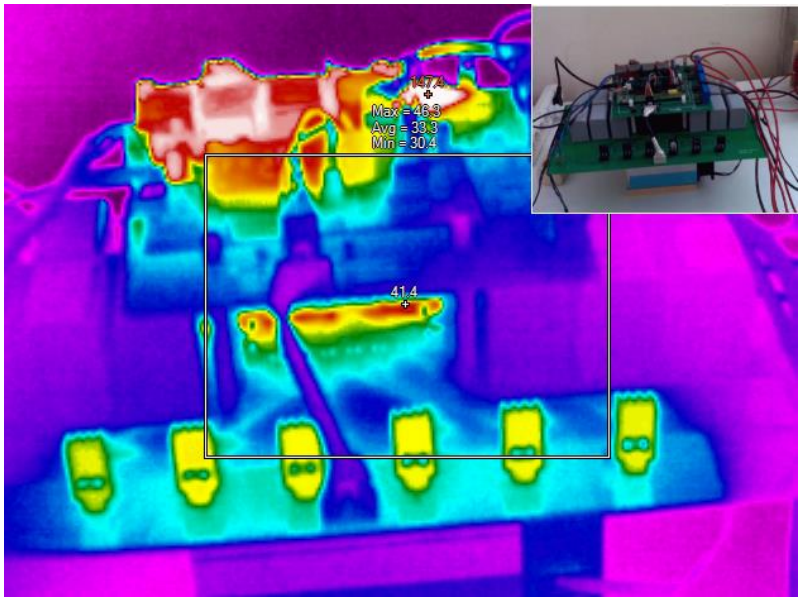



Figure 5-24: Thermal image of inverter power stage and interface board

Thermal image of inverter filter block is given in Fig. 5-24. Maximum temperature of converter side inductors is measured as 47.4°C when ambient temperature is 28.1°C.

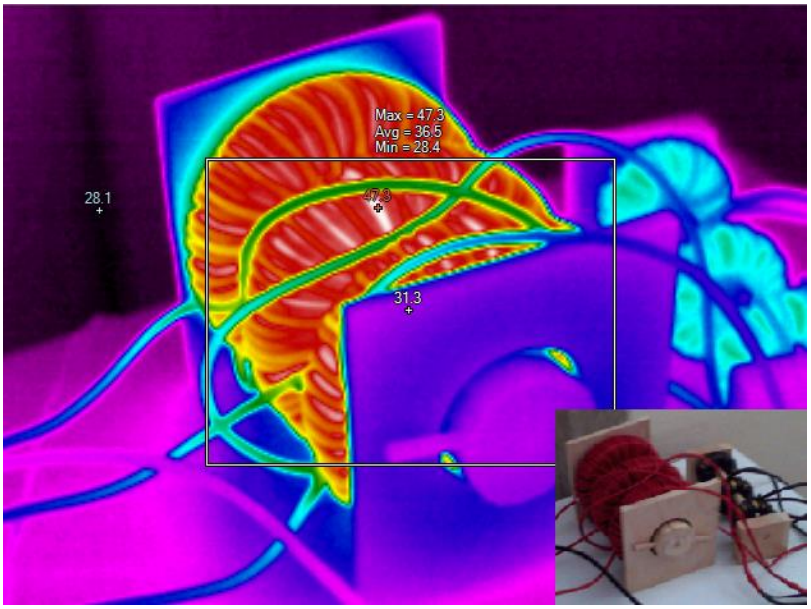



Figure 5-25: Thermal image of inverter filter block

# CHAPTER 6

# CONCLUSIONS and FUTURE WORK

## 6.1. Conclusions

Within the scope of this thesis, a 30 kW grid connected voltage source three-phase inverter with SiC MOSFET module has been designed and implemented in order to work with a phase-shifted full bridge MPPT converter, in such a way that these two converters compose a full system solution PV supply to transfer photovoltaic energy into the grid in an efficient and robust way. Emergence of commercial SiC based power MOSFETs, which have low turn-on and turn-off times, has enabled to increase switching frequency compared to traditional Si based switching components. This circumstance was one the main motives of this thesis in the scopes of increasing the switching frequency in order to reduce passive component volumes of inverter, such as LCL filter and DC link capacitor volume and decreasing losses which leads to reduce in heat sink volume and having better efficiency.

In the design stage of three-phase inverter, inverter parameters such as passive component values, rated voltage selection, pulse with modulating method and inverter control method has been selected, and inverter designed based on various design methodologies.

Optimum switching frequency has been selected by making the trade-off between decrease of passive components' volume and increase of losses occurring in the power stage of inverter with the increase of switching frequency into consideration. Besides, as explained in the design section, filter size was not completely depended on switching frequency. In order to maintain the stability of inverter control loop, a

moderate inductance value between inverter output and grid was needed. So that, after some point increase of switching frequency was not advantageous in any ways.

LCL filter parameters has been determined to have enough attenuation at the switching frequency primarily. Although smaller size of LCL filter had enough attenuation at the switching frequency, in order to be in the safe side by considering control loop stability of inverter, LCL filter parameters determined accordingly, as stated in the design section. Active damping method was not preferred in LCL filter since the losses occurring due to the passive damping method was tolerable.

SPWM was used as the modulating method due to the fact that its simplicity and to make loss calculations more accurate in order to show SiC MOSFETs' advantages in a more explicit way, despite the fact that SVPWM modulating method was more advantageous via enabling the reduction of necessary DC link voltage, so that decreasing losses occurring in SiC MOSFETs.

Synchronously rotating reference frame control was used as the control method of the three-phase inverter, again for its simplicity. Although implementation of this control method was easy, it was inefficient in terms of attenuating low order harmonics resulting from grid voltage harmonics, mainly $5^{th}$ and $7^{th}$ order. In order to reduce the harmonics, grid line-to-neutral voltages had been imitated at the output of the inverter, apart from the necessary changes that are needed to control active and reactive power flow.

Loss components, such as switching and conduction losses of SiC MOSFETs and LCL filter losses were calculated in the design section for various output powers in order to determine heat sink requirement and to forecast efficiency of three-phase inverter. According to efficiency calculations inverter efficiency at rated output power arose as 99%. With regard to calculated loss components, heat transfer circuitry of power stage had been deduced and necessary heat sink requirement was calculated. Heat sink selection was made based on this value.

In order to implement three-phase inverter, two electronic board which are interface and power plane boards had been designed. The main purpose of this interface board was to make measurements which is necessary for control loop and to transfer gate

drive signals from DSP board to gate drivers, by buffering those signals to reach the adequate current level for gate drivers. Gate driver PCB boards and DC link capacitors was mounted on power plane board, which was designed to meet the requirements of minimum inductive paths that are necessary for SiC MOSFET module to operate in a safe way. Three-phase inverter controller software had been implemented in Code Composer Studio environment using TI TMDSDOCK28335 Experimenter Kit as controller board.

Designed and implemented three-phase inverter had been operated in the field with PSFB MPPT converter, energized by 23.75 kW total installed capacity solar array. Three-phase inverter output characteristics had been investigated and in the grid connected close loop mode, and various powers up to 22.32 kW had been transferred into grid. Inverter switching characteristics, drain-source voltage, unfiltered line current and zero voltage switching phenomenon were examined with the change of dead time and output line current.

Total harmonic distortion of three-phase inverter had been recorded at various output powers and a minimum THD value of 3.84% had been obtained at maximum output power of 22.32 kW. In order to investigate the effect of LCL filter inductance on total harmonic distortion of line currents, grid connection was made with an increased grid side inductance of 1.5 mH, and 2.26% THD had been obtained at 5.62 kW output power.

Experimental efficiency values was calculated from recorded input and output power values. 98.55% peak efficiency at half of rated output power and 98% efficiency at peak output power had been obtained. From half load to full load the difference between theoretical and experimental efficiency values changed between 0.5% and 1%.

A journal paper, All SiC Grid-Connected PV Supply with HF Link MPPT Converter: System Design Methodology and Development of a 20 kHz, 25 kVA Prototype, have been published on MDPI Electronics (May 2018) partially based on the research work had been done in this thesis [5].

## 6.2. Future Work

Designed three-phase grid connected voltage source inverter presented in this thesis has reached 22.32 kW peak output power with a 98% efficiency and a minimum of 3.84% total harmonic distortion of line current at peak output power. Although most of the performance objectives has been fulfilled, in order to increase performance of three-phase inverter and to measure the effects new methods, some future work can be conducted.

Instead of synchronous rotating reference frame control, in order to attenuate the low order harmonics, stationary reference frame control can be used. Stationary reference frame control utilizes PR controller instead of PI controller, so that this controller can show better performance, since PI controller does not remove steady-state error completely when the signal is time varying. To further attenuate low order harmonics, such as $3^{rd}$, $5^{th}$ and $7^{th}$ order harmonics, a harmonic compensator block can be added in parallel with the PR controller.

In order to reduce the losses occurring in SiC MOSFETs, DC link voltage can be decreased, so that current ripple occurring in the unfiltered current, flowing through SiC MOSFETs, can be decreased for the same switching frequency. DC link voltage can be decreased by implementing two methods. Third harmonic injection method can be used to decrease the DC link voltage down to 560 V while using SPWM. Instead of using SPWM, SVPWM modulating technique can be used to decrease DC link voltage and hence switching frequency current ripple, so that efficiency of three-phase inverter can be increased.

Instead of using LCL filter method, some various filter types, such as LLCL filter or LTCL filter can be designed and implemented in order to measure and compare their effects on total harmonic distortion, THD of line currents, and to attenuate switching frequency current ripple. By this way output filter volume can be decreased while the system performance is the same or better.

Lastly a signal controlled three-phase relay can be used for grid connection, instead of a manual AC contactor. Grid connection is made manually when the DC link of the three-phase inverter reaches 700 V. By this way three-phase inverter grid

connection can be made automatically, and also inverter can protect itself from excessive grid disturbances, such as voltage and frequency oscillations.

# REFERENCES


**[1]** REN 21, Renewables 2017: global status report. 2017.

**[2]** R. Fu, D. Chung, T. Lowder, D. Feldman, K. Ardani, R. Fu, D. Chung, T. Lowder, D. Feldman, and K. Ardani, "U.S. Solar Photovoltaic System Cost Benchmark : Q1 2017 U.S. Solar Photovoltaic System Cost Benchmark : Q1 2017," Nrel, no. September, 2017.

**[3]** ABB, "ABB string inverters," vol. 2014, p. 2, 2014.

**[4]** J. Rabkowski, D. Peftitsis, and H. Nee, "Design Steps Towards a 40-kVA SiC Inverter With an," pp. 1536–1543, 2012.

**[5]** S. Öztürk, M. Canver, I. Çadırcı, and M. Ermiş, "All SiC Grid-Connected PV Supply with HF Link MPPT Converter: System Design Methodology and Development of a 20 kHz, 25 kVA Prototype," Electronics, vol. 7, no. 6, p. 85, May 2018.

**[6]** F. Iov, M. Ciobotaru, D. Sera, R. Teodorescu, F. Blaabjerg, Power electronics and control of renewable energy systems, in Proceedings of PEDS'07, pp. P-6–P-28, 27–30, Nov 2007.

**[7]** M. Ciobotaru, R. Teodorescu, F. Blaabjerg, Control of single-stage single-phase PV inverter, in Proceedings of EPE'05, pp. P.1–P.10 (2005).

**[8]** IEEE-SA Standards Board, IEEE Std 929-2000: IEEE recommended practice for utility interface of photovoltaic (PV) systems, Jan 2000.

**[9]** D. Meneses, F. Blaabjerg, O. García, J.A. Cobos, Review and comparison of step-up transformerless topologies for photovoltaic AC-module application. IEEE Trans. Power Electron. 28(6), 2649–2663(2013).

**[10]** R. Teodorescu, M. Liserre, P. Rodriguez, in Grid Converters for Photovoltaic and Wind Power Systems. Wiley, New York (2011).

**[11]** S.B. Kjaer, J.K. Pedersen, F. Blaabjerg, A review of single-phase grid-connected inverters for photovoltaic modules. IEEE Trans. Ind. Appl. 41(5), 1292–1306 (2005).

**[12]** S.B. Kjaer, Design and Control of an Inverter for Photovoltaic Applications, PhD Thesis, Department of Energy Technology, Aalborg University, Aalborg, Denmark, Jan 2005.

**[13]** Kjær, Søren Bækhøj. Design and control of an inverter for photovoltaic applications. Institute of Energy Technology, Aalborg University, 2005.

**[14]** J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si - Evaluation of potentials for performance improvement of inverter and DCDC converter systems by SiC power semiconductors," IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2872–2882, 2011.

**[15]** N. C. Sintamarean, F. Blaabjerg, H. Wang, and Y. Yang, "Real field mission profile oriented design of a SiC-Based PV-inverter application," IEEE Trans. Ind. Appl., vol. 50, no. 6, pp. 4082–4089, 2014.

**[16]** A.G. Yepes, F.D. Freijedo, O. Lopez, J. Doval-Gandoy, Analysis and design of resonant current controllers for voltage-source converters by means of Nyquist diagrams and sensitivity function. IEEE Trans. Ind. Electron. 58(11), 5231–5250 (2011).

**[17]** V. Kaura, V. Blasko," Operation of a phase locked loop system under distorted utility conditions", IEEE 11th Annual Applied Power Electronics Conference and Exposition, Vol. 2, pp. 703-708, 3-7 March 1996.

**[18]** L.R. Limongi, R. Bojoi, C. Pica, F. Profumo, A. Tenconi," Analysis and comparison of phase locked loop techniques for grid utility applications," Power Conversion Conference 2007, pp. 674-681, 2-5 April 2007.

**[19]** N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications, and Design." 3rd Edition, John Wiley & Sons, Inc., 2002.

**[20]** Texas Instruments, "TMS320x2834x Delfino Enhanced Pulse Width Modulator ( ePWM ) Module Reference Guide," July, 2009.

**[21]** CSUN SOLAR. CSUN260-60P Datasheet. http://www.solarsynergy.co.nz/pdf/255-60P%2040mm.pdf. Accessed: 20.09.2017.

**[22]** K. Fujii, Y. Noto, M. Oshima, and Y. Okuma, "1-MW Solar Power Inverter with Boost Converter using all SiC Power Module Keywords," 2015 17th Eur. Conf. Power Electron. Appl. (EPE'15 ECCE-Europe), pp. 1–10, 2015.

**[23]** IEC Standard for Standard Voltages, IEC Standard IEC 60038 2002-07.

**[24]** J. Feng, H. Wang, J. Xu, M. Su, W. Gui and X. Li, "A Three-Phase Grid-Connected Micro-Inverter for AC Photovoltaic Module Applications," in IEEE Transactions on Power Electronics, vol. PP, no. 99, pp. 1-1.

**[25]** J. W. Kimball and M. Zawodniok, "Reducing Common-Mode Voltage in Three-Phase Sine-Triangle PWM With Interleaved Carriers," in IEEE Transactions on Power Electronics, vol. 26, no. 8, pp. 2229-2236, Aug. 2011.

**[26]** Y. M. Chen, K. Y. Lo and Y. R. Chang, "Multi-string single-stage grid-connected inverter for PV system," 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, 2011, pp. 2751-2756.

**[27]** SpeedFit Design Simulator™, USA: Wolfspeed, Available at: https://www.wolfspeed.com/speedfit, Accessed on: Feb. 24, 2018.

**[28]** M. Jasinski, Direct power and torque control of AC-DC-AC converter-fed induction motor drives, Ph.D. Thesis, Warsaw University of Technology, Warsaw, Poland, 2005.

**[29]** M. Liserre, Innovative control techniques of power converters for industrial automation,Politecnico di Bari, Ph.D. Thesis, Italy, 2001.

**[30]** K. Jalili, Investigation of Control Concepts for High-Speed Induction Machine Drives and Grid Side Pulse-Width Modulation Voltage Source Converters, PhD Thesis, Technischen Universität Dresden, p. 174, 2009.

**[31]** M. Liserre, F. Blaabjerg, A. Dell'Aquila, Step-by-step design procedure for a grid connected three-phase PWM voltage source converter. Int. J. Electron. 91(8), 445–460 (2004).

**[32]** M. Liserre, A. Dell'Aquila, F. Blaabjerg, Genetic algorithm-based design of the active damping for an LCL-filter three-phase active rectifier. IEEE Trans. Power Electron. 19(1), 76–86 (2004).

**[33]** M. Liserre, A. Dell'Aquila, F. Blaabjerg, Stability improvements of an LCL-filter based three-phase active rectifier, IEEE, 2002, pp. 1195–1201.

**[34]** Cree Inc., CCS050M12CM2, Datasheet, Rev. C, pp. 1-10, 2013.

**[35]** D. Graovac, M. Pürschel, and K. Andreas, "MOSFET Power Losses Calculation Using the Data- Sheet Parameters," Infineon Technol. AG, no. July, pp. 1–23, 2006.

**[36]** SpeedFit Design Simulator™, USA: Wolfspeed, Available at: https://www.wolfspeed.com/speedfit, Accessed on: Feb. 24, 2018.

**[37]** Magnetics Inc., 0078337A7, Datasheet, Rev. 2016-11-16, pp. 1, 2016.

**[38]** Magnetics® Inductor Design tool, USA: Magnetics, Available at: https://www.mag-inc.com/Design/Design-Tools/Inductor-Design, Accessed on: Feb. 24, 2018.

**[39]** Micrometals Inc., T225-40, Datasheet, Rev. 20160713, pp. 1, 2016.

**[40]** F. Blaabjerg, R. Teodorescu, M. Liserre, A.V. Timbus, Overview of control and grid synchronization for distributed power generation systems. IEEE Trans. Ind. Electron. 53(5), 1398–1409 (2006).

**[41]** A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, F. Blaabjerg, Evaluation of current controller for distributed power generation systems. IEEE Trans. Power Electron. 24(3), 654–664 (2009).

**[42]** Y. Bae, T. K. Vu, and R. Y. Kim, "Implemental control strategy for grid stabilization of grid-connected PV system based on German grid code in symmetrical low-to-medium voltage network," IEEE Trans. Energy Convers., vol. 28, no. 3, pp. 619–631, 2013.

**[43]** FISCHER ELEKTRONIK. LA17 Datasheet. https://www.fischerelektronik .de/fileadmin/fischertemplates/download/Katalog/heatsinks.pdf. Accessed: 20.09.2018

**[44]** Seung-Gi Jeong and Min-Ho Park, "The Analysis and Compensation of Dead-Time Effects in PWM Inverters," IEEE Trans. on Ind. Electronics, vol. 38, no. 2, April 1991, pp. 108-114.

**[45]** IEC Standard for Electromagnetic compatibility (EMC) - Part 4-7: Testing and measurement techniques - General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto, IEC Standart IEC 61000-4-7:2002.