ULTRA-LOW POWER INTERFACE ELECTRONICS DESIGN FOR FULLY IMPLANTABLE COCHLEAR IMPLANTS

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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ABSTRACT

ULTRA-LOW POWER INTERFACE ELECTRONICS DESIGN FOR FULLY IMPLANTABLE COCHLEAR IMPLANTS

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Cochlear implants are one of the most successful neural prosthesis where users could go from being profoundly deaf to enjoying high degree of speech perception. However, subsequent aesthetic concerns, damage risks and high power dissipation associated with bulky external units of cochlear implants have redirected recent studies to fully implantable cochlear implants (FICI). Although, implantable sensors occupies the largest portion of the previous researches on FICIs, design of the low powered signal conditioning interface circuit is a bottle-neck to accomplish a FICI system. In this thesis, a novel fully integrated interface circuit is designed to process signals from an implantable multi-frequency piezoelectric (PZT) cantilever set for stimulation of the auditory neurons.

The 1st generation FICI interface is focused on power dissipation of the front-end signal conditioning circuit. Power of the front-end circuit is reduced through a novel logarithmic amplifier design that combines amplification and compression stages. The conditioned signal controls the biphasic rectangular current pulses for neural stimulation. Single channel performance of the circuit has been tested with a thin film pulsed-laser deposition (PLD) PZT sensor. The interface generates biphasic current in

the range of 110-430 μA for acoustic input of 60-100 dB sound pressure level (SPL). Power dissipation of the front-end signal conditioning and the overall system for 8-channel operation is projected from measurement as 51.2 and 691.2 μW, respectively.

After validating the 1st generation interface performance, power dissipation and input range of the sensor front was improved at the 2nd generation FICI interface through novel current mode circuits. The conditioned signal is converted into biphasic neural stimulation current with a 7-bit user-programmed DAC to enable patient fitting (calibration). The proposed circuit introduces an optimized stimulation current waveform to reduce the electrode voltage and hence supply voltage of the stimulator (most power hungry part) by about 20%. The designed system has been tested with up to 60 dB input dynamic range (40-100 dB SPL) while the minimum threshold and maximum comfort levels of the system are 0 and 1 mA, respectively. The 8-channel interface has been validated to be fully functional with the front-end and the overall circuit power dissipation of 19.7 and 471.7 μW, when excited by a mimicked speech signal. The proposed 2nd generation interface electronics is the first sub-500 μW FICI interface that provides more than 30 years of operational lifetime, and reduces the healthcare cost and risks associated with surgical battery replacements.

The implantable device performance of the 2nd generation FICI interface electronics has been validated through in-vivo tests on a guinea pig. After validating healthy and partially-deafened hearing performance of the guinea pig, the electrical stimulation performance of controlled current stimulator and the FICI interface electronics were tested and compared. The neural stimulation capability of acoustically excited FICI system with intra-cochlear electrodes has been validated with 55 dB hearing threshold and 45 dB input dynamic range. The proposed system is the first FICI interface electronics with ultra-low power dissipation and wide dynamic range that is also validated with in-vivo tests.

Keywords: Fully Implantable Cochlear Implant, Neural Stimulation, Bionic Ear, Ultra-Low Power, Interface Electronics

ÖZ

TAMAMEN İMPLANTE KOKLEAR İMPLANTLAR İÇİN ÇOK DÜŞÜK GÜÇLÜ ARAYÜZ ELEKTRONİĞİ TASARIMI

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Koklear implantlar en başarılı nöral protezdir, öyle ki işitme kaybı olan implant kullanıcıları yüksek kalitede işitme algısına kavuşabilmektedir. Fakat, implantasyon sonrasında dış parçadaki parçadan dolayı oluşan estetik endişeler, zarar riski ve harcadıkları yüksek güçten dolayı bu yöndeki çalışmaları tamamen implante koklear implant (FICI) tasarımına yöneltmiştir. Bu çalışmaların büyük bir çoğunluğu implante sensorler ile ilgili olmasına rağmen tamamen implante bir sistem için en önemli problem düşük güçlü bir arayüz elektroniği tasarımıdır. Bu tez çalışmasında çoklu frekans piezoelektrik tramplen yapılar sayesinde algılanan sesin şiddeti ve frekansına göre işitme sinirlerini uyaracak bir arayüz elektroniği tasarlanmıştır.

1. jenerasyon arayüz elektroniğinde ön taraftaki sinyal işleme devresinin güç tüketimi, yükseltici ve sıkıştırıcı safhalarını birleştiren yeni bir logaritmik yükseltici devresi ile optimize edilmiştir. İşlenen sinyal, uyarım akımı üreten devreyi sürerek sinir uyarımı için gerekli iki fazlı kare akım dalgalarının üretilmesini sağlamaktadır. Devrenin tek kanallı performansı ince film PLD PZT sensor ile test edilmiştir. Arayüz devresi girişteki 60 ile 100 dB SPL arasındaki akustik sesler için 110 ile 430 μA arasında

değişen iki fazlı akım dalgaları üretmektedir. Sinyal işleme ve tüm uyarıcı devrelerin 8 kanallı operasyonu için harcadıkları güç miktarı sırası ile 51.2 ve 691.2 μW'tır.

2. jenerasyon FICI arayüz elektroniği ön safhadaki sinyal işleme devresinin gücünü daha da düşürecek yeni akım modunda çalışan devreler içermektedir. İşlenen sinyal, iki fazlı sinir uyarım akımına çevrilmektedir ki bu akım seviyesi 7-bit DAC yardımı ile hasta eşiğine göre ayarlanabilmektedir. FICI arayüz elektroniğinin harcadığı gücün büyük bir çoğunluğu yüksek voltajda çalışan sinir uyarımı kısmında harcanmaktadır. Bu sebeple, önerilen devre optimize akım dalgaları kullanarak elektrot voltajını dolayısı ile güç kaynağı voltajını %20 düşürmeyi sağlamaktadır. Tasarlanan devre 60 dB (40-100 dB) giriş seviyesi aralığında test edilmiş, sistemin minimum eşik ve maksimum konfor seviyeleri sırası ile 0 ve 1 mA olarak belirlenmiştir. 8 kanallı devre konuşma sesini taklit eden sinyali ile test edildiği zaman sinyal işleme ve tüm uyarım devresinin harcadığı güç 19.7 ve 471.7 μW'tır. Sonuç olarak 2. jenerasyon arayüz elektroniği 500 μW altında güç harcayan ilk FICI devresidir ve 30 yıldan fazla pil ömrü sunarak maliyeti ve pil değişimi sırasındaki ameliyat risklerini azaltmıştır.

2. jenerasyon FICI arayüz elektroniği devresinin implante cihaz performansı kobay üzerindeki in-vivo testler ile ispatlanmıştır. Kobayın işitme ve kısmi işitme kaybı ölçümleri yapıldıktan sonra kontrol edilebilen bir akım kaynağı ile elektriksel uyarım testleri yapılmıştır. Daha sonra, koklear içine yerleştirilen elektrot yardımı ile FICI sisteminin performansı ölçülmüş ve sonuçlar ile karşılaştırılmıştır. PZT sensör ile birleştirilen FICI sistemi 55 dB'den yüksek seslerde ve 45 dB giriş ses aralığında işitme sinirleri uyarabilmektedir. Önerilen FICI sistemi, çalışması in-vivo testler ile ispatlanan düşük güç tüketimine ve geniş giriş aralığına sahip ilk devredir.

Anahtar Kelimeler: Tamamen Entegre Koklear İmplant, Sinirsel Uyarım, Biyonik Kulak, Çok-Düşük Güçlü, Arayüz Elektroniği

To My Mother, Father, Brother and My Wife

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CHAPTER 1

INTRODUCTION

According to the World Health Organization (WHO), 466 million people have disabling hearing loss greater than 40 dB sound pressure level (SPL) as of 2018 where 34 million of these are children. Hearing loss can be mild, moderate, severe or profound and leads to difficulty in hearing sounds that range from daily conversations to loud noises [1]. Conventional hearing aids can be used for the treatment of mild-to-moderate hearing loss and occupy the largest part of the market. However, for treatment of severe-to-profound hearing loss, where average loss is greater than 90 dB SPL, cochlear implants (CIs) have to be utilized. A CI is the most successful of neural prostheses with more than 120,000 utilizing patients worldwide [2]. Its operation principle is based on direct stimulation of the auditory nerve, bypassing the eardrum, ossicles and damaged hair cells. The CI is based on the idea that there are enough auditory nerve fibers left for stimulation. Once the nerve fibers are stimulated, they fire and propagate neural impulses to the brain. The brain interprets them as sounds.

While CIs are the most successful neural prostheses with modern versions targeting high quality music perception [2]–[4], aesthetic concerns and frequent battery replacement in CI systems with bulky external components have redirected recent studies to fully implantable cochlear implants (FICIs) [5]–[7]. Moreover, improvements at microelectromechanical systems (MEMS) and complementary metal oxide semiconductor (CMOS) technologies enable to shrink the volume and power dissipation of the electronic systems [8], [9]. Therefore, feasibility of long lasting implantable systems become appropriate.

The fully implantable cochlear implant systems are deal with two main sub-systems, which are implantable sensors and the signal conditioning interface electronics. The implantable sensor detects the sound vibration and convert it into electrical signals where these signals are converted into neural stimulation pulses through interface electronics. Previous studies are mainly focused on sensor design of the FICIs where implantable microphones provide good sound detection [10]–[12]. On the other hand, interface electronics was required to use implantable sensors as the hearing device.

This thesis aims to design a low power, wide dynamic range and low-volume interface electronics for fully implantable cochlear implants. The interface electronics is utilized to sense the multi-channel piezoelectric (PZT) sensor outputs and stimulate the auditory neurons at cochlea according to amplitude and frequency of the incoming sound. In this chapter, introduction of hearing mechanism of human ear and hearing loss problem is provided. Possible solutions of hearing problems are discussed where cochlear implants received the main focus since they are the most successful neural prosthesis. Section 1.1 explains the anatomical overview of the ear and hearing mechanism. Section 1.2 summarizes the details of cochlear implants with different aspects to be considered. Section 1.3 describes requirements of fully implantable cochlear implants with previously reported interface electronics examples. Section 1.4 presents the objective of the thesis by considering goals and achievements gained by the thesis. Finally, the organization of the thesis is outlined in Section 1.5.

1.1. Ear and Hearing

The five primary senses, i.e. hearing, vision, olfaction, taste and feeling, are utilized to perceive our nature where five sensing organs are the windows of our body connecting us to the world. Hearing is the ability to sense the sounds where mammalians, such as humans, hear the sound at the nature through their ears. Any anatomical problem at the ear may causes hearing loss which can be cured through hearing aids depending on the level of hearing loss. In this part of the chapter,

anatomical properties of the ear and how hearing occur is going to be explained. Then, possible reasons of hearing loss and solutions of these problems are going to be described.

1.1.1. Anatomy of the Ear

The human ear is separated into three parts, which are the outer ear, the middle ear, and the inner ear [13] as shown in Figure 1.1. The outer ear consists of the pinna (auricle) and the ear canal where pinna directs the acoustic sound to the ear canal that transfer the sound to the middle ear. The ear canal is an air filled 2.5 cm long and 5 to 7 mm diameter tube which provides about 10-12 dB amplification at approximately 2500 Hz. Another function of the outer ear is to protect remaining portion of the auditory system from external hazards such as insects and dusts [14]. The middle ear starts with tympanic membrane (eardrum) placed at the end of ear canal converting acoustic sound into mechanical vibrations. The membrane is made of several skin layers and have a concave shape curving slightly inward as seen in Figure 1.2 [15]. The pressure waves striking on the membrane surface vibrates it with a magnitude proportional with the intensity of the sound. The remaining part of the middle ear is the air-filled cavity with 2 cm^3 of volume [14] that forms the link between outer ear and the fluid filled inner ear. This connection is realized by the ossicles, which are three tiny bones, malleus, incus, and stapes. The pressure at the middle ear is kept at atmospheric pressure through the help of Eustachian tube also called as auditory tube.

The ossicles transfers the mechanical vibration on the eardrum to the beginning of the inner ear (oval window) where the malleus with the largest area is connected with eardrum and the stapes with the lowest area is mounted on the oval window. The effective area on the link between tympanic membrane and malleus is around 55 mm^2 and the area of stapes footplate is 3.2 mm^2. Although the force applied to eardrum and the oval window is same, the pressure (force (F) per unit area (A)) at the oval window is 17 times higher (24.6 dB) that provides more vibration [14]. If the sound was directly transferred from air filled medium to fluid medium, there would be 30 dB

lost due to this transfer. However, about 25 dB of this loss is compensated via the ratio between the eardrum and the stapes footplate.

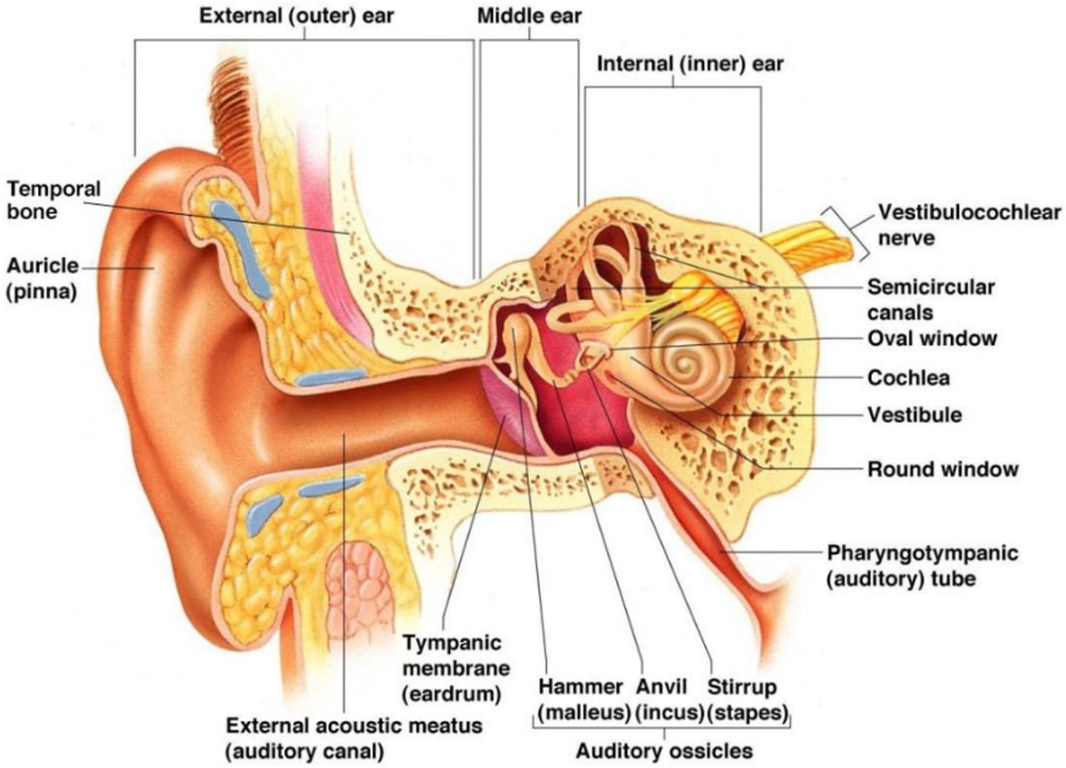


Figure 1.1. Anatomy of the human ear [16].

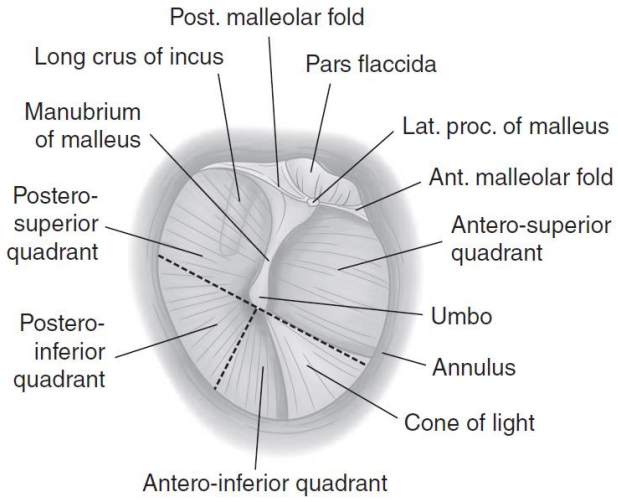


Figure 1.2. Schematic of the tympanic membrane [15].

The inner ear is located at very dense portion of the temporal bone named as petrous. The inner ear can be divided into three sections as shown in Figure 1.3, the semicircular canals (superior, lateral, and posterior), the vestibule, and the cochlea [14]. The semicircular canals and the vestibule are utilized for vestibular system to maintain balance of the body. The cochlea is sensing organ of the hearing that has a snail shape with approximately 2.5 turns. The cochlear tube has three compartments filled with fluid, which has a cross-section as shown in Figure 1.4 (a). The *scala media* is filled with endolymph fluid which has high sodium (Na+) concentration, on the other hand, the *scala vestibuli* and *scala tympani* is filled with perilymph that has lower Na+ and higher potassium (K+) concentration. The two fluid fields (scala tympani and scala media) are separated by basilar membrane. The vibration at the oval window vibrates the fluid inside cochlea where the round window satisfies the pressure stability. The vibration at the fluid displaces scala media hence the basilar membrane. The organ of Corti, shown in Figure 1.4 (b), is the sensing part of the cochlea that lies on the basilar membrane and has several thousands of sensory receptors called *hair cells*. The hair cells convert mechanical stimuli into electrical activity where each hair cell has bunch of tiny hairs on top of it that detect vibration. The electrical activity is transferred to the brain through auditory nerves.

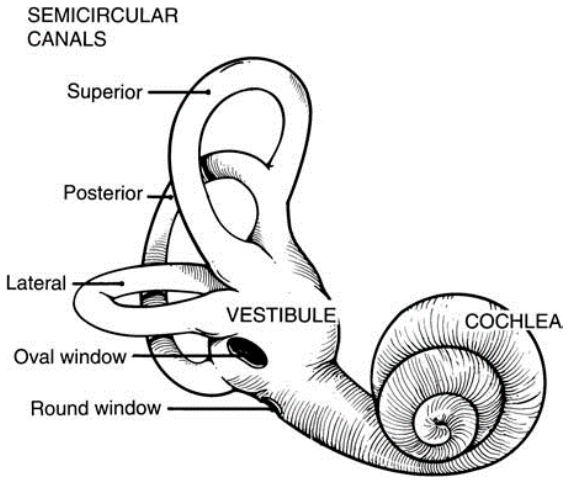


Figure 1.3. Schematic diagram of the inner ear [14].

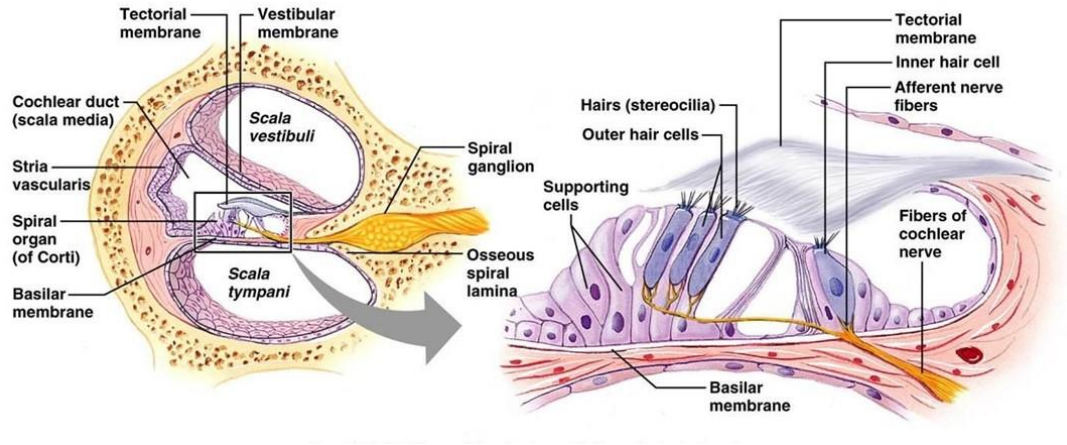


Figure 1.4. Cross section of the compartments at cochlea and the organ of Corti [17].

1.1.2. Hearing Mechanism

Hearing is a process of converting acoustic waves into electrical signals that are transferred through the peripheral to the central auditory system. Figure 1.1 shows different parts of the ear that converts the time and frequency information of the sound pressure waves into electrical activities for stimulating the auditory nerve. The incoming sound pressure waves hit the pinna (outer ear), and the pinna funnels the incoming sound pressures to the ear canal. This causes the eardrum to vibrate according to the frequency of the sound and hence converts acoustic sound pressures to mechanical vibrations. Ossicles within the middle ear work as a lever mechanism and amplify the mechanical vibration energy applied to the cochlea via stapes. The stapes connects to the oval window, and is the smallest named bone in the human body. The end section of the stapes is termed as footplate, and attached to the oval window of the cochlea. When the stapes footplate pushes on the oval window, it causes movement of fluid within the cochlea.

In the inner ear, the cochlea transforms the mechanical vibrations to vibrations in fluid. Pressure variations within the fluids of the cochlea lead to displacements of basilar membrane. Figure 1.5 presents the effect of vibration at the basilar membrane hence the hair cells. When the basilar membrane is displaced upward, the hairs on the hair cells are bended according to applied shear force. This shear force triggers a series of

electrical and chemical reactions inside the hair cells. Outer hair cells provide positive mechanical feedback amplification, named as cochlear amplification. Inner hair cells generate electrical stimuli from fluid pressure. Therefore, the auditory nerve fibers are activated through the help of hair cells. Stimulation signals are transferred to the central auditory system, and finally incoming sound is heard.

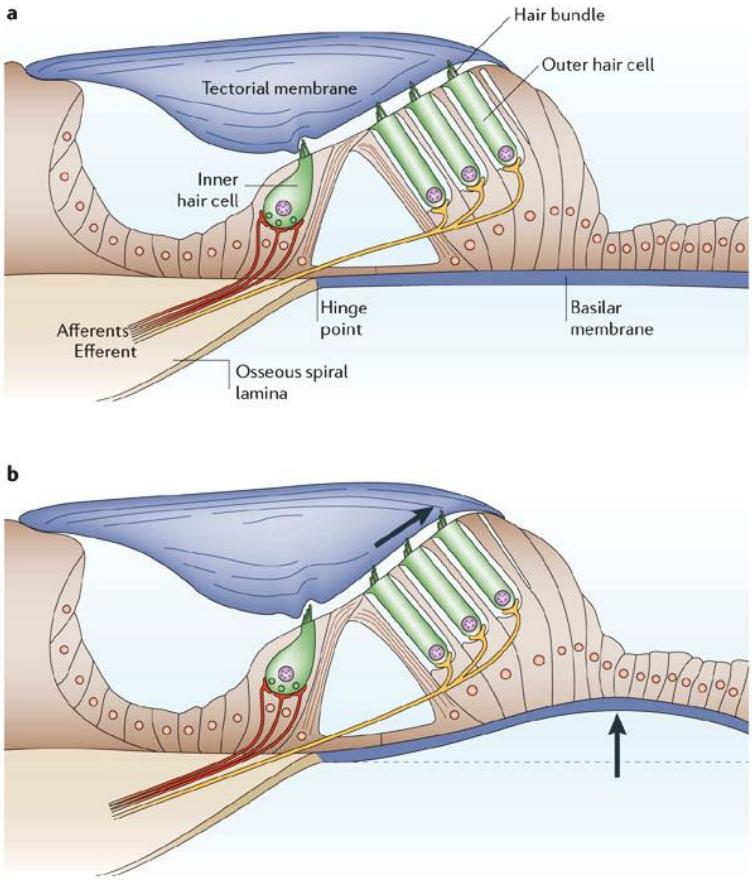


Figure 1.5. Basilar membrane vibration and its effect on organ of Corti [18].

Cochlea is responsible from the frequency discrimination of the incoming sound. Human peripheral auditory system is capable of sensing frequencies ranging from 20 - 20,000 Hz. Upon the vibrations of the oval window, basilar membrane starts to oscillate as well as the cochlear fluid. Depending on the frequency of the sound, specific portions of the basilar membrane resonate and resonating portion causes movement of the hair cells at that section. Figure 1.6 shows the frequency spectrum

of the human cochlea from base to the apex. Low-frequency sounds create traveling waves in the fluids of the cochlea that cause the basilar membrane to vibrate with largest amplitude of displacement at the apex of the basilar membrane. On the other hand, high-frequency sounds create traveling waves with largest amplitude of displacement at the base (near the stapes) of the basilar membrane. If the signal is composed of multiple frequencies, then the resulting traveling wave will create maximum displacement at different points along the basilar membrane. The cochlea therefore acts like a spectrum analyzer, and decomposes complex sound into its frequency components.

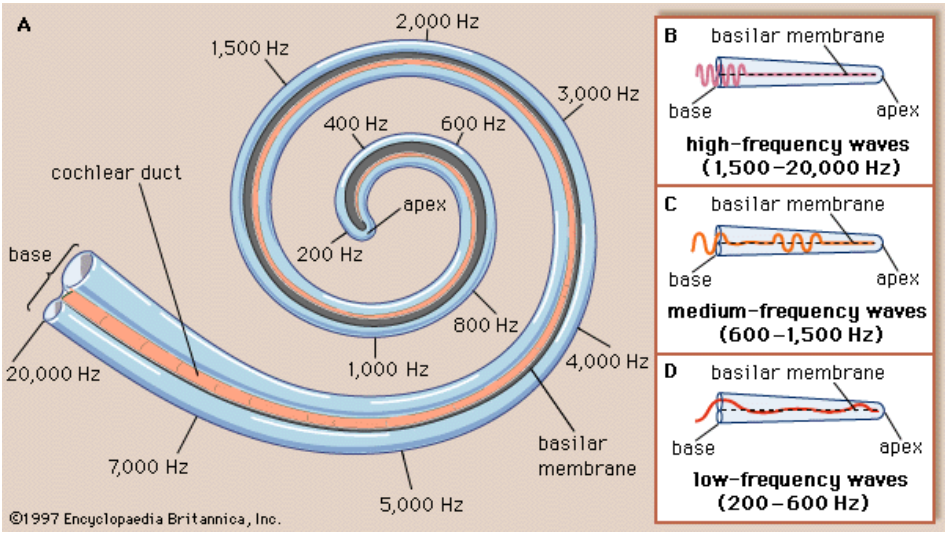


Figure 1.6. Frequency response of the human cochlea where different frequencies cause maximum vibration amplitude at different points along the basilar membrane [19].

1.1.3. Hearing Loss and Treatments

Hearing loss can be caused by many reasons where a person, which does not have good quality hearing perception, is said to have hearing impairment. Hearing impairment is grouped under two main subjects: *conductive hearing loss* and *sensorineural hearing loss*. Conductive hearing loss is induced from reduction of sound intensity during its travel from outer ear to the cochlea. The outer and middle ear are conducting the sound from the air to the cochlea. The sensorineural hearing

loss is reasoned by loss of conversion of mechanical vibration to neural impulses at cochlea [15], [20]. The traditional hearing aids are the most well known hearing loss treatment method, which occupies the largest market in this field. The hearing aids are utilized for the treatment of conductive hearing loss problems such as absorption of the sound at the eardrum or at the ossicles. The incoming sound is amplified through the hearing aid and delivered as sound waves to the outer ear. Therefore, the intensity loss of the sound is covered that provide treatment for moderate to serve hearing disorders [2], [21]. For the disorders at the vibration mechanism of the ear, i.e. eardrum and ossicles, middle ear implants are utilized, where incoming sound is detected by a microphone and converted into micro-vibrations via a transducer implanted at the middle ear [22], [23].

The principal cause of sensorineural hearing loss is damage or complete destruction of the sensory hair cells. If the hair cells are damaged, the auditory system has no way of transforming acoustic pressure waves (sound) to neural impulses, and that in turn leads to hearing impairment [24]. Figure 1.7 presents the anatomical view of the normal and deafened ears where the sensorineural hearing loss leads to loss of hair cells. In general, a small number of cells may remain for some patients, usually in the apical (low frequency) part of the cochlea. Fortunately, the cell bodies are far more robust [25], [26].

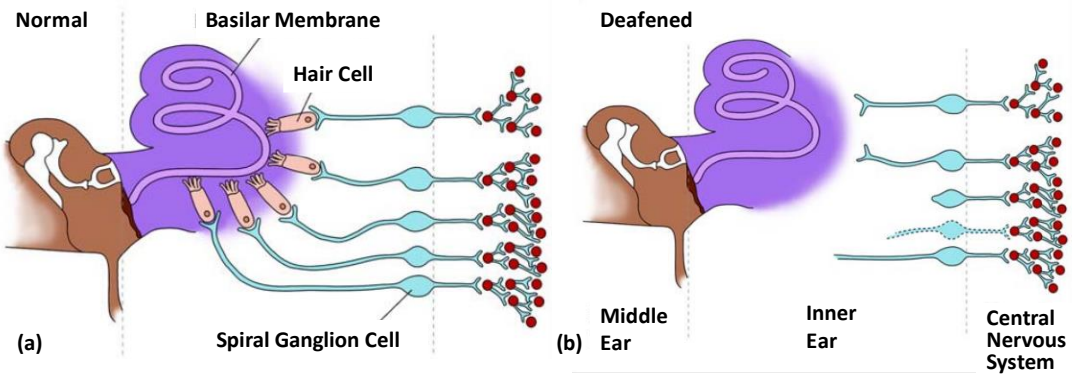


Figure 1.7. Anatomical view of (a) normal and (b) deafened ear with sensorineural hearing impairment [27].

Damage of the hair cells, that provides sensing of the vibrations at different frequencies, causes loss of fine-tuning of the incoming sound and leads to hearing losses from severe-to-profound level. This kind of hearing impairment can be fixed by Cochlear Implants (CIs) which take the sound as the input and convert it to electrical pulses for stimulation of the auditory neurons [27]–[29]. However, for the patients with ossified cochlea or no auditory neurons the CIs do not provide a solution. Therefore, Auditory Brainstem Implants (ABIs) that operates with a similar mechanism with CIs but directly stimulate the cochlear nuclei at the brainstem [30], [31]. Although, ABIs provide useful perception of the environmental sounds, CIs are the most successful neural prostheses where modern CIs aim to deliver high quality music perceptions [2]–[4]. Figure 1.8 presents treatment devices for the hearing losses. The hearing aids and the middle ear implants are utilized for conductive hearing loss whereas the cochlear implants and the brainstem implants are applicable for sensorineural hearing loss.

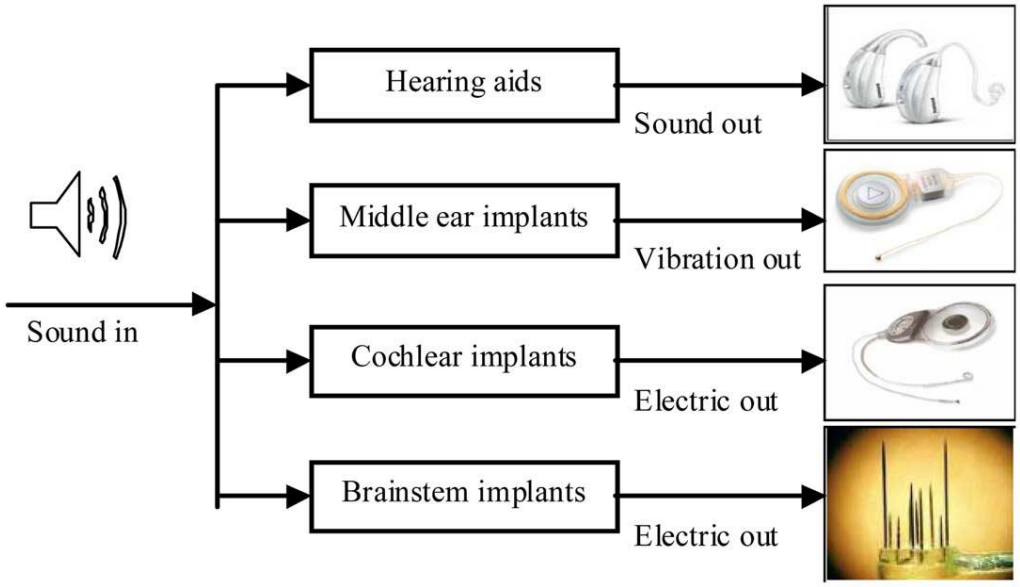


Figure 1.8. Hearing loss treatment methods through hearing aids, middle ear implants, cochlear implants and brainstem implants [2].

1.2. Cochlear Implants (CIs)

The cochlear implant is based on the idea that there are enough auditory nerve fibers left for stimulation. Once the nerve fibers are stimulated, they fire and propagate neural impulses to the brain. The brain interprets them as sounds. Figure 1.9 shows a typical modern cochlear implant system that converts sound to electric impulses delivered to auditory nerve. The ear external processor (1) with ear hook and a battery case (2) uses a microphone to pick up sound, converts the sound into a digital signal, processed and encodes the digital signal into a radio frequency (RF) signal. The antenna inside a headpiece (3) is held in place by a magnet attracted to an internal receiver (4) placed under the skin behind the ear. A hermetically sealed stimulator (5) contains active electronic circuits that derive power from the RF signal, decode the signal, convert it into electric currents, and send them along wires (6) threaded into the cochlea. The electrodes (7) at the end of the wire stimulate the auditory nerve (8) connected to the central nervous system, where the electrical impulses are interpreted as sound.

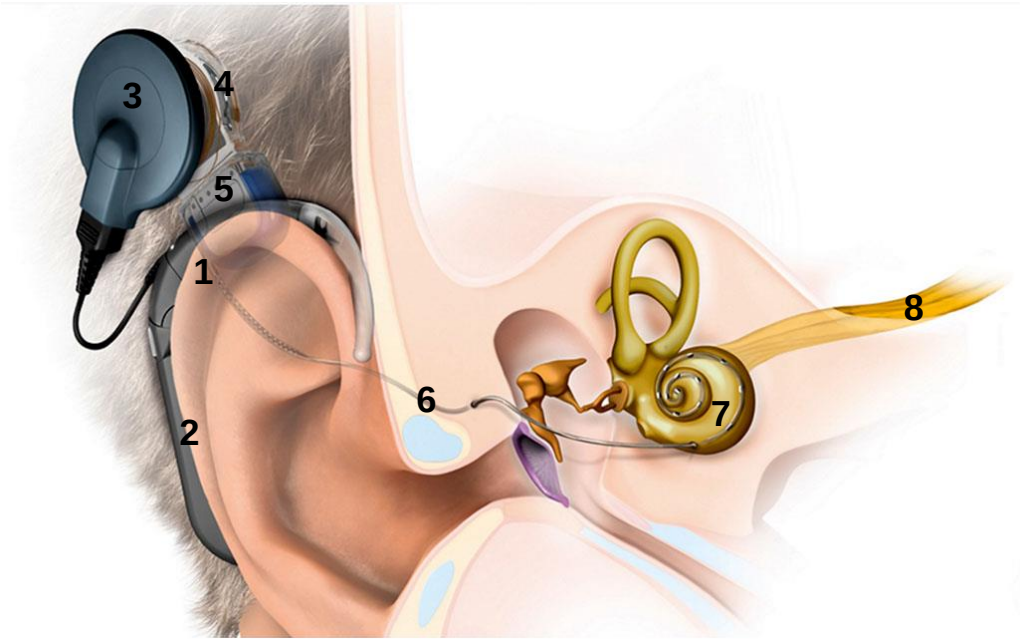


Figure 1.9. Typical modern cochlear implant system that converts sound to electric impulses delivered to auditory nerve [32].

Figure 1.10 shows the operational block diagram of a modern cochlear implant system. The overall system mainly composed of two units: external and internal units. The external unit includes a microphone that picks up the sound and converts to a digital signal. The digital signal then processed by a speech processor and encoded into an RF signal. The RF signal is sent to the transmitter coil with a power amplifier. The transmitted RF signal is received by a receiver coil at the internal unit. The information at the signal is then decoded and used for generating electric current at the stimulator. The generated electrical signals is sent to the appropriate electrodes which are wires threaded along the cochlea and used for stimulating the auditory nerves at the inner ear. The power required by the decoder and stimulator blocks is provided by a power unit, which uses the received RF signal to generate the required energy. The modern cochlear implant systems also include a patient fitting option to adjust the stimulation current level according to the patient. The speech processor holds the patient specific information that can be modified by a PC fitting program [2], [27].

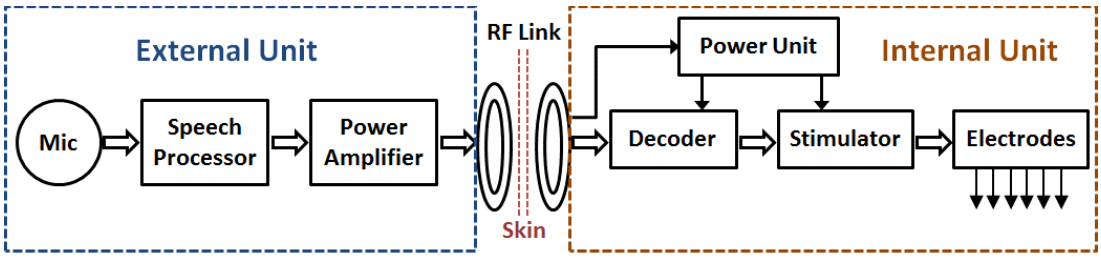


Figure 1.10. Operational block diagram of a modern cochlear implant.

All the conventional cochlear implant devices have the following features in common: a microphone that picks up the sound, a signal processor that converts the sound into electrical signals, a transmission system that transmits the electrical signals to the implanted electrodes, and an electrode or an electrode array (consisting of multiple electrodes) that is inserted into the cochlea by a surgeon. Different electrodes are stimulated depending on the frequency of the signal. Electrodes near the base of the cochlea are stimulated with high-frequency signals, while electrodes near the apex are stimulated with low-frequency signals. The signal processor is responsible for breaking the input signal into different frequency bands or channels and delivering the

filtered signals to the appropriate electrodes. The main function of the signal processor is to decompose the input signal into its frequency components, much like a healthy cochlea analyzes the input signal into its frequency components.

In the cochlear implant system, the stimulating strategy which is determined by the sound processor unit plays an extremely important role in generating the sounds heard by users. It functions to convert sounds into a series of electric impulses which determines which electrodes should be activated in each cycle. Many stimulating strategies have been developed over the past years such as advanced combinational encoder (ACE) [33], continuous interleaved sampling (CIS) [34], spectral peak (SPEAK) [35], and HiRes120 [36] strategies, which are frequently used in today's commercial cochlear implant. CIS is the most widely used sampling strategy in the latest devices which is also presented in Figure 1.9 [2], [27]. Figure 1.11 presents the block diagram and operation principle of CIS strategy. In this strategy, the sound is passed through bandpass filters with a number ranging from 5 to 20, each of which corresponds to a different electrode. Then, the output of each filter is fed to envelope detection stage. Envelope detection can be achieved with the help of a circuit consisting of a half-wave or full-wave rectifier with a low-pass filter; or by taking the Hilbert transform of the output of the bandpass filter. After that, the obtained temporal envelope is logarithmically compressed in the amplitude compression stage. Then, the biphasic pulse carrier whose pulse rate is predefined in each implant is modulated by the compressed envelope. In CIS strategy, the stimulation pulses of each electrode are applied in non-overlapping sequences so that no spatial channel interaction exists at the location of excitable nervous tissue. Since there is no simultaneous stimulation, only one current source is sufficient this strategy which also helps to decrease the power dissipation.

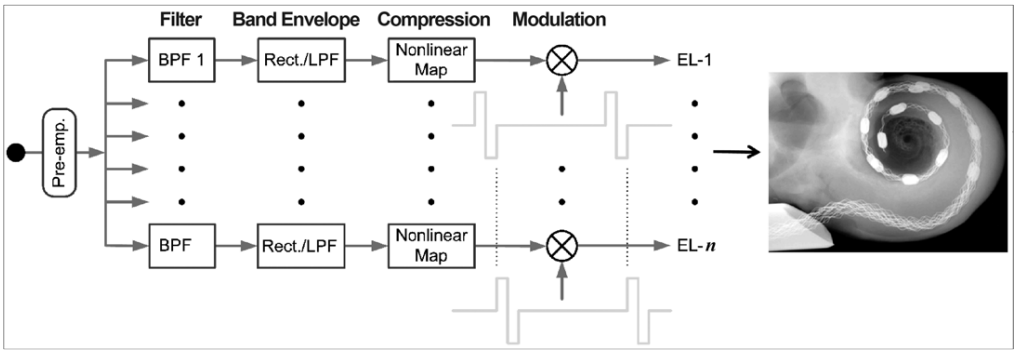


Figure 1.11. Block level representation of CIS strategy [27].

Improvements in sound-processing strategies, in the number of electrodes and channels, and in the rate of stimulation have yielded improved sentence and word recognition scores in patients. However one of the most critical issues for CIs is the power consumption and energy efficiency of the system. Cochlear implants are generally powered by an on-board battery which could be either disposable or rechargeable. The biological cochlea dissipates about 14 μW of power at regular operation which is estimated by impedance calculations [37], [38]. However, the power consumption of many commercial implant systems is around 40 mW where this requires regular daily recharging or replacing the battery [39]. The battery lifetime problem mainly arises from the power-hungry external sound-processing unit, which transmits the actuation signal to the implanted electrode via RF transmission. Furthermore, other electronic components utilized in conventional CIs (such as microphone, front-end filters) contribute to the power consumption. To overcome these problems, an autonomous, low-power, and fully implantable CI system is required.

1.3. Fully Implantable Cochlear Implants

Although CIs are the most successful neural prostheses, the requirement to wear an external processor that communicates with the implanted device via a radio-frequency coil increases the power consumption, limits the activities that can be undertaken while

wearing the device, leads to some patients feeling stigmatized and contributes to the high cost of these devices [10], [40]–[42]. Therefore, researchers in this area try to eliminate these problems via fully implantable, self-powered, and stand-alone cochlear prosthesis systems.

There are many studies in the literature for FICIs which are focused on the design of implantable sensor as a microphone to detect the incoming sound [7], [10]–[12], [43]–[45]. Although these sensors provide promising responses for sound detection, they gives all detected frequencies at the single output which requires electrical filters to process different frequencies. In a previous study in our group, Ilik *et al.* proposed a piezoelectric acoustic sensor that acts as a mechanical filter and senses incoming sound in certain frequency bands [46]. However, an interface electronics is required to use these implantable sensors as the hearing device where only limited number of study has focused on this research.

Sarpeshkar et al. proposed an ultra-low power cochlear implant processor as an analog bionic ear where the processor detects the inputs from electret microphone and generates digital control signals for neural stimulation [47]. Figure 1.12 presents block diagram of the bionic ear processor that drives 16 spectral channels. The interface senses 77 dB input dynamic range from electret microphone and amplified through a preamplifier. Then the signal is compressed to a 57 dB internal dynamic range through an automatic gain control (AGC). The amplified signal is separated into different frequency components through 16 bandpass filters where the filtered signal at each channel are envelope detected and applied to a logarithmical analog to digital converters (ADC). The ADC converts the input signal data into digital domain while compressing it into electrical range of the cochlea. Finally, the outputs of ADCs are sequentially scanned according to CIS stimulation strategy. Although the whole processor unit dissipates 211 μW, the obtained outputs require a digital to analog converter (DAC) to control the stimulation current. In addition, the system does not include a neural stimulation branch that operates with high voltage and most power hungry part of the neural stimulation systems.

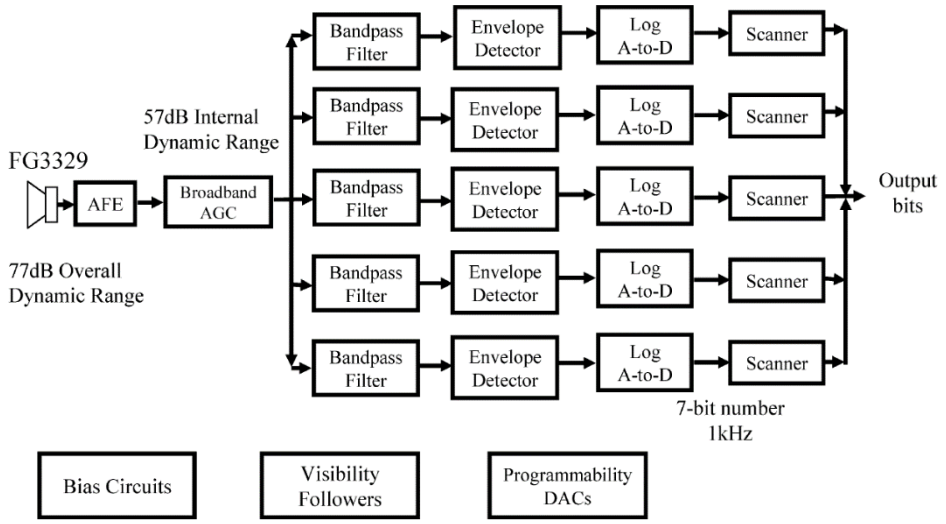


Figure 1.12. Block diagram of the analog bionic ear processer presented in [47].

Georgiou *et al.* proposed a totally implantable cochlear processer which senses the input data from electret microphone and drives off-chip high voltage neural stimulator [48]. Figure 1.13 (a) presents the block diagram of the FICI system presented in [48] where only the analog signal processing unit is explained in detailed. The proposed system operates with 16 channels where each channel has an analog processor unit as shown in Figure 1.13 (b). The processors first detect the microphone output through voltage to current converter (transconductor) unit, which has a controllable gain satisfied by a feedback from the automatic gain control (AGC) circuits. The generated current signal is provided to bandpass filters whose center frequencies are distributed in the human hearing range. The bandpass filters also includes clipping detectors that satisfies the input of AGC circuits. The filter outputs are then applied to a current limiter to prevent the large transients, which are faster than response time of the AGC. The limited current is full-wave rectified and low-pass filtered to determine the input power level at each channel. Finally, the current level is amplified through a current amplifier (current mirrors) and compressed to fit the 60 dB input dynamic range of the system to the electrical dynamic range (<20 dB) of the cochlea. The outputs of analog signal processor is the provided to a patient fitting and stimulation circuit where the proposed system operates with 4 V and can provides stimulation currents only at low

current levels. Although the processor unit operates with 126 μW, the system requires a high voltage stimulator to be used at more realistic cochlear implant applications.

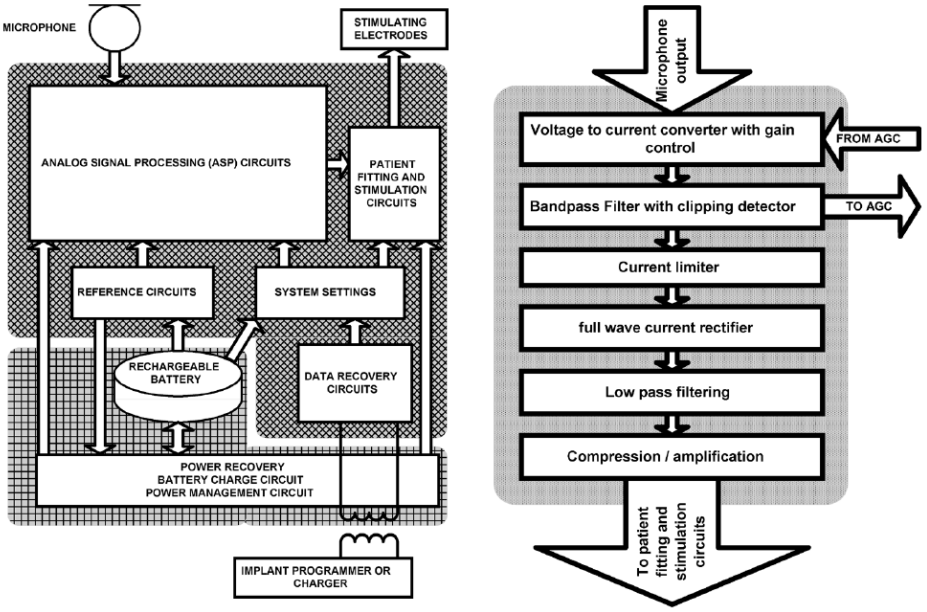


Figure 1.13. (a) Block level operation of totally implantable cochlear implant and (b) the analog signal processing unit for a single channel presented in [48].

Both of the cochlear implant circuits in [47] and [48] include optimizations for the front-end signal conditioning but not for the high voltage neural stimulation unit that delivers current pulses to the auditory neurons. More recently, an implantable low-power signal conditioning IC has been reported by Yip *et al.* for a piezoelectric middle-ear sensor [49]. Figure 1.14 presents the block diagram of FICI system on chip (SoC) where the circuit is divided into 3 main parts the piezoelectric sensor fron-end, the reconfigurable sound processor and the arbitrary waveform stimulator. The sensor front-end first detect the signals coming from middle-ear PZT sensor through a charge amplifier, then the signal is further increased by programmable-gain amplifier. The amplified signal is then provided to ADC that moves the signal to digital domain. At next stage the digital data is applied to reconfigurable sound processor that utilizes bandpass filters at the first stage to obtain different frequency components at the input. The filtered signal is then envelop detected and compressed

like in the previous FICI interfaces. The arbitrary waveform current stimulator at the last stage provides neural stimulation currents according to compressed data and patient fitting requirements.

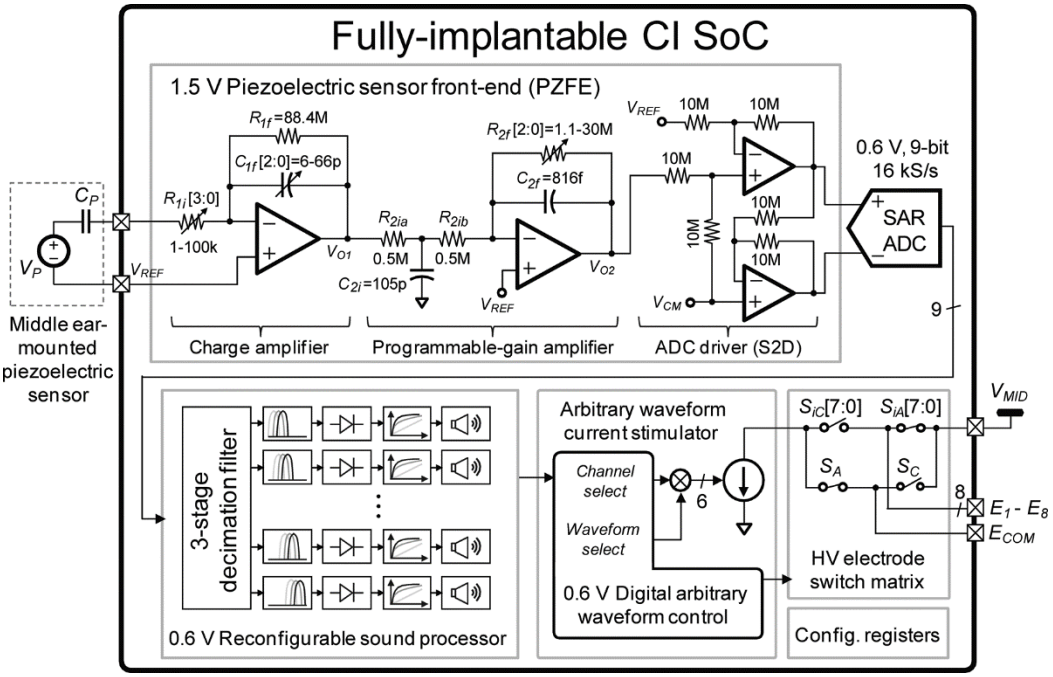


Figure 1.14. Block diagram of the FICI system on chip proposed in [49].

Although optimized stimulation pulse shape at the back-end of the FICI SoC leads to reduced system power dissipation of about 572 μW, the single-sensor architecture with 8 filters to isolate distinct frequencies results in a non-optimized front-end for power dissipation.

Jang *et al.* proposes a micro-electromechanical system that senses the input sound through mechanical filters and delivers electrical stimulation to the auditory neurons [50]. The proposed system utilizes artificial basilar membrane (ABM) as a mechanical filter to detect the input sound and generate electrical signals. The electrical signals are converted into neural stimulation pulses through a signal processor designed on the printed circuit board (PCB). The signal processor first amplify the mechanical filter outputs with a low noise CMOS op-amp and the amplified signal is converted into DC through a rectifier. The rectified DC voltage is then utilized as a reference

voltage to determine the amplitude level of the stimulation current. The stimulation current is applied as biphasic pulses where the stimulation pulse width can be arranged by clock pulse generator.

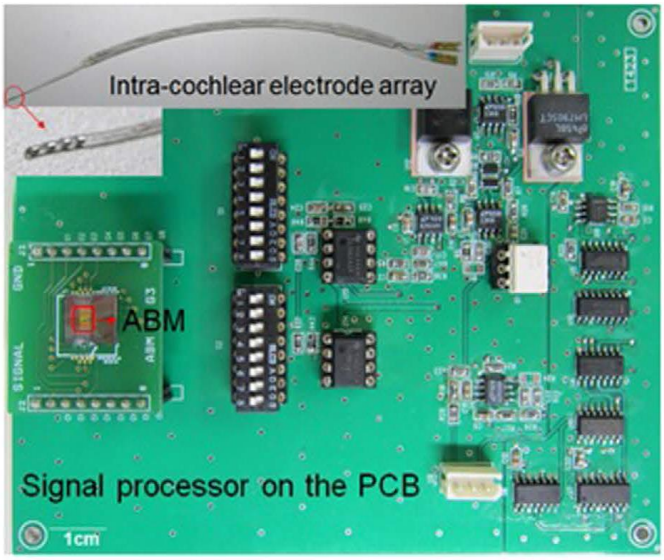


Figure 1.15. Proposed ABM and signal processor for neural stimulation circuit in [50].

Even though the proposed design in [50] provides operation of sound sensing and neural stimulation, the sound processor is implemented off-chip and is not optimized for important FICI considerations such as power dissipation, compression rate, stimulation current level, and patient fitting compatibility.

1.4. Objectives of the Thesis and Organization

The CIs are the key solution for sensorineural hearing loss where they provide sound perception by directly stimulating the auditory neurons. CIs are used for more than 40 years and today implanted in around 220.000 individuals worldwide. Recent studies on cochlear implants are focused on totally implantation of the devices to resolve the daily battery recharge/replacement requirement, damage risk of external components especially if exposed to water (shower, rain, swimming, etc.), and aesthetic concerns particularly for children and young adults. In the scope of

FLAMENCO (A Fully-Implantable MEMS-Based Autonomous Cochlear Implant) Project [51] a fully implantable and autonomous CI concept, exploiting the functional parts of the natural hearing mechanism and mimicking the hair cells via a set of piezoelectric cantilevers to cover the daily acoustic band. The cantilevers act as transducers for stimulating the auditory nerves via a low-power signal conditioning electronics and the cochlear electrode, and for recharging the battery via energy harvesting. The main objective of this thesis is to propose an ultra-low power mixed-signal circuit to detect the piezoelectric cantilever outputs and stimulate the auditory neurons. Design criteria for the signal conditioning interface electronics can be listed as follows:

1. The first and the most critical aspect for implantable devices is the power dissipation of the electronic circuits that determine lifetime of the system. The limited capacity of implantable batteries leads to ultra-low power requirement at the next generation FICI interface electronics that prolongs their operation.
2. The second criteria for the interface electronics is the low noise operation at the detection part. Since the low volume implantable sensors also have low amplitude at their output, the sensing stage of the interface electronics must operate with low noise to provide high sensitivity.
3. The input dynamic range of the CI is highly effective on the speech perception of the patient where input ranges above 50 dB provides enough range for perception of daily sound. The proposed design targets 60 dB input dynamic range to achieve good speech perception with high quality detection.
4. The FICI interface electronics includes neural stimulation circuit for stimulation of the auditory neurons. The stimulation current level at the output of the FICI system determines the minimum threshold and maximum comfort levels of the implant where these levels are changing from patient to patient. Therefore, the interface must include patient fitting compatibility to arrange these levels.
5. The stimulation current waveform shape is another aspect that figure-out efficient stimulation of the neurons. The proposed design utilizes exponential

biphasic current pulses instead of standard rectangular biphasic pulses to reduce the electrode voltage hence power dissipation of the system.

6. The area and volume of the interface electronics is limited by the anatomy of the ear where it must fit to the middle ear for a FICI system. Therefore, the interface electronics must be suitable for on-chip integration to provide low device size.

The remaining parts of the thesis is organized as follow: **Chapter 2** presents the 1st generation FICI interface electronics design that optimizes the front-end signal conditioning electronics rather than the stimulator part. The circuit senses 8 piezoelectric sensors' outputs and provide neural stimulation signal according to CIS stimulation strategy where only single channel performance has been designed for this generation. The front-end unit reduces power dissipation by combining amplification and compression of the sensor output through an ultra-low power logarithmic amplifier. The amplified signal is envelope-detected, and fed to a voltage controlled current source as a reference for stimulation current generation. The generated reference current is converted into biphasic pulses through a switch matrix that enables charge balanced current for safe stimulation of the neurons. The single channel performance has been tested with a thin film pulsed-laser deposition (PLD) PZT sensor for sound levels between 60-100 dB sound pressure level (SPL).

The design and validation of 2nd generation FICI interface electronics is presented in **Chapter 3**. The interface electronics senses 8 channel Piezoelectric (PZT) sensors, which are then processed by the proposed circuit to stimulate the auditory nerves consistently with the input amplitude level. The sensor outputs are first amplified and range-compressed through ultra-low power logarithmic amplifiers (LAs) into AC current waveforms, which are next rectified through custom current-mode circuits. The envelopes of the rectified signals are extracted, and are selectively sampled as reference for the stimulation current generator, armed with a 7-bit user-programmed DAC to enable patient fitting (calibration). Adjusted

biphasic stimulation current is delivered to the nerves according to CIS stimulation strategy through a switch matrix. Each current pulse is optimized to have an exponentially decreasing shape, which leads to reduced supply voltage, and hence ~20% lower stimulator power dissipation. The circuit has been designed and fabricated in 180nm high-voltage CMOS technology with up to 60 dB measured input dynamic range, and up to 1 mA average stimulation current. The 8-channel interface has been validated to be fully functional with 470 μW power dissipation, when stimulated by a mimicked speech signal.

Chapter 4 presents validation of the 2nd generation FICI interface electronics at a real application through in-vivo tests on a guinea pig. First, the hearing response of a healthy guinea pig is measured through auditory brain response (ABR) tests. Then the emission tests are carried to validate performance of the hair cells at cochlea. The guinea pig is deafened by applying high level sound for along time. Then ABR and emission tests of the deafened guinea pig is done to validate loss of hearing. To test the auditory neurons performance an electrical ABR (eABR) tests was conducted through a calibrated current source. Finally, the 2nd generation FICI interface electronics, which is driven by a low volume PZT sensor, is utilized to stimulate the auditory neurons of the deafened guinea pig. The obtained results are compared with the eABR and ABR measurements and FICI operation of the proposed interface electronics is validated.

Chapter 5 includes the conclusions of the thesis and include future works to be applied for improving the system performance of the FICI system.

CHAPTER 2

1st GENERATION FICI INTERFACE ELECTRONICS

The electronics of the conventional CIs are placed outside the body, and the processed signal is delivered to the electrodes by RF transmission. This is one of the key factors increasing the overall power dissipation. The proposed FICI system in the FLAMENCO project utilizes 8 PZT sensors to detect input sound and an integrated interface electronics process the sensor outputs which will be implanted to the middle ear. In this chapter, an ultra-low power and fully-implantable cochlear implant interface circuit is proposed in order to reduce power dissipation compared to aforementioned systems, and improve the signal conditioning simultaneously. The circuit senses signals from a set of piezoelectric cantilevers with different resonance frequencies, and stimulates the auditory neurons according to the power level and frequency of the input signal. The 1st generation FICI interface electronics mainly focused on improvements of front-end signal conditioning circuits without optimizing the neural stimulation part. The primitive goal of the design is to mainly operate in analog region without requiring analog to digital or digital to analog converters (ADCs or DACs) where previous reported FICI interface electronics operates in both region with higher power dissipation [49], [52]. In order to further limit the power dissipation of the circuits are mainly operates in subthreshold region with reduced power budget. The low volume of the middle ear limits the sensors size and output voltage of the sensors. Therefore, the front-end circuit has to operate with low noise to highly detect the input data. The organization of this chapter is as follows: The proposed circuit design is briefly described in next section and provides the sub-block details with design explanations. Section 3 presents FICI test results with a thin film piezoelectric sensor and gives the discussions.

2.1. Interface Circuit Design and Description

Figure 2.1 depicts the block diagram of the FICI system with 8 piezoelectric (PZT) sensors delivering signals at different frequency bands. Implantable PZT sensors generate low voltage signals from input sound due to their limited size. Thus, the first block of the interface is a Logarithmic Amplifier (LA). The dynamic range of daily sound of relevance is around 40 dB, but the electrical stimulation range of the diseased cochlea is below 15 dB [52]. The LA helps to both amplify the PZT sensor output and compress the input sound range to the electrical dynamic range of the cochlea. The compression was previously done by a compressor after the envelop detector. With the help of the LA the logarithmic compressor is eliminated which also leads to decrease power consumption of the system. The LAs enabled for 125 μs at each period since corresponding electrode only active at the given period. This also helps to decrease the power consumption of the circuit. The differential output of the LA is then envelope detected through a full-wave rectifier to obtain the sound level at each PZT sensor. The envelope detector output is sampled with a switch, and held stable as a reference to determine the amplitude of the stimulation current. The sampled signal is fed to the stimulation current generator block, which adjusts the current level to stimulate the auditory neurons. As the final stage, the stimulation current is converted into a biphasic pulse, and is transferred to the corresponding electrode (E_1-E_8) with the help of a switch matrix. The switch matrix control for biphasic current is provided by a High Voltage switch control block, which uses level shifters to generate high voltage switch control signals from the channel selection signals. The control block is more like the speech processor block in commercial cochlear implants that generates enable signals and activate electrodes according to CIS stimulation strategy. The utilized CMOS process technology was chosen as XFAB 180nm High Voltage process which includes both low voltage and high voltage transistors. Low voltage transistors are useful for low voltage operation at the front-end circuits where high voltage transistors are a must for stimulation stage where electrode voltages can reach to 10 V. Design and analysis of each sub-circuit is provided below.

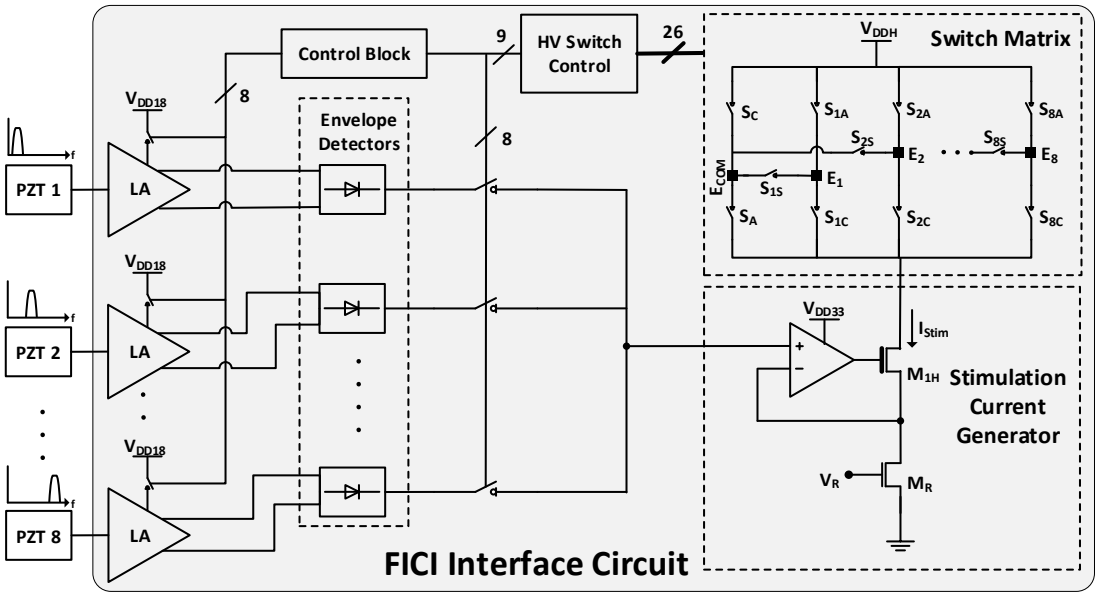


Figure 2.1. System architecture of 1st generation FICI interface electronics.

2.1.1. Logarithmic Amplifier (LA)

Previously reported cochlear implant interfaces compressed the input sound with a nonlinear function through a DC compression stage after the envelope detector, to cover all daily sound levels [27], [53], [54]. In the scope of this work, an LA has been designed as the first stage to both amplify and logarithmically compress the signal from the PZT sensor [55]. Dual function of the amplifier eliminates power consumption associated with the compression block in previous designs. The LA is composed of 5 stages as shown in Figure 2.2 (a) and provides high enough gain to detect the low voltage sensor output (<1 mV). As the input amplitude increases, each stage enters the limiting state (saturation) one by one from the 5th stage toward the 1st. Increasing the number of stages leads to higher power dissipation, and early saturation of the output voltage. The number of stages in the LA is hence optimized to simultaneously satisfy minimum voltage detection, input voltage range, and power dissipation requirements.

Figure 2.2 (b) presents the topology utilized at each logarithmic amplifier stage. Power consumption is managed through selective power gating of a lower supply voltage

(V_{DD}=1.8 V) compared to the rest of the FICI interface. When a particular channel is not sampled, the logarithmic amplifier is dynamically disabled through enable signal (V_{EN} in the figure) for power management. The low power and low frequency operation of the system leads to low DC droops, and low di/dt induced AC noise, which limits the fluctuations on the amplifier supply.

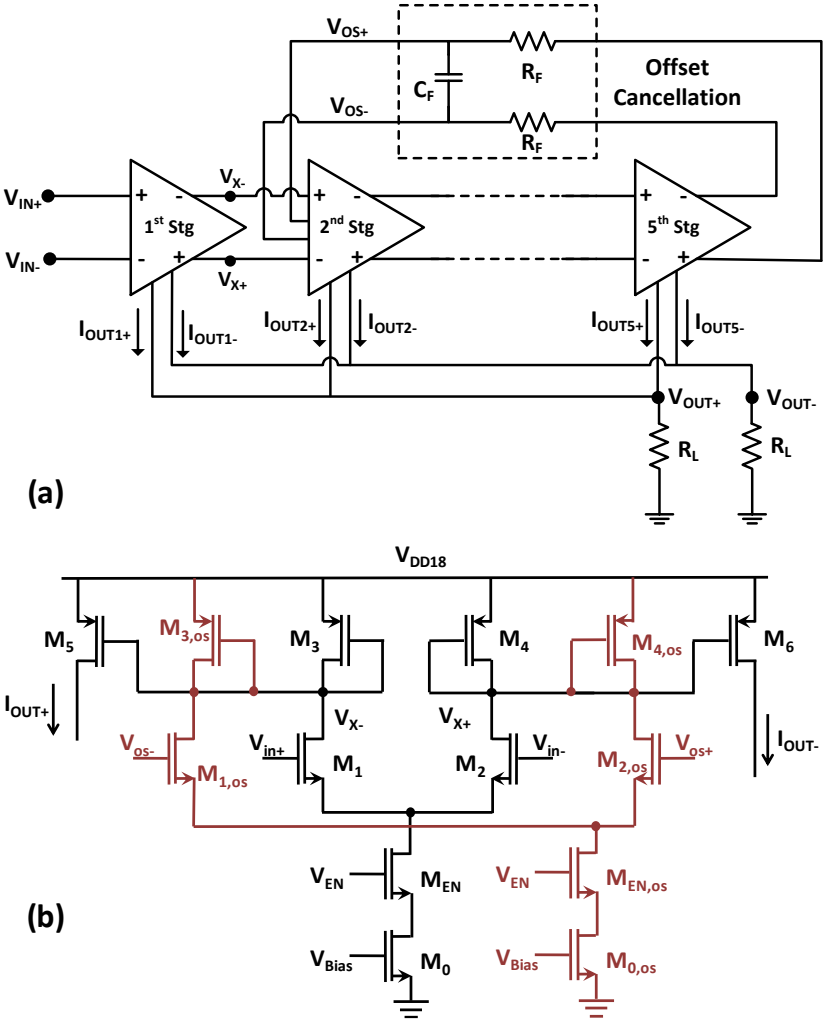


Figure 2.2. (a) Logarithmic amplifier circuit with offset cancellation feedback from the last stage to the 2nd stage, (b) Amplifier stage design, with the 2nd stage additions for enhanced offset cancellation highlighted in red color.

The differential output current from each amplifying stage (I_{OUT1-5}) is delivered to a resistive load through current mirrors (M_3-M_6), to be summed with the differential

output from the other stages. The input stage of each amplifier includes an isolated NMOS, which improves the gain through increased transconductance (g_m) for the same bias current and transistor size. The staging amplifiers operate in subthreshold domain for lower power dissipation, and include diode connected transistors as active load, which results in stage voltage gain of A_v (Eq. (2.1)). Total output voltage of the LA is given in equation (2.2).

$$A_v = g_{m1}/g_{m3} \tag{2.1}$$

$$V_{OUT} = R_L(I_{OUT1} + I_{OUT3} + I_{OUT3} + I_{OUT4} + I_{OUT5}) \tag{2.2}$$

where R_L is the load resistance and $I_{OUT,i}$ is the AC output current at each stage which is given in Eq. (2.3). The output current at each stage is proportional with the transconductance of the input transistors and the input voltage of corresponding stage. For subthreshold operation the transconductance of a MOSFET is given in Eq (2.4) where I_D is the drain current, n is the subthreshold slope factor and V_T is the thermal voltage [56]. The drain current, which is provided in Eq. (2.5), has exponential characteristic with respect to the gate hence the input voltage.

$$I_{OUT,i} = \left(g_{m,M1,2}\right)_i v_{in,i} \tag{2.3}$$

$$g_m = I_D/2nV_T \tag{2.4}$$

$$I_D = 2n\mu_e C_{ox}\frac{W}{L}V_T^2 e^{\frac{V_G - V_{TH}}{nV_T}}\left(e^{\frac{-V_S}{V_T}} - e^{\frac{-V_D}{V_T}}\right) \tag{2.5}$$

where μ_e is the mobility C_{ox} is the oxide capacitance, W is the width of the MOSFET, L is the length of the MOSFET, V_G is the gate voltage, V_S is the source voltage, and V_D is the drain voltage. As the staging amplifier saturated the effect of output current of the corresponding stage is no more related with the input voltage. Therefore, saturation of the cascade amplifier stages provides logarithmical compression of the output.

Feedback from the last stage is applied to the 2nd stage in order to cancel the effect of DC offset at the input. Figure 2.2 (b) highlights the offset cancellation enhancements (in red color) to the amplifier at the 2nd stage. Saturation of the stages causes clipping of amplifier output, and hence reduces the effect of offset cancellation, but built-in low-pass filter with low cut-off frequency in the feedback loop ensures continuous operation of the LA.

Subthreshold operation of the LA contributes to reduced noise level at the input. The total noise of a MOSFET can be modeled as given in Eq. (2.6), where first and second terms shows the drain thermal noise and gate voltage flicker noise, respectively [56].

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m} + \frac{K_f}{C_{ox}WLf} \tag{2.6}$$

where *k* is the Boltzman constant, T is operation temperature, g_m is transconductance of the MOSFET, and γ is the excess noise factor which is around 1/2 for weak inversion region. The empirical coefficient K_f for NMOS devices is essentially independent of bias, fabrication, and technology, while for PMOS devices, this coefficient is smaller and depends on biasing condition [56], [57]. C_{ox}, *W*, and *L* are technology and design parameters that represent the oxide capacitance, width and length of the MOSFET. *f* is the operation frequency.

The total input referred noise for the 1st and the 2nd stages of the amplifier is given in Eq. (2.7) and Eq. (2.8). The input referred noises of 3rd-5th stages are same with the first stage; hence the total input referred noise ($v_{eq,LA}^2$) can be expressed as shown in Eq. (2.9).

$$\overline{v_{eq,stg1}^2} = 2\left(\overline{v_{n,M_1}^2} + \frac{g_{m3}^2}{g_{m1}^2}\left(\overline{v_{n,M_3}^2} + \overline{v_{n,M_5}^2} + \frac{\overline{v_{n,R_L}^2}}{R_L^2 g_{m5}^2}\right)\right) \tag{2.7}$$

$$\overline{v_{eq,stg2}^2} = 2\left(2\overline{v_{n,M_1}^2} + \frac{4g_{m3}^2}{g_{m1}^2}\left(2\overline{v_{n,M_3}^2} + \overline{v_{n,M_5}^2}\right) + 2\overline{v_{n,R_F}^2}\right) \tag{2.8}$$

$$\overline{v_{eq,LA}^2} = \overline{v_{eq,stg1}^2}\left(1 + \frac{4}{{A_v}^4} + \frac{4}{{A_v}^6} + \frac{4}{{A_v}^8}\right) + \overline{v_{eq,stg2}^2}\frac{1}{{A_v}^2} \tag{2.9}$$

where A_v is the voltage gain at first stage as given in Eq. (2.1). Noise coming from the next stages can be reduced by increasing the voltage gain (A_v). When the voltage gain is larger than 10 V/V, the total input referred noise can be approximated as given in Eq. (2.10). The input transistors M_1 and M_2 are the most critical components that influence the input referred noise of the amplifier. The size of these MOSFETs are arranged to get higher transconductance hence lower thermal noise. The flicker noise of the circuit is reduced by using large gate area at M_1 and M_2. Moreover, high voltage gain leads to $g_{m1} >> g_{m3,5}$ and decreases the effect of M_3 and M_5 on the input referred noise. Figure 2.3 presents simulation at the variation of the input referred noise of the LA with frequency. Since the total input referred noise is integrated from 10 Hz to 10 kHz as 6.83 μV_{rms}, the amplifier provides safe operation for inputs >100 μV.

$$\overline{v_{eq,LA}^2} \approx \overline{v_{eq,stg1}^2} \tag{2.10}$$

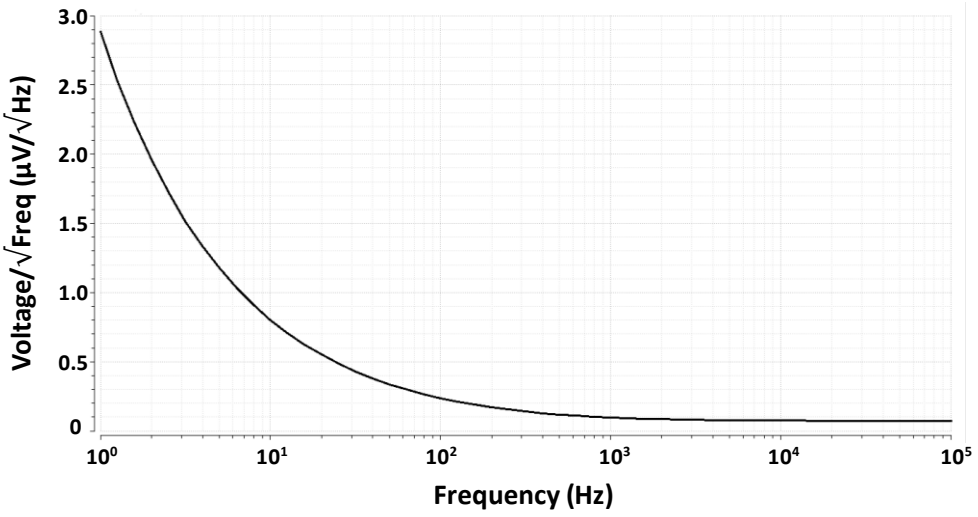


Figure 2.3. Simulation of the input referred noise density variation with frequency.

Figure 2.4 shows simulation result of the LA where the 60 dB input voltage range has been compressed to 22 dB output voltage range and the input voltage is amplified to enough level for compression. Moreover, the operation frequency of the circuit has no significant deviation up to 10 kHz. The designed amplifier dissipates less than 3 µW power from 1.8 V supply.

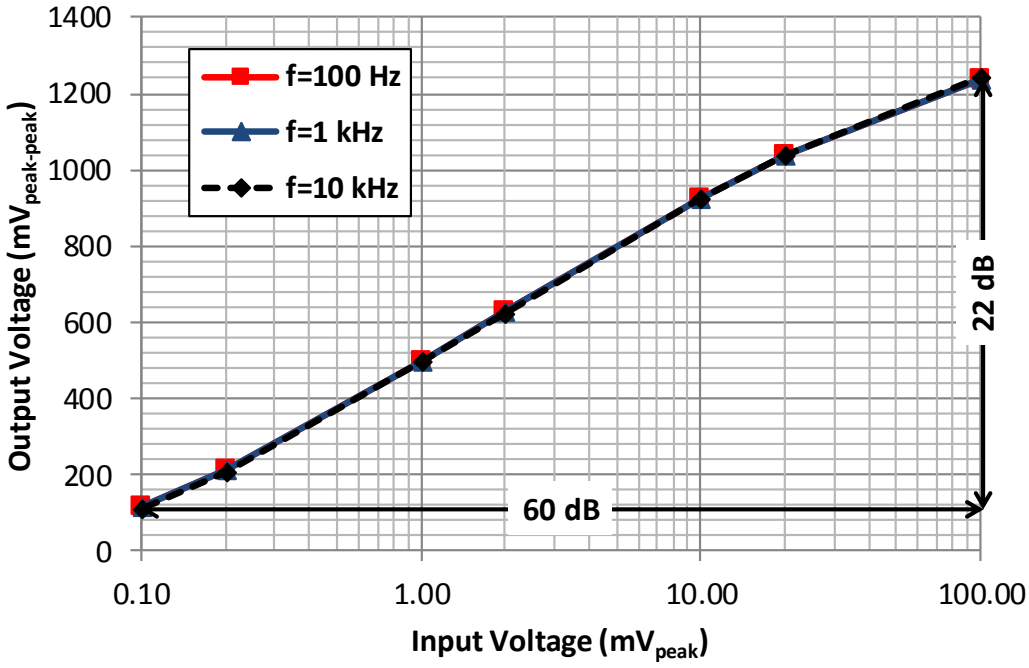


Figure 2.4. Input-output characteristics of the logarithmic amplifier for different input frequency levels.

2.1.2. Envelope Detector

The envelop detector at the next stage of the FICI system senses the amplitude of the signal from the amplifier and control the stimulation current level. The envelope detection can be achieved with either half-wave or full-wave rectification which are presented in Figure 2.5 (a) and Figure 2.5 (b). Half-wave rectifiers with a single diode have high output ripple. On the other hand conventional full-wave rectifiers have lower output ripple, but suffer from twice the voltage drop and higher power dissipation due to four-diode design.

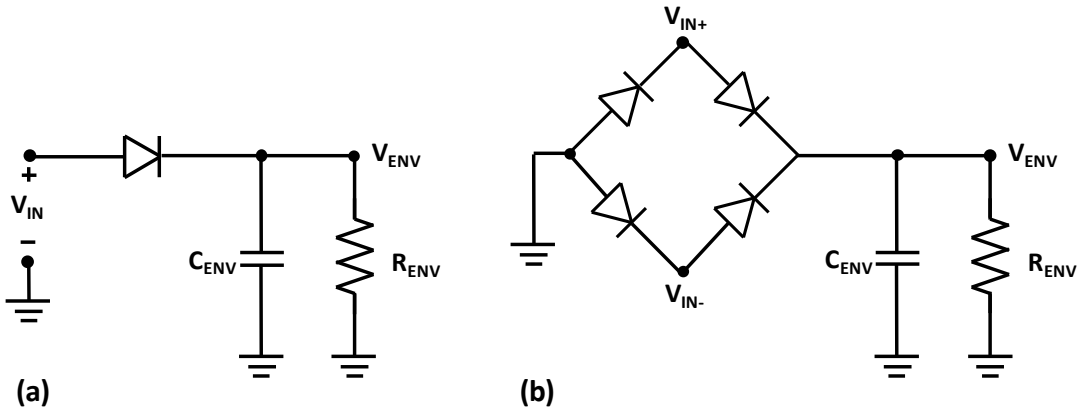


Figure 2.5. (a) Half-wave and (b) full-wave rectifier topologies.

The designed envelope detector can achieve full-wave rectification with only two diode-connected MOSFETs, as shown in Figure 2.6. The differential output of the previous stage provides both non-inverted and inverted outputs which enable the full-wave rectification. The operation principle of the envelope detector is as follow: When V_{AMP+} is positive, MOSFET M_1 turns ON to charge the envelope capacitor C_{ENV} up to peak voltage, minus a diode drop. When V_{AMP+} falls below C_{ENV} voltage, M_1 is turned OFF. V_{AMP-} signal is the inverse of V_{AMP+}, and works in a similar fashion. The passive structure of the envelope detector limits the power dissipation to voltage drops at diode-connected transistors. The voltage drop is minimized by using PMOS transistor that has lower threshold voltage and zero source-to-bulk voltage. Bulks of the PMOS transistors are shorted to their sources via bulk regulation transistors (M_{B1-B4}), which prevents the threshold voltage variation due to body effect. The envelope detector capacitor (C_{ENV}) and resistor (R_{ENV}) are arranged to have a cut-off frequency of 400 Hz which is close to the frequency of temporal pitch observed in daily life [24], [28]. The envelope detector output is sampled with a switch, and held stable as a reference to determine the amplitude of the stimulation current.

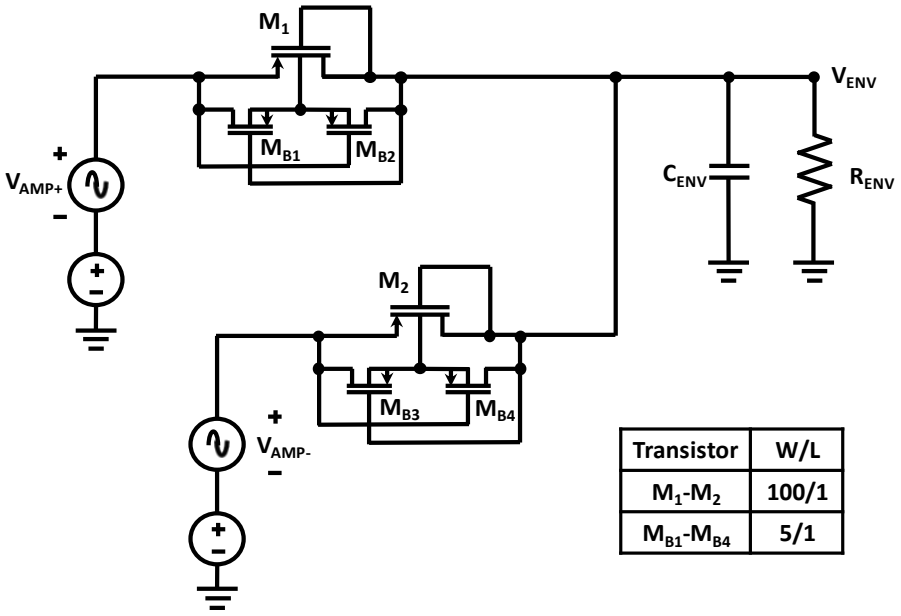


Figure 2.6. 2-Transistor full-wave rectifier circuit with bulk regulation capability.

2.1.3. Stimulation Current Generator

For the stimulation current generator a current source with a voltage controlled resistor (VCR) is designed which is shown in Figure 2.7. The stimulation current is determined by the envelope detector voltage V_{ENV} and the resistance of the M_R, which operates in linear region. Ghovanloo *et al.* shows the superiority of current source generator with voltage controlled resistor (VCR) and a feedback amplifier [58]. Figure 2.8 shows the most widely used current mirror topologies for stimulation where the output current is controlled by reference current. The output resistance of a simple current mirror, r_0, is not high enough for biomedical micro-stimulation applications, especially when it decreases at high currents, and causes the stimulus current to vary considerably with output voltage variations. Fully cascode (FC) and wide swing cascode (WSC) current mirrors, shown in Figure 2.8 (b) and (c), respectively, are used in many designs to increase the current source output resistance by a large factor ($g_m r_o$). The WSC current mirror is advantageous in terms of voltage compliance compared to FC structure. The voltage compliance of FC and WSC current mirrors are V_{DD}-V_{Dsat}-V_{TH} and V_{DD}-$2V_{Dsat}$, respectively. The designed voltage controlled

current source provides both high output impedance and high voltage compliance. The voltage compliance of this voltage-controlled current source can be as high as V_{DD}-V_{ENV}, if the OpAmp gain and the size of transistor M_1 are large enough. The output resistance of the designed current generator is given in Eq. (2.11).

$$R_{OUT} = Ag_{m,M_H}r_{o,M_H}R_{M_R} \tag{2.11}$$

where A is the open loop voltage gain of the feedback amplifier, r_{o,M_H} is the output resistance of M_H transistor, and R_{M_R} is the resistance of voltage controlled resistor. High gain of the feedback amplifier provides higher output for the current generator which results in lower load sensitivity for the stimulation current. Figure 2.7 also depicts the utilized single stage active loaded differential amplifier for feedback, which provides about 50 dB voltage gain. The amplifier is supplied by 3.3 V to provide enough voltage for driving the high voltage M_H transistor that is connected to the high voltage switch matrix. The negative feedback at the amplifier equalizes drain voltage of M_R to the input voltage (V_{ENV}); hence the generated stimulation current is $I_{stim} = V_{ENV}/R_{M_R}$. The maximum and minimum stimulation current level can be customized for the patient by controlling the gate voltage of M_R.

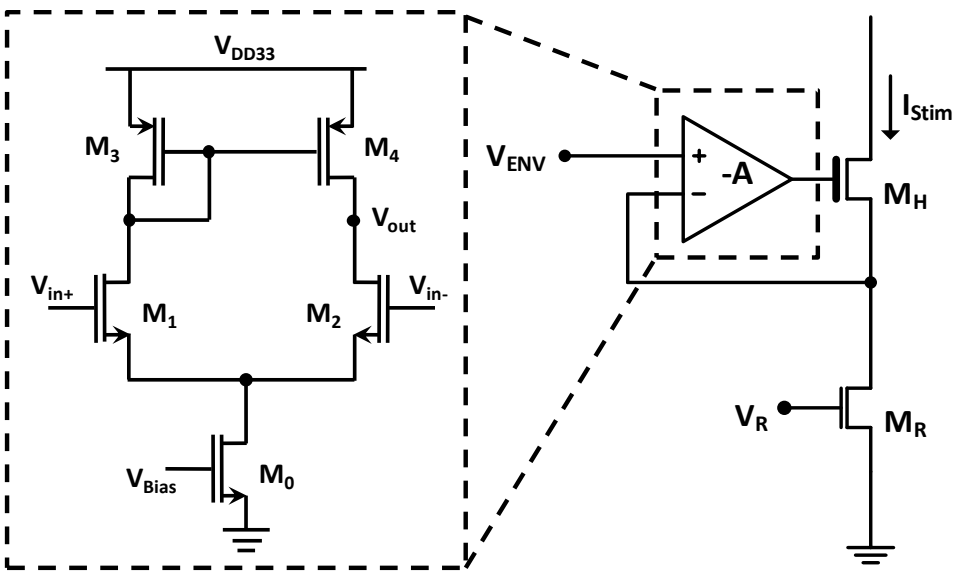


Figure 2.7. Schematic diagram of stimulation current generator with VCR.

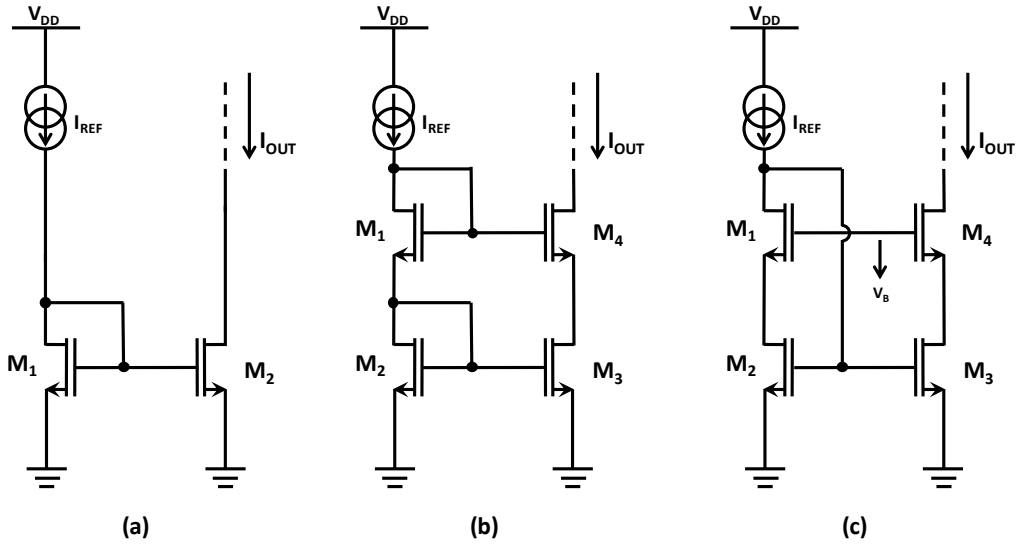


Figure 2.8. Schematic of the (a) simple current mirror, (b) fully cascode current mirror, and (c) wide swing cascode current mirror.

2.1.4. Switch Matrix

As the final stage, the generated stimulation current is converted into a biphasic pulse, and is transferred to the corresponding electrode (E_1-E_8) with the help of a switch matrix. Figure 2.9 (a) depicts schematic diagram of the switch matrix used to drive Electrode 1, and the biphasic stimulation current generated through the control of this matrix in time domain. $S_{1,A}$ and S_C in the switch matrix are PMOS switches whereas $S_{1,C}$, $S_{1,S}$, and S_C are NMOS switches. The switch matrix provides biphasic current pulse as shown in Figure 2.9 (b). The anodic pulse is generated by turning ON $S_{1,A}$ and S_A while the cathodic pulse is propagated through $S_{1,C}$ and S_C. The load driven by the switches is the electrode tissue impedance, which is modeled as a series resistor-capacitor pair (R_S=1kΩ~10kΩ, C_d=1nF~10nF) [49], [59]. Switch $S_{1,S}$ is utilized to remove the charge on the capacitor at the load, and prevents the charge imbalance at the electrodes by shorting them to the common electrode (E_{COM}) when they are disabled. The switch matrix is powered by a high voltage supply (V_{DDH}=7-10 V) to deliver sufficient voltage to the stimulation electrodes. The stimulation electrode is driven according to the well-known Continuous Interleaved Sampling (CIS) sound

processing strategy, which provides sequential interleaved stimulation of the electrodes at fixed frequency and delivers better performance compared to other synchronous implementations [60], [61]. The control of the switch matrix and the enable signals are generated by the control block which is designed by sequential and combinational logic CMOS circuits.

Figure 2.10 shows simulation result of the generated biphasic current pulses from the stimulation current generator and the switch matrix circuits. As the envelope detector voltage increases the amplitude current level also increases. The amplitude of the current pulse can also be controlled by the gate voltage (V_R) of the M_R transistor and can be increased up to 500 μA.

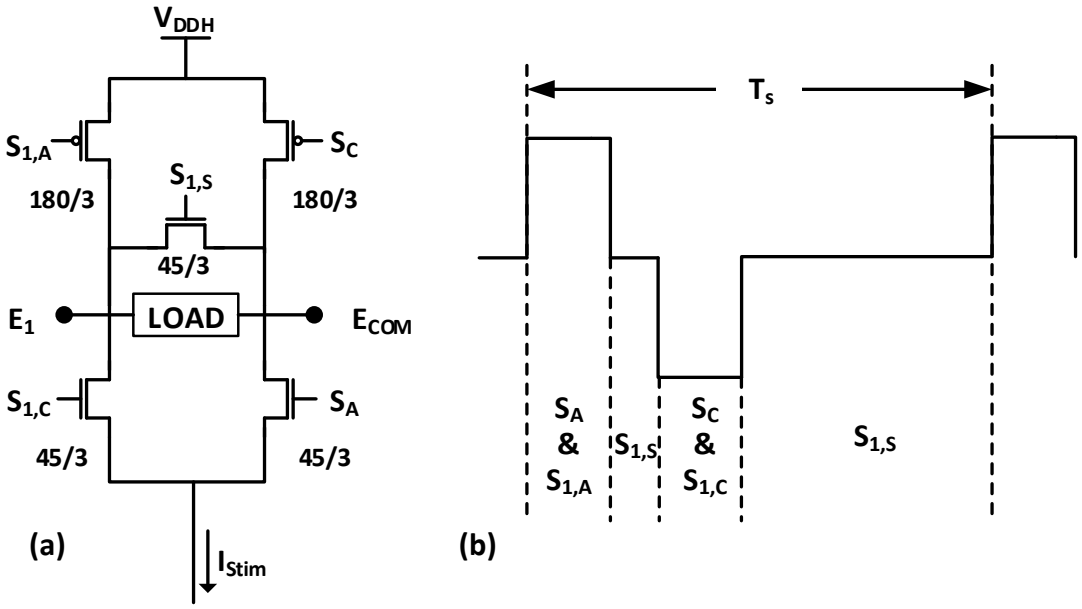


Figure 2.9. (a) Switch matrix utilized at Electrode 1, and (b) generated biphasic stimulation current.

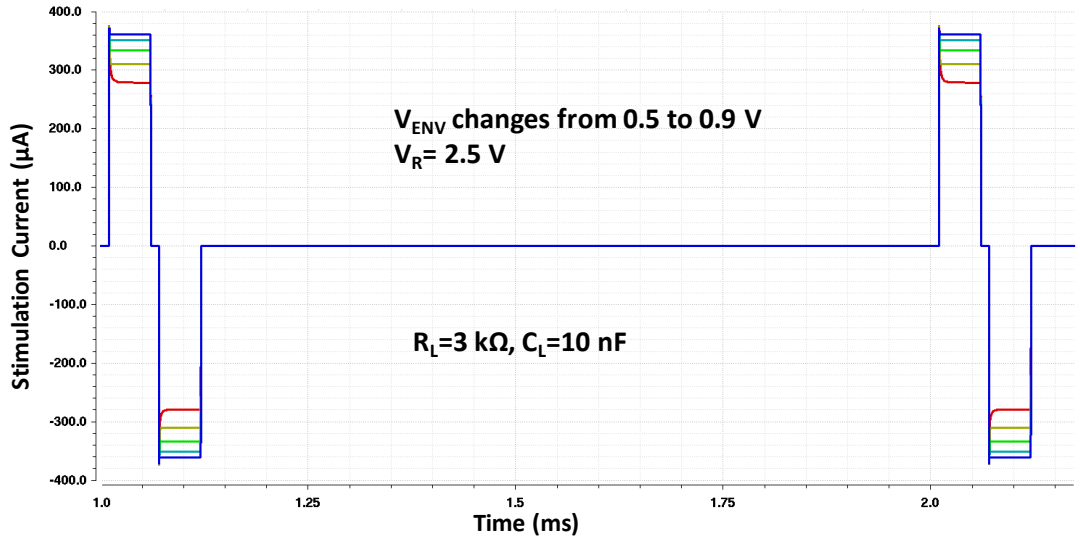


Figure 2.10. Simulation result of the generated biphasic current pulse from stimulation current generator and switch matrix circuits for different envelope detector voltages.

2.2. Test Results and Discussions

The FICI interface circuit was designed and implemented in XFAB 180nm high-voltage CMOS technology. Figure 2.11 presents the die micrograph of the implemented FICI interface circuit, where layout of the 1-channel neural stimulation circuit is highlighted. The remaining parts of the die are utilized for test circuits and includes design of Salar Chamanian that are designed in the scope of FLAMENCO project. The fabricated chip was packaged to a CQFP84 and a test PCB is designed to conduct proper tests of the chip. Figure 2.12 presents the designed and implanted test PCB for the tests of the stimulation circuit where packaged interface electronic is placed on the middle of the PCB. The implemented chip is designed in a testable manner all the sub-blocks can be tested individually. Moreover, the designed PCB is also compatible with testability of the chip and provide comfortable testing of the design.

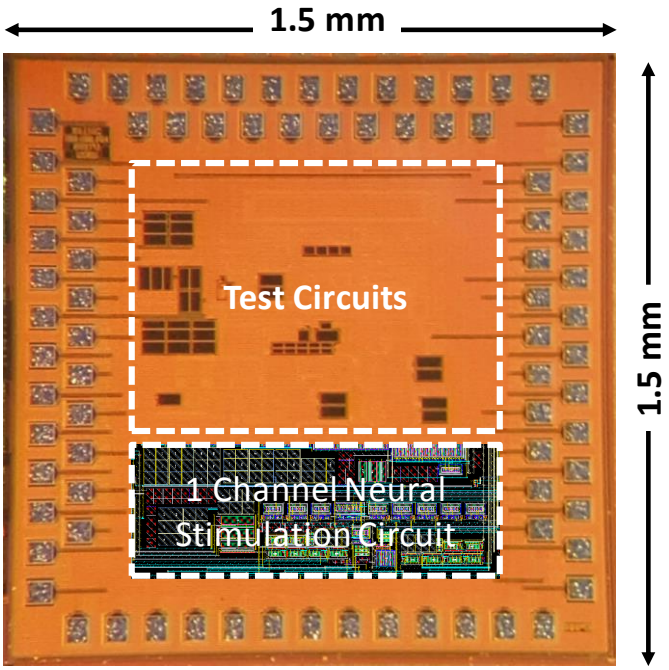


Figure 2.11. Die micrograph of designed and implemented FICI interface circuit.

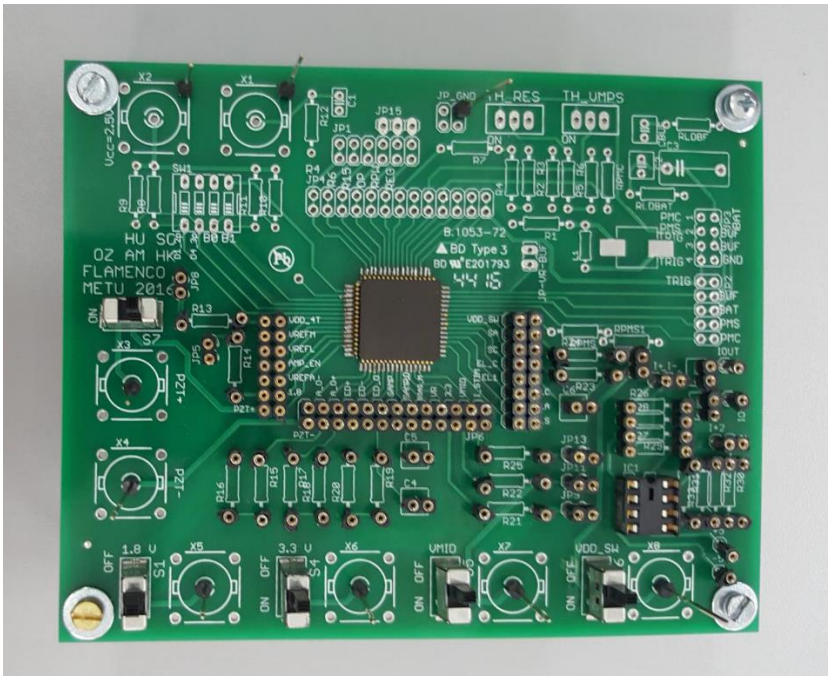


Figure 2.12. Test PCB of the 1st generation FICI interface electronics.

As the first step, the performance of amplifier was tested for varying input voltage and frequency conditions. The logarithmic amplifier not only amplifies the sensed voltage at the input, but fits the input voltage range to the electrical dynamic range of auditory neurons as well. Figure 2.13 shows the input-output characteristics of the logarithmic amplifier that compresses 40 dB input voltage to 12 dB of the output. The compression is done according to $y = Cln(x) + D$ where the compression ratio is determined by *C*. The trendline shows that LA output is linearly changing with the logarithm of the input. Although the simulations provide wider input dynamic range the obtained test results provide limited compression range which is still enough to capture daily sound levels. The amplifier has been tested at different frequencies. The validated bandwidth of the amplifier is high enough to provide frequency independent performance. The amplifier output has no significant deviation up to 5 kHz, covering the frequency band for daily speech. Since daily sounds are not observed at high frequencies, the amplifier design provides a favorable trade-off between bandwidth and power dissipation.

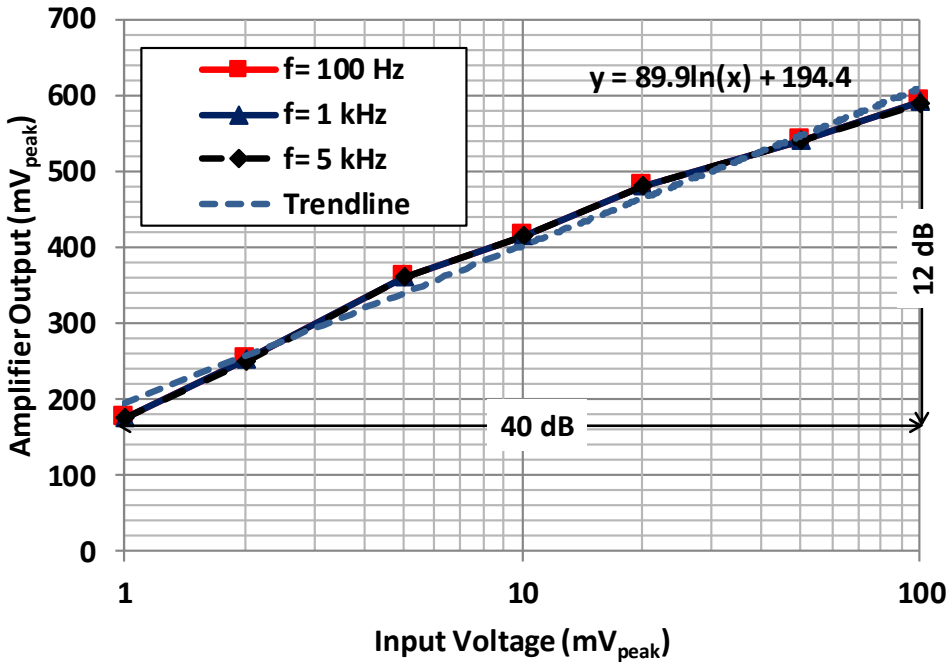


Figure 2.13. Output voltage variation of the logarithmic amplifier with respect to the input peak voltage at different frequencies.

The single channel performance of the FICI interface circuit has been tested with a thin film PLD PZT sensor to provide a proof of concept. Figure 2.14 shows the test setup of the design. The input sound of the testing system is generated by a speaker which is driven by a signal generator to control the sound frequency and level. The generated sound level by the speaker has been measured by sound dB meter. The incoming sound vibration has been detected by the PZT sensor on a parylene membrane and converted into electrical signal. Size of the sensor is adjusted to be 5x5 mm^2 which can be implanted on the eardrum or on the umbo at middle ear [14], [62]. The fabrication process of the sensor is similar with the one explained in [63]. Moreover, a more compact design that fits 8 PZT sensors to the volume of the middle ear has been proposed in [46]. Figure 2.15 presents frequency response of the PZT sensor attached on the membrane at different input sound levels. The resonance frequency of the PZT sensor is 1330 Hz. The sensor output at resonance frequency changes from 1 mV to 100 mV at a range of 60-100 dB SPL. The sensor output is then fed to the FICI interface on the testing board which is powered by a DC source. Test results of the FICI interface are observed with the help of a digital signal oscilloscope.

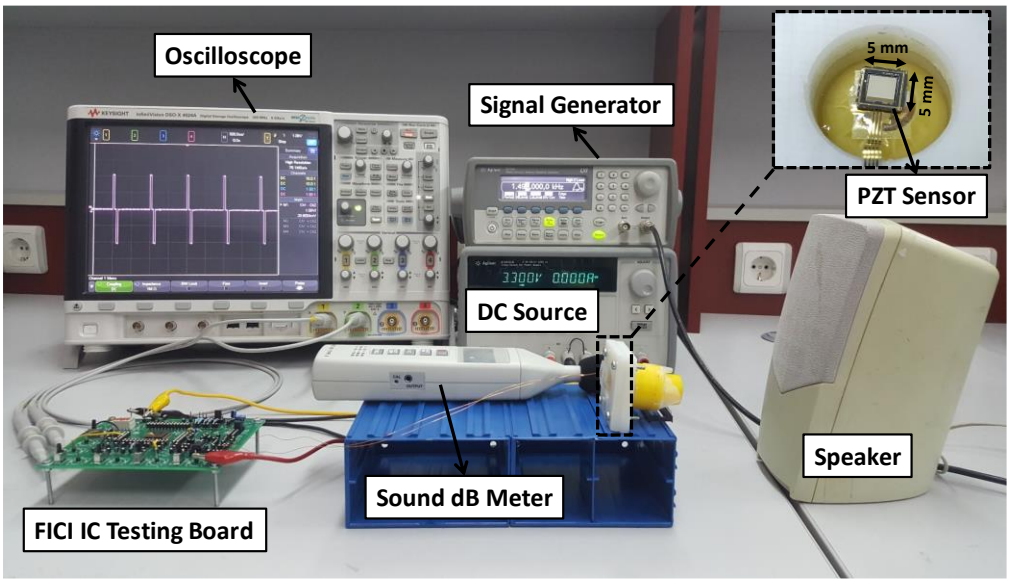


Figure 2.14. Test setup of the single channel FICI interface circuit with a thin film PZT sensor that fits on the eardrum.

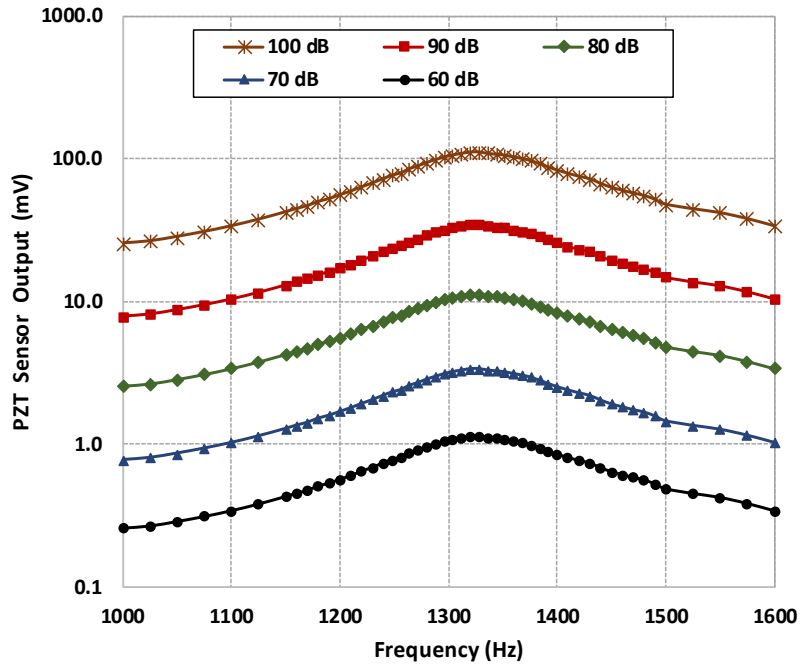


Figure 2.15. Frequency response of the thin film PLD PZT sensor on the parylene membrane.

The neural stimulation performance of the FICI is then tested with an artificial neural load (R_s=3 kΩ and C_d=10 nF). Figure 2.16 shows neural stimulation current generated at Electrode 1, for different input sound levels at the resonance frequency of the PZT sensor. The generated biphasic pulses have linear response with the input sound level. The stimulation current amplitude changes between 110 and 430 μA, which represent the threshold and comfort levels. The stimulation generator is programmed to yield 1000 pulses/s with 50 μs of biphasic pulse width per phase.

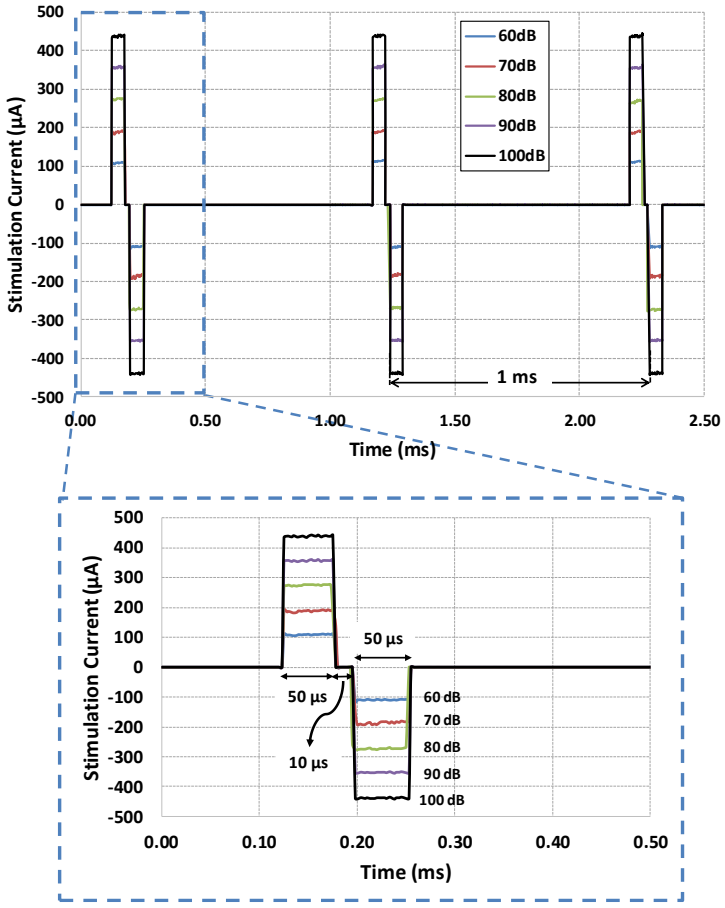


Figure 2.16. Stimulation current generated by the FICI interface electronics when fed with a thin film PLD-PZT film PLD PZT sensor attached on the parylene membrane.

Table 2.1 shows power consumption for various blocks in the FICI system. The logarithmic amplifier, envelope detector and control unit operate with 1.8 V supply voltage. The average power dissipation of the logarithmic amplifier in one period is less than 3 µW due to the implemented power management scheme. The stimulation current generator operates with standard 3.3 V supply to drive M_{1H} with a sufficiently high voltage, and provides wide operation range for this high threshold transistor. The switch matrix that actuates the stimulation current requires at least 7 V in order to accommodate the high impedance of the electrode-tissue interface. The high voltage switch control circuit is hence supplied with 10 V in this implementation in order to completely turn the switches ON and OFF, and prevent leakage to the auditory neurons. Different supply voltages can be utilized at the FICI system through power

management circuits with DC-DC converters, which is out-off scope of this study. The front-end signal conditioning circuit, excluding the stimulation current, dissipates only 25.43 and 51.2 μW at single and 8-channel operation, which is the lowest value in literature to the best of our knowledge. Total power dissipation of the single and 8-channel circuit at 110 μA stimulation current is 105.43 and 691.2 μW, respectively. Implantable neural stimulator systems can be powered by Lithium/Manganese Dioxide ($LiMnO_2$) batteries with 3.3 V nominal voltage and 300 mAh/gram gravimetric capacity density [64]. Using a power management circuit with a modest 70% power conversion efficiency, total power dissipation of the neuralstimulator can be kept below 1 mW. The proposed system can thus operate for 37 days on a 1 gram battery.

Table 2.1. Power consumption of the 1st generation FICI interface electronics.

System Components	Supply Voltage (V)	Power (μW)	
		1-Ch	8-Ch
Logarithmic Amplifier	1.8	0.35	2.8
Envelope Detector	1.8	0.38	3.0
Control Block	1.8	20.0	20.0
Stimulation Current Generator	3.3	1.7	5.2
Switch Matrix (Stimulator)	7-10	80	640
HV Switch Control	10	3	20.2
Total		105.43	691.2

Table 2.2 presents comparison of the FICI interface with the state-of-the-art. The input dynamic range of the proposed design is slightly lower than the previously reported interface circuits, but provides sufficient range to cover daily sounds [65], [66]. The input dynamic range of the circuit is designed according to the range of the targeted PZT sensor. The input dynamic range of the amplifier can be increased by extending the gain and cascaded stage numbers if the system dynamic range is targeted differently, but there is likely to be a power dissipation penalty. Neural stimulation

consumes 479 μW in [49] using non-rectangular stimulation waveforms. The proposed FICI interface in this work dissipates 640 μW with regular biphasic pulses. This can be further decreased by optimizing current waveform shape, which is not the focus of this work. Most of the previously reported studies operate both in analog and digital domains to obtain filtering and compression of the incoming sound, whereas the proposed design eliminates digital filter and compression blocks. Therefore, the proposed circuit does not require ADC and DAC blocks to switch between analog and digital domains. The front-end signal conditioning circuit, which is the main focus of this design, has the lowest power consumption compared to the previous studies due to the circuit reduction and power optimization techniques detailed in previous sections.

Table 2.2. Comparison of 1st generation FICI interface electronics with state-of-the-art.

Parameters	Sarpeshkar TBME05 [47]	Georgiou JSSC05 [48]	Yip JSSC15 [49]	**This Work**
Technology	1.5 μm	0.8 μm	180 nm	180 nm
Number of Electrodes	16	16	8	8
Operation Domain	Analog + Digital	Analog	Analog + Digital	**Analog**
Dynamic Range (dB)	77	45	59	40
Front-End Power (μW)	211	126	93	**51.2**
Stimulator Power (μW)	-	2000*	479	640

To sum up, an ultra-low power FICI interface circuit has been proposed, which senses multiple signals from PZT sensors with distinct resonant frequencies, and stimulates the auditory neurons with biphasic stimulation current. The logarithmic amplifier (LA) array carries out the amplification and compression of the signals from PZT sensors. Amplification and compression are separately implemented functions in previous cochlear implant designs with higher aggregate power dissipation. Each LA is powered by the lowest supply voltage in the system when active, and is otherwise

power-gated to further reduce both active and idle power dissipation. The neural stimulation performance of the interface circuit has been tested with a thin film PLD PZT sensor while driving an artificial neural load. The system provides 110 μA stimulation current for 60 dB of input sound, which is the threshold stimulation level of the system, and the comfort level of 430 μA for 100 dB SPL. The minimum power dissipation of the front-end and overall FICI interface is 25.4 μW and 105.4 μW respectively for single channel. For 8-channel operation, the front-end circuit dissipates 51.2 μW, and the full circuit dissipates 691.2 μW.

While the front-end circuit achieves the lowest power dissipation in the literature, full circuit power dissipation has to be further decreased. Moreover, the patient fitting compatibility of this system requires a DAC to operate properly. Finally, the input dynamic range of the system can be further increased to obtain better speech perception. The 2nd generation FICI interface electronics which is explained at the next chapter is focused on improving overall performance of this system by applying novel analog and digital circuit techniques.

CHAPTER 3

2nd GENERATION FICI INTERFACE ELECTRONICS

The previous generation provides one of the lowest front-end signal conditioning circuit for the FICI interface electronics, however the most power hungry part of the system is the neural stimulation part which dissipates more than 90% of the total power. Therefore, in addition to front-end circuit improvements, the 2nd generation FICI design focused on power reduction at the stimulator part of the circuit. Although, power is one of the most critical parameter for implantable medical devices, it is not the only criteria to be considered. Hence, the new generation design also provides wider input dynamic range to detect the daily sounds, includes patient fitting capability that calibrates the implant according to patient needs, and high stimulation current compatibility for wider load operation.

In the 2nd generation design a bionic ear interface is proposed, which includes power optimized current-mode circuits to process the acoustic sensor voltage, and stimulate the auditory neurons through efficient current waveforms with the lowest system power dissipation to date. The input sound is sensed by the low-volume 8-channel PZT transducer operating with high sensitivity. The sensed signals are compressed into dynamic range of the auditory neurons, which are then stimulated by the current pulses at the desired frequency and power level. The proposed interface was tested with a mimicked speech signal that validates operation of the system at a real application. The organization of this chapter is as follows: The design specifications of the interface electronics is provided in next section. Section 2 includes the details of the interface, which is followed by further discussion of neural stimulation scheme in Section 3. Section 4 presents the test results and discussions.

3.1. Design Criteria and Specifications

Before going deep details of the design the specifications and limitations of the system must be included that shows the necessity of the improvements compared to previous design. The proposed interface electronics is designed in the scope of FLAMENCO Project [51] which is an implantable bionic ear as shown in Figure 3.1. Operation principle of the system is as follow: as the sound comes the pinna directed incoming sound through the eardrum. The eardrum vibrates according to input sound level and frequency. The vibration on the eardrum is detected by multi-channel PZT sensors that capture sound frequency and level. The sensor outputs are provided to the signal conditioning interface electronics which stimulate the auditory neurons according to sensor outputs. The neural stimulation pulses are delivered to auditory neurons through a cochlear electrode. The power requirement of the interface is supplied by a rechargeable battery which can be charged through an RF coil. The RF coil is also utilized for applying patient fitting after the implantation. The subject of this thesis is the signal conditioning interface unit, for which design specifications are outlined in this section.

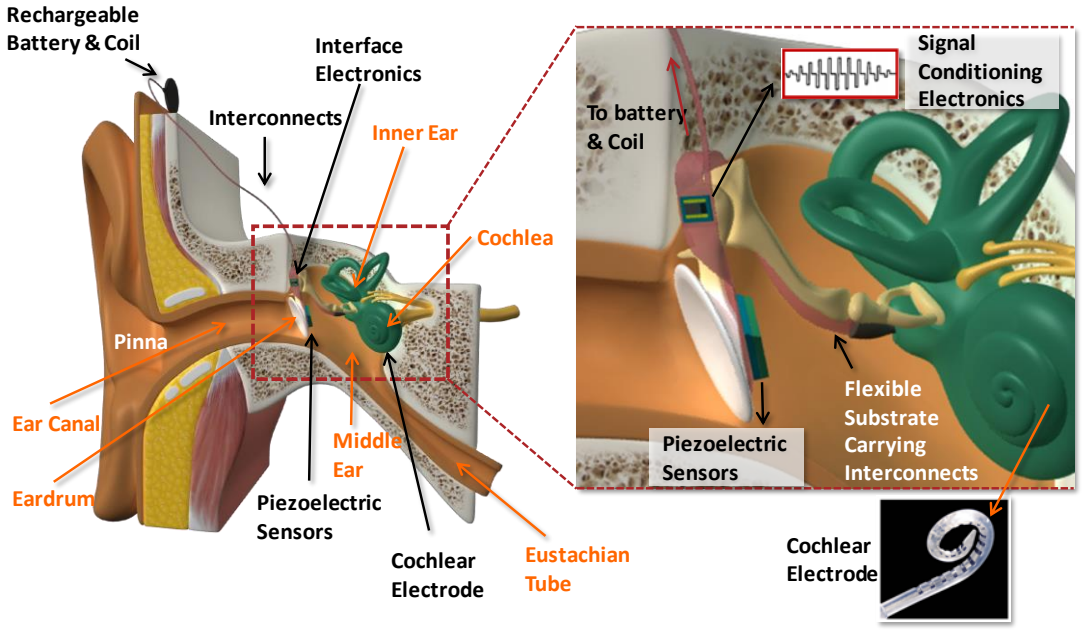


Figure 3.1. FICI system proposed at FLAMENCO Project [51].

First, the conditioning electronics and the transducers must fit into the middle ear (2 cm^3) and the transducer footprint must be less than the size of the eardrum (55 mm^2) [14]. The low volume sensor by our group [46] includes 8 cantilever beams with different resonant frequencies for sound detection, covering the common sound band from 200 Hz to 5 kHz [67], [68]. The number of cantilever beams determines the number of spectral channels, which highly influences the speech perception of the patients. Previous studies report that speech perception gets better with increasing number of channels, but does not significantly improve beyond 7 channels [69]. Hence, 8 channels utilized in the proposed design provide sufficient spectral resolution with acceptable hardware complexity and power dissipation associated with the conditioning circuits.

PZT sensors collectively provide mechanical filtering since each one oscillates with the frequency component of the incoming signal that matches with its resonant frequency. The power requirement of the circuits that condition the PZT signals is the crucial part of the design. For a 200 mAh and 3.6 V implantable rechargeable battery [70], the total power consumption must be lower than 600 μW to dissipate 1% of the total energy with 12 hours continuous usage. Typical power conversion (regulation) circuits have about 85% efficiency at best. Therefore, implantable signal conditioning circuits must consume less than 500 μW to achieve lifetime beyond 30 years by recharging the battery to its 90% capacity for 1000 cycles.

Another critical design parameter for the signal conditioning circuit is the input dynamic range, which highly influences the speech perception of the patient. Daily sound level ranges between 40 dB SPL (e.g. in a quite library) and 100 dB SPL (e.g. helicopter noise) [6]. Previous studies have shown that an input dynamic range of 50 dB provides adequate speech perception in multichannel CIs [71], which is thus used as the lower bound for signal conditioning and transducer design. Therefore, the 2nd generation FICI interface electronics is designed by considering these specifications.

3.2. Interface Circuit Design and Description

Figure 3.2 shows the block diagram of the bionic ear interface that senses voltage signals from 8 piezoelectric (PZT) sensors with different center frequencies. The interface circuitry pre-dominantly operates in current mode to minimize power dissipation due to current-to-voltage conversion and vice versa. The size constraint on the PZT sensors limit their output signal amplitude, which must be amplified at the first stage of the interface. Therefore, an improved version of the low-power wide-range Logarithmic Amplifier (LA), which was proposed in previous generation, is designed as the first stage. Although the dynamic range of daily observed sounds is around 60 dB, the electrical dynamic range of the diseased cochlea is limited to 20 dB [52], [71]. Thus, the LA is designed to logarithmically compress the input sound range to the electrical dynamic range of the cochlea. In previous design AC current generated by the logarithmic amplifier converted into voltage through load resistors however at new design the current output is fed to the next stage. In previous design AC current generated by the logarithmic amplifier converted into voltage through load resistors however at new design the current output is fed to the next stage. The AC current output of the LA is delivered to an original current rectifier and multiplier with a low-pass filter. A sample/hold circuit samples the filter output to generate a reference for the stimulation current generator, which drives the current level required by the auditory neurons. The sampled signal is compared with a hysteresis comparator and if the input level high enough it is provided to the stimulation current generator. This enables to system to disable the stimulation part which is the most power hungry part of the system. The sampled signal is converted into a biphasic pulse through a switch matrix, which directs the current pulse to the correct electrode (E_1-E_8) to stimulate the corresponding auditory neurons. The enable signals for the LAs and corresponding channel selection signals at sample/hold blocks are provided by the control unit. The voltage amplitude of the selection signals are boosted through level shifters to be compatible with the high voltage switch matrix control block for the biphasic current. Design and analysis of each sub-circuit is provided in the following sections.

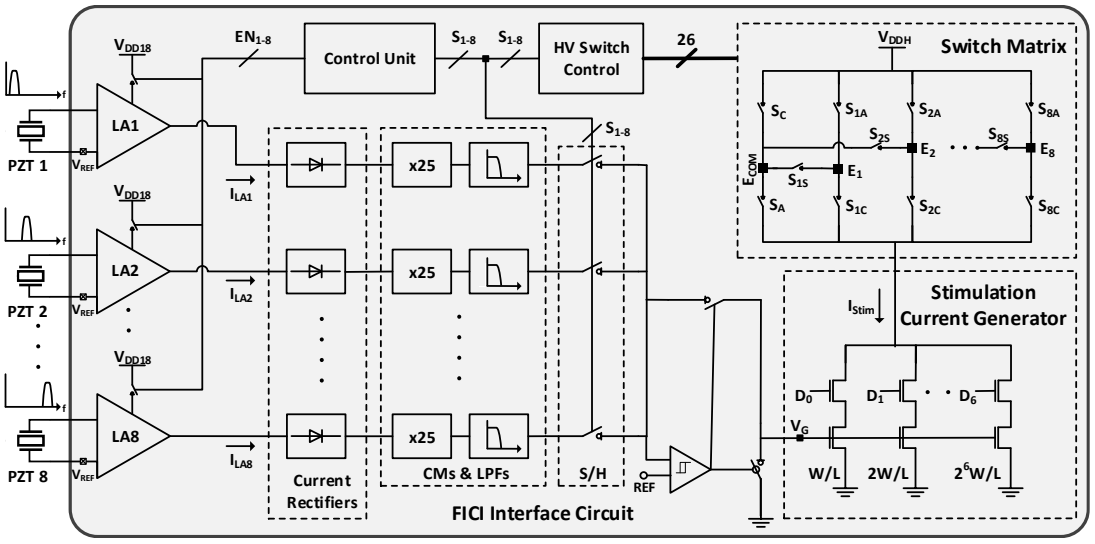


Figure 3.2. 2nd generation FICI (bionic ear) interface circuit block diagram.

3.2.1. Logarithmic Amplifier (LA)

Each sensor output at the first stage is amplified using a custom designed logarithmic amplifier that also compresses the incoming sound to the electrical dynamic range of neurons. The dual function of the amplifier optimizes system power dissipation better compared to the previously reported cochlear implant interfaces, which implement a separate DC compression stage after the downstream envelope detection stage [49], [52], [72]. The designed LA for the 2nd generation FICI is a modified version of the 1st generation which is presented in [55]. Figure 3.3 shows the LA of 1st generation interface and the modified LA for the new generation circuit where the new generation provides single ended AC current as the output instead of differential voltages. The number of stages in the circuit is minimized for minimum power dissipation with the constraint to deliver the desired input compression range. The LA circuit optimized as such for 5 stages in order to amplify the full sensor output voltage (0.1-100 mV) provided in [46] to acceptable levels. As the input amplitude increases, each stage of the LA enters the limiting state (saturation) one by one from the last stage toward the first as in the case of 1st generation design.

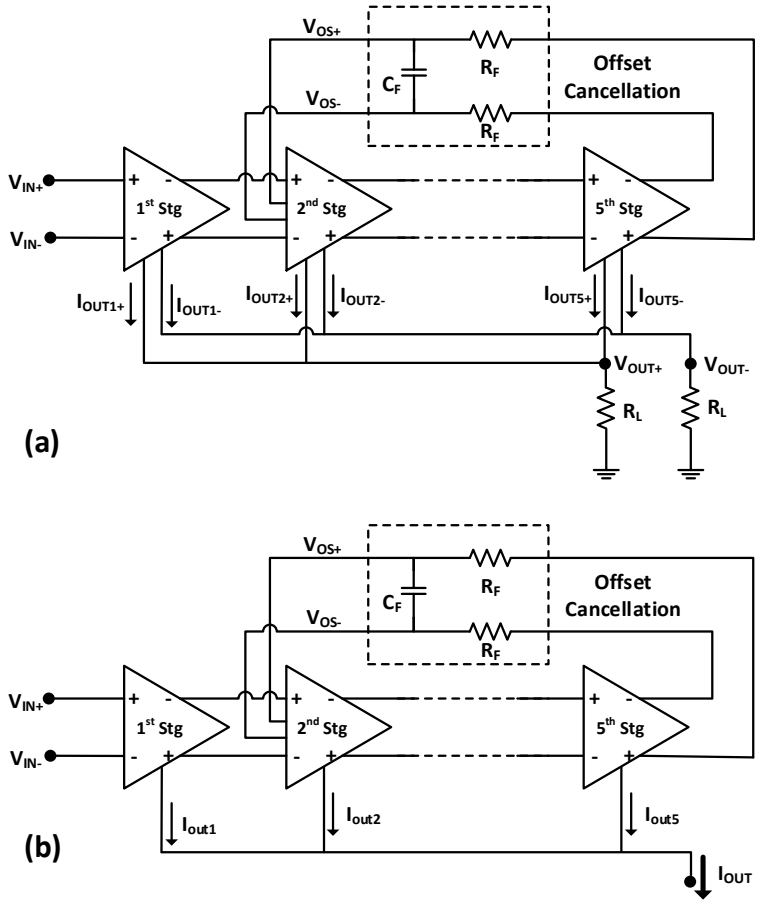


Figure 3.3. Logarithmic amplifier with (a) voltage output and (b) current output designed for 1st and 2nd generation FICI interface electronics.

Figure 3.4 presents the circuit design of each logarithmic amplifier stage. PZT sensor output is applied to the inputs of the differential amplifier at the first stage that generates differential output voltages (V_{X+} and V_{X-}) to drive the next stage. The current on M_4 with both DC and AC components is copied through mirror transistor M_5. The DC current (I_{Bias}) at the output is extracted with the bias branch, leaving only the AC component (I_{ac}) at the output. Since the input resistance of the current rectifier is considerably lower than the output resistance of the amplifier, nearly all of the AC current is transferred to the rectifier stage. The total output current of the logarithmic amplifier (I_{OUT}) is obtained by summing output currents of each amplifier stage ($I_{out,i}$). The relationship between output current and input voltage is provided by Eq. (3.1) in terms of the circuit parameters given all the amplifiers operate in linear region:

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}(1 + A_v + (A_v)^2 + (A_v)^3 + (A_v)^4) \tag{3.1}$$

where A_v is the voltage gain of the differential pair and can be written as $A_v = g_{m,M1}/g_{m,M3}$. The input stage of each amplifier includes an isolated NMOS, which improves the overall gain through increased transconductance (g_m) for the same bias current and MOSFET size. The output current of the logarithmic amplifier can be rewritten using Taylor series as given in Eq. (3.2) and (3.3).

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}\sum_{i=0}^{k-1}(A_v)^i, \qquad k = 1, 2 \ldots 5 \tag{3.2}$$

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}\left(\frac{(A_v)^k - 1}{A_v - 1}\right) \tag{3.3}$$

where k is the number of amplifiers operating in linear region. When the input voltage increases, the number of amplifiers in linear region decreases, which causes reduction in the LA gain, as expected.

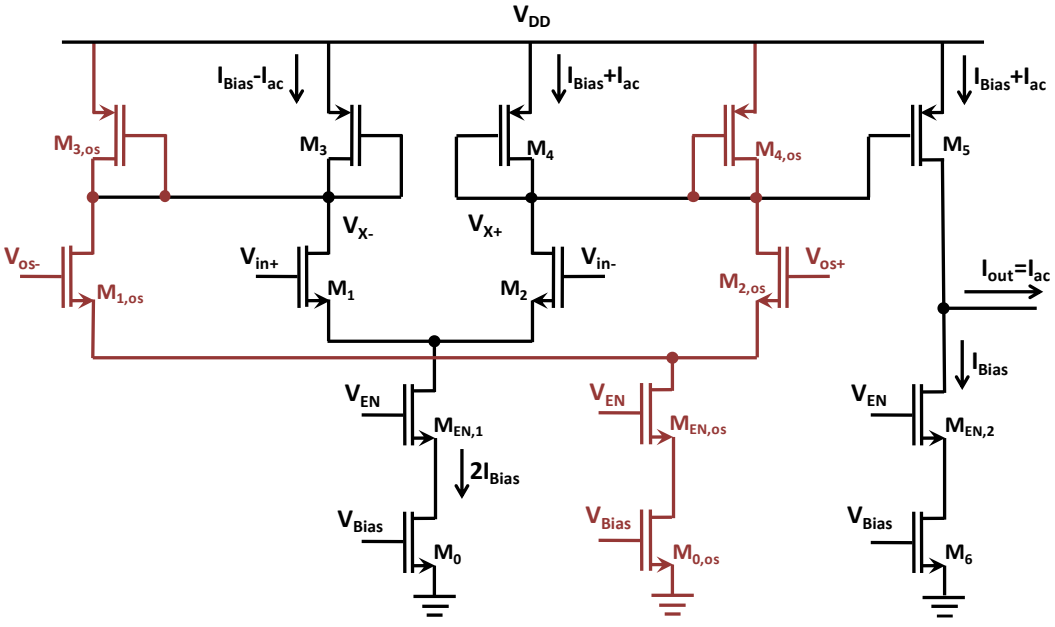


Figure 3.4. Amplifier stage design, with the 2nd stage additions for enhanced offset cancellation highlighted in red color.

The amplifier stages are biased to operate in subthreshold domain for lower power dissipation and higher gain due to increased transconductance. The power consumption of the logarithmic amplifier is further decreased through selective power gating of a lower supply voltage (V_{DD}=1.8 V) compared to the rest of the FICI interface. When a particular channel is not sampled, the LA is dynamically disabled through a power management control signal (V_{EN} in the Figure 3.4).

Feedback from the last stage is applied to the 2nd stage in order to cancel the effect of DC offset at the input. Figure 3.4 highlights the offset cancellation enhancements (in red color) to the amplifier at the 2nd stage. An RC filter has been applied as the feedback loop with cut-off frequency <0.1 Hz to avoid feedback interactions within the hearing band (20 Hz – 20 kHz). High value required from the RC product to achieve the target cut-off frequency is challenging for the on-die integration of the filter. A pseudo-resistor MOS structure with high resistance has hence been utilized as shown in Figure 3.5 (a). The pseudo-resistor structure is built from a parasitic source-body-drain pnp transistor, and is activated when the diode connected PMOS transistors are forward biased. Two series pseudo-resistor structures have been utilized to provide resistive operation at a wider offset range. Since this structure passes current only in one direction, another resistive pair with reverse direction has been connected in parallel to provide bidirectional operation. Figure 3.5 (b) shows that the resistance of the structure is more than 450 GΩ for voltage difference lower than ±250 mV. The capacitance in the RC filter can thus be decreased below 10 pF, and is implemented using on-die MIM caps.

Figure 3.6 shows the obtained input-output characteristics of the designed logarithmic amplifier for different frequencies where the circuit compress the 60 dB input range to 20 dB electrical dynamic range. The circuit does not show a significant deviation at the characteristic up to 10 kHz. The off-set cancellation performance of the circuit is simulated by applying different offset voltages between the inputs of the circuit. Figure 3.7 shows simulation response of the amplifier at varying input voltages and

off-set voltage values. The results showed that the output voltage is slightly deviated with the applied off-set voltage; however, the circuit is still functional.

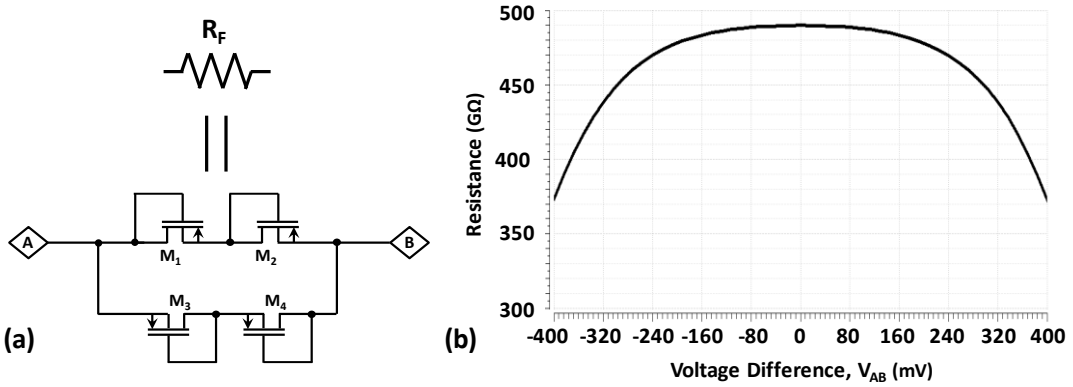


Figure 3.5. (a) Schematic of pseudo-resistor MOS structure, and (b) simulation that shows variation of resistance with voltage across the resistor.

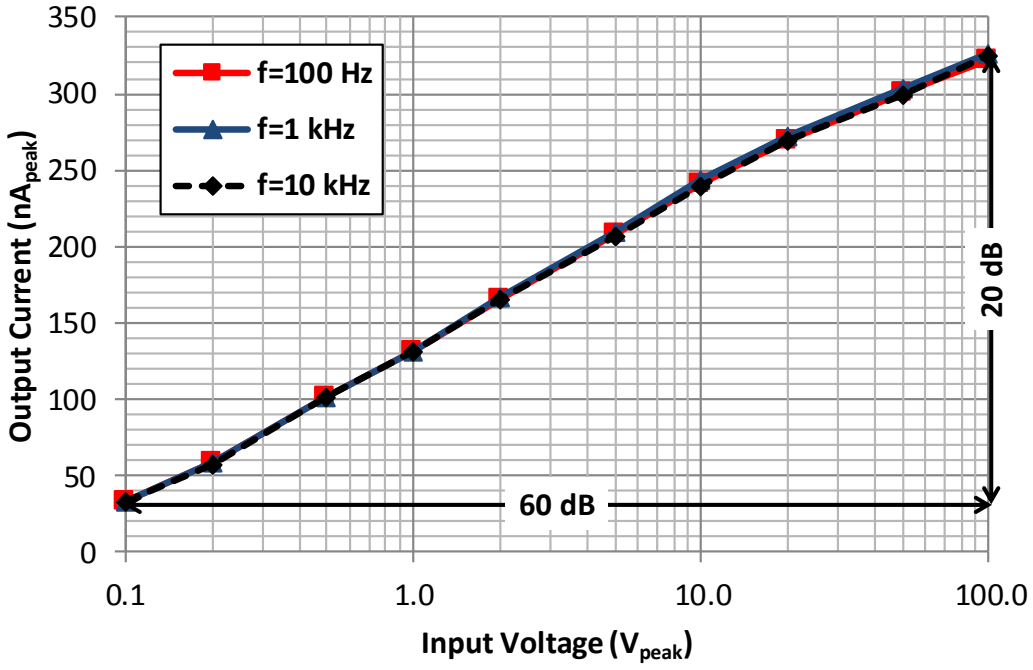


Figure 3.6. Simulation result of variation of the output voltage with respect to the input voltage and frequency.

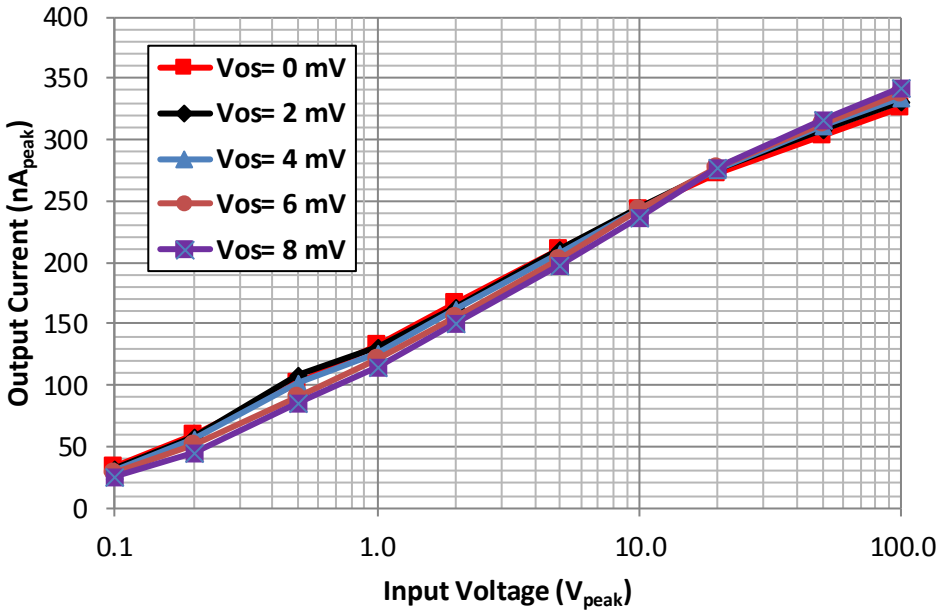


Figure 3.7. Simulation result of variation of the output voltage with respect to the input voltage at different applied off-set voltages.

3.2.2. Current Rectifier and Multiplier with Low-Pass Filter

The next stage rectifies, multiplies, and filters the logarithmic amplifier current output, as illustrated in Figure 3.8. Diode connected NMOS (M_5) and PMOS (M_6) transistors provide low resistance at the rectifier input. The operation principle of the current rectifier is as follows: Input current (I_{IN}) flows through M_6 with M_5 turned OFF during the positive phase. M_6 is similarly turned OFF during the negative phase while the current is sinked from M5 transistor. The current through M_5 is mirrored with cascode current mirrors that generate positive current on M_7. Thus, both positive and negative half cycles are summed on M_7, and copied to the low-pass filter circuit through $M_{7\text{-}10}$ cascode 5x current multiplier. The copied current is then multiplied 5x once more through $M_{11\text{-}14}$, and is delivered (I_{LP}) to the diode connected high voltage NMOS transistor (M_{15}). M_{15} gate has a 25 pF capacitor to form a low-pass filter. The filter is designed with 400 Hz cutoff frequency, which is close to the frequency of temporal pitch observed in daily life [24], [28]. The current generated by the current multiplier with low-pass filter is used as a reference for the stimulation current generator, which

operates on high voltage supply and is made up of high voltage transistors. The design therefore requires the current multiplier to have a 3.3 V supply voltage instead of the 1.8 V supply used by the current rectifier.

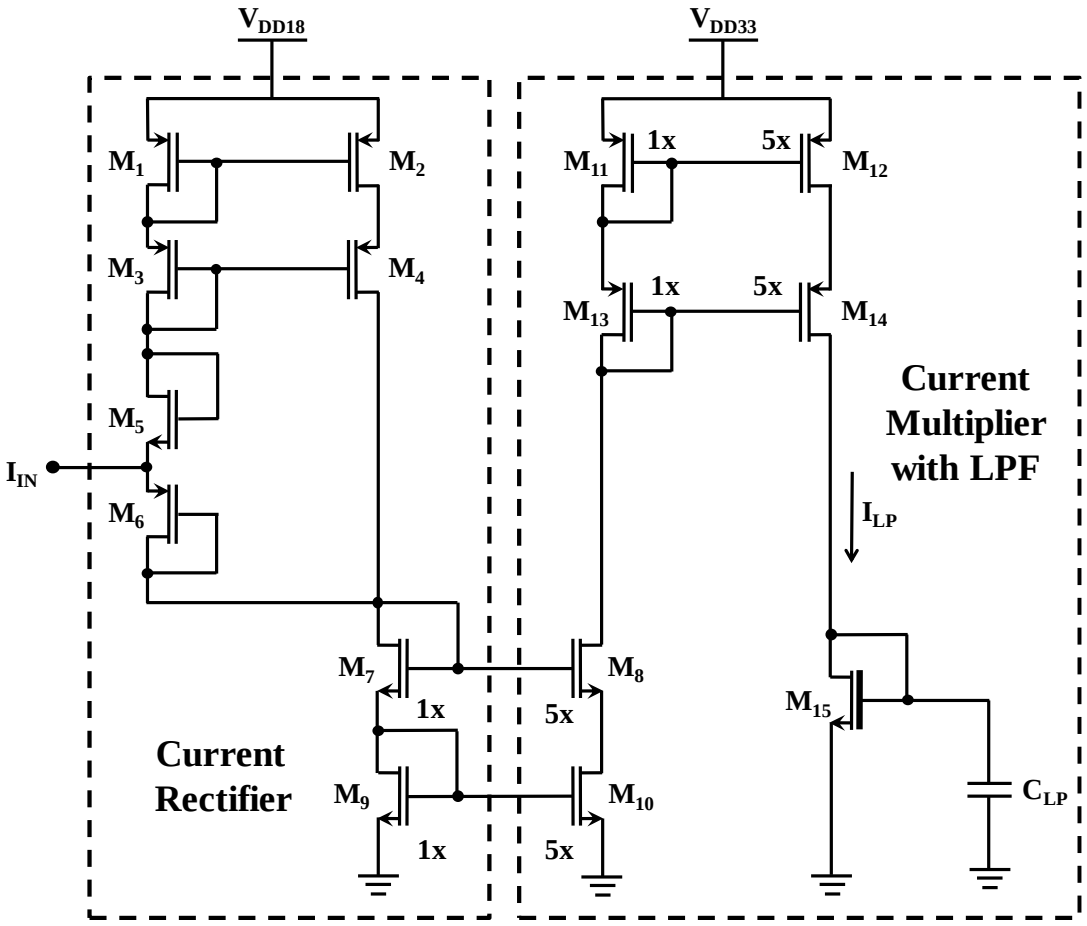


Figure 3.8. Schematic diagram of the current rectifier and multiplier with the low-pass filter.

3.2.3. Sample and Hold Circuit

The voltage on the capacitor at the output of low pass filter is sampled with the sample and hold circuit shown in Figure 3.9. The capacitor voltage at the input is copied with a buffer circuit which prevents loading of the sampling to the previous stage. A single stage differential amplifier is utilized as the buffer. Since the operation frequency of the system is quite low the simple structure provides high enough gain with low power dissipation. The buffered voltage is sampled on the hold capacitor with a switch for

100 μs where another shorted switch is placed after the capacitor to prevent charge injection effect. The shorted switch controlled with negative cycle of the sampling switch. The system includes 8 Sample and Hold (S/H) circuits where output of all these circuits are connected to an analog multiplexer that gives output of the corresponding hold circuit to the current generator block as a reference.

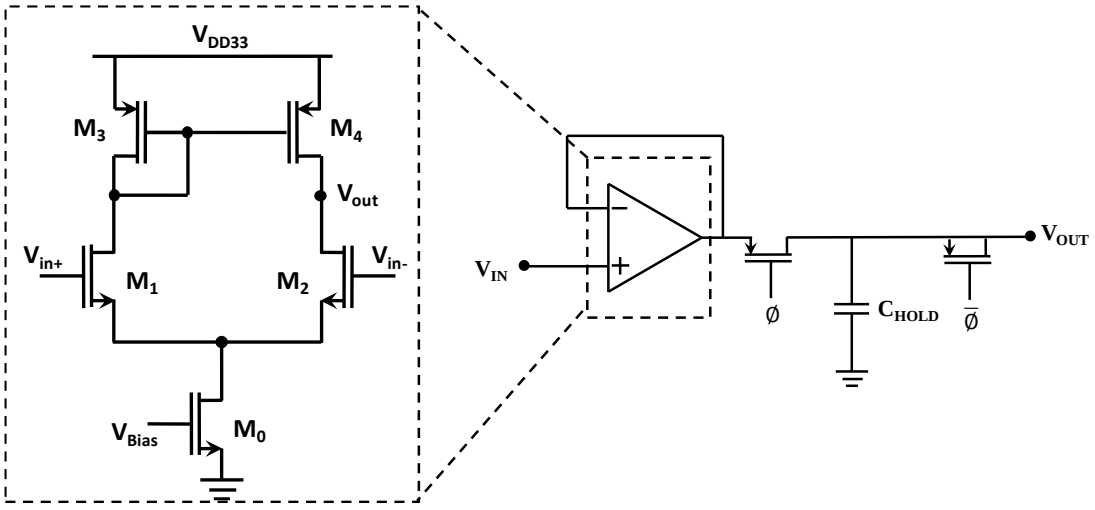


Figure 3.9. Sample and hold circuit with differential amplifier as the buffer stage.

3.2.4. Stimulation Current Generator

The sampled gate voltage of the low pas filter is provided as the gate voltage of the current source transistors (V_G) as shown in Figure 3.10. Where the level of gate voltage directly implies the stimulation current level. The current generator circuit also operates as a 7 bit digital to analog converter where stimulation current threshold and maximum comfort level can be determined by controlling these digital signals. This topology yields easy and wide range control of the current. Moreover, since the topology includes DAC and current generation operations at the same time, it dissipates less power compared to previous generation current generator circuits [49], [73]. The current generator block is able to supply more than 1 mA stimulation current.

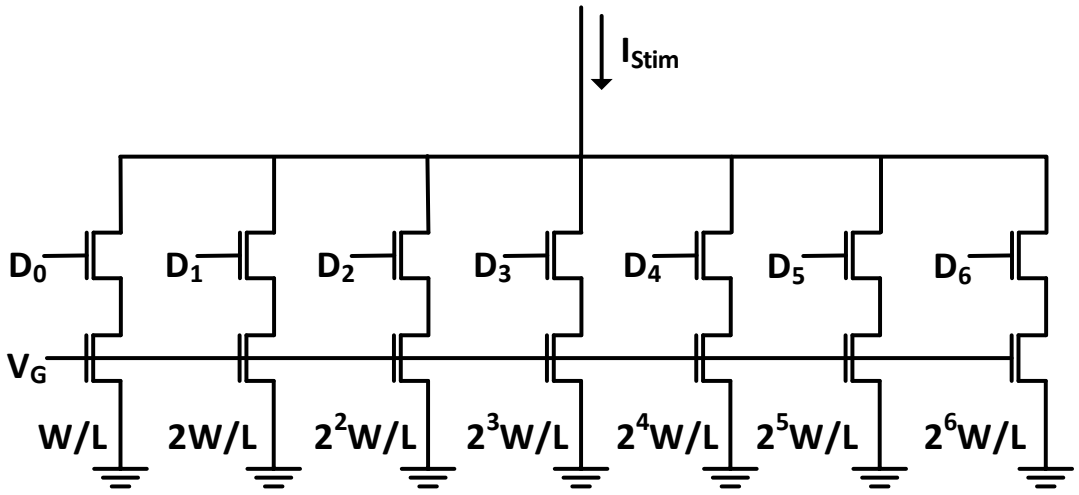


Figure 3.10. Schematic of the 7-bit stimulation current generator.

3.2.5. Switch Matrix

The switch matrix circuit utilizes the same topology as in the 1st generation design (Figure 3.11 (a)); however, the order of switching has been changed to provide cathodic pulse before the anodic one [74], [75]. Figure 3.11 (b) shows the generated biphasic stimulation current in time domain with cathodic pulse first. After the cathodic pulse is generated through S_C and $S_{1,C}$ switches, the anodic pulse is applied with S_A and $S_{1,A}$ in order to supply the discharged current back to the neurons. S_C and $S_{1,A}$ in the switch matrix are PMOS switches whereas S_A, $S_{1,S}$, and $S_{1,C}$ are NMOS switches to enable better transmission at high and low voltage, respectively. Switch $S_{1,S}$ is utilized to remove the residual charge remaining on the capacitor at the load, and prevents charge imbalance at the electrodes. The switch matrix is supplied by high voltage (V_{DDH}) to deliver a sufficiently high potential at the stimulation electrodes. The electrodes are enabled according to the well-known Continuous Interleaved Sampling (CIS) sound processing strategy, which provides sequential interleaved stimulation of the electrodes at fixed frequency, and delivers better performance compared to other synchronous implementations [60], [61]. CIS switch control signal timing is explained in the next section

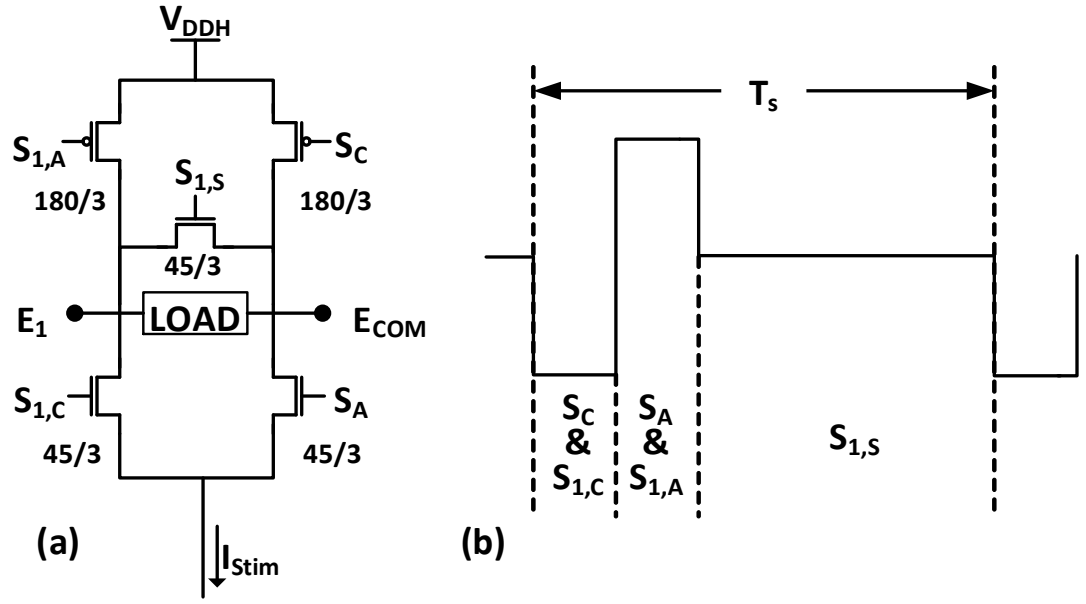


Figure 3.11. (a) Switch matrix utilized at Electrode 1, and (b) generated biphasic stimulation current.

3.2.6. Control Unit

The control unit generates power enable signals for the logarithmic amplifiers, selection signals to switch between channels for sampling, and switch matrix control signals for 8-channel CIS stimulation. The core is a resettable one-hot finite state machine (FSM), as depicted in Figure 3.12 (a). The state machine generates interleaved enable signals (S[1:8]) that stimulate the electrodes sequentially according to CIS strategy. The timing diagram for the digital control of the electrode switch matrix is given in Figure 3.13, which shows switch control signals and the enable signals. The stimulation is timed using a low frequency clock (CLK_{LO}) that has a period of 1 ms, hence neural stimulation frequency is determined as 1 kHz. The stimulation frequency is determined by considering the neural refractory period of the nerve fiber which is around 1 ms [24]. Previous studies also shown that the nerves are not able to properly respond electrical stimulation higher than 1 kHz and for lower frequencies the speech perception will be decreased [76]. A 100 µs stimulation pulse at each channel enables 50 µs cathodic and anodic phase widths. After CLK_{LO} falling

edge starts the operation, channel select signals are consecutively enabled through the one-hot FSM running on a higher frequency clock (CLK_{HI}) at 10 kHz. CLK_{HI} is generated by a ring oscillator, and is also used to trigger a ring counter, as shown in Figure 3.12 (b), in order to generate CLK_{LO}. This implementation ensures the two clocks have synchronous timing. The logarithmic amplifier enable and sampling signals (EN[1:8]) are acquired for 100 μs, and generated just before the enabling period of the corresponding channel. After the stimulation of the last channel, a done signal is generated to reset the machine, and the process repeats at next falling edge of the low-frequency clock. The anodic and cathodic pulses at each stimulation electrode are obtained from electrode selection signals (S[1:8]) and the clock signals using the combinational logic circuit in Figure 3.12 (c). The control unit is designed to accommodate different channel modes, programmed through "CH_MODE[0:1]" signals. The system can operate at 1, 4, 6 or 8 channels, which allows user tradeoffs between sound perception quality and power dissipation. The control unit is powered by the lower 1.8 V supply voltage for reduced power dissipation. The generated switch control signals go through a set of level shifters at the control unit interface for turning the high voltage switches on and off properly.

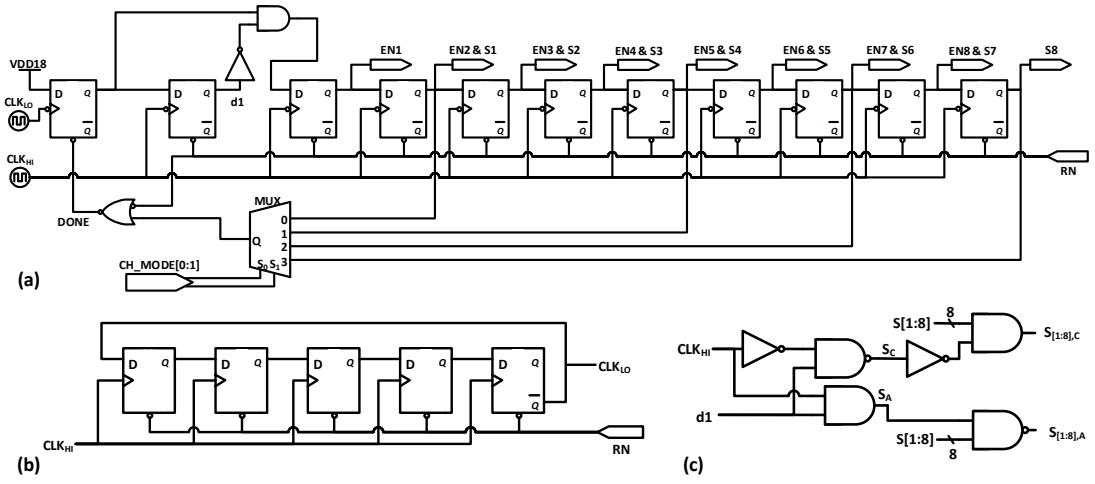


Figure 3.12. (a) Schematic diagram of .the resettable one-hot state machine implementation for the control unit, (b) ring counter for generating CLK_{LO} from CLK_{HI}, and (c) designed combinational circuit that generates switch matrix control signals.

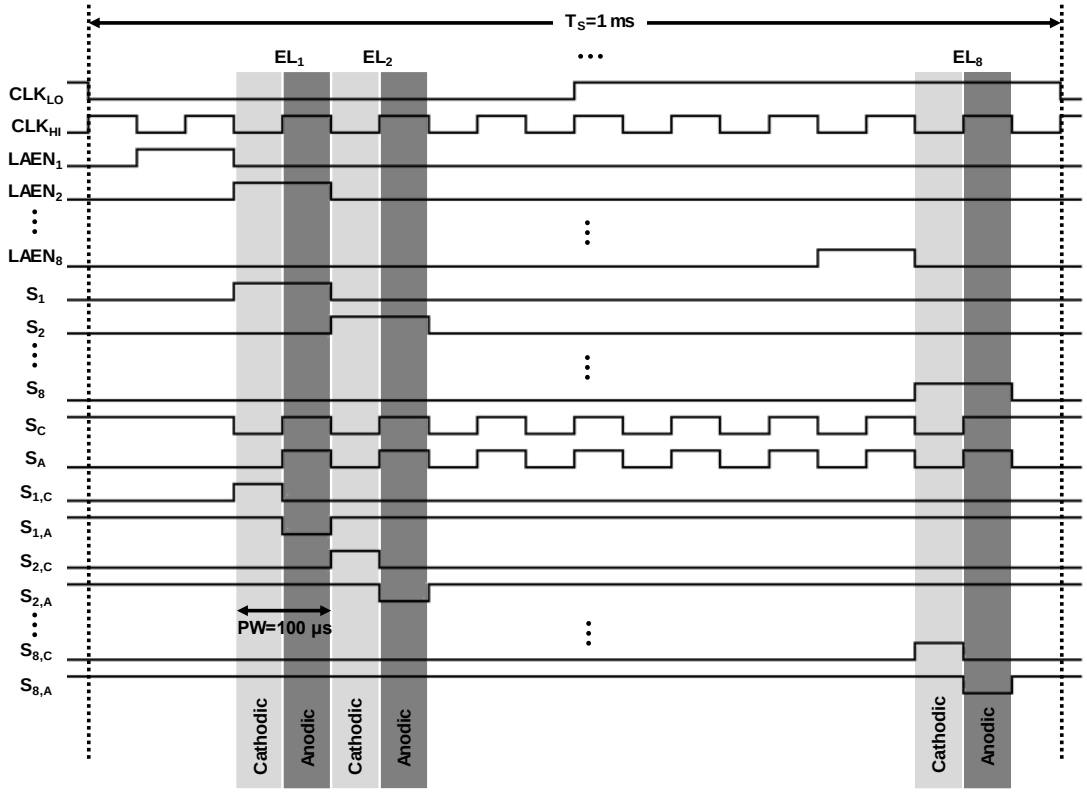


Figure 3.13. Timing diagram for the digital control of the electrode switch matrix.

3.2.7. Hysteresis Comparator

As shown in Figure 3.2 the sampled envelope detector voltage is compared with a reference voltage (REF) to enable the stimulation current generator. If the sampled voltage is higher than REF voltage it is supplied to the stimulation current generator and the stimulation is activated. On the other hand, if the sampled voltage is not high enough the stimulation current is turned off by connecting V_G to ground and excess power dissipation of the most power hungry part of the system is prevent. In the proposed design REF is chosen as 1.8 V, which is higher than threshold voltage of high voltage transistors at the stimulation current generator. Figure 3.14 shows the schematic diagram of designed hysteresis comparator which is composed of 3 stages. The first stage is a input differential pair where active load stage provides the hysteresis characteristics of the comparator. The positive and negative trip points are determined according to the ratio between the W/L ratios of input transistors and the

load transistors. The next two stages of the comparator are utilized to increase gain and slew rate of comparator to provide fast transition at the output. Figure 3.15 shows simulation of the designed hysteresis comparator where the difference between the trip points is determined around 250 mV to provide wide enough margin to tolerate the noise at the output of the sample circuit. The total power dissipation of the comparator is around 1.5 μW.

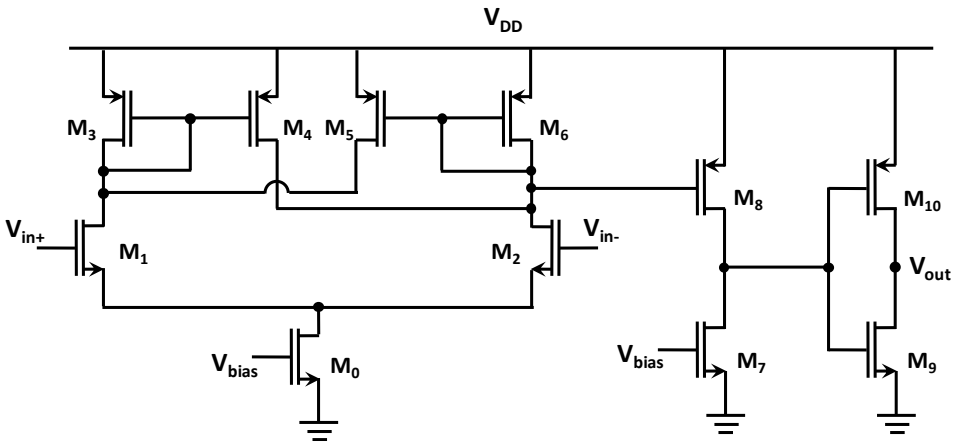


Figure 3.14. Schematic of the designed hysteresis comparator.

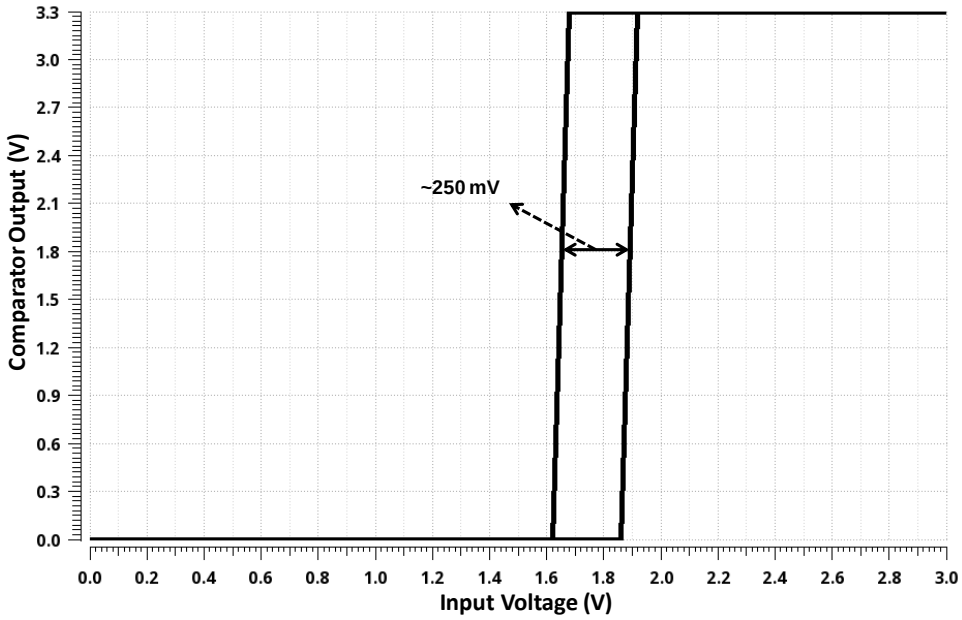


Figure 3.15. Simulation of input-output characteristic of the designed hysteresis comparator.

3.2.8. Voltage Reference

In order to bias the operating circuits such as amplifiers and comparators a voltage reference circuit is required to provide supply and temperature independent operation. The most well-known reference circuit is a bandgap voltage reference which utilizes parasitic bipolar junction transistors (BJTs) for adapting the circuit to CMOS technology [77]–[79]. This topologies combine complementary to absolute temperature (CTAT) voltage and proportional to absolute temperature (PTAT) voltages to generate temperature independent biasing. However, power dissipation of these voltage references limits their application for biomedical circuits. Seok *et al*. proposed a pico-Watt power 2 transistor voltage reference for biomedical applications that can operate down to 0.5 V supply [80]. In the proposed system this voltage reference is modified to achieve the system needs as shown in Figure 3.16.This reference voltage circuit requires depletion type transistor (M_1 and M_3) in addition to enhancement type transistors (M_0 and M_2). The gate of depletion transistors are connected to the ground and generate reference current where this current is independent of supply voltage. Then this reference current is passed on diode connected transistors to generate reference voltage. Two reference voltages are generated to bias the low voltage and mid voltage circuits that are operate with 1.8 and 3.3 V, respectively. Although the original design operates at pico-Watt power range, the proposed system is designed at high voltage process which is not suitable to operate with such current ranges. Therefore the circuit is designed to operate with 10 nA supply current. Figure 3.17 shows simulation result of the reference circuit with respect to the supply voltage variation where the reference voltages VREF_L and VREF_M generate 300 and 600 mV, respectively at 1.8 V supply voltage. The simulation also includes process corner simulation that shows variation at the result at different process un-idealities. As shown from the figure the line regulation of VREF_L and VREF_M are 0.3% and 0.7%, respectively. Moreover, the reference voltage variation with respect to process corners are lower than ±5 mV at 1.8 V supply which is quite tolerable at biomedical circuit applications. Figure 3.18 shows

simulation of the temperature dependency of the circuit where VREF_L and VREF_M has ±0.5 mV and ±2.5 mV, respectively.

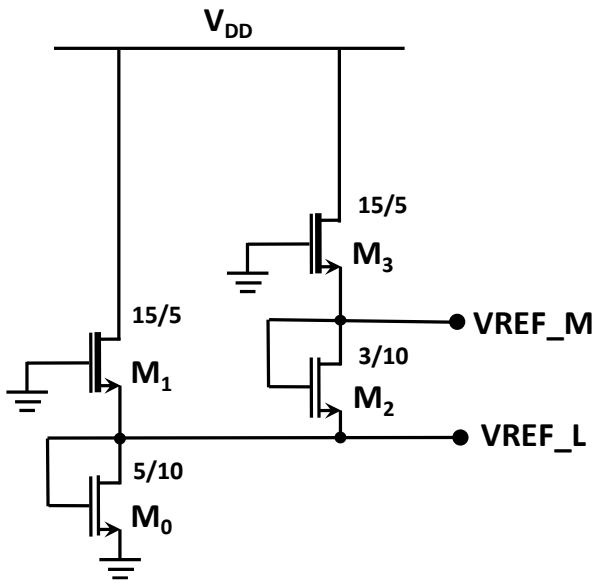


Figure 3.16. Schematic of the modified 4 transistor voltage reference.

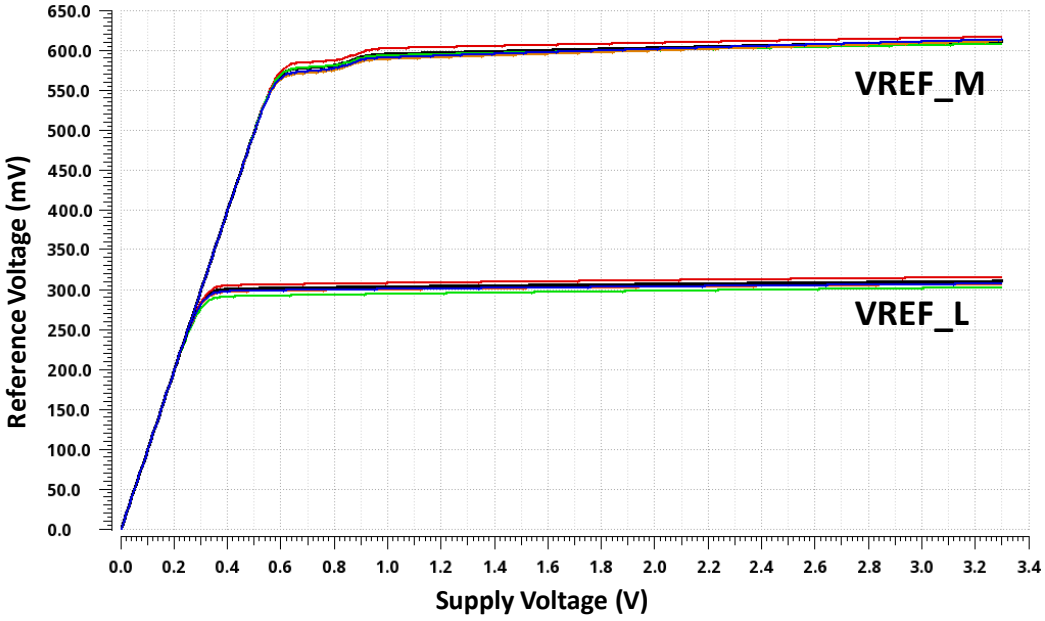


Figure 3.17. Simulation of the voltage reference outputs with respect to supply voltage.

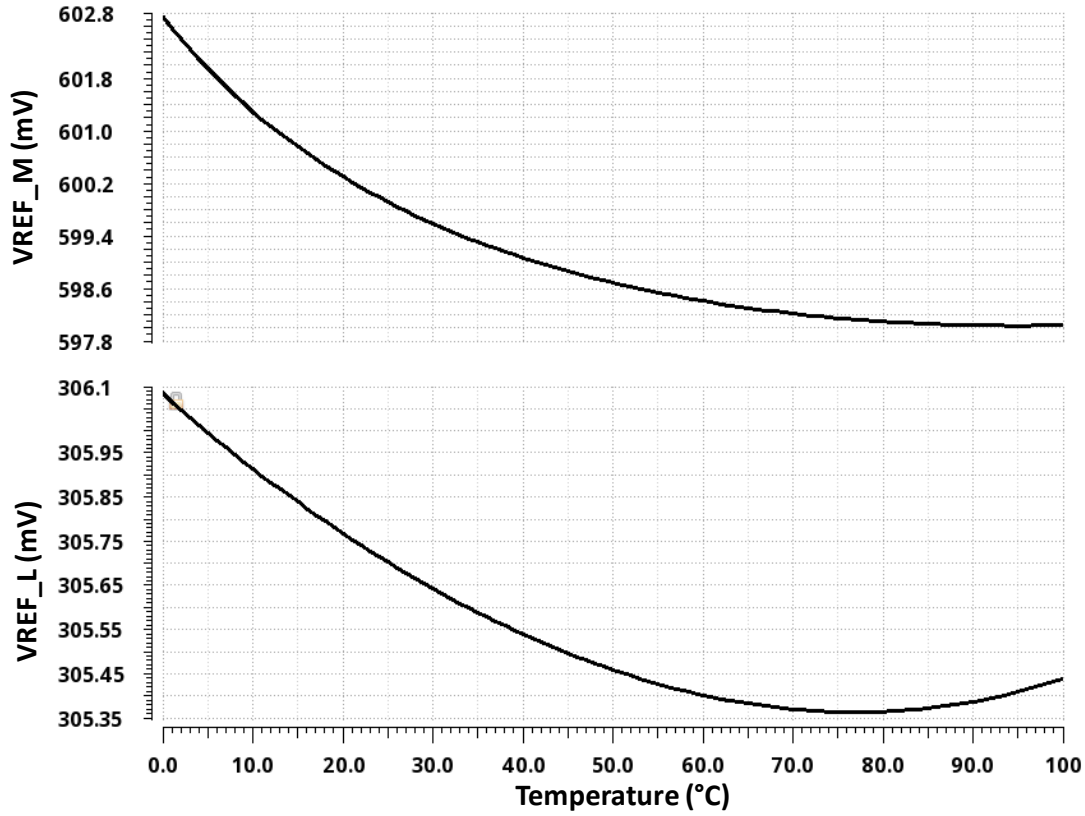


Figure 3.18. Simulation of the voltage references outputs with respect to temperature.

3.2.9. Overall System Simulation

The full system provides 8 channel FICI operation where complete system simulation for varying input with 1-4-6 and 8 channels operation is shown in Figure 3.19. As can be seen from the simulation the stimulation of the channels are arranged according to CIS stimulation strategy and as the waveform amplitude changes the stimulation current level also varies. The total power dissipation of the system is around 600 μW which is 70 μW lower than previous design which comes from the improvements at the front end signal conditioning circuit. However, total power dissipation of the system must be even lowered to provide long lasting FICI operation. Therefore, the stimulator part of the system is optimized with efficient neural stimulation waveforms, which is explained in next section, to significantly reduce the overall system power.

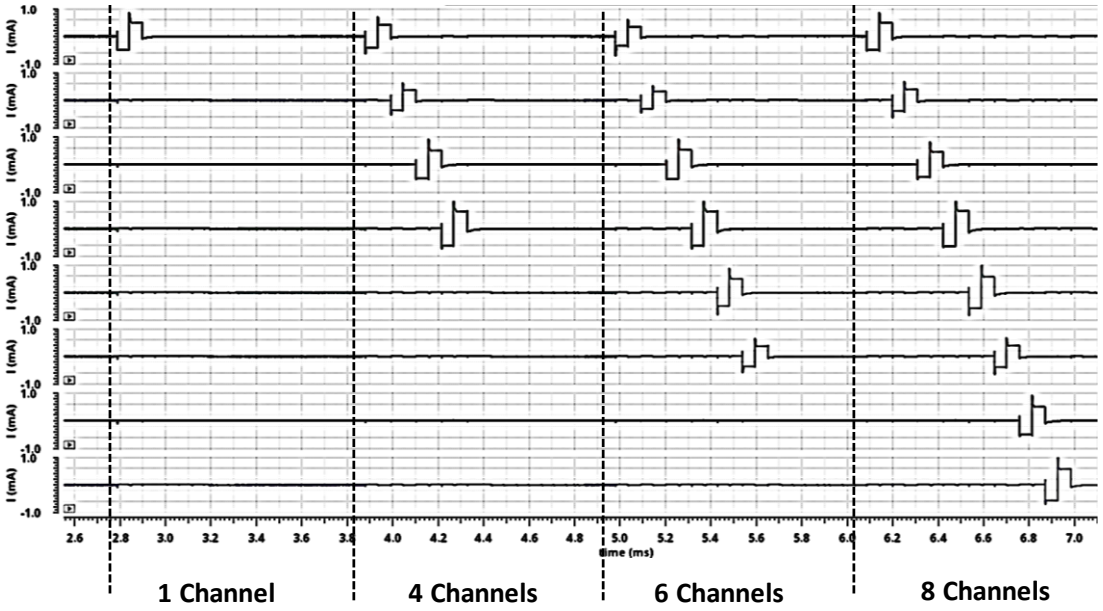


Figure 3.19. Simulation of 1-4-6 and 8 Channels operation of the 2nd generation FICI interface electronics.

3.3. Efficient Neural Stimulation

The neural stimulator is the most power hungry part of the design, and accounts for more than 90% of the total power dissipation due to the high voltage requirement at the stimulation electrodes. The well-known rectangular constant-current stimulation that is also utilized at commercial cochlear implants suffers from inefficiency of charge transfer and high voltage levels with few undesired consequences, including formation of undesirable chemical products. Although recent studies has improved the efficiency of charge transfer through modified stimulation current waveform shape [49], [81], the peak voltage remains high and can be further optimized. In [81] seven stimulus waveforms shown in Table 3.1 were tested while the pulse width was varied from 0.001 to 0.5 ms. The most efficient waveform that maximized the charge injection capacity of the electrode while providing the lowest threshold charge for neural activation was searched. Linear and exponential decrease, and Gaussian waveforms were found to be the most efficient pulse shapes.

Table 3.1. Current pulse waveforms tested in [81]. *K* is the stimulus strength factor.

1	Rectangular (Rect)	$K[u(t) - u(t-\tau)]$
2	Linear increase (LinInc)	Kt
3	Linear decrease (LinDec)	$K(\tau - t)$
4	Exponential increase (ExpInc)	$K(e^{-\frac{5(\tau-t)}{\tau}})$
5	Exponential decrease (ExpDec)	$K(e^{-\frac{5t}{\tau}})$
6	Gaussian (Gauss)	$\frac{K}{(\tau/5)\sqrt{2\pi}} e^{-(\frac{t-\frac{\tau}{2}}{\sqrt{2}\frac{\tau}{5}})^2}$
7	Sinusoidal (Sin)	$K \sin(\frac{\pi t}{\tau})$

The study presented in [82] contains results on the design of electrical signals for delivering charge through electrodes to achieve neural stimulation while reducing the peak electrode voltage for retinal prosthesis. Stepped decreasing current in [82] reduces the maximum electrode voltage, but the waveform is not slope-optimized, and utilizes limited number of steps at each phase. Therefore, both waveform shape and slope of the waveform must be optimized to obtain the best performance.

The conventional model of the electrode tissue interface is depicted in Figure 3.20 (a) with three lumped system components. Bulk resistor (R_{bulk}) models the substance between two electrodes, whereas the electrode-tissue interface is modeled with a capacitor (C_{surf}). The leakage resistor (R_{leak}) is used to model the redox reactions occurring at the electrode surface that is connected in parallel with the C_{surf} [83]. R_{leak} is typically ignored, since it has a very large value. Bulk resistance and surface capacitance values have been reported in 1-10 kΩ and 1-10 nF range, respectively [59], [83], [84]. Figure 3.20 (b) shows the rectangular stimulation current and the electrode voltage for the given R-C model. The electrode voltage increases during the stimulation, and reaches its maximum value at the end of the pulse phase. The maximum electrode voltage can be reduced by applying a non-rectangular pulse shape, i.e. a decreasing current waveform, which maintains a low electrode voltage.

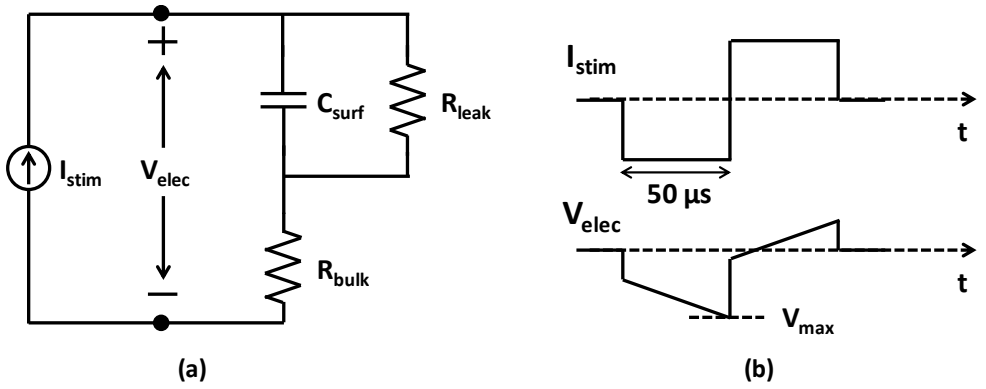


Figure 3.20. (a) Three-element model of the electrode tissue interface, and (b) the electrode current and voltage waveforms.

Different waveforms such as linear decreasing, exponential decreasing, and Gaussian distributed current pulse shapes were tested with the electrical model to minimize the electrode voltage. The average current per phase must be identical for all to provide the same charge level. Since the stimulation current is supplied through a constant current generator circuit for simplicity, the waveform shape can only be changed in stepped manner, which is the most efficient and practical approach to apply different shapes. The discrete time expressions for different waveform shapes are given in Eq. (3.4)-(3.7).

$$I_{rect} = A_{rect} \tag{3.4}$$

$$I_{gauss}(n) = A_{gauss} e^{-0.5\left(\frac{n(2\alpha_{gauss})}{N-1}\right)^2} \tag{3.5}$$

$$I_{lin}(n) = A_{lin}(K - \alpha_{lin} n) \tag{3.6}$$

$$I_{ex}(n) = A_{ex} e^{-\alpha_{ex} n} \tag{3.7}$$

where *A* is the amplitude coefficient of the applied currents, α_{gauss} is the coefficient that determines the standard deviation, N is the window length that is determined according to maximum step number, *K*=127 is the design constant that is obtained from 6-bit current generator (2^7-1), α_{lin} and α_{ex} are the constants used to determine

slope of the linear and exponential currents. The maximum step number of the current waveform is determined as N=10 since any higher N does not provide significant resolution benefit at the electrode [82] while increasing the power dissipation due to higher switching losses. The net charge transferred to the electrodes is preserved at the same level to provide fair comparison across different waveform shapes, with total charge per phase given by:

$$\sum_{n=1}^{10} I(n)\Delta T_{ph} \tag{3.8}$$

where $I(n)$ is the current amplitude at the nth step and ΔT_{ph} is the current step size. For 50 µs stimulation phase width (T_{ph}) and 10 steps, waveform ΔT_{ph}= 5 µs. The electrode voltage for a given electrical model is the sum of resistor and capacitor voltages, which can be expressed in discrete time domain as in Eq. (3.9):

$$V_{elec}(k) = R_{bulk}I_{stim}(k) + \frac{1}{C_{surf}}\sum_{i=0}^{k} I_{stim}(i)\Delta t \tag{3.8}$$

where Δt is the time step for summation, which is chosen as 1 ns (<< τ_{RC} and T_{ph}) to provide accurate calculation. Figure 3.21 illustrates stimulation currents with different pulse waveform shapes, and corresponding electrode voltages, where all pulses provide 500 µA average current at each stimulation phase. The electrode-tissue interface model has R_{bulk}=3 kΩ and C_{surf}=10 nF [49]. The waveform shapes are optimized by varying the slope parameter (α) to obtain the lowest maximum electrode voltage at each shape. Maximum electrode voltage (V_{Max}) is shown for each waveform type in Figure 3.22, where all values are normalized with respect to the maximum electrode voltage of the rectangular waveform. The optimized waveforms provide 9%,17% and 20% electrode voltage reduction for Gaussian, linear decreasing and exponential decreasing current pulses, respectively. Hence, the lowest electrode voltage is obtained for exponential decreasing waveform shape, which allows reduction in supply voltage by 20%. The power dissipation of the interface is thus

reduced by at least 20% for the same average current, and potentially more depending on the extend of leakage diminution with voltage, which varies significantly with process technology.

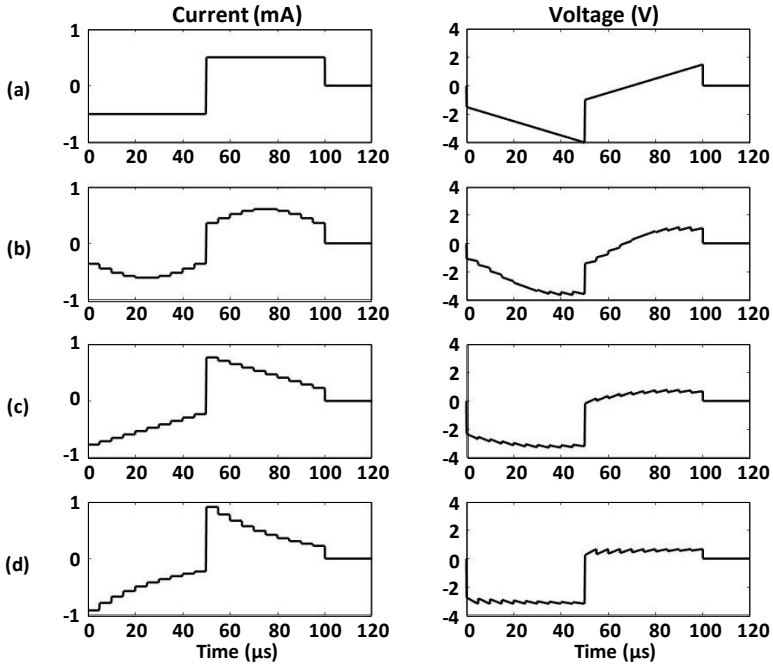


Figure 3.21. Stimulation current and corresponding electrode voltages for (a) rectangular, (b) Gaussian, (c) linear and (d) exponential pulse shapes.

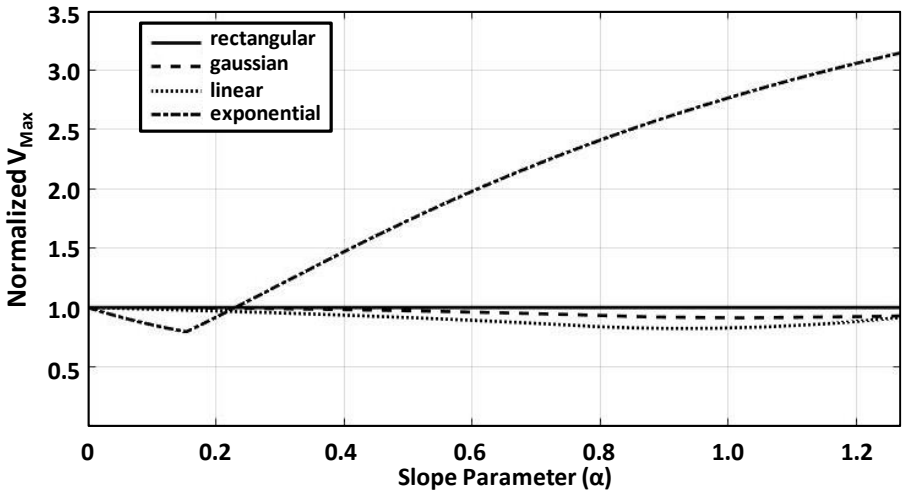
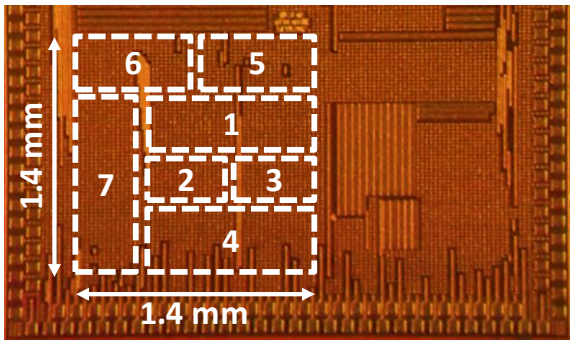


Figure 3.22. Variation of the normalized (V_{Max}) with respect to the slope parameter (α).

3.4. Test Results and Discussions

The 2nd generation FICI interface circuit is designed and fabricated in XFAB 180nm high-voltage CMOS technology, where the die micrograph is depicted in Figure 3.23, with 1.4x1.4 mm^2 active die area. The implemented chip is packaged on CPG 120 package which has 120 pin connections and allows to check all the testing blocks at a single package. Figure 3.24 shows designed and implemented testing PCB of the 2nd generation FICI interface electronics that also includes buck and boost DC-DC converters to generate 1.8 V and 5.5-10 V from3.3 V supply to power-up low and high voltage circuits.



1. **Logarithmic Amplifiers**
2. **Current Rectifiers**
3. **CMs & LPFs**
4. **Sample/Hold**
5. **Control Unit**
6. **Stimulation Current Generator**
7. **Switch Matrix**

Figure 3.23. Die micrograph of the implemented 2nd generation FICI interface electronics.

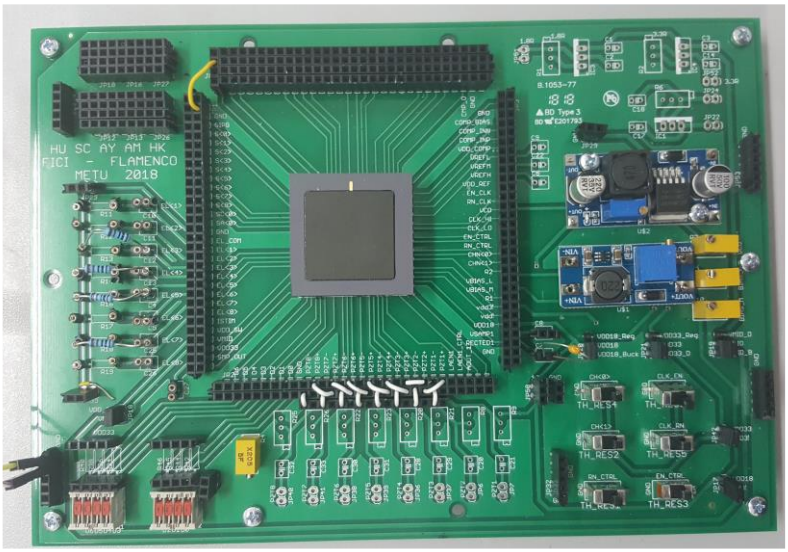


Figure 3.24. Fabricated test PCB of 2nd generation FICI interface electronics.

As the first, performance of the logarithmic amplifier (LA) is tested to validate compression performance of the system. Figure 3.25 depicts the measured input/output characteristics of the LA operating at 5 kHz, with input representing the sensor output range from [46]. The amplifier compresses the 60 dB input dynamic range into 17 dB electrical range, while providing AC current output. As the input voltage increases the number of amplifying stages reduces, hence the amplifier compresses the input range. The trendline in the figure illustrates the logarithmic compression of the output current with respect to the input voltage. The validated bandwidth of the amplifier is high enough to provide frequency independent performance up to 5 kHz, covering the frequency band for daily speech.

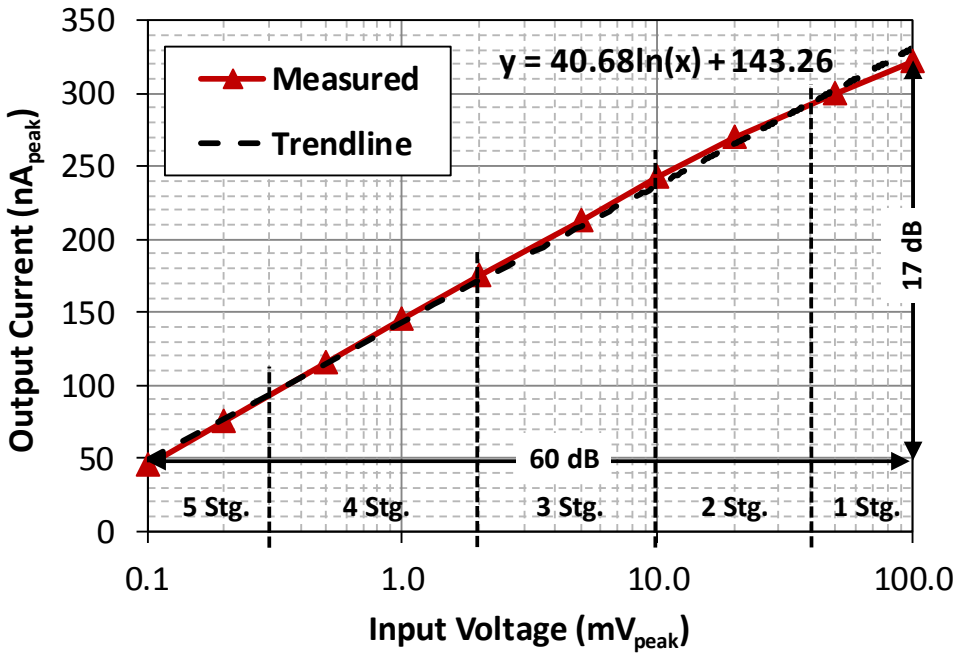


Figure 3.25. Measured input voltage versus output current characteristic of the LA.

Then, overall operation of 8-channel FICI interface circuitry is validated by applying different input voltage levels as sensor output. Figure 3.26 illustrates the measurement of the generated 8-channel stimulation currents based on CIS, where current level at each channel can be tuned by changing the digital control signals D_0-D_6. As illustrated, although the input voltage increases linearly from 1st to 8th channel, the

stimulation current level changes logarithmically to fit the input to the electrical dynamic range of the ear.

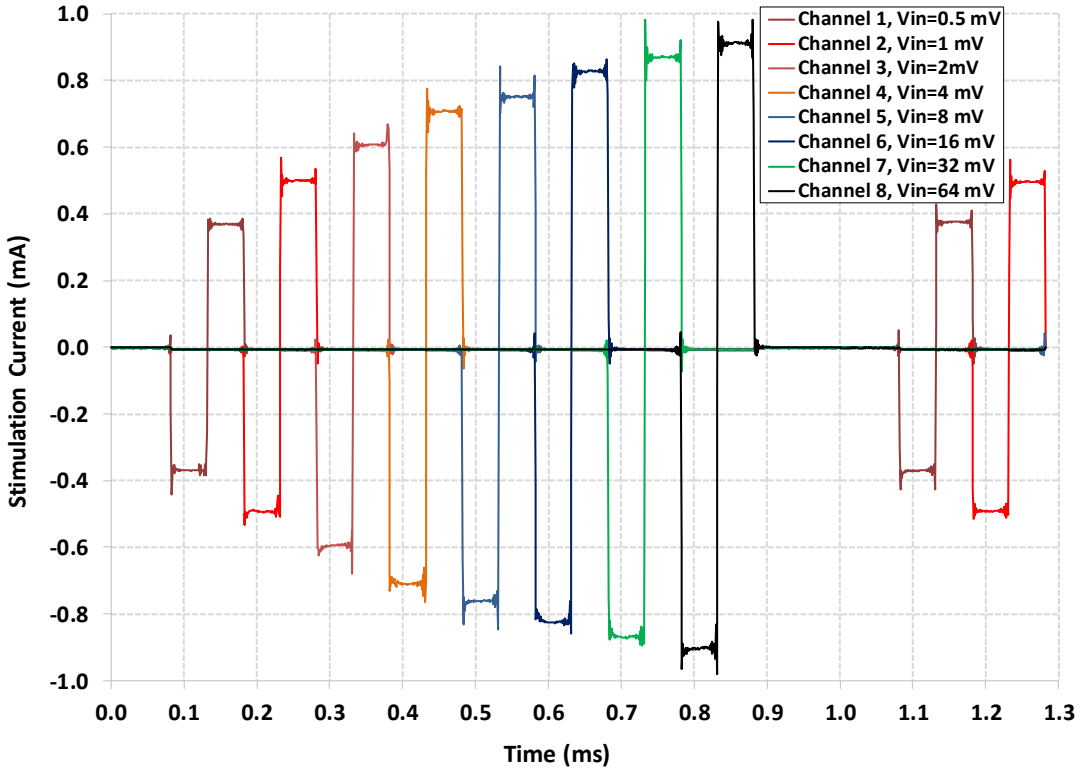


Figure 3.26. Generated 8-channel stimulation (CIS) currents where input peak voltage increases linearly from 0.5 mV (1st channel) to 64 mV (8th channel).

Neural stimulation waveform is validated next by changing the waveform shape via D_0-D_6 control. Figure 3.27 depicts the stimulation current and the electrode voltage for rectangular and optimized exponential decreasing waveforms with artificial neural load (R_{bulk}=3 kΩ and C_{surf}=10 nF[49]). As expected from simulations, optimized waveform shape leads to reduction in the maximum electrode voltage by 20%. Although the amplitude of the optimized stimulation current waveform is higher, the average value is not. The result firmly concedes 1.5 V reduction in high voltage supply, from 7 V to 5.5 V.

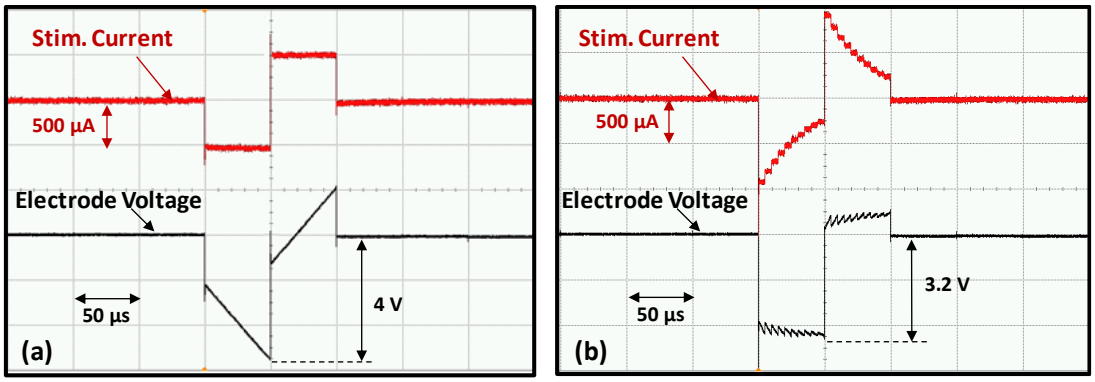


Figure 3.27. Stimulation current and electrode voltage for (a) rectangular and (b) optimized exponential current waveforms.

The implemented FICI interface electronics is then tested with a speech signal "A white silk jacket goes with any shoes", which is a common sentence utilized in speech-in-noise tests [85]. Figure 3.28 depicts the test setup. The sound is detected through a microphone, and is converted into digital speech data through Matlab. The mechanical filters presented in [46] are imported into Matlab, and applied to the speech data to mimic the 8 channel PZT sensor output. The 8-channel PZT sensors were designed by Bedirhan İlik where the sensor topology is presented in Figure 3.29 (a). Validation of the fabricated sensors (Figure 3.29 (b)) are continuing, hence simulation results of the design is utilized to provide mechanical filtering characteristics of the sensors as provided in Figure 3.29 (c). The mimicked speech signals are then applied to the FICI interface electronics through Keysight 33522B signal generator, which is controlled by BenchVue software. The output response of the interface electronics is measured through NI9232 high voltage data acquisition board (DAQ) and LabVIEW software.

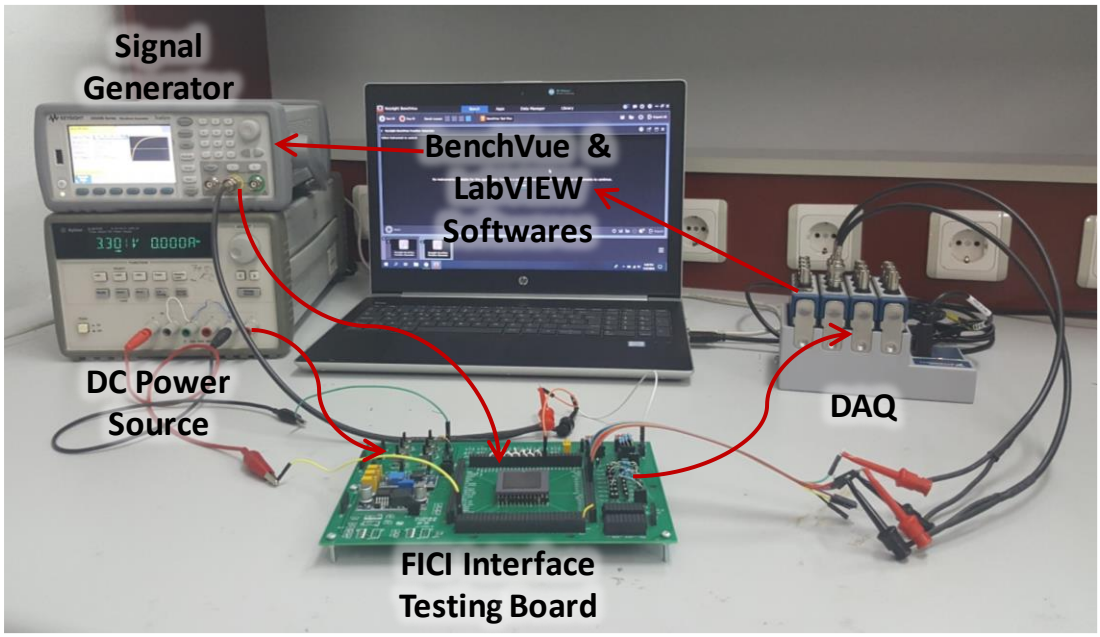


Figure 3.28. Test setup of the 2nd generation FICI Interface electronics with speech signal.

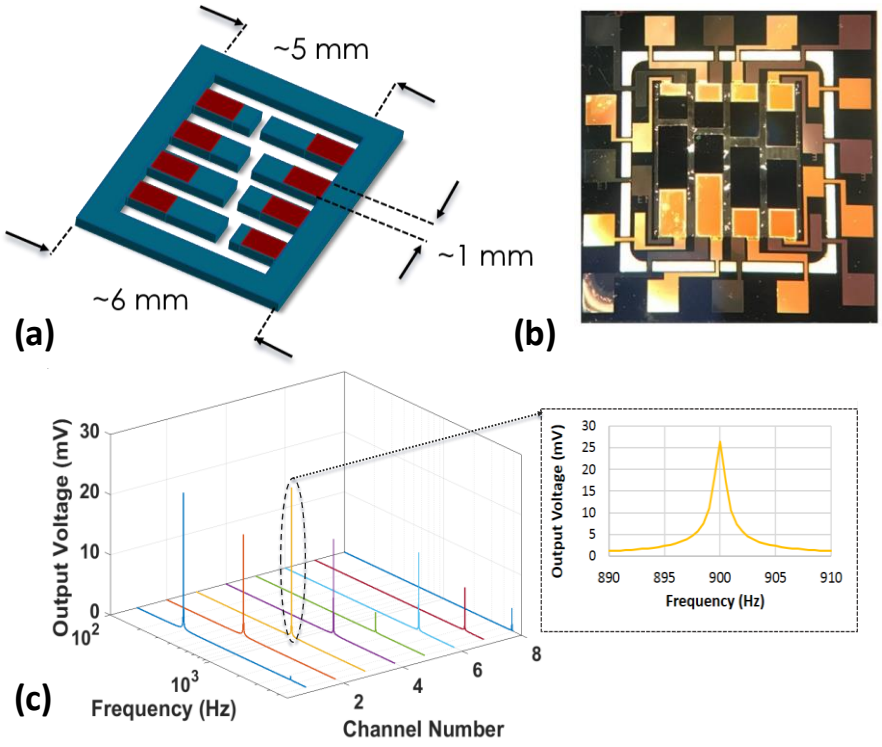


Figure 3.29. (a) Schematic view of the 8-channel PZT sensors, (b) fabricated device micrograph, and (c) simulation results of mechanical filter characteristics of the sensors [86].

Figure 3.30 (a) and (b) show the histogram of the speech signal, and the measured electrodogram from the 8-channel FICI interface, respectively, confirming that different frequency components of the speech are correctly obtained at the corresponding FICI channels. The FICI outputs have high precision at low frequency (<3 kHz), which captures the voice range. The reconstructed speech signal from the stimulation electrodes of the FICI interface electronics (Figure 3.31 (b)) is compared against the time-domain waveform of the speech signal recorded by the microphone (Figure 3.31 (a)). Although mechanical filters lead to limited perception of high frequency components, the envelope of the reconstructed signal coincides with the envelope of the real speech signal, which validates operation of the interface in a real application. The power dissipation for the given speech signal is measured as 472 μW, while operating with the optimized current waveform.

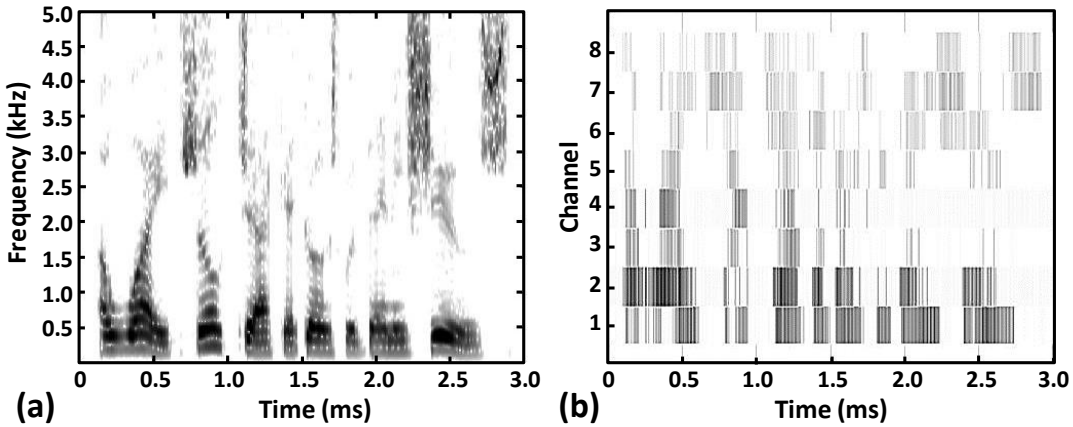


Figure 3.30. (a) Histogram of the speech signal recorded by the microphone, and (b) electrodogram from the stimulation electrodes of 8-channel FICI interface.

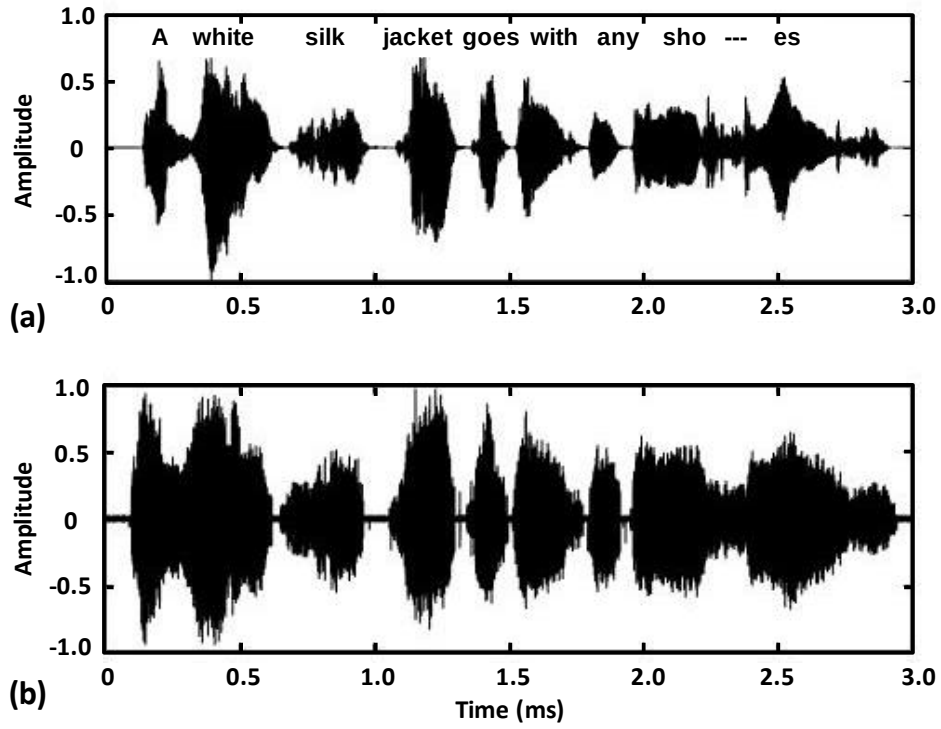


Figure 3.31. Time-domain waveform for (a) the speech signal recorded by the microphone, and (b) the reconstructed speech signal from stimulation electrodes of the FICI interface electronics.

Table 3.2 details the power dissipation analysis of the FICI interface electronics for rectangular and optimized exponential current pulse shapes. The optimized waveform enables reduction of the supply voltage of the current stimulator (switch matrix and HV switch control), which is the most power hungry part of the design. Hence, the total power dissipation of the system is reduced by about 20% through waveform shape optimization. Moreover, the front-end signal conditioning circuit (system excluding the stimulator) operates with 19.7 μW, which is one of the lowest value provided in the literature. Table 3.3 presents comparison of the FICI interface with the state-of-the-art circuits. The input dynamic range of the proposed circuit is similar to the previous reports, and provides adequate perception of the input sound. 7-bit patient fitting resolution provides better control of minimum threshold and maximum comfort level of the stimulation current. The circuit predominantly operates in current mode, with minimum overhead associated with current-voltage signal translations,

and provides the lowest power dissipation both for the front-end signal conditioning and stimulator units.

Table 3.2. Power Consumption of the 2nd generation FICI Interface Circuit.

System Components	Rectangular		Optimized Exp.	
	Voltage (V)	Power (µW)	Voltage (V)	Power (µW)
Logarithmic Amplifier	1.8	2.1	1.8	2.1
Current Rectifier	1.8	2.0	1.8	2.0
Current Multiplier with LPF	3.3	2.3	3.3	2.3
Sample and Hold	3.3	3.2	3.3	3.2
Control Block	1.8	2	1.8	2
HV Switch Control	7-10	10.2	5.5-8	8.1
Switch Matrix (Stimulator)	7-10	570	5.5-8	452
Total		591.8		471.7

Table 3.3. Comparison of 2nd generation FICI interface electronics with state-of-the-art.

Parameters	TBME05 [47]	JSSC05 [48]	JSSC15 [49]	1st Gen. FICI	2nd Gen. FICI
Technology	1.5 µm	0.8 µm	180 nm	180 nm	180 nm
Active Die Area (mm^2)	9.6 x 9.2	3.5 x 6.0	1.8 x 1.9	2.0 x 1.5	1.4 x 1.4
Number of Electrodes	16	16	8	8	8
Dynamic Range (dB)	77	60	60	40	**60**
Patient Fitting	7-bit	5-bit	6-bit	-	**7-bit**
Front-End Power (µW)	211	126	93	51.2	19.7
Stimulator Power (µW)	-	2000*	479	640	452
Total Power (µW)	-	2126	572	691.2	**471.7**

To conclude the presented ultra-low power bionic ear interface senses the implantable PZT outputs and stimulates the auditory neurons accordingly. The interface is designed, implemented, and fabricated in 180 nm HV process, and is validated through a speech signal to demonstrate proof-of-concept operation with both circuit design and waveform optimizations. The proposed system is the first FICI interface with 60 dB input dynamic range and patient fitting compatibility (stimulation current from 0 to 1 mA, minimum threshold and maximum comfort levels, respectively) that operates with total power dissipation of ~470 μW. The superior power dissipation profile of the system results from the concomitant optimizations in system architecture, circuit design, and stimulation waveform shape. Sub-500 μW operation of the interface electronics enables long-term system reliability with a lifetime of more than 30 years, using a typical implantable battery with limited capacity. A major impediment in the prolonged use of cochlear implants is hence overcome, which results in reduction of healthcare cost and risks associated with surgical battery replacements.

Although, performance of the 2nd generation FICI interface electronics has been validated with electrical signal that mimics speech signal and with artificial neural load, testing the interface with acoustically driven PZT sensor and stimulating auditory neurons of a living subject validates operation of the system at a real application. Therefore, the next chapter includes application of the system to a guinea pig ear as an in-vivo test.

CHAPTER 4

IN-VIVO TESTS OF THE FICI INTERFACE ELECTRONICS

In-vivo tests of biomedical devices help to observe viability of the design on a living subject and show appropriateness of the system for a real application. To demonstrate the performance of the proposed interface electronics in product-like environment, the system has to be tested on an animal such as guinea pig. The in-vivo tests must be carried in the following order: As the first step, normal hearing performance of the guinea pig has to be tested through auditory brainstem response (ABR) measurements. Then, distortion products of otoacoustic emissions (DPOAE) of the healthy ear is measured to observe the functionality of hair-cells. Next, the hair-cells are damaged in order to (at least partially) deafen the ear. The damage of the hair-cells is observed by DPOAE. Afterward, the auditory neurons are stimulated with a controlled current source, and electrically evoked auditory brainstem response (eABR) performance is measured. After validation of electrical stimulation, the cochlear electrode is placed inside cochlea of the guinea pig, and stimulation of the auditory neuron is done through the FICI interface electronics. The 2^{nd} generation FICI interface electronics is combined with a PZT sensor, which senses the sound inputs for the acoustical tests. As a result, the in-vivo tests of acoustical input FICI system with wide dynamic range and ultra-low power dissipation are conducted for the first time in the literature.

Organization of this chapter is as follows: The next section presents ABR tests of a healthy guinea pig. Section 2 includes DPOAE tests of healthy and damaged hair-cells at the cochlea of the guinea pig. The eABR tests of the guinea pig are presented in Section 3. Finally, Section 4 presents validation of the proposed FICI system with in-vivo tests.

4.1. ABR Tests of the Guinea Pig

The ABR is a recording of the discharge of auditory neurons due to acoustical stimulation, which is measured from far-field. The measured potentials are generated from nuclei of the auditory pathway [87]. Before starting the measurements, the guinea pig must be anesthetized. The most widely used anesthesia for guinea pigs is the combination of Ketamine (90 mg/kg) and Xylazine (10 mg/kg) where the anesthesia level is controlled during the experiment and external dose of ketamine can be applied to complete the measurements. The recordings of brainstem response are conducted with the SmartEP software and Universal Smart Box hardware systems of Intelligent Hearing Systems (IHS).

Figure 4.1 shows the test setup for the ABR measurements of a guinea pig. The sound is provided by high frequency transducers with insert earphones, which are plugged to the ears of the guinea pig. The brain response of the guinea pig is measured via an optical amplifier with needle electrodes are utilized as the probes of the amplifier. The measurement electrodes are connected as shown in Figure 4.2: Electrode on the right mastoid *(A2)* is connected to the Red Inverting *(-)* electrode position. Electrode on the left mastoid *(A1)* is connected to the Blue non-inverting *(+)* electrode position. Electrode on the forehead *(Fpz)*, connected to the Black ground electrode position. To obtain significant, clean, and repeatable responses, it is better to have impedance close to 1 kΩ. Since the hardware is based on differential amplifiers, the impedance should be matched across each channel. Both the amplifier and the high frequency transducers are controlled by Universal Smart Box. Since the ears of guinea pigs are more sensitive to high frequency sounds the measurements are conducted by applying 16 kHz tone-burst acoustic stimuli for 2 ms. The measurements are taken with 21.1 Hz stimulation rate for 512 times and averaged.

Figure 4.3 and Figure 4.4 show the measured ABR recordings for acoustical stimuli from right and left ears, respectively, where the observed waveform shapes are consistent with previous ABR recordings in [87]–[89]. The acoustical stimuli is applied with 90 dB SPL and reduced systematically to determine the threshold level

of hearing at each ear. As the sound level decreases the latency of the peaks are delayed in time and amplitude of the observed peaks are reduced as expected. For the right ear, minimum threshold is determined around 45 dB; on the other hand the left ear has a threshold around 35 dB.

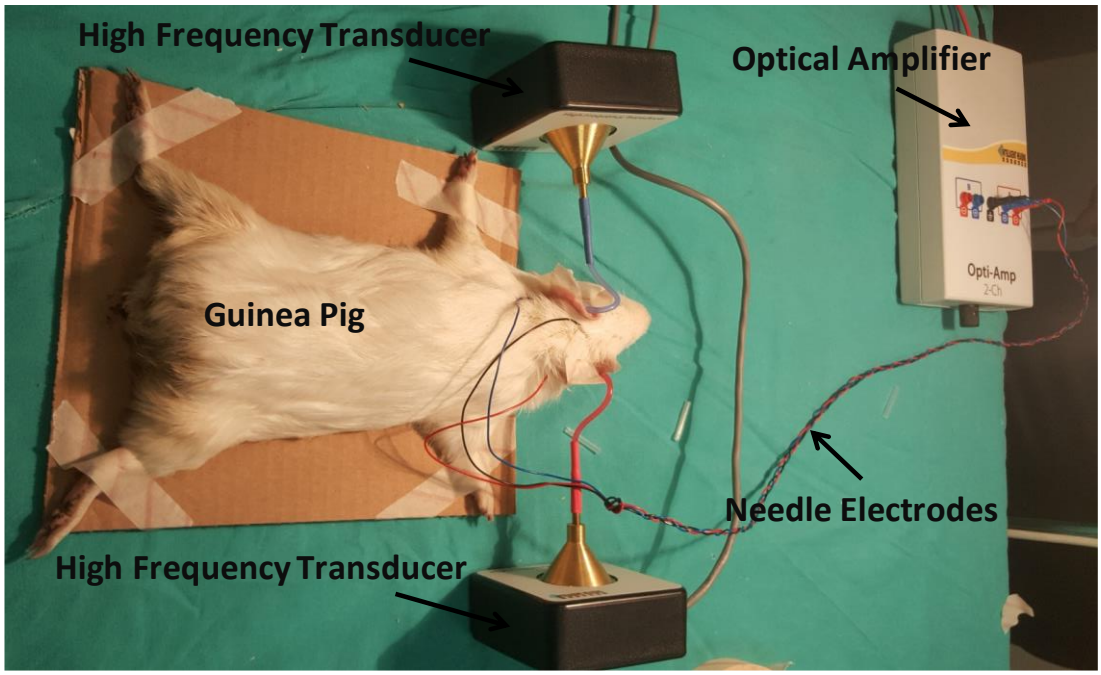


Figure 4.1. Test setup for the ABR measurements with high frequency transducers.

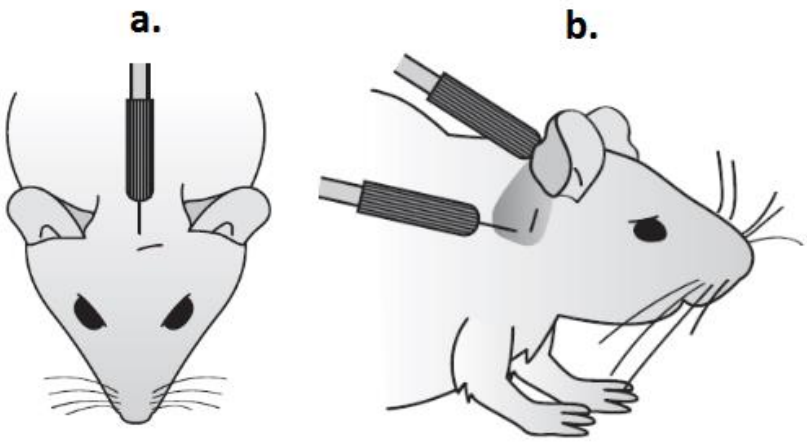


Figure 4.2. Placement of measurement electrodes to the (a) forehead and (b) mastoids.

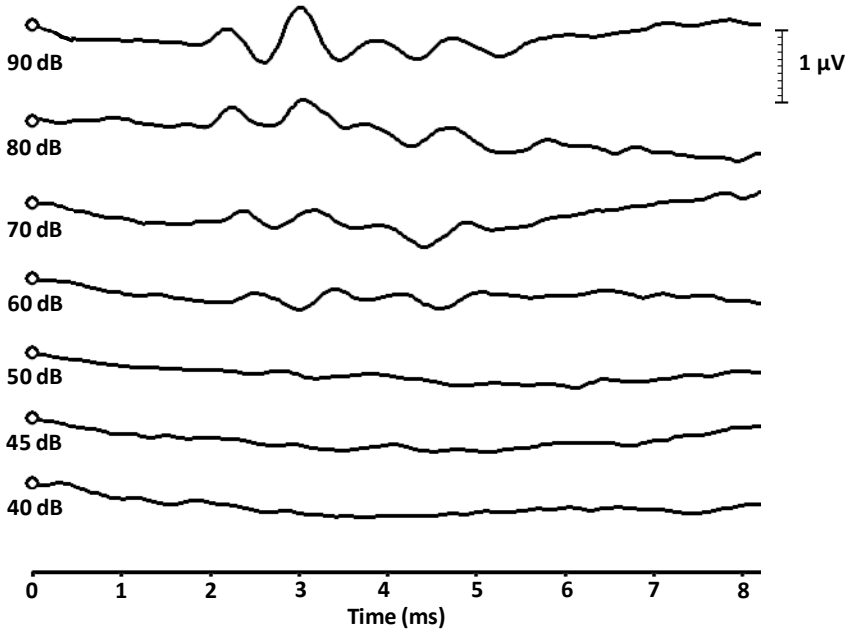


Figure 4.3. ABR response of the guinea pig for 16 kHz tone-burst stimuli at right ear.

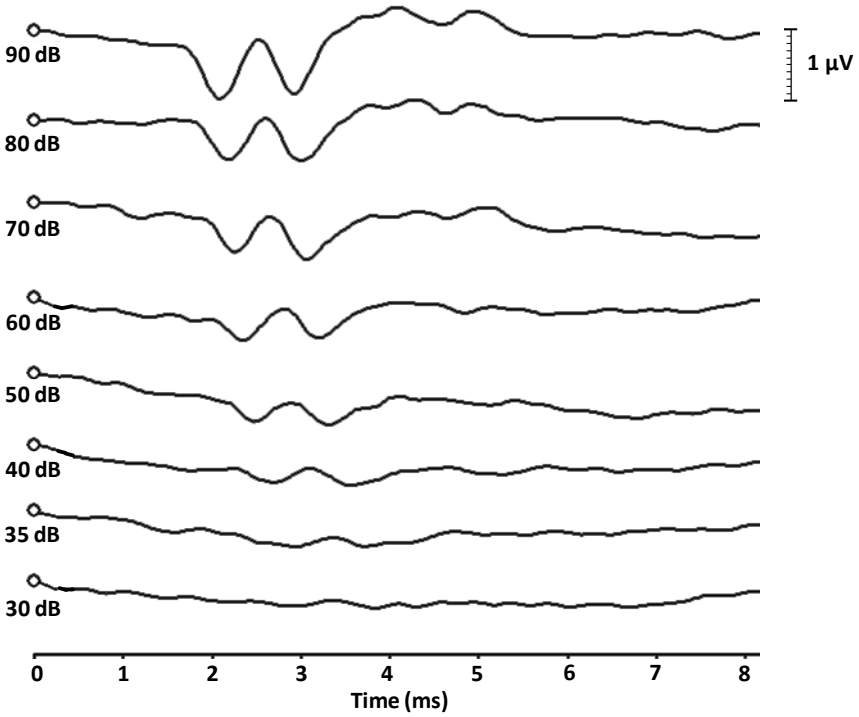


Figure 4.4. ABR response of the guinea pig for 16 kHz tone-burst stimuli at left ear.

4.2. DPOAE Tests of the Guinea Pig

After proving that guinea pig ear respond to acoustical stimuli, the functionality of hair cells in cochlea can be measured. The absence of hair cells is the most significant reason to use cochlear implant as the hearing device. In order to verify the functionality of outer hair cells, the otoacoustic emissions, which are sounds originated from the motion of hair cells, can be utilized. The otoacoustic emissions can be measured by applying two acoustic signals with close frequency and observe the reflecting sounds by a microphone at the ear canal. This method is called as distortion product otoacoustic emission (DPOAE) that is first applied by D. Kemp in 1978 [90]. Figure 4.5 illustrates formation of otoacoustic emission formation. Figure 4.5 (a) shows traveling waves at the basilar membrane with frequencies f_1 and f_2. When these frequencies match with the corresponding frequency position, maximum resonance is observed as shown in Figure 4.5 (b). Since this operation is non-linear, distortion products of these signals are generated at $2f_1$-f_2 and $2f_2$-f_1 where DPOAE waves of these signals are traveling at opposite direction as presented in Figure 4.5(c).

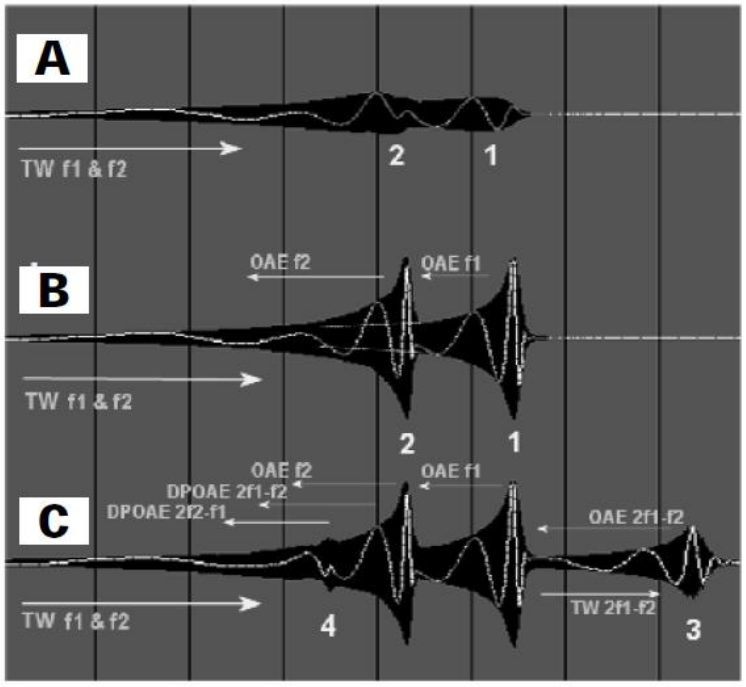


Figure 4.5. Development of traveling waves and otoacoustic emission formation [91].

In our system the hair cell functionality is determined by DPOAE for both low and high frequencies. The DPOAE provides frequency dependent functionality of the hair cells. Figure 4.6 shows placement of earphones and microphone to the guinea pig ear for DPOAE measurement. The red and blue tubes provide acoustic signal with close frequencies and the microphone (black cable) senses the otoacoustic emission at the ear canal. The components are plugged to the ear through a special apparatus.

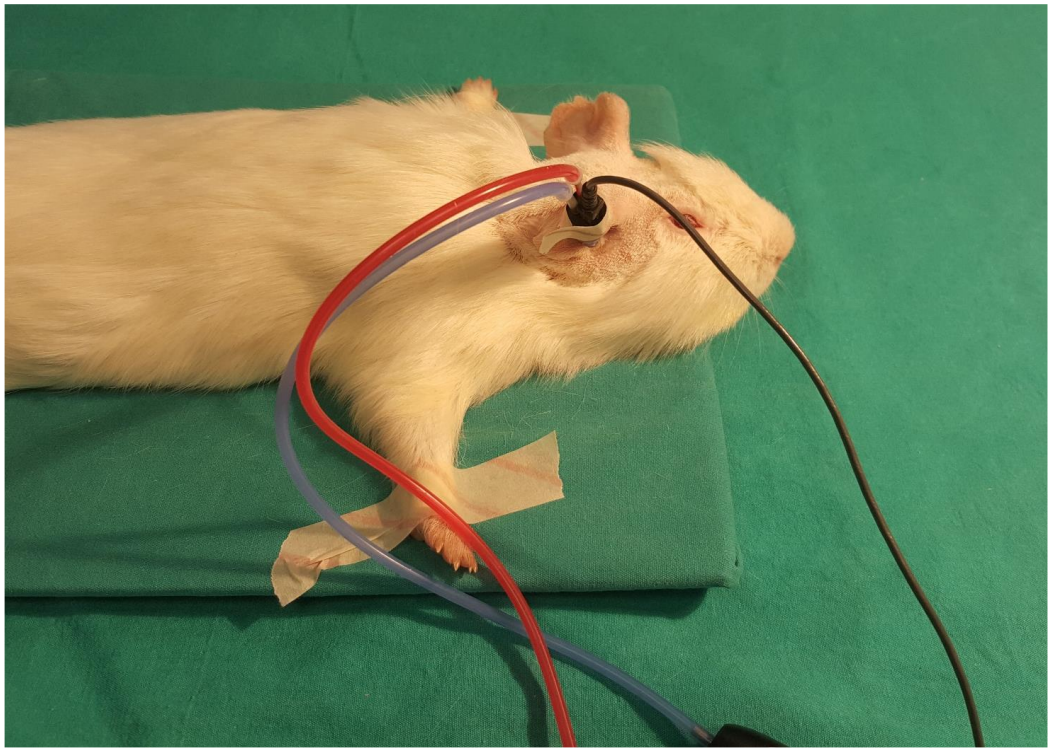


Figure 4.6. Earphone and microphone placement for DPOAE measurement on guinea pig.

As the first functionality of the outer hair cells, which are close to the base of basilar membrane and correspond to high frequency are measured. Figure 4.7 shows DPOAE recording of the guinea pig from left and right ears at the frequency range of 16 kHz to 32 kHz. High frequency transducers are utilized to give acoustical sound, since regular earphones are not suitable to provide sound at this range. The measurements show that the response of the hair cells is above the noise level for both ears and provide functionality of these hair cells.

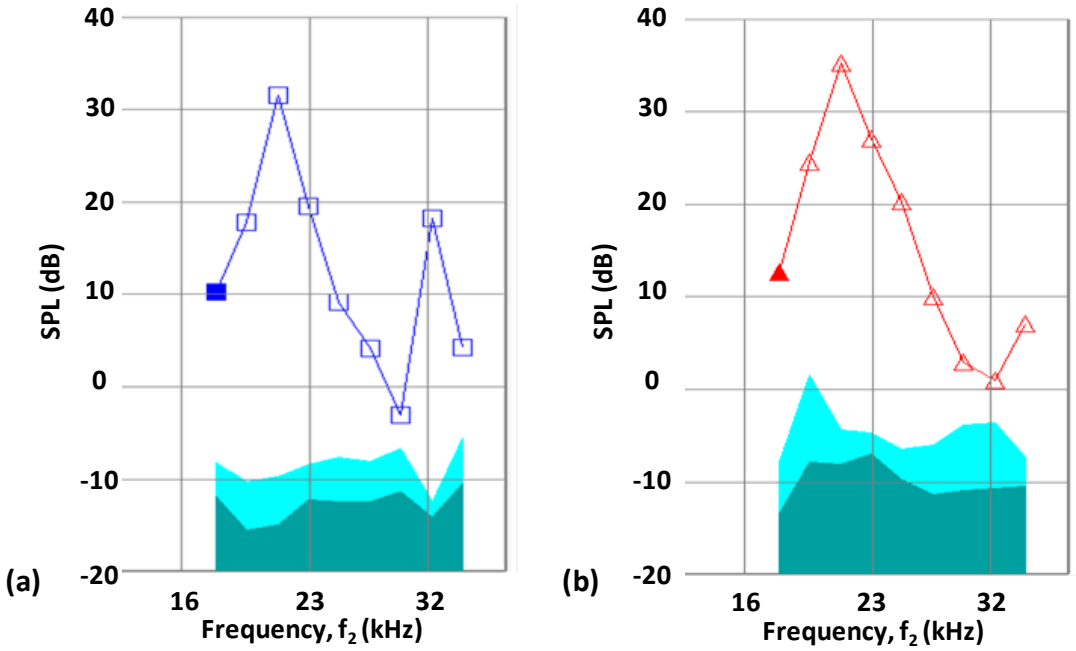


Figure 4.7. DPOAE recording for high frequency sounds from (a) left and (b) right ears of the guinea pig.

The low frequency response of the guinea pig is measured from right ear since the cochlear electrode implantation is going to be placed to this ear. The cochlear electrode has two stimulation electrodes which are close to apex position, and are hence effective at low frequencies. The low frequency sound signals are supplied from ER3A earphones (Etymotic©) that can provide sound signals up to 16 kHz stimulation. Figure 4.8 shows DPOAE recordings taken from the right ear of a healthy guinea pig at the frequency range of 500 Hz to 8 kHz. The response shows that guinea pig has fine hearing above 4 kHz which provides signals above the threshold level. As the next step, the guinea pig is partially deafened through a surgery and the DPOAE response is measured at low frequencies. Figure 4.9 shows the low frequency DPOAE response, where the results are much worst compared to healthy ear. The signals measured at partially deafened ear has results below the noise level around 6 kHz. Moreover the respond above 3 kHz are highly observed below 0 dB SPL, which is a threshold for functionality.

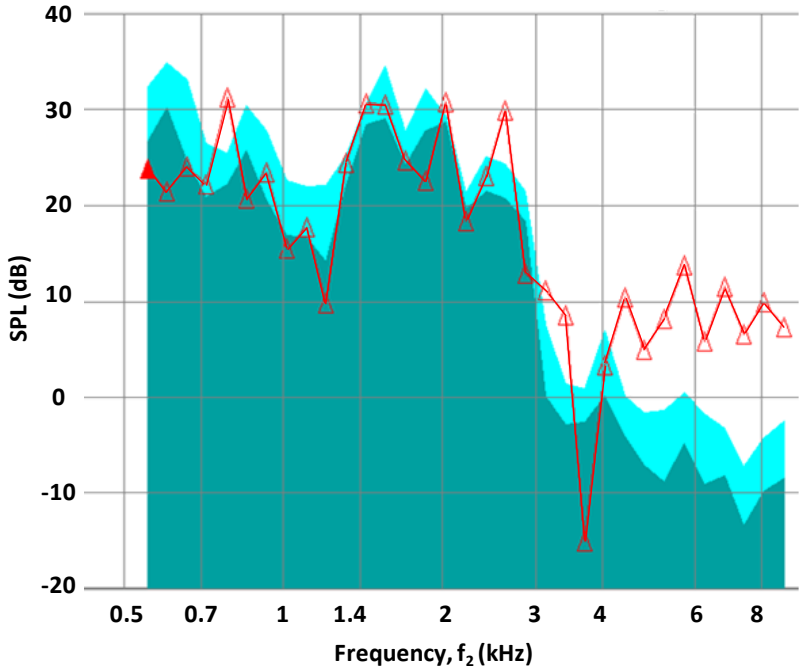


Figure 4.8. DPOAE recordings for low frequency sounds from right ear of healthy guinea pig.

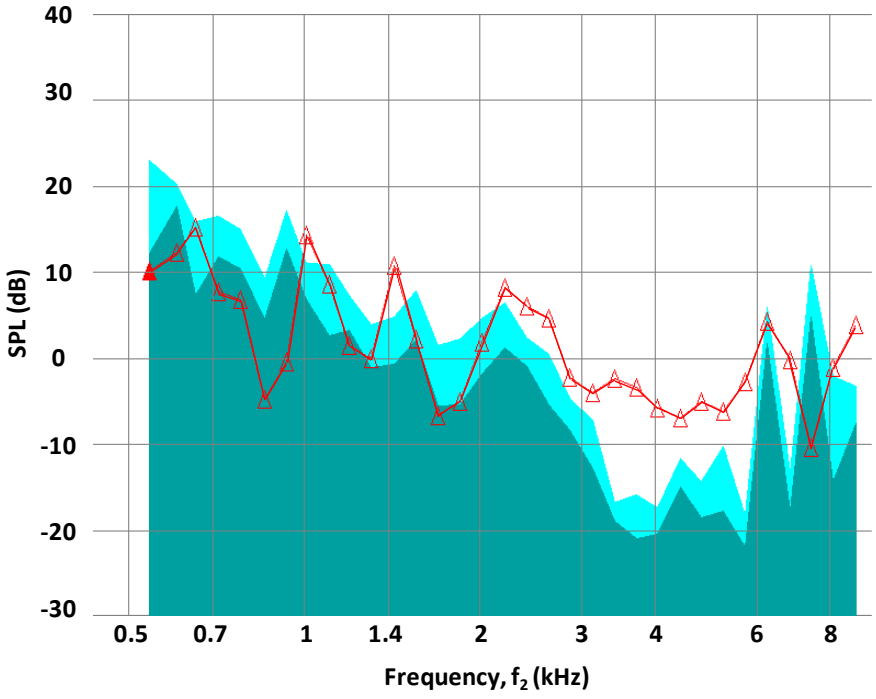


Figure 4.9. DPOAE recordings for low frequency sounds from right ear of partially deafened guinea pig.

4.3. eABR Tests with a Controlled Current Source

Before applying electrical stimulation with the designed FICI interface, the electrical stimulation of auditory neurons is verified with a controlled current source, which is a low current stimulator provided from IHS. Before the tests the guinea pig must be anesthetized similar with the one explained in ABR section. Figure 4.10 shows the block diagram of the electrically evoked auditory brainstem response (eABR) test setup. The Universal Smart Box drives the Low Current Stimulator and tunes the stimulation current level. The stimulator evokes auditory neurons of the Guinea Pig. The ABR of the guinea pig is measured through optical amplifier which delivers the measured results to the Universal Smart Box. The eABR tests are carried by stimulating the promontory through needle electrode similar with the one shown in Figure 4.11. In the presented figure, the electrode is transtympanically pierced through the tympanic membrane; however in our case the electrode is placed surgically. This electrode delivers biphasic rectangular electrical pulses, which has a 50 μs stimulation pulse width per phase. In addition, a reference stimulation electrode is placed subcutaneously in the pre-auricle area of the ipsilateral ear.

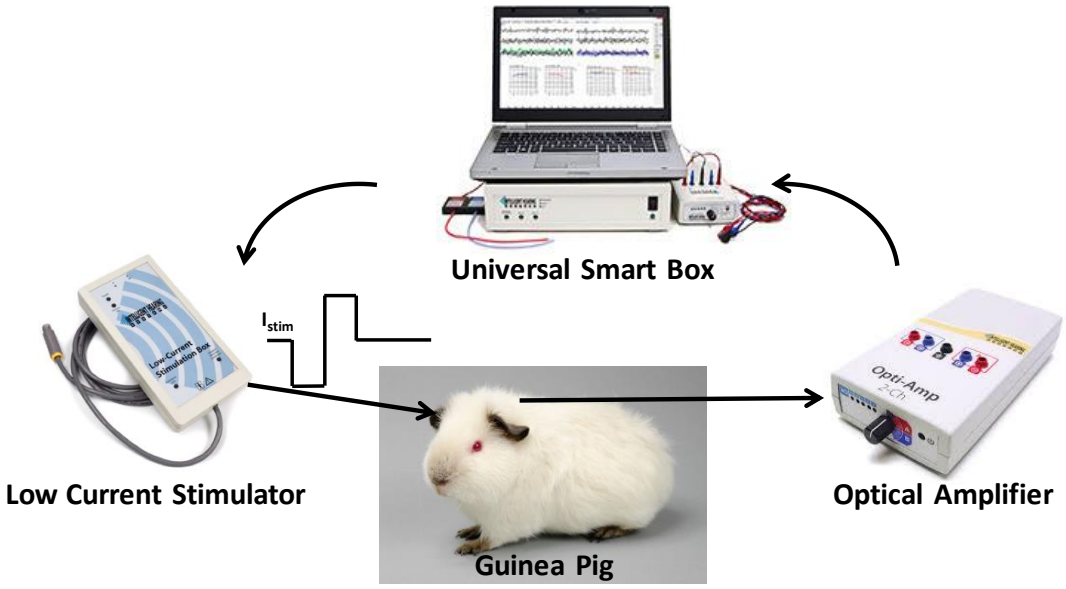


Figure 4.10. Block diagram of the eABR test setup with controlled current source.

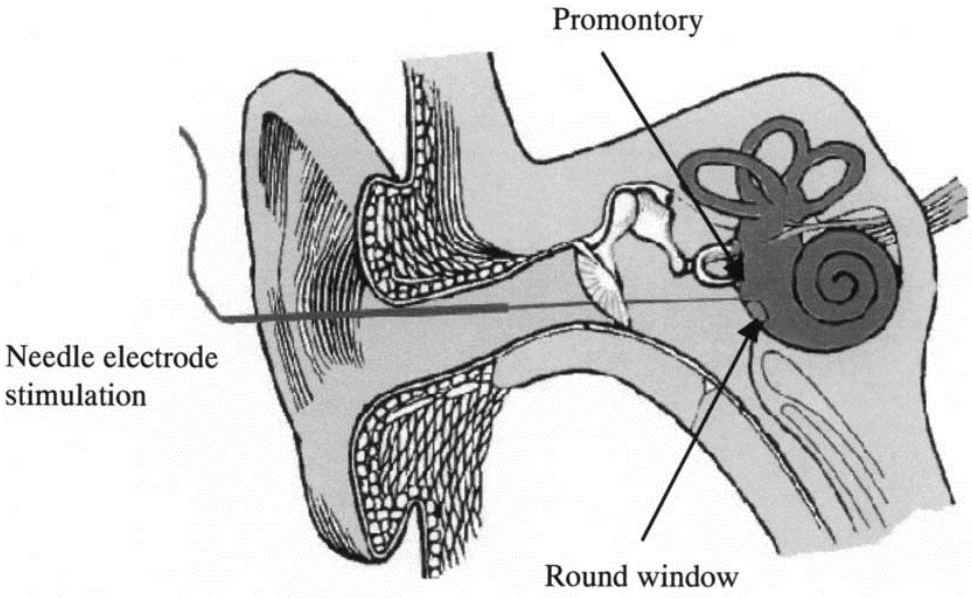


Figure 4.11. Electrical stimulation of promontory with needle electrode [92].

The needle electrodes for the measurement of the ABR recordings is placed as shown in Figure 4.12. The Inverting (-) electrode is connected to Vertex (Cz), the Non-Inverting (+) is connected to the back of the Neck, and finally the ground electrode is connected to the Mid-Forehead (or Leg) of the guinea pig.

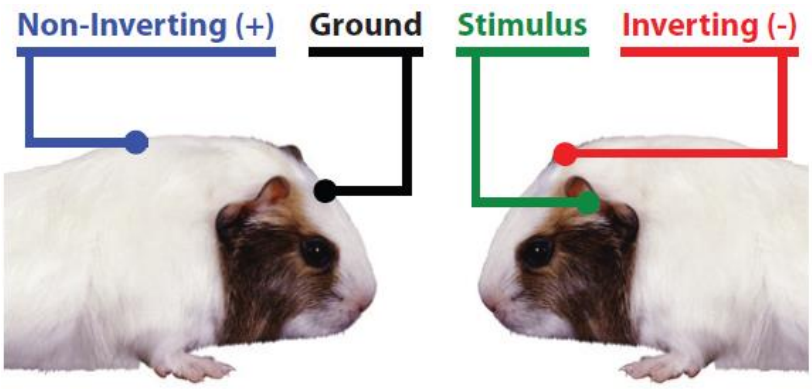


Figure 4.12. Recording electrode placement for eABR tests of the guinea pig [93].

Figure 4.13 shows the measurement result of the eABR tests with controlled current source where the stimulation current is increased gradually to observe the change at the brainstem response and determine the threshold level for the stimulation current

amplitude. The threshold level is determined around 500 μA peak value which is consistent with previously reported eABR results [87]. Increment at the stimulation leads to monotonic increment at the peak value of ABR response as expected, where the stimulation performance is tested up to 1 mA current amplitude. However, the stimulation performance is highly dependent on the position of the stimulation electrode on the promontory. Therefore, direct stimulation of the auditory neurons through intra-cochlear electrodes provides much more stable response, which is applied for eABR tests of the FICI interface, as explained in next section.

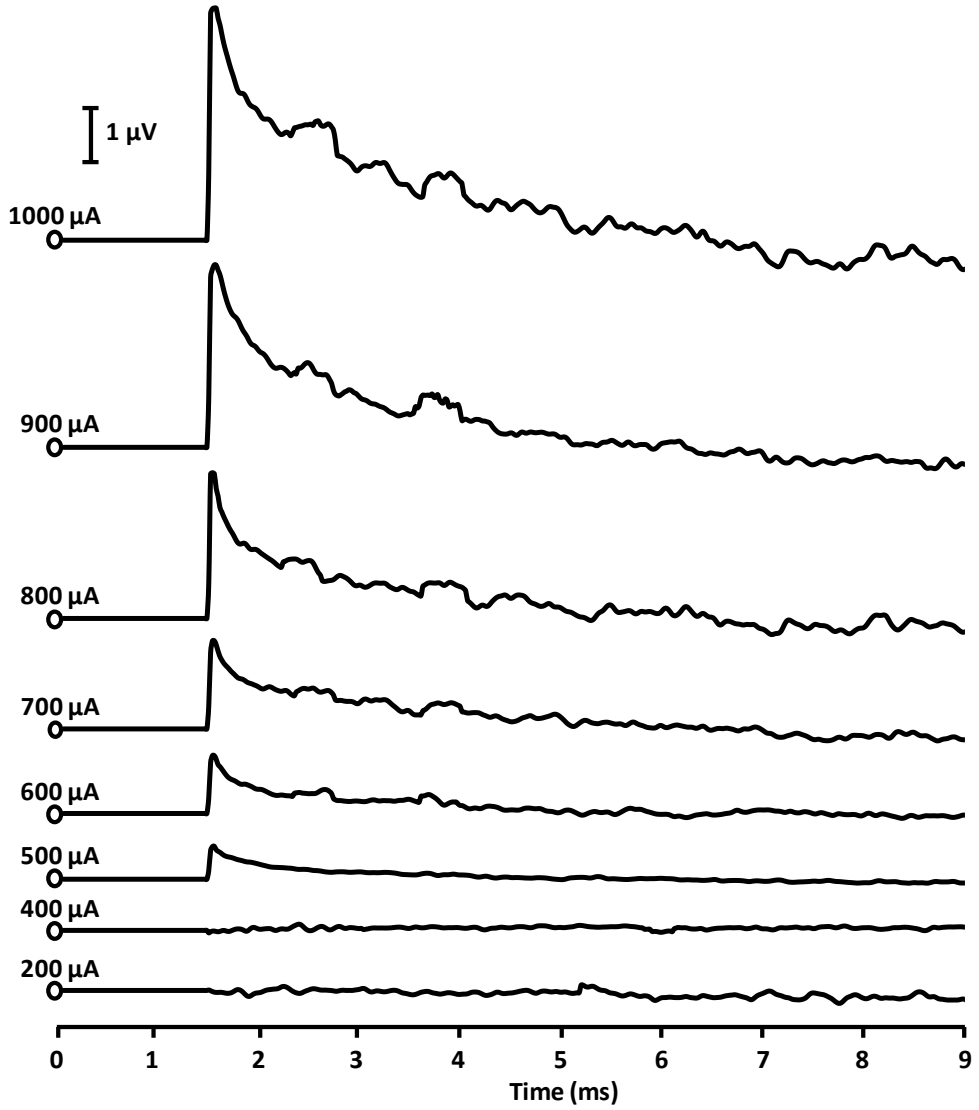


Figure 4.13. Measurement results of the eABR tests with controlled current source.

4.4. eABR Tests with the FICI Interface Electronics

After validating electrical stimulation of the auditory neurons through eABR tests with controlled current source, the next step is to validate operation of the FICI system with intra-cochlear eABR tests. Figure 4.14 presents the block diagram of the intra-cochlear eABR test setup with the FICI system. The control of the test setup is arranged by Universal Smart Box where synchronization of electrical stimulation signal and the acquisition system is provided by a signal generator. The signal generator provides external trigger TTL signal and the low frequency clock of the FICI system at 21.1 Hz, which corresponds to sweep rate of the acquisition. Therefore, the FICI interface provides single stimulation at every period of acquisition. The Universal Smart Box controls the earphone ER3 that provides sound output at specified frequency and sound pressure level (SPL). The sound output is detected by the FICI system through the PZT sensor on the membrane where the earplug of the ER3 is mounted to the sensor holder that mimics the ear channel. The PZT sensor output is then applied to the FICI interface that stimulates the auditory neurons through intra-cochlear electrodes. The eABR response of the guinea pig is measured with the optical amplifier, and is provided to the USB Box. The recording electrodes of the optical amplifier are connected similar with the eABR measurements as explained in the previous section.

The intra-cochlear electrodes were placed with a surgery, which is conducted by Prof Mehmet Birol Uğur and Assoc. Prof. Hakan Tutar. The guinea pig was anesthetized during the surgery and experiment. The incision of the surgery was made from post-auricul (behind the ear) and the muscles were dissected to reach the bulla. Then the bulla was drilled to find the round window. A hole was opened to the round window and the intra-cochlear electrode was inserted to the tympanic duct. The cochlear electrodes include 2 stimulation electrodes placed inside the cochlea and a common electrode placed outside the bulla under the muscles (extra-cochlear).

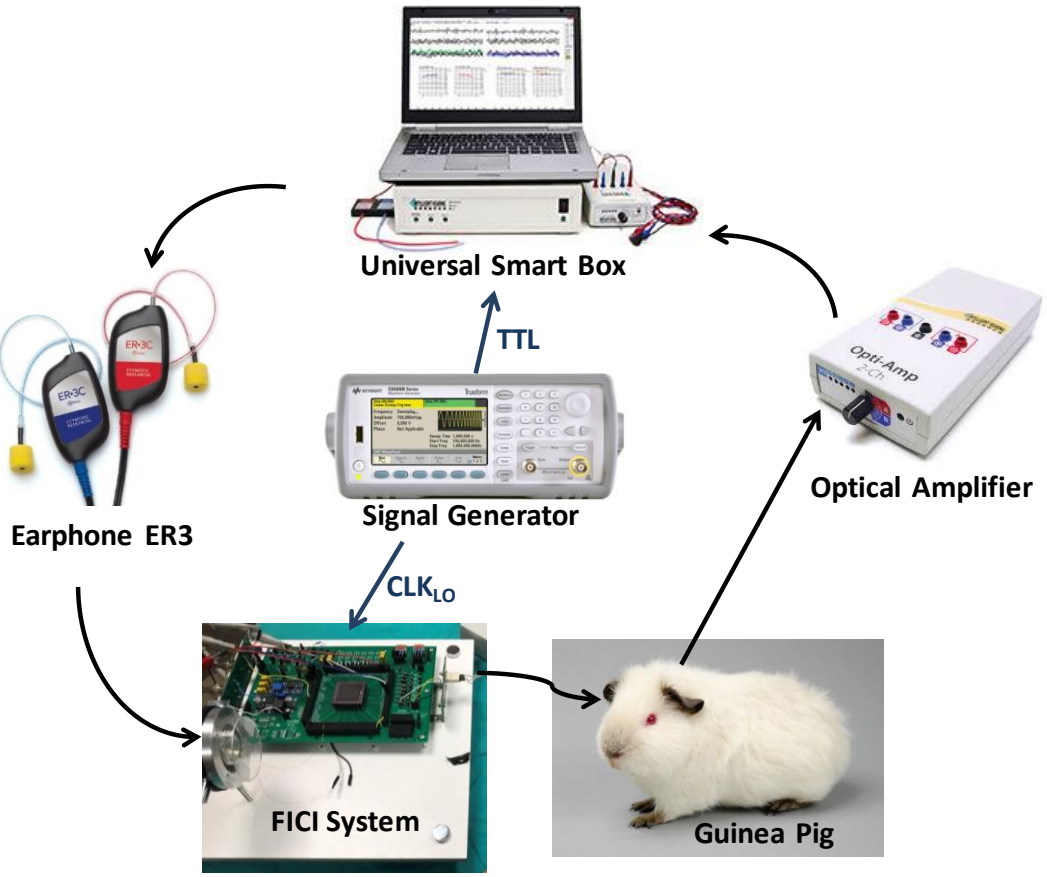


Figure 4.14. Block diagram of the intra-cochlear eABR test setup with the FICI system.

Figure 4.15 presents the FICI system under the in-vivo tests which also shows the surgically placed stimulation electrodes. The in-vivo tests are carried with low profile PZT sensor that can be placed to the middle ear. The PZT sensor is mounted on a parylene membrane that mimics the ear drum. The parylene membrane is placed on a sensor holder that has a cavity with 10 mm diameter and 2 cm length to mimic the ear canal. The sound input of the system is provided through the ER3 earphone where the earphone is plugged to the designated cavity. The PZT sensor on the membrane converts the sound vibration into electrical signals, which are sensed by the 2nd generation FICI interface electronics. The FICI interface generates biphasic neural stimulation currents to stimulate the auditory neurons of the guinea pig through the intra-cochlear electrodes. The stimulation response is observed by the ABR measurements via the optical amplifier and the Universal Smart Box.

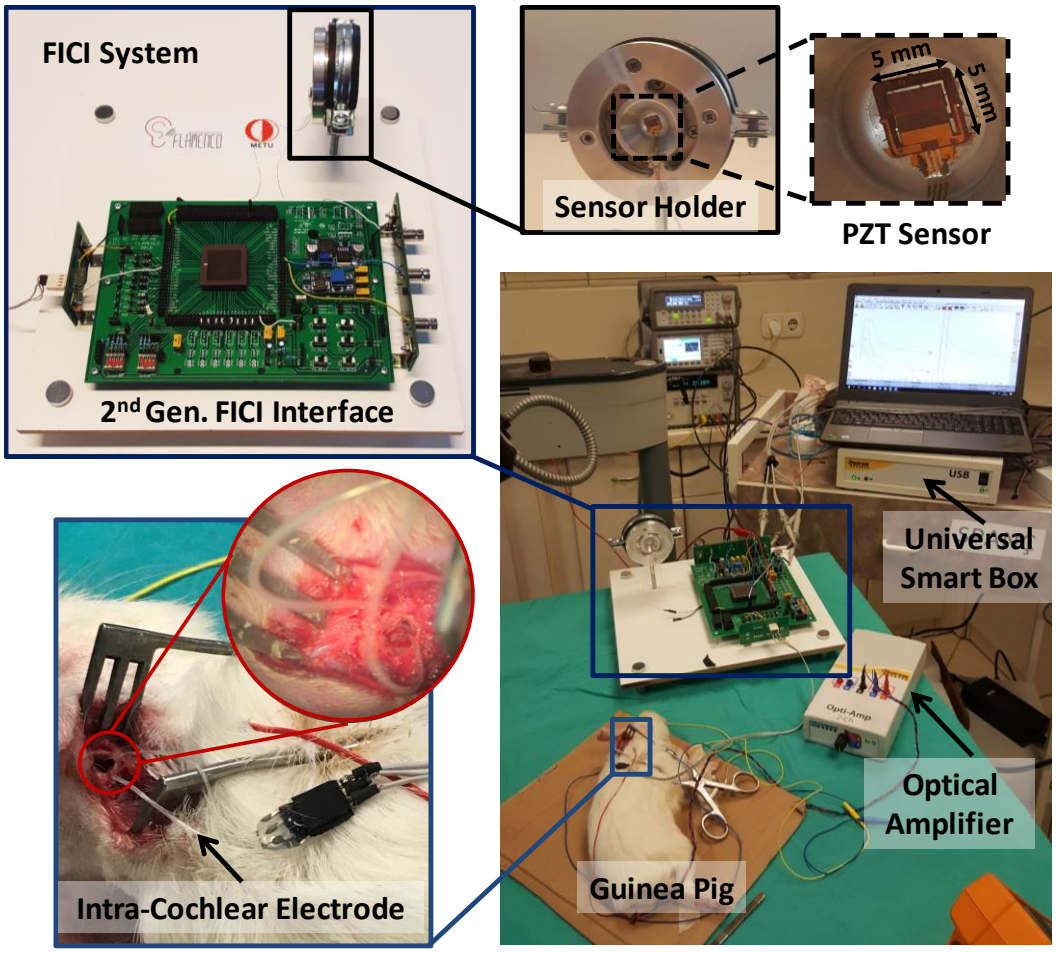


Figure 4.15. FICI system under the in-vivo tests.

Figure 4.16 presents the measurement results of the eABR tests with the FICI interface electronics. The tests are conducted with 1 kHz acoustical sound, which is the resonance frequency of the PZT sensor as shown in Figure 4.17. The system was first operated with 100 dB SPL, which was then gradually decreased to find the hearing threshold of the guinea pig. The obtained waveforms from the eABR with FICI system measurements are similar with the eABR with controlled current source presented in previous section. Reducing the sound level leads to reduction at the ABR of the guinea pig. For 50 dB sound input the ABR measurement does not provide a peak. Therefore, the hearing threshold of the system is around 55 dB. The input dynamic range of system is 45 dB which is 20 dB larger than previously reported FICI system with intra-cochlear stimulation [50]. In order to observe the frequency selectivity of the FICI

system the PZT sensor was also excited with 3 kHz acoustic sound and the eABR measurements were obtained as shown in Figure 4.18. The obtained eABR measurements for 90, 95 and 100 dB at 3 kHz stayed around the noise level, which shows that there were no brain response for these conditions.

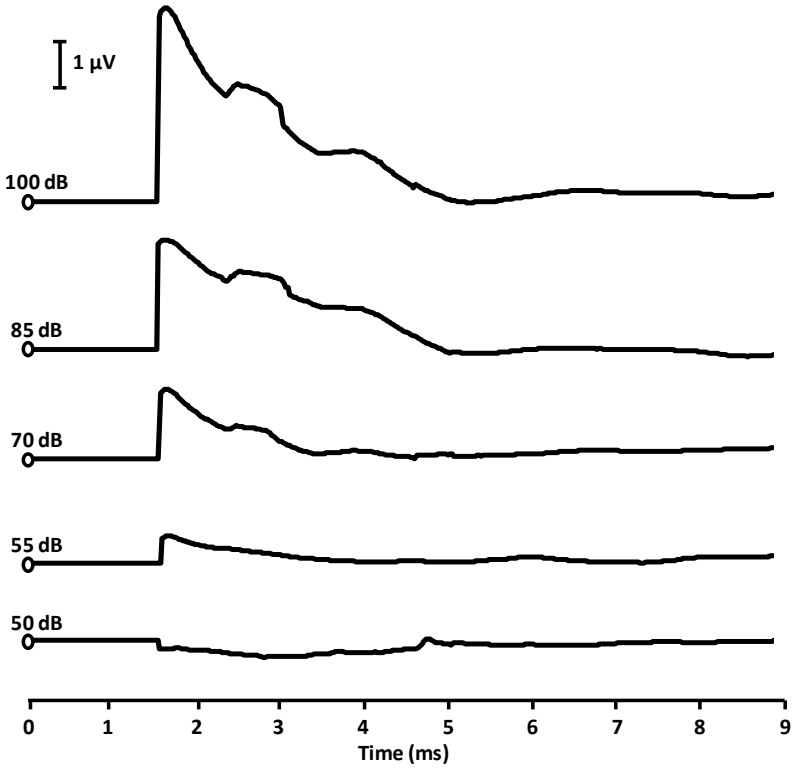


Figure 4.16. Measurement result of the eABR tests with the FICI interface electronics while the PZT sensor was excited by 1 kHz (resonance frequency) acoustic sound.

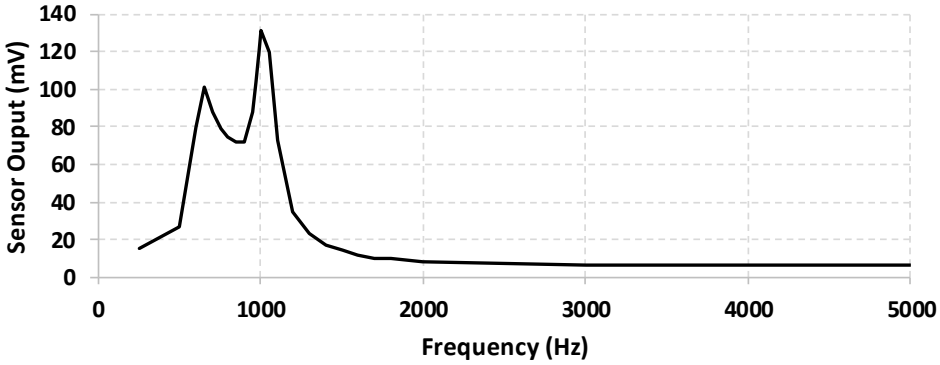


Figure 4.17. Frequency response of the PZT sensor on PDMS membrane at 95 dB SPL.

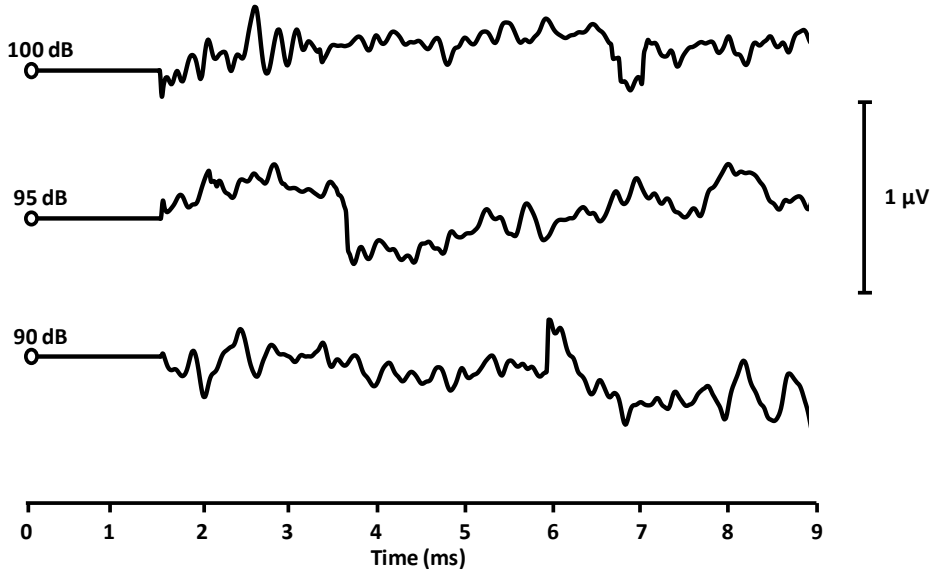


Figure 4.18. Measurement result of the eABR tests with the FICI interface electronics while the PZT sensor was excited by 3 kHz (an off-resonance frequency) acoustic sound.

To sum up, the proposed 2nd generation FICI interface electronics is combined with a low volume PZT sensor and neural stimulation performance of the system is tested by utilizing intra-cochlear electrodes placed inside the scala tympani. Before conducting the in-vivo tests the normal and deafened hearing performance of the guinea pig is observed with ABR and DPOAE measurements. Then, electrical stimulation of the auditory neurons of the guinea pig was tested by the measurements of eABR with controlled current source. Finally, the eABR tests with the FICI system was conducted. The results showed that the proposed system is able to electrically stimulate the auditory neurons for input sound levels above 55 dB and has a dynamic range of about 45 dB. The proposed interface electronics is the first FICI system validated with in-vivo tests, while operating with ultra-low power an wide input dynamic range.

CHAPTER 5

CONCLUSION AND FUTURE WORK

In the scope of this Ph.D thesis, an ultra-low powered Fully Implantable Cochlear Implant (FICI) interface electronics design has been suggested. The interface electronics was first concentrate on the low power sensor front-end at 1st generation interface. The validated system performance is then improved with novel current mode circuits. The 2nd generation interface also reduced the neural stimulator power by optimized current waveforms that enables to reach the lowest power dissipation in literature. The neural stimulation performance of 2nd generation FICI interface electronics was validated with in-vivo tests which is conducted for the first time in literature with such a low power and wide dynamic range operation (to the best of authors knowledge). The research can be divided into three frameworks: *i)* The 1st generation FICI interface electronics, *ii)* The 2nd generation FICI interface electronics with sub-500 μW power dissipation and *iii)* In-vivo tests of the FICI interface electronics on guinea pig. Design and specifications of each generation were extensively explained in the referred chapters. The performance of implemented interface electronics are validated through low-volume custom MEMS PZT sensors and with electrical signals that mimics the speech waveform. The in-vivo tests of the FICI system on a guinea-pig validate feasibility of the system as a next generation neural prosthesis. This chapter highlights the overview and major achievements of each frameworks of the research. Finally, further improvements that can improve the research are suggested as future work.

5.1. Summary of Contributions

The 1st generation FICI interface electronics is designed to sense the PZT sensors output with ultra-low power front-end signal conditioning circuit and generate biphasic rectangular current pulses to stimulate auditory neurons according to sound level. The major achievements according to previously reported specifications are as follow:

- Power dissipation of the implantable devices is one of the most critical issue to be considered during the design, therefore the proposed system focused on power reduction at the front-end signal conditioning circuit by operating at analog domain.

- The power dissipation of the system is further decreased by combining the amplifier and compression stages at the logarithmic amplifier at the first stage of the system. Moreover, the logarithmic amplifier at each stage are only enabled when corresponding channel is activated to prevent extra power dissipation of the system

- The low volume middle ear PZT sensors provide low electrical signals at the output, the 1st generation FICI interface electronics is designed to have low input referred noise (< 10 μV) that finely captures the sensor outputs.

- The 1st generation FICI interface electronics was tested with custom low volume MEMS PLD PZT acoustic sensor and operation of the system is validated for the input sound range of 60-100 dB SPL. The interface is able to provide biphasic neural stimulation current from 110 μA to 430 μA which are the threshold and maximum comfort levels of the system, respectively.

- The 8-channel front-end signal conditioning and the FICI interface electronics dissipates 51.2 μW and 691.2 μW, respectively, that enables

one of the lowest power for FICI system with rectangular biphasic situation current.

The 2nd generation FICI interface electronics has a novel design, which predominantly operates at current domain to reduce the power dissipation of the system. The proposed system has superior performance compared to previous generation where the achieved contributions are provided as follow:

- Although the 1st generation FICI interface electronics highly optimizes the front-end signal conditioning circuit the most power hungry part of FICI systems are the neural stimulation circuits which occupies more than 90% of the total power. Therefore, the 2nd generation FICI system focuses on optimization of overall block power. For the front-end signal conditioning design, the system predominantly operated in current domain to reduce the power dissipation where the designed system operates with 19.7 μW, which is lower than half of the previous design power and provides the lowest value in literature.

- The high power dissipation of neural stimulation circuit is mainly due to the high voltage requirement of rectangular biphasic current pulses, however in the proposed system the neural stimulation waveforms were optimized to reduce the electrode voltages. The optimized exponential waveform shape enables 20% supply voltage hence the system power reduction. The total power dissipation of the 2nd generation FICI interface electronics at 8-channel operation is around 472 μW, which is the lowest value in the literature to the best of authors knowledge.

- The power dissipation is one of the most critical parameter for the design but input dynamic range and the patient fitting compatibility are also critical for FICI systems. The proposed system provides up to 60 dB input dynamic range that cover the whole daily sound ranges from 40 dB SPL

(in a quite library) to 100 dB SPL (helicopter noise). For the patient fitting, the stimulation current generator circuit is designed to control the current level through 7-bit digital switches which enables to change the stimulation current between 0 to 1 mA (minimum threshold and maximum comfort levels).

- The performance of 2nd generation FICI interface electronics is also validated with a mimicked speech signal to demonstrate the proof-of-concept operation. The circuit is the first sub-500 μW FICI system in literature that enables more than 30 years operation lifetime with a typical implantable battery with limited capacity.

After the electrical tests of the 2nd generation FICI interface electronics completed the neural stimulation performance of the circuit is validated with in-vivo tests on a guinea pig. The achievements through these tests are as follow:

- As the first, hearing performance of the guinea pig was tested through ABR and DPOAE measurements. The minimum hearing threshold level the guinea pig was measured through the ABR tests for both ears. The DPOAE tests provided the functionality of the outer hair cells at the cochlea. Then the guinea pig was partially deafened through surgery and the functionality loss of hair cells was observed with a new DPOAE measurements for comparison.

- The auditory neurons of partially deafened guinea pig was stimulated with controlled current source and eABR measurements were conducted to validate that the neurons can be electrical evoked. The results showed that the auditory neurons can be stimulated from the promontory with 500 μA peak current as a threshold. For higher currents the eABR waveforms shows monotonic increment as expected.

- After validating electrical stimulation of the auditory neurons the intra-cochlear stimulation of the neurons were tested through the 2nd generation FICI interface electronics. The FICI interface was driven with a low volume MEMS PZT sensor that detect the acoustic sound input of the system. The minimum hearing threshold of the FICI system was determined as 55 dB where the input dynamic range of neural stimulation system is 45 dB (55-100 dB). The obtained eABR waveforms show a similar trend with the one observed at the controlled current source.

- At a glance, the 2nd generation FICI interface electronics is the first implantable system that is validated through in-vivo tests while operating with ultra-low power dissipation and wide input dynamic range.

5.2. Future Work

Despite the presented research in this thesis is comparable with state-of-the-art, there are many opportunities to improve the system for future work. Some of these studies are discussed as follow:

- The in-vivo tests of the FICI interface electronics provides promising results for the implantation of the system as a biomedical device, however an efficient on-chip power management circuit is required to provide low and high voltage supplies of the circuit.

- The 8-channel performance of the system is tested with electrical input signals, whereas acoustic sensor interface of the system is tested with single channel operation. The 8-channel performance of the FICI system will be tested with properly designed 8 PZT sensors in the speech band. Furthermore, the channel number of the system will be increased to increase the speech perception, but the trade-off between the power dissipation must be taken into consideration.

- The proposed interface electronics are designed to provide amplitude modulated stimulation current generation according to input sound level, a pulse width modulated stimulation current will be tested to keep the stimulation current at low level and reduce the power of the system. While increasing the pulse width the stimulation frequency has to be lowered which is also effective on the speech perception.

- In the designed system, the stimulation electrodes are fired according to CIS stimulation strategy that minimize the interference between channels. An asynchronous stimulation strategy will be applied to the system such as only 4 of 8 channels that have maximum inputs can be activated for stimulation. By this way, overall power dissipation of the system will be further reduced.

- The implemented design utilizes electrode shorting technique for residual charge balancing at the electrodes, which will have problems due to uncontrolled short circuit currents. A more controllable on-chip charge balancing technique can be added to the system.

- The ultra-low power dissipation of the presented study leads to increase life time of the implantable devices. Another option to prolong life time of the system is to import energy harvesting [94]–[96] as a sustainable source.

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PUBLICATIONS

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