HYSTERESIS BAND CONTROL OF HYBRID ACTIVE POWER FILTER:
AN APPLICATION TO A MEDIUM-FREQUENCY INDUCTION MELTING
FURNACE

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ABSTRACT

HYSTERESIS BAND CONTROL OF HYBRID ACTIVE POWER FILTER: AN APPLICATION TO A MEDIUM-FREQUENCY INDUCTION MELTING FURNACE

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In order to prevent the harmful effects of Medium-Frequency Induction Melting Furnaces to the grid they are connected, it is very important to keep the unintended current harmonics generated by them within allowed limits. Since Medium-Frequency Induction Melting Furnace load contains variety of harmonics and interharmonics in a wide range, a flexible solution with no parallel resonance risk should be implemented. A Hybrid Active Power Filter is the most suitable solution for such a case. In this research work, hysteresis band control algorithm is proposed and implemented to control the hybrid active power filter. Moreover, some challenging design issues are investigated; such as, adaptive hysteresis band design, proposal of novel performance evaluation criterion, implementation of hierarchical control system architecture and the comparison of hysteresis band control with traditional methods. In addition to these design issues, the whole system is simulated and put into practice at field so that the experimental results could be compared with the theoretical ones. The experimental results prove that the proposed Hybrid Active Power Filter system effectively suppresses the most dominant harmonics and interharmonics of Induction Melting Furnace load.

Keywords: HAPF, Hysteresis Current Control, IMF, Interharmonics, Power Quality

ÖZ

HİSTERESİZ-BANT KONTROLLÜ MELEZ ETKİN GÜÇ SÜZGECİ: ORTA-FREKANS ENDÜKSİYON ERGİTME OCAĞI UYGULAMASI

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Şebekeye bağlı Orta-Frekans Endüksiyon Ergitme Ocaklarının zararlı etkilerini önlemek için üretmiş oldukları istenmeyen akım harmoniklerini standartlarda önerilen seviyeye indirmek büyük önem taşır. Orta-Frekans Endüksiyon Ergitme Ocağı yükü geniş bir bantta harmonik ve ara-harmonik içerdiği için paralel rezonans yaratmayacak esnek bir çözüm üretilmesi gerekmektedir. En uygun çözüm Melez Etkin Güç Süzgecidir. Bu araştırma çalışmasında, Melez Etkin Güç Süzgecini kontrol etmek için histeresiz-bant kontrol algoritması önerilmiş, modellenmiş ve uygulanmıştır. Ayrıca, uyarlanabilir histeresiz bandı tasarımı, yeni performans değerlendirme kriteri önerisi, hiyerarşik control sistemi mimarisi uygulanması ve önerilen metodun geleneksel metotlarla karşılaştırılması gibi önemli konularda araştırma yapılmıştır. Bu konuların yanında, sistemin bütün olarak benzetim çalışmaları yapılmış ve sonrasında sahada uygulanmıştır; böylelikle teorik verilerle pratikte alınan sonuçlar karşılaştırılmıştır. Saha verileri değerlendirildiğinde önerilen histeresiz-band kontrollü Melez Etkin Güç Süzgeci'nin Orta-Frekans Endüksiyon Ergitme Ocağı yükünün baskın harmonik ve ara-harmoniklerini etkili bir biçimde süzdüğü belirlenmiştir.

Anahtar Kelimeler: Endüksiyon Ergitme Ocağı, Güç Kalitesi, Harmonik ve Ara-harmonikler, Histeresiz-Band Kontrol, Melez Etkin Güç Süzgeci.

To My Wife

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
APF	Active Power Filter
BPF	Band Pass Filter
CB	Circuit Breaker
CPLD	Complex Programmable Logic Device
CSC	Current Sourced Converter
DF	Distortion Factor
DFT	Discrete Fourier Transform
DI	Digital Interface Board
DSP	Digital Signal Processor
DTM	DC Link and Temperature Measure Board
DVR	Dynamic Voltage Restorer
EAF	Electric Arc Furnace
FACTS	Flexible AC Transmission System
FB	Firing Board
FFT	Fast Fourier Transform
FLC	Fuzzy Logic Control
FPGA	Field Programmable Gate Array
GTO	Gate Turn-Off Thyristor
HAPF	Hybrid Active Power Filter
HBC	Hysteresis Band Control
HMI	Human Machine Interface
HPF	High Pass Filter
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IMF	Induction Melting Furnace
IP	Internet Protocol

KVL	Kirchoff's Voltage Law
LPF	Low Pass Filter
LV	Low Voltage
MV	Medium Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NTC	Negative Temperature Coefficient
PCC	Point of Common Coupling
PEBB	Power Electronics Building Blocks
PI	Proportional Integral
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
PQ	Power Quality
PWM	Pulse Width Modulation
RMS	Root Mean Square
SB	Supply Board
SF	Suppression Factor
SHEx	Selective Harmonic Extractions
SMPS	Switch Mode Power Supply
SRF	Synchronous Reference Frame
STATCOM	Static Compensator
SVC	Static VAR Compensator
TCP	Transmission Control Protocol
TDD	Total Demand Distortion
TDM	Time Division Multiplexing
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioner
UPS	Uninterruptable Power Supply
VCM	Voltage and Current Measure Board
WCS	Water Cooling System
VSC	Voltage Sourced Converter

CHAPTER 1

INTRODUCTION

Following the great advancements in semiconductor physics and power electronics, non-linear loads have become widely used more than ever in industry. Excessive use of those non-linear loads significantly deteriorates the quality of the electrical power supplied via transmission and distribution systems. Power Quality (PQ) is defined as the perfection of delivered electrical power in terms of wave shape, frequency, amplitude, and sustainability [1]-[3]. Current and voltage waveforms of an ideal electrical grid should be in forms of perfect sinusoidal wave in-phase to each other having constant frequency and defined constant magnitude [1]-[3]. In addition to their quantifiable parameters, the sustainability is also an important factor for PQ analysis of an electrical grid [1]-[3]. Voltage and frequency transients, reactive power, short duration voltage sag and swells [4], long duration over- and under-voltages, voltage imbalances, DC offsets in voltage and current waveforms, voltage and current harmonics, interharmonics, notching, high frequency noises, and flickers are the most widely known PQ problems [2], [3].

Flexible AC Transmission System (FACTS) devices had been introduced to overcome some of the PQ problems at fundamental frequency by making use of power electronics converters to form a transmission system allowing an enhanced controllability and increased power transfer capability [3], [5]-[8]. Static Compensators (STATCOM) [9]-[11], and Static VAR Compensators (SVC) [12], [13] are well known FACTS devices providing reactive power compensation, voltage regulation and flicker mitigation [3]. Moreover, vulnerable industrial loads can be protected from the short duration voltage sag and swells via specialized power electronics converters [3] such as Dynamic Voltage Restorer (DVR) [14]-[16]. In

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addition to those PQ problems, harmonics and interharmonics, as the main subject of this research work, can be suppressed by various systems including passive and active solutions. In the following sections of this chapter, harmonics, interharmonics, their harmful effects, and an Induction Melting Furnace (IMF) load, one of the most problematic loads in terms of current harmonics [17]-[22], are described.

1.1.   Definition of Harmonics and Harmonic Problems

Harmonics, as defined in IEEE guide for harmonic control in electrical power systems [1], are sinusoidal components of a periodical quantity having frequency components which are integer multiples of the fundamental frequency of that periodical quantity. They are generated by various sources such as power electronic converters, saturated electromagnetic equipment and other non-linear loads [23], [24]. Especially with the increased integration of power electronic converters to the power system, harmonics have become an important subject for the power system [23], [24]. Controlled electrical machines, Switch Mode Power Supplies (SMPS), three- and single-phase bridge rectifiers, pulse-width modulated inverters, and static compensators are some examples of the power electronics devices which are serious harmonic sources [23]. Those harmonics generated by the normal operation of semiconductor converters are defined as the characteristic harmonics, and their frequencies are generally in a form given in (1.1) [1].

$$h = kq \pm 1 \qquad\qquad (1.1)$$

,where h is the harmonic order, k is any integer, and q is the pulse number of the power electronics converter. For example, 5th, 7th, 11th, 13th, … are the characteristic harmonics of a six-pulse converter.

On the other hand, induction and synchronous machines, metal melting and shaping furnaces, power transformers, cycloconverters, and some pulse burst heaters are the examples of other industrial nonlinear loads that may generate harmonics [23]. Unlike characteristic harmonics, non-characteristic harmonics are caused by asymmetrical

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delay angles, imbalance in the ac power system, or demodulation of characteristic harmonics and classified as the non-characteristic harmonics [1].

Those characteristic and non-characteristic harmonics causes some serious problems in the power system [24], [25]. Some of the harmful effects of harmonics are listed as follows [24], [25]:

  i.   Excessive losses and temperature rise in transformers, transmission lines and electrical machines.

  ii.   Capacitor bank and cable failures due to dielectric breakdown,

  iii.   Misoperation of protection relays, malfunctioning of switching elements and various power meters,

  iv.   Electromagnetic interference to communication lines,

  v.   Mechanical oscillations and torque ripples in rotating electrical machinery,

  vi.   Over-voltages and unintended resonances in power system.

Severity of those effects depends on the type of harmonic source, its location in the power system, and the characteristics of the transmission/distribution network.

In order to illustrate the generation of harmonics, a three phase diode bridge rectifier, widely used in Uninterruptable Power Supplies (UPS) and various motor drives, has been simulated. The simulation results are given in Figure 1.1. As can be seen from Figure 1.1.a, line current waveforms of each phase are highly distorted, which causes a harmonic spectrum as given in Figure 1.1.b. Since the current waveforms have quarter wave symmetry, there are no even order harmonics can be observed from Figure 1.1.b. In addition, harmonics which are integer multiple of three do not exist due to the three phase converter topology.

Harmonic content of a periodical waveform can be described with the help of some measures such as Distortion Factor (DF), Total Harmonic Distortion (THD), and Total Demand Distortion (TDD) [1]. DF is defined as the ratio of Root-Mean-Square (RMS)

of the harmonic content to RMS fundamental content in percentage representation (1.2), THD is the definition of DF when the quantities are current or voltage (1.3, 1.4), and TDD as the ratio of RMS harmonic current distortion to the maximum demand load current (1.5).
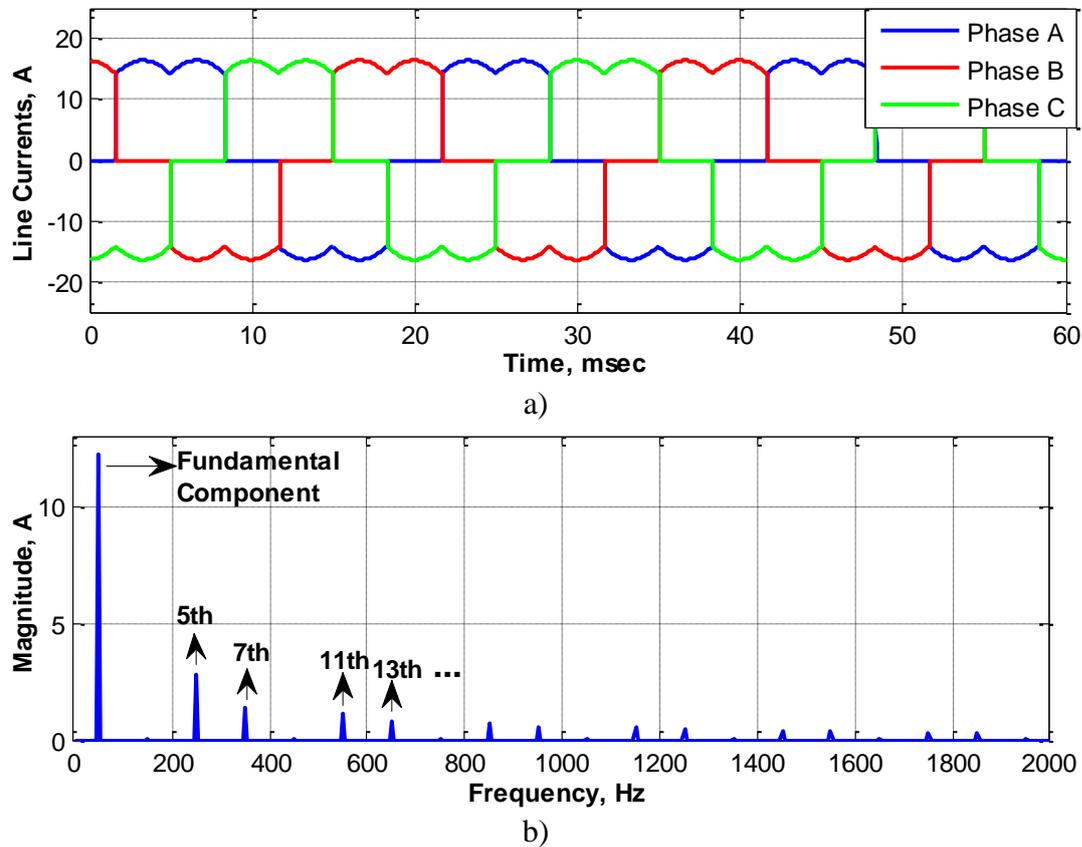
Figure 1.1 Simulation results of three phase diode bridge rectifier, a) line current waveforms and b) harmonic spectrum of line current of phase A

$$DF = \sqrt{\frac{Sum\,of\,squares\,of\,all\,harmonics}{Square\,of\,amplitude\,of\,fundamental}}\,x100\% \qquad (1.2)$$

$$THD\,(current) = \sqrt{\frac{I_{RMS}^2 - I_F^2}{I_F^2}}\,x100\% \qquad (1.3)$$

$$THD\,(voltage) = \sqrt{\frac{E_{RMS}^2 - E_F^2}{E_F^2}}\,x100\% \qquad (1.4)$$

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$$TDD = \frac{\sqrt{I_{RMS}^2 - I_F^2}}{I_{MAX\_DEMAND}} \, x100\% \qquad (1.5)$$

Each individual harmonic voltage and current has allowed limits determined by the regulatory authorities of each country and international standards [1]. Allowed limits for individual voltage harmonics and total voltage distortion as suggested in [1] are given in Table 1.1. Similarly, allowed limits for individual current harmonics and THD as suggested in [1] are given in Table 1.2.

Table 1.1 Allowed limits for individual voltage harmonics and total distortion

Bus voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5

Table 1.2 Allowed limits for individual current harmonics and total distortion

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed						
* All power generation equipment is limited to these values of current distortion, regardless of actual I_{SC}/I_L.						
Where, I_{SC} = maximum short-circuit current at Point of Common Coupling (PCC). I_L = maximum demand load current (fundamental frequency component) at PCC.						

Characteristic and non-characteristic harmonics, appeared in the power system, can be analyzed in terms of positive-, negative- and zero-sequence symmetrical components too [19], [26]. Positive-, negative- and zero-sequence characteristic and non-characteristic harmonics are listed in Table 1.3. However, those symmetrical component representations are only valid for power system elements that their current is synthesized by the fundamental frequency grid voltage such as rotating electrical machines, power transformers, basic n-pulse power electronics converters, and line commutated converters. However, this is not the case for some other industrial loads generating non-integer multiples of harmonics [20], [22], [27].

Table 1.3 Symmetrical components of characteristic and non-characteristic harmonics

3 Phase Sinusoidal Current Systems	Characteristic Harmonics	Non-characteristic Harmonics
Positive-Sequence	1st, 7th, 13th, 19th, …	4th, 10th, 16th, 22nd, …
Negative-Sequence	5th, 11th, 17th, 23rd, …	2nd, 8th, 14th, 20th, …
Zero-Sequence	3rd, 9th, 15th, 21st, …	6th, 12th, 18th, 24th, …

1.1.1. Definition of Interharmonics and Interharmonic Sources

Interharmonics are defined as the frequency component of a periodic quantity that is not an integer multiple of the fundamental frequency of the supply system [28]. In other words, interharmonics cover a wide range of frequencies in the frequency spectrum other than the integer multiples of the fundamental frequency [29]. Interharmonics have similar harmful effects on the power system as harmonics; in addition, they cause some other problems due to their uncharacteristic frequencies. [20]. Interharmonic frequencies have potential to interact with passive shunt reactive power compensation systems resulting in amplification of some interharmonic frequencies instead of suppressing them [17]. Amplified interharmonics have destructive effects on those reactive power compensation equipment [27].

The majority of interharmonics are generated by the converters making use of two AC systems running at different frequencies, if they are fed from common dc link [19]-[22], [29]. This phenomenon is named as cross-modulation phenomenon [17], [19], [20] and the mathematical expression of it is given in the following sections of this chapter.

Table 1.4 Voltage interharmonic limits based on flicker for PCC voltage less than 1kV

Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)
16	5.00	27	1.78	38	0.81	49	0.28
17	4.50	28	1.64	39	0.78	50	0.25
18	3.90	29	1.54	40	0.71	51	0.23
19	3.45	30	1.43	41	0.64	52	0.25
20	3.00	31	1.33	42	0.57	53	0.27
21	2.77	32	1.26	43	0.50	54	0.29
22	2.53	33	1.20	44	0.48	55	0.35
23	2.30	34	1.13	45	0.43	56	0.4
24	2.15	35	1.05	46	0.38	57	0.58
25	2.03	36	0.95	47	0.34	58	0.77
26	1.90	37	0.85	48	0.31	59	0.95

The most common interharmonic sources are double conversion systems such as cycloconverters, High Voltage Direct Current (HVDC) converters, variable speed AC motor drives, and the metal shaping and melting systems like ladle furnaces, Electric Arc Furnaces (EAF), and IMFs. [19], [20], [22], [29]. Although, interharmonics are as harmful as harmonics to the power system, there is not, unfortunately, any regulation regarding interharmonics yet. However, the last version of the IEEE standard for harmonic power has defined the interharmonics and proposed some suggestions of the voltage interharmonics of EAF loads for the prevention of flicker only [28]. Those voltage interharmonic limits, determined for 60-Hz fundamental frequency grid for voltage level 1kV or less, are as given in Table 1.4. Allowed limits

for the interharmonic frequencies from 61 to 104 Hz are identical to those given in Table 1.4 except the frequency of interest must be subtracted from 120 before reading the corresponding value [28]. It is suggested in this thesis that some regulations for the interharmonics, caused by usual operation of various industrial loads, should also be integrated to standards.

1.2.   Harmonic Suppression Techniques

Suppression of harmonic and interharmonic problems described in the previous section is essential for power system. Indeed, allowed limits for voltage and current harmonics has already been defined in various standards [1], [28] and Turkish grid code [30]. Harmonic suppression systems, in other words filters, can be divided into two categories namely passive filters and Active Power Filters (APF). The most common, easy to implement, cheap and conventional solutions to harmonic problems are passive filters. However, they have some disadvantages, some of which are listed as follows:

- Passive filters may cause resonance with the other passive loads,
- Their performance is strongly dependent on the grid voltage and impedance conditions,
- They have a fixed reactive power compensation characteristics,
- Upgrading of a passive filter or changing of its filtering characteristics are very hard.

As the power electronics converter technologies have been advancing rapidly, severity of harmonic problems, their features and transient behaviors have also been changed. To meet the challenging requirements of harmonic loads and overcoming the disadvantages of conventional passive filter solutions, active filtering systems have become widely used recently with the advancements in semiconductor industry. In this section of the thesis, different passive filter topologies and their characteristics are

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introduced then active filtering systems, their topologies, classification and comparison are mentioned in detail.

1.2.1. Passive Filters

Passive filters composed of reactor, capacitor and resistor are widely used for the suppression of power system harmonics due to the fact that they are cheap and easy to implement. Passive filters can be implemented to the power system in series or shunt circuit topologies. Series passive filters behave as high impedances for the frequencies intended to be blocked, and low impedances for the rest of the frequencies. Shunt passive filters, on the other hand, behave as a low impedance path to the ground for the harmonic frequencies intended to be filtered out, and high impedance path for the rest of the frequencies. By this way unwanted harmonic currents flow towards passive filter instead of grid side. It should be noted that shunt passive filters subject to currents that are intended to be filtered out; however, series passive filters subject to all of the load current. For this reason, only shunt passive filters are used for the grid connected harmonic filtering applications. Shunt passive filters also provide reactive power to the grid.

The most common conventional shunt passive filter topologies used for utility grid applications are single-tuned 2nd order undamped, 2nd order damped, and 2nd order C-type as given respectively in Figure 1.2.a, b, and c. C-type shunt passive filters, illustrated in Figure 1.2.c, are specially designed to reduce the losses in damping resistor [31] and they are used in lots of industry applications such as metal industry [32], HVDC systems [33] and railway [34]. 2nd order damped filter, illustrated in Figure 1.2.b, is also one of the commonly used passive filter topologies for various industry applications [35]-[37] and this topology is the improved version of single-tuned 2nd order undamped filter topology [38] in terms of parallel resonance problem. However, it has very little impact on high order harmonics [37]; for this reason, this topology is also called as 2nd order High Pass Filter (HPF) in the literature [35]-[37].
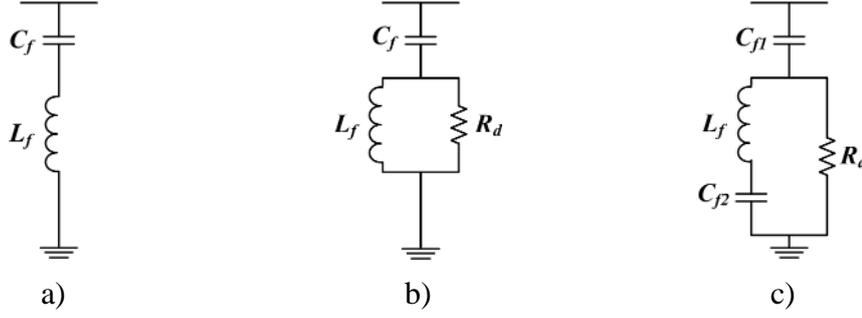
Figure 1.2 Conventional passive filter topologies: a) single-tuned 2nd order undamped, b) 2nd order damped, and c) 2nd order C-type

Single-tuned 2nd order undamped passive filter topology, illustrated in Figure 1.2.a, shows a typical Band Pass Filter (BPF) characteristics and is the most commonly used passive filter topology due to their simplicity in design. This passive filter behaves as low impedance path around the designed tuning frequency and high impedance path for rest of the frequencies, which makes it a typical BPF. However, its characteristics and thus the performance change with the changing utility grid conditions. Moreover, single-tuned passive filter topology causes a parallel resonance with the grid impedance and it amplifies some frequency components a bit lower than tuning frequency. The impedance of the single-tuned 2nd order passive filter topology is as given in (1.6).

$$Z_{filter} = R_{filter} + j\left[wL_{filter} - \frac{1}{wC_{filter}} \right] \tag{1.6}$$

As can be deduced from (1.6) that the lowest filter impedance occurs when imaginary part of the expression is zero. This situation occurs for a specific frequency value and this frequency is defined as the tuning frequency. Tuning frequency, f_o, can be expressed as in (1.7) with respect to filter inductance, L_{filter}, and capacitance, C_{filter}.

$$f_o = \frac{1}{2\pi\sqrt{L_{filter}C_{filter}}} \tag{1.7}$$

Since single-tuned passive filter is a reactive power source at the fundamental frequency, the required amount of reactive power should also be designed thoroughly.

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The reactive power support, $kVAR_{filter}$, of single-tuned harmonic filter can be calculated as given in (1.8).

$$kVAR_{filter} = m\frac{V_{l-n}^2}{Z_{filter,fund}}$$ (1.8)

,where V_{l-n} is the line to neutral voltage of the bus, m is the number of phases, $Z_{filter,fund}$ is the filter impedance at fundamental frequency.

Another design parameter for single-tuned harmonic filter is the sharpness of the attenuation characteristics, which is also defined as quality factor, Q, of the filter and can be calculated by the equation (1.9). Although R_{filter} value given in this equation can be an external damping resistor connected in series with the filter, this value is chosen as the internal resistance of the series inductor for the undamped filter topologies in order to reduce the losses on the external damping resistor.

$$Q = \frac{1}{R_{filter}}\sqrt{\frac{L_{filter}}{C_{filter}}}$$ (1.9)

One of the most important design considerations is that the tuning frequency should not be exactly the same as the harmonic frequency to be suppressed but a bit lower value of it. If the tuning frequency is exactly the same as one of the characteristic harmonic frequencies than the filter will behave as a short circuit path for that frequency resulting in possible excessive currents due to other harmonic sources in Point of Common Coupling (PCC).

It has already mentioned in this chapter that single-tuned passive filters cause parallel resonances due to their interaction with source impedance, L_s. The parallel resonance frequency can be expressed as given in (1.10) and appears at frequency a bit lower than the tuning frequency as can be deduced from (1.10) by using the tuning frequency equation (1.7). It is important that this parallel resonance frequency does not coincide with any other harmonic frequency, otherwise, those harmonics may be amplified.

$$f_{res} = \frac{1}{2\pi\sqrt{(L_{filter} + L_s)C_{filter}}}$$

(1.10)

In order to better observe the parallel resonance problem, load to source current transfer characteristics of a typical 5th harmonic single-tuned 2nd order passive shunt filter tuned to 240Hz is shown in Figure 1.3.
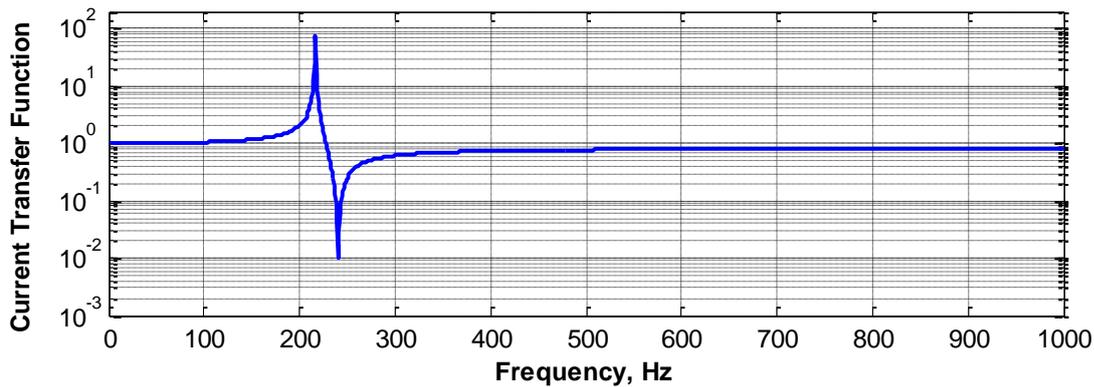
Figure 1.3 Single-tuned 2nd order undamped passive shunt 5th harmonic filter current transfer characteristics

1.2.2. Active Power Filters

Active harmonic filtering concept and APF operating principles were firstly introduced in early 1970s [39], [40] and improved rapidly in the following decades with the enhancements in power electronics area. Although, Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) and Gate Turn-Off Thyristors (GTOs) are used as semiconductor switches in the early works, researchers started preferring Insulated Gate Bipolar Transistors (IGBTs) due to their superior electrical features. Advancements on semiconductor physics, Digital Signal Processors (DSP), Field Programmable Gate Arrays (FPGA), common usage of hall-effect sensors and thus decreasing costs forced much more researchers to work on APF area for the mitigation of unwanted harmonics [41]-[45].

Basic operating principle of the APF is to measure the harmonic content causing distortion in the load side and to inject each individual harmonic to the utility grid with exactly the same magnitude as corresponding reference but anti-phase. By this way, the load side and corresponding filter side individual harmonics tend to cancel out each other, resulting in an undistorted waveform at the source side. To observe the APF operating principle, a basic illustration in Figure 1.4 is given. As can be seen from Figure 1.4, distorted current waveform drawn by nonlinear load is filtered out by the shunt APF modelled as a controlled current source resulting in a pure sinusoidal current waveform at the source side. It should be noted that this illustration is an ideal representation of APF operation; there is no need, in practice, for totally filtering out all the harmonics but mitigating them below allowed limits is enough as mentioned in earlier sections.

Compensating current or voltage waveforms are generated by Pulse Width Modulation (PWM) converters consisting a DC link energy storage element. The DC storage element can be inductor or capacitor depending on the employed converter topology. The DC link can be regulated at desired value by transferring active power from utility grid, there is no need for external DC source. However, this operation requires a small amount of current reference at fundamental frequency in order to sustain the DC link and compensate losses.
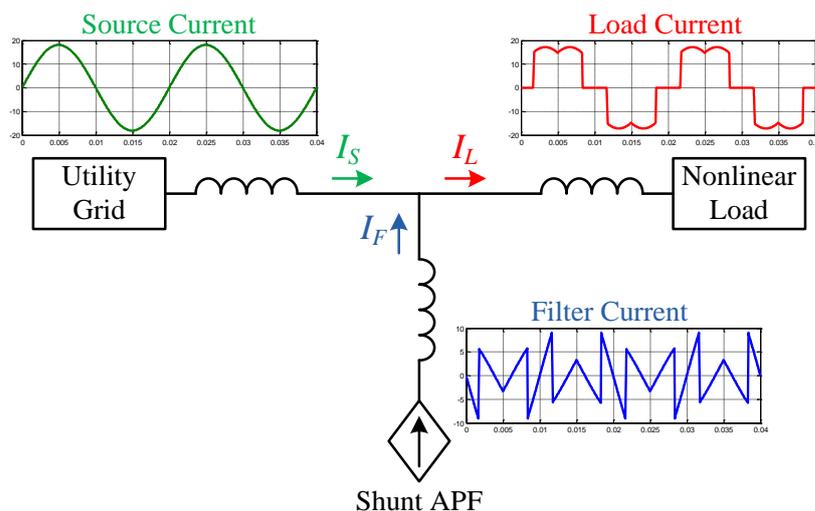
Figure 1.4 Basic operation principle of active filtering

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In addition to current or voltage harmonic suppression purposes, APFs can also be used for reactive power compensation, voltage regulation and load balancing depending on the requirements of the load.

1.2.2.1. Classification of APF

APFs can be classified into several types in terms of both their converter topologies and used system configurations. APF converters can be divided into two types in terms of their converter topologies namely Voltage Sourced Converter (VSC) and Current Sourced Converter (CSC).

VSC based APFs make use of voltages as their dc link and hence capacitors are used as the energy storage elements. VSC type converters condition the dc link voltage by using semiconductor switches in order to generate necessary voltage waveform on the converter terminals. By this way, those APFs are then able to inject corresponding reference currents or voltages into the grid depending on the system configuration. VSC based APFs should be coupled to the grid via a coupling inductor, which also helps filtering out the high frequency voltage ripples generated by the converter. Typical circuit diagram of the three-phase three-wire two-level VSC based APF topology and its grid connection are as illustrated in Figure 1.5.a and b, respectively.

a)   b)
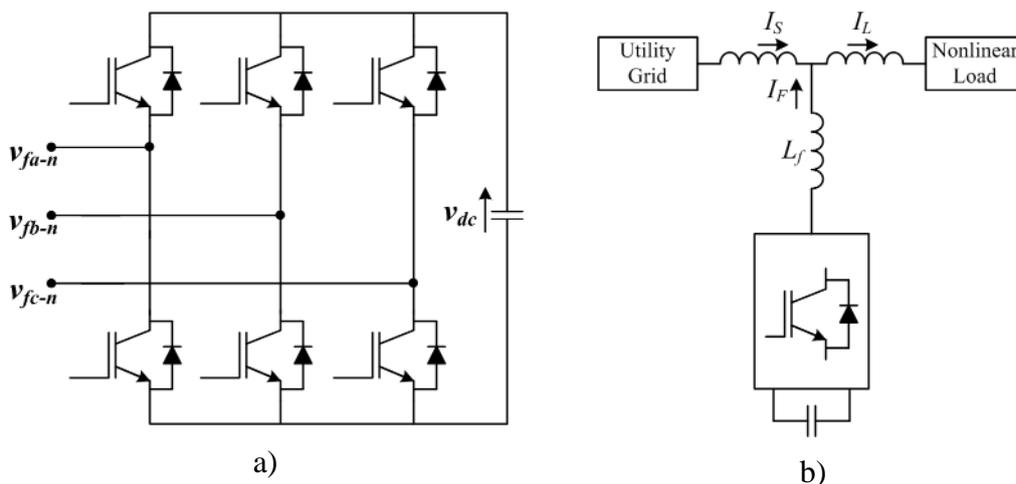
Figure 1.5 VSC type APF topology a) circuit diagram of three-phase three-wire two-level converter and b) system configuration

Although Figure 1.5 shows a three-phase three-wire circuit topology, VSC converters can be single-phase, three-phase four-wire or multilevel depending on the power system conditions, load characteristics and design requirements.

CSC based APFs, on the other hand, make use of currents as their dc link and hence inductors are used as the energy storage elements. CSC type converters condition the dc link current by using semiconductor switches in order to generate necessary current waveform on the converter terminals. By this way, those APFs are then able to inject corresponding reference currents or voltages into the grid depending on the system configuration. CSC type APFs require a filtering capacitor at the converter terminals in order to filter out high frequency current ripples generated by the converter. Similar to VSC type, CSC type APFs are also connected to the utility grid via coupling inductors. Typical circuit diagram of the three-phase three-wire two-level CSC based APF topology and its grid connection are as illustrated in Figure 1.6.a and b, respectively. Although Figure 1.6 shows a three-phase three-wire circuit topology, CSC converters can be single-phase, three-phase four-wire or multilevel depending on the power system conditions, load characteristics and design requirements.
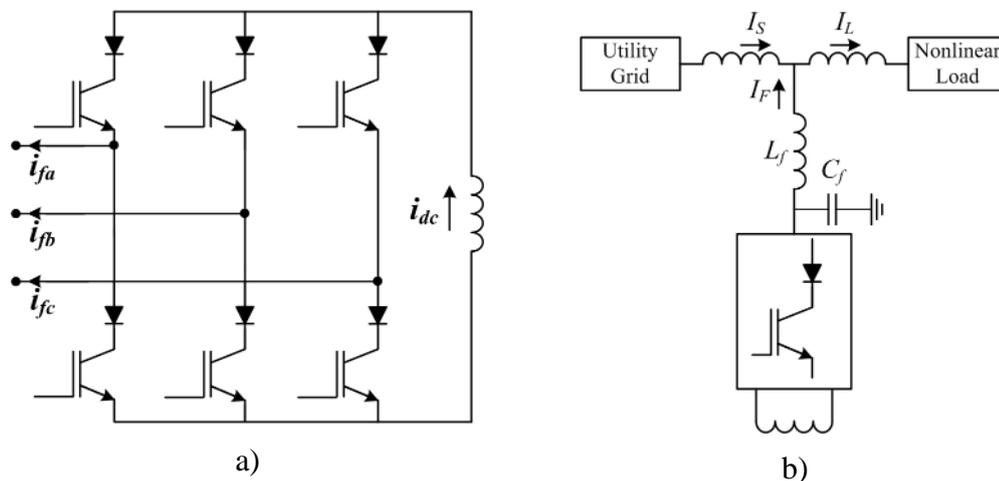
Figure 1.6 CSC type APF topology a) circuit diagram of three-phase three-wire two-level converter and b) system configuration

When available power ratings, allowed switching frequency, conduction and switching losses features are considered, using IGBTs as semiconductor switches for both VSC and CSC configurations seem to be the most advantageous solution as compared to GTOs or MOSFETs. It is important to note that the semiconductor switch connections are different from each other for VSC and CSC topologies. While VSC topology contains semiconductor switches with anti-parallel body diodes, semiconductor switches are connected in series with a diode for CSC topology. Commercially available IGBTs, that product ranges of the most famous manufacturers with respect to voltage and current ratings are illustrated in Figure 1.7, are generally sold together with anti-parallel body diode [46]-[50]. For this reason, there is a need for external series diode modules for CSC type converters, which brings extra cost and size for CSC type converters. Also, using inductors as dc link causes an increase in losses [51]. Despite those disadvantages, CSC topology has also some superiorities to VSC topology such as robust current controllability, high reliability and fast response. However, VSC type converters have become much more popular among researchers due to their small size, lower initial cost and higher efficiency.
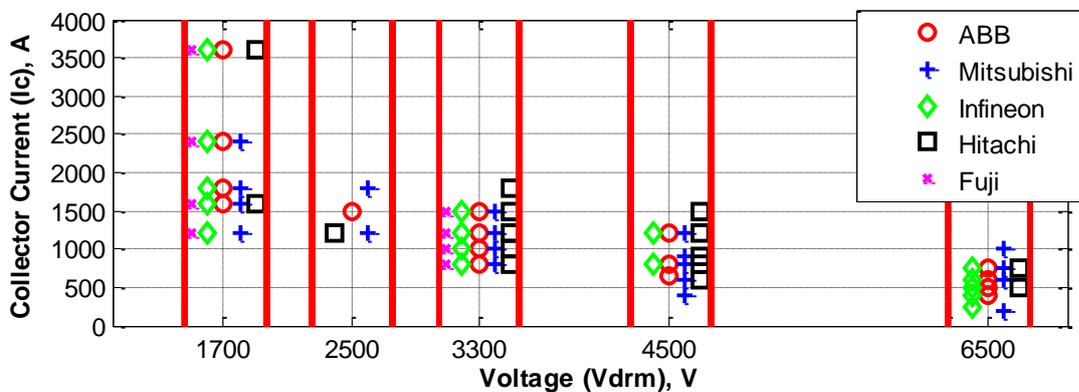
Figure 1.7 IGBT product lines of the most famous semiconductor manufacturers

APFs can also be divided into four types in terms of their system configurations namely shunt APF, series APF, Unified Power Quality Conditioner (UPQC) and Hybrid Active Power Filter (HAPF) [52], [53]. Shunt APFs generally are used for the

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mitigation of current harmonics and reactive power compensation [54], [55]. Figure 1.8 shows the representation of shunt APF and the operating principle is mentioned in previous section using illustration in Figure 1.4. The illustration shown in Figure 1.9 describes the topology of series APF. Series APFs are often used for suppressing the voltage harmonics and providing bus voltage regulation on source or load side [56]-[58]. It can be considered as the dual of shunt APF topology, and its basic operating principle is as illustrated in Figure 1.9. Series APF injects a voltage component, V_F, to the power system with a specially designed power transformer in a way that this voltage appears in series between source and load sides of the distribution bus. By this way, voltage harmonics can be prevented, and bus voltage can be regulated in either side of the transformer. A drawback of the series APF is that the series transformer is subjected to full load current resulting in an oversized transformer for power converter.
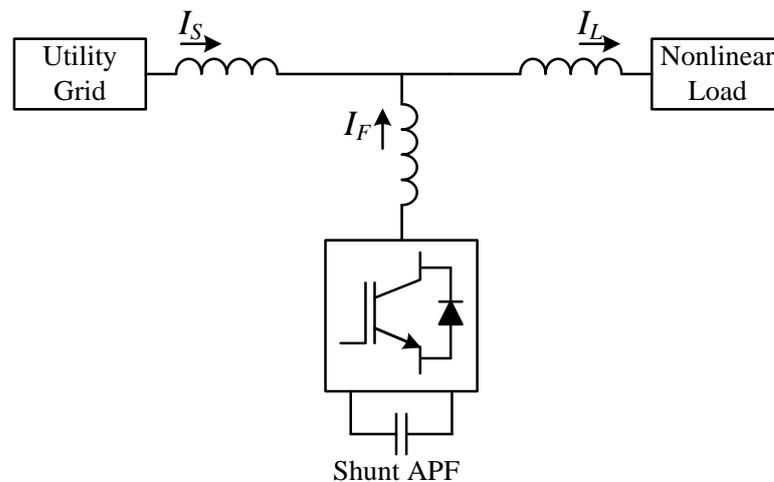
Figure 1.8 Shunt Active Power Filter

Another type of active filtering system is UPQC. UPQC is composed of a series and a shunt APF connected back-to-back with a common DC link as shown in Figure 1.10. This type of power conditioning system can manage voltage and current harmonic filtering, voltage regulation, and reactive power compensation [59]. Although, UPQC

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seems to be an ideal system solving all the capabilities of active filtering systems, it is not preferred by the researchers as much as series or shunt APFs due to its complex control mechanism and high initial cost.
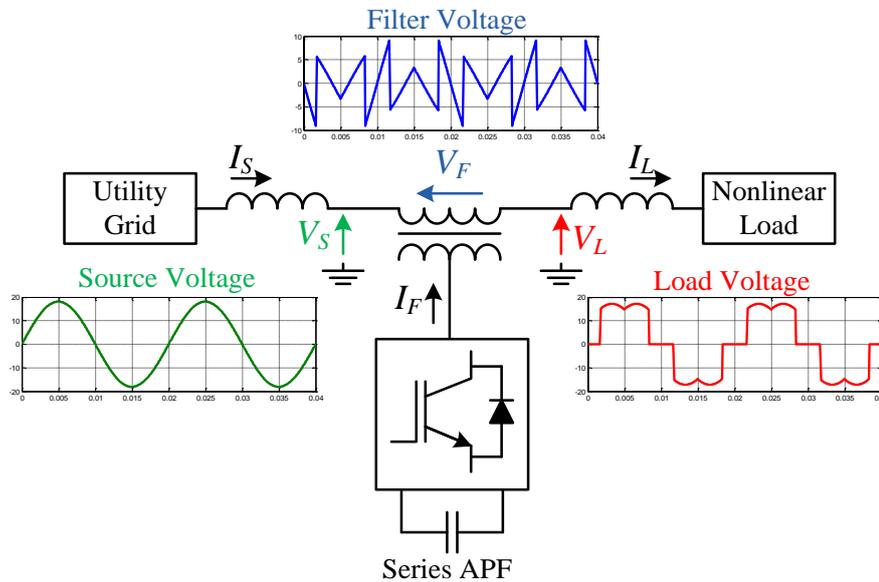
Figure 1.9 Series APF and its basic operating principle
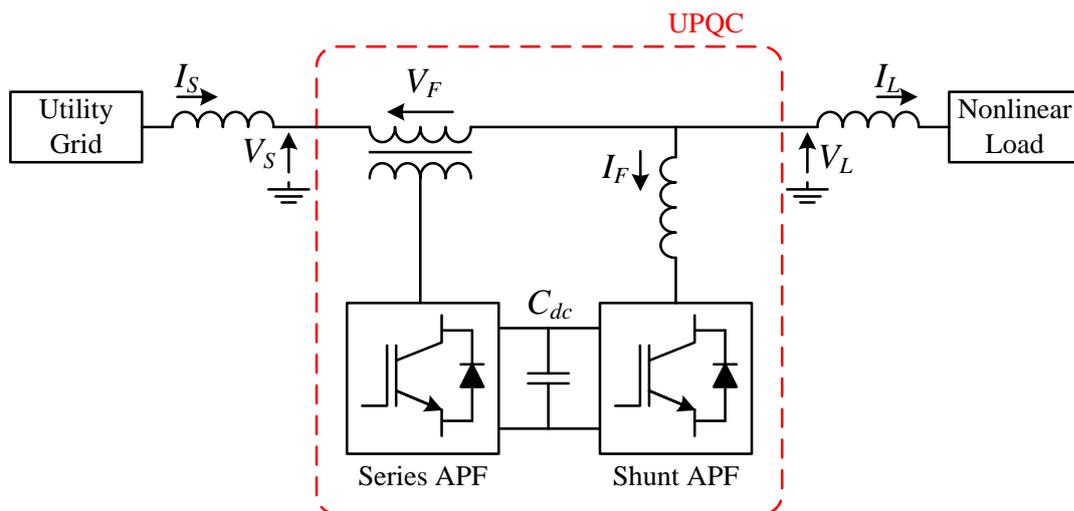
Figure 1.10 Unified Power Quality Conditioner

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APF systems can also be application specific with the integration of different control philosophies. Various researchers have implemented different and advanced control systems on APF converters [60]-[72] such as sliding mode control [64], predictive current control [65], constant power control [66], sinusoidal source current control [66], [67], Proportional Integral (PI) control [68], Kalman filter based PI control [69], proportional control [70], multi-rate fractional order repetitive control [71], and hysteresis band current control [72].

Finally, as the last type of active filtering device, HAPF systems are formed with the combination of active and passive filtering equipment. Their working principle and various topologies are mentioned in the following section.

1.2.2.2.   **Hybrid Active Power Filters**

As the APF systems has been used more and more in the industry and become popular, researchers found out that APF systems have some problems especially for high power and wide frequency applications. It has been a more preferable solution for some researchers to use passive filters together with APF converters in high power applications in order to reduce the size of relatively expensive APF converters. Moreover, passive filters also integrated to APF systems for applications that require suppression of harmonics in a wide-frequency range or require individual suppression of harmonics at a specific frequency. Those combined systems of both passive filters and APF converters are then called as HAPF and various researchers has been implemented different HAPF topologies in the literature [19], [20], [52], [53], [73]-[91]. One of the most preferred HAPF topology is the combination of a shunt APF and shunt passive filters as shown in Figure 1.11 [73]-[75]. The aim of using passive filters in this topology is to filter out the harmonics that are out of the designed range of APF by passive filters. By this way, APF converter installed capacity can be reduced. Passive filter part in this topology can be a single tuned LC filter or a combination of different LC filters tuned to different frequencies depending on the requirements of the application.
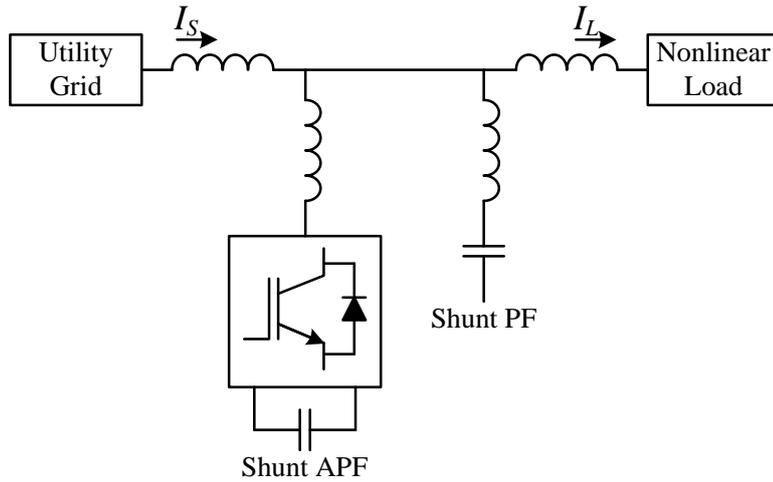
Figure 1.11 Combination of a Shunt APF and shunt passive filter

Another HAPF topology is the combination of series APF and a shunt passive filter as can be seen in Figure 1.12 [76]-[79]. In this topology, APF is used to suppress voltage harmonics and regulate the voltage in either side of the injection transformer while passive filter or combination of passive filters are designed to suppress current harmonics. The HAPF topology illustrated in Figure 1.13, on the other hand, is a series APF connected in series with a shunt passive filter [80], [81]. In this HAPF topology, APF converter is used to eliminate the series and parallel resonant risk of the passive filter and to provide an improved harmonic suppression performance.
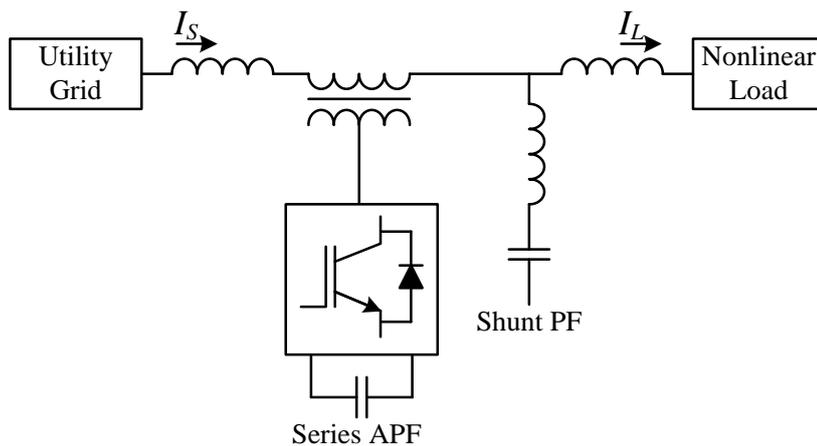
Figure 1.12 Combination of a series APF and shunt passive filter
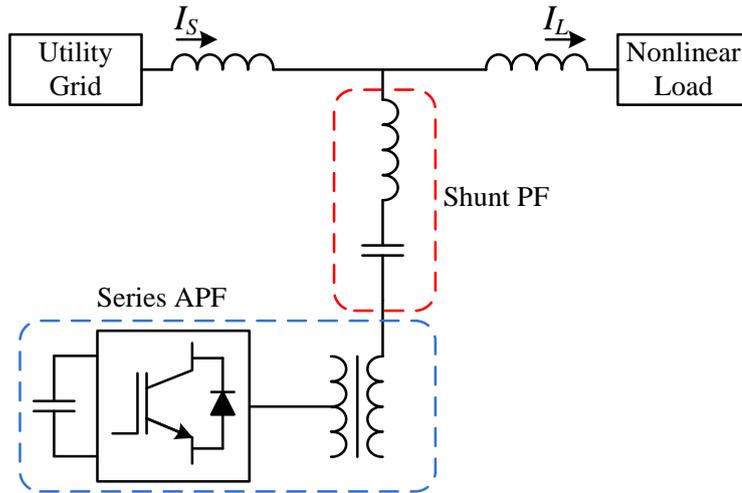
Figure 1.13 Series APF connected in series with shunt passive filter
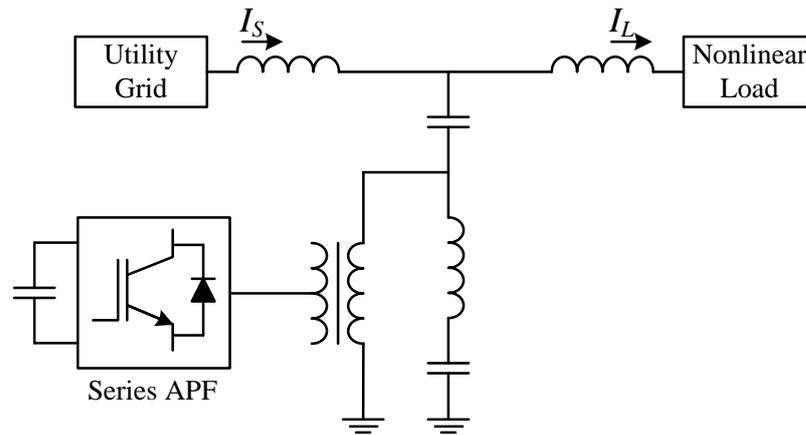
Figure 1.14 Injection type HAPF

Another combination of APF and passive filters is called as injection type HAPF and the circuit diagram of it is as given in Figure 1.14 [82]-[85]. This topology is the advanced version of the HAPF topology given in Figure 1.13. The most important advantage of this HAPF topology is to tune the LC filter located in the parallel branch of series APF to fundamental frequency so that series APF can be short circuited at fundamental frequency. Therefore, fundamental frequency source voltage totally drops on series capacitor instead of APF terminals resulting in reduced APF capacity

and semiconductor ratings. Although this topology has brought some important features, it still contains a bulky injection transformer and increased number of passive elements.
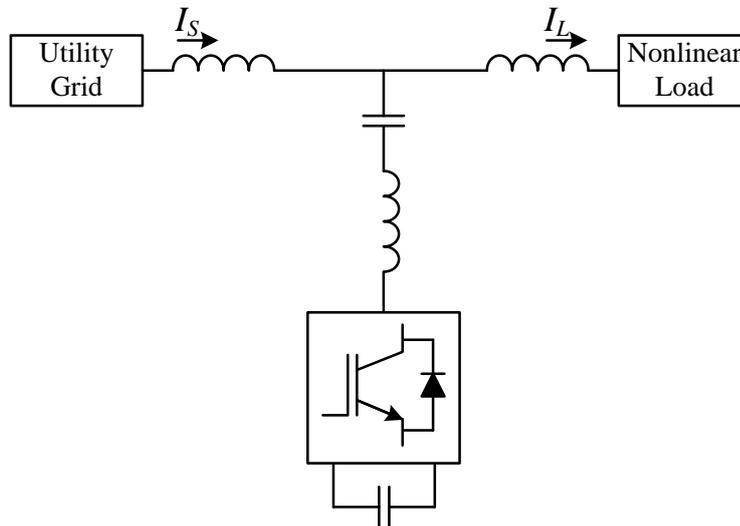
Figure 1.15 Circuit topology of a shunt HAPF

Shunt HAPF topology, on the other hand, is a shunt APF connected to grid via a passive filter coupling element as shown in Figure 1.15 [19], [20], [86]-[91]. The most important feature of this HAPF topology is that APF converter never generates voltage waveform in fundamental frequency [19], [20] which is due to high impedance characteristics of the passive filter at fundamental frequency [20]. Therefore, DC link of the HAPF converter can be reduced significantly, providing a decrease in switching losses, as compared to an APF system suppressing the same load harmonic profile [19]. Since passive filter behaves as a coupling element for the HAPF converter, its impedance characteristics determines the frequency range and bandwidth for which the HAPF is effective [20]. Some researchers suggest the use of combination of passive filters tuned to different frequencies instead of a single tuned one in order to make the HAPF effective for various frequency ranges [86] at the expense of reduced suppression performance between tuning frequencies.

1.2.2.3. Comparison of APF and HAPF

Different APF and HAPF topologies are mentioned in previous sections. Although each individual active filtering system topology may be suitable for different applications, a generalized comparison between APF and HAPF topologies can be made. HAPF topologies are superior to APF in terms of reduced DC link voltage thus lower semiconductor ratings and switching losses [19], [20], [89], significantly reduced converter installed capacity [86], [87], increased effective frequency range [20], reduced overall costs [88], [89], and more effective filtering of switching ripple [86]. However, HAPF topologies have also some drawbacks as compared to APF such as fixed amount of reactive power support at fundamental frequency [19], [20], existence of passive filter components, and reduced suppression performance for the frequencies out of the interested frequency range.

Considering the listed superiorities, a shunt HAPF topology is a suitable solution for the suppression of medium frequency IMF load which is the harmonic current source under investigation by this thesis and described in the following section.

1.3. Medium Frequency Induction Melting Furnaces

Medium Frequency IMF installation has become widely used for the last two decades in metal melting and forming industry, especially in small or medium size steel-melting facilities, due to their competitive installation cost and low running costs. Another reason for entrepreneurs to prefer IMF system is that they can be much smaller in size as compared to electric arc or ladle furnaces. Installed capacities of IMF systems can be 10-kW up to 32-MW with operating frequencies of $150 - 250$ Hz for medium frequency IMFs. Metal melting capacities of IMF installations have known to reach up to 60 tons.

1.3.1. Brief Description

IMF system melts the metals charged into the ladle via excessive heat caused by eddy currents inside the charged metals due to the changing magnetic field created by the

work coil wounded to the ladle in a solenoidal way [92]. Although IMF work coil had been driven by a motor-generator setup based frequency converters in early years [93], high power converters equipped with thyristors or IGBTs have been used for nearly half a decade with the advancements in power semiconductor industry [94]. A simplified circuit diagram of a typical medium frequency coreless IMF installation is as given in Figure 1.16. In high power density IMFs, work coil is fed by a single phase load resonant solid state converter, as can be seen in Figure 1.16, operating in a predetermined frequency range. Load resonant converters can change the operating frequency during a complete melting cycle in order to maintain tuning to the natural frequency of the work coil [95]-[97]. Therefore, input power of the IMF system can be kept nearly constant during a melting period. Load resonant converter DC link is usually fed from a 12- or 24-pulse thyristor rectifier, as can be seen Figure 1.16.
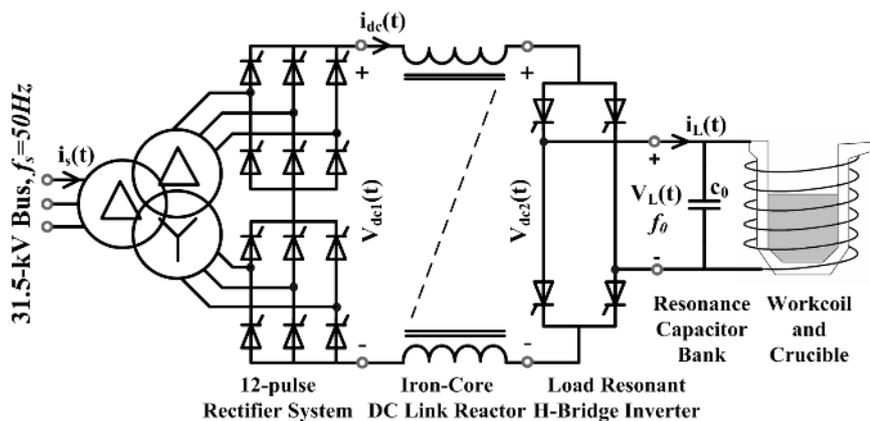
Figure 1.16 A simplified circuit diagram of a typical medium frequency coreless IMF installation

1.3.2. Power Quality Problems

In this section of the thesis, IMF system as a load in power system is evaluated in terms of common power quality problems such as flicker, voltage sag/swell, current/voltage unbalance, reactive power and power system harmonics. Flicker,

voltage sag/swell, and voltage/current unbalance analysis has been conducted in [17] and the following findings have been reported:

i.   The contribution of the IMF installation to the flicker is measured at medium-voltage (MV) bus using the method described in [98]. The contribution of IMFs to the flicker is found to be negligibly small.

ii.   Voltage sags and swells at PCC are not the characteristics of medium frequency coreless IMF load. The origin of the voltage sags and swells recorded during the measurements is mainly the faults in the outside or inside of the small steel-melting facility under investigation.

iii. Unbalanced bus voltages and line currents are not the characteristics of the medium-frequency coreless IMF load, because each IMF is supplied from the power system via a 12-pulse or a 24-pulse controlled rectifier.

Reactive power demand of the IMF load, on the other hand, is relatively low as compared to most of the industrial loads as can be seen in Figure 1.17. The input power factor of the IMF installation is around 0.96 lagging. Since some power system operators require a penalty limit for reactive power while some others require full compensation, reactive power demand of the IMF load should be compensated. Reactive power demand variation of the IMF load is not in a rapidly changing form.
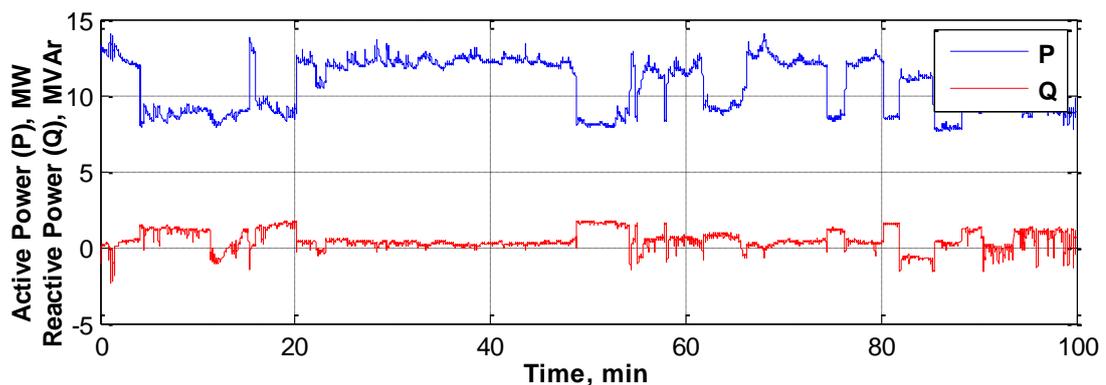
Figure 1.17 Active and reactive power measurements of the IMF load

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For this reason, the use of FACTS devices is not recommended for the reactive power compensation of the IMF load, instead load-break-switch switched tuned or detuned shunt passive harmonic filters are suggested. However, in this case, series and shunt resonance characteristics of those filters should be analyzed in detail in order to prevent failures caused by current harmonics of the IMF load. Therefore, the harmonic content of the IMF load voltage and currents should also be analyzed.

Although the IMF load is not a severe voltage harmonic source, it is one of the most problematic loads in the power system in terms of current interharmonics. This is because, the medium frequency coreless IMF system structure given in Figure 1.16 produces harmonic and interharmonic current components in the supply side due to the cross-modulation phenomenon in the AC-DC-AC link of the multi-pulse rectifier and load resonant converter cascade [17], [19], [20], [22], [99]. Furthermore, those harmonic and interharmonic current components vary in time in terms of both frequency and magnitude because of the changing operating frequencies of the load resonant converter during a melting cycle [17], [19], [20]. Change in the operating frequency of load resonant converter is caused by the random content and quality of the metal loads charged into the furnace ladle. In addition, the furnace ladle can also be charged with extra metals during melting phase. Frequencies of interharmonic components, f_{ih}, caused by mentioned cross-modulation phenomenon can be formulated as in (1.11).

$$f_{ih} = \left(1 \pm nP\right) f_s \pm 2k f_o(t) \tag{1.11}$$

where P is the pulse number of the rectifier circuit, f_s the frequency of the supply side power system, f_o the operating frequency of the load resonant converter, index $n = 0$, 1, 2, 3, …, and index $k = 1, 2, 3, ...$

Since operating frequency of the load resonant converter in Figure 1.16 changes from 150 to 250 Hz, the corresponding most dominant interharmonic frequencies due to cross modulation phenomenon can be calculated to be changing between 250 to 550 Hz by using (1.11) with $n = 0$, $k = 1$. As index n and k changes, various interharmonic

frequencies can be found by using (1.11). However, the magnitudes of those interharmonics tend to decrease dramatically as index n and k increase.

a)

b)
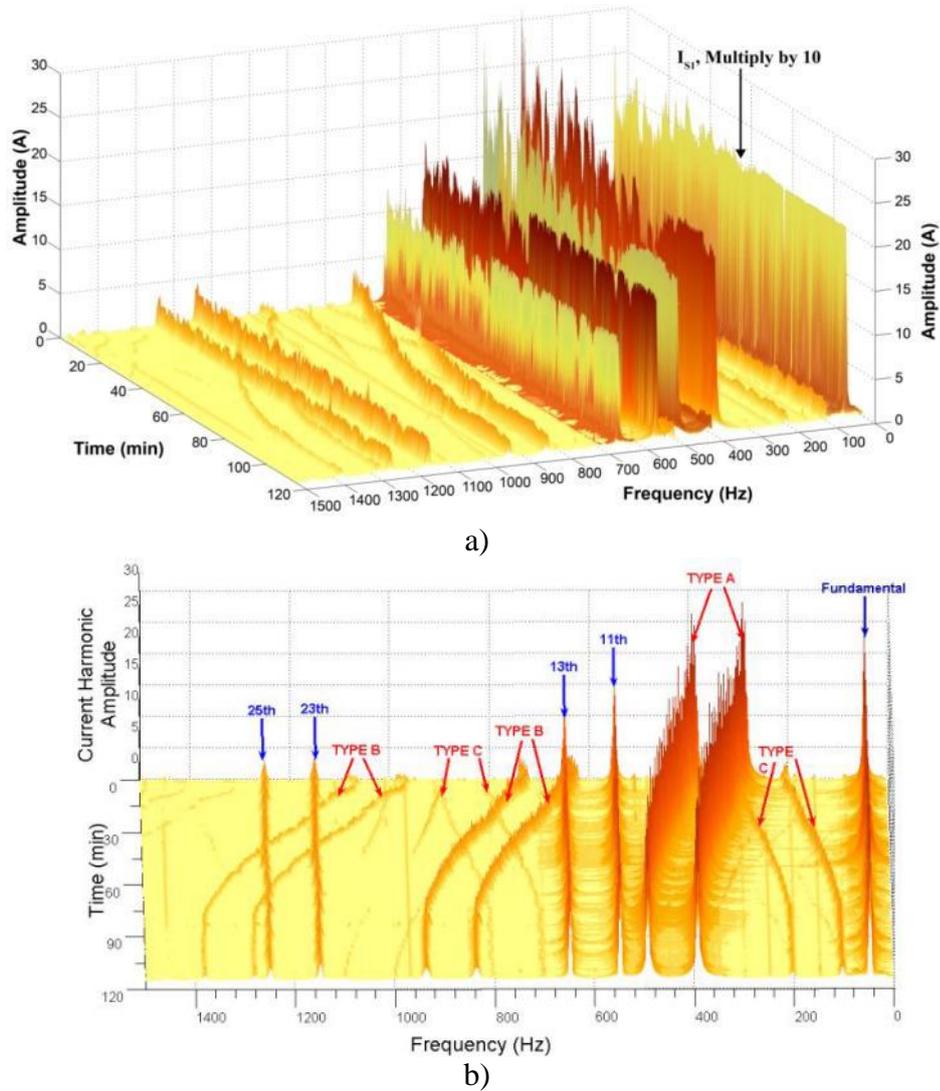
Figure 1.18 Variations in supply-side line current interharmonics and harmonics for a 12-pulse IMF installation during a typical melting cycle (deduced from the data recorded in the field) [17]. Type A: Interharmonics due to the cross modulation of fundamental supply frequency f_s and the inverter output fundamental frequency referred to the dc link $2f_o$, where $f_{cr} = 2f_o \pm f_s$. Type B: The cross modulation of f_s with current harmonic frequencies at the dc link at $2kf_o$, with $k = 2, 3, \ldots$, where $f_{cr} = 2kf_o \pm f_s$. Type C: The cross modulation of supply harmonic current frequencies at $(1 \pm 12n)f_s$, for $n = 1, 2, 3, \ldots$, and the dc-link current harmonic frequency at $2f_o$, where $f_{cr} = (1 \pm 12n)f_s \pm 2f_o$

Also, the result of (1.11) can be negative or positive. The minus sign for the resultant frequency in this equation implies that the corresponding frequency is in a negative-sequence form, while a plus sign implies positive-sequence.

Interharmonic frequencies and their symmetrical components have been calculated by using (1.11) at $k = 1, 2$ and $n = 0, 1$ for load resonant converter operating frequencies, f_o, 150, 175, 185, 200, 225, and 235 Hz in [20] and the findings can be observed in [20]. Time varying harmonics and interharmonics can be observed in the harmonic spectrum of IMF load, given in Figure 1.18, deduced by the field measurements of the steel melting facility under investigation [17].

1.4. Scope of the Thesis

Harmonic distortion in both transmission and distribution networks due to non-linear loads in industry and domestic applications has become a serious problem for a few decades. Various researchers have worked on mitigating unwanted harmful harmonic components caused by those nonlinear loads [31]-[45], [52]-[59], [73]-[91]. Passive filtering systems have been implemented widely by lots of researchers to overcome harmonic problems due to their low cost and efficiency [31]-[38]. However, due to resonance risk, source impedance dependent performance, and fixed compensation characteristics of passive filter solutions, active filtering equipment have become an important alternative especially for the compensation of rapidly changing nonlinear loads.

Active filtering solutions can also be used for reactive power compensation and load balancing in addition to their harmonic mitigation feature. There have been proposed various active filtering topologies in the literature [52]-[59], [73]-[91], however conventional shunt APF system is the most preferred topology. On the other hand, HAPF topologies have also been proposed by some of the researchers due to their advantages such as low dc link requirement, low converter capacity, effectiveness in wide frequency range and extra reactive power support [73]-[91]. By this way, HAPF topologies overcome the drawbacks of APF and passive filters by keeping the advantages of both.

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In this thesis, a HAPF system composed of nine identical three-phase three-wire two-level shunt HAPF units is designed and implemented in order to eliminate the harmonics and time varying interharmonics of a medium frequency coreless IMF load. Each of the shunt HAPF units consists a series LC filter connected in series with the HAPF converter. The implemented system has been successfully installed to a steel melting facility located in Hatay/Turkey. The steel melting facility contains three medium frequency coreless IMF loads operating randomly resulting in a random profile of harmonics and interharmonics, frequencies and magnitudes of which are changing in time. Hysteresis current control strategy is implemented as the waveform modulation method of each HAPF converter due to its basic implementation and impressive current reference tracking characteristics. Performance of the implemented system has been verified by the field measurements that the proposed system can suppress all the harmonics, interharmonics, and THD of the steel melting facility below allowed limits. A new performance evaluation criteria, namely Suppression Factor, for wide frequency harmonic filtering equipment is proposed and implemented system is evaluated using this criteria.

Moreover, the mathematical model of the hysteresis switched three-phase three-wire two-level HAPF converter is derived for eight possible switching schemes. Using this model, a fuzzy logic based hysteresis bandwidth generation method is proposed and implemented in the field in order to reduce the switching losses caused by hysteresis current control. By this way, hysteresis band can be narrowed for better reference tracking or widened for reducing the switching count thus losses according to the proposed hysteresis band generation method. The reduction in overall losses with the fuzzy hysteresis band method is observed without a significant reduction in harmonic suppression performance by analyzing the field measurements. Furthermore, effects of sampling frequency and execution time on hysteresis switching are also formulized and some suggestions are proposed for the current tracking errors, one of the drawbacks of proposed HAPF system. All of the necessary formulation are derived, used methods are explained, and both simulation and experimental results are given in the following chapters of the thesis, outline of which is given below.

In Chapter 2, system topology is introduced and operating principle of hysteresis band controlled HAPF is described. Firstly, circuit diagram of HAPF converter and single line diagram of the steel melting facility is given. Then, the reference generation method of proposed method is given by describing in detail the auxiliary methods used in the reference calculation procedure. Finally, the details of hysteresis band control technique and proposed waveform modulation method is mentioned in detail. Comparison of proposed method with conventional HAPF control method is made and the mathematical model of hysteresis band controlled HAPF converter is derived.

In Chapter 3, design procedure for all of the circuit parameters of HAPF converter is stated. In order to reach this aim, first of all, harmonic content of the load is analyzed using the field measurements. Then, input LC filter parameters are designed according to the deductions made by harmonic content analysis made. Finally, converter parameters are determined by using the simulation model and theoretical results are given by using this model.

In Chapter 4, implementation of proposed HAPF system and experimental results are presented. Semiconductors, dc link capacitors and passive filters as a power stage in the implemented system are introduced. In addition to the power stage, control and protection circuits, water cooling system, flowchart of the control algorithm and hierarchical control system architecture are also given in detail in this chapter. Finally, the results of the experiments conducted in the field and their evaluations are also discussed.

Further improvements and future works are stated in Chapter 5. Firstly, adaptive fuzzy hysteresis band control method, its formulation, simulation results and field implementations are shown. Then, effect of sampling frequency and execution time on the reference tracking performance of hysteresis band control method is analyzed and some improvements as a future work are proposed.

In chapter 6, general conclusions and suggested improvements are discussed.

In Appendix A, mathematical expressions of converter phase voltages for each of the hysteresis band control switching schemes are derived.

In Appendix B, symmetrical component analysis results of each of the harmonics and interharmonics with 5 Hz steps are illustrated for the steel melting facility under investigation.

In Appendix C, harmonic analysis report of the steel melting facility under investigation before and after the suppression of its harmonics are given.

1.5. Original Contributions of the Research Work

The research work described in this thesis has some important original contributions to the literature, and those contributions are mentioned in this section.

The proposed Hybrid Active Power Filter with the proposed hysteresis band current control algorithm is the only industrial application published in the literature in terms of the active suppression of time varying harmonics and interharmonics in a wide range. The proposed Hybrid Active Power Filter is shown to be very effective for the suppression of all the dominant harmonics and interharmonics of the IMF load. Moreover, since very few researchers have been conducting research on active filtering systems operating in a wide frequency range, an effective performance evaluation criterion is missing for the evaluation of the performance of the filtering equipment in a wide frequency range. A novel performance evaluation criterion, namely Suppression Factor, is proposed in this thesis and the short and long term field performance of the Hybrid Active Power Filter is evaluated for the entire frequency range during a sufficiently long recording period by using Suppression Factor concept. After successive implementation of the proposed hysteresis band current control method to the HAPF system, an artificial intelligence based improvement is added to the control algorithm in order to further increase the power efficiency of the Hybrid Active Power Filter. In this way, an adaptively changing hysteresis bandwidth is generated via fuzzy logic relations to reduce the switching losses of HAPF for the first time in the literature on three-phase three-wire two-level voltage sourced converters. It is shown in the results of the research work that the adaptive fuzzy hysteresis band current control strategy is reduced the overall losses of implemented HAPF system by around 9%.

CHAPTER 2

HYSTERESIS BAND CONTROL OF HAPF

For the compensation of PQ problems, especially harmonic distortion, of the IMF load introduced in the previous section, a HAPF topology together with the Hysteresis Band Control (HBC) is proposed in this research work. The details of the converter topology, control system components, and theory of the implementation will be mentioned in the following sections.

2.1. Circuit Topology and System Description

The steel melting and forming facility, the main concern of harmonic compensation problem, has two 12-pulse and one 24-pulse medium frequency IMFs each of them is run randomly depending on the workload, type and amount of the steel to be melt. The single-line diagram illustrating all the components of the facility is given in Figure 2.1.

In addition to the IMF installations, steel melting facility contains some other loads like dust collector blowers, lightning, electrical machines, and cooling pumps etc. Those other loads do not create considerable harmonic distortion, but they only consume reactive power. Circuit breaker (CB) switched detuned filter banks has already been installed at the Medium Voltage (MV) bus for the compensation of reactive power consumed by the steel melting and forming facility. The reason for the detuning of filter banks is for avoiding possible resonances due to the harmonics and interharmonics generated by the IMF load [18].

In addition to the mentioned PQ problems of IMF in earlier parts of the thesis, the whole steel melting plant load can be considered as a three-phase three-wire balanced

system. In order to show the balanced structure of the overall plant load, voltage and current waveforms of the source, load, and the sum of all phases are given in Figure 2.2 - Figure 2.4 by using the measurements of class A PQ analyzer introduced in [100].
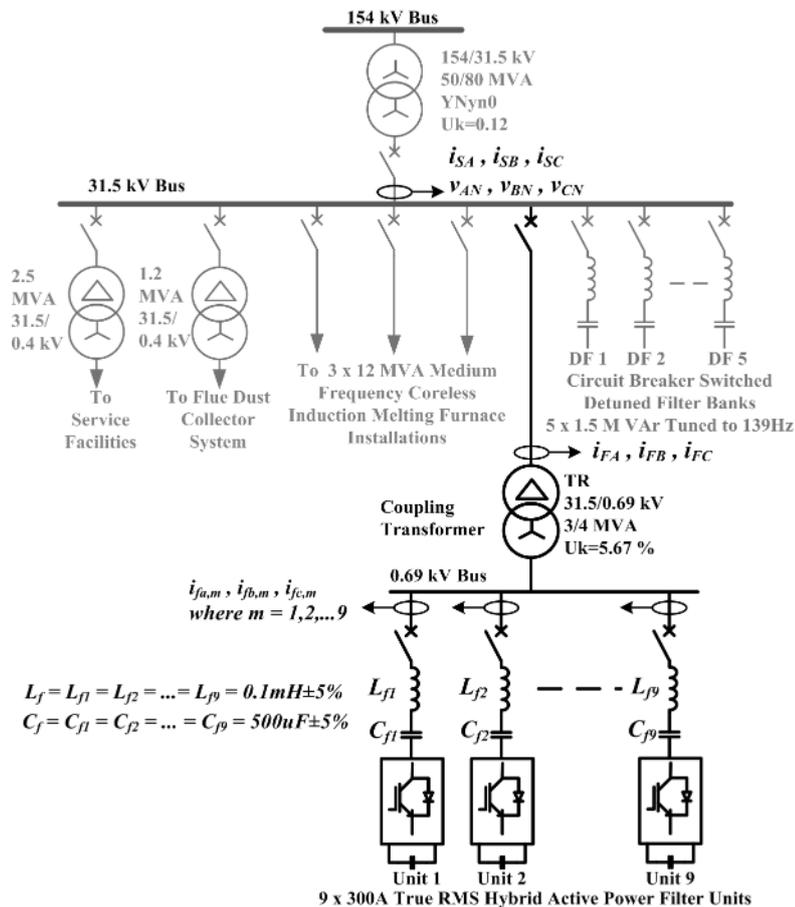
Figure 2.1 Single line diagram of the steel melting facility

Figure 2.2.a shows the phase voltage waveforms of the grid together with the sum of all instantaneous phase voltages. For better evaluation, Figure 2.2.b is given as the zoomed version of the sum of all instantaneous voltages. Similarly, the line current waveforms of the source while HAPF is operating are illustrated in Figure 2.3.a with the sum of all the instantaneous values and its zoomed version in Figure 2.3.b. Since Figure 2.3 contains both the load and the HAPF, the load current waveforms alone are

also given as the same form with the previous figures in Figure 2.4. As can be observed from the Figure 2.2 - Figure 2.4 that the sums of all current and voltage waveforms are almost zero. Actually, measured small amounts (less than 1% of the phase parameters) in the summation can be attributed to the cumulative error of the voltage and current measurement transformers. Thus, steel melting plant load under investigation is a three-phase three-wire balanced load.
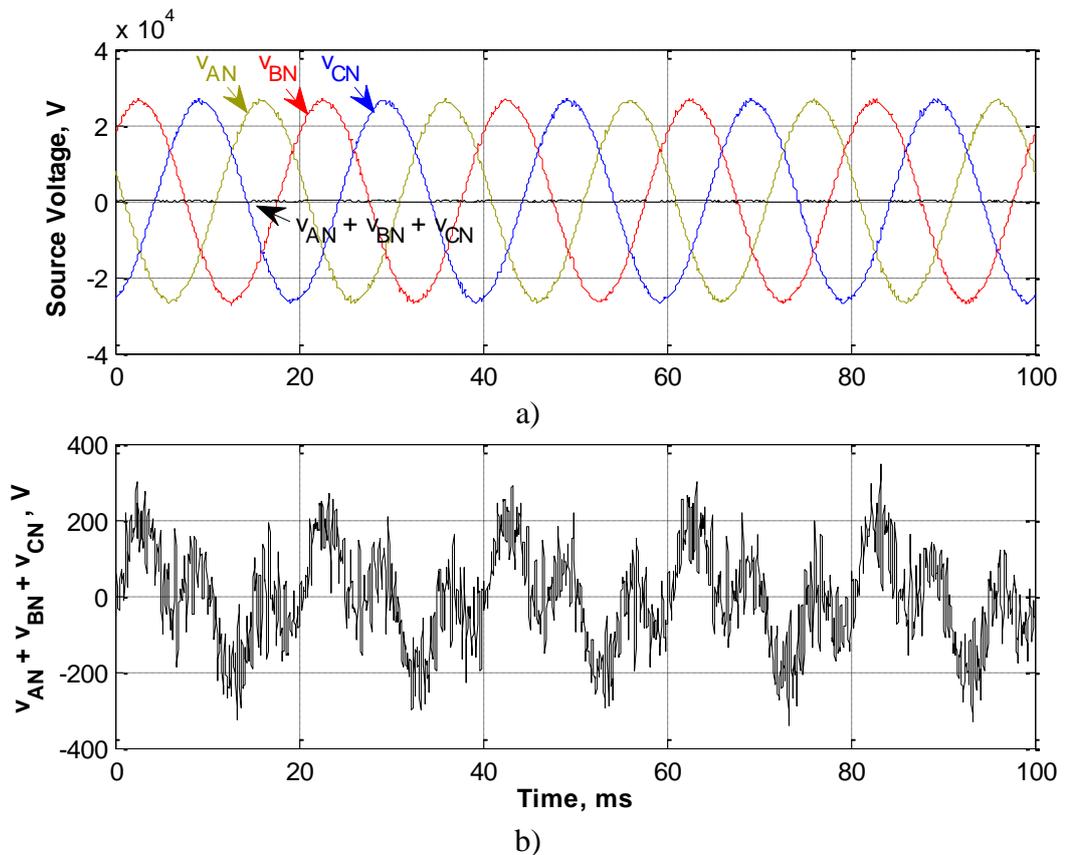
Figure 2.2 Source voltages (field measurements) a) l-to-n voltage waveforms and b) sum of instantaneous values of l-to-n voltages

Moreover, it is also formulated in earlier chapters that some harmonics may exist in a negative or positive sequence form by (1.11). If there are more than one IMF installations operating simultaneously in the steel plant, there may exist both positive and negative sequence current components at the same time for some harmonics and

interharmonics, considering the working regime of a single IMF load. Figure 2.5.a, b and c show symmetrical components, deduced from the field measurements, of some selected harmonic, interharmonic, and fundamental components of the load current in order to illustrate the existence of both positive and negative sequence components simultaneously.
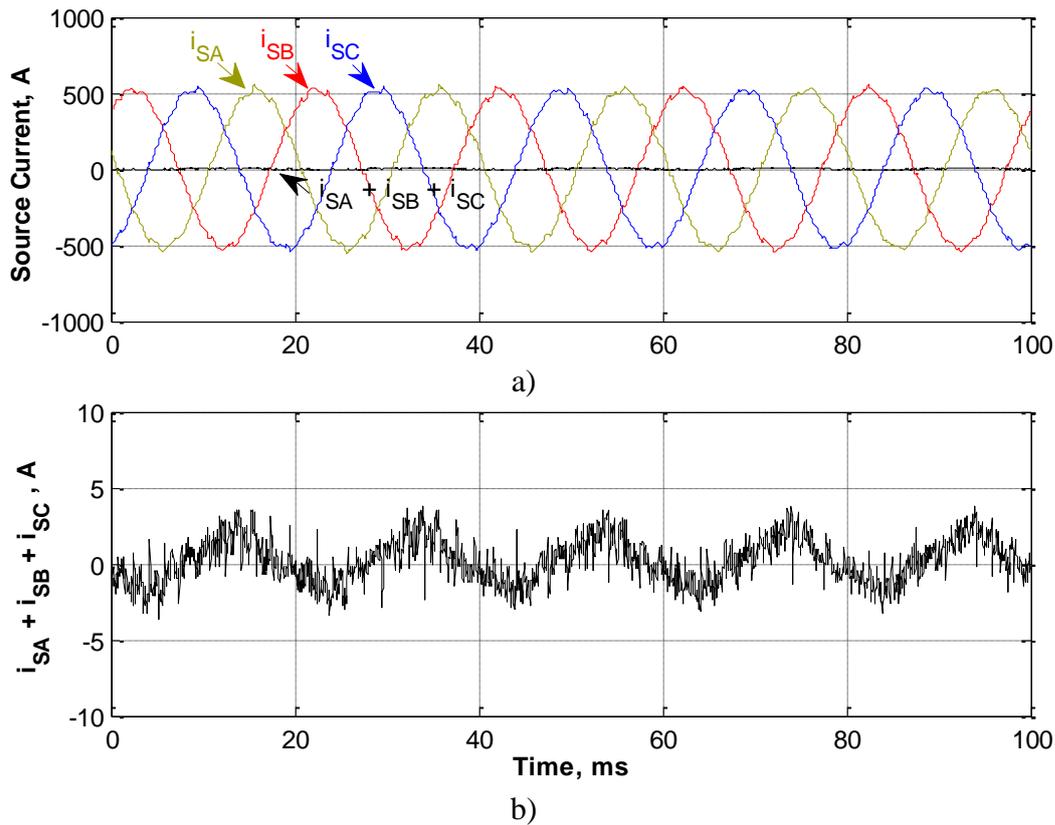
Figure 2.3 Source currents of the steel melting facility containing HAPF system (field measurements) a) line current waveforms and b) sum of instantaneous line currents

Figure 2.5.a shows the symmetrical component analysis of fundamental frequency component, 50 Hz in this particular application. It can be seen in this figure that fundamental component does not contain negative or zero sequence components, which implies that the IMF load is a balanced and symmetric load. Existence of both

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negative and positive sequence components is illustrated in Figure 2.5.b for the 7th harmonic component of the load current. It should be noted that 7th harmonic is one of the most dominant characteristic harmonics in power system and it always appears as a positive sequence form. However, it can also be in negative sequence form for the melting facility load. Symmetrical component analysis for an interharmonic frequency has also been given in Figure 2.5.c. It can easily be observed in Figure 2.5.c that both negative and positive sequence components may exist at the same time for an interharmonic, 435 Hz for this particular time interval. Although, there may exist both positive and negative sequence current components for some harmonic and interharmonic frequencies, this is not certain that those frequencies always contain both symmetrical components.
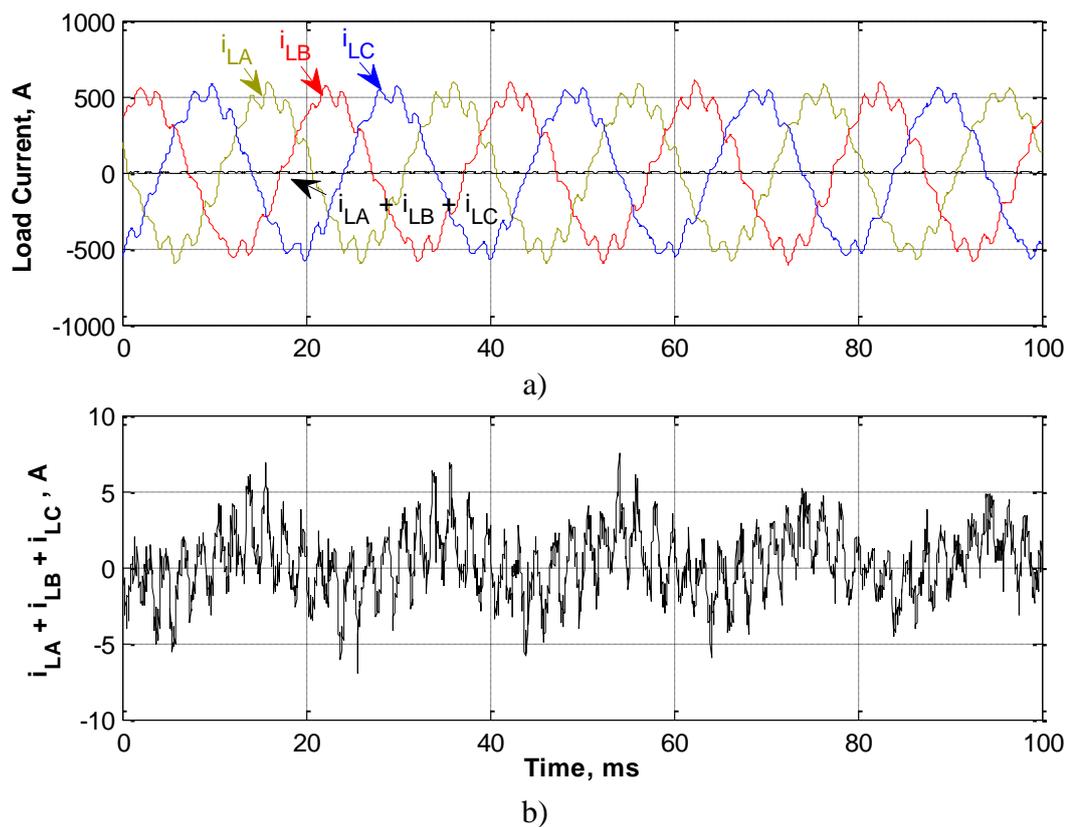
Figure 2.4 Currents consumed by all loads in the steel melting facility (field measurements) a) line current waveforms and b) sum of instantaneous line currents

The existence of the symmetrical components strongly depends on the working regime of each of the furnaces and resonant frequency for the load resonant converters driving them. One of the important conditions for the existence of both symmetrical components is that there must be at least two IMF loads operating at the same time for the steel melting facility.
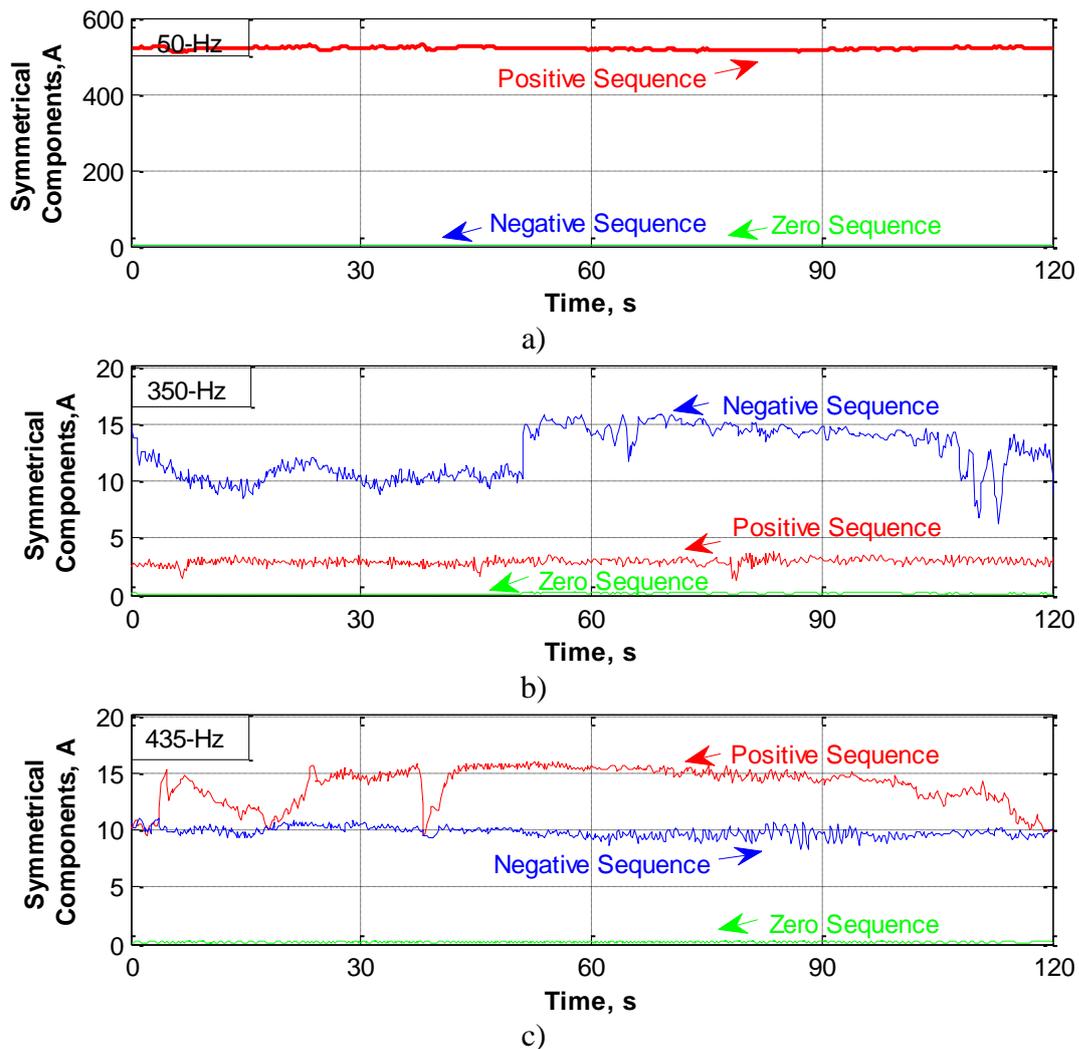
Figure 2.5 Symmetrical components analysis of a) fundamental component, b) a sample harmonic component, and c) a sample interharmonic component

The HAPF system proposed for the suppression of harmonics and interharmonics of the load under investigation has been connected to the MV bus of the steel melting

plant via a specially designed coupling transformer. The transformer was designed and manufactured in ELTAŞ Transformer Co. Izmir/TURKEY [101] considering the harmonic content of the HAPF converter currents. Nine identical HAPF units, each has intended to provide 280kVA of apparent power, are connected in parallel to the 690V transformer secondary bus. Therefore, the total installed capacity of the HAPF system reaches up to 2.5 MVA.

Each HAPF unit basically contains a three-phase three-wire VSC in series with an LC type input filter. The circuit diagram of each identical HAPF unit is as given in Figure 2.6. Each HAPF unit has some auxiliary circuits and devices for the proper and safe operation as shown in Figure 2.6. A discharge circuitry is used for the discharging of DC link capacitors in case of any fault or stopping procedure. Discharging resistor is switched using contactors for discharge operation. A contactor switched pre-charge branch should also be needed for soft energizing the passive LC filter, since it draws excessive current at cold start. The pre-charge resistor helps limiting the inrush current of LC filter. After pre-charging the passive elements, the CB is switched automatically and short circuit the pre-charge branch for normal operation of HAPF units. CB is also used for overcurrent protection purposes.
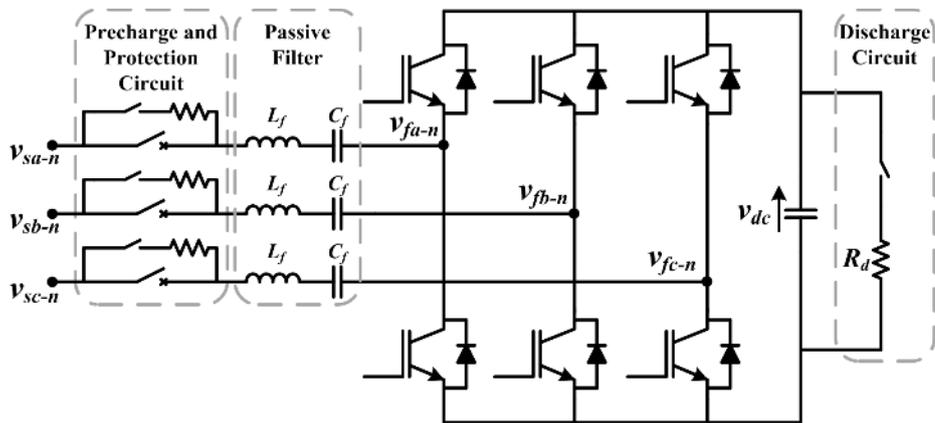
Figure 2.6 Circuit topology of each HAPF unit

2.2.   Generation of Current References

As the characteristics of the IMF load, similar to most of the other industrial harmonic sources, harmful harmonics and interharmonics appear in current waveforms. Those harmonics and interharmonics should be thoroughly analyzed so that the HAPF system can generate the proper reference signals thus the proper current waveform. In this thesis, some auxiliary methods have been used for the generation of filter current references. Phase Locked Loop (PLL), Synchronous Reference Frame (SRF) method and Selective Harmonic Extraction (SHEx) are some of the important methods used for the control algorithm. Moreover, use of the correct waveform modulation technique has also an essential part of the proper realization of reference signals. For this purpose, HBC has been proposed in this particular research work and mathematical background of HBC is explained in detail for the following sections.

2.2.1. Phase Locked Loop (PLL)

The phase angle of source voltage has a great importance for the reference calculation of utility connected power electronics converters. PLL is the most widely used and effective method for obtaining phase angle. Output of PLL is basically used for the reference for any other relative phase angles of currents and voltages inside the system. Furthermore, a reference phase angle locked to source voltage is needed for regulation of reactive and active power flow at fundamental frequency, which is a necessity for DC link regulation of the converter. In addition to fundamental frequency reference calculations, PLL phase angle can also be used to generate an integer multiple of it, which creates a virtual phase angle for an integer multiple of fundamental frequency. Obtaining integer multiple of fundamental frequency is important for creating precise references for active harmonic filtering equipment especially when fundamental frequency deviates around its rated value. For example, to illustrate the importance of integer multiple of phase angles, when fundamental frequency changes 0.5 Hz for a 50 Hz system, the 25th harmonic frequency changes 12.5 Hz which may correspond to calculation failure of harmonic references. However, if PLL is used, it robustly follows the voltage waveform even if the grid

synchronous frequency changes. The expected outcome of the PLL is as given in Figure 2.7, where T in this figure represents the period.

The block diagram for the calculation of phase angles of the source voltages via PLL method is as illustrated in Figure 2.8. Instantaneous values of source voltages are transformed to dq reference frame via a sequence of Clarke [102], [103] and Park [102], [103] transformations. This sequence of transformations is called as SRF method and it is also used for the reference current calculation. Detailed description of SRF method is given in the following section. V_d component of the signal transformed to dq reference frame is applied to PI controller and then integrated to get θ angle. It should be noted that the resultant angle is used as the feedback for Park transformation block. Moreover, V_d^* reference in the block diagram, Figure 2.8, is used for determining the phase that the PLL is locked on d reference, thus it should be zero for this particular application in order to get a similar waveform given in Figure 2.7.
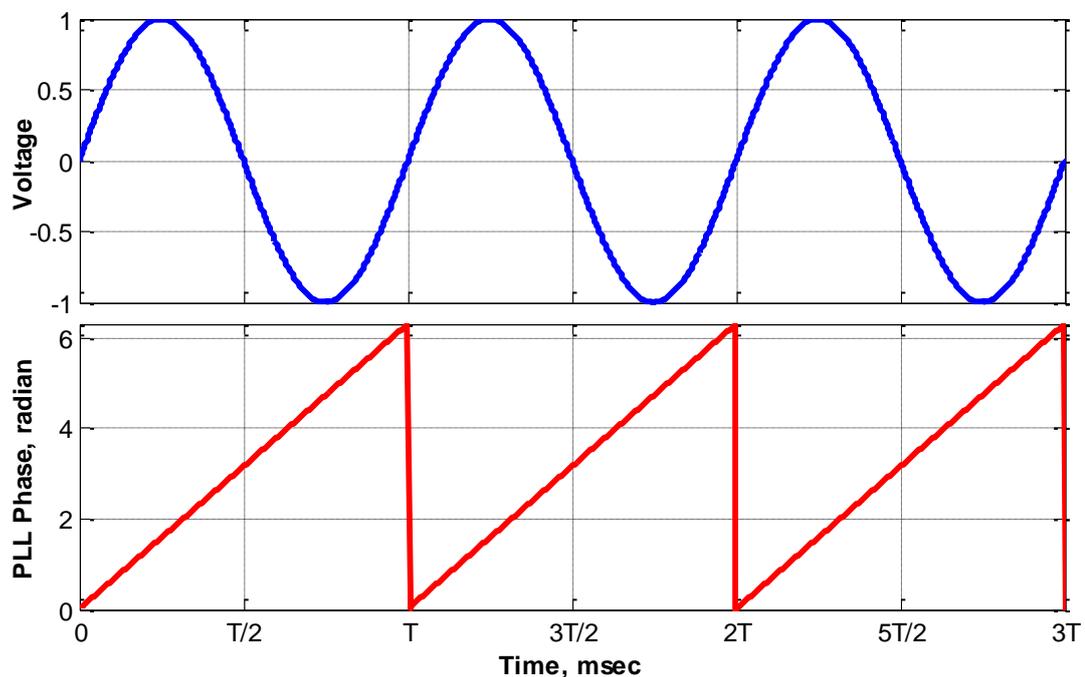
Figure 2.7 Illustration of PLL output waveform

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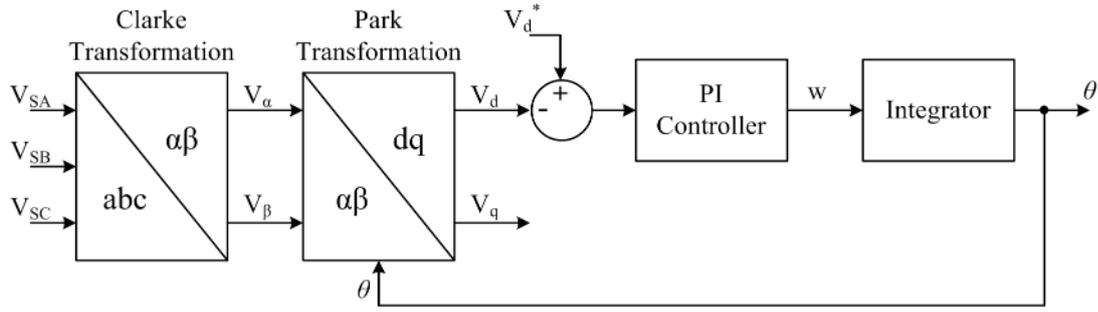
Figure 2.8 Block diagram representation of PLL

2.2.2. Synchronous Reference Frame (SRF)

Alternating signals can be represented as vectors rotating with an angular velocity of its angular frequency, w_S, on a Cartesian coordinate reference frame as illustrated in Figure 2.9.a. Magnitudes of those vectors are the peak values of corresponding signal phases. Alternating signal vector representations are shown to be rotating with an angular velocity since they are observed by an observer on the stationary reference frame. Suppose that, the reference frame is also rotating with any angular velocity towards either clockwise or counter clockwise direction. In this case, the alternating signal vectors should be represented by their relative angular velocities with respect to rotating reference frames. Figure 2.9.b and c illustrate the same alternating signal vectors with respect to reference frames rotating clockwise with an angular velocity of w_1 and counter clockwise with an angular velocity of w_2, respectively. As can be seen from Figure 2.9.b, relative angular velocity of alternating signal vector is $w_S - w_1$ with respect to the reference frame rotating in the same direction with the signal. Please note that if the velocity of rotating reference frame exceeds the velocity of signal vectors, signal vectors are observed as if they are rotating towards opposite direction. Similarly, alternating signal vectors are observed as if they are rotating with angular velocity of $w_S + w_2$ with respect to the reference frame rotating in opposite direction as illustrated in Figure 2.9.c. On the other hand, if the reference frame is chosen to rotate at exactly the same angular velocity with the alternating signal, this reference frame is called as the SRF. Considering the previous explanations, it can be

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reached by inspection that the alternating signal vectors are observed as if they are stationary with respect to SRF as shown in Figure 2.10.

By using SRF method, all the harmonic content of the IMF load under investigation by this thesis can be obtained. An SRF rotating synchronously with the fundamental frequency of the load current signal should be formed in order to reach this aim. Forming an SRF requires two successive transformation processes, namely Clarke and Park transformations [102], [103]. At first, three phase signal vectors should be converted to perpendicular two phase, namely phase α (alpha) and β (beta), representation as illustrated in Figure 2.11.b by using the Clarke Transformation.
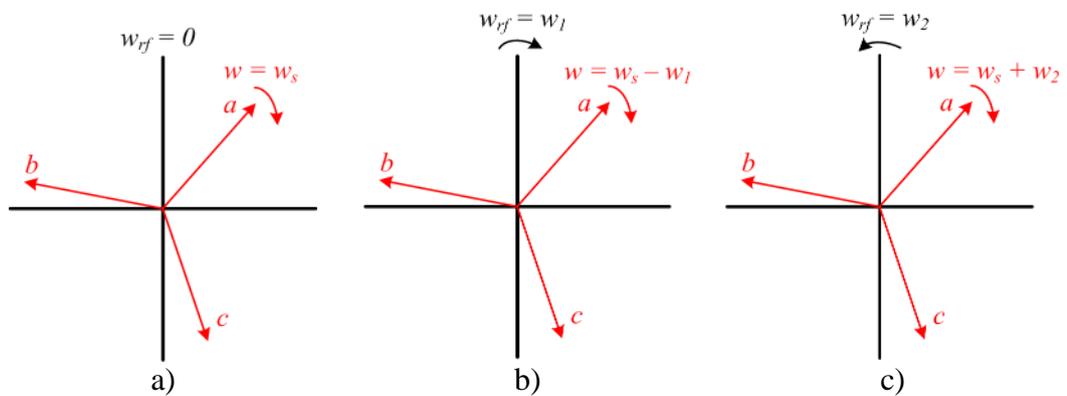
Figure 2.9 Representation of three phase signals in a) stationary reference frame, and reference frames turning b) clockwise and c) counter clockwise direction
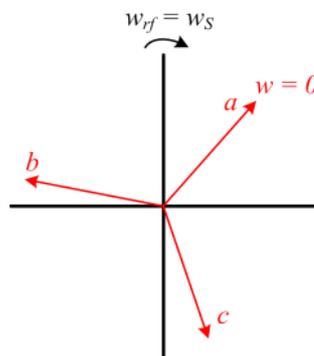
Figure 2.10 Representation of three phase signals in a synchronously rotating reference frame
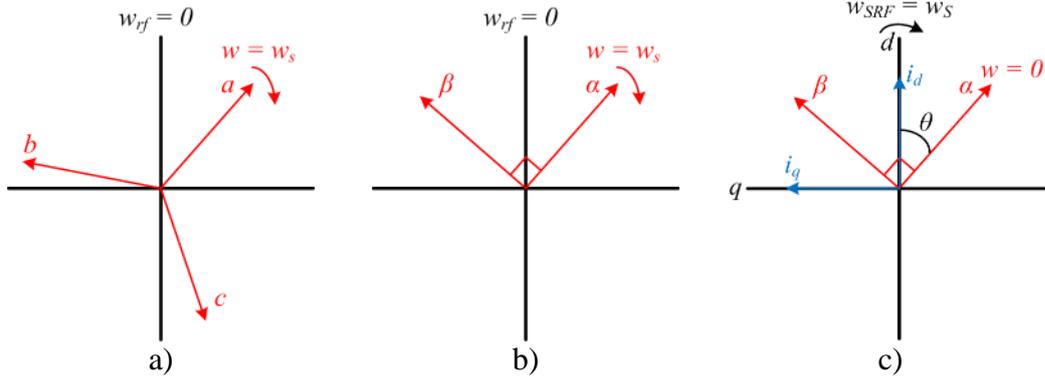
Figure 2.11 Alternating current signals in a) three phase form and two-phase representations with respect to b) stationary and c) synchronous reference frames

Power invariant Clark transformation and its corresponding inverse transformation matrices are as given in (2.1) and (2.2), respectively. Clarke transformation matrices are given for current signals however they are also valid for voltage signals too.

$$
\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = C \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} \\ 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.1}
$$

$$
\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = C^{-1} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \dfrac{1}{\sqrt{2}} & 1 & 0 \\ \dfrac{1}{\sqrt{2}} & -\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} \\ \dfrac{1}{\sqrt{2}} & -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{2.2}
$$

Following Clarke transformation, two-phase representation of the signals should be converted to direct (d) and quadrature (q) axes of SRF by using Park transformation as illustrated in Figure 2.11.c. The projections of alpha and beta phases on the d and q axes of SRF are constant values depending on the θ angle and can be found by using the well-known Park transformation matrix given in (2.3). Corresponding inverse transformation matrix is also given in (2.4).

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$$
\begin{bmatrix} i_d \\ i_q \end{bmatrix} = P \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.3}
$$

$$
\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = P^{-1} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.4}
$$

Rate of change of θ angle is the angular velocity of the SRF which is also the fundamental frequency of the signal under investigation. As mentioned in earlier section, θ angle can be found by using the PLL method.
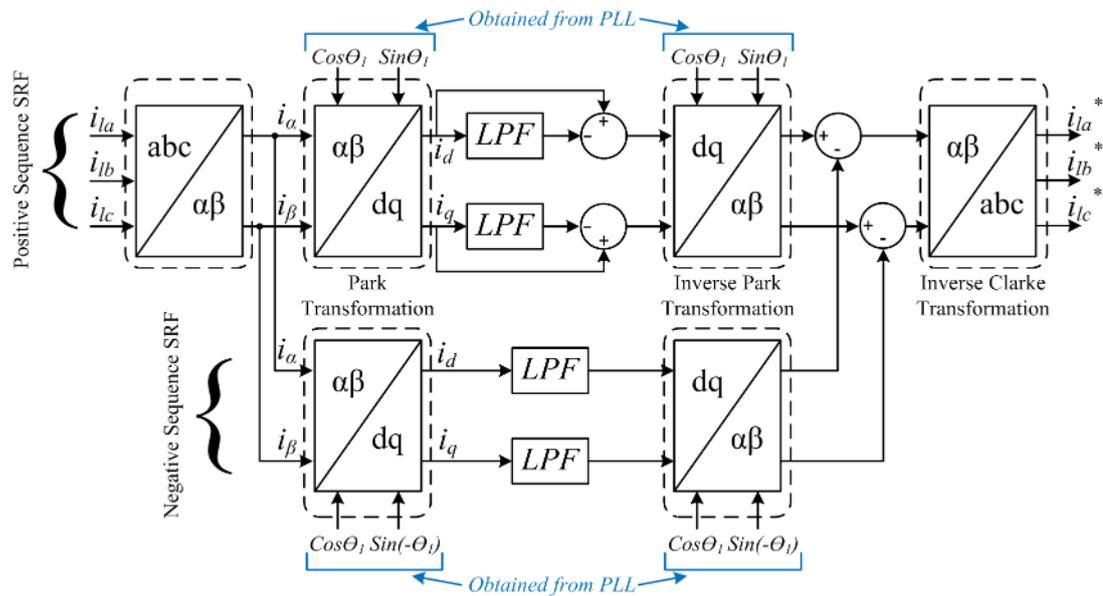
Figure 2.12 Block diagram representation of the current reference calculation based on SRF method

Finally, after Park transformation, the signal under investigation is now being observed by the point of view of an observer on the SRF rotating at fundamental frequency. Therefore, fundamental frequency component appears as a dc component while all the other harmonic components are in their relative frequencies with respect to SRF. For example, suppose a sample signal contains a positive sequence

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fundamental component, 50 Hz, a negative sequence 300 Hz, and a positive sequence 350 Hz components. Applying SRF method will lead to a resultant signal in which positive sequence 50 Hz component appears as a DC, the negative sequence 300 Hz component as negative sequence 350 Hz, and the positive sequence 350 Hz as positive sequence 300 Hz. Symmetric components have an important role in SRF method, if 350 Hz component were in positive sequence form then it would appear as 400 Hz. Considering the signal after SRF method has been applied, the fundamental frequency component can be easily extracted from the whole signal with the help of a Low Pass Filter (LPF) having cutoff frequency of 20-30 Hz without any distortion on the other components.

Remaining signal, after extracting the fundamental component, contains all the harmonics of the load current but with respect to SRF. In order to obtain the reference signal in three phase abc domain, the remaining signal should be multiplied by inverse transformation matrices given in (2.2) and (2.4). The overall block diagram representing the reference generation by SRF method is as given in Figure 2.12. As shown in Figure 2.12, negative sequence components of fundamental frequency should also be extracted in order to eliminate the fundamental currents caused by unbalance.

2.2.3. Selective Harmonic Extraction (SHEx)

A nonlinear load to be compensated may consist some harmonic components which are not wanted in converter reference current. Therefore, those harmonics should be extracted from the reference current signal. Some reasons for extraction of a harmonic from reference signal may be that the harmonic may not exceed allowable limits thus there is no need to further suppress it in order to reduce converter capacity, that the active filtering equipment may not be able to compensate it even if it is included in the reference, and that there is another active or passive filtering equipment designed specifically to suppress it. The load under consideration of this thesis contains 23rd and 25th characteristic harmonics due to the 12- and 24-pulse structures of IMFs. Since the HAPF converter specifically designed to suppress harmonics and interharmonics

from 250 to 650 Hz, input LC filter has a very large impedance and phase delay at 23rd and 25th harmonic frequencies. Therefore, HAPF converter may not be able to suppress 23rd and 25th characteristic harmonics even if there exist very high reference signals for them. For those reasons, 23rd and 25th characteristic harmonics are needed to be extracted from current reference signal and left uncompensated with a suggestion of passive harmonic filter equipment tuned to those frequencies.
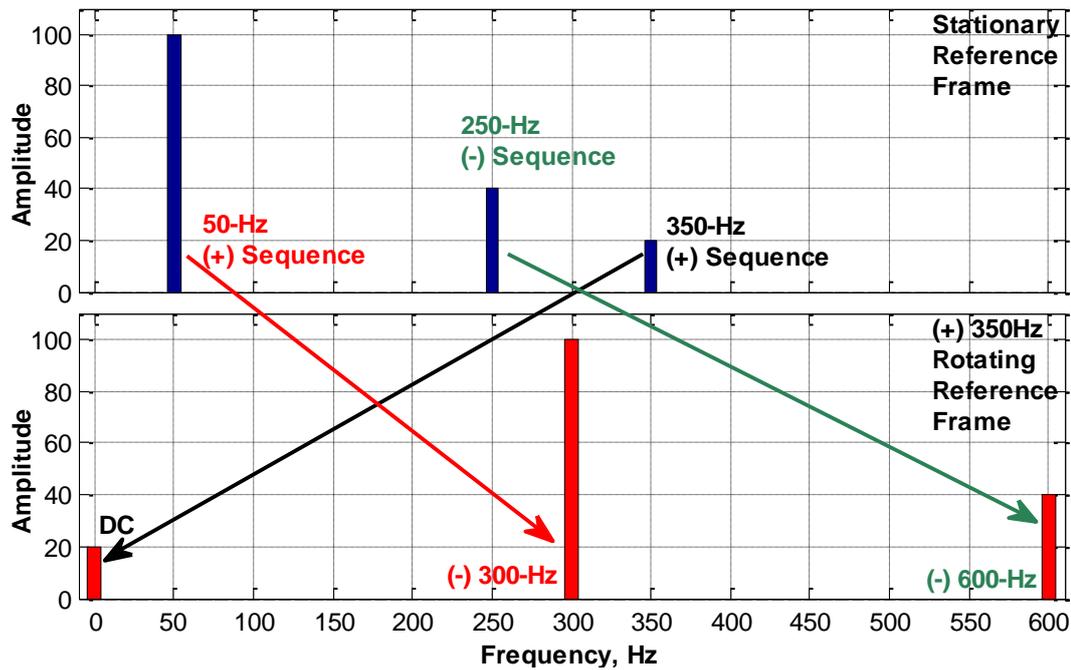
Figure 2.13 Illustration for the use of rotating reference frames on SHEx method

SHEx [19], [20] is a method for extracting unwanted harmonic components from the converter reference current without any effect on other frequency components. This method selectively obtains the harmonic to be extracted by using SRF rotating at that harmonic frequency. The selected harmonic will appear as a DC signal relative to the SRF because it has the same frequency with the rotating frame. Other harmonic components appear as AC signals relative to the rotating reference frame. An example representing the use of rotating reference frames on SHEx method can be seen in

Figure 2.13. Figure 2.13 shows the frequency spectrum of an example signal and its relative form with respect to a rotating reference frame (350 Hz, in positive direction).

In order to obtain the selected frequency alone, all the other components other than DC should be totally filtered out by an LPF without any attenuation on DC component. The corner frequency of the LPF should be thoroughly designed. For this reason, the whole load frequency spectrum should be known before applying the SHEx method in order to make sure that there is not any closely located harmonic component relatively rotating around SRF frequency, which may cause wrong calculation of selected harmonic frequency. An illustration of an effective filtering for obtaining the DC component of the example signal in Figure 2.13 is given in Figure 2.14.
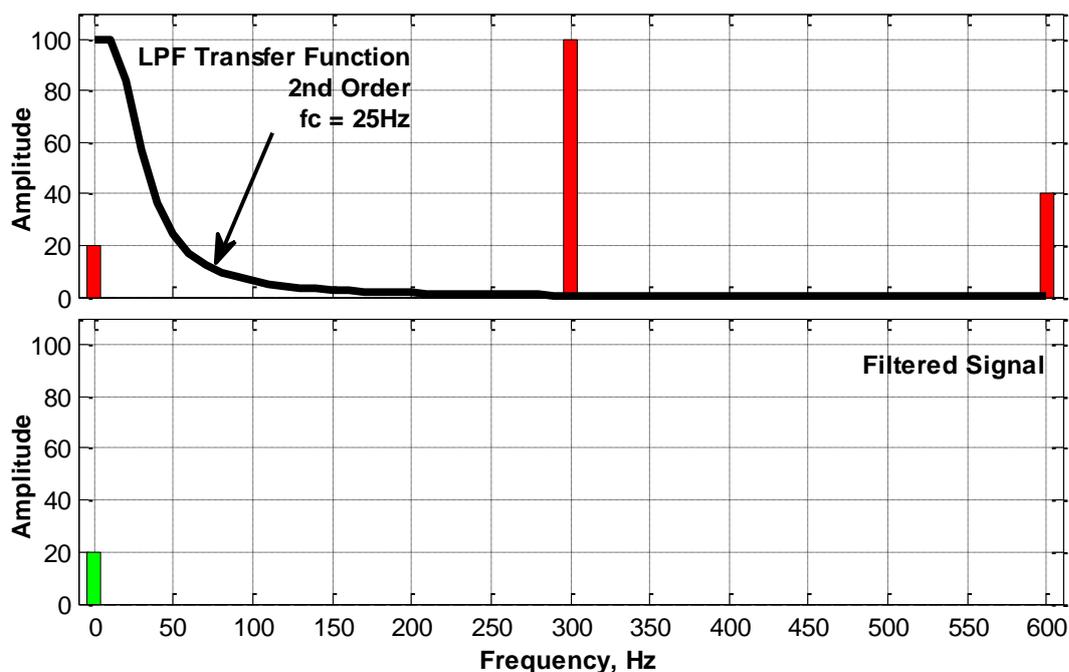
Figure 2.14 Illustration for an effective filtering of transformed signal on SHEx method

Another alternative for filtering out relative frequencies may be the use of mean calculation for the whole waveform transformed to rotating reference frame. Since all

the relative frequencies other than selected harmonic appear as AC signals, mean calculation may give satisfactory results. However, reference calculation may cause time delays as the mean calculation data window gets larger. Moving windows may improve the calculation delays and accuracy if the moving window size is selected as the integer multiple of all the relative harmonic frequencies. However, this is not applicable for this specific harmonic load content since it contains lots of interharmonics which are not integer multiple of each other.
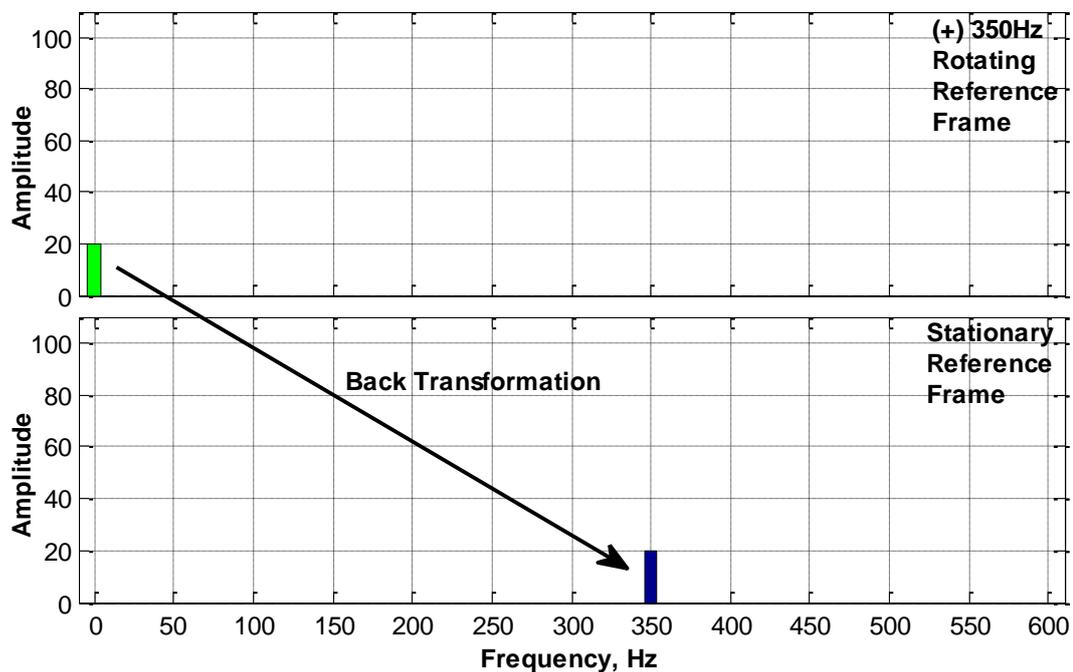
Figure 2.15 Illustration for the back-transformation on SHEx method

After effectively filtering all the other relative frequencies, the resultant signal should be back-transformed to get exactly the same form of the selected frequency as before applying the SHEx method. Illustration of the effect of back-transformation is given in Figure 2.15 again on the example signal introduced in Figure 2.13. The application of SHEx method on the system under investigation is given as the block diagram in Figure 2.16. Selected harmonic frequencies are converted to rotating reference frames

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using SRF technique mentioned earlier, properly filtered, back-transformed to alpha beta domain and finally ready for extraction from the converter reference signal as shown in Figure 2.16. By this way, HAPF converter never generates the 23rd and 25th characteristic harmonic current references.
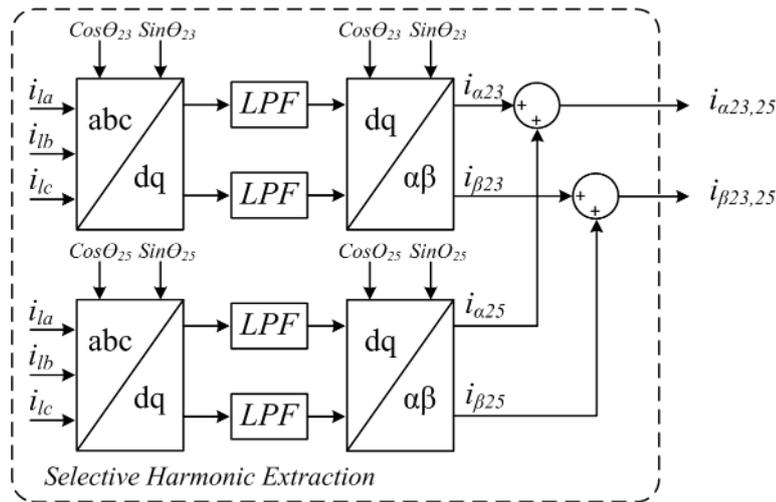
Figure 2.16 Block diagram representation of SHEx method

2.2.4. Control and Waveform Modulation Methods

Generated reference currents should be used for the modulation of output voltages and currents in order to realize the intended waveform for the HAPF converter. The HAPF converter implemented for this particular study can only modulate the output voltage due to its VSC topology. By this way, a modulated voltage waveform appears at the output terminals of the converter and it is eventually converted to current on the impedance of input LC filter due to the voltage drop between source ($v_{sa\text{-}n}$, $v_{sb\text{-}n}$, $v_{sc\text{-}n}$) and converter voltages ($v_{fa\text{-}n}$, $v_{fb\text{-}n}$, $v_{fc\text{-}n}$). It is essential to note that voltage-to-current magnitude and phase transfer functions of each harmonic component differ from each other due to the fact that input LC filter together with coupling transformer has an impedance characteristics over the whole frequency spectrum. The single phase equivalent circuit with nine parallel HAPF modules and a sample impedance

characteristics for dominant harmonic frequencies are given in Figure 2.17 and Figure 2.18, respectively.
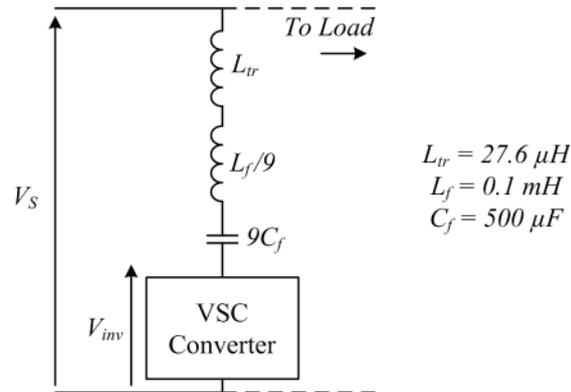
Figure 2.17 Single phase equivalent circuit with 9 parallel HAPF units
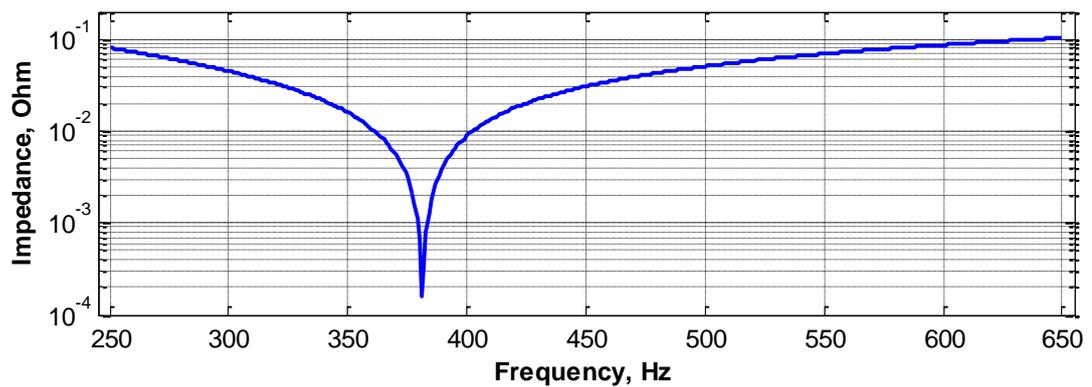
Figure 2.18 Impedance characteristics of the LC filter together with the coupling transformer

A widely used conventional control method, namely Proportional Control or K control, has been introduced for the HAPF converters [20], [70], [76], [86], [87], [104]-[106]. This method is based on the generation of the converter voltage as the multiplication of source current with a proportionality constant. The HAPF converter under investigation has already been implemented using the conventional control

method [20], and it has observed that the control method does not effectively suppress some harmonic components. Therefore, an HBC methodology is proposed in this research work for a better reference tracking performance. Both conventional and proposed methods are explained in detail for the following parts.

2.2.4.1. Proportional Control as a Conventional Control Method

Proportional control is a widely used control method for active filtering equipment as well as HAPF systems [20], [70], [76], [86], [87], [104]-[106]. The simplified block diagram showing the components of proportional control is given in Figure 2.19. Measured source currents are converted to SRF domain, rotating at fundamental frequency, and its dc component is extracted from the d and q components in order to extract the fundamental component from the reference signal. Before applying back transformation, 23rd and 25th characteristic components are also extracted from the reference. The resultant reference signal is back-transformed to instantaneous current form and multiplied by a proportionality constant K to generate harmonic voltage references. Note that the dc link regulation method is not shown in Figure 2.19 for the sake of simplicity. Finally, the voltage references are compared with a carrier signal as a Sinusoidal PWM technique in order to realize it on the converter hardware.
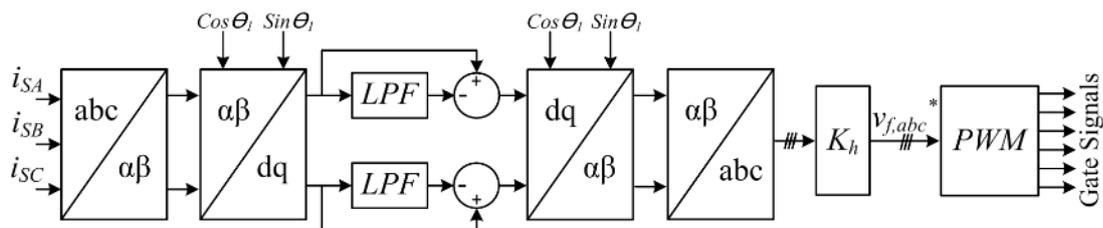
Figure 2.19 Simplified block diagram of the proportional control method

A converter making use of proportional control strategy can be considered as a current-controlled voltage source since the voltage is directly proportional to the source harmonic current with a proportionality constant K as illustrated in Figure

2.20.a. As the converter ideally does not generate fundamental component voltage, except a small amount for dc link regulation, it can be modelled as a short circuit at fundamental frequency. Thus, the equivalent circuit at fundamental frequency turns out to be as given in Figure 2.20.b.
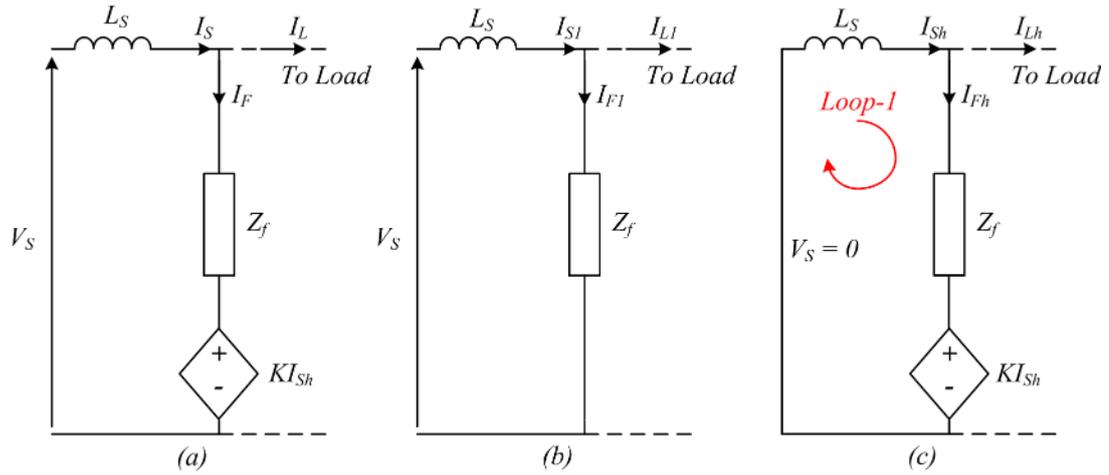
Figure 2.20 Representations of the control system on a) single phase, b) fundamental frequency, and c) harmonic equivalent circuits

On the other hand, the converter behaves as a current-controlled voltage source, while an ideal grid as a short circuit for the other harmonic frequencies. The equivalent circuit representation for the harmonic frequencies is illustrated in Figure 2.20.c. For the *Loop-1* of harmonic equivalent circuit, (2.5) can be written using Kirchoff's Voltage Law (KVL).

$$V_S = I_{Sh}L_S + Z_F I_{Fh} + KI_{Sh} \tag{2.5}$$

where V_S is the source voltage vector, I_{Sh} the source current vector, I_{Fh} the filter current vector, Z_F the filter impedance vector, L_S the source impedance vector, and K the proportional control constant.

By re-arranging the (2.5), (2.6) can be deduced.

$$V_S = (K + L_S)I_{Sh} + Z_F I_{Fh} \qquad (2.6)$$

Equation (2.6) can also be considered as the KVL equation of the *Loop-2* in Figure 2.21. As can be deduced from the illustration in Figure 2.21, proportional control method behaves as if it puts a virtual resistance to the source side of the equivalent circuit. By this way, the load current harmonics eventually shared between source and filter side branches depending on the distribution of impedances. Please note that since filter branch contains an LC filter, its impedance is almost zero at resonance frequency and increases as the frequency gets apart from resonance frequency as illustrated in Figure 2.18. Therefore, the filtering performance is expected to reduce for the harmonic and interharmonic frequencies far from the resonance frequency. Increasing proportionality constant *K* may improve the filtering performance but it is at the expense of losing transient stability [105]. In order to enhance the filtering performance of the HAPF system and provide an effective current tracking together with a better transient stability, Hysteresis Band Current Control method is proposed and implemented in this thesis.
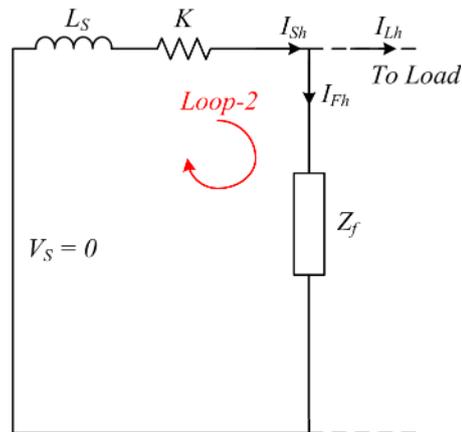
Figure 2.21 Circuit representation for the mathematical model of proportional control algorithm

2.2.4.2.　　　　Proposed Hysteresis Band Control Method

Hysteresis band control is a waveform modulation method allowing the control system to track a current reference; even though, the inverter is VSC type. Reference current tracking is handled for each phase individually via turning on the upper or lower switch of a converter leg corresponding to each phase. In order to limit the switching frequency, a hysteresis band width is defined for current reference so that the necessary acts can be applied when instantaneous current passes the bands in any direction. The illustration showing the hysteresis band control method and current paths corresponding to switching states for both positive and negative current directions are given in Figure 2.22. $S_X = 1$ in Figure 2.22, means that the IGBT on the upper half of the leg, corresponding to phase x, is turned on while the one in lower half is turned off. Similarly, $S_X = 0$ means that the IGBT on the lower half of the leg, corresponding to phase x, is turned on while the one in upper half is turned off.
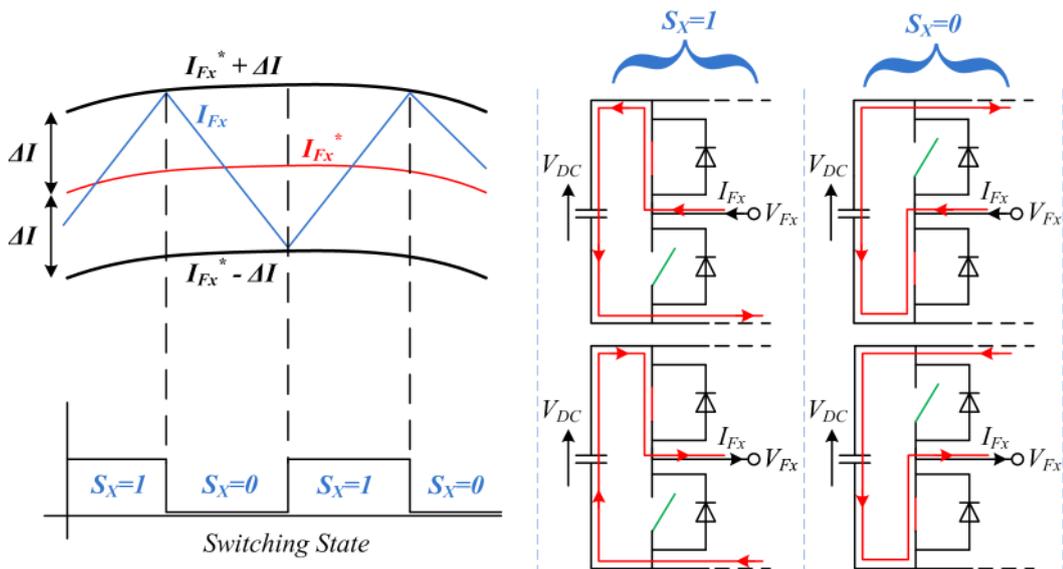
Figure 2.22 Hysteresis band control illustration and current paths for switching states

Hysteresis Band Control method has been widely used for power electronics converters due to its basic theory and easy implementation [19], [72], [87], [89], [91], [107]-[121]. Various researchers have implemented hysteresis band control for motor drive [108]-[111], APF [72], [112]-[118], HAPF [19], [89], [91], DVR [119], static compensator [120]-[121], and general VSC [122]-[124] applications. Different than other implementations, hysteresis band control of HAPF system is implemented in this thesis work for the suppression of time varying harmonics and interharmonics of IMF load for the first time in literature.
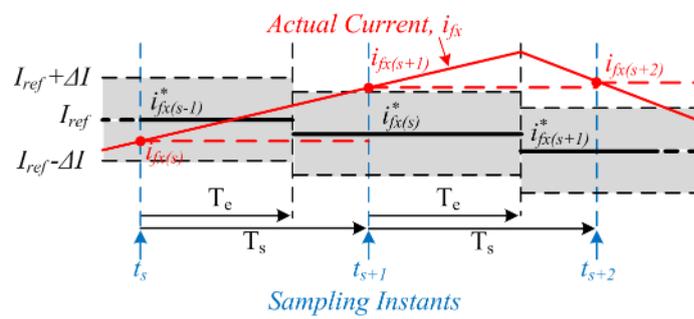
Figure 2.23 Illustration for the digital implementation of hysteresis switching

Hysteresis band control, generally, has been implemented via analog circuitries [114]. However, some applications including this research work have implemented the hysteresis band control via digital controllers [125]. Due to the restrictions of the digital implementation such as execution time and sampling frequency, some tracking errors may arise. The HBC method illustration considering the digital implementation is given in Figure 2.23, however, the effect of both sampling frequency and execution time on hysteresis band control is focused on in detail on Chapter 5. In Figure 2.23, $\ldots t_s,\ t_{s+1},\ t_{s+2}\ldots$ are the sampling instants, T_s the fixed sampling period, T_e the execution time, i_{fx} the actual current in analog form in phase x of each HAPF unit, $i_{fx(s)}$ the digitized actual current sampled at t_s, and $i_{fx}^*{}_{(s)}$ the reference value of the HAPF current calculated in T_e just after t_s from the samples collected at t_s. Furthermore, HBC allows strict current tracking without any significant phase error, which provides better

utilization of active filtering equipment. On the other hand, it causes high switching losses in order to reach good current tracking [89], [120]-[126]. The switching frequency is not constant, it is indeed distributed at high frequencies [89], [120]-[126]. Some researchers have already conducted research to solve these problems [109]-[111], [114], [119], [126]-[128].

Hysteresis band control is an analog based method; thus, some problems may arise for the digital implementation of it. Moreover, if the converter is three-phase three-wire converter, the instantaneous values of each phase interfere the dynamic switching behavior of others. The most important drawback is obviously high switching loss. An adaptive fuzzy hysteresis band based modification has already been conducted in this thesis in order to reduce the switching losses without a significant reduction in performance and it is given on Chapter 5. In addition to those disadvantages, there have been observed during the field tests that hysteresis band controlled HAPF converter generates high frequency current harmonics unlike traditional voltage control methods. The observed high frequency currents cause an overheating on the iron core filter reactor although the rms and peak values of filter current is less than proportional control. Table 2.1 summarizes the advantages and disadvantages of HBC as a HAPF system control method.

Table 2.1 Advantages and disadvantages of hysteresis band control method

Advantages	Disadvantages
Basic theory	High switching losses
Easy implementation	Digital implementation problems
Good transient stability	Variable switching frequency
Better current protection	Phase interaction for three-phase three-wire converters
Better filtering performance for active filtering equipment	High frequency current components in converter current
Better reference tracking	

The block diagram representation of the proposed control system is given in Figure 2.24. The control system creates the reference current signals using PLL signal generation, interharmonic and harmonic current reference generation, selective

harmonic extraction, and dc link regulation parts. After creating the reference currents, hysteresis band controller in Figure 2.17 modulates the inverter output waveform by creating proper IGBT gate pulses. PLL generation and selective harmonic extraction parts of the control system has already been explained in previous parts, however, interharmonic and harmonic current reference generation part is still needed to be clarified.

The harmonic and interharmonic currents are based on the operation regime of overall load system. Since there are lots of load feeders in the steel melting facility, total load currents (I_{LA}, I_{LB}, I_{LC}) are obtained by subtracting filter currents (I_{FA}, I_{FB}, I_{FC}) from the source currents (I_{SA}, I_{SB}, I_{SC}), both measured at MV level. Since the HAPF converter is physically connected to Low Voltage (LV) bus (690V), the current reference should also be referred to LV side so that the actual filter currents will be in correct phase and magnitude after transformed to MV side. By this way, a transformer conversion is applied to the load currents and they are transformed to LV side as given in Figure 2.24. An important feature of transformer conversion is that it creates proper phase shifts needed for Δ/Y transformer for both positive and negative-sequence current components.

If the signal were just converted using turns-ratio multiplication and constant phase shift, the reference would be wrong because positive-sequence harmonics shifted 30 degrees in positive direction while negative-sequence-harmonic components in negative-direction.

23rd and 25th harmonic components are extracted from the load current signal in αβ domain using SHEx method after transformer conversion. Then an SRF is generated at fundamental frequency to eliminate the fundamental component of the load current as illustrated in Figure 2.24 in order not to generate reference signals in fundamental frequency. After that the resultant signal is multiplied with a suppression gain for satisfactorily suppressing the interharmonic and harmonic components instead of totally eliminating them. G in Figure 2.24 is a real number between 0 and 1, by this way, HAPF capacity can be adjusted such that each individual harmonic and THD at

source current waveform stays within allowed limits. Further mitigation of harmonics and thus reducing the THD more than recommended in standards [1], [28], [30] is not necessary and economical.

In addition to harmonic and interharmonic components of load current, a direct-axis current component for dc link regulation and a quadrature-axis current component for eliminating fundamental frequency voltage reference should also be added to reference.

If eventually converter do not generate voltage component at fundamental frequency except a negligible amount for dc link regulation, there will be an inevitable fundamental current component due to the impedance of input LC filter given in (2.7), which is expected and explained in detail in Chapter 3. Therefore, this expected current component should be added to reference, otherwise, hysteresis controller will generate fundamental voltage in order to eliminate fundamental current. It should also be noted that current signal due to LC filter is added to quadrature-axis component of the reference since it is obviously a reactive current due to reactive impedance. However, the current component due to dc link regulation is added to direct-axis component of the reference since it should be an active current, allowing bi-directional transfer of active power to regulate dc link voltage.

$$j2\pi f_1 L_F + \frac{1}{j2\pi f_1 C_F} \qquad (2.7)$$

where, f_1 is the fundamental frequency, L_F the filter inductance and C_F the filter capacitance.

The resultant signal after adding all the necessary components is finally back-transformed to stationary reference frame (*abc* domain) and converted to gate signals via hysteresis band controller. In the following section, the mathematical model of hysteresis band controller is developed for the implementation on three-phase three-wire two-level HAPF converters in order to understand the dynamics of waveform modulation.
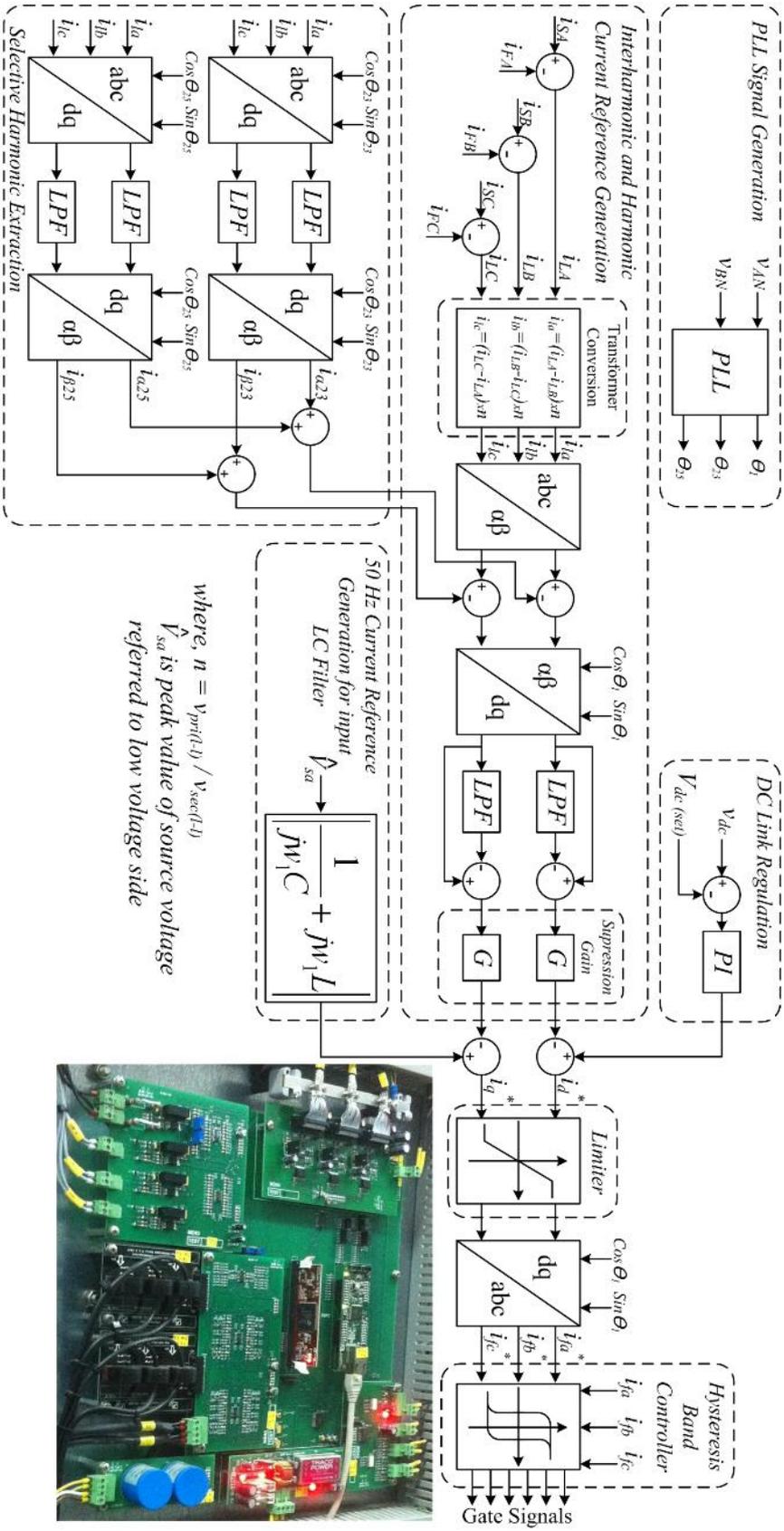
Figure 2.24 Block diagram representation of the proposed hysteresis current control method

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2.2.4.2.1. Mathematical Modelling of Hysteresis Band Controlled HAPF

In this thesis, a fixed hysteresis band structure has been used for the implementation of hysteresis band control. The fixed hysteresis bandwidth has been defined for the reference signal and associated acts have been applied when instantaneous values of phase currents passes the thresholds according to the criteria given in Table 2.2 using the terminology of digital implementation in Figure 2.23. Switching states S_a, S_b and S_c for phases a, b and c are determined by the comparison of digitized actual phase currents sampled at instant t_s ($i_{fa(s)}$, $i_{fb(s)}$, $i_{fc(s)}$) with the calculated current references inside a hysteresis band ($i_{fa}^{*}{}_{(s)} \pm \Delta I$, $i_{fb}^{*}{}_{(s)} \pm \Delta I$, $i_{fc}^{*}{}_{(s)} \pm \Delta I$) using the samples collected at t_s during execution time T_e. Since HAPF converter under investigation is a three-phase three-wire converter, there are three IGBT legs representing each phase. Thus, there are eight (2^3=8) possible switching schemes in a form of $S_a S_b S_c$, which are *000*, *001*, *010*, *011*, *100*, *101*, *110*, *111*. The corresponding simplified equivalent circuits for each switching schemes are shown in Table 2.3.

Table 2.2 Switching criteria for hysteresis band control

Hysteresis Switching Criteria	
If $i_{fx(s)} > i_{fx}^{*}{}_{(s)} + \Delta I$	then $S_X = 1$
If $i_{fx(s)} < i_{fx}^{*}{}_{(s)} - \Delta I$	then $S_X = 0$
If $i_{fx}^{*}{}_{(s)} - \Delta I < i_{fx(s)} < i_{fx}^{*}{}_{(s)} + \Delta I$	then do not change the previous switching pattern
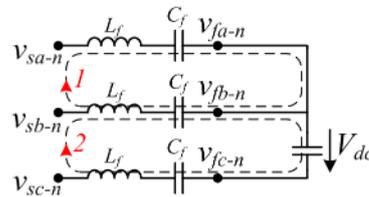
Figure 2.25 Equivalent circuit for switching scheme "001"

Table 2.3 List of hysteresis switching schemes and their corresponding equivalent circuits

Switching Scheme	Equivalent Circuit
000 - 111	
001	
010	
011	
100	
101	
110	

Each switching scheme has unique voltage values for the terminals ($v_{fa\text{-}n}$, $v_{fb\text{-}n}$, $v_{fc\text{-}n}$) of the HAPF converter. Voltage derivations for an example switching scheme, "001", is derived in this section, while the other derivations are given in Appendix A. To formulate the behavior of the switching scheme "001", the equivalent circuit given in Figure 2.25 is solved using the KVL equations of loop-1 and -2 as (2.8) and (2.9) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \tag{2.8}$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} - v_{dc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \qquad (2.9)$$

where, v_{Coa}, v_{Cob} and v_{Coc} are the initial voltage values across the series filter capacitor C_f for each phase, and n represents the virtual neutral point which can be considered as the neutral point of the coupling transformer secondary.

Balanced system constraints for three-phase three-wire converter can be written as (2.10) and (2.11).

$$i_{fa} + i_{fb} + i_{fc} = 0 \qquad (2.10)$$

$$v_{sa-n} + v_{sb-n} + v_{sc-n} = 0 \qquad (2.11)$$

HAPF converter voltages v_{fa-n}, v_{fb-n} and v_{fc-n} can be expressed via coupling transformer secondary voltages v_{sa-n}, v_{sb-n} and v_{sc-n} as given respectively in (2.12) – (2.14).

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} = v_{fa-n} \qquad (2.12)$$

$$v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} = v_{fb-n} \qquad (2.13)$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} = v_{fc-n} \qquad (2.14)$$

Eqn. (2.15) can be obtained by making use of (2.8) – (2.11).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3\int i_{fb}dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} - v_{dc} = 0 \qquad (2.15)$$

Substitution of (2.13) into (2.15) gives (2.16). Then (2.17) is obtained by rearranging (2.16).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} - v_{dc} = 0 \qquad (2.16)$$

$$v_{fb-n} = -\frac{v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \qquad (2.17)$$

In order to find a relation for the sum of cumulative initial voltages across the capacitors of each phase, (2.18) is derived by summing up (2.12), (2.13), (2.14) and using (2.11).

$$v_{Coa} + v_{Cob} + v_{Coc} = -(v_{fa-n} + v_{fb-n} + v_{fc-n}) \qquad (2.18)$$
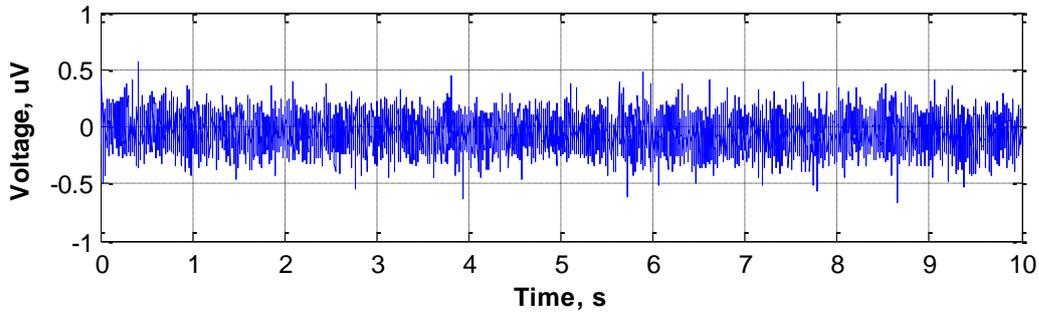
Figure 2.26 Sum of converter terminal voltages for normal operation (simulation results)
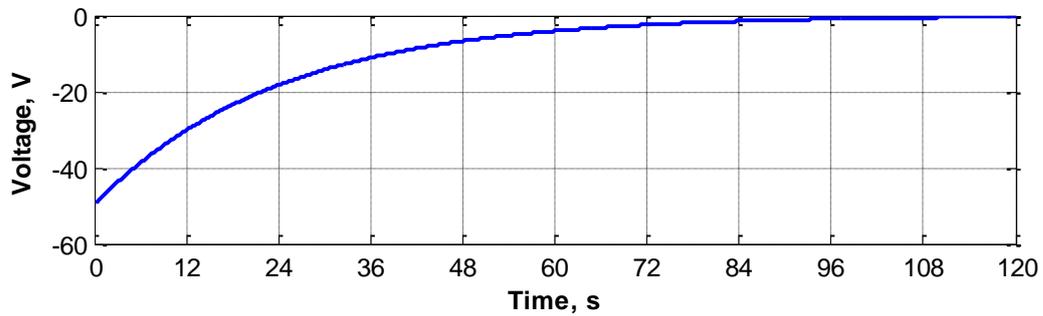
Figure 2.27 Sum of converter terminal voltages in the case of a fault (simulation results)

Sum of HAPF converter terminal voltages are assumed to be zero unless there is a common mode noise or initial voltage on one of the filter capacitors at start-up. This assumption can be proved by using the PSCAD simulation showing the sum of converter terminal voltages in Figure 2.26. As can be seen in Figure 2.26, the sum of converter terminal voltages is negligible during HAPF system normal operation. On the other hand, if there is a common mode noise in the system or filter capacitors of one phase starts with an initial voltage, the sum of HAPF converter terminal voltages can be different than zero. For rapidly decreasing the common mode effects, discharge resistors are connected in parallel with each filter capacitor on proposed HAPF converters. The effect of discharge resistors on the sum of HAPF converter terminal voltages with an unexpected initial voltage condition of one of the capacitors is simulated on PSCAD and the result is given in Figure 2.27. As can be deduced from Figure 2.26 and Figure 2.27, sum of HAPF converter terminal voltages can be assumed as zero ($v_{fa-n} + v_{fb-n} + v_{fc-n} = 0$). For this reason, right hand side of (2.18) can be neglected, thus (2.18) can be reduced to (2.19).

$$v_{fb-n} = -\frac{v_{dc}}{3} \qquad (2.19)$$

Since $v_{fa-n} = v_{fb-n}$ and $v_{fc-n} = v_{fb-n} + v_{dc}$ by inspection on equivalent circuit in Figure 2.25, (2.20) and (2.21) can be directly obtained from (2.19).

$$v_{fa-n} = -\frac{v_{dc}}{3} \qquad (2.20)$$

$$v_{fc-n} = +\frac{2v_{dc}}{3} \qquad (2.21)$$

Applying the same derivation to other switching schemes, given in Appendix A, eventually yields the phase voltage values in Table 2.4 with respect to virtual neutral point for all of the switching schemes. As can be understood from Table 2.4, terminal voltage of a phase is strongly dependent on the states of other phases since the converter topology is three-phase three-wire VSC. For example, the voltage value of phase a, v_{fa-n}, at $S_a = 1$ is $2V_{dc}/3$ when the states of both phase b and c are zero, $V_{dc}/3$

when the state of only one of the phase *b* and *c* are one, and *0* when states of both phase *b* and *c* are one. Figure 2.28 illustrates a piece of simulation for verifying the voltage values given in Table 2.4.

Table 2.4 Phase voltages of each HAPF converter with respect to virtual neutral point for all switching schemes

Switching Scheme	V_{fa-n}	V_{fb-n}	V_{fc-n}
000 – 111	*0*	*0*	*0*
001	$-V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
010	$-V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$
011	$-2V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$
100	$2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
101	$V_{dc}/3$	$-2V_{dc}/3$	$V_{dc}/3$
110	$V_{dc}/3$	$V_{dc}/3$	$-2V_{dc}/3$
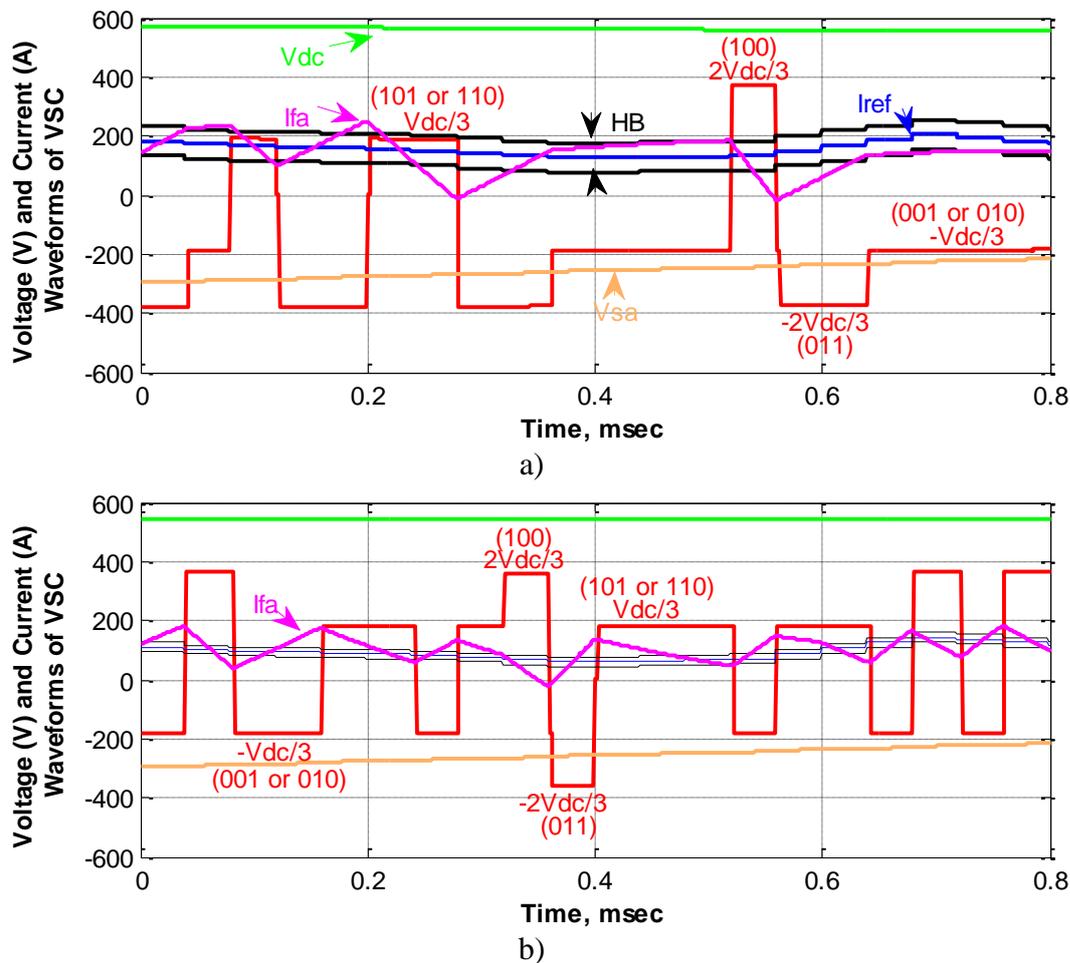
Figure 2.28 Simulation waveforms illustrating the converter voltage levels for a) wide and b) narrow hysteresis band

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In addition to analyzing the terminal voltages, the formulation for the converter currents is also needed for proper modeling of the hysteresis band control of HAPF system. In order to reach this aim, simplified single phase equivalent circuit in Figure 2.29.a should be solved for each phase individually with (2.22).

$$-v_{fx-n} + \frac{1}{C_f}\int i_{fx}dt + v_{Cox} + L_f\frac{di_{fx}}{dt} + v_{sx-n} = 0 \tag{2.22}$$

where, v_{Cox} is the initial instantaneous capacitor voltage for phase x.
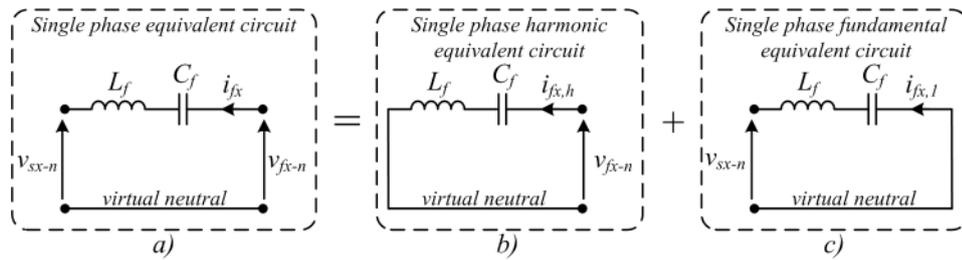
Figure 2.29 Single phase equivalent circuit representation of HAPF system for each phase with respect to virtual ground

HAPF converter input LC filter is designed such that the capacitor of the filter carries almost all of the fundamental frequency voltage due to the impedance characteristics of the filter. Thus, for the sake of simplicity, source voltage is assumed to be blocked on the filter capacitor (blocking capacitor assumption) yielding (2.23) and (2.24), since converter is not designed to generate fundamental component voltage at steady state except a negligible amount for dc link regulation. Equation (2.23) is the mathematical formulation of fundamental frequency equivalent circuit illustrated in Figure 2.29.c.

$$v_{sx-n} = \frac{1}{C_f}\int i_{fx,1}dt + v_{Cox,1} \tag{2.23}$$

$$L_f\frac{di_{fx,1}}{dt} \sim 0 \quad (negligible) \tag{2.24}$$

where $i_{fx,1}$ is the fundamental component of the line current of phase x and $v_{Cox,1}$ is the fundamental component of the initial voltage drop of the filter capacitor.

When (2.23) and (2.24) are considered, (2.22) can be reduced to (2.25), which also represents the dynamic behavior of harmonic equivalent circuit in Figure 2.29.b.

$$\frac{1}{C_f}\int i_{fx,h}dt + v_{Cox,h} + L_f \frac{di_{fx,h}}{dt} = v_{fx-n} \tag{2.25}$$

where $i_{fx,h}$ is the harmonic component of the line current of phase x and $v_{Cox,h}$ is the harmonic component of the initial voltage drop of the filter capacitor.

Equation (2.25) shows that the harmonic currents are the outcome of only applied converter voltages with respect to virtual ground. Changing switching schemes according to the criteria in Table 2.2, corresponds to different converter voltages given in Table 2.4. Those converter voltages yield a dynamic current behavior represented by the differential equation in (2.25).

In addition to the mathematical representation of the dynamic current behavior, the hysteresis band width is also important for understanding the content of the HAPF current. Since hysteresis band represents the allowed limits of the actual current with respect to intended reference current, the tracking error increases as the hysteresis band width is increased. Narrowing the hysteresis band provides better tracking performance at the expense of higher switching frequency and thus higher switching losses as illustrated on the simulation results given in Figure 2.28. Narrowing the band, indeed, provides better tracking performance up to a limit dictated by the digital implementation of hysteresis band control. Due to some problems of the digital implementation of hysteresis band control, bandwidth and the tracking performance is not linearly proportional to each other, the reason of which is thoroughly analyzed in Chapter 5.

CHAPTER 3

DESIGN OF CIRCUIT PARAMETERS FOR HAPF CONVERTER

HAPF system can be divided into two parts, the first part is the active part formed by inverter and the other is the passive part composed of input LC filter. Components to be designed for active part are installed capacity, semiconductor currents, dc link voltage, cooling requirements etc, while resonance frequency, w_o, reactive power support, filter inductor, L_f, and filter capacitor, C_f, for the passive part. Some parameters can be determined via theoretical calculations considering the load characteristics; however, some others may require simulations. For this reason, it is vital to analyze the load characteristics before starting the design procedure. In this chapter, steel melting facility load together with the IMF installations is investigated based on the field measurements. In addition, design of input LC filter parameters is explained in detail. Finally, a simulation environment is formed with the designed LC filter for tuning the control system and observing the effect of inverter parameters.

3.1. Harmonic Content of the Load Analyzed from the Field Measurements

Harmonic problems and sample harmonic spectrum for a single IMF installation has already been given in introduction part of the thesis. However, the steel melting facility under investigation contains three randomly operating IMF installations together with some other industrial loads. In order to observe the overall harmonic behavior of steel melting facility load, Class A type field measurements [100] were conducted for a time interval during which all the three IMF installations are available

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for normal operation. The raw data is post-processed via Fast Fourier Transform (FFT) with 200 msec windows in order to get a harmonic spectrum of 5 Hz resolution as given in Figure 3.1. As can be seen from Figure 3.1, the prominent harmonics and interharmonics are located between 250 and 550 Hz for almost all frequencies. It is observed that two, four and six prominent interharmonics are observed simultaneously and their frequencies are changing irregularly in time while one, two and three IMF installations are in operation, respectively. In addition to those prominent harmonics and interharmonics, 11th and 13th characteristic harmonics due to 12-pulse, and 23rd and 25th characteristic harmonics due to both 12- and 24-pulse structures of the load resonant IMF converters can also be observed.
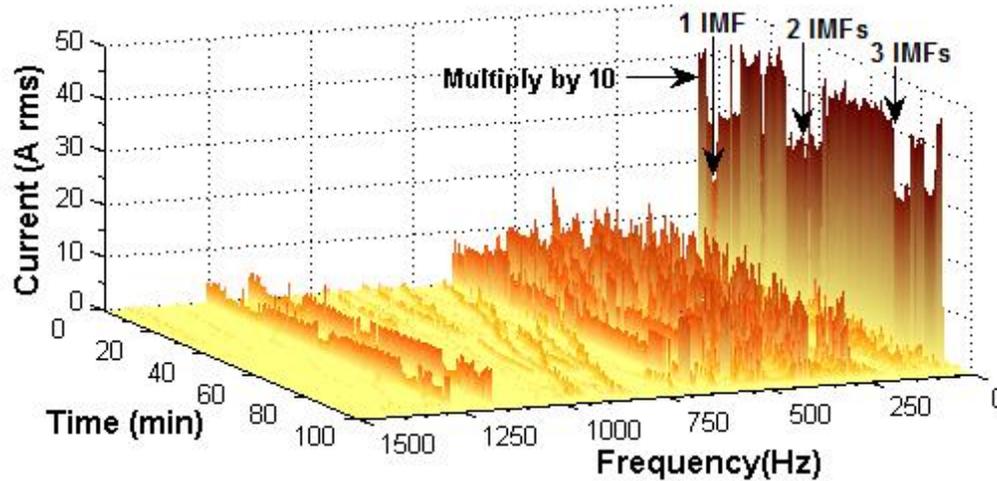
Figure 3.1 Frequency spectrum of interharmonics and harmonics of the line current waveforms for the steel melting facility containing three IMFs (field measurements)

Furthermore, as mentioned before, those harmonics and interharmonics may appear as negative sequence, positive sequence or both sequences at the same time. Since Figure 3.1 is not suitable to illustrate the symmetrical components for each individual harmonic frequencies, symmetrical components analysis is also conducted for each harmonic and interharmonic frequency from 250 Hz to 550 Hz with 5 Hz steps. Mentioned analysis is given in Appendix B in detail. The following findings are obtained from the results of symmetrical components analysis:

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i) Harmonic and interharmonic frequencies from 250 to 355 Hz, except 7th harmonic, appear only in negative sequence form,

ii) Harmonic and interharmonic frequencies from 440 to 545 Hz appear only in positive sequence form,

iii) Harmonic and interharmonic frequencies between 360 and 435 Hz and 7th harmonic may appear only positive sequence, only negative sequence or both at the same time,

iv) 11th, 13th, 23rd and 25th characteristic harmonics appear as expected [19], [20], [26] that 11th and 23rd are only negative while 13th and 25th harmonics are only positive sequence.

3.2. Design of Input LC Filter

Input LC filter, together with the coupling transformer, behaves as a transfer impedance to convert inverter terminal voltages to HAPF system line currents. The design parameters for input LC filter are filter inductance, L_f, filter capacitance, C_f, and natural frequency, w_o. Design criteria for those parameters is mentioned in the following sections.

3.2.1. Natural Frequency Determination

Since prominent harmonic and interharmonic frequencies lay between 250 and 550 Hz, it is vital to keep impedance characteristics as minimum value as possible over this frequency range so that required interharmonic and harmonic currents can be generated with a lowest possible voltage drop and phase difference. For this reason, natural frequency of the input LC filter is chosen to be 385 Hz for nine parallel operating HAPF units. The chosen value determined as a bit smaller value than the 400Hz, midway between 250 and 550 Hz. The reason for choosing natural frequency closer to lower boundary, 250 Hz, instead of higher boundary, 550 Hz, is that the impedance characteristics rapidly increases for the frequencies lower than natural frequency. By choosing 385 Hz as the natural frequency, the LC filter impedances of

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both 250 Hz and 550 Hz are made close to each other for nine parallel units, as can be observed in Figure 3.2.

An important point for natural frequency determination of input LC filter is that natural frequency increases as the number of HAPF units in operation decreases as given in Figure 3.2, which causes higher voltage drops for low frequencies on input filter than the nine HAPF unit case. Actually, this situation does not arise a decrease in filtering performance for hysteresis band control, unlike proportional control, but it causes an increase in the need of minimum dc link requirement for the inverter in order to suppress the same load characteristics as nine HAPF unit case. On the other hand, proportional control is highly fragile for changes in the number of parallel HAPF units. The filtering performance dramatically decreases for the low frequencies as natural frequency moves toward higher values, since proportional control method is highly dependent on the filter impedances as mentioned before.
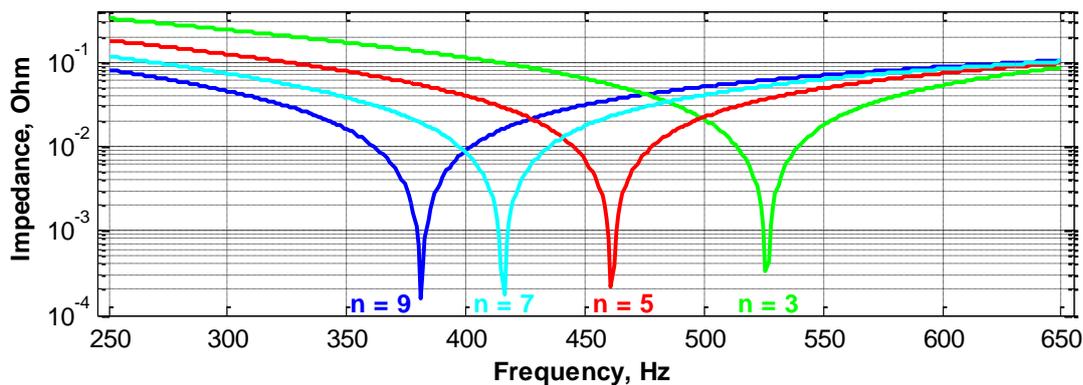
Figure 3.2 Impedance characteristics of the input LC filter with different number of parallel HAPF unit

3.2.2. Reactive Power Support and Minimum DC link Requirement

Determination of only natural frequency, solely, is not enough for designing input LC filter because there are infinitely many number of L-C pairs satisfying a specific natural frequency, $w_o=\sqrt{LC}$. Figure 3.3 illustrates the impedance characteristics curves

of different $L = L_{tr} + L_f$ (filter inductor together with coupling transformer) and corresponding C_f values for the same natural frequency. It is obvious in Figure 3.3 that the filter overall impedance values are increasing as the filter inductor increases. Actually, changing filter parameters, LC, affects not only the impedance characteristics but also minimum dc link voltage required for worst case operation [129, 130] and reactive power production at fundamental frequency. The basic philosophy underlying the determination of filter parameters is given as follows:

i) Minimum dc link voltage requirement for the worst case filtering operation,

ii) Fundamental component of the reactive power support due to the series LC filter.
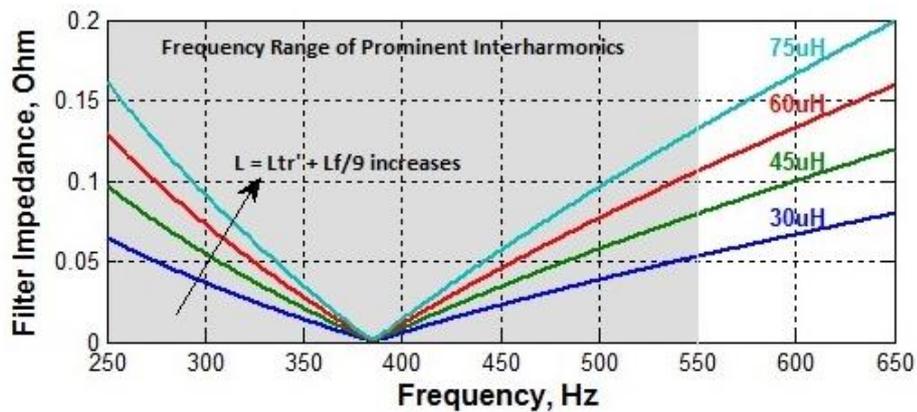
Figure 3.3 Impedance characteristics for different filter inductance values together with coupling transformer

Minimum required inverter dc link voltage can be determined as the sum of all voltage components due to the existing harmonic and interharmonic currents over the coupling impedance as if their peak values coincide [19], [129], [130]. In order to reach this aim, IMF duty regime has been observed from the field recordings and worst case condition was determined such that three IMF installations are operating at the same time with resultant interharmonic frequencies appear at highest possible coupling impedances [19]. Moreover, produced capacitive reactive power, due to the fact that filter impedance is subjected to fundamental frequency grid voltage, is also calculated

for different filter inductances. Minimum dc link voltage requirement and reactive power support are drawn on the same graph over the filter inductor together with coupling transformer as given in Figure 3.4.
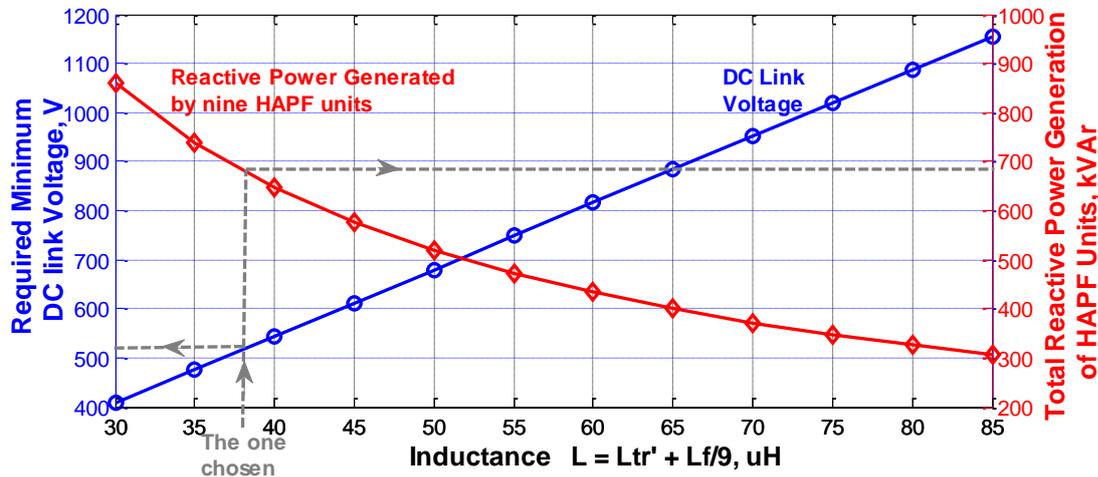
Figure 3.4 Required minimum dc link voltage and total reactive power support for filter inductances

Choosing the dc link voltage value as low as possible is very useful for reducing the voltage stress on semiconductors and switching losses. It is one of the most important feature of the HAPF topology that dc link voltage can be lower than grid voltage [19], [20], [52], [53], [129]. In order to reduce the dc link voltage, filter inductor should be decreased as can be seen from Figure 3.4, however this act, at the same time, causes a higher reactive power support thus fundamental frequency currents flowing through inverter. All the design parameters are taken into consideration and filter inductor together with the coupling transformer is chosen as 38 µH so that corresponding minimum dc link requirement is lower than 550V and total reactive power support is around 700 kVAR. The chosen value is determined considering the following concerns:

i) Total reactive power support should be around 700 kVAR for supporting the MV reactive power compensation,

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ii) Magnitude of fundamental frequency current components, conduction losses and thus semiconductor stress should be as low as possible,

iii) Minimum dc link requirement thus switching losses should be as low as possible.

Furthermore, filter inductor value is also important for hysteresis switching. Increasing filter inductor provides a reduction in the rate of change of current, di/dt. By this way, a more stable tracking performance can be obtained especially for digital implemented control systems, which is also mentioned in Chapter 5. Since dc link and reactive power support parameters are more dominant than the hysteresis tracking performance in terms of inverter capacity and efficiency, another solution is proposed in Chapter 5 for enhancing the current tracking performance.

3.3.   Simulation Model and Theoretical Results

Input LC filter parameters are designed as described in previous parts, however, design of inverter parameters needs circuit simulations in addition to theoretical results. Inverter design parameters such as a sample converter line current waveform, dc link voltage ripple, dc link current waveforms, IGBT losses etc. can be obtained using the simulation environment and those findings can be used in experimental verification.

EMTDC/PSCAD [131] simulation environment has been used for the simulation of both electrical circuit and the control algorithm. One of the most important feature of this simulation environment is that it has some structures specifically designed for power electronics applications. Moreover, EMTDC/PSCAD allows writing scripts in FORTRAN programming language in order to model the control algorithm too. Therefore, the converter components with realistic simulation models can be evaluated using the control algorithm, which allows testing the system with all the components. As another feature, EMTDC/PSCAD provides a recording system for both reading the external data as inputs and importing the simulation results to a text file.

In this thesis, the field recordings are exported to the simulation environment as a steel melting facility load instead of using artificial non-linear loads provided by the program in order to make the simulation circuit more realistic. Proposed control algorithm is also written in FORTRAN programming language as a script instead of using pre-defined power electronics control blocks provided by the simulation environment. PLL, SHEx and SRF methods together with the hysteresis switching have also been implemented in the script by modelling the sampling frequency of the hardware too.

The screenshot of the simulation environment in system level can be seen in Figure 3.5. HAPF modules 1-9 shown in this figure contains each HAPF unit with both electrical circuit and control algorithm. Screenshot of one of the identical HAPF unit blocks is also given in Figure 3.6. The HAPF system and the proposed control algorithm have been simulated and the results of the simulation model are given in this section of the thesis. There have been numerous runs for the simulation model in order to reach to the most effective design, however, only the results of finalized model is given.

Figure 3.7 shows the waveforms of source, HAPF and load current in MV level. The proposed HAPF system is shown to be very successful for the suppression of harmonics and interharmonics of the IMF load. Actually, the source current THD is decreased to 2.99% while the load current THD is 8.57%. Figure 3.7 shows also waveforms of the HAPF system before HAPF converters are turned on. The corresponding filter current waveform when the HAPF converter is turned off represents the behavior of passive part of the HAPF system. The corresponding part of the filter current waveform contains only reactive power at fundamental frequency due to input LC filter of HAPF converter. This part also contains some harmonics too, which is due to the fact that some harmonic and interharmonic current components of the IMF load naturally flow through the LC filter according to the filter impedances of corresponding frequencies.
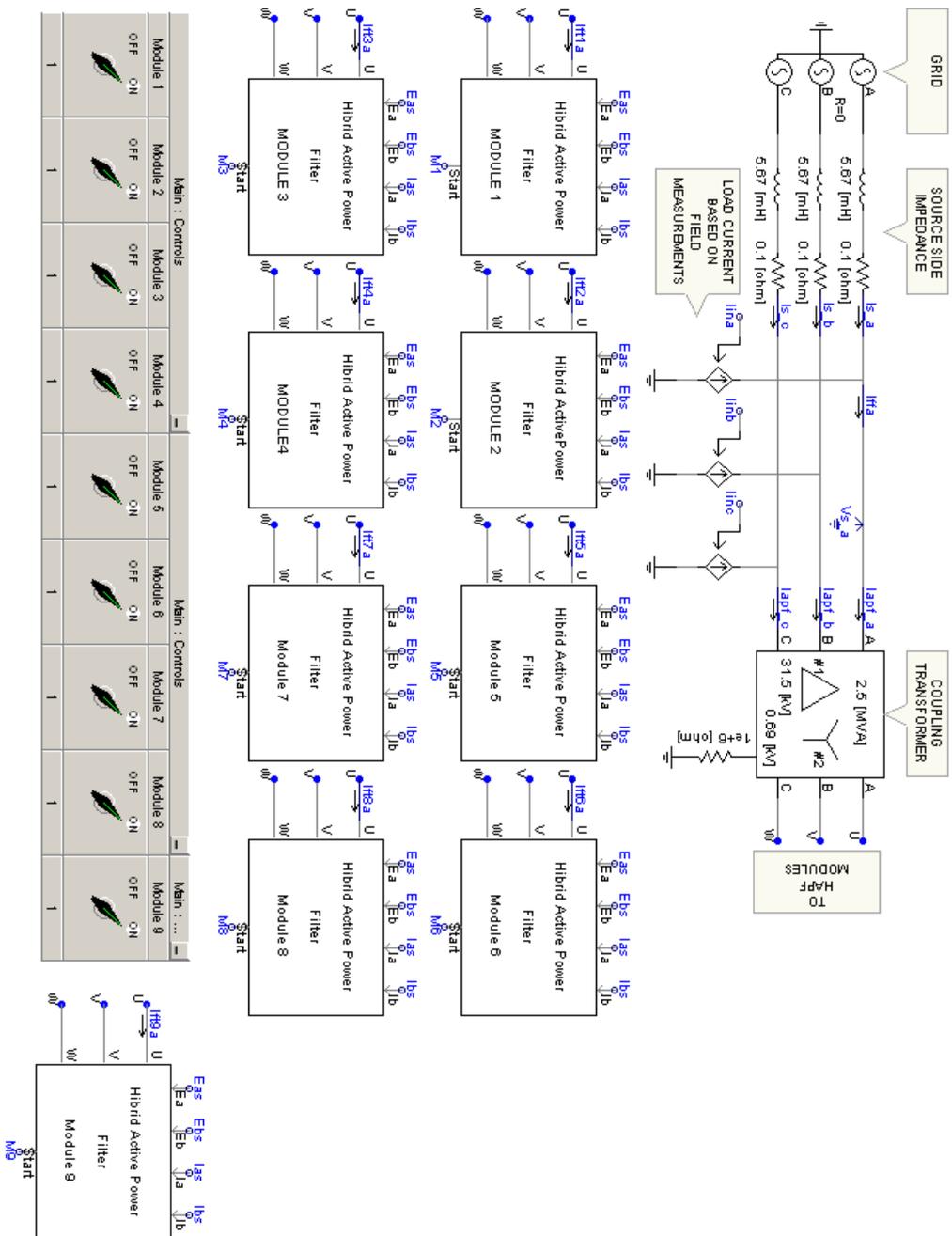
Figure 3.5 Screenshot of the simulation environment in system level
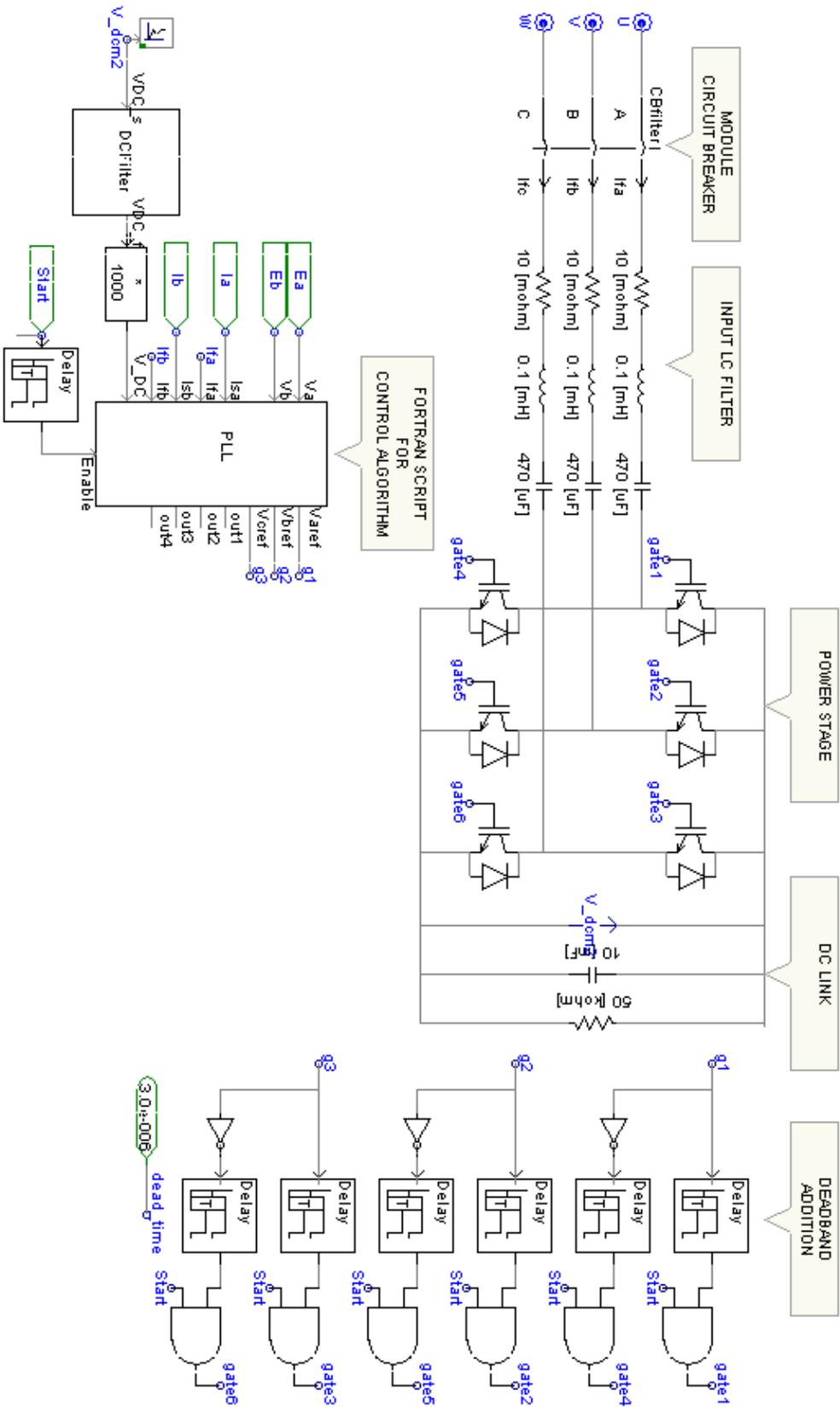
Figure 3.6 Screenshot of the simulation environment for each HAPF unit

The harmonic spectra of load, HAPF and source current waveforms given in Figure 3.7 are drawn in a common graph in Figure 3.8. Note that the proposed HAPF system model and the control system architecture effectively suppresses the interharmonics caused by the IMF load under investigation.

The dominant interharmonics for the particular instant of the load regime are 295, 355, 395, and 455Hz. The interharmonics at 295 and 395 Hz are caused by an IMF load operating at converter frequency 172.5 Hz, while the interharmonics at 355 and 455 Hz are due to another IMF installation operating at converter frequency 202.5 Hz.
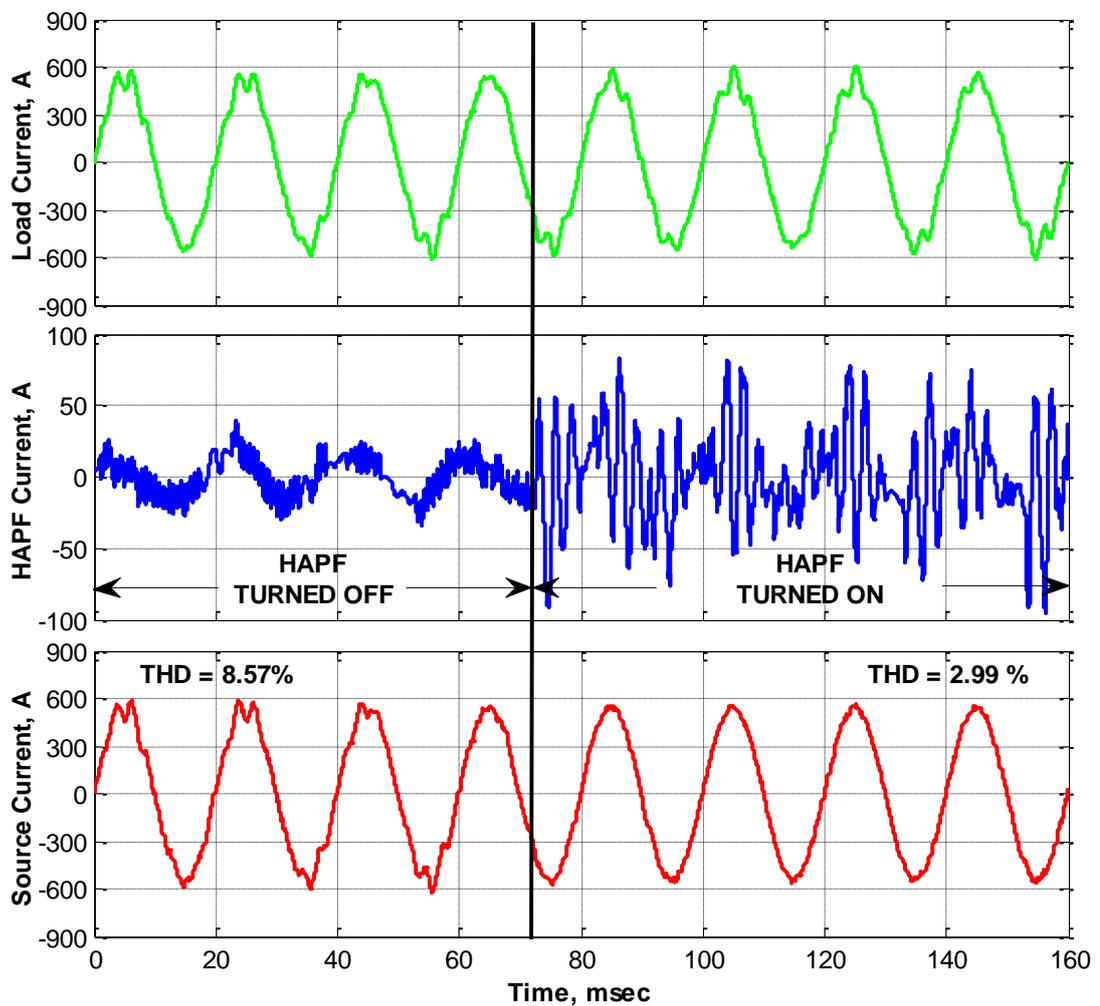
Figure 3.7 Waveforms of load, HAPF and source currents in MV level (simulation results)

In addition to MV level results, it is also important to analyze the performance of each HAPF unit in LV level too. A proper DC link voltage level should be reached before starting of harmonic suppression. For this purpose, each HAPF unit starts with short intervals of DC link build-up and DC link regulation phases. Figure 3.9 illustrates the start-up behavior of each HAPF unit. The DC link build-up phase are divided into two sections as can also be seen from Figure 3.9.
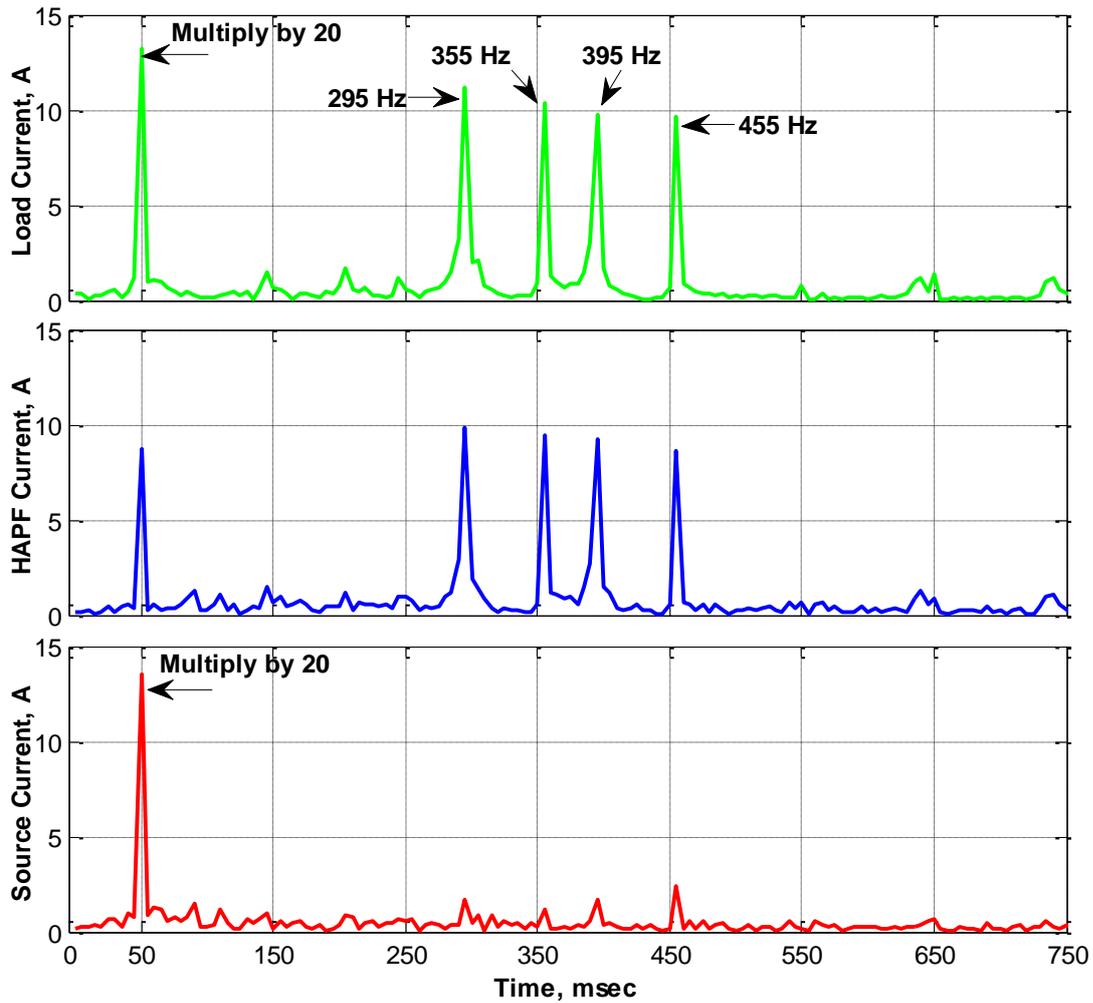
Figure 3.8 Harmonic spectrum of the load, HAPF and source current waveforms (simulation results)

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During DC link build-up, an active current reference are tracked by the hysteresis current controller in addition to the inevitable reactive current component due to input LC filter. The only difference between part1 and part2 of the DC link built-up phase is the magnitude of the active current reference. Part-1 provides a soft starting by a small active current reference in order to avoid any in-rush currents towards semiconductors, then the Part-2 follows with a higher active current reference by increasing the PI controller limits in order to accelerate the DC link build-up. Once the required DC link value is reached, the converter regulates the dc link voltage for some time without harmonic filtering as shown in Figure 3.9. Finally, the normal control algorithm operation for the suppression of load harmonic content starts, the DC link regulation behavior of which is also given in Figure 3.9.
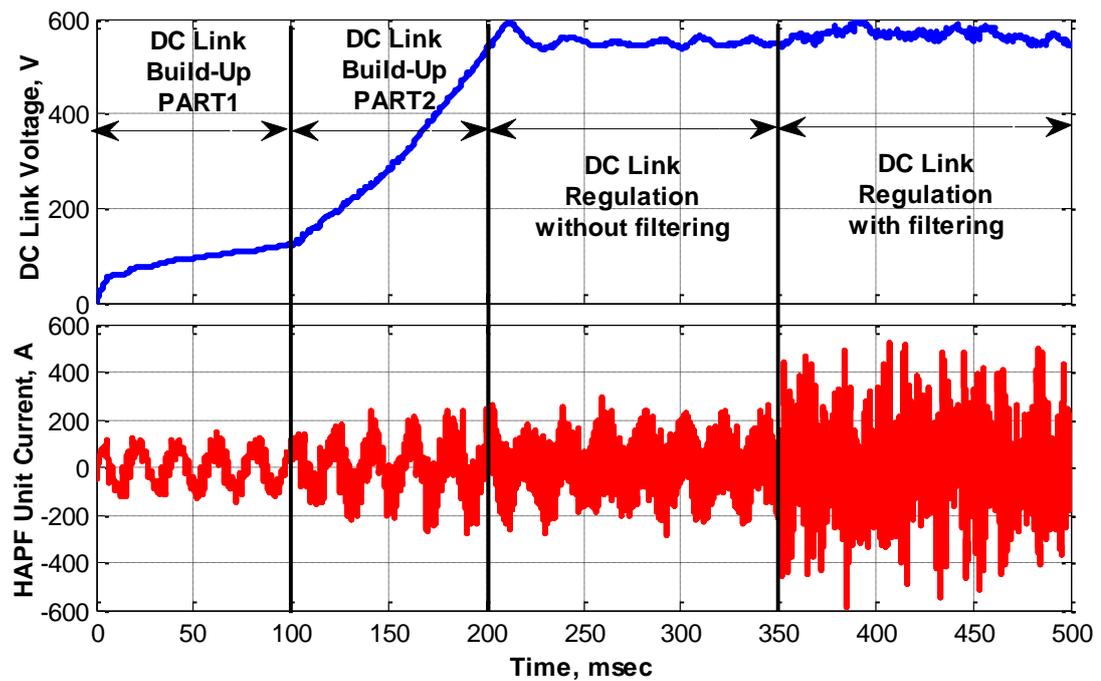
Figure 3.9 Illustration of start-up phases of each HAPF unit

The switching behavior of each HAPF unit due to the hysteresis current control philosophy is shown in the sample HAPF unit current in Figure 3.10. This figure represents the typical hysteresis switching waveform for the tracking of reference

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current signal. When the harmonic spectrum of the HAPF unit current is analyzed, the harmonic and interharmonic content of it can be deduced as given in Figure 3.11 using the FFT of the exported signal.
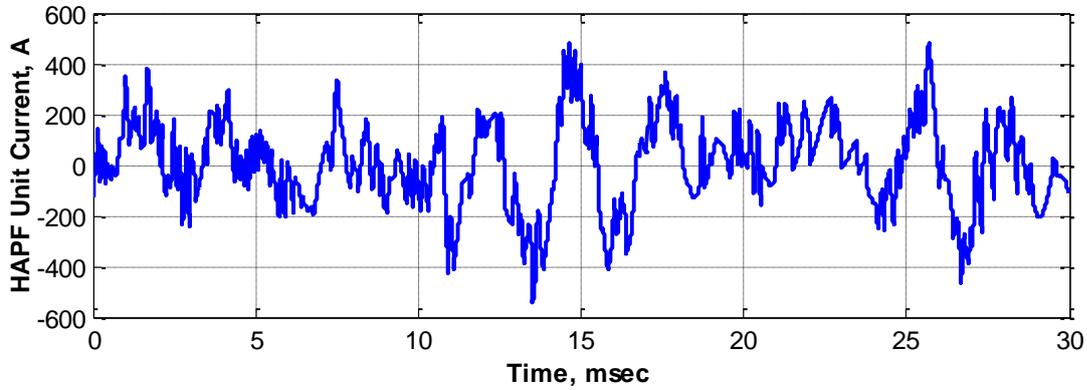
Figure 3.10 HAPF unit current waveform with hysteresis current control philosophy
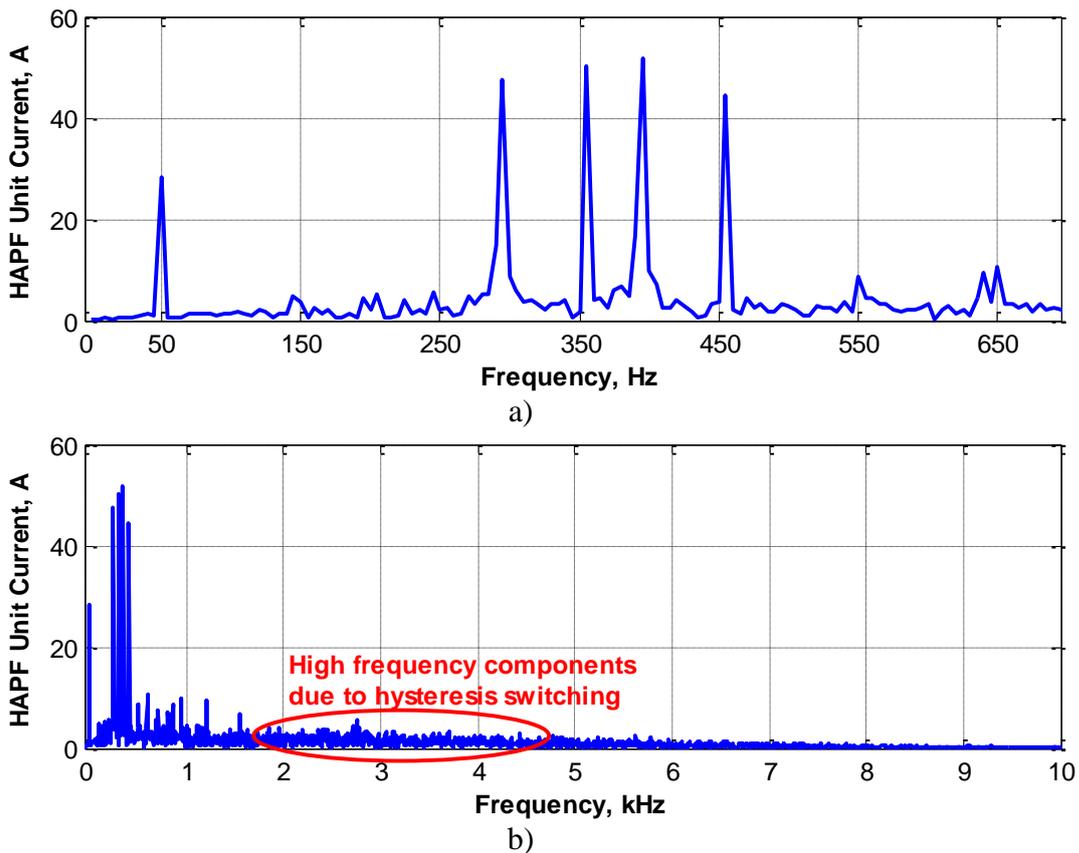
Figure 3.11 Harmonic spectrum of the HAPF unit current in order to show a) dominant interharmonics and b) high frequency components

Figure 3.11.a shows that the interharmonic content of the HAPF unit current strongly related to the ones at MV level. Since the hysteresis switching causes high frequency and irregular switching behavior, the whole frequency band (up to 10kHz) should also be investigated in order to observe those frequency components. As can be observed from Figure 3.11.b, high frequency components arising from hysteresis switching appear from 2 kHz up to 5 kHz with mostly concentrated around 3 kHz. The effect of switching frequency is shown as distributed around a wide range as expected instead of integer multiples of a single frequency, which is a drawback of proposed hysteresis current control method.

CHAPTER 4

IMPLEMENTATION OF PROPOSED HAPF SYSTEM TO IMF AND EXPERIMENTAL RESULTS

The proposed HAPF system, composed of nine identical HAPF units, has been implemented in the field for the verification of proposed solution to harmonic problems of steel melting facility under investigation. Overall view of the implemented system is given in Figure 4.1. In this chapter, the components of the implemented system and experimental results are presented in detail.

Figure 4.1 View of the HAPF system implemented in the field

4.1. Power Stage

The power stage is part of the HAPF unit and composed of input LC filter, dc link and converter semiconductor switches. Those high power electronics equipment are introduced in the following sections. A field photograph showing the power stage is given in Figure 4.2.
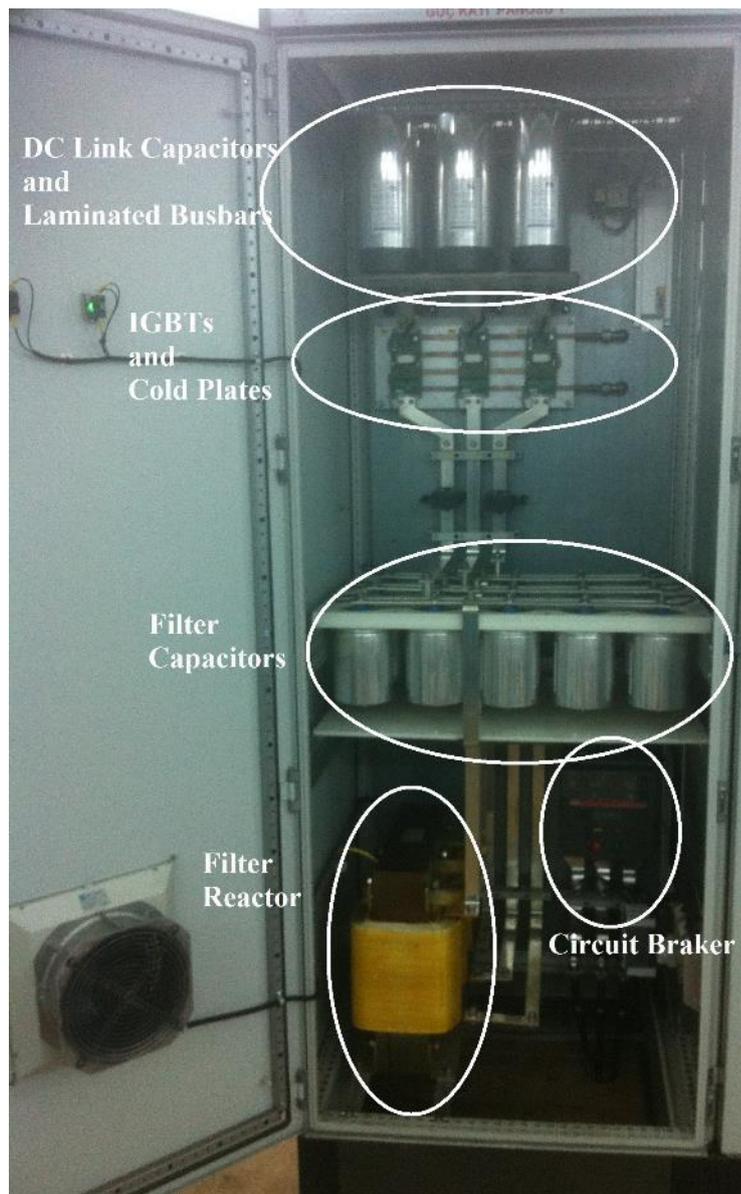
Figure 4.2 View of the power stage for each of the nine identical HAPF units

4.1.1. Semiconductor Switching Equipment

The switching equipment used in the power electronic converter is IGBT, which allows high speed switching on high voltage and current conditions. Since the converter is three-phase three-wire two-level converter topology, there must be six IGBTs in order to implement it. Thus, two-pack IGBT modules of Semikron (SEMIX854GB176HD) are used for each phase. The circuit representation of each module is as given in Figure 4.3. The voltage and current ratings of each individual IGBT are 1200V and 600A, respectively. In order to operate IGBTs, IGBT gate driver card of Semikron (SKYPER 32PRO R) is used. The driver provides a feedback signal for observing the semiconductor health, analog case temperatures of each IGBT in the module, and shoot-through protection. Since the electrical power to be conditioned in the converter is very high, the overall loss in the IGBTs is also too high to be cooled down via air ventilation despite a good efficiency. For this reason, IGBT modules are mounted on an aluminum cold plate which contains copper tubes located exactly under hottest points. The cold plate is supplied by MERSEN company. Since IGBT control signals are high frequency signals, low inductance flat cables with minimum possible length are used to connect gate drivers to control card.
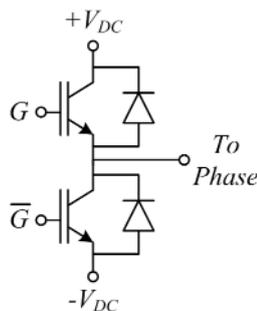
Figure 4.3 Dual Pack IGBT module used in HAPF unit power stage

Inductance on the current path between IGBTs and dc link capacitors are minimized by keeping the path as short as possible. For the same concern, positive and negative current paths are designed as busbars squeezed to each other with an insulation sheet

between them, as given in Figure 4.4. Also, capacitors are evenly distributed through the dc bus for distributing the current path over the maximum cross-section. Therefore, the voltage overshoots that IGBTs are exposed to during turn-off are kept at reasonable level. Since the converter are designed with 550V dc link voltage, voltage overshoot margin is 650V for 1200V IGBTs.
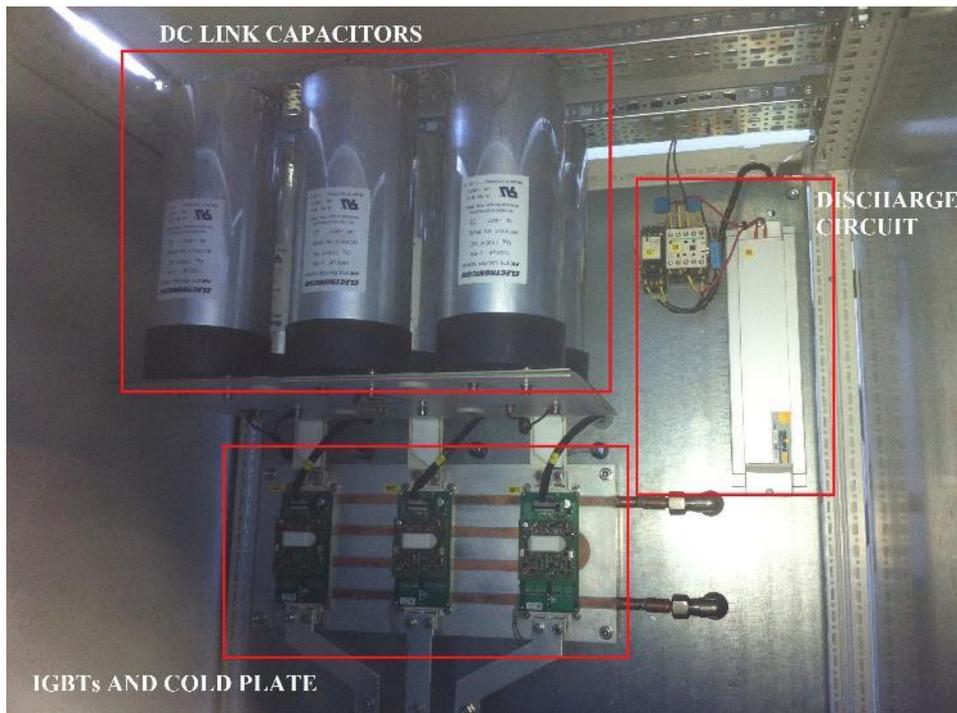
Figure 4.4 View of the dc link, semiconductors and busbar arrangement for the field implementation

4.1.2. DC Link Capacitor

DC link capacitor is determined as 9 mF using the simulations by taken into account voltage ripple and dc link current concerns. Due to the instantaneous current and capacity restrictions, dc link capacitor is implemented as a six-pack capacitor bank illustration of which is shown in Figure 4.5. DC link capacitors are chosen to be dry type metallized film power electronic capacitors in order to provide fast and high

current ripples with a self-healing property. The dc link voltage value is theoretically calculated as 550V with 10% ripple as mentioned in Chapter 3, however, the rated voltage of the capacitors used in implemented system have been chosen as 1100V. The reason for choosing such higher voltage capacitors is that the capacitors, in worst case, may be charged up to the 1000V the peak value of 690V grid voltage. The worst case condition is realized when all of the IGBTs are OFF state resulting in a three-phase diode rectifier mode of operation.
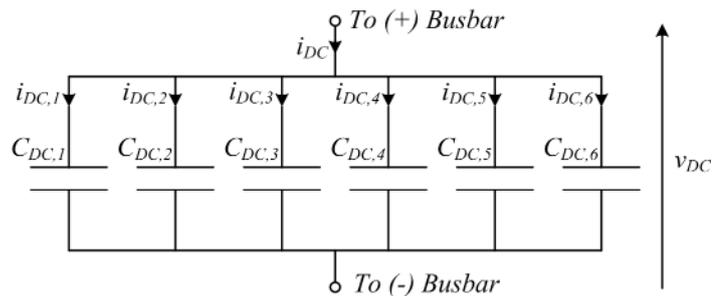
Figure 4.5 Capacitor bank for the DC link implementation
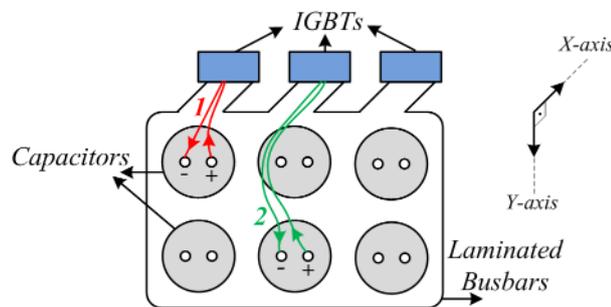
Figure 4.6 Illustration of capacitor arrangement on DC link busbars

The current rating of individual capacitors is designed a bit higher than expected dc link current divided by the number of capacitors due to the fact that the currents of the individual capacitors ($i_{DC,1} - i_{DC,6}$) are not shared equally. Unequal current sharing is caused due to the arrangement of capacitors, field view of which is given in Figure

4.4, on the dc link busbars with respect to IGBTs as illustrated in Figure 4.6. Although dc link is designed as laminated busbars to reduce both resistance and inductance of the connection, there may still exist impedance differences between the current paths of capacitors (path 1 and 2 as illustrated in Figure 4.6) especially during high frequency commutation of currents between semiconductors.
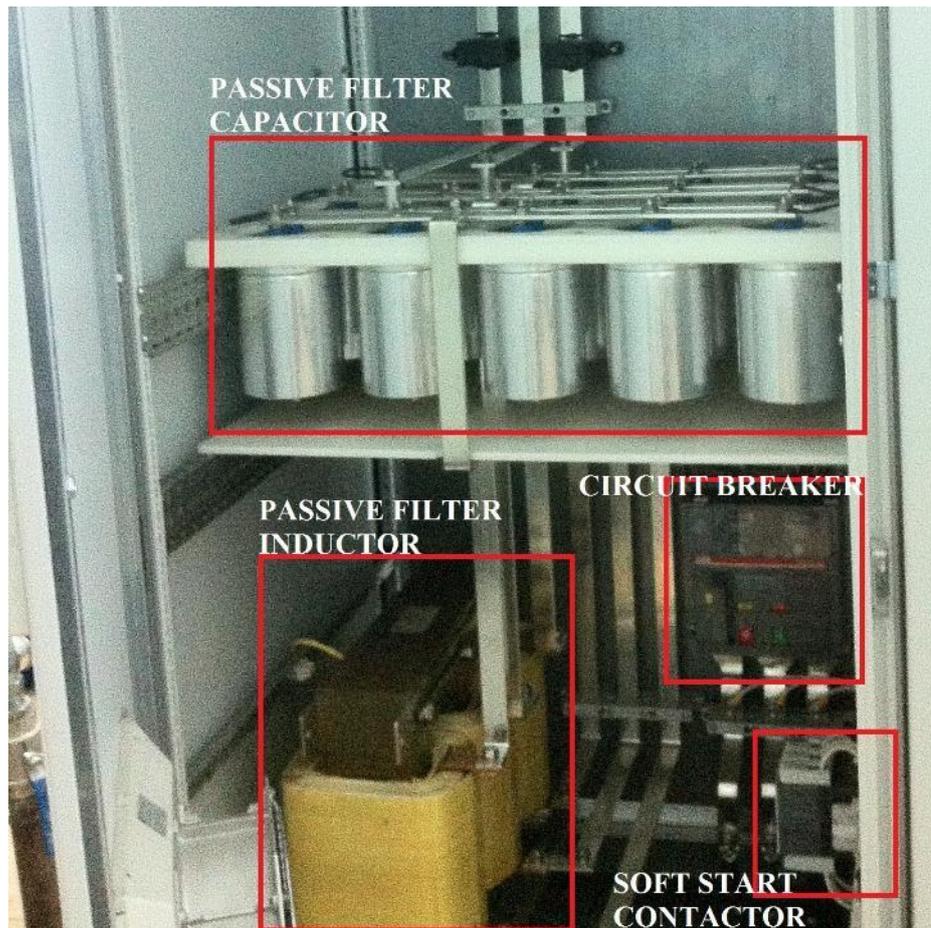
Figure 4.7 View of the passive filter of each HAPF unit

4.1.3. Passive Filter

Passive filter is implemented in the HAPF system as given in Figure 4.7 by taking into account both analytical calculations and simulation results. Passive filter capacitor

carries almost all of the fundamental frequency grid voltage between its terminals due to the impedance characteristics of the passive filter. However, the voltage drop on the capacitor terminals due to harmonic and interharmonic currents are very low as compared to fundamental component. Therefore, filter capacitor ratings are determined considering the fundamental frequency voltage with some tolerance. The filter capacitor is the standard product of Electronicon, Germany and is an AC power electronics capacitor equipped by metallized film technology with castor oil for effective cooling. In addition, it has self-healing feature. In order to provide faster discharging on turn-off procedure, parallel resistors are externally connected to the terminals of capacitors. Five capacitors are used as a bank for each phase as can be seen in Figure 4.7.

The reactor is designed by the company Hans von Mangoldt. For the design, not only fundamental current component but also some dominant harmonic currents are given together with the rms current rating to the producer in order to specifically design the filter reactor for HAPF application. The reactor is composed of copper sheets wounded on laminated iron core with type F insulation material. There is an important issue for the design of the filter reactor that the reactor core is overheated due to the high frequency currents caused by hysteresis switching, which should be taken into account when the waveform modulation method is hysteresis band switching.

4.2.   Control and Protection Circuits

There are some mechanisms for controlling various system level operations of HAPF system and some protection means to prevent harmful situations. In this section of the thesis, protection means and measurement equipment are mentioned then the operation of control system devices is described as sub-sections.

For the safety of the operators and protection of the converter components, a discharge mechanism has been installed to the dc link of each of the HAPF units. The aim of the discharge mechanism is to make sure that dc link voltage is at safe level as soon as possible when the HAPF unit is turned-off. In order to reach this aim, a powerful resistor is connected to dc link busbars via a contactor, as can be seen in Figure 4.4,

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for fast reclosing. The resistor chassis is made of aluminum and is mounted on the mounting plate of panel in order to cool down the resistor.

Before turning the HAPF system on, the passive component must be energized. The initial energization process causes a very high inrush current due to the passive filter response. The simulation of passive filter elements on the worst-case energization process is as given in Figure 4.8. The worst-case inrush current occurs at the switching instant when the corresponding instantaneous grid voltage is at peak value. In order to prevent the harmful effects of passive filter inrush current, a soft start circuitry has been added to the system as can be seen in Figure 4.7. An automation code is implemented for soft-switching the passive filter through a resistor with the help of a contactor. Three seconds after soft energization of the passive filter, a circuit breaker by-passing the contactor-resistor pair is turned on so that all the current is commutated to circuit breaker for proceeding to normal energization of passive filter. By the feedback of circuit breaker state, short-circuited contactor can be turned off under zero current condition thus significantly increasing the lifetime of it.
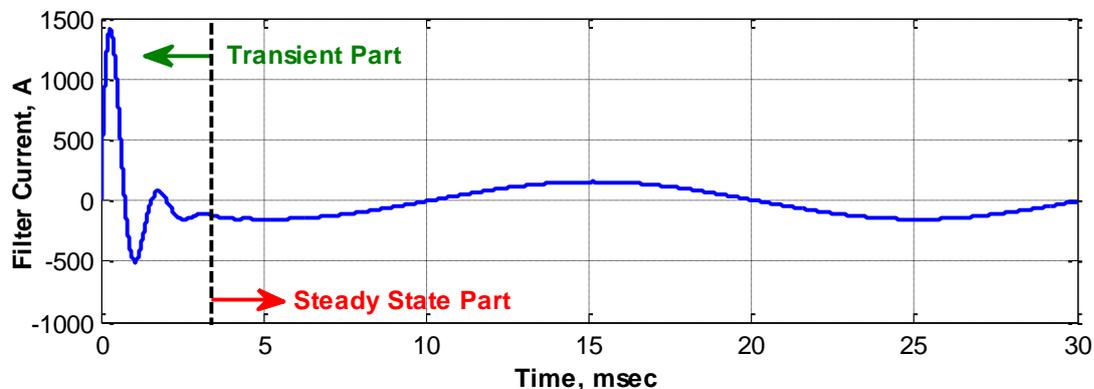
Figure 4.8 Simulated current waveform of the passive filter during energization under worst case conditions

Overload and short-circuit protection is provided by using the three pole circuit breaker seen in Figure 4.7. The circuit breaker, supplied by ABB, has an adjustable

trip unit rated at 800A current and 690V grid voltage. It had observed several times in the field after some period of normal operation that the electronic trip unit of the circuit breaker failed and started tripping the system wrongly although there was not any over-currents. After some discussion with the manufacturer, it is found out that the magnetic fields created by the harmonics and interharmonics may cause failures on the trip unit electronics after some period of operation.

In addition to unit level protections, the HAPF system itself is protected at MV level via a protection relay, SEPAM – Schneider Electric, and a metal clad circuit breaker located at the feeder reserved for HAPF system for undervoltage, overcurrent and earth fault.

For the control and measurement purposes, some sensors are used in the HAPF system. Current transducers are used on each HAPF unit for the measurement of unit currents. DC link voltage is measured via a resistive divider located at the control card. IGBT case temperatures are sensed via Negative Temperature Coefficient (NTC) temperature sensors and given to controller analog channels.

Calculating the control system references can only be possible by measuring the MV side source and HAPF currents. HAPF currents are measured via a toroidal current measurement transformer having conversion ratio of 100/5A. The secondary of HAPF current measurement transformer is connected serially MV relay and all nine HAPF units then short circuited. Source current is obtained from the already available measurement cell of the steel melting facility without preventing the other systems from taking the measurements. The short-circuited termination of the measurement transformer is serially connected to all of the HAPF units and then again terminated with a short circuit.

4.2.1. DSP Board

Control system algorithm has been implemented on a PCB composed of modular boards realizing various duties. The main DSP board, shown in Figure 4.9, is composed of five parts namely DC link and Temperature Measure (DTM) board,

Voltage and Current Measure (VCM) board, Supply Board (SB), Firing Board (FB), and Digital Interface (DI) board. Each board is indicated and labeled in Figure 4.9.
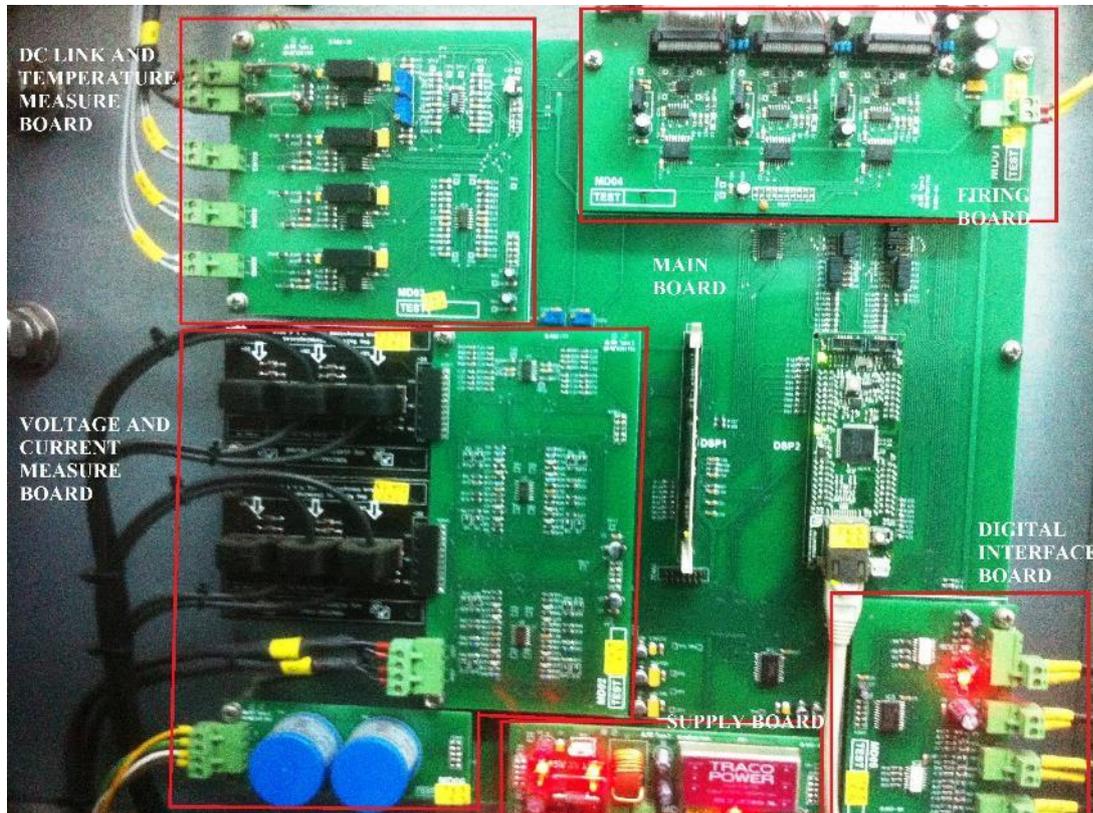
Figure 4.9 The main DSP board and its modular components

DTM board is responsible for the pre-processing of dc link voltage and IGBT case temperatures. DC link voltage is down-scaled to low voltage level via a resistive divider and the resultant signal is fed to isolation amplifier before reaching to controllers in order to provide an isolation between main board and power stage. Similarly, temperatures of IGBT cases are measured by NTC temperature sensors fed to isolation amplifier before reaching main board.

VCM board contains toroidal current transducers in order to obtain the instantaneous current values get from current measuring transformers. Also, PCB type precise

voltage transformers are used for down-scaling the voltage values get from voltage measuring transformers. This board contains scaling and offset adding circuitry for each voltage and current signal in order to increase resolution of Analog to Digital Converter (ADC) by covering the whole voltage range of DSP analog input channels.

FB is responsible for sending the IGBT gate triggering pulses to the corresponding gate drivers. The triggering pulses and corresponding feedback signals are transferred between gate driver and main board via isolation amplifiers.

SB contains an off-the-shelf isolated SMPS and its auxiliary components. SB provides the necessary power for all the sub-modules connected to main board. Moreover, input and output passive filters for the proper operation of SMPS are also located in this board.

Peripheral digital signals are sent and/or received by the main board using the DI board. It contains opto-coupler Integrated Circuits (ICs) for optical isolation of digital signals.

The main DSP board contains two DSP's, one of them is a powerful controller, TMS320F28335, having floating point core with clock frequency 150MHz, which hereinafter will be named as control DSP. The control algorithms for HAPF system power electronics hardware are handled via control DSP. Sampling frequency of the measured signals is chosen to be 25 kHz thus time interval of 40μsec between two successive sampling instants is available for the execution of control algorithm. Since there are lots of time consuming operations to be handled by control DSP, some operations are determined as the responsibility of another controller. Monitoring of field signals, RMS, mean, FFT calculations and sending them to Human Machine Interface (HMI) via Ethernet communication are the most important duties of this controller (TI Stellaris ARM Cortex M3), which hereinafter will be named as monitoring DSP.

Control algorithms, fulfilled by control DSP, have already been explained in previous parts of the thesis, therefore, only the duties of monitoring DSP will be mentioned in this section. The block diagram showing all the responsibilities of monitoring DSP is

given in Figure 4.10. It is essential to note that although monitoring DSP is required to conduct floating point calculations, it is actually a fixed point controller. The floating point calculations are handled by monitoring DSP by making use of IQmath library [132], which is an open source library for floating point structures formed by fixed point variables. All the information processed by monitoring DSP is sent to HMI via a TCP/IP communications handling algorithm specifically designed for this application by the author via modifying the open source uIP (micro IP) [133] library. In addition to processed data signals, generated alarm bytes are also added to the communication frame in order not to use lots of copper cables for each alarm signal.
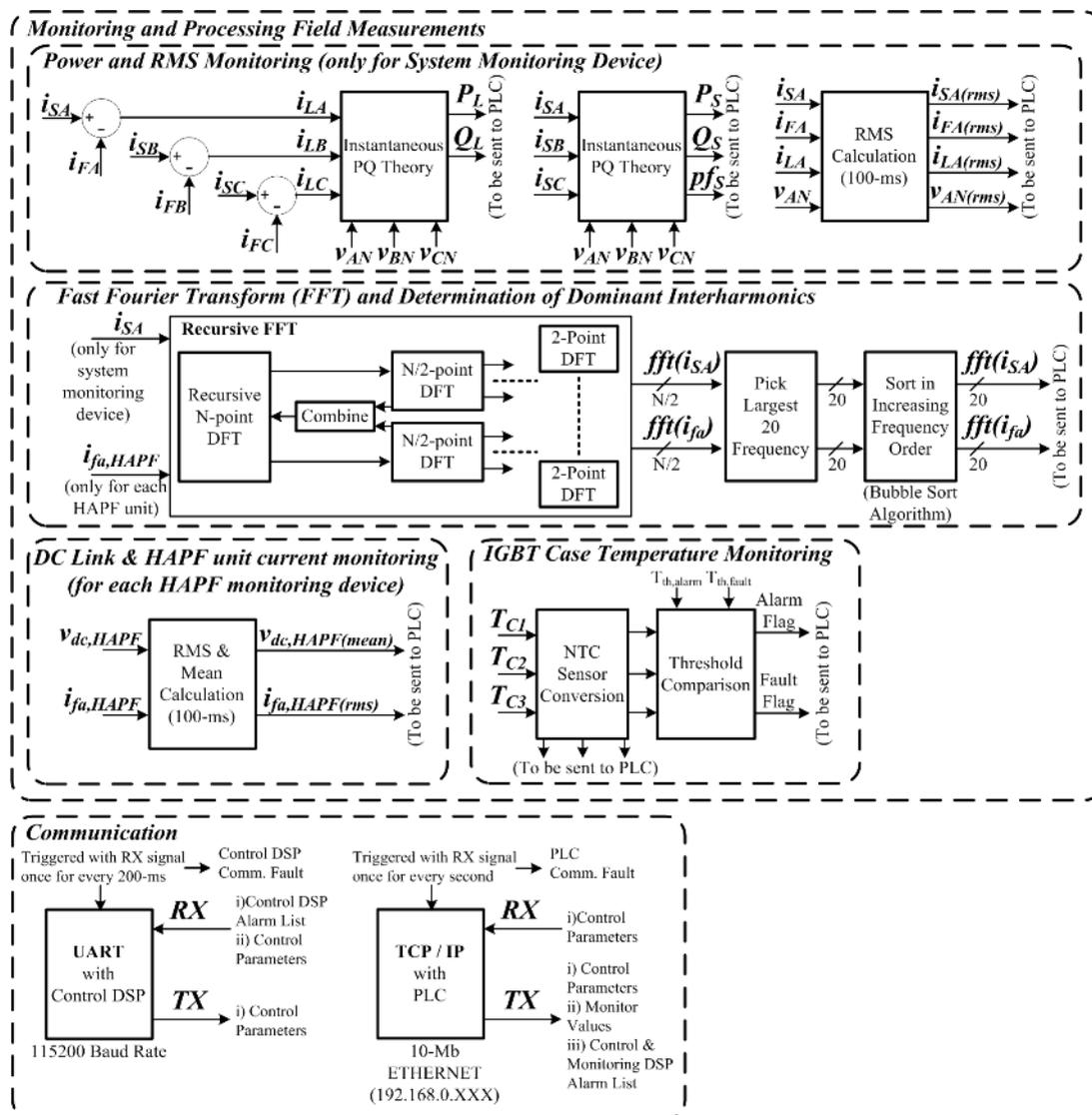
Figure 4.10 Block diagram representation of the responsibilities for monitoring DSP

As can be seen in Figure 4.10, monitoring DSP duties are divided into two classifications namely system monitoring device and HAPF unit monitoring devices. HAPF unit monitoring devices are responsible for the operations related to each HAPF unit, while system monitoring device handles the system level calculations. System monitoring DSP calculates the RMS values of MV signals and calculates active and reactive powers by using instantaneous PQ theory [134] – [136]. Monitoring DSPs of each HAPF unit, however, calculates the mean value of dc link voltage, RMS value of unit line current, IGBT case temperatures and generate corresponding alarm signals.

In addition to basic RMS and mean calculations, the monitoring DSPs handle FFT in order to illustrate the harmonic and interharmonic content of each HAPF unit and MV source and filter currents. In order to reach this aim, a recursive FFT algorithm, shown in Figure 4.10, is used for the calculation of harmonic content as fast as possible. The algorithm works as the recursive operation of 2-point Discrete Fourier Transform (DFTs) up to N-point DFT calculations, where N must be some integer power of 2 (2^n, n is integer). Since the dominant harmonic frequencies vary in time, the most dominant harmonics and interharmonics with 5 Hz resolution should be sent to HMI instead of sending the whole frequency band in order to reduce the communication frame size. For this reason, a bubble sort algorithm is used to sort all the harmonic frequencies and most dominant twenty frequencies are added to the communication frame together with their magnitudes.

4.2.2. Industrial Automation System

In order to handle the system level control operations other than the converter control algorithm, an industrial automation system structure has been assembled. The main duties of industrial automation system is to operate CBs, control MV relays, provide HMI, manage Water Cooling System (WCS) commands, handle reclosing of HAPF system, operate automatized start, stop and fault procedures etc. Programmable Logic Controller (PLC), with brand name Siemens S7-1200, and necessary I/O modules have been used to manage all the mentioned functions. Also, various types of

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industrial relays are also used as the auxiliary components of industrial automation system to adapt different voltage levels and deliver high power to required units. PLC controller together with its I/O modules, miniature circuit breakers, various relays, connectors, power supplies and HMI are located inside the control panel shown in Figure 4.11.
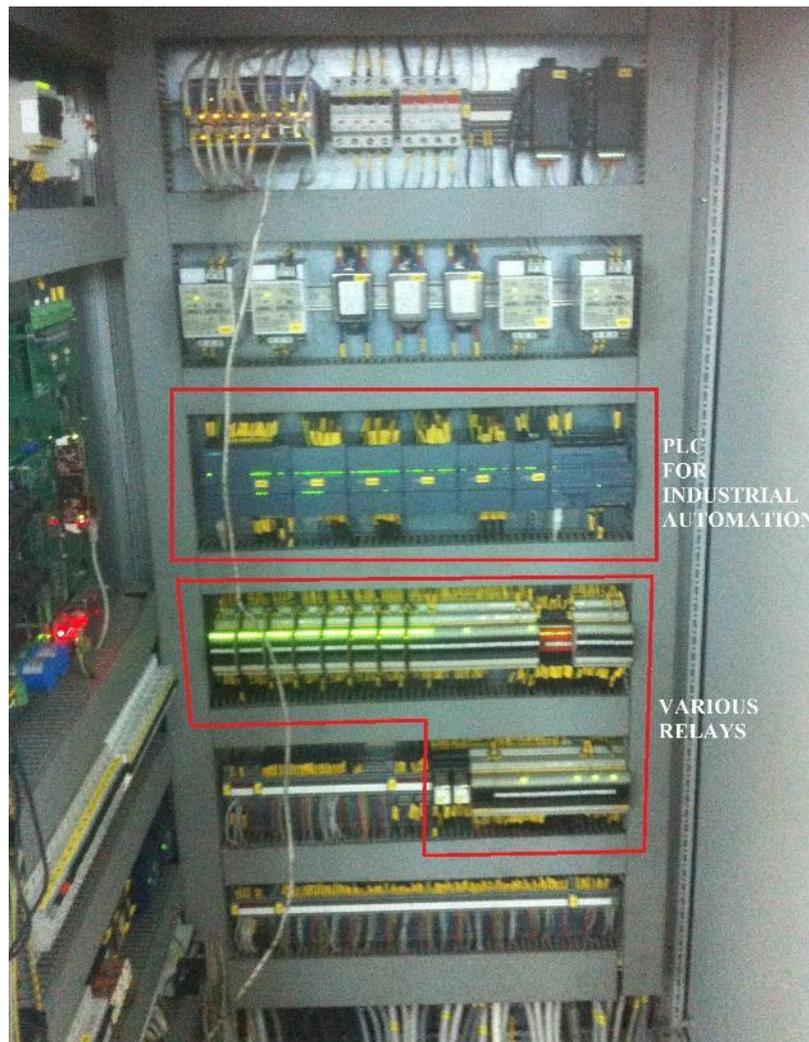
Figure 4.11 Control panel for handling industrial automation and user interface

HMI is a touch panel monitoring device, which is the product of Siemens. HMI contains a software, in WinCC Flexible, to read/write information from/to memory

blocks of PLC. By this way, all voltage current values, frequency spectrum, and HAPF unit semiconductor temperatures are shown on this touch panel computer. Also, CB controls, start, and stop commands can be sent to corresponding components of the HAPF system via HMI.

4.3.   Water Cooling System

High power semiconductor devices, due to their non-ideal structure, cause two kinds of loss components during operation, namely conduction loss and switching loss. While conduction loss is the loss component during conduction of current due to the on-state voltage drop of the semiconductor, switching loss is the one due to the existence of high voltages and currents at the same time during every switching instant. Both loss components are dissipated as heat exactly at the semiconductor junction. Manufacturers specify the maximum allowed junction temperature, 125 °C for the devices used in this system, in order not to harm the semiconductor devices. Since converter currents are very high, cooling the semiconductors via forced ventilation is not sufficient for keeping the junction temperature of them at reasonable values.
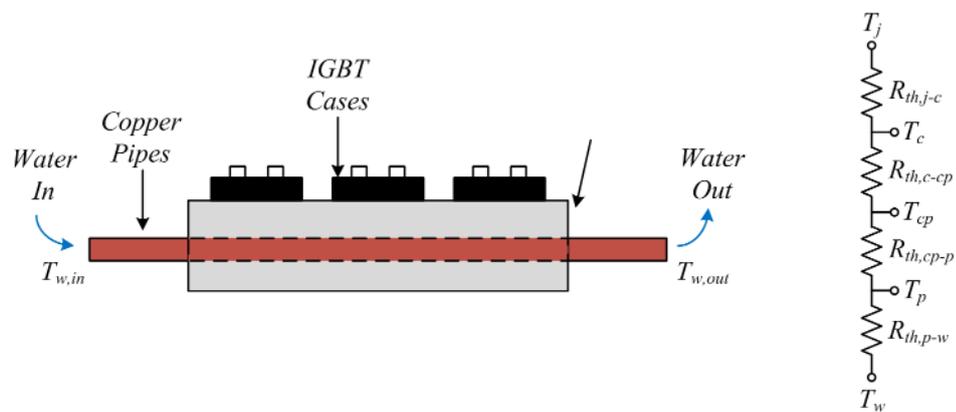
Figure 4.12 Illustration of cooling plate structure and corresponding thermal resistances

For this reason, AlSiC cold plates with buried copper pipes are used to allow the water flow inside them. An illustration showing the cooling plate, semiconductors, and copper pipes is as given in Figure 4.12. Temperature and the flow of inlet water is

determined by considering the temperature drop on the thermal resistances of junction to IGBT case ($R_{th,j-c}$), case to cold plate, ($R_{th,c-cp}$), cold plate to pipe, ($R_{th,cp-p}$), and pipe to water, ($R_{th,p-w}$), as given in Figure 4.12. The cooling liquid, soft water for this particular research work, is forced to flow through the copper pipes with a certain pressure created by the redundantly working pumps in water cooling system given in Figure 4.13.

Figure 4.13 Water cooling system installed in the field

As the flowing water absorbs the dissipated heat, its temperature increases too. If the water does not cooled down, the junction temperature will eventually reach dangerous values. Therefore, the cooling water is cooled down inside the WCS via a water-to-water heat exchanger. WCS is controlled by the industrial automation system. Liquid

flowing system is a semi-closed cycle one connected to air via a filter. Cooling water reaches to each module through the thick polymer water pipes and hoses connected parallel to each other as shown in Figure 4.14.

Figure 4.14 View of cooling water hose connections and polymer main pipes

4.4.   Flowchart of the Control Algorithm

As mentioned in early sections, the control system has been composed of two controller, one is the control DSP and the other is monitoring DSP. Real-time programming philosophy is used to realize the algorithms due to the time dependent nature of the application. When the system is run, time is divided into equal intervals via timer interrupts so that the control algorithm is triggered in real time. Even if the controller has completed all the duties for a time interval, it waits in idle mode until the next trigger signal arises. At the instant of each trigger, the controllers initiate the

sampling of necessary inputs and calculate all the duties during a certain time, execution time. The most important rule for this kind of programming is that the execution time, t_e, should be smaller than the time between two successive sampling instants. In other words, the necessary calculations corresponding to a sampling instant and resultant acts should be completed before the next samples arise. Software flowchart is given for both control and monitoring DSPs in Figure 4.15 and Figure 4.16, respectively.
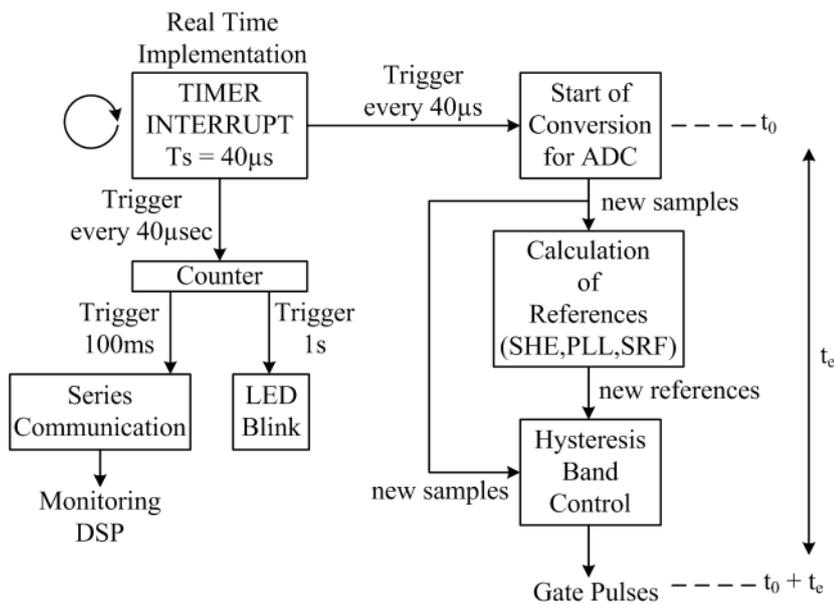
Figure 4.15 Software flowchart of the control DSP

As can be seen in both figures that all the functions in the flowchart are time dependent and triggered by the interrupt tick signals. Control DSP handles the time critical reference calculations for HAPF converters, while the monitoring DSP processes the sampled data and sends them to industrial automation system just for user observation. Thus, the output of control DSP is updated in every sampling period, however, monitoring DSP sends the resultant data every second. Slow data transfer cycle of monitoring DSP is due to the fact that the change of the observable data should be as slow as user can observe.
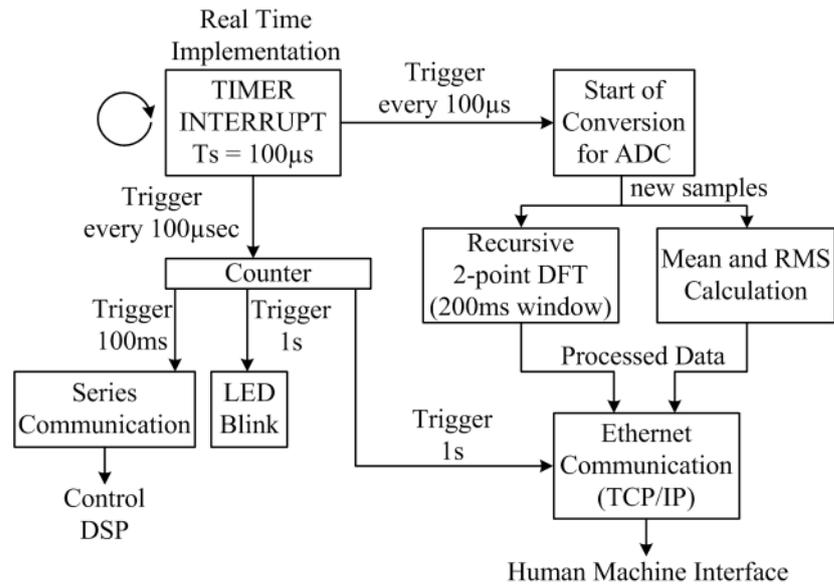
Figure 4.16 Software flowchart of the monitoring DSP

4.5. Hierarchical Control System Architecture

Various digital control system architectures have been proposed for APF systems in order to handle the coordination of signal processors together with other auxiliary equipment [137] – [142]. An array of resonant controllers have been proposed in [137]. Fully digital FPGA based control system architecture is suggested in [138]. Ref. [139] recommends an FPGA based System-on-Chip solution for the control of APF. A hierarchical control system architecture has been proposed for three-phase four-wire APF systems in [140]. Ref. [141] recommends a digital deadbeat current control structure. An APF implementation of a hierarchical information structure has been illustrated in [142]. Although those control systems are fully digitalized and designed specifically for APFs, neither of them proposes a generalized architecture for a modular and scalable control system for modular APFs. On the other hand, handling the control duties for distributed, modular and scalable systems have been satisfied via hierarchically partitioned control system architectures by various researchers [143] – [150]. Mentioned control system architectures have been used in various areas like MARX modulator [143], telescope systems [144], autonomous vehicles [145], microgrids [146], [147], power systems [148], parallel operated VSC system [149],

and discrete event systems [150]. In addition to those mentioned systems, high power electronic converters composed of Power Electronics Building Blocks (PEBB) should also equipped with modular and scalable hierarchical control system architectures [151].

4.5.1. Power Electronics Building Blocks (PEBB) Concept

High power electronics converters have recently been composed of generic modules, PEBB, in order to reduce size, cost, losses and weight [152], [153]. In addition to physical benefits, PEBB based structures provide hardware standardization and flexibility in the design [152]. APF systems designed using PEBBs have also been proposed in the literature [154] in order to take advantage of this concept.

Similarly, the control system should also be modular, scalable and standardized so that the modularity and efficiency of the overall system can be maximized. Hierarchical control system architectures have been proposed [155] – [160] as a suitable control system structure for PEBB based power electronics converters and an IEEE Standard guiding the suitable control system architecture has been published in 2011 [151]. It is mentioned in all of the works [155] – [160] and IEEE guide [151] that the control system architecture should be divided into hierarchical layers. The division of layers can be determined using the functional and temporal properties of the control system components [161]. All the requirements such as timing, duties, interfaces, communication frames etc. should be determined for a general PEBB based converter.

4.5.2. Implementation

The control system architecture proposed and implemented in this thesis is an example of the control system architecture proposed in IEEE guide [151], with some suggestions and contributions on it [162]. By this way, the control system is partitioned into four hierarchical layers as given in Figure 4.17 according to their functional and temporal requirements. The strictest difference for the partitioning is the timing concerns as can be seen in Figure 4.17. While the bottom layer gathers

information or acts against an action in less than 1μs, the top layer updates information about the system for each second. The complexity of the control duties are dramatically increases from top to bottom layer.
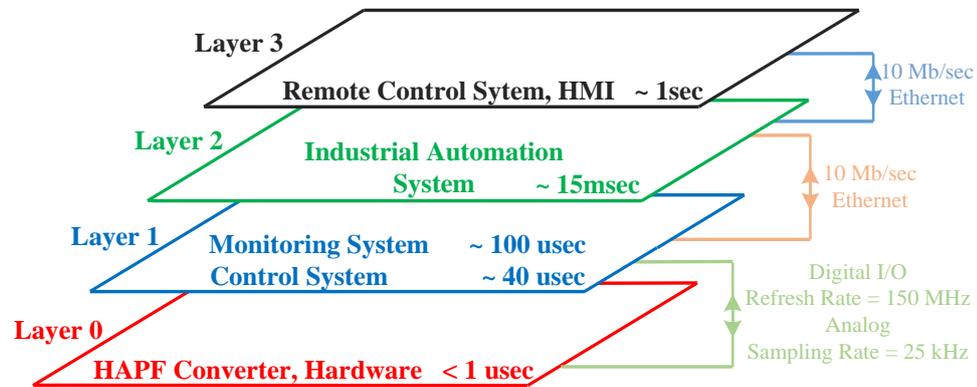
Figure 4.17 Functional and temporal partitioning of hierarchical control layers

Layer 3, the top layer, composed of human machine interface and remote control equipment. It is responsible for monitoring of the overall system to the user and accepting user commands [162]. The next layer, Layer 2, is used to determine the working state of the system and handles the industrial automation duties like circuit breaker, relay, WCS controls. Layer 1 contains control system devices that realizes the converter control algorithm. Power electronic converter switching instants are determined by this layer. The bottom layer, Layer 0, contains hardware of the converter, the semiconductor switches, filters, sensors, and analog signal electronics. The designed and implemented hierarchical control system architecture for the modular HAPF system under investigation is given in Figure 4.18.

The IEEE guideline for high power converters [151] also suggests a useful communication structure and necessary data to be transferred between hierarchical layers. The proposed control system architecture utilizes the suggested structure together with some extra details specifically needed for the HAPF system under investigation.
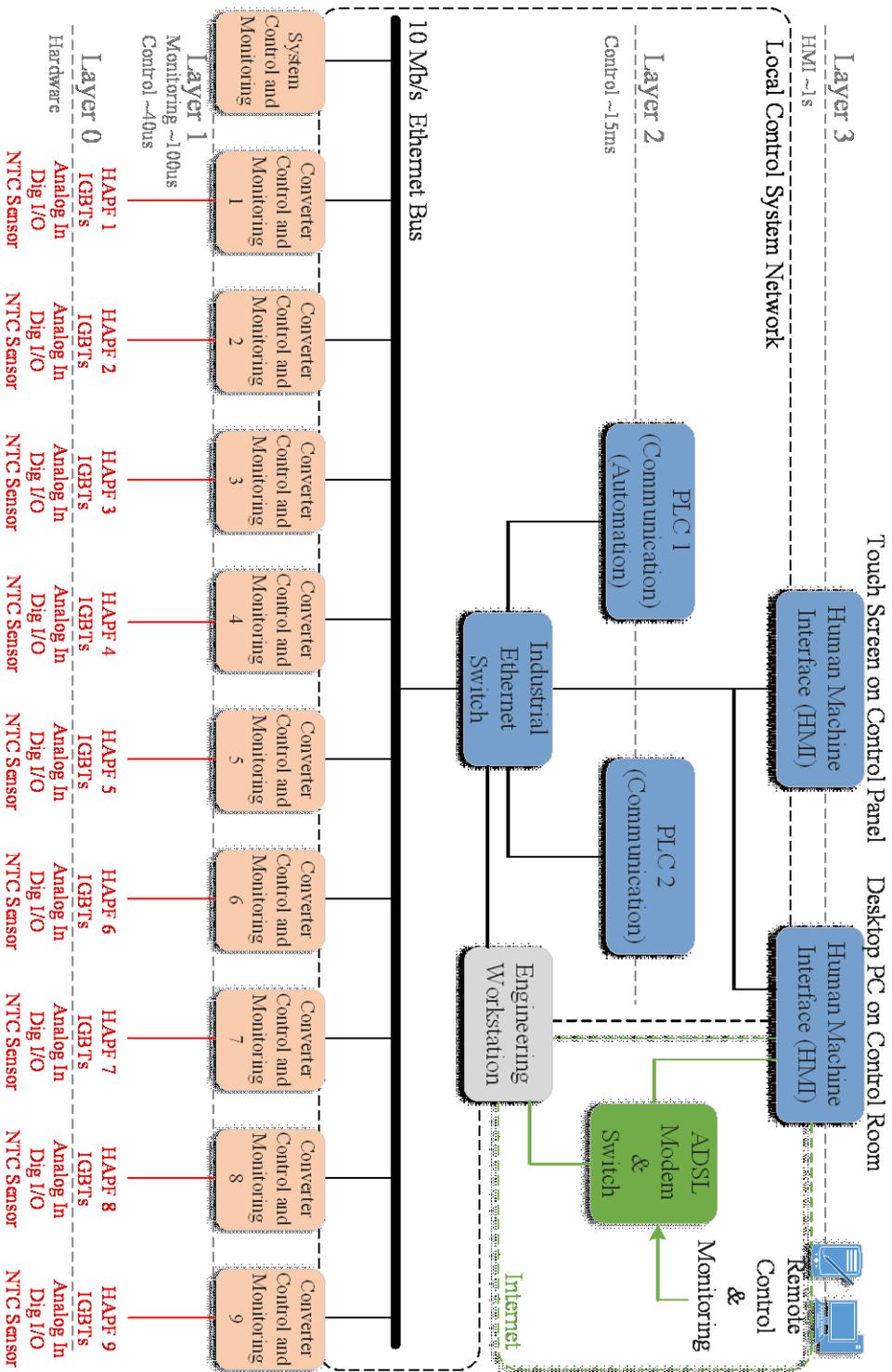
Figure 4.18 Hierarchical control system architecture proposed for modular HAPF system

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The devices located in the same layer are not allowed to communicate to each other for the sake of reduced complexity. However, the devices belonging to two successive layer communicates to each other due to the hierarchical structure of the control system layers. The communication structure is coordinated by the PLCs, as an industrial automation controller, which are located in Layer 2.

In order to avoid the clashes during communication structure of ten processors located in Layer 1, the real time is divided into equal intervals, each of them are reserved for the communication of a specific controller. This type of communication method is called Time Division Multiplexing (TDM) and the illustration of TDM is given in Figure 4.19. Each reserved time interval is 200 ms long and it is assumed that the necessary information is sent from PLC to DSPs and corresponding answer is returned during this time interval. Actually, bidirectional data transfer lasts less than reserved time interval, but some time buffers are added to avoid data collisions in case of repetition of lost packets.
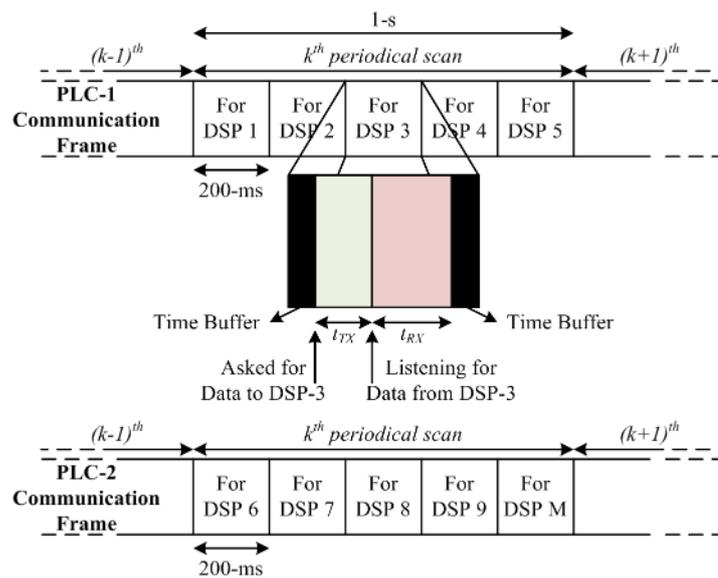
Figure 4.19 Illustration of TDM based communication frame

4.6. Experimental Results

The HAPF system mentioned in this chapter is implemented in the steel melting and forming facility owned by ER CELIK Metallurgy Co, Iskenderun/TURKEY. All the components of the implemented system are given in detail including brand names and part numbers at Table 4.1.

Table 4.1 Components of the implemented HAPF system

Hybrid Active Power Filter System	
Rated Power	2.7 MVA
Rated Voltage	690 V
Number of HAPF Units	9
3-Ph Coupling Transformer (Eltaş)	3.0/4.0 MVA , 31.5/0.69 kV DYn11, $U_k = 5.6\%$
HAPF Units	
Inverter Topology	Three Phase Full Bridge Inverter
Blocking Reactor (H.v Mangoldt)	0.1 mH/ph, iron core
Blocking Capacitor Bank (Electronicon)	500 uF/ph
Switching Method	Hysteresis Band Switched
Power Semiconductor (Semikron SEMIX854GB176HD)	1700V, 600A IGBT
Power Semiconductor Driver Circuit (Semikron SKYPER 32PRO R)	+15V, Flat Cable Signal Link
Switching Frequency	3.5 - 5 kHz
DC Link Voltage	550V
Cold Plate Cooling System (Mersen)	Single Side, Copper Pipe, Al Plate 10lt/min Flow Rate
DC Link Capacitors (Electronicon)	Dry Resin, MKP, Polypropilen 1100Vdc 1.5mF x 6

The implemented system successfully verified in the field that it satisfactorily suppresses all the interharmonic and harmonic frequencies to the allowed limits by the international standards [1], [28] and Turkish grid code [30] on power quality. In order to show the harmonic filtering performance over 100 minutes time interval for a wide frequency range, Figure 4.20 is drawn for both load and source current waveforms at MV level. The harmonic spectra for both load and source current waveforms are post-processed using FFT having 5 Hz resolution for every 200 msec

during 100 minutes period and shown respectively in Figure 4.20.a and Figure 4.20.b. According to given figure, all interharmonic and harmonic frequencies are successfully mitigated for the simultaneous operation of 1, 2 and 3 IMF installations considering all the steel melting phases (boring, melting and refining). The time varying characteristics of the IMF load harmonics can also be seen in Figure 4.20.
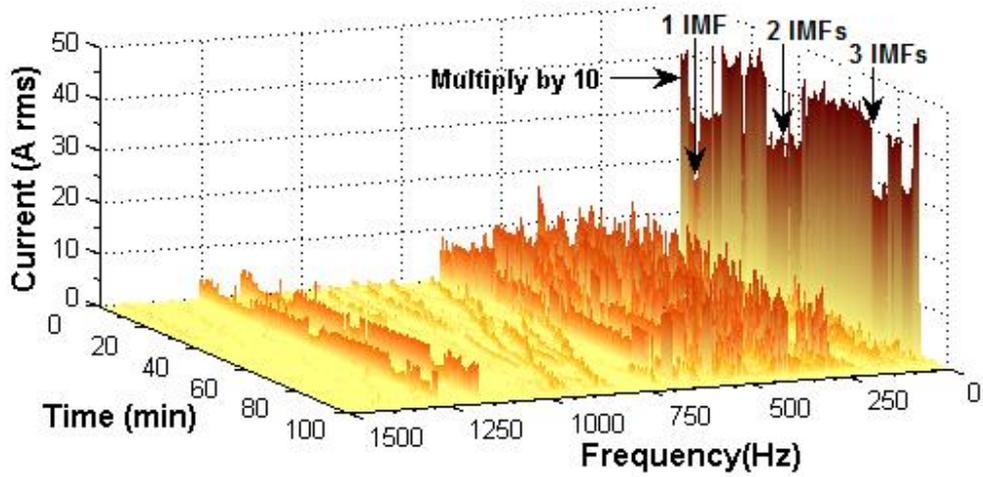
a)
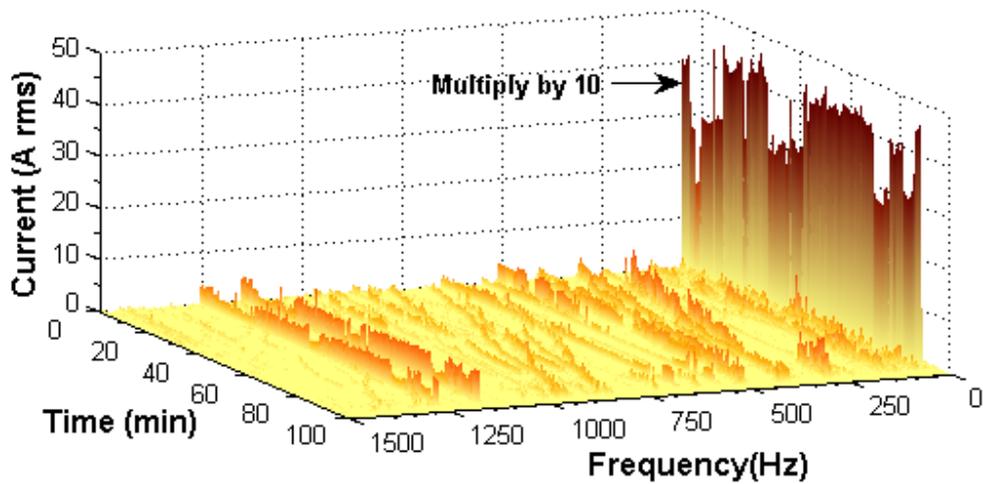
b)

Figure 4.20 Harmonic spectra of the field measurements a) load current and b) source current
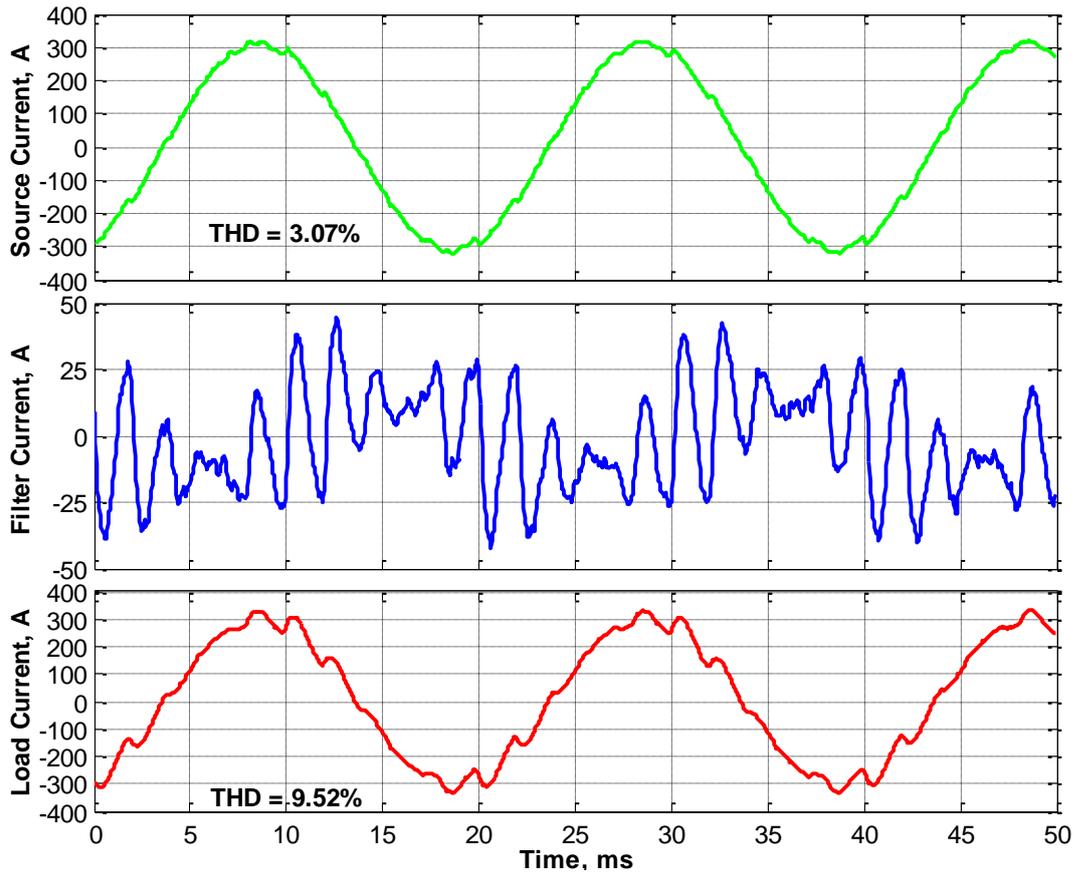
Figure 4.21 Source, HAPF and load current measurements while only one IMF is in operation

The MV waveforms and the corresponding harmonic spectra of the proposed HAPF system can be seen in Figure 4.21 to Figure 4.26 while one, two and three IMF installations are simultaneously in operation.

The THD of the load current waveform is shown to be reduced by the HAPF system from 9.52% to 3.07% at the source side as given in Figure 4.21 for only one IMF load is in service. When the corresponding waveforms together with their remaining parts in a 200 msec window are analyzed via FFT, the RMS values of each individual harmonic frequency can be observed as harmonic spectra given in Figure 4.22. It can be observed from Figure 4.21 and Figure 4.22 that all the harmonics and interharmonics are satisfactorily suppressed for this particular instant. Considering the

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dominant harmonics in Figure 4.21 and equation (1.11), operating frequency of the load resonant converter driving IMF in operation is calculated to be 150 Hz.
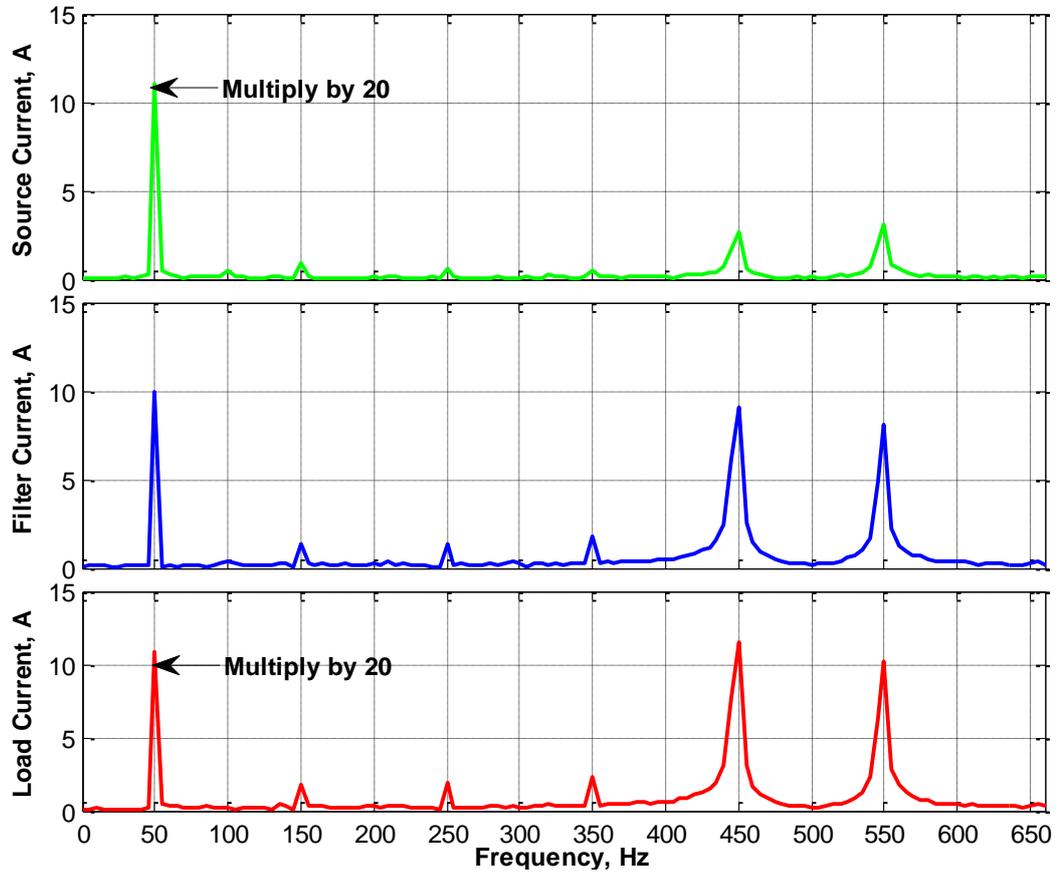
Figure 4.22 Harmonic spectra of the source, HAPF and load current waveforms while only one IMF is in operation

By this way, 250 and 350 Hz components due to the working regime of existing IMF load are expected to be in negative and positive sequence form using (1.11), respectively. Moreover, 11th and 13rd characteristic power system harmonics are also observed in this figure, which is due to the 12-pulse structure of the IMF driver as expected by (1.1).

Figure 4.23, on the other hand, represents the MV waveforms of the source, HAPF and load currents while two IMF installations are simultaneously in operation. As can

be understood from this figure that the THD of the load current waveform, 9.44%, reduced to 3.93% at the source current measurement. Similar to one IMF operation case, harmonic content of all of the current waveforms in Figure 4.23 can be drawn with 5 Hz resolution (200 msec window) as given in Figure 4.24.
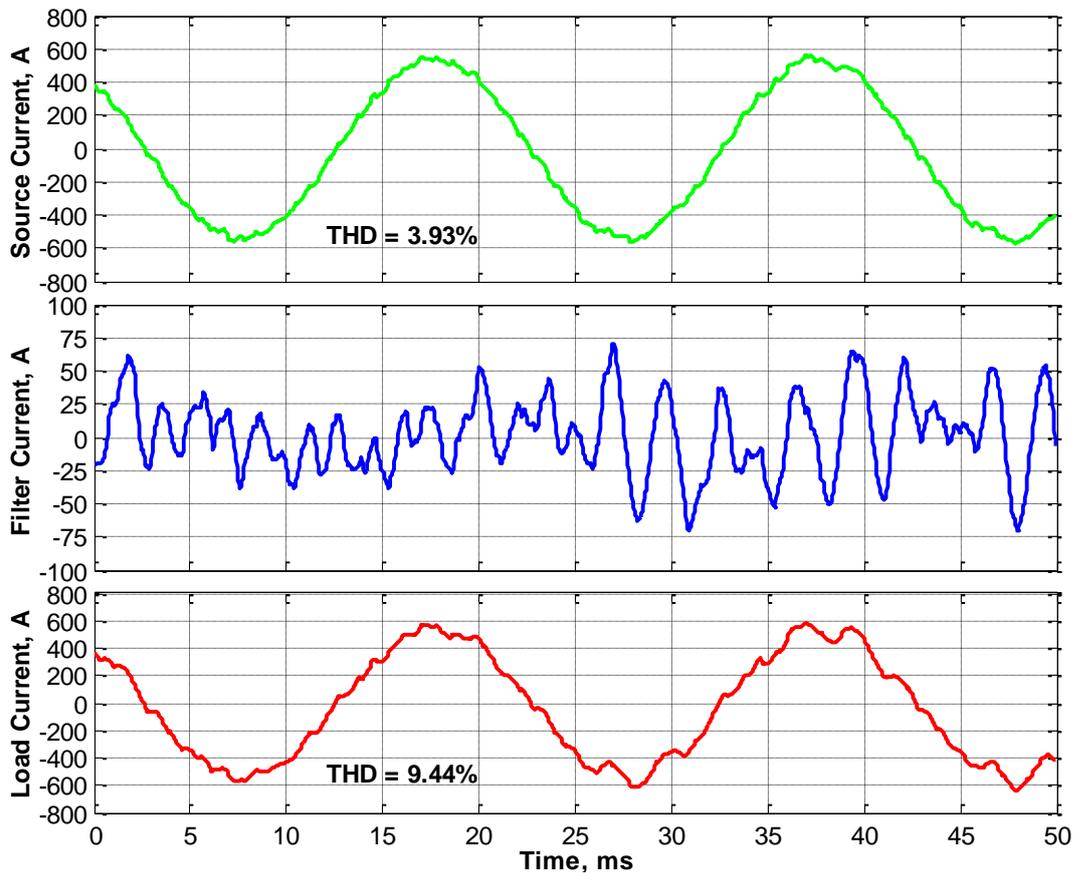
Figure 4.23 Source, HAPF and load current measurements while two IMFs are simultaneously in operation

When the harmonic and interharmonic content of spectrum in this figure is analyzed, the dominant interharmonics appear as 295, 395, 315, 415 Hz together with characteristic 11th and 13th power system harmonics. Those interharmonics represent the typical behavior for simultaneous operation of two IMF installations. 295 and 395 Hz interharmonic frequencies are due to one IMF load driven at load resonant frequency of 172.5 Hz, while 315 and 415 Hz components are due to another IMF

load driven at load resonant frequency of 182.5 Hz by inspection using (1.11). 11th and 13th characteristic power system harmonics are the natural cause of 12-pulse rectification of the IMF drivers. It is observed in the field during tests that total magnitude of 11th and 13th harmonic components are tend to be less than the sum of the contributions of each IMF driver while even number of IMF loads are simultaneously in operation; since they are connected to the MV grid via different transformers having different phase lags.
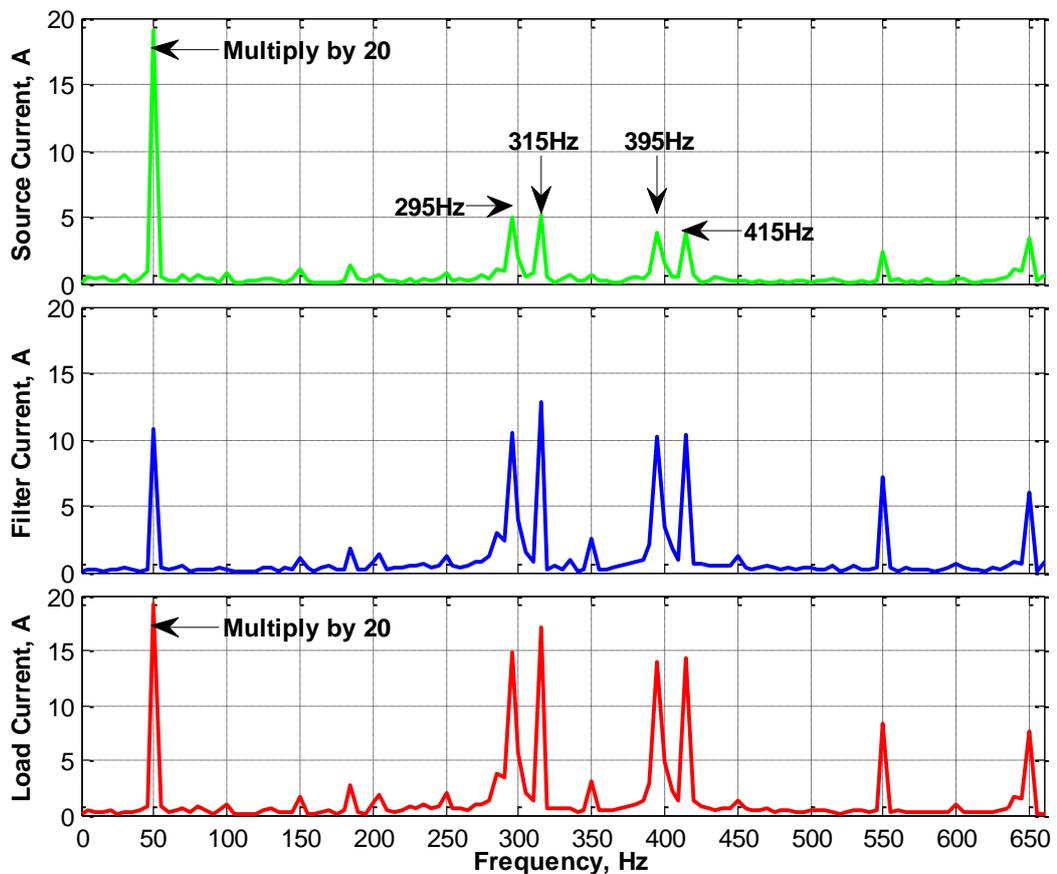
Figure 4.24 Harmonic spectra of the source, HAPF and load current waveforms while two IMFs are simultaneously in operation

The source, HAPF and load current waveforms illustrating the performance of HAPF system while three IMF installations are simultaneously in operation are given in Figure 4.25. The implemented HAPF system is shown to reduce the THD of the load

current from 9,52% down to 2.88% at the source side. When the harmonic spectra of the corresponding waveforms are analyzed, it is shown in Figure 4.26 that six individual harmonic frequencies appear at the same time as expected. Those frequency pairs can be listed as 340 – 440 Hz, 350 – 450 Hz, and 380 - 480 Hz, corresponding respectively to IMF load driver operating frequencies of 195, 200, and 215 Hz by using (1.11).
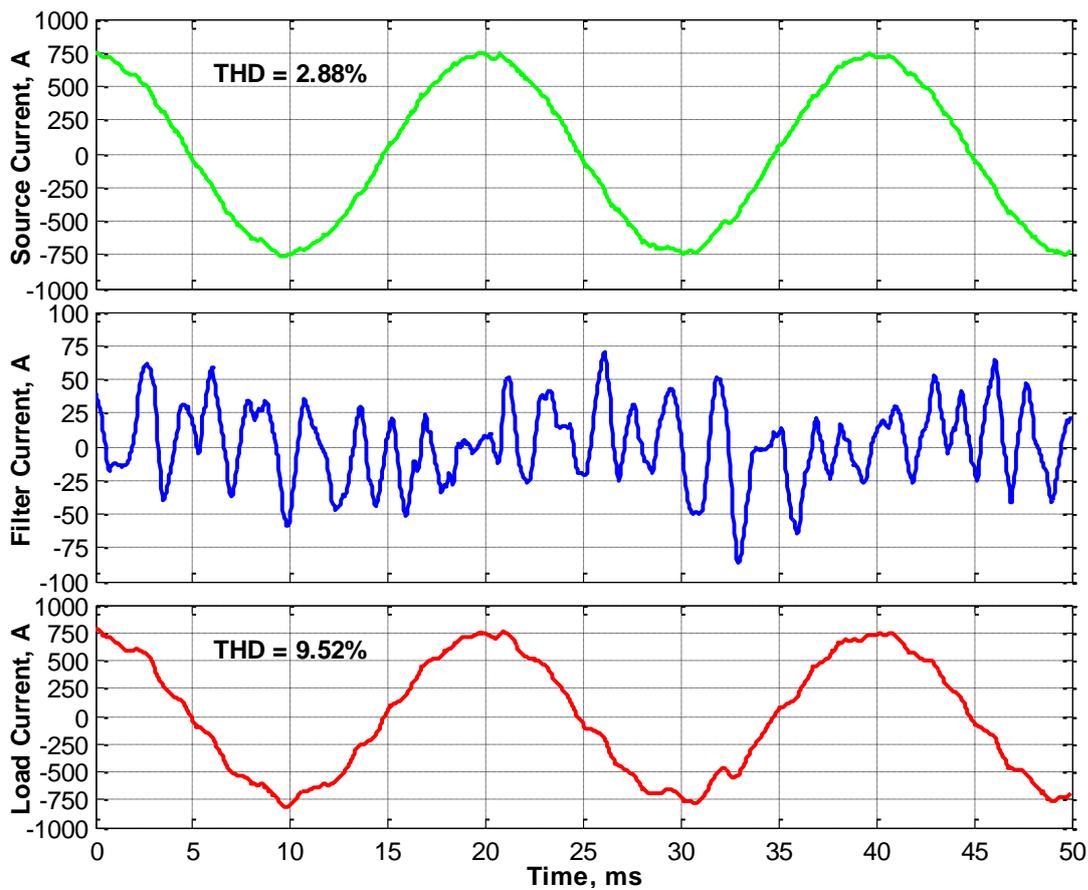
Figure 4.25 Source, HAPF and load current measurements while three IMFs are simultaneously in operation

Table 4.2 Summary of Harmonic Filtering Performance

	1 IMF	2 IMFs	3 IMFs
Load THD	9.52%	9.44%	9.52%
Source THD	3.07%	3.93%	2.88%

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The filtering performances of the implemented HAPF system are summarized in Table 4.2 for the simultaneous operation of one, two and three IMF loads. The table shows that the designed and implemented HAPF system is successful for the each of the duty regime. However, since those THD values are calculated for a specific instant, it is essential that the THD values should be calculated for a longer period of time at least a melting period long (around 45 minutes [17]). For this reason, THD value is calculated for source current waveform during 75 minutes and given in Figure 4.27, which verifies the performance over the whole melting cycle.
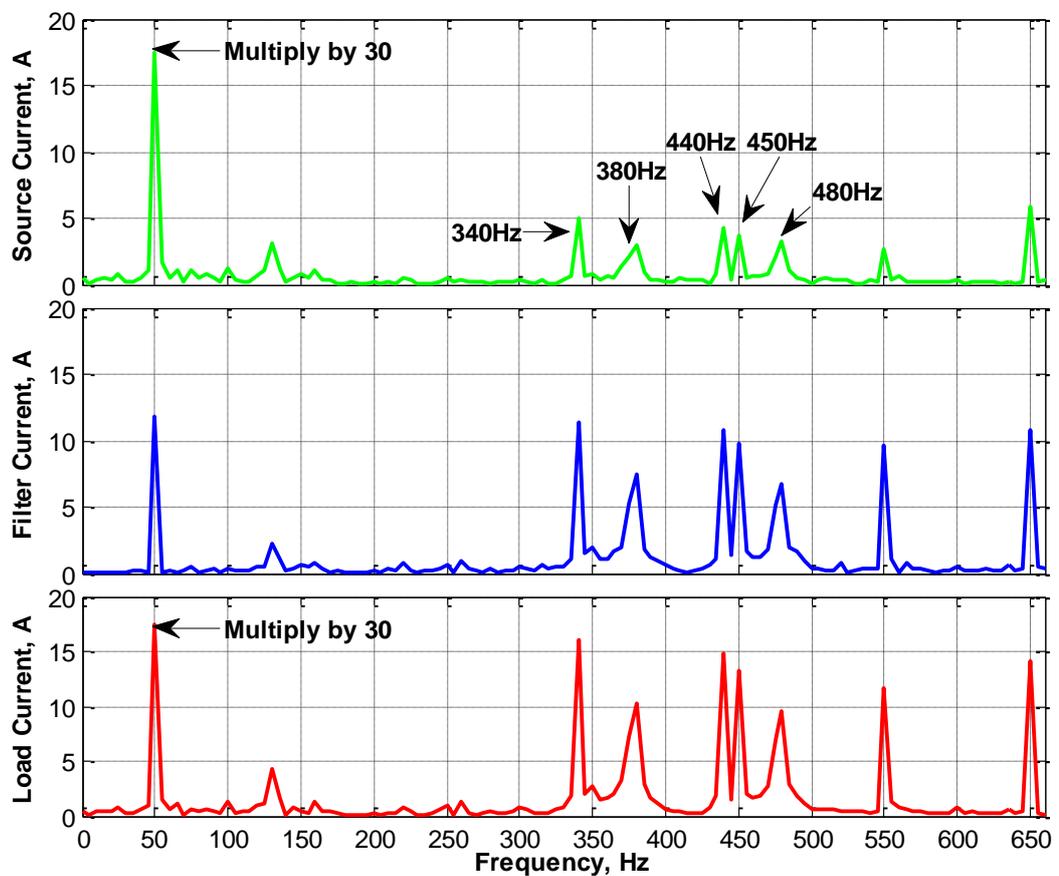
Figure 4.26 Harmonic spectra of the source, HAPF and load current waveforms while three IMFs are simultaneously in operation

It should be noted that the IMF load driver operating frequencies for each IMF depend on the quality of the metal molded, the phase of metal melting process and extra

material charges to the ladle. Although it is observed in the field that usual working regime yields an increase in operating frequency during standard metal melting process, different iron ore percentages and indiscriminately charging of metals to the ladle during process cause a random behavior for the IMF load harmonics and interharmonics.
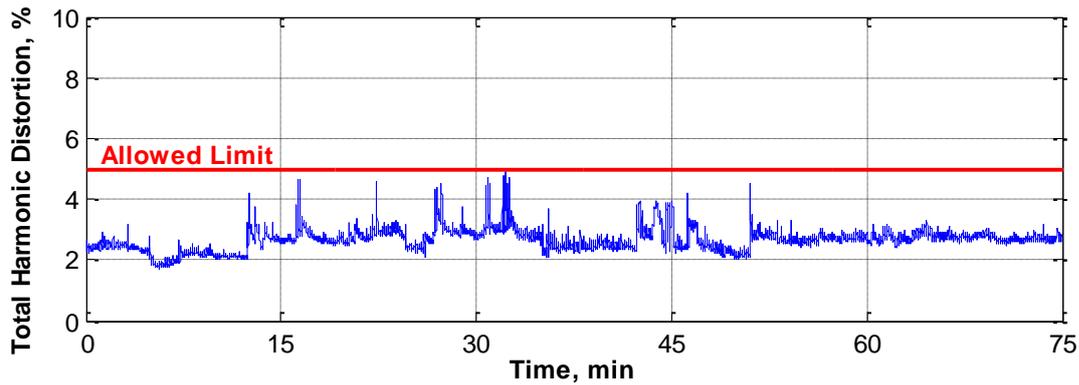
Figure 4.27 Total Harmonic Distortion, THD, of the source current waveform at MV side (field measurements)
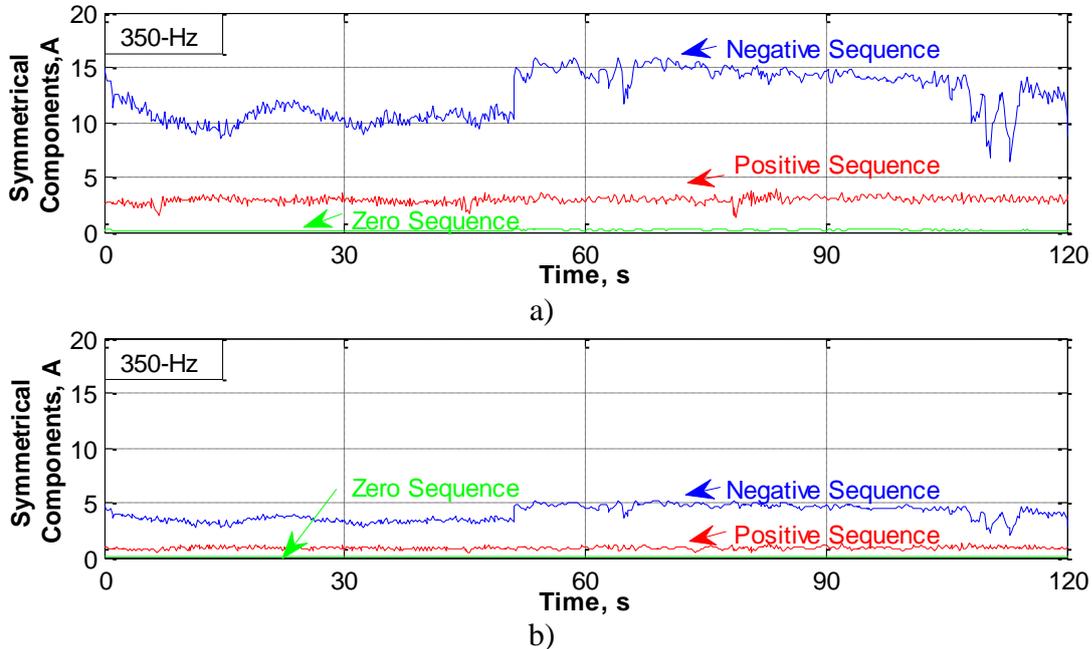
Figure 4.28 Simultaneous appearance of both negative and positive sequences for 350 Hz at a) load current and b) source current

Each IMF load, as mentioned in previous sections, causes two interharmonic frequencies 100 Hz apart from each other due to the cross-modulation phenomenon, where the smaller frequency is negative and the greater is positive sequence form for three phase systems. When two or more IMF installations are simultaneously in operation, any interharmonic may appear positive, negative, or both at the same time. Figure 4.28.a and Figure 4.29.a shows the field measurements of the load current containing both positive and negative sequences at the same time respectively for 350 and 435 Hz harmonic frequencies. The proposed HAPF system has also shown to be successful under balanced but unsymmetrical working conditions as can be understood from the source current field measurements given in corresponding figures Figure 4.28.b and Figure 4.29.b.
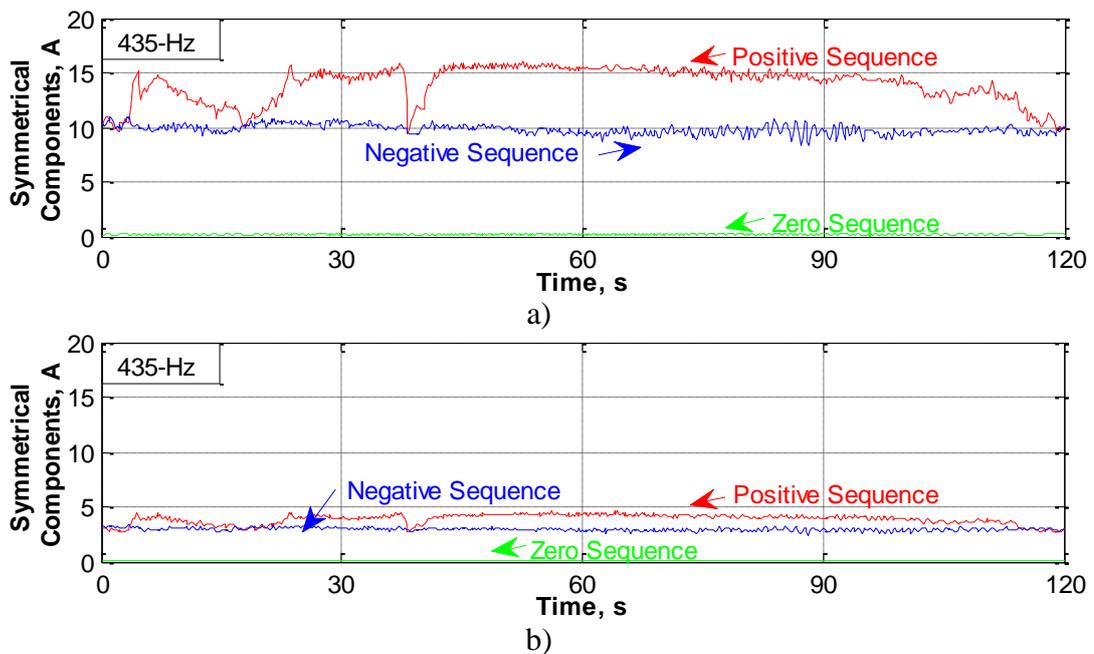
Figure 4.29 Simultaneous appearance of both negative and positive sequences for 435 Hz at a) load current and b) source current

In addition to MV results, HAPF unit currents of each of the converter should also be analyzed at LV level. For this purpose, the oscilloscope recordings have been drawn in Figure 4.30.a together with the illustration of approximate reference signal and

corresponding high and low hysteresis bands. The characteristics of hysteresis switching can easily be understood from this figure. It is also shown in Figure 4.30.a that the HAPF unit current waveform usually passes the hysteresis bands, the reason of which is explained in detail at Chapter 5.2. In order to evaluate the occurrence of hysteresis bands violations, reference tracking error of the corresponding waveform, in Figure 4.30.a, is given in Figure 4.30.b. The hysteresis switched current of the converter exceeds the hysteresis bands by up to 250A, which should cause high frequency components in the harmonic spectrum.
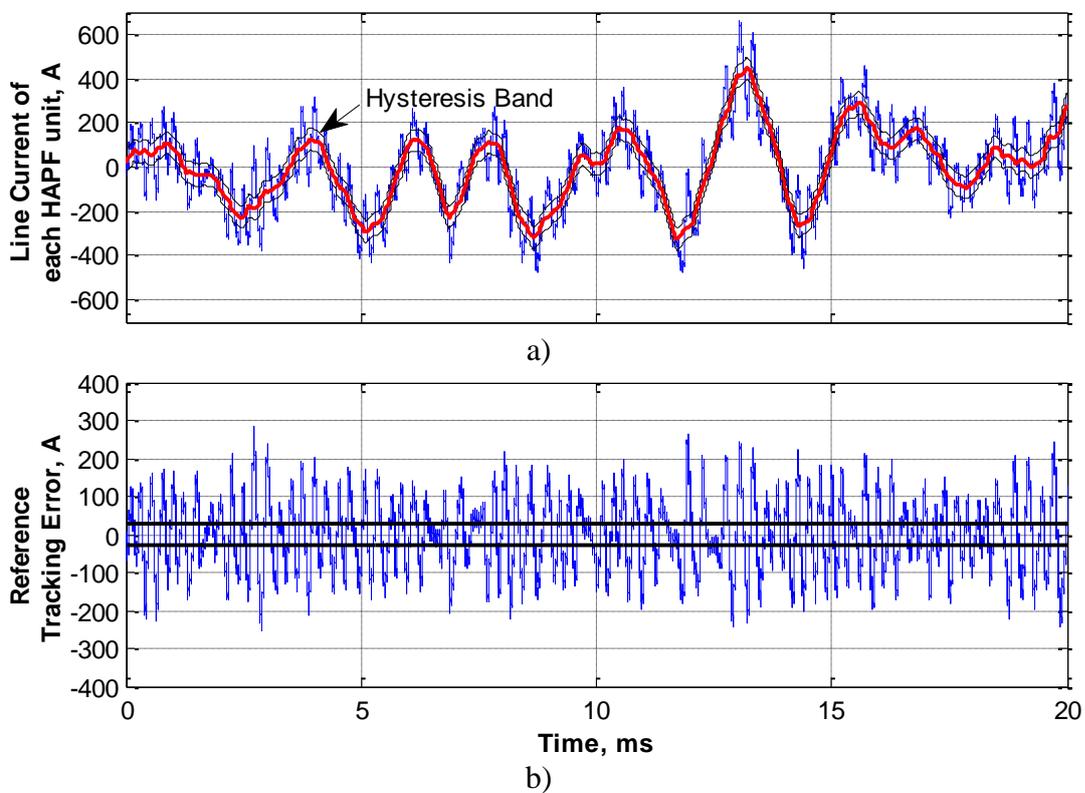
Figure 4.30 a) Line current waveform of each HAPF units, tracked reference, implemented hysteresis bands, and b) corresponding reference tracking error

The harmonic spectrum for examining the dominant harmonic and interharmonic content of the corresponding waveform is given in Figure 4.31.a using the 200msec window (5-Hz resolution) of oscilloscope recordings. As shown in this figure, the

dominant interharmonic pairs due to the IMF working regime are 315 - 415 Hz and 330 – 430 Hz. Those interharmonic frequencies correspond to a simultaneous operation of two IMF installations with driver operating frequencies 182.5 Hz and 190 Hz, respectively. As mentioned before, there should also be high frequency components due to the hysteresis switching. The harmonic spectrum showing the higher frequencies is given in Figure 4.31.b. The high frequency harmonic components are distributed, as expected, from 3 kHz to 4.5 kHz. Unfixed switching frequency can be considered as a drawback of hysteresis current control method [89], [120], [126] and the switching frequency can be fixed to a certain value using advanced methods [111], [114], [119], [127], which is not the subject of this research work.

a)

b)
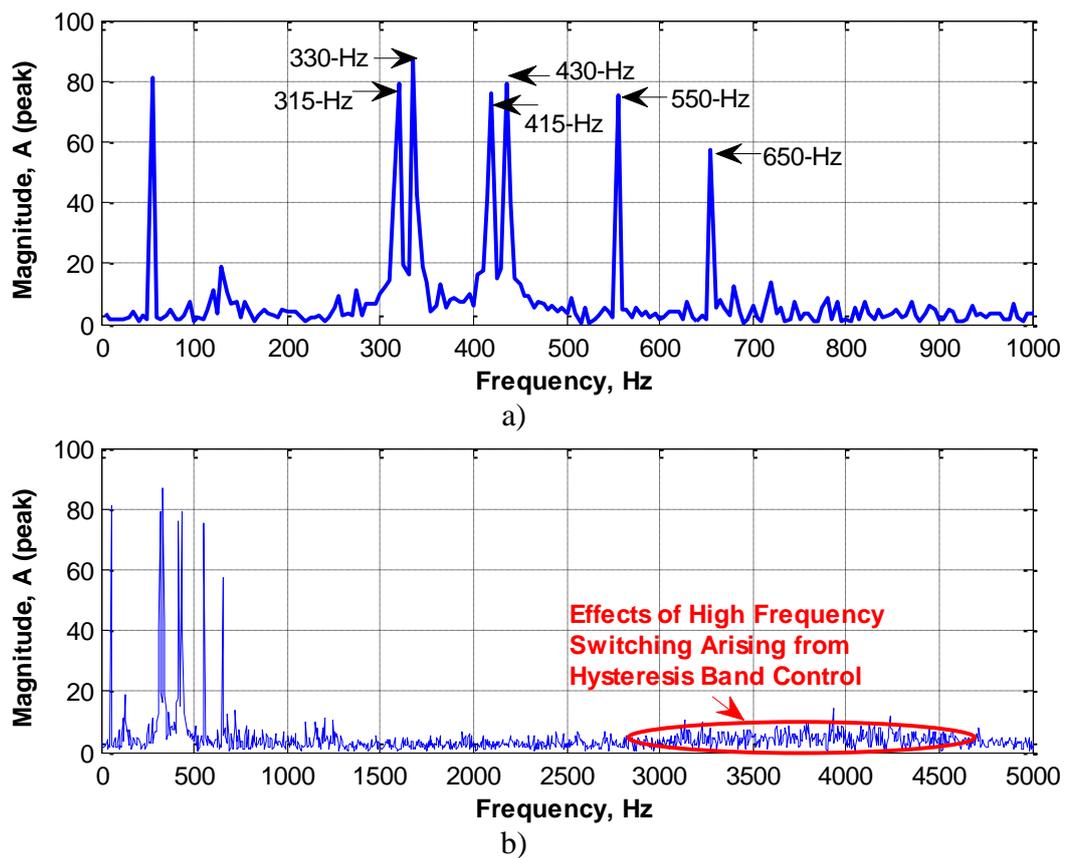
Figure 4.31 Harmonic spectrum of the HAPF unit currents a) dominant harmonics and interharmonics, and b) high frequency components due to hysteresis switching

Mitigation of each individual harmonic is important because of the suggested limits for each integer multiple harmonics of the fundamental frequency in standards [1], [28] and grid codes [30]. Otherwise, excessive operating penalties may be charged to the electricity users. The allowed limits for each individual current harmonic are as given in Table 1.2. Only harmonics corresponding to odd and even multiples of fundamental frequency have limits as can be seen from Table 1.2. Unfortunately, there is not any regulation on interharmonics because of the fact that traditional industrial loads only creates harmonics due to fundamental frequency voltage causing only integer multiples of current harmonics as mentioned in the first chapter of this thesis.

The detailed analysis for all current harmonic components up to 40th harmonic is given in Appendix C during the field measurement period of 26 days, and all the individual subgroup harmonics except 23rd and 25th components are shown to be within allowed limits by standards. Nevertheless, this criteria is not enough for the performance evaluation of the proposed HAPF system since the IMF load harmonics to be suppressed are distributed among a wide frequency range. For this reason, a novel performance criteria, namely Suppression Factor (SF), is proposed in this research work for a wide frequency filtering equipment and described in the following section.

4.6.1. Suppression Factor as an Evaluation Criteria for Wide Frequency Filtering Equipment

Harmonics and interharmonics caused by industrial loads can be mitigated by using various active and/or passive power filtering equipment. Those filtering equipment can be optimized for increased suppression performance when the frequency range of harmonics to be mitigated is narrow. On the other hand, performance of filtering equipment may be different for each harmonic frequency, if the frequency range of harmful harmonics is wide. For this reason, a novel performance evaluation criteria should be defined for these kind of filtering equipment; since their characteristics may change as the frequency changes. Some researchers have been using performance evaluation methods [163] – [167]; nevertheless, neither of them gives satisfactory

information about the effectiveness of filtering equipment over a wide frequency range.

In this part of the thesis, a novel performance evaluation criteria for wide frequency harmonic filtering equipment, SF, is proposed. Theoretical calculations of SF for various active and passive filter topologies have been given. The behavior of APF and HAPF under different control methods have been analyzed theoretically in terms of SF. Moreover, field implementation results and recordings of both proportional control method and hysteresis band control method under investigation of this thesis have been compared in terms of SF criteria.

4.6.1.1. Definition of Suppression Factor

Although all of the filtering equipment are designed to inject current or voltage having exactly the same magnitude and anti-phase to load side reference signal, it may not be the case in practice. Filtering devices may fail to track the reference resulting in some magnitude and/or phase errors. Since the vector sum of load and filter current or voltage forms the source side current or voltage, the phase and magnitude of the filter side have a great importance for an effective filtering, which is illustrated in Figure 4.32. Although SF can be used for both current and voltage harmonics, it will be used, from now on, for the current harmonics in order to relate it to the specific case being investigated in this thesis.
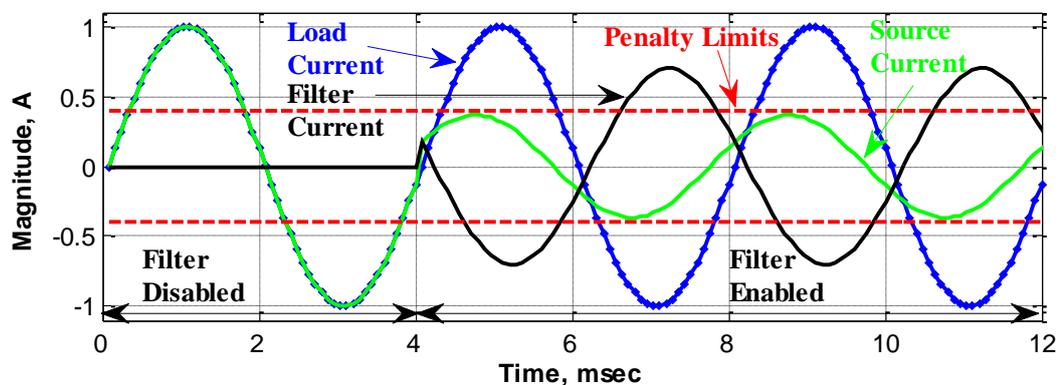
Figure 4.32 Illustration of practical filtering for a sample harmonic frequency

SF, as a novel criteria, is an indicator of the effective percent of the filter current magnitude which provides a decrease in source current magnitude for each individual harmonic frequency [168]. Its mathematical expression is given in (4.1).

$$\% SF_h = \frac{\left|I_{h,load}\right| - \left|I_{h,source}\right|}{\left|I_{h,filter}\right|} x100 \qquad (4.1)$$

Percentage SF of 100% for a harmonic component indicates that the filter current is in correct phase (anti-phase) with the load current for that harmonic component. This does not mean that the corresponding frequency totally vanished, instead it shows that the amount of injected filter current cause the same amount of decrease in source current for that particular frequency. Figure 4.32 shows the illustration of a practical filtering for a sample harmonic component. As can be observed from Figure 4.32, the magnitudes of load, filter and source current waveforms are 1.0, 0.7 and 0.38 units, respectively. This means that only 0.62 units of load current can be suppressed by 0.7 units of filter current, which yields 88.6% suppression factor.

4.6.1.2. Evaluation of Various Filtering Equipment

In this section, theoretical evaluations of various passive and active filtering topologies are analyzed. Used filter topologies and their harmonic equivalent circuits are given in Figure 4.33. Single-tuned passive shunt harmonic filter (Figure 4.33.c), combination of passive shunt filters (Figure 4.33.d), voltage mode controlled APF (Figure 4.33.e), and voltage mode controlled HAPF (Figure 4.33.f) topologies are selected for the evaluation in terms of SF criteria. Since the frequency range of the IMF load under investigation by this thesis is from 250 to 550 Hz, those sample filter topologies are evaluated for this frequency range.
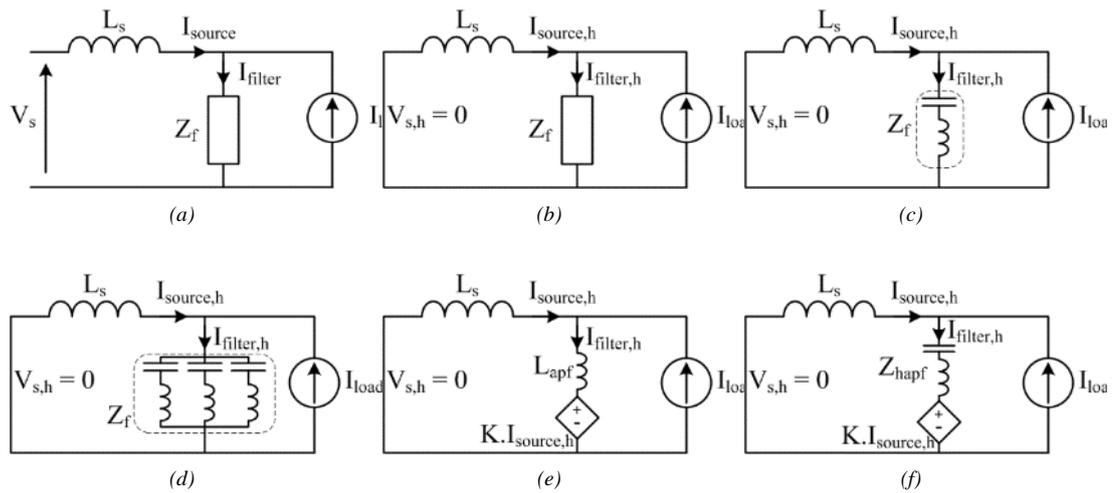
Figure 4.33 a) Generalized equivalent circuit, b) generalized harmonic equivalent circuit for c) single-tuned passive filter, d) combination of passive filters, and proportional controlled e) APF and f) HAPF.

Theoretical curves of the single tuned shunt harmonic filter topology in Figure 4.33.c is given in Figure 4.34. The tuning frequency is chosen to be the midway of the whole frequency range so that as much frequency components as possible are covered by the filter characteristics. As can be observed from Figure 4.34 that, this filter topology is very successful for the frequency components near tuning frequency; however, it has almost no effect for the rest of the frequency components. Although, decreasing Q factor increases the suppression performances of some other frequencies, it is not possible to decrease the Q factor to cover the whole frequency range.
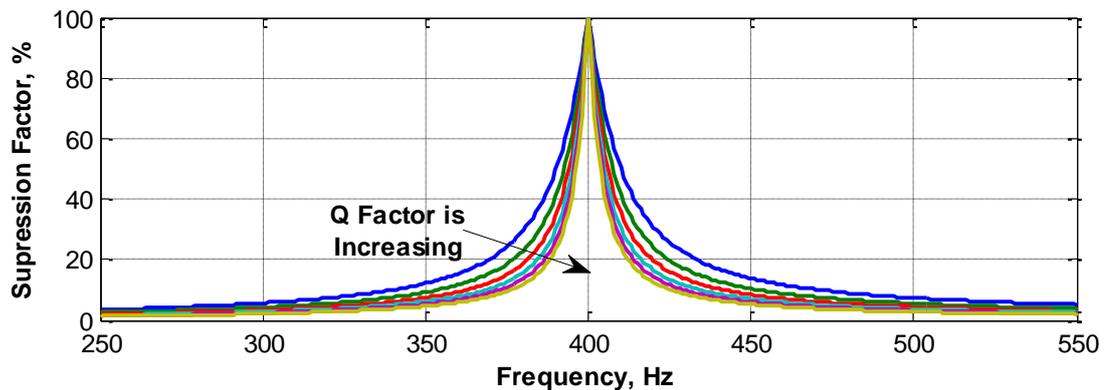
Figure 4.34 Theoretical Suppression Factor for single-tuned passive filter topology given in Figure 4.33.c

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An improvement on the SF values for a wider frequency range can be provided by using combination of passive harmonic filters each of which is tuned to different frequencies as illustrated in Figure 4.33.d. Figure 4.35 shows the theoretical SF values for the combination of three shunt harmonic filters. Tuning frequencies of those filters are chosen so that as much frequency components as possible are covered by the filter characteristics. This filter topology provides more effective suppression as compared to single tuned passive shunt harmonic filter, however, it has still limited SF values over the whole frequency range. This topology provides very effective suppression around tuning frequencies at the expense of reduction in suppression performance in between tuning frequencies. Although, decreasing Q factor increases the suppression performances of some other frequencies nearby each tuning frequency, it still has no effect to the frequencies lay in between tuning frequencies.
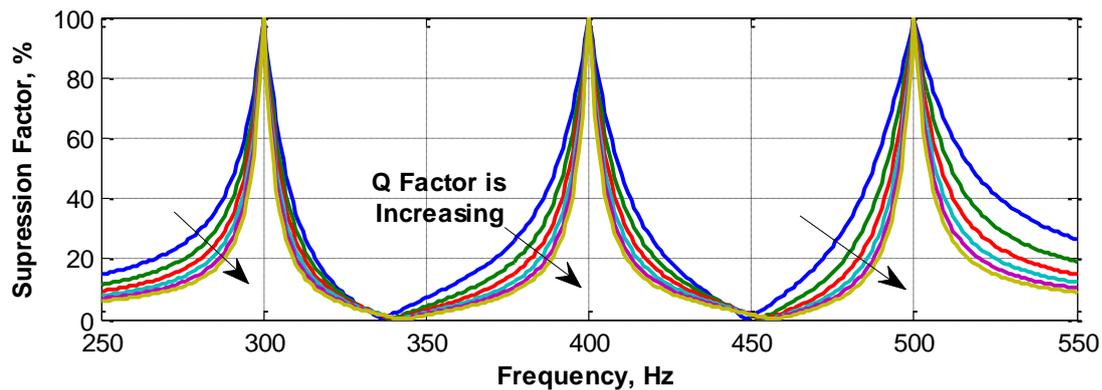
Figure 4.35 Theoretical Suppression Factor for combination of passive filters given in Figure 4.33.d.

To overcome the problems of passive filters, active filtering solutions has been used by various researchers. Sample APF and HAPF topologies are also analyzed in terms of SF. In addition, their control method should also be considered for evaluating their suppression performance. Proportional control method, described previously as a conventional control method in earlier chapters, is used as the control method for the sample APF topology given in Figure 4.33.e. Figure 4.36 illustrates the SF curves of

the APF system. As expected, APF system is much more effective for the suppression of harmonics spread in a wide frequency range. As can be seen from Figure 4.36, increasing proportionality constant improves the suppression performance however, it cannot be increased to high levels due to the stability problems.
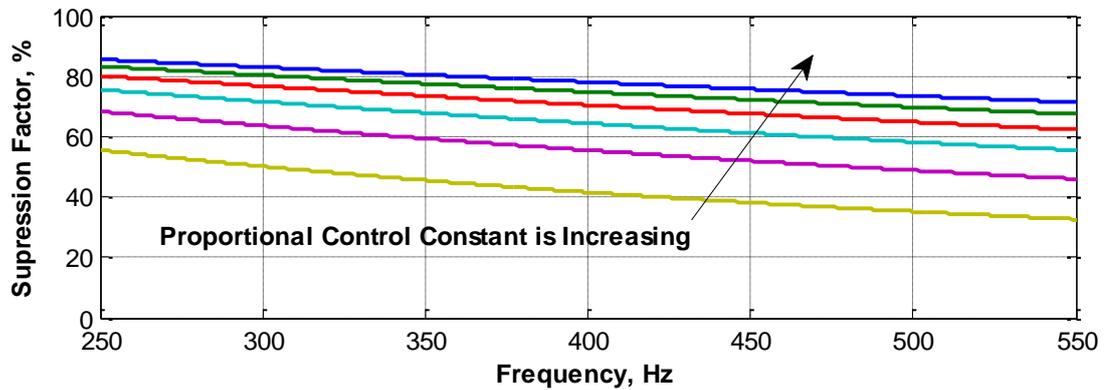
Figure 4.36 Theoretical Suppression Factor for proportional controlled APF topology given in Figure 4.33.e
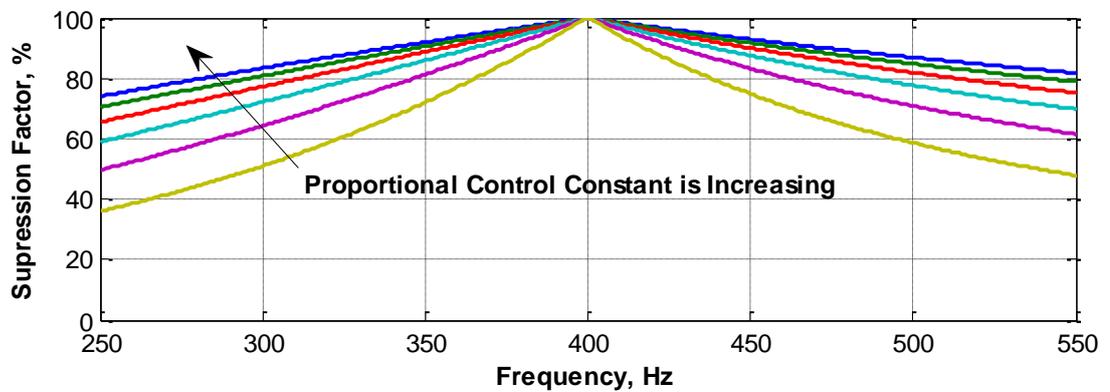
Figure 4.37 Theoretical Suppression Factor for proportional controlled HAPF topology given in Figure 4.33.f

HAPF converter topology, illustrated in Figure 4.33.f, can be used to increase SF values over the whole frequency range due to its impedance characteristics. Passive part tuning frequency should be tuned to the midway of the whole frequency range so

that its characteristics show low impedance for as much frequency as possible. Figure 4.37 illustrates the theoretical suppression factor for the HAPF system controlled by proportional control method. As can be seen from this figure, suppression performance of HAPF topology is very high around tuning frequency, and modest as the frequency gets far from tuning frequency. Similar to APF case, increasing proportionality factor improves the suppression performance however, it cannot be increased to high levels due to the stability problems.

4.6.1.3.   Evaluation of Proposed Hysteresis Band Current Controlled HAPF Topology

After finding out that HAPF topology is superior to passive and APF topologies, it is necessary to find proper control method for maximum suppression performance. Since the proportional control method is a voltage mode control method, it has a dependency on the coupling element impedance characteristics as mentioned in earlier sections. An adaptive proportional resonant control algorithm can improve the suppression performance at the expense of excessive computational burden. Using current mode control methods, on the other hand, helps the improvement of suppression performance due the fact that they track the reference current resulting in almost no phase error for each harmonic frequency. For this reason, hysteresis band current controlled HAPF topology, given in Figure 4.38, proposed in this thesis is able to have 100% of SF over the whole frequency range, theoretically. Figure 4.39 shows the SF values of the proposed hysteresis band current controlled HAPF topology by using the field measurements.
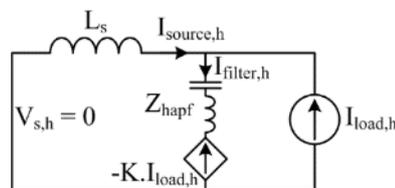
Figure 4.38 Harmonic equivalent circuit of HAPF controlled with proposed hysteresis band control method

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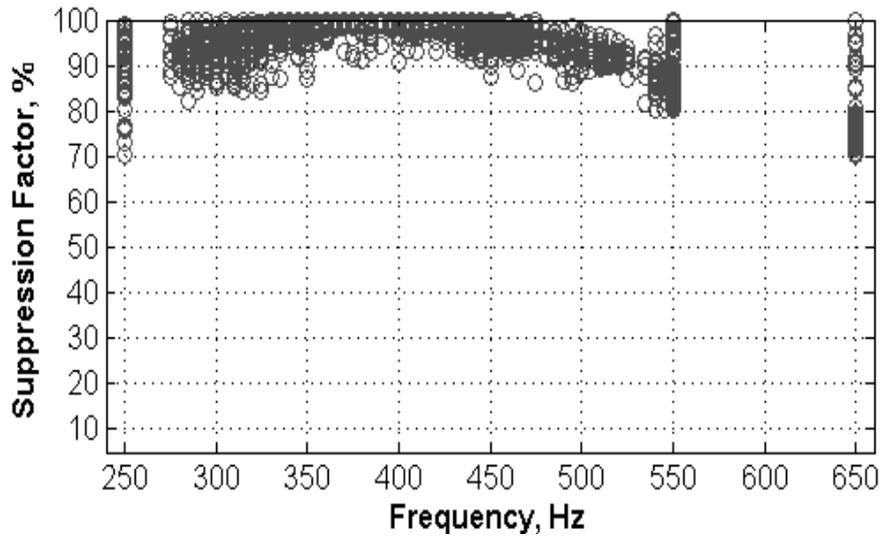
Figure 4.39 Harmonic suppression performance of HAPF system with proposed hysteresis band control (deduced from field measurements)

It can be deduced from Figure 4.39 that the proposed method provides SF values above 90% for most of the interharmonic and harmonic frequency. The SF graph is formed in a cloud diagram form so that the suppression performance can be observed over a long time interval including loading transients. Each point in SF cloud diagram represents the calculation of SF for a specific harmonic frequency corresponding to each 200 msec window during a whole recording time. By this way, SF value of each harmonic frequency can be calculated tens of times to give a clue for the long term and dynamic performance.

CHAPTER 5

FURTHER IMPROVEMENTS ON HYSTERESIS BAND CONTROL

Following the successful implementation and tests of hysteresis band control in the field on a steel melting facility, it is found out that there are some points ,which still need to be clarified and can be further improved, on the system and control algorithm. In this chapter of the thesis, some further improvements and analysis for the critical issues about hysteresis band control are addressed.

The proposed control system mentioned in Chapter 4 very successfully suppresses all the harmonics and interharmonics however it has some disadvantages due to nature of hysteresis band modulation technique. The most important disadvantage is having high and irregular switching frequencies thus high switching losses [91]. Therefore, as a first section of this chapter, a novel fuzzy logic based adaptive hysteresis band generation method for the reduction of switching losses has been proposed [169]. Then, the possible reasons for the hysteresis band tracking errors are formulized and some solutions to that problem is suggested as another section.

5.1. Adaptive Fuzzy Hysteresis Band Control for Reducing the Switching Losses

Fuzzy Logic Control (FLC) algorithms have been used for the control of different industrial power converters. [108], [117], [118], [169], [170] – [178]. The most common application of FLC on APFs is to use it for the dc link regulation of the converter [118], [172], [173] because of its known advantages as compared to

traditional PI control [172], [173]. On the other hand, some other works in literature have already proposed FLC for the generation of adaptive hysteresis band [108], [174] – [178]. Width of the hysteresis band has been changed adaptively by making use of fuzzy expressions for a series APF [174], shunt APFs [175], [176], motor drive converter [108], and grid connected inverters [177], [178].

In this part of the thesis, a novel adaptive fuzzy hysteresis band current control system is proposed by making use of fuzzy expressions for both HAPF current and integral of its harmonic components. By this way, the switching losses of the semiconductor switches of the HAPF converter is reduced notably without any significant change in reference tracking performance.

5.1.1. Formulation of Fuzzy Control Parameters

In order to represent the hysteresis bandwidth by the fuzzy expressions, the circuit diagram in Figure 2.6 should be analyzed. If the grid voltage and the converter itself are considered as voltage sources, circuit diagram in Figure 2.6 can be represented as a single phase equivalent circuit shown in Figure 5.1. The voltage loop equation in Figure 5.1 can be written as (5.1). In order to simplify (5.1) and reach meaningful results, a couple of assumptions should be made.

$$-v_S(t) + \frac{1}{C_f}\int i_f(t)dt + v_{CO} + L_f\frac{di_f(t)}{dt} + v_{inv}(t) = 0 \tag{5.1}$$
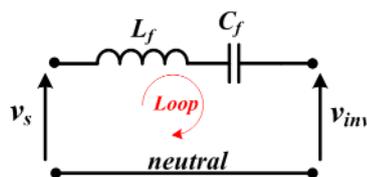
Figure 5.1 Single phase equivalent circuit of the HAPF converter

Assumption 1 – Blocking Capacitor Assumption: The impedance of the input LC filter is designed such that it behaves as almost capacitive impedance at fundamental frequency. Also, converter is controlled in order not to generate voltage components

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at fundamental frequency too, except a negligibly small amount for dc link regulation as mentioned in earlier chapters of the thesis.

By making use of those information, the source voltage at fundamental frequency can be assumed to appear totally on the terminals of the filter capacitor as a voltage drop [70], yielding (5.2).

$$v_S \cong v_{CO} + \frac{1}{C_f} \int i_{f,fund}(t)dt \tag{5.2}$$

By using assumption 1, the voltage loop equation in (5.1) can be simplified as given in (5.3). Rearranging (5.3) turns out to be (5.4).

$$\frac{1}{C_f} \int i_{f,harm}(t)dt + L_f \frac{di_f(t)}{dt} + v_{inv}(t) = 0 \tag{5.3}$$

$$\frac{di_f(t)}{dt} = -\frac{v_{inv}(t)}{L_f} - \frac{1}{L_f C_f} \int i_{f,harm}(t)dt \tag{5.4}$$
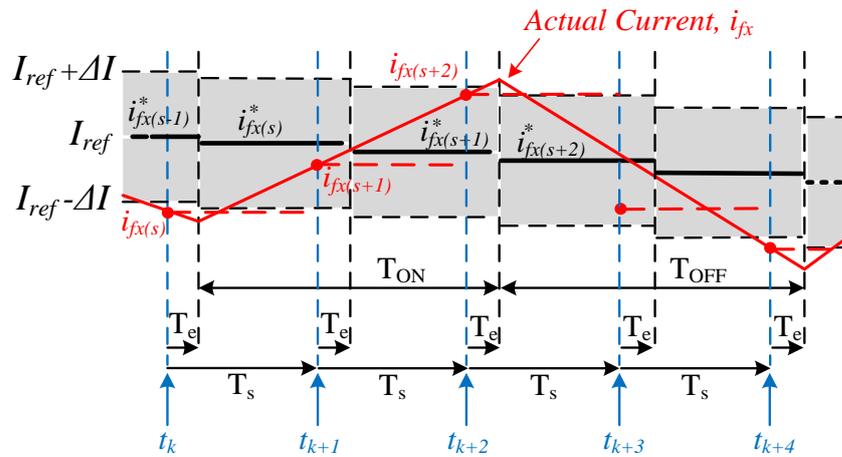
Figure 5.2 Illustration of sample switching for the digital implementation of hysteresis current control

In order to observe the mathematical model of hysteresis switching by using (5.4), an illustration showing the digital implementation of hysteresis band is given in Figure 5.2. In Figure 5.2, T_e stands for the execution time, the time needed for the completion of all control duties, T_s the sampling period, i_{fx} the actual current waveform of phase

x, I_{ref} the reference current signal and ΔI the hysteresis band. For the sake of simplicity, only two switching instants are illustrated. There needs to be another assumption for the proper formulization of switching period by (5.4) and Figure 5.2.

Assumption 2 – Linear LC Filter Response and Fast Control Hardware Assumption: It is assumed that the control hardware is fast enough so that the execution time, T_e, and sampling period, T_s, are small enough so that the reference tracking error is negligible as compared to hysteresis band ΔI. Moreover, the hysteresis band, ΔI, is small enough thus the LC filter response can be considered linear [89].

By using the linear switching behaviors, T_{on} and T_{off} time intervals in Figure 5.2 corresponding respectively to switch on and off periods can be approximated as given in equations (5.5) and (5.6). Rearranging (5.5) and (5.6) results to (5.7) and (5.8), which are the mathematical formulization of T_{on} and T_{off} time intervals.

$$\frac{\Delta i_f}{T_{ON}} = \frac{v_{inv}(t)}{L_f} - \frac{1}{L_f C_f}\int i_{f,harm}(t)dt \tag{5.5}$$

$$\frac{\Delta i_f}{T_{OFF}} = \frac{v_{inv}(t)}{L_f} + \frac{1}{L_f C_f}\int i_{f,harm}(t)dt \tag{5.6}$$

$$T_{ON} = \frac{L_f \Delta i_f}{v_{inv}(t) - \frac{1}{C_f}\int i_{f,harm}(t)dt} \tag{5.7}$$

$$T_{OFF} = \frac{L_f \Delta i_f}{v_{inv}(t) + \frac{1}{C_f}\int i_{f,harm}(t)dt} \tag{5.8}$$

Since the switching period, T_{sw}, for any instant can be considered to be the sum of switch on and off time intervals, switching period can be found as given in (5.9).

$$\frac{1}{f_{SW}} = T_{SW} = T_{ON} + T_{OFF} = \frac{2v_{inv}(t)L_f \Delta i_f}{v_{inv}(t)^2 - \left(\frac{1}{C_f}\int i_{f,harm}(t)dt\right)^2} \tag{5.9}$$

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It should be noted that reaching (5.9) can only be possible by assuming inverter terminal voltage, v_{inv}, to be the same for T_{ON} and T_{OFF} time intervals which is not always the case as mentioned in Chapter 2. This assumption is valid because (5.9) is only used for showing a relation between parameters instead of reaching an exact result. Indeed, these proportional relations are enough for creating a fuzzy relation between switching frequency and integral of harmonic currents, there is no need for exact proportionality factors or equations doing so. Especially for three phase three wire converters, converter voltage at any phase strongly related to the switching positions of others as mentioned earlier. This situation shows that the fuzzy relations rather than exact relations can be more useful to determine the proper hysteresis band for this particular application.

It obvious at (5.9) that the hysteresis bandwidth and the switching frequency is inversely proportional to each other. Thus this equation can also be used for deducing a fuzzy relation between switching frequency thus switching losses and integral of harmonic currents. As can be understood from (5.9) that the integral of harmonic currents are inversely proportional to switching frequency. Therefore if integral of harmonic currents is represented by linguistic expressions like "HIGH" and "LOW", hysteresis band would be narrowed without considerable increase in switching frequency for "HIGH" valued integral of harmonic currents. Similarly, hysteresis band should be widened in order not to increase switching losses for "LOW" valued integral of harmonic currents.

Furthermore, it is widely known that the switching losses on a semiconductor switch is proportional to switched current. Similar to previous condition, hysteresis band can be narrowed for "LOW" values of HAPF current in order to provide better reference tracking. If the HAPF current is "HIGH", on the other hand, hysteresis band should be widened in order to reduce switching frequency thus switching losses.

In this thesis, a complete method making use of both HAPF current and the integral of its harmonic currents is proposed to generate novel adaptive fuzzy hysteresis bands. The proposed improvement has been implemented in the field [169].
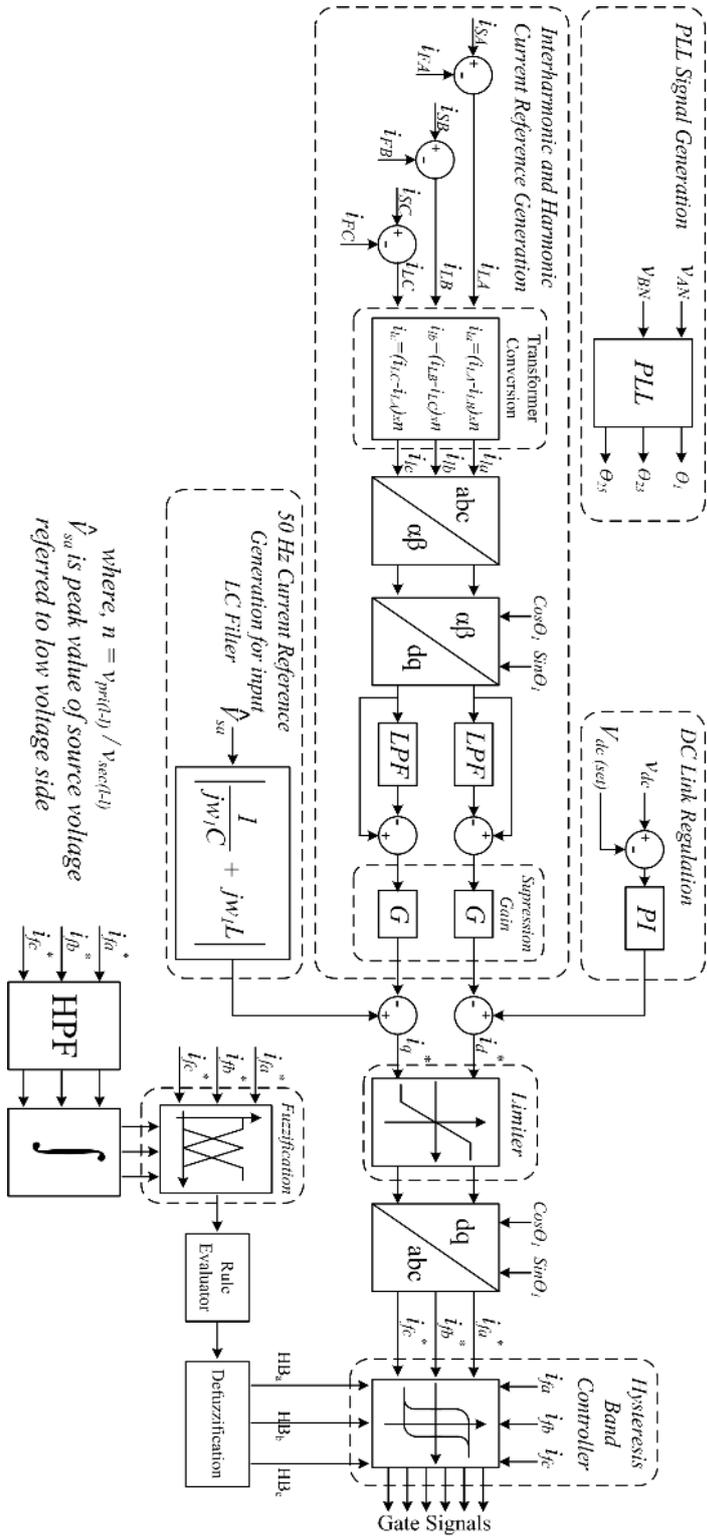
Figure 5.3 Control block diagram of the adaptive fuzzy hysteresis band control method

The block diagram representing the overall control system together with integrated adaptive fuzzy hysteresis band generation technique is given in Figure 5.3. As can be seen from Figure 5.3, interharmonic and harmonic current reference generation block, the same as fixed hysteresis band control proposed in Chapter 2, calculates the current signals to be tracked. In order to satisfy other requirements of control system, PLL signal generation, DC link regulation and 50Hz reference generation blocks are already integrated into the overall control block diagram in Figure 5.3. The ultimate current references are then limited and back-transformed to abc domain. This form of reference signal is ready for the modulation to create gate pulses by hysteresis band controller with the provided adaptive fuzzy hysteresis bandwidth.

5.1.2. Generation of Linguistic Expressions and Fuzzy Hysteresis Band

Adaptively changing hysteresis bandwidth is generated by a sequence of processes, those processes are explained in this section in detail. At first, the HAPF line current and integral of its harmonic currents should be mapped to proper linguistic expressions. In order to reach this aim, there is a need for fuzzy membership functions corresponding to each linguistic expression.

In this particular research, those fuzzy membership functions have been determined with the help of Fuzzy Logic Toolbox of MATLAB by using the real field data and switching loss model formed in EMTDC/PSCAD simulation environment. HAPF current values are divided into four linguistic expressions as given in Figure 5.4, namely "VERY LOW", "LOW", "HIGH", and "VERY HIGH", by using the MATLAB toolbox. The resultant fuzzy membership functions have been linearized for the sake of reduced computational burden in control hardware and they are tuned for optimized switching loss results via simulations in PSCAD environment as given in Figure 5.5. Similarly, integral of harmonic currents also divided into two linguistic expressions, namely "HIGH" and "LOW", and their membership functions are determined by manual iterations conducted in PSCAD simulation environment. It is

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also known that the fuzzy membership functions can be optimized using advanced techniques like neural networks [171]. The linearized and manually optimized fuzzy membership functions are as given in Figure 5.6.a and b, respectively for HAPF current and integral of its harmonic currents.
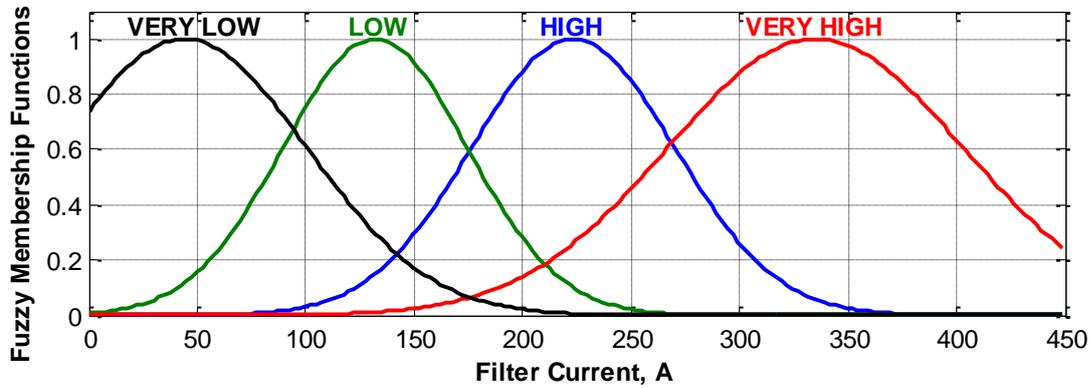
Figure 5.4 Fuzzy membership functions of input variable HAPF current (MATLAB Fuzzy Logic Toolbox)
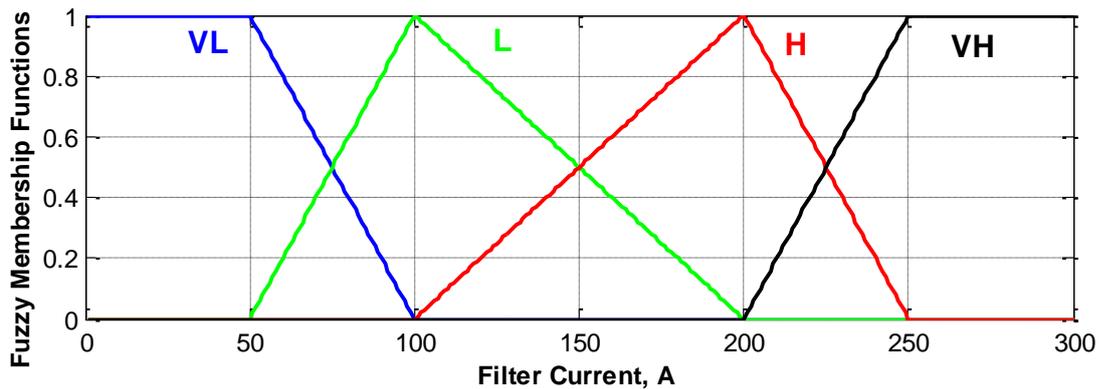
Figure 5.5 Fuzzy membership functions of input variable HAPF current (Manually optimized using PSCAD)

Once fuzzy membership functions are determined and instantaneous HAPF current and integral of its harmonic currents are mapped with fuzzification process to defined linguistic expressions, there should be a Fuzzy Rule Matrix in order to evaluate the resultant linguistic expressions. This matrix defines the necessary narrow or widen act of the hysteresis band for corresponding linguistic expressions. Considering the previously mentioned relation between linguistic expressions and the hysteresis band

narrowing or widening act, a Fuzzy Rule Matrix, given in Table 5.1, is used for the proposed control method. Using the matrix given in Table 5.1, the degree of membership for the output variables to the narrow or widen act can be determined. There are six output linguistic variables namely "N", "NN", "NNN", "W", "WW", and "WWW", where "N" corresponds to "Narrow", "W" corresponds to "Widen", two and three successive letters respectively represent more and much more "Narrow" or "Widen" act.
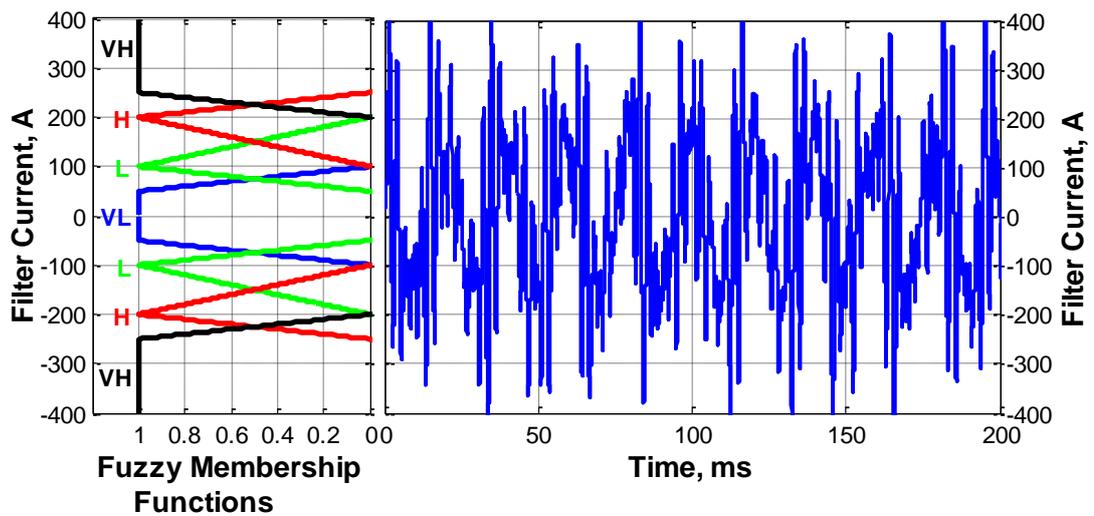
a)
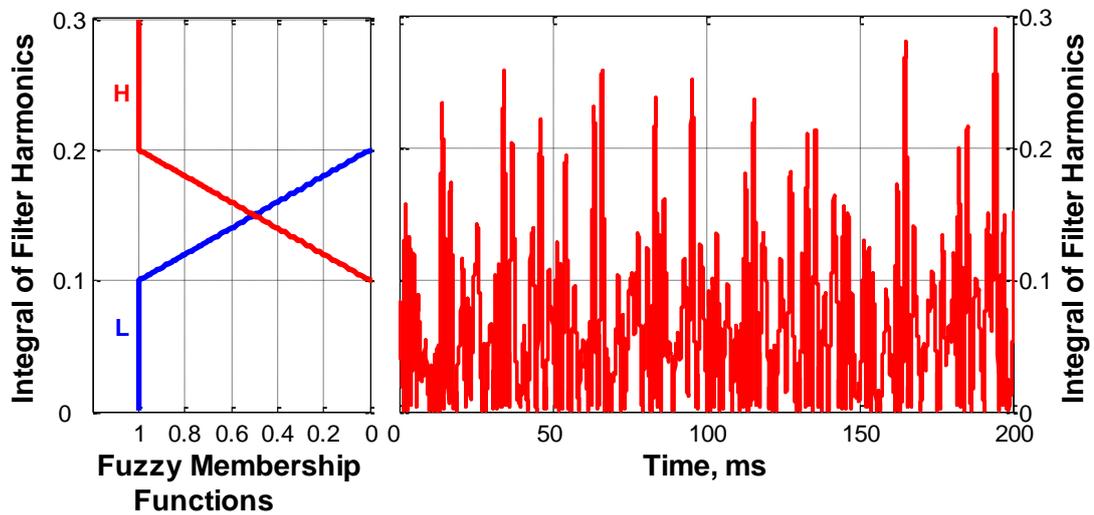
b)

Figure 5.6 Fuzzy membership functions of a) HAPF current and b) integral of its harmonic currents together with corresponding waveforms

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Table 5.1 Fuzzy Rule Matrix

		i_{ref}			
		Very Low	Low	High	Very High
$\int i_{ref,h}$	Low	NN	N	WW	WWW
	High	NNN	NN	W	WW

The mapping of input variables to the output ones is obtained in two steps. First, a temporary value, T_{ij}, is given to each element of the rule matrix located in i^{th} row and j^{th} column by taking the minimum of the membership degrees of the corresponding rows and columns. For example, T_{13} is determined by the minimum of the degree of membership of the filter current to "HIGH" variable and the degree of membership of the integral of the current harmonics to "LOW" variable. Second, the degree of membership of the output variables "N", "NN", "NNN", "W", "WW", and "WWW" can be determined by the criteria given in Eqns. (5.10)– (5.15). It should be noted that, at any instant during operation, more than one output variable may contain non-zero values.

$$D_N = T_{12} \tag{5.10}$$

$$D_{NN} = \sqrt{T_{11}^2 + T_{22}^2} \tag{5.11}$$

$$D_{NNN} = T_{21} \tag{5.12}$$

$$D_W = T_{23} \tag{5.13}$$

$$D_{WW} = \sqrt{T_{13}^2 + T_{24}^2} \tag{5.14}$$

$$D_{WWW} = T_{14} \tag{5.15}$$

Finally, the fuzzy output variables are defuzzified to generate a dynamically changing hysteresis band according to the formula given in (5.16) [169].

$$HB = HB_{base} + \frac{15D_{WWW} + 10D_{WW} + 5D_W - 5D_N - 10D_{NN} - 15D_{NNN}}{D_{WWW} + D_{WW} + D_W + D_N + D_{NN} + D_{NNN}} \qquad (5.16)$$

5.1.3. Simulation Results

Adaptive fuzzy hysteresis band improvement together with proposed control system have been simulated on the PSCAD simulation environment. Similar to previous simulations, field measurements of steel melting facility are integrated to simulation model as IMF load.

In order to show the adaptively changing hysteresis bandwidth, a 7 milliseconds long current waveform is given in Figure 5.7. As can be seen from Figure 5.7, hysteresis band is large for the instants corresponding to high currents; however, it is narrow for the instants corresponding to low currents. This observation correctly represents the expected behavior of suggested adaptive fuzzy hysteresis band structure. Harmonic suppression performance, on the other hand, can be evaluated by looking at the MV current waveforms, which are given in Figure 5.8. Figure 5.8 shows that the suggested control algorithm successfully suppresses the harmonics and interharmonics of the IMF load under investigation. Indeed, the source current THD is shown to be reduced from 8.7% down to 3.2% when HAPF system starts operation.
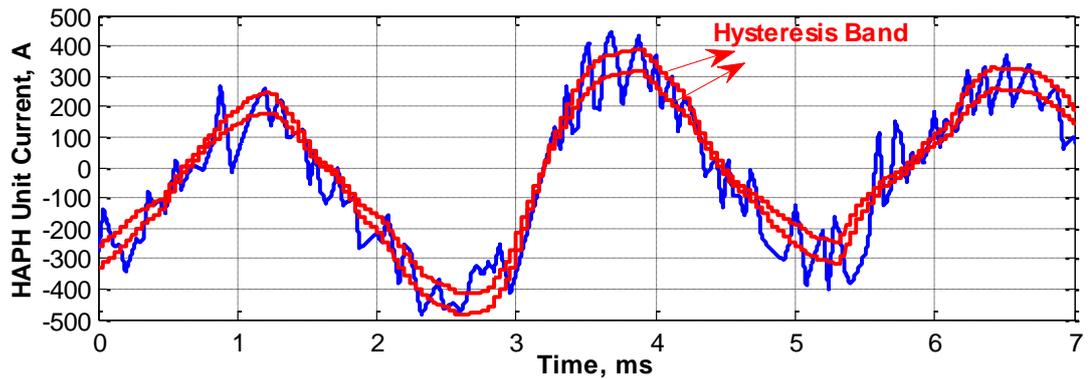
Figure 5.7 Sample current waveform of a HAPF unit together with corresponding hysteresis band (simulation results)
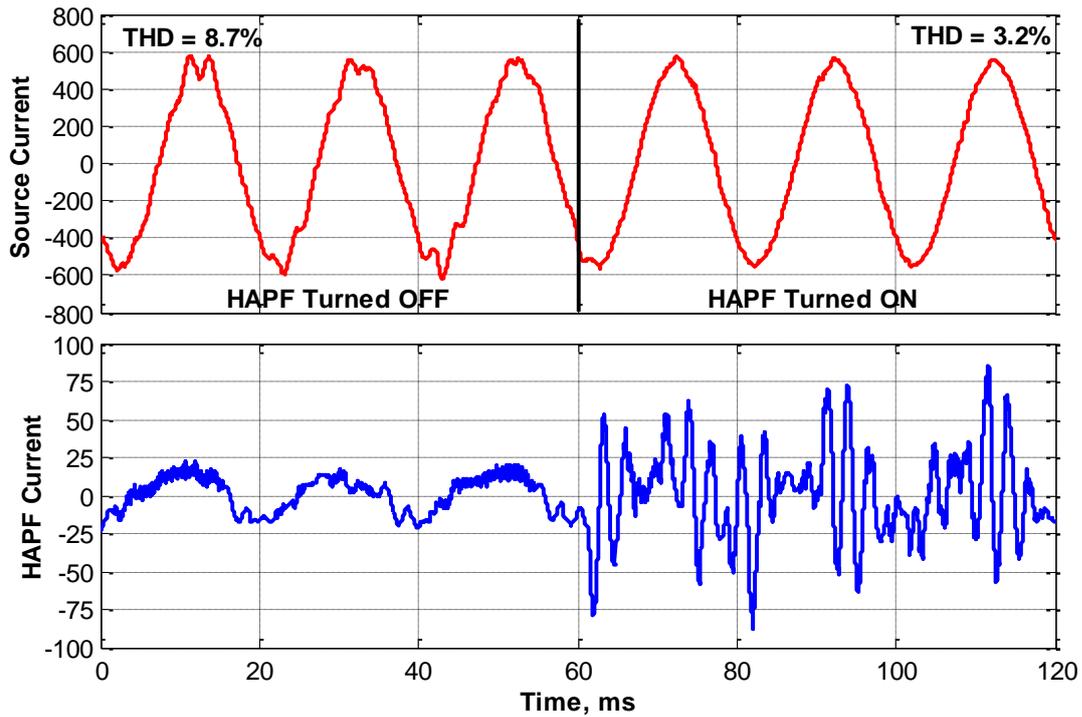
Figure 5.8 MV waveforms of the source and HAPF currents (simulation results)

Table 5.2 Simulation results of both fuzzy and fixed band hysteresis current control

	Average Switching Frequency	Average Switching Loss	Source Current THD (%)
Fuzzy Band	3737 Hz	2331 W	3.20
Fixed Band	3772 Hz	2571 W	3.17

It is essential to investigate the effect of suggested adaptive fuzzy hysteresis band improvement on switching loss, which is the main motivation of forming an adaptive band. In order to observe the contribution of the fuzzy band structure, separate simulations have been run for both fixed and fuzzy hysteresis band so that they can be easily compared under the same conditions. Average switching loss, average switching frequency and THD values are noted during 650 msec simulation run as comparative parameters and tabulated in Table 5.2. Simulation results have shown that the suggested fuzzy band improvement provides approximately 9% reduction in average switching losses although average switching frequency is kept in the similar values. The performance of the suggested fuzzy band structure is verified by

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comparing the THD values of both fixed and fuzzy hysteresis band values. THD results in Table 5.2 shows that the fuzzy hysteresis band does not cause a reduction in harmonic and interharmonic suppression performance.

5.1.4. Experimental Results

Proposed hysteresis band control together with integrated adaptive fuzzy band improvement has been implemented in the field as a software patch to the existing HAPF system installed in the steel melting facility under investigation. Similar to other experiments, results given in this section are also recorded while three IMF installations are simultaneously in operation.
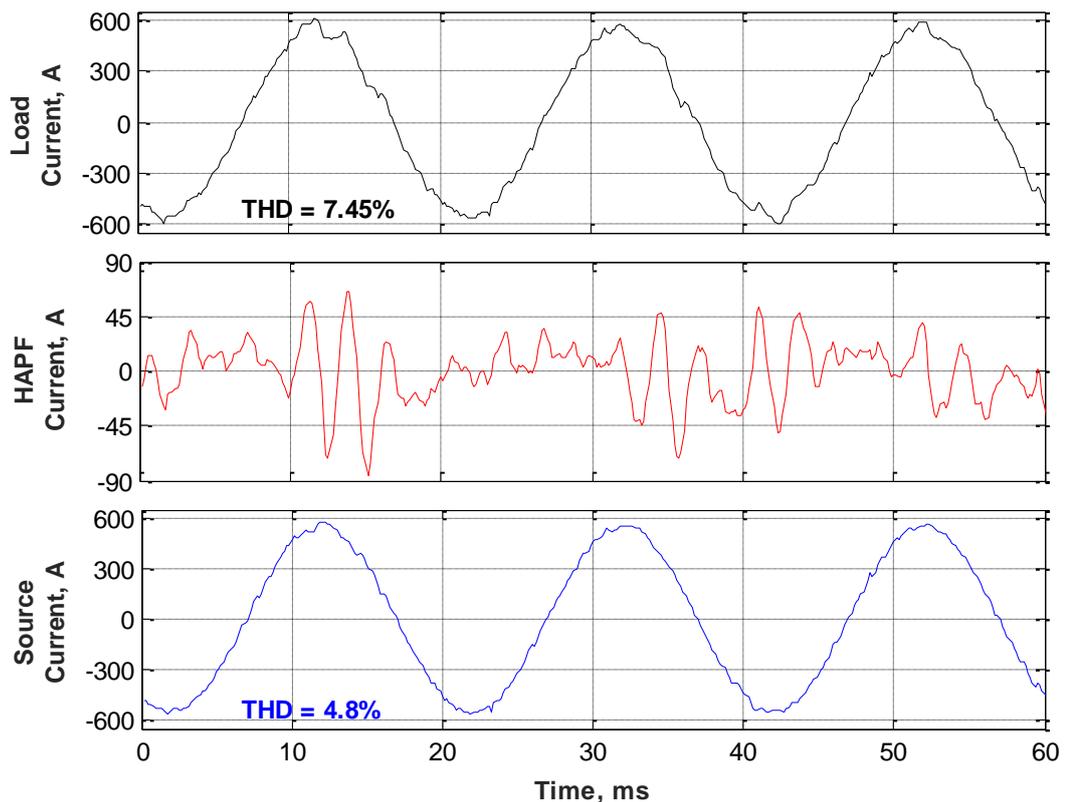
Figure 5.9 MV current waveforms for the proposed adaptive fuzzy hysteresis band current control method

In order to observe the harmonic and interharmonic suppression performance of the HAPF system, the recorded MV waveforms are drawn in a same graph given in Figure 5.9.

It can be seen in Figure 5.9 that the THD is decreased from 7.45% at the load side to 4.8% at the source side by the HAPF system. Harmonic suppression performance for each individual harmonic or interharmonic can be observed by looking at the harmonic spectra for load, source and HAPF currents, which is given in Figure 5.10. As can be understood from Figure 5.10 by using the mentioned methods in earlier chapters that there are three IMF loads simultaneously in operation with load resonant frequencies 172.5, 195 and 212.5 Hz causing corresponding interharmonic frequency pairs 295-395, 340-440, and 375-475 Hz, respectively.
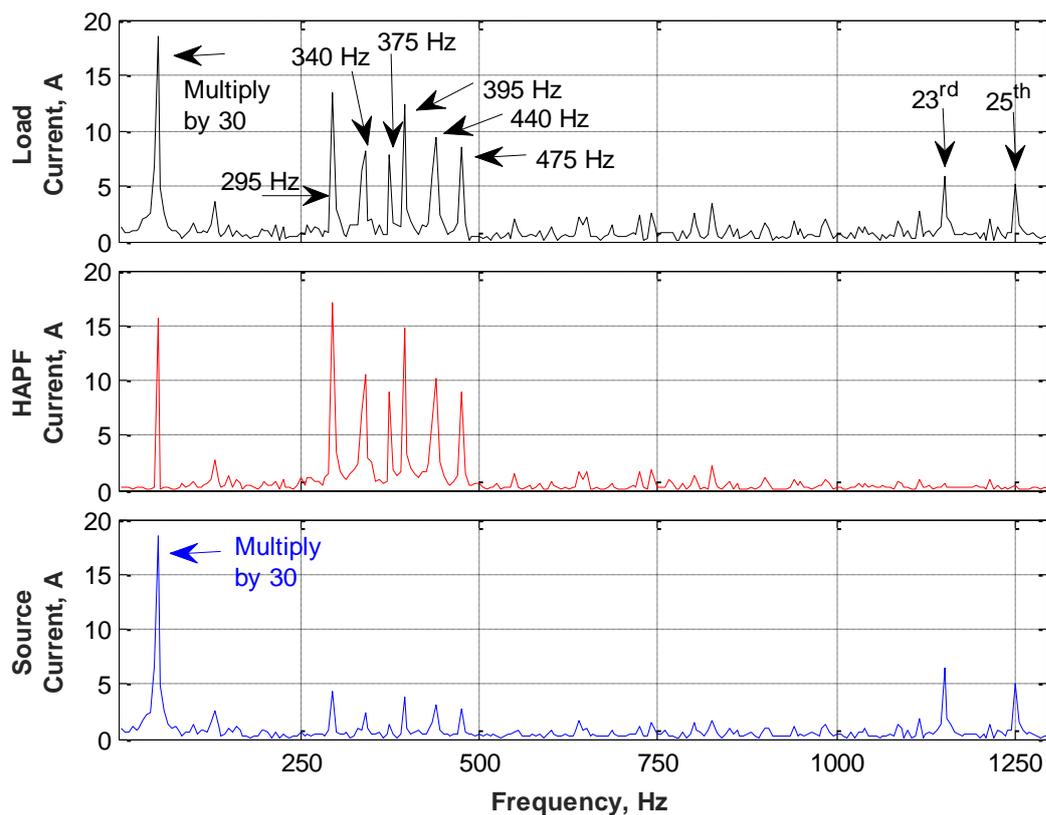
Figure 5.10 Frequency spectrum of the MV current waveforms for the proposed adaptive fuzzy hysteresis band current control method

Adaptively changing hysteresis band structure can be observed using the oscilloscope recordings of one of the nine identical HAPF units at LV side. Mentioned recordings is given in Figure 5.11. Red colored circles, in Figure 5.11, illustrates the hysteresis band widening and narrowing instants corresponding respectively to high and low current values. It can also be observed from this figure that hysteresis band may still be high for low currents too, which is due to the fact that integral of harmonic currents are also considered for the determination of hysteresis band.
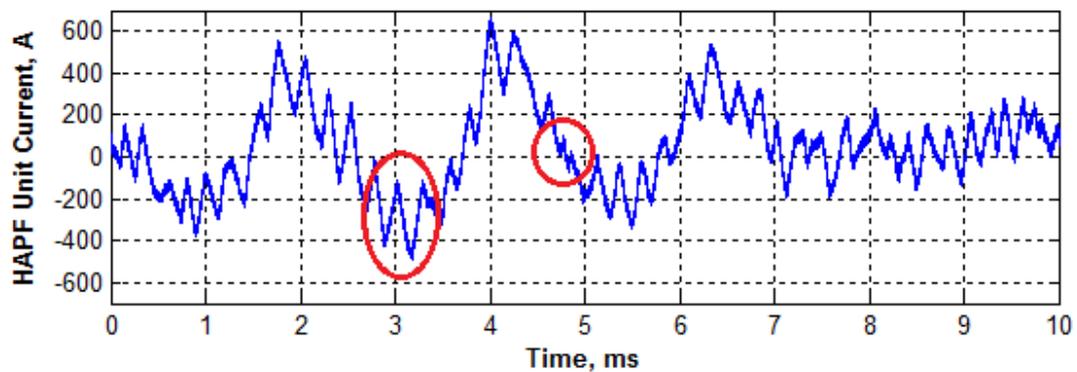
Figure 5.11 Field record of the current waveform for one of the HAPF units

It is shown in this section that the proposed hysteresis band control algorithm together with the integration of adaptive fuzzy band improvement has successfully implemented in the field to suppress interharmonics and harmonics of IMF loads. However, there is still a point that is not clear, whether the proposed improvement provides a decrease in overall losses or not.

5.1.5. Evaluation of Reduction in Overall Losses of Adaptive Fuzzy Hysteresis Band

Adaptive fuzzy hysteresis band control improvement is needed to be run for sufficiently long time period in order to show its superiority in terms of overall losses; since, the simultaneous experiments under the same working conditions are not

possible for fuzzy and fixed hysteresis band control methods. For this reason, the proposed fuzzy band improvement and the fixed band method had been run separately during five hours, which is sufficiently long period for an IMF load having complete melting cycle of 45 minutes, and the measurements are recorded. Since the operation time is sufficiently long, both working conditions can be assumed to be similar. Thus, the results surely give a good approximation for overall loss comparison.

Figure 5.12 and Figure 5.13 show the overall efficiency of the HAPF system respectively for fixed and fuzzy hysteresis band control techniques. As can be observed from those figures, adaptive fuzzy hysteresis band improvement provides a significant reduction, around 9.2%, in overall losses.
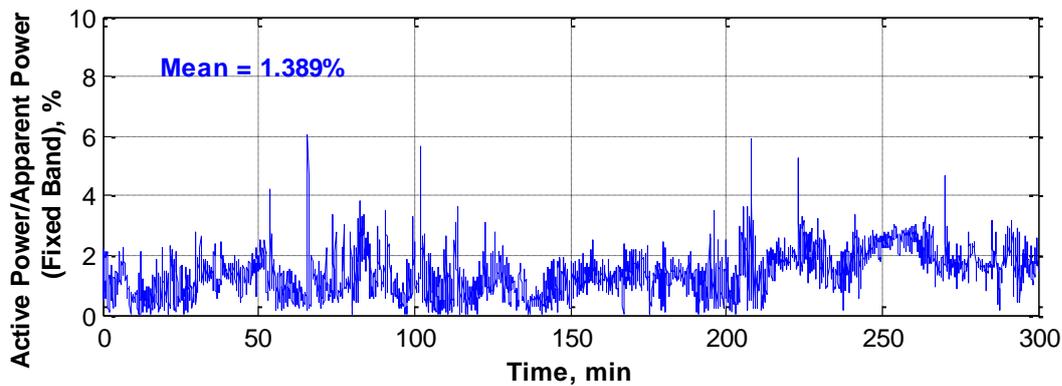
Figure 5.12 Efficiency curves of fixed band hysteresis current control for the entire measurement period

Although the results show that the adaptive fuzzy band philosophy provides and improvement on overall losses, the formulization is not enough for a complete relation between hysteresis band and fuzzified input parameters HAPF current and integral of its harmonic currents but it only gives an idea on proportionality relation, which is still valid for fuzzy control. The reason for this issue is because of that control hardware is not fast enough and reference tracking error is not negligible with respect to hysteresis bandwidth despite the fact that it is assumed to be so during formulation

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part. Reference tracking error, indeed, may reach up to the twice of the width of hysteresis band, the reasons of which is analyzed and details are given in the following section in detail.
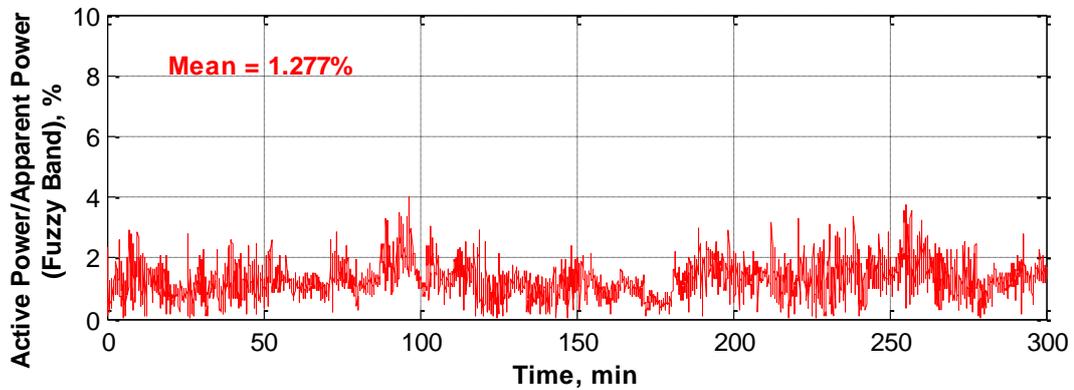
Figure 5.13 Efficiency curves of the adaptive fuzzy band hysteresis current control for the entire measurement period

The change in the mentioned assumption made during the formulation may make the formulization more complex but it still will not affect the proportionality relation between the input parameters and switching frequency. In fact, the errors in formulation is compensated by the MATLAB fuzzy logic toolbox due to the nature of fuzzy membership functions since they are determined using the exact field measurements and theoretically calculated corresponding switching loss terms.

5.2.   Effect of Sampling Frequency and Execution Time on Current Tracking Performance

Hysteresis band controlled waveform modulation technique and an improvement on it are mentioned for the control of proposed HAPF system investigated so far in this thesis. However, digital implementation of hysteresis band modulation strategy, known to be an analog method, is not yet introduced properly. In this section of the thesis, digital implementation of hysteresis band modulation strategy is formulized

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and effect of sampling frequency and execution time on current tracking performance is analyzed.

Digitizing of field measurements and computational delays have an important role on the control dynamics for digital implementation of hysteresis current control. For the sake of simplicity the term sampling period will be used as a constant time interval between two successive sampling instants and execution time as a maximum necessary time for the completion of all digital processes for reference generation.

Sampling period has been shown as an important parameter for digital systems in the literature so as for hysteresis band control [126], [179] – [189]. Choosing a high sampling frequency thus low sampling period has been suggested in various applications like grid connected inverter [179], PWM rectifier [180], motor drives [181] – [183], and shunt APF [184]. It is suggested in [184] that the quality of APF current waveform can be enhanced by increasing the sampling frequency. Also, [126] and [185] has used dynamically changing sampling periods by predicting the reference signal in order to overcome the tracking errors caused by periodic sampling instants. In addition to sampling periods, execution time has also been mentioned as an important parameter for hysteresis band control technique [186] – [189]. The use of powerful controllers has been suggested by [186] in order to reduce the effect of execution delay on hysteresis band controlled APF. The increase in torque ripples has been related to execution time in [187] and [188]. Ref. [188] has suggested that the time consuming processes should not be implemented during a sampling period. Finally it has been pointed out in [189] that reducing solely the sampling period is not enough for the reduction of unintended effects without any decrease in execution time too.

In this section of the thesis, the effects of both sampling frequency and execution time on the reference tracking performance of hysteresis band controlled HAPF converter are investigated and the findings are verified with simulation results. Using the verifications on simulation environment, reference tracking performance of field implemented HAPF system under investigation by this thesis is compared with the

simulation model of it and its control system. Finally, some solutions to reference tracking error problem of the implemented HAPF system are proposed.

5.2.1. Modelling of Reference Tracking Error

Analysis derived for the mathematical representation of the converter in Figure 2.6 and its single phase equivalent circuit in Figure 5.1 has already been reached in this chapter as (5.4). Using (5.4), one can model the worst case reference tracking error with the help of an illustration, given in Figure 5.14, showing the digital implementation of hysteresis band control. In Figure 5.14, T_e is execution time, T_s sampling period, $i_{fx}(s)$ the actual current of phase x sampled at sampling instant t_s, $i_{fx}^*(s)$ the reference current of phase x calculated by the samples collected at t_s, and ΔI the hysteresis band. Green shaded area in Figure 5.14 represents the interval where the actual current lays out of hysteresis band. In order to obtain worst case reference tracking error, it is assumed that the actual current passes the band immediately after t_s sampling instant. By this way, the controller would be able to understand that the current is out of band after reference current signals corresponding to next sampling instant is calculated. An assumption is required for the linear representation of hysteresis switching behavior.
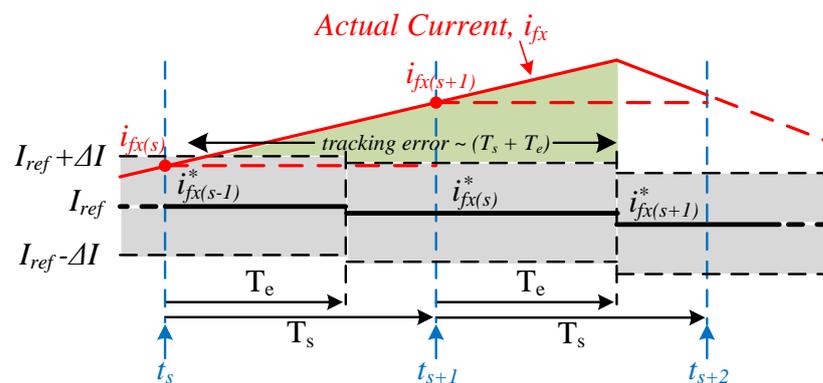
Figure 5.14 Illustration of worst case switching condition for hysteresis band control

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Assumption – Linear LC Filter Response: Execution time T_e, sampling period T_s, (T_s + T_e), and hysteresis band ΔI are small enough so that LC filter step response can be consider in linear region [89].

Using the assumption, Figure 5.14, and (5.4), (5.11) can be reached. By rearranging (5.11), one can obtain (5.12) in order to represent worst case error.

$$\frac{\Delta i_L}{T_s + T_e} = -\frac{v_{inv}(t)}{L_f} - \frac{1}{L_f C_f}\int i_L(t)dt \tag{5.11}$$

$$error = \frac{T_s + T_e}{L_f}\left[-v_{inv}(t) - \frac{1}{C_f}\int i_L(t)dt\right] \tag{5.12}$$

When (5.12) is observed, it can be understood that the reference tracking error depends on the coupling filter inductor L_f, sampling period T_s, execution time T_e, and the inverter terminal voltage v_{inv}. Inverter terminal voltage has been derived in Chapter 2 and it is strongly depends on the dc link voltage V_{dc} and the switching positions of other phases. All the possible inverter voltage values can observed by looking at Table 2.4. Following measures can be taken by the evaluation of (5.12) in order to reduce reference current tracking error:

i) Increasing sampling frequency hence reducing sampling period T_s at the expense of higher switching losses.

ii) Reducing execution time T_e by using more powerful controller or using parallel processing [186]. By this way sampling period can also be decreased [189].

iii) Keeping the dc link voltage as low as possible. However, it should be high enough to generate harmonic references [129].

iv) Increasing filter inductance L_f. Actually it may eventually cause an increase in dc link voltage in order to be able to provide necessary voltage for the harmonic references [129].

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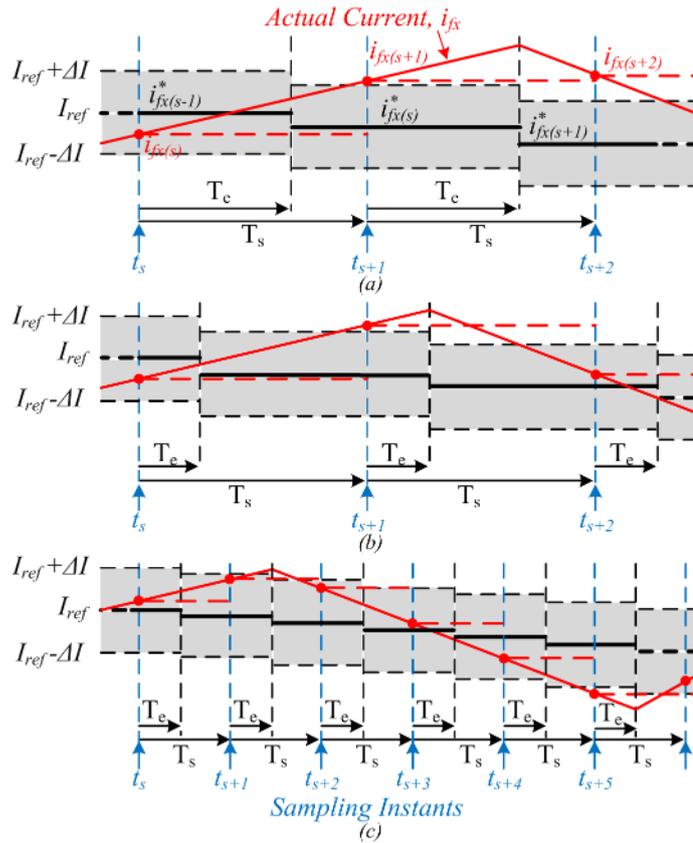
Figure 5.15 Illustration showing the digital implementation of hysteresis band control for a) the field implemented control system, b) reduced execution time, and c) reduced both execution time and sampling period

The value of coupling inductor L_f is inversely proportional to reference current tracking error. Thus, increasing inductance dramatically improves the reference tracking performance. However, similar to majority of converter types, coupling inductor value is an important design parameter for VSC based HAPF converter, and choosing of filter inductance is mentioned in detail at Chapter 3. For this reason, it is not possible to change filter inductance for this particular research. DC link voltage, also, an important design parameter and it is already designed to be the minimum possible value at Chapter 3. Hence, it is not possible to further reduce DC link voltage too.

Eventually, sampling period and execution time are the remaining parameters for reducing the reference tracking performance of proposed hysteresis band controlled

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HAPF converter. Since the reference current tracking error is proportional to the sum of those two parameters, reducing both sampling period and execution time provide an advantage for the improvement of tracking performance. Three scenarios has been run for illustrating the effects of both sampling period and execution time on the EMTDC/PSCAD simulation environment, and the results are given in the following section.
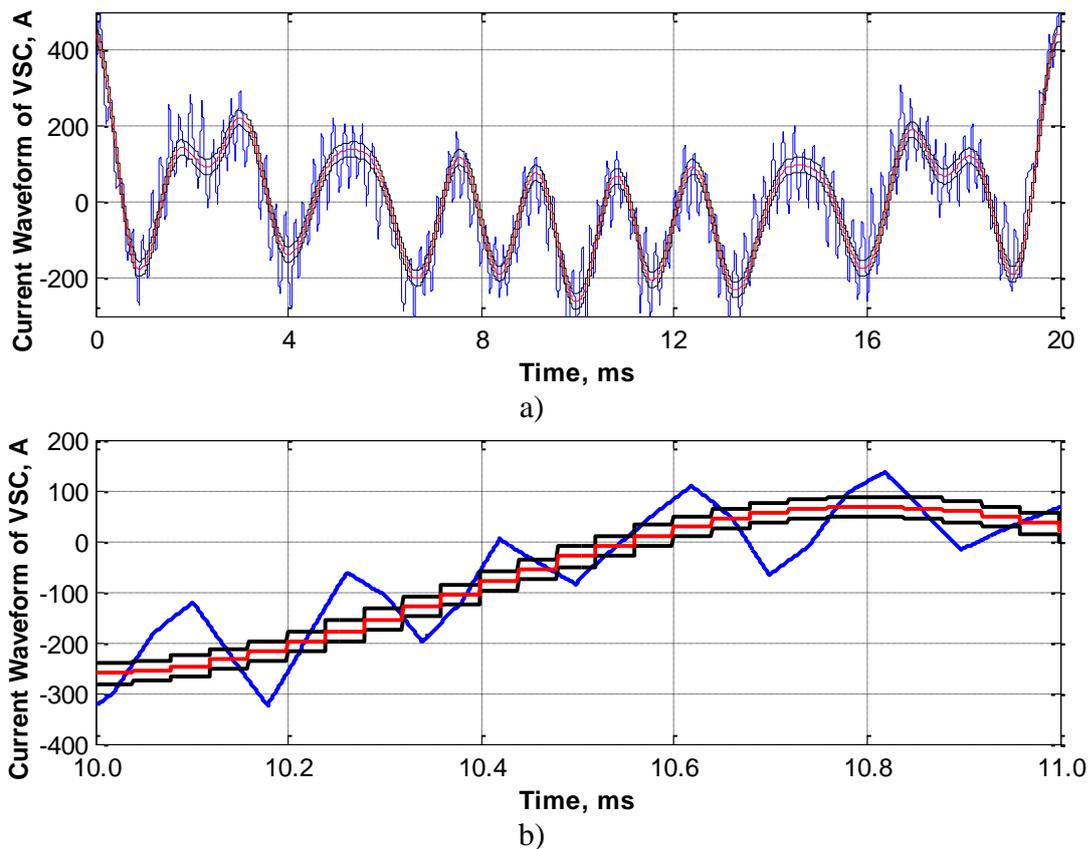
Figure 5.16 Simulation results of scenario-1 a) sample 20-ms waveform and b) 1-ms part of the sample waveform for observing switching instants

5.2.2. Simulations of Different Digital Implementation Scenarios

Field implemented HAPF converter and the digital implementation of proposed hysteresis band control algorithm are modeled using real field measurements on

EMTDC/PSCAD simulation environment in order to observe the effects of sampling period and execution time on reference tracking error. Before mentioning simulation results, an illustration, given in Figure 5.15, showing the possible simulation scenarios should be investigated to provide an idea about the aim of conducted work. In Figure 5.15.a, the sample illustration for the field implemented control system is given. On the other hand, sample illustrations for reduced execution time and reduced execution time together with sampling period cases are given in Figure 5.15.b and c, respectively. All those three illustrations show that the improvement of reduced sampling frequency and execution time at the expense of higher switching frequency can be clearly observed. The simulation models of all three cases are given in this part of the thesis.

Scenario – 1 (f_s = 25 kHz, T_s = 40 µs, and T_e = 20 µs): This scenario can be considered as the implementation of the digital control algorithm implemented in the field. The sampling frequency implemented in the field is 25 kHz and the average execution time of the implemented control system has been measured as 20 µs. When the simulation is run under these conditions, a current waveform given in Figure 5.16.a is reached. For providing a better observation of the digital implementation, zoomed version of the resultant waveform is also shown in Figure 5.16.b. In addition to current waveforms, an error graph, in Figure 5.17, is also drawn for a better observation of reference current tracking performance. As can be seen in Figure 5.17, reference current tracking error reaches up to four times larger than the width of hysteresis band.
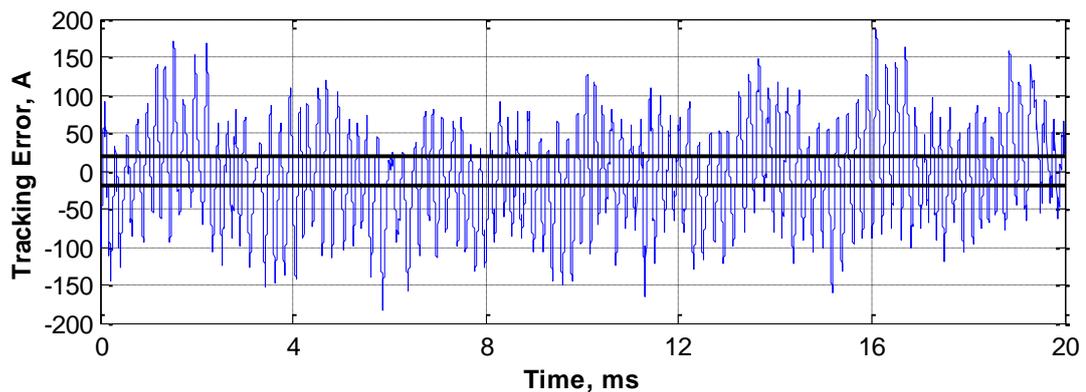
Figure 5.17 Reference tracking error of hysteresis current control for simulation scenario-1
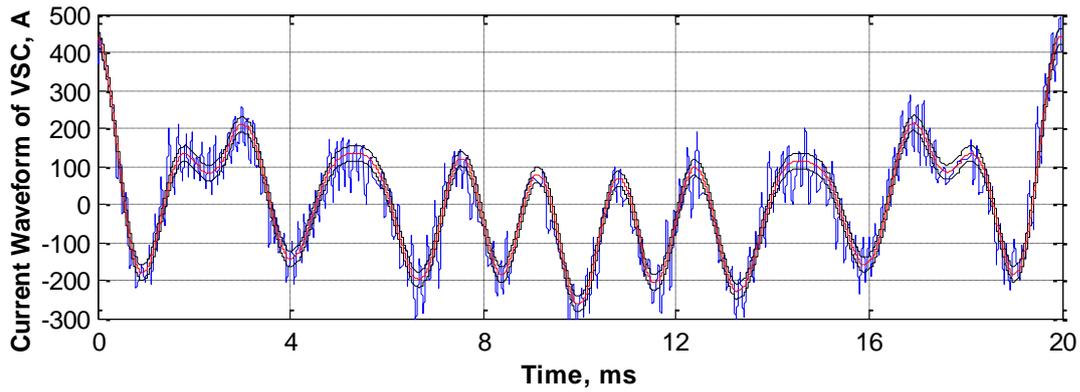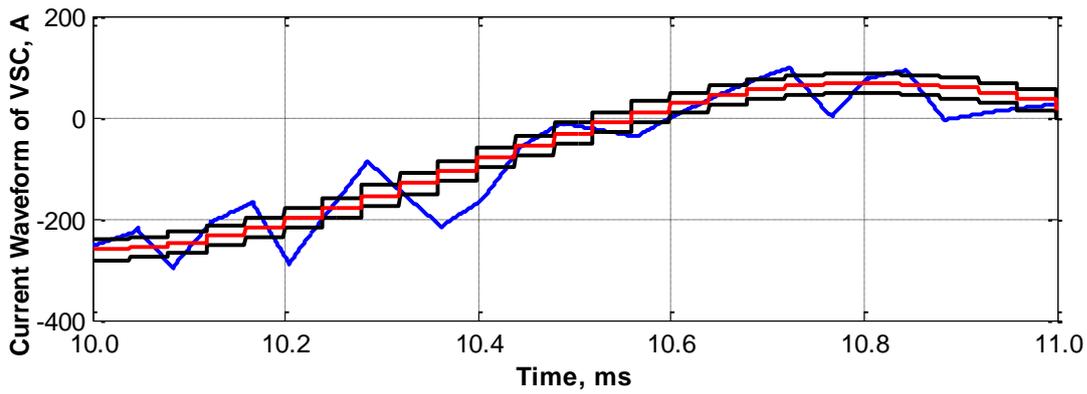
Figure 5.18 Simulation results of scenario-2 a) sample 20-ms waveform and b) 1-ms part of the sample waveform for observing switching instants
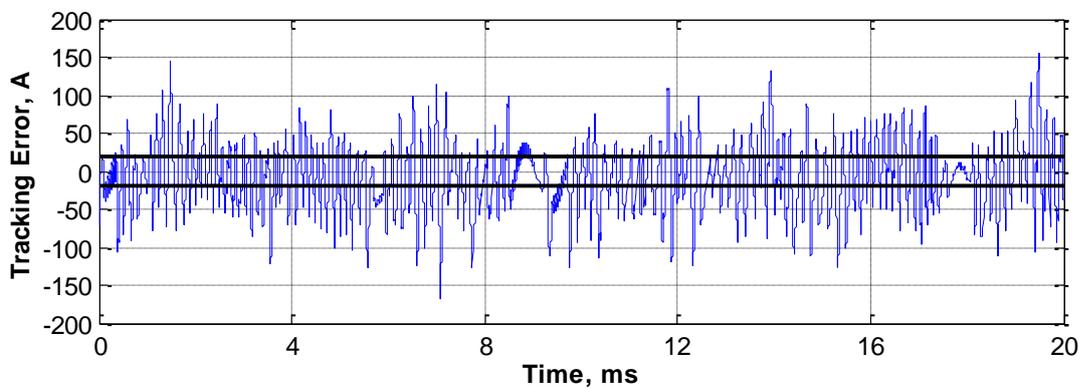
Figure 5.19 Reference tracking error of hysteresis current control for simulation scenario-2

Scenario – 2 (f_s = 25 kHz, T_s = 40 µs, and T_e = 5 µs): In order to observe the effect of reduced execution time on the reference tracking performance of hysteresis band

control method, execution time value is reduced to 5µs for this simulation scenario which is corresponding to Figure 5.15.b. Current waveform of scenario -2 for the same time interval as the first scenario is given in Figure 5.18.a. Moreover, a zoomed version of this waveform, given in Figure 5.18.b, is also provided so that the digital implementation of the hysteresis band control can be traced. Reference current tracking performance can be compared to other scenarios by looking at the error curve shown in Figure 5.19. As can be recognized from Figure 5.19 that the reduction in execution time reduces the errors thus increases the reference tracking performance.
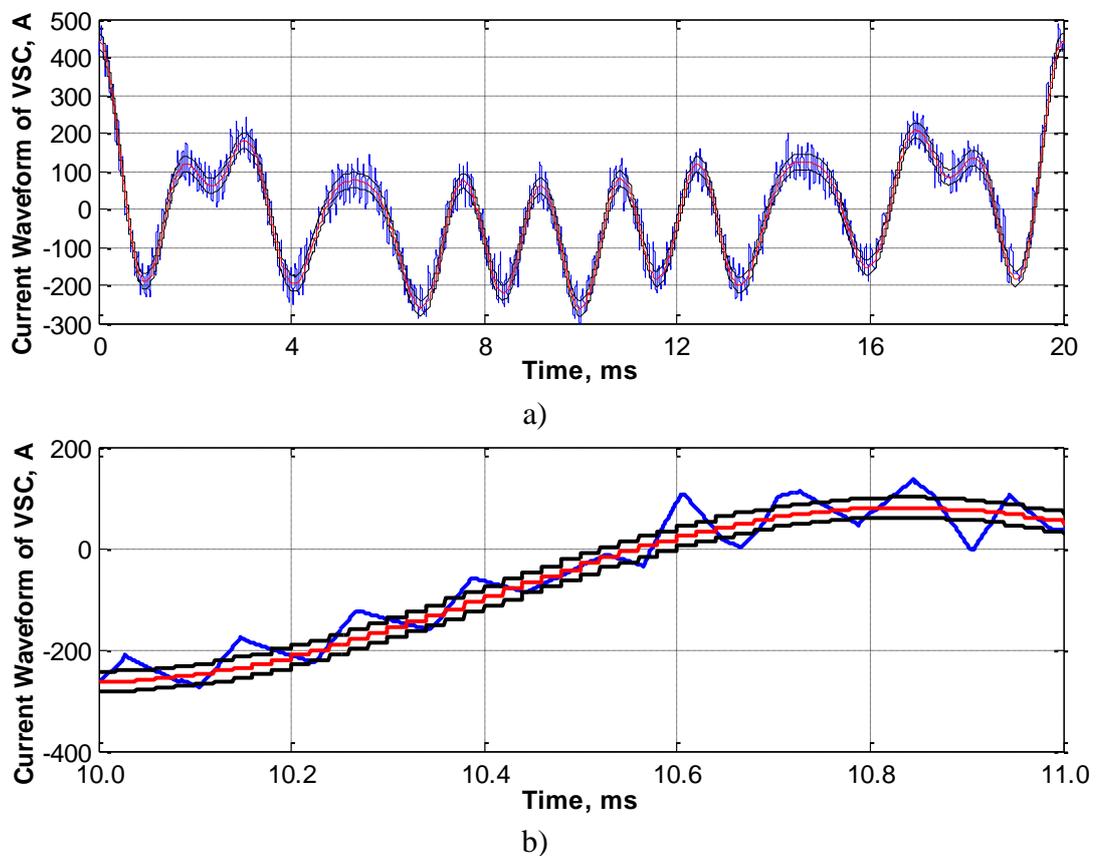
Figure 5.20 Simulation results of scenario-3 a) sample 20-ms waveform and b) 1-ms part of the sample waveform for observing switching instants

Scenario – 3 ($f_s = 50\ kHz$, $T_s = 20\ µs$, and $T_e = 5\ µs$): Finally in this scenario, sampling period is also halved together with the previous reduction in execution time, which

corresponds to the illustration in Figure 5.15.c. Please note that the reduction in sampling period can only be possible with the reduced execution time, which is due to the fact that all the necessary calculations for a control system should be completed between two successive sampling instants. When this scenario is modelled and run in simulation environment, current waveform in Figure 5.20.a is reached. Similar to other scenarios, a zoomed version of this waveform is also drawn as given in Figure 5.20.b in order to better understand the behavior of digital implementation. Furthermore, reference current tracking performance can be analyzed by using the error graph given in Figure 5.21. Satisfying the expectations, reference current tracking error is significantly reduced and reduced down to acceptable values as shown in Figure 5.21. Although this scenario provides and improvement in reference tracking performance, it also cause an increase in switching frequency thus higher losses.
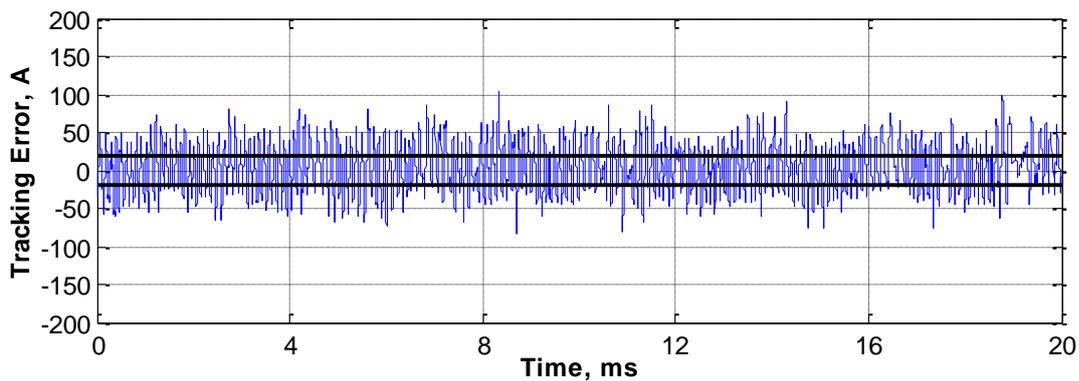
Figure 5.21 Reference tracking error of hysteresis current control for simulation scenario-3

5.2.3. Evaluation of Field Implemented HAPF System and Suggestions

First scenario in the simulation results is already defined in previous sections as the case of the HAPF system implemented in the field. In this section, real field measurement are compared with the results obtained from the simulation scenario-1

in order to show their similarities. Figure 5.22.a shows 20 msec long oscilloscope reading, collected in the field, and it represents current waveform of one of the HAPF units. As a first opinion, it can be seen in Figure 5.22.a that the field current often seem to exceed the hysteresis band. Similar to evaluation of simulation results, reference tracking error for the field recordings are also deduced and drawn in a graph as given in Figure 5.22.b. As can be seen in Figure 5.22.b, current waveform of the implemented HAPF converter exceeds the hysteresis band by significant amounts as expected. This situation may cause some harmonics around switching frequency to reach high magnitudes. The frequency spectrum given in Figure 5.23 verifies this hypothesis.
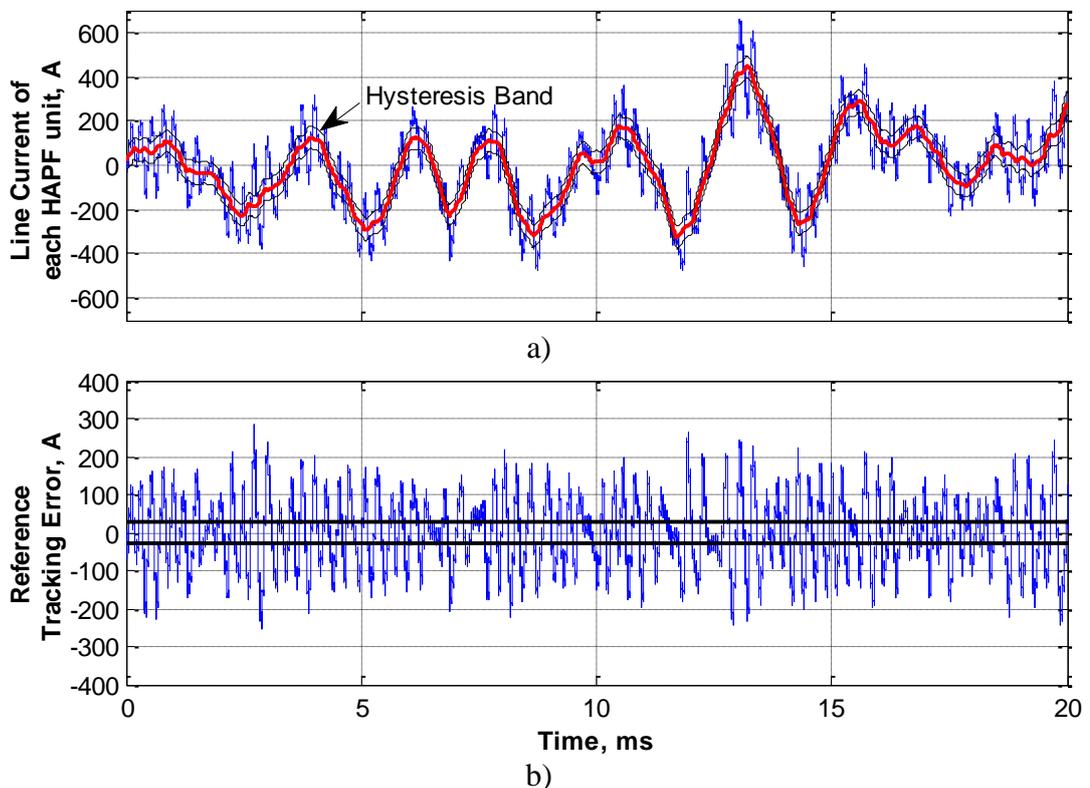
Figure 5.22 a) Line current waveform of an HAPF unit, tracked reference, implemented hysteresis bands, and b) corresponding reference tracking error (field measurements)
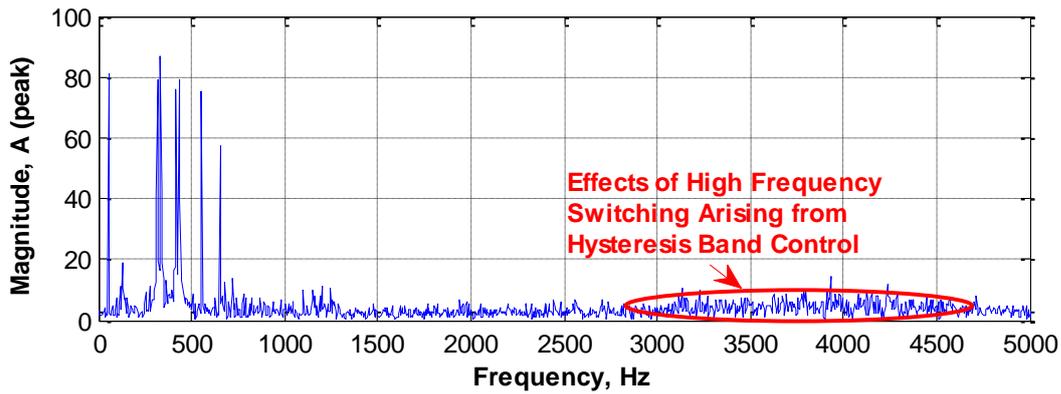
Figure 5.23 Harmonic spectrum of the HAPF unit current collected in the field

In this part of the thesis, reference current tracking errors, observed in the field, is analyzed and the causes of this problem are verified to be the insufficient sampling frequency and excessive execution time. It is put forward that increase in sampling frequency and reduction in execution time together enhance the performance of the digitally implemented hysteresis band modulation technique. Then, this hypothesis is verified in simulation environment. As a result of the analysis given in this chapter, the following counter measures should be taken in order to increase the reference tracking performance of the HAPF system implemented in the field [190].

i) Optimization in the control algorithm, unnecessary computational burden should be eliminated or moved to an auxiliary processor.

ii) Processors allowing a parallel processing like FPGA or Complex Programmable Logic Device (CPLD) can be used to decrease execution time.

iii) Sampling frequency should be increased at the expense of higher switching frequency and higher losses. However, this can only be possible after the improvements on execution time which is due to the fact that all the necessary calculations should be completed before next samples are collected. Moreover, higher switching losses can be eliminated by integration of adaptive fuzzy hysteresis bands as given in this chapter. Use of fuzzy bands will be much more effective with improved current tracking performance.

CHAPTER 6

CONCLUSIONS

In this research work, the design and implementation of a three phase three wire two level shunt connected HAPF is carried out. The overall system is designed and developed to suppress the time varying harmonics and interharmonics of the IMF load.

The developed system is connected to MV bus of the steel melting facility of ER CELIK Metallurgy Hatay/Turkey via a specially designed coupling transformer. In the LV side, on the other hand, there are nine identical HAPF converters. In the scope of the thesis, the HAPF converters controller is implemented by three different control methods namely proportional control, hysteresis band current control and adaptive fuzzy logic control. Their harmonic and interharmonic suppression performances are investigated and the results are given accordingly in the related chapters. The comparison of the filtering performances are made and a novel performance evaluation criterion, Suppression Factor, is proposed. All the necessary design steps are given in detail in the related sections.

The results of this research proves that all the harmonics and interharmonics of the IMF load under investigation are successfully suppressed by all the three different control method.

The following conclusion can be drawn from the results of theoretical and experimental work of this research:

i) IMF load is one of the most problematic loads in terms of its harmonic and interharmonic current content. Thus, an extensive study should be made to suggest penalty limits for the interharmonics of industrial loads as well as harmonics.

ii) HAPF converter topology is the most effective system for the suppression of harmonics and interharmonics spread over a wide range, 250 – 550 Hz for this particular application. This is because of the low impedance characteristics of the coupling element over the entire frequency range and possibility of using low dc link voltage.

iii) Traditional voltage mode control methods, proportional control, are not effective for the loads having harmonic frequencies in a wide range. Current controls, HBC, are better for reference tracking and thus harmonic suppression of this kind of loads.

iv) Advanced techniques, FLC or neural networks, can be used to decrease the switching losses of the hysteresis band current controlled HAPF converters at the expense of slightly decreased suppression performance.

v) Hierarchical control system architectures should be implemented for the control of high power module power electronics converters composed of PEBBs.

vi) Existing performance evaluation criteria are not enough to describe the performance of the filtering equipment operating in a wide frequency range. The novel criterion, Suppression Factor, can be used to analyze the effectiveness of these equipment.

vii) In order to decrease the reference tracking errors of the hysteresis band controlled converters, the sampling frequency should be increased with the reduced execution time. In order to reach this aim, unnecessary computational burden can be eliminated and faster controllers or controllers allowing parallel processing should be used.

Although necessary improvements have been investigated and implemented to the proposed HAPF converter topology, there is still a need to clarify some points that are not clear and to further contribute to the power quality of IMF loads. The suggested future works to the research work described in this thesis is given below:

i) Due to hysteresis current modulation technique there are high frequency components in the HAPF line current waveform. Although the RMS and peak values of this current are less than the waveform in proportional control case, they cause the filter reactor to overheat. This is due to the high frequency current ripples of HBC which does not appear in voltage mode control methods. For this reason, the iron core losses of the reactor subjected to hysteresis switching should be analyzed and the reactor design should be updated to reduce operating temperature of the reactor.

ii) Since HAPF system proposed in the scope of this thesis does not manage to suppress 23rd and 25th characteristic harmonics, a passive filter solution should be suggested and implemented for the suppression of these harmonics.

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APPENDIX A

MATHEMATICAL MODELLING OF CONVERTER VOLTAGES FOR HYSTERESIS BAND CONTROL SWITCHING SCHEMES

Each switching scheme has unique voltage values for the terminals ($v_{fa\text{-}n}$, $v_{fb\text{-}n}$, $v_{fc\text{-}n}$) of the HAPF converter. Voltage derivations for each possible switching scheme except "001" which is already given in earlier parts of the thesis, are derived in this part of the thesis.

A.1. Switching Schemes "000" and "111"

Switching schemes "000" and "111" shows similar behavior and their equivalent circuit representation is illustrated in Figure A.1. By inspection, all the terminal voltages are found out to be 0, that is $v_{fa\text{-}n}=0$, $v_{fb\text{-}n}=0$, $v_{fc\text{-}n}=0$.
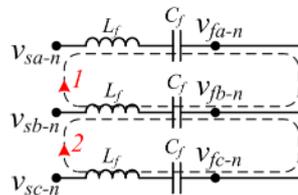
Figure A.1 Equivalent circuit representation of the switching schemes "000" and "111"

A.2. Switching Scheme "010"

Equivalent circuit representation of the switching scheme "010" is as illustrated in Figure A.2.
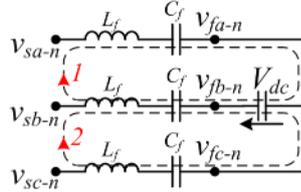
Figure A.2 Equivalent circuit representation of the switching scheme "010"

In order to formulate the behavior of the switching scheme "010", the equivalent circuit given in Figure A.2 is solved using the KVL equations of loop-1 and -2 as (C.1) and (C.2) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} - v_{dc} \qquad (C.1)$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} - v_{dc} \qquad (C.2)$$

where, v_{Coa}, v_{Cob} and v_{Coc} are the initial voltage values across the series filter capacitor C_f for each phase, and n represents the virtual neutral point which can be considered as the neutral point of the coupling transformer secondary.

Balanced system constraints for three-phase three-wire converter can be written as (C.3) and (C.4).

$$i_{fa} + i_{fb} + i_{fc} = 0 \qquad (C.3)$$

$$v_{sa-n} + v_{sb-n} + v_{sc-n} = 0 \qquad (C.4)$$

HAPF converter voltages $v_{fa\text{-}n}$, $v_{fb\text{-}n}$ and $v_{fc\text{-}n}$ can be expressed via coupling transformer secondary voltages $v_{sa\text{-}n}$, $v_{sb\text{-}n}$ and $v_{sc\text{-}n}$ as given respectively in (C.5) – (C.7).

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} = v_{fa-n} \tag{C.5}$$

$$v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} = v_{fb-n} \tag{C.6}$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} = v_{fc-n} \tag{C.7}$$

Equation (C.8) can be obtained by making use of (C.1) – (C.4).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3\int i_{fb}dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} + 2v_{dc} = 0 \tag{C.8}$$

Substitution of (C.6) into (C.8) gives (C.9). Then (C.10) is obtained by rearranging (C.9).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} + 2v_{dc} = 0 \tag{C.9}$$

$$v_{fb-n} = \frac{2v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \tag{C.10}$$

In order to find a relation for the sum of cumulative initial voltages across the capacitors of each phase, (C.11) is derived by summing up (C.5), (C.6), (C.7) and using (C.4).

$$v_{Coa} + v_{Cob} + v_{Coc} = -(v_{fa-n} + v_{fb-n} + v_{fc-n}) = 0 \tag{C.11}$$

Sum of converter terminal voltages are found out to be zero in Chapter 2. ($v_{fa\text{-}n}$ + $v_{fb\text{-}n}$ + $v_{fc\text{-}n}$ = 0). Thus, (C.10) can be rewritten as (C.12) by using (C.11).

$$v_{fb-n} = \frac{2v_{dc}}{3} \tag{C.12}$$

Since $v_{fa-n} = v_{fc-n}$ and $v_{fc-n} = v_{fb-n} - v_{dc}$ by inspection on equivalent circuit in Figure A.2, (C.13) and (C.14) can be directly obtained from (C.12).

$$v_{fa-n} = -\frac{v_{dc}}{3} \tag{C.13}$$

$$v_{fc-n} = -\frac{v_{dc}}{3} \tag{C.14}$$

A.3. Switching Scheme "011"

Equivalent circuit representation of the switching scheme "011" is as illustrated in Figure A.3.
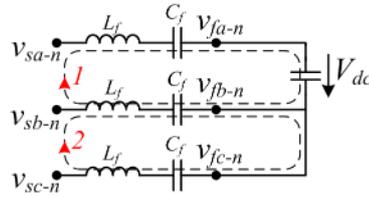
Figure A.3 Equivalent circuit representation of the switching scheme "011"

In order to formulate the behavior of the switching scheme "011", the equivalent circuit given in Figure A.3 is solved using the KVL equations of loop-1 and -2 as (C.15) and (C.16) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} + v_{dc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \tag{C.15}$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \tag{C.16}$$

Equation (C.17) can be obtained by making use of (C.15), (C.16), (C.3) and (C.4).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3\int i_{fb}dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} + v_{dc} = 0 \qquad \text{(C.17)}$$

Substitution of (C.6) into (C.17) gives (C.18). Then (C.19) is obtained by rearranging (C.18).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} + v_{dc} = 0 \qquad \text{(C.18)}$$

$$v_{fb-n} = \frac{v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \qquad \text{(C.19)}$$

Using the deduction in (C.11) on (C.19) yields (C.20).

$$v_{fb-n} = \frac{v_{dc}}{3} \qquad \text{(C.20)}$$

Since $v_{fb\text{-}n} = v_{fc\text{-}n}$ and $v_{fb\text{-}n} = v_{fa\text{-}n} + v_{dc}$ by inspection on equivalent circuit in Figure A.3, (C.21) and (C.22) can be directly obtained from (C.20).

$$v_{fa-n} = -\frac{2v_{dc}}{3} \qquad \text{(C.21)}$$

$$v_{fc-n} = \frac{v_{dc}}{3} \qquad \text{(C.22)}$$

A.4. Switching Scheme "100"

Equivalent circuit representation of the switching scheme "100" is as illustrated in Figure A.4.
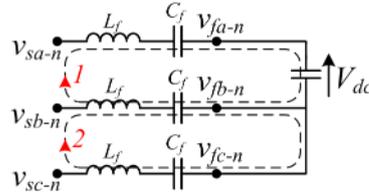
Figure A.4 Equivalent circuit representation of the switching scheme "100"

In order to formulate the behavior of the switching scheme "100", the equivalent circuit given in Figure A.4 is solved using the KVL equations of loop-1 and -2 as (C.23) and (C.24) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa} dt}{C_f} - v_{Coa} - v_{dc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb} dt}{C_f} - v_{Cob} \qquad (C.23)$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc} dt}{C_f} - v_{Coc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb} dt}{C_f} - v_{Cob} \qquad (C.24)$$

Equation (C.25) can be obtained by making use of (C.23), (C.24), (C.3) and (C.4).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3\int i_{fb} dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} - v_{dc} = 0 \qquad (C.25)$$

Substitution of (C.6) into (C.25) gives (C.26). Then (C.27) is obtained by rearranging (C.26).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} - v_{dc} = 0 \qquad (C.26)$$

$$v_{fb-n} = -\frac{v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \qquad (C.27)$$

Using the deduction in (C.11) on (C.27) yields (C.28).

$$v_{fb-n} = -\frac{v_{dc}}{3} \qquad (C.28)$$

Since $v_{fb-n} = v_{fc-n}$ and $v_{fb-n} = v_{fa-n} - v_{dc}$ by inspection on equivalent circuit in Figure A.4, (C.29) and (C.30) can be directly obtained from (C.28).

$$v_{fa-n} = \frac{2v_{dc}}{3} \qquad (C.29)$$

$$v_{fc-n} = -\frac{v_{dc}}{3} \qquad (C.30)$$

A.5. Switching Scheme "101"

Equivalent circuit representation of the switching scheme "101" is as illustrated in Figure A.5.
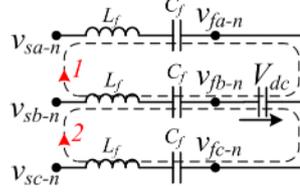
Figure A.5 Equivalent circuit representation of the switching scheme "101"

In order to formulate the behavior of the switching scheme "101", the equivalent circuit given in Figure A.5 is solved using the KVL equations of loop-1 and -2 as (C.31) and (C.32) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa} dt}{C_f} - v_{Coa} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb} dt}{C_f} - v_{Cob} + v_{dc} \quad \text{(C.31)}$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc} dt}{C_f} - v_{Coc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb} dt}{C_f} - v_{Cob} + v_{dc} \quad \text{(C.32)}$$

Equation (C.33) can be obtained by making use of (C.31), (C.32), (C.3) and (C.4).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3 \int i_{fb} dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} - 2v_{dc} = 0 \quad \text{(C.33)}$$

Substitution of (C.6) into (C.33) gives (C.34). Then (C.35) is obtained by rearranging (C.34).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} - 2v_{dc} = 0 \quad \text{(C.34)}$$

$$v_{fb-n} = -\frac{2v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \quad \text{(C.35)}$$

Using the deduction in (C.11) on (C.35) yields (C.36).

$$v_{fb-n} = -\frac{2v_{dc}}{3} \tag{C.36}$$

Since $v_{fa-n} = v_{fc-n}$ and $v_{fb-n} = v_{fa-n} - v_{dc}$ by inspection on equivalent circuit in Figure A.5, (C.37) and (C.38) can be directly obtained from (C.36).

$$v_{fa-n} = \frac{v_{dc}}{3} \tag{C.37}$$

$$v_{fc-n} = \frac{v_{dc}}{3} \tag{C.38}$$

A.6. Switching Scheme "110"

Equivalent circuit representation of the switching scheme "110" is as illustrated in Figure A.6.
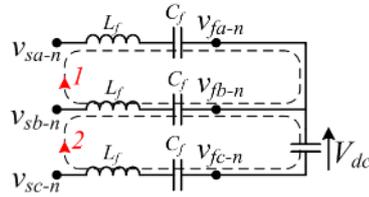
Figure A.6 Equivalent circuit representation of the switching scheme "110"

In order to formulate the behavior of the switching scheme "110", the equivalent circuit given in Figure A.6 is solved using the KVL equations of loop-1 and -2 as (C.39) and (C.40) respectively.

$$v_{sa-n} - L_f \frac{di_{fa}}{dt} - \frac{\int i_{fa}dt}{C_f} - v_{Coa} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \tag{C.39}$$

$$v_{sc-n} - L_f \frac{di_{fc}}{dt} - \frac{\int i_{fc}dt}{C_f} - v_{Coc} + v_{dc} = v_{sb-n} - L_f \frac{di_{fb}}{dt} - \frac{\int i_{fb}dt}{C_f} - v_{Cob} \tag{C.40}$$

Equation (C.41) can be obtained by making use of (C.39), (C.40), (C.3) and (C.4).

$$-3v_{sb-n} + 3L_f \frac{di_{fb}}{dt} + \frac{3\int i_{fb}dt}{C_f} + 2v_{Cob} - v_{Coa} - v_{Coc} + v_{dc} = 0 \tag{C.41}$$

Substitution of (C.6) into (C.41) gives (C.42). Then (C.43) is obtained by rearranging (C.42).

$$-3v_{fb-n} - v_{Coa} - v_{Cob} - v_{Coc} + v_{dc} = 0 \tag{C.42}$$

$$v_{fb-n} = \frac{v_{dc}}{3} - \frac{(v_{Coa} + v_{Cob} + v_{Coc})}{3} \tag{C.43}$$

Using the deduction in (C.11) on (C.43) yields (C.44).

$$v_{fb-n} = \frac{v_{dc}}{3} \tag{C.44}$$

Since $v_{fa-n} = v_{fb-n}$ and $v_{fb-n} = v_{fc-n} + v_{dc}$ by inspection on equivalent circuit in Figure A.6, (C.45) and (C.46) can be directly obtained from (C.44).

$$v_{fa-n} = \frac{v_{dc}}{3} \tag{C.45}$$

$$v_{fc-n} = -\frac{2v_{dc}}{3} \tag{C.46}$$

SYMMETRICAL COMPONENT ANALYSIS REPORT FOR INTERHARMONIC FREQUENCIES

Symmetrical components are used to represent a three phase system with two sets of balanced phasors and a set of single phase phasor. Balanced three phase phasors are called as positive and negative sequence components, while the single phase phasor is called as zero sequence component. Positive, negative and zero sequence symmetrical components of a three phase system can be deduced using the transformation matrix given in (B.1). Corresponding inverse transformation matrix is also given in (B.2). The symmetrical components transformation matrices in (B.1) and (B.2) are given for current signals however it is also valid for voltage signal.

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} I_0 \\ I_+ \\ I_- \end{bmatrix} \tag{B.1}$$

$$\begin{bmatrix} I_0 \\ I_+ \\ I_- \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{B.2}$$

In equations (B.1) and (B.2), I_a, I_b and I_c are respectively phase a, b and c current phasors, while I_0, I_+ and I_- are respectively zero, positive and negative symmetrical components. The symbol a is a phasor rotation operator which rotates a phasor by 120 degrees, that is $a = e^{2/3\pi i}$. Similarly a^2 is a phasor rotation operator which rotates a phasor by -120 degrees, that is $a = e^{-2/3\pi i}$. In order to analyze the symmetrical components of each of the harmonic and interharmonic components with 5 Hz

resolution, the entire field record is divided into 200msec long windows. For each window, phase *a*, *b* and *c* current records are post-processed via FFT, by this way, magnitude and phase information of each harmonic and interharmonic component corresponding to each phase are derived. When these magnitude and phase information are combined in phasor representation for each phase and multiplied with symmetrical components transformation matrix in (B.2), the phasor representation of positive, negative and zero sequence symmetrical components are reached for any particular data window. In this section of the thesis, symmetrical components of harmonic and interharmonics for the entire measurement period are given in the following figures, which Figure B.1 represents 150 Hz, Figure B.2 represents 250 Hz, Figure B.3 to Figure B.16 represent interharmonics between 265 and 535 Hz with 5 Hz steps, Figure B.17 represents 550 Hz, and Figure B.18 represents 650 Hz components.
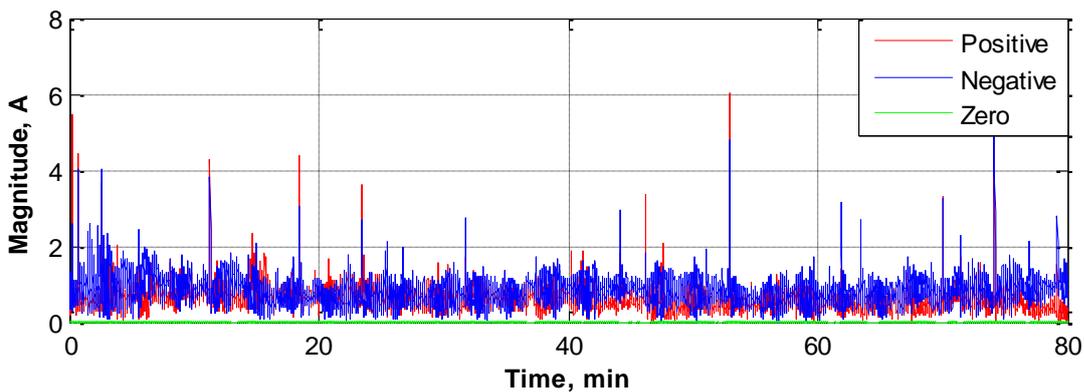
Figure B.1 Symmetrical components of 150 Hz current harmonic of steel melting facility at MV level
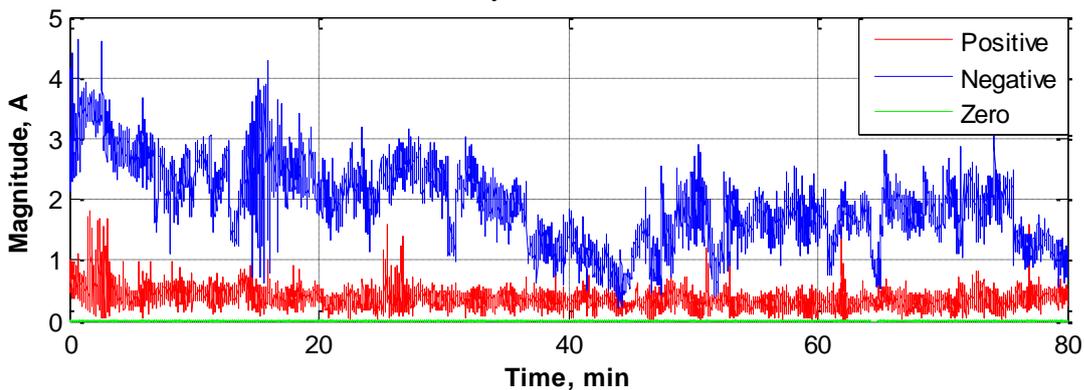
Figure B.2 Symmetrical components of 250 Hz current harmonic of steel melting facility at MV level
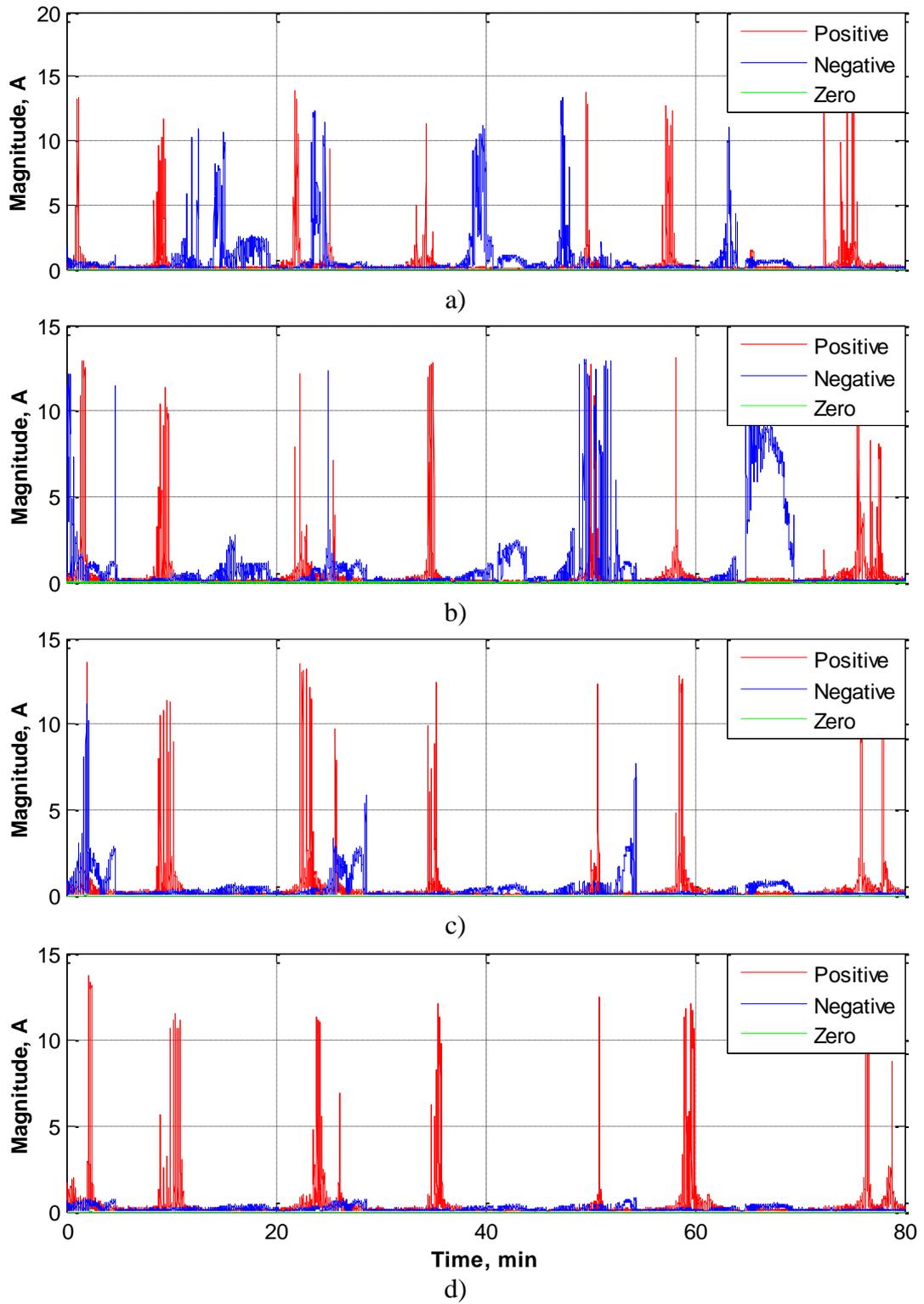
190
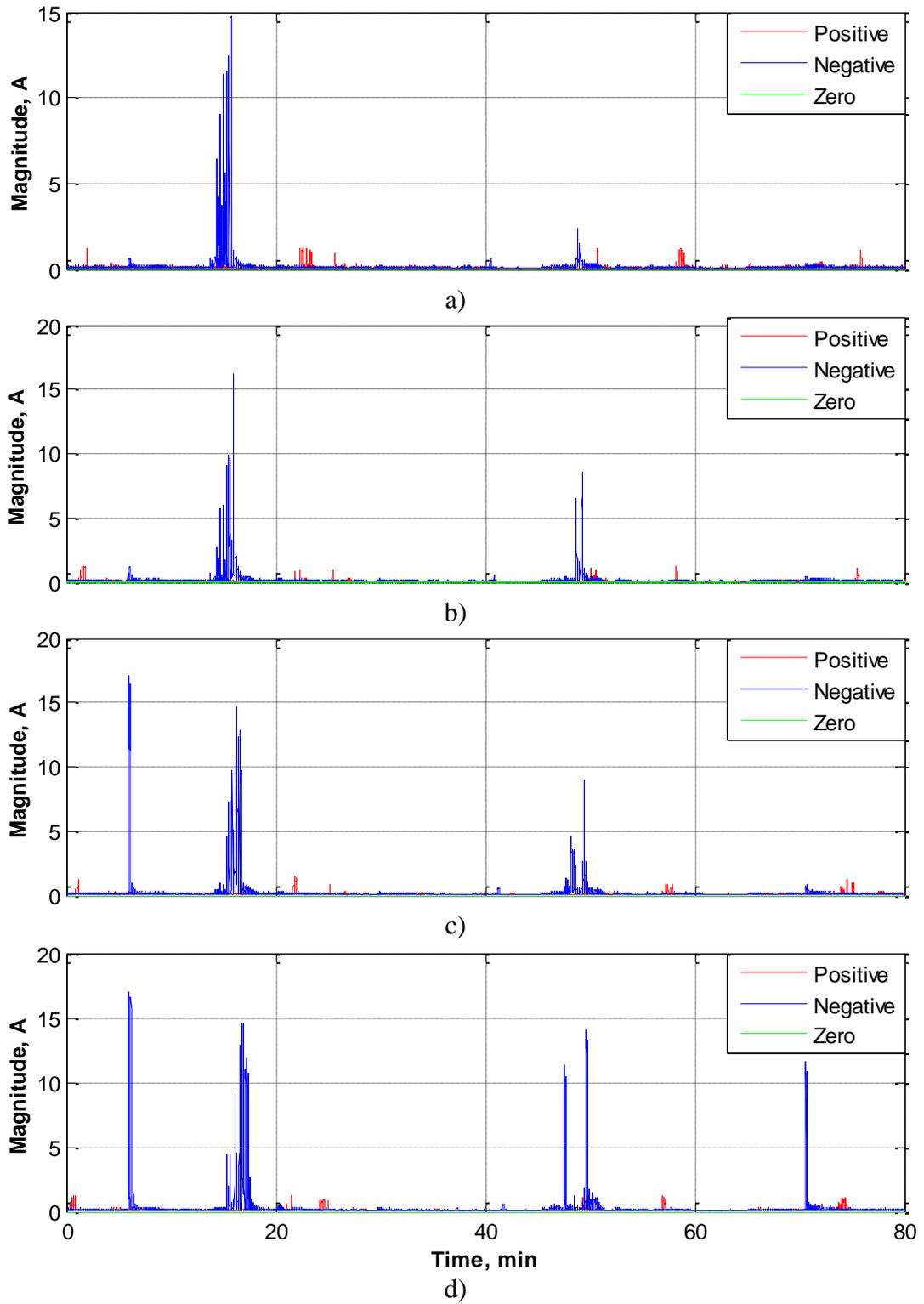
Figure B.3 Symmetrical components of a) 265 Hz, b) 270 Hz, c) 275 Hz, and d) 280 Hz current interharmonics of steel melting facility at MV level
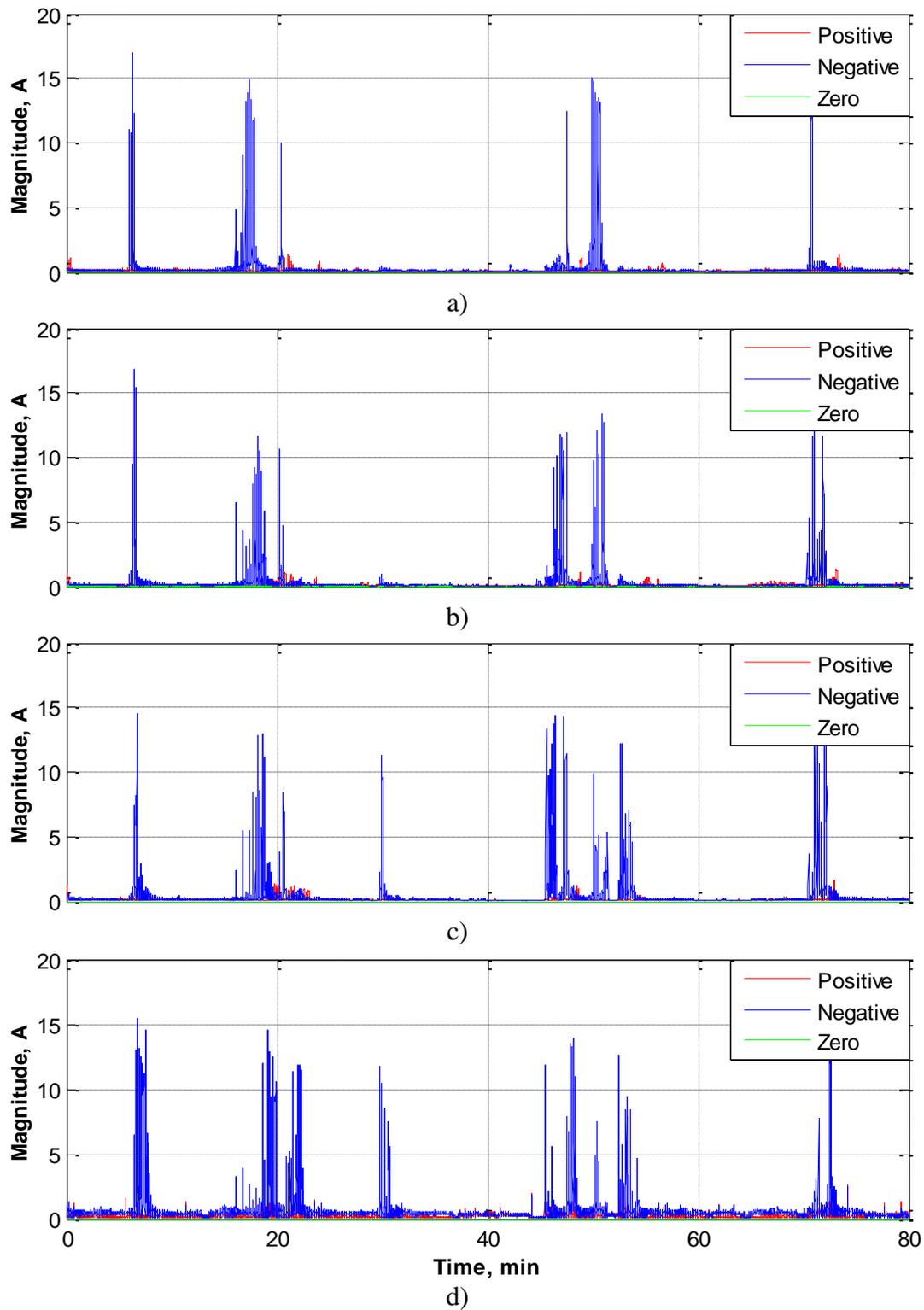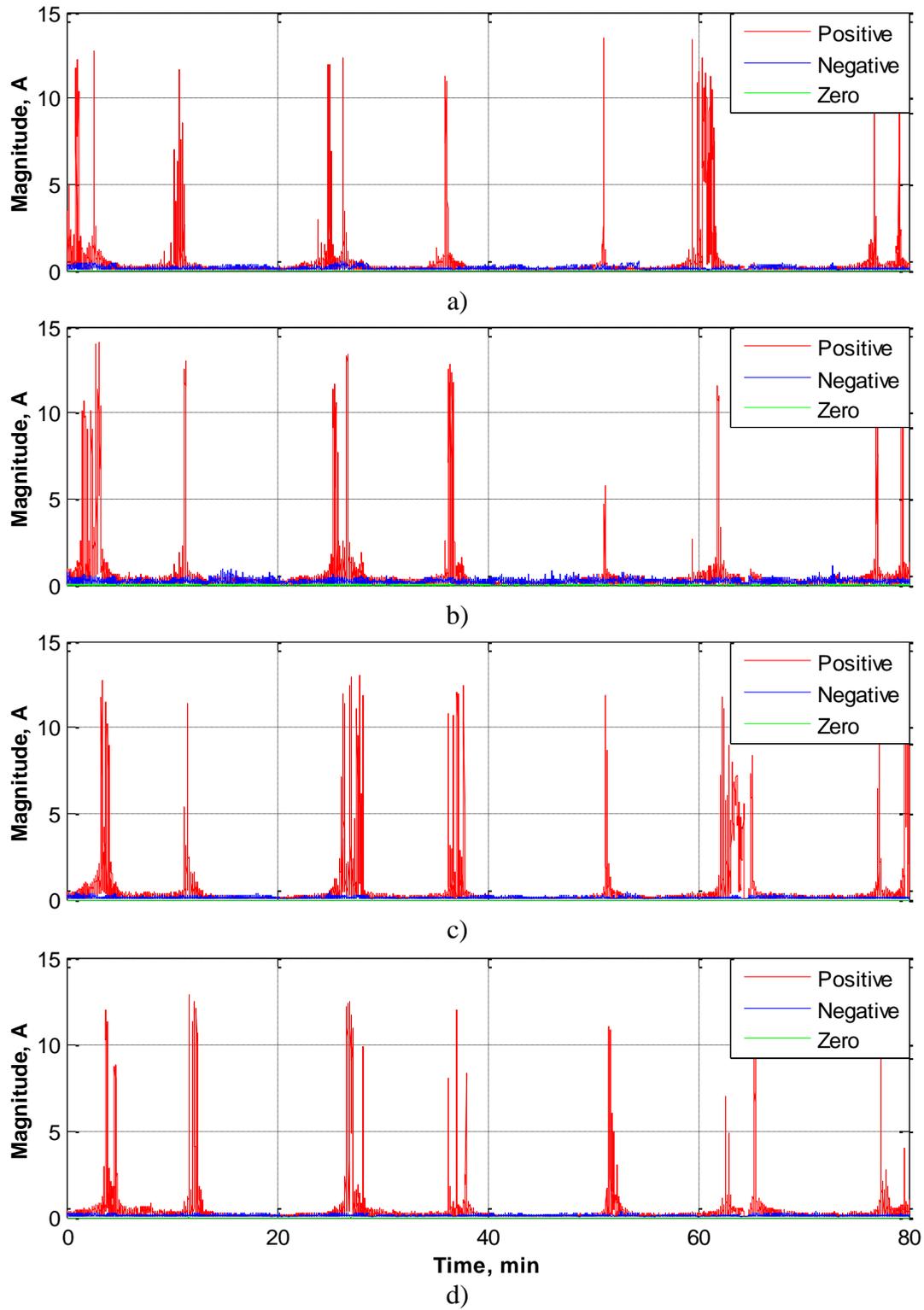
Figure B.4 Symmetrical components of a) 285 Hz, b) 290 Hz, c) 295 Hz, and d) 300 Hz current harmonic and interharmonics of steel melting facility at MV level
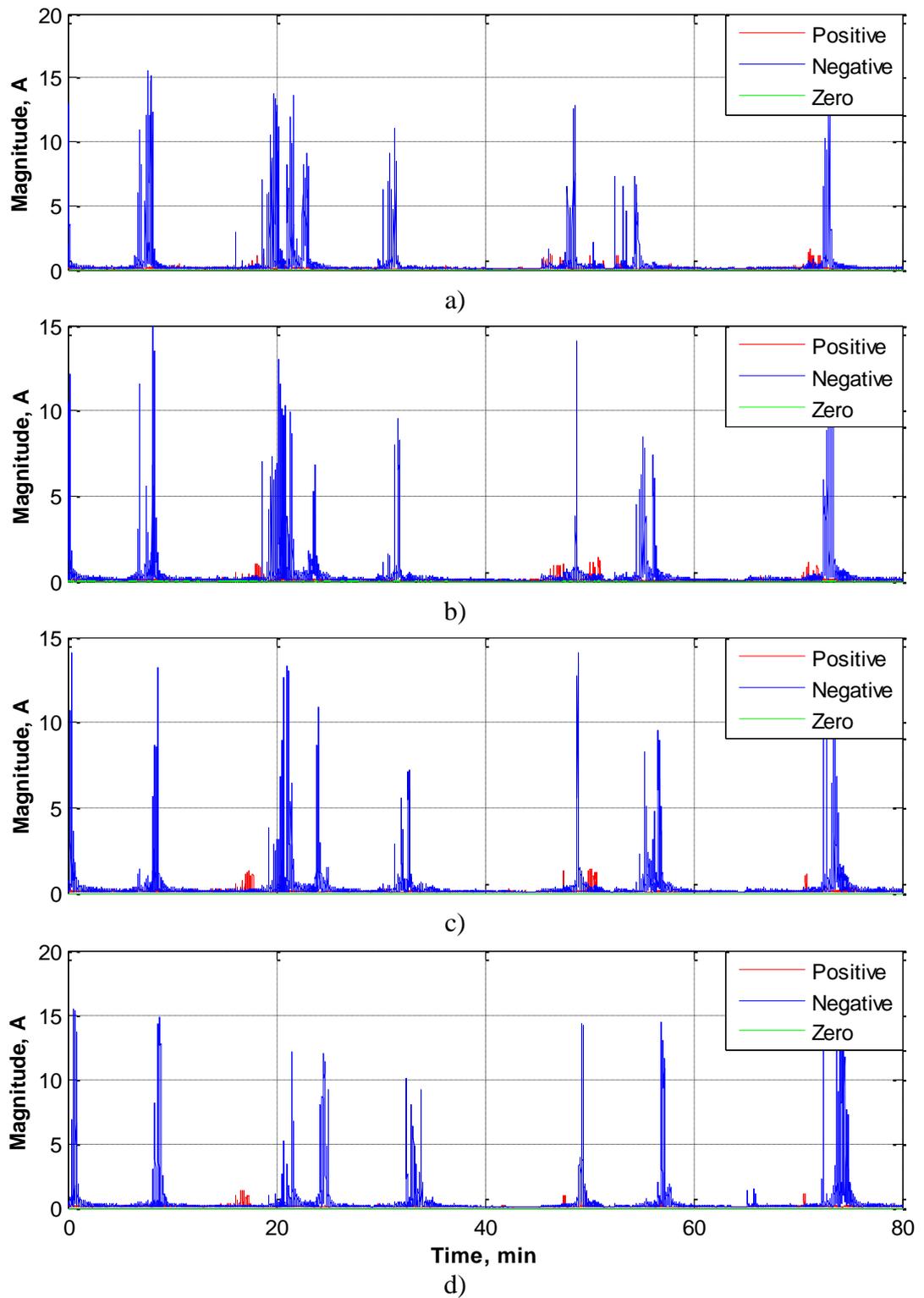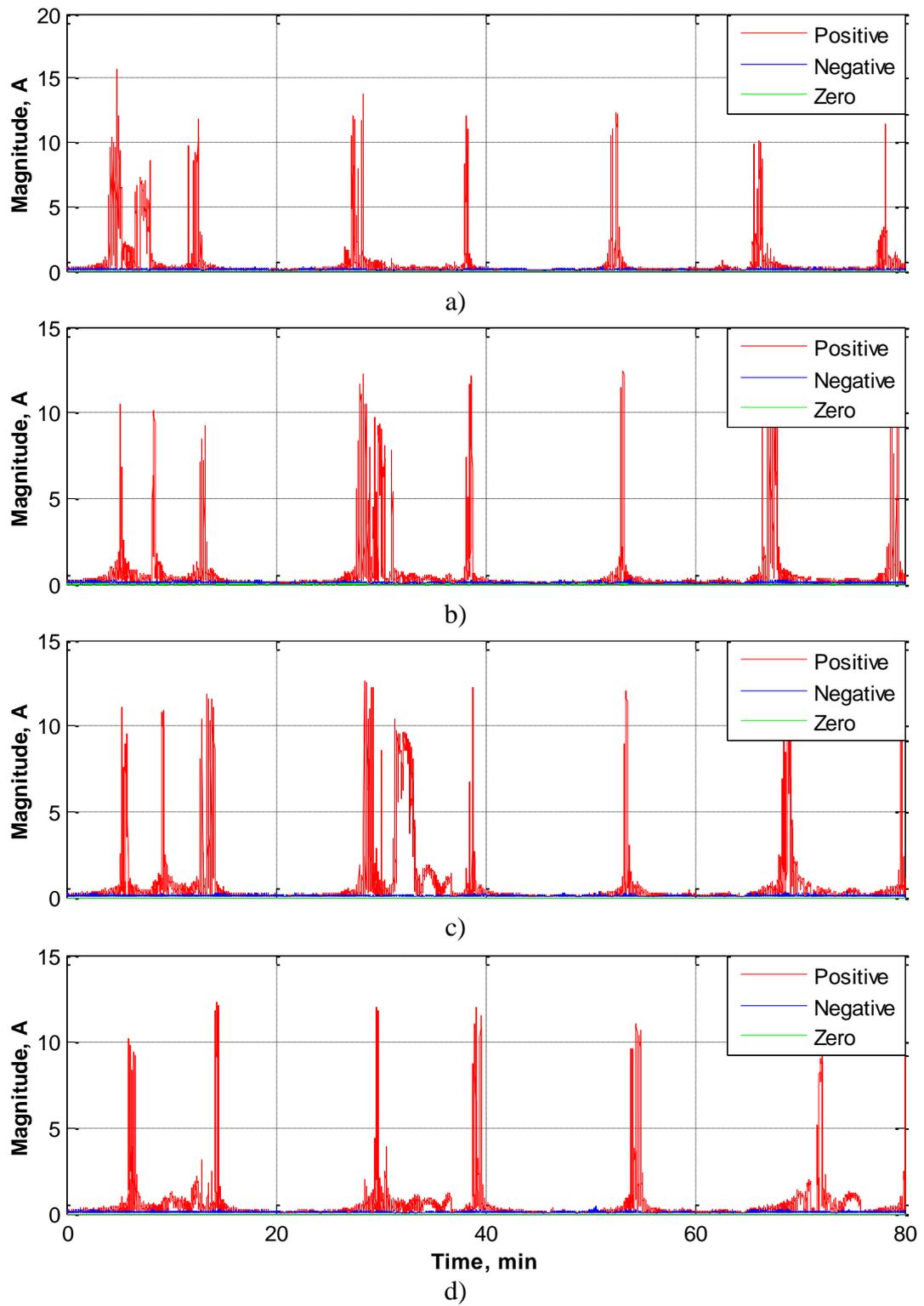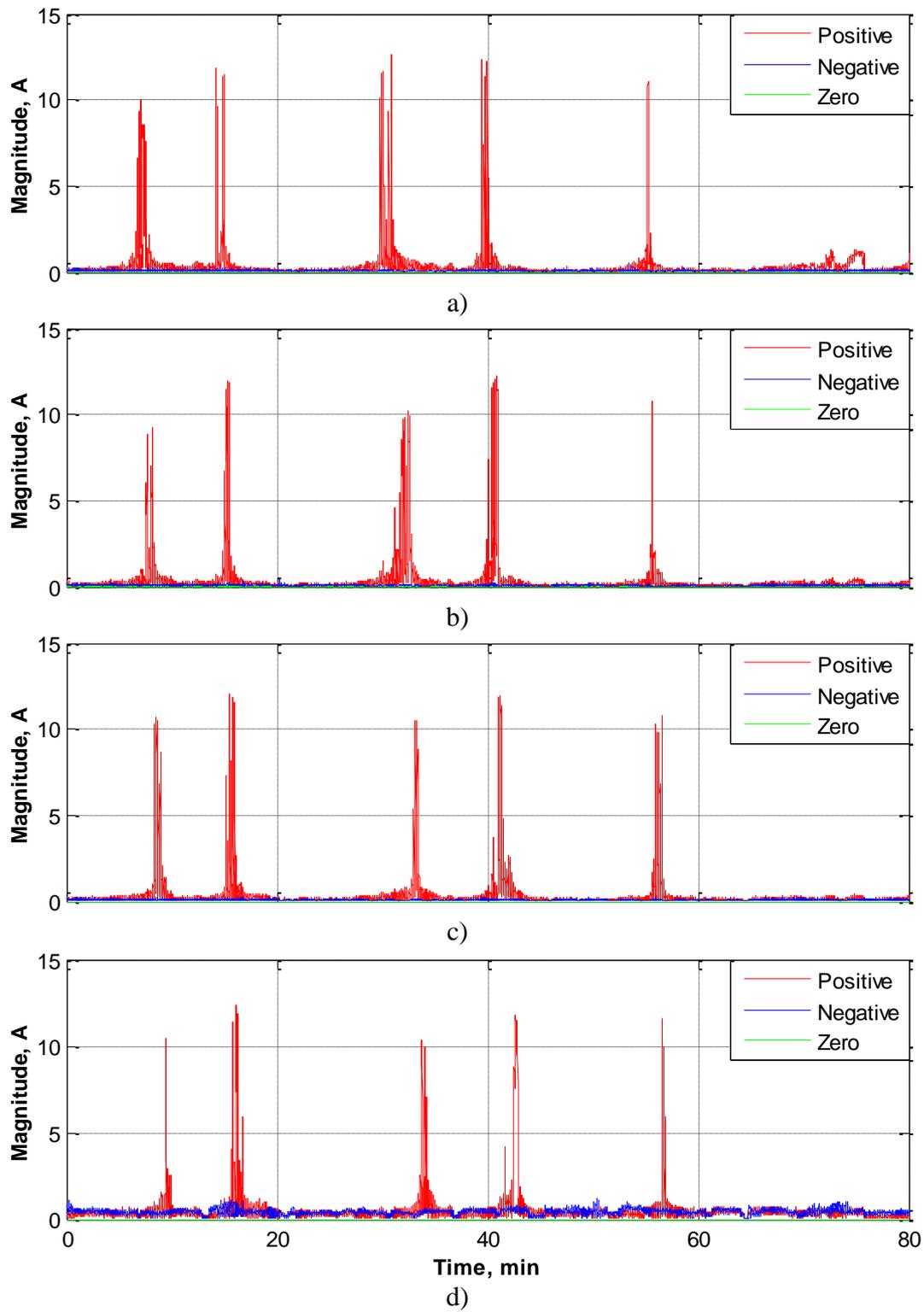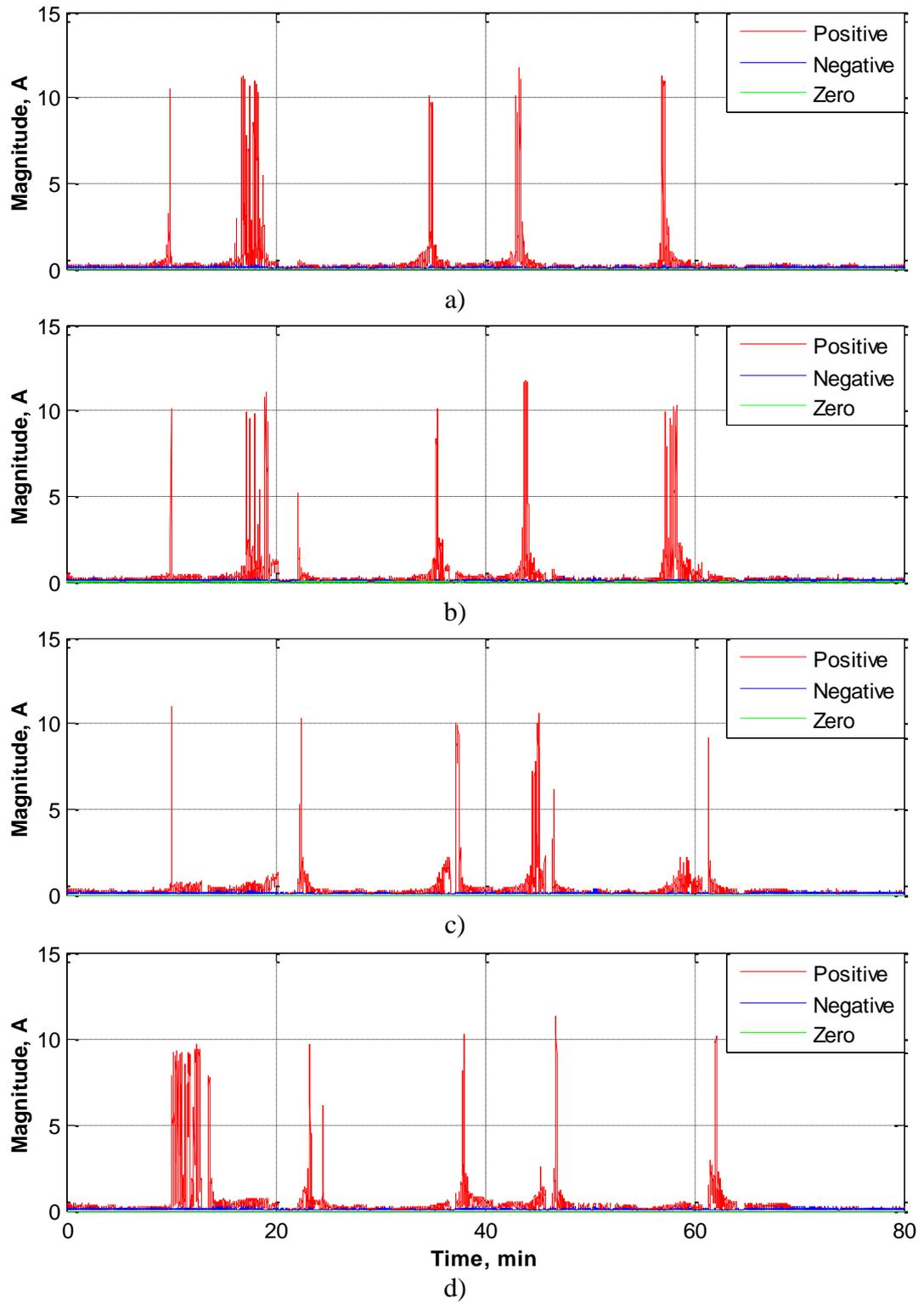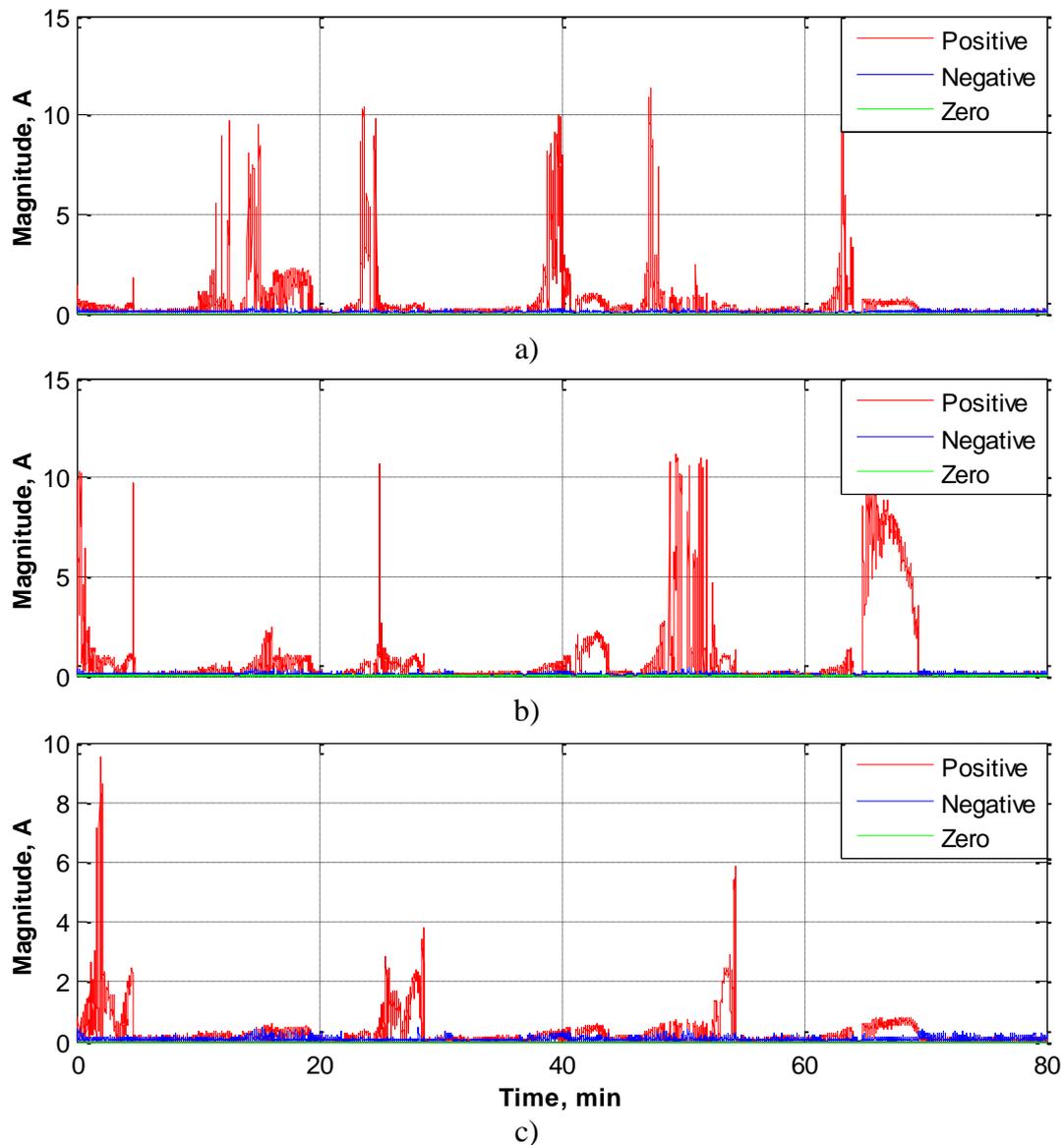
Figure B.5 Symmetrical components of a) 305 Hz, b) 310 Hz, c) 315 Hz, and d) 320 Hz current interharmonics of steel melting facility at MV level
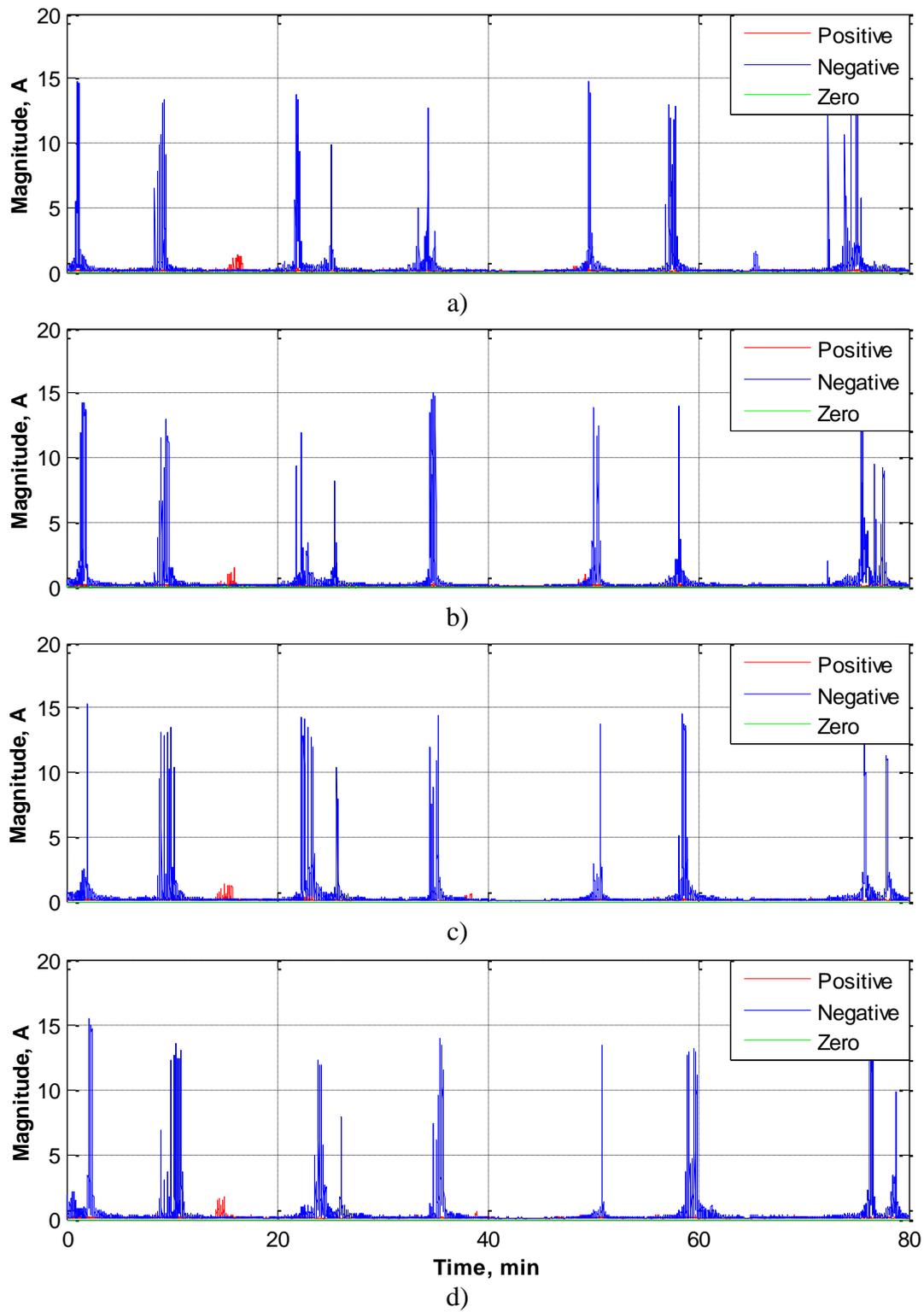
Figure B.6 Symmetrical components of a) 325 Hz, b) 330 Hz, c) 335 Hz, and d) 340 Hz current interharmonics of steel melting facility at MV level
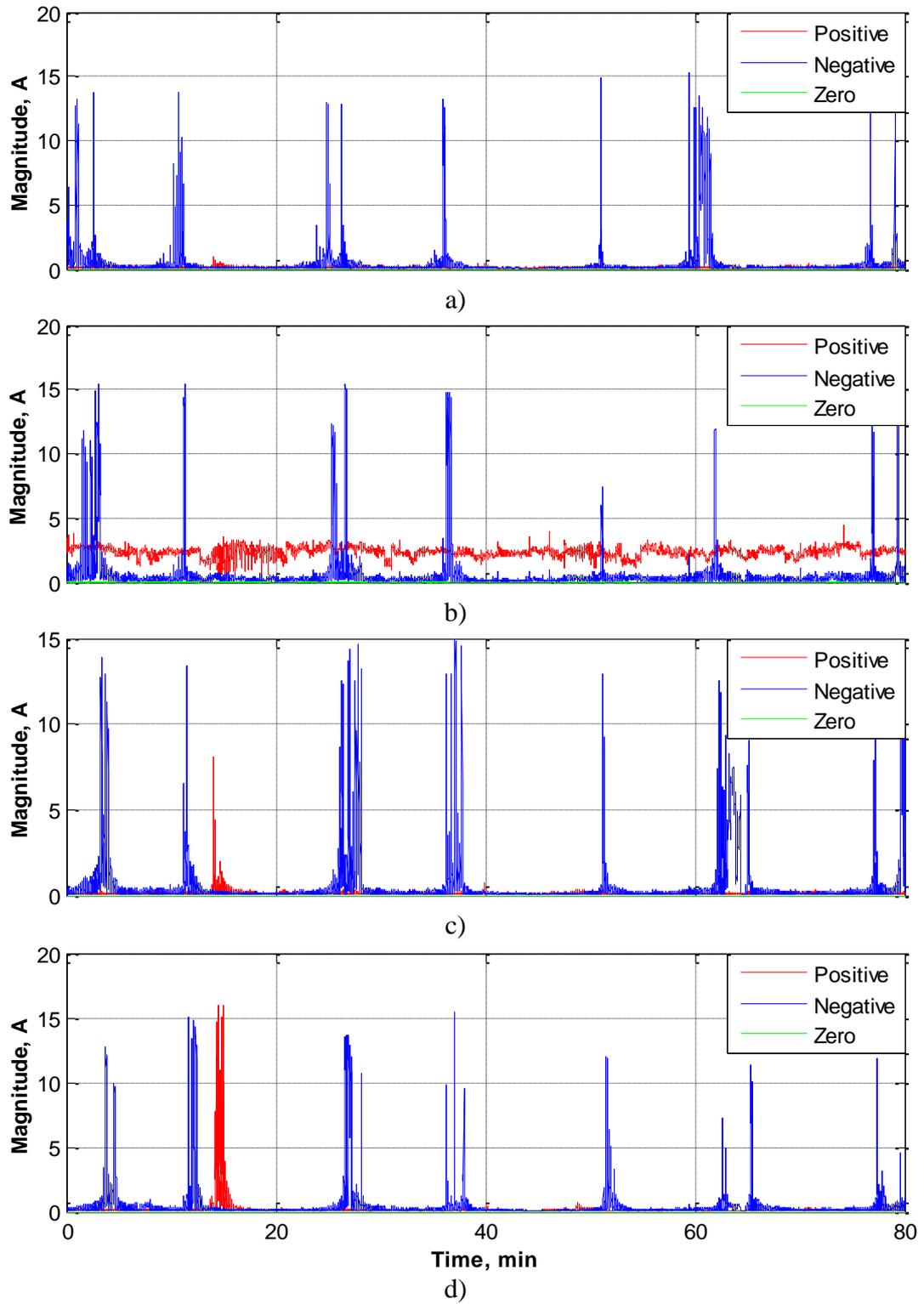
Figure B.7 Symmetrical components of a) 345 Hz, b) 350 Hz, c) 355 Hz, and d) 360 Hz current harmonic and interharmonics of steel melting facility at MV level

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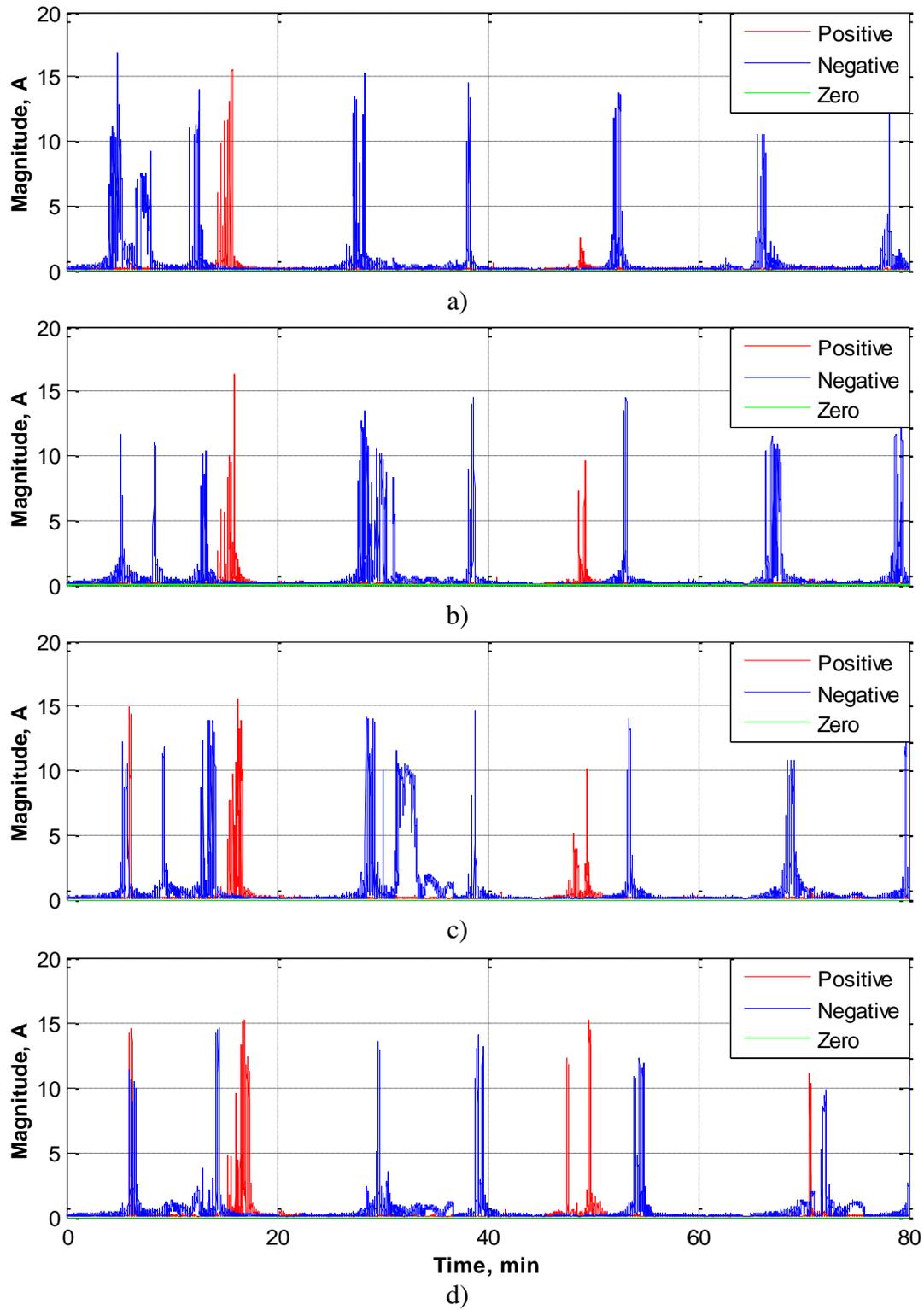
Figure B.8 Symmetrical components of a) 365 Hz, b) 370 Hz, c) 375 Hz, and d) 380 Hz current interharmonics of steel melting facility at MV level
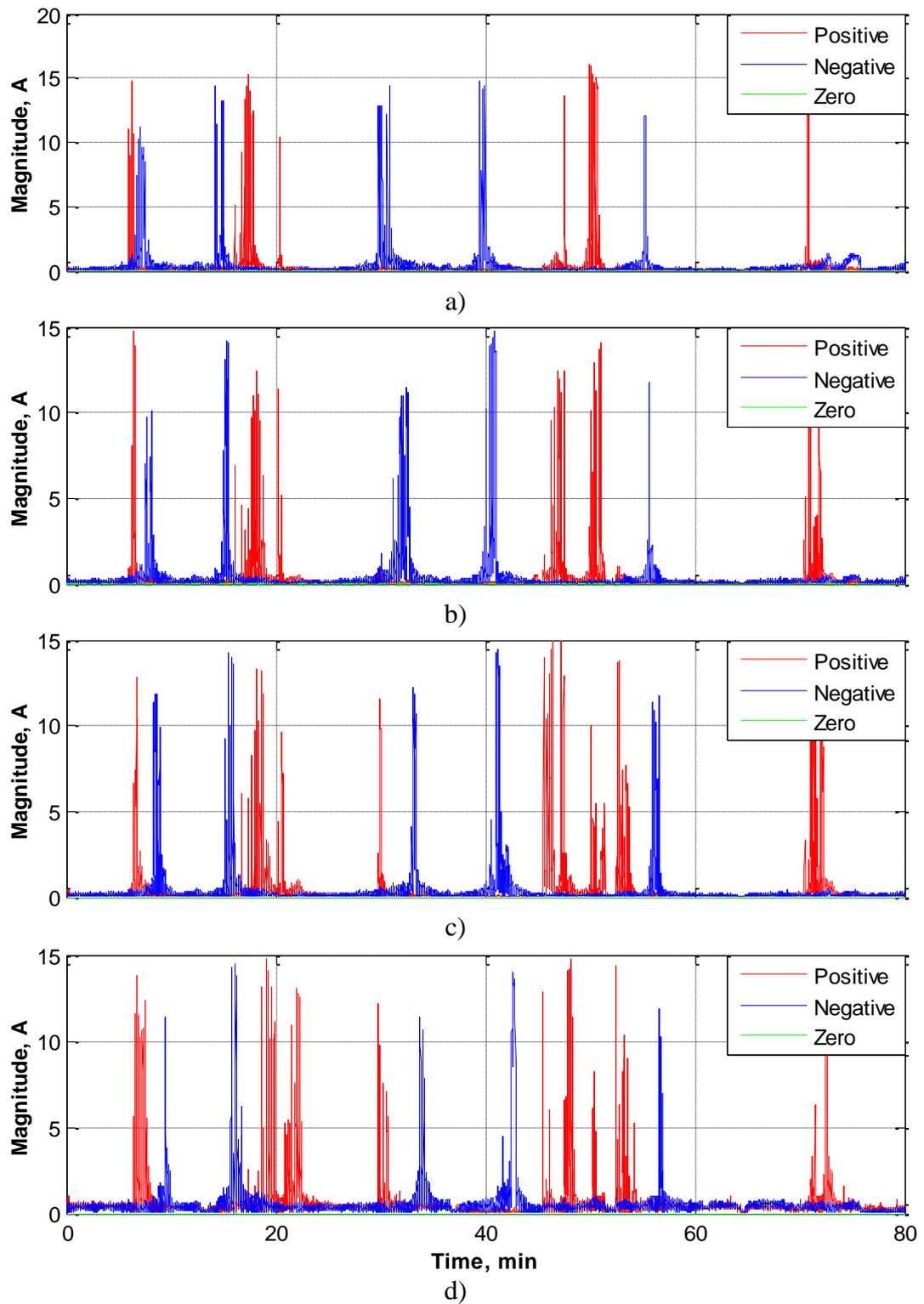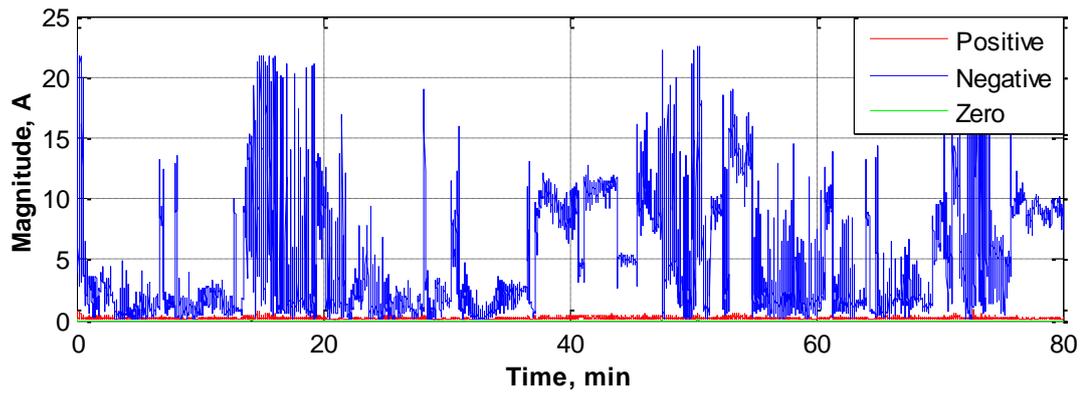
Figure B.9 Symmetrical components of a) 385 Hz, b) 390 Hz, c) 395 Hz, and d) 400 Hz current harmonic and interharmonics of steel melting facility at MV level
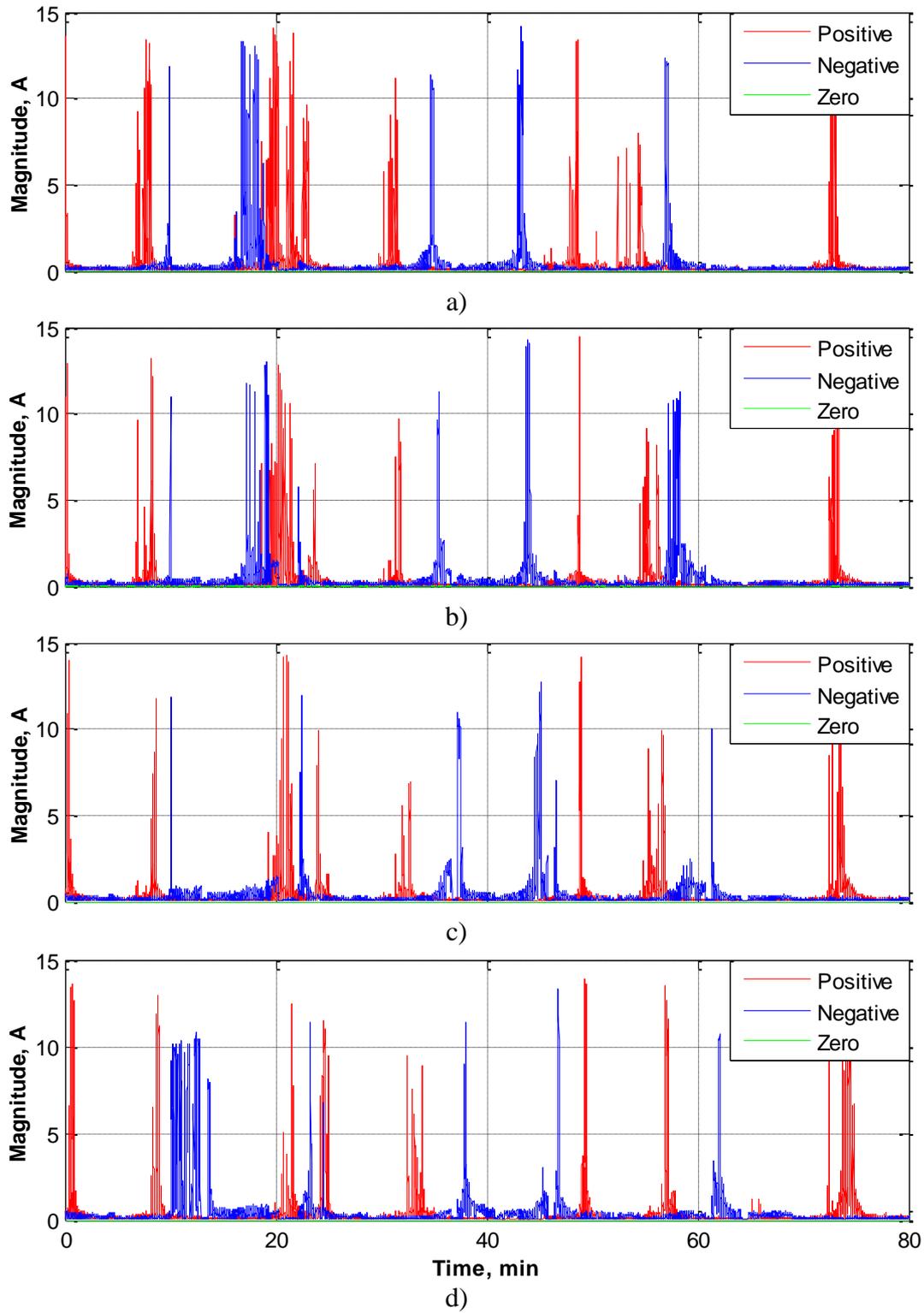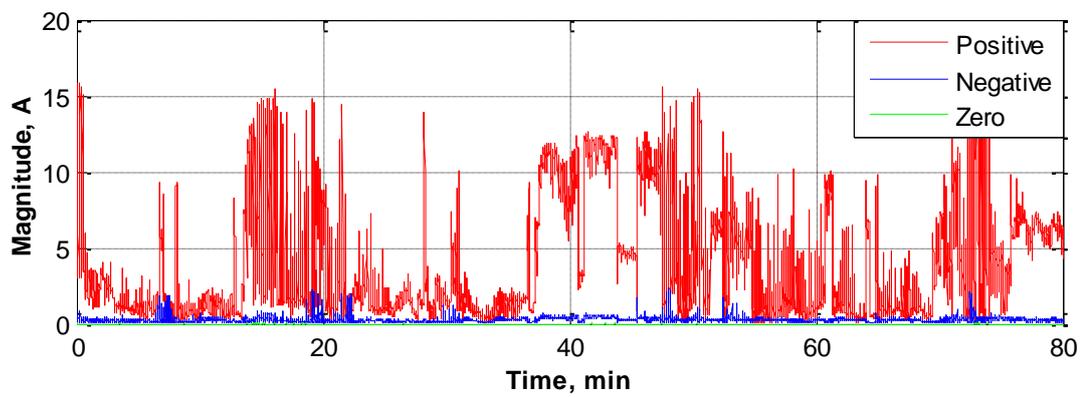
Figure B.10 Symmetrical components of a) 405 Hz, b) 410 Hz, c) 415 Hz, and d) 420 Hz current interharmonics of steel melting facility at MV level

Figure B.11 Symmetrical components of a) 425 Hz, b) 430 Hz, c) 435 Hz, and d) 440 Hz current interharmonics of steel melting facility at MV level

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Figure B.12 Symmetrical components of a) 445 Hz, b) 450 Hz, c) 455 Hz, and d) 460 Hz current harmonic and interharmonics of steel melting facility at MV level

Figure B.13 Symmetrical components of a) 465 Hz, b) 470 Hz, c) 475 Hz, and d) 480 Hz current interharmonics of steel melting facility at MV level

Figure B.14 Symmetrical components of a) 485 Hz, b) 490 Hz, c) 495 Hz, and d) 500 Hz current harmonic and interharmonics of steel melting facility at MV level

Figure B.15 Symmetrical components of a) 505 Hz, b) 510 Hz, c) 515 Hz, and d) 520 Hz current interharmonics of steel melting facility at MV level

Figure B.16 Symmetrical components of a) 525 Hz, b) 530 Hz, and c) 535 Hz current interharmonics of steel melting facility at MV level

Figure B.17 Symmetrical components of 550 Hz harmonic current component of steel melting facility at MV level

Figure B.18 Symmetrical components of 650 Hz harmonic current component of steel melting facility at MV level

APPENDIX C

HARMONIC ANALYSIS REPORT

Current and voltage waveforms of steel melting facility under investigation by the research work have been collected at MV level and are analyzed in terms of harmonic content in this section of the thesis. Since international standards suggests limits for harmonics only, interharmonic content is not considered for this harmonic analysis report.

Field measurements have been collected during 26 days by a multipurpose power quality analyzer [100] with data sampling rate of 25.6 kHz. Sampled data has been post-processed by using Fourier Transform in 200 ms window, resulting in 5 Hz resolution. Subgroup harmonics [100] are used to determine exact value of each individual harmonic component. Figure C.1 - Figure C.10, represents the magnitudes of each individual harmonic up to 40th as a percentage of maximum demand (I_L). In addition to individual harmonics, TDD curve is given in Figure C.11. It is deduced from Figure C.1 - Figure C.11 that the proposed solution to the harmonic problem of IMF load under investigation is very effective for the suppression of even and odd harmonics and successfully mitigates them below allowed limits except some high frequency ones. Figure C.8 shows that the proposed system has no significant effect on 23rd and 25th harmonics. Thus, a passive filter solution tuned to a proper frequency in between 23rd and 25th harmonics should be implemented for mitigating them below allowed limits. It is also seen from the report that high frequency harmonic components, especially the ones larger than 20th harmonic, sometimes exceeds the limit.
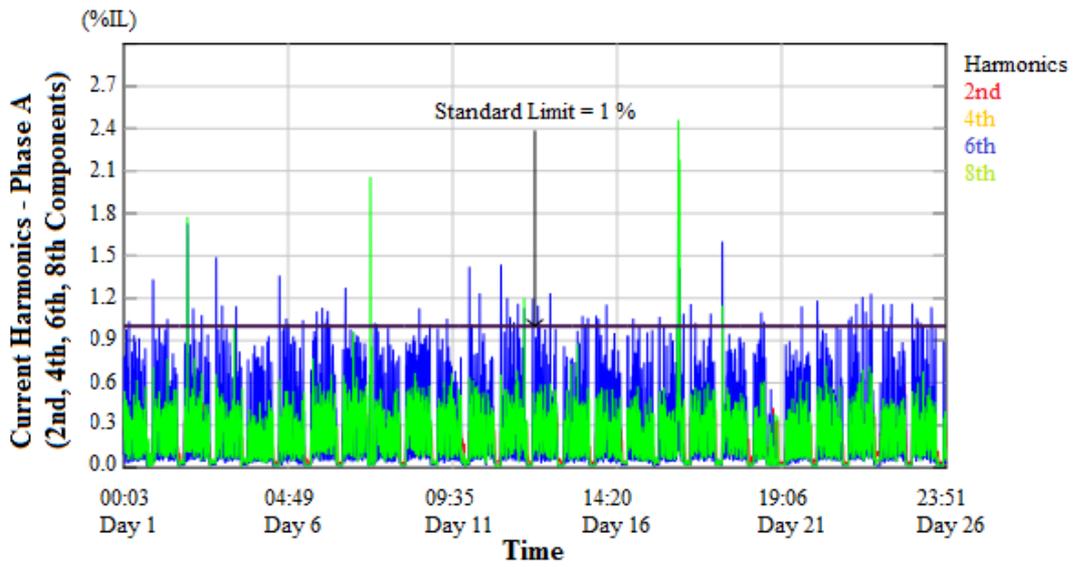
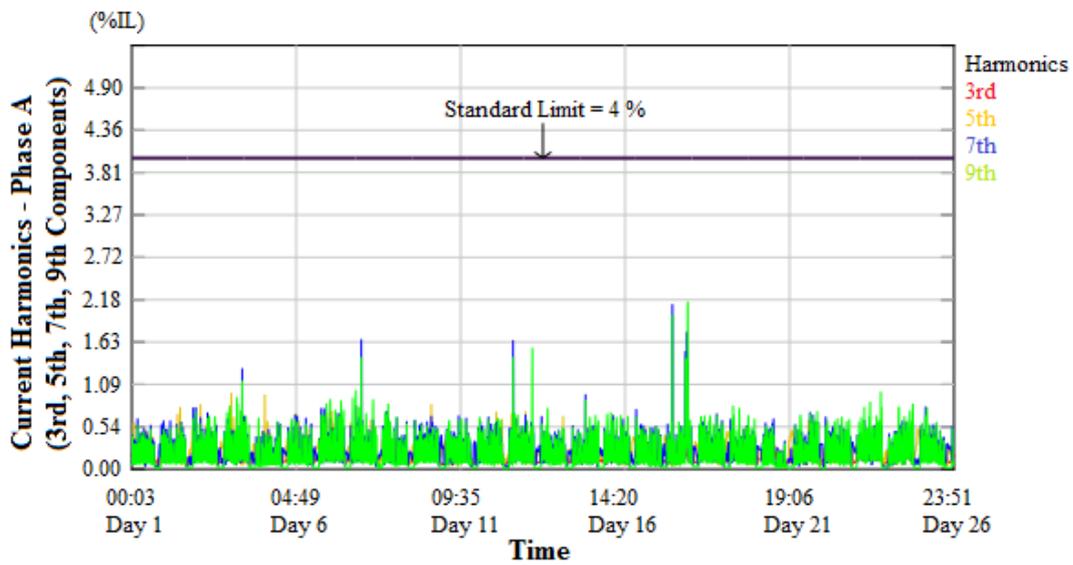**Figure C.1** 2nd, 4th, 6th and 8th current harmonics of steel melting facility at MV level

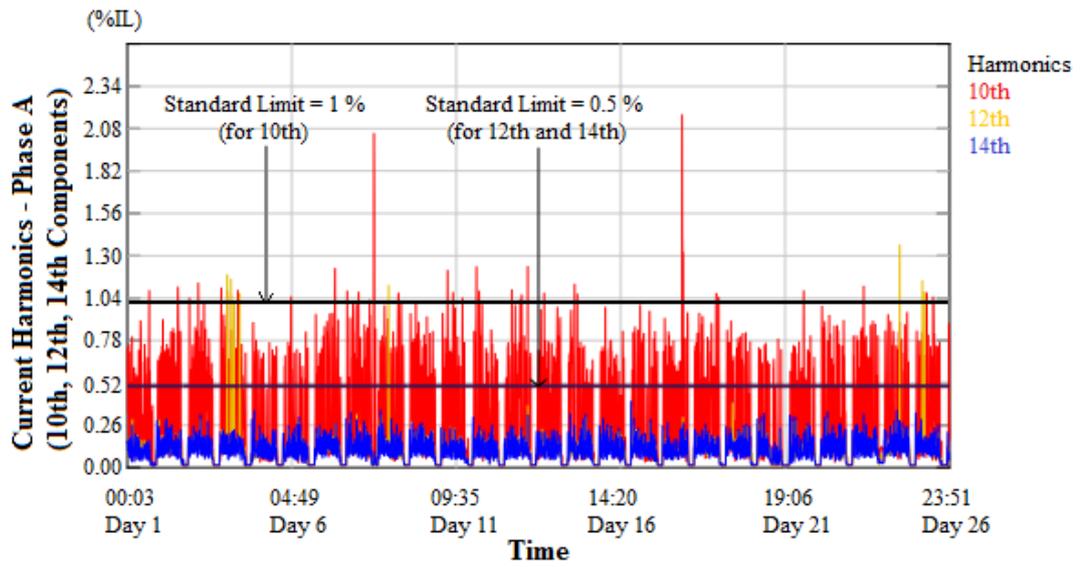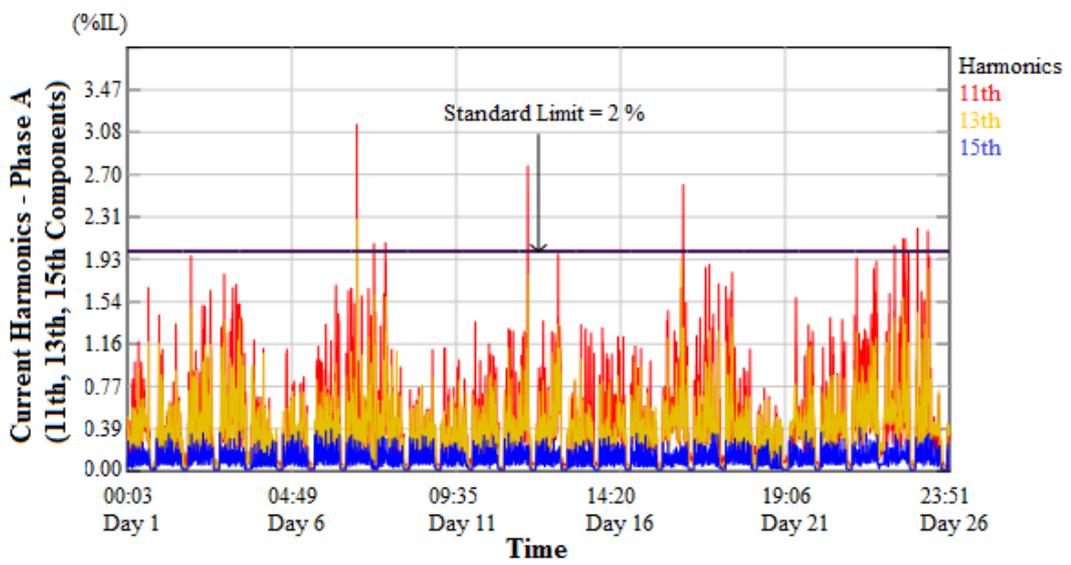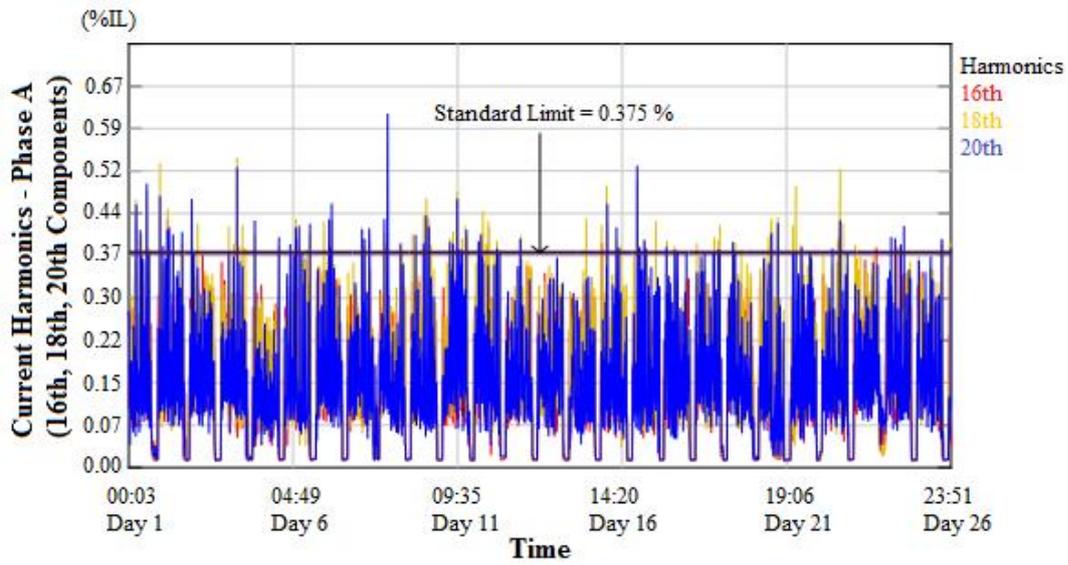**Figure C.2** 3rd, 5th, 7th and 9th current harmonics of steel melting facility at MV level

Figure C.3 10th, 12th and 14th current harmonics of steel melting facility at MV level

Figure C.4 11th, 13th and 15th current harmonics of steel melting facility at MV level

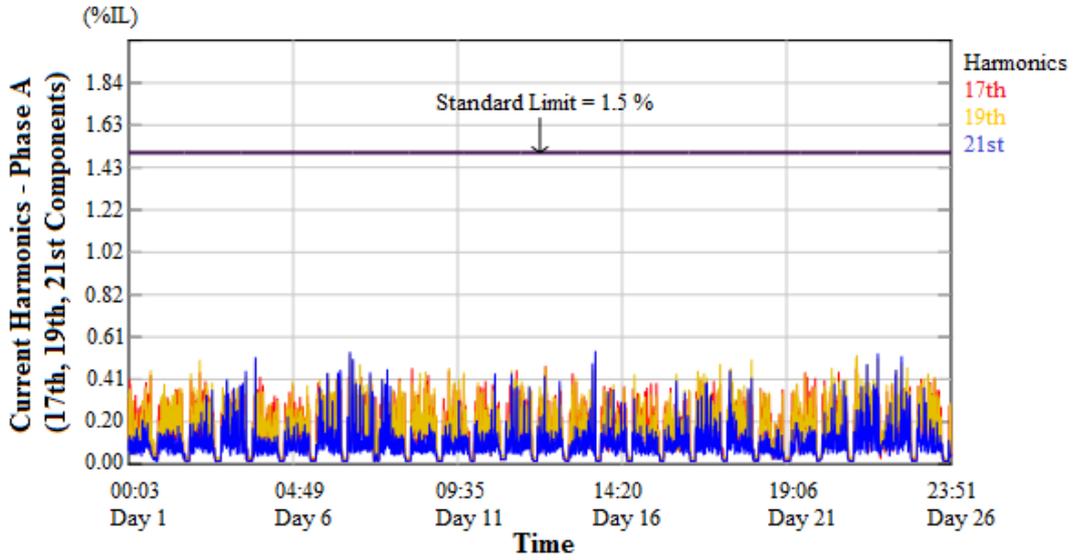**Figure C.5** 16th, 18th and 20th current harmonics of steel melting facility at MV level

Figure C.6 17th, 19th and 21st current harmonics of steel melting facility at MV level
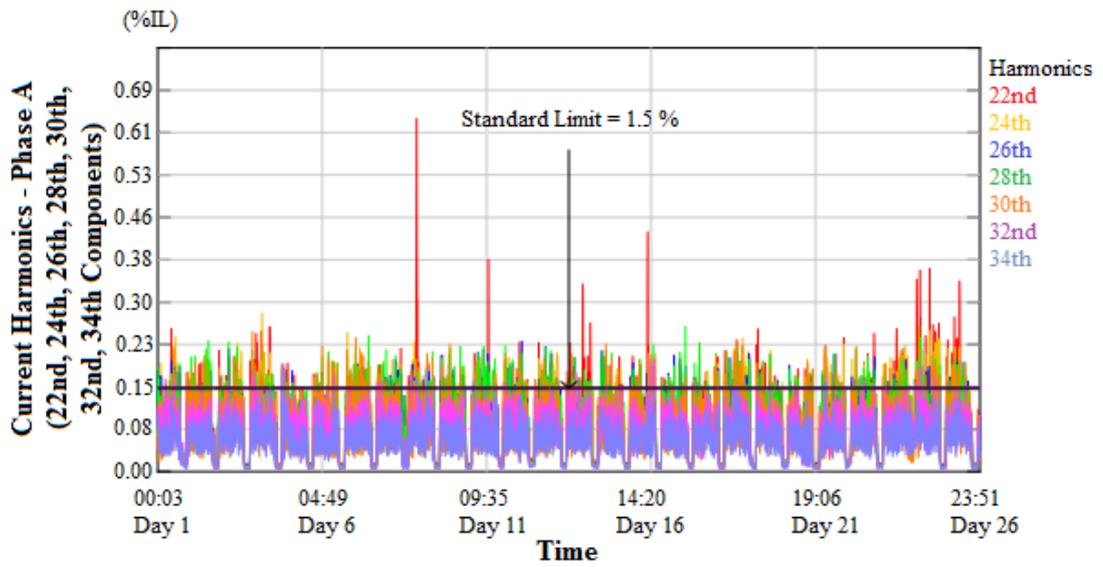
Figure C.7 22nd, 24th, 26th, 28th, 30th, 32nd and 21st current harmonics of steel melting facility at MV level
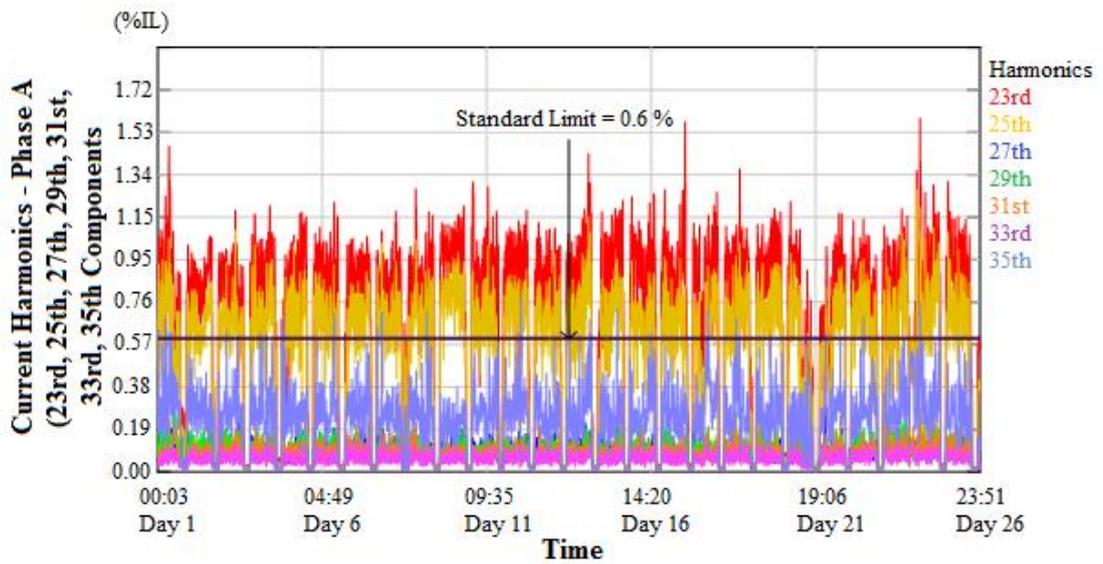
Figure C.8 23rd, 25th, 27th, 29th, 31st, 33rd and 35th current harmonics of steel melting facility at MV level

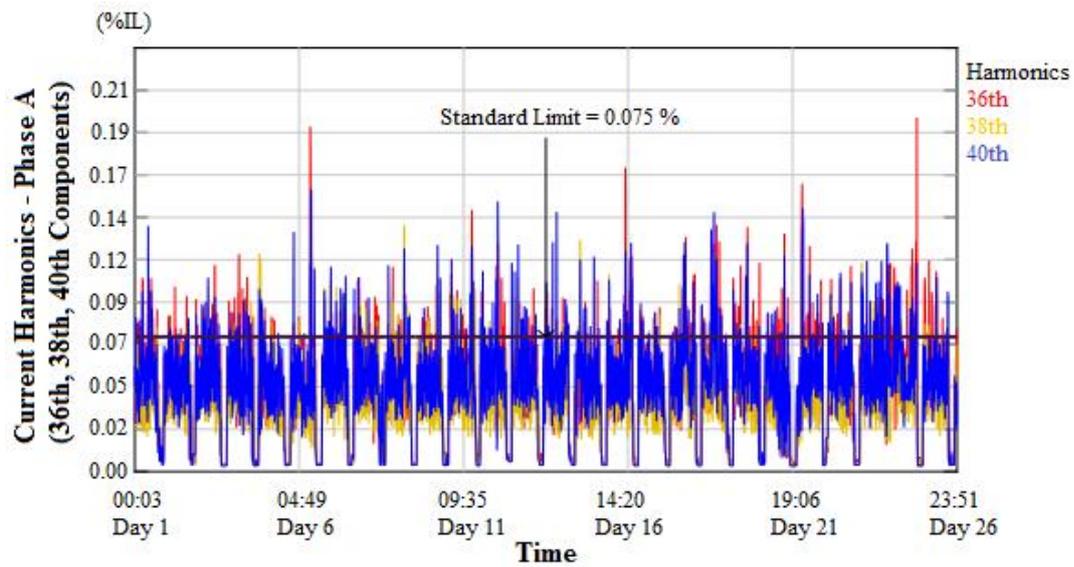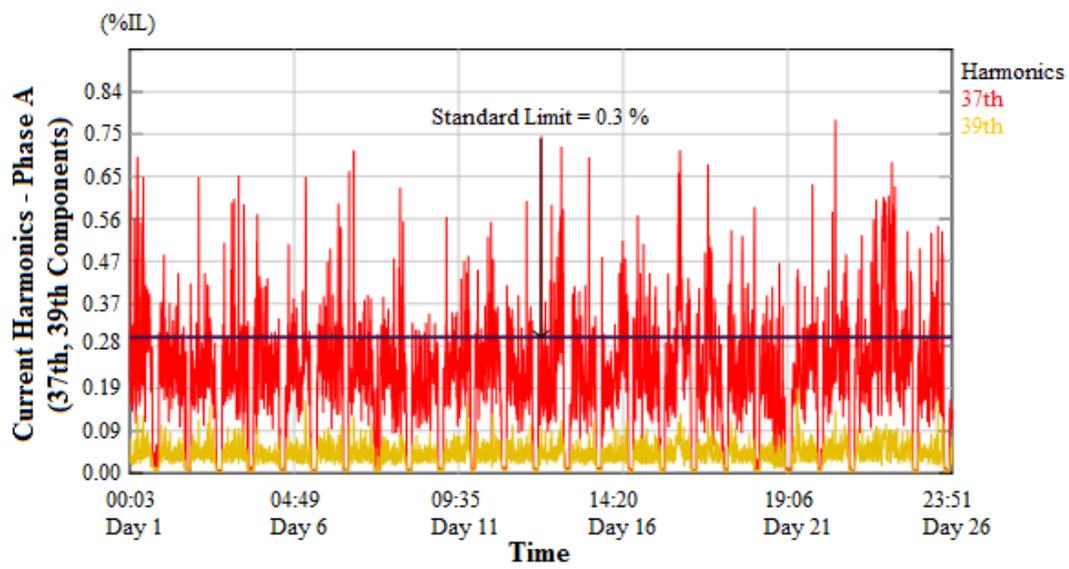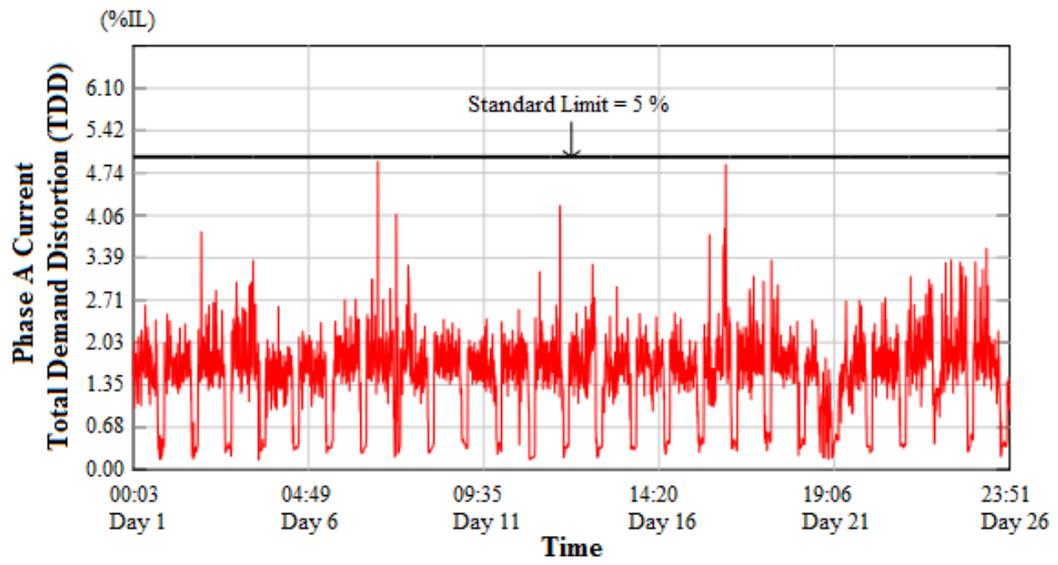**Figure C.9** 36th, 38th and 40th current harmonics of steel melting facility at MV level

Figure C.10 37th and 39th current harmonics of steel melting facility at MV level

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Figure C.11 Current Total Demand Distortion (TDD) of the steel melting facility at MV level

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Peer Reviewer: ECCE '16, INTELEC '17, APEC 17', APEC '18

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1. E. Durna, "Adaptive Fuzzy Hysteresis Band Current Control for Reducing Switching Losses of Hybrid Active Power Filter", *IET Power Electronics*, vol. 11, no. 5, pp. 937-944, 2018.

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