DIFFERENTIAL K-BAND VECTOR MODULATOR IC DESIGN AT 180 NM CMOS SOI PROCESS

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ABSTRACT

DIFFERENTIAL K-BAND VECTOR MODULATOR IC DESIGN AT 180 NM CMOS SOI PROCESS

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Massive MIMO and beamforming are technologies that may enable ultrafast 5G network. They are predicted to be used widely in next-generation high capacity communication systems. In the implementation of beamforming and MIMO, the large number of antennas and RF control components are utilized. However; some challenges related to power consumption, control complexity, cost, and size of transceiver have arisen. Vector Modulator (VM) may be one possible effective solution to these challenges because it merges the tasks of both phase shifter and attenuator. In other words, VM controls both amplitude and phase of RF signal with simple control and the reasonable cost and size.

In this thesis work, the design of SOI-based RFIC vector modulator is presented. VM is targeted to operate in 20-25 GHz, possible 5G band. Vector modulator consists of passive parts, which are baluns, Lange quadrature coupler, Wilkinson in-phase combiner, and active parts, which are digital step attenuator (DSA) and switch matrix. Switch matrix and DSA, which are composed of active switches and resistances, are designed and optimized with Cadence Design System. Spiral Marchand baluns,

Lange quadrature coupler and Wilkinson in-phase combiner are designed and simulated with Sonnet's 3D Electromagnetic Software.

Finalized VM design is simulated and results are presented. Final design has 6.5 dB insertion loss, better than 10 dB return loss, 48 dBm IIP_3, 38 dBm input P_{1dB}, 0.5 dB amplitude and 1-degree phase resolution in active regions, where outputs can take value.

Keywords: RFIC, MMIC, Vector Modulator, Digital Step Attenuator, Phase Shifter, Phased Array Systems

ÖZ

180 NM CMOS SOI PROSESİNDE FARKSAL K-BAND VEKTÖR MODÜLATÖR ENTEGRE DEVRE TASARIMI

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Yüksek kapasite ve hızdaki 5G ağlarını oluşturan temellerden; Büyük ölçekli çoklu-girdi çoklu-çıktı ve hüzmeleme teknolojilerinin gelecekte yaygın olarak kullanılacağı tahmın ediliyor. Büyük ölçekli çoklu-girdi çoklu-çıktı ve hüzmeleme teknolojilerinde çok sayıda anten ve RF kontrol elemanları gerekiyor. Bu da güç tüketimi, kontrol zorluğu, maliyet ve alan açılarından alıcı-verici devrelerinde sınırları zorlamaktadır. Genlik ve faz kontrolünü beraber yapabilen Vektör Modülator(VM), kabul edilebilir maliyet ve alanıyla gelecek uygulamalarda olası çözüm olarak gözüküyor.

Bu tez çalışmasında, CMOS SOI tabanında üretilmek üzere tasarlanmmış bir Vektör Modülatör sunulmaktadır. Vektör Modülatör, olası 5G bandı olan 20-25 GHz bandında çalışacak şekilde tasarlanmıştır. VM farksal olarak tasarlanmıştır ki farksallığın gürültü bağışıklılığı, ortak-mod karışıklığı bastırma gibi avantajlarından kullanılsın. Balun, Lange kuplör, Wilkinson güç bölücü vektör modülatörde kullanılan pasif elemanlardır. Sayısal zayıflatıcı ve anahtar matrisi ise kullanılan aktif elemanlardır. Aktif anahtar, direnç ve kapasitanslardan oluşan aktif kısımların tasarımı ve optimi-

zasyonları Cadence Design System kullanılarak yapıldı. Pasif kısımlar ise Sonnet 3D Electromagnetic kullanılarak tasarlanıp optimize edildi.

Son VM tasarımı 6.5 dB araya girme kaybı, 10 dB'den iyi geri dönüş kaybı, 48 dBm IIP_3, 38 dBm giriş P_{1dB}, 0.5 dB genlik ve 1 derecelik faz çözünürlüğüne sahiptir.

Anahtar Kelimeler: RFIC, MMIC, Vektör Modülatör, Sayısal Sinyal Zayıflatıcı, Faz kaydırıcı, Faz dizili sistemler

To my loving parents

Cengiz and Esra

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In the end, I want to thank God Almighty. Since the perfections found in all beings which are the cause of acclaim and tribute are His, praise too belongs to Him.

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LIST OF ABBREVIATIONS

CAD	Computer Aided Diagnosis
CMOS	Complementary Metal Oxide Semiconductor
DSA	Digital Step Attenuator
FET	Field Effect Transistor
GSM	Global Systems for Mobile Communications
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
LSB	Least Significant Bit
MMIC	Microwave Monolithic Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon On Insulator
TTL	Transistor-Transistor Logic
VM	Vector Modulator

CHAPTER 1

INTRODUCTION

Wireless networks are evolving in order to satisfy the demand of the community. For example; at the 1980s, 1G was the just voice-centric analog communication system. However, today, 4G provide us text messaging, internet access, media entertainment, and social networks etc., which became the parts of our life. For the community demands of next decades, 4G seems to be insufficient. In order to satisfy future community demands, scientists and industry work on the 5th generation of mobile networks (5G).

Envisaged future demands and challenging 5G targets aiming to fulfill these demands can be explained as follows.

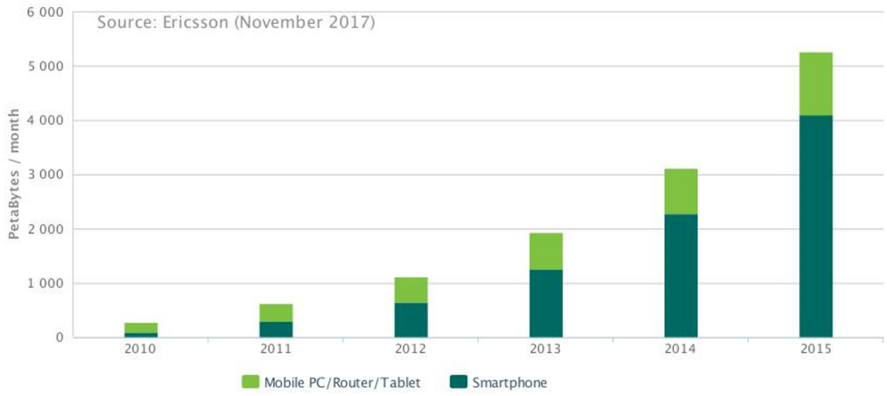

Figure 1.1: Monthly Data Usage from 2010 to 2015 [1]

First, according to Ericsson reports, data traffic created by smartphone, mobile PC, router, and tablets has 20 times growth during 2010-2015, as in Figure 1.1. Similar growth is expected from 2015 to 2023, as shown in Figure 1.2. In addition to increase in today's mobile devices (smartphones, tablets etc.), many new IoT devices

and smart applications will need to use the mobile network, which all result in huge mobile data traffic in the future. Therefore, to satisfy future network demand, one of the challenging design targets of 5G is having x1000 network capacity than today's capacity.

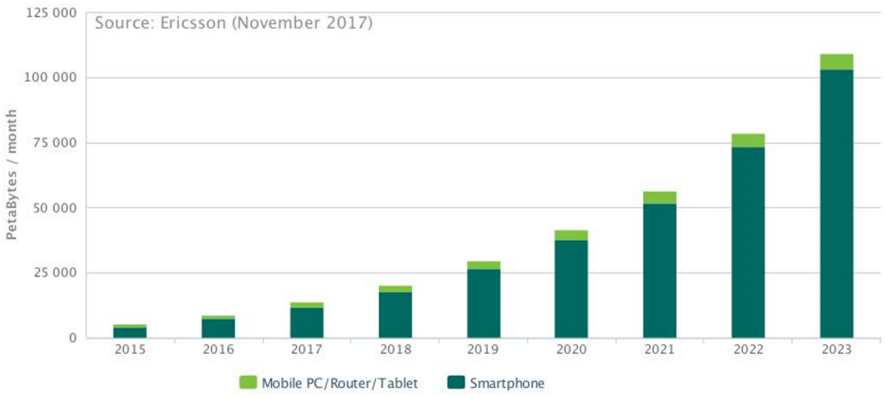

Figure 1.2: Monthly Data Usage from 2015 to 2023 [1]

Secondly, demand for media entertainment such as augmented reality, high definition and 3D video are increasing drastically. As shown in Figure 1.3, while mobile video traffic is less than half of the total mobile data traffic in 2015; in 2023, mobile video traffic is envisaged to be more than 80% of total traffic.

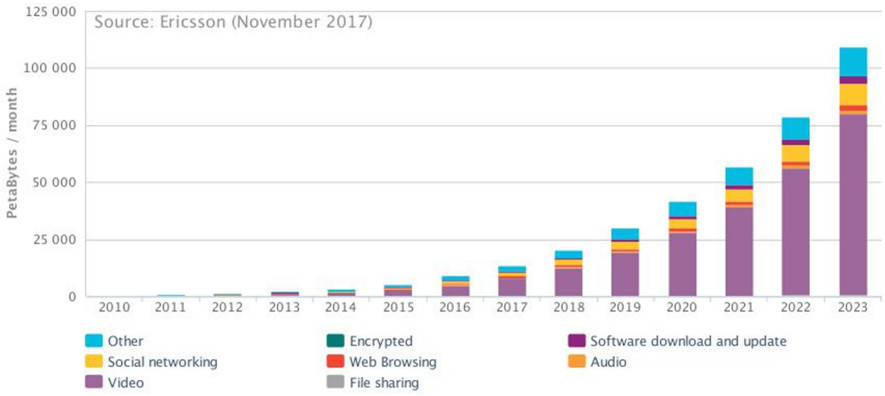

Figure 1.3: Distribution of Applications in Total Data Traffics [1]

However, mobile access to high-quality multi-media service requires fast mobile internet experience. Therefore, another challenging target of 5G is fiber-like mobile internet with peak rates of up to 10 Gbps for stationary users and 1 Gbps for mobile

users. This means 10 times faster than 4G LTE.

Thirdly, smart cities, autonomous driving, public safety robots with haptic feedback and new medical applications are some of the envisaged future advances. However, these applications need lower latency and higher reliability than today's 4G. Therefore, 5G is planned to have less than 1ms round-trip latency, which is around 20 ms for LTE-A.

Fourthly, it is envisaged that almost every physical objects will be connected to the network. This phenomenon named Internet of Things (IoT). It is expected that hundreds of devices will serve every person. However, practical implementation of IoT may require machine to machine (M2M) communications, which is different than today's traditional person to person communication. Hence, some fundamental changes required in cellular networks to make this massive connectivity implementable, which is another challenging target of 5G.

Fifthly, energy efficiency is another concern in the 5G roadmap. Increasing number of base stations and massively connected devices in 5G require more energy efficient technologies to create more 'Green' World. Moreover, more efficient handsets are inevitable to provide 5G comfort to users because ultra-fast communication result in hot devices with very low battery lifetime, which contradicts with freedom of mobility of 5G. Moreover, IoT requires also more efficient devices to make battery lifetime years, not days. Therefore, energy-efficient devices with long life batteries are another target to experience 5G comfort.

As a result, 5G promise us to satisfy needs of society at least for next decade and it has very challenging targets for this purpose. In this work, vector modulator is designed for 5G base band applications, with the hope of creating better future and society.

1.1 What is Vector Modulator (VM)?

Vector Modulator is an RF device which is used to adjust both amplitude and phase of RF signal. That is, it combines functions of both phase shifter and attenuator.

Operation of vector modulators is based on vector-sum principle. It is possible to use two or more vectors. As an example, the vector-sum principle with two (I-Q) vectors is illustrated in Figure 1.4.

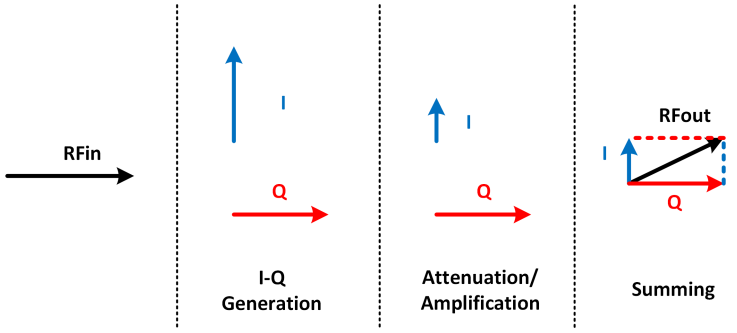

Figure 1.4: Vector Modulation concept by using I-Q Vectors

First, signal splits into 90-degree separated two vectors. Then, these vectors are amplified or attenuated. Finally, vectors are summed to obtain the output signal with the desired phase and amplitude. To realize these steps, quadrature power splitter, amplifier/attenuator, and power combiner are used.

1.2 Some General Applications of Vector Modulator

Vector Modulator is an RF signal control component with the capability of both amplitude and phase control. Therefore, it has many uses in RF systems. Some of the uses are cancellation of unwanted jamming signals, cancellation of crosstalk between co-located communication systems, complex weights for phased array antennas, and quadrature amplitude modulation [15].

Firstly, millimeter wave (mm-Wave), which is above the 30 GHz, will be used in 5G beside the current sub-6 GHz bands. The reason behind mm-Wave establishment is that sub-6 GHz spectrum is quite crowded and insufficient to provide higher bandwidth. However, at higher frequencies, propagation attenuation and directivity increases. Therefore, it is not possible to provide widespread coverage with traditional network topology at these frequencies. Therefore, **new small cell networks and beamforming** are offered to improve coverage at high frequencies, as illustrated

in Figure 1.5. Higher directive gain can be achieved by beamforming and that results in improvement in signal to interference ratio (SIR) and increase in throughput [4]. Beamforming is created by phased array antenna. In phased array systems, each antenna should be fed with appropriate amplitude and phase, as illustrated in Figure 1.6, to improve side-lobe suppression or steering nulls. Instead of attenuator and phase shifter, VM can be used with the advantages of low cost, small size, low power consumption and accurate control [20].

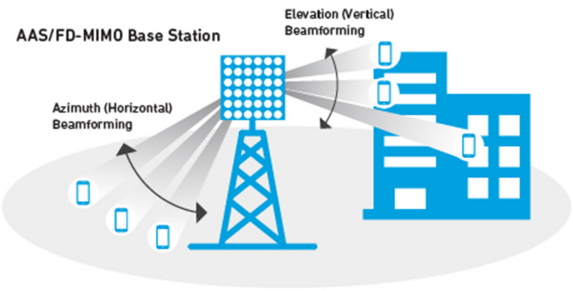

Figure 1.5: Beamforming at base station [2]

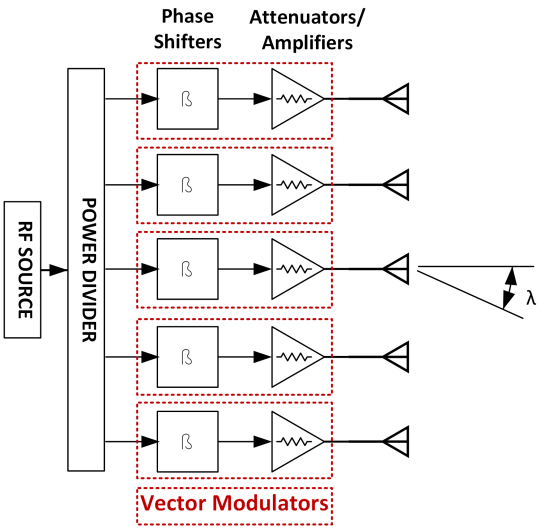

Figure 1.6: Analog Beam Forming Topology

Beamforming techniques can be analog, digital or hybrid. As in Figure 1.7, analog beamforming controls the phase of each signal by utilizing low-cost phase shifters, which is the advantage of that technique.

On the other hand, as in Figure 1.8, digital beamforming provides unique advantages

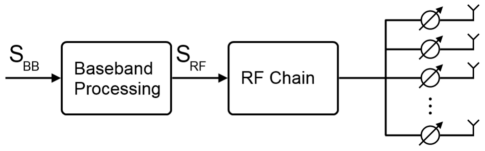

Figure 1.7: Analog Beamforming

such as the direction of arrival estimation, flexible control of antenna radiation patterns, and adaptive beam and nulls steering to improve the SIR at the expense of dedicated RF chain for each antenna array element (which is increasing the cost and complexity) [4].

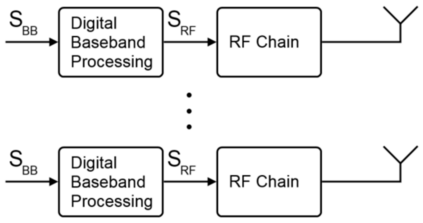

Figure 1.8: Digital Beamforming

To balance the performance and cost/complexity, hybrid beamforming technique is developed by mixing analog and digital beamforming, as in Figure 1.9. Most of the researches for 5G focus on hybrid beamforming to achieve better performance with low cost.

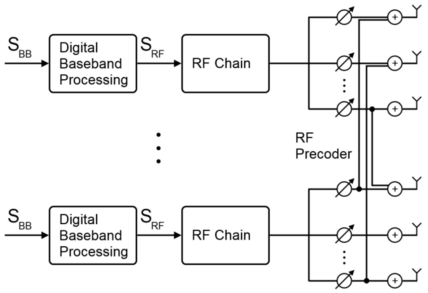

Figure 1.9: Hybrid Beamforming

Beside, beamforming techniques can also be classified as either switched-beamforming or adaptive-beamforming, according to beam capability. Switched networks consist

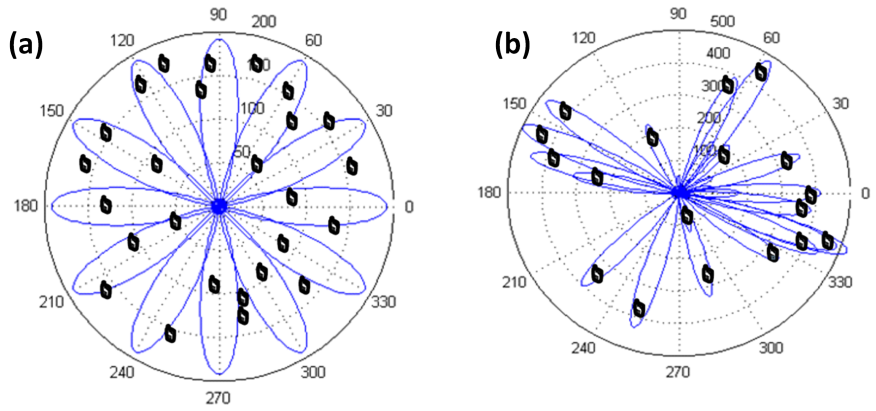

Figure 1.10: Switched (a) and Adaptive (b) Beamforming Techniques

of passive couplers and phase shifters. It is inexpensive and easy to realize in the existing cellular system. However, it suffers from interference because predefined beams may include undesired users, as in Figure 1.10-a. On the other hand, adaptive beamforming utilizes more precise phase and amplitude control components, resulting in expensive implementation, and it requires complex algorithms for operation. Adaptive beamforming show better performance of interference rejection and better coverage at the same power level, as in Figure 1.10-b. The majority of recent studies related to beamforming and massive MIMO focus on adaptive beamforming due to its optimum performance promoting 5G [4].

In massive MIMO systems, there are hundreds of antennas. Hence, beamforming in massive MIMO utilizes the huge number of RF amplitude/phase control component. It is quite important to use high linearity, low cost, low size, and efficient RF components for overall system performance. Moreover, the control algorithm of adaptive beamforming in massive MIMO systems is quite complex. To reduce the processing time and cost, the load of RF components should be minimized.

Therefore, for the beamforming applications, it is quite important to control amplitude/phase precisely with easy control, which is aimed in this VM design.

Secondly, beamforming provides electronically scanning for radar and imaging applications [33]. With the help of beamforming, it is possible to focus on the intended region with reliable electronic control. For example, advanced driver assistance systems (ADAS) make use of beamforming to detect different distance and side of the

vehicle, as illustrated in Figure 1.11.

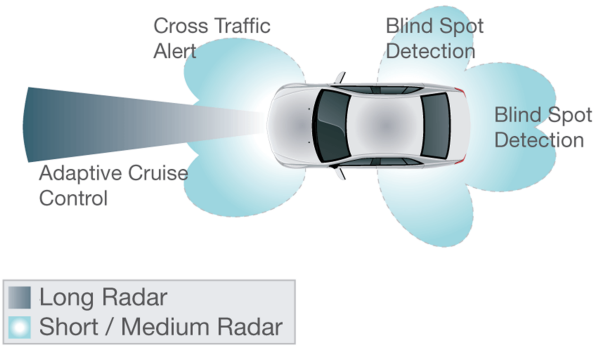

Figure 1.11: Common use of beamforming in commercial ADAS systems [3]

Besides the beamforming phase array systems, **direct carrier modulation** is another possible application of VM. That is, many modulation schemes such as BPSK, QPSK, QAM can be implemented without the need of up-converting mixer and associated filters, as shown in Figure 1.12. Therefore, it results in a more compact transceiver with less cost and complexity [32][15][14]. For example, [29] demonstrates a direct carrier transmitter with 60 Mb/s data rate and operating at 110 GHz with 64 QAM.

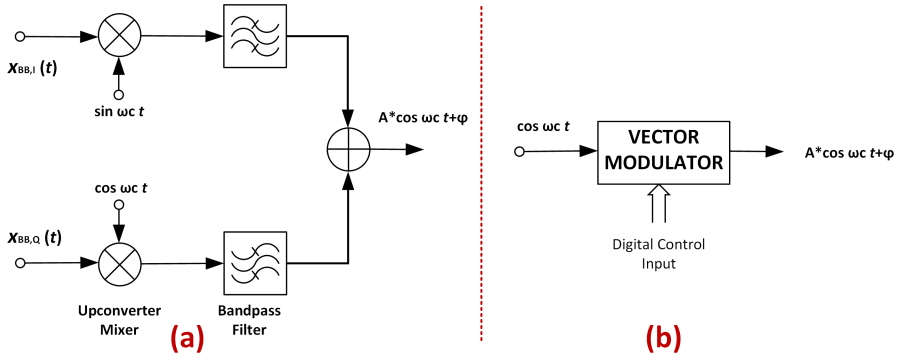

Figure 1.12: Block diagram of (a) Modulation with up-converting mixer and filters, (b) Direct carrier modulation

Moreover, vector modulator can be utilized as **RF cancellers** in transceivers which have a capability of simultaneous transmit and receive (**STAR**), or In-Band Full-Duplex (IBFD) [27]. STAR capability provide doubling spectral efficiency by reusing the same frequency for transmission and receiving. Due to this advantage, 5G wireless systems are envisioned to have STAR capability.

Today, there are 7 off-the-shelf vector modulators offered by Analog Devices [6][7] [8][9][10][11][12]. In the future, with increasing applications of communication devices and radars, the need for high-performance RF components will also increase.

1.3 Previous Studies/Alternatives

As mentioned in the previous section, VM consists of several sub-blocks, which are mainly responsible for vectors generation, amplitude modification and output combining. There are various alternatives of these sub-blocks. For example, vectors can be generated with poly-phase filters, passive quadrature couplers or active circuits. Moreover, amplitude modification can be realized with either analog push-pull attenuators, digital step attenuators or variable gain amplifiers. Similarly, output power combining can be realized with passive or active combiners. Therefore, many different VM designs were presented in the literature, by using various alternatives of these sub-blocks.

As in discussed detailed in [5], there are various VM topologies such as Digital Vector Modulator [31], Impedance Transformer Technique, Analog Phase Shifter and Gain Circuit [16], Vector Modulator Using Differential Amplifiers[42], Shifted-Quadrant Microwave Vector Modulator[28], I-Q Vector Modulator[18], Analog Monolithic Vector Modulator[46], and Three Vectors Summation VM[23].

All these designs have either digital or analog control. Depending on the control type, output coverage of VM changes. While analog controlled VM designs provide continuous amplitude in a certain range or continuous phase shift of 360-degree [19], digital controlled VM can only give discrete amplitude/phases. However, control complexity increases in the analog controlled VM at the expense of full coverage.

As expected, recent researches are focused especially on RFIC or MMIC VM due to their compactness, compatibility of mass production and reliability. For comparison, some recent VM designs are discussed below. All presented designs are implemented in IC except for the first one. Designs are presented and evaluated briefly.

In one of the recent work, [27], a vector modulator is designed to be used as RF can-

cellers in simultaneous transmit and receive (STAR) systems. This VM is designed to operate in 1.5-6 GHz and prototyped on PCB. First, I and Q are generated by 90-degree hybrid. Then, I-Q are made differential by 180-degree hybrids. With the help of switches, either positive or negative components of I-Q channels are selected, to make four quadrants possible. Then, amplitudes of selected I-Q components are adjusted by voltage-variable attenuators. Lastly, I and Q components are recombined to obtain the desired output. In this design, passive combiner and divider are used instead of active counterparts in order to achieve very low intermodulation distortion, which is essential for STAR applications. Although area and insertion loss of the design are poor, this design is simple and enough for verifying VM performance in STAR applications.

In another recent design of VM, [33], a novel quadrature coupler used to generate I-Q signals. Then, balanced I-Q signals are generated by balun to drive differential 4-bit variable gain amplifiers (VGAs). By setting amplification coefficients of the differential VGAs positive or negative, the signal phase can be shifted to the desired quadrant. By output balun, the single-ended output generated. The 4-bit control provides 16 equally separated output phases. Operating frequency of this work is 80-96 GHz. Despite the advantages of low power consumption, NF (12 dB) and area (core area: 0.54 x 0.12 mm2); this design has low phase resolution of 22.5-degree with no amplitude resolution. That is, it can be used only as digital phase shifter with 22.5-degree resolution. Moreover, its linearity is not good (-6 dB IP_{1dB}).

Besides, in the fully integrated design of [20], firstly, a balanced signal is generated by active differential pair unbal (unbalanced to balanced). Then, the signal split into two branches and amplified by programmable gain amplifiers (PGAs). Then, I-Q are generated and combined with second-order polyphase RC filter. However, due to the high loss of RC filter, an additional interstage amplifier is needed to boost the RF signal. Then, the single-ended output generated by the balun. Operating frequency of this work is 2.9-3.1 GHz. One of the drawbacks of this design is poor linearity (-42 dBm IP_{1dB}) due to multistage active circuits. Moreover, its power consumption is high and bandwidth is narrow mainly due to polyphase RC filter (which is used as quadrature summing network). Besides, it has 2.7 dB noise figure of and 40 dB gain. Its size is moderate with the dimesnsion of 1.43mm x 0.95mm.

Moreover, in the [47], vector modulator operating in W-band is designed in 45 nm CMOS SOI and utilized to control the phase of each antenna in the eight elements 370-440 GHz phased-array transmitter. In this work, VM is composed of hybrid-coupler to generate I-Q signals and 3-bit voltage gain amplifier (VGA) to weight them. It shifts W-band signal in a single quadrant only, that is 0-90. Because quadrupler, which is used to generate 370-440 GHz signal from the W-band signal, expands the 0-90 phase shift to 0-360 degree. Therefore, VM can be implemented as a single-ended topology without the need of some additional lossy blocks to achieve 0-360 phase shift such as cross-switches in differential designs or 0-180 phase shifter. Although this VM has low resolution and no information about linearity and NF, it shows the concept of VM use in tera-hertz phased array applications.

In another work, [39], VM is designed in 45 nm SOI CMOS for 5G wireless systems. Differential I-Q components are generated by the polyphase filter.Polyphase filter is implemented as a single stage instead of multistage to reduce losses at the expense of bandwidth. However, by changing the capacitance values by adjusting the bias of the MOS capacitor, its corner frequency can be controlled between 12.5-15.7 GHz. After polyphase filter, cross-connected MOS switches and voltage controlled current source (VCCS) are utilized. MOS switches make 0/180 degree phase shift and VCCS makes vector weighting and addition. While the VM has a compact design (0.18 mm2) and good resolution (1.5 degrees at optimum amplitude levels), it has high power consumption (75 mW). There is no information in the paper about NF and linearity of the VM. In [41], the same VM is used as a phase shifter after each antenna for the implementation of four elements phased array receiver supporting two MIMO channels. Moreover, in [38] and [40], the same VM is used as a phase shifter for the implementation of four channel phased array transmitter and receiver. These works show VM design and its 5G application within completeness.

Besides, there are 6 off-the-shelf vector modulators offered by Analog Devices, [10] [11] [9] [8] [12] [6].These products have IP_{1dB} lower than 21 dB and operate up to 2.7 GHz. Another product of Analog Devices, [7], is a vector modulator based 4-channel beamforming core chip for phased arrays operating in 8-16 GHz. This VM design consists of an I-Q generator, VGA for each branch and combiner.

To conclude, in the literature and market, there are various VM designs, which are designed as standalone or within the SoC.

1.4 Research Objectives and Thesis Organization

In this work, it is aimed to design differential vector modulator with **high linearity and power handling** for the base station application. It is aimed to be IIP3 better than 50 dBm and P_{1dB} better than 35 dBm. **Moreover**, in order to reduce control load of phased arrays or MIMO systems by reducing the control complexity, it is designed as digital controllable. **Besides**, it is aimed to have amplitude and phase resolutions of 0.5 dB and 1°, respectively, to make it suitable for base station applications such as code-division-multiple-access (CDMA), which is requiring precise amplitude control. Operation frequency is targeted at 20-25 GHz, which may be possible 5G band or, at least, enough for proof of concept for mm-wave applications. **Furthermore**, differential topology is chosen so that make the designed VM **easily adaptable to differential transceivers**. Advantages and disadvantages of balanced topology are discussed in detail in the following chapter.

The 2^{nd} chapter describes the theory and design of the vector modulator. After the overview and mathematical analysis of vector modulator, the layout is presented. Then theory, design, and performances of sub-blocks are examined in detail.

In the 3^{rd} chapter, simulation results of complete VM are presented. Noise figure, linearity, insertion and return losses, phase and amplitude resolutions and ranges are presented in detail.

The 4^{th} chapter concludes all work and suggests some possible future works.

CHAPTER 2

THEORY AND DESIGN OF VECTOR MODULATOR

In this chapter, a detailed analysis of the VM is presented. Overview of VM, its mathematical analysis, advantages of differential topology and overall layout are presented.

2.1 Overview of VM

VM is used to control the phase and the amplitude of the RF signal. In this work, VM is designed to meet objectives stated in the previous chapter, which are high linearity, simple control, precise amplitude and phase resolution, operation at 20-25 GHz band, and differential topology. In order to achieve **high linearity**, passive components are selected instead of active counterparts. Besides, to avoid complex control, digital step attenuators are utilized instead of analog attenuators. Sub-blocks' design details are presented in detail in following chapters. **Furthermore**, it is designed to be fabricated in 0.18 um SOI process to benefit advantages of SOI devices such as higher drive currents, less junction capacitance, reduced short channel effects, better sub-threshold slope and intrinsic immunity to radiation-induced latch-up effects [13].

VM designed in this thesis is composed of quadrature Lange coupler, baluns, digital step attenuator (DSA), 2x2 switch matrix, and Wilkinson in-phase combiner. Operation of VM can be illustrated as in Figure 2.1 and can be explained as follows:

1. I-Q are generated with the Lange Coupler at the input.
2. Differential I-Q obtained by spiral type Marchand balun.
3. Amplitudes of I-Q are adjusted by differential 4-bits digital step attenuator.

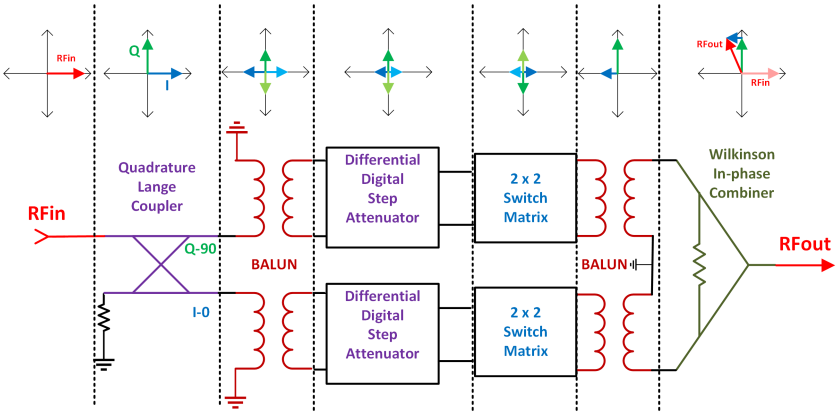

Figure 2.1: Vector Modulator topology

4. I or Q may be shifted 180-degrees by 2x2 switch matrix to obtain outputs at the other quadrants. For example, as in Figure 2.1, in order to obtain output in the second quadrant, Q channel is shifted 180 degrees. 2x2 matrix performs this 180-degree phase shift by changing differential line order.

5. Differential I-Q are converted to single-ended I-Q by the balun.

6. Single-ended I-Q are combined by Wilkinson in-phase combiner before output.

Differential topology is used in VM design to take the following advantages.

- First of all, wirebonds of IC packages have significant inductance at the input/output pins, especially at high frequencies[13]. Thanks to differential topology, effects of inductances introduced by ground pins are minimized by eliminating the need of ideal ground inside the circuit. That is, in differential circuits, there is no return signal through the ground; what travels in one line comes back on the other line of balanced lines.

- Rejection of parasitic coupling that may result from neighbor components. This coupling is dominant especially in high levels of integration and high frequencies. Because the disturbances are in common mode, they rejected substantially by differential circuits [22].

- Reduced total harmonic distortion and increase in IIP2 because symmetric circuits do not generate even-order distortion [37].

- Electromagnetic radiation, which may cause unwanted interference, is much less in differential topologies [22].

In addition to these common advantages, differential topology has another specific advantage for VM application. By crossing the balanced line, a 180-degree phase shift can be obtained by the small 2x2 switch matrix.

Besides these advantages of differential components over single-ended (SE), there are some disadvantages such as higher noise figure, larger size and higher power dissipation due to a doubled number of components.

The VM is implemented as differential to take the mentioned advantages and also make it compatible with the differential transceiver.

2.2 Mathematical Analysis of VM

Operation of VM is based on **vector sum method**. Detailed **mathematical analysis of ideal VM** is as follows:

Let input, RF_{in} is

$$RF_{in} = cos(\omega.t) \tag{2.1}$$

I-Q, generated by Lange coupler, are expressed by 2.2 and 2.3, respectively.

$$I = \frac{1}{\sqrt{2}}.cos(\omega.t) \tag{2.2}$$

$$Q = \frac{1}{\sqrt{2}}.cos(\omega.t + \frac{\pi}{2}) \tag{2.3}$$

By DSA, I and Q are attenuated X and Y dB, respectively. These attenuated signals are expressed as 2.4 and 2.5.

$$I_{X_{dB}attenuated} = \frac{1}{\sqrt{2}}.10^{\frac{X}{20}}.cos(\omega.t) \tag{2.4}$$

$$Q_{Y_{dB}attenuated} = \frac{1}{\sqrt{2}}.10^{\frac{Y}{20}}.cos(\omega.t + \frac{\pi}{2}) \tag{2.5}$$

Finally, attenuated I and Q are combined to obtain RF_{out}, that can be expressed as 2.6.

$$RF_{out} = C.cos(\omega.t + \alpha) \tag{2.6}$$

C and α are the amplitude and phase of RF_{out}, which are expressed by 2.7 and 2.8.

$$C = \sqrt{\frac{1}{2}.((10^{\frac{X}{20}})^2 + (10^{\frac{Y}{20}})^2)} \tag{2.7}$$

$$\alpha = \arctan(10^{\frac{Y-X}{20}}) \tag{2.8}$$

The goal of the VM is to adjust amplitude, C, and phase shift, α, with certain resolution and range. Range and resolution are defined by application requirements. According to these requirements, sub-blocks of VM are designed.

Attenuation level can be expressed in dB by 2.9. As expected, attenuation depends on both X and Y.

$$Attenuation\ in\ dB = 20 * \log(\frac{1}{C}) = -10 * \log(\frac{10^{\frac{X}{10}} + 10^{\frac{Y}{10}}}{2}) \tag{2.9}$$

Equation 2.8 shows that phase shift, α, depends on only relative attenuation, |Y-X|. Table 2.1 shows the phase shift for different relative attenuations. As expected, when X=Y, α became 45 degrees. When relative attenuation, |Y-X|, gets larger, α deviates from 45 degree. However, after relative attenuation of 16 dB, phase shift starts to saturate and changes slowly. Therefore; vicinity of 0, 90, 180 and 270 degrees are blind regions of VM. That is, it is difficult to obtain an output at these regions with different amplitudes. It requires high attenuation level, which makes the DSA design hard. In this thesis, DSAs are designed to have the maximum attenuation of 7.5 dB. Because; larger than 7,5 dB attenuation requires more complicated DSA design. Although 7.5 dB provides limited phase range, it is enough to see concept and results.

Table2.1: Relative attenuation and phase shift relation

|Y-X|	|α-45|	|Y-X|	|α-45|	|Y-X|	|α-45|
0	0	**7**	20.9	**14**	33.7
1	3.3	**8**	23.3	**15**	34.9
2	6.5	**9**	25.5	**16**	36.0
3	9.7	**10**	27.5	**17**	37.0
4	12.7	**11**	29.3	**18**	37.8
5	15.6	**12**	30.9	**19**	38.6
6	18.4	**13**	32.4	**20**	39.3

2.3 The Layout of the Designed Vector Modulator and its Sub-Blocks

The Layout of the designed VM is presented in Figure 2.2. Total chip size, with pads, is 2mm x 2mm. From left to right, there are the Lange coupler, the baluns, the DSA, the baluns, and the Wilkinson combiner.

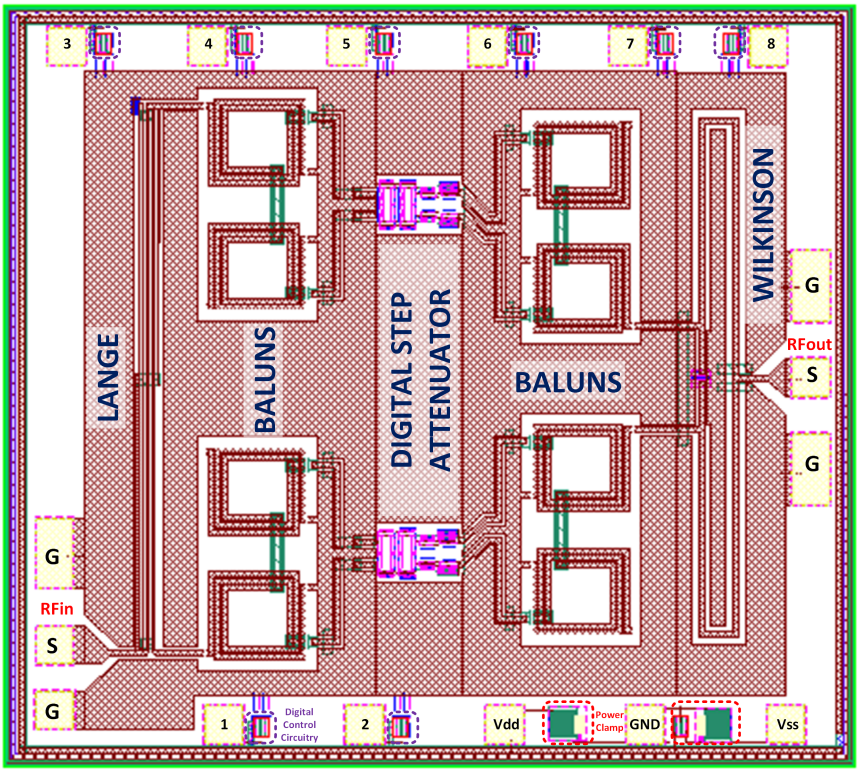

Figure 2.2: Layout of Vector Modulator

The 2x2 switch matrix is excluded from the layout to make it more compact. However, this compact version makes the evaluation of the topology on the first quadrant possible and it is sufficient to provide proof of concept.

At the top and bottom side, there are 11 DC pads corresponding to 8 digital control inputs of two DSA and 3 supply inputs, V_{dd}, V_{ss} and ground. Ground-Signal-Ground (GSG) pads for RF_{in} and RF_{out} are located at left and right, respectively.

ESD protection circuits are used at all digital inputs. Moreover, RC triggered power clamps are used for ESD protection between the V_{dd}, V_{ss}, and GND. In design kit of

the CSOI7RF process, there are useful tools to design schematic and layout of ESD protection circuits.

Near each digital inputs, digital control circuitry are utilized to generate required control voltage of digital step attenuator.

Although VM is designed as differential, passive sub-blocks of VM -balun, Lange and Wilkinson coupler- need ground. Therefore, passive sub-blocks are designed as coplanar due to lack of back-via in CSOI7RF process. All passive sub-blocks are simulated using Sonnet EM Suite. Active DSA and switch matrix are designed and simulated using Cadence.

Before the detailed explanation of sub-blocks, amplitude and phase imbalances will be defined, which are critical figures of merit of passive sub-blocks (balun, Lange and Wilkinson coupler). Ideally, outputs of combiners, dividers or baluns have equal amplitudes and desired phase differences. This desired phases are 0, 90, and 180 degrees for the in-phase combiner, the quadrature hybrid, and the balun, respectively. However, in reality, there are inevitable deviations from ideal amplitude and phase case. These deviations named by amplitude and phase imbalance and figured by (2.10) and (2.11), where port 1 represents input and port 2 and 3 represent outputs.

$$AmplitudeImbalance = 20 \times \log(S_{31}/S_{21}) \tag{2.10}$$

$$PhaseImbalance = \angle S_{31} - \angle S_{21} - DesiredPhase \tag{2.11}$$

As stated in [21], typical values for amplitude and phase balances are $\pm 10^{\circ}$ and $\pm$1dB, respectively, for commercial discrete baluns. Moreover, for Marki power dividers and quadrature hybrid couplers, amplitude imbalance is typically less than 0.25 dB and 0.4 dB,respectively. Also, phase imbalance is less than several degree for Marki couplers [30]. In this work, amplitude and phase imbalances of all blocks are minimized to reduce control complexity of VM and SNR degeneration. The passive parts of this work have less than 0.2 dB and 2°, amplitude and phase imbalances, respectively.

2.3.1 Quadrature Lange Coupler

In Vector Modulator(VM), the signal is first divided into in phase-quadrature (I-Q) component by quadrature coupler. I-Q signals mean 90-degree out of phase with equal amplitude signals. There are several quadrature coupler types such as branch-line, coupled line, and Lange couplers. These can be implemented lumped or distributed. Size of distributed couplers generally depends on wavelength and so frequency. At low frequencies, lumped couplers are used due to compactness [17]. However, at high frequencies, with short wavelengths, distributed couplers may be preferable due to ease in design, large bandwidth (BW) and low loss. Lange coupler is used widely in IC due to its low insertion loss, large BW and compact size[48].

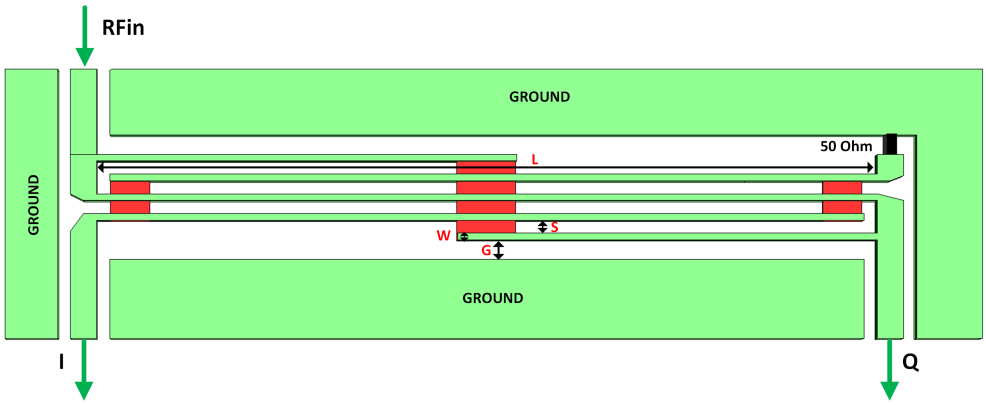

Figure 2.3: Layout of Lange Coupler

Lange coupler consists of interdigitated quarter wave coupled lines. Major design parameters of the Lange coupler are finger number, line width (W), line spacing (S), length (L) and ground spacing (G), as shown in Figure 2.3. These parameters are optimized using Sonnet EM Suite parametric sweep. After optimization, design parameters are set as Table 2.2.

Table2.2: Lange Parameters

Finger Number	4	**Line Spacing (S)**	8 um
Line Width (W)	4 um	**Length (L)**	1500 um
Ground Spacing (G)	12 um		

Lange's important figures of merit are amplitude-phase imbalance, insertion loss (IL), return loss, and isolation, which are aimed to better than 0.5dB/4°, 4 dB, 15 dB, and 15 dB, respectively.

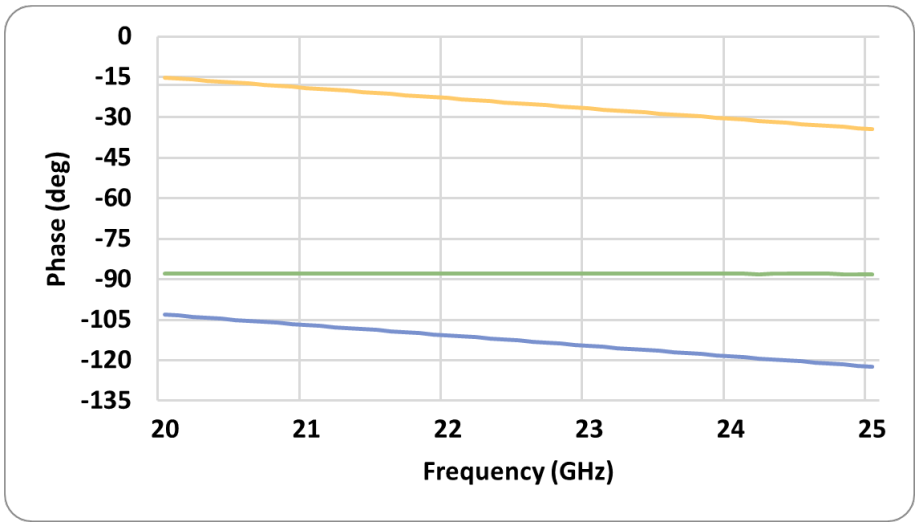

Figure 2.4: Transmission Phases of the Lange Coupler (S_{21} and S_{31}) and their difference ($\angle(S_{21}) - \angle(S_{31})$

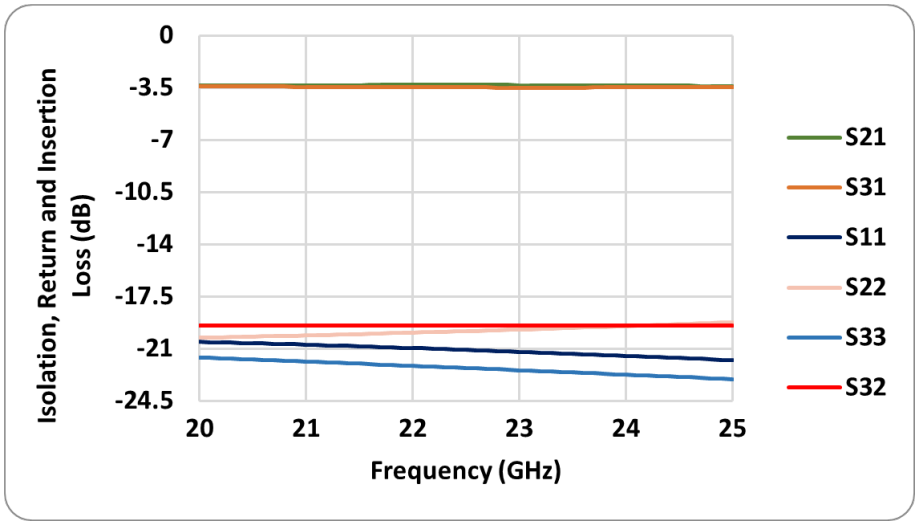

Figure 2.5: Isolation (S_{23}), Return (S_{ii}) and Insertion Losses (S_{21} and S_{31}) of the Lange Coupler

As illustrated in Figure 2.5 and 2.4, the designed Lange Coupler has;

- Amplitude imbalance less than 0.2 dB and phase imbalance less than 2 degree,
- IL (S_{21} and S_{31}) less than 3.6 dB,

- Isolation (S_{32}) better than 19 dB,
- Return Loss (S_{11}, S_{22} and S_{33}) better than 19 dB,
  in the operation bandwidth of 20-25 GHz, which are obtained by Sonnet.

2.3.2 BALUN

Balun (balanced-unbalanced) is a device that converts single-ended (SE) signal to differential signal, or vice versa (Generally, it is bi-directional). Balun is used widely in RF systems to combine SE and differential components (such as LNA, mixer, antenna etc.). It can be also used as impedance matching components.

In this VM design, baluns are used to connect the combiner/divider to the differential sub-blocks, which are digital step attenuator and switch matrix.

For on-chip IC application, there are many balun types such as transformers, distributed (LC) baluns, transmission line baluns, and active baluns [22].

Transformers are most commonly used type due to its compact size. However, in the frequency range of the VM, 20-25 GHz, due to coupling capacitances between primary and secondary windings of transformer, insertion loss is very high [21]. Therefore, spiral Marchand balun is used instead of transformer type. In spite of larger size than the transformer, it has good amplitude and phase balance and small insertion loss in operating frequency.

As shown in Figure 2.6, spiral Marchand balun consists of two quarter-wave coupled lines [49]. Major design parameters of the spiral Marchand balun are number of turns of spirals, the line width (W), the line spacing (S), the ground spacing (G) and the spiral size (L). Space between two spirals is not critical. These parameters affect not only return and insertion loss but also phase and amplitude imbalances. These parameters are optimized with Sonnet EM Suite parametric sweep. Optimized values are presented in Table 2.3.

Balun's important figures of merit are amplitude-phase imbalance, insertion loss (IL), return loss, and isolation, which are aimed to better than 0.5dB/4°, 4 dB, and 15 dB, respectively.

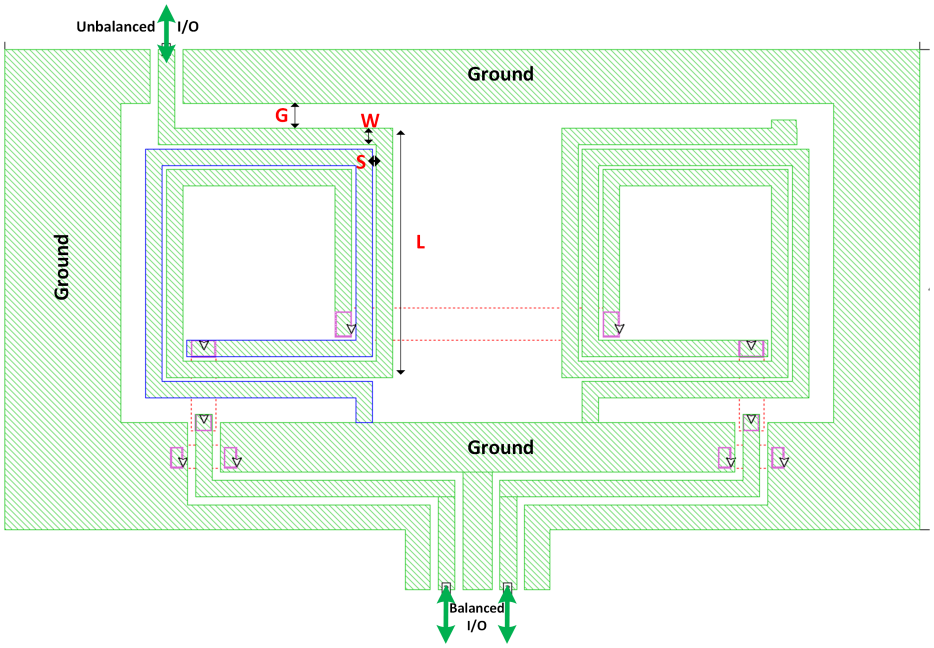

Figure 2.6: Spiral Marchand Balun Layout

Table2.3: Balun Parameters

Turn Number Of Spirals	1.5	**Line Spacing(S)**	4 um
Line Width (W)	16 um	**Spiral Size(L)**	240 um
Ground Spacing(G)	24 um		

As illustrated in Figure 2.8, the designed BALUN has;

- Amplitude imbalance less than 0.1 dB,
- Phase imbalance less than 1.5 degree,
- IL (S_{21} and S_{31}) better than 4 dB,
- Return Loss (S_{11}) better than 12 dB,
  in the operation bandwidth of 20-25 GHz, which are obtained by Sonnet EM Suite.

In addition, another Balun performance specification is common mode rejection ratio (CMRR). It is the ratio of the differential to common mode gain. That is, it defined by vectorial addition of two inputs. Therefore, CMRR depends on phase and

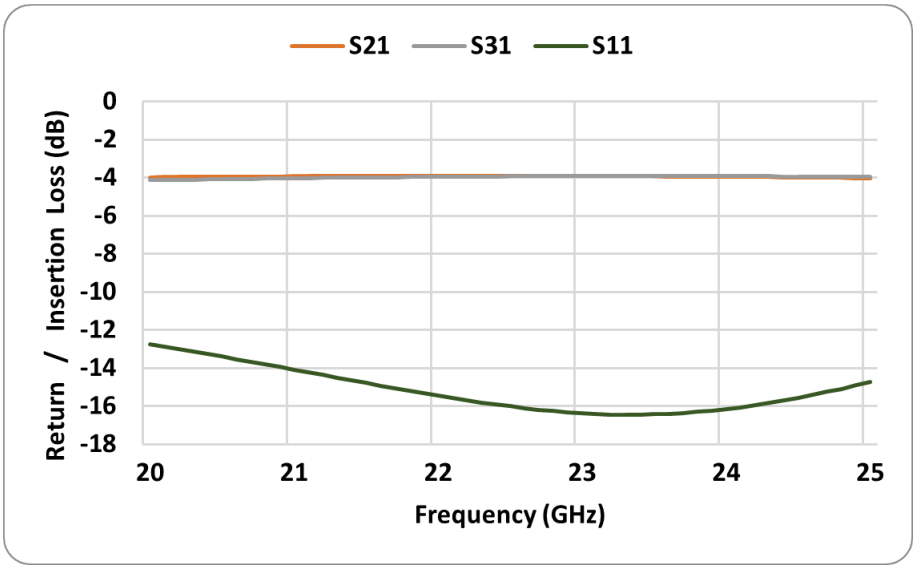

Figure 2.7: Return (S_{11}) and Insertion Losses (S_{21} and S_{31}) of the Balun

amplitude imbalance. The relationship between CMRR, amplitude and phase balance is illustrated in Figure 2.9. As a rule of thumb, a 0.1 dB improvement in amplitude balance improves the CMRR by the same amount as a 1° improvement in phase balance. CMRR of the designed BALUN is better than 30 dB, which can be classified as high-performance balun [25].

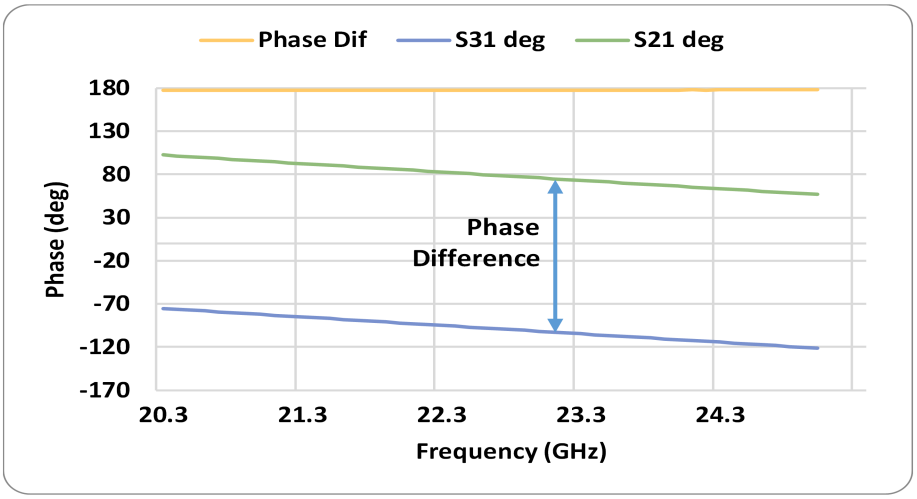

Figure 2.8: Transmission Phases of the Balun ($\angle(S_{21})$ and $\angle(S_{31})$) and their difference($\angle(S_{21}) - \angle(S_{31})$

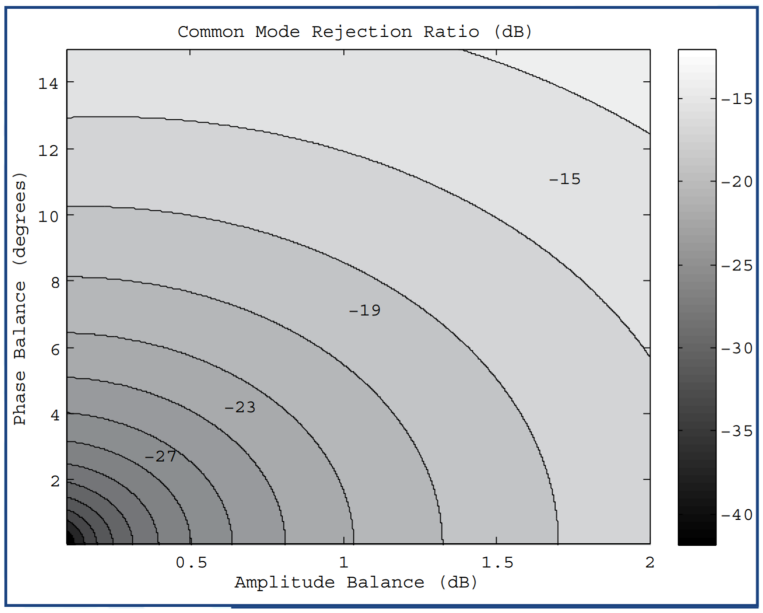

Figure 2.9: CMRR as a function of amplitude and phase imbalance[25]

It should be noted that phase difference of balanced outputs is almost constant and 180 degree in the operating frequency. However; the phases of S_{21} and S_{31} changes with frequency, which makes control of whole VM frequency dependent. This situation can be observed in Figure 2.8. In other words; required VM's inputs for certain desired output phase depend on input frequency.

2.3.3 Digital Step Attenuator (DSA)

As stated in chapter 1.5 (Research Objectives), VM is aimed to have 0.5 dB amplitude and 1° phase resolutions to be compatible with certain base station applications such as code-division-multiple-access (CDMA). Also, digital control is preferred for VM to reduce control complexity. Therefore, digital step attenuator with 0.5 dB LSB is designed to adjust the amplitude of I and Q signal.

Depending on their control types, attenuator can be divided into two categories: Analog and Digital. Analog attenuators are controlled by analog voltage and attenuation levels can be continuous. On the other hand, Digital attenuators are controlled by digital inputs and attenuation levels are discrete. In this study, digital step attenuator (DSA) is used due to its followings advantages over analog ones:

1. **Control of DSA is easier.** Because; while analog attenuators have nonlinear voltage-attenuation characteristics, DSA only requires binary digital control inputs

2. **Generally, DSAs have better linearity.** The reason is that analog attenuators use transistors as the varying resistors and these transistors introduce large distortion characteristic [13].

In literature, there are different DSA designs such as distributed attenuators using p-i-n diodes, switched path attenuators, switched Pi/T attenuators.

In this design, switched T attenuators are used due to its compact size, good matching and CMOS compatibility.

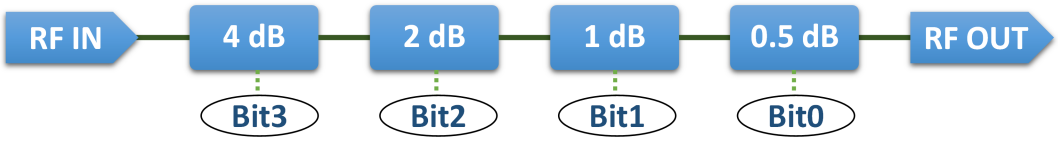

Figure 2.10: Symbolic 4 Bits Digital Step Attenuator

DSA consists of switchable attenuation blocks having different attenuation levels. 4 bits provide 2^4 different attenuation states. Figure 2.10 shows 4 bits DSA symbolically. Each attenuation block consists of resistive bridged T networks and switching elements. By binary control bit (BitX), blocks can be set either reference (ideally 0 dB) or attenuation state (0.5, 1, 2 or 4 dB). Reference and attenuation states are shown in Figure 2.11. Ideally, in the reference state, all signal pass through series switch with no insertion loss. In attenuation state, the series switch is open and signal pass through the resistive network, resulting in the desired attenuation.

However, in real life, there are undesired parasitics. Parasitics are mainly due to shunt capacitance of components ($C_{parasitic}$), off-state capacitances (C_{OFF}) and on-state resistances (R_{ON}) of switches. These parasitics are shown in Figure 2.12 with blue color.

As expected, these parasitics cause some non-idealities in attenuation and phase characteristics. **Firstly,** the reference state's insertion loss is not 0 dB as in ideal case. It

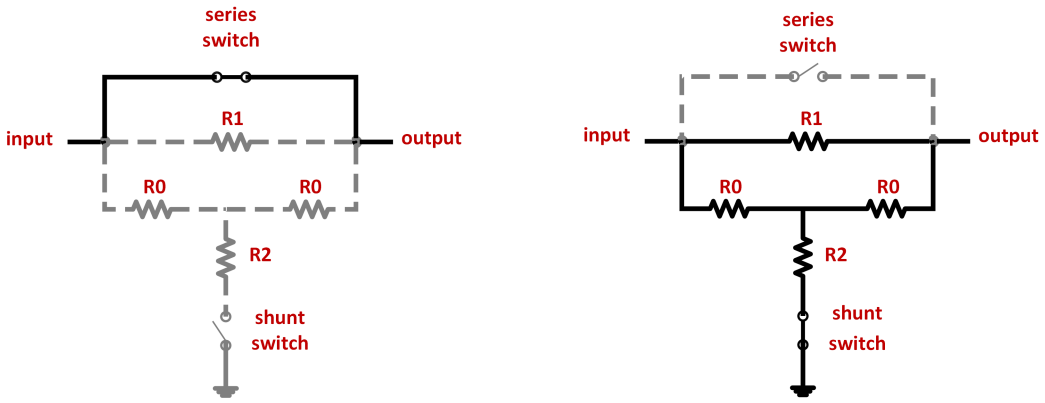

Figure 2.11: Reference and Attenuation States of One Block

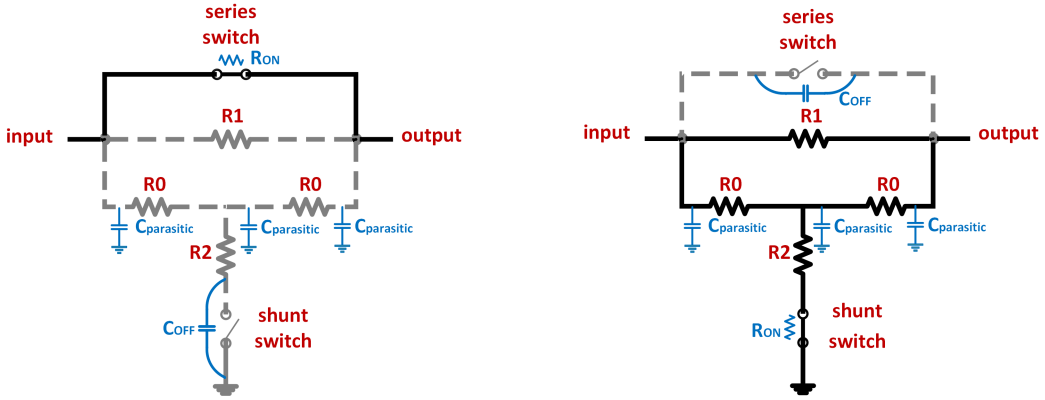

Figure 2.12: Reference and Attenuation States of One Block with Parasitics

has some losses, which results from mentioned parasitics. **Secondly,** frequency roll-off characteristics in attenuation can be seen. That is, attenuation of block changes with frequency. **Thirdly,** different phase characteristics of attenuation and reference states are another non-ideality. That is, transmission phases of ON and OFF states are different. This can be defined quantitatively by equation 2.12

$$Phase\ Difference\ of\ ON\ and\ OFF\ state = \angle(S_{21})_{ref.\ state} - \angle(S_{21})_{att.\ state} \tag{2.12}$$

These non-idealities complicate the overall control of VM. As mentioned; for simple control of VM, it is important to conserve 90-degree phase difference between I-Q channels. However, the different phase characteristics result in phase imbalance of I-Q channels.

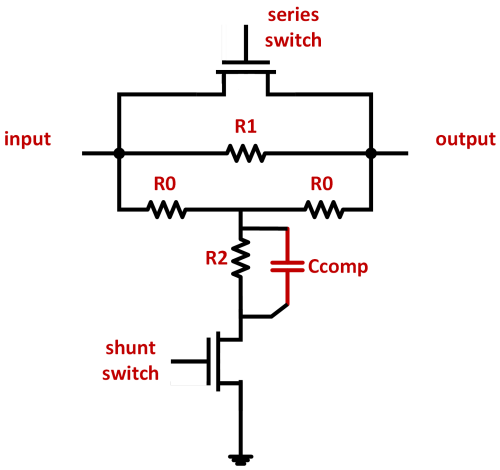

Figure 2.13: Compensated Block

Detailed analyses about possible causes of phase shift and compensation techniques are explained well in [13]. One way to compensate the last two non-idealities is adding parallel capacitor, C_{comp}, with R_2, as shown in Figure 2.13. C_{comp} is the simple and sufficient solution for the DSA which have no wire bonds and no large attenuation bits. Wire bonds and large bits' large parasitics make the compensation difficult. Whether the bit is 'large' or not depends on operation frequency and power capacity of DSA. To handle high power, transistors and resistors should be larger and parasitics also get larger. Similarly, at higher frequencies, parasitics also become dominant. For this design, larger than 4 dB bits create a problem and requires complicated compensation.

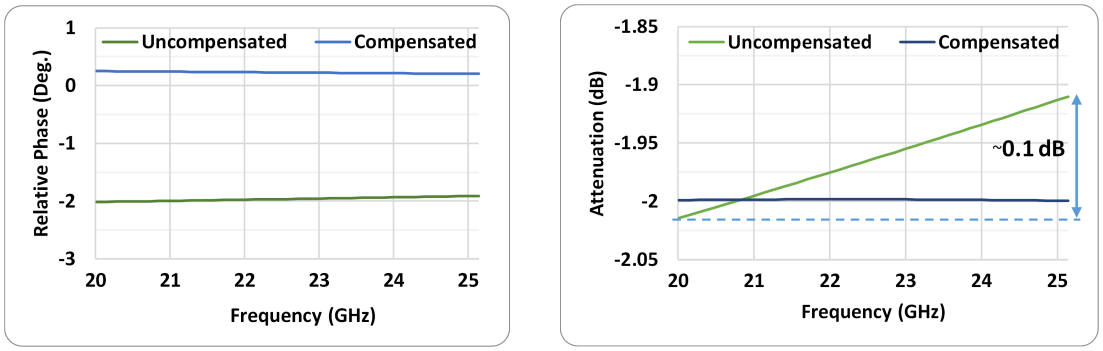

Figure 2.14: Relative Phase ($\angle(S_{21})_{ref.\ state} - \angle(S_{21})_{att.\ state}$) and Attenuation ($S_{21}$) of 2-dB Block with and without compensation

To see compensation effect clearly, 2 dB bit's attenuation and relative phase are shown in Figure 2.14. Blue lines represent the compensated results while greens are uncompensated. **Without compensation,** attenuation deviates 0.1 dB in operation frequency range and phase difference between the ON-OFF state is about -2 degrees. These figures may seem to be negligible. However, complete DSA consisting 4 bits result in serious deviation. **After compensation**, attenuation becomes linear and phase difference gets close to zero.

2.3.3.1 Design Parameters

- **The Number of Bits and Resolution:** DSA requirements are defined according to VM specifications. By the help of system simulation of the whole VM, the requirements of the DSA can be described. Then, the number of bits and resolution can be calculated. As stated, in this work, VM with 0.5 dB amplitude and 1° phase resolution is aimed. To provide this specifications, DSA is design to have **0.5 dB** resolution. Also, for the proof of concept, 4 bits DSA is utilized, which provide **7,5 dB** maximum attenuation.

- **Resistances:** Values of resistances can be calculated easily by 2.13 and 2.14. A is the desired attenuation in dB, Z_0 is the system characteristic impedance, 50 Ω for most RF design.

$$R_1 = \frac{Z_0}{(10^{\frac{A}{20}} - 1)} \tag{2.13}$$

$$R_2 = Z_0 \times (10^{\frac{A}{20}} - 1) \tag{2.14}$$

  In addition, physical dimensions of resistances are important to avoid resistor overheating. Required minimum width calculated using equations provided by the factory. The maximum current passing through resistance, which is used in width calculation, is obtained by transient simulation in Cadence Spectre. Maximum current passing through resistances of bits are presented in Table

- **The Number of Switching Transistor to be Stacked:** Transistors of selected technology withstand maximum 2.5 V_{rms} between its source-drain terminals. Therefore, the maximum voltage swing of each series and shunt switches are calculated by transient analyses. For example, in attenuation state, the series

Table2.4: Maximum current of DSA resistances

	R1		R2		R3	
	Current-mA	Widht-um	Current-mA	Width-um	Current-mA	Width-um
0.5 dB	38.5	44	2.7	3	2.9	2
1 dB	37	47	4.9	6.2	5.2	4.6
2 dB	33.3	46.5	8.7	11.9	9.5	10.5
4 dB	27.3	40.5	14	10.5	17	23.5

switch of Bit-4dB has 0.82 V_{rms} voltage swing, which can be calculated by equation 2.15, where X is attenuation value, P_{max} is maximum input power, Z_0 and p_0 are reference impedance and power, 50 Ω and 1 mW, respectively. It should be noted that the number of transistors depends on maximum input power, P_{max}, and attenuation value, X.

$$Voltage\ Drop\ of\ Series\ Switch = \sqrt{10^{\frac{P_{max}}{10}} \times Z_0 \times p_0} - \sqrt{10^{\frac{P_{max}-X}{10}} \times Z_0 \times p_0} \tag{2.15}$$

Therefore 1 transistor is enough, no stacking is required in the series switch. Similarly, all shunt switches are exposed to maximum 2.23 V_{rms} voltage swing when 20 dBm, the maximum input power, is applied at the reference state, where all shunt switches are OFF. Therefore only 1 transistor is also enough for all shunt switches. In Figure 2.15, Bit-4dB is illustrated to show switches and their transient voltage drop.

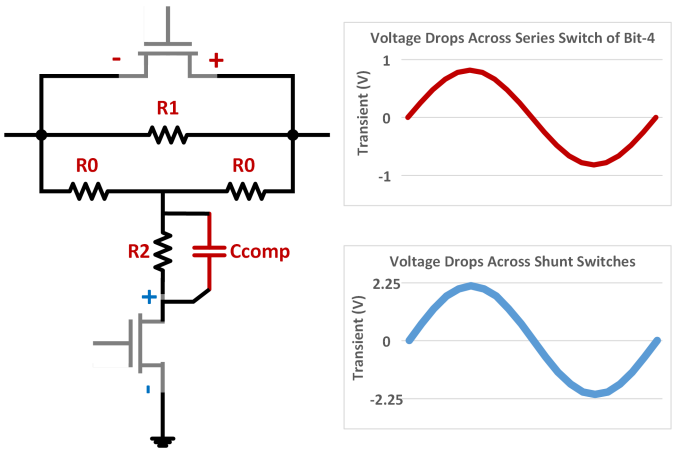

Figure 2.15: Transient voltage drops across switches of Bit-4dB

- **Switching Transistor Width:** Switching transistor width affects some design

specifications such as P_{1dB} and maximum allowable input power. For this DSA, 1 dB compression point is targeted at 30 dBm and input power is limited at 20 dBm. Therefore, width is optimized to handle input power and achieve required P_{1dB}. It should be noted that larger transistor has larger parasitics, which make compensation hard. Hence, the width should be large enough, not too much.

- C_{comp}**:** Compensation capacitances are in the order of tens pF. Exact capacitance values can be obtained easily with tuning. During optimization of C_{comp}, R_2 and R_1 also should be optimized iteratively in order to keep attenuation at the desired value.

2.3.3.2 Figures of Merit

- **Linearity:** It is the important measure showing the circuit's ability to handle large signals. Desensitization and intermodulation are undesired results of nonlinearity. P_{1dB} and IIP3 are common parameters describing the tolerances to desensitization and intermodulation, respectively. In this DSA design, IIP3 and P1dB are better than 50 dBm and 40 dBm. These results are obtained by Harmonic Balance simulation performed with Cadence.

- **Resolution:** Resolution is the possible minimum attenuation step, which is equal to attenuation value of the least significant bit, which is 0.5 dB in this design.

- **Attenuation Range:** Maximum attenuation depends on both bit numbers and resolution by equation 2.16. The DSA design has **7.5 dB** maximum attenuation.

$$Maximum\ Attenuation = Resolution \times (2^{\#\ of\ bits} - 1) \tag{2.16}$$

- **Insertion Loss(IL):** IL of DSA is the undesired attenuation of reference state due to $R_{ON}s$, ON resistances of series switches, and leakage through shunt paths. This DSA design has better than 0.9 dB IL.

  The resolution, attenuation range, and IL are presented in Figure 2.16.

- **Attenuation Error:** Step and state errors are important measures showing attenuation accuracy. Step error is defined as the difference between resolution

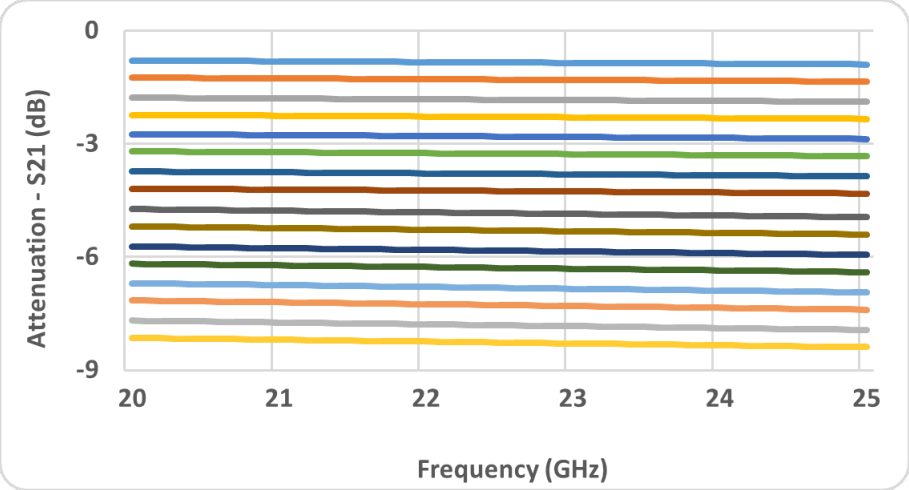

Figure 2.16: All Attenuation States of DSA

and phase difference of consecutive states. Step error is less than 0.15 dB as shown in Figure 2.17 for all attenuation states.

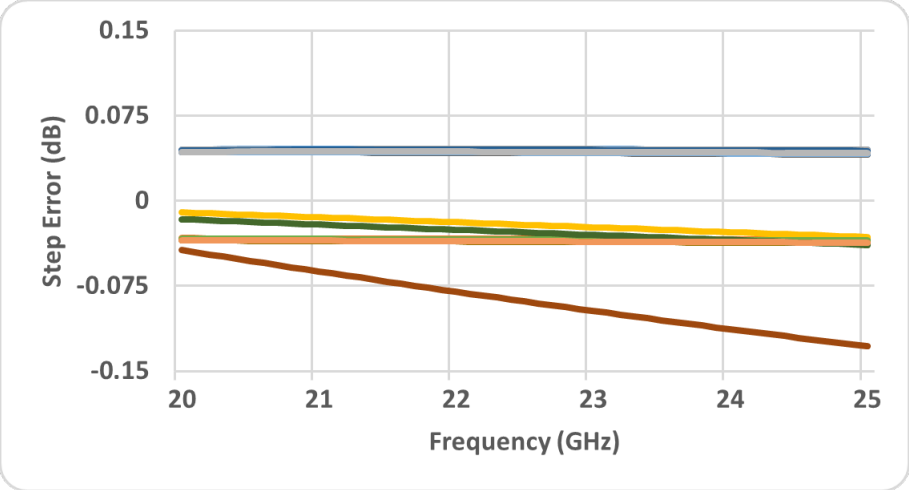

Figure 2.17: Step Error of DSA

State error is the deviation from the desired attenuation. That is, state error is cumulative of the step error. Figure 2.18 shows the state errors for all attenuation states, which are less than 0.15 dB.

- **Phase coherency:** As mentioned, in RF systems, in order to control amplitude and phase of the signal independently, phase characteristics of different attenuation states should be close as possible. As shown in Figure 2.19, transmission

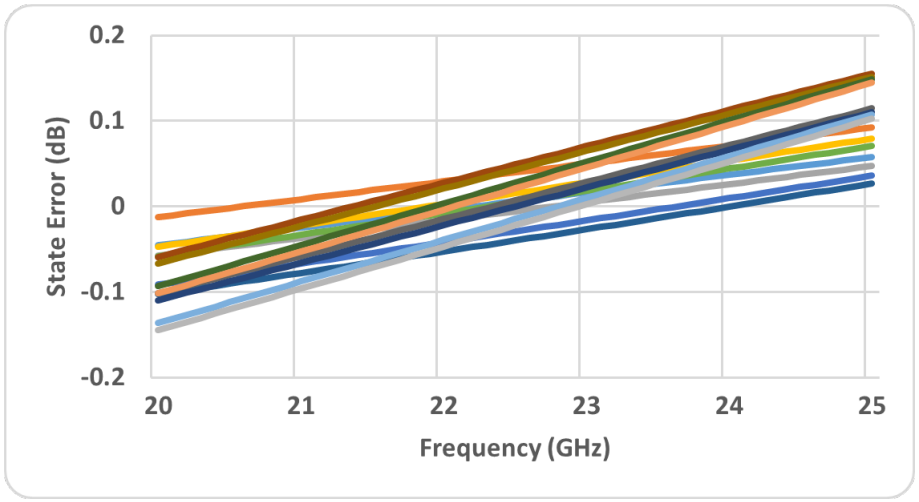

Figure 2.18: State Error of DSA

phase variations are less than 1°.

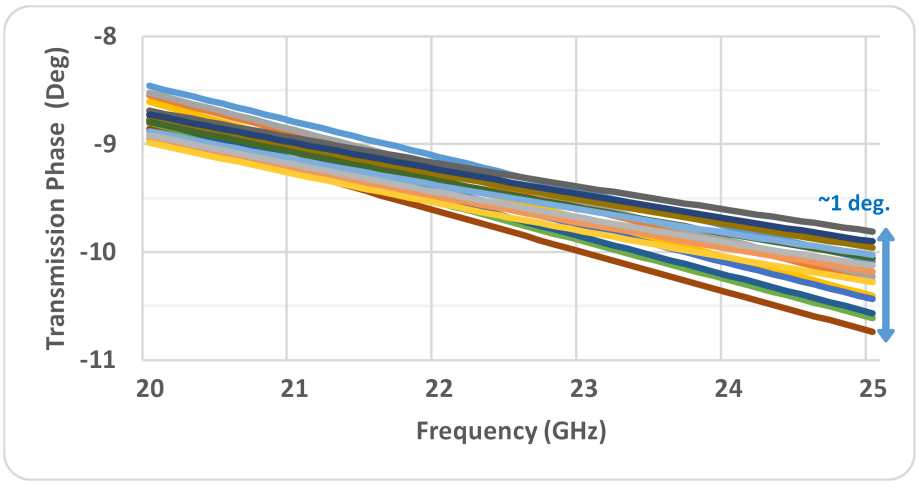

Figure 2.19: $\angle S_{21}$ of all attenuation states

- **Return Loss:** S_{11} and S_{22} are shown in Figure 2.20. Return loss is better than 12 dB for all attenuation states.

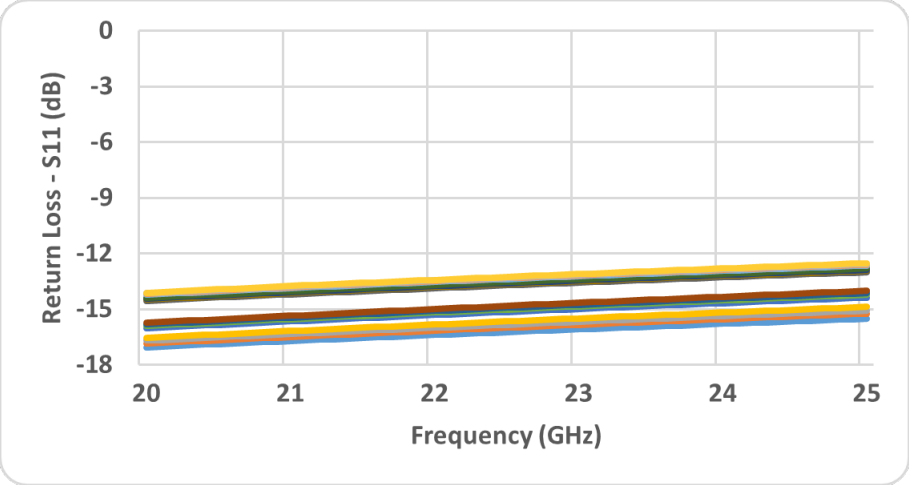

Figure 2.20: Return Losses of DSA

2.3.4 2x2 Switch Matrix

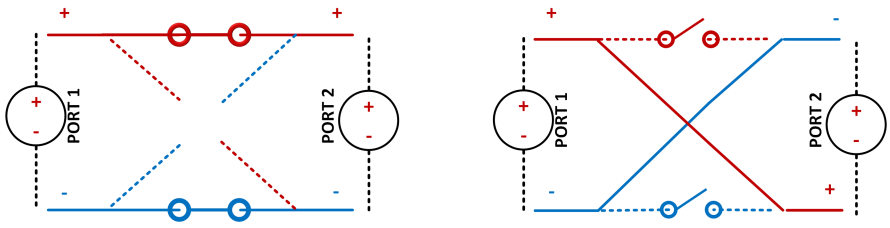

Figure 2.21: 180-degree phase shifting by crossing differential lines

The 180-degree phase shift is required to be able to get output at any quadrant. For this purpose, 2x2 switch matrix is designed. Differential signal can be shifted 180 degrees by crossing the complementary lines, which is illustrated in Figure 2.21.

Switch matrix consists of series-shunt switches, as in Figure 2.22. Size and number of these series-shunt switches are critical design parameters. Making series switch larger provides better insertion loss at ON state (Because R_{ON} decreases). However, large series switch results in bad isolation in OFF state (Because, C_{OFF} increases). It induces some leakage between complementary lines, increasing insertion loss. Moreover, increasing number of series switch results in better isolation (It is similar to connecting capacitor C_{OFF}'s in series). However, it also increases insertion loss (It similar to connecting resistance R_{ON}s in series). Besides, small shunt switch is preferable

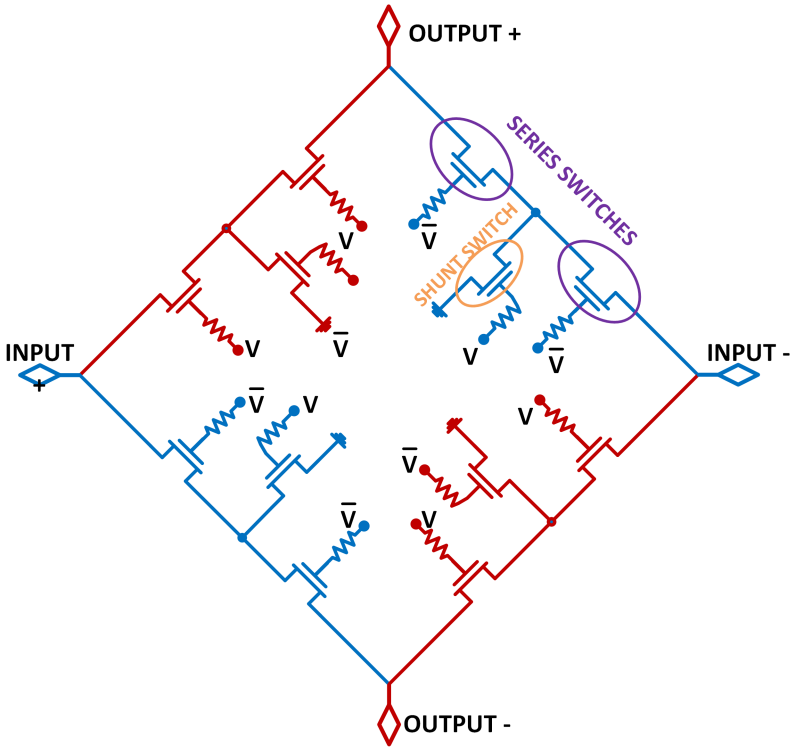

Figure 2.22: Switch Matrix

due to its good isolation in OFF state, preventing power leakage to ground.

Size and number of series-shunt switches are optimized with Cadence Spectre to get optimum insertion loss and matching. After optimization, size and numbers are set as in Table 2.5.

Table2.5: Switch Parameters

Number of Series Switches	1	**Number of Shunt Switches**	1
Width of Series Switches	240 um	**Width of Shunt Switches**	1 um

Switch matrix is simulated by Cadence Spectre with differential input and output. (That is, PORT1 is connected to balanced input and PORT2 is connected to balanced output, which are shown in 2.21). As shown in Figure2.23(a-b), return and insertion losses are better than 20 dB and 0.46 dB, respectively. As shown in Figure 2.23(d), the difference of transmission phases between two states is 180 degrees.

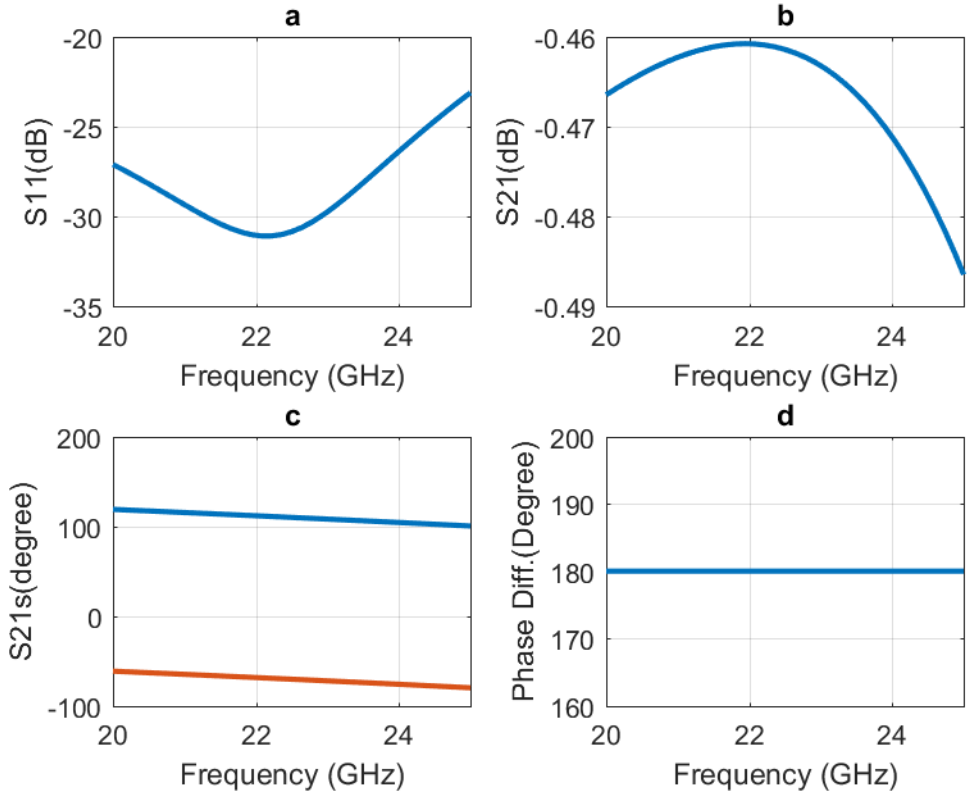

Figure 2.23: (a)Return Loss, (b)Insertion Loss, (c)Transmission Phase of both state, and (d)Phase difference of states **of switch matrix**

2.3.5 In-Phase Wilkinson Combiner

As a last operation of VM, I and Q are combined. This combining should be in-phase. In this VM design, Wilkinson combiner is utilized due to its perfect matching of input/output and perfect isolation between inputs.

Besides the Wilkinson Combiner, there are several alternatives combining techniques such as lossless T-junction or resistive combiner. However, these combiners are not matched at input/outputs or have not perfectly isolated outputs [34].

As illustrated in Figure 2.24, Wilkinson combiner consists of one $2Z_0$ Ω resistor and two quarter wavelength transmission lines with $\sqrt{2}Z_0$ characteristic impedance.

As illustrated in Figure 2.24, the quarter wavelength transmission lines are folded to get the more compact layout. Major design parameters of Wilkinson combiner are line width (W), ground spacing (G), and length (L). Approximate value of those are

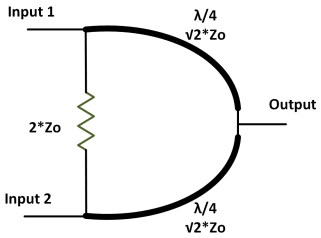

Figure 2.24: Wilkinson Combiner

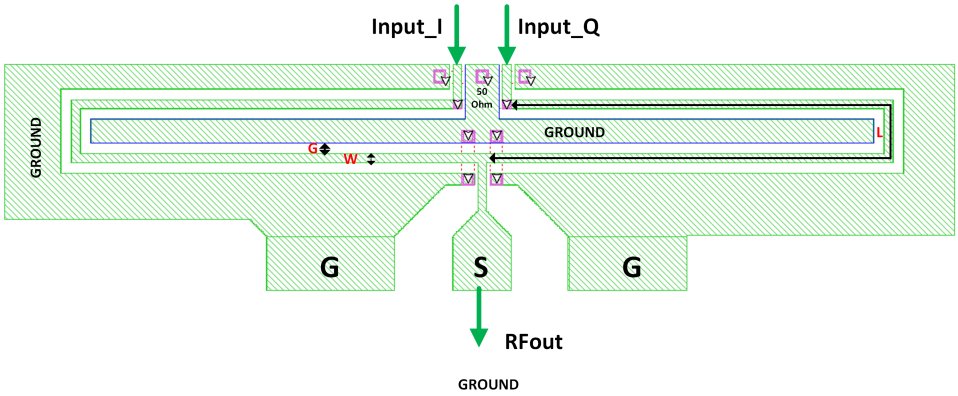

Figure 2.25: Wilkinson Layout

calculated by the help of coplanar waveguide calculator. Then, fine-tuning is done using Sonnet EM analysis program. After optimization, design parameters are set as in Table 2.6.

Table2.6: Wilkinson Parameters

Line Width (W)	15 um	**Length (L)**	1400 um
Ground Spacing(G)	18um		

Wilkinson's important figures of merit are amplitude-phase imbalance, insertion loss (IL), return loss, and isolation, which are aimed to better than 0.5dB/1°, 4 dB, and 15 dB, respectively.

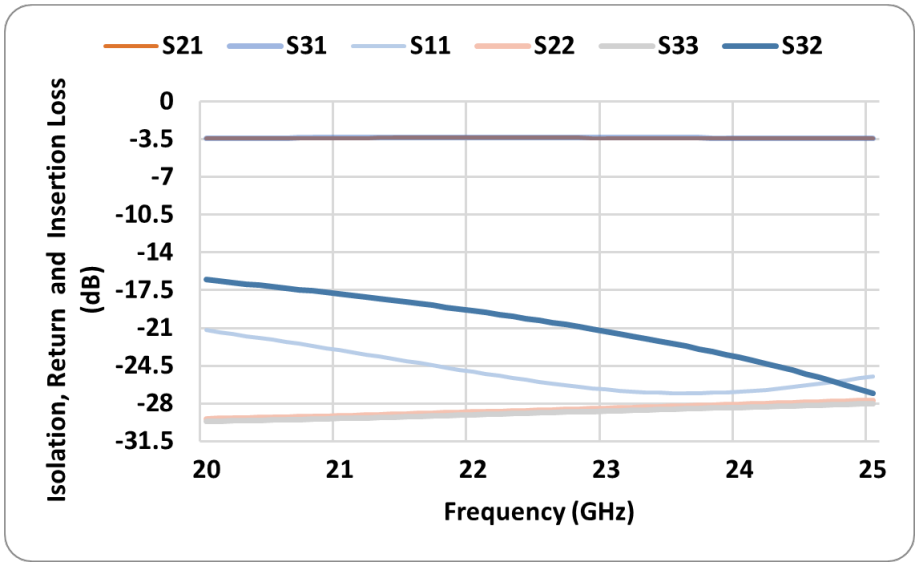

Figure 2.26: Isolation (S_{23}), Return (S_{ii}) and Insertion Losses (S_{21} and S_{31}) of the Wilkinson Combiner

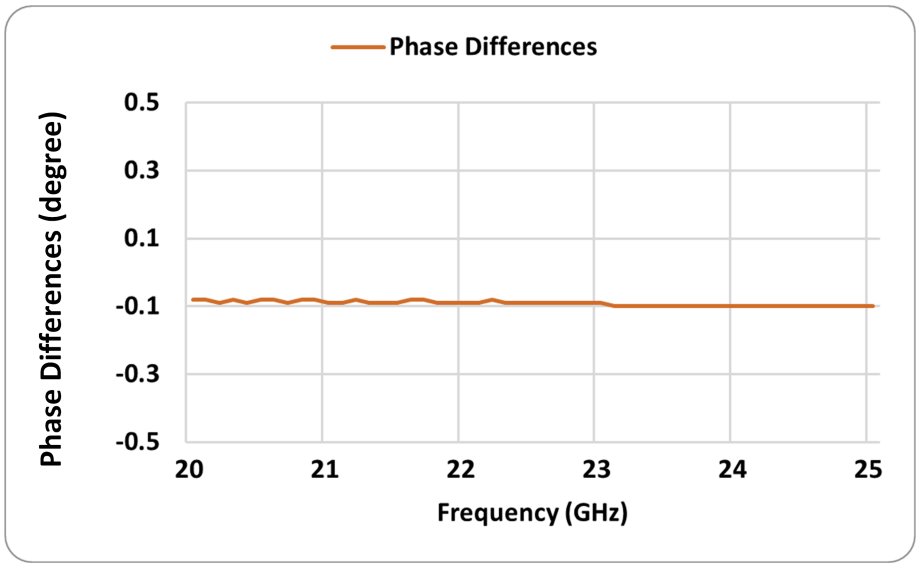

Figure 2.27: Transmission Phases difference ($\angle(S_{21}) - \angle(S_{31})$ of the Wilkinson Combiner

As illustrated in Figure 2.26 and 2.27, the designed Wilkinson Combiner has;

- Amplitude imbalance less than 0.2 dB and phase imbalance less than 0.1 degree,
- IL (S_{21} and S_{31}) less than 3.6 dB,
- Isolation (S_{23}) better than 14 dB,
- Return Loss (S_{11}, S_{22} and S_{33}) better than 20 dB,
  in the operation bandwidth of 20-25 GHz, which are obtained by Sonnet EM Suite.

CHAPTER 3

SIMULATIONS OF DESIGNED VECTOR MODULATOR

In this chapter, simulation setup and simulation results of overall VM are presented. Insertion loss (IL), return loss (RL), range and resolutions of output's amplitude and phase, noise figure (NF) and linearity (P_{1dB}, IIP_3) performances are discussed.

By showing the reason of insufficient interest to CSOI7RF process (which is the proposed process in this VM design), multi-project wafer (MPW) company cancels the tape-out, without informing early. Therefore, designed VM has not been fabricated. (It is advisable to select popular process for fabrication to be not faced with tape-out cancellation.) Therefore, measurement results of designed VM cannot be obtained.

Passive parts (baluns, Wilkinson power combiner, and quadrature coupler) are designed, optimized and simulated with Sonnet EM Suite. Optimization and simulation of passives are time-consuming and a bit tedious process. However, there are some useful tips to reduce simulation time. **Firstly**, it is useful to use divide and conquer method. For example, when a circuit is simulated without subdivision, circuit conductors are meshed into N subsections and simulation time is proportional to N^3. However, when the circuit is divided into two pieces, and mesh resolution is kept constant, simulation time becomes roughly $2 \times (\frac{N}{2})^3 = \frac{N^3}{4}$, which is four times faster than simulating without dividing. Though, simulating divided circuit results in ignorance the coupling between divided parts. That is, the interaction between divided parts takes place via only connecting ports, there is no fringing field coupling between sections. In order to minimize the effect of subdivision on the results, division axes should be chosen cautiously so that to avoid dividing the circuit at a junction where there is coupling between the divided parts. **Secondly**, to reduce simulation time, it is logical to start with big meshes (so fewer subsections) and make

coarse tuning with fast simulation. Then, make meshes small for fine-tuning. In [35], [36] and [43], these useful tips for fastening EM optimization process are discussed in detail. During the optimization of the designed VM, these tips are used effectively. For instance, each sub-block of VM is drawn and optimized **individually**. Moreover, sub-blocks are also subdivided into several parts if possible. For example, as seen in Figure 3.1, Lange coupler is subdivided into seven parts. It should be noted that parts

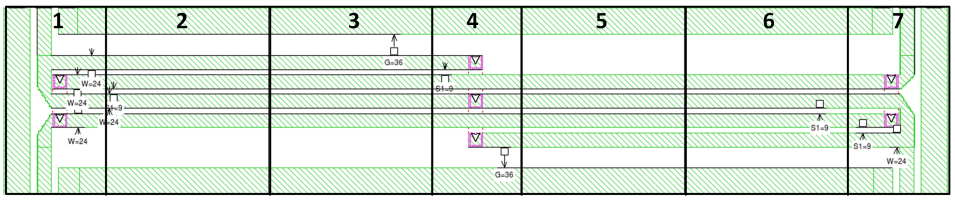

Figure 3.1: Subdivided Lange Coupler Layout

2,3,5 and 6 are identical, which results in a remarkable reduction in simulation time. After optimization of the Lange coupler, it is combined with baluns, as in Figure 3.2, and simulated again. Due to the imperfect matching and interaction between them,

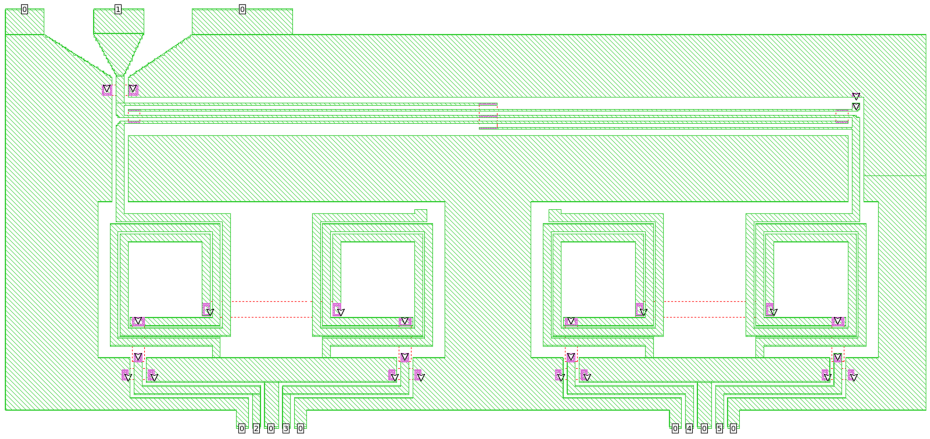

Figure 3.2: Lange Coupler and Balun Layout

additional optimization is required for combined Balun-Lange structure. In a similar way, balun and Wilkinson combiner is combined and optimized. Then, optimized Balun-Lange and Balun-Wilkinson parts are connected with ideal attenuator block in the layout, and complete structure is simulated and optimized again. After, final optimization, S-parameters of passive parts are created and exported to Cadence Environment and combined with active parts, which are DSA and switch matrix. Then,

the overall design of VM, which is illustrated as black-box in Figure 3.3, is simulated by Cadence Spectre and results are presented.

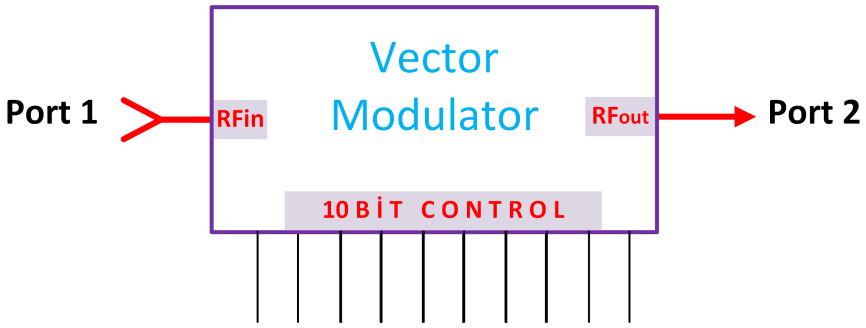

Figure 3.3: Vector Modulator as a black box

3.1 Insertion Loss

The total insertion loss of the VM in reference state, where all attenuation blocks are at their reference states, is 6.5 dB. This loss is due to mainly Lange coupler and Wilkinson combiner. These results are obtained by S-parameter analysis of Cadence Spectre Circuit Simulator.

3.2 Return Loss

Return losses of input (port 1) and output (port 2) at all 1024 states are presented in Figure 3.4(a-b). As seen, input return loss is better than 17 dB while that of output is better than 10 dB. That is, input and output ports have good matching with 50 Ω. These results are obtained by S-parameter analysis of Cadence Spectre Circuit Simulator.

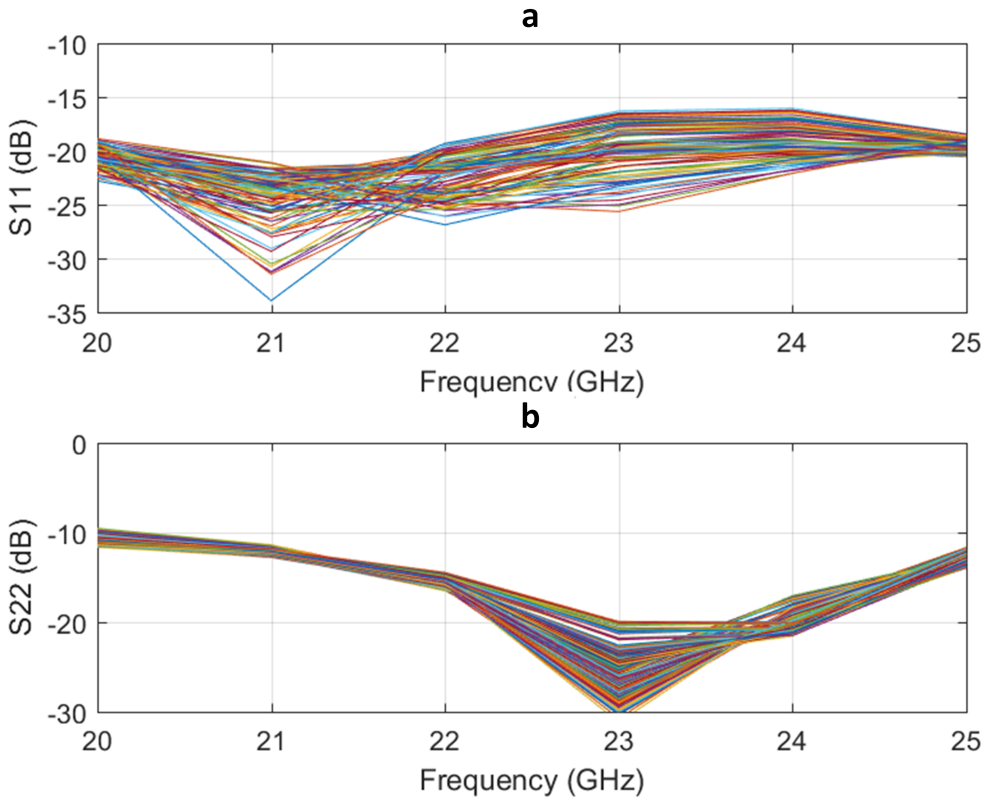

Figure 3.4: (a)Return Loss of Port 1 (S_{11}) (b)Return Loss of Port 2 (S_{22})

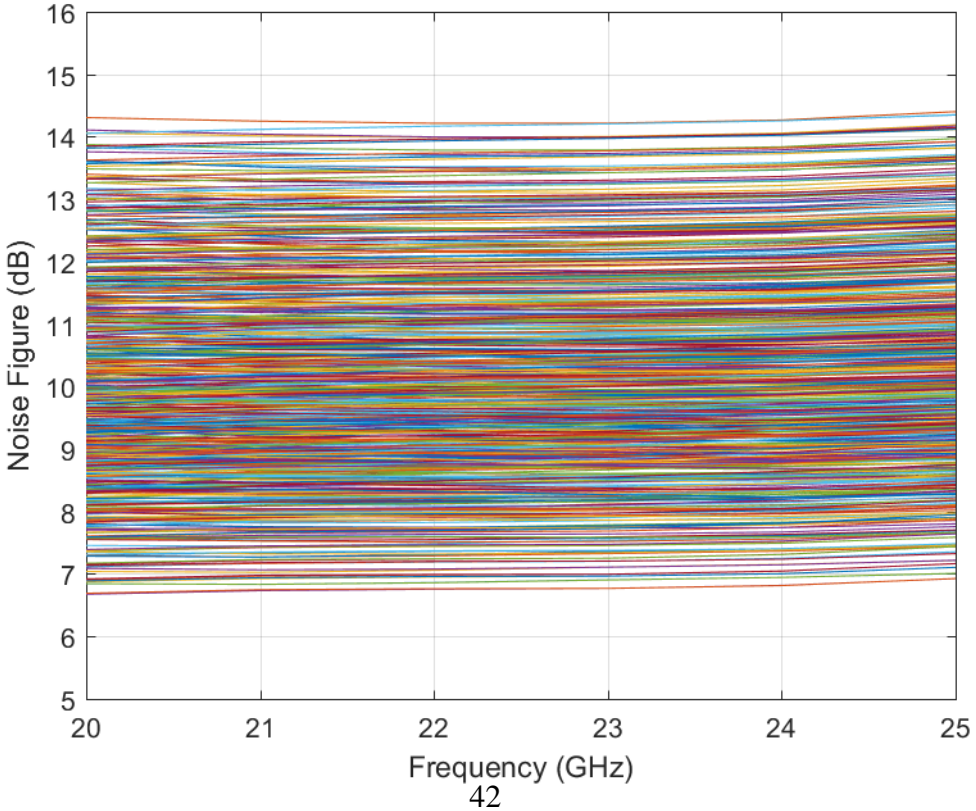

Figure 3.5: Noise Figure of Vector Modulator

3.3 Noise Figure

Noise Figures of Vector Modulator at all 1024 states are plotted in Figure 3.5. It varies between 7 and 14 dB with different attenuation states. This variation is an expected result because digital step attenuator consists of resistive attenuation network. Different attenuation states have different resistances and introduce different noises. These results are obtained by Noise analysis of Cadence Spectre Circuit Simulator.

3.4 Phase and Amplitude Range and Resolution

As explained in the second chapter in detail, phase shifting capability of the designed vector modulator is limited due to the attenuation capacity of digital step attenuators. Maximum relative attenuation of designed digital step attenuators is 8 dB, and this limits the active region, where output can take values. Outside of the active region can be named as the blind region, where output cannot take values.

Phase shift and amplitude characteristic of vector modulator can be observed clearly in polar plot of transmission coefficient, S_{21}. As shown in Figure 3.6, there are four active regions.

At the -9 dB attenuation circle (depicted as blue in Fig 3.6), there is almost 45-degree phase range in one quadrant. From 23 to 68 degrees phase shift is possible in the first quadrant. By the help of switch matrix, outputs can be shifted 90, 180 and 270 degrees to get output at other quadrants. As expected, other quadrants also have 45-degree phase range. Therefore, this VM can also be used as phase shifter with 45-degree resolution.

Phase resolution is approximately 1-degree in the active regions.

At the 45, 133, 226 and 314 degrees, amplitude range is 7.5 dB, which is also the range of digital step attenuator. It varies from insertion loss, which is -6,5 dB (at the reference state), to maximum attenuation, which is -14 dB.

Amplitude resolution is about 0.5 dB in active regions.

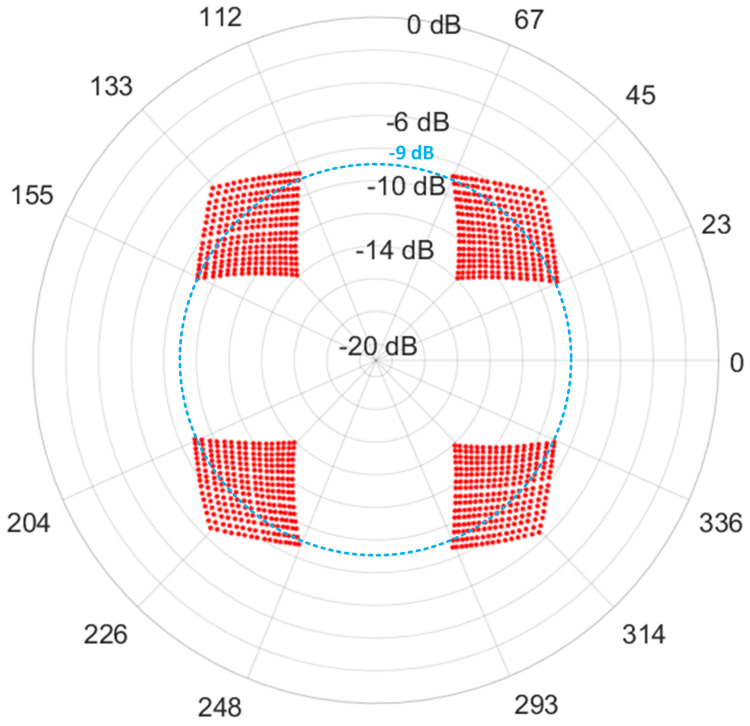

Figure 3.6: Constellation Diagram of Vector Modulator Output

The polar plot in Figure 3.6 drawn at the 23.3 GHz. This constellation is rotating with frequency due to balun characteristic. (This is explained in Chapter 2, Balun section)

These results are obtained by S-parameter analysis of Cadence Spectre Circuit Simulator.

3.5 Linearity

Input IP_3 is simulated with Harmonic Balance simulation performed by Cadence Spectre Circuit Simulator. As illustrated for six states including corners in Figure 3.7, input IP_3 of VM is better than 48 dBm in the operation band. All 1024 states lay on between 48-56 dBm.

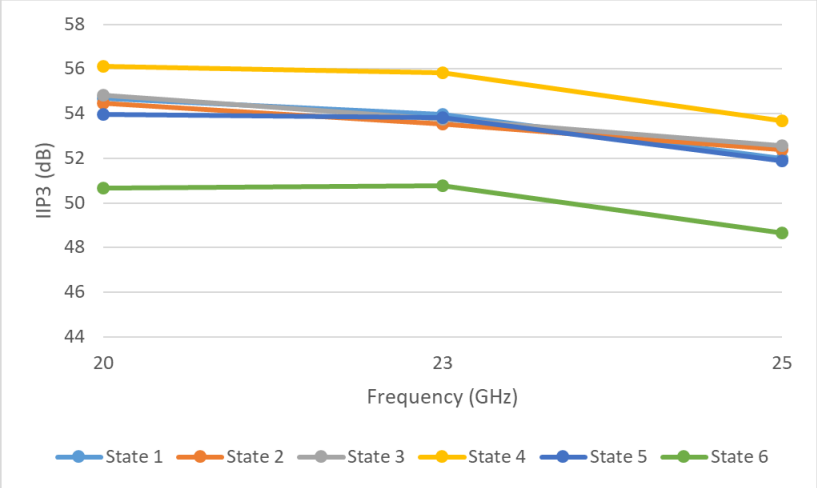

Figure 3.7: IIP3 of VM

P_{1dB} is simulated with transient analysis performed by Cadence Spectre Circuit Simulator. As illustrated for 64 different states in Figure 3.8, IP1dB is better than 38 dBm.

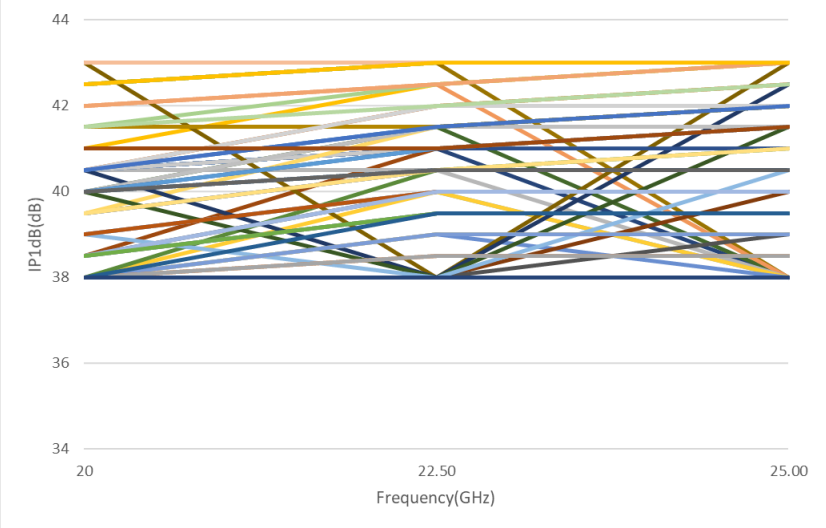

Figure 3.8: IP1dB of VM

These results show that the VM is suitable for applications requiring high linearity. This high linearity is achieved with the help of passive couplers and digital step attenuators.

3.6 Performance Summary

Table 3.1 shows the performance summary of the proposed vector modulator and some similar works. The designed VM is unique in terms of power handling and high linearity. Moreover, it has phase and amplitude control with high resolution without complex control, which is better than other works in literature. These performances make the designed VM suitable for the base station applications, within the convenience of research objectives. However; one insufficiency of this design is limited amplitude and phase ranges due to attenuator capacity.

Table3.1: Summary of Vector Modulator Performance

Parameter	**This Work**	[33]	[50]	[26]
Technology	SOI CMOS 0.18 μm	FDSOI CMOS 28 nm	CMOS 0.13 μm	CMOS 0.13 μm
Operating Freq. (GHz)	20-25	80-96	21.5-24.5	15-26
Input Return Loss (dB)	<-17	<-11.5	<-10	<-10
Output Return Loss (dB)	<-10	-	<-15	<-10
Noise Figure (dB)	6.5-14	12	6.5	-
Input P_{1dB} (dBm)	**38**	**-6**	**-25**	**-0.8**
Input IP_3 (dBm)	**48**	-	**-13**	-
Insertion Loss/Gain (dB)	-6.5	0.83	15	-4
Phase Resolution (degree)	**1**	**22.5**		**22.5**
Amplitude Resolution (dB)	**0.5**	-		-
Phase Range (degree)	23-67,112-155, 204-248,293-336	360		360
Amplitude Range (dB)	7.5	0		0
Static Power Cons. (mW)	0	21.6	40m	11.7
Number of Control Bits	10	4	4	4
Voltage Supply (V)	$\mp$2.5 V	1.2	1.5	1.5
Chip Size (including PADs) (mm X mm)	2 X 2	0.54 X 0.12	2.11 X 1.43	0.75 X 0.6
Chip Size (excluding PADs) (mm X mm)	1.7 X 1.7	-	-	0.33 X 0.6

CHAPTER 4

CONCLUSION AND FUTURE WORK

For the most of the communication systems and radars, amplitude and phase control is vital. Especially, in phased array systems, amplitude and phase control components are used in large quantities. Moreover, many modulation schemes such as BPSK, QAM can be implemented with direct carrier modulation, resulting in more compact topologies. To propose an alternative solution for these applications, the vector modulator is designed in this work. Proposed vector modulator is operating in 20-25 GHz.

Vector Modulator is used to adjust both amplitude and phase of RF signal in one circuit. That is, it combines the functions of both phase shifter and attenuator.

Operation of vector modulators is based on vector-sum principle. By adjusting amplitudes of I-Q vectors, desired attenuation and phase shift is obtained at the output.

Quadrature Lange coupler, baluns, digital step attenuator (DSA), 2x2 switch matrix, and Wilkinson in-phase combiner are used to realize balanced VM.

The proposed vector modulator is designed to be fabricated on a commercial $0.18\mu m$ SOI process. Sonnet EM Suite is used for EM simulation of Lange coupler, baluns, and Wilkinson power combiner. Cadence is used to design active DSA and switch. Finally, all parts are combined in Cadence and layout is generated.

The proposed vector modulator has high linearity with 48 dBm IIP_3. It has moderate noise figure with maximum 14 dB. Its size is $1.7x1.7mm^2$ excluding PADs. Its insertion loss is 6.5 dB. Vector modulator is controlled with 10 bits digital inputs. Also, it is unique with its topology which is composed of passive quadrature coupler, Wilkin-

son combiner, baluns, switch matrix, and DSA. These sub-blocks are chosen among alternatives to make VM having high linearity, high power handling and simple digital control.

As a summary, the proposed vector modulator is unique in the literature with its high linearity, power handling capacity and novel topology. Although this VM has not full phase shifting capacity of 360°, it is believed that this study will be enough for proof of concept of this topology and will be beneficial for the future research on Vector Modulators with high power and linearity.

Future works:

1. Insertion phase depends on frequency due to baluns and coupler characteristics. That is, for the desired phase shift at the output, different control inputs required for different frequencies. This frequency dependency of control input can be solved by either utilizing additional control block which sets the input of DSAs according to input frequency and desired output phase shift or by designing the novel baluns/couplers with flat phase characteristics.

2. In order to cover all I-Q plane, digital step attenuator with higher attenuation level can be designed. Moreover, three vectors can be utilized instead of two vectors(I-Q) to obtain more uniform constellation at the expense of more components, losses and control complexity.

3. Output at the I and Q axis can be achieved with canceling out the Q(I) branch and feeding only I(Q) branch to the output. By this way, output at I and Q axis can be achieved without the need of digital step attenuator with higher attenuation level.

4. Negative voltage generator can be designed in order to get rid of negative supply requirement.

5. This design's layout area limits the number of DC control pads. Instead of parallel control, serial peripheral interface (SPI) can be designed to have the more compact layout and serial communication capability.

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