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Comparison of Two Alternative Fabrication Processes for a Three-Axis Capacitive MEMS Accelerometer

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Abstract

This paper presents a three-axis capacitive MEMS accelerometer implemented by fabricating lateral and vertical accelerometers in a same die with two alternative processes: a double glass modified dissolved wafer (DGM-DWP) and a double glass modified silicon-on-glass (DGM-SOG) processes. The accelerometers are implemented with a 35µm structural layer, and the three-axis accelerometer die measures 12mmx7mmx1mm in each process. Each process includes a second glass wafer which, not only allows implementing a top electrode for the vertical accelerometer, but also forms an inherent cap for the entire structure. Thanks to the stress-free structural layer coming from the SOI wafer, the DGM-SOG process allows obtaining the same rest capacitance values in each side of the accelerometer, which is one of the most important challenges for a functional high performance operation.

Keywords: Three-axis capacitive MEMS accelerometer, glass-silicon-glass, SiGeB, SOI

1. Introduction

There are many accelerometer fabrication methods classified as bulk micromachining. One of these methods is the dissolved wafer process (DWP) that uses the highly doped layer as an etch-stop. However, the highly doped structural layer, which has a maximum thickness of 20µm, has high amount of stress due to the nature of the boron diffusion [1]. Even though this stress can be considerably reduced in highly doped epitaxially-grown SiGeB wafers by introducing Ge into the lattice in the modified dissolved wafer

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process (MDWP) [2-4], still it can prevent the operation of vertical accelerometers. Another alternative is to use the modified silicon-on-glass process (M-SOG) which allows implementing the structural layer from single crystal silicon, which is a stress free material [5]. A glass-silicon-glass sandwich accelerometer concept consisting of only a vertical accelerometer fabricated with bulk micromachining is already reported in the literature [6-8]. However, this paper reports, for the first time, a three-axis capacitive accelerometer, which comprises of individual lateral and vertical accelerometers in the same die, fabricated by using two alternative processes with sandwich structures, to assess their feasibility.

2. Fabrication

The proposed fabrication processes, which use the same mask set, are based on the glass-silicon-glass sandwich structure concept. Figure 1 shows the fabrication steps of the proposed processes. Each process begins with formation of the bottom electrode for the vertical accelerometer, anchor points, and pad metallization on a glass substrate. After the growing and patterning of a thin insulator layer on either the SOI wafer (Fig. 1a (ii)) or the highly doped SiGeB wafer (Fig. 1b (ii)), the device layer is patterned by using DRIE. Then, the silicon wafers are anodically bonded to the bottom glasses on each process. The DGM-DWP continues with thinning of handle layer by grinder and rest of the handle layer is etched by ethylenediamine pyrocatechol (EDP) until the highly doped region (Fig. 1a (v)). On the other hand, the removal of the handle layer and buried oxide layer of the SOI is performed by DRIE and BHF in the DGM-SOG, respectively (Fig. 1b (v)). Finally, each process is completed after the anodic bonding of the top glass. Figure 2 shows an SEM image of glass-silicon-glass interface and fabricated a three-axis capacitive MEMS accelerometer in the wafer and die level.

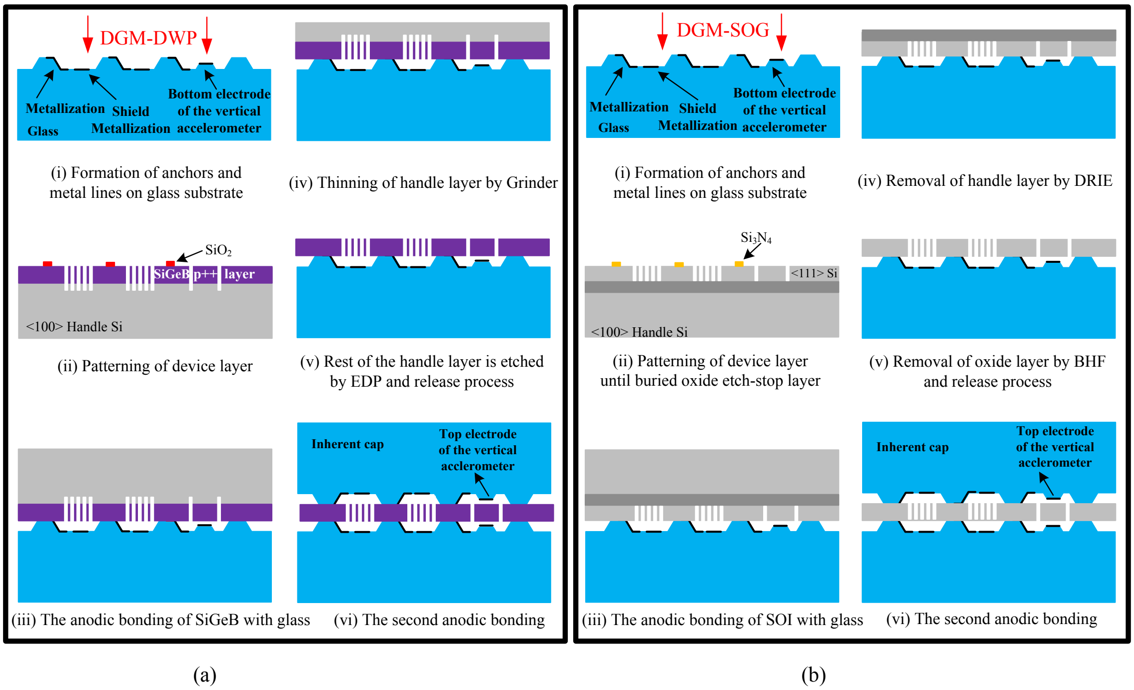
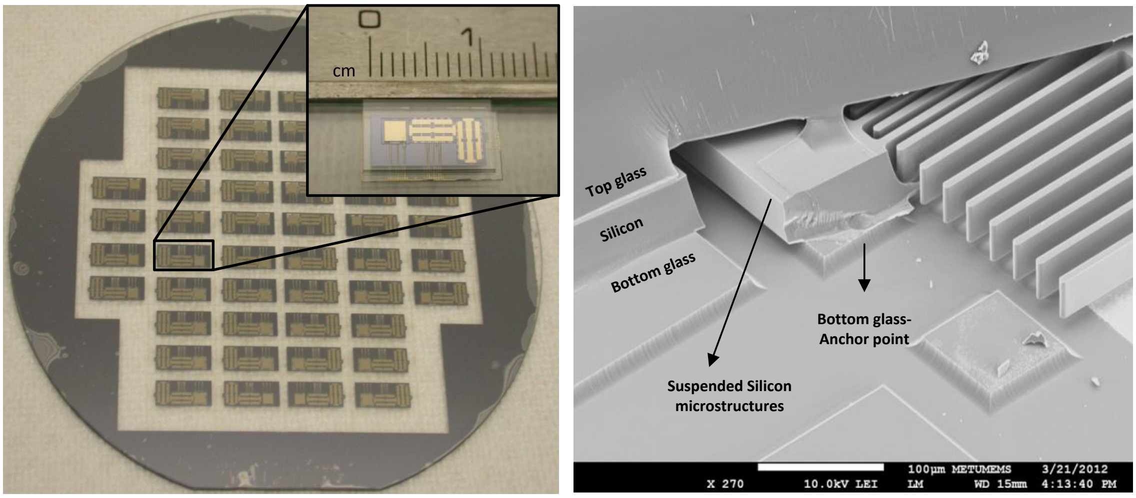


Fig. 1. The fabrication steps of the proposed processes: (a) a double glass modified dissolved wafer (DGM-DWP) process and (b) a double glass modified silicon-on-glass (DGM-SOG) process.



(a) (b)

Fig. 2. Fabricated three-axis capacitive MEMS accelerometer (a) wafer and die level; (b) an SEM image of glass-silicon-glass interface. The three-axis accelerometer looks similar in each process and each die measures 12mmx7mmx1mm.

3. Experimental Results

The rest capacitance values of a three-axis capacitive MEMS accelerometer fabricated with two alternative methods are measured for the comparison of fabrication results. Table 1 shows designed and measured capacitance values of the lateral and vertical accelerometer for two fabrication processes. There is a high mismatch between the capacitances formed between the proof mass and the top and the bottom electrodes of the vertical accelerometer fabricated by using the DGM-DWP. On the other hand, this mismatch is much smaller for the vertical accelerometer fabricated by using the DGM-SOG, and the reason of the small mismatch is the measurement conditions. Furthermore, the small deviation from the designed capacitance values for the vertical accelerometer fabricated by using the DGM-SOG is related to the fringing fields. Figure 3 shows the buckling amounts, which are the main reason of the capacitance mismatch, for the vertical accelerometers fabricated by using each process. Even a small amount of height difference between the anchor region and the proof mass causes the capacitance mismatch in the vertical accelerometer. It should be noted that this situation is not a major problem for the lateral accelerometer.

Table 1. The rest capacitance values of the lateral and vertical accelerometer.

Rest Cap. (pF)	**Designed**			
	Left side	**Right side**	**Top side**	**Bottom side**
The lateral	9.33	9.33	-	-
The vertical	-	-	11.34	11.34
Rest Cap. (pF)	**Measured (DGM-DWP)**			
	Left side	**Right side**	**Top side**	**Bottom side**
The lateral	9.87	9.88	-	-
The vertical	-	-	25.62	13.05
Rest Cap. (pF)	**Measured (DGM-SOG)**			
	Left side	**Right side**	**Top side**	**Bottom side**
The lateral	9.66	9.67	-	-
The vertical	-	-	13.36	14.05

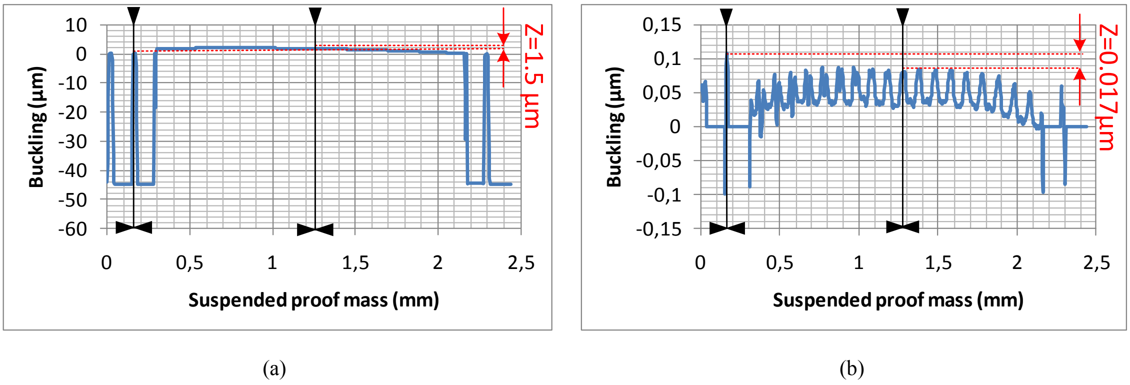


Fig. 3. The optical profiler measurement result for vertical capacitive accelerometer fabricated with (a) DGM-DWP where the buckling is 1.5µm and (b) DGM-SOG where the buckling is only 0.017µm.

4. Conclusion

This paper reports two fabrication processes for a three-axis capacitive MEMS accelerometer implemented by lateral and vertical accelerometer in a same die and compares the fabrication results. Clearly, there is a need for a highly stress-free structural layer especially to implement the vertical accelerometer. Such stress free structural layers are already present in the SOI wafers, which are typically used in the M-SOG process reported in [5]. This paper shows that the DGM-SOG process allows the proper fabrication of the MEMS capacitive vertical accelerometer, unlike the DGM-DWP process.

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