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An Optimized Analog Drive-Mode Controller for Vibratory MEMS Gyroscopes

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Abstract

This paper presents an optimized analytical design procedure for the drive mode analog controllers used in vibratory MEMS gyroscopes. The behaviour of the controller during start-up is analyzed in detail including the effect of the limited voltage swing of the controller circuitry. As a result, an optimum design procedure is developed for controller design, which is also experimentally verified in a practical implementation demonstrating a settling time of only 50msec without any overshoot, for a gyroscope having a quality factor (Q-factor) of 50,000. The new design procedure makes drive mode settling times almost insensitive to the Q-factor, making it suitable to obtain very-fast-starting MEMS gyroscopes even if they are packaged under high-vacuum.

Keywords: MEMS gyroscopes; drive mode controller; self-oscillation loop.

1. Introduction

Stability of the drive mode oscillation in high-Q MEMS gyroscopes is very critical for the overall system stability [1], which is closely related to optimum controller design. Fig.1 shows a sample analog drive mode controller circuit, which regulates amplitude of the drive mode oscillation in real-time by measuring the oscillation amplitude and generating a feedback voltage in order to minimize the error between the measured and reference amplitudes. Analog controllers are often selected for their simple implementation and predictable behavior [1-3]. The Proportional-Integral (PI) controller is a prevailing method for the amplitude regulation because of its zero steady-state error; however, the low frequency pole of the envelope characteristics of the drive-mode oscillation amplitude and the pole of the controller at DC put a significant constraint on the loop gain, creating a trade-off between the stability and settling

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time. This problem can be solved with modified topologies to fasten the settling time [4, 5] at the expense of complex design. This paper proposes a new analytical design approach for conventional analog controllers, which reduces the settling time with the help of a pole-zero cancellation method, where the effect of the low frequency pole of the drive mode envelope transfer function of the gyroscope has been removed.

2. Theory of Pole-Zero Cancellation Method

Fig.1 shows the simplified circuit diagram of the conventional drive mode controller circuitry. Envelope dynamics of the system portion operating at the drive mode resonance frequency (between A and B) is used for simplicity instead of using complete dynamics. Eq. 1 shows the transfer function of this envelope model.

$$H_{env}(s) = \frac{K_{env}}{s+\beta/2} \cdot F(s) \tag{1}$$

where, β is the drive mode bandwidth, K_{env} is a scalar of the envelope model, and F(s) is the transfer function of the low-pass filter.

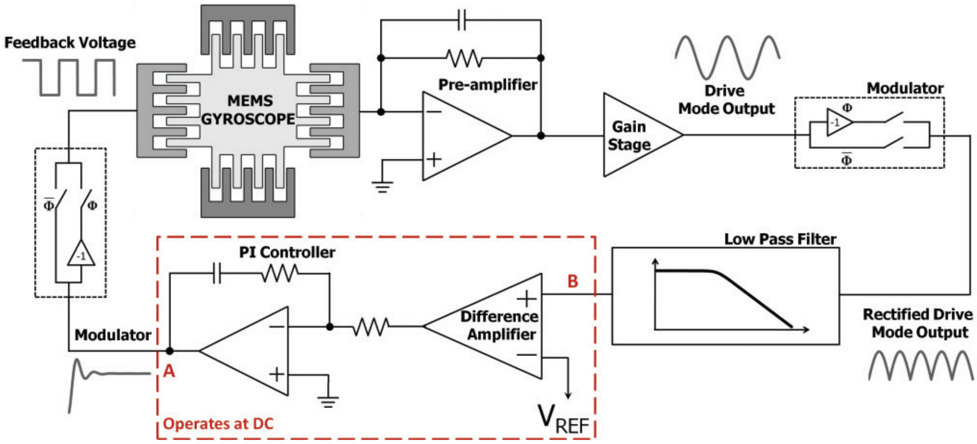

Fig. 1. Simplified circuit diagram of the conventional drive mode controller circuitry.

The envelope transfer function shown in Eq. 1 has a pole at *β/2*, which can be very low for a high-Q sensor. This low frequency pole and pole of the integrator at zero frequency (DC) cause a very low unity-gain frequency for a stable operation. This low unity gain frequency results in a very high settling time in the range of hundreds of milliseconds. To improve this settling time, the low frequency pole coming from the envelope model should be cancelled by means of a zero. Use of PI controller is an effective method to achieve this cancellation, where the low frequency pole of the envelope transfer function is cancelled, and at the same time the steady state error of the integrator reduces down to zero.

There are two major steps in the proposed design procedure. First, the pole-zero cancellation method is used to remove the low frequency pole of the drive mode dynamics. Second, open-loop gain is set to give a sufficient phase margin resulting in reduced over-shoot and improved settling time. Table 1 shows mathematically how pole-zero cancellation works and proportional gain factor (K_P) is determined.

Table 1. Pole-zero cancellation and determination of proportional gain factor (K_P).

$\text{Open Loop Transfer Function} = \underbrace{\frac{K_{env}}{s+\beta/2}}_{\text{Envelope Model}} \overbrace{F(s)}^{\text{Low Pass Filter}} \cdot \underbrace{K_P \cdot \frac{s+K_I/K_P}{s}}_{\text{Controller}}$	$K_P = \frac{\omega_{unity}}{K_{env}}$

Fig.2 shows the simulated transient response of the ideal drive mode control loop designed using pole-zero cancellation method. According to the simulation result, the system has an over-shoot of 7% and a settling time of 18msec for an error band of 1%.

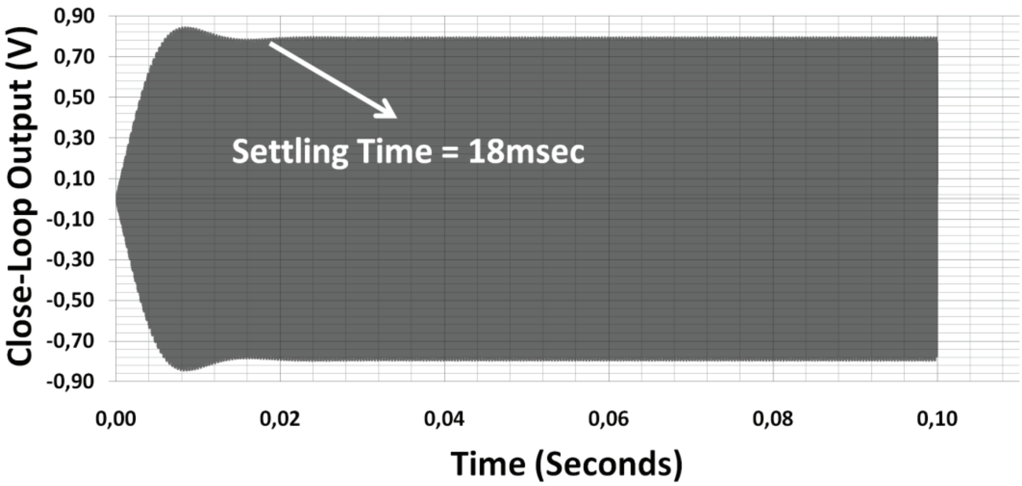

Fig. 2. Simulated transient response of the ideal drive mode control loop designed using pole-zero cancellation method.

3. Effect of the Limited Voltage Swing on the Transient Performance

In the above analysis, effect of the limited voltage swing of the control circuitry is not taken into account. Just after the system is powered up, demodulator output is around zero, and instrumentation amplifier output, which is also the input of the PI controller, is at $-V_{REF}$ voltage. At the beginning of start-up, integrator capacitor is initially discharged and behaves as a short circuit. Therefore, during at the beginning of the start-up, PI controller reduces to an inverting amplifier with a gain equal to $-K_P$. Consequently, opamp used in the PI controller saturates because of high K_P value and large input signal magnitude equal to V_{REF}. Due to saturated PI controller opamp, negative-feedback loop in the system is broken and mechanical sensor operates in the open-loop configuration. In this open-loop configuration, drive mode resonator is driven by a square waveform with amplitude of maximum voltage swing of the controller. Open-loop operation continues until input of the difference amplifier approaches V_{REF} such that controller input becomes small enough allowing the controller opamp operate in its expected linear region. In this condition, controller loop closes, making the system work in closed-loop configuration.

Fig.3(a) shows the overall settling behavior of the practical system where the settling time is composed of initial start-up time determined by the open-loop characteristics of the system and final small-signal settling time determined by the closed-loop behavior of the system. A good system design requires minimization of initial start-up time as well as final small-signal settling time, where both optimization requirements call for similar set of K_P and K_I values to achieve an optimized performance. Eq. 2 shows the initial start-up time expression of the system including the effect of limited voltage swing of the controller circuitry.

$$t_{start-up,initial} = \frac{V_{ref}}{V_{PI,SWING} \cdot K_{env}} \qquad (2)$$

where, $V_{PI,SWING}$ is the maximum voltage swing of the controller, and V_{REF} is the reference voltage determining drive mode oscillation amplitude. This equation also shows that the settling time expression is independent of the Q-factor. Note that in practical cases, small-signal settling time is much less compared to initial start-up time; therefore, the expression given in Eq. 2 can be used to approximately define the overall settling time.

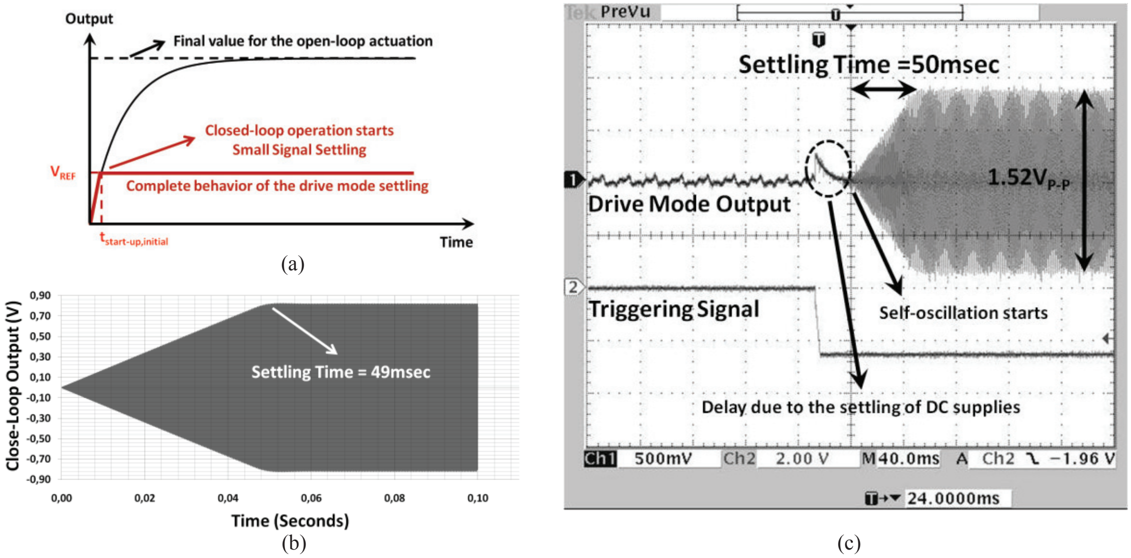

Fig. 3. (a) Overall settling behavior of the practical system (b) simulated start-up characteristics including the effect of the limited voltage swing of the controller circuitry (c) measured results of the start-up characteristics.

Fig.3(b) shows the simulated start-up characteristics including the effect of limited voltage swing of controller circuitry, and Fig.3(c) demonstrates the measured results of the start-up characteristics without over-shoot and with an overall settling time of 50msec for an error band of 1%. The same controller is also simulated for different sensors with different Q-factors varying between 5,000 and 100,000 resulting almost in a constant settling time.

4. Conclusion

This paper presents a design procedure to achieve an optimized drive mode controller. The effect of the limited voltage swing of the controller circuitry on the overall system performance is analyzed. The proposed design procedure yields a settling time of 50msec without overshoot.

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