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Light trapping by micro and nano-hole texturing of single-crystalline silicon solar cells

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Abstract

The efficiency of a solar cell strongly depends on the interaction between the incoming light beam and the surface of the device. Any process enhances light-surface interaction increases absorption probability of the light; thus, improves generated current, in turn. Generated current could be improved either by light trapping or by increased device thickness. Considering fabrication costs and recombination losses, mechanically thin optically thick wafers are being focused on in terms of light trapping properties. Surface texturing among the other methods is an effective and more lasting technique in reducing reflections and improving light trapping. In order to maximize the absorption of light and the efficiency of the cell, various light trapping schemes have been proposed so far. In this study, texturing silicon (Si) wafer surface with periodic holes using two top-down fabrication techniques: Metal Assisted Etching (MAE) and Reactive Ion Etching (RIE) was focused on. Following the design of optical masks with patterns of different hole sizes and distributions, hole-textured surfaces with dimensions varying from micron scale to submicron scale were fabricated using both etching techniques. Hole-textured surfaces with desired hole depth values could be successfully fabricated. It was observed that surface having periodic holes with 4 μm diameter, 5 μm gap between holes and 8 μm depth could result in 15.7% efficiency.

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1. Introduction

The traditional solar cell production is based on formation of random pyramids on the surface through an anisotropic etching process [1]. Although random pyramid approach is well-established and successful for standard wafer sizes, it is not the most preferable method for the wafers with low physical thicknesses. Various other surface structures have been proposed to create effective light-trapping for high absorption in crystalline Si solar cells [2,3]. Among them, formation of periodic micro- and nano-hole structures on the surface was shown to be promising approach for high efficiencies in solar cells with lower thicknesses [4,5]. Both MAE, and RIE were used to form periodic arrays of nano and micro holes on Si wafers. In both cases optical lithography was used to define the geometry and distribution of the holes. In the end, solar cells were fabricated on these surfaces using standard cell procedures to observe the effect of surface micro structures on cell performance.

2. Experimental part

With optimizing process conditions for different masks having various distribution of holes, hole-textured surfaces with dimensions varying from micron level to submicron level have been fabricated using both RIE and MAE methods. Depending on hole diameters, resist thickness should be defined properly. After clarifying correct lithography process parameters, pattern transfer could be successfully achieved which was examined by optical microscope imaging. Once pattern was defined, depth scaling was done by controlling etching parameters. Different metals with different film thicknesses, and different surface cleaning conditions for a successful etching, and removing metal from the surface could be counted as the important etching parameters to be controlled. MAE results in desired structures on the surface, unless there is no residual resist left after lift-off process. Else, it would result with an unsuccessful etching. In order to prevent it, an appropriate cleaning procedure was carried out [6]. Also for RIE, if the process parameters are not chosen in a proper way for the dimension of designed holes, then it may end up with an undesirable etch profile. For both etching techniques, appropriate process parameters were defined, and utilized. process. After fabrication of desired surface structure, corresponding solar cells were fabricated, which was followed by optical and electrical characterization steps.

Following surface patterning and necessary cleaning steps, fabrication sequence for standard cell structure was applied. The first process step is doping through which p-n junction is obtained by means of $POCl_3$ diffusion in a tube furnace at low vacuum conditions. Glass layer formed during diffusion is etched by dilute hydrofluoric acid (HF) dipping which is followed by standard cleaning procedure. After cleaning, dry oxidation at low temperature is carried out to form a thin silicon dioxide (SiO_2) layer with a thickness less than 10 nm to enhance surface passivation by saturating dangling bonds. Oxidation is followed by silicon nitride (SiN_x) deposition onto front surface of the cell which will both act as an antireflection coating and also improve surface passivation quality. SiN_x deposition is carried out in a parallel plate, PECVD system at around 400 ^{o}C. Metallization is the step following silicon nitride deposition. Front side metal pattern is defined by industrial screen printing method as an H patterned silver (Ag) grid whereas rear side metallization was done by thermal evaporation of aluminum (Al) due to adhesion problems of industrial Al pastes onto polished surfaces. Firing of front side metal grid is carried out in an industrial 8-zone firing furnace which is followed by laser edge isolation. Then, optical and electrical characterization tests were carried out.

2.1. Structure

In the cell process demonstrated in Fig. 1., p-type silicon wafers with <1-0-0> orientation having thickness of 525 μm and resistivity of 1-5Ω-cm were used as substrate. Prior to MAE process, lift-off method was used to obtain the metal film in the regions where holes were intended to form. During RIE process, we applied a short plasma descum, in order to get rid of resist residues and make efficient etching on surface.

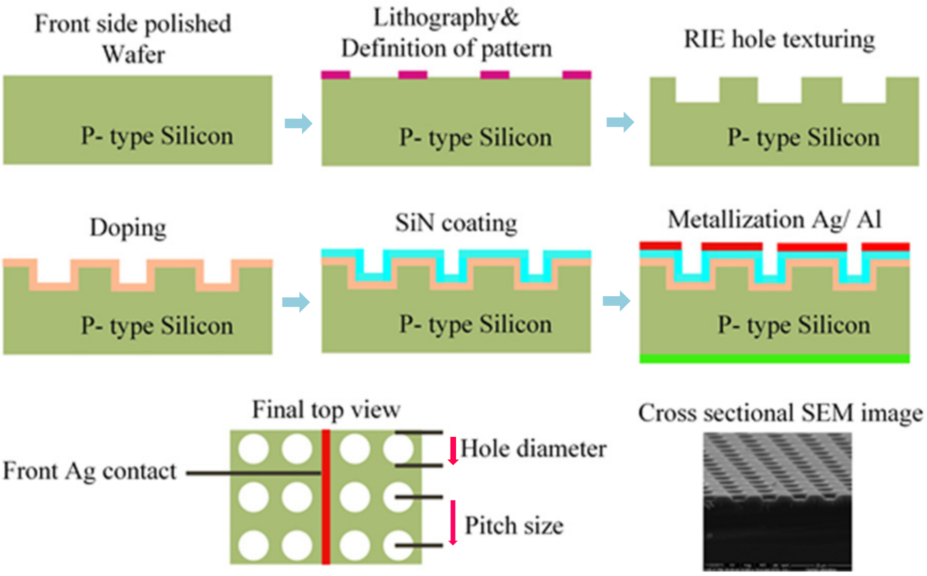

Fig. 1. Process scheme and cross sectional SEM image of textured surface.

2.2. Characterization

Optical properties of the surface with holes were characterized by reflection and transmission measurements. All optical measurements were carried out within the wavelength range from 400 to 1100nm using an integrating sphere attached system. After fabricating solar cells, key cell parameters (efficiency, open circuit voltage, short circuit current, and fill factor) were measured by a solar simulator and resultant data were analyzed as a function of hole size and distribution. Hole morphology, depth and distribution of the final devices was examined by SEM imaging. The optimum features for the best cell performance were then determined. Finally, the same experimental procedures were applied on thinner Si wafers to observe the increased benefit of periodic hole texturing in wafers with lower mechanical thicknesses. Thin Si has the benefits of not only independence on bulk lifetime, but also less material consumption, basic disadvantage is low absorption due to indirect band gap, and the best solution for that is light trapping textures with appropriate Si thickness [7,8].

3. Results

Reflection data is converted into AM1.5G weighted reflection using (1) and plotted as a function of filling ratio as shown in Fig. 2.

$$R = \frac{\int_{400}^{1100} R(\lambda)I(\lambda)d\lambda}{\int_{400}^{1100} R(\lambda)d\lambda} \tag{1}$$

As the ratio of unetched area to the whole surface area increased, averaged reflection also increased as expected. The AM1.5G weighed reflection reached at a minimum value of 9.56% when hole coverage fraction was 8.6%.

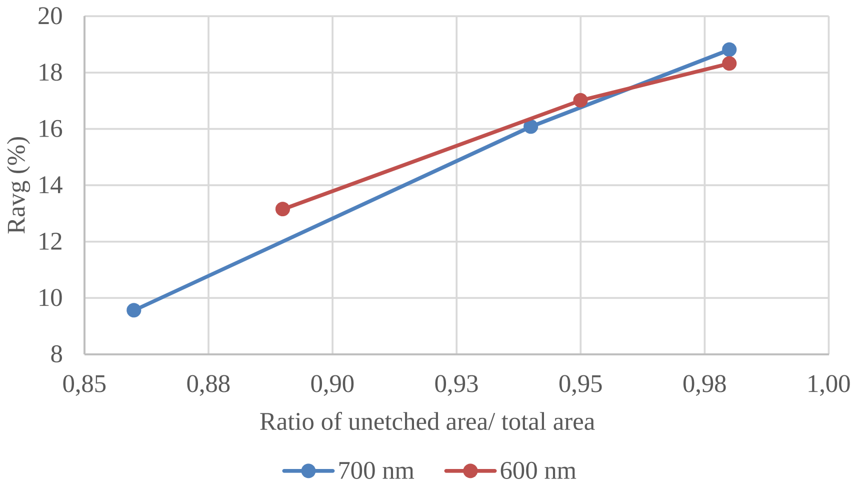

Fig. 2. Average reflection values according to unetched area/total area ratio of devices including holes with diameter of 600- 700 nm.

In order to analyze surface morphology SEM imaging was carried out for different hole sizes. The periodicity and the depth optimizations could be done according to these images. For RIE, etching time, and gas ratios could be optimized and depth of holes could be obtained as desired. For MAE, proper etching parameters, chemical concentrations, time could be varied, holes with designed dimensions, and wires in holes could be shortened or eliminated according to final device performance [9]. In Fig. 3. SEM images of the textured surfaces with holes having 1.2 µm pitch size applied RIE, and 9 µm pitch size after MAE are shown. For MAE, inevitably formed nanowires within the holes eliminated by KOH etching for sufficient time at suitable concentration.

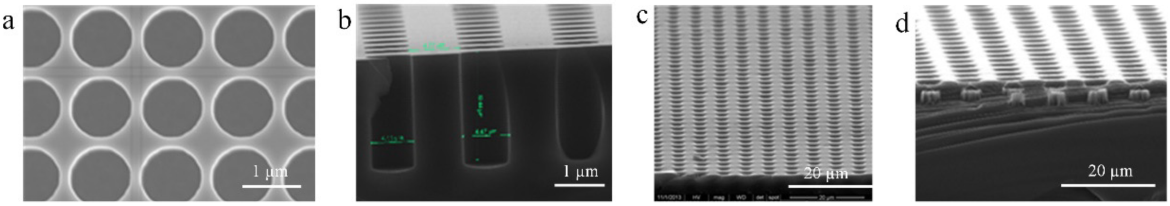

Fig. 3. (a) Top view of RIE textured surface, (b) cross sectional view of RIE done surface, (c) top view of MAE textured surface, (d) cross sectional SEM image of MAE done surface.

Fabricated solar cells with different patterns ended up with different device performance. Amongst them, holes of 4 µm diameter and 5 µm gap showed a remarkable trend for varying hole depths. As plotted in Fig. 4., increasing hole depth resulted in better cell performance.

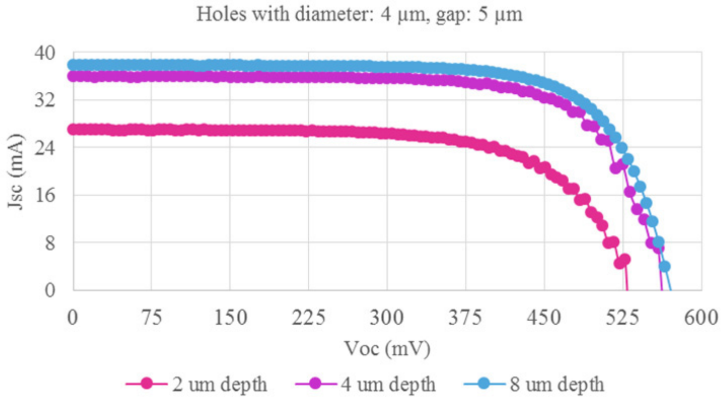

Fig. 4. J_sc (mA) versus V_oc (mV) comparison of surfaces having holes with diameter: 4 µm, gap: 5 µm, and depth: 2- 4- 8 µm.

Solar cells with micron and submicron sized holes were optically and electrically analyzed. The depth could be defined according to process parameters and periodicity of the textures. As can be seen in a surface having periodic holes with 4 µm diameter, 5 µm gap and depths 2- 4- 8 µm let us make a good decision to decide our next step.

Table 1. Performance of solar cells patterned with RIE textured surfaces having periodic holes with 4 µm diameter, 5 µm gap.

Depth (µm)	V_oc (*mV*)	J_sc (*mA/cm*^{2})	FF (*%*)	η (*%*)
2	527.7	27.0	67.5	9.6
4	563.3	35.9	72.5	14.7
8	569.9	37.8	72.8	15.7

Key performance parameters of these cells are given in Table 1,. It is expected that with an optimized passivation quality results are expected to be much better [10].

4. Conclusion

Si surfaces having different hole distribution and depth had better optical and electrical properties compared to bare ones. In order to obtain holes with sizes varying between micron to submicron level, both MAE and RIE methods were applied within the scope of this study. For MAE process, the length of the holes can be controlled with etching time, also wires that is seen in Fig. 3. (d) can be removed with diluted KOH solution. For RIE process depending on hole pitch size and desired depth gas ratios and etching times could be optimized in order to obtain ideal structure. Considering increasing J_sc values for increasing hole depth, it is expected that the reflection losses could be further lowered when optimization of antireflective coating for aforementioned periodic hole structures is completed. Also with more proper doping and passivation recipes, higher FF and V_oc values could be reached which will end up with greater cell efficiency values.

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