An Autonomous Interface Circuit Based on Self-Investing Synchronous Energy Extraction for Low Power Piezoelectric Energy Harvesters

An Autonomous Interface Circuit Based on Self-Investing Synchronous Energy Extraction for Low Power Piezoelectric Energy Harvesters

B Çiftci[1], S Chamanian[1], H Uluşan[1], and H Külah[1,2]

[1] Department of Electrical and Electronics Engineering, METU, Ankara, Turkey
[2] METU-MEMS Center, Ankara, Turkey

E-mail: cberkay@metu.edu.tr

Abstract. This paper presents a self-powered interface circuit to rectify and manage the AC output of the piezoelectric energy harvesters (PEH) by utilizing Self-Investing Synchronous Electric Charge Extraction technique (SI-SECE). The system invests charges from the battery to PEH to improve the electromechanical coupling factor and consequently the energy extraction by utilizing only one external component. The circuit was implemented in 180 nm CMOS technology where high voltage (HV) MOS transistors are utilized to tolerate high open circuit output voltages of PEHs. MEMS PEH with 4.7 nF inherent capacitance has been used to charge a 1 µF storage capacitor. Proposed interface circuit extracts 18.55 µW that is 33 % more than traditional SECE (13.95 µW) for 250 Hz PEH excitation frequency and 2.3 V piezoelectric open circuit voltage amplitude. At the output power of 48.5 µW, maximum power conversion efficiency of 62.4% is achieved as charge investment and corresponding conduction and switching losses on investing transistors. SI-SECE delivers power with 4.5x relative performance improvement over on-chip full-bridge rectifier.

1. Introduction

Harvesting energy from environmental sources could offer an opportunity to completely eliminate the bulky battery needed to power up wireless sensor networks (WSNs) and implantable electronic devices. Although harvesting energy from vibration and motion does not provide the maximum harvested power density (µW/cm^2) among existing energy sources, abundance of environmental vibrations makes vibration-based transducers more attractive sources of energy generation [1]. Piezoelectric energy harvesters (PEHs) have superior properties over other vibration-based transducers in terms of output power level and ease of integration [2].

In order to utilize the generated energy from PEHs, an interface circuit is required to rectify AC output of PEH and sustain a DC level required for electronic circuits in WSNs. Mostly, full-bridge rectifiers are used for energy conversion whose performance for low coupled PEH are severely affected by the built-in capacitance of PEHs. The theoretical analysis of various PEH interface circuits have been conducted in [3] to enhance the power extraction by modifying the damping force that the transducer could generate. Even though Synchronized-Switch Harvesting on Inductor (SSHI) technique in [4] is able extract more power compared to other nonlinear energy extraction approaches, Synchronous Electric Charge Extraction (SECE) method in [5] provide almost load independent architecture. A pre-biasing method implemented with discrete components to invest charge within synchronous switching [6] enables significant enhancement at the output power of PEH compared to

full-bridge rectifier (FBR). Nevertheless, the operation needs multiple off-chip inductors and high supply voltages. In [7], energy-investing PEH interface circuit was proposed to increase the extracted power by investing energy from battery utilizing only one inductor. However, an extra off-chip capacitor and a diode were used to generate negative voltage supply and it also suffers from the start-up problem.

This paper presents a self-powered and autonomous interface circuit to improve, rectify, and manage AC output of PEH by utilizing Self-Investing Synchronous Electric Charge Extraction technique (SI-SECE). The circuit invests charges from the battery to PEH to improve the electromechanical coupling factor and consequently the energy extraction. In the following section, the proposed circuit and its operation phases have been briefly described. Section 3 presents the experimental results of the fabricated SI-SECE chip. Finally, the work is concluded in Section 4.

2. Interface Circuit

The circuit is composed of seven main sub-blocks: Start-up block, negative voltage converter (NVC), peak detector (PD), sign detector (SD), reverse current detector (RCD), adjustable pulse generator, and switch control circuitry as shown in Figure 1. Figure 2 presents the die micrograph of SI-SECE chip implemented in 180 nm HV CMOS technology. It occupies an area of 0.79 μm^2. SI-SECE system invests and extracts energy twice throughout a full swing of PEH by utilizing only one external component (inductor).

Full operation of the system contains 4 phases summarized with measured results in Figure 3. In phase I, as PEH makes its swing, rectified PEH voltage, V_{PZT}, rises. PD, which was extensively analyzed in [2], finds the peak point of V_{PZT} and the system passes to phase II by turning S_2 ON. Here, charge available on piezoelectric capacitance, C_{PZT}, is transferred to the inductor. When V_{PZT} is close to zero, zero-crossing detector in switch control circuitry gives a signal to end phase II. During phase III, stored charge on the inductor is transferred to storage capacitance, $C_{STORAGE}$, with the help of S_1&S_3. RCD determines the instant at which all stored charge on the inductor is delivered to $C_{STORAGE}$ (end of phase III). In phase IV, RCD triggers adjustable pulse generator whose pulse width is controlled by V_{PG}. Depending on the polarity of PEH terminals, SD determines which switches (S_4&S_7 or S_5&S_6) are turned ON for investing charge. Phase IV is finished at the end of investing pulse duration and the system turns back to charge generation phase (phase I).

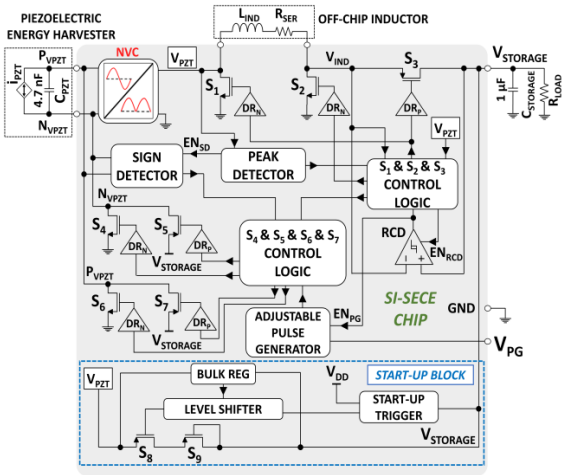

Figure 1. Self-Investing Synchronous Energy Extractor interface circuit.

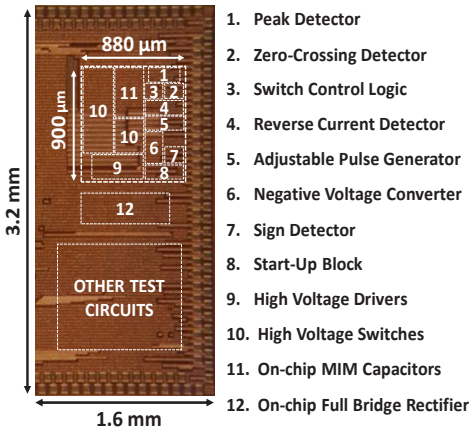

Figure 2. Die micrograph of the implemented SI-SECE chip.

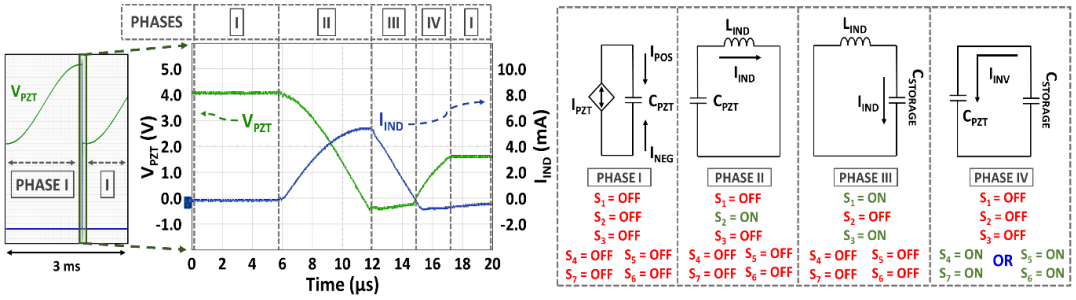

Figure 3. Summary of operation phases and measured waveforms of V_{PZT} and I_{IND}.

2.1. Zero-Crossing Detector

Zero-crossing detector (ZCD) presented in Figure 4 is designed to detect the point where V_{PZT} reaches zero voltage level and finalize the phase II. When V_{PZT} crosses 0 V towards negative voltage, the current drawn by M_1 from V_{DD} is mirrored with the help of M_5 & M_6 and node V_B is pulled to V_{DD}. ZCD is completely disabled except for phase II to minimize the power dissipation.

2.2. Adjustable Pulse Generator

Figure 5 depicts the adjustable pulse generator used in phase IV to determine the time period of energy investment. Delay time constituted by inverters and on-chip RC components can be adjusted with the bias voltage V_{PG}. As the input voltage transits from low to high, M_5 and M_7 change states while M_4 is still ON that pulls node V_X to ground through M_4 and M_5. After the delay, capacitor C_D is discharged which turns M_6 ON and pulls up V_X to V_{DD} to finalize the generated output pulse V_{PULSE}.

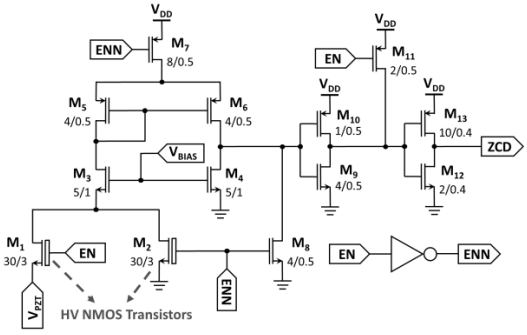

Figure 4. Zero-crossing detector.

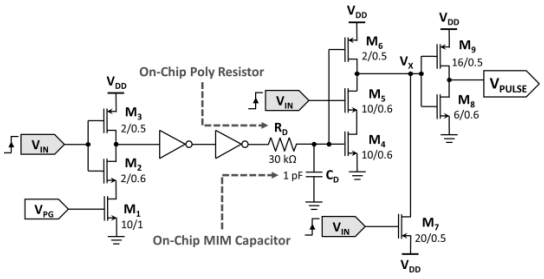

Figure 5. Adjustable pulse generator.

3. Experimental Results

Figure 6 shows the test setup for experimental analysis of the SI-SECE circuit. During tests, custom MEMS PEH with 4.7 nF C_{PZT} was excited at 250 Hz with shaker table. Figure 7 depicts experimentally measured waveforms of V_{PZT} and $V_{STORAGE}$ that presents charging of $C_{STORAGE}$. After the charging process, an amount of charge on $C_{STORAGE}$ is invested into C_{PZT}, which slightly lessens $V_{STORAGE}$. Experimental power conversion efficiency and extracted power as a function of piezoelectric open circuit voltage $V_{OC(PZT)}$ is presented in Figure 8. Maximum power conversion efficiency of 62.4% is achieved due to dominant conduction and switching losses on investing transistors. Dependency of the extracted power to $V_{STORAGE}$ is plotted in Figure 9. SI-SECE circuit extracts 18.55 µW that is 33% more than traditional SECE operation (13.95 µW) for the same conditions. Furthermore, the proposed system extracts power with 4.5x relative performance improvement over on-chip FBR.

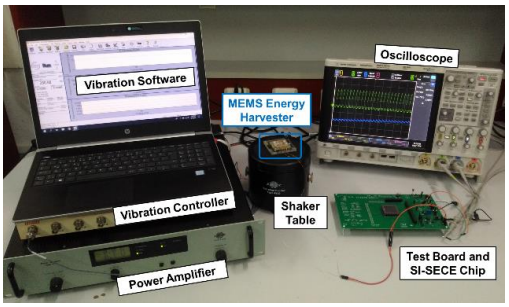

Figure 6. Test setup for performance analysis of SI-SECE chip.

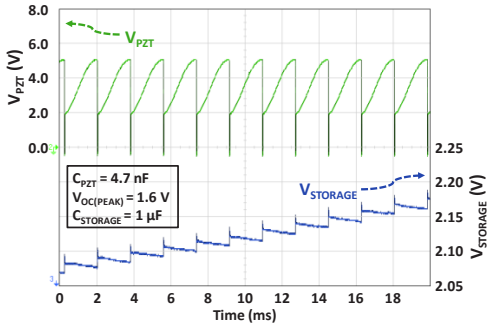

Figure 7. Measured waveforms of rectified piezoelectric voltage V_{PZT} and storage voltage.

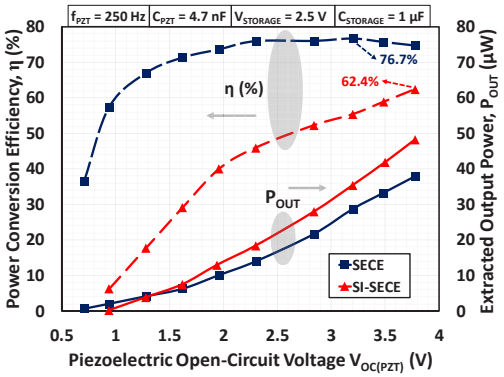

Figure 8. Experimental power conversion efficiency and extracted power versus $V_{OC(PZT)}$.

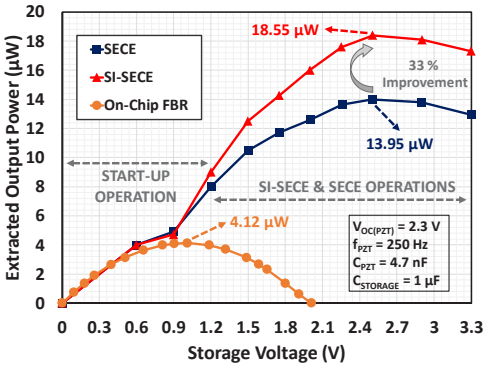

Figure 9. Experimental extracted power versus storage voltage $V_{STORAGE}$.

4. Conclusion

A self-investing energy harvesting interface circuit with significant power increment is presented in this paper. The SI-SECE circuit can extract power from MEMS-based PEH autonomously by using only an inductor. Test results of the fabricated SI-SECE chip showed that the circuit was able to provide 33% more power to the load compared to conventional SECE. Due to the fact that current flowing through C_{PZT} is not limited during investment process, conduction and switching losses become dominant which leads to maximum power conversion efficiency of 62.4%. It is predicted that the efficiency of SI-SECE circuit can be further increased in the future through the investment process in energy packages.

Acknowledgement

This work has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (grant no:682756) and it is in part supported by the Scientific & Tech. Research Council of Turkey (TUBITAK), grant no:117E003.

References

[1] Vullers R J M *et al* 2010 *IEEE Solid-State Circuit Magazine* **2** 29–38
[2] Chamanian S *et al* 2018 *IEEE TPEL* doi: 10.1109/TPEL.2018.2841510
[3] Dicken J *et al* 2012 *IEEE Transactions on Power Electronics* **27** 4514–29
[4] Ramadass Y and Chandrakasan 2010 *IEEE Journal of Solid-State Circuits* **45** 189–204
[5] Hehn T *et al* 2012 *IEEE Journal of Solid-State Circuits* **47** 2185–98
[6] Dicken J *et al* 2009 *Proc. PowerMEMS* (Washington DC: USA) pp 75–78
[7] Kwon D and Rincon-Mora G 2014 *IEEE Journal of Solid-State Circuits* **49** 2277–91