NON-FOSTER IMPEDANCE MATCHING FOR ELECTRICALLY SMALL ANTENNAS

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ABSTRACT

NON-FOSTER IMPEDANCE MATCHING FOR ELECTRICALLY SMALL ANTENNAS

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At low frequencies, non-Foster matching improves the performance of ESAs and overcomes the limitations imposed by the electrical size of antenna. Thus, the major objective of this thesis is to design and implement a non-Foster matching network in order to improve the bandwidth of an ESA beyond the levels that cannot be reached by conventional passive matching. Negative impedance converters (NICs), which are specific circuits to realize negative circuit elements, are used to design such non-Foster circuits.

In this context, a systematical design procedure for a non-Foster matching network is presented and implemented to match a 10-cm monopole antenna between 150 MHz and 500 MHz. A BJT based NIC is built to generate a series combination of a negative inductor and a negative capacitor together with an inductive T-dualizer which is a circuit that is used to transform small radiation resistance of the ESA to a desired constant value. The performance of the overall network is measured between 100 MHz and 1 GHz with different input power levels and different loads. A bandwidth of 684 MHz from 127 MHz to 811 MHz is achieved with a VSWR that is better than 3.57 while the unmatched antenna has a VSWR that is no better than 8.72 until 850 MHz.

Besides, the effects of input power and load changes on matching performance are examined and commented.

Keywords: Keywords: Electrically Small Monopole Antennas, Negative Impedance Converters, Non-Foster Impedance Matching

ÖZ

ELEKTRİKSEL OLARAK KÜÇÜK ANTENLER İÇİN FOSTER OLMAYAN EMPEDANS UYUMLAMASI

Altuntaş, Orhun Tevfik
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Düşük frekanslarda, Foster olmayan uyumlama, elektriksel olarak küçük antenlerin performansını artırır ve antenin elektriksel boyutunun getirdiği sınırlamaları aşar. Bu tezin amacı, elektriksel olarak küçük bir antenin bant genişliğini geleneksel pasif eşleştirmeyle erişilemeyen seviyelerin ötesinde geliştirmek için Foster olmayan bir empedans uyumlandırma devresi tasarlamak ve uygulamaktır. Negatif devre elemanlarını gerçekleştirmek için spesifik devreler olan negatif empedans dönüştürücüler, bu tür Foster olmayan devreleri tasarlamak için kullanılır.

Bu bağlamda, 10 cm boyunda tek kutuplu bir anteni 150 MHz ile 500 MHz arasında eşlemek için Foster olmayan bir empedans uyumlama devresinin tasarım prosedürü sistematik bir şekilde sunulmuş ve uygulanmıştır. Elektriksel olarak küçük antenin küçük radyasyon direncini istenen sabit bir değere dönüştürmek için kullanılan bir devre olan bir endüktif T-dualizer ile birlikte bir negatif indüktör ve bir negatif kondansatör dizisi üretmek üzere bir BJT bazlı negatif empedans dönüştürücü tasarlanmıştır. Bütün devrenin performansı, farklı giriş gücü seviyeleri ve farklı yükler ile 100 MHz ve 1 GHz arasında ölçülmüştür. Empedans uyumlaması yapılmamış antenin 850 MHz'e kadar 8.72' den daha iyi olmayan bir gerilim duran dalga oranı varken, uyumlama ile 127 MHz' den 811 MHz'e 684 MHz bant genişliği 3.57 gerilim

duran dalga oranı ile elde edilmiştir. Ayrıca, giriş gücü ve yük değişimlerinin uyumlama performansına etkileri incelenerek yorumlanmıştır.

Anahtar Kelimeler: Elektriksel Olarak Küçük Tek Kutuplu Antenler, Negatif Empedans Dönüştürücüler, Foster Olmayan Empedans Uyumlama

To my family

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

AWR MWO®: AWR Microwave Office®

BJT: Bipolar Junction Transistor

ESA: Electrically Small Antenna

GFET: Graphene Field Effect Transistor

METU: Middle East Technical University

MMIC: Monolithic Microwave Integrated Circuit

NIC: Negative Impedance Converter

OCS: Open Circuit Stable

PCB: Printed Circuit Board

RTD: Resonant Tunneling Diode

SCS: Short Circuit Stable

SMT: Surface-mount Type

SNR: Signal to Noise Ratio

SoC: System on Chip

UAV: Unmanned Air Vehicle

USV: Unmanned Surface Vehicle

THD: Total Harmonic Distortion

VHF: Very High Frequency

VSWR: Voltage Standing Wave Ratio

CHAPTER 1

INTRODUCTION

1.1. MOTIVATION AND APPROACH

Device miniaturization has been an emerging topic in electronics area for decades. Researchers are continuously seeking for methods to minimize the electronics equipment without causing a degradation of performance in order to obtain low-cost, practical, reliable and fully integrated systems. Accordingly, a remarkable progress has been achieved by circuit design engineers in the area of silicon technology. Computing devices that comprised of thousands of active devices are now capable to fit into a single chip. Still, engineers are working to develop smaller technologies in order to boost system-on-chip (SoC) solutions.

Together with the developments in the area of semiconductor and computer technology, wireless and mobile communication technology has also been evolved. As a consequence of merging of this development and the need for remote communication, almost every electronics device has now a wireless communication equipment integrated to the device. Hence, smaller communication equipment has become an increasing demand in the industry to shrink the size of devices more. An antenna is a natural part of a communication equipment, and thus should be minimized to keep step with the technology. However, it is well known by every RF engineer that an antenna must have a certain electrical size which is comparable to its wavelength in order to be able to receive and transmit information efficiently. Thus, the focus of RF circuit designers has been shifted to implementations with electrically small antennas (ESAs) to catch up with the trend of miniature devices. Yet, Bode-Fano criterion states that while shrinking the antenna in size, it is not possible to keep

performance metrics such as bandwidth and efficiency [1,2]. As a result of this limitation, it may never be possible to implement a passive, high performance, wideband electrically small antenna.

The usage of wideband electrically small antennas is not only common for civilian applications but also a growing demand in military communication systems. Efficient designs in a limited space has always been a concern for military electronics. Conventional dipole or monopole antennas are still in use for military applications such as voice, telemetry and direction finding as well as other purposes on platforms such as tanks, ships, unmanned air and surface vehicles (UAV and USV). Especially for UAV and USV, the size and weight of the antennas are of particular concern where the need for low profile, low weight and low observable radiating elements are essential [3]. Both limited space and wideband communication requirements pinpoints the usage of electrically small antennas in an efficient way.

Increasing demand of ESAs in both civilian and military applications pushed the researchers to find a way out of limitations defined by Bode-Fano criterion. The limitations possessed by electrically small antennas can be listed under three main headlines; input impedance, radiation performance and bandwidth. Input impedance of ESAs are characterized by high reactance and a small radiation resistance. In other words, ESAs are highly reactive antennas which stores much of their input energy in near field. Hence, impedance characteristics of ESAs put a limit on radiation performance. Achievable bandwidth is another matter about ESAs. ESAs inherently possess a high Q-factor. Considering the fact that bandwidth of an ESA is inversely proportional to Q-factor, achievable bandwidth is limited. More detailed information on the relation between bandwidth and Q-factor is also given in section 2.1.2.

Aforementioned negative features of ESAs can be dealt with active matching techniques which passes beyond the limitations imposed by physical dimensions. By means of active circuits, it is possible to cancel out the reactance of ESA and match the remaining radiation resistance to 50 Ω over a wide frequency interval. The idea is

based on canceling the reactance of a small antenna by implementing a negative inductor or a negative capacitor or a combination of them at the input port. Such negative elements are called non-Foster impedances and the overall technique is known as non-Foster impedance matching.

At this point, giving a brief definition of the terms “Foster” and “non-Foster” is appropriate. Foster’s reactance theorem states that for a lossless passive two-terminal element, the reactance always increases monotonically with the frequency [4]. Elements that are consistent with this theorem are called Foster impedances such as an inductor and a capacitor. Simply, elements which disobey the Foster’s reactance theorem are called non-Foster impedances such as a negative inductor or a negative capacitor. In Figure 1.1, a simple non-Foster impedance matching operation is demonstrated conceptually in comparison with passive conventional matching. If a capacitance is resonated with an ideal negative capacitance of same value, the net reactance becomes zero for all frequency spectrum. In the case of conventional passive matching, zero net reactance can be achieved at one frequency. Hence, by means of non-Foster impedances, it is possible to overcome the limitations imposed by Bode-Fano criterion which is based on the physical properties of electrically small antennas.

The main motivation of this thesis study is to implement non-Foster impedances at the input of an electrically small monopole antenna in order to cancel out its reactance and match the radiation resistance to a constant 50 Ω. Since the non-Foster impedances are, by definition, negative elements, they produce energy rather than consuming. In other words, active circuits are required to obtain non-Foster elements. Such circuits that have the ability of generating non-Foster impedances are called negative impedance converters (NIC). Generally speaking, NICs are comprised of non-linear devices such as transistors and operational amplifiers of which practical implementations can be found in [5-7]. In this thesis, a transistorized version of negative impedance converter circuit is designed and fabricated to generate a series of a negative capacitor and a negative inductor. Thereby, a non-Foster matched wideband

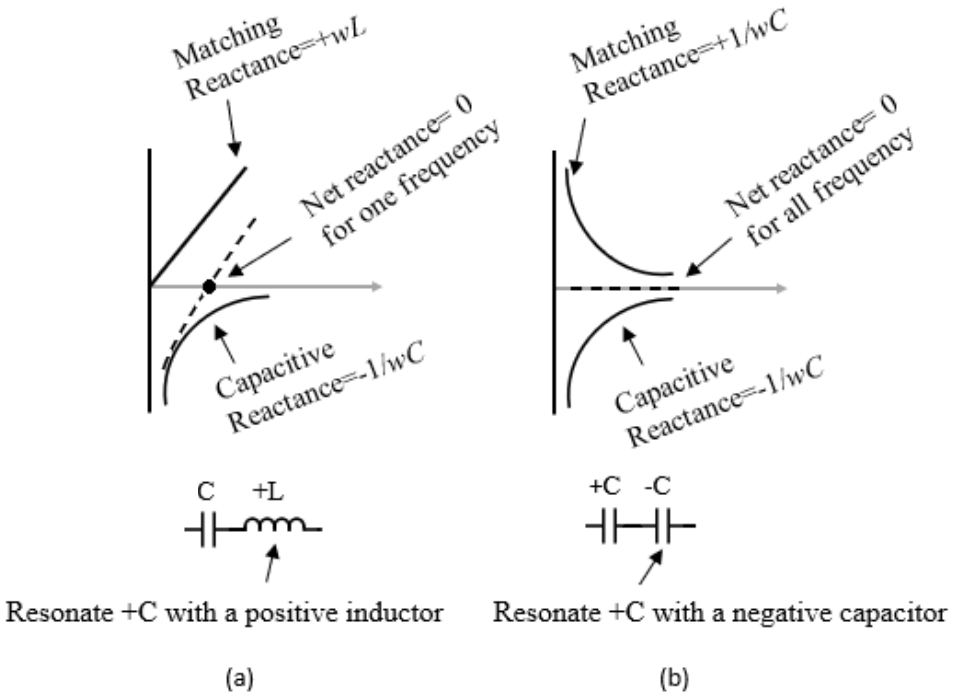

Figure 1.1. Conventional Matching versus non-Foster matching [8]. a) Passive Conventional Matching b) Non-Foster Matching

electrically small antenna is obtained at the end. Implementations and theory of NICs are given in more detail in Chapter 2.

Although the idea of generating non-Foster impedances seems to be very promising, it has also some limitations imposed by active non-linear devices present in the circuit. Positive feedback paths of non-Foster circuits may give rise to stability problems, which is handled in detail in Chapter 3. Moreover, especially in high power applications, the effects of non-linearities come into play as examined in Chapter 4.

Non-foster impedances are not only restricted to applications of electrically small antennas. Series negative inductors are used to obtain fast-wave low-dispersion transmission lines [9] and true time-delay lines [10] in addition to provide rejection of parasitic deterioration in integrated circuits [11]. However, these applications are beyond the scope of this thesis.

1.2. ORGANIZATION OF THE THESIS

Having completed the motivation and approach of this thesis, the rest of the study is organized as follows.

Chapter 2 begins with the definition and fundamental knowledge about electrically small antennas in order to have a clear understanding before building non-Foster impedance matching circuit. The relationship between Q-factor and achievable bandwidth is given by formulations from the literature. Before diving into negative impedance converters, equivalent lumped circuit model of an electrically small monopole is given with approximate formulas. Following, negative impedance converters are defined, and a comprehensive literature review is supplied. Meanwhile, operation logic of NICs is described by use of two-port ideal hybrid parameters. Besides, the transistorized NIC topology which is fabricated in the context of this thesis work is analyzed in detail by means of small signal equivalent circuits. Upon the completion of NICSs, a review of non-Foster matching literature is presented in order to make use of previous experiences in design phase. Knowing that a non-Foster impedance only cancels the reactance of antenna, a method called inductive T-dualizer is introduced in order to transform small radiation resistance of antenna to a constant 50 Ω. Gathering all information on NICs and inductive T-dualizer, a non-Foster matching circuit is designed in AWR Microwave Office® (AWR MWO®) design environment with an ideal negative impedance converter and ideal lumped circuit elements to match a 10 cm monopole antenna, which is modeled as a series combination of capacitance and radiation resistance. At the end of chapter 2, the effects of transistor parameters on circuit response are investigated such as collector-base capacitance and small signal emitter resistance.

Chapter 3 addresses the design and implementation of a practical non-Foster matching circuit. Component spice models that are created by component manufacturers are used in circuit design rather than ideal models. First of all, a systematical design

procedure is presented in order not to get lost in complex design phase. Following, the input impedance and return loss measurements of the real antenna, which is used in this thesis study, is given with no matching at all. By analyzing the input impedance characteristic of the antenna, required non-Foster impedances are revealed to match the antenna. As a result of this analysis, an RLC equivalent circuit of the antenna is built up. Prior to the design of non-Foster matching circuitry, stability problem of NICs are introduced. Different methods of stability analysis are presented. Completing the necessary theoretical background, a non-Foster matching circuit is designed and simulated in AWR MWO® for the real antenna introduced in the beginning of Chapter 3. In addition, a stability analysis is conducted on the design to explore the unstable modes of the circuit and compensate them.

Chapter 4 is devoted to fabrication and evaluation of measurement results of the matching circuit designed in Chapter 3. First of all, the features of printed circuit board (PCB) material and circuit components are presented together with the layout. Onwards, the input impedance and return loss measurements of non-Foster matched antenna are presented in comparison with measurements of unmatched case and simulation results. Furthermore, the circuit is measured under different input power levels to explore the non-linear behavior of the transistors. Following, simulation results related to harmonic distortion, efficiency improvement and transducer gain improvement are presented. Finally, load of non-Foster matching circuit is altered among three different values in order to learn if it is possible to obtain better matching results with a load other than the one implemented at first.

Chapter 5 discusses all work done within the scope of this thesis and future tendencies on non-Foster matching of antennas.

CHAPTER 2

BASIC CONCEPTS

2.1. ELECTRICALLY SMALL ANTENNAS

The electrical dimensions of an antenna are specified by the free-space wavelength at the operating frequency. Since the word "small" is a comparative expression, it is substantive to put a limit for the definition of ESA. No certain definition exists to describe an ESA, yet there are some limitations specified in the literature. Definition of an ESA, fundamental limitations of ESAs and ideal equivalent circuit representation of an electrically small monopole will be described in sections 2.1.1, 2.1.2 and 2.1.3, respectively.

2.1.1. DEFINITION OF ELECTRICALLY SMALL ANTENNA

Wheeler, in 1947, stated that an antenna can be classified as small when its maximum dimension is less than the radian length where radian length is defined as $1/2\pi$ of free-space wavelength at the operating frequency [12]. Figure 2.1 shows an example of a dipole antenna located in a virtual sphere with a radius "a". Applying the criteria stated above, the relation between antenna physical length and free-space wavelength can be established as in Eq. 2.1, where $2a$ and λ are the maximum dimension of antenna and wavelength, respectively.

$$2a < \frac{\lambda}{2\pi} \tag{2.1}$$

Employing the relation between wavenumber k and free-space wavelength, $k=2\pi/\lambda$, Eq. 2.1. can be written as Eq. 2.2.

$$ka < 0.5 \tag{2.2}$$

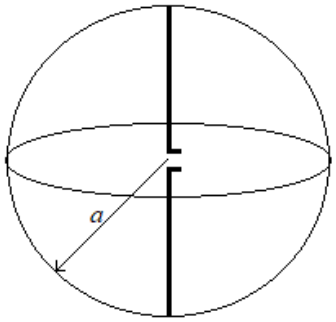

Figure 2.1. A dipole antenna inside a hypothetical sphere

Later, in 1981, Hansen put a different limitation for electrically small antennas [13]. He used the constraint given in Eq. 2.3 in his study related to fundamental limitations in antennas.

$$ka < 1 \tag{2.3}$$

Although there is no strict definition for an antenna to be electrically small, one can make a deduction by evaluating different limitations in the literature. In a more general manner, a small antenna can be defined as an antenna whose largest dimension is much smaller than a wavelength at the frequency of interest.

2.1.2. LIMITATIONS OF ELECTRICALLY SMALL ANTENNAS

The first contribution about the limitations of small antennas have been made by Wheeler [12]. Later, authors have made contributions to formulate the relation

between quality factor and electrical size of an antenna, and these studies are well summarized in [14]. As stated in previous section, electrical size "ka" of an ESA is small, leading to some limitations on antenna performance such as radiation quality factor and bandwidth. The radiation quality factor is defined as 2π times the ratio of energy stored in the reactive field of the antenna to the radiated and dissipated energy [15]. Hence, a high-Q antenna will store much of the input energy while radiating a small portion. A rough formulation of minimum Q-factor of an antenna with $ka < 1$ is presented in Eq. 2.4 which is derived by using spherical wave functions [13].

$$Q_{min} = \frac{1 + 3k^2a^2}{k^3a^3(1 + k^2a^2)} \tag{2.4}$$

It is worthy to note that for $ka << 1$, the Q-factor is inversely proportional to the cube of the antenna size. As the size of antenna decreases, the Q-factor of an antenna rapidly increases meaning that the stored energy in the reactive field is getting much higher than the radiated energy. Another formulation for Q-factor is given by Eq. 2.5, revealing Eq. 2.4 shows a small deviation from exact results near $ka = 1$ [16].

$$Q_{min} = \frac{1}{k^3a^3} + \frac{1}{ka} \tag{2.5}$$

One way or another, the Q-factor of an ESA is significantly high, and this characteristic of small antennas shrinks the bandwidth of operation as a result. The maximum achievable fractional bandwidth of a standalone antenna in terms of Q-factor and voltage standing wave ratio (VSWR, s) is given by Eq. 2.6 [17].

$$B_{max} = \frac{1}{Q_{min}} \frac{s - 1}{\sqrt{s}} \tag{2.6}$$

When Q >> 1 condition holds, fractional bandwidth can also be written as in Eq 2.7 [18].

$$B = \frac{1}{Q} \tag{2.7}$$

Both formulations show that the Q-factor of antenna is inversely proportional to the bandwidth. Therefore, some additional designs are needed for wideband operations of small antennas. Bandwidth can be improved by implementing a passive lossless matching circuitry as depicted in Figure 2.2. However, the bandwidth is limited by minimum tolerable reflection coefficient according to Bode-Fano Criterion stating that one can lower the reflection coefficient at the expense of smaller bandwidth [1,2]. Even so, this criterion is valid for passive matching and can be violated by active matching techniques.

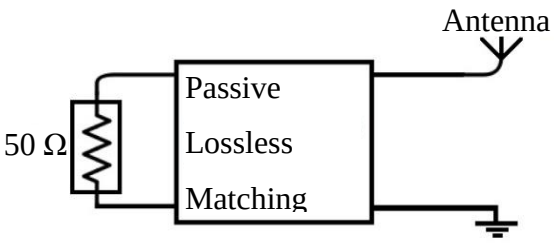

Figure 2.2. Bandwidth improvement implementing passive lossless matching

2.1.3. EQUIVALENT MODEL OF ELECTRICALLY SMALL ANTENNAS

It is important to understand the small antenna theory and its equivalent circuit parameters before building a matching circuitry. Different small antenna types are investigated and analyzed in terms of its equivalent circuit parameters in [19] such as dipole, loop and dielectrically loaded antennas. In the case of antenna length is much smaller than a wavelength, antenna reactive parts can be represented by just a capacitor for a dipole and monopole or just an inductor for a loop antenna.

A vertical monopole antenna of length L above a perfect ground plane is depicted in Figure 2.3. Equivalent antenna capacitance and radiation resistance of the short monopole are given in Eq. 2.8 and Eq. 2.9 as

$$C_{ant} = \frac{2\pi \in_0 L}{\ln\left(\frac{L}{\rho}\right) - 1} \tag{2.8}$$

$$R_{rad} = 40\pi^2 \left(\frac{L}{\lambda}\right)^2 \tag{2.9}$$

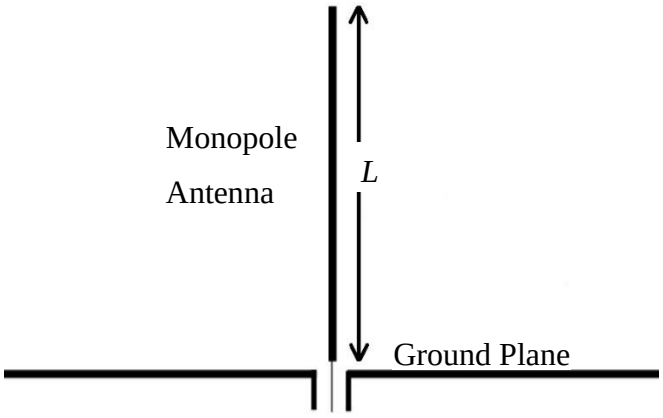

Figure 2.3. A monopole antenna above ground plane

where $\in_0$ is the permittivity of free-space, ρ is the wire radius, L is the antenna length and λ is free space wavelength [20]. In Figure 2.4, radiation resistance and reactance vs L/λ of a 10 cm monopole with radius 0.75 cm are plotted according to equations 2.8 and 2.9 in order to visualize significant difference between them. It is seen from the Figure 2.4 that the reactance of electrically small monopole is much higher than the radiation resistance especially for small values of L/λ. For example, for $L/\lambda = 0.05$ point, the radiation resistance is around 1 Ohm, while the reactance of the antenna is -250 Ohms. The significant gap between the reactance and the radiation resistance clarifies why small antennas store much of its input energy. As stated in the beginning of this section, reactive part of an electrically small monopole can be represented by just a capacitor. Hence, a lumped model for a small monopole can be developed as a capacitor in series with a radiation resistance as in Figure 2.5.

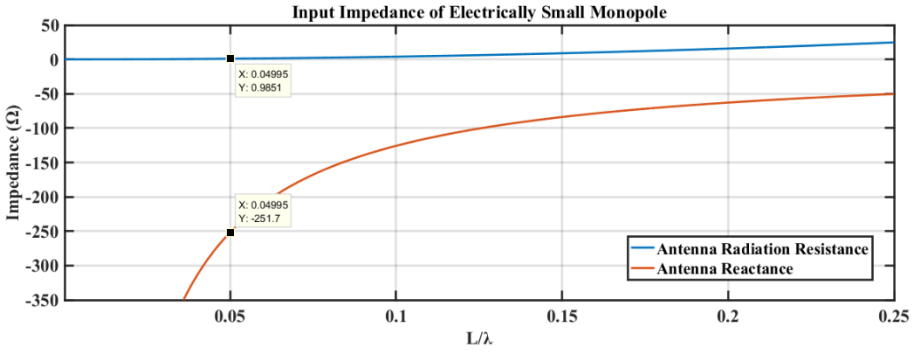

Figure 2.4. Input reactance and radiation resistance of monopole antenna vs. L/λ

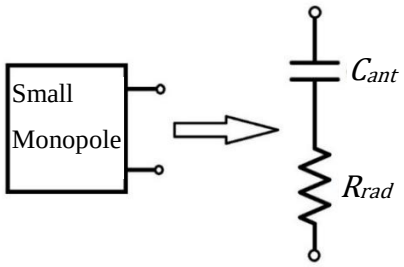

Figure 2.5. Equivalent lumped model of a small monopole [20]

2.2. NEGATIVE IMPEDANCE CONVERTERS

A negative impedance converter is an active two-port network where the driving port impedance is converted to the negative of a load impedance, $Z_{L,}$ connected to the other port [21]. Figure 2.6 demonstrates the conceptual operation of a two-port ideal negative impedance converter, where k is a positive number representing the conversion coefficient. Theoretically, when one port is loaded by an arbitrary impedance, the input impedance seen from the other port is equal to the negative of the load impedance times a conversion coefficient, k. In the next section, a review and an analysis of NICs is given in order to lead the way through a deeper understanding.

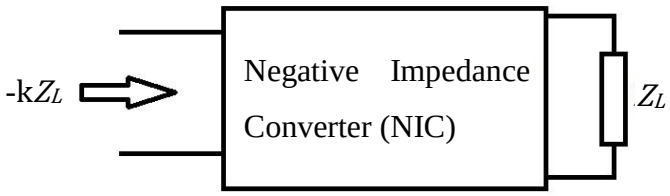

Figure 2.6. Ideal two-port representation of a negative impedance converter

2.2.1. A REVIEW OF NICs

The first proposal of negative impedance converters dates back to 1920s and can be attributed to Marius Latour according to Merrill's study, in which, a negative impedance converter design is utilized based on vacuum tubes in 1951 [22]. He generated negative resistors for long telephone lines to increase transmission gain. In 1953, Linvill [5] proposed four different types of NICs comprised of BJTs which are floating (balanced) open-circuit stable (OCS), grounded (unbalanced) OCS, floating short-circuit stable (SCS) and grounded SCS. All four types of Linvill's NICs are depicted in Figure 2.7. Grounded type NICs are designed to be connected as a shunt element to the network while floating types are to be connected as series. There are also two simplified conditions on stability of Linvill's NICs. The first one is that if the input to the NIC is at the emitter of the transistor, the NIC will be OCS by ensuring that the NIC sees an open circuit at its input and the second condition is that if the input to the NIC is at the base-collector junction, the NIC will be SCS by ensuring that the NIC sees a short circuit at its input [23]. Linvill specified bulkiness, relatively short life, deterioration with age and limited ruggedness as the weaknesses of vacuum tubes over transistors. Topologies suggested by Linvill were the voltage-inversion type NICs, yet there are also current-inversion types in the literature proposed by Yanagisawa [6] and Larky [7]. Including topologies of Linvill, Larky and

Yanagisawa, all known transistor NICs are catalogued well in [24]. However, very few of them were built as successfully stabilized prototypes which proves the inherent stability problems of the negative impedance converters. As the review of NICs continues, the meanings of voltage-inversion type and current-inversion type will be explained throughout the section.

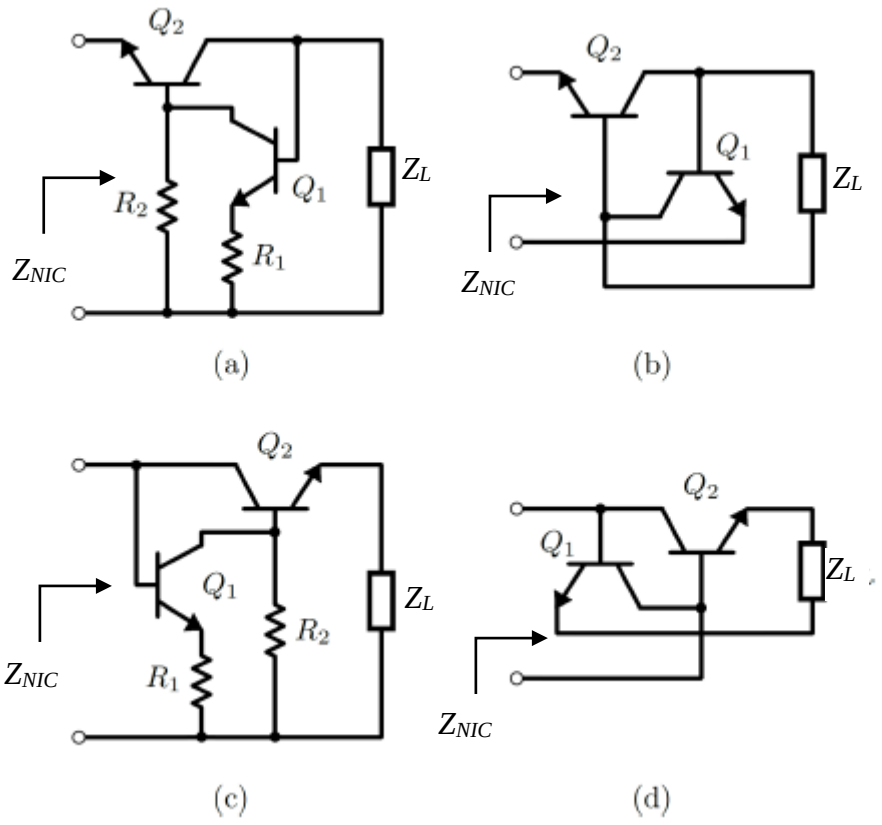

Figure 2.7. Linvill's ideal NICs [12] (a) Grounded OCS NIC circuit (b) Floating OCS NIC circuit (c) Grounded SCS NIC circuit (d) Floating SCS NIC circuit

It is comprehensible to approach the NIC circuits with a general two-port representation before diving into the implementations with electrical components. Figure 2.8 shows a general hybrid parameter equivalent of a two-port network.

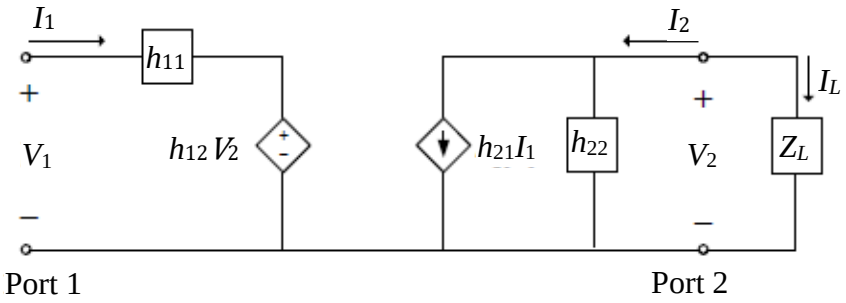

Figure 2.8. h-parameter representation of a two-port network with an arbitrary load (Z_L) [21]

Port equations in terms of voltages and currents can be written as follows:

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{2.10}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{2.11}$$

where,

$$h_{11} = \frac{V_1}{I_1}\Big|_{V_2=0},\ h_{12} = \frac{V_1}{V_2}\Big|_{I_1=0},\ h_{21} = \frac{I_2}{I_1}\Big|_{V_2=0} \text{ and } h_{22} = \frac{I_2}{V_2}\Big|_{I_1=0}.$$

Eq. 2.11 can be manipulated using the relation $I_2 = -V_2/Z_L$ to write V_2 in terms of I_1 as in Eq. 2.12.

$$V_2 = -\frac{h_{21}Z_L I_1}{h_{22}Z_L + 1} \tag{2.12}$$

Combining Eq. 2.10 and Eq. 2.12, the relation between input impedance, $Z_{in} = V_1/I_1$, and load impedance, Z_L, in terms of hybrid parameters is obtained and given in Eq. 2.13.

$$Z_{in} = h_{11} - \frac{h_{12}h_{21}Z_L}{h_{22}Z_L + 1} \tag{2.13}$$

From Eq. 2.13, it can be deduced that for certain values of h parameters, the ideal NIC behavior can be achieved. For instance, to get a negative impedance converter with a

conversion coefficient k, h_{11} and h_{22} must be equal to zero and product $h_{12}h_{21}$ must be equal to k.

So, the input impedance, $Z_{in} = -kZ_L$, is achieved. In order to get a negative impedance, the conversion coefficient k must be a positive value. Therefore, the terms in product, $h_{12}h_{21}$, cannot have opposite signs. In other words, both h_{12} and h_{21} can be either positive or negative. Depending on the sign of them, the configuration of NIC is current-inversion type or voltage-inversion type. The first case, which both h_{12} and h_{21} are positive and unity, is called as current-inversion type. In this case, the port equations of the ideal two-port network in Figure 2.8 can be written as $V_1 = V_2$ and $I_1 = I_2$. Therefore, the current I_L flowing through the load is equal to the negative of current I_1. So, input impedance Z_{in} at port 1 can be written as in Eq.2.14.

$$Z_{in} = \frac{V_1}{I_1} = \frac{-I_1 Z_L}{I_1} = -Z_L \tag{2.14}$$

A unity negative impedance conversion is obtained by making the voltages equal across the load and port 1, while currents are flowing in opposite directions. Hence, for a current inversion type NIC, h parameters of the network can be expressed by the matrix defined in Eq. 2.15.

$$\mathrm{h} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{2.15}$$

Larky's negative impedance converter depicted in Figure 2.9 can be shown as an example of current inversion type [7]. It is stated in his work that when port 2 is terminated with a load Z_L, the input impedance seen from port 1 can be approximated by the relation given in Eq. 2.16.

$$Z_{in} = -\frac{R_1}{R_2} Z_L \tag{2.16}$$

The second case, which both h_{12} and h_{21} are negative and unity, is called as voltage inversion type. In this case, the port equations of the ideal two-port network can be

written as $V_1 = -V_2$ and $I_1 = -I_2$. As a result, the current I_L flowing through the load

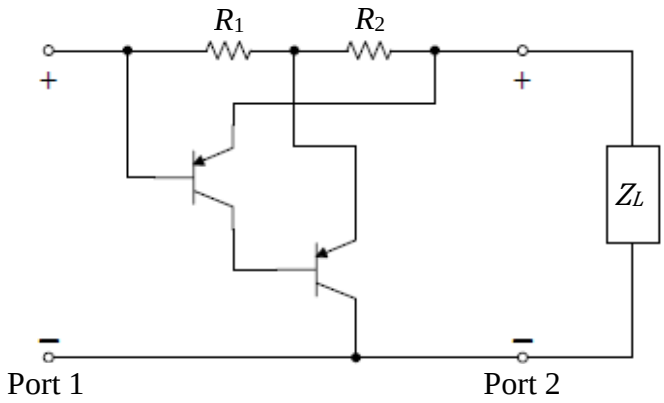

Figure 2.9. Larky's current inversion NIC circuit [7]

is in the same direction with the current I_1 flowing into port 1. Hence, the input impedance looking into port 1 can be can be calculated as in Eq. 2.17.

$$Z_{in} = \frac{V_1}{I_1} = \frac{-I_L Z_L}{I_L} = -Z_L \tag{2.17}$$

A unity negative impedance conversion is obtained by making the voltage across the load Z_L opposite with the voltage across port 1, while currents flowing into port 1 and load are in the same direction. This type of NICs are called voltage-inversion type. Two port hybrid parameters of voltage-inversion type NICs are then expressed as in Eq. 2.18.

$$\mathrm{h} = \begin{pmatrix} 0 & -1 \\ -1 & 0 \end{pmatrix} \tag{2.18}$$

Having covered the ideal two-port representation of NICs, a detailed analysis also must be done on the circuits to understand dynamics of NICs and to implement it at the end. In terminology, if one side of the load of an NIC is connected to ground, it is

called grounded or unbalanced NIC. If any side of the load of an NIC is not connected to ground, then it is called floating or balanced NIC. In Figure 2.10, Linvill's floating

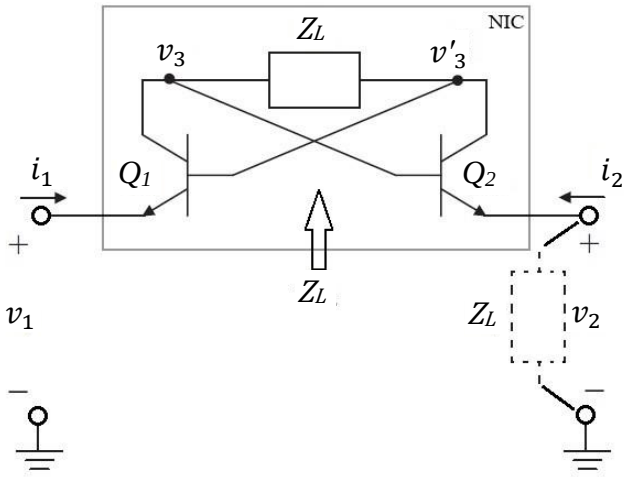

Figure 2.10. Linvill's floating OCS NIC circuit with a hypothetical load

OCS NIC topology, which is comprised of two back to back bipolar junction transistor (BJT), is depicted with a load Z_L to be inverted. Note that the biasing circuit is excluded for the sake of simplicity.

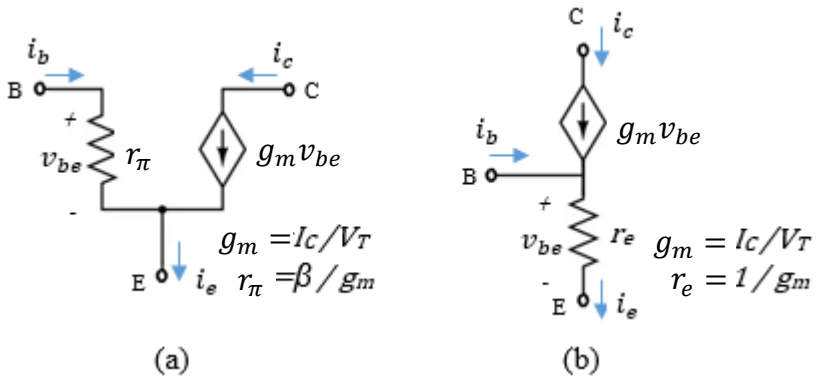

Figure 2.11. Small signal models of a BJT. (a) hybrid-π model (b)T model [25]

If another load is connected to v_2 port with same value of the original load, the impedance looking into v_1 port must be equal to zero if NIC operates the way it is supposed to work. To analyze the operation of the circuit, small signal models of the transistors are used. Small signal T and hybrid-π models of a bipolar junction transistor are given in Figure 2.11, where small signal parameters g_m, r_π and r_e are calculated from DC operating points.

When the transistors Q_1 and Q_2 are replaced by small signal T model equivalent, the topology given in Figure 2.10 transforms to the circuit given in Figure 2.12.

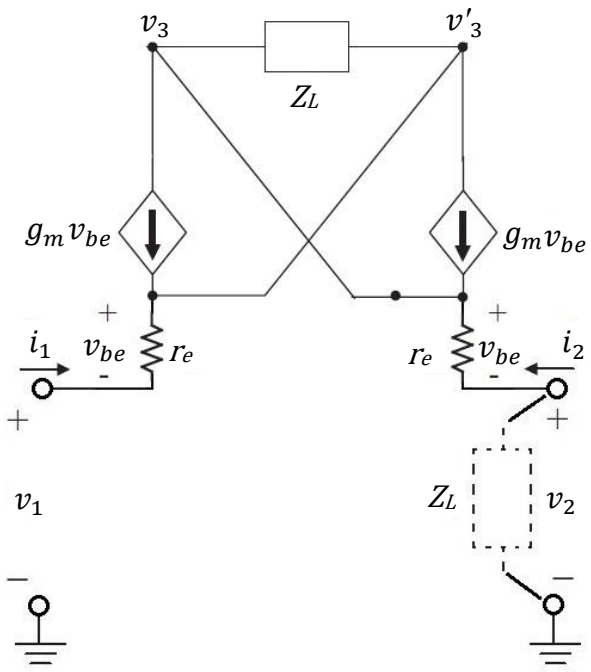

Figure 2.12. Small signal equivalent of Linvill's floating NIC topology

The equations defining the circuit can be written for the nodes v_1, v_2, v_3 and v'_3 as in Eq. 2.19 to Eq. 2.22. The equations are written assuming that the transistors are

identical and their DC operating points are same. So, the small signal parameters g_m, r_π and r_e are same for both transistors.

$$\frac{v_1}{r_e} - \frac{v'_3}{r_e} = i_1 \tag{2.19}$$

$$\frac{v_3}{r_e} - \left(\frac{1}{r_e} + \frac{1}{Z_L}\right) v_2 = 0 \tag{2.20}$$

$$\left(\frac{1}{r_e} - g_m\right) v_1 + g_m v_2 + \left(\frac{1}{Z_L} - g_m\right) v_3 + \left(g_m - \frac{1}{r_e} - \frac{1}{Z_L}\right) v'_3 = 0 \tag{2.21}$$

$$g_m v_1 + \left(\frac{1}{r_e} - g_m\right) v_2 - \left(\frac{1}{r_e} + \frac{1}{Z_L} - g_m\right) v_3 - \left(g_m - \frac{1}{Z_L}\right) v'_3 = 0 \tag{2.22}$$

If the equation set Eq. 2.19 to Eq. 2.22 are solved for $Z_{in} = \frac{v_1}{i_1}$, the relation in Eq. 2.23 is obtained.

$$Z_{in} = 2g_m r_e Z_L - 2Z_L - 2r_e \tag{2.23}$$

For BJTs with a high transconductance g_m, the small signal parameter r_e can be written as $g_m = 1/r_e$ [26]. Hence, for an ideal transistor with infinite transconductance, the impedance looking into v_1 port is equal to zero as expected.

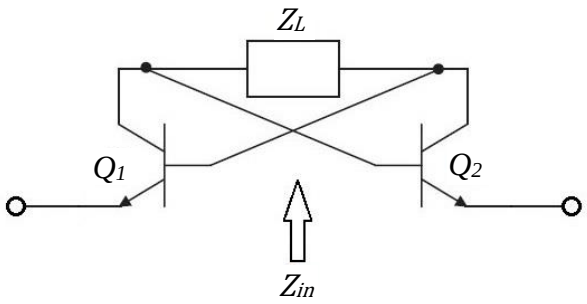

Figure 2.13. Linvill's floating NIC circuit (Standalone case)

In [21], another hybrid-π small signal analysis is conducted for Linvill's floating OCS NIC for a standalone case depicted in Figure 2.13. In this case, the input impedance

looking into the emitter terminals of the transistors is found to be $Z_{in} = -Z_L + 2/g_m$. Eventually, with the assumption of an ideal transistor with an infinite transconductance g_m, the NIC will give the negative of the load Z_L between its emitter terminals.

2.2.2. A REVIEW OF NON-FOSTER MATCHING LITERATURE

Previous research on non-Foster impedance matching networks for electrically small antennas is summarized well in [8] and [27]. The first practical work on non-Foster matching of small antennas was published by Harris and Myers in 1968 [20]. An amplifier based NIC, which is depicted in Figure 2.14, was built and measured with short monopole antennas. The relation between input voltage (V_1) and input current (I_1) can be written as in Eq. 2.24.

$$V_1 = A_v V_1 + I_1 Z_L \tag{2.24}$$

The input impedance (Z_{in}) is then calculated by Eq. 2.25. With a voltage gain of 2, the impedance seen from the input terminals of the amplifier is found to be $-Z_L$.

$$Z_{in} = \frac{Z_L}{1 - A_v} \tag{2.25}$$

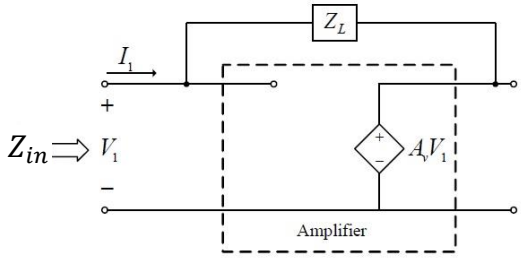

Figure 2.14. Amplifier Based NIC [10]

Two test antennas were used in that work, one of which is 2.5″ monopole with 2.5″ diameter top hat, and the other is 10″ monopole with 10″ diameter top hat. The gains of test antennas are compared to the case of unmatched 16-foot whip antenna. They managed to get 2 dB to 10 dB improvement on the gain of the test antennas between 0.5 MHz and 10 MHz.

They also discussed noise effect on the circuit performance. It is stated that external noise is the primary noise source on the circuit rather than circuit itself. Besides that, non-linear behavior of the circuit was examined by applying different power levels to test antennas. It is revealed that as the power received by the test antenna increases, the linearity of the non-Foster circuit starts to deteriorate. Although some experiments are made on the linearity of the circuit, there was not enough cases to determine dynamic range of the operation [21]. One more conclusion drawn from the work was that the performance of the antenna at high frequencies is limited by the maximum frequency at which the NIC can provide a negligible phase shift.

After the first work presented by Harris and Myers, three non-Foster impedance matching networks were presented by Perry in 1973 [28]. In this work, non-Foster matching networks were implemented for 3″ height monopole antenna, and the antenna gain was compared to unmatched 16-foot whip antenna. As a result, 10 dB to 30 dB gain improvement was shown between 0.3 MHz and 2.5 MHz.

One of the matching networks presented by Perry was the same topology that Harris used. As a reminder, an amplifier based NIC was used in that topology. At the end, a negative impedance was obtained from the input terminals of the amplifier by means of a voltage gain of two. The second topology fabricated by Perry was comprised of two cascaded operational amplifiers given in Figure 2.15. Like the first topology, the aim was to provide the negative version of load impedance (Z_L) from V_1 port by adjusting the voltage gain to two. Since both operational amplifiers (emphasized in red box) are cascaded inverting amplifiers, the voltage gain between V_2 port and V_1 port can be written as in Eq. 2.26.

$$\frac{V_2}{V_1} = \frac{\sqrt{2}R}{R} x \frac{\sqrt{2}R}{R} = 2 \tag{2.26}$$

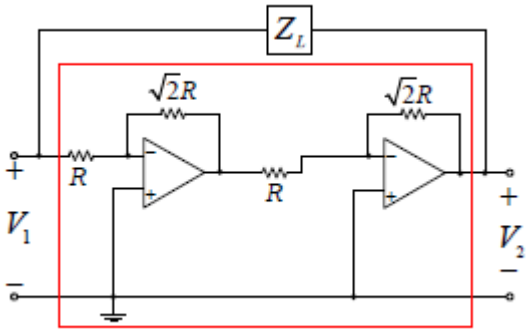

Figure 2.15. Negative impedance converter based on cascaded operational amplifiers [28]

Third and the last topology designed by Perry is based on a two-transistor NIC. The topology is shown in Figure 2.16. If a simple small signal analysis is carried out with T-models, Z_{in} can be derived as in Eq. 2.27 with the assumptions of g_m >>1 and r_e >>1.

$$Z_{in} = -\frac{R_1}{R_2} Z_{in} \tag{2.27}$$

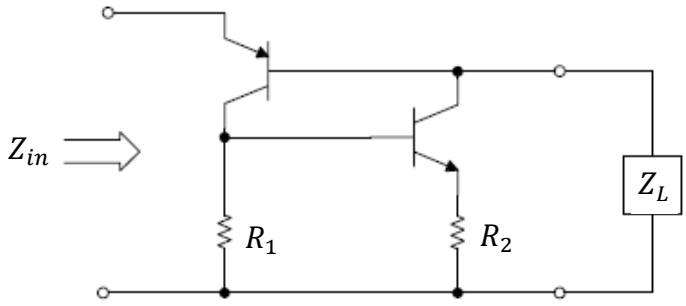

Figure 2.16. Negative impedance converter based on two transistors [28]

Perry obtained excellent results regarding the improvement of antenna gain (up to 35 dB relative to the unmatched whip). However, his work is valid up to 5 MHz. Besides that, there were no measurement on the noise performance of the circuit.

Both Harris and Perry could not achieve a matching performance beyond a few MHz. The reason why they are limited to a few MHz is that a parallel combination of a resistor and a capacitor is used as the equivalent antenna model which is only valid for low frequencies [21].

Shakill et. al [29], in 2000, provided a non-Foster impedance matching topology based on an NIC comprised of FET transistors in their patent. In addition to reactance compensation, he provided an inductive T-dualizer type transformer to match the frequency dependent radiation resistance to a constant value for a short dipole.

Another valuable contributor to the non-Foster matching literature is Sussman-Fort by his work in 2009 [8], also summarizing his previous works [27, 30-32]. In this work, a 6″ monopole and a 12″ dipole antennas were the test antennas to be matched with non-Foster matching circuits. The measurements were given comparatively with no matching case and passively matched cases. The matching circuit of Sussman-Fort is different from the previous authors in terms of connection type to the antenna. As opposed to parallel connections utilized by previous works, he inserted the generated

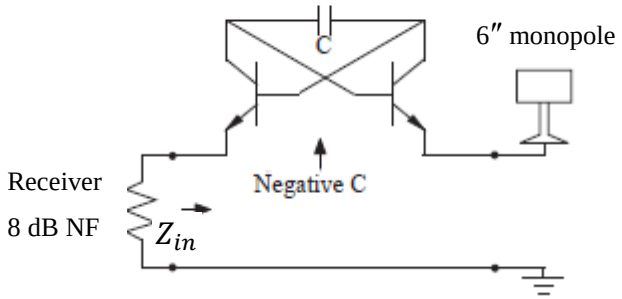

Figure 2.17. Sussman-Fort's series non-Foster matching configuration for 6″ monopole [8]

negative impedances as a series floating element, as depicted in Figure 2.17. By means of serial implementation, 10 dB to 25 dB gain improvement is obtained between 20 MHz and 100 MHz unlike the studies of Harris and Myers which is confined in a bandwidth of a few MHz.

Sussman-Fort used Linvill's floating NICs to realize signal-to-noise ratio (SNR) improvement, when compared to no matching, for receive cases from 20 MHz to 120 MHz. As a result, SNR improvement up to 9 dB was achieved for 6″ monopole. Other than 6″ monopole, a non-Foster matched 12″ dipole antenna is also measured over a 12″ lossy-matched blade antenna as given in Figure 2.18. In this case, an SNR improvement of 10 dB and more is reported over blade antenna from 33 MHz to 63 MHz. Further studies on dipoles was conducted by Sussman-Fort, reporting that the non-Foster matched frequency range is extended in between 60 MHz and 400 MHz [27]. Despite the fact that the measurement results are shown, stabilization of a non-Foster matching network is never investigated in detail in his previous works [8,27,30-32].

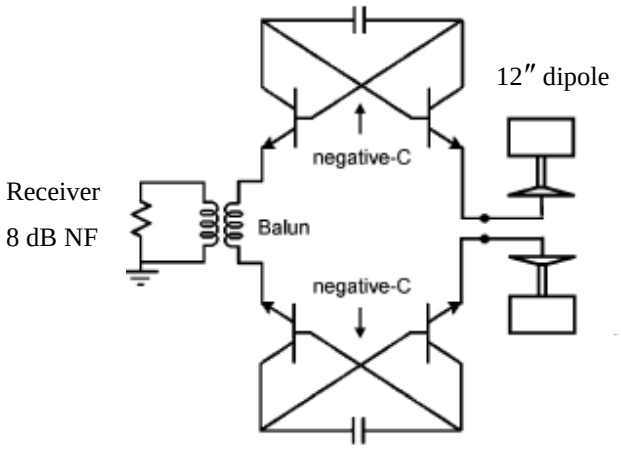

Figure 2.18. Sussman-Fort's series non-Foster matching configuration for 12″ dipole [8]

Another exceptional contribution was made to non-Foster matching literature by O. Tade et al. in 2013 [33]. A chassis antenna with a base of 50 mm x 50 mm is loaded

with a non-Foster matching circuit, and operation bandwidth was reported in between 695 MHz and 1.5 GHz with a return loss of better than 10 dB. Together with broadband operation, a dedicated stability analysis is conducted resulting in a stable operation that reaches up to 1.5 GHz. Carefully designed feedback loops and symmetry in component placements are the key factors of such broadband operation according to [34].

M.M. Jacob, in 2016, concentrated on advantages and practical limitations of high-performance antennas matched with non-Foster matching networks [23]. In this work, a parasitic array was loaded with non-Foster matching network to reduce phase dispersion and to obtain squint-free patterns. It was reported that 10-15% squint free bandwidth enhancement is obtained when compared to passive matched parasitic array. In addition to squint-free bandwidth enhancement, it is stated in this work that a steerable radiation patterns can be achieved by means of tunable negative impedances obtained via an NIC and a varactor.

Nagarkoti, in his works [14, 35, 36], designed non-Foster circuits using three different NIC topology which are based on graphene field effect transistor (GFET), BJT and resonant tunneling diodes (RTD). In BJT based design, a floating negative capacitance NIC configuration is used to match a small planar monopole. It is shown that the measurement results are in a well agreement with the simulation results up to 1 GHz. Other designs which are comprised of RTDs and GFETs are used to obtain a capacitive - inductive compensation for small monopoles. Measured results of RTD-based and GFET-based non-Foster matching circuits are presented. It is shown that the results agreed well with simulations up to 2 GHz. Besides all these work, noise performance of the circuit for BJT-based case was also investigated. It is revealed that the dominating source of noise is coming from the shot noise of transistors. In other words, it makes the biggest contribution to the noise figure of non-Foster circuit. Hence, system performance degrades due to the added noise, especially in receive mode.

2.2.3. NON-FOSTER MATCHING NETWORK DESIGN WITH IDEAL NIC

Negative impedances generated by NICs can be used to cancel out the large capacitive reactance of electrically small monopole antennas in matching circuits. Even so, the removal of the reactance may not be enough for a good matching since the radiation resistance of a small antenna is small too. Hence, in addition to removal of the reactance, it is necessary to provide a matching between the antenna radiation resistance and the system impedance. A general diagram of a whole ideal matching circuitry including the antenna and additional circuit blocks is given in Figure 2.19 and will be explained in detail in this section.

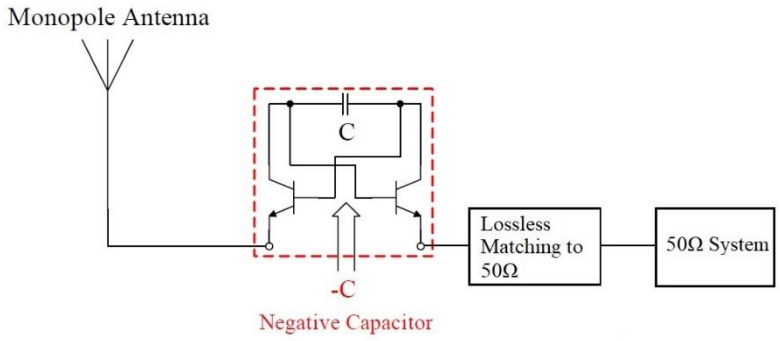

Figure 2.19. Block diagram of matching circuitry

In Figure 2.19, an electrically small monopole is matched to a 50Ω system using Linvill's floating OCS NIC as a negative capacitance generator. Series inclusion of a negative capacitor cancels the capacitive reactance of the monopole and leaves a radiation resistance which is proportional to the square of frequency. After that, the frequency dependent radiation resistance of monopole is matched to 50Ω system with a lossless matching circuitry. An inductive-T dualizer depicted in Figure 2.20 can be used to transform frequency-squared-dependent radiation resistance to a constant 50Ω

[8]. Eq. 2.9 can be written as in Eq. 2.28 using the relation $\lambda = c/f$, where λ is wavelength, c is the speed of light and f is the frequency.

$$R_{rad} = 40\frac{\pi^2 L^2}{c^2} f^2 \tag{2.28}$$

Hence, the radiation resistance can be defined as $R_{rad} = Kf^2$ where $K = 40\pi^2 L^2/c^2$ is a constant.

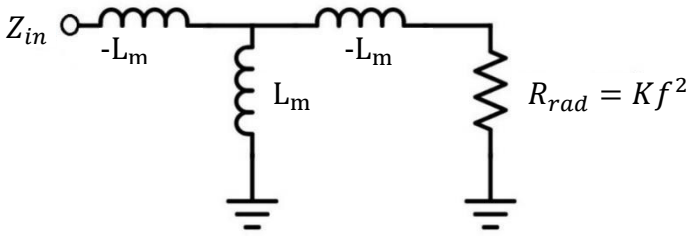

Figure 2.20. Inductive-T Dualizer [8]

The operation of the inductive-T dualizer, depicted in Figure 2.20, can be understood by defining and calculating the input impedance, Z_{in}. Z_{in} is written in terms of the component values in Eq. 2.29, where L_m is inductance of the inductors and ω is the frequency in rad/s.

$$Z_{in} = \left(\frac{(R_{rad} - j\omega L_m)j\omega L_m}{R_{rad}}\right) - j\omega L_m \tag{2.29}$$

Simplifying the Eq. 2.29, Z_{in} is obtained in a simpler form as in Eq. 2.30.

$$Z_{in} = \frac{\omega^2 L_m^2}{R_{rad}} \tag{2.30}$$

One last step is carried out to clarify how the radiation resistance transforms into a frequency independent constant value. As mentioned before, radiation resistance R_{rad}

can be written as $R_{rad} = Kf^2$. Eq. 2.30 is manipulated using the relations $R_{rad} = Kf^2$ and $\omega = 2\pi f$ and Z_{in} is derived as in Eq. 2.31.

$$Z_{in} = \frac{4\pi^2 \mathrm{L}_\mathrm{m}^2}{K} \tag{2.31}$$

Hence, it is inferred from Eq. 2.31 that Z_{in} can be adjusted to a required constant value by implementing an appropriate inductance value. The design in Figure 2.21 finalizes the ideal matching diagram. So, Z_{in1} is equal to sum of radiation resistance and antenna reactance and can be written as $Z_{in1} = R_{rad} + jX_{ant}$. Series inclusion of a negative capacitor to the antenna removes the reactive part of the antenna impedance. So, $Z_{in2} = R_{rad}$ relation holds. Finally, with an appropriate choice of inductors, radiation resistance is transformed to a constant $Z_{in} = 50\Omega$.

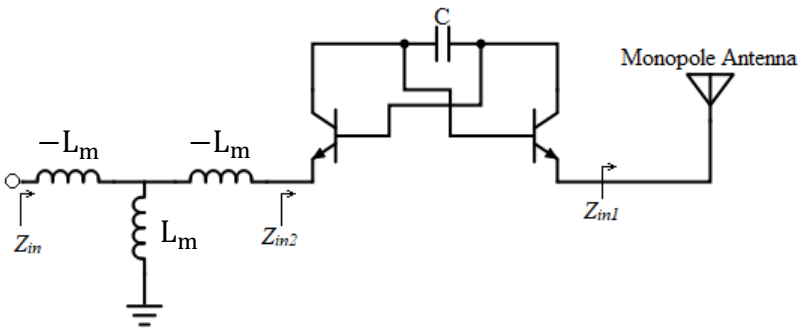

Figure 2.21. Combination of NIC and inductive T-dualizer

2.2.3.1. ANALYSIS OF IDEAL NON-FOSTER MATCHING CIRCUIT

It is preferred to approach the problem with ideal conditions to make a proof of concept, before implementing the matching circuitry with practical simulation models of the circuit components. Based on the Linvill's floating OCS NIC configuration, the circuit in Figure 2.22 is simulated by using AWR MWO®.

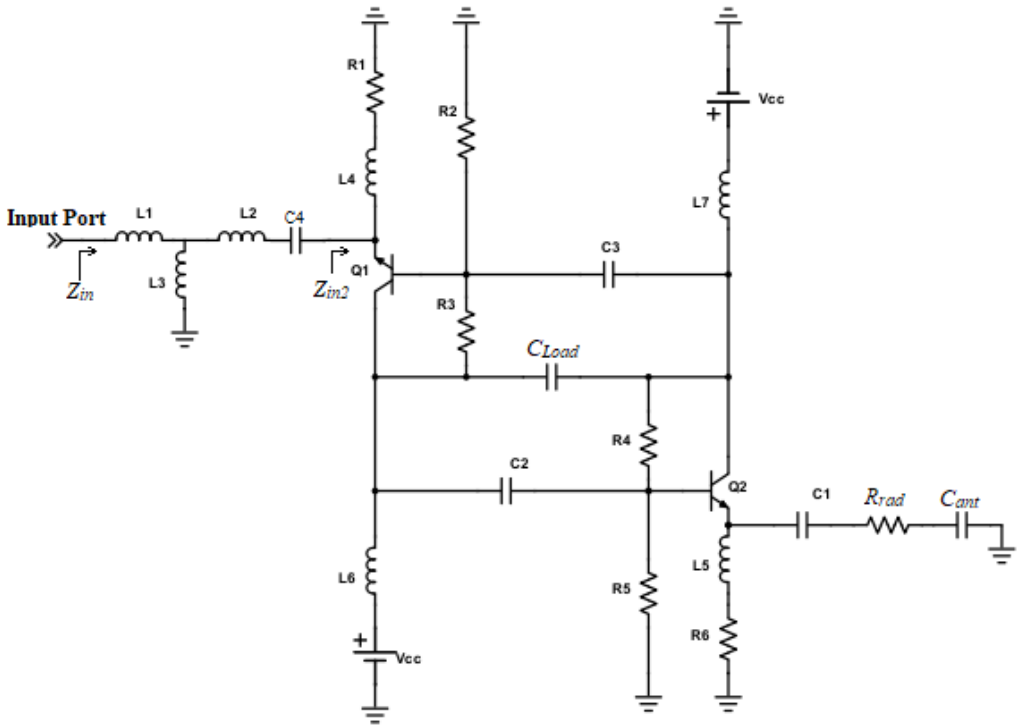

Figure 2.22. Schematic of Ideal Matching Circuitry

A monopole antenna with 10 cm length and 0.75 cm radius is modelled as a series combination of a capacitor (C_{ant}) and resistor (R_{rad}) based on the Eq. 2.8 and Eq. 2.9. The bill of materials of the circuit is given in Table 2.1.

C_{Load} is chosen equal to the capacitance of antenna model, that is, 3.5 pF. In section 2.2.1, it is stated that the transconductance g_m of the transistors affect the inversion performance. Higher transconductance means the better inversion performance of the NIC. So, the g_m parameters of the transistors are set to infinity, and all parasitic effects of the transistors are neglected. Figure 2.23 shows antenna reactance without any matching and the reactance of Z_{in2} after the inclusion of capacitive loaded NIC.

Table 2.1. *Bill of Materials (Ideal NIC)*

Component	Value	Description
R1, R6	50 Ω	Biasing
R2, R5	20 kΩ	Biasing
R3, R4	20 kΩ	Biasing
L1, L2	-7.47 nH	Inductive T- Dualizer
L3	7.47 nH	Inductive T- Dualizer
L4, L5, L6, L7	1 H	RF Choke
Q1, Q2	-	Transistor
C_{Load}	3.5 pF	Load Capacitor to be Inverted
C1, C2, C3, C4	10 uF	DC Blocking Capacitor

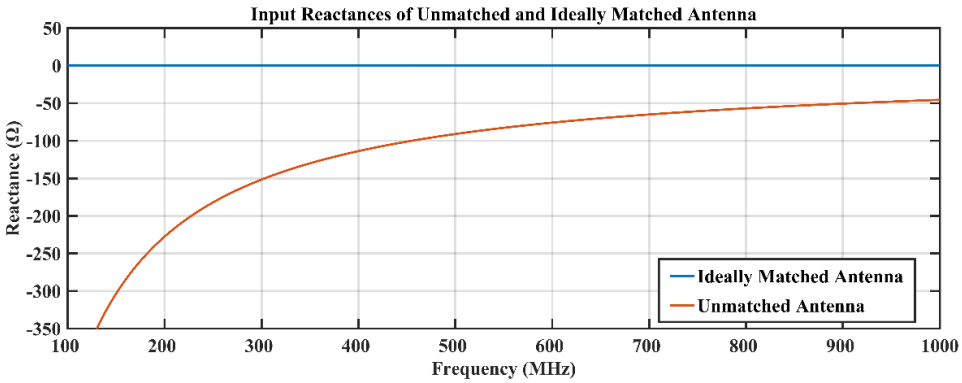

Figure 2.23. Reactance of antenna model and Z_{in2}

As seen from Figure 2.23, the NIC functions as an ideal impedance converter canceling the capacitive reactance of antenna. Besides canceling the reactance of antenna, it is crucial to match the remaining antenna radiation resistance while implementing the NIC. Figure 2.24 shows the resistive part of Z_{in2} after the inclusion of NIC.

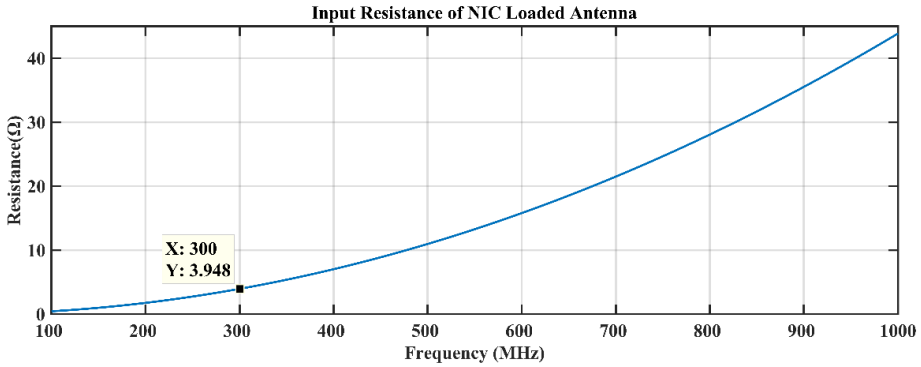

Figure 2.24. Input Resistance of NIC Loaded Antenna, Z_{in2}

As seen from Figure 2.24, the remaining resistance increases with square of the frequency. This resistance is ideally matched to constant 50 Ω by implementing an inductive T-dualizer as proposed earlier. It is easy to calculate the necessary inductance value by finding the constant K and substituting it in Eq 2.31. The constant K is found to be $0.44x10^{-16}$ from the relation $K = 40\pi^2L^2/c^2$. Finally, substituting it in Eq. 2.31, Eq. 2.32 remains to be solved for inductance L_m which is found to be 7.47 nH.

$$Z_{in} = \frac{4\pi^2 \mathrm{L_m}^2}{0.441x10^{-16}} = 50\Omega \tag{2.32}$$

Having determined all the necessary components for matching, the ideal NIC circuit is simulated. Figure 2.25 shows the real and imaginary parts of input impedance Z_{in}. It is seen from the graph that the real part of input impedance is set to 50 Ω while the imaginary part of it is set to zero as desired.

Another figure of merit in impedance matching theory is reflection coefficient, S_{11}. S_{11} is usually stated in dB and defined as the logarithm of ratio of reflected power (P_r) to the incident power (P_i). The formulation of $S_{11,dB}$ is given in Eq. 2.33.

$$S_{11,dB} = 10\log_{10}\left(\frac{P_r}{P_i}\right) \tag{2.33}$$

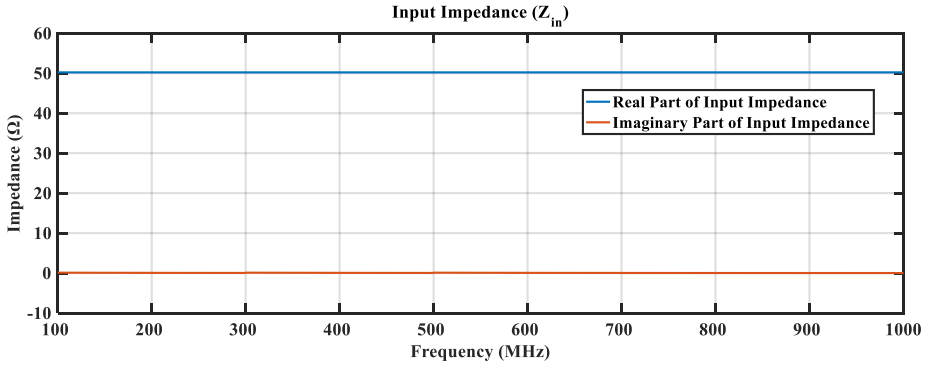

Figure 2.25. Imaginary and Real Parts of Input Impedance, Zin

For the ideal NIC configuration, $S_{11,dB}$ is simulated and plotted in Figure 2.26. In the ideal case, return loss better than 50 dB is obtained over 100 MHz – 1 GHz band.

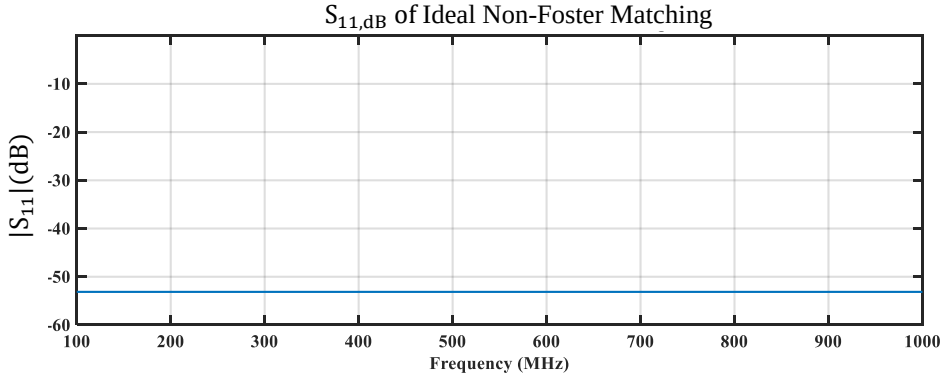

Figure 2.26. Ideal Non-Foster Matching, $S_{11,dB}$

Having obtained the ideal behavior of the NIC circuitry, it is logical to investigate the effects of transistor parameters to the circuit. By doing so, the transistor selection and settling DC operating point of it will be an easier task.

2.2.3.2. EFFECTS OF TRANSISTOR PARAMETERS

- **Effect of Collector-Base Capacitance**

Examining the small signal equivalent of the NIC helps to have a solid understanding about which parameters can be effective on circuit response. In Figure 2.12, a small signal model of Linvill's floating NIC is given. If the circuit is examined closely, it is observed that the collector-base capacitances of the transistors remain parallel to the load by means of cross coupled branches as given in Figure 2.27. Hence, they add up to the load capacitance and changes the circuit behavior.

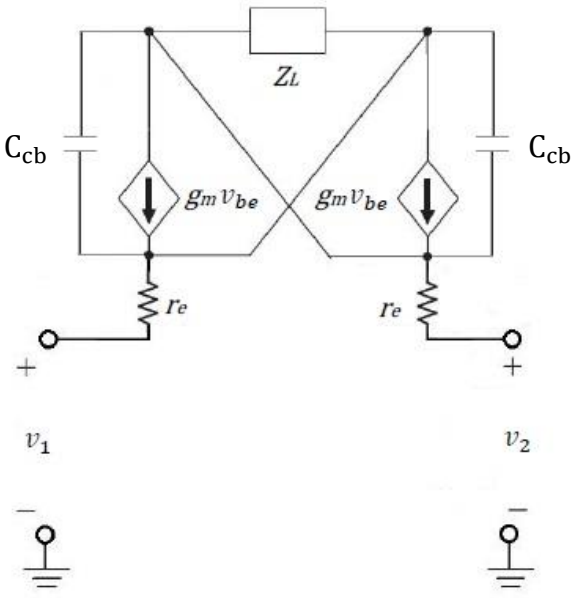

Figure 2.27. Small signal equivalent of Linvill's floating NIC topology with C_{cb}

In Figure 2.28, the imaginary impedance seen from the circuit is plotted for various values of collector-base capacitance. If the collector-base capacitances of transistors

are set to zero, the input reactance is equal to zero over the frequency band. As the collector-base capacitances are increasing, they add up to the load capacitor and deteriorates the circuit response.

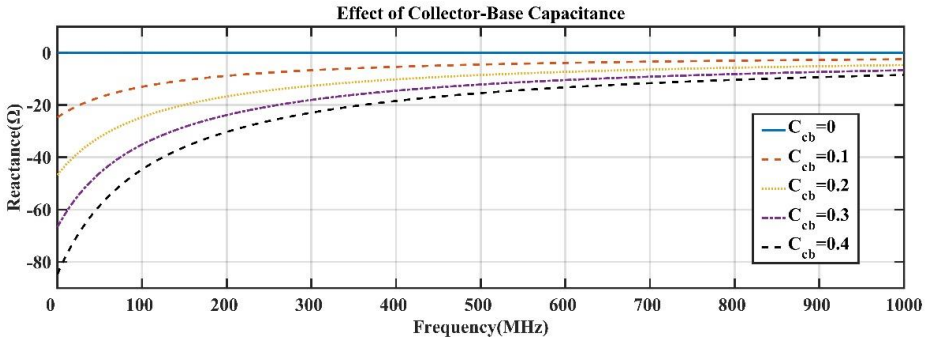

Figure 2.28. Imaginary Part of Input Impedance with Swept Collector-Base Capacitance

Although such a precise design consideration is hard to achieve in practical circuits, it is beneficial to keep in my mind that the variation of collector-base capacitance of the selected transistor must not be too wide within the frequency range of operation.

One more aspect to take notice is that if the total of collector-base capacitances of transistors exceeds the negative capacitance required for the application, overcompensation will occur, and required negative capacitance will not be achieved. In other words, the capacitance to be inverted must be smaller than the total of two collector-base capacitances.

- **Effect of small signal emitter resistance**

In Figure 2.22, the schematic of ideal matching circuitry shows that both RF input port and antenna port are connected to emitter terminals of the transistors. This topology suggests that both ports see a small signal emitter resistance looking into the emitter

terminals of the transistors. These resistances are connected in series to the antenna impedance. So, some of the RF energy is dissipated on small signal emitter resistances. Figure 2.29 gives the real part of the impedance seen from input port excluding the inductive T-dualizer. Inductive T-dualizer is excluded in simulation to see the effect of small signal emitter resistances more clearly.

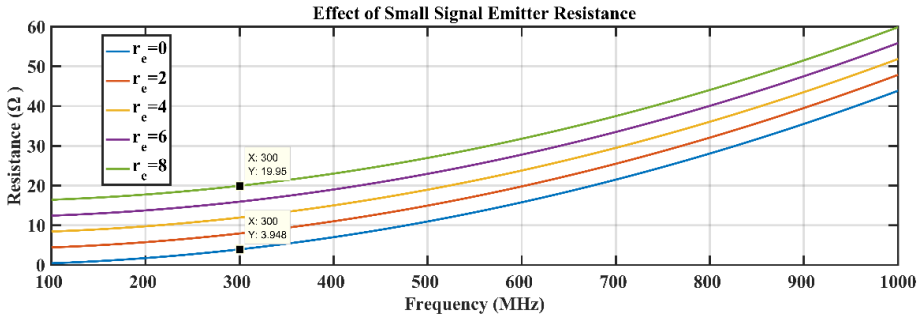

Figure 2.29. Real Part of Input Impedance with Swept Small Signal Emitter Resistance

In Figure 2.29, the sample point is taken as 300 MHz. If the data cursors on upper and bottom lines are examined, 16 Ω difference can be seen. This difference is the result of 8 Ω small signal emitter resistance per transistor. The formula for small signal emitter resistance is given in section 2.2.1 as $r_e = V_T/I_E$ where V_T=26 mV is thermal voltage constant and I_E is the emitter current. Hence, the emitter current may be adjusted to a reasonably high value within the maximum ratings of the transistor to minimize the effect of r_e. For instance, if an emitter current of 26 mA is set as DC operating point, small signal emitter resistance will be 1 Ω which can be neglected in a 50 Ω RF system. On the other hand, increasing the emitter current will increase the power consumption and heat generation. Thus, the choice of emitter current can be decided depending on the application.

In this section, effects of collector-base capacitances and small signal emitter resistances of transistors are investigated with simulations. Keeping those effects and

the design of ideal non-Foster matching network in mind, it is logical to move on with practical design scheme.

CHAPTER 3

DESIGN OF PRACTICAL NON-FOSTER IMPEDANCE MATCHING NETWORK

3.1. DESIGN APPROACH

Spice models of components are used to make simulations of electronic circuits closer to practical ones. While ideal models do not consider parasitic and non-ideal effects of components, spice models are prepared by manufacturers including those effects as much as possible. There are spice models of various components and transistors of manufacturers in AWR MWO®. Other than circuit components, radiation resistance and capacitance of ESA was also calculated from idealized equations in previous chapter. If R_{rad} and C_{ant} are also replaced by real antenna parameters in simulation, the simulation results will be closer to the practical responses.

Stability is another aspect of design consideration. Once the overall circuitry is determined, the stability performance of the circuit should be investigated since NIC circuits are prone to instability due to the positive feedback loops present in the circuit. The stability of the NIC depends on many factors including the biasing points of the transistors, the configuration of layout, the passive loads to be converted and external loads connected to NIC [21]. With so many factors affecting the circuit behavior, it is beneficial to follow a systematic approach in design process. The diagram of design flow is given in Figure 3.1.

First, the input impedance and return loss of unmatched antenna which is used in practical work is given in this chapter. Second, the methods for analyzing stability of a non-Foster impedance matching network is examined. Finally, a non-Foster matching network is implemented with spice models in AWR Microwave Office® and

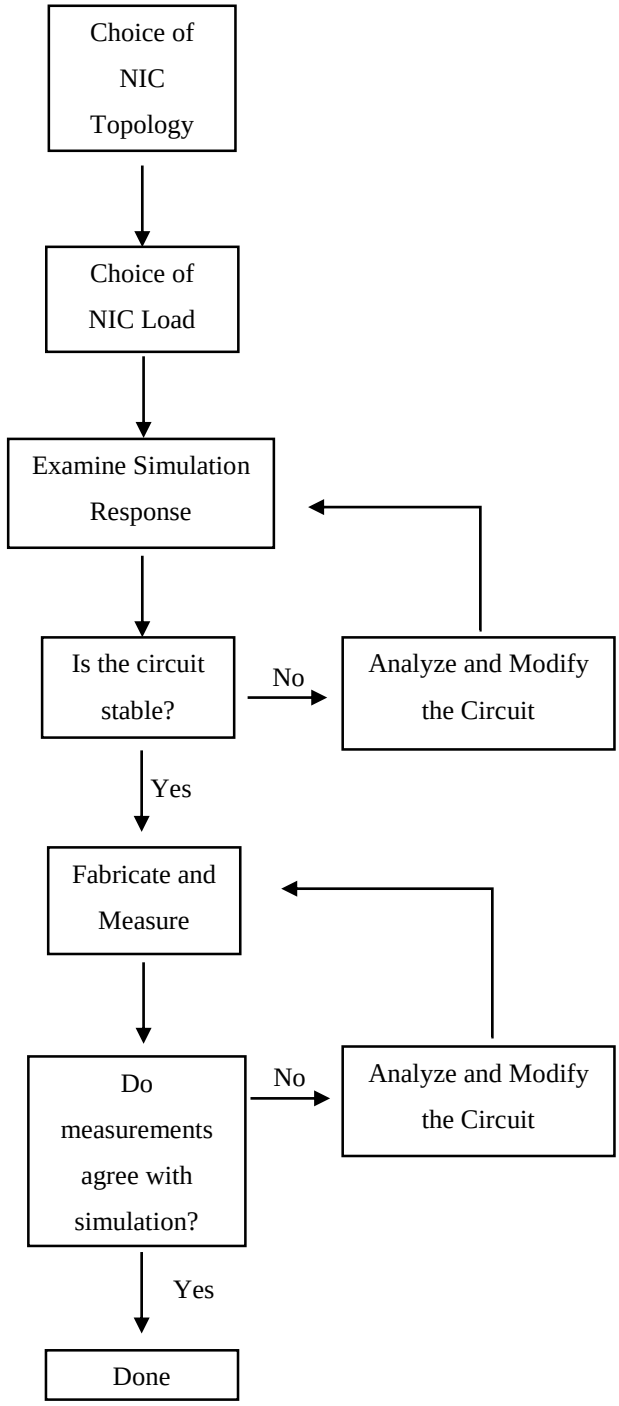

Figure 3.1. Design flow of non-Foster impedance matching circuit

simulation results for stability are presented. Simulation results which are related to matching performance of design is left to Chapter 4 in order to give comparative results with the measurement data.

3.2. ELECTRICALLY SMALL ANTENNA MEASUREMENTS

Input impedance of an antenna is defined as the impedance presented at its terminals according to IEEE Standard Definitions of Terms for Antennas [15]. The impedance characteristic of the ESA is the main factor in the design of NIC circuit. The load of NIC is chosen according to input reactance of the ESA to cancel out that reactance over a wide range of frequencies. It is proposed to design an inductive T-dualizer after cancelling out the reactance of ESA in chapter 2. The purpose of this design is to match the remaining ESA radiation resistance to 50 Ω. Like NIC circuit, the components of inductive T-dualizer are selected based on input resistance characteristic of ESA. Hence, the components of non-Foster impedance matching network are selected considering the input impedance characteristics of unmatched ESA. The photograph of ESA used in this thesis is given in Figure 3.2.

Figure 3.2. 10 cm-long monopole antenna

The ESA to be matched is a 10 cm-long monopole antenna with a 1 cm diameter. Main design criterion is to maintain a 5 dB $|S_{11}|$ bandwidth between 150 MHz and 500 MHz. The measurements of unmatched monopole antenna are taken using HP 8720D Vector Network Analyzer, which stores S_{11} data as a complex value, between 100 MHz and 1 GHz. Based on the measurements, $S_{11,\,dB}$ plot of unmatched monopole antenna is given in Figure 3.3. The trajectory of $S_{11,\,dB}$ shows that the unmatched antenna fails to achieve better than -2 dB matching until 800 MHz.

As mentioned earlier in this section, input impedance characteristic of unmatched antenna determines the load of negative impedance converter circuit. If the input reactance of the unmatched antenna is known, the negative of the same reactance can be employed by inverting the load of NIC. So, Eq 3.1 is used to calculate input impedance of unmatched antenna from S_{11} values, where $Z_0 = 50\ \Omega$ is the characteristic impedance of the system to be matched.

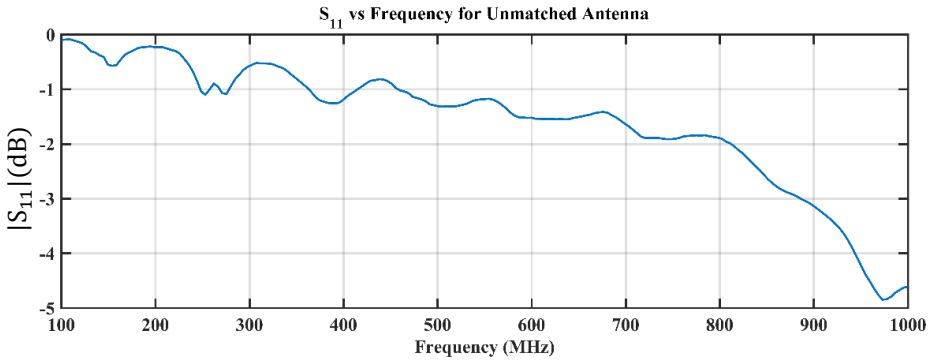

Figure 3.3. Measured $S_{11,\,dB}$ vs frequency for unmatched 10 cm-long monopole antenna

$$Z_{in} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{3.1}$$

Real part and imaginary parts of unmatched antenna input impedance are depicted in Figure 3.4. The blue line and red line show the real part and imaginary part of unmatched antenna, respectively. The unmatched antenna is modelled as an RLC

circuit according to input impedance curves to perform simulations for non-Foster matching in AWR MWO®.

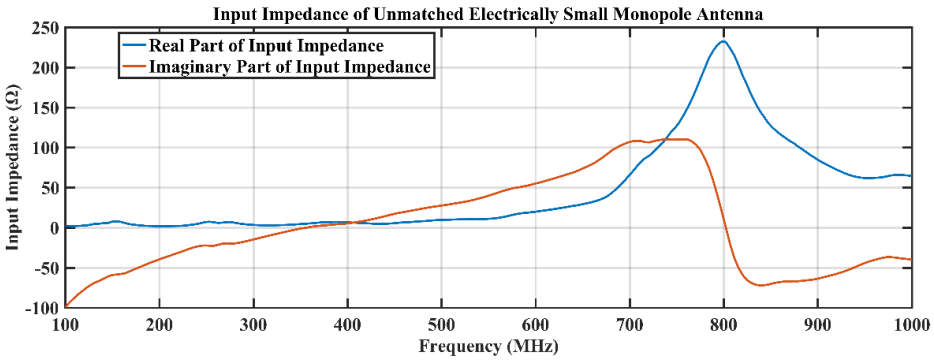

Figure 3.4. Measured input impedance for unmatched electrically small monopole antenna

The imaginary part of antenna impedance modeled as a series of an ideal inductor (L_{ant}) and an ideal capacitor (C_{ant}). The values of L_{ant} and C_{ant} is set to fit the antenna reactance curve. It is revealed that for C_{ant} = 14 pF and L_{ant} = 14 nH, the antenna reactance model is in agreement with measurement up to 478 MHz with a maximum deviation of 5 Ω. The reactance of series combination of C_{ant} and L_{ant} can be seen on same graph with measured antenna reactance in Figure 3.5. The red curve indicates the measured unmatched antenna reactance while the blue curve represents simulated LC model.

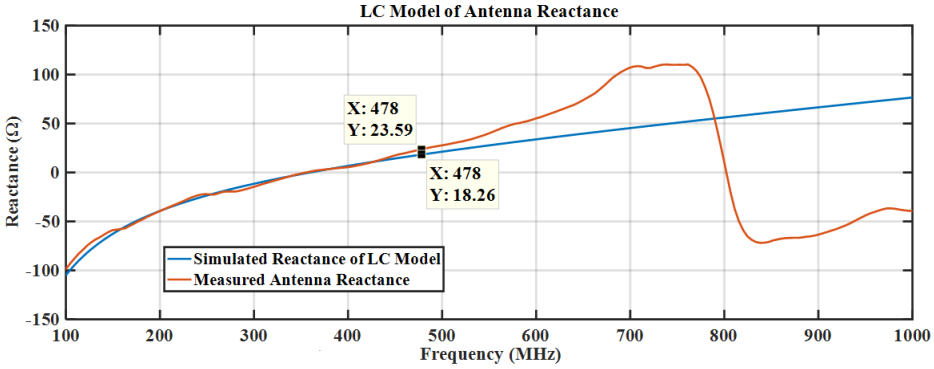

Figure 3.5. Comparison of reactance of simulated LC model and measured unmatched antenna

Then, the radiation resistance (R_{rad}) of unmatched antenna needs to be modeled for simulation. Since R_{rad} of unmatched antenna is a frequency dependent parameter, it is useful to model it with an equation to use in AWR MWO®. The curve fit function of MATLAB® is used to extract the equation for radiation resistance of unmatched antenna. The frequency dependent equation of R_{rad} is given in Eq 3.2, where f stands for frequency.

$$R_{rad} = 6.3x10^{-8}f^3 + 4.1x10^{-5}f^2 - 0.027f + 6.7 \quad (3.2)$$

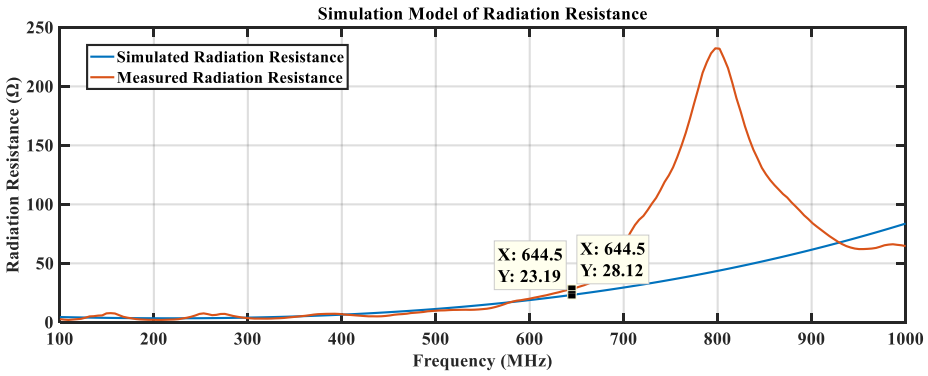

Figure 3.6. Comparison of radiation resistance of simulated model and measured unmatched antenna

The simulation model of R_{rad} and measured antenna radiation resistance is demonstrated in Figure 3.6. Blue line represents the simulation model of R_{rad} given by Eq. 3.2, and red line represents measured R_{rad} of unmatched antenna. Simulation model of R_{rad} is fitted well to the measured antenna radiation resistance data up to 644.5 MHz with a maximum deviation of 5 Ω.

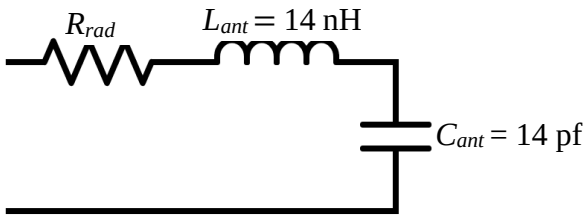

Figure 3.7. Equivalent RLC model of 10 cm monopole ESA with 1 cm diameter

Upon obtaining the antenna parameters for simulation, an RLC model of the electrically small monopole antenna is formed and given in Figure 3.7.

3.3. STABILITY OF NON-FOSTER MATCHING NETWORKS

BIBO Stability is a time domain property of linear time-invariant networks that every bounded input yields a bounded output as time approaches to infinity [37]. One of the biggest drawbacks associated with the use of non-Foster circuits, at microwave frequencies, is their inherent stability problems [38]. Therefore, it is crucial to utilize proper stability tests to detect a potential instability before building a circuit. There are various kinds of stability analysis for feedback networks in literature. Several papers are dealing with stability analysis of feedback networks based on Nyquist Criterion to check if the corresponding transfer function has any poles in the right half of the complex plane (RHP) [39-45]. Nyquist Criterion states that if any pole of closed loop transfer function of a feedback network lies in RHP, the network is unstable [46].

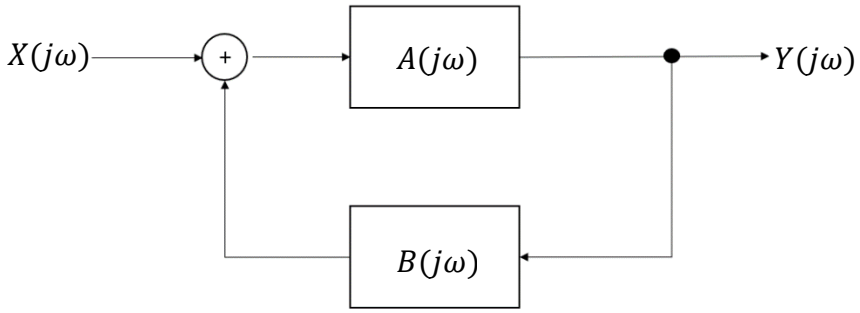

Figure 3.8. An illustration of a closed loop network

An example of a closed loop feedback network is given in Figure 3.8. The closed loop transfer function $H(j\omega)$ between input $X(j\omega)$ and output $Y(j\omega)$ can be written as:

$$H(j\omega) = \frac{A(j\omega)}{1 - A(j\omega)B(j\omega)} \tag{3.3}$$

where $H(j\omega)$, $A(j\omega)$ and $B(j\omega)$ are closed loop transfer function, forward transfer function and feedback gain, respectively. The denominator of right-hand side of Eq. 3.3 is called the characteristic equation of the network and determines whether the network is stable or not. Zeros of characteristic equation constitutes the poles of the feedback network, and there must not be any poles in the RHP to assure stability.

It is difficult to obtain output-to-input closed-loop transfer function to test them by Nyquist Criteria at microwave frequencies. Instead, simpler analysis methods are used based on S parameters such as *K*-factor or Rollet Criterion [47–50]. *K*-factor is a well-known stability analysis method that is used to predict stability of a linear two-port network. The definition of *K*-factor is given in Eq. 3.4.

$$K = Z_0 \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{21}S_{12}|^2}{2|S_{21}S_{12}|} \tag{3.4}$$

K-factor of a linear two-port network, depicted in Figure 3.9, describes the conditions for source (Z_S) and load impedances (Z_L). The network is said to be unconditionally stable if *K*-factor is greater than one for all values of source and load impedances for all frequency spectrum. If *K*-factor is greater than one for some set of source and load

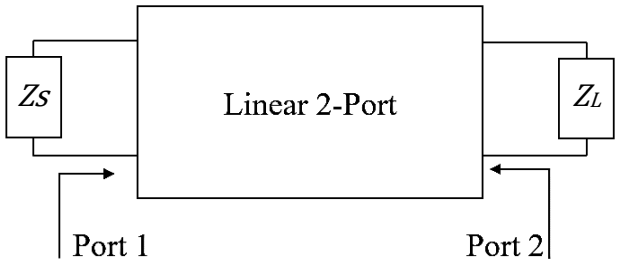

Figure 3.9. A general linear two-port network

impedances, then the network is said to be conditionally stable. Although output-to-input closed-loop transfer function method and *K*-factor method are widely used methods, they can end up with faulty conclusions about stability [51,52]. For instance, in [52], it is reported that a non-Foster circuit analyzed by *K*-factor method turn out to be stable although the circuit exhibits instability due to its internal structure. Hence, other kinds of tests must be performed to predict the stability of whole system. The internal structure of a non-Foster impedance matching network must also be considered while analyzing stability. A safer way to assure the correct stability analysis is to make a complete pole-zero identification including the internal nodes of the network. The pole-zero identification technique relies on the calculation of a Single-Input Single-Output (SISO) transfer function of a circuit linearized about a particular steady-state [53]. The technique is based on placing a small signal current source parallel to the node to be analyzed as depicted in Figure 3.10. Considering the node voltage $V_n(j\omega)$ as output, the impedance seen by the small signal current perturbation $i_n(j\omega)$ gives the frequency response of the linearized circuit as in Eq 3.5 [54].

$$H(j\omega) = \frac{V_n(j\omega)}{i_n(j\omega)} \tag{3.5}$$

The frequency response obtained from the node is then mapped to pole-zero locations on the complex plane by pole-zero identification algorithm using STAN tool. STAN

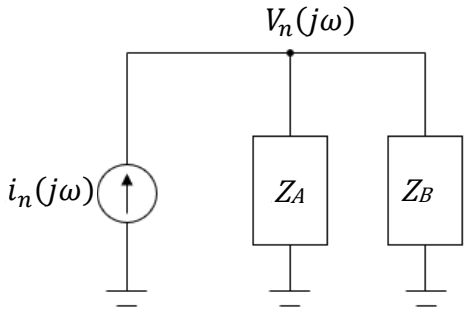

Figure 3.10. Small signal excitation to a linearized circuit at node n

is a software developed by AMCAD Engineering to work collaboratively with the main commercial CAD tools such as AWR MWO®. The poles remaining in right half of the complex plane gives the unstable modes of the node. Normally, unstable modes of all nodes are the same. Nevertheless, the procedure must be conducted for all nodes in the examined circuit to make sure that there is not a hidden unstable mode, i.e. a RHP pole that is related to internal nodes of the circuit [11].

3.4. DESIGN OF NON-FOSTER IMPEDANCE MATCHING NETWORK WITH COMPONENT SPICE MODELS

Impedance characteristic of the monopole antenna with 10 cm length and 1 cm diameter is measured and given in section 3.2. It is revealed that input reactance of the antenna possesses a behavior of a series combination of a capacitance and an inductance. The radiation resistance of the antenna is also modeled as a polynomial as in Eq. 3.2 for simulation purposes. In this section, design of a complete non-Foster impedance matching network is described and simulated with component spice models including NIC and inductive T- dualizer. As specified in chapter 2, Linvill's floating NIC topology is chosen in this thesis work. The first reason of this choice is that there are many examples of successfully stabilized practical implementations in literature [8,14,21,23,34,55]. The second and the last reason is that a floating NIC can be connected directly in series between the antenna and the RF system. Since the antenna reactance is modelled as series combination of inductor and capacitor, the load of the NIC is chosen in the same way. The diagram of non-Foster impedance matching network for electrically small monopole antenna is given in Figure 3.11.

The idea is that after cancelling capacitive-inductive behavior of the monopole antenna, remaining radiation resistance is matched to 50 Ω using an inductive T-dualizer. However, this circuit configuration requires two additional negative inductors ($-L_m$) in dualizer part which means two more NIC circuit is needed.

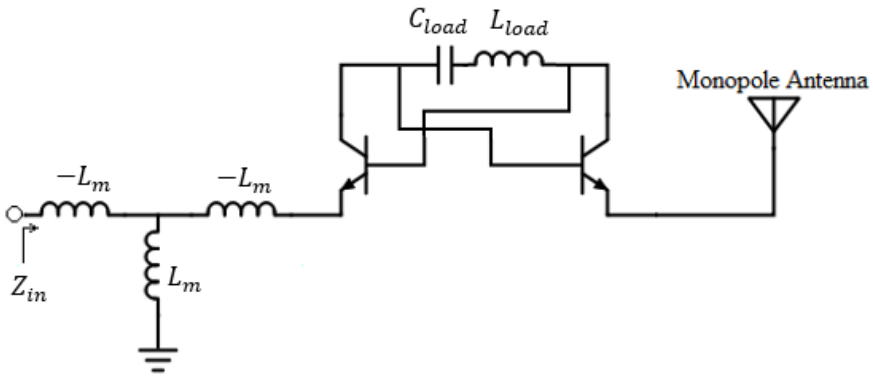

Figure 3.11. Circuit diagram of capacitive-inductive non-Foster matching

Since it is already an exhaustive work to design a successfully stabilized NIC circuit, implementing two additional NICs is not feasible. As a solution, the rightmost negative inductor of inductive T-dualizer can be implemented by adding its value to the L_{load} to get rid of one of the additional NICs, and the leftmost one can be omitted from the design at the expense of some operational bandwidth loss. Hence, the design in Figure 3.11 can be modified as in Figure 3.12.

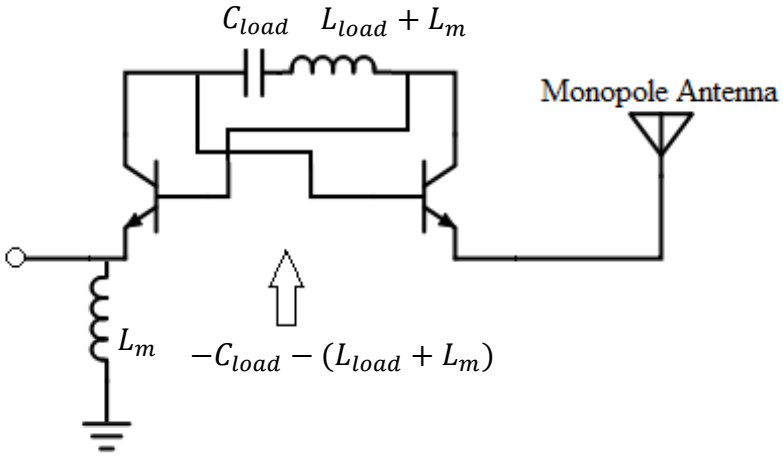

Figure 3.12. A feasible method for implementing Inductive T- dualizer

It is better to mention design specifications, before going into further detail in the design of the circuit. First and main goal is to achieve return loss better than -5 dB between 150 MHz and 500 MHz. The second goal is to maintain stability without violating the first goal. At the end, it is aimed to match the antenna with stabilized negative capacitor-inductor in the desired band.

The first thing to do is to choose transistor in the design phase. The matching network is comprised of two BFR740L3RH NPN transistors produced by Infineon Technologies. BFR740L3RH transistors are suitable for low voltage applications from VHF to 12 GHz. Besides that, collector-base capacitance (C_{cb}) of the transistor is changing in a very small interval between the minimum of 0.09 pf and the maximum of 0.12 pf [56]. As mentioned in Chapter 2, it is important to choose a transistor with a small variation of C_{cb}.

Having chosen the transistors of the design, a proper DC biasing must be implemented for them. Maximum ratings and electrical characteristics of transistors must be considered in the design of biasing part. A voltage divider type bias circuitry with emitter stabilization resistor is implemented. A typical implementation of voltage divider type biasing scheme is shown in Figure 3.13 including RF choke inductors. RF choke inductors are placed for isolation of RF signal from DC biasing while the resistor on the emitter branch of transistor provides DC stabilization.

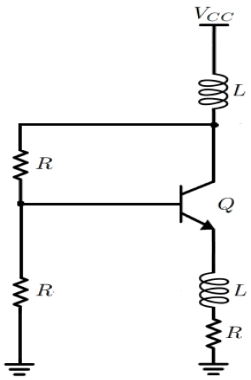

Figure 3.13. Voltage divider type biasing scheme with emitter stabilization resistor

Once the DC biasing topology is determined, whole non-Foster matching circuit is designed and subjected to stability analysis using pole-zero identification algorithm which is explained in previous section. All internal nodes of the circuit are analyzed for stability to explore if there is a hidden unstable mode. Fortunately, all analyzed nodes of the circuit lead to the same pole-zero locations, so the system does not have a hidden mode. The result of stability analysis is given in Figure 3.14. It is seen that there is a pair of complex conjugate poles appearing at 1362.4 MHz in right half of complex plane. This complex conjugate pair of poles indicate a possible oscillation and thus must be removed.

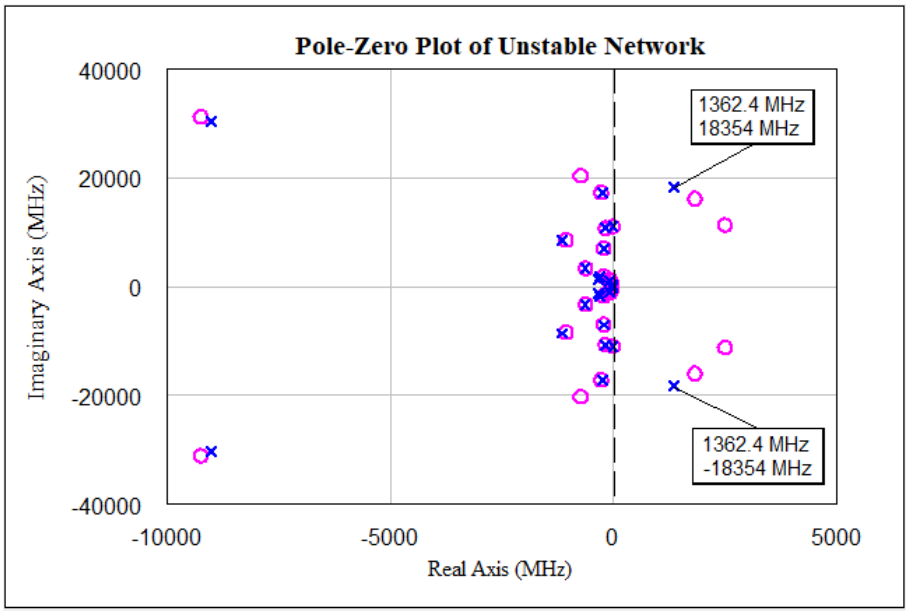

Figure 3.14. Pole-zero plot of unstable non-Foster impedance matching network

In [57], a systematic approach for stabilization of multi transistor circuits is explained. Conventional control techniques (CCTs) in linear control theory such as P (proportional), I (integral) and D (derivative) can be applied in order to stabilize the matching network. Inclusion of series or shunt resistors provides a proportional control, while the integral or derivative control can be implemented by placing

reactive elements. Figure 3.15 shows possible locations for placing the stabilization components. Branches (1) and (2) are directly connected in series between antenna and input, hence these branches are to be avoided for stabilization component placement in order not to degrade the performance of matching network. Apart from degrading circuit performance, additional stabilization components must not distort non-Foster behavior of the circuit. To clarify, the impedance matching network must still be able to generate desired negative impedance after the addition of stabilization elements. When viewed from this aspect, branch (7) is also inappropriate since the load impedance to be inverted is directly affected by an element placed in that branch. In a similar manner, branches (3) and (5) are directly related to DC bias points of the transistors so these branches are also not applicable. Therefore, stabilization elements are placed in remaining branches (4) and (6) as suggested in [11]. Following the addition of stabilization components, pole-zero analysis is repeated to find out if the unstable poles of the matching network are removed or not. The pole-zero plot of the design after the stabilization process is shown in Figure 3.16. It can be seen that the pair of complex conjugate poles does no longer exist in right half of complex plane. Therefore, stabilization of the network is achieved.

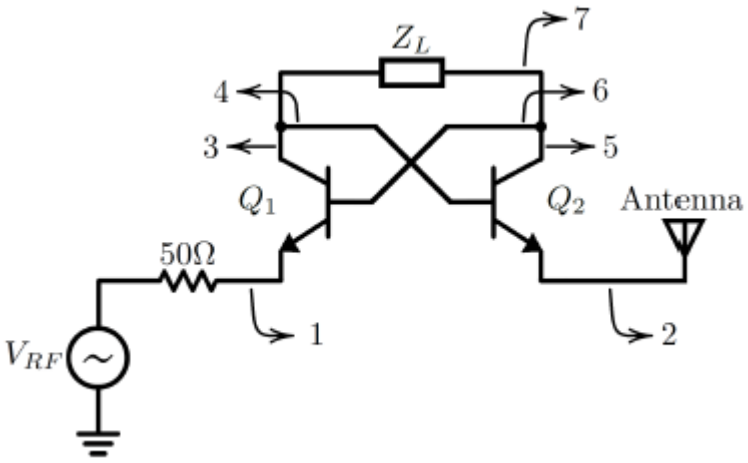

Figure 3.15. A floating NIC circuit connected between antenna and input. Branches (1) to (7) are shown for possible locations of stabilization circuits [11]

Upon achieving stability, whole schematic of non-Foster matching network is completed and given in Figure 3.17 with all components. The components C5, C6, C7, C9, C10, C11 are bypass capacitors that short AC signals and noise to the ground to produce clean DC signal for biasing. It is important to note that at each DC biasing branch, three parallel bypass capacitors are placed. The reason behind placing three bypass capacitors in parallel is that, in practice, the capacitors have series parasitic inductances that distort the operation. In other words, the effects of series parasitic inductances are minimized by placing the capacitors in parallel. The components L3 and L4 are choke inductors which are connected between DC supply and transistor to isolate RF signal from DC signal. Inductors L2 and L5 are also choke inductors with

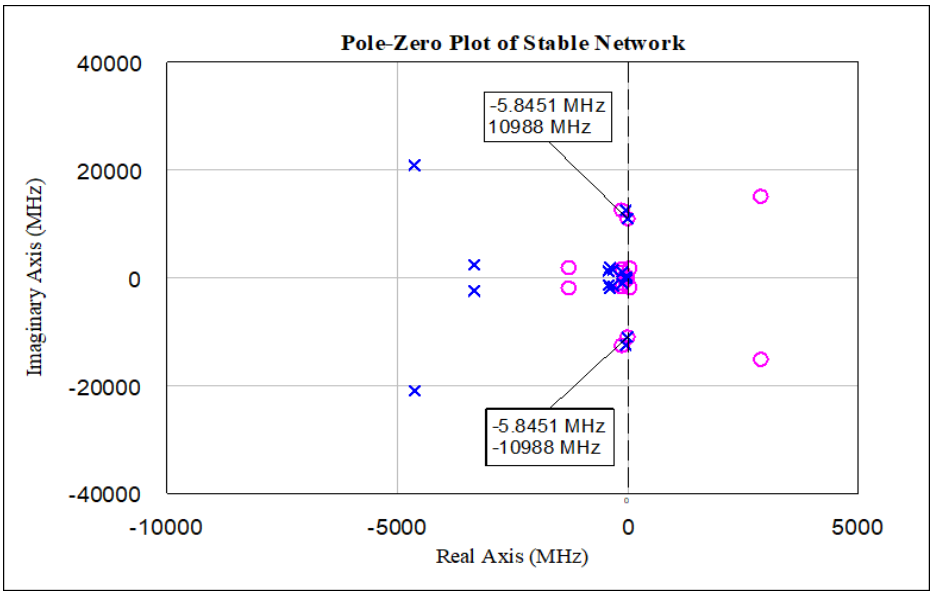

Figure 3.16. Pole-zero plot of stabilized non-Foster impedance matching network

a similar task with L3 and L4. They isolate emitter of transistor from R1 and R6 to maintain a floating operation between input port and antenna. The capacitors C1, C2, C3 and C8 are decoupling capacitors to block DC signals. Components in red box (R_{rad}, C_{ant}, L_{ant}) are the equivalent parameters of antenna for only simulation purposes.

The load of the circuit is comprised of C4 and L6 which are inverted to cancel out the reactance of the antenna. R2, R3, R4 and R5 are voltage division resistors for DC bias. Finally, the components R8, R9, L7 and L8 are stabilization elements which are placed based on the procedure defined in [11].

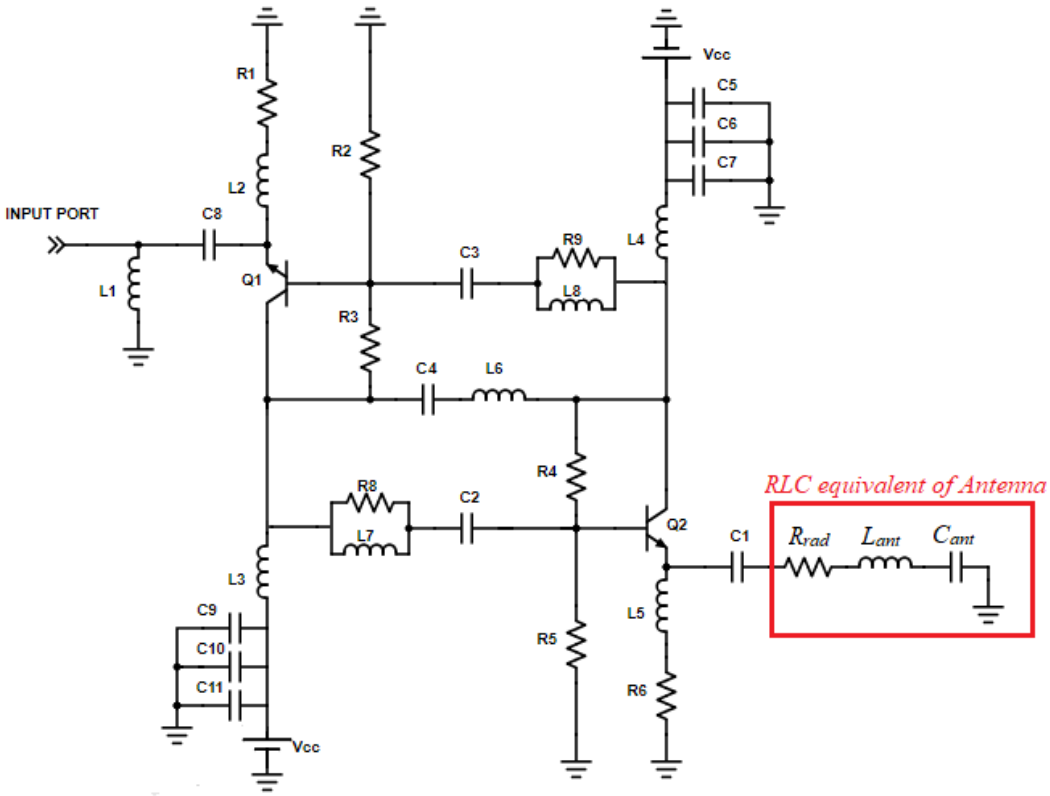

Figure 3.17. Schematic of fabricated non-Foster Impedance Matching Network

CHAPTER 4

FABRICATION AND MEASUREMENT RESULTS

4.1. FABRICATION

The input characteristics of a 10-cm monopole antenna is investigated in section 3.2. Based on the characteristics of the antenna, a lumped equivalent model is extracted. As a result, input reactance of the antenna is modelled as a series combination of an inductor and a capacitor. Besides, a polynomial function is constructed to model antenna input resistance. In the view of impedance information of antenna, it is concluded that the non-Foster impedance matching network should impose compensation of reactance by inverting a series combination of a capacitor and an inductor. In addition, a resistive compensation should be utilized to match the frequency dependent radiation resistance of the antenna.

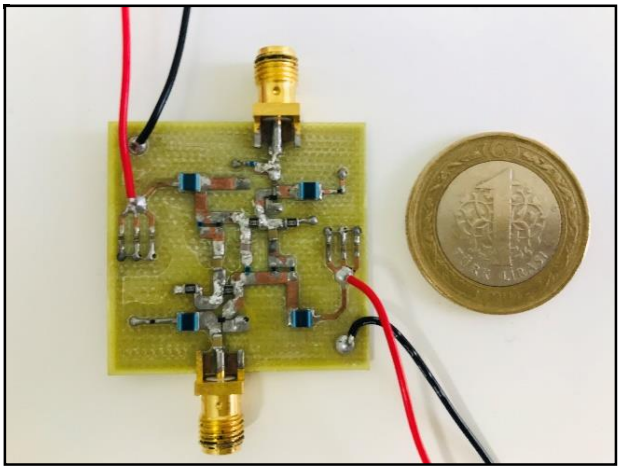

Figure 4.1. Fabricated non-Foster matching network on 4 cm x 4 cm FR-4 substrate

Before fabrication of the circuit, net values of the components are determined and optimized by performing simulations based on various trials until a 5 dB bandwidth in between 130 MHz and 800 MHZ is obtained. Although, design criterion is in between 150 MHz and 500 MHz, the simulated circuit is optimized until a wider bandwidth is obtained to compensate the deviations that might come from manufacturing process.

Table 4.1. Numerical values and description of functions of circuit elements

Component	Value	Description
R1, R6	100 Ω	Biasing, Emitter stabilization
R2, R3, R4, R5	20 kΩ	Biasing
R8, R9	150Ω	Stabilization resistors
C1, C2, C3, C8	0.1 uF	DC blocking capacitor
C5, C9	1 nF	Bypass capacitor
C6, C10	10 nF	Bypass capacitor
C7, C11	100 nF	Bypass capacitor
C4	15 pF	Load capacitor
L1	20 nH	Resistive compensation
L2, L3, L4, L5	4.7 uH	RF choke
L6	25 nH	Load inductor + Resistive compensation
L7, L8	36 nH	Stabilization inductors
Q1, Q2	-	Bipolar Junction Transistors

The non-Foster impedance matching network, the schematic of which is given in Figure 3.17, is fabricated on a 4 cm x 4 cm FR-4 substrate with a thickness of 0.8 mm and relative permittivity (ϵ_r) of 4.4. The conductor on PCB is chosen as 1 oz. copper. The design is based on Linvill's floating OCS NIC which is comprised of two cross-coupled BJTs (BFR740L3RH) and voltage divider type biasing configuration. The fabricated circuit is shown in Figure 4.1. The components of the circuit are selected as surface-mount type (SMT) in order to be flexible in fabrication process. That is to say, it is easier to mount or demount SMT components compared to through-hole types. In addition, circuits that have smaller form-factor can be built with SMT

components. All components used in fabrication are listed in Table 4.1 with their values and functions.

The layout of the fabricated non-Foster matching network is shown in Figure 4.2. The backside of PCB is reserved for ground plane of the circuit. The connections between front side and backside of the PCB are provided by means of non-plated through holes which are filled with conducting cables and solder.

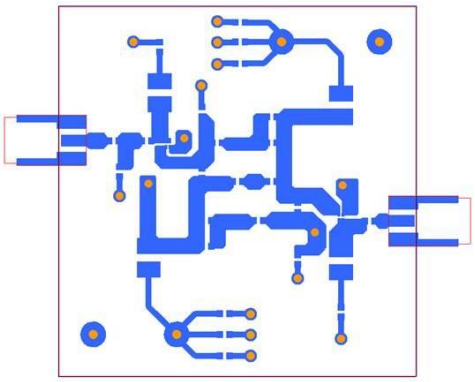

Figure 4.2. Layout of the fabricated non-Foster impedance matching network

4.2. MEASURED AND SIMULATED RESULTS

Upon completion of fabricated non-Foster impedance matching network, measurements which are related to performance of the network are taken by using HP 8720D Vector Network Analyzer in between 100 MHz and 1 GHz. These measurements include input reactance, input resistance and return loss under varying conditions such as input power and load impedance. Throughout this section, aforementioned measurements of fabricated non-Foster impedance matching network are presented in comparison with the simulation results obtained by AWR MWO®. Furthermore, the measurement results are evaluated also for non-Foster matched and unmatched cases, comparatively.

4.2.1. INPUT IMPEDANCE AND RETURN LOSS

The imaginary part of input impedance for overall non-Foster network is measured and given comparatively with simulation results in Figure 4.3 from 100 MHz to 1 GHz. Input reactance of unmatched antenna is also added to the figure in order to observe the differences between non-Foster matched and unmatched cases. The blue curve in Figure 4.3 represents the simulated imaginary part of input impedance with matching network. The red and orange curves stand for measured imaginary parts of input impedance with and without matching network, respectively. It can be seen from the figure that input reactance of unmatched antenna starts from -100 Ω and increases to the vicinity of 100 Ω until the resonance point of antenna. With the inclusion of matching network, input reactance of antenna is confined between -35 Ω and 50 Ω.

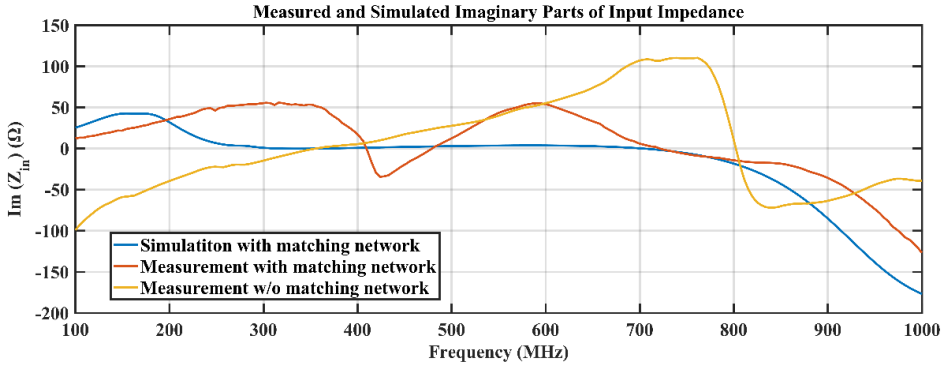

Figure 4.3. Comparison of simulated and measured input reactance with 0 dBm input power with and without non-Foster matching network

Although it seems to be a good improvement on antenna performance, the measured input reactance of non-Foster matched antenna seems to be quite different from simulation result. That is to say, input reactance of simulated matching network is zero over a wide frequency range while measured response is fluctuating around it. One possible explanation for this observation can be parasitic effects of the PCB coming

from manufacturing process. The circuit response may be deteriorated, due to non-ideal effects originated from non-plated through-hole vias. Apart from reactive matching performance of the network, the resistive matching performance is also measured and given comparatively with measured unmatched and simulated matched cases in Figure 4.4.

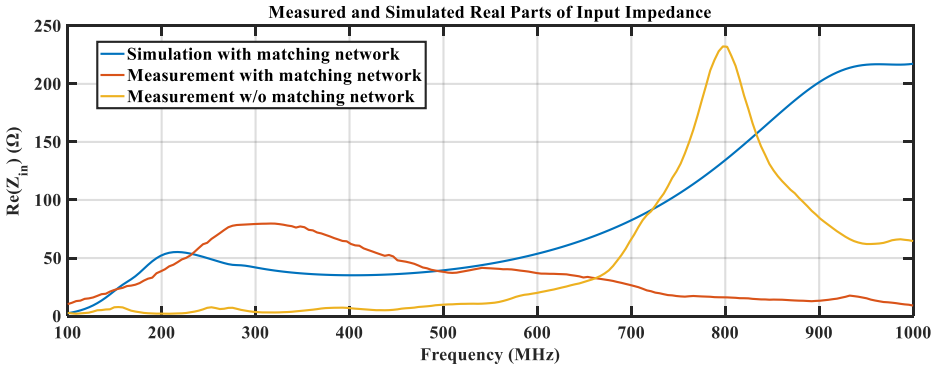

Figure 4.4. Comparison of simulated and measured input resistance with 0 dBm input power with and without non-Foster matching network

The blue curve in the figure represents the simulated real part of input impedance with matching network. The red and orange curves stand for measured real parts of input impedance with and without matching network, respectively. As seen from Figure 4.4, measured real part of the non-Foster matched antenna agrees quite well with simulation results in between 150 MHz and 600 MHz. In this frequency interval, a significant improvement can be seen on the radiation resistance of the antenna. Small radiation resistance of the unmatched antenna is improved by the inclusion of non-Foster matching network and confined between 40Ω and 80Ω. Beyond 600 MHz, the gap between simulated and measured responses is escalating as frequency increases. The reason why simulated and measured responses diverge beyond 600 MHz is that the antenna approaches its resonance point. In the vicinity of resonance, the model developed for electrically small region is no longer valid.

Apart from input impedance, input return loss ($|S_{11}|$ in dB) of matched antenna is also demonstrated in Figure 4.5, comparatively with simulated return loss and measured return loss of unmatched antenna. Measured return loss of matched antenna, simulated return loss of matched antenna and measured return loss of unmatched antenna are demonstrated by red curve, orange curve and blue curve, respectively. When the curves are inspected, it can be seen that measured -5 dB bandwidth of matched antenna agrees well with the simulation result. Besides, the pattern of both curves looks alike. Yet, there are certain differences along the frequency intervals specified by green circles. The reason of these differences is same with the reasons of impedance deteriorations. Other than that, when the curves of measured matched and measured unmatched cases are compared, a great enhancement can be seen especially below 600 MHz. Moreover, overall -5 dB bandwidth is measured as 684 MHz with a lowest point of -21.82 dB at 473.5 MHz.

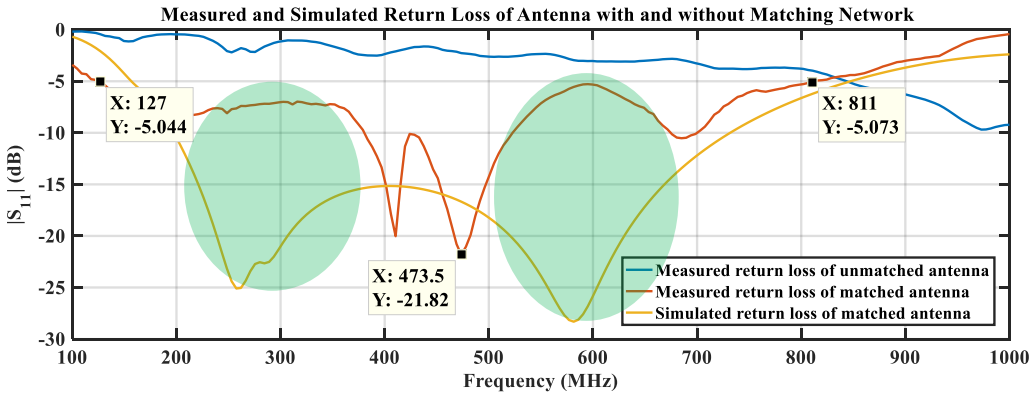

Figure 4.5. Comparison of simulated and measured return loss of antenna with 0 dBm input power with and without non-Foster matching network

Note that both measured and simulated results in this section are taken with 0 dBm input power. Yet, it can be useful to see the effects of different input power levels in order to evaluate how the circuit behavior changes accordingly.

4.2.2. RETURN LOSS WITH VARYING INPUT POWER

When dealing with active circuits, non-linear effects of them must be taken into consideration. Transistors are inherently non-linear devices. Thus, non-Foster matching networks comprised of transistors are also non-linear. Oscillation problem is one of the non-linear properties which is mentioned in Chapter 3. The other non-linearities introduced by transistors are gain compression, harmonics and intermodulation effects [58]. Yet, in this section, only return loss versus different input power levels is examined. In Figure 4.6 below, the return loss measurements are given under different input power excitations from -6 dBm to 3 dBm with 3 dBm steps. As demonstrated in the figure, blue, red, orange and purple curves represent -6 dBm, -3 dBm, 0 dBm and 3 dBm power levels, respectively. While the patterns of -6 dBm, -3 dBm and 0 dBm curves are similar to each other, the pattern of 3 dBm curve shows a significantly better match especially from 400 MHz to 700 MHz.

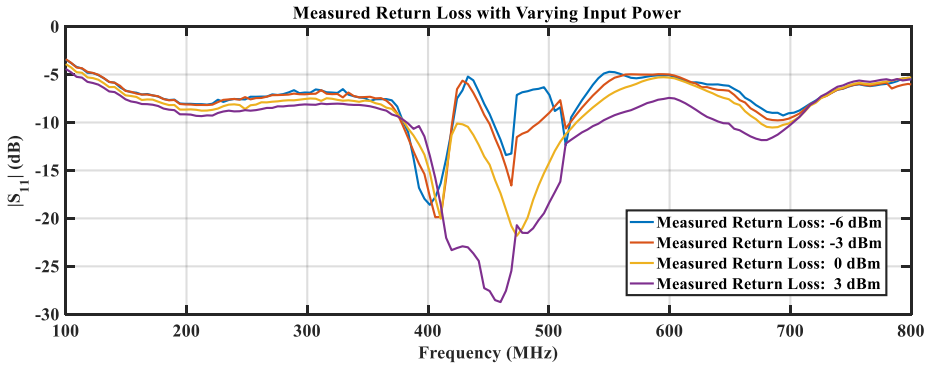

Figure 4.6. Comparison of measured return loss under different input power levels

However, a better match due to a higher input power may not be an evidence for a better performance. When strong signals applied to the input terminals, circuit response deviates from low power response due to the increased loss resistances of

the active circuit [21]. This behavior should be taken into consideration according to the application area. For example, performance of a non-Foster matched antenna may suffer from non-linear behavior in high power transmit applications. To recover the dissipated power over the loss resistances, Class-C or Class-B topologies can be utilized instead of Class-A in order to increase efficiency as proposed in [59].

4.2.3. HARMONIC DISTORTION

Speaking of non-linearity in previous section, another aspect related to that is harmonics generation. Because of the presence of non-linear devices in the circuit, the output signal that is transferred to the antenna is not an exact replica of the input signal, which means distortion. Harmonics can be defined as the produced signals by this distortion that operates at the integer multiples of the fundamental frequency. Although there is no strict threshold for power of harmonics, they are preferred to be as low as possible. Typically, strongest harmonics should be about 20 dB or more below the power of the fundamental tone [23].

One way to characterize the distorted signal is to calculate total harmonic distortion (THD). THD is defined as the square root of the ratio of sum of the powers of all harmonic components to the power of fundamental frequency. THD is usually expressed in percentage or dB form, formulas of which are given in equations 4.1 and 4.2 where P_1 to P_n are the powers of fundamental frequency and its integer multiples.

$$\text{THD (\%)} = 100 \text{ x} \sqrt{\frac{P_2 + P_3 + .. + P_n}{P_1}} \tag{4.1}$$

$$\text{THD (dB)} = 20 \log\left(\frac{\text{THD(\%)}}{100}\right) \tag{4.2}$$

Total harmonic distortion of the non-Foster matching network is calculated by conducting simulations using the harmonic powers up to sixth. Higher order harmonics are excluded from calculations since they have negligible effect. The fundamental frequencies are chosen at three distinct points which are 150 MHz, 300 MHz and 450 MHz. In order to see the effect of input power on harmonics, THD values are calculated for input powers of -6 dBm and 0 dBm, separately. In Table 4.2, using each individual harmonic power, THD (dB) and THD (%) are calculated and given for -6 dBm input power. The same calculations are carried out for 0 dBm input power and THD values are given in Table 4.3.

Table 4.2. Harmonic powers and THD values for -6 dBm input power

Frequency (MHz)	Fundamental Power (dBm)	Second Harmonic Power (dBm)	Third Harmonic Power (dBm)	Fourth Harmonic Power (dBm)	Fifth Harmonic Power (dBm)	Sixth Harmonic Power (dBm)	THD (dB)	THD (%)
150	-14.11	-66.63	-56.46	-94.84	-84.47	-91.57	-41.93	0.8
300	-11.22	-62.18	-47.85	-72.47	-75.29	-92.34	-36.47	1.5
450	-8.15	-55.65	-55.18	-75.31	-85.62	-100.27	-44.58	0.59

Table 4.3. Harmonic powers and THD values for 0 dBm input power

Frequency (MHz)	Fundamental Power (dBm)	Second Harmonic Power (dBm)	Third Harmonic Power (dBm)	Fourth Harmonic Power (dBm)	Fifth Harmonic Power (dBm)	Sixth Harmonic Power (dBm)	THD (dB)	THD (%)
150	-7.48	-48.11	-36.44	-68	-49.82	-79.15	-28.49	3.76
300	-4.97	-45.51	-29.95	-42.02	-48.16	-57.28	-24.94	5.66
450	-2.33	-47.78	-25.21	-36.64	-35.91	-56.36	-22.22	7.74

When each individual harmonic and THD values are compared for 0 dBm and -6 dBm input powers, it is observed that the values for 0 dBm input power are higher. Hence,

harmonic distortion increases with increasing input power which supports the observations of high power non-linearity in previous section.

4.2.4. TRANSMISSION EFFICIENCY AND TRANSDUCER GAIN

One of the expectations from non-Foster matching circuits is to increase transferred power to the radiation resistance of the antenna. So, an analysis in simulation environment is carried out whether the non-Foster matching circuit fulfils this expectation. In Figure 4.7, power transferred to the radiation resistance is plotted for both non-Foster matched and unmatched antenna with 0 dBm input power between 100 MHz and 500 MHz. It is observed that at 250 MHz, -5.7 dBm power is transferred while it is -2.7 dBm for 400 MHz. However, when the simulated return loss plot, which is given in Figure 4.8, is examined, approximately 10 dB better return loss is observed for 250 MHz. One interpretation for this ambiguity is that the portion of radiation resistance in total impedance is smaller at low frequencies compared to high frequencies. In other words, circuit losses dominate the radiated power at low frequencies.

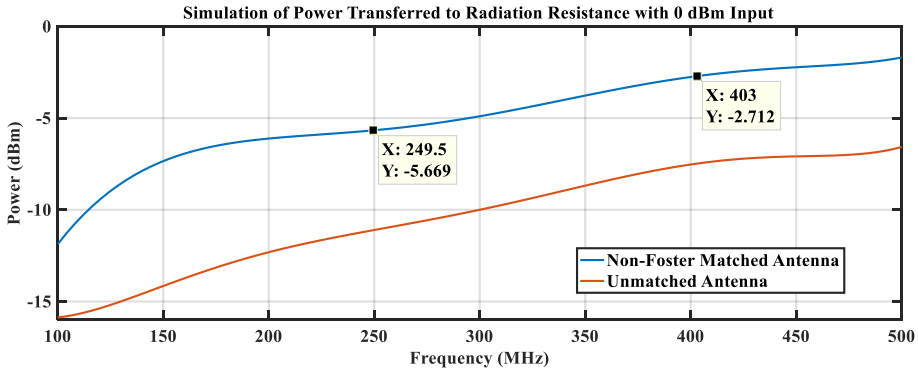

Figure 4.7. Comparison of power transferred to the radiation resistance

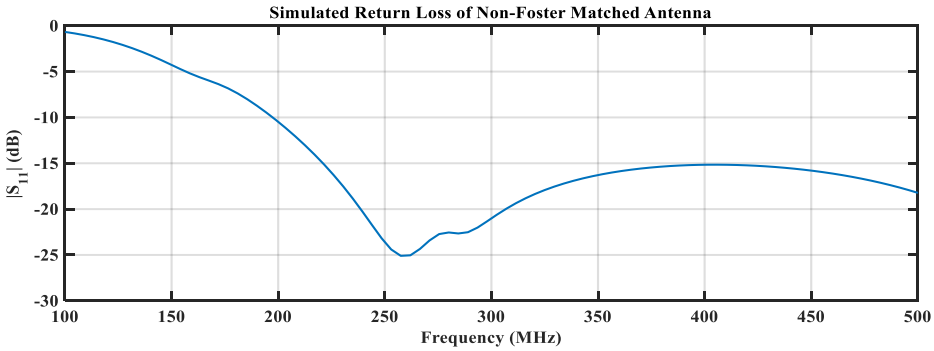

Figure 4.8. Simulated Return Loss of non-Foster matched antenna

Having done the analysis of transferred power, it is also possible to calculate transmission efficiency which is defined as the ratio of radiated power to the input power.

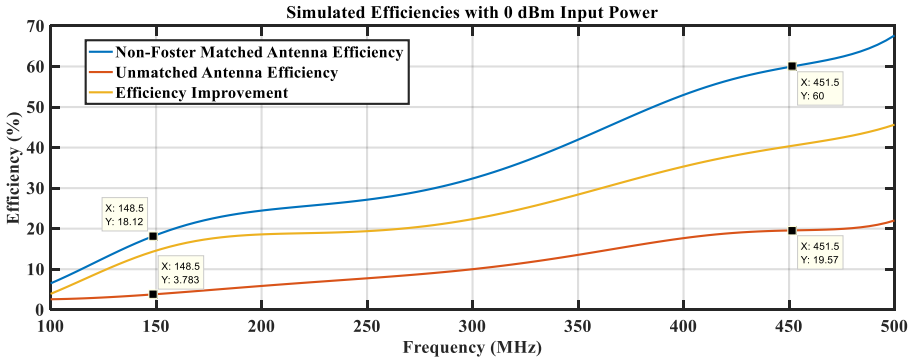

Figure 4.9. Simulation of transmission efficiency

In Figure 4.9, simulated transmission efficiencies for non-Foster matched and unmatched antenna are plotted with 0 dBm input power. Also, the efficiency improvement is shown by orange curve. It is observed that 15% to 40% efficiency improvement is achieved between 150 MHz and 450 MHz.

Besides, the transducer gain improvement, i.e. the improvement of transferred power to the radiation resistance when compared to the unmatched case, is simulated with 0 dBm input power between 100 MHz and 500 MHz and is given in Figure 4.10. As seen from the figure, a maximum of 6.82 dB and a minimum of 4.77 dB transducer gain improvement is obtained.

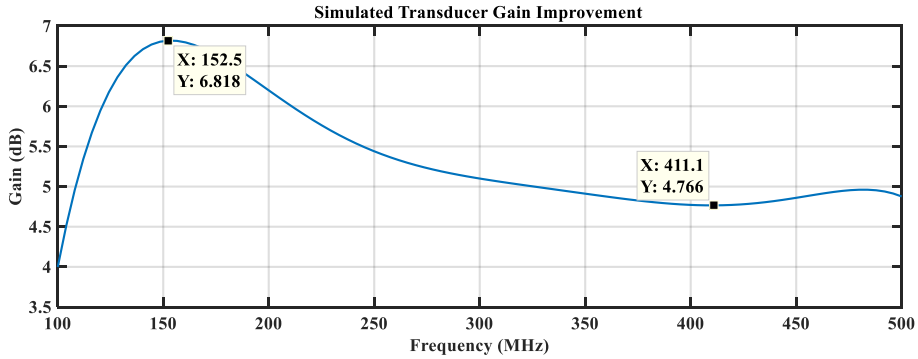

Figure 4.10. Simulation of transducer gain improvement

Note that due to the large wavelengths in the bandwidth of interest, it is not practical to measure antenna properties in anechoic chamber of METU facilities. Nevertheless, simulation results presented in this section sufficiently highlight the improvements introduced by non-Foster matching network.

4.2.5. RETURN LOSS WITH VARYING LOAD CONDITIONS

As given in the beginning of this chapter, a 15-pF capacitor is used as a capacitive load of the negative impedance converter. So far, all measurements are taken with the same circuit and the same load. However, it should be evaluated if a different load can give a better matching performance. The basis of this thought is that the fabricated non-Foster matching circuit may be suffering from parasitic effects coming from

solder joints, substrate of PCB or microstrip traces. As a result of cumulative effects of aforementioned reasons, it is possible that the negative impedance generated by the non-Foster circuit may not be the exact response for its load. Therefore, it is worth examining the response of the circuit with different load conditions and investigating the changes on overall performance.

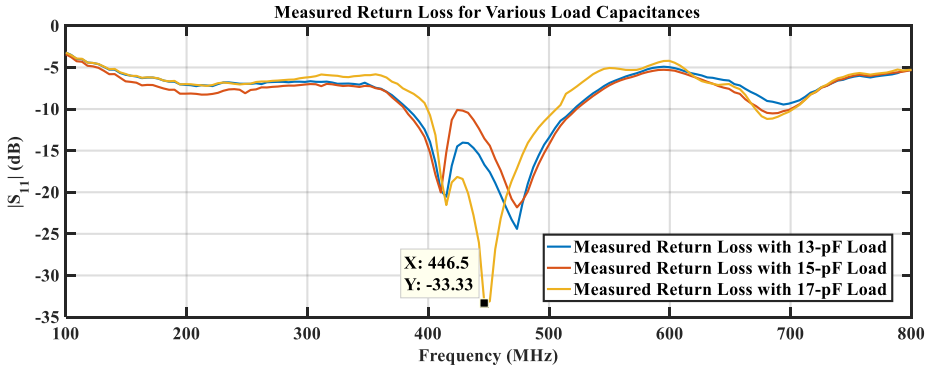

Figure 4.11. Comparison of measured return loss with different load capacitors

At this point, return loss measurements are taken for three different values of load capacitance, which are 13 pF, 15 pF and 17 pF. These measurements are shown in Figure 4.11, where blue, red and orange curves stand for 13 pF, 15 pF and 17 pF load capacitances, respectively. Note that although the measurement for 15-pF load is given in previous section, it is also intentionally included in Figure 4.11 in order to be able to make a comparison with other measurements. When return loss curves are compared, it can be seen that all measurements are similar to each other in terms of curve patterns. Apart from that, at 446.5 MHz point, a return loss of -33.33 dB is observed with 17 pF load. Although it seems to be a great result in a narrow band, it is important to keep in mind that the prior aim of non-Foster matching is to provide good matching performance at electrically small regions, i.e. low frequencies, with a wideband characteristic. Hence, when low frequency performance is considered, 15-pF load seems to have a few dB better result between 100 MHz and 300 MHz.

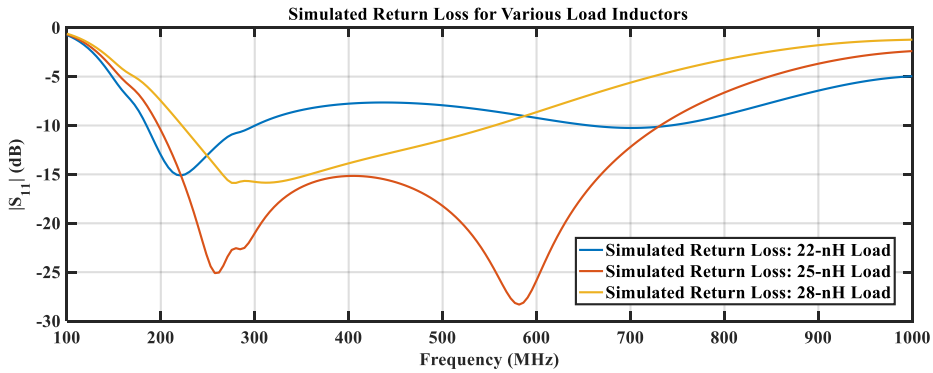

Figure 4.12. Comparison of simulated return loss with different load inductors

The electrically small antenna used in this thesis study possesses an inductive reactance in addition to capacitive reactance as given in Section 3.2. This is why the load of negative impedance converter is chosen as a series combination of a capacitor and an inductor in the first place. Thus, similar to analysis for various load capacitors, an investigation for different values of load inductors should also be carried out.

Unfortunately, analysis for load inductors remained limited to only simulation due to the lack of component. Return loss simulations are made for three different values of load inductor, which are 22 nH, 25 nH and 28 nH. These simulations are presented in Figure 4.12, where blue, red and orange curves stand for 22 nH, 25 nH pF and 28 nH load inductors, respectively. As seen from the figure, a change of load inductor is much more effective than a change of load capacitance on matching performance. It is an expected result since the load inductor is used for resistive compensation in addition to reactive compensation. In other words, changing the value of load inductor affects not only input reactance of non-Foster matching network but also input resistance of it.

CHAPTER 5

CONCLUSION

5.1. CONCLUSION AND REMARKS

Reactance of electrically small antennas is significantly high as their radiation resistance is very small which leads to high Q-factor resulting in narrow operation bandwidth. Herein, the major objective of the study is to enhance the performance of an electrically small monopole by implementing a non-Foster impedance matching network at the input of the antenna. In addition to reactance cancellation, a work for improvement of radiation resistance is done in order to ensure a broad operating frequency range.

Beginning with the definition and fundamental limitations of electrically small antennas, theoretical background of non-Foster impedance matching is discussed in all aspects in Chapter 2. Along with a comprehensive literature review, an ideal non-Foster matching network is simulated in AWR MWO® Design Environment to match a 10-cm monopole which is modeled as series of a capacitor and a radiation resistance. The proof of concept is achieved with all ideal elements. Besides, effects of small signal emitter resistances and collector-base capacitances on circuit performance are discussed. It is revealed that collector-base capacitances of transistors add up to load impedance of the negative impedance converter leading to unexpected additional reactance. Furthermore, it is observed that small signal emitter resistances of the transistors remain series to radiation resistance of the antenna which may cause unintended power dissipation. Thus, in the phase of transistor selection, parameters of the transistors should be evaluated to keep away from unintended circuit responses. Obviously, the effects of aforementioned parameters of the transistors are unique to

selected topology of the negative impedance converter, which is Linvill's open circuit stable NIC in this thesis. With a different topology, a reexamination on the effects of transistor parameters must be done.

In chapter 3, a systematic design procedure is introduced, and a practical non-Foster matching circuit is designed for 10-cm monopole antenna. Return loss of an unmatched 10-cm monopole is measured to be no better than -2 dB up to 800 MHz. Design and stabilization of a series combination of a -15 pF capacitor and a -25 nH inductor is presented. It is shown by pole – zero analysis that the circuit has a pair of complex conjugate poles at 1362.4 MHz which indicates a possible oscillation. In order to eliminate the unstable mode of the circuit, a parallel combination of a resistor and inductor is placed in the feedback branches according to the stabilization procedure described in [11]. Furthermore, schematic of whole matching circuitry is given with simulation results related to matching performance in Chapter 3 as well.

In Chapter 4, the fabrication details, implementation and measurements of non-Foster matching network are presented. Performance of the circuit is measured between 100 MHz and 1 GHz in comparison with simulated results. When the results of unmatched and non-Foster matched cases are compared, it is seen that return loss is significantly enhanced between 100 MHz and 800 MHz with a -5 dB bandwidth of 684 MHz. Furthermore, in addition to reactance cancellation, the radiation resistance of the antenna is considerably improved from a few ohms to 40-80 ohms. Differences between simulated and measured results are discussed and commented in terms of parasitic and non-ideal effects. Moreover, the changes in return loss seen at the input port of the antenna are examined under different input power levels. It is concluded that the changes of return loss with increased input power are related to increased loss resistances in the circuit. This non-linear effect should be considered when designing non-Foster circuits for high power transmit applications. In addition, harmonic distortion, transmission efficiency and transducer gain analysis are shown by simulations. Between 150 MHz and 500 MHz, efficiency improvement from 15% to 40% and gain improvement from 4.77 dB to 6.82 dB are achieved when compared to

unmatched antenna. Finally, return loss of the non-Foster matched network is examined under different capacitive and inductive load conditions. It is revealed that an inductance change is more effective than the capacitance change since the load inductor is responsible for both reactive compensation and resistive transformation.

To make a general assessment of this thesis study, it can be stated that the performance of non-Foster matching network is sensitive to effects introduced by PCB parasitics, soldering and tolerances of components that were purchased from manufacturers. It is worthy to note that even two transistors purchased from same manufacturer may not be identical. In addition, the fabricated circuit was measured in a close indoor environment which can cause further differences between measurements and simulations. Naturally, measurement environment was not included as a model in simulations since building a model for a specific environment requires a dedicated research and effort which is beyond the scope of this thesis. Although the fabricated circuit is not a ready-to-use product, with a suitable integrated circuit technology, differences between simulation and measurement results can be further reduced. Dynamic range of the non-Foster matching networks is another issue that needs further investigation as the input power level drastically affects the input impedance and thus matching performance. Nevertheless, despite the fact that some differences exist between simulations and measurements, both results sufficiently emphasize the advantages of using non-Foster networks in ESA matching applications.

5.2. FUTURE WORK

Tracing the work done in the context of this thesis, future lines of the non-Foster matching concept can be drawn as follows.

First, as an alternative to PCB, integrated circuits can be implemented to overcome the distortions such as parasitic effects and other inaccuracies introduced by

fabrication process. By doing so, frequency limitations can be further extended as published by Kolev in [60]. In this work, -1 pF capacitor is obtained between 1 GHz and 5 GHz by means of monolithic microwave integrated circuit (MMIC) technology. Apart from frequency limitations, reliability of the circuits can also be improved with integrated circuits. In addition, smaller form-factors can be achieved.

Second, other active devices create alternatives to implement non-Foster matching networks such as operational amplifiers or resonant tunneling diodes (RTDs). Non-Foster circuits with RTDs can solve frequency limitations and potential instability problems as stated in recently published works [14,35].

On the other hand, noise figure is another figure of merit especially in receiver applications. Considering the fact that the non-Foster applications includes active devices, it is not easy to establish a technique for the estimation of added noise. This problem is handled with an interesting point of view by M. Jacob and D. Sievenpiper in [61]. The noise model of a BJT-based NIC is developed around biasing point in order to estimate noise addition. So, further methods and implementations might be developed for noise analysis in non-Foster circuits.

In high power transmit applications, BJT-based non-Foster circuits are suffering from non-linear properties of active devices. Gain compression are the most crucial non-linear effect when dealing with high input powers. Other biasing schemes such as Class-B and Class-C may be implemented to enhance power efficiency in transmit applications.

Finally, self-tuning non-Foster circuits can be another future research topic to be implemented with electrically small antennas. With a smart circuit, the impedance changes at the antenna port can be tracked and load of non-Foster circuit can be adjusted accordingly by means of variable capacitors and inductors.

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APPENDICES

A. TRANSISTOR PARAMETERS

Most of commercial electronics simulators use simulation models of BJT transistors based on Gummel-Poon model. In this section, the Gummel-Poon spice parameters of the transistors used in this thesis are given below.

GUMMEL-POON SPICE PARAMETERS OF BFR740L3RH:

TNOM=25 IS=1.362e-015 BF=632 NF=1.027 VAF=120 & IKF=0.09421 ISE=1.4e-013 NE=2.6 BR=100 NR=1 VAR=1.7 & IKR=0.0035 ISC=5e-015 NC=2 RB=2 IRB=0.000889 & RBM=0.6 RE=0.1019 RC=5.14 XTB=-2.482 EG=1.034 & XTI=0.808 CJE=3.14e-013 VJE=0.8119 MJE=0.1431 & TF=1.667e-012 XTF=200 VTF=0.3493 ITF=0.3 PTF=1 & CJC=8.419e-014 VJC=0.4412 MJC=0.3364 XCJC=0.6466 & TR=2.786e-008 CJS=2.229e-013 MJS=0.2684 VJS=0.4393 & FC=0.8156 KF=2.56e-011 AF=1