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Comparison of Two Alternative Silicon-On-Glass Microfabrication Processes for MEMS Inertial Sensors

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Abstract

This paper presents experimental comparison of a modified silicon-on-glass (M-SOG) process to a previously-reported classical SOG (C-SOG) process based on the use of SOI wafers, yielding a stress free <111> silicon structural layer with desired structure thickness. The basic difference between these processes is the sequence of the step at which the silicon microstructures are defined by DRIE, making M-SOG more robust against critical dimension (CD) variations. Overall, M-SOG provides a simple, high yield, reliable, and robust solution for producing high performance MEMS inertial sensors, and these advantages are experimentally verified over C-SOG, both completed by following the identical process parameters and by using the same mask set.

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Keywords: Silicon-On-Glass (SOG) process; MEMS inertial sensors

1. Introduction

SOG processes are attractive for high-performance MEMS inertial sensors, since they offer very low parasitic capacitances as well as flexible routing of interconnects over glass substrates. An example is the dissolved wafer process (DWP) [1], where the structural layer thickness is practically limited to 20 μm , besides there is stress induced by deep boron diffusion. An epitaxially-grown boron-doped SiGe layer eliminates stress [2], but high Ge concentration significantly increases thermoelastic damping, limiting sensor quality factors. Moreover, DWP etchants require the use of <100> silicon, however, <111> silicon

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is reported to be a better mechanical material considering “the uniformity of elastic constants with crystallographic orientation” [3]. Alternative SOG processes [4-7] allows using $\langle 111 \rangle$ structural silicon without any thickness limitation. However, in some of these processes [4, 5], the silicon layer is suspended over a glass substrate before defining the critical structures, which suffers from CD variation due to heat generated during DRIE [8]. Clearly, there is a need for combining the advantage of “producing thick, high quality stress-free $\langle 111 \rangle$ silicon structural layers” offered by the C-SOG processes with the advantage of “high CD control” offered by the DWP. This paper reports an M-SOG process combining these features and presents an experimental comparison of the M-SOG and C-SOG processes.

2. Fabrication

The fabrication processes of both C-SOG and M-SOG are based on the SOG micromachining using SOI wafers. The use of SOI substrates allows selection of an optimum device layer thickness (35 μm) for achieving maximum aspect ratio in DRIE (typically 35:1) with minimum possible feature size ($\sim 1 \mu\text{m}$).

Figure 1 shows the fabrication steps of the C-SOG and M-SOG processes. Both processes begin with the formation of anchor and pad metallization on a glass substrate. The C-SOG process continues with the formation of a thin aluminum layer on the SOI wafer as an etch stop layer for DRIE. Then, SOI wafer is anodically bonded to the glass and it is followed by the removal of handle and buried oxide layers of SOI wafer by DRIE and RIE/BHF, respectively. Finally, microstructures are defined by DRIE over the glass substrate. On the other hand, in the M-SOG process microstructures are formed on the SOI wafer and then it is anodically bonded to the glass substrate. The M-SOG process is completed after the removal of the handle and buried oxide layers. The basic difference between the two processes is the sequence of the step at which the silicon microstructures are defined by DRIE.

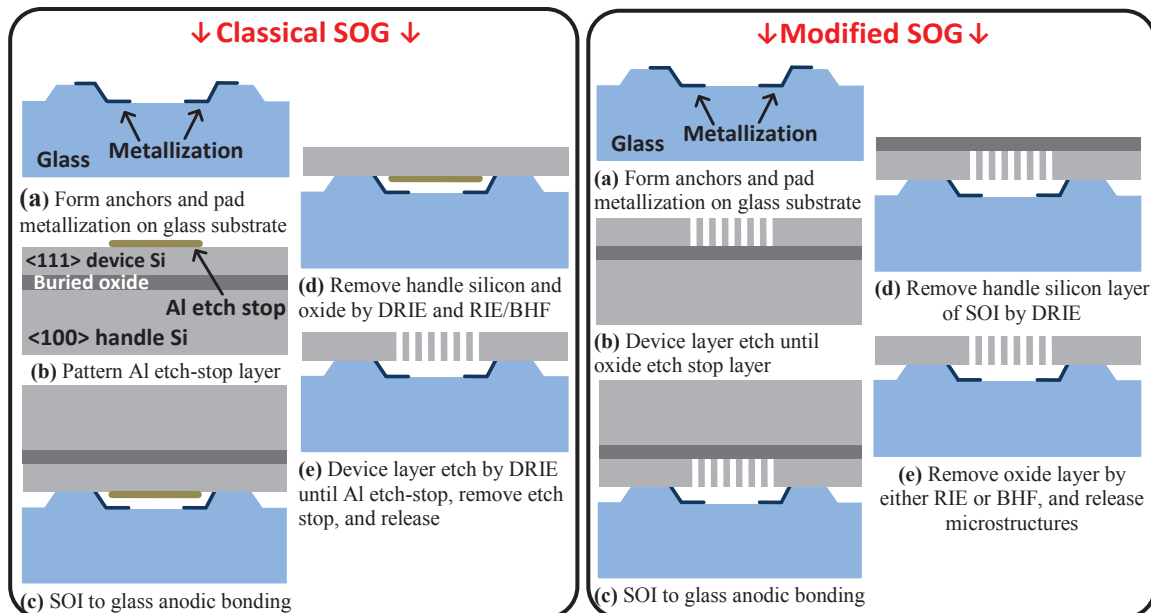


Fig. 1. Fabrication steps of the C-SOG (left) and M-SOG (right) processes. The difference between the two is the sequence of DRIE; in the C-SOG DRIE is performed over the glass substrate, in the MSOG DRIE is performed on the SOI wafer.

3. Experimental Results

The experimental comparison is carried out by visual inspection and resonance tests on the gyroscope prototypes which are fabricated using the C-SOG and M-SOG processes under identical process conditions and with the same mask set. Figure 2 shows the top, bottom, and cross-sectional views of the comb fingers and spring beams, respectively, fabricated in both C-SOG and M-SOG processes.

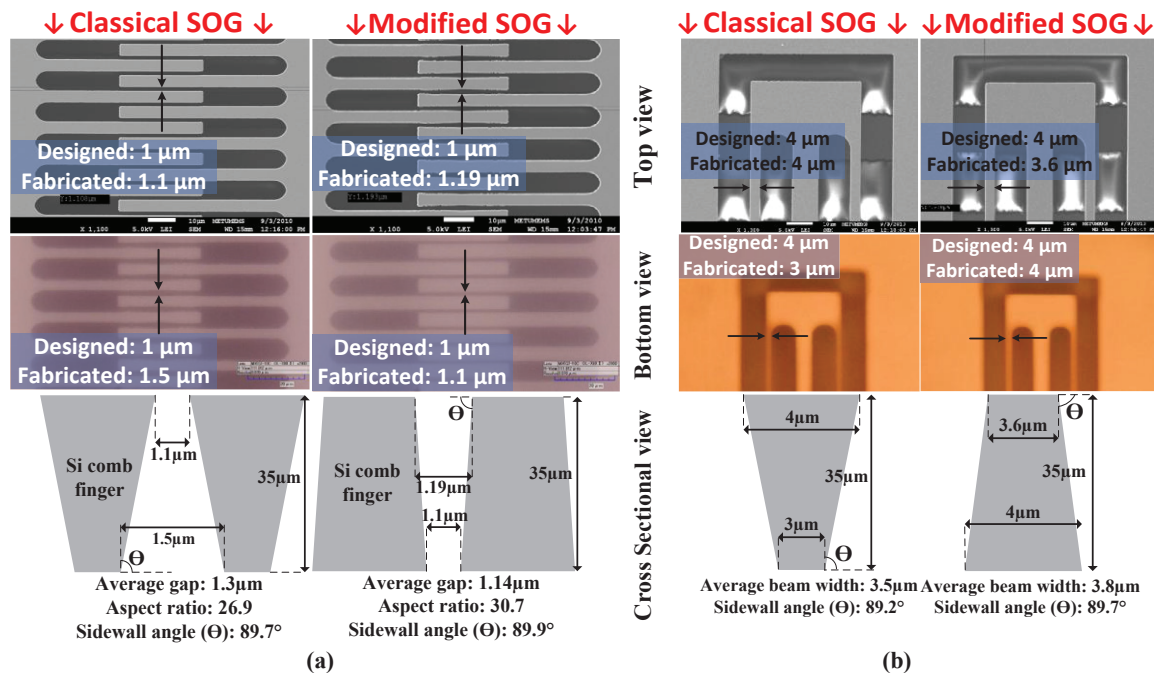


Fig. 2. Top, bottom, and cross-sectional views of the (a) comb fingers, (b) spring beams, respectively, fabricated in both C-SOG and M-SOG processes. The M-SOG process preserves the critical dimensions closer to the design values compared to the C-SOG process.

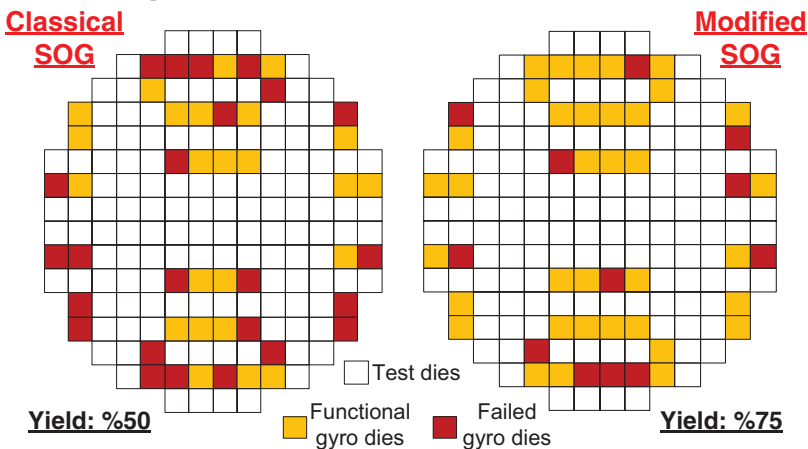


Fig. 3. Production yield of C-SOG (left) and M-SOG (right) processes. The wafer contains a number of test dies to test other sensors than gyros. The production yield of the M-SOG process (75%) is about 1.5 times higher than the C-SOG process (50%) under identical process conditions and with the same mask set.

The M-SOG process preserves the critical dimensions within 14% of design values with a vertical etch profile very of 89.9° and an aspect ratio of 30.7, which is clearly better than the results achieved by the C-SOG (30% CD variation, 89.7° profile angle, and aspect ratio of 26.9). Moreover, Figure 3 shows that M-SOG yield (75%) is about 1.5 times higher than C-SOG yield (50%) under identical process conditions. Table 1 shows the measured resonance frequencies of the gyroscopes fabricated with the M-SOG and C-SOG. The gyroscope prototypes fabricated by the M-SOG process have resonance frequencies much closer to the design values, thanks to enhanced CD control.

Table 1. Comparison of the designed and measured resonance parameters of the sensors fabricated in the C-SOG and M-SOG processes. The gyroscope prototypes fabricated by the M-SOG process have resonance frequencies much closer to the design values.

Resonance Parameter		Designed	Measured Average	
			C- SOG	M-SOG
Drive	Freq.(kHz)	15	11.6	13.8
	Gain (dB)	-	-41.9	-38.7
Sense	Freq.(kHz)	16.5	12.1	13.2
	Gain (dB)	-	-23.3	-20.8

Finally, the advantage of M-SOG process is experimentally verified by the performance results of a sample gyroscope which demonstrates exceptional angle random walk and bias instability performances of $0.014^\circ/\sqrt{\text{hr}}$ and $0.39^\circ/\text{hr}$, respectively.

4. Conclusion

This study presents an experimental comparison between two alternative SOG processes, C-SOG and M-SOG, based on the use of SOI wafers. These processes are compared using the fabricated gyroscope prototypes by visual inspection and resonance tests. It has been observed that M-SOG provides higher production yield and better CD control.

In summary, M-SOG process is a simple, high yield, reliable and robust solution for MEMS inertial sensors, and it can also be adapted to a wide range of MEMS devices.

References

- [1] Gianchandani Y B, Najafi K. A bulk silicon dissolved wafer process for microelectromechanical devices. *J Microelectromech Syst*, 1992; 1-2, p. 77-85.
- [2] Duwel A, Weinstein M, Gorman J, Borenstein J and Ward P. Quality factors for MEMS gyros and the role of thermoelastic damping. *MEMS*, 2002; p. 214-219.
- [3] Kim J, Cho D and Muller R S. Why is (111) silicon a better mechanical material for MEMS. *Transducers*, 2001; p. 662-665.
- [4] Alper S E, Temiz Y and Akin T. A compact angular rate sensor system using a fully decoupled silicon-on-glass MEMS gyroscope. *J Microelectromech Syst*. 2008; 17-6, p. 1418-1429.
- [5] Sawyer W D, Prince M S and Brown G J. SOI bonded wafer process for high precision MEMS inertial sensors. *J Micromech. Microeng*, 2005; 15, p. 1588-1593.
- [6] Cabuz C, Ridley J A. SOI/Glass process for forming thin silicon micromachined structures. *US Patent*, 2002; 0081821 A1.
- [7] Chen S, Chien H T, Lin J Y and Hsu Y W. A method for fabricating MEMS accelerometers. *Electronic Materials and Packaging* 2008; p. 84-87.
- [8] Alper S E, Aydemir A and Akin T. Stepped etching for preserving critical dimensions in through wafer Deep Reactive Ion Etching of thick silicon. *Transducers*, 2009; p. 1110-1113.