DESIGN AND IMPLEMENTATION OF POWER QUALITY MONITORING SYSTEM FOR DISTRIBUTION SYSTEMS

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DESIGN AND IMPLEMENTATION OF POWER QUALITY MONITORING SYSTEM FOR DISTRIBUTION SYSTEMS

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ABSTRACT

DESIGN AND IMPLEMENTATION OF POWER QUALITY MONITORING SYSTEM FOR DISTRIBUTION SYSTEMS

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Smart grid concept is a significantly important topic all over the world. The consumers should be supplied with power sources that is as clean as possible. The quality of delivered power depends on parameters defined in different standards such as The Electrical Distribution System Supply Reliability and Quality of Electricity Regulation in Turkey. To achieve complete control on the grid, Power Quality (PQ) should be monitored and controlled at the end of the power distribution system. Considering the number of the consumers in the distribution system, this is achieved by designing a stand-alone, high-performance, and real-time Power Quality Monitoring device, which can monitor adjacent consumers but at the same time with the lowest possible cost. In Turkish distribution system topology, there exists 12 feeders at the transformer substations at most. Hence a required monitoring system should be able to measure and/or calculate voltage and current phases of two sides of the transformer and current phases of the 12 feeders. The main objective of this study is to measure standard-defined power quality parameters for 64 sources in real-time with a circuit that is fitting in the smallest

FPGA possible. Within the scope of this thesis, a real-time system, which may form the processing sub-system of a power quality monitoring device that is capable of measuring PQ parameters in accordance with international standard IEC 61000-4-30, is implemented on FPGA. The developed system is evaluated using synthetic test data constructed on MatLAB and the results are compared with the expected values.

Keywords: power quality monitoring, FPGA, power quality parameters, distribution systems

ÖZ

DAĞITIM SİSTEMLERİ İÇİN GÜÇ KALİTESİ İZLEME SİSTEMİ TASARIMI VE UYGULAMASI

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Akıllı şebeke kavramı, bütün dünyada önemli bir konudur. Tüketicilere iletilen güç, olabildiğince temiz olmalıdır. Dağıtılan gücün kalitesi, Türkiye Elektrik Piyasası Dağıtım Sisteminde tanımlanan Elektrik Enerjisinin Tedarik Sürekliliği, Ticari ve Teknik Kalitesi Yönetmeliği gibi farklı standartlarda tanımlanan parametrelere bağlıdır. Şebeke üzerinde tam kontrolün sağlanabilmesi için dağıtım sisteminin sonunda, Güç Kalitesi izlenmeli ve kontrol edilmelidir. Dağıtım sistemlerindeki tüketici sayısı göz önüne alındığında, bu kontrolün sağlanabilmesi, tek başına, yüksek performanslı ve gerçek zamanlı çalışabilen, yakın tüketicilerin ortak kullanımına olanak sağlayabilen, en ucuz cihazla mümkün olacaktır. Türk dağıtım sistemlerinin topolojisi incelendiğinde, trafo merkezlerinde, en fazla 12 fiderler var olmaktadır. Bu nedenle, gerekli olan izleme sistemi, transformatörün iki tarafının gerilim ve akım fazlarını ve bu 12 fiderin akım fazlarını ölçebilecek yetenekte olmalıdır. Bu çalışmanın amacı, standartlarca tanımlanan Güç Kalitesi izleme

parametrelerini gerçek zamanlı olarak 64 kaynak için ölçerken mümkün olan en küçük FPGA içine sığabilmektir. Bu tez kapsamında, Güç Kalitesi izleme parametrelerini uluslararası IEC 61000-4-30 standardında tanımlandığı şekilde ölçebilen bir cihazının işlemci alt sistemini oluşturacak gerçek zamanlı bir sistem FPGA üzerinde uygulanmıştır. Geliştirilen sistem, MatLAB'da oluşturulan sentetik test verileriyle değerlendirilmiş ve sonuçlar beklenen değerlerle karşılaştırılmıştır.

Anahtar kelimeler: güç kalitesi izleme, FPGA, güç kalitesi parametreleri, dağıtım sistemleri

to loving memory of my mother

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LIST OF ABBREVATIONS

FPGA	: Field Programmable Gate Array
PQD	: Power Quality Device
IEC	: International Electrotechnical Commission
LUT	: Look Up Table
LUTRAM	: Look Up Table Random Access Memory
FF	: Flip Flop
BRAM	: Block Random Access Memory
DSP	: Digital Signal Processing
IO	: Input / Output
R2SDF	: Radix-2 Single-Path Delay Feedback
ADC	: Analog to Digital Converter
GPIO	: General Purpose Input / Output
NA	: Not Applicable

CHAPTER I

INTRODUCTION

Smart grid and power quality concepts are important and interesting topics. Over the years, various projects were developed in Turkey [1-10]. These studies covered power generation and transmission sides of the grid. However, to achieve exact control, power should also be monitored at the distribution systems. Considering number of consumers at the distribution side, integration of power quality monitoring devices on everywhere would be difficult and expensive. Therefore, the device to be developed should be able to monitor geographically adjacent consumers simultaneously, while preserving low cost characteristic.

When Turkish low voltage side topology is examined, there exists 12 feeders at the transformer substations at most. The system should monitor these feeders and two sides of the transformer. This topology and how many channels to be measured at the same time is explained in Figure 1.1. Therefore, the system should monitor 64 channels (or sources) and calculate 48 of them except for neutral channels.

These issues construct the objective and motivation of this study which is designing and implementing real-time, high-performance, low cost power quality monitoring device which is capable of measuring 64 channels and calculating standard-defined power quality parameters of 48 channels at the same time, while being suitable for previously developed and integrated Power Quality monitoring systems in generation and transmission sides of the grid.

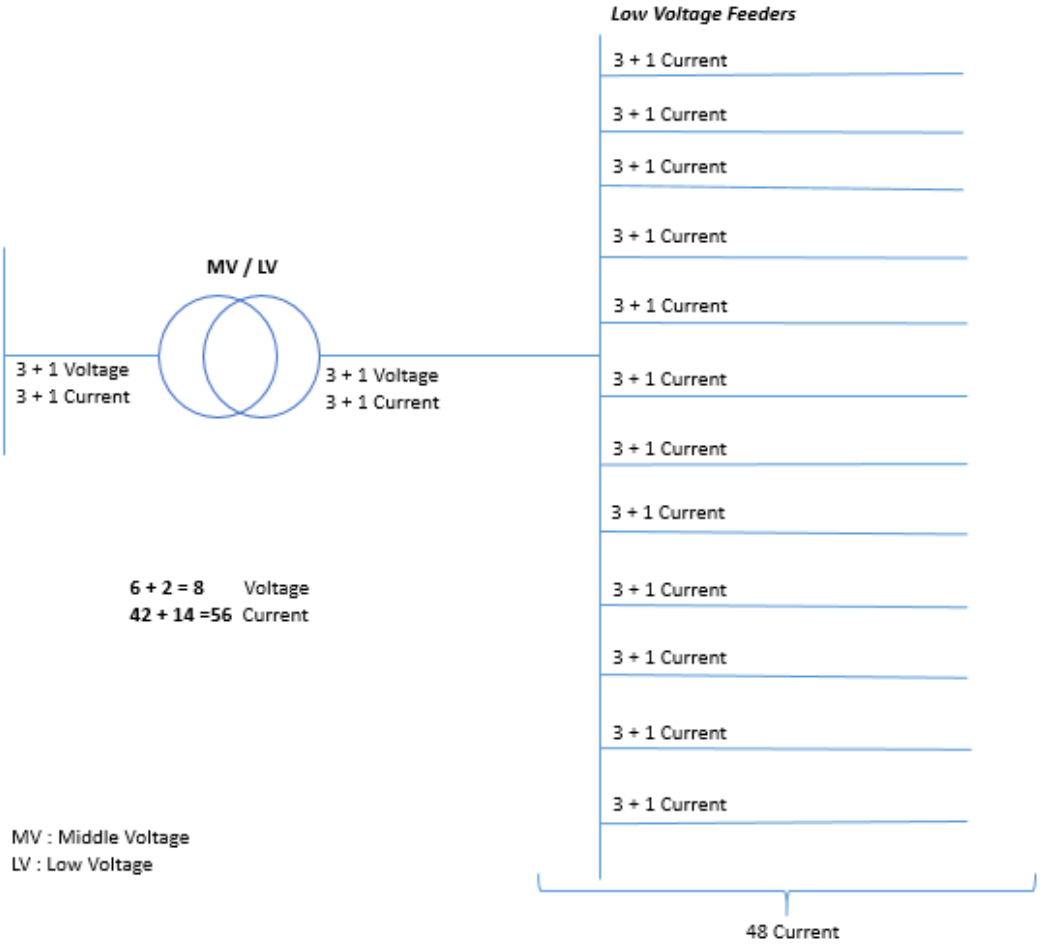

Figure 1.1: Turkish Distribution System Topology

When the previous studies on this subject are examined, it can be observed that implementing power quality monitoring device for this much of channels at the same time to calculate this much of parameters have not been attempted yet. Chapter 2 discussed the complexity of the problem at hand and provides the explanations of measured power quality parameters' signal processing algorithms.

In Chapter 3, overall system architecture design steps are given and block diagram of the overall system is clarified and sub-systems of the design are defined.

Chapter 4 consists of implementation details of power quality parameters. Algorithms are constructed and implemented on FPGA in accordance with specified requirements of the system.

The sub-systems and the overall design are evaluated in terms of accuracy, timing requirements and resource utilization. Designed tests and test data are given in Chapter 5 along with evaluation results.

Finally, the thesis is ended with our conclusion and future work in Chapter 6.

CHAPTER II

BACKGROUND AND LITERATURE REVIEW

2.1 Signal Processing Algorithms of Power Quality Devices (PQD)

End-users of the distribution systems want to know the quality of the power they get. Why their lights flicker, what affects their equipments' lifetime and what causes overheating in their power electronic devices, etc. are important questions for them and they can get answers to these questions with a power quality monitoring device which is specifically designed for distribution systems.

Power Quality is defined by the International Electrotechnical Comission (IEC) in the standard IEC 61000-4-30 [14] as follows: it is the behavior of the electricity at a given point on an electrical grid, evaluated against a set of technical parameters that are defined in the standards. The measurement methods and uncertainties for these parameters are also defined in the above standard and categorized into three classes (A, B and S).

The standard-defined parameters included within the scope of this study are listed below:

- Power Frequency
- Magnitude of the Supply Voltage
- Supply Voltage Dips and Swells
- Voltage Interruptions
- Voltage and Current Harmonics
- Underdeviation, Overdeviation, and Crest Factor
- Supply Voltage Unbalance

- Active, Reactive, and Apparent Power

2.1.1 Power Frequency

Power frequency of the system is a result of rotation of electrical machines and motors [11]. For steady and synchronously connected systems, all machines rotate at the same speed and standard frequency can be obtained. However, minor speed variations between the electrical machines and changes in the load cause variations in the frequency.

The power frequency variations in large grids are small. Frequently, the frequency of the supply voltage is very similar to the frequency of the power system. Throughout a disturbance, the result of a power system frequency measurement is between about 49.3 and 50.4 Hz as shown in Figure 2.1 [11]. The question arises whether this kind of variation will have a major negative effect on distribution systems or not. Standard motors which are employed for instance in household appliances could operate with any supply voltage frequency. Induction motors such as the ones used in refrigerators will operate at various speeds according to the power frequency however, a major increase in frequency may lead saturation of the induction motor, which could then get overheated [12,13].

According to the standard [14], power system frequency calculation should be done every 10 seconds. Calculation method is defined as the accumulative duration of integer cycles during 10 seconds divided by the number of the integral cycles. In addition, the effects of multiple zero crossing shall be attenuated. Also, for Class A where precise measurements are necessary, the measurement uncertainty of power frequency shall not exceed ±10 mHz.

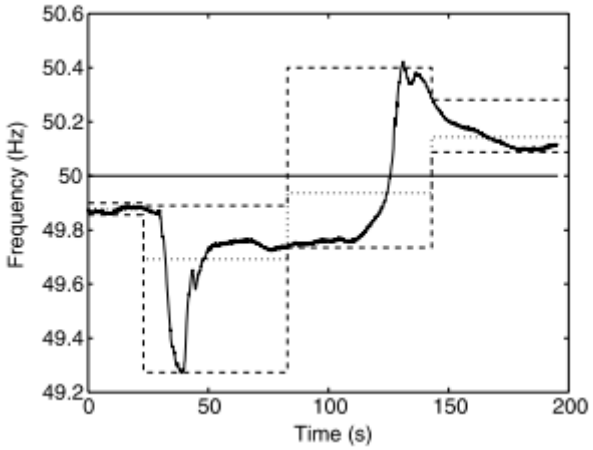

Figure 2.1: Frequency Variation Example Measured in Transmission System

2.1.2 Magnitude of the Supply Voltage

A balanced three-phase AC (Alternating Current) sinusoidal voltage waveform is shown in Figure 2.2 and defined with the following equations.

$$V_a(t) = \sqrt{2}\,V\cos(2\pi ft + \varphi)$$

$$V_b(t) = \sqrt{2}\,V\cos(2\pi ft + \varphi - 120°)$$

$$V_c(t) = \sqrt{2}\,V\cos(2\pi ft + \varphi + 120°)$$

where

f: Voltage frequency

V: Voltage magnitude

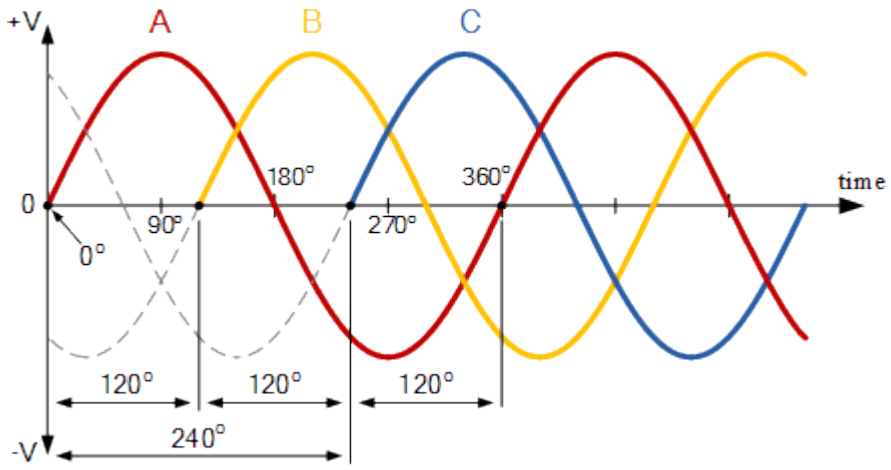

Figure 2.2: Three-phase Voltage Waveform

The RMS (Root Mean Square) value of the voltage is defined as the magnitude of the supply voltage according to IEC 61000-4-30 [14].

Variations in voltage magnitude which is V in Equation 2.1 can affect the performance and functionality of the equipments in distribution systems. Any overvoltage, which will be defined as voltage swell later, can cause insulation failure in long-term. Undervoltages, which will be defined as voltage sag later, could lead to reduced starting torque and overheating during full-load operation. The light output and lifetime of incandescent lamps are directly affected by voltage magnitude [11]. Because of these effects of variations in the magnitude of the supply voltage, the associated parameter is included in various standards. According to IEC 61000-4-30, the calculation shall be the Root Mean Square value of magnitude of the supply voltage over 10-cycle time interval for 50 Hz power systems. Aggregation method is also defined in the standard.

2.1.3 Supply Voltage Dips and Swells

A short-duration of under-voltages are defined as voltage dips or voltage sags. Voltage dip is a reduction in the magnitude of the supply voltage followed by a recovery after a short period of time. Voltage dip is defined for poly-phase systems in IEC 61000-4-

30 as follows: a voltage dip starts when the RMS input voltage of the channels is below the pre-defined dip threshold and ends with the URMS (value of the RMS voltage measured over one cycle) voltage on all the phases are equal to or above the voltage dip threshold plus the hysteresis voltage. The duration of a voltage dip is defined as the time difference among the start time and the end of time of the voltage dip [14]. Generally, threshold for voltage dip is defined as 90% of its stable RMS value. Voltage dip is shown in Figure 2.3 [15].

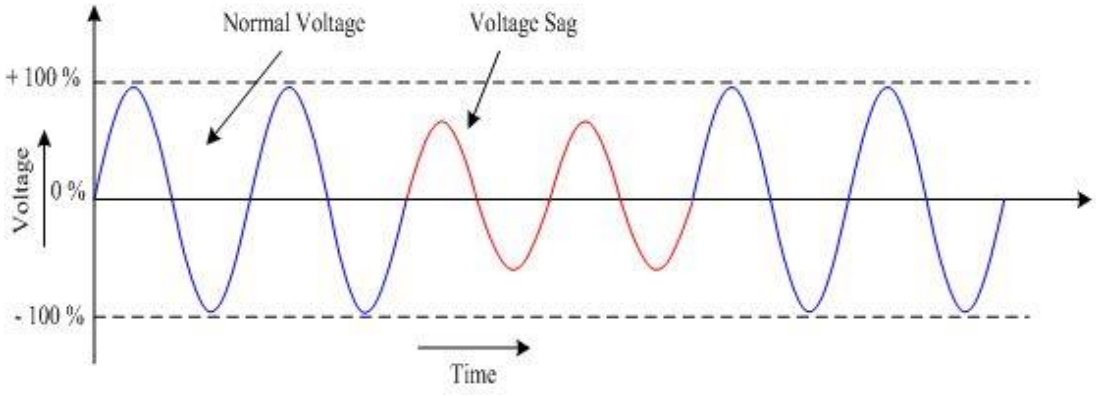

Figure 2.3: A Voltage Dip

A short-duration of over-voltages are defined as “Voltage Swells”. Voltage swell is an increase in the magnitude of the supply voltage followed by a recovery after a short period of time. Voltage swell is defined in the standard IEC 61000-4-30 as follows: a voltage swell begins with magnitude of the input supply voltage of the phases are above the pre-defined swell threshold and ends when the magnitude of the supply voltage on all phases are equal to or below the swell pre-defined threshold. The duration of a voltage swell is the time difference among the beginning and the end of the voltage swell [14]. Generally, threshold of voltage dip is defined as 110% of stable value of the magnitude of the supply voltage. Voltage swell is shown in Figure 2.4 [15].

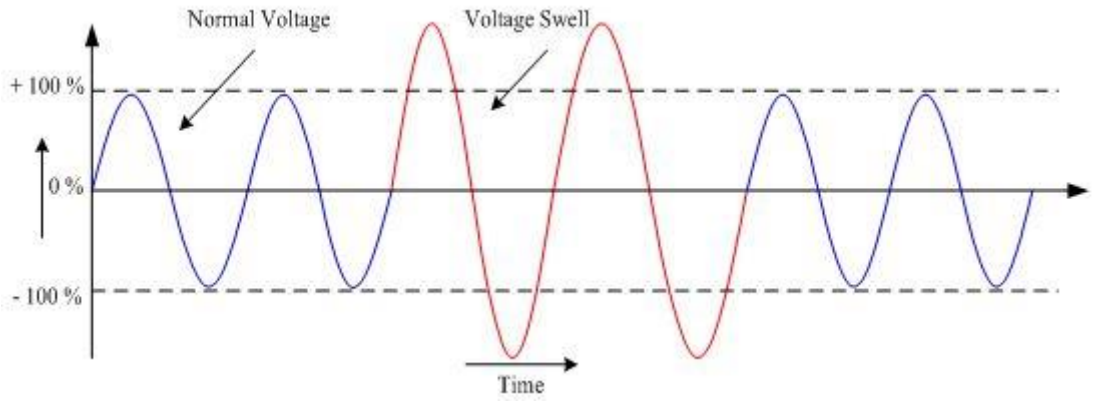

Figure 2.4: A Voltage Swell

As mentioned in 2.1.2, variations in the magnitude of the supply voltage can affect the lifetime and performance of equipments. Therefore, voltage dips and swells are considered as power quality parameters and their measurement method and uncertainty are defined in the IEC 61000-4-30. For Class A, the basic measurement U_{rms} of a voltage dip and swell shall be performed every half-cycle on each measurement channel. The cycle duration depends on the frequency of the system. The measurement uncertainty shall not exceed ±0,2 % of U_{din} [14].

2.1.4 Voltage Interruptions

Voltage interruption is defined in the standard IEC 61000-4-30 for poly-phase systems as follows: a voltage interruption begins when the magnitude of the supply voltages of all phases fall below the pre-defined voltage interruption threshold and ends when the magnitude of the supply voltage on any one phase is equal to or greater than the pre-defined voltage interruption threshold. The duration of a voltage interruption is the time difference among the beginning and the end of the voltage interruption. The voltage interruption threshold is set by the user of the monitoring system [14]. Voltage interruption is shown in Figure 2.5 [16].

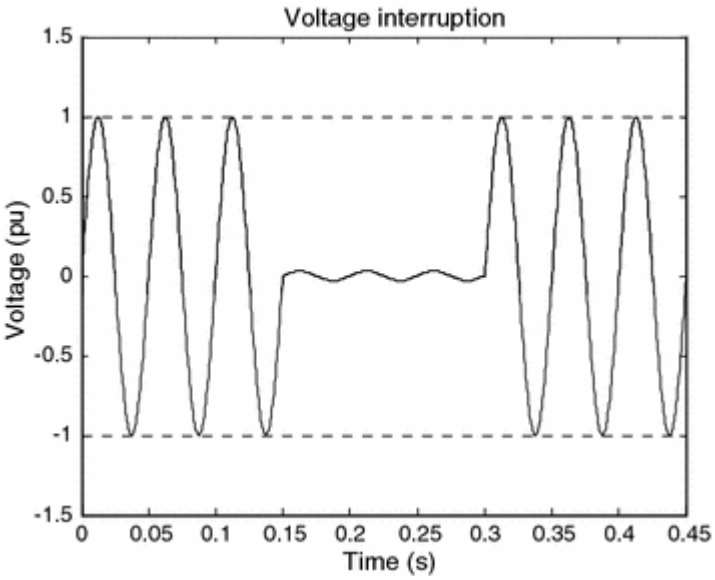

Figure 2.5: A Voltage Interruption

2.1.5 Voltage and Current Harmonics

In distribution systems, waveforms of the supply voltage and current are assumed not to be sinusoidal shape. The waveform is composed of various sine-waves with different magnitudes, phase angle, and frequency. However, their frequencies are integer multiples of the system frequency.

Waveform distortion is caused by non-linear elements in the power system. Non-linear elements take non-sinusoidal currents for sinusoidal voltages. Therefore, the current waveform through a non-linear element gets distorted. These non-linear elements could be transformers, arc furnaces, halogen lights, and power electronics components such as HVDC links, Flexible ac Transmission System (FACTS) devices, ASDs, and switched mode power supplies [11]. Consequences of waveform distortion can be listed as [17]:

- Resonance,
- Unstable neutral phase,

- Equipment and component overheating,
- Performance reduction in electric machines' operations,
- Electromagnetic interference with communication systems,
- Overloaded capacitors.

In electrical distribution systems, odd number of harmonics are dominant. Even number of harmonics have less effect on waveform distortion. Modern rules on harmonic distortion state that equipment should not generate any even harmonics. A typical waveform affected by odd number of harmonics is given in Figure 2.6 [18].

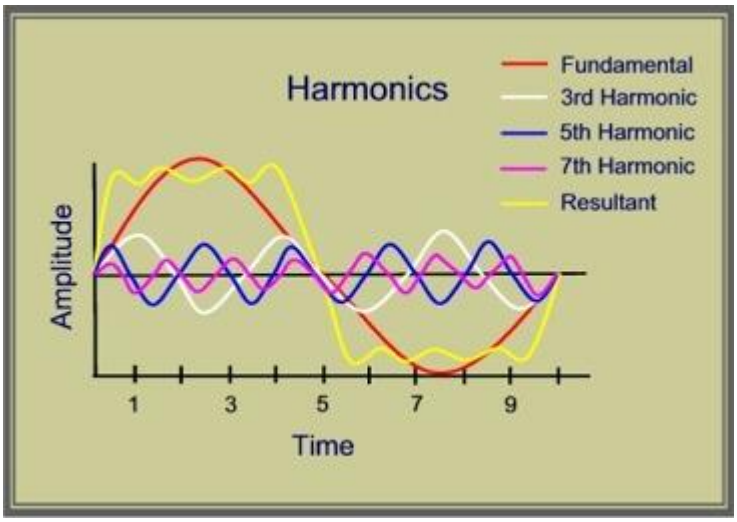

Figure 2.6: Waveform Affected by Odd Number of Harmonics

Measurement method and uncertainty of harmonic distortion are standardized in IEC 61000-4-30 [4] and IEC 61000-4-7 [19].

2.1.6 Underdeviation, Overdeviation and Crest Factor Parameters

Underdeviation, overdeviation and crest factor parameters are calculated to obtain how much the waveform is distorted. Measurement method of these parameters are defined in power quality standards.

The overdeviation is defined as;

- If $U_{rms\text{-}200ms,i} < U_{din}$ then $U_{rms\text{-}over,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \geq U_{din}$ then $U_{rms\text{-}over,i} = U_{rms\text{-}200ms,i}$

The underdeviation is defined as;

- If $U_{rms\text{-}200ms,i} > U_{din}$ then $U_{rms\text{-}under,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \leq U_{din}$ then $U_{rms\text{-}under,i} = U_{rms\text{-}200ms,i}$

where

$U_{rms\text{-}200ms,i}$: 200 ms aggregated RMS result

U_{din} : Declared supply voltage by a transducer ratio

$U_{rms\text{-}over,i}$: Overdeviation result

$U_{rms\text{-}under,i}$: Underdeviation result

Underdeviation and overdeviation measurements are only defined for Class A [14].

Crest factor is a time-domain parameter which indicates distortion on the top of the waveform. It is defined as the ratio of the amplitude of the signal and its magnitude [11]:

$$C_r = \frac{V_{max}}{V_{rms}}$$

2.1.7 Supply Voltage Unbalance

In this section, the variations in voltage between the phases in poly-phase power systems is discussed. Supply voltage unbalance exists when magnitudes of the line voltages or the phase angles between consecutive lines are not equal.

Supply voltage unbalance is caused by;

- Enormous individual loads operating single-phase,
- Faulty distribution of these single-phase loads by the multiple phases of the poly-phase systems [17].

In high-voltage and medium-voltage networks, most of the loads are three-phase loads. However, in distribution systems, single-phase loads have more importance [11]. Therefore, measurement of voltage unbalance is crucial. An example of unbalanced three-phase voltage is given in Figure 2.7 [20].

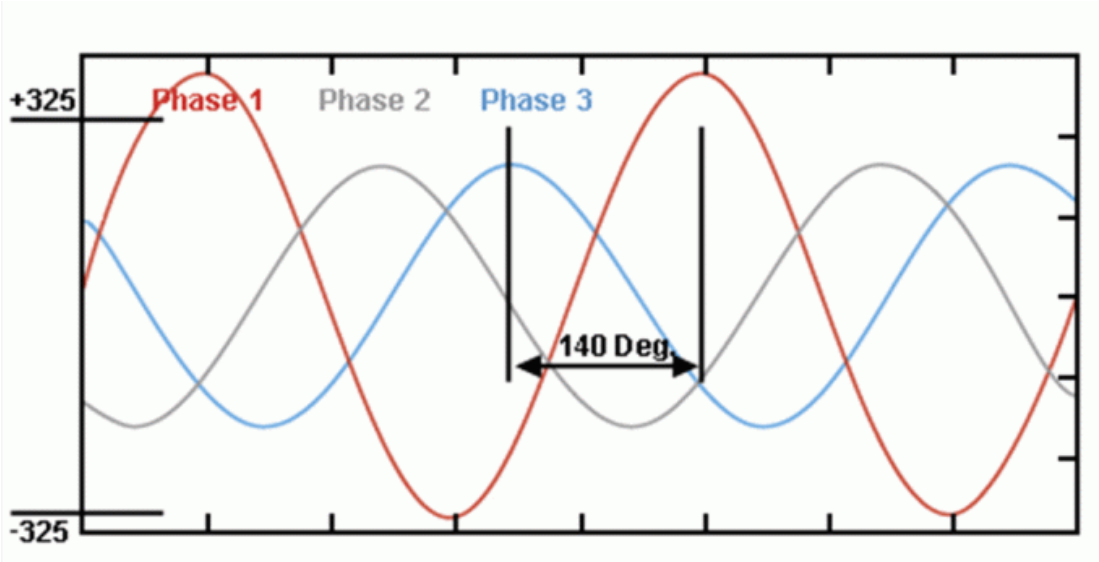

Figure 2.7: Unbalanced Voltage Waveform

Symmetrical components method is used for evaluating the supply voltage unbalance. Measurement uncertainty for Class A is defined in IEC 61000-4-30 [14].

2.1.8 Active, Reactive and Apparent Power

Electronic circuits are composed of three main elements: resistor, capacitor and inductor. Capacitors and inductors cause phase shift between current and the supply voltage. However, resistors cause no shift between them as shown in Figure 2.8. Power consumed on purely resistive loads is true power, measured in Watts.

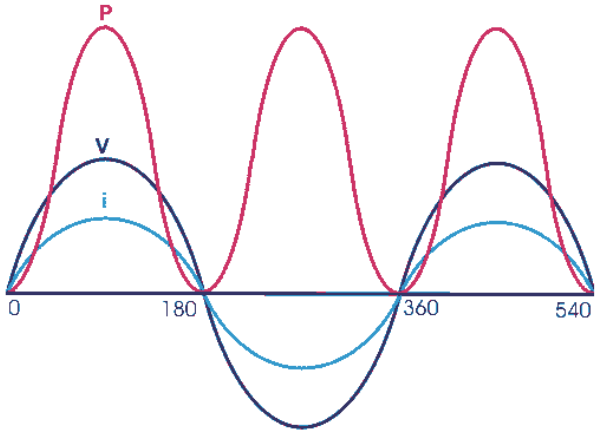

Figure 2.8: True Power

Power of loads consisting of inductors and capacitors is defined as reactive power and measured in Volt-Amper reactive (VAr). Current waveform leads the supply voltage waveform by 90 degrees and this results in negative reactive power in capacitive loads as shown in Figure 2.9.

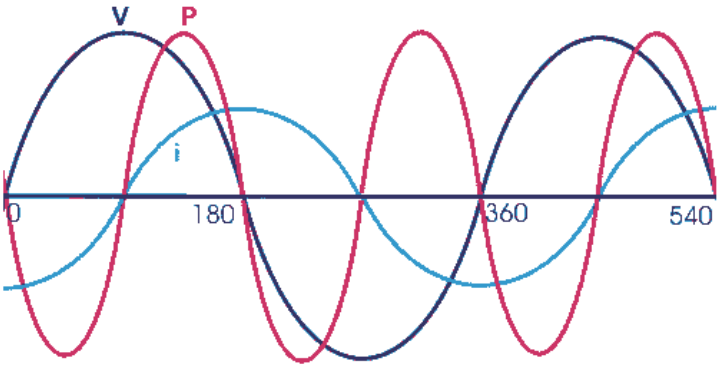

Figure 2.9: Inductive Power

On the other hand, if load is inductive, current waveform lags the supply voltage waveform by 90 degrees and the produced power is positive reactive power as shown in Figure 2.10.

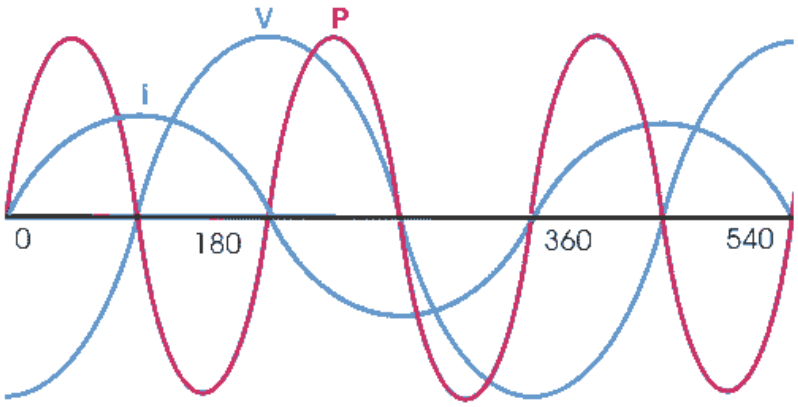

Figure 2.10: Capacitive Power

When the system has a load composed of resistors, capacitors, and inductors, the angle between voltage and current varies. This results in the combination of true and reactive power and forms apparent power, measured in volt amps (VA).

The formulas for the three types of power can be written as:

$$P = V\ I\ cos\theta$$

$$Q = V\ I\ sin\theta$$

$$S = V\ I$$

where

P: Active Power,

Q: Reactive Power,

S: Apparent Power,

V: Voltage Magnitude,

I: Current Magnitude,

θ: Angle among the supply voltage and current waveforms.

The relationship between these three types of power can be formulized in the following equations and shown in Figure 2.11.

$$P = \sqrt{S^2 - Q^2}$$

$$Q = \sqrt{S^2 - P^2}$$

$$S = \sqrt{P^2 + Q^2}$$

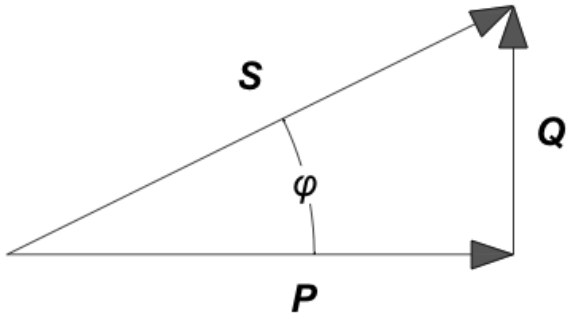

Figure 2.11: The Relationship between Apparent, Active and Reactive Power

Power measurement is not mentioned in the standard IEC 61000-4-30. However, it is included within the scope of the study.

2.2 Literature Study

Power Quality device for distribution systems should be able to operate with transmission network devices. In the scope of National Power Quality Project of Turkey, Power Quality devices are installed at the transmission network. Over the years, several studies are made for this project and proposed in [1-9]. Power Quality studies in Turkey is started by taking nationwide snapshots of the transmission system which is presented in [1]. PQ parameters are measured in accordance with IEC-61000-

4-30 at 205 different locations in the transmission system in [2]. After examination of field PQ data, a novel extensible database architecture is presented in [3]. Interharmonics and flicker measurements are comprehensively studied in [4] by focusing on iron and steel industry. A method for measuring light flicker based on Kalman filtering is presented in [5]. Nationwide real-time monitoring system for electrical quantities and power quality of the electricity transmission system is presented in [6]. The system defines an interface between transmission and distribution networks. The developed system has many capabilities such as measuring Power Quality parameters in distribution and transmission lines, detecting fault locations, GPS synchronization for harmonic phasor measurement and having a web-enabled national event recording system. The system calculates Power Quality parameters according to IEC 61000-4-30 and it is implemented on Mini-ITX motherboard. The outputs of the system are collected by National Monitoring Center for PQ (NMCPQ). Power Quality measurements at 601 points in the transmission system are stored in PQ database and are assessed in [7]. A Wind-Electric Power Monitoring and Forecast Center (WPMFC) which is composed of database, forecast software, data processing and application servers is presented in [8]. A Multipurpose Platform (MPP) for Power System Monitoring and analysis with sample grid applications is proposed in [9]. The system is capable of calculating Power Quality parameters according to IEC 61000-4-30, analyzing them, logging events, measuring synchronized phasors and identifying inter area oscillation. 450 devices had been installed until 2014. Each device is composed of a Mini-ITX motherboard, analog signal conditioning circuitry, digital I/O circuits, DAQ unit and GPS-based synchronization circuitry with current transducers.

Although Power Quality concept is studied over the years, implementing Power Quality Monitoring devices on FPGA is a relatively new application area [21 – 28].

An FPGA based Power Quality Monitoring System is proposed in [21]. The system is implemented in Xilinx Virtex 5 LX110T and evaluated at a transformer substation. The developed system is capable of calculating power frequency, magnitude of the supply voltage and current, current harmonics, active, reactive and apparent power and power factor.

An FPGA based Power Quality Monitoring using FFT method for single phase power metering is proposed in [22]. The system is implemented in Xilix Artix 7 evaluation board and evaluated by simulation. The developed architecture is capable of calculating 256-point FFT for current harmonics, phase angle, power factor and active, reactive and apparent power.

An online Electric Power Quality disturbance detection system is proposed in [23]. The system is implemented in Xilinx Virtex 5 LX110T FPGA and is evaluated at a transformer substation. It focuses on detecting voltage sags, swells and interruption parameters.

A novel concept of secondary substation monitoring is proposed in [24]. The developed system is capable of calculating current harmonics, voltage transients, phase-to-phase voltage estimation and detecting faulty phases, and faulty phase conductors.

An application-specific instruction set processor for Power Quality Monitoring is proposed in [25]. The design is implemented in Xilinx Kintex-7 70T FPGA by using a soft processor and is evaluated by simulation. The developed system is capable of calculating power frequency, magnitude of the supply voltage and current, and current harmonics.

An FPGA based smart sensor for detection and classification of Power Quality disturbances is proposed in [26]. The developed system consists of FPGA based processor and neural network for classification. It is capable of calculating current harmonics, transient voltages and detecting voltage sags, swells and interruption for 6 channels at the same time.

A smart sensor network for Power Quality monitoring in electrical installations is proposed in [27]. The system is implemented on Xilinx Spartan 6 FPGA and evaluated at a transformer substation. The developed architecture is capable of calculating power factor, current harmonics and detecting voltage sags, swells and interruption.

An FPGA based online Power Quality Monitoring System for electrical distribution network is proposed in [28]. The system is implemented in Xilinx Virtex 5 LX110T FPGA and evaluated at a transformer substation. The developed device is capable of calculating power frequency, current harmonics, power factor, active, reactive and apparent power while detecting voltage sags, swells and interruption parameters for 7 channels at the same time.

The designed architecture for this study is compared with the systems given in [21–28] with respect to their features and the comparison is presented in the following table.

Table 2.1: Comparison with Former Systems

	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	Thesis
Power Frequency	x				x			x	x
The Supply Voltage Magnitude	x	x			x			x	x
Supply Voltage Dips and Swells	x		x			x	x	x	x
Voltage Interruptions	x		x			x	x	x	x
Current Magnitude	x	x			x			x	x
Current Harmonics	x	x		x	x	x	x	x	x
Power Factor	x	x					x	x	x
Active, Reactive, Apparent Power	x	x						x	x
Voltage Harmonics									x
Voltage Unbalance									x
Current Unbalance									x
Underdeviation									x
Overdeviation									x
Crest Factor									x
Voltage Transients				x		x			
Number of Sources	NA	NA	NA	8	NA	6	NA	7	48

CHAPTER III

OVERALL SYSTEM ARCHITECTURE

Before constructing the overall architecture, requirements of the system should be defined clearly. These requirements can be related to the capabilities and features of the overall system, power quality parameters that will be measured and/or calculated, or relationships among the sub-systems. For the power quality monitoring system to be developed in this thesis, the requirements except for relationships are as follows:

- The system should be designed to be integrated into the distribution systems.
- The system should be working in real-time.
- The system should have enough ADCs for measuring all phases of 16 feeders.
- ADC resolution should be chosen to be compatible with IEC 61000-4-30 Class A uncertainties.
- The system should be capable of monitoring 16 feeders or 48 channels at the same time.
- The system should be capable of measuring and/or calculating the following quantities and power quality parameters;
    1. Power System Frequency
    2. Magnitude of the Supply Voltage
    3. Voltage Dips and Swells
    4. Voltage Interruption
    5. Voltage Harmonics
    6. Voltage Unbalance
    7. Underdeviation, Overdeviation, Crest Factor
    8. Magnitude of Current
    9. Current Harmonics

10. Current Unbalance
11. Active, Reactive and Apparent Power

- The system should be capable of storing the measured and/or calculated results of these quantities and parameters.

After defining these requirements, sub-systems are conceived as follows:

- Power Frequency Calculation Unit
- Magnitude Calculation Unit
- Harmonic Calculation Unit
- Phase Angle Calculation Unit
- Event Detection Unit, which includes voltage dips, swells and interruption
- Unbalance Detection Unit
- Power Calculation Unit
- Parameter Calculation Unit, which includes underdeviation, overdeviation and crest factor

This list then leads to determination of relationships among these sub-systems.

- Supply voltage should be filtered before calculating power frequency.
- Magnitude Calculation Unit should be capable of measuring both supply voltage and current.
- Harmonic Calculation Unit should be capable of calculating 1024-point FFT for both supply voltage and current.
- Phase Angle Calculation Unit should take frequency result as an input.
- Event Detection Unit should take magnitude of the supply voltage result as an input.
- Unbalance Detection Unit should take magnitude of the supply voltage and current, and phase angle results as an input.
- Power Calculation Unit should take magnitude of the supply voltage and current, and phase angle results as an input.

- Parameter Calculation Unit should take magnitude of the supply voltage as an input.
- All sub-systems should have control signals to provide handshaking mechanisms among other sub-systems.

These relationships between the sub-systems also form the dependencies among them and the dependencies lead to constructing the data flow and division of the computation into 4 steps as follows:

1st Step :

- Apply low pass filter to the supply voltage

2nd Step:

- Calculate magnitude of the supply voltage
- Calculate magnitude of the current
- Calculate harmonics of the supply voltage
- Calculate harmonics of the current
- Calculate power frequency

3rd Step:

- Calculate phase angle between the supply voltage and current
- Calculate phase angle between feeder's phases

4th Step:

- Detect events which are voltage dips, swells and interruptions
- Calculate active, reactive and apparent power
- Calculate other parameters which are underdeviation, overdeviation and crest factor
- Detect supply voltage unbalance
- Detect current unbalance

According to the determined data flow and the above steps, the overall system architecture is constructed as shown in Figure 3.1.

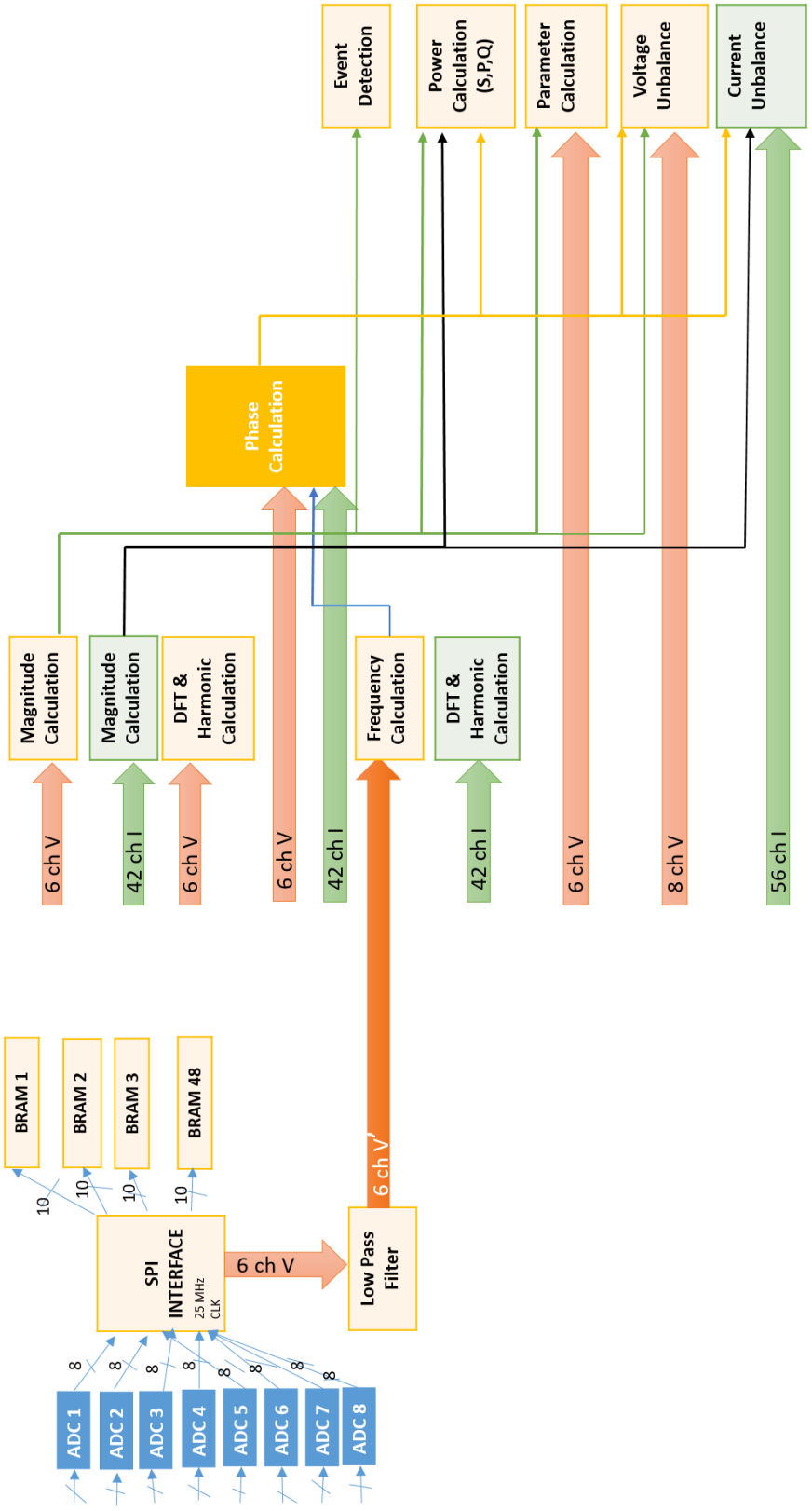

Figure 3.1: Overall System Block Diagram

CHAPTER IV

IMPLEMENTATION OF POWER QUALITY PARAMETERS ON FPGA

In this section, our implementation details of the algorithms of the selected power quality parameters of this thesis are explained. Presentation order of these parameters is based on relative complexities of the algorithms and the data flow among parameters as was defined in previous chapter.

4.1 Harmonic Calculation Unit

The Fast Fourier Transform (FFT) algorithm is used for the computation of discrete Fourier transform (DFT) of the supply voltage and current. Using FFT, we represent signals in frequency domain. By the frequency domain representation of the signals, integer multiples of the fundamental frequency can be obtained.

Harmonic calculation part of the study requires the heaviest computation among all power quality parameters. To optimize this computation, three different designs are implemented in different platforms.

4.1.1 Implementation on ARM

Since the target hardware in this study is Zynq, the first design is composed of ARM and FPGA. Cooley-Tukey FFT algorithm [29] is implemented on ARM with Ne10 library activation and the performance is evaluated. Computation result of 1024 point FFT for one channel takes about 55 milliseconds. The obtained result is printed on Xilinx SDK Software Serial Interface and given in the following figure.

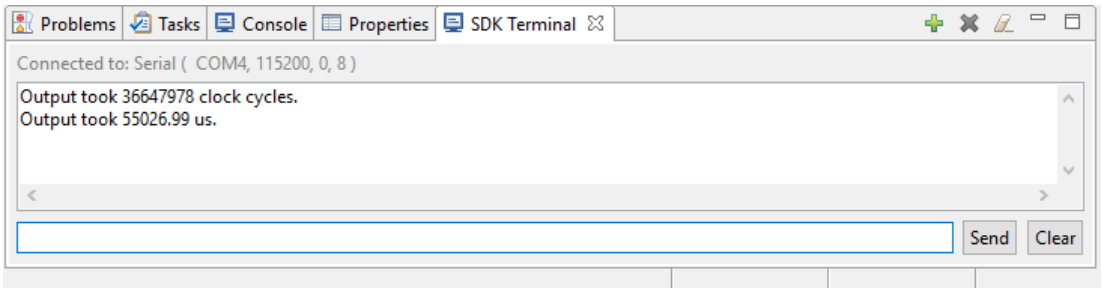

Figure 4.1: Result of Harmonic Calculation Implementation on ARM

The total operation time will then be 2.64 secs for all channels since ARM does not have parallel processing capabilities in bare metal mode of operation, but the total should not exceed 50 milliseconds for real-time operation. Hence, this design option is abandoned.

4.1.2 Implementations on FPGA

4.1.2.1 R2SDF Implementation

The most popular pipelined FFT architectures can be listed as follows:

- Radix-2Multipath Delay Commutator (R2MDC) [30]
- Radix-2 Single-path Delay Feedback (R2SDF) [31]
- Radix-4 Multipath Delay Commutator (R4MDC) [30]
- Radix-4 Single-path Delay Feedback (R4SDF) [32]

For 16-point decimation in frequency (DIF), these architectures are shown in the following figures [33] (C: commutator, BF: butterfly). In DIF algorithm, the decimation is handled in the frequency domain and the complex multiplication (blue Xs in the following figures) takes place after butterfly's addition and subtraction operations.

In R2MDC architecture as shown in Figure 4.2, in each stage, half the data stream of incoming data is delayed by a memory or shift register and processed with the second half data stream.

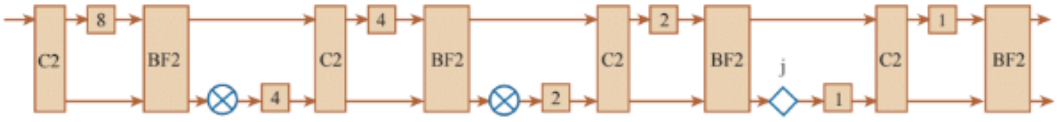

Figure 4.2: R2MDC Architecture

In R2SDF architecture as presented in Figure 4.3, the memory is first used to save the first half of the input data stream and then delay output data. A single data stream goes through the multiplier at every stage.

Figure 4.3: R2SDF Architecture

R4SDF is similar to R2SDF but consists of Radix-4 butterflies and uses 3 memory blocks to save 3 parts of the input data at each stage as given in Figure 4.4.

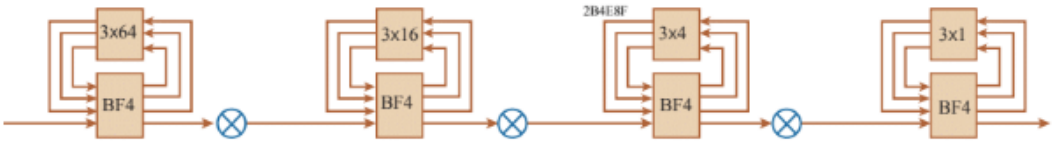

Figure 4.4: R4SDF Architecture

R4MDC architecture is similar to R2MDC but consists of Radix-4 butterflies and uses 3 shift registers at each stage as shown in Figure 4.5.

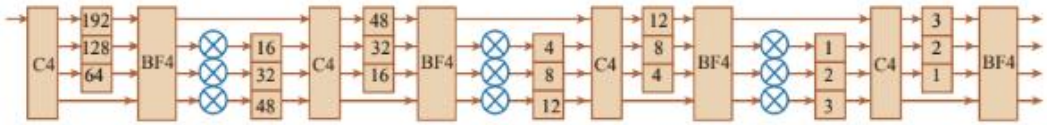

Figure 4.5: R4MDC Architecture

The study in [34] compares these architectures and identifies R2SDF to have the lowest memory demand. R2SDF is also chosen for our implementation in this thesis.

1024-point R2SDF architecture consists of functionally similar ten ($\log_2 1024$) stages. First stage's input data is 1024 consecutive samples of raw data. This data is input to FFT module one by one on each rising edge of the clock input of the module. Second stage's input data is the output of the first stage, and so on. The output data of the last stage is the result of the FFT module.

One stage consists of four modules which are Butterfly, FIFO, Coefficient ROM and Multiplier as shown in Figure 4.6 for the first stage of 1024-point FFT.

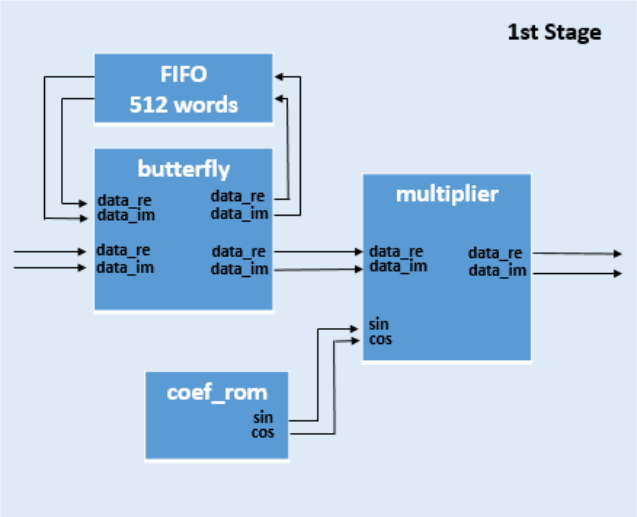

Figure 4.6: First Stage of 1024-point FFT Algorithm

Butterfly module takes input data and starts counting. A butterfly in m^{th} stage of total n stage counts until $2[\log_2(n-m)]$. Let's name this limit CNT_MAX. If input data's index is lower than CNT_MAX, butterfly passes data to FIFO. If input data's index is bigger than CNT_MAX, butterfly adds its real part to FIFO output's real part and subtracts its imaginary part from FIFO output's imaginary part. This way it prepares data at the specified point in the following figure which is prepared for 8-point FFT for simplification.

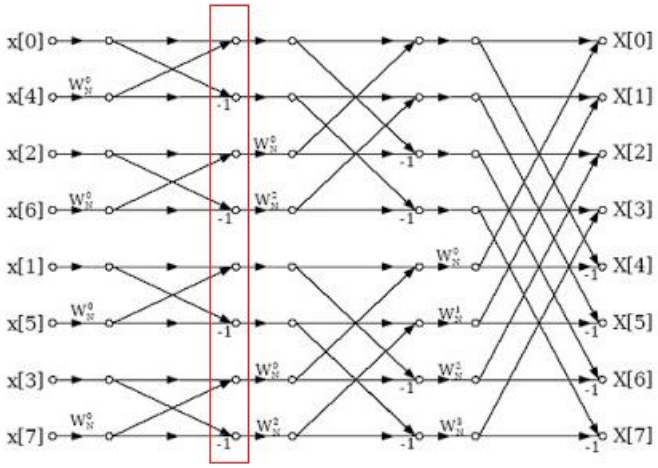

Figure 4.7: Butterfly Module (N=8)

Calculating every coefficient during execution will slow the operation down. That's why all coefficients are calculated ahead and stored in RAM. Coefficient ROM module counts input data for specifying index, then outputs related coefficient.

Multiplier module takes Butterfly's and Coefficient ROM's outputs and multiplies. It prepares data at the specified point in the following figure. Because FPGA has DSP resources in the slices, this module calculates the result in one clock cycle. After calculation, it passes the result to next stage's Butterfly module.

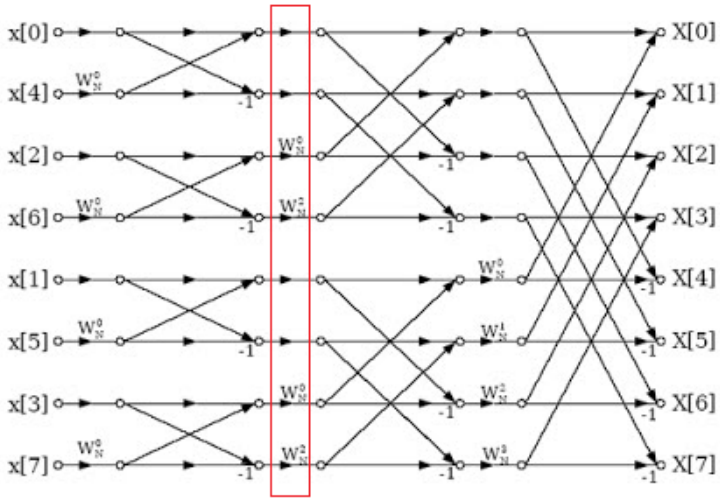

Figure 4.8: Multiplier Module

Top module block design of FFT module is given in the following figure.

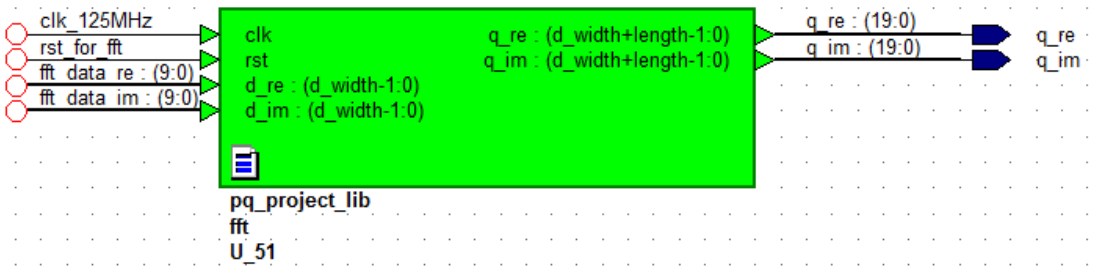

Figure 4.9: FFT Module Block Design

One channel 1024-point R2SDF DIF FFT algorithm post-implementation resource utilization result is given in Table 4.1. Operating frequency of the design is obtained as 125MHz. Hence clock period is 8 ns. Delay of the design is about 1034 clock which is based on delay on FIFOs and number of stages. By implementing 48 FFT Calculation modules, total processing time can be calculated as: [1024 + 10 + (512 + 256 + 128 + … + 1] * 8 ns = 16464 ns which is sufficient for the required real-time operation. Only problem with this design is the DSP use (4%) hence we can only support 25 channels. By forcing the synthesizer to limit the DSP utilization, we can force the system to use LUTs for multiplication. In this case, LUT utilization is so high that total resources are not enough for 48 channels. Hence, this design is abandoned too.

Table 4.1: R2SDF Resource Utilization (N=1024)

Resource	Utilization	Available	Utilization %
LUT	1642	218600	0.75
LUTRAM	168	70400	0.24
FF	492	437200	0.11
BRAM	6	545	1.10
DSP	36	900	4.00
IO	62	362	17.13
BUFG	1	32	3.12

4.1.2.2 Time Multiplexed R2SDF Implementation

Instead of implementing 48 FFT modules, one module can be used by all 48 channels in turn as shown in Figure 4.10 (Ch: channel).

After last sample of one channel leaves the pipeline structure, the first sample of the next channel can enter the pipeline. If reset time and other control mechanisms are taken into account, total processing time for the required time multiplexed R2SDF structure will be 48 * (1024 + 10 + 1024) * 8 ns = 794112 ns. It is more than enough for real-time operation. If calculation is reversed, 20 ms / [(1024 + 10 + 1024) * 8 ns] = 1208.89 channels can be supported with this design.

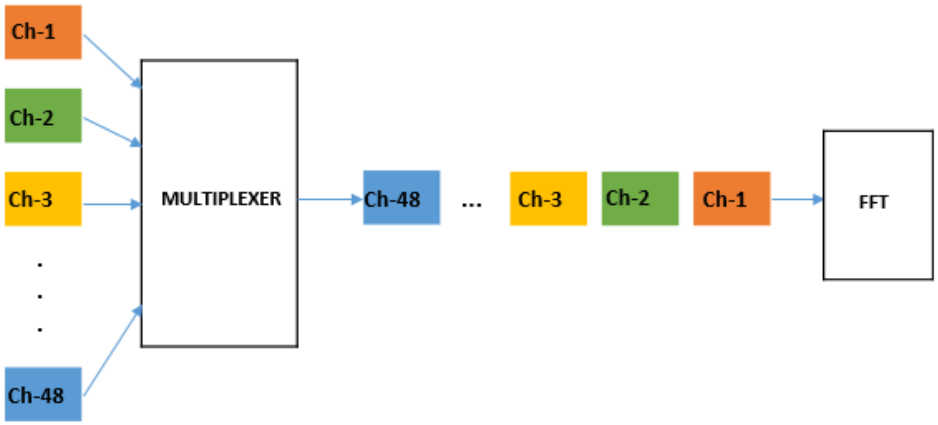

Figure 4.10: Time Multiplexed R2SDF Architecture

All channel data are stored in FIFOs which are implemented as BRAM. The advantage is that LUT resources are not exhausted. Data width of FIFOs is chosen as 2*1024 words. As soon as 1024 words are stored, multiplexer module starts the reading process from top to bottom. Channel-48 waits other channels for a total of 47*2*1034*8 ns = 777568 ns. Since, sampling frequency is 1024*50Hz = 51.2kHz, FIFO for Channel-48 can collect maximum 1024 + 40 samples. In this way, FIFOs will not be full, and data loss does not occur. Hence, real-time operation is satisfied. Multiplexer module's functionality is explained in Figure 4.11.

Post-implementation resource utilization of Time Multiplexed R2SDF architecture, which consists of 48 FIFOs, Multiplexer and FFT modules, is given in the following table.

Table 4.2: Time Multiplexed R2SDF Implementation Resource Utilization

Resource	Utilization	for Zynq ZC706 (%)
LUT	7727	3.53
LUTRAM	624	0.89
FF	10155	2.32
BRAM	50	9.17
DSP	36	4
IO	53	14.64

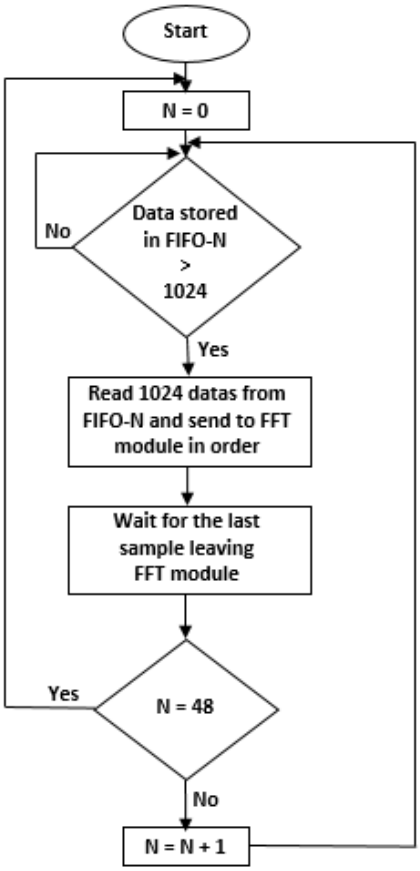

Figure 4.11: Multiplexer Module Algorithm

4.2 Power Frequency Calculation Unit

As was mentioned previously, the power frequency of the grid and the supply voltage frequency are very close terms. Supply voltage is affected from its harmonics. Before calculating voltage frequency, harmonic components should be eliminated. Thus, power frequency calculation unit is composed of a low pass filter module and a frequency calculation module.

4.2.1 Low Pass Filter Module

FIR low pass filter module is designed and implemented using the following equation:

$$y[n] = \sum_{i=0}^{N-n} b_i \, x[n-i]$$

where

$y[n]$: Output signal

$x[n]$: Input signal

N: The filter order

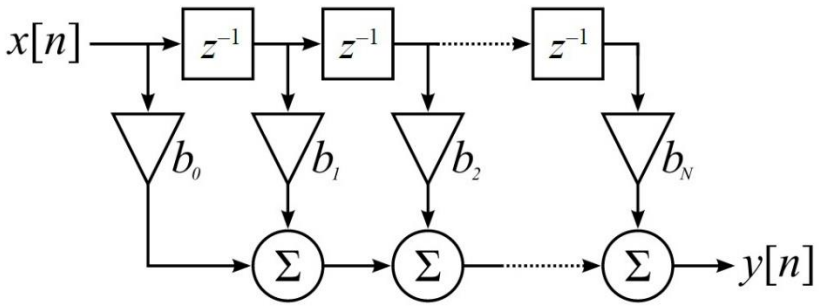

Figure 4.12: Nth order FIR Low Pass Filter with (N+1) Taps

In the designed filter, N is chosen as 3. Thus, the filter has 4 taps and creates 3 points phase shift. This phase shift should be eliminated to correctly calculate phase angles of the channels. Thus, filtered signal is shifted by 3 point for elimination.

Each sample of the input signal x[n] enters the delayline in order. They are multiplied with b coefficients and accumulated to form y[n] output signal. This FIR LPF method is chosen because it has no feedback and it is implemented in hardware very easily.

As a first step, the algorithm is implemented in MatLAB environment and tested. As test data, addition of a pure cosine signal, its harmonics and randomly produced noise signal is used as shown in Figure 4.13. On the right side of Figure 4.13, multiple zero crossings can be observed.

During the test, it is observed that negative and positive half cycle's duration and amplitude of the output signal are not equal. The output signal is not oscillating around zero because of randomly produced noise data. As a consequence, frequency calculation results are not correct. To solve this problem, DC component of the test data should be removed. This process is implemented before and after the low pass filter. Elimination after LPF gives less percentage error. The result is shown in Figure 4.14.

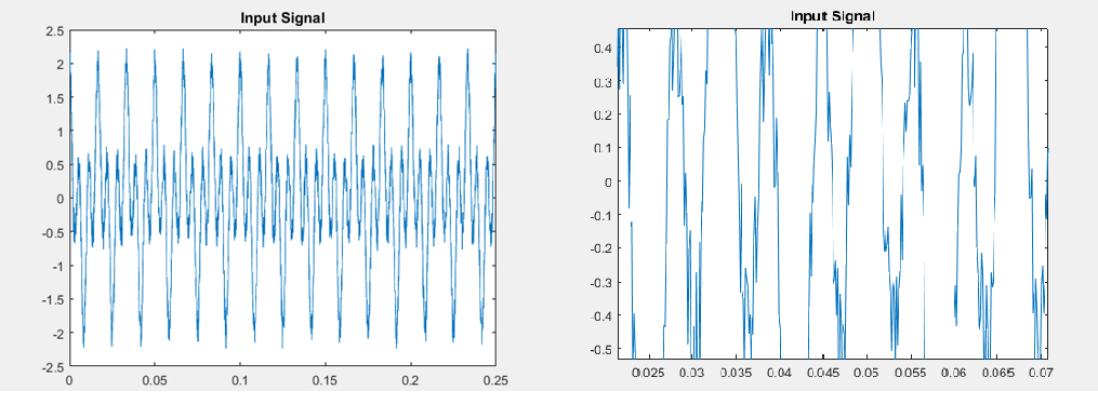

Figure 4.13: Input Test Signal

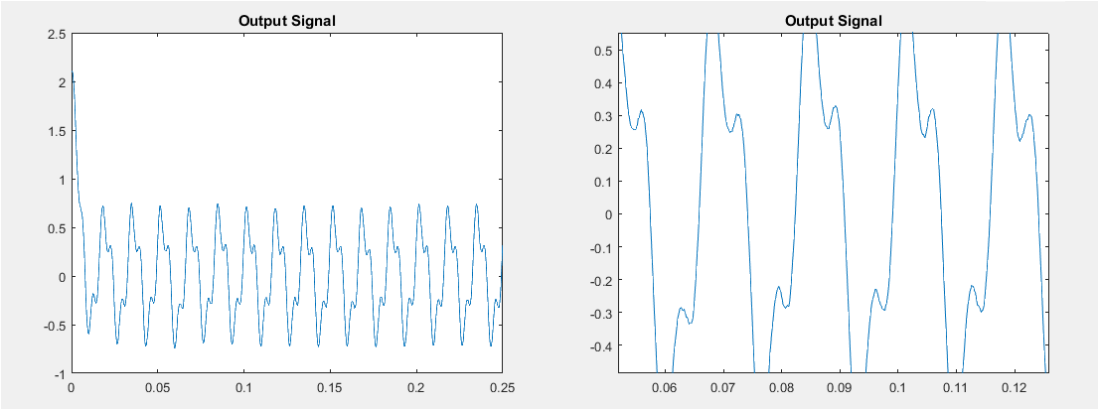

Figure 4.14: FIR LPF Output Signal

It is clear on the right side of the figure that multiple zero crossings are eliminated and the output signal is oscillating around zero.

4.2.2 Frequency Calculation Module

For frequency calculation, time difference between two zero crossings is measured as shown in Figure 4.15. For this measurement, MSB (Most Significant Bit) of the input data is monitored since the input signal is signed and the MSB indicates if it is negative or not. MSB changing from one to zero is detected.

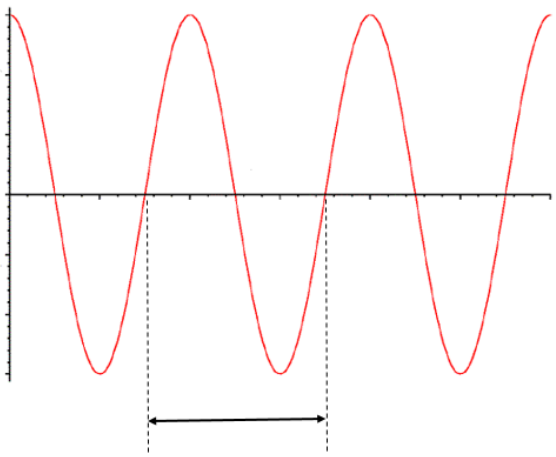

Figure 4.15: Example for Zero Crossings

For measurement of time difference between two zero crossings, a counter is defined. This counter starts counting after the first detection and keeps counting until detecting second zero crossing. The system frequency is the result of operating frequency divided by this counter. In this way, measurement uncertainty does not exceed 2 * operating frequency of the system. Flow chart for calculating frequency is given in Figure 4.16.

Block design of the implemented LPF and frequency measurement units are given in Figure 4.17 and Figure 4.18.

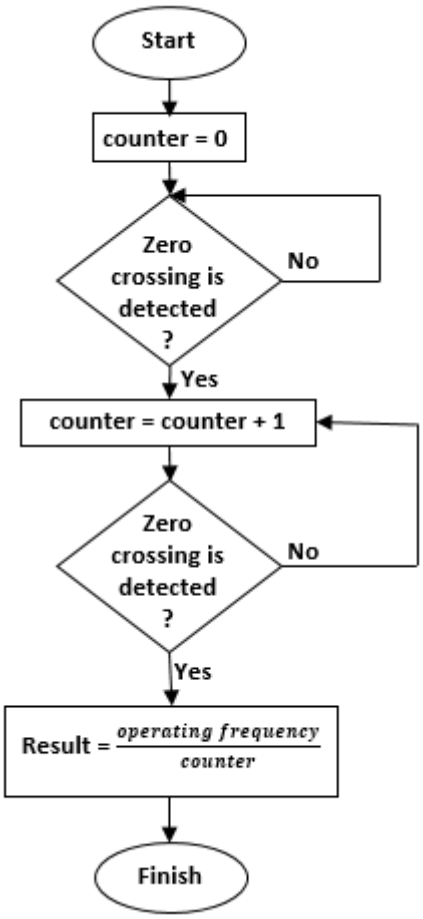

Figure 4.16: Flow Chart for Frequency Calculation

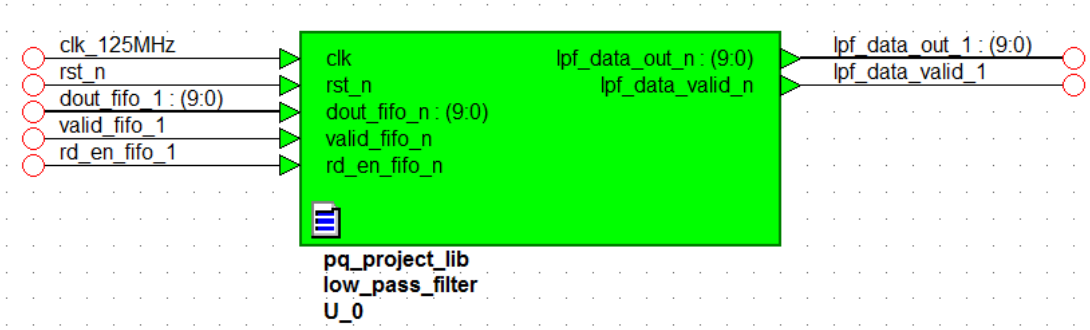

Figure 4.17: Block Design of Low Pass Filter Module

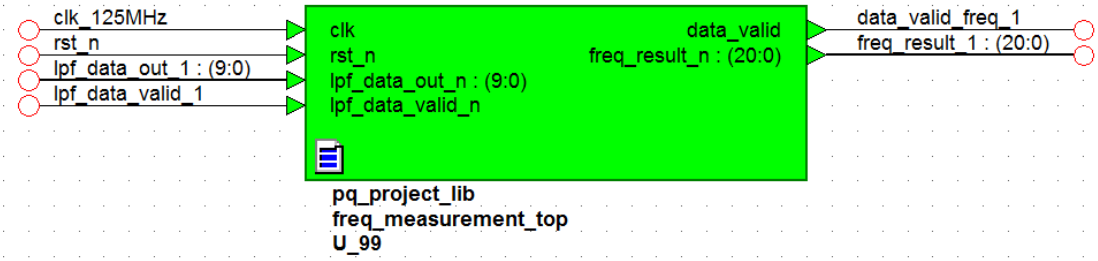

Figure 4.18: Block Design of Frequency Measurement Module

4.3 Magnitude Calculation Unit

Root Mean Square (RMS) values of both the supply voltage and current are calculated according to the following equations.

$$V_{rms} = \frac{1}{N}\sqrt{\sum_{k=1}^{n} {V_k}^2}$$

$$I_{rms} = \frac{1}{N}\sqrt{\sum_{k=1}^{n} {I_k}^2}$$

where

V_{rms}: Magnitude of the supply voltage

I_{rms}: Magnitude of current

V_k: kth sample of the supply voltage waveform

I_k: kth sample of current waveform

For this formulation, the flow chart shown in Figure 4.19 is constructed. For each step in the flow chart, a module is designed and implemented. Each module takes data from former module, processes the data, and send the result to the next one. For streaming data passing through multiple modules, valid signals are used for handshaking mechanisms. Designed architecture is given in Figure 4.20, Figure 4.21 and Figure 4.22. Designed architecture for magnitude calculation module is composed of 5 sub-modules. These sub-modules can be listed as;

- enable_rms_module
- signal_square
- adder_of_squares
- divider
- square_root

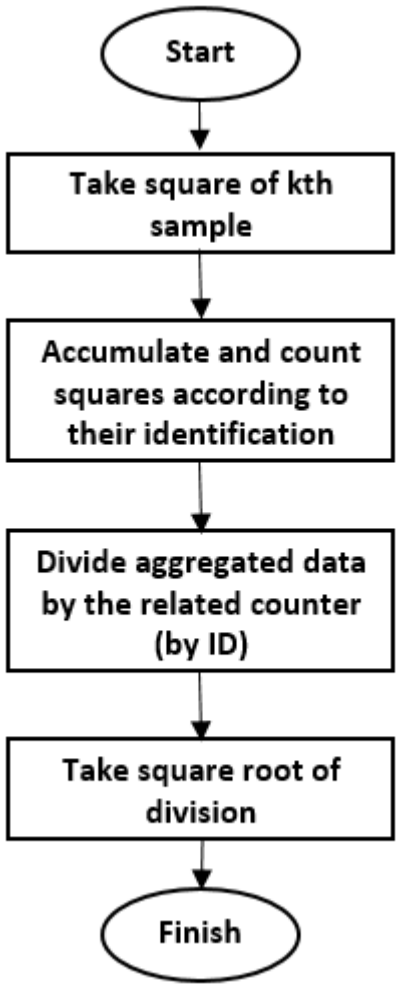

Figure 4.19: Flow Chart for Magnitude Calculation Algorithm

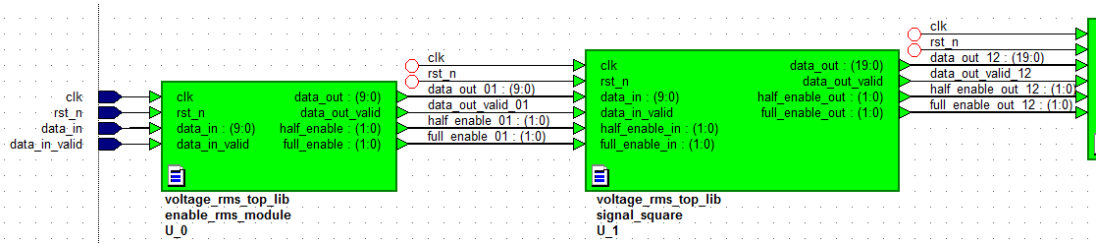

Figure 4.20: The First Part of Magnitude Calculation Module

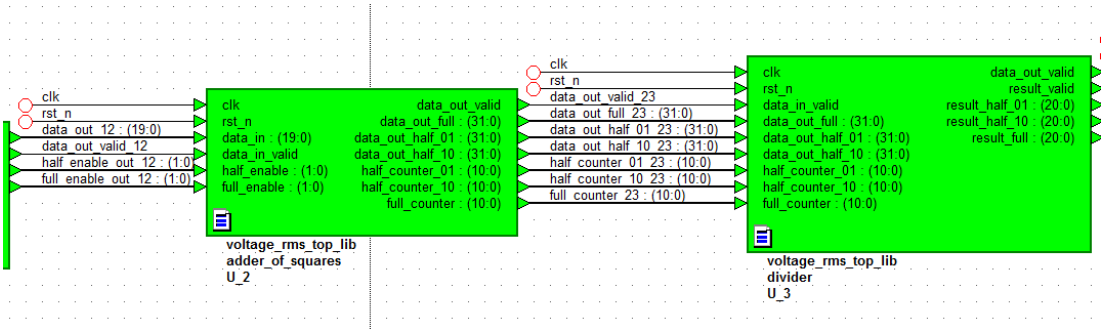

Figure 4.21: The Second Part of Magnitude Calculation Module

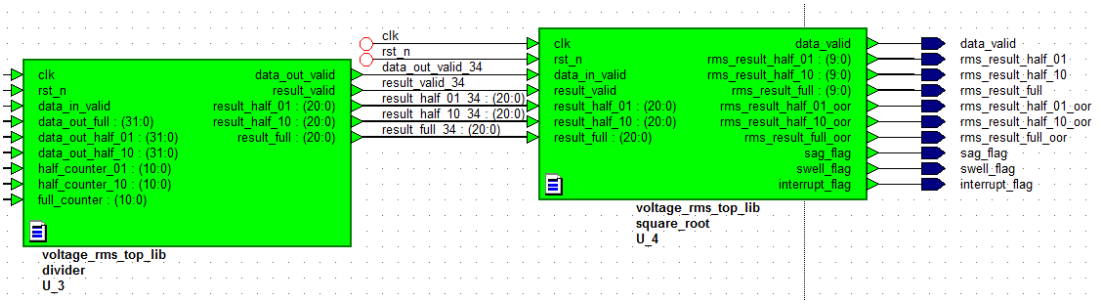

Figure 4.22: The Third Part of Magnitude Calculation Module

For parameters like supply voltage dips and swells, we use half cycle magnitude of the supply voltage. For continuous data coming from ADCs (Analog to Digital Converter), it is necessary to specify which sample belongs to which half cycle and full cycle, as they will be accumulated accordingly. 'enable_rms_module' takes incoming data, does identification, also enables rest of the module for starting processing. Half cycle identification is done according to data being negative or positive. Full cycle identification is just for separating consecutive cycles. This identification process is exemplified in Figure 4.23.

'signal_square' module waits enable signal from former module 'enable_rms_module', which asserts valid signal for enabling, and multiplies incoming data with itself irrespective of half and full identification. The result of this module is ready within one clock cycle, and valid signal is asserted to notify next module.

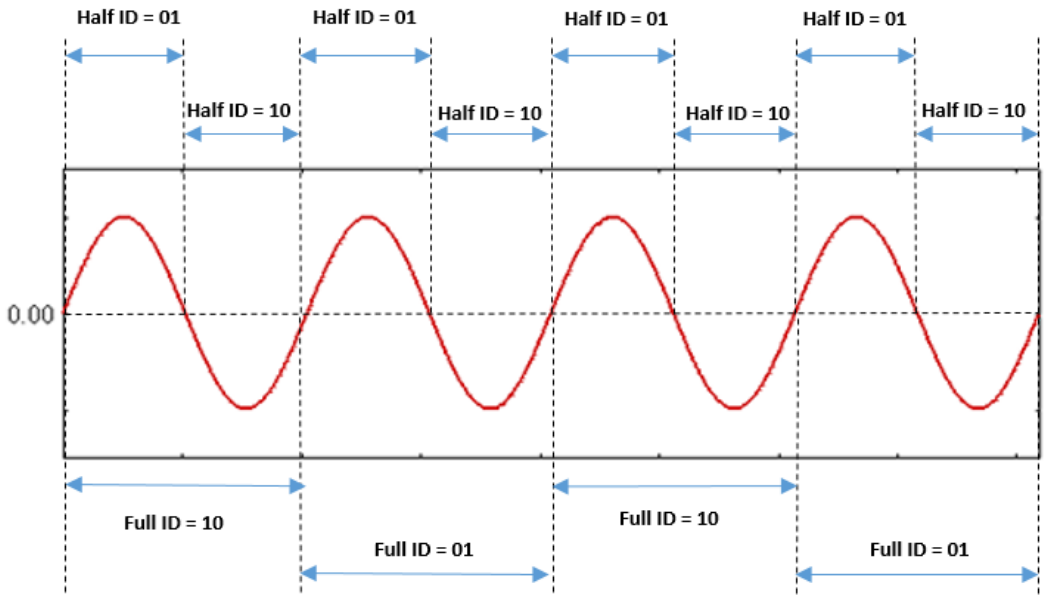

Figure 4.23: Half and Full Cycle Identifications

'adder_of_squares' module accumulates incoming data with respect to its half and full identification. Naturally, it prepares two half cycle and one full cycle aggregated output data for the next module.

This module also counts how many data is accumulated for each output data and asserts valid signal for the next module.

'divider' module waits for valid signal from former module. After 'adder_of_squares' asserts valid signal, 'divider' module divides accumulated data by the related counter.

'square_root' module consists of two RAMs. The first RAM contains square root results and the second RAM contains squares of these results. This module waits the valid signal from 'divider' and then, searches input data in the second RAM. After input data hits certain interval in the second RAM, result will be the related data in the first RAM.

4.3.1 Voltage Dips, Swells and Interruption

A module for calculation of voltage dips, swells and interruption is implemented under magnitude calculation unit to simplify the computation. This module takes square of the result and compares with RAM values. If square of the result is lower than the minimum number in the pre-calculated RAM, voltage dip flag asserts high. If square of the result is bigger than the maximum in the pre-calculated RAM, voltage swell flag asserts high. Maximum and minimum numbers in the RAM are thresholds, and specified as follows:

Voltage Dip Threshold = 220 – (220 * 0.1) = 198 V_{rms}

Voltage Swell Threshold = 220 + (220 * 0.1) = 242 V_{rms}

Thus, the RAM stores (242 – 198 + 1) numbers. Another threshold is defined for voltage interruption, and it is calculated as;

220 * 0.1 = 22 V_{rms}

Out-of-range flags are used for indicating which half-cycle or full-cycle caused the dip, swell, or interruption. These flags can be seen from the following figure, which shows the magnitude calculation unit's output ports.

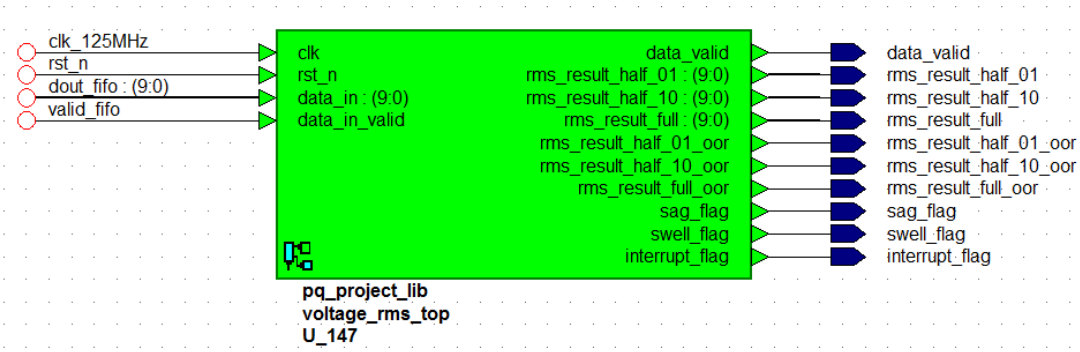

Figure 4.24: Magnitude Calculation Unit Block Design

4.4 Phase Calculation Unit

Before calculating active power, reactive power and apparent power, phase angle between the supply voltage and current should be obtained. Phase calculation unit consists of zero-cross module, phase difference module and phase calculation module.

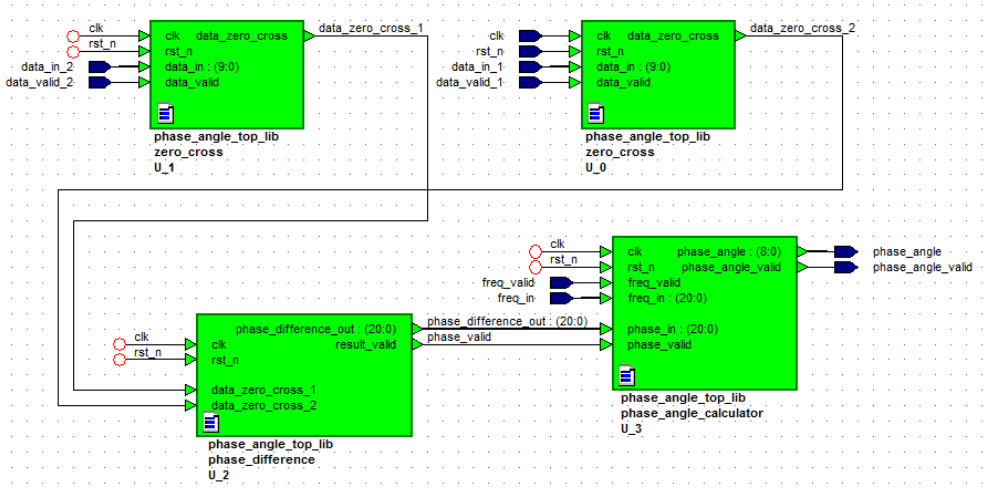

Figure 4.25: Modules of Phase Calculation Unit

Zero-cross modules wait until non-negative data and sets data_zero_cross output signals high. Phase difference module waits for data_zero_cross input signals' rising edges and counts and/or measures the time difference between these two inputs. Finally, phase angle calculator module takes the time difference from phase_difference module and frequency from power frequency calculator module and then divides these two and outputs phase angle result with valid signal. Algorithm for this process is explained in Figure 4.26.

For detecting unbalance on the supply voltage and current channels, phase angles between the three-phases should be obtained. Therefore, another module is designed with a similar algorithm, except for different number of inputs. This top module takes three phases of the supply voltage and current which belong to the same feeder, and calculates phase angle among these. Thus, this module outputs three phase angle

results, which are between first and second, first and third and second and third phases. Top module block design is given in Figure 4.27.

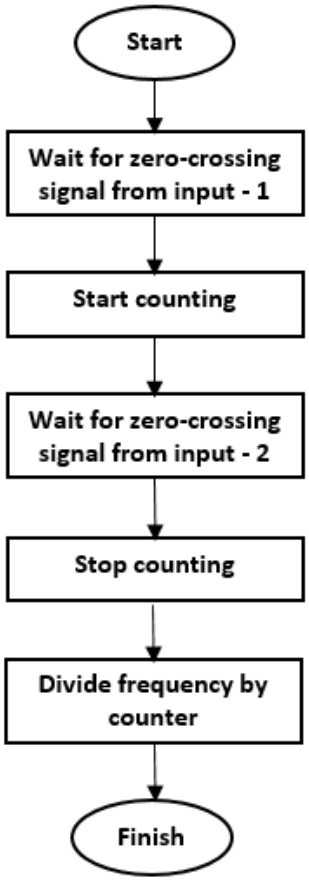

Figure 4.26: Algorithm for Phase Angle Calculation

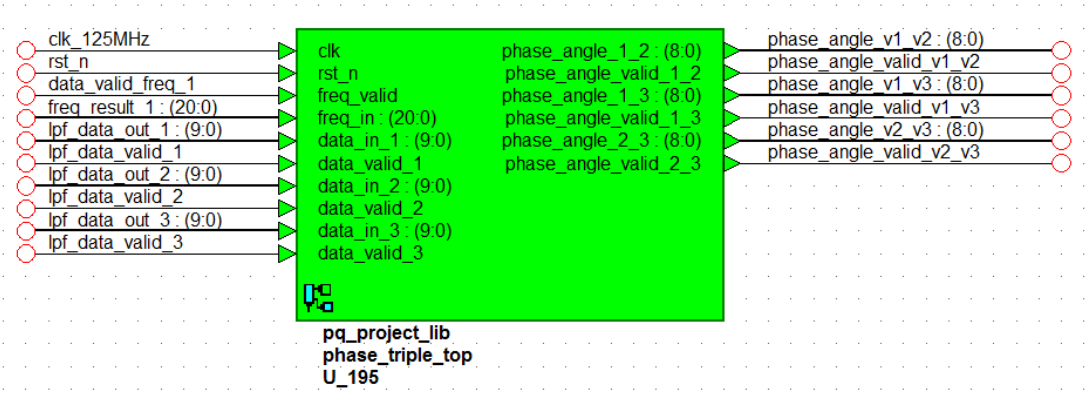

Figure 4.27: Phase Angle Calculation Top Module for Three-Phases

Input data for three-phases are outputs of Low Pass Filter module which receives input signal whose dc component is removed. Because, to calculate phase difference correctly, the inputs should not have multiple zero-crossings and should oscillate around zero.

4.5 Unbalance Detection Unit

Unbalance is the situation where the angles between three phases or the magnitude of the phases are not equal. For detecting unbalance on the supply voltage and current channels, outputs of Magnitude Calculation Unit and Phase Angle Calculation Unit for three-phases are taken as inputs. After the computation, three flags are asserted, which indicate unbalance existence and whether it is caused by magnitude or phase angle difference.

By the advantage of existing parallel processing capability in our platform, magnitude difference and angle difference among three-phases are detected individually. In case of results from other modules being not asserted at the same time, results are stored in registers with rising edge of valid signals

If there is a difference in either of them, unbalance flag is asserted high and if there is not a difference among phases in terms of both magnitude and phase angle, unbalance flag is asserted low. This is implemented as an OR gate. The algorithm for this computation is explained in Figure 4.28.

Input and output ports of Unbalance Detection Unit can be clearly seen in block design, which is given in Figure 4.29.

Unbalance Detection Unit is independent from the unique specifications of voltage and current channels. Therefore, one design is used for both the supply voltage and current.

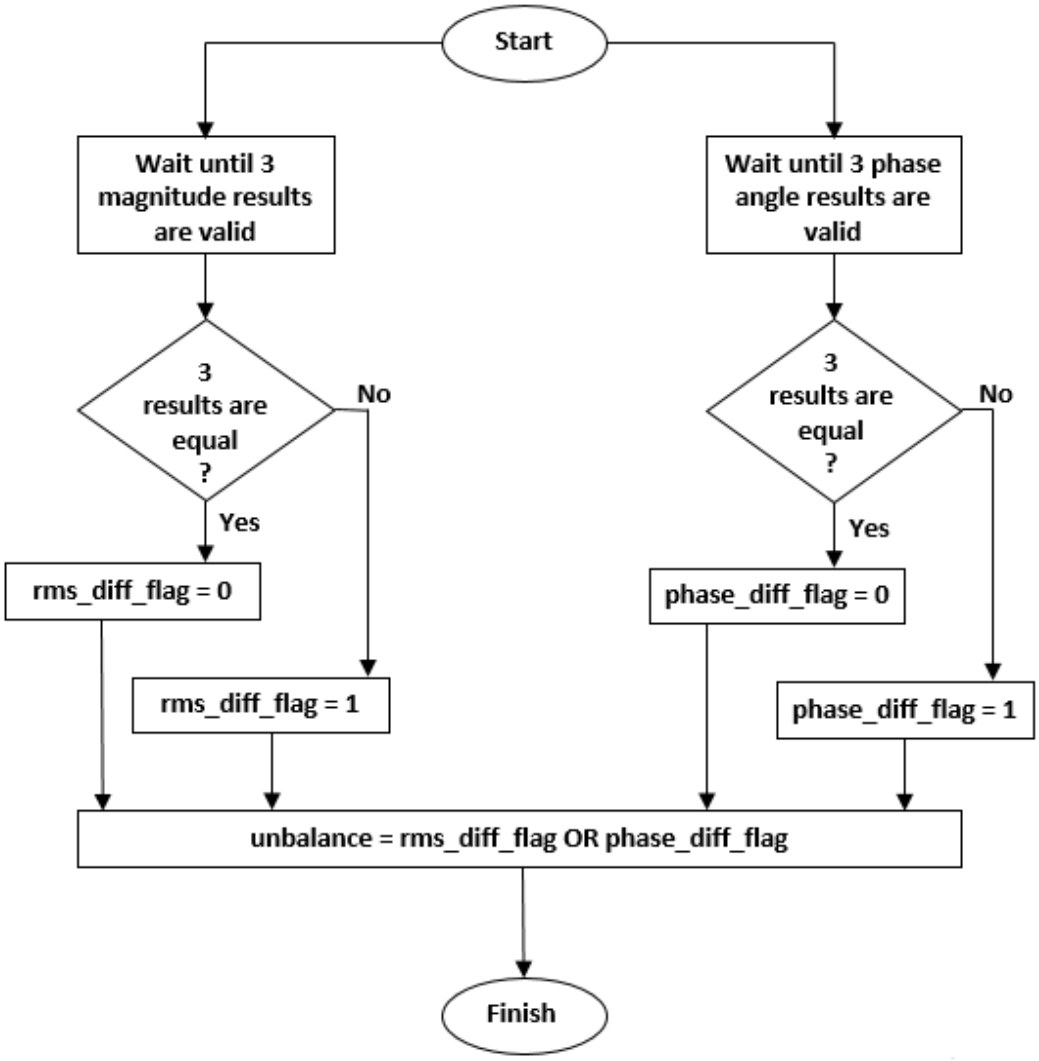

Figure 4.28: Unbalance Detection Algorithm

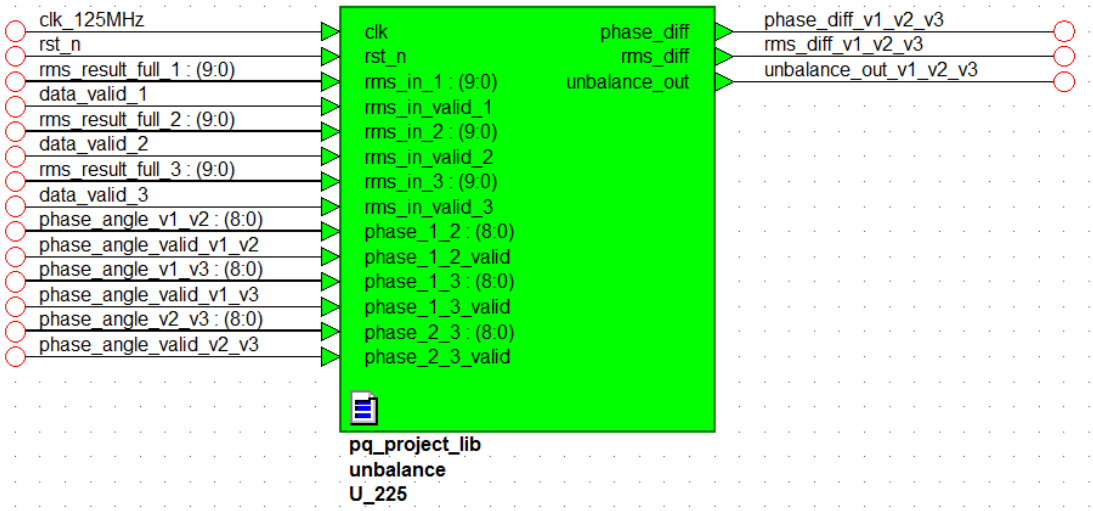

Figure 4.29: Unbalance Detection Unit Block Design

4.6 Power Calculation Unit

Power Calculation Unit is responsible for calculation of active power, reactive power and apparent power. Active and reactive power can be calculated by multiplying voltage and current sample-by-sample and then computing mean. This requires more resource compared to implementing following equations.

$$P = V \cdot I \cdot \cos\theta$$

$$Q = V \cdot I \cdot \sin\theta$$

$$S = V \cdot I$$

where

P: Active Power,

Q: Reactive Power,

S: Apparent Power,

V: Voltage Magnitude,

I: Current Magnitude,

θ: Angle among the supply voltage and current waveforms.

By examining the equations, it is clear that this unit needs magnitude of the supply voltage and current, along with the phase angle between them.

Cosine and sine values between 0 and 359 degrees are pre-calculated, multiplied with 1024 and stored in RAM, since Vivado Synthesizer does not support non-constant real-valued expressions. Using the output of the related Phase Angle Calculation Unit, cosine and sine results of the angle is fetched from RAM. Multiplication with 1024 is implemented because the result of cosine and sine should be converted and fraction being attenuated. While calculating the powers, the result is then divided by 1024 for correction. Division by 1024 is simply done with Least Significant Bits reduction. Pseudo code for RAM content can be written as follows:

```
1 for i:= 0 to 359 do
2       COS_RAM(i) = 1024 * cos(i);
3       SIN_RAM(i) = 1024 * sin(i);
4 end
```

Algorithm for power calculation is explained in Figure 4.30. The module takes valid signals of Magnitude Calculation Unit and Phase Angle Calculation Unit for handshaking mechanism. Input and output signals is shown in Figure 4.31.

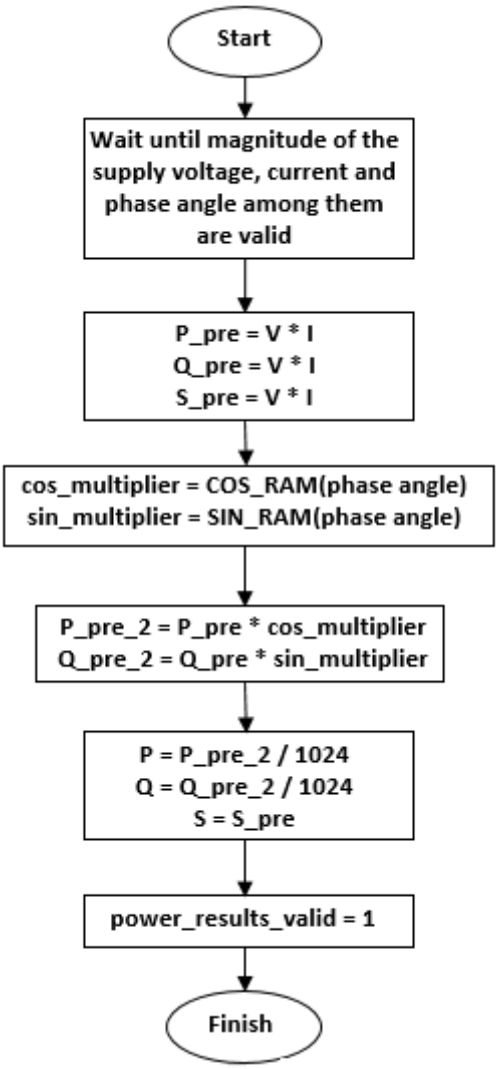

Figure 4.30: Algorithm of Power Calculation Unit

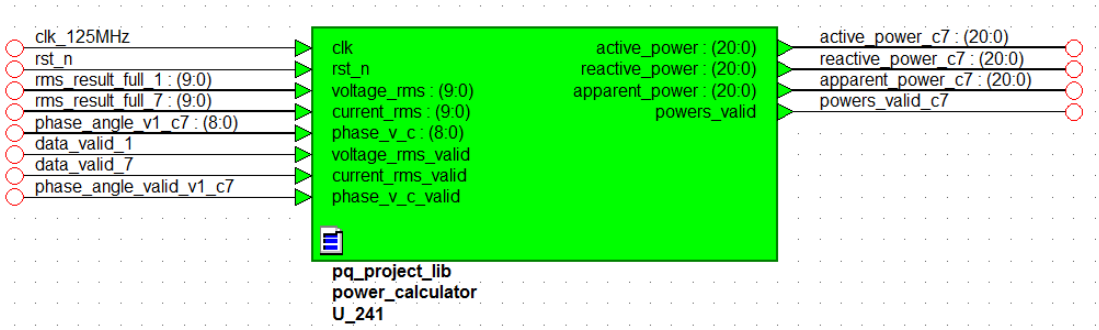

Figure 4.31: Power Calculation Unit Block Design

4.7 Parameter Calculation Unit

This unit is implemented to calculate underdeviation, overdeviation and crest factor parameters. As was mentioned earlier

The overdeviation is defined as follows [14]:

- If $U_{rms\text{-}200ms,i} < U_{din}$ then $U_{rms\text{-}over,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \geq U_{din}$ then $U_{rms\text{-}over,i} = U_{rms\text{-}200ms,i}$

The underdeviation is defined as follows [14]:

- If $U_{rms\text{-}200ms,i} > U_{din}$ then $U_{rms\text{-}under,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \leq U_{din}$ then $U_{rms\text{-}under,i} = U_{rms\text{-}200ms,i}$

where

$U_{rms\text{-}200ms,i}$: 200 ms aggregated RMS result

U_{din} : Declared supply voltage by a transducer ratio

$U_{rms\text{-}over,i}$: Overdeviation result

$U_{rms\text{-}under,i}$: Underdeviation result

Aggregation is defined as the square root of the arithmetic mean of the squared input values. Therefore, for 200 ms aggregation, 10 cycle magnitude of the supply voltage values should be aggregated. Implemented module for magnitude of the supply voltage performs RMS calculation, but it waits sequential inputs while their valid signal stays high. However, for aggregation, 10 magnitude data will be ready in 200 ms while there is time difference among them. Therefore, RMS calculation algorithm can not be used

as it is. Instead of writing new modules, a controller is implemented to be used in front of the RMS calculation module and an evaluation module is implemented afterwards.

The controller module stores the magnitude results in a FIFO and starts reading as soon as 10 data is collected. Therefore, implemented RMS module calculates $U_{rms\text{-}200ms,i}$. The evaluation module takes $U_{rms\text{-}200ms,i}$ and outputs underdeviation and overdeviation parameters according to above equations. Algorithm for this operation is explained in Figure 4.32.

Crest factor is defined as;

$$C_r = \frac{V_{max}}{V_{rms}}$$

where

C_r : Crest factor

V_{max} : Maximum value of the supply voltage samples

V_{rms} : RMS value of the supply voltage

Crest factor calculation module finds the maximum value of the supply voltage and divides it by the prepared RMS result provided by the Magnitude Calculation Unit. Algorithm for this operation is explained in Figure 4.33.

The modules defined in this section are implemented at the same top module. Input and output signals of the modules is shown in the block design of the unit and given in Figure 4.34 and Figure 4.35.

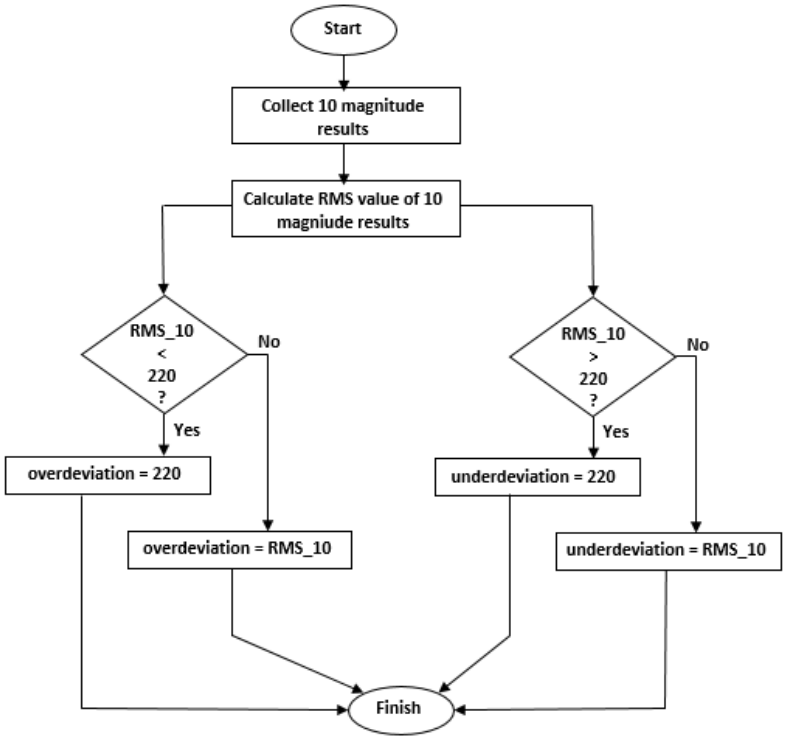

Figure 4.32: Algorithm for Underdeviation and Overdeviation Parameter Calculations

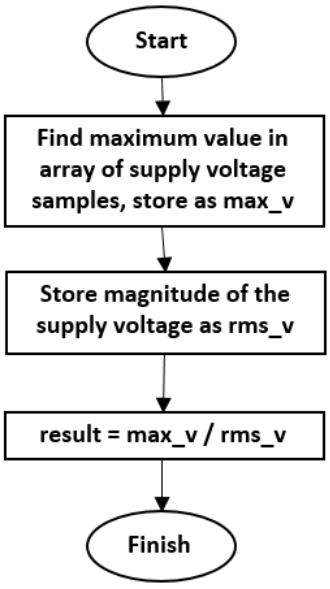

Figure 4.33: Algorithm for Crest Factor Calculation

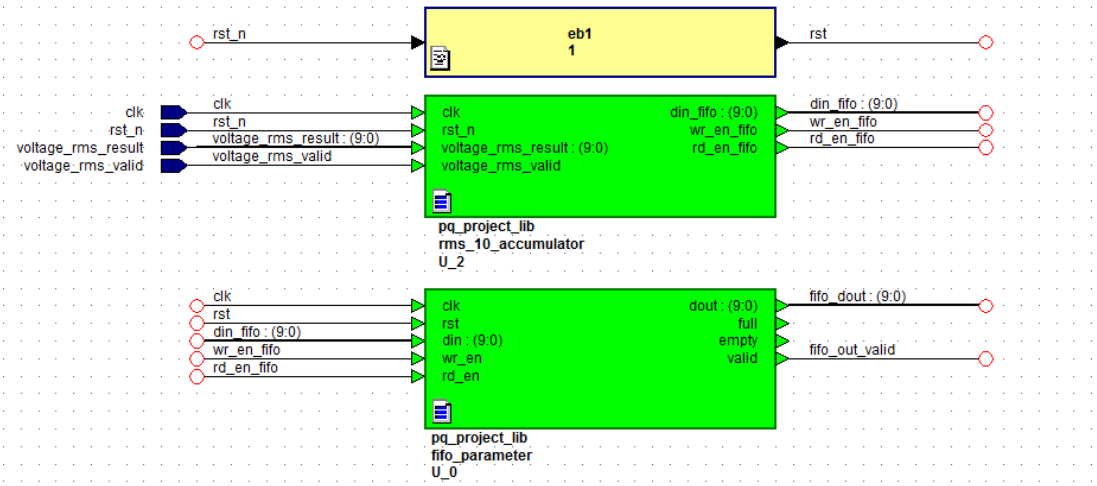

Figure 4.34: Block Design of Parameter Calculation Unit (Part 1)

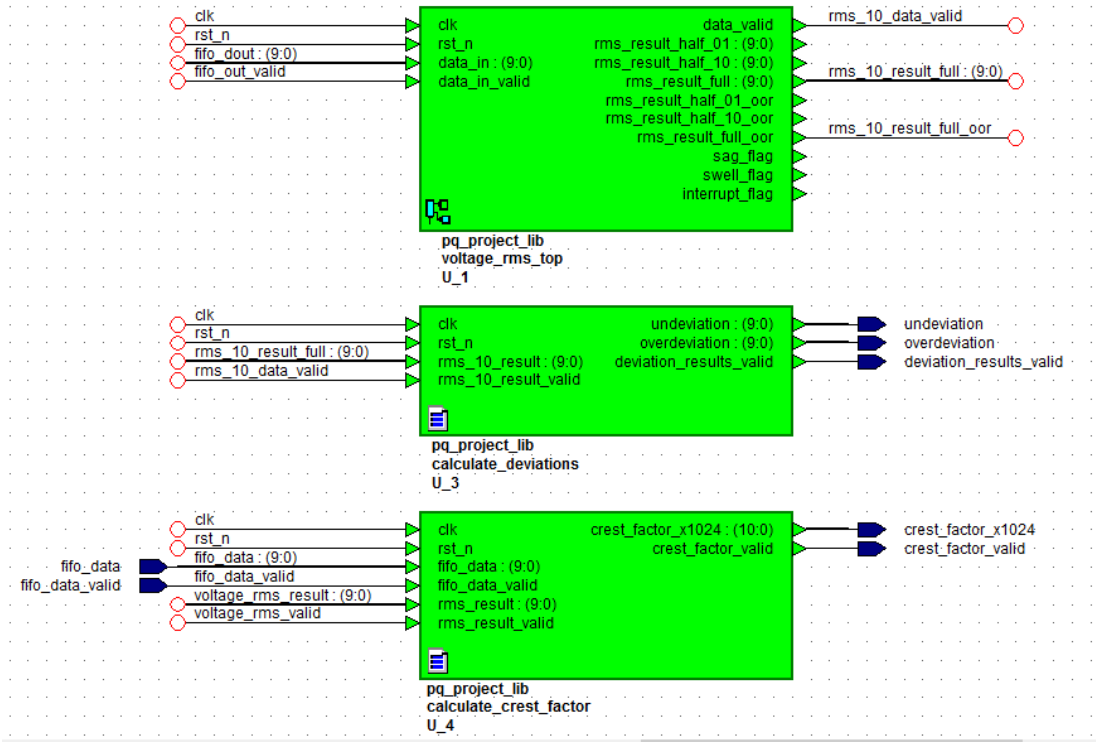

Figure 4.35: Block Design of Parameter Calculation Unit (Part 2)

Calculated crest factor result is obtained by multiplying the actual value with 1024 not to lose fraction.

CHAPTER V

EVALUATION OF THE SYSTEM

Overall system and all sub-systems are evaluated individually in terms of accuracy (functional correctness), timing requirements and resource utilization. While testing accuracy, for each sub-system and overall system, synthetic test data is constructed on MatLAB in accordance with relation to other sub-systems. In other word, test data values and timings are adjusted to act like the other sub-systems.

Accuracy evaluation of the units is done in Vivado by Xilinx. Post-implementation functional simulation method is used.

Timing requirement evaluation of the units is the process of defining timing constraints and controlling the design's compatibility with timing reports which belong to post-implementation design. The reason for that this is timings may have been miscalculated after the synthesis since place and route process is not completed, setup and hold time violations are measured using shortest distances but not using real distances on FPGA.

Resource utilization evaluation of the designed units is the report of the post-implementation design phase. This has the same reason with timing evaluation. Synthesizer may have changed resources to satisfy the timing requirements.

This section starts with the evaluation of the sub-systems sorted with respect to data flow and ends with the overall system.

5.1 Evaluation of Sub-Systems

Evaluation of the sub-systems are given in the same order as the one presented in Chapter 4.

5.1.1 Evaluation of Harmonic Calculation Unit

Multiplexer module controls the rest of the design. Therefore, output signals of the Multiplexer should be studied carefully to apply correct test processes to other modules.

Next module to be evaluated is the Harmonic Calculation module. Since this module calculates 48 different results for each channel, the test process should include confirmation of all. Total simulation time should be chosen accordingly, not the Vivado default value, since time multiplexing is applied and it takes about 794112 ns to complete one cycle worth of input data for all channels.

Harmonic Calculation unit is the first one implemented in this thesis. At the beginning of the evaluation process, no timing requirements are defined. Maximum operating frequency of the unit is found to be 125 MHz. Total operation time of the Multiplexer Unit is calculated using this frequency. The total operation shall not exceed one cycle of the power system, which is 20 milliseconds. The total operation time of the Harmonic Calculation unit is found as follows:

48*2*1034*8 ns = 794112 ns

After specifying the operating frequency of the Harmonic Calculation Unit as 125 MHz which is shown in Figure 5.1, the other units are designed to be compatible with this. This is essential because use of another frequency in the system may cause metastability problems.

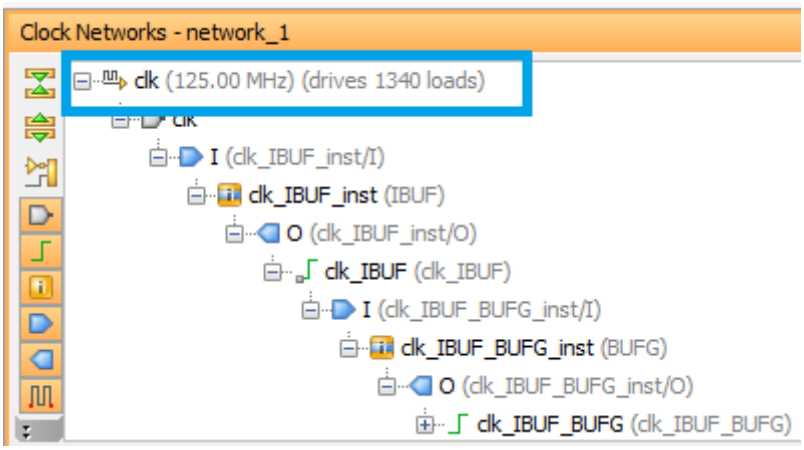

Figure 5.1: Post-Implementation Clock Network of Harmonic Calculation Unit

For accuracy evaluation of the Harmonic Calculation Unit, the same test data used in the overall design evaluation is used. The test data is composed of a pure sinusoidal waveform with its harmonics with smaller magnitudes and randomly produced noise data. The test data is composed of 10 signals with different amplitudes and frequencies. The test data attributes are given in Table 5.1.

Table 5.1: Harmonic Calculation Test Data Attributes

Harmonics	Amplitude (%)	Amplitude	Frequency (Hz)
1	100	128	50
2	10	12.8	100
3	12	15.36	150
4	15	19.2	200
5	20	25.6	250
6	14	17.92	300
7	9	11.52	350
8	8	10.24	400
9	11	14.08	450
10	5	6.4	500

The specified test data constructed on MatLAB is plotted and given in Figure 5.2. The data is stored in data_array on Vivado and is given as input data to Harmonic Calculation Unit.

DFT result of the same test data is computed on MatLAB and two results are compared. Percentage error, which is calculated according to following equation, and comparison results are shown in Table 5.2.

$$\% \text{ Error} = (R_{FPGA} - R_{MatLAB}) / R_{FPGA} * 100$$

where

R_{FPGA} : Result of FPGA simulation

R_{MatLAB} : Result of MatLAB computation

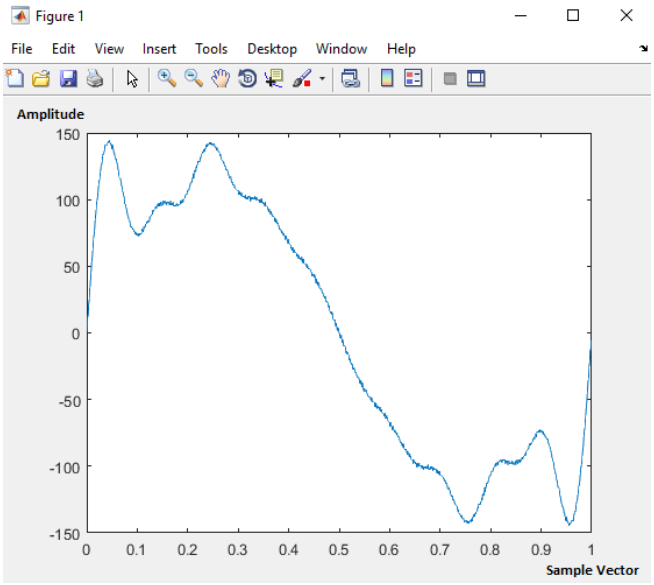

Figure 5.2: Harmonic Calculation Test Data on MatLAB

Table 5.2: Comparison of MatLAB and FPGA Results

Harmonics	Expected Amplitude	MatLAB Result	FPGA Result	FPGA Result Amplitude	% Error
1	128	65531	64110	125.21	-2.23
2	12.8	6585	6456	12.61	-1.51
3	15.36	7835	7575	14.79	-3.85
4	19.2	9833	9469	18.49	-3.84
5	25.6	13147	12994	25.38	-0.87
6	17.92	9148	9085	17.74	-1.01
7	11.52	5873	5806	11.34	-1.59
8	10.24	5222	5285	10.32	0.78
9	14.08	7228	7327	14.31	1.61
10	6.4	3246	3222	6.29	-1.75

Finally, for resource utilization evaluation, post-implementation design report is provided in the following table for Time Multiplexed R2SDF Implementation for 48 channels.

Table 5.3: Post-Implementation Resource Utilization of Harmonic Calculation Unit

Resource	Utilization	for Zynq ZC706 (%)
LUT	7727	3.53
LUTRAM	624	0.89
FF	10155	2.32
BRAM	50	9.17
DSP	36	4
IO	53	14.64

5.1.2 Evaluation of Power Frequency Calculation Unit

Power Frequency Calculation Unit consists of a low pass filter module and a frequency calculation module, which are evaluated individually.

While evaluating the accuracy of Low Pass Filter, test data constructed on MatLAB, described in the previous subsection, is given as input. FIFO reading timing value is also presented. In other words, because the Multiplexer module reads from FIFO's and controls the rest of the design, Low Pass Filter module test data should act, in terms of data format and timings, as the FIFO output. Output signals of the module is checked only for not having multiple zero-crossing.

Functional operation of this Low Pass Filter module is independent of input data length. Thus, input data array size is chosen as 32-word and output array is checked for whether it is increasing, non-decreasing, decreasing or non-increasing. Input data array is a part of MatLAB simulation data, which was described in the previous section. Simulation results are recorded in a text file for evaluation. Post-implementation functional simulation as well as input and output data arrays are provided in Figure 5.3 and below. Output data array is non-increasing which is the functionality for removing multiple zero-crossings.

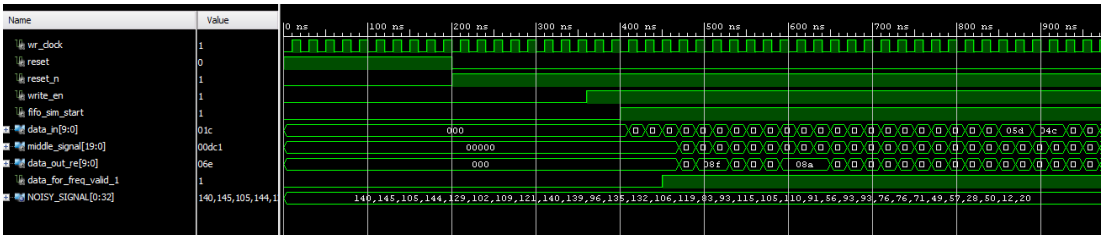

Figure 5.3: Functional Simulation of Low Pass Filter Module

input_data = (140, 145, 105, 144, 129, 102, 109, 121, 140, 139, 96, 135, 132, 106, 119, 83, 93, 115, 105, 110, 91, 56, 93, 93, 76, 76, 71, 49, 57, 28, 50, 12, 20)

output_data = (145, 143, 143, 142, 140, 139, 138, 138, 138, 136, 135, 134, 133, 132, 130, 128, 127, 126, 125, 123, 120, 119, 118, 116, 114, 112, 110, 108, 105, 103, 100, 96, 93, 90, 87, 84, 81, 78, 75, 72, 69, 66, 63, 61, 59, 57, 55, 53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)

For timing evaluation of Low Pass Filter module, timing constraint for 125 MHz is applied and post-implementation timing report shows compatibility as given in Figure 5.4.

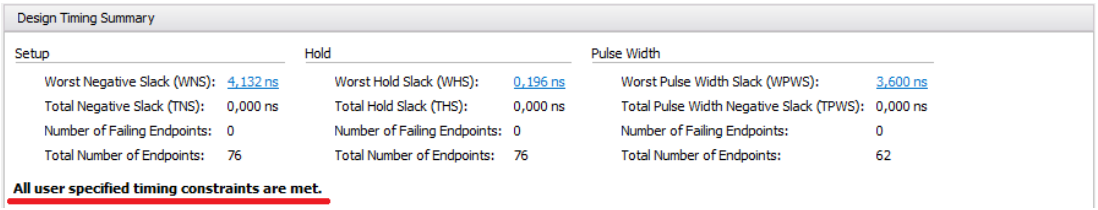

Figure 5.4: Post-Implementation Timing Report of Low Pass Filter Module

For resource utilization, post-implementation design report is given in Table 5.4.

Table 5.4: Post-Implementation Resource Utilization of LPF Module

Resource	Utilization	Available	Utilization %
LUT	97	218600	0.04
FF	61	437200	0.01
IO	45	362	12.43
BUFG	1	32	3.12

While Frequency Calculation module is being evaluated, the test data should act as the output of the Low Pass Filter module. Therefore, if these modules are desired to work together in real-time, it is necessary to design a test process which completely covers the operation of the previous module.

For accuracy evaluation, test data is different from the one which is used for the overall design, because Low Pass Filter output data has no multiple zero-crossing. Therefore, test data is chosen to have almost pure sinusoidal waveform. Calculated frequency

result is compared according to test data's array width. 1024-word long input test data which consists of 4 times repeated 256-word long sinusoidal cycle is applied. Thus, expected frequency result is 256 (hexadecimal 100) and valid signal should be asserted high 4 times. Expected behavior of these output signals are obtained and shown in Figure 5.5.

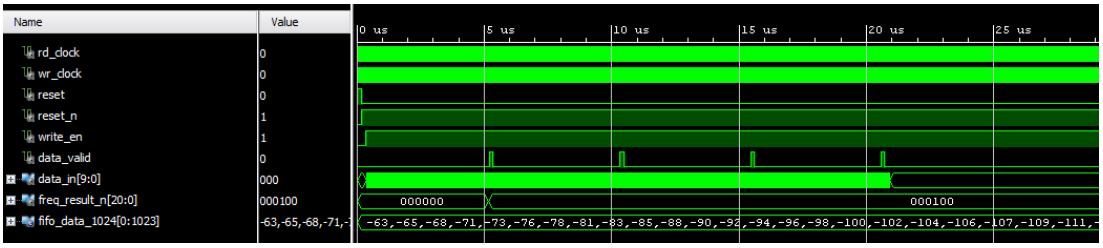

Figure 5.5: Functional Simulation of Frequency Calculation Module

For timing evaluation, timing constraint for 125 MHz is applied and post-implementation timing report shows compatibility as given in Figure 5.6.

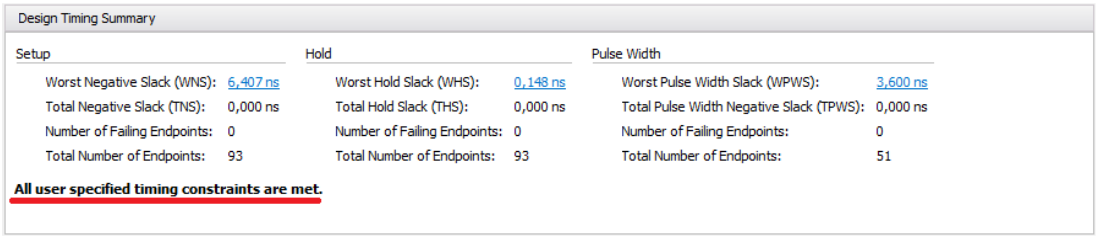

Figure 5.6: Post-Implementation Timing Report of Frequency Module

For resource utilization evaluation, post-implementation design results are shown in Table 5.5.

Table 5.5: Post-Implementation Resource Utilization of Frequency Module

Resource	Utilization	Available	Utilization %
LUT	38	218600	0.02
FF	50	437200	0.01
IO	26	362	7.18
BUFG	1	32	3.12

5.1.3 Evaluation of Magnitude Calculation Unit

This unit is designed to calculate root mean square values of both the supply voltage and current. Input data of the module comes from Multiplexer, and output data is used by Power Calculation Unit, Parameter Calculation Unit, and Unbalance Detection Unit.

To evaluate accuracy of this module, test process is designed to simulate the behavior of the Multiplexer module. Thus, the test data constructed for the overall design is used. In addition, it is essential for this module to assert flags, used for handshaking, at the proper rising edge of the clock, because its output data affects the operation of other three units. Simulation result is shown in Figure 5.7. Input data array is fifo_data_1024_311 in the figure.

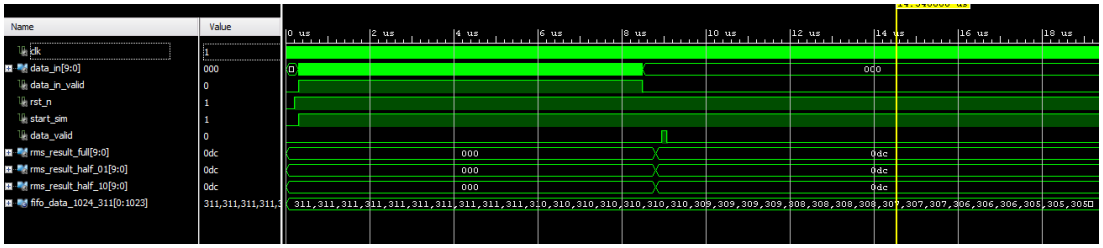

Figure 5.7: Functional Simulation of Magnitude Calculation Unit

Pure cosine signal is chosen for functional simulation to evaluate easily. Input data amplitude is 311, therefore magnitude result should be 311 * 0.707. Simulation result is 220 (hexadecimal: DC) for half cycles and full cycles.

For timing evaluation of Magnitude Calculation unit, timing constraint for 125 MHz is applied and post-implementation timing report shows **incompatibility** as given in Figure 5.8.

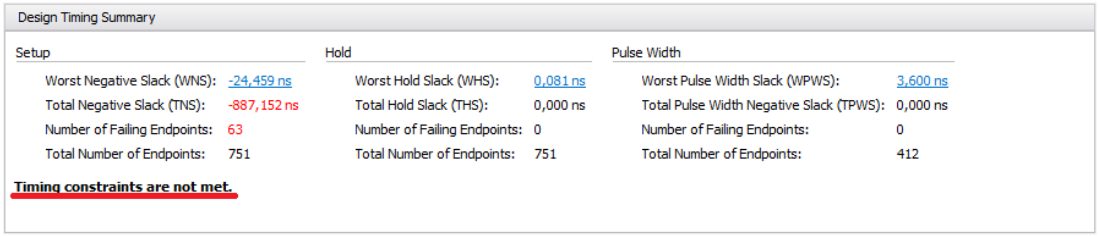

Figure 5.8: Post-Implementation Timing Report of Magnitude Calculation Unit

The above incompatibility problem should be solved. Magnitude Calculation Unit is found to be capable of working with 25 MHz clock. This is compatible with the system requirements. In other words, operating this module with 25MHz does not affect the real-time operation of the Power Quality monitoring system. However, if the rest of the design operates with 125 MHz clock and another clock domain exists, this may cause metastability problems. Dealing with these problems requires control mechanisms such as additional control flag signals or dual-clock memories to ensure safe data flow. These solutions will increase the resource utilization in contrast to our main objective, which is fitting in the smallest device possible. Therefore, timing problem is handled in another way. Magnitude Calculation Unit is modified to do its computation once for every power system cycle and assert control flags after 40 ns operation. In this manner, the units, which are dependent to this one, will read the output signals when they are stable. This solution is verified by operating it with other units simultaneously.

For resource utilization evaluation, post-implementation report of the supply voltage calculation version of the unit is given in Table 5.6.

5.1.4 Evaluation of Event Detection Module

While the test process for this evaluation includes the behavior of Magnitude Calculation Unit, the constructed test data on MatLAB should be chosen to trigger the supply voltage dips, swells, and interruption. It is essential for this unit to assert detection flag signals as soon as it happens.

Table 5.6: Post-Implementation Resource Utilization of Magnitude Calculation Unit

Resource	Utilization	Available	Utilization %
LUT	1995	218600	0.91
FF	411	437200	0.09
IO	285	362	78.73
BUFG	1	32	3.12

Since this module is included in Magnitude Calculation Unit, timing and resource utilization reports are the same. Only evet flag assertions are evaluated in terms of accuracy.

To trigger interrupt flag, amplitude is adjusted to 12. Simulation result with high interrupt_flag is shown in Figure 5.9. Output results of magnitude calculations are hexadecimal 3FF, which indicates out-of-range result.

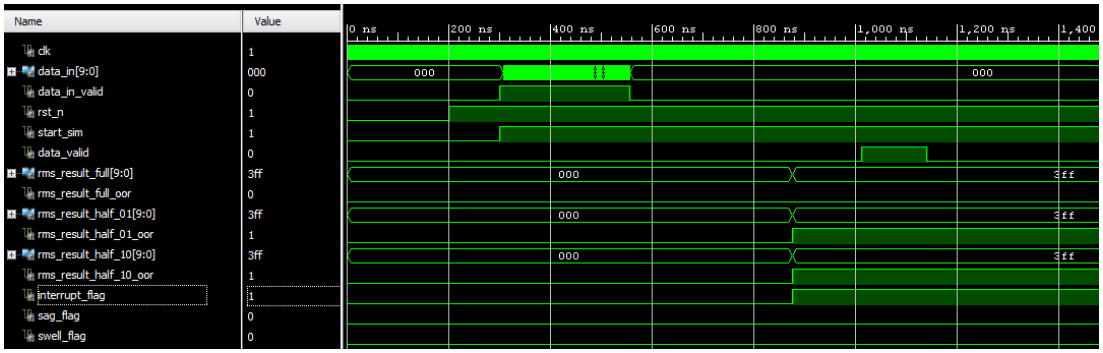

Figure 5.9: Functional Simulation Result with High Interrupt Flag

To trigger sag flag, amplitude is adjusted to 212. Simulation result with high sag_flag is shown in Figure 5.10. Output results of magnitude calculations are hexadecimal 3FF, which indicates out-of-range result.

To trigger swell flag, amplitude is adjusted to 354. Simulation result with high swell_flag is shown in Figure 5.11. Output results of magnitude calculations are hexadecimal 3FF, which indicates out-of-range result.

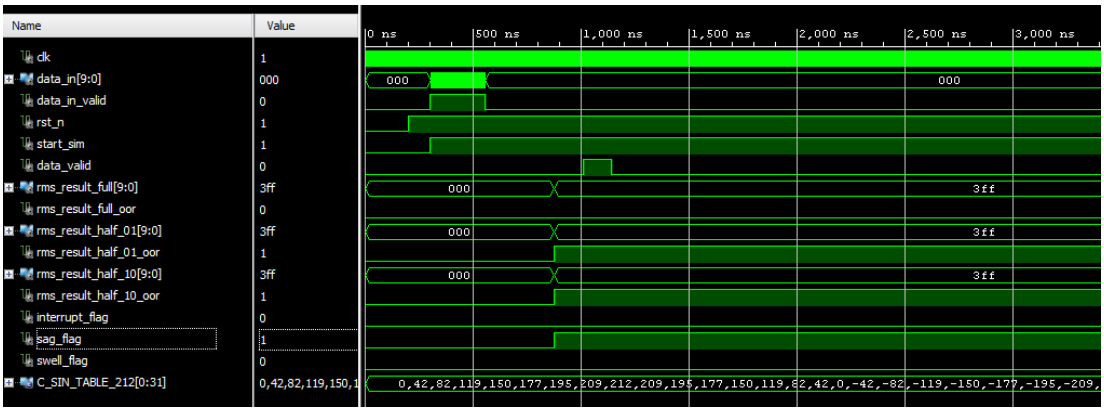

Figure 5.10: Functional Simulation Result with High Sag Flag

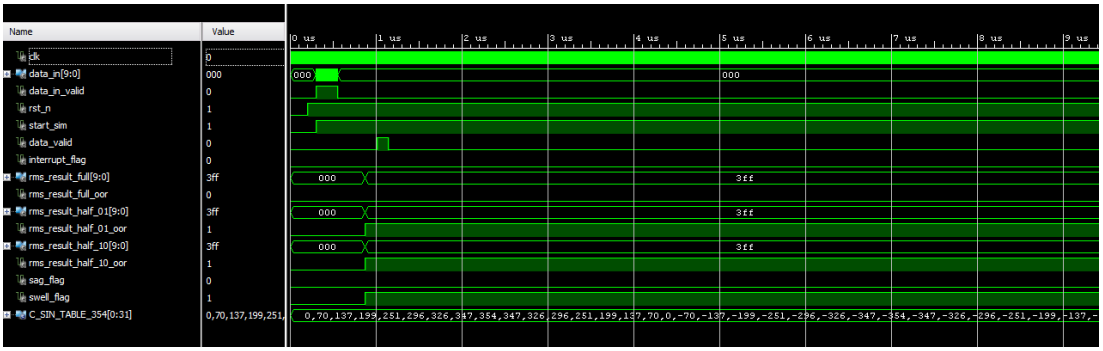

Figure 5.11: Functional Simulation Result with High Swell Flag

5.1.5 Phase Angle Calculation Unit

This unit consists of two Zero Crossing Modules, a Phase Difference module, and a Phase Angle Calculation module while having dependency to Frequency Calculation unit. Each of the sub-modules are evaluated individually.

The second version of Phase Angle Calculation Unit, which is designed to calculate three phase angle, is not evaluated. Since this is only a top module consists of the first version, there is no need for functional simulation.

Zero Crossing modules takes input from Multiplexer, and output data to Phase Difference module which outputs data to Phase Angle Calculation module. Therefore, test processes of these modules are different but compatible with each other. It is very important to create Multiplexer and Frequency Calculation unit behaviors while testing accuracy.

For accuracy evaluation of Phase Angle Calculation unit, two test data which are almost pure sinusoidal waveforms having phase shift are constructed on MatLAB. Data arrays for two inputs and simulation result are provided as follows:

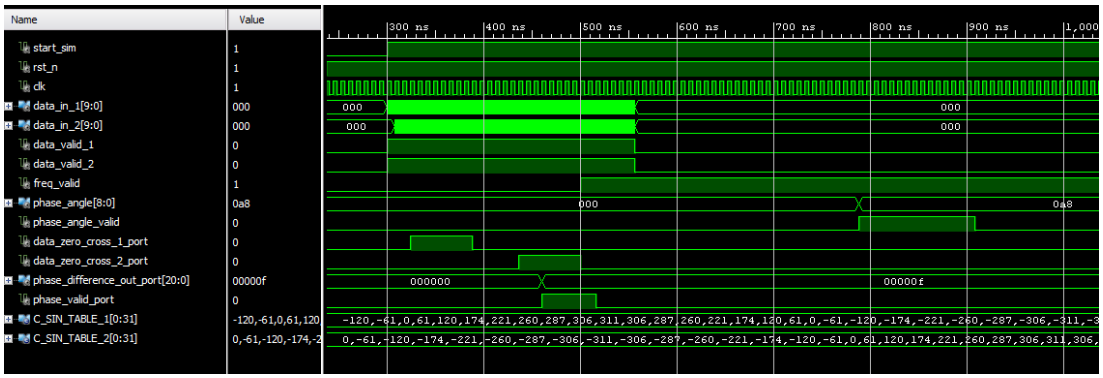

Figure 5.12: Functional Simulation of Phase Angle Calculation Unit

input_data_1 = (-120, -61, 0, 61, 120, 174, 221, 260, 287, 306, 311, 306, 287, 260, 221, 174, 120, 61, 0, -61, -120, -174, -221, -260, -287, -306, -311, -306, -287, -260, -221, -174)

input_data_2 = (0, -61, -120, -174, -221, -260, -287, -306, -311, -306, -287, -260, -221, -174, -120, -61, 0, 61, 120, 174, 221, 260, 287, 306, 311, 306, 287, 260, 221, 174, 120, 61)

Input data array widths are 32 and the difference between negative-to-positive data transmission points is 15 samples. Therefore, phase angle result should be 360 / 32 * 15 = 168.75 degrees. It is calculated 168 (hexadecimal: A8) as shown in the figure.

For timing evaluation of the unit, timing constraint for 125 MHz is applied and post-implementation timing report shows incompatibility as given in Figure 5.13.

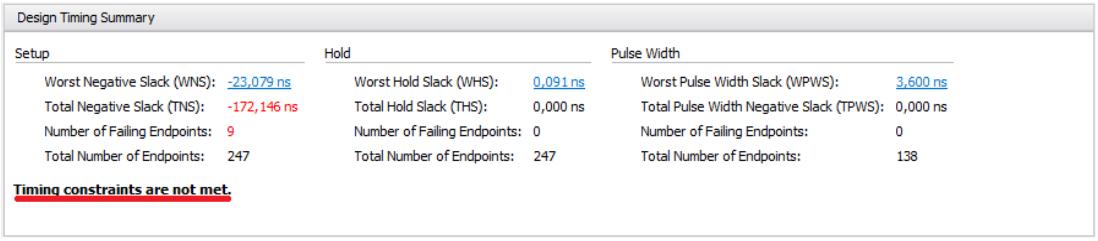

Figure 5.13: Post-Implementation Timing Report of Phase Calculation Unit

Because of the same problems explained previously for Magnitude Calculation Unit, instead of designing a new algorithm or an architecture, some modifications as the one in Magnitude Calculation Unit are applied and verified operating it with other units simultaneously. Post-Implementation resource utilization of this unit is given in Table 5.7.

Table 5.7: Post-Implementation Resource Utilization of Phase Calculation Unit

Resource	Utilization	Available	Utilization %
LUT	688	218600	0.31
FF	136	437200	0.03
DSP	1	900	0.11
IO	62	362	17.13
BUFG	1	32	3.12

5.1.6 Unbalance Detection Unit

Unbalance Detection Unit receives output ports of Magnitude Calculation Unit and Phase Angle Calculation Unit. These output ports consist of data and valid signals. While this unit is evaluated for functional accuracy, these data and valid signals are controlled to simulate behavior of previous modules.

Although there exist units for the supply voltage and current, they use the same algorithm. Thus, only one of them is evaluated.

The Unbalance Detection Unit outputs three flags. These flags indicate differences among phase magnitudes and phase angles as well as unbalance existence. During test procedure, input ports are chosen to trigger each scenario.

To trigger phase_diff flag, different phase angle values are used as inputs. Valid signals are given at the same time, which is not essential to the design. Simulation result shows high value at phase_diff and unbalance ports which are presented in Figure 5.14.

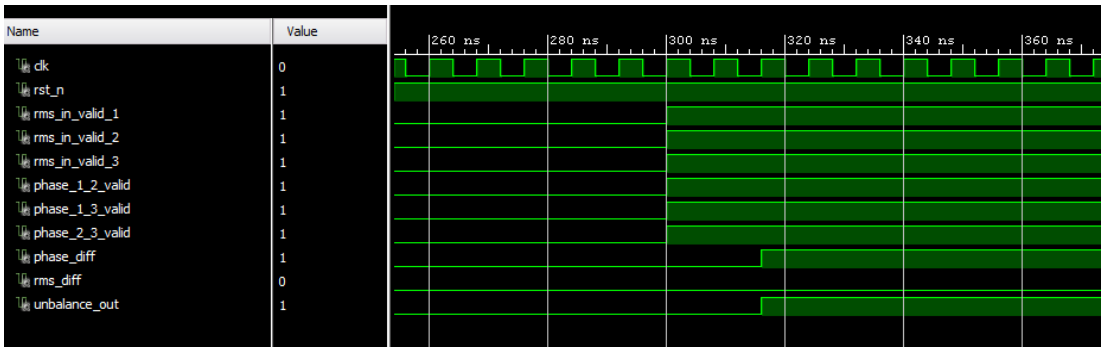

Figure 5.14: Simulation Result of Different Phase Angles

To trigger rms_diff flag, different magnitude values are used as inputs. Valid signals are adjusted. Simulation result shows high value at rms_diff and unbalance ports which are presented in Figure 5.15.

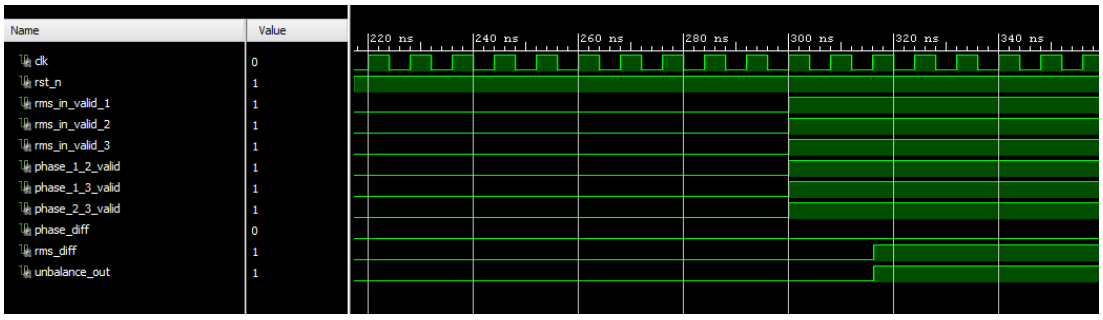

Figure 5.15: Simulation Result of Different Magnitude

The third scenario is no existence of unbalance. To trigger this condition, the same values for three magnitude inputs and three phase angle inputs are adjusted with proper valid signals. Simulation result shows low value at phase_diff, rms_diff and unbalance flags as presented in Figure 5.16.

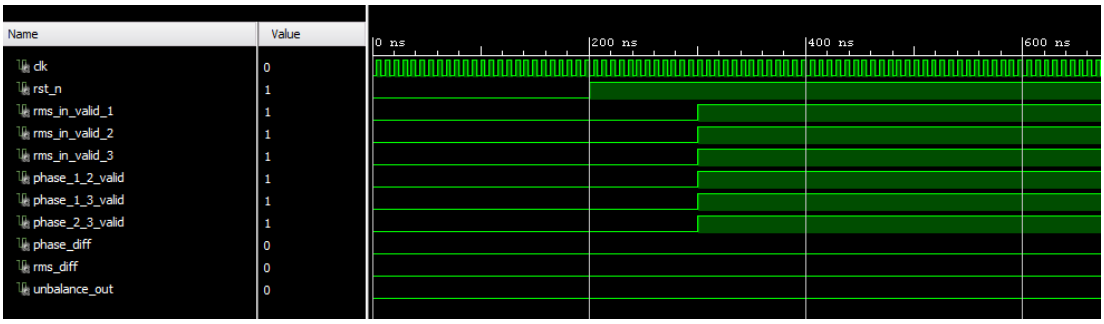

Figure 5.16: Simulation Result of Low Unbalance

The last simulation for Unbalance Detection Unit is used for timing analysis. In this test bench, valid signals are asserted at different time and output flag response time is analyzed. phase_diff and rms_diff flags are dependent on three inputs each. These flags are computed and asserted 2 clock-cycle delay after the last valid signal's high assertion, but there is no delay for unbalance port, it is asserted at the same clock signal with other flags. This operation is defined in Figure 5.17.

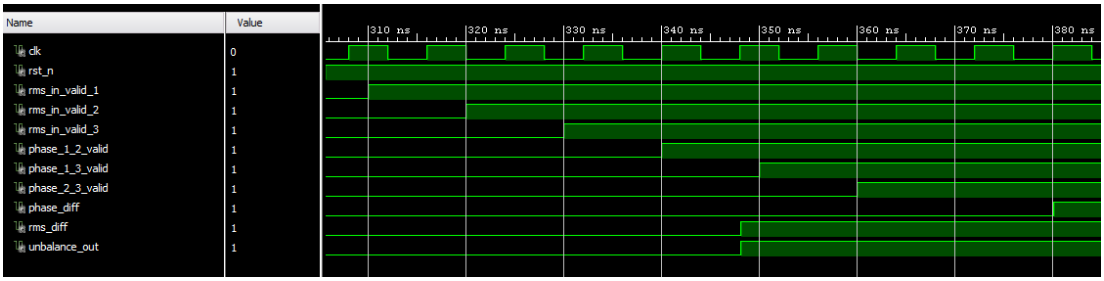

Figure 5.17: Simulation Result of Flag Timings

Time constraint is adjusted to 125MHz and post-implementation timing summary report shows compatibility, as in Figure 5.18.

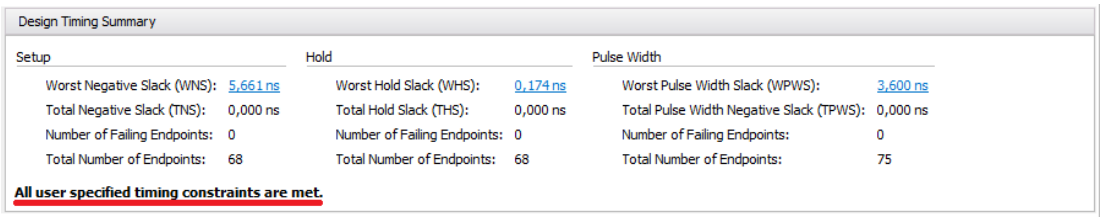

Figure 5.18: Post-Implementation Timing Report of Unbalance Detection Unit

Post-implementation resource utilization of Unbalance Detection Unit is presented in Table 5.8.

Table 5.8: Post-Implementation Resource Utilization of Unbalance Detection Unit

Resource	Utilization	Available	Utilization %
LUT	43	218600	0.02
FF	74	437200	0.02
IO	68	362	18.78
BUFG	1	32	3.12

5.1.7 Power Calculation Unit

Power Calculation Unit receives outputs of Magnitude Calculation Unit and Phase Angle Calculation Unit. While testing accuracy of this module, output signal's behavior of these modules are used to construct the test procedure.

For functional accuracy testing, several data sets are used. Data sets, expected values and simulation results are presented. Expected values are calculated as in the equations given in Section 2.1.8.

The first data set is chosen as follows:

V_{rms} = 220 V

I_{rms} = 28 A

$\theta = 30^o$

Expected power results are calculated as follows:

$P_{exp} = V_{rms} * I_{rms} * \cos(\theta) = 220 * 28 * \cos(30) = 5334.716$ W

$Q_{exp} = V_{rms} * I_{rms} * \sin(\theta) = 220 * 28 * \sin(30) = 3080$ VAr

$S_{exp} = V_{rms} * I_{rms} = 220 * 28 = 6160$ VA

Simulation results are obtained as in Figure 5.19.

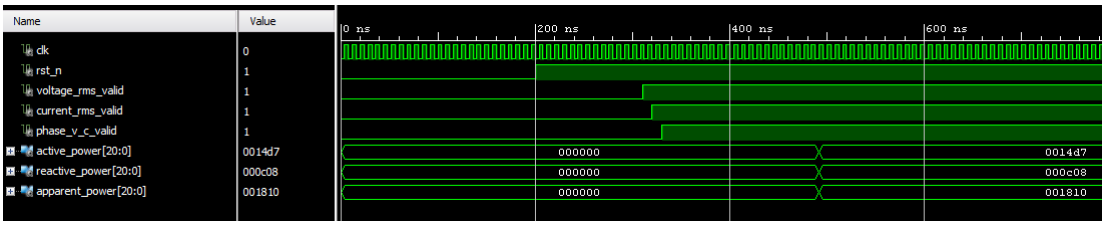

Figure 5.19: The First Simulation of Power Calculation Unit

P_{obt} = 5335 W

Q_{obt} = 3080 VAr

S_{obt} = 6160 VA

Percentage errors are calculated according to expected and obtained values as follows:

$P_{error} = (P_{obt} – P_{exp}) / P_{obt} * 100 = (5335 – 5334.716) / 5335 * 100 = 0.00532$

$Q_{error} = (Q_{obt} – Q_{exp}) / Q_{obt} * 100 = (3080 – 3080) / 3080 * 100 = 0$

$S_{error} = (S_{obt} - S_{exp}) / S_{obt} * 100 = (6160 - 6160) / 6160 * 100 = 0$

The other tests are given in Table 5.9 and simulation results are given in order.

Table 5.9: Power Calculation Unit Experimental Results

Dataset				**Expected Values**		
#	**V**	**I**	**θ**	**P**	**Q**	**S**
2	210	42	41	6656.54	5786.44	8820
3	230	23	25	4794.37	2235.65	5290
4	225	36	15	7823.99	2096.43	8100
Dataset	**Obtained Results**			**% Error**		
#	**P**	**Q**	**S**	**P**	**Q**	**S**
2	6658	5788	8820	0.0219	0.0269	0
3	4794	2236	5290	-0.0077	0.0156	0
4	7823	2096	8100	-0.0126	0.0205	0

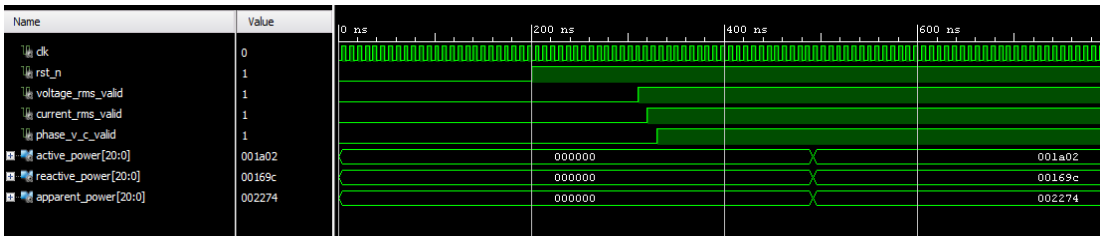

Figure 5.20: The Second Simulation of Power Calculation Unit

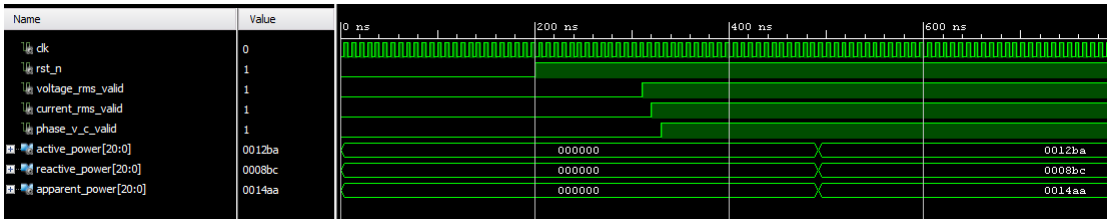

Figure 5.21: The Third Simulation of Power Calculation Unit

Time constraint for 125MHz is applied and post-implementation timing summary report shows compatibility, as given in Figure 5.23.

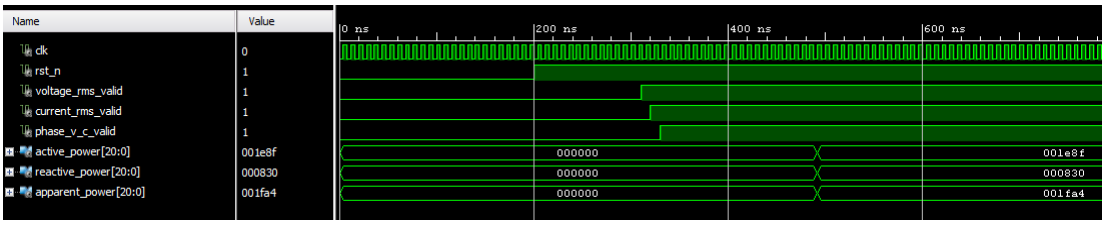

Figure 5.22: The Fourth Simulation of Power Calculation Unit

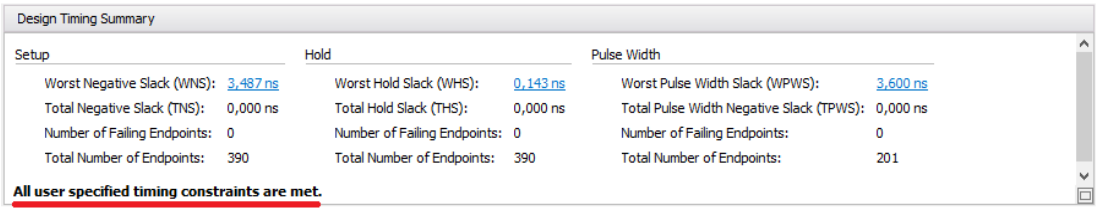

Figure 5.23: Post-Implementation Timing Report of Power Calculation Unit

Implemented design resource utilization is given in the following table for one channel.

Table 5.10: Post-Implementation Resource Utilization of Power Calculation Unit

Resource	Utilization	Available	Utilization %
LUT	216	218600	0.10
FF	200	437200	0.05
DSP	3	900	0.33
IO	98	362	27.07
BUFG	1	32	3.12

5.1.8 Parameter Calculation Unit

This unit responsible for calculation of underdeviation, overdeviation and crest factor parameters. Underdeviation and overdeviation are calculated in one module and crest factor is the result of another one. Therefore, these modules are evaluated separately.

For accuracy evaluation of underdeviation and overdeviation parameters, 10 values suitable for being magnitude result of the supply voltage are chosen. These values are given in the following array.

data_array = (220, 230, 210, 205, 245, 223, 222, 221, 220, 218)

RMS result of this array, which is 200 ms aggregation of the magnitude of the supply voltage, is calculated as 221.6366. For a constant U_{din} = 220V, underdeviation and overdeviation parameters are calculated according to the following equations.

The overdeviation is defined as follows [14]:

- If $U_{rms\text{-}200ms,i} < U_{din}$ then $U_{rms\text{-}over,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \geq U_{din}$ then $U_{rms\text{-}over,i} = U_{rms\text{-}200ms,i}$

The underdeviation is defined as follows [14]:

- If $U_{rms\text{-}200ms,i} > U_{din}$ then $U_{rms\text{-}under,i} = U_{din}$
- If $U_{rms\text{-}200ms,i} \leq U_{din}$ then $U_{rms\text{-}under,i} = U_{rms\text{-}200ms,i}$

where

$U_{rms\text{-}200ms,i}$: 200 ms aggregated RMS result

U_{din} : Declared supply voltage by a transducer ratio

$U_{rms\text{-}over,i}$: Overdeviation result

$U_{rms\text{-}under,i}$: Underdeviation result

From these equations, expected result of the parameters are;

$U_{rms\text{-}over,i} = U_{rms\text{-}200ms,i} = 221.6366$

$U_{rms\text{-}under,i} = U_{din} = 220$

Experimental results are obtained as shown in Figure 5.24.

$U_{rms\text{-}over,i} = 222$ (hexadecimal DE)

$U_{rms\text{-}under,i} = 220$ (hexadecimal DC)

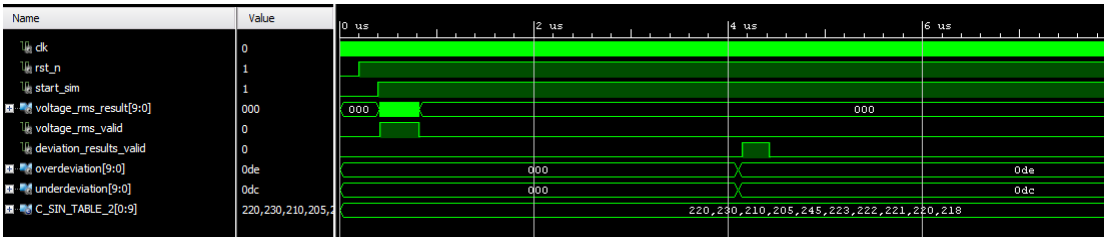

Figure 5.24: Simulation of Underdeviation and Overdeviation Calculation

Percentage error for underdeviation is 0 but, overdeviation is calculated as follows (exp: expected, obt: obtained):

$\%U_{error} = (U_{obt} - U_{exp}) / U_{obt} * 100 = (222 - 221.6366) / 222 * 100 = 0.164\ \%$

For timing evaluation, time constraint for 125MHz is applied and post-implementation timing summary report shows incompatibility as shown in Figure 5.25. Parameter calculation unit encapsulates the Magnitude Calculation Unit which has the timing problem as described previously. The solution is explained in Magnitude Calculation Unit.

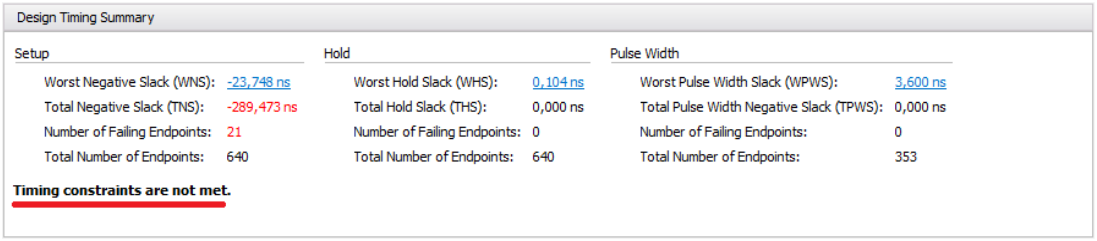

Figure 5.25: Post-Implementation Timing Report of Underdeviation and Overdeviation Calculation

For resource utilization evaluation, post-implementation design result is provided in Table 5.11.

Table 5.11: Post-Implementation Resource Utilization of Underdeviation and Overdeviation Calculation

Resource	Utilization	Available	Utilization %
LUT	785	218600	0.36
FF	352	437200	0.08
IO	44	362	12.15
BUFG	1	32	3.12

LUT resource utilization exceeds expectations because of defining FIFO, which is used for storing RMS results, behaviorally, not by using an IP Core.

For accuracy evaluation of crest factor parameter calculation, data array consists of 32 values is applied for detection of V_{max} and V_{rms} result is asserted with valid flag, since these the behavior of previous modules.

data_array = (-120, -61, 0, 61, 120, 174, 221, 260, 287, 306, 311, 306, 287, 260, 221, 174, 120, 61, 0, -61, -120, -174, -221, -260, -287, -306, -311, -306, -287, -260, -221, -174)

V_{rms} = 220

V_{max} of the data array is 311. Thus, crest factor is expected as follows:

crest_factor = V_{max} / V_{rms} = 311 / 220 = 1.4136

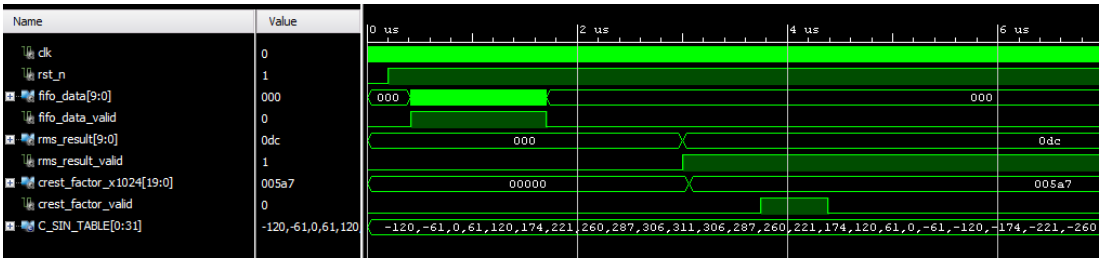

Figure 5.26: Simulation of Crest Factor Calculation

Crest factor parameter is obtained as 1447 (hexadecimal 5A7) as shown in Figure 5.26. As was mentioned previously, this result is calculated by multiplying crest factor by 1024. Thus, obtained crest factor is 1447 / 1024 = 1.4131.

Percentage error is calculated as follows (exp: expected, obt: obtained):

$\%CF_{error} = (CF_{obt} - CF_{exp}) / CF_{obt} * 100 = (1.4131 - 1.4136) / 1.4131 * 100 = -0.0354$

For timing analysis, time constraint for 125MHz is applied and post-implementation timing summary report shows incompatibility as shown in Figure 5.27. Instead of defining another time domain which may result in metastability problems, the solution which is the one used for the Magnitude Calculation Unit is applied and confirmed by functionally simulating the units simultaneously.

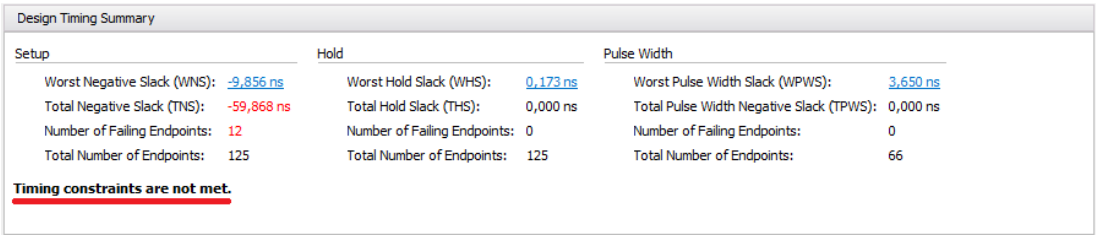

Figure 5.27: Post-Implementation Timing Report of Crest Factor Calculation

Resource utilization report of the implemented design is shown in Table 5.12.

Table 5.12: Post-Implementation Resource Utilization of Crest Factor Calculation

Resource	Utilization	Available	Utilization %
LUT	297	218600	0.14
FF	65	437200	0.01
IO	51	362	14.09
BUFG	1	32	3.12

As a summary, all of the units are capable of operating using 125MHz clock. Some of them which are using division are not compatible with the specified timing constraint. This is resolved by using delayed valid signals for next modules. In this way, only data flow from or to these modules is slowed down.

5.2 Evaluation of the Overall System

The system is capable of measuring and/or calculating standard-defined power quality parameters for 48 channels. The implemented overall design uses time multiplexing. Thus, the implemented circuit is reserved for one channel for about 16544 ns, which was calculated in Section 4.1.2.2. Each sub-system outputs the results for each channel. These results could be stored in BRAMs and read for functional verification. This is not included within the scope of this thesis. Defined outputs as well as input ports and their bit-lengths are shown in Figure 5.28 for clarification. In this figure, some abbreviations are needed to be explained as follows:

- wr_clk is the clock to write into FIFOs.
- rst and rst_n are the resets for the system.
- source_id indicates which channel currently using the circuit.
- din_fifo ports are used to give input data to the system.
- wr_en ports are used for enabling writing into FIFOs.
- _v1, _v2, _v3 suffixes indicate 3 channels of the selected voltage feeder for simulation.

- _c7, _c8, _c9 suffixes indicate 3 channels of the selected current feeder for simulation.

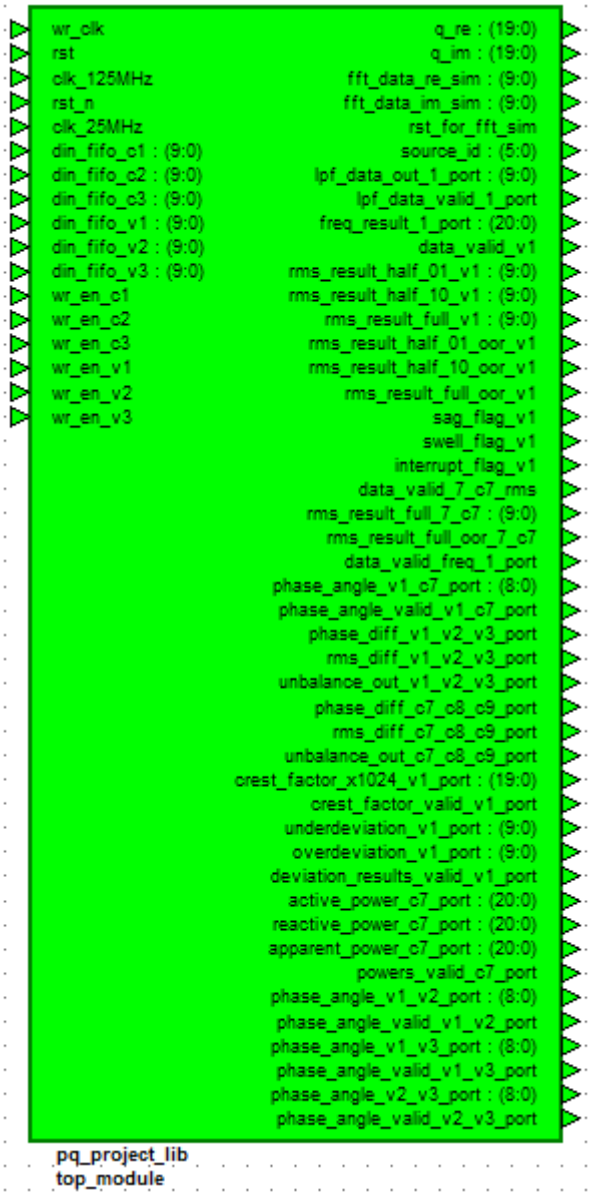

Figure 5.28: Top Module Input and Output Ports

ADC and SPI (Serial Peripheral Interface) blocks in Figure 5.29 are not implemented. The input test data, which is used during the overall system evaluation process, should be act as the output of the SPI block.

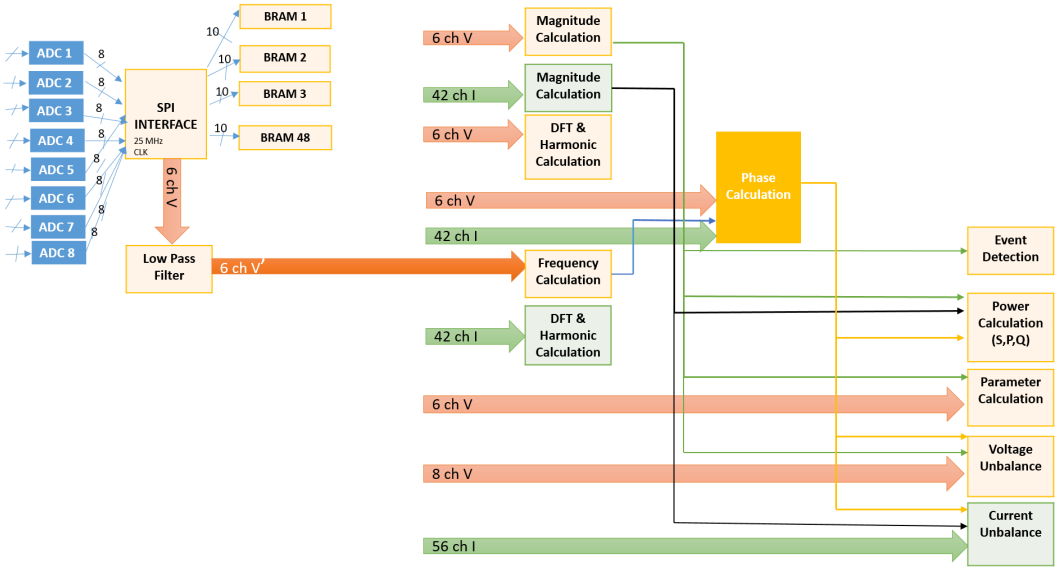

Figure 5.29: The Overall System Block Design

For accuracy evaluation of the overall design, the test data is composed of a pure sinusoidal waveform with its harmonics with smaller magnitudes and randomly produced noise data. Constructed signals on MatLAB are given in Figure 5.30 for voltage and in Figure 5.31 for current. These are for the two channels of two feeders. The test data of the other channels are similar to these ones except for phase angle.

To be able to implement the system, the result of only one channel's results are included in simulations because of the number of GPIO ports. For numerical results, percentage errors are calculated.

The simulation result of the overall design is provided as an overview in Figure 5.32. For functional evaluation of the system, each parameter result is interpreted individually by magnifying related part in the overall design simulation overview.

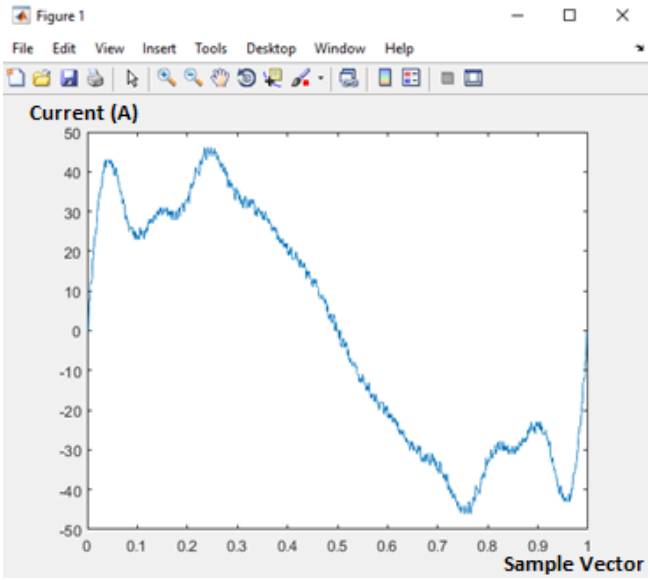

Figure 5.30: Current Test Data for Overall System Evaluation

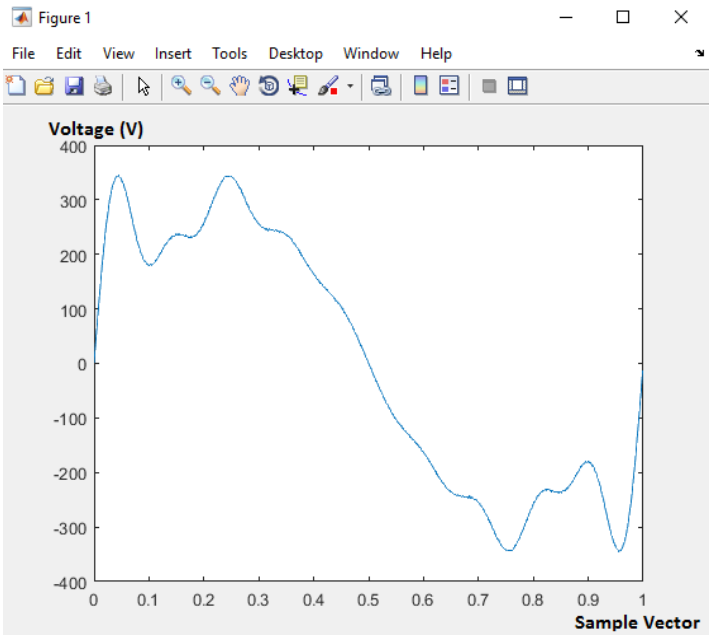

Figure 5.31: Voltage Test Data for Overall System Evaluation

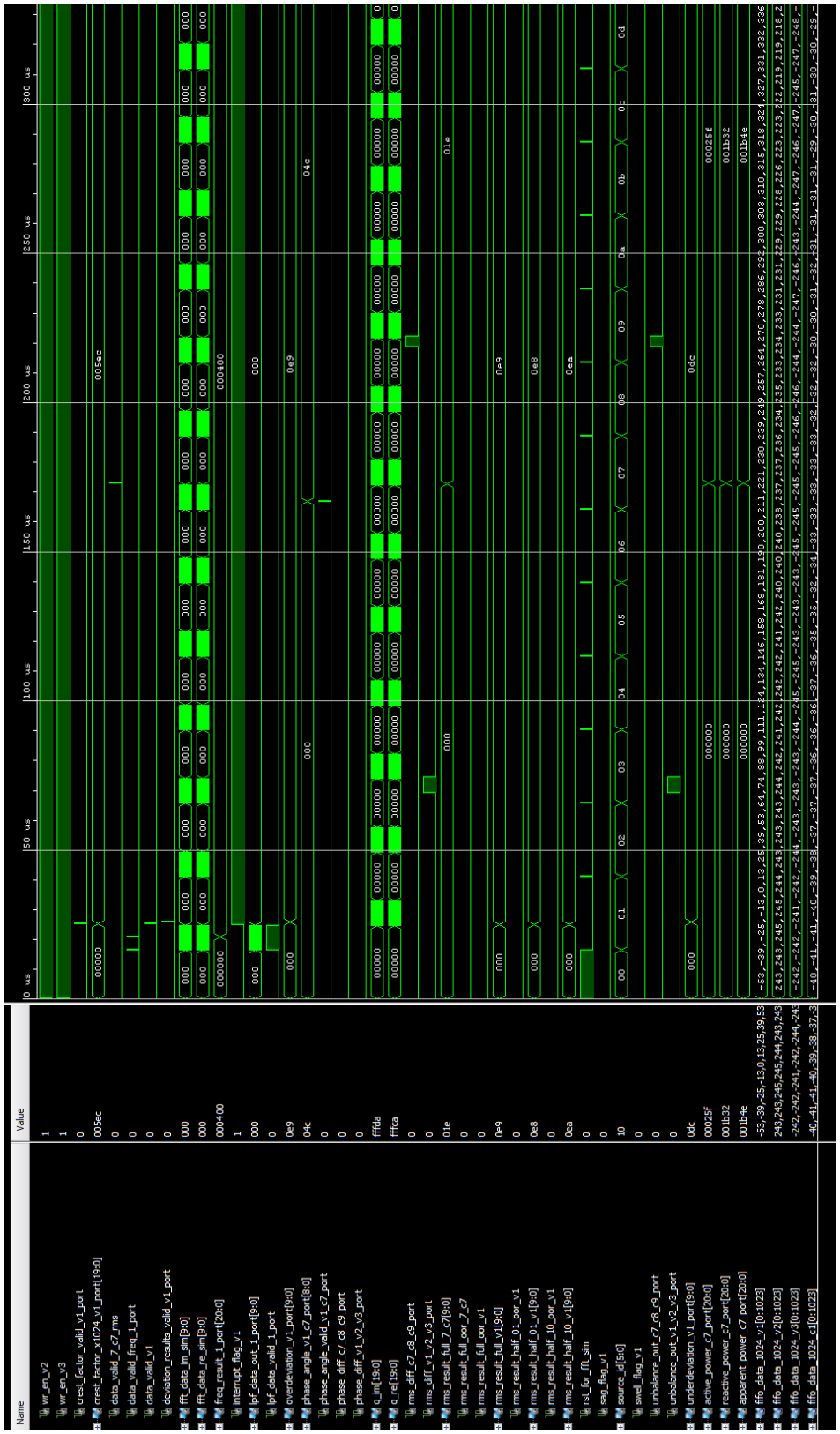

Figure 5.32: Overall System Simulation Overview

Harmonic Calculation Unit result is evaluated in the same way as was explained in sub-system evaluation section. Results are compared with MatLAB results and are presented in Table 5.13. Obtained results are also shown in the following figure as a graph.

Table 5.13: Overall System Harmonic Result Comparison

Harmonics	Expected Amplitude	MatLAB Result	FPGA Result	FPGA Result Amplitude	% Error
1	310	158760	156806	306.26	-1.22
2	31	15860	15709	30.68	-1.04
3	37.2	18940	18908	36.93	-0.73
4	46.5	23590	23545	45.98	-1.13
5	62	31710	32043	62.58	0.93
6	43.4	22010	22299	43.55	0.34
7	27.9	13790	13975	27.29	-2.24
8	24.8	12310	12707	24.82	0.08
9	34.1	17410	17947	35.05	2.68
10	15.5	7690	7861	15.35	-0.98

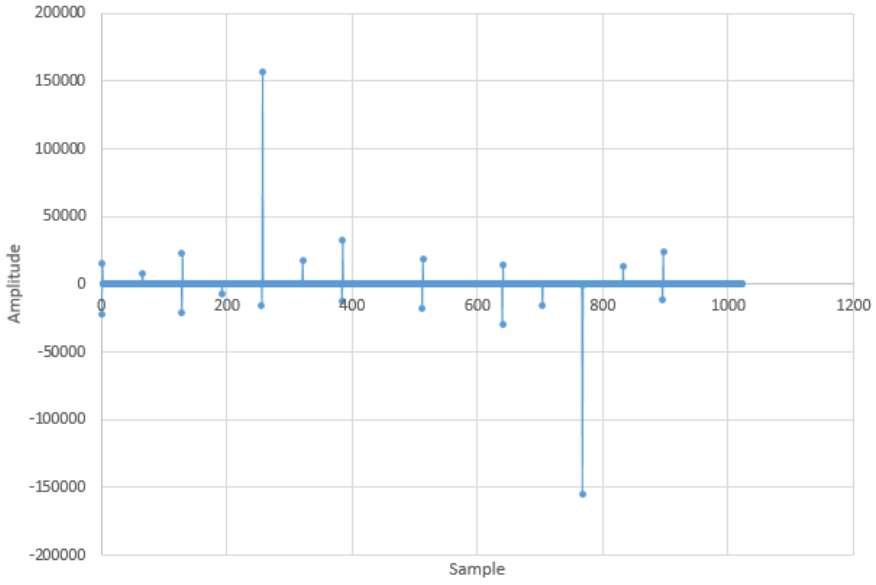

Figure 5.33: Overall System Harmonic Result Graph

Power frequency is measured as 1024 (hexadecimal: 400) and is shown in Figure 5.34. The expected result is 1024. Percentage error is 0.

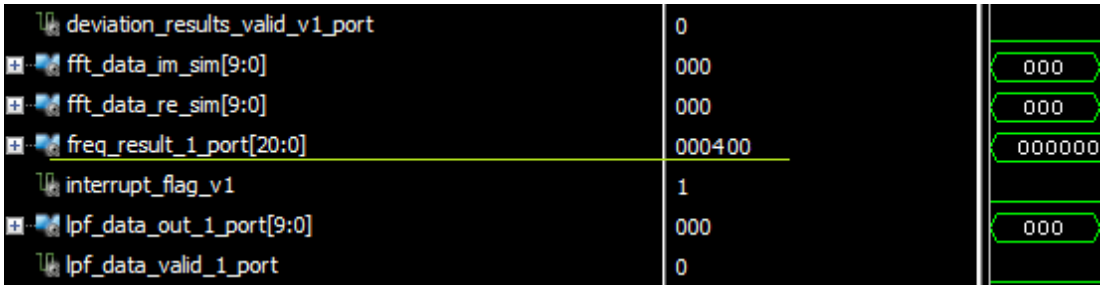

Figure 5.34: Overall System Power Frequency Result

Magnitude Calculation Unit result is given in Figure 5.35 for voltage and in Figure 5.36 for current. Expected results for both the supply voltage and current are calculated on MatLAB and compared with the obtained results. Results and percentage error are provided below (exp: expected, obt: obtained):

$Vrms_{exp}$ = 233.4240 V

$Irms_{exp}$ = 30.0013 A

$Vrms_{obt}$ = 233 V (hexadecimal: E9)

$Irms_{obt}$ = 30 A (hexadecimal: 1E)

% Error (Voltage) = (233 – 233.4240) / 233 * 100 = -0.18197

% Error (Current) = (30 – 30.0013) / 30 * 100 = -0.00433

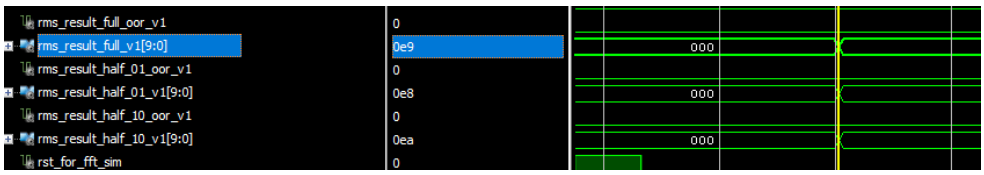

Figure 5.35: Overall Magnitude Calculation Voltage Result

Figure 5.36: Overall Magnitude Calculation Current Result

Phase angle calculation depends on the transition from negative to positive values and its index in test data array. Transition index is 4 for voltage and 222 for current. Thus, the expected result is calculated as follows:

φ = (222 – 4) * 360 / 1024 = 76.641^{o}

Obtained result is 76^{O} (hexadecimal: 4C) as shown in Figure 5.37. Percentage error is calculated as follows:

% Error = (76 – 76.641) / 85 * 100 = 0.8434 %

Figure 5.37: Overall Phase Angle Calculation Result

Unbalance detection result is shown in Figure 5.38. Short duration high result on rms_diff flag is caused by calculation of magnitudes at different times. As soon as three magnitude results are ready, unbalance flag is asserted low as shown in Figure 5.39. This result is obtained from a different simulation with a different set of output ports for a closer look to Unbalance Detection Unit.

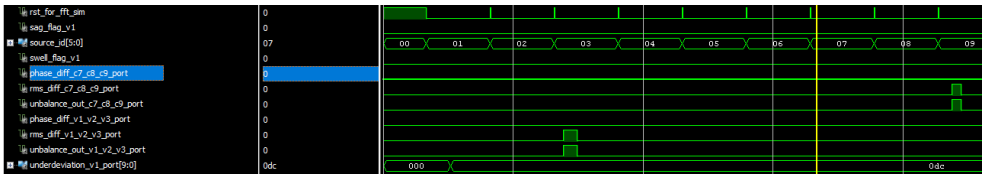

Figure 5.38: Overall Unbalance Detection Result

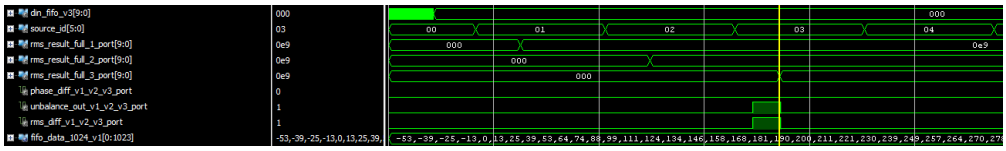

Figure 5.39: Overall Unbalance Detection Result Individual Test

Power calculation results are presented in Figure 5.40. Expected results are calculated with obtained phase angle to only evaluate this unit's functionality. Results and percentage errors are provided below (exp: expected, obt: obtained):

P_{exp} = 230 * 30 * cos(85^o) = 601.3746 W

Q_{exp} = 230 * 30 * sin(85^o) = 6873.7434 VAr

S_{exp} = 230 * 30 = 6900 VA

Obtained results from simulation are as follows:

P_{obt} = 607 W (hexadecimal: 25F)

Q_{obt} = 6962 VAr (hexadecimal: 1B32)

S_{obt} = 6990 VA (hexadecimal: 1B4E)

% Error (P) = (607 – 601.3746) / 607 * 100 = 0.92675 %

% Error (Q) = (6962 – 6873.7434) / 6962 * 100 = 1.26769 %

% Error (S) = (6990 – 6900) / 6990 * 100 = 1.2875 %

Figure 5.40: Overall Power Calculation Result

Parameter Calculation Unit underdeviation and overdeviation results are given in Figure 5.41 and crest factor result is presented in Figure 5.42. Magnitude calculation valid signal is asserted high during more than 10 cycles to trigger 200ms aggregated calculation of underdeviation and overdeviation. For expected results, obtained Vrms result is used to only evaluate this unit's functionality.

For a constant U_{din} = 220 V, the expected underdeviation result should be U_{din} and the overdeviation result should be Vrms. The obtained results for these parameters confirm functionality.

Underdeviation = 220 (hexadecimal: DC)

Overdeviation = 233 (hexadecimal: E9)

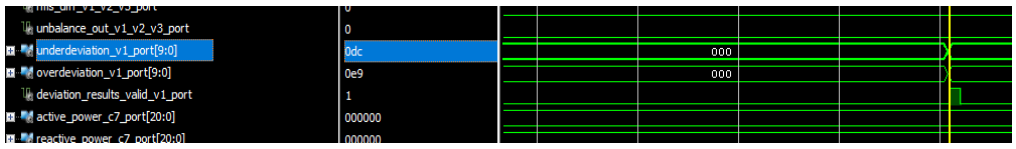

Figure 5.41: Overall Underdeviation and Overdeviation Result

The expected result of crest factor is as follows:

V_{max} = 344 V

CF_{exp} = 344 / 233 = 1.47639

The obtained result of crest factor multiplied with 1024 is as follows:

CF_{obt} = 1516 (hexadecimal: 5EC) / 1024 = 1.48047

Percentage error is calculated as;

% Error = (1.48047 – 1.47639) / 1.48047 * 100 = 0.275588 %

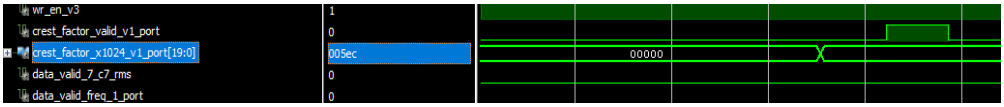

Figure 5.42: Overall Crest Factor Result

All of the obtained results as well as calculated percentage errors are presented in Table 5.14 for an overview.

Table 5.14: Overview of the Obtained Results

Parameter	Measured / Calculated	% Error
Harmonics (1)	156806	-1.22
Harmonics (2)	15709	-1.04
Harmonics (3)	18908	-0.73
Harmonics (4)	23545	-1.13
Harmonics (5)	32043	0.93
Harmonics (6)	22299	0.34
Harmonics (7)	13975	-2.24
Harmonics (8)	12707	0.08
Harmonics (9)	17947	2.68
Harmonics (10)	7861	-0.98
Frequency	50	0
Voltage Magnitude	233	-0,18
Current Magnitude	30	-0,01
Phase Angle	76	0.84
Unbalance	Detected	0
Active Power	607	0.93
Reactive Power	6962	1.27
Apparent Power	6990	1.29
Underdeviation	220	0
Overdeviation	233	0
Crest Factor	1.48047	0.28

For timing evaluation, 125MHz timing constraint is applied and post-implementation timing summary report shows compatibility as in Figure 5.43. Operating frequency result is given in Figure 5.44.

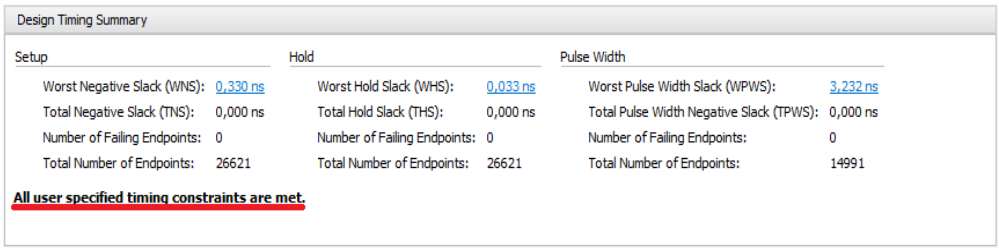

Figure 5.43: Overall Post-Implementation Timing Report

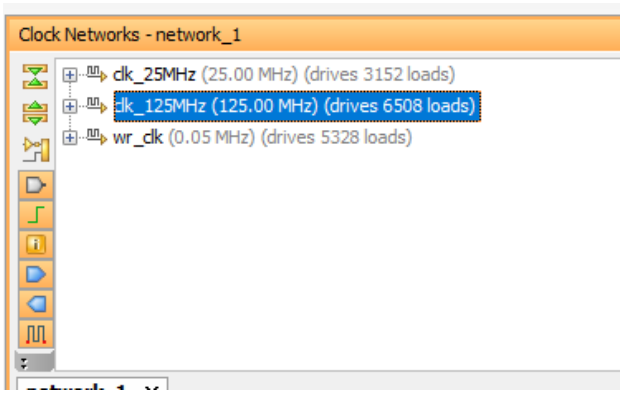

Figure 5.44: Overall Operating Frequency

For resource evaluation, post-implementation resource utilization report for 48 channels is provided in Table 5.15. In this report, IO utilization should not be taken into account. This is caused by simulating two channels by setting their unit results as output ports as was mentioned at the beginning of this section.

Table 5.15: Overall Post-Implementation Resource Utilization

Resource	Utilization	Available	Utilization %
LUT	33631	218600	15.38
LUTRAM	396	70400	0.56
FF	14331	437200	3.28
BRAM	52.50	545	9.63
DSP	46	900	5.11
IO	342	362	94.48
BUFG	3	32	9.38

Post-implementation power report is shown in Figure 5.45. Also, Post-Implementation device view is given in Figure 5.46 to display routing resources.

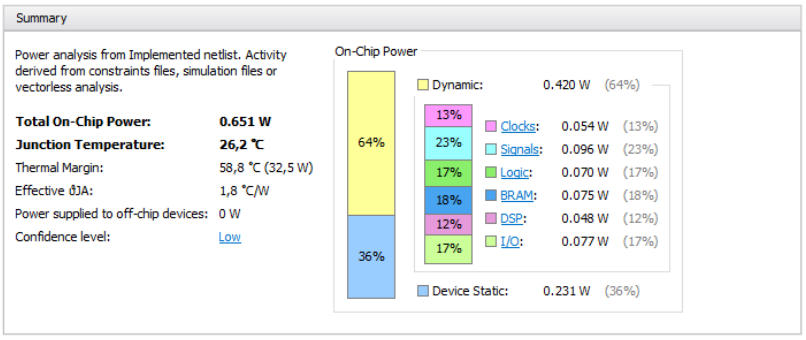

Figure 5.45: Overall Post-Implementation Power Report

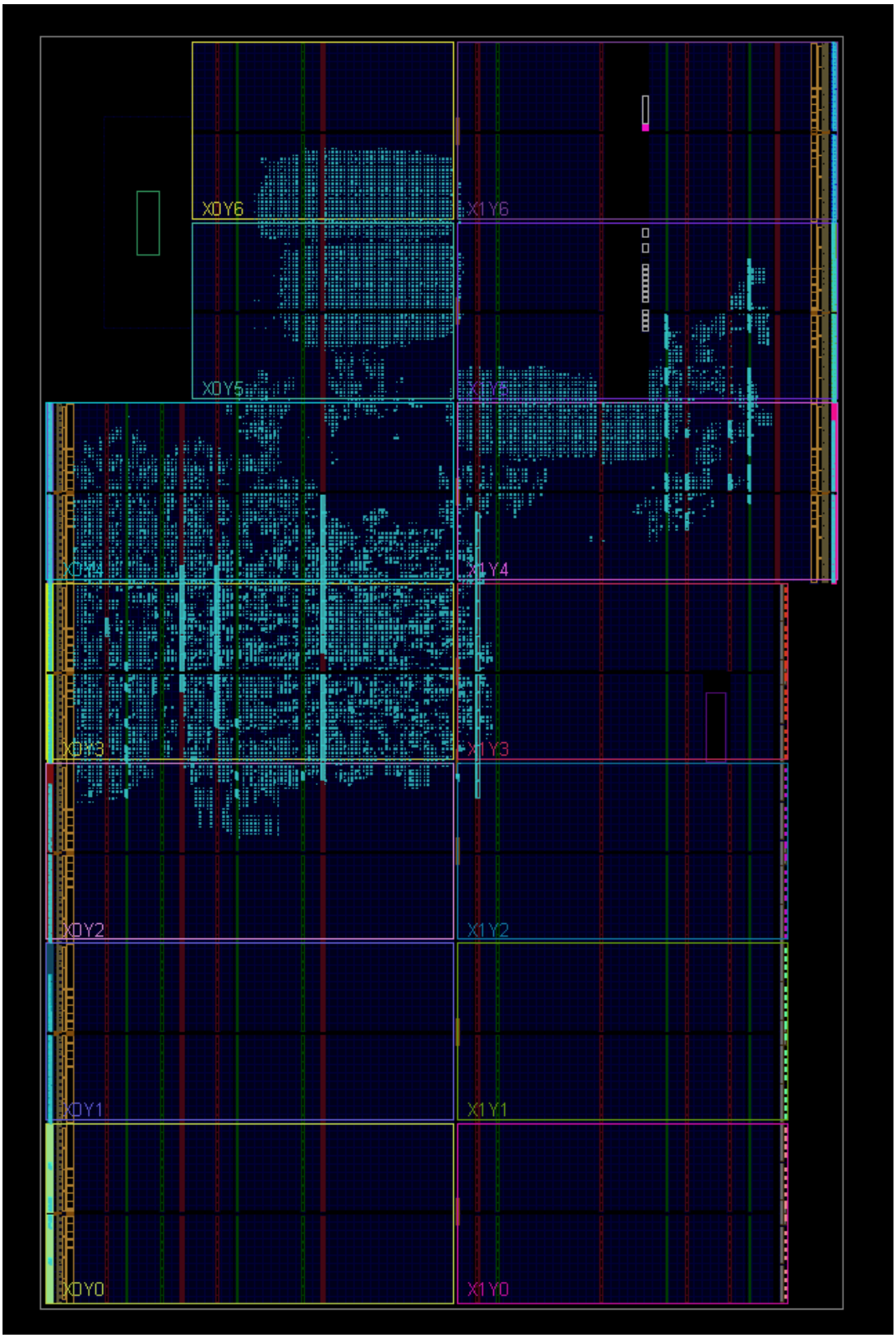

Figure 5.46: Overall Post-Implementation Device View

CHAPTER VI

CONCLUSION AND FUTURE WORK

In this thesis, a real-time, high-performance, low cost architecture which is suitable for being the processor unit of a power quality monitoring system is designed and implemented on FPGA. Standard-defined power quality parameters are measured and/or calculated. These sub-systems and overall system architectures are tested individually using synthetic data constructed on MatLAB. The architecture is evaluated in terms of accuracy, timing requirements and resource utilization.

One of the main objectives of this study is to fit the circuit in the smallest FPGA possible. After getting post-implementation resource utilization result of the overall design for Zynq 706 Evaluation Board, smaller FPGAs are searched. The same design is synthesized for XC7Z015CLG485, which is currently 130$ [35]. Post-synthesis design resource utilization is shown in Figure 6.1.

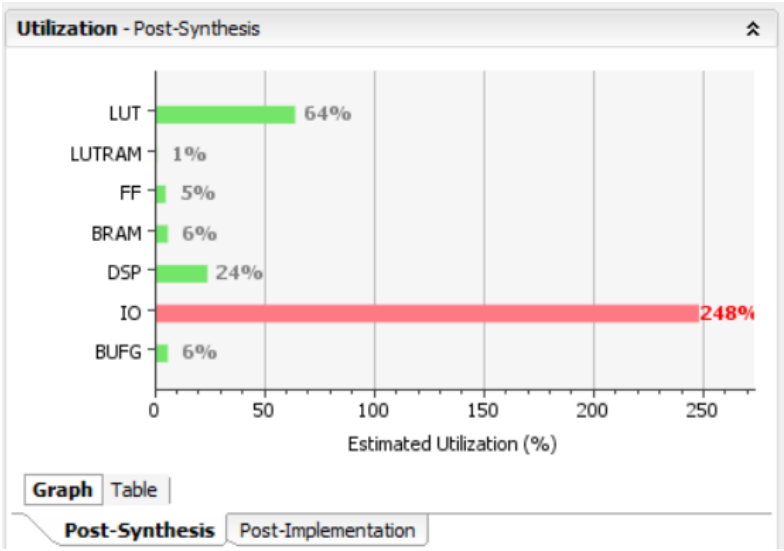

Figure 6.1: Post-Synthesis Resource Utilization for XC7Z015

IO utilization is trivial for this implementation. The synthesized design is the one used for implementing on Zynq 706 for comparison. Implementing BRAMs for storage and then reading results in order are the solution for this utilization problem.

Operating frequency for this synthesis is obtained as 66.66MHz, which is more than enough for our time-multiplexed architecture. Harmonic Calculation Unit sets the upper bound for timing. Total computation time for this clock frequency is calculated as: 48 * (1034 + 1024) * 15 ns = 1481760 ns and this is not exceeding real-time operation requirement.

Developed system is not capable of aggregating the calculated results as defined in IEC 61000-4-30. Power quality parameters are measured and/or calculated in every cycle of the power system. For future work, results of the parameters could be aggregated on ARM side on the Zynq device. In this way, floating point computations could easily be done and data loss would not be too much in comparison to FPGA.

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