ASSESSMENT OF FLEXIBLE SINGLE CRYSTAL SILICON THIN FILM TRANSISTORS

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submitted by **MUAMMER KOZAN** in partial fulfillment of the requirements for the degree of **Master of Science in Micro and Nanotechnology Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Almıla Güvenç Yazıcıoğlu
Head of Department, **Micro and Nanotechnology** _____

Prof. Dr. Ahmet Oral
Supervisor, **Micro and Nanotechnology, METU** _____

Assist. Prof. Dr. Selçuk Yerci
Co-Supervisor, **Electrical and Electronics Engineering, ODTÜ** _____

Examining Committee Members:

Prof. Dr. Ali Çırpan
Chemistry, ODTÜ _____

Prof. Dr. Ahmet Oral
Micro and Nanotechnology, METU _____

Assoc. Prof. Dr. Hande Toffoli
Physics, ODTÜ _____

Assist. Prof. Dr. Serdar Kocaman
Electrical and Electronics Engineering ODTÜ _____

Assoc. Prof. Dr. Şinasi Barış Emre
Physics Engineering, Ankara University _____

Date: 09.09.2019

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Muammer Kozan

Signature:

ABSTRACT

ASSESSMENT OF FLEXIBLE SINGLE CRYSTAL SILICON THIN FILM TRANSISTORS

Kozan, Muammer
Master of Science, Micro and Nanotechnology
Supervisor: Prof. Dr. Ahmet Oral
Co-Supervisor: Assist. Prof. Dr. Selçuk Yerci

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Mechanically flexible large-area electronics are becoming more popular with such devices as sensors and medical devices. Organic, inorganic and organic/inorganic hybrid materials have been used for these systems. Although inorganic silicon is used for these systems, it is mostly in the amorphous or polycrystal form. Electron and hole mobilities for these forms are lower than single-crystal silicon. Therefore, to make a high-performance transistors single crystal silicon should be used. In this thesis, flexible single-crystal silicon thin-film transistors are tried to build and characteristics of the devices are examined. In the building process firstly, Si wafers are doped with SOD material and SOG is used as the dielectric material. To form the flexible single-crystal Si layer SOI wafers and KOH etched Si wafers are used. When silicon is thinned it is harder to handle; therefore, kapton tape is used as a plastic substrate. After forming the thin Si layer MOSFETs are designed to build in three different sizes. Gate lengths of these transistors are designed to be 50 μm, 75 μm, and 100 μm. Width of the transistors are tried to be kept the same around 400nm, thus different W/L ratios for each transistor can be achieved. By following these design parameters successful thick Si substrate MOSFETs are formed. Characterization for the built devices are done with Nanomagnetic Instruments ezHEMS device and Keithley 2612 source

meter. With the help of the generally accepted transistor equations found I_{DS} and mobility values are used to calculate some other transistor parameters. On the other hand, due to the fragile structure of thinned Si wafer, a successful flexible single-crystal thin film transistor cannot be built. However, it is shown that with a specifically designed cleanroom tools for thin silicon layer handling functional flexible thin-film transistors can be achieved.

Keywords: Flexible thin-film transistor, SOD, MOSFET, Single-crystal silicon

ÖZ

ESNEK TEKLİ KRİSTAL YAPILI SİLİSYUM İNCE FİLM TRANSİSTÖRLERİN İNCELENMESİ

Kozan, Muammer
Yüksek Lisans, Mikro ve Nanoteknoloji
Tez Danışmanı: Prof. Dr. Ahmet Oral
Ortak Tez Danışmanı: Dr. Öğr. Üyesi Selçuk Yerci

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Mekanik olarak esnek geniş alanlı elektronik cihazlar medikal uygulamalar ve sensörler ile gittikçe popülerleşmeye başladı. Organik, inorganik ve organik/inorganik hibrit yapıdaki malzemeler mekanik olarak esnek ve geniş alanlı elektronik cihazlarda kullanıldı. Bu sistemler için inorganik malzeme olarak silisyum kullanılmasına rağmen kullanılan silisyum amorf ve çoklu kristal yapılıydı. Amorf ve çoklu kristal yapılı silisyumda elektron ve hole hareketliliği tekli kristal yapılı silisyumdan küçük olduğu için yüksek performanslı bir transistör üretiminde tekli kristal yapısında silikon kullanılmalıdır. Bu tez çalışmasında esnek tekli kristal yapılı silisyum ince film transistörler yapılmaya çalışılmıştır ve tasarlanan yapılan cihazların çalışma karakteristiği incelenmiştir. Oluşturma sürecinde öncelikle Si pullar SOD malzemesi ile katkılandı ve SOG malzemesi yalıtkan olarak kullanıldı. Esnek tekil kristal Si tabakaların oluşturulması için SOI pul ve KOH ile aşındırılmış Si pul kullanıldı. Silisyum inceltildiği zaman işlemesi zor bir malzeme olduğundan kapton bant ince silisyum tabakaya taban olarak kullanıldı. İnce tabaka Si elde edildikten sonra MOSFET'ler üç farklı boyutta tasarlandı. Bu transistörlerin kapı uzunluğu 50 μm, 75 μm ve 100 μm olarak tasarlandı. Farklı W/L oranı elde edilebilmesi için genişlik parametresi 400 μm etrafında sabit tutulmaya çalışıldı. Bu parametrelere uyarak kalın

Si alttaşlı MOSFET'ler oluşturuldu. Oluşturulan cihazların karakterizasyonu Nanomanyetik Cihazlar şirketinin Ez-HEMS cihazı ve Keithley şirketinin 2612 kodlu kaynakölçer cihazıyla yapıldı. Genel kabul görmüş transistor denklemlerinin yardımıyla bulunan I_{DS} ve hareketlilik değerleri diğer transistor parametrelerini hesaplamak için kullanıldı. Öte yandan inceltilmiş Si pulun kırılgan yapısından dolayı esnek tekli Kristal ince film transistörler yapılamadı. Ancak özellikle ince film silisyum tabaka idare etmek için kullanılacak temiz oda gereçleri ile esnek ince film transistörlerin oluşturulabileceği gösterilmiştir.

Anahtar Kelimeler: Esnek ince film transistör, SOD, MOSFET, Tekli kristal silisyum

To my family

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LIST OF ABBREVIATIONS

TFT	Thin Film Transistor
MESFET	Metal semiconductor field-effect transistor
MISFET	Metal insulator semiconductor field-effect transistor
MOSFET	Metal oxide semiconductor field-effect transistor
LCD	Liquid crystal display
CVD	Chemical vapor deposition
μ_{eff}	Effective mobility
μ_{sat}	saturation mobility
μ_{FE}	Field effect mobility
FET	Field effect transistor
NMOS	N-type Metal Oxide semiconductor
V_T	Threshold voltage
IC	Integrated circuit
V_{GS}	Gate to source voltage
I_{DS}	Drain to source current
V_{DS}	Drain to source voltage
C_i	Gate capacitance per unit area
g_{DS}	Conductance
g_m	Transconductance
f_{CO}	Cut off frequency
ADP	Atmospheric downstream plasma
DCE	Dry chemical etching
AFM	Atomic force microscope
rms	Root mean square
CMP	Chemical mechanical polish
TMAH	Tetra methyl ammonium hydroxide
eV	Electron volt
SOI	Silicon on insulator
PDMS	polydimethylsiloxane
ITO	Indium tin oxide
SOD	Spin on dopant
SOG	Spin on glass
RTA	Rapid thermal annealing
BOE	Buffered oxide etchant
PI	Polyimide
PET	Polyethylene terephthalate
NM	Nano membrane
FinFET	Fin field effect transistor
DUV	Deep ultraviolet lithography
FGA	Forming gas anneal
DRIE	deep reactive ion etching
ALD	Atomic layer deposition

Sq	Square
HEMS	Hall effect measurement systems
UV	Ultraviolet
IV	Current voltage

LIST OF SYMBOLS

CdS	Cadmium Sulfide
CdSe	Cadmium Selenide
a-Si:H	Amorphous Silicon
Poly-Si	Poly Crystalline Silicon
c-Si	Single Crystalline Silicon
W	Channel width
L	Channel length
HNO_3	Nitric acid
HF	Hydrofluoric acid
KOH	Potassium hydroxide
SiO_2	Silicon dioxide
Ar	Argon
CF_4	Carbon tetrafluoride
PH_3	Phosphane
B_2H_6	Diborane
BBr_3	Boron tribromide
$POCl_3$	Phosphoryl chloride
BF_3	Boron trifluoride
Al	Aluminum
Au	Gold
V	Volt
F	Farad
A	Ampere
SiH_4	Silane
Ti	Titanium
TiN	Titanium nitride
HfO_2	Hafnium Oxide
H_2	Hydrogen
N_2	Nitrogen
N_2O	Dinitrogen monoxide
Cr	Chromium
Xe_2F	Xenon difluoride
Al_2O_3	Aluminum oxide
SiN	Silicone Nitride
P	Phosphorus
KI	Potassium iodide
I	Iodine
O_2	Oxygen
t	Distance between same size NMOS
ε_0	Permittivity of free space
ε_r	Dielectric constant

CHAPTER 1

INTRODUCTION

Invention of the transistor was at Bell Laboratories on December 23, 1947, in Murray Hill, New Jersey. William Shockley, John Bardeen, and Walter Brattain were the inventors; however, the contribution of William Shockley, who had been working for a semiconductor-based switching device for a decade, was more significant [1].

Although the first transistor created in 1947, a conceptual framework for thin-film transistors (TFTs) was presented by Lilienfeld in 1930. This conceptual work can be identified today as a metal-semiconductor field-effect transistor (MESFET). Five years later Lilienfeld introduced a new concept which is called metal insulator semiconductor field-effect transistor (MISFET)[2].

After the invention of the transistors and after their technological advantages such as switching capability was observed, more complex transistors were developed. In 1960s first metal oxide semiconductor field-effect transistor(MOSFET) and the first TFT are produced [2]. TFTs in this era were made using compound semiconductors such as CdS or CdSe. Effective mobility (μeff) for CdS and CdSe TFTs were higher than 40 cm2/Vs. In 1973 first Liquid crystal display (LCD) was produced with CdSe TFTs. Unfortunately, this kind of LCD has never been produced on a large substrate area. The main reasons were reliability over large areas and the uncontrollability of properties of compound semiconductors [3].

In 1979 an important step in TFT progress was taken. Spear and Le Comber at the University of Dundee in Scotland produced a TFT with hydrogenated amorphous silicon (a-Si:H). They produced a-Si:H in by glow discharge plasma chemical vapor deposition (CVD). They noticed that electrical properties of a-Si:H can be controlled by phosphorous(P) and boron (B) impurities because dangling bonds in a-Si are

terminated by hydrogen [4]. Even though a-Si:H TFTs have low μeff values compared to polycrystalline Si, large-area fabrication was possible with a-Si:H. Therefore a-Si:H thin films were chosen to be the primary semiconductor material for TFTs which will used in active matrix LCDs. Active Matrix LCDs are a type of screens which has a built-in driving circuit behind the screen panel. To build TFTs with larger mobility, developers in the 80's began to use pol-Si films. Poly-Si thin films ensured higher performance than a-Si:H; however, they required a high-temperature process to produce. Thus in the 90s low temperature, the poly-Si production method at around 550 ˚C process was introduced. Before the low-temperature process is introduced poly-Si is produced around 750 ˚C. However, in a low-temperature process, large-area applications were still a major problem. Organic semiconductors also investigated in the 90s. They have major advantages over poly-Si with low processing temperature, however, their lack of stability and low-performance parameters is still an issue today [2]. In recent years there are many studies on single crystal silicon(c-Si) TFTs. By using c-Si performance parameters can be improved significantly and since c-Si is used in the electronics industry for long time problems such as stability and large-area application can be overcome [5].

1.1. TFT Operation and Structure

TFTs are a class of field-effect transistors (FET) which consist of the semiconductor layer, dielectric layer, and conductive layer. In the conductive layer, there are three terminals of TFTs which are a drain, source, and gate. TFTs and MOSFETs have some similarities; however, there are some key differences both in their structure and working principle. First of all semiconductor layer in TFTs are amorphous or polycrystalline; on the other hand, the semiconductor layer in MOSFETs is mostly single crystalline. There is also a difference in the substrate layer. TFTs use insulator substrate and MOSFETs mostly uses semiconductor substrates. And related to substrate issue TFTs rely on accumulation as a working principle and MOSFETs rely on inversion in working principle. In Figure 1.1 structures for a TFT and a MOSFET can be found.

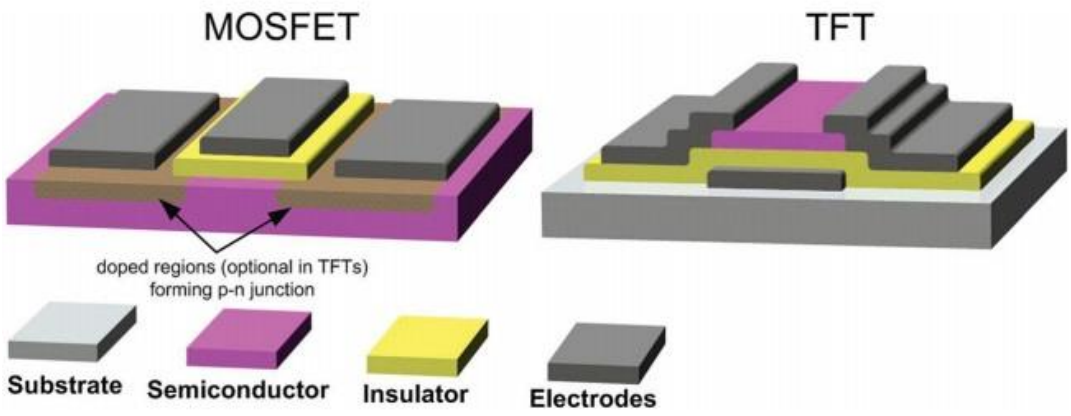


Figure 1.1. Physical structures of MOSFET and TFT [6]

There are four different TFT structures with four different layer configurations. Based on the of the terminals these structures can be either coplanar or staggered (whether gates and drain-source are on the same side or opposite sides) and according to gate position they can be either bottom or top gate. Fabrication choice, processing temperature, lithography mask, etc. can create different advantages for different TFT structures. For example, when the dielectric layer requires high temperatures staggered bottom gate structures are commonly used, whereas if the semiconductor layers, such as poly-Si, require high temperature, using coplanar top gate structure can be advantageous. In Figure 1.2 four different structures for TFT can be seen [7,8]

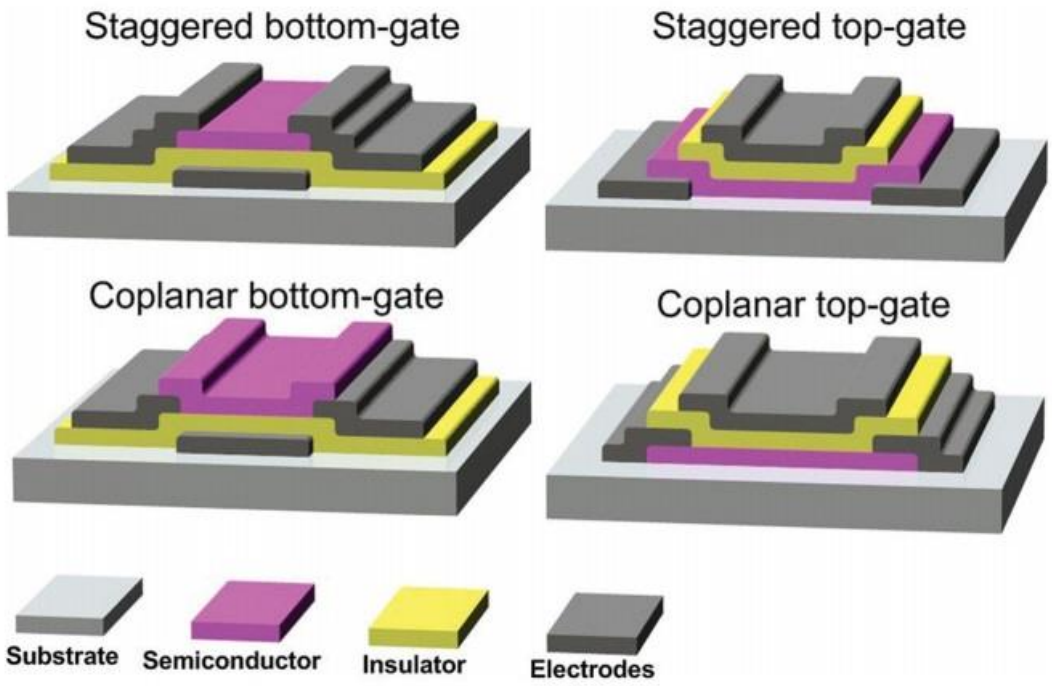


Figure 1.2. Four most commonly used physical structures for TFT [6]

Focusing on operation, in n-type TFTs enhancement or depletion mode can be decided by considering whether the threshold voltage (V_T) is positive or negative. In enhancement mode, a positive V_T is required to open gate-to-source channel and in depletion mode, the gate-to-source channel is always open and a negative V_T voltage is required to close the channel. Enhancement mode is more preferred because in depletion mode positive V_T should be applied to the device to turn off. Nevertheless, depletion type device is very advantageous for certain integrated circuit (IC), such as loads for NMOS logic circuitry.

To turn on the device gate-to-source voltage (V_{GS}) should be bigger than V_T. When the TFT is turned on a large density of electrons is accumulated in the semiconductor and insulator interface. Furthermore, a relatively large drain-to-source current (I_{DS}) flows according to drain-to-source voltage. (V_{DS}) State of $V_{GS} > V_T$ is called on state and it has two main sub-states depending on V_{DS}:

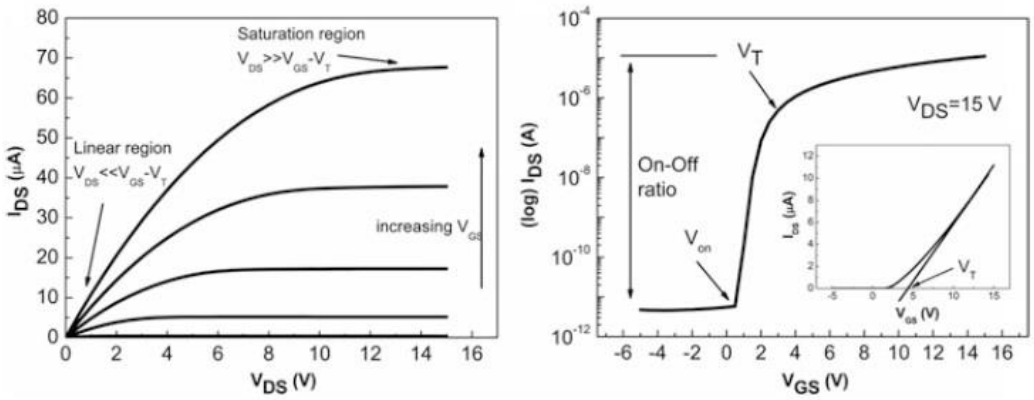


Figure 1.3. Typical output and transfer curves for n-type TFT [2]

- When $V_{DS} << V_{GS} - V_T$ n type TFT is in linear region and I_{DS} can be calculated as:

$$I_{DS} = C_i \mu_{FE} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2], \qquad (1.1)$$

  C_i is the gate capacitance per unit area, μ_{FE} the field-effect mobility, W the channel width, and L the channel length of the device.

- When $V_{DS} >> V_{GS} - V_T$ n-type TFT is in saturation region and I_{DS} can be calculated as

$$I_{DS} = \frac{1}{2} C_i \mu_{sat} \frac{W}{L} (V_{GS} - V_T)^2, \qquad (1.2)$$

  μ_{sat} is saturation mobility.

In Figure 1.3 a characterization for TFT which involves output and transfer curve can be seen. Output curves provide information about the effectiveness of channel pinch off and contact resistance. Channel pinch of describes the end point of the charge accumulation on the semiconductor material of TFT, and contacts resistance is the resistance between metal contact and semiconductor gate and drain terminals.

Transfer curve provides information about the following electrical parameters:

- On-off ratio – This parameter is simply the ratio of highest I_{DS} in the on state and lowest I_{DS} in the off state values in a TFT. Higher I_{DS} results in better driving capability and lower I_{DS} results in low leakage current. Therefore, lower on-off ratio is preferable;
- Threshold voltage (V_T) – It corresponds to the value of V_{GS} when accumulation of the electrical charge between the insulator layer and semiconductor layer interfaces rises a significant value. V_T can be calculated by using a linear extrapolation of the I_{DS}-V_{GS} at low V_{DS};
- Turn-on voltage – It is the V_{GS} value in which I_{DS} rises drastically. It can be observed in the I_{DS}-V_{GS} curve in Figure 1.3 easily;
- Subthreshold swing (S) – It is the V_{GS} value required to raise I_{DS} by one decade.

$$S = \left(\frac{dlog(I_{DS})}{dV_{GS}}|max\right)^{-1}, \qquad (1.3)$$

Lower S value is preferred because it results in low power consumption and higher speed

Mobility is the main parameter that affects the maximum I_{DS} and the switching speed. There are several different ways to determine mobility and most relevant ways are given below:

- Effective mobility – It is regarded as the closest estimation for the μ value. To be determined conductance (g_{DS}) and V_T must be calculated at low V_{DS}:

$$\mu_{eff} = \frac{g_{DS}}{C_i\frac{W}{L}(V_{GS}-V_T)}, \qquad (1.4)$$

- Field-effect mobility – It is a very common way to determine μ value in TFTs. To calculate transconductance (g_m) at low V_{DS} must be acquired:

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_{DS}}, \quad (1.5)$$

- Saturation mobility – It is calculated very similar to μ_{FE} and also to calculate it g_m must be determined. However, high-value V_{DS} must be used:

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2}{\frac{1}{2} C_i \frac{W}{L}} \quad (1.6)$$

The mobility of the free carriers in the channel of a TFT device has a direct effect on maximum operating frequency or cut off frequency. (f_{CO})The performance of a TFT circuit is sensitive to this parameter. It can be calculated: with:

$$f_{CO} = \frac{\mu V_{DS}}{2\pi L^2} \quad (1.7)$$

All of the mentioned parameters have great importance in evaluating TFTs and they help researchers understand whether devices can be integrated into more complex systems [2], [6].

1.2. Flexible TFT Structures

Flexible electronics is a relatively new and rapidly raising branch of electronics. According to per market projection by IDTechx, the market value of printed and flexible electronics will exceed 70 B USD by 2027. To build flexible electronic devices, flexible TFTs are needed as building blocks. Previously described TFT technologies can be integrated into flexible substrates such as polymer films,

metal sheets ,and paper. In this integration, both process temperature of TFT and compatibility between materials that are used in TFT have major importance. The reliability and stability of the TFT device are also major factors in flexible electronics. Flexible amorphous silicon (a-Si) is used as a semiconductor layer for TFTs in flexible TFTs. Due to low charge carrier mobility (around $1cm^2/Vs$) new types of semiconductor materials are desired. Organic semiconductors have also been investigated in recent years for flexible TFTs because of their inherent flexible structure and low process temperature. However organic semiconductors have relatively low mobility and stability. Search for high mobility and stability materials are continued with oxide semiconductors and poly-Si. Poly-Si has a higher process temperature; therefore, producing flexible TFT arrays is harder. Oxide semiconductors have relatively higher mobility and lower process temperature; however, to get higher mobility c-Si offers the best option. Although the c-Si transistor offers charge carrier mobility exceeding 1000 cm^2/Vs, the processing temperature for c-Si transistor is higher than 900 ˚C [9-11]. In this thesis work we attempt to build c-Si thin film by solving the above mentioned issues. First production attempts from before researches are summed up.

CHAPTER 2

PRODUCTION METHODS FOR SINGLE CRYSTAL SILICON THIN FILM TRANSISTORS

2.1. Traditional Thinning Methods for Single Crystal Silicon Wafer

For numerous operations thinned silicon wafers are used extensively. The main goal for thinning silicon wafer is to minimize the packaged circuits in mobile devices such as cellular phones, memory cards, tablets, etc. To achieve high quality working devices at the end etching silicon wafer from the backside while fabricating the device on the front side is the most logical method. Time and cost efficiency is also significantly important in the thinning process. Several different methods have been developed over the years. Mechanical grinding, chemical mechanical polishing, chemical etching and atmospheric downstream plasma (ADP) dry chemical etching (DCE) can be considered four primary thinning methods. Since the desired thickness can be very thin, sometimes it is necessary to use these methods together [12].

2.1.1. Mechanical Grinding

Mechanical grinding offers a high thinning rate; therefore, it is the most preferred thinning technique. All of the commercial mechanical grinders offer two-step grinding. These steps are coarse grinding with a thinning rate of about 5 μm/sec and fine grinding with a thinning rate of about 1 μm/sec. Fine grinding step is necessary for removing the damaged layer and achieve better surface roughness. Mechanical grinding damages can be observed by X-ray topography, which shows most of the damage is located about 20 μm deep. With fine grinding most of this damage can be removed; however, the remaining defect band near the surface can still be observed in Figure 2.1

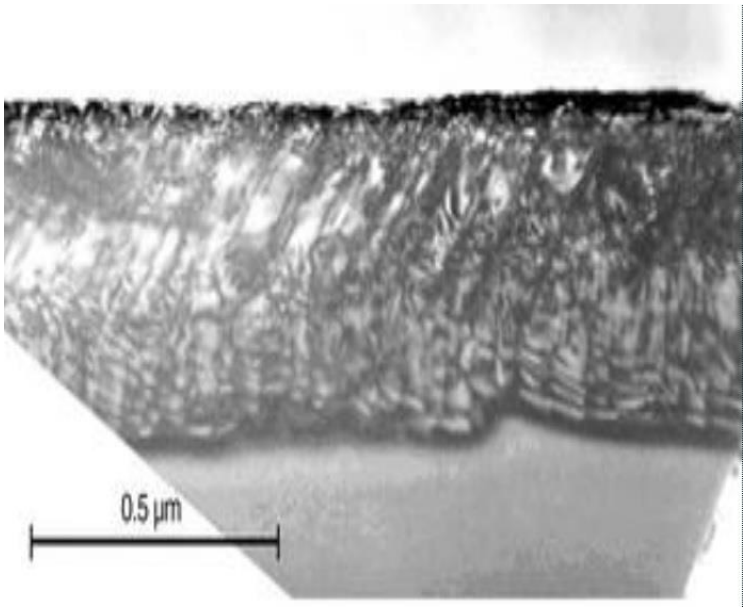


Figure 2.1. Near surface damage after mechanical grinding observed by transmission electron microscope. Surface damage is the area which has a darker color [12].

Defect band thickness is affected by thinning conditions and it is about 0.1 µm and 1 µm. Defects remaining after fine grinding also causes warpage in the silicon wafer. For further mechanical grinding on the wafer can cause broken samples. Therefore it can be deduced that additional thinning is necessary. Moreover, a high removal rate with coarse grinding causes rough wafer surfaces. Roughness values can be measured with the atomic force microscope (AFM) and it is around 2 µm (rms). Fine grinding can lower surface roughness to 2nm (rms) which is still 10 times larger than a polished silicon wafer. In summary, an additional thinning process is needed after mechanical grinding to remove the remaining defect layer and reduce surface roughness [12,13]. In Figure 2.2 and Figure 2.3 warpage and surface damage of the mechanical grinding can be seen respectively.

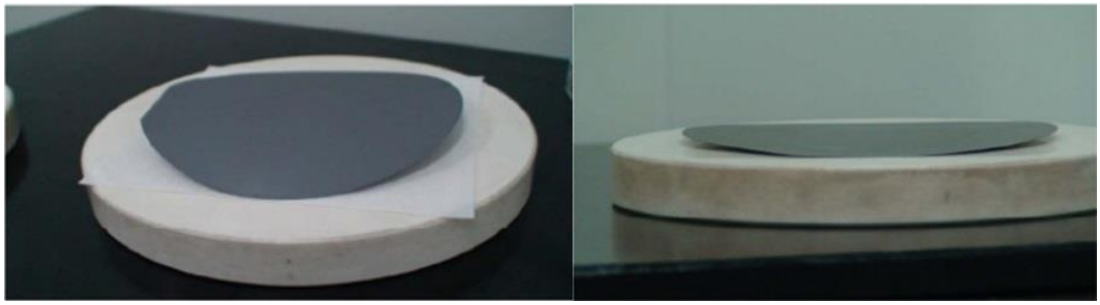


Figure 2.2. Picture of wafer warpage after mechanical grinding. Caused by near surface damage [13].

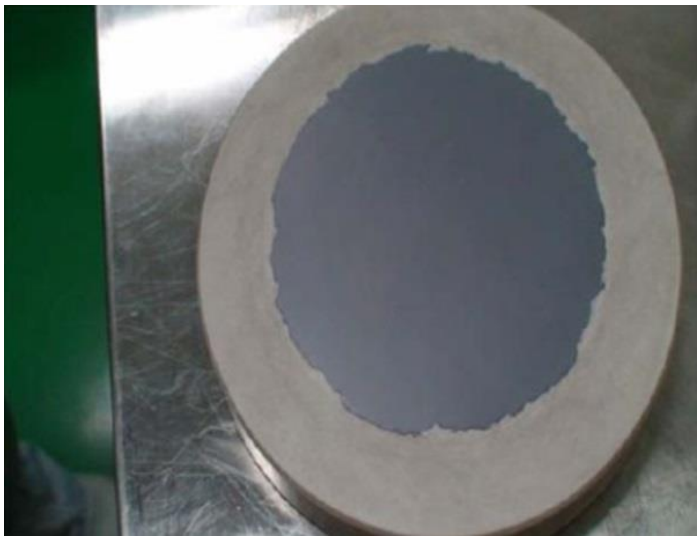


Figure 2.3. Wafer with rough surface after coarse mechanical grinding. To get higher speed grinding and thinner Si wafer all of the mechanical grinding is done with coarse grinding which results surface damage in the picture [13].

2.1.2. Chemical Mechanical Polishing

Chemical mechanical polishing is widely used technique in semiconductor industry. It is mainly used for reliable interconnects between multilayer chips and polishing thin silicon wafers. In the CMP process a wafer is rotated with a device which looks like spin coater and a carrier is press down on the wafer surface with a rotating polishing pad covered with silica slurry with specific chemical properties. (Figure 2.4) Thinning rate for CMP is only reaches a few micrometers per minute. Therefore, it is wise to use CMP after mechanical grinding for finer surfaces and devices[12,14].

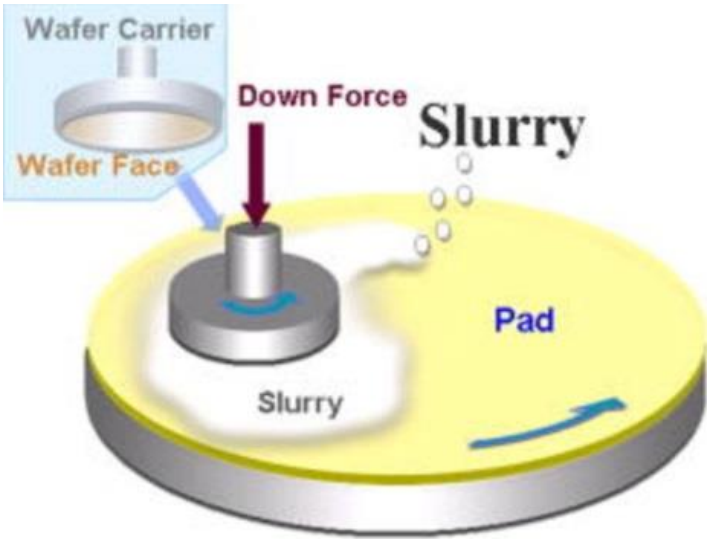


Figure 2.4. CMP diagram [15]

2.1.3. Wet Chemical Etching

Wet chemical etching is the most common etching technique for silicon. To etch one side of the wafer one approach is spin etching. As the name suggests spin etching is done by removing the etchant periodically by rotating the wafer. The most commonly used chemicals in spin etching are HNO3 and HF mixtures. Different mixtures of these two chemicals results in different etching rates [12]. Several other chemicals are widely used in silicon processing. Specifications for KOH and TMAH chemical etchants can be found in the following parts.

2.1.3.1. KOH Etching

KOH etching is classified as anisotropic etch which can be identified as unequal etching of the planes of the bulk silicon wafer. KOH selectively etches (100) plane much faster than (111) plane and results in V shape holes which has 54.7 ˚ angle with surface. In large areas and longer time etching, V shape does not occur. Selectivity of KOH between SiO2 and Si is also not sufficient enough to do etching in large proportions. The etching rate of KOH heavily depends on solution temperature and concentration. Roughness of the Si surface after KOH etching is also related to

concentration and it decreases with increasing concentration[16]. In Figure 2.5 and Figure 2.6 etching rate of KOH for Si and SiO2 can be found.

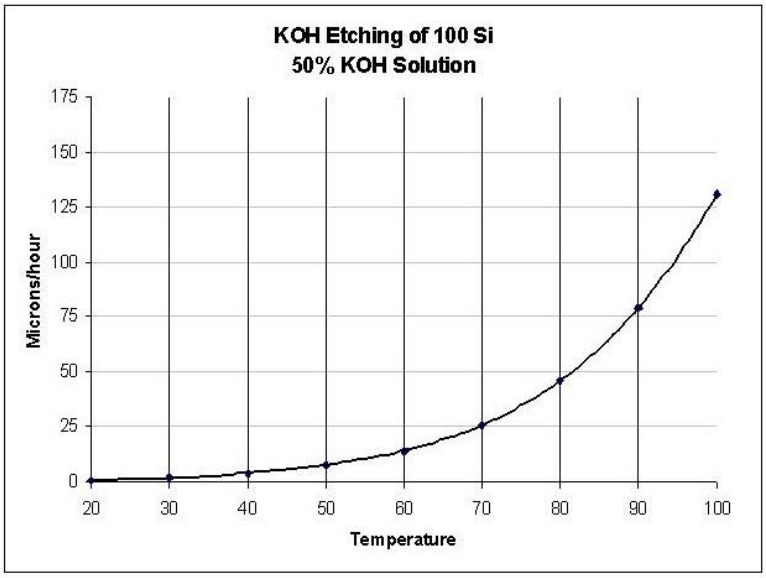


Figure 2.5. Etch rate of 50% KOH in weight for (100) plane of Si [17]

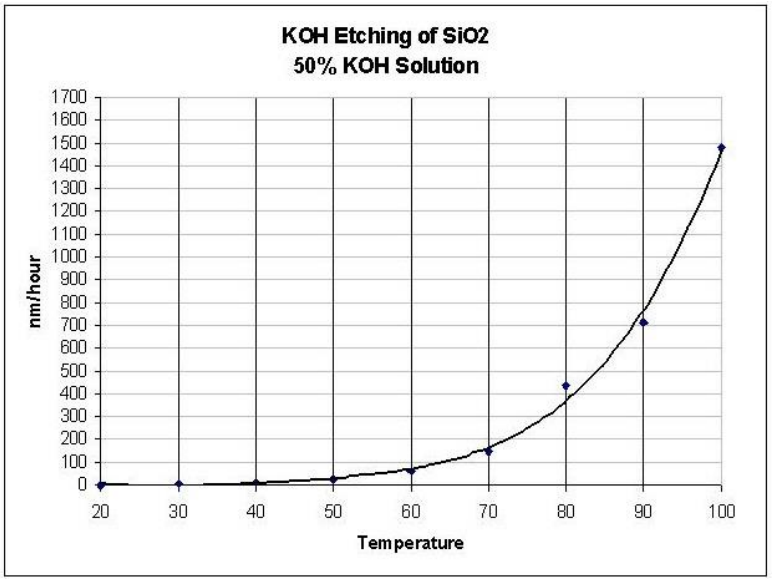


Figure 2.6. Etch rate of 50 % KOH in weight for SiO2 [17]

2.1.3.2. TMAH Etching

TMAH stands for tetramethylammonium hydroxide and similar to KOH it is also an anisotropic etchant. It is commercially available in various concentrations up to 25%. The etch rate of the chemical is strongly depended on both concentration and temperature. Roughness of the surface after TMAH etching depends on concentration as well and it decreases with increasing concentration. TMAH etching also results in V-shaped etched due to different etch rates of between (100) and (111) once again with an angle 54.7 ˚. In a longer time and large area etches it behaves like KOH. However, TMAH offers much better selectivity between SiO2 and Si. In the following Figure 2.7 and Figure 2.8 etch rates of 25% TMAH for Si and SiO_2 can be seen respectively [18].

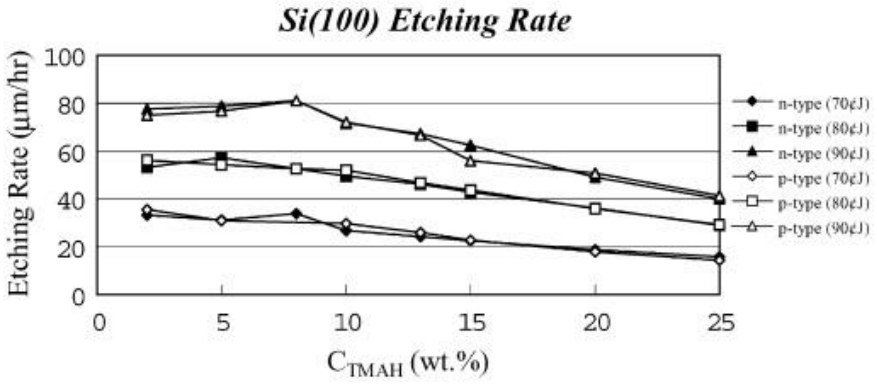


Figure 2.7. Etching rate of TMAH Si(100) for various concentrations and temperatures[19]

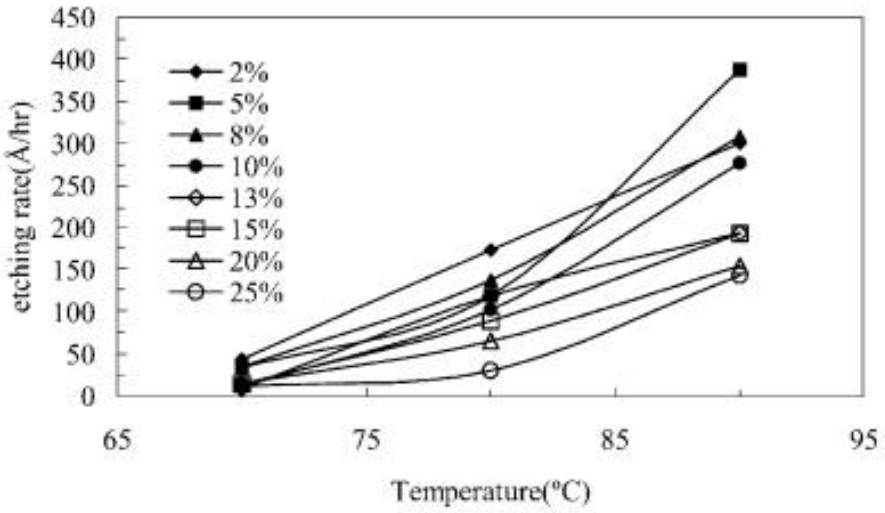


Figure 2.8. Etching rate of TMAH SiO2 for various concentrations and temperature [19]

2.1.4. Atmospheric Downstream Plasma Dry Chemical Etching (ADP-DCE)

Dry etching is a relatively new method for thinning. Ar/CF_4 plasma is used for the ADP-DCE process. Thinning rate for the ADP-DCE process is about 20 μm and rms roughness of the surface is around 0.3 nm. Although roughness value seems insignificant, needle-like hillocks in the silicon surface are observed in AFM measurements. Additionally to the ADP-DCE traditional dry etching process which uses fluorine or chlorine-containing plasmas also used for thinning [12].

2.2. Doping of Silicon

The doping of semiconductors can be summarized as introducing impurities to the semiconductor crystal structure to change the conductivity of the material. Doping semiconductor materials can be done during the production of the wafer or partially after the wafer is produced. Partial doping has a major role in producing microelectronic devices such as MOSFETs. Depending on the nature of introduced impurity there are two types of doping; n-type and p-type. Partially doping is done by using the two methods below:

- Diffusion
- Ion Implantation[20]

2.2.1. Diffusion

Diffusion is simply moving of particles from high concentration to low concentration by random motion. The transport of these particles occurs gradually in the medium. In semiconductor, medium impurity has to move in the crystal lattice of the medium. Three different ways for an impurity to diffuse through a crystal lattice are as follows:

- Empty space diffusion: As name suggests dopants move into empty space crystal defects. These empty spaces occur even in perfect crystals; therefore, diffusion also occurs.
- Inter lattice diffusion: An impurity moves between the bulk crystal atoms in the crystal.
- Changing places: Impurity atoms and lattice atoms change places.

In Figure 2.9 mechanics of above-mentioned diffusions are illustrated respectively.

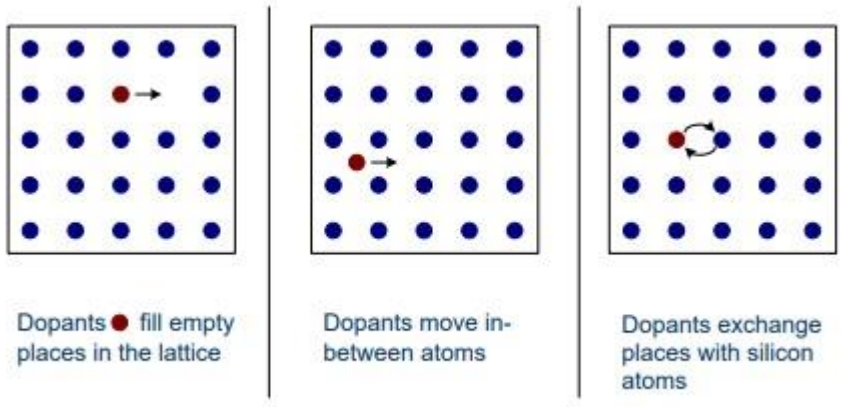


Figure 2.9. Illustration of diffusion processes [21]

In the dopant concentration point of view, there are two kinds of diffusion processes; diffusion with exhaustible source and diffusion with the inexhaustible

source. Inexhaustible source case limited amount of the source also limits the diffusion process. Since there is a limited amount of dopant on the surface longer diffusion time results in lower surface concentration. Therefore, deeper diffusion is possible into bulk substrate with low doping concentration. An inexhaustible source process dopant concentration on the surface always remains constant. As a result, impurities that penetrating through the semiconductor surface are freshened repeatedly.

2.2.1.1. Diffusion Methods

Diffusion for silicon occurs at high temperatures around 1200 ˚C. To achieve these high temperatures generally ovens with quartz tubes are used. According to doping material, there are three methods for diffusion.

Diffusion from the gas phase:

Doping materials in gaseous form such as phosphine (PH_3) or diborane (B_2H_6) are mixed with a carrier gas (generally argon or nitrogen) and are transmitted to stacked silicon wafers. In high-temperature concentration balance between silicon surfaces and gas mixture takes place.

Diffusion with solid source:

Solid dopant slices are placed between silicon wafers then when temperature increases in the quartz tube dopants slices release the impurities in gaseous form. A carrier gas helps these impurities to reach silicon surfaces and concentration balance occurs between the surface and the gaseous medium.

Diffusion with liquid source:

The liquid source method presents two ways of doping the silicon wafers. In the gas source and solid source, a quartz oven should be used exclusively. On the other hand, in liquid source method dopant materials can be spin-coated on the wafer and rapid thermal annealing can be done for the diffusion activation. Since partial doping is necessary to produce devices like MOSFETs a mask of SiO_2 is used. Boron bromide

(BBr_3) and phosphoryl chloride ($POCl_3$) cannot penetrate through the oxide layer; therefore, undesired areas are not doped [21].

2.2.2. Ion Implantation

Ion implantation offers a highly controllable doping method by accelerating charged doping ions onto silicon wafer. Depth of the penetration can be set very precisely by changing the voltage which is needed to accelerate charged ions. Ion implantation takes place at room temperature, therefore, penetrated charged ions cannot diffuse back. Partial doping can be done by masking undesired parts by photoresist.

An ion implanter generally consists of following parts:

- Ion source: Dopant sources in gaseous form ionized in this part, for example, boron trifluoride BF_3
- Accelerator: Ions from the ions source are forced to accelerate under approximately 30 kilo electrons volts.
- Mass separator: This part separates ions by weight using deflectors. Ions out of the range of weight are deflected more or less than desired ions.
- Acceleration lane: Charged ions reach enough velocity to penetrate silicon wafer with the help of several 100keV accelerators.
- Lenses: Lenses focuses the ion beam and provides better control.
- Distraction: Electric fields diffract the ions to irradiate parts that should be doped.
- Wafer station: Large rotating holders to receive ion beam.

In Figure 2.10 illustration of an ion implanter is given.

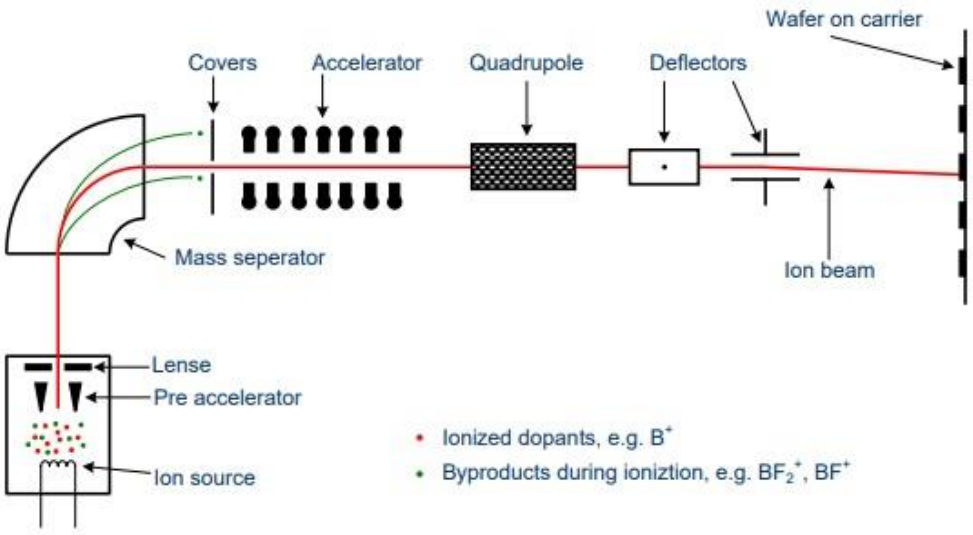


Figure 2.10. Illustration of an ion implanter [21]

Mechanics of ion implantation is very different from diffusion. In diffusion impurities move naturally from high concentration to lower concentration with high temperature; whereas, in ion implantation, high-speed doping ions penetrate by force into silicon lattice. Therefore, doping ions replace the silicon in the crystal lattice. However, ions do not bond with silicon atoms in the lattice right away and as a result, they do not create electron and holes which are the main causes for improved conductivity. Moreover, forced penetration of ions results in crystal damages in the lattice structure. To complete the doping process, samples should be heated to high temperatures. Although 500 ˚C ambient temperature is enough to mend crystal damage, the silicon wafer is heated up to 1000 ˚C to achieve better doping.

Channeling is also a major problem for ion implantation. Because of the highly ordered crystal structure, there are channels where charged ions do not encounter any silicon atoms for a great distance. Deeper penetration can be possible in this situation. There are two ways to prevent channeling which are wafer alignment and scattering. Both of the solutions for channeling have the same principle which is to change the direction of the charged ions so that they encounter silicon atoms [21]. In Figure 2.11 an illustration for channeling preventing methods is given.

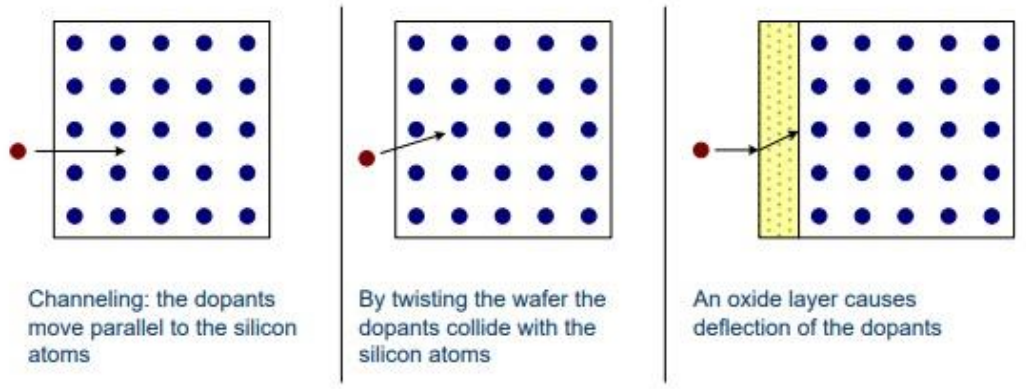


Figure 2.11. Channeling effect for ion implantation [21]

2.3. Producing TFTs with Silicon on Insulator Wafers

Silicon on insulator wafers (SOI) is a kind of wafer that has a thin single crystalline top layer, buried amorphous (generally SiO_2) insulator middle layer and thick single-crystalline Si layer at the bottom. There have been several reasons to use SOI wafers; however, many of the reasons can be summarized as the need for faster devices. Since SOI MOSFETs have an insulating SiO_2 layer between the doped source and drain regions and bulk Si layer, parasitic capacitances between terminals are significantly lower than traditional MOSFET structures. Lower parasitic capacitances result in faster circuits. Similarly, as MOSFET structures get smaller traditional bulk Si MOSFETs do not perform as well as SOI MOSFETs. There are two major methods for producing SOI wafers which are wafer bonding and SIMOX processes. In wafer bonding, two Si wafers are bonded with high temperature and forming a SiO_2 layer between interface. Bond between Si and O atoms results very reliable strong structure. After bonding back etching and polishing of one wafer results SOI structure. On the other hand, SIMOX can be explained as ion implantation of high dose oxygen. As explained in the ion implantation part some annealing steps are necessary for reliable SOI structures. However, unlike doping oxygen atoms should not diffuse through the Si bulk structure [22].

In the following parts, SOI wafers are used for their very thin single crystal silicon layer. The ultimate goal for this work is to build single-crystal silicon thin-film transistors. Therefore, getting thin-film silicon is the fundamental step. As it is mentioned SOI's single crystal silicon layer is on top of the SiO_2 layer. In this structure producing a suspended single crystal layer is relatively easier than back etching bulk Si wafer. E. Menard et al. in their work followed a similar approach [23]. They used an SOI wafer which has 340nm thick single crystal silicon layer. After cleaning the native oxide on the SOI wafer by diluted HF(1%) solution, samples are coated with Al(20nm: 0.1nm/s) and Au(100nm: 1nm/s). To pattern sample surface into desired shape photolithography and appropriate etching for coated metals is used. Ribbon shaped silicon layers are preferred for shorter process time. Long (15mm) and narrow (5μm) ribbon-shaped silicon layers are easy to retrieve from the suspended structure and does not require long time chemical processes. After shaping, anisotropic etching with TMAH is used to reach the SiO_2 layer. Coated metal layers act as masks for TMAH etching in this step. Au and Al layer can be removed or used as electrons after the anisotropic etching step. Created silicon strips are strongly attached to the SiO2 layer. Highly concentrated HF(49%) is used to remove the oxide layer completely and formed suspended ribbon structures. Even though, desired thin film layers are fabricated to build TFTs these ribbons have to be transferred into a plastic substrate. For this purpose dry transfer printing method is used. Firstly with the help of flat-surfaced polydimethylsiloxane (PDMS) strips are removed from the SOI surface. Researchers are using indium tin oxide (ITO, 100-nm thick) coated mylar sheets as plastic substrates. Photoresist (SU8-5; Microchem Corp.) is both used for transferring ribbons from PDMS to mylar sheet and as dielectric materials for produced structures. Coated Al and Au are not removed from strips; therefore they are used as drain and source [23]. Scheme for process is given in detail in Figure 2.12. Microscopic images for resulted ribbons are also given in Figure 2.13.

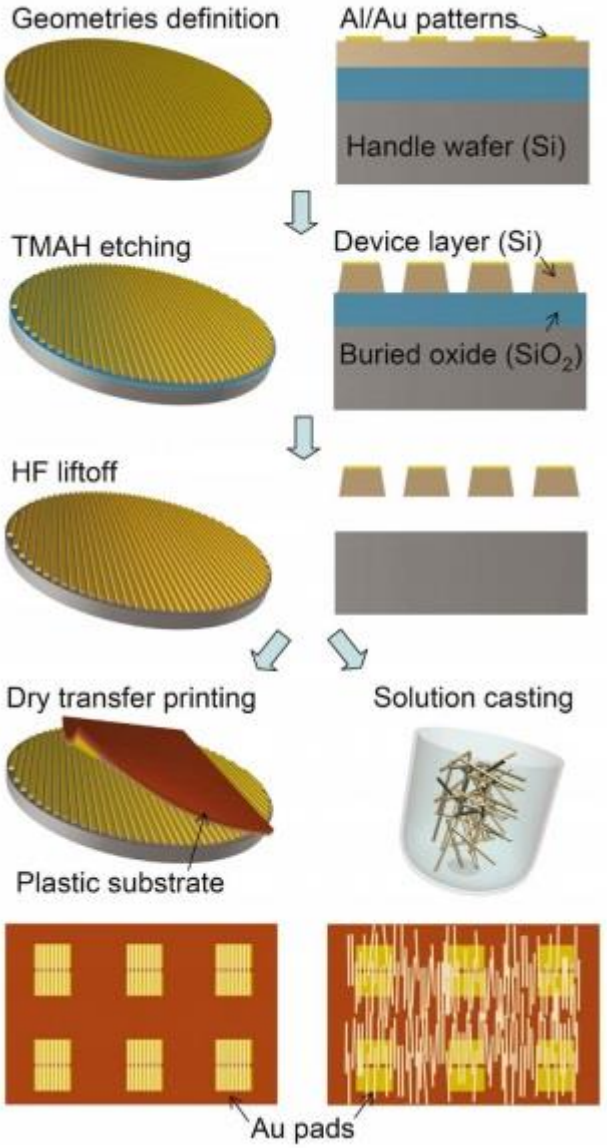
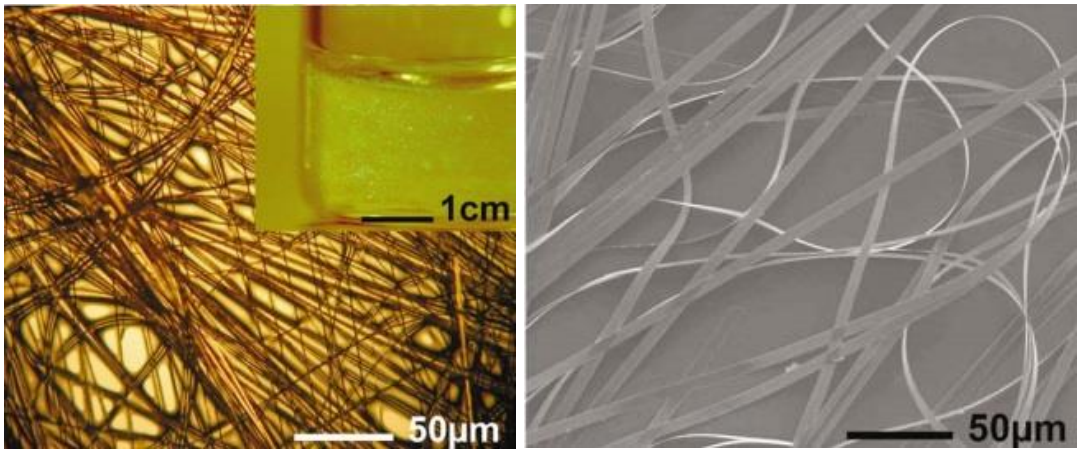


Figure 2.12. Step by step illustration of TFT production [23]



a) b)

Figure 2.13. a) Optical microscope picture of solution cast tangled strips b) Silicon micro strips showing flexibility (thickness 340 nm; widths 5 µm; lengths 15 mm) [23]

On/off ratio of the resulting devices are around 10^3. Analysis also shows that (Figure 17) linear regime mobility (μ_{FE}) is 180cm^2/V measured using a parallel plate capacitance model. Capacitance of the dielectric measured from the capacitor test structure formed near the circuit is 2.85nF/cm^2.

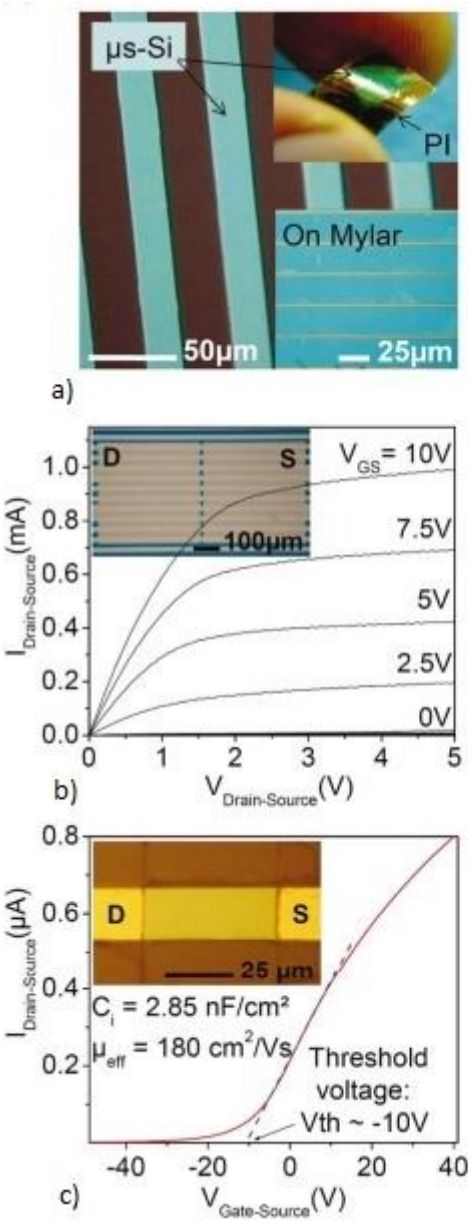


Figure 2.14. a) A top view of resulted TFT structure on PDMS coated kapton sheet. b) Drain to source current (IDS) drain to source voltage (VDS) characteristics for TFTs made with silicon strips. c) Drain to source current (IDS) gate to source voltage characteristics for TFTs made with silicon strips [23]

The same group of researchers developed their TFTs later the same year by using spin-on dopants on their design. Since the research is done by the same group process steps are the same except the spin-on dopant (SOD) and spin-on-glass part (SOG). As it is mentioned before plastic substrates cannot withstand temperatures

higher than 150 ˚C. In the previous work, the nearly same group of researchers used previously doped SOI wafers. However, results show that the doping level is not in the desired region and also they cannot perform partial doping. In this time the same group first coats the SOI (100 nm silicon layer 200nm buried oxide layer) wafer with SOG and anneals in RTA at 700 ˚C for 4 minutes. Performing photolithography (with Shipley 1805 photoresist) a mask is created with desired open windows. To remove SOG layer buffered oxide etchant (BOE) is used for the 50s. SOG layer will act as an oxide layer and will block undesired doping. SOD material is coated after the BOE step and it is cured at 950 ˚C in RTA for 5s. Both SOD and SOG layers are removed with BOE solution again for the 90s. The remaining steps are the same in the previous work of the same researchers. In Figure 2.15 illustration of TFT production using SOD is shown. Resulting structures is shown in Figure 2.16 [24].

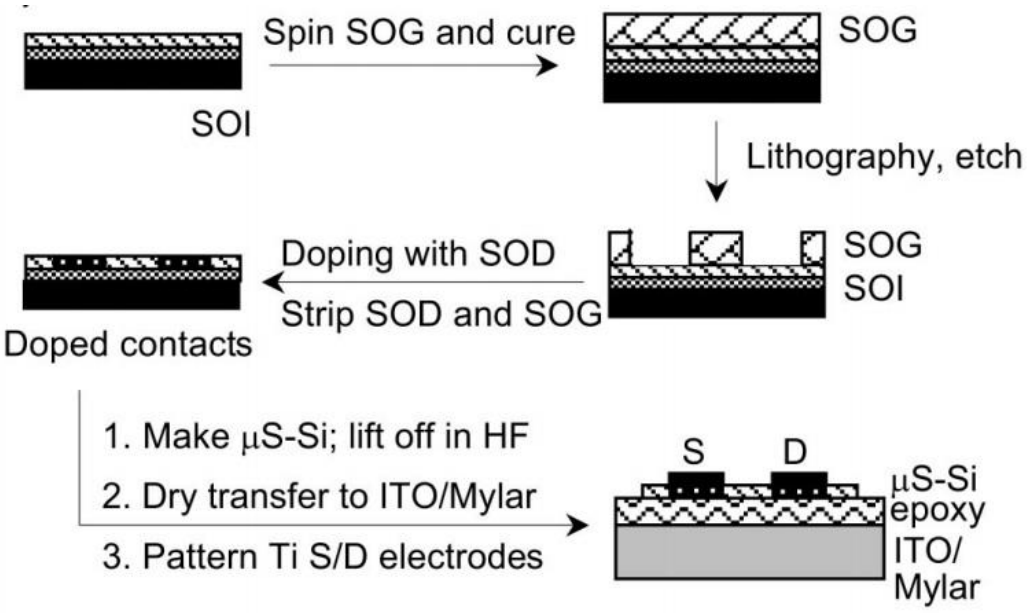


Figure 2.15. Illustration of TFT structures using spin on glass and spin on dopants [24].

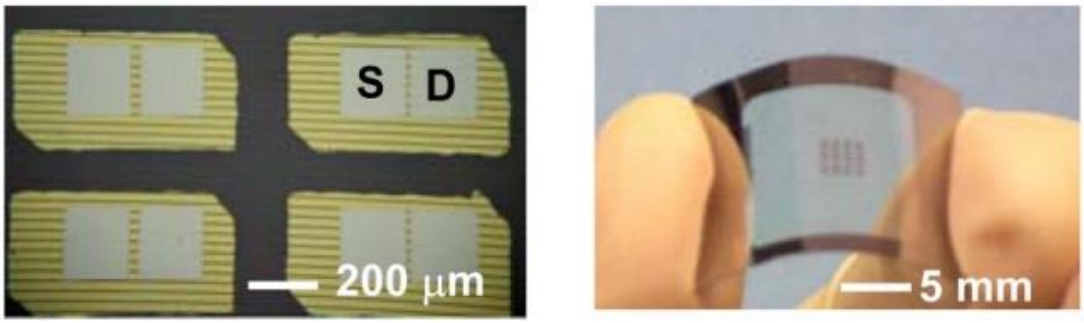


Figure 2.16. Images for produced flexible TFT structures [24]

On/off ratio of the resulting product is improved to 10^4 and similarly, linear regime mobility determined by application of standard field-effect transistor models is improved to 240 cm^2/V [24]. Other improvements on the TFT characteristics can be seen in Figure 2.17

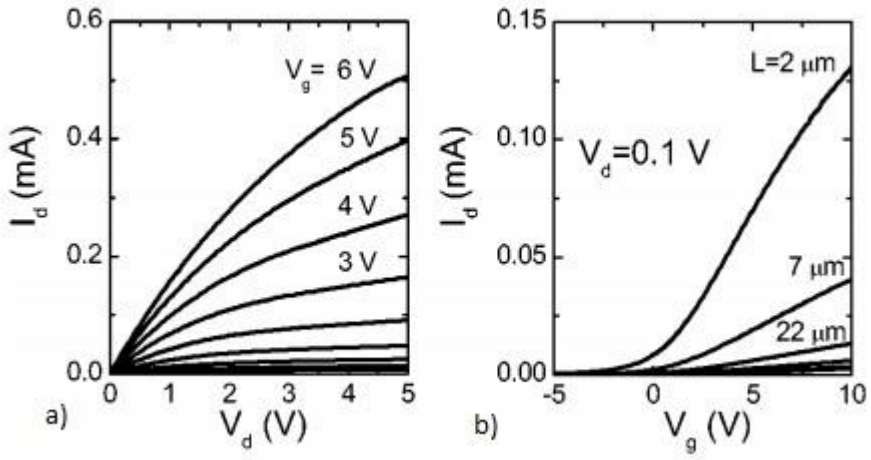
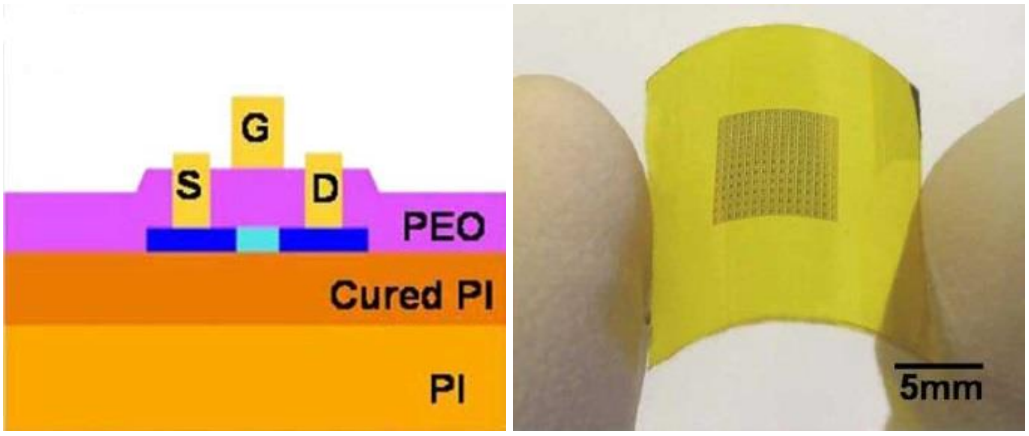


Figure 2.17. a) Drain to source current (IDS) drain to source voltage (VDS) characteristics for TFTs made with SOG and SOD. b) Drain to source current (IDS) gate to source voltage characteristics for different gate lengths of TFTs made with SOG and SOD [24]

To improve their research nearly the same group of researchers again published a paper. In this work, researchers tried to reach optimum results by using better methods along production. Production of the TFTs starts with depositing the SiO_2 layer on SOI (Soitec unibond with a 290-nm top Si Layer) wafer by chemical vapor deposition. The lithography step is used to form a SiO_2 mask with BOE etching.

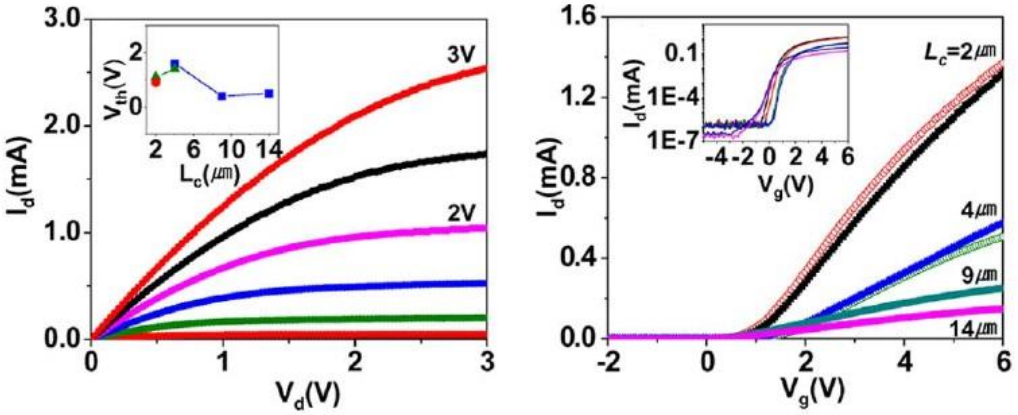
Unlike previous work, solid source doping is used to achieve higher doping concentration. The same techniques from these chapters are used and silicon ribbons are transferred into PI(polyimide) sheets spin-coated with a thin layer of PI. (1 μm) Dielectric layer is also SiO_2 coated with plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and N_2O at 250 ˚C. Finally, Cr (5nm) and Au (100nm) are coated as source and drain contacts. As it can be understood from device production researcher used top to bottom approach this time [5]. Figure 2.18 shows the schematic and final structure of the TFTs.



a) b)

Figure 2.18. a) Schematic of produced TFTs b) Image of flexible produced TFTs [5]

The resulting structures have an on/off ratio higher than 10^5 and they have intrinsic mobility of 510 cm^2/V. It can be said that the performance parameters of TFTs are significantly improved. However, if the process method is closely examined it can be seen that every method used in this work is better than previous ones. For example, instead of using SOD and SOG, solid source doping and CVD deposited SiO_2 is used. Later methods have significant superiority on previous ones. In previous works, temperature and time concerns may lead researchers to use inferior methods. On the other hand in this research, they tailored materials and processes for better TFT design. Figure 2.19 characteristics of these better TFTs are given [5].



a) b)

Figure 2.19. a) Drain to source current (IDS) drain to source voltage (VDS) characteristics for TFTs with LC (Channel length)= 9 μm, LO (Lo; defined by the distance that the gate electrode extendsover the doped source/drain regions) = 5.5 μm, and W = 200 μm. Inset shows the threshold voltage as a function of channel length for the devices. b) Drain to source current (IDS) gate to source voltage characteristics for different gate lengths of TFTs with different LC and LO values. inset shows a logarithm plot of b) transfer curves [5]

There is another research group that tried to further the research on silicon thin-film transistors with SOI wafers. Their process flow is relatively similar; however, they made some crucial changes in the flow concerning time and performance problems. Process generally starts with doping of the SOI wafers top Si layer. Unlike previous examples, researchers have tried ion implantation for doping Si layer. As it is mentioned in previous pages, ion implantation is very directional and has to be annealed after the implanting process. To achieve high doping and low sheet resistivity for TFT, ion implantation should be focused on either top of the Si layer or bottom of the Si layer. The reason for this positioning is they introduced a new transfer method for TFT which is called flipped transfer. It will be mentioned in the following parts of this chapter. After performing ion implantation on the samples, the objective of this researches is to reach buried oxide and completely remove it. In any of the published works, their method is not explained elaborately. However, they refer to the work of previously mentioned researchers. In the dry transfer printing method, instead of using PDMS as a transporter for Si nano-membranes (NM), polyethylene terephthalate (PET) substrate is directly used to remove Si NMs with the help of SU-8 photoresist.

Since the top to bottom approached is acknowledged for TFTs another dielectric layer should be coated on top of Si NMs to form a gate structure. SiO_2 coated with e-beam deposition is chosen for both dielectric constant and temperature concerns. Finally, Ti/Au is coated for gate, drain and source contacts. The final structure of the TFTs is also different from previous examples. It is called a double-gated structure and can be seen in Figure 2.20 [25 –27].

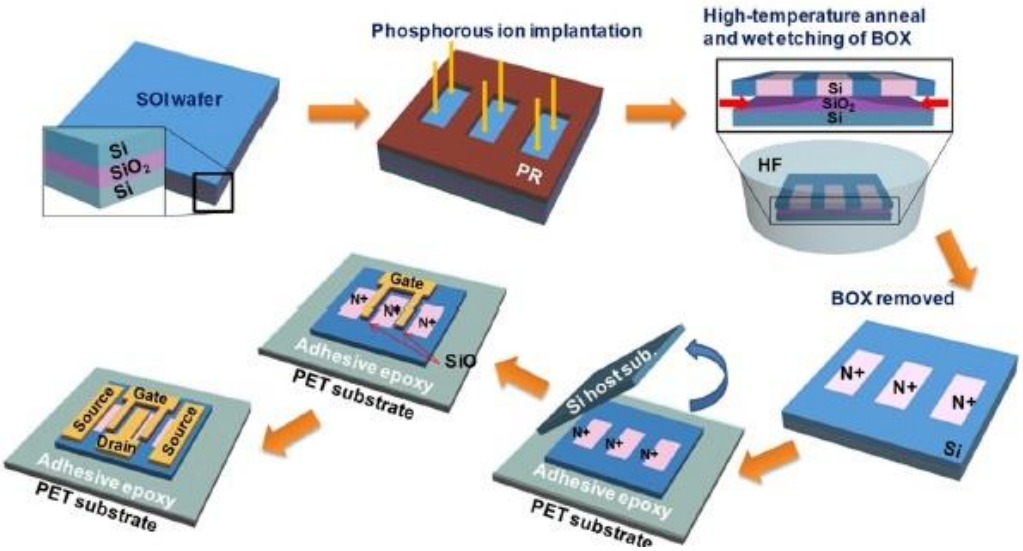
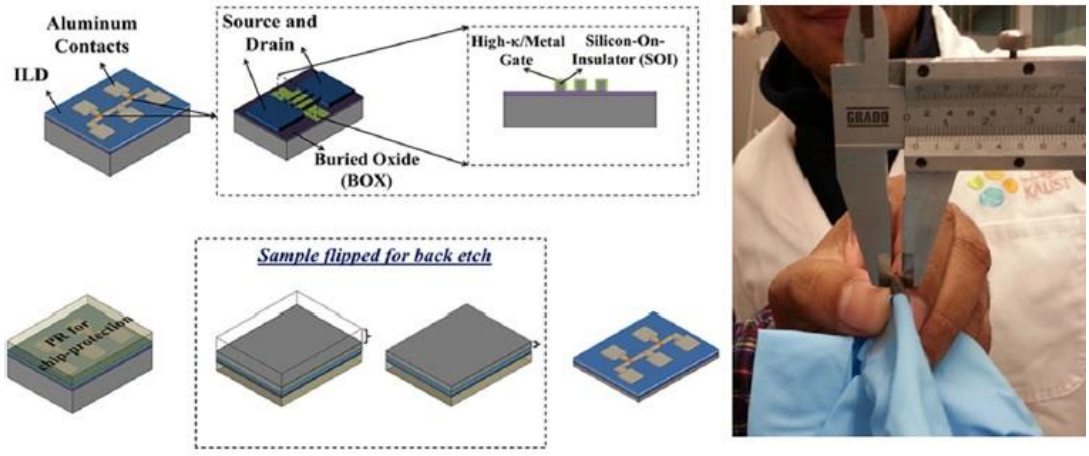


Figure 2.20. Process flow for Ion implanted flipped dry transferred TFT structures [26]

Working frequency of TFTs is the major concern for these researchers. Therefore, there is not much information about their current-voltage characteristics compare with previous researches.

Finally, to produce a bendable transistor, FinFet is produced with an SOI wafer. However, the production approach is completely different than other examples. FinFet is completely another structure of transistor therefore in this paragraph main focus will be thinning method and hypothetical adaptation for MOSFET structure. In the published work, researchers processed Fin Fet structure on top of the SOI wafer. Process steps for FinFET have similar steps to MOSFET. Firstly, fins are patterned down (sub-20 nm width) by using deep ultraviolet lithography (DUV) followed by extreme resist trimming then gate stacks are formed with 10–20 nm TiN/2–4 nm HfO_2.

(250nm - 1µm gate lengths) Ion implantation is applied to partially dope source and drain region and to activate doping 1000 ˚C for 10s. As the last step before thinning forming gas anneal (FGA) is performed at 420 ˚C with H_2/N_2 gas mixture. Finally, the device layer is protected with coating photoresist and wafer is back etched with mechanical grinding. Researchers claim that 50 µm thick and 7.5 cm^2 surface area having samples are mechanically flexible enough to have a 0.5 mm bending radius [28]. In Figure 2.21 these process steps and flexibility of the final device can be found. Hypothetically a MOSFET can be built into a thick SOI wafer and similar results can be observed.



a) b)

Figure 2.21. a) Process flow for flexible 50µm thick FinFET structure. b) Optic image for final FinFET structure with bending radius of 0.5mm [28]

2.4. An Unorthodox Method for Si Wafer Thinning

Wearable technology is the latest trend in microelectronics technology. Many research groups are trying to produce a bendable single crystal silicon layer to improve the performances of existing wearable technologies. Producing a flexible thin single crystal silicon layer is a crucial part of flexible TFT production. For this purpose, a research group followed a different method other mentioned existing ones. In this method bulk, Si wafer is used and thinned as a plate rather than strips or ribbons. Many

of the previous thinned Si layers has nanometer-size thickness; however, in this research size can be adjustable and in the micrometer regime. The process starts with 400nm growing thermal oxide layer. Using photolithography trenches is a pattern on the SiO_2 surface. After reaching Si surface deep reactive ion etching (DRIE) helps to open up directional deep trenches. Deep trenches are coated with Al_2O_3 using atomic layer deposition to protect the trenches from isotropic etching. Isotropic etching with Xe_2F is applied to undermine the upper Si layer. Finally, the suspended Si layer can be removed from bulk. Reportedly, 5 μm thick single crystal silicon layers are achieved [29]. Similar to FinFET research hypothetically a MOSFET can be produced on a Si wafer and these thinning steps can be applied. In Figure 2.22 process flow is illustrated.

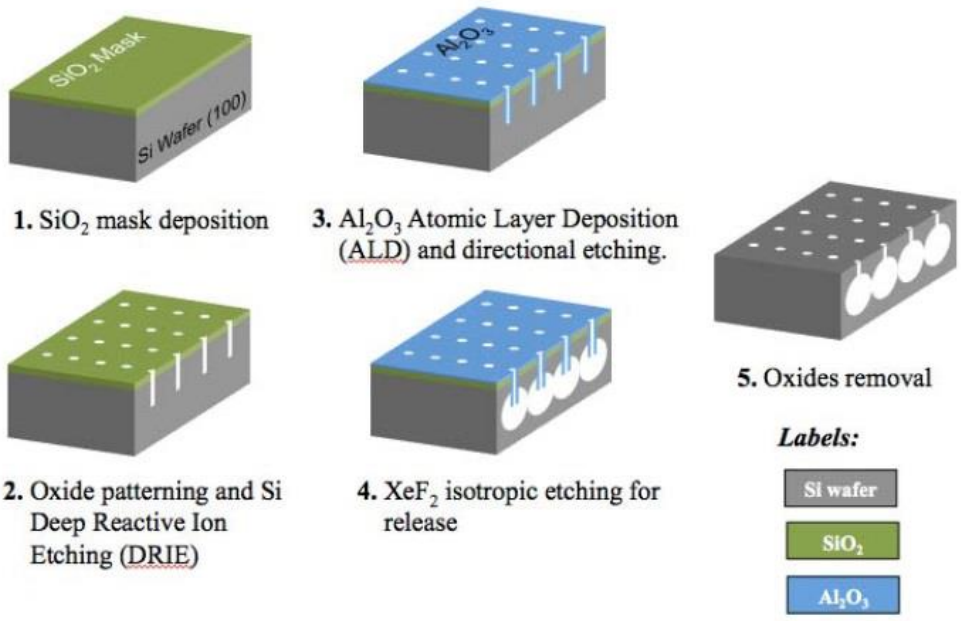


Figure 2.22. Process flow for producing thin silicon films [29]

CHAPTER 3

DESIGN OF SINGLE CRYSTAL THIN FILM TRANSISTORS

Designing the process steps for single crystal thin film silicon wafers should be done thoughtfully. Every step should be considered both individually and as a whole. Although each production step is done individually, they will build an electronic device at the end. Therefore, their contribution to the final product should be taken into consideration while designing each step. In this chapter, process design will be examined step by step and the reasoning behind that design will be explained in every step thoroughly.

3.1. Silicon Wafer Selection

Silicon wafer is the base material for all of the process steps. To make this selection the first type of final product should be decided. In this work, the final product is decided to be n-type MOSFET. The reason behind this decision is that NMOS transistors offer higher mobility and lower on-resistance. Therefore, faster devices can be achievable [30]. As crystal structure (100) Si surface MOSFETs is chosen. In the lattice structure of silicon while (100) and (110) planes are etched by KOH and TMAH (111) planes act as etch stopper [31].

3.2. SiN_x Growth on Si Wafer

In the KOH etching chapter, it is mentioned that selectivity of the KOH between SiO2 and Si is not pronounced. In the design both KOH and TMAH are used; however, to simplify the process, only one of them is chosen. By growing SiN_x on top of Si wafer, KOH etching has become a prime contender for thinning. As it is seen in the wet etching part KOH offers faster etching than TMAH and TMAH solution loses its effectiveness rapidly by time. As a result, it is decided that SiN_x should be grown

with a CVD oven. On the other hand, KOH etching of SiN_x is infinitesimal. As a resulting thickness of the SiN_x layer is not a major design parameter..

3.3. Thinning

CVD oven in the GUNAM grows a mixture of SiO_2 and SiN_x. SiO_2 can be etched isotopically using either hydrofluoric acid (HF) or buffered hydrofluoric acid (BHF). Photoresist can be used as a mask for this process [32]. After SiN_x and SiO_2 mixture is shaped by photolithography thinning is done by using a 50% KOH solution at 90 ˚C. In figure 8 etching rate of the solution can be deducted to be 80 µm/h. The thickness of the used silicon wafer is 500 µm. However, KOH etching is not a very thickness dependable etching method. As a result, little less than 3 hours of both side Si wafer etch will be sufficient for flexible thickness of Si wafer. Another issue for the thinned wafer is handling. Handling a thin flexible wafer for further processing is very hard. To prevent accidental loss of thinned wafer thinning is done with SiN_x masks. The design of the mask is given in Figure 3.1.

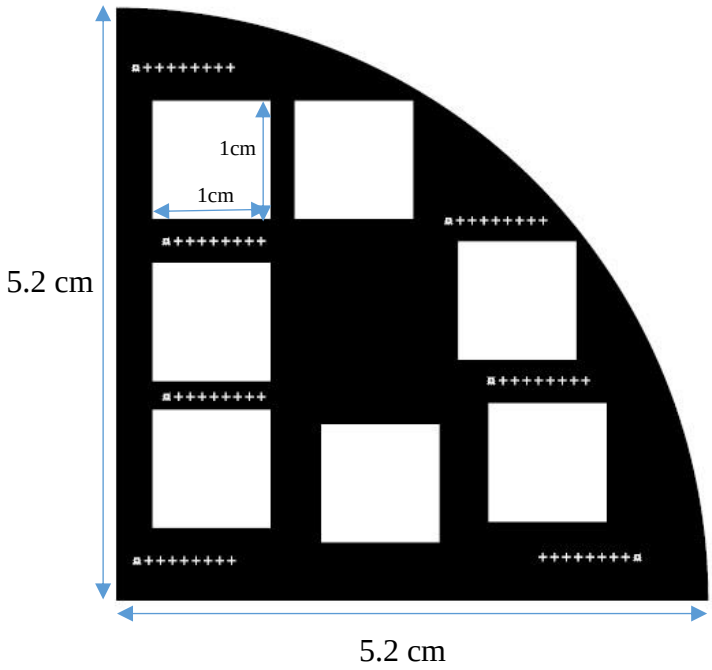
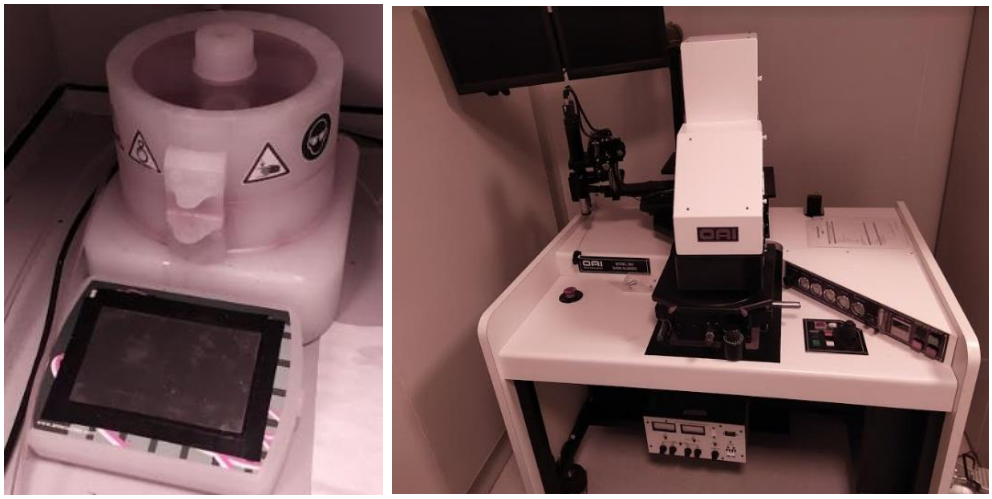


Figure 3.1. Designed mask for thinning. White parts are the opening that will be etched.



a) b)

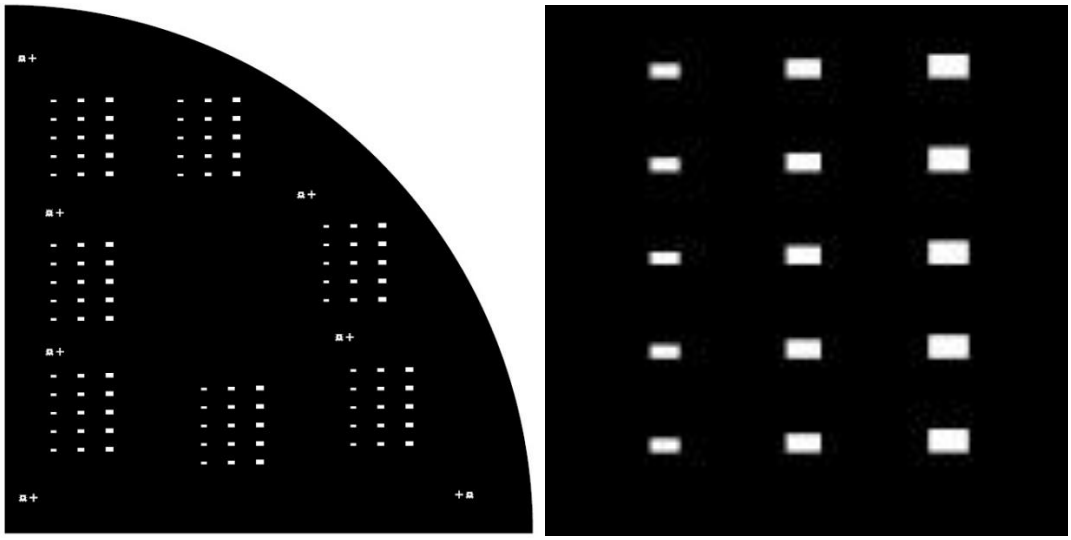
Figure 3.2. a) Picture of Polios spin coater at GUNAM b) Picture of mask aligner at GUNAM

Mask is designed for a quarter of the 4-inch wafer. The purpose of the black parts is to make easier to handle samples. Six existing white squares will be thinned and NMOS transistor will processed on them. Small crosses are designed for alignment of the future steps. To add more steps the number of crosses is more than the existing steps. In this way making changes or adding more process steps will be easier.

3.4. Doping of Source and Drain Terminals

In NMOS transistor source and drain, terminals should be doped with phosphorous(P); therefore they will be n-type doped. Concerning threshold voltage (V_T) transistors chosen to be produced depletion type which means V_T is chosen to be negative. The reason behind that is to achieve working devices even in low positive voltages. In depletion type NMOS transistors parts between source and drain is also doped. It is explained that a SiO_2 mask is required for partial doping of Si. Since SOG material is both easier to form with spin coater and faster to process instead of SiO_2, oxide-based SOG material is used. SOG material also is used by previous researchers. In this research, they spin-coated the material at different speeds. The speed of the spin coater designates the thickness of the SOG layer. After spin-coating 700 ˚C for 4

minutes of rapid thermal annealing(RTA) step hardens the material. To shape the SOG layer similar photolithography step is used. The designed mask for the doping process is given in Figure 3.3.



a) b)

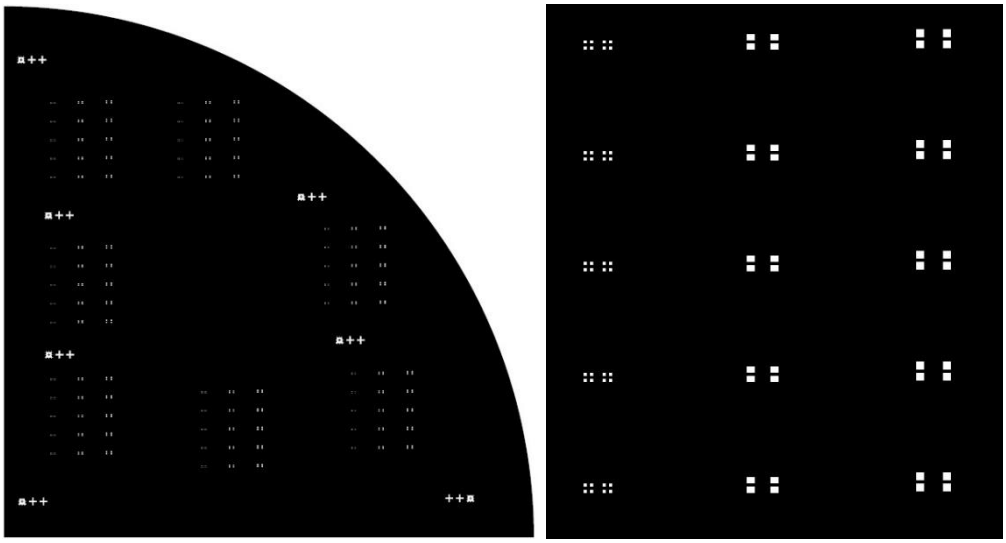
Figure 3.3. a) Designed quarter wafer sized doping mask b) Close up for a cell of the mask

Figure 3.4. Picture of RTA oven in GUNAM

Openings created for doping have various sizes which will result in NMOS transistors with various W/L ratios. After the photolithography step, the n-type SOD dopant will be spin-coated. To find optimum doping concentration for thinned Si layer a study based on previously published works on other researchers is done and 950 ˚C for 8 minutes is found as optimum doping level.

3.5. Forming Dielectric Layer

For a similar reason, in the doping process mask, SOG is used as dielectric material in NMOS transistors. SOG is spin-coated on top of partially doped silicon layer and annealed at 700 ˚C for 4 minutes in RTA. In this step to reach the source and drain terminals of NMOS transistors openings on the SOG layer should be constituted. Again photolithography process is carried on with a mask in Figure 3.5.



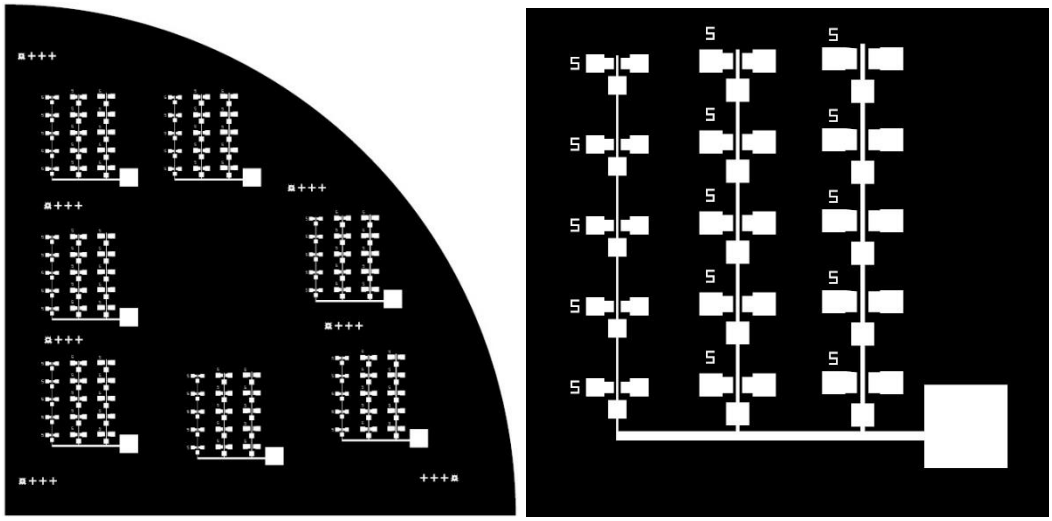
a) b)

Figure 3.5. a) Designed quarter wafer sized mask for source and drain ohmic contact. b) Close up for a cell of the mask

As many examples above after photolithography step BHF etching will be performed to the samples.

3.6. Metallization

In this work a new type of thinned NMOS transistor is attempted; therefore, working on metallization is not a primary concern. For heavily doped n-type silicon materials practical materials for ohmic contact are metals such as aluminum(Al), gold(Au) and platinum(Pt) [33]. Based on previous published researches Al/Au coating is preferred. Thicknesses for these materials are chosen to be 20 nm with 0.1nm/s rate for Al and 100nm with 1 nm/s for Au [23]. In the metallization step gate and connections between transistors will also be formed with these metals. To only coat the desired regions on the Si layer another photolithography step is necessitating the design of Figure 3.6.

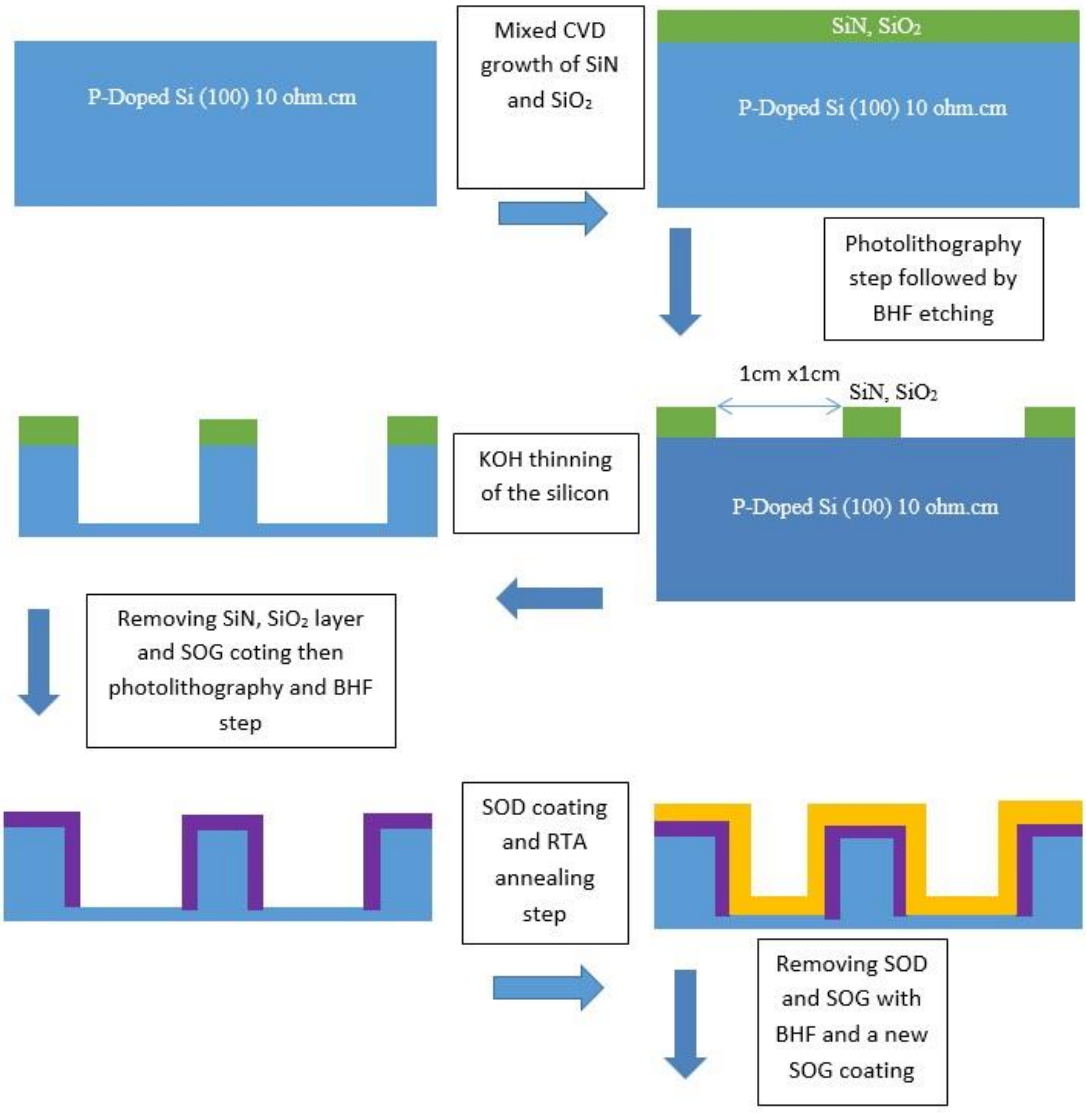


a) b)

Figure 3.6. a) Designed quarter wafer sized metallization mask b) Close up for a cell of the mask

In the mask, the final form of the transistors is shown. The letter S indicates that the terminal is used as a source. All of the gate terminals are connected and connected to a larger pad for more comfortable measurements. After lithography processes, samples are coated and lift-off undesired metal parts are removed. Finally, an annealing step is performed to better the ohmic contacts. Thinned NMOS transistors are transferred using kapton tape as the final step.

Figure 3.7. Picture of Nanovak thermal evaporation system in SPMG laboratory


P-Doped Si (100) 10 ohm.cm
Mixed CVD growth of SiN and SiO2
SiN, SiO2
P-Doped Si (100) 10 ohm.cm
Photolithography step followed by BHF etching
1cm x1cm
SiN, SiO2
P-Doped Si (100) 10 ohm.cm
KOH thinning of the silicon
Removing SiN, SiO2 layer and SOG coting then photolithography and BHF step
SOD coating and RTA annealing step
Removing SOD and SOG with BHF and a new SOG coating

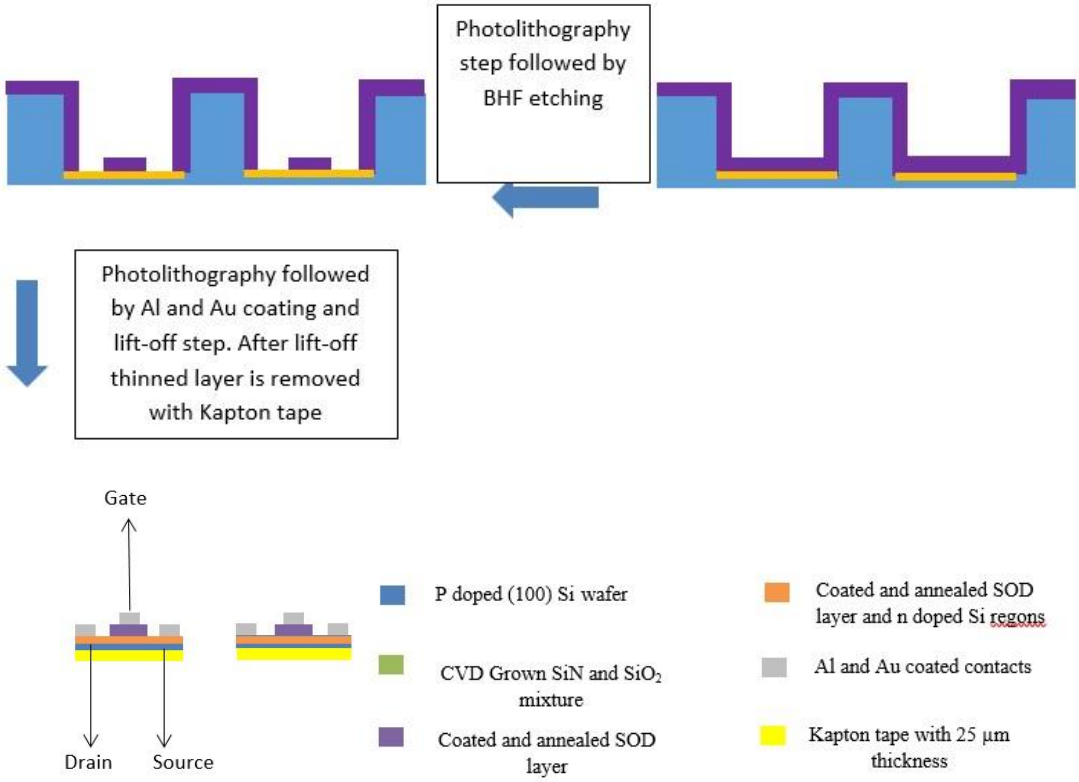


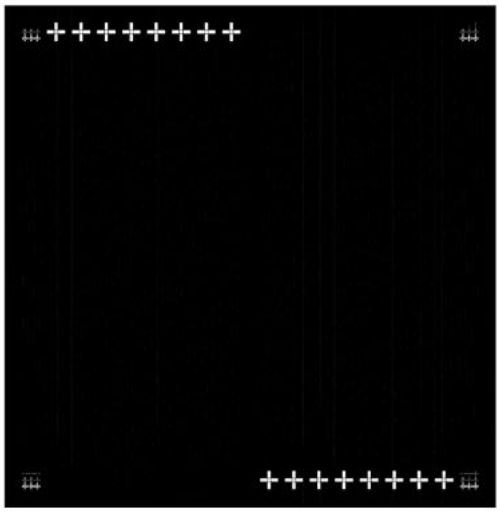
Figure 3.8. Illustration for designed production method

CHAPTER 4

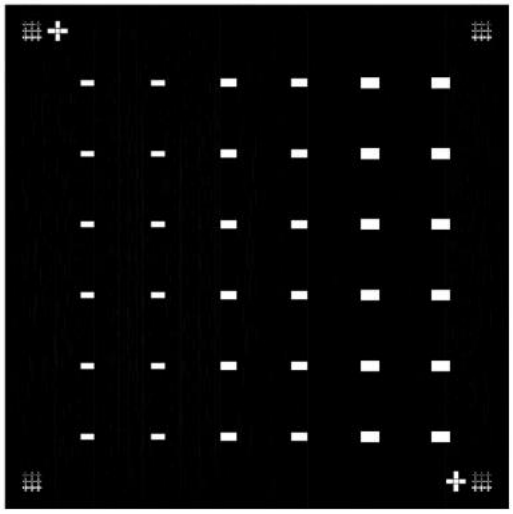
MICROFABRICATION OF SINGLE CRYSTAL SILICON THIN FILM TRANSISTORS

4.1. Producing Thick Substrate NMOS Transistors Using SOG and SOD in Low Temperature

Plastic substrates can withstand temperatures up to 150 ˚C. With this information, we decided to try to cure the SOD and SOG materials at this temperature and build a thick substrate depletion-mode NMOS transistors. If working transistors are achieved, flexible thin-film transistors can be directly built on top of thin single-crystal wafers with plastic substrate. Plastic substrates can help to handle wafer properly. To build NMOS transistors the same processes from the design part are applied using smaller photolithography masks. These masks can be seen in the following figures.

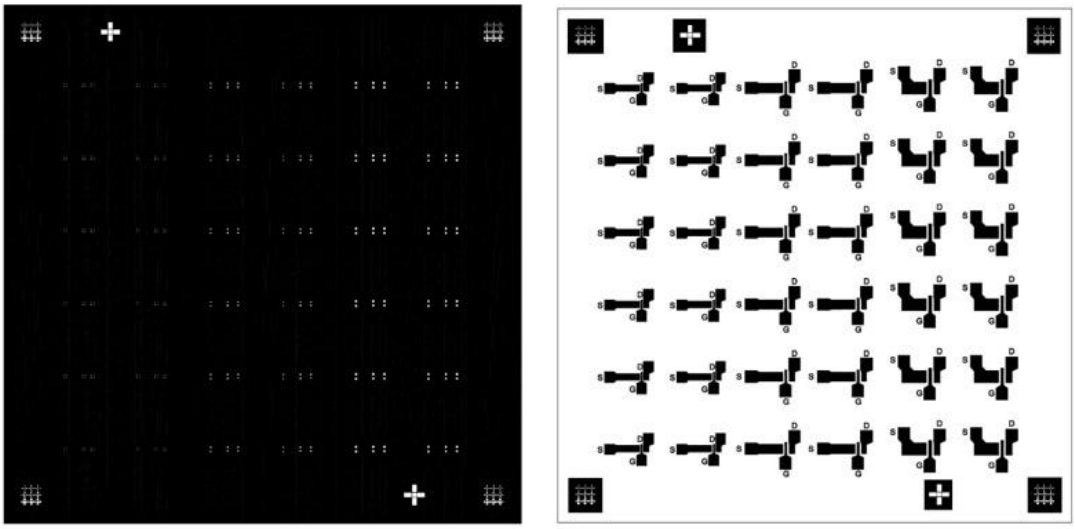


a)



b)

Figure 4.1. a) Mask for alignment marks. b) Mask for partial doping process which is for source and drain terminals.



a) b)

Figure 4.2. a) Mask for ohmic contacts of source and drain terminals. b) Final metallization mask for NMOS transistors

From Figure 4.2 b) it can be seen that metallization is done using a negative photoresist process. Also from the same figure, it can be deduced that there are three different sizes for the designed transistors. The channel lengths for these transistors are 50 µm, 75µm, and 100µm. The channel widths for these transistors are 250 µm, 350µm, and 500 µm. As the name of the chapter suggests SOD and SOG curing processes for these transistors are done in a vacuum oven at 150 ˚C instead of RTA oven. In the following Figure 4.3, final structure of the device with L=100µm is shown.

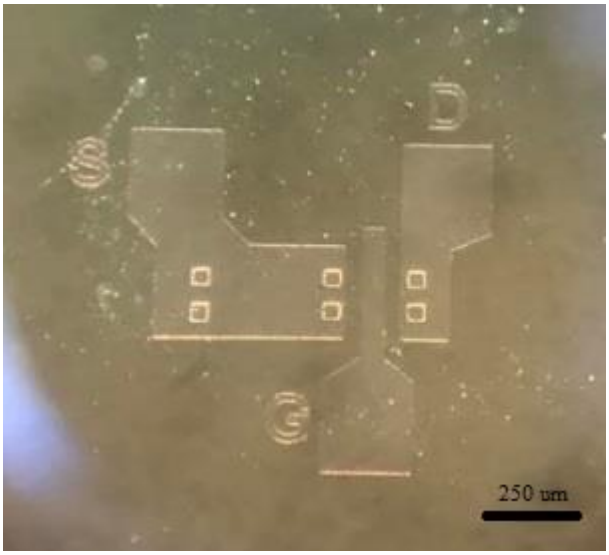


Figure 4.3. Microscope picture of the build NMOS transistor with L=100µm

Measurements of the NMOS transistors are done using Keithley 7612 and probes we build with the equipment in the lab. Since probes are not perfect results of the transistors are not constant. In Figure 4.4 IV graph for the NMOS transistor with L=100µm can be found.

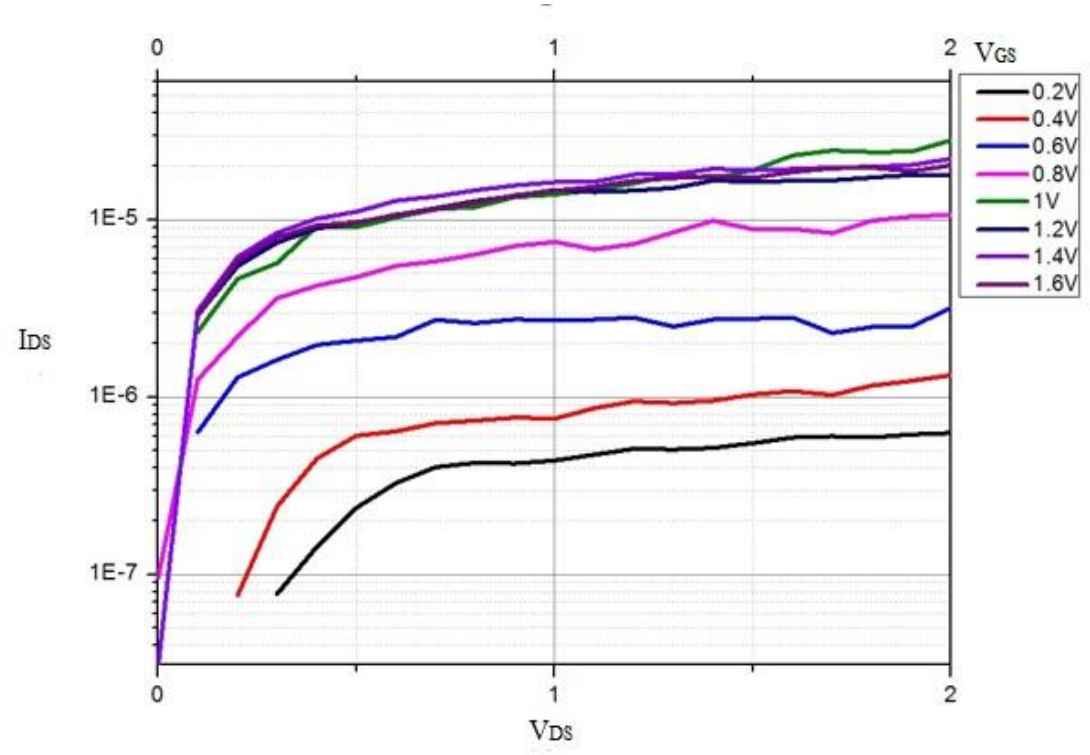


Figure 4.4. I_{DS} vs V_{DS} graph for different V_{GS} values for NMOS transistor with L=100µm

From the above graph, we can say that there is a transistor behavior. However, since the graph is so inconsistent we cannot calculate any transistor parameters from it. The other transistors are tried to be measured also; however, none of them showed any characteristics and during measurements, our probe set up is broken. Although samples show transistor behavior, failure in the higher voltages caused us to move on with higher temperatures for SOD and SOG materials.

4.2. Finding Optimal Doping Conditions for n-type SOD

Before building NMOS transistors, doping concentration, mobility and sheet resistance of the doped material should be optimized to form the best possible device. Three different published works are based on optimization. In one of the researches, p-type SOD is coated with spin coater at 9900 rpm for 15s then samples are annealed at 200 ˚C on hot plate. As annealing step researchers are used 800-950 ˚C for 2s-120s in argon (Ar) ambient. In the experiments (100) oriented 1-10 ohm.cm resistive

450µm thick p-type doped Si wafers are used [34]. For optimization instead of trying all of the annealing steps only 900 ˚C for 120s is tried. Since RTA in our laboratory has leakage in the chamber, the process carried out in the atmospheric conditions. In our experiments (100) oriented 1-10 ohm.cm resistive 500 µm thick p-type doped Si wafers are used. In our work n-type SOD is used for doping because our final device will be NMOS transistor. To measure sheet resistivity, mobility and doping concentration ezHEMS device from Nanomagnetics Instruments is used. To get better measurements corner of the square samples are coated with 5nm chromium and 100nm Au is coated. The results of our work are given in Figure 4.6.

Figure 4.5. Picture of ezHEMS device from Nanomagnetics Instruments

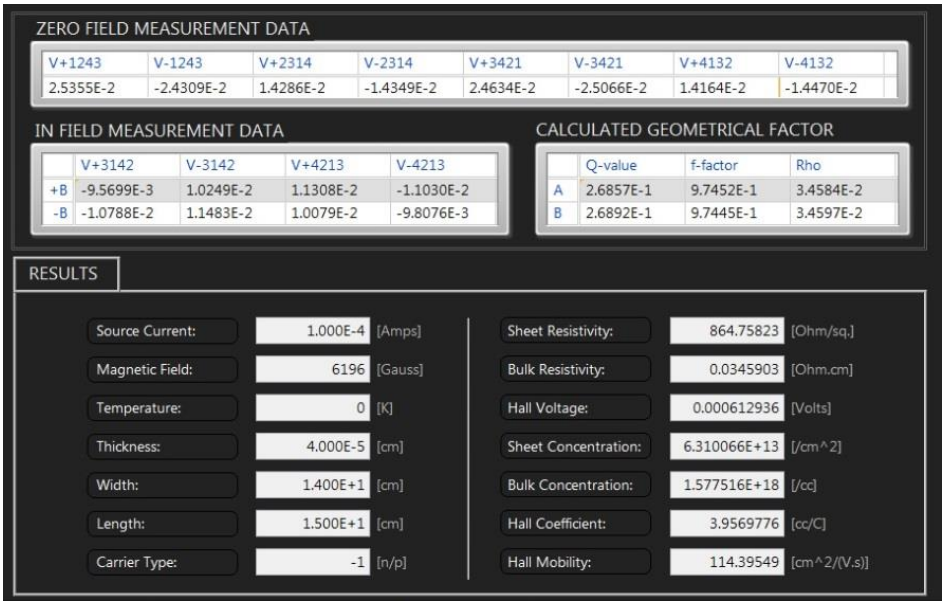


Figure 4.6. ezHEMS results of 9900 rpm spin coated 900 ˚C annealed for 120s with RTA

The size of the sample is 1.5cm * 1.5cm and measurements are taken for 400nm thickness. In the close look of the results, it can be seen that n-type doping is succeeded from carrier type being -1. When carrier type is 1 sample doping is p-type and for -1 it is n-type. Sheet resistivity is also measured with 4 point probe technique and found around 640 ohm/sq validating our closeness of the two values

In other research, samples are spin-coated 2000 rpm and time value is not mentioned. In RTA, samples are ramped to 950 ˚C, 1000 ˚C and 1050 ˚C for the 20s and annealed at these temperatures for 10s, 30s, and 60s and cooled downed to room temperature in 20s in Ar ambient. In this work, organic polymer-based SOD materials are used therefore different results from our experiments are expected. Only information about used Si wafers in the work is that they have (100) orientation [35]. In our experiments (100) p-type Si wafers are spin-coated with 2000 rpm speed for 60s. After spin-coating samples are directly placed into RTA for 30s for 950 ˚C. RTA is ramped to 950 ˚C in 20s and cooled down to as low temperature as possible in 60 s. After annealing samples are again coated with Cr and Au. In Figure 4.3 Ez-HEMS results are given.

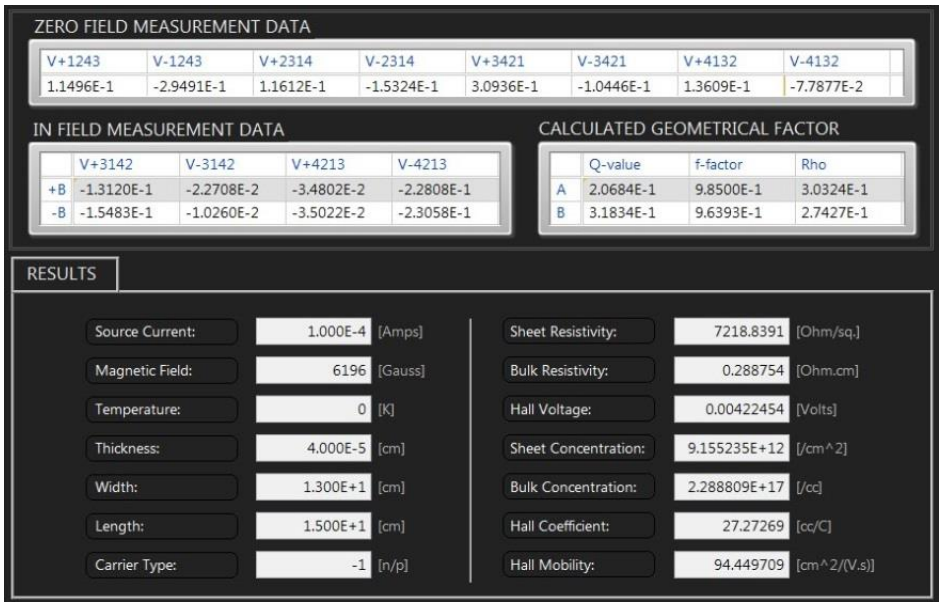


Figure 4.7. ezHEMS results of 2000 rpm spin coated and 950 ˚C annealed for 30s with ramping to 950 ˚C in 20s and cooled downed to room temperature in 60s with RTA

The size of the sample is 1.5cm x 1.5cm and measurements are taken for 400nm thickness. Again from the carrier type parameter, it can be seen that n-type doping is achieved. For this sample, seems results cannot be validated because sheet resistance is out of the range of 4 point probe device. However, the first experiment was better in sheet resistivity, mobility, and carrier concentration parameters.

In the last research, we based on our experiments, p-type (100) oriented 5-15 ohm.cm resistive 300 μm thick Si wafers are coated with n-type filmtronics SOD-P509 in the spin coater with 1000 rpm. After coating samples are annealed at an atomic furnace for 10, 15, 25 and 30 minutes [36]. In our experiment we used RTA oven instead of an atomic furnace and RTA oven in our laboratory cannot withstand more than 15 minutes in 950 ˚C. (100) oriented 1-10 ohm.cm resistive 500 μm thick Si wafer are coated with spin coater at speed of 1000 rpm for 60s. Then, samples are directly placed into the RTA oven for 10 and 15 minutes. Finally, corners of the samples are coated with Cr and Au and measured with ezHEMS device. In Figure 4.8 and Figure 4.9 results for these measurements can be seen.

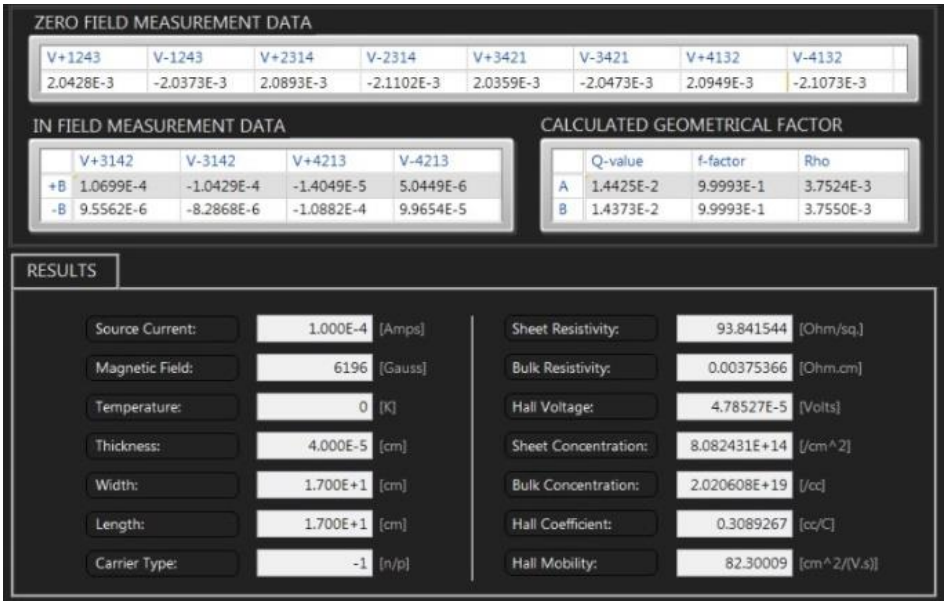


Figure 4.8. ezHEMS results of 1000 rpm spin coated 950 ˚C annealed for 10 minutes with RTA

Figure 4.9. ezHEMS results of 1000 rpm spin coated 950 ˚C annealed for 15 minutes with RTA

Sample sizes are 1.5cm x 1.5cm and measurements are taken for 400 nm thickness. From carrier type parameter it can be seen that n-type doping is successful. Both of the samples are measured with 4 point probe method to validate the results and Figure 4.8 sheet resistivity is found around 135 ohm/sq. and for Figure 4.9 sheet

resistivity is found around 450 ohm/sq. These results are very close to the ezHEMS results; therefore it can be said that measurements are trustworthy. Looking closely at the results Figure 4.6 offers better mobility; however, results in Figure 4.8 offers better sheet resistance and relatively close mobility values to Figure 4.6 results. In Table 4.1 all of the results are shown.

Table 4.1. Results of the experiment done by us following the steps of research materials

Spin Coating Speed (rpm)	RTA Temperature (°C)	Curing Time(minute)	Mobility ($cm^2/V.s$)	Sheet Resistance (ohm/sq.)
9900	900	2	114.4	864.8
2000	950	0.5	94.4	7218
1000	950	10	82.3	93.8
1000	950	15	108.6	349.2

To further the experiment results three samples are also added with both 1000 rpm and 2000 rpm spin coating and 4, 8 and 12 minutes of 950 ˚C RTA process. The results of these experiments are given below.

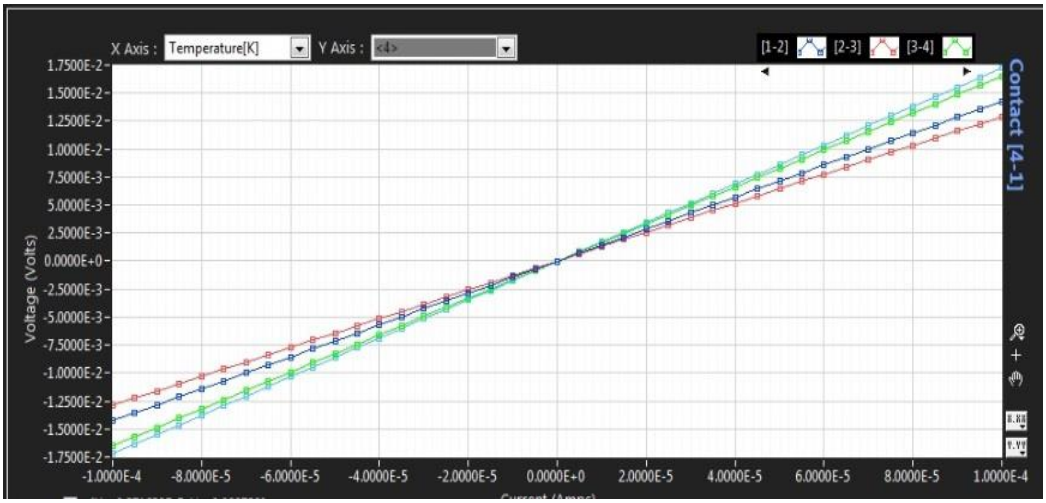
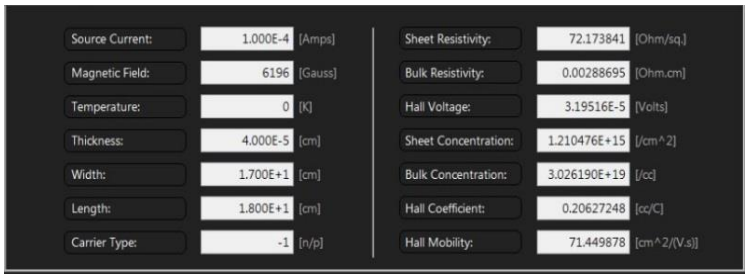
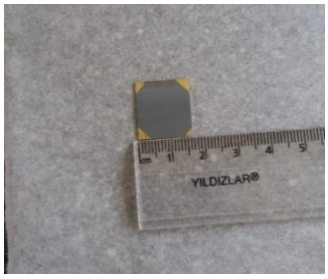


Figure 4.10. Voltage versus current graph for every contact of 1000 rpm spin coated 950 ˚C annealed for 4 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)





a) b)

Figure 4.11. a) ezHEMS results of 1000 rpm spin coated 950 ˚C annealed for 4 minutes with RTA b) Picture of the sample L= 17 mm W= 16mm thickness is assumed 400nm in the measurements.

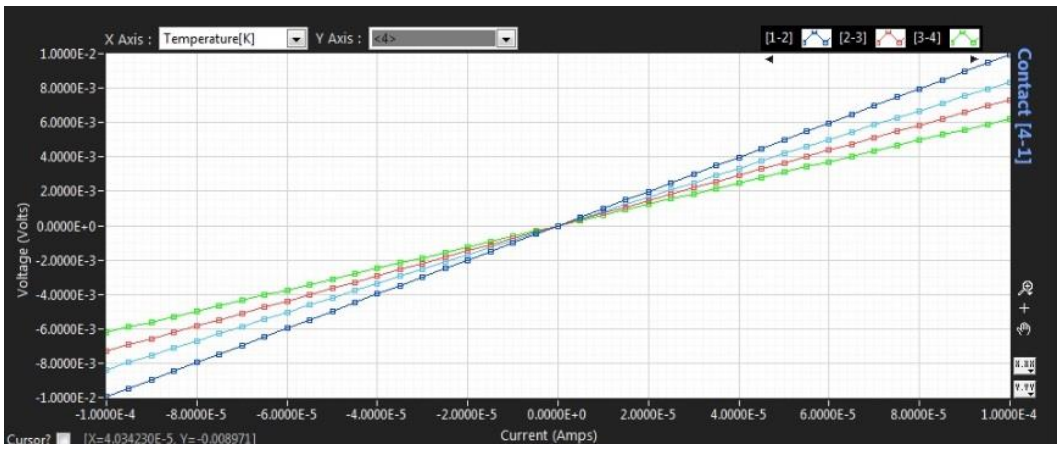
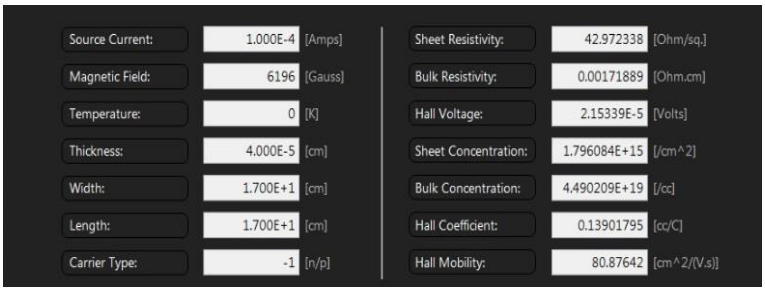
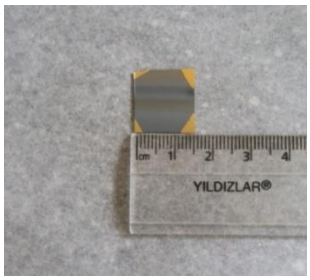


Figure 4.12. Voltage versus current graph for every contact of 1000 rpm spin coated 950 ˚C annealed for 8 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)





a) b)

Figure 4.13. a) ezHEMS results of 1000 rpm spin coated 950 ˚C annealed for 8 minutes with RTA b) Picture of the sample L= 16 mm W= 16mm thickness is assumed 400nm in the measurements

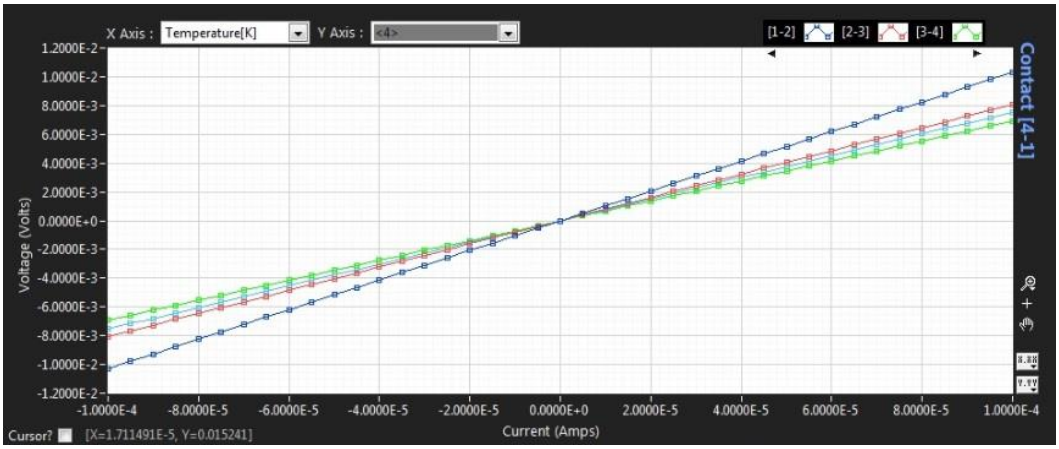
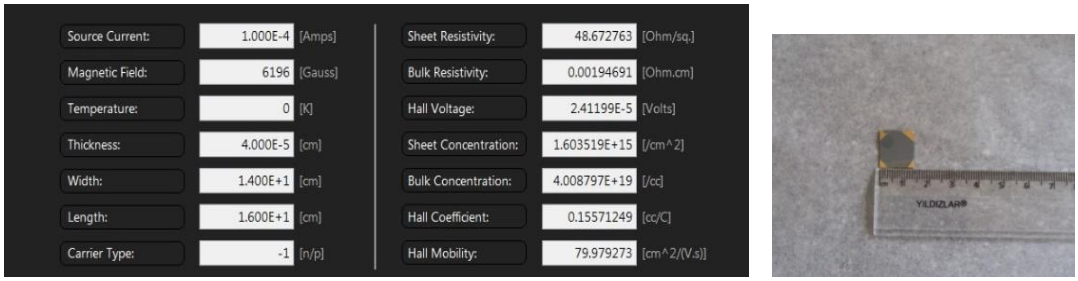


Figure 4.14. Voltage versus current graph for every contact of 1000 rpm spin coated 950 ˚C annealed for 12 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)



a) b)

Figure 4.15. a) ezHEMS results of 1000 rpm spin coated 950 ˚C annealed for 12 minutes with RTA b) Picture of the sample L= 15 mm W= 13mm thickness is assumed 400nm in the measurements

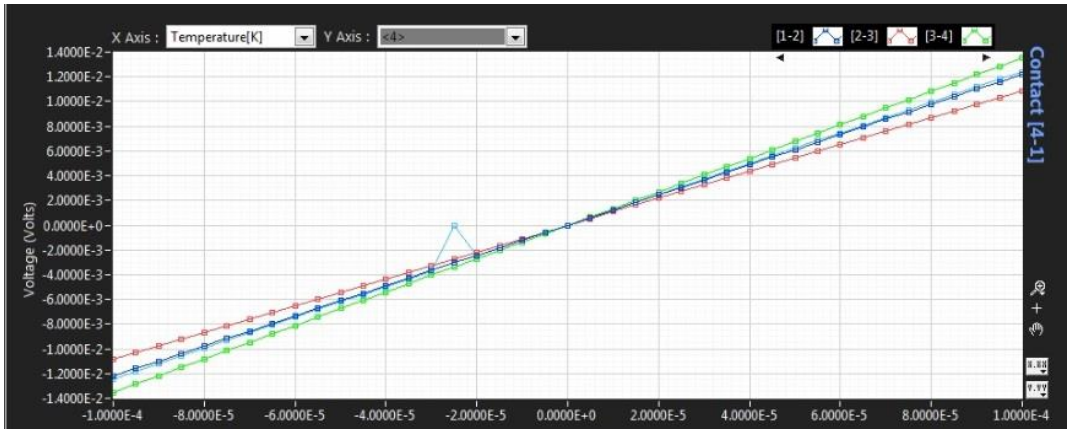
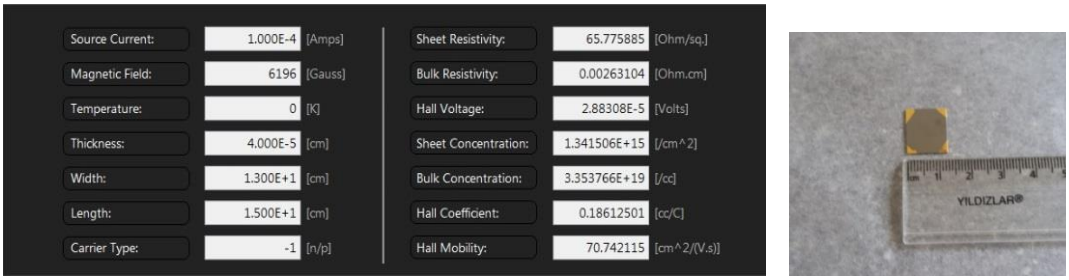


Figure 4.16. Voltage versus current graph for every contact of 2000 rpm spin coated 950 ˚C annealed for 4 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)



a) b)

Figure 4.17. a) ezHEMS results of 2000 rpm spin coated 950 ˚C annealed for 4 minutes with RTA b) Picture of the sample L= 16 mm W= 14mm thickness is assumed 400nm in the measurement

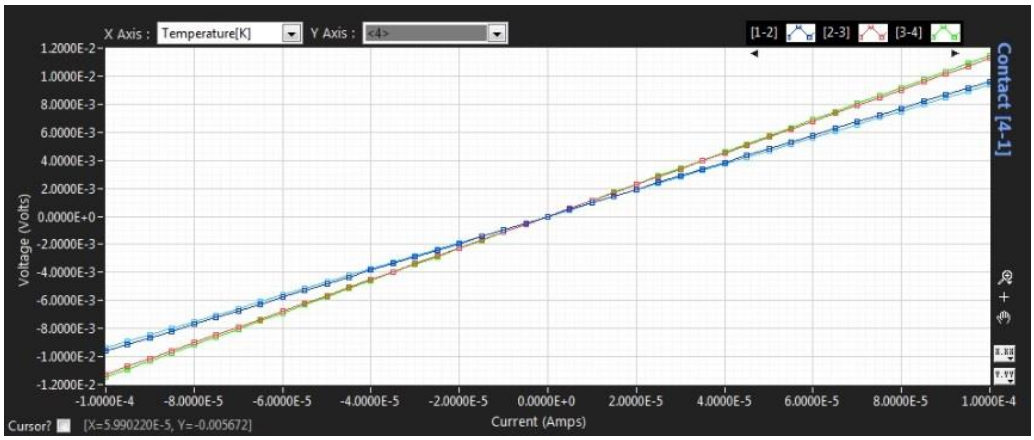
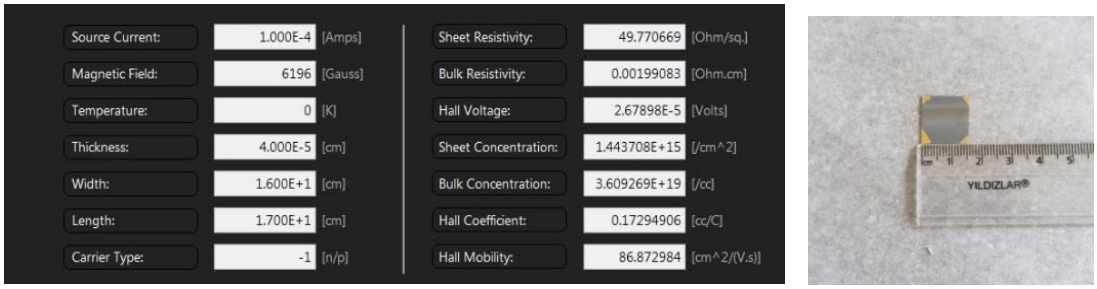


Figure 4.18. Voltage versus current graph for every contact of 2000 rpm spin coated 950 ˚C annealed for 8 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)



a) b)

Figure 4.19. a) ezHEMS results of 2000 rpm spin coated 950 ˚C annealed for 8 minutes with RTA b) Picture of the sample L= 17 mm W= 16mm thickness is assumed 400nm in the measurements

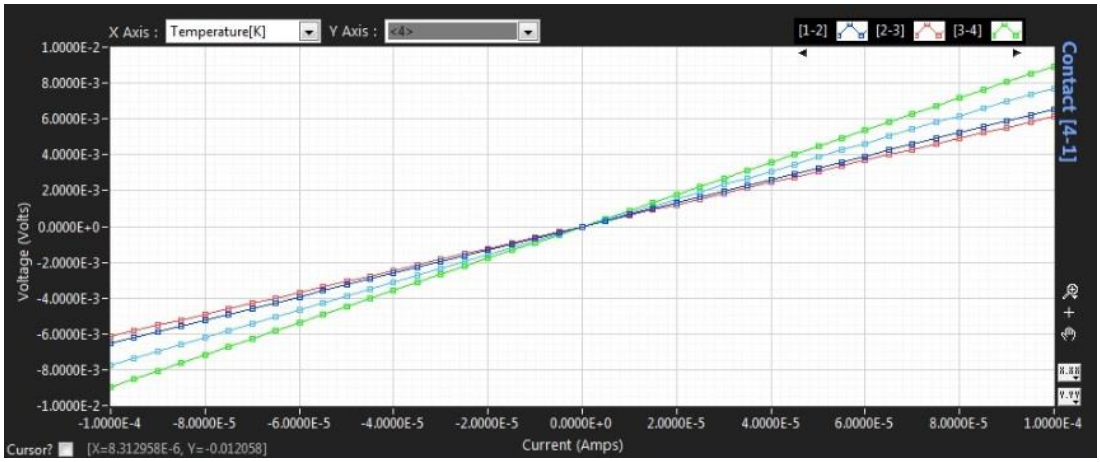
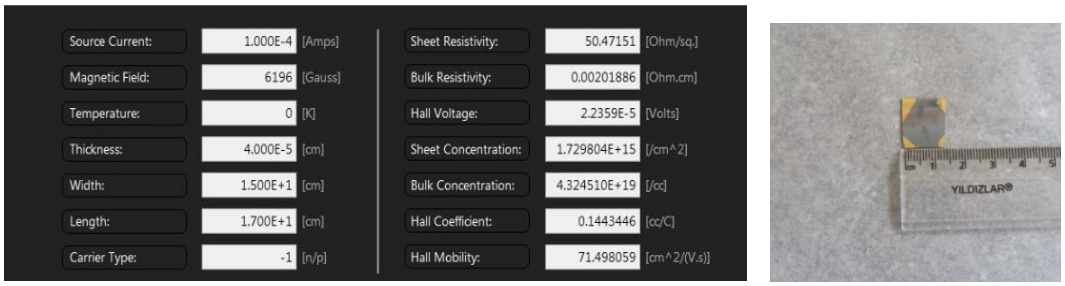


Figure 4.20. Voltage versus current graph for every contact of 2000 rpm spin coated 950 ˚C annealed for 12 minutes with RTA(royal blue between 1-2, red between 2-3, green between 3-4 and light blue between 4-1)



b) b)

Figure 4.21. 45 a) ezHEMS results of 2000 rpm spin coated 950 ˚C annealed for 12 minutes with RTA b) Picture of the sample L= 15 mm W= 13mm thickness is assumed 400nm in the measurements

Since all of the dimensions of the samples and sizes of the coated metals are not equal voltage versus current lines are not the same. However, they are close to each other which means ohmic contacts at the corners are functional. After doing a series of experiments on doping, results of different coating speeds and different annealing times are compared. In the below Table 4.2 comparison between 1000 rpm and 2000 rpm coating speeds for mobility and sheet resistance is given

Table 4.2. Comparison between 1000 rpm and 2000 rpm spin coating speeds for SOD process

Spin Coating Speed (rpm)	RTA Temperature (°C)	Curing Time(minute)	Mobility ($cm^2/V.s$)	Sheet Resistance (ohm/sq.)
1000	950	4	71.4	72.2
1000	950	8	80.9	42.9
1000	950	12	80	48.6
2000	950	4	70.74	65.8
2000	950	8	86.9	49.8
2000	950	12	71.5	50.5

Since 2000 rpm speed offers more mobility and not near sheet resistivity in the production process it is decided to be chosen.

4.3. Producing Doped Thin Film Silicon Layer From SOI Wafer

To pursue a similar approach to chapter 2.3 thin transistor approach an SOI wafer is purchased with a 300nm single crystal silicon layer on top of the 2000nm buried oxide layer. The production method for the SOI wafer is Unibond which means that SOI wafers are produced by directly bonding a thermally grown SiO_2 coated Si wafer and clean Si wafer. The resistivity of the thin silicon layer for this wafer is 1-10 ohm.cm. In this process, there are three main parts; photolithography, coating, and etching. To produce a better coating negative photoresist process is used which means

that black parts in Figure 4.22 will be removed and transparent parts will get thicken after UV exposure. Process steps are given below starting with photolithography:

- Az5214 photoresist is coated at 4000 rpm for 45s on the Si wafer.
- The photoresist is cured on the hot plate at 110 ºC for 50 s.
- Using mask aligner and designed mask in Figure 4.22 samples are exposed to ultraviolet light in desired parts. Exposure time was 15s with the mask.
- The photoresist is cured again on the hot plate for 120s at 120°C.
- The sample is exposed to UV light for 120s.
- To solve exposed photoresist and form designed pattern samples are placed in the developer solution. Used developer solution is AZ MIF 726 and developing time is 60 seconds.

Figure 4.22. Designed mask for lithography

After photolithography, Al and Au coating is done. In this experiment, the metal coating is used as a mask for TMAH etch. As it is pointed out previous chapters thermally grown SiO_2 is a better mask for TMAH; however, the Si layer on top of the SOI wafer is very thin and when the thermal growth process is applied it will get thinner.

- In the evaporator, 20nm Al with the speed of 0.1nm/s and 100nm Au with a speed of 0.4 nm/s are coated.

- After coating samples are dipped in acetone and with help from an injector metal layers are peeled.
- For one last step samples are heated at 250 ºC for 4 minutes on the hot plate.

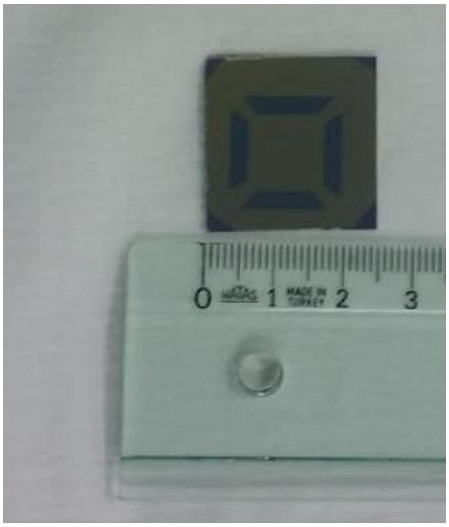


Figure 4.23. Coated sample before etching. Yellow parts are gold to prevent TMAH etching.

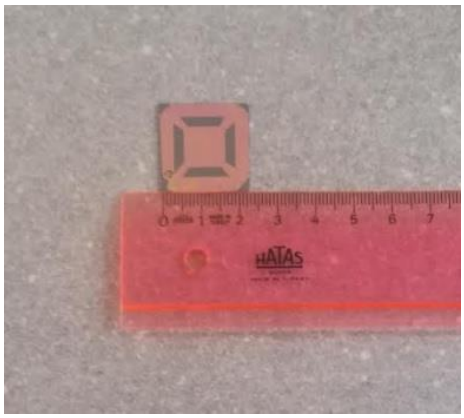
The etching part consists of two different etching first one is silicon etch to reach the buried oxide layer and the second part is metal etch to remove the mask. Steps for etching part is given below:

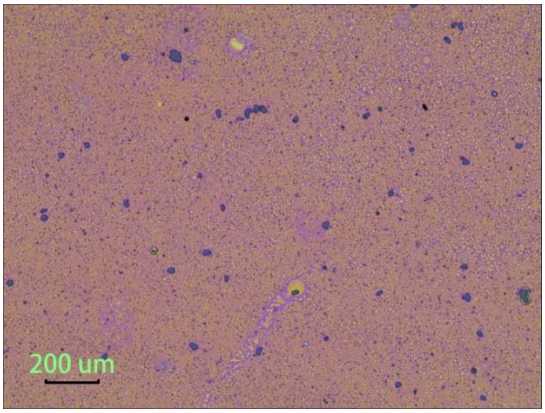
- Si layer is etched by 25% TMAH solution at 70ºC. Etch time was 30s.
- 16 grams KI, 4 grams I and 160 ml water are mixed to get etching solution for gold and aluminum.
- Samples are exposed to the solution for 30 s.

Figure 4.24. Picture of undoped and shaped Si layer on SOI wafer

The upper silicon layer has a thickness of 300nm which means to handle and continue process there is a need for a plastic substrate. As it is indicated many times before plastic substrates cannot withstand high temperatures such as it is needed to complete doping. Therefore, the doping process comes before the releasing process. Doping is done based on previous experiments and steps are:

- SOD is coated at 2000 rpm 60s and cured at 950 °C for 480s.
- Samples are exposed to BOE solution for 3 minutes to remove residue of SOD.

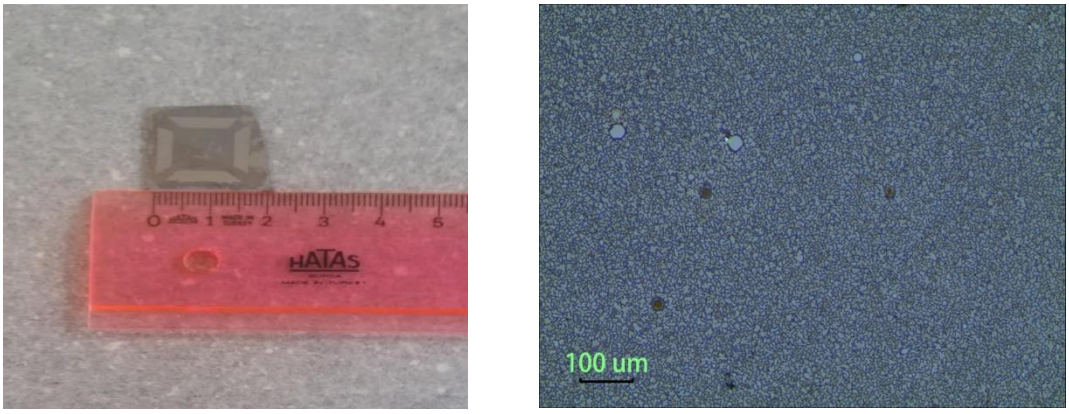




a) b)

Figure 4.25. a) Picture of doped Si layer on top of SOI wafer. b) Microscope picture for surface of the sample

Sample in the Figure 4.25 a) is measured with 4 point probe prove technique and sheet resistance is found as 124.6 ohm which is proof that it is doped and conductive. The final step is releasing the upper Si layer. When the buried oxide layer is completely removed Si layer will be connected to substrate by corner connections and they can be broken off easily. To etch oxide layer samples are exposed to %49 HF solution; however, HF solution is also harmed Si layer and after 1-hour samples look like Figure 4.26.



a) b)

Figure 4.26. a) Picture of sample after 1 hour %49 HF etch. b) Microscope picture of the same sample

When samples are measured with 4 point probe technique no result is found. It can be said that samples are no longer conductive. Conclusion that HF is also etched Si layer in 1 hour can be reached easily under these circumstances. To be sure about our results Si layer is also tried to be transferred on to kapton tape and measured with the ezHEMS device. In the following figures, pictures of transferred Si layers and results can be seen.

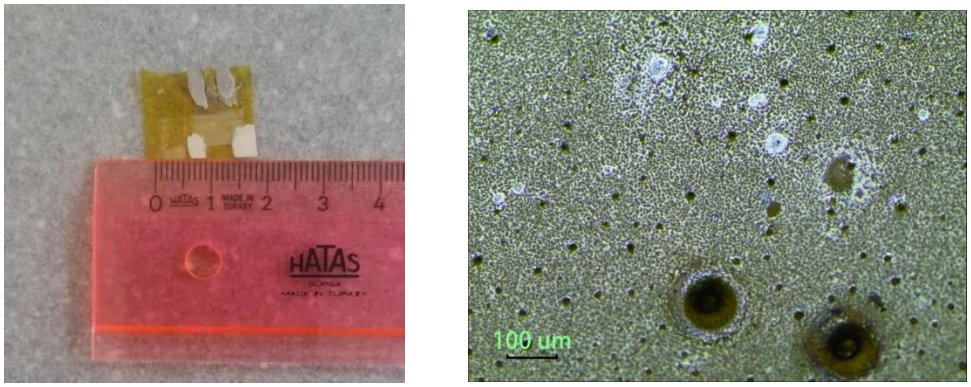


Figure 4.27. a) Picture of Si layer transferred on to kapton tape and contacts are formed with silver paint. b) Microscope picture of same sample

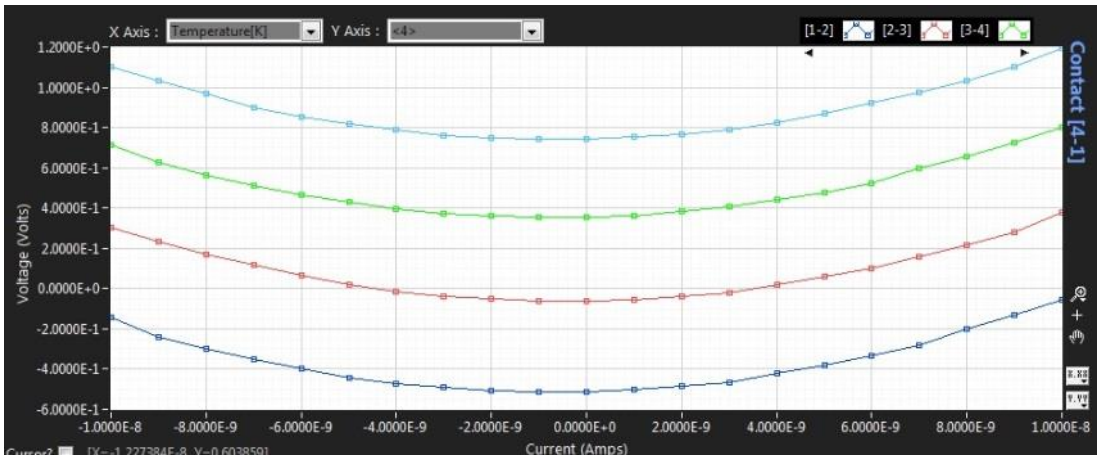


Figure 4.28. ezHEMS IV graph for Si layer transferred to kapton tape

From graphs in Figure 4.28, it can be concluded that there is no conductivity between 4 contacts which is formed with silver paint. With these results initial conclusion that the Si layer gets etched by HF is also confirmed.

At this point, it is crucial to check that large etching time in concentrated HF constitutes a problem. To check that A new mask is formed with thin strips like in the previous chapters. The same processes are applied until releasing step. In Figure 4.29 new mask can be seen.

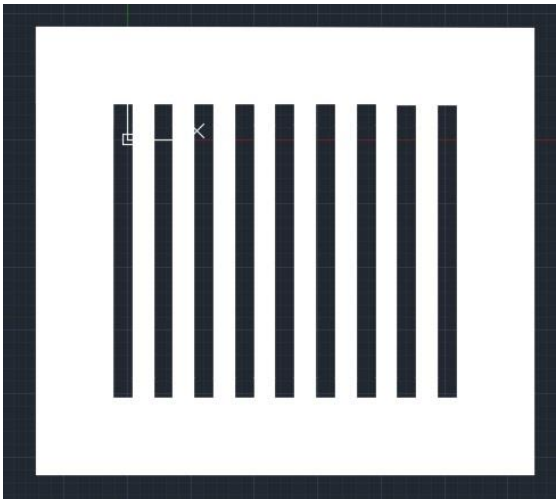


Figure 4.29. Mask for reaching buried oxide layer. Width of the strips are 400 µm and length of the strips are 1cm.

After following the exact steps with the same parameters for releasing step samples are exposed to the %49 HF solution for just 5 minutes. In the following figures, pictures for process steps can be found.

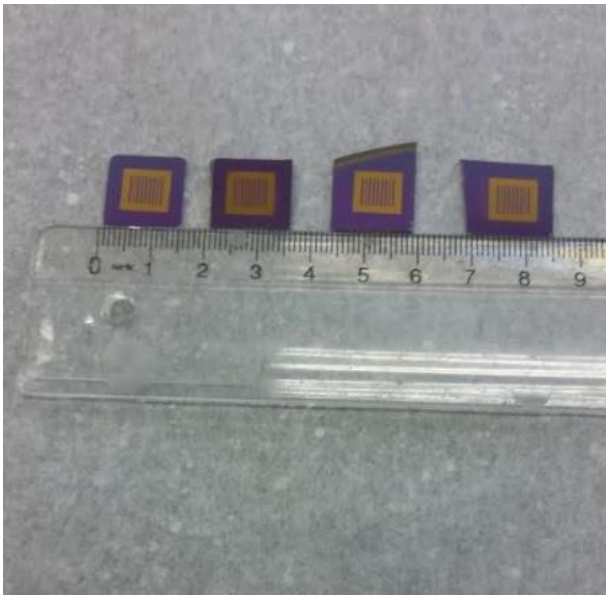


Figure 4.30. Coated samples before etching. Yellow parts are gold to prevent TMAH etching.

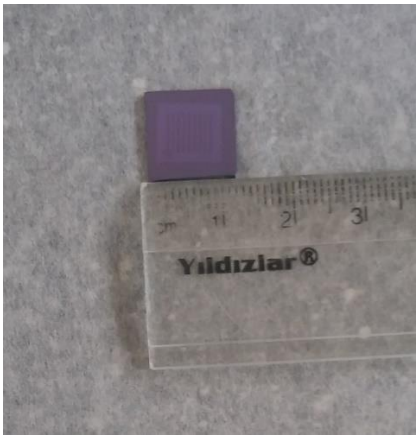


Figure 4.31. Picture of undoped and shaped Si layer on SOI wafer

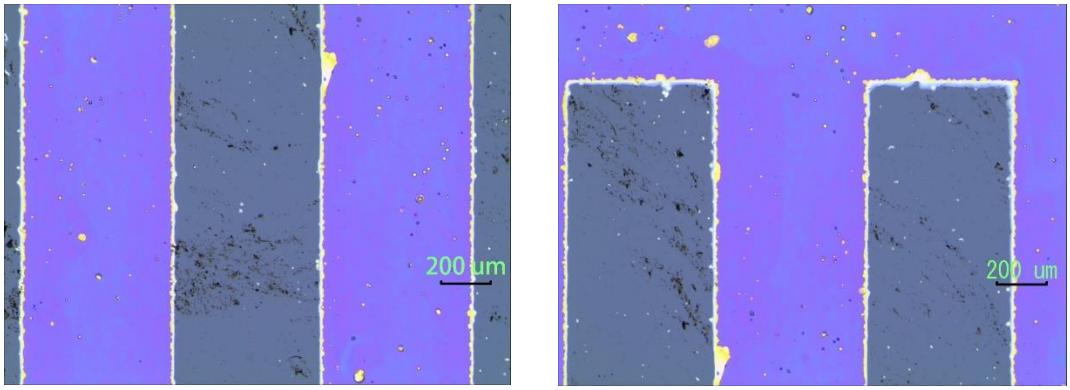


Figure 4.32. Microscope picture of the samples in the figure 4.29

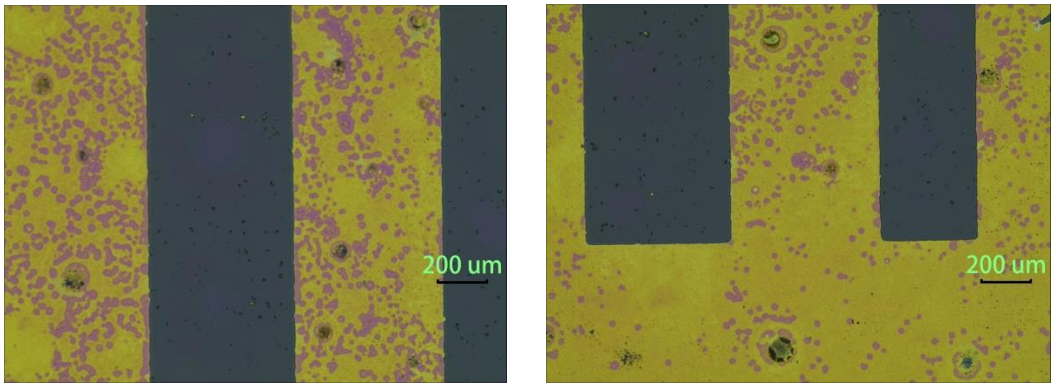


Figure 4.33. Microscope pictures of the samples after 5 minutes of %49 HF etching

As can be seen in Figure 4.33, exposure of HF for a significantly smaller time also harms the Si layer. After getting these result we decided to back down from this method and use a direct approach.

4.4. Thinning and Testing the Doped Silicon Flexibility.

Thinning without damaging the silicon wafer is crucial in the production of NMOS transistors. The main goal for this work is to build a flexible transistor which can only be possible with thinning and transferring the silicon wafer into a plastic substrate elegantly. In the methods for the thin-film transistor making chapter, there are several neat ways to obtain thin-film silicon is described. However, many of them require costly equipment and materials. Furthermore, nearly all of them include elaborate processing techniques. To minimize the accidental wafer breakage in this research a very different and simplistic method is followed. In the design section, a SiN_x and SiO_2 growth for silicon wafer is mentioned. As the first step, this layer is grown on to silicon layer. Since KOH etching of silicon is infinitesimal thickness was not important. To be safe 100nm of SiN_x and SiO_2 layer is grown. Since this layer will only be used as a protective mask for KOH etching, photolithography step is needed to shape the layer. Photolithography step is given in detail below:

- Az5214 photoresist is coated at 4000 rpm for 45s on the Si wafer.
- The photoresist is cured on the hot plate at 120 ºC for 60 s.
- Using mask aligner samples are exposed to ultraviolet light in the desired parts. The exposure time was 120s with the mask.
- To solve exposed photoresist and form designed pattern samples are placed in the developer solution. Used developer solution is AZ MIF 726 and developing time is 60 seconds.
- The photoresist is cured again on the hot plate for 60 s at 120°C.
- Samples are etched in BOE for 8 minutes.
- To remove photoresist layer samples are cleaned with acetone isopropyl alcohol and deionized water.

Parameters on the above steps are tested and controlled in detail before the experiment. In the below Figure 4.34 pictures of samples after the above steps are given.

a) b)

Figure 4.34. a) Image of samples before BOE etching b) Image of the samples after BOE etching photoresist layer is removed

After obtaining the designed patterned on top of the silicon layer silicon etching can be performed. KOH selected as etchant because of mask availability, etching speed, and process simplicity. As explained before the higher concentration of KOH solution offers better roughness, but at the same time, it offers slower etching speed. After some experimentation, we decided that 50% of concentration can both be fast and offers good roughness. Process steps of KOH are given below in detail:

- Without any additional process, samples are directly exposed to KOH solution.
- KOH concentration is 50%, temperature 90 $°C$ Etch time is 2 hours 40 minutes.
- Some of the openings that are created for thinning are broken after KOH solution.
- Some of the openings are mishandled by the holder and broken of.

In Figure 4.35 there is an image of samples after KOH etching.

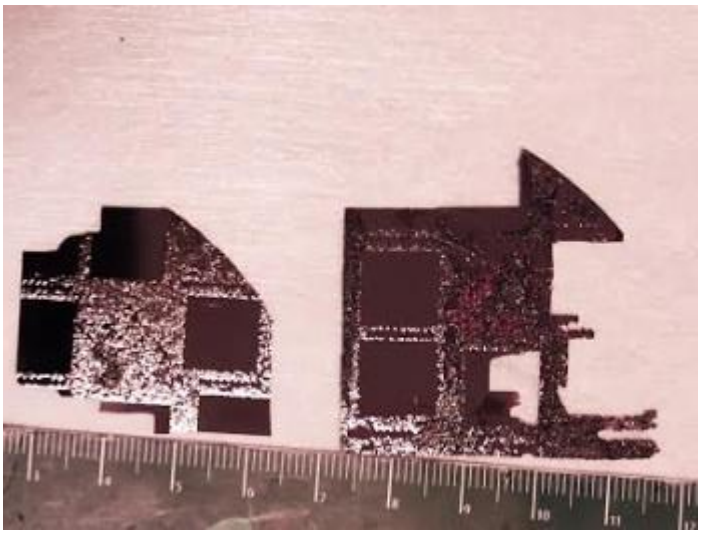


Figure 4.35. Image of the samples after KOH etching.

After KOH etching samples are cleaned with acetone, isopropyl alcohol, and deionized water to remove chemical residue. Some broken pieces are used to measure the final silicon thickness which is 30 μm. Furthermore, some of the broken pieces are used to show flexibility. Figure 4.36 and Figure 4.37 images for thickness and flexibility can be found.

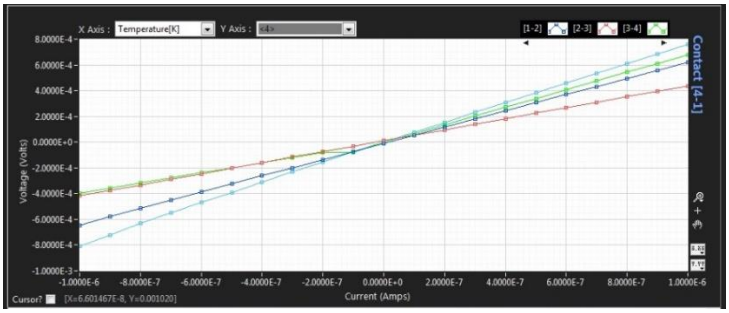
Figure 4.36. Image of measuring thickness with micrometer. Flexibility of 30 μm thickh silicon layer coated with SOG on kapton tape. L=10mm W=6mm

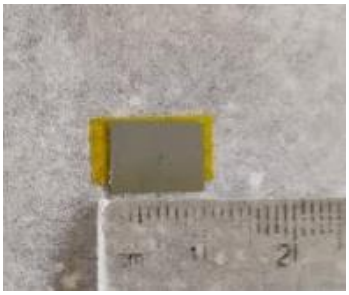
Figure 4.37. Flexibility of 30 μm thickh silicon layer coated with SOG on kapton tape. L=10mm W=6mm

After testing the flexibility we need to know that the doping process that is optimized for a thick silicon wafer is applicable for 30 μm thick silicon layer. To be able to process thinned wafers easily, samples are not transferred to kapton tape. Moreover, as it is explained before plastic substrates cannot withstand high temperatures that are required for diffusion. Step for doping process are:

- To dope the samples, first desired openings should be created with the help of SOG.
- In this process openings created with thinning are directly doped because to measure the parameters such as mobility and sheet resistance relatively large size of the thinned wafer is required.
- Using PR, designed mask is transferred to the sample and shaped with BOE solution.
- SOD is coated at 2000 rpm 60s and cured at 950 °C for 480s.
- Samples are exposed to BOE solution for 3 minutes to remove residue of SOD.

After doping process samples are transferred to kapton tape by breaking from the thick windows of thick silicon wafer. With the help of ezHEMS device parameters of the doped silicon wafer is measured. In the following figures, images of samples and results of ezHEMS device are given.





b) b)

Figure 4.38. a) Voltage versus current graph of doped thin silicon wafer. b) image of the doped thin silicon wafer L=10mm W=6mm t=30µm.

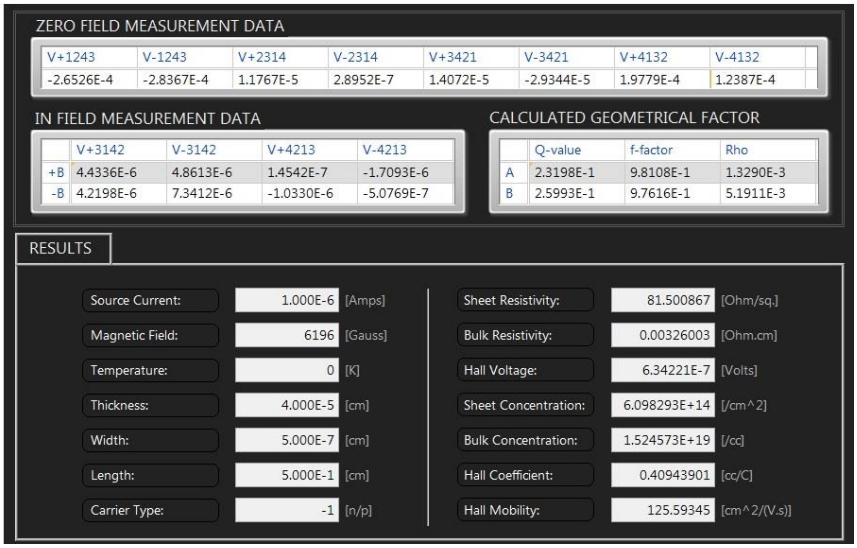


Figure 4.39. Ez HEMS results of 30 µm thick flexible doped silicon wafer

When the results are examined it can be said that mobility and sheet resistance values are very close to the 500 µm thick samples. Voltage versus current graph shows us there is some inequality; however, since the dimensions of the sample are not equal to each other different IV lines are very reasonable. At the end of this experiment, we are sure that a thin flexible doped wafer with the same parameters as a thick silicon wafer can be produced. The next step of completing this work is to build NMOS transistors on top of thinned wafers.

4.5. Producing Traditional NMOS transistors

Before moving on to produce a thin flexible NMOS transistor, the operation of the thick transistors should be controlled. By using the same masks given in the designed part, traditional NMOS transistors are built. For fast and easy process instead of clean Si wafers 300nm thick thermally grown SiO_2 coated wafers are used. Again to speed up the process alignment mark mask is not used instead process is started directly with partial doping mask in Figure 3.1 and the following masks are used respectively. Process is started with photolithography:

- Az5214 photoresist is coated at 4000 rpm for 45s on the Si wafer
- The photoresist is cured on the hot plate at 120 ºC for 60 s.
- Using mask aligner samples are exposed to ultraviolet light in the desired parts. The exposure time was 120s with the mask.
- To solve exposed photoresist and form designed pattern samples are placed in the developer solution. Used developer solution is AZ MIF 726 and developing time is 60 seconds.
- The photoresist is cured again on the hot plate for 60 s at 120°C.
- Samples are etched in BOE for 8 minutes.
- To remove photoresist layer samples are cleaned with acetone isopropyl alcohol and deionized water.

In Figure 4.40 BOE etched Si wafer picture is given.

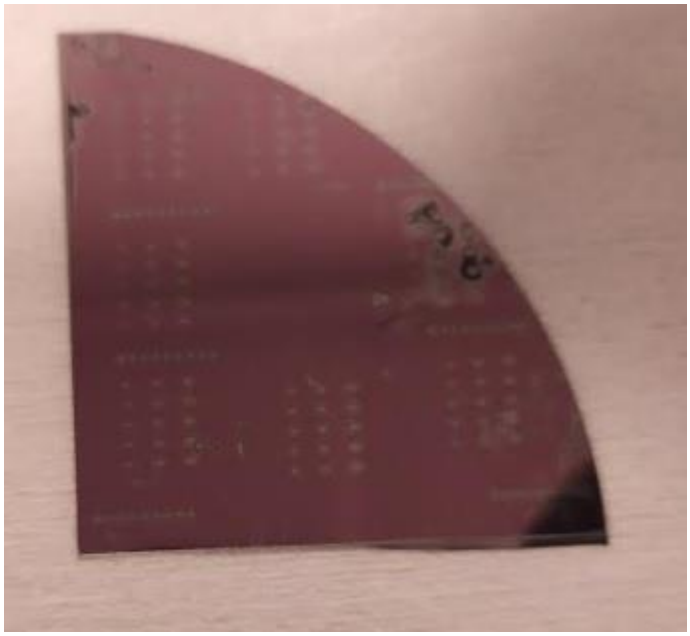


Figure 4.40. BOE shaped Si wafer. Partial doping opening can be seen.

The doping step is the same as before processes. Therefore there is no need to write steps again. After doping step gate oxide should be formed. Since it is a traditional NMOS transistor it is decided not to use SOG. Instead of the SOG oxide layer is coated by sputtering and its thickness is 200nm. Since there is no alignment mark in these transistors cleaning with BOE after the doping step is cut short and remaining thermally grown oxide layer used as an alignment mark. Following process is forming the ohmic contacts and has the following steps:

- Using a photolithography process designed mask is transferred on top of the SiO_2 layer.
- With the help of the BOE solution photoresist mask is transferred to the SiO_2 layer. Etching time is 3 minutes.
- Using the photolithography process again designed mask for metallization is transferred on top of the SiO_2 layer.
- After photolithography O_2 plasma is applied for cleaner Si surface for ohmic contacts.

- Using thermal evaporator Cr and Au is coated. The thickness of the Cr is 20nm with the rate of 0.1nm/s and the thickness of the Au is 50nm with the rate of 0.4nm/s.

Cr and Au used as ohmic contacts because they are tested before in the doping experiments. Since we need working transistors to examine the results and finally compare them with thin ones working ohmic contacts are chosen. In Figure 4.41, Figure 4.42, Figure 4.43 and Figure 4.44 final shape of the transistors can be seen.

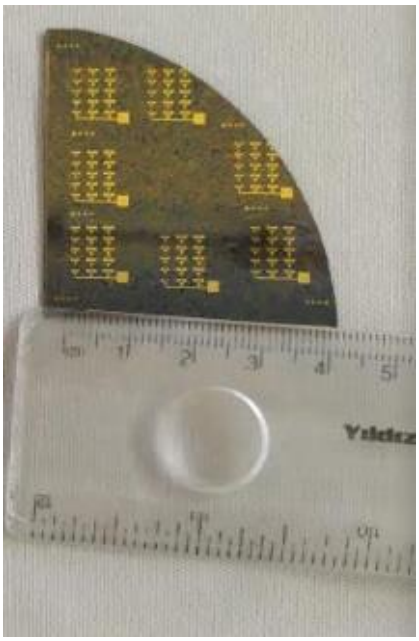


Figure 4.41. Final form of the transistors on the quarter of the 4 inch Si wafer

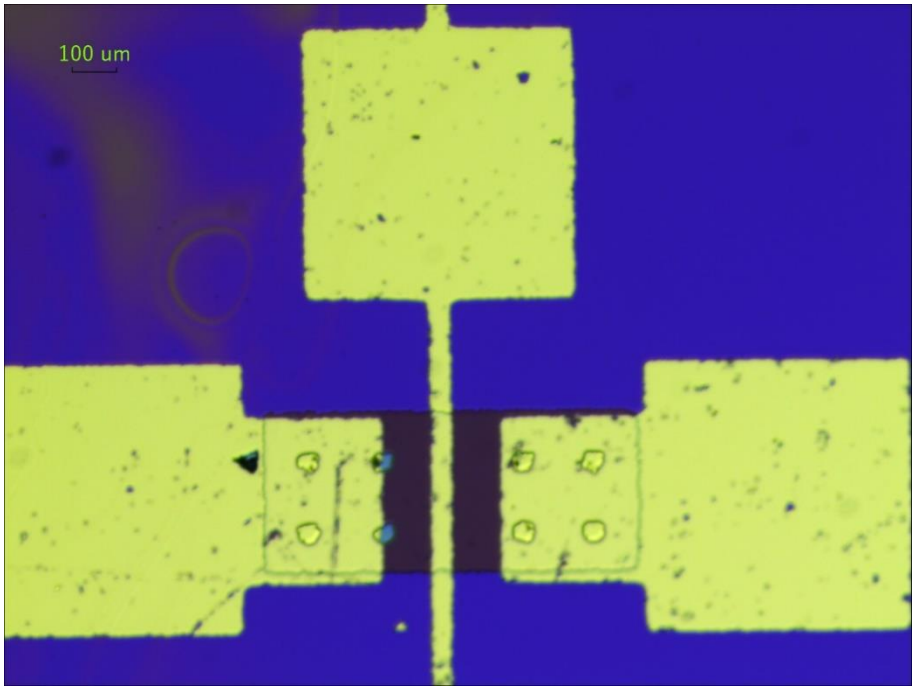


Figure 4.42. Microscope image of the L_1=50 µm transistor

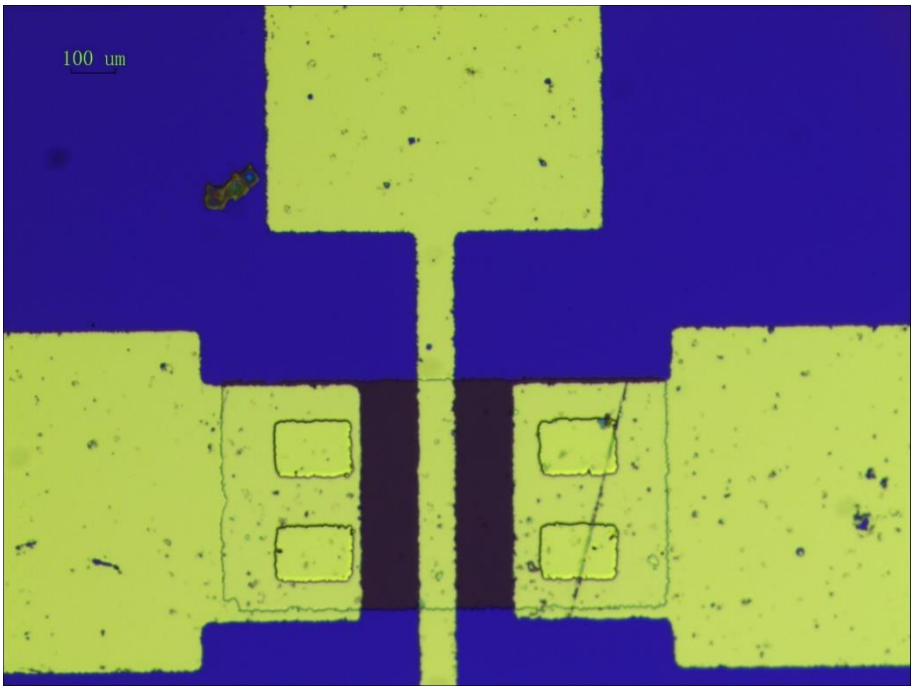


Figure 4.43. Microscope image of the L_1=75 µm transistor

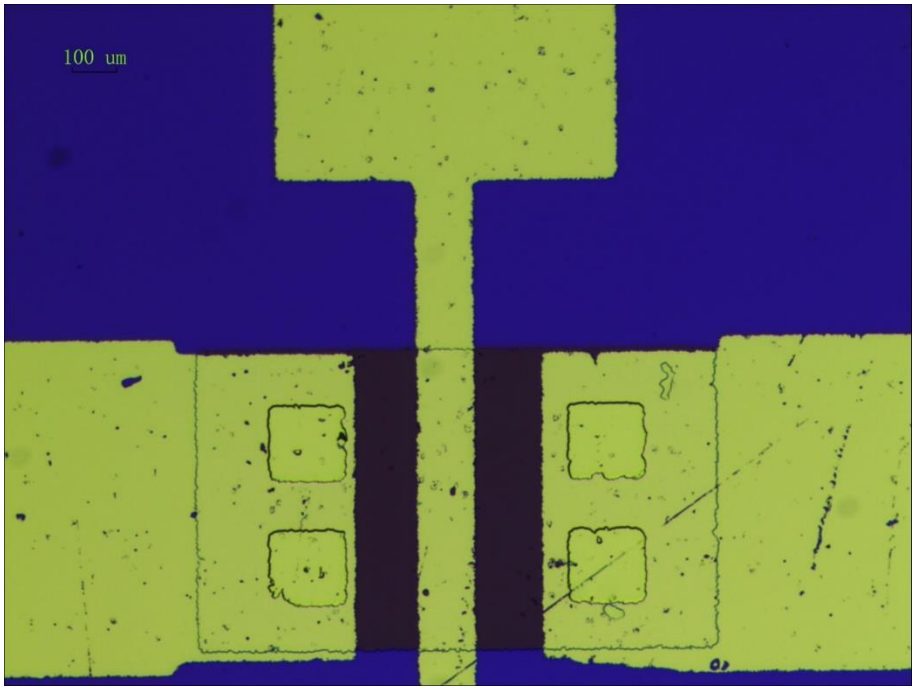


Figure 4.44. Microscope image of the L_1=100 µm transistor

In the design part, it is decided that transistors are depletion mode. However, in the IV measurements since the doping level is very high changing V_{GS} does have a very insignificant effect on I_{DS}. To see transistor behavior from these built MOSFETs, we decided to measure between the drain of one transistor and the source of another transistor. Therefore, partially doped rectangular for one MOSFET acts as a drain or source. In the final structure that is shown in Figure 4.41, there are 7 squares and every square has 18 MOSFETs with 3 different sizes to test. Original sizes for depletion mode designed MOSFETs are from smallest to largest; L_1=50 µm, W_1= 350 µm, L_2=75 µm, W_2=450µm, L_3=100µm and W_3=550µm. Since transistors are not working horizontally now parameters should be calculated again vertically. Distance between the same transistors are also different. Distance is denoted as t and values are; t_1= 1500µ, t_2=1400µ, t_3=1300µ. Metal pads formed for gate contacts originally have also different sizes. For NMOS1 gold pad is a square with 400µm edge size and for NMOS2 and NMOS3 gold pad is also a square with 500µm edge size. In Figure 4.45 pictures of the equipment that is used to take IV measurements are given.

a) b)

Figure 4.45. a) Picture of the sample on Nanomagnetic Instruments' Ez-HEMS room temperature head. b) Picture of Keithley 2612 sourcemeter device which is used to take IV measurements.

In the following figures IV graphs for the different size MOSFETs are given and in between pictures parameters for MOSFETs are calculated.

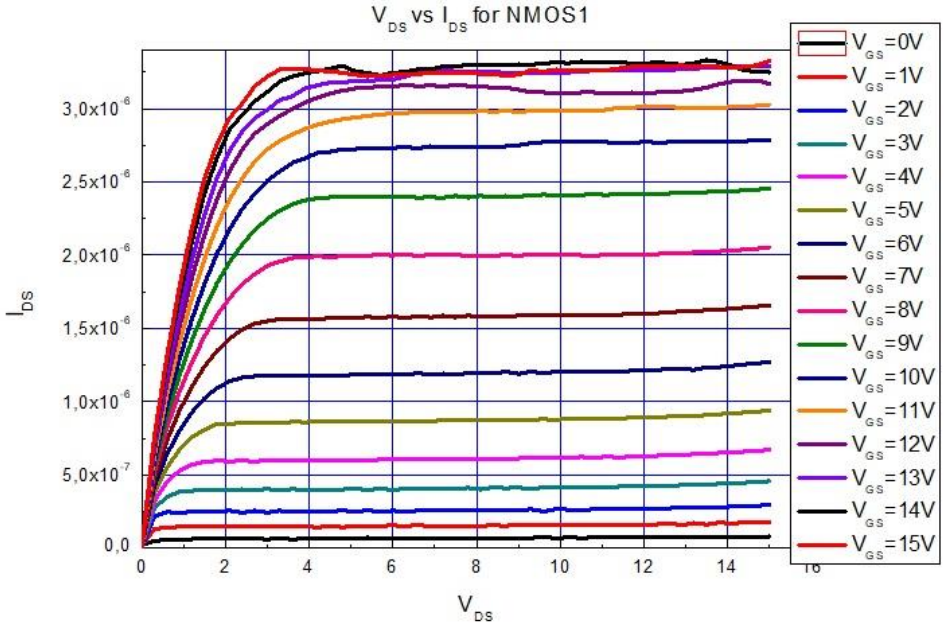


Figure 4.46. V_{DS} vs I_{DS} graph with different V_{GS} values for NMOS1

From Figure 4.46 above it can be said that NMOS transistors are working properly. To check the quality of the transistors we can calculate μsat and on/off ratio. Saturation mobility can be calculated by using the equation 1.2 and V_T value that is

approximated from the graph. On the other hand, On/off ratio can be easily calculated by just dividing the on-state drain to source current to off-state drain to source current. As L parameter distance between two doped regions in the same-sized transistors is used which is denoted as t_1. For W parameter metal-coated areas between two same-sized dope regions are used; however, the width of the coated metal between transistors is not constant. To have a meaningful result average width is used. In this transistors, W/L ratio is found 0.095. Rest of the calculations are in below:

- $C_i=\frac{\varepsilon_r \varepsilon_0}{d}$ = 1.64*10^{-4} F/m^2 where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant of SiO_2 and d is the thickness of the SiO_2 layer between gate and Si layer. ε_0 is 8.854*10^{-12} and ε_r is assumed as 3.7 which is the lowest value for SiO_2 [37]. The lowest value is accepted because sputtered SiO_2 is used. As mentioned before the thickness of the oxide layer coated with sputtering is 200nm.
- I_{DS} value taken from Figure 4.46 as 2.8 μA and V_T is estimated by using equation 1.1 and non-linear curve fit function of the Origin Lab program to be 6.6V for V_{GS}=10V. Estimation can be examined in Figure 4.47. In the estimation with curve fitting, some assumptions are made; therefore, some deviation is understandable. By using IV graph estimated V_T and equation 1.2 μsat is calculated as 155.5 cm^2/V.s. As a reminder equation 1.1 and 1.2 are given below:

$$I_{DS} = C_i \mu_{FE} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2], \quad (1.1)$$

$$I_{DS} = C_i \mu_{sat} \frac{W}{L}(V_{GS} - V_T)^2, \quad (1.2)$$

- On/off ratio is relatively simple to find. In Figure 4.46 for higher V_{GS} values transistor is not working properly therefore correct V_{GS} should be chosen. For V_{GS}= 10 on/off ratio is found 34.7. The reason behind the small on/off ratio is small W/L ratio. Since transistors are not working in the way we designed small on/off ratio is very normal it can be avoided just raising the W/L ratio.

- Since V_T is known g_m can be calculated using the below equation.

$g_m=\frac{2I_{DS}}{(V_{GS}-V_T)}$ in saturation region (4.1) [38]

- Using the equation 4.1 and V_T from the graph g_m saturation for V_{GS}=10 is found 1.1 µA/V

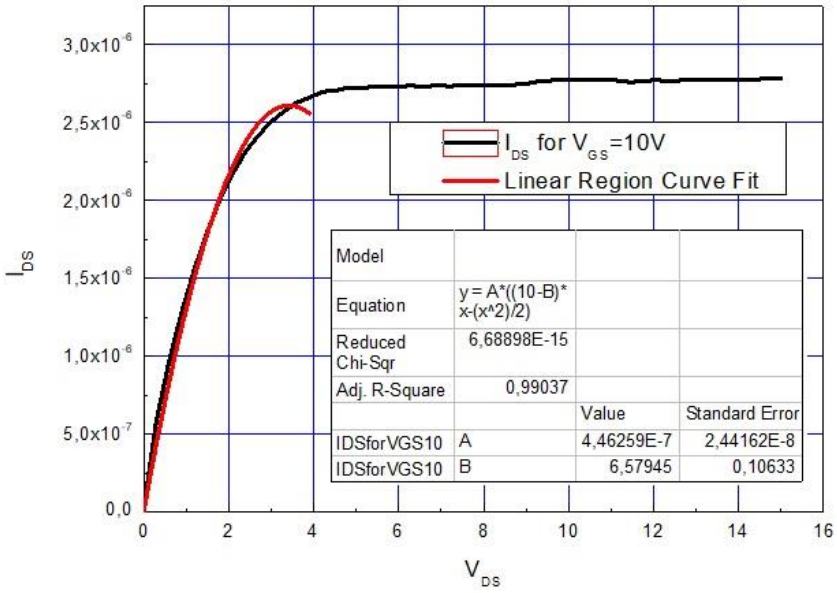


Figure 4.47. Linear region curve fit for NMOS1

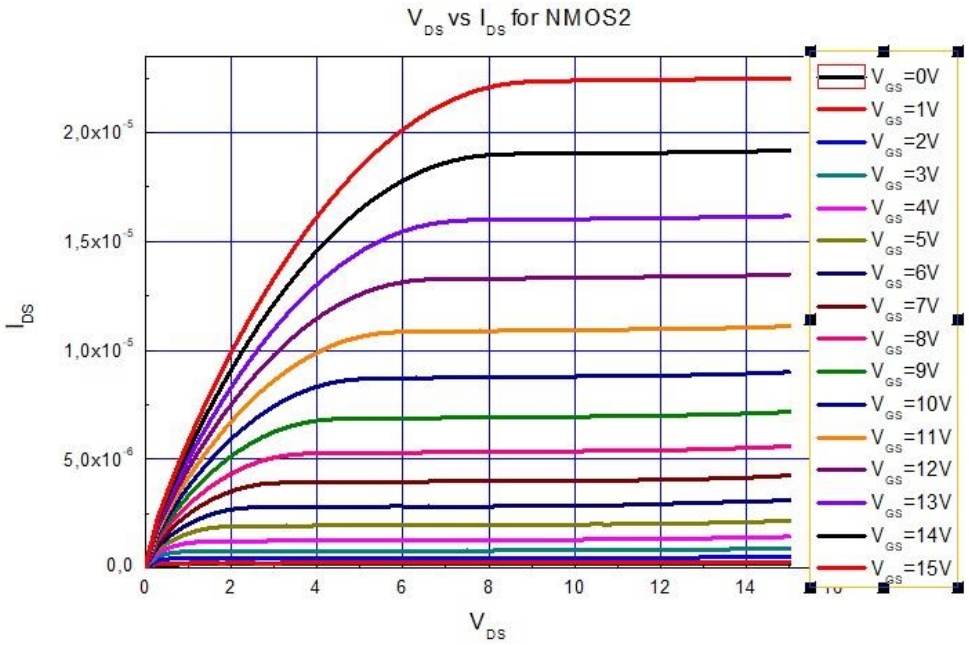


Figure 4.48. VDS vs IDS graph with different VGS values for NMOS2

- C_i is the same for every transistor which is $1.64*10^{-4}$ F/m^2
- I_{DS}=9 µA from Figure 4.48. From the curve fitting for linear region in Figure 4.49 V_T is found 5.6 V. W/L ratio for these transistors are averaged 0.162. By using the equation 1.2 and V_T value from curve fitting µsat is calculated 175 cm^2/V.s.
- The on/off ratio for V_{GS}=15 V is 102.7. Again it can be higher with a higher W/L ratio.
- Using the equation 4.1 and V_T from the graph g_m in saturation for V_{GS}=10V is found 4.2 µA/V

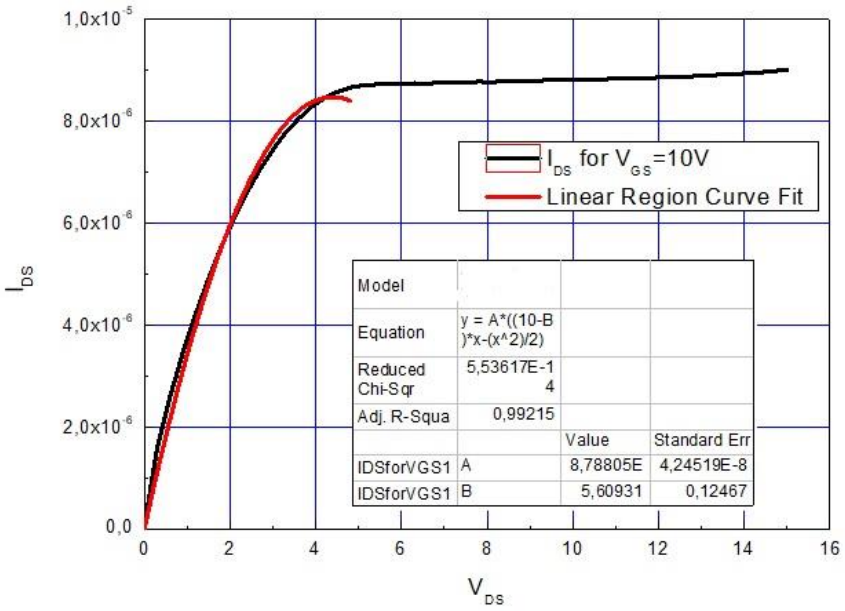


Figure 4.49. Linear region curve fit for NMOS2

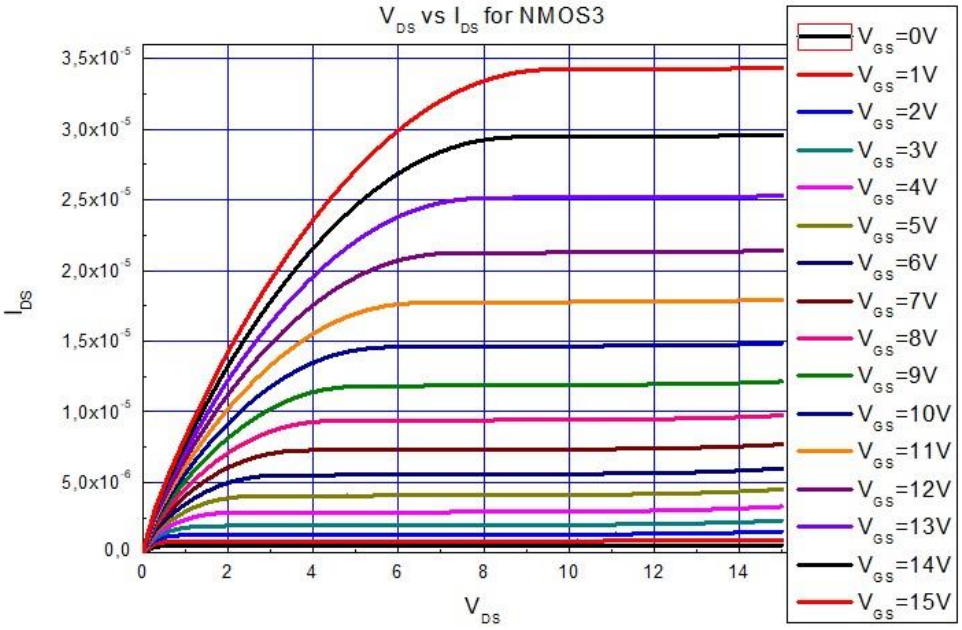


Figure 4.50. VDS vs IDS graph with different VGS values for NMOS3

- C_i is the same for every transistor which is $1.64*10^{-4}$ F/m^2

- I_{DS}=14.8 µA from Figure 4.50 . From Figure 4.51 V_T is estimated as 4.9 V. W/L ratio for these transistors are averaged 0.195. Using the equation 1.2 and V_T value from the graph μ_{sat} is calculated 178 cm^2/V.s.
- The on/off ratio for V_{GS}=15 V is 61.7. When the W/L ratio is higher this value also be higher.
- Using the equation 4.1 and V_T from the graph g_m is found 6.8 µA/V

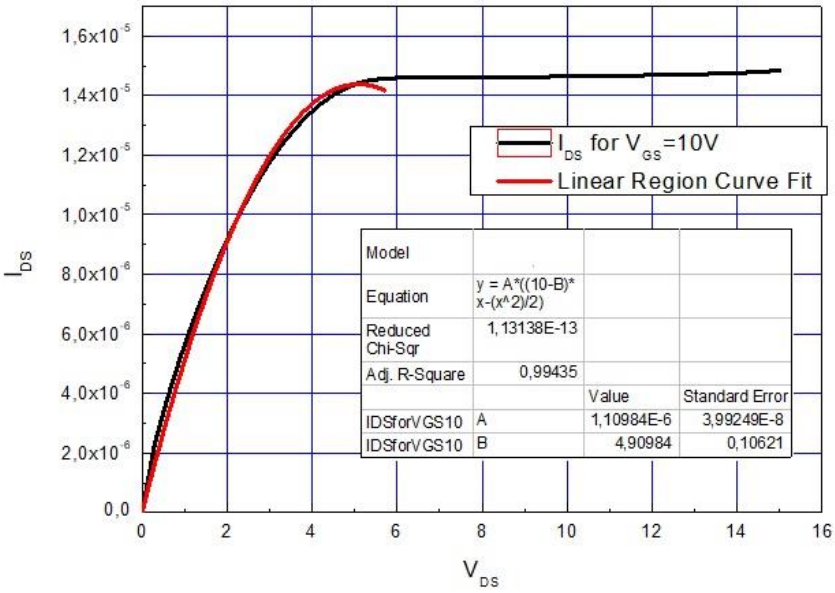


Figure 4.51. Linear region curve fit for NMOS3

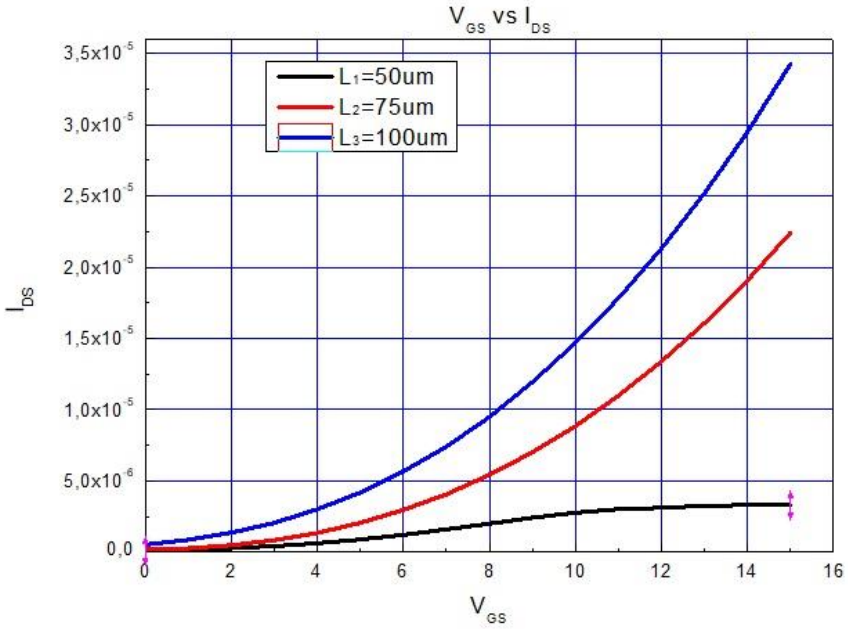


Figure 4.52. V_{GS} vs I_{DS} for different size transistors.

As a result, it can be said that working transistors can be built by using SOD material at relatively low temperatures and in a shorter time that is required to build traditional transistors. However, transistors are not perfect. Since channel lengths are higher and channel widths are lower some problems are observed. By looking at the graphs above one possible problem is body effect. Body effect is the problem of changing V_T values because of an ungrounded body of the MOSFETs. It is understandable because in these examples a p-type doped body terminal is not built. On the other hand, there is a very few channel length modulation. Probable reason behind that gate metals are reaching all of the MOSFET's functional surface, thus allowing the charge inversion on the Si surface. Channel length modulation can be denoted by $\lambda=1/V_A$ and V_A can be found by calculating the ohmic behavior of the MOSFETs in the saturation region and then finding their linear functions slope. Since it is not highly observed in these transistors we will not calculate this parameter. In the following chapter, a thin film NMOS transistor is tried to build by merging the data we accumulate from all of the previous experiments.

4.6. Producing Thin Flexible NMOS Transistors

Previous experiments on doping and thinning showed us flexible and conductive silicon wafer samples can be produced. Designs for NMOS transistor building are given in the previous chapter. Using those designs and knowledge that is obtained from previous experiments transistor building process is started using SiN and SiO2 grown thick silicon wafer which is shown in Figure 4.53.

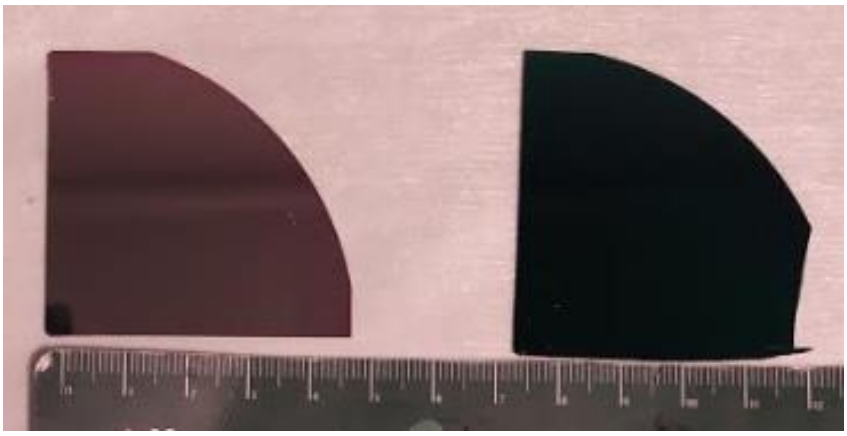


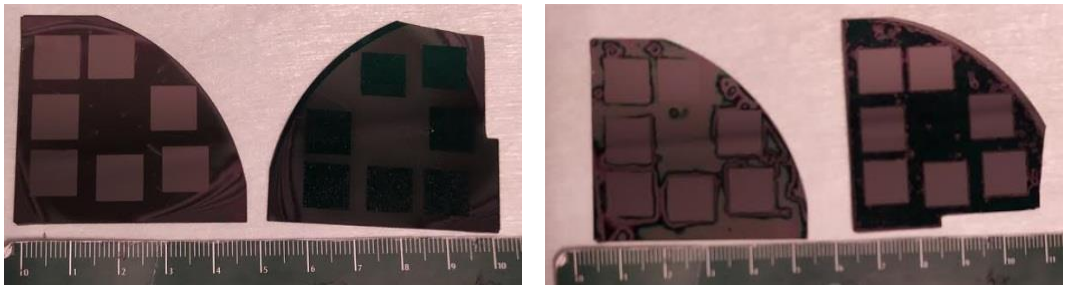
Figure 4.53. Image of SiN and SiO_2 grown silicon wafers

In Figure 4.53 samples are looking a little bit unshapely. When two quarter of 4 inch wafers etched in the KOH etching set up in our laboratory one of them always rubs to glass beaker which causes breakage on the wafer.To prevent damaging the wafer, we shaped the wafer before beginning the process. After growing SiN and SiO_2, photolithography step to form a KOH etching protection mask is described below:

- Az5214 photoresist is coated at 4000 rpm for 45s on the Si wafer
- The photoresist is cured on the hot plate at 120 ºC for 60 s.
- Using mask aligner samples are exposed to ultraviolet light in the desired parts. The exposure time was 120s with the mask.
- To solve exposed photoresist and form designed pattern samples are placed in the developer solution. Used developer solution is AZ MIF 726 and developing time is 60 seconds.

- The photoresist is cured again on the hot plate for 60 s at 120°C.
- Samples are etched in BOE for 8 minutes.
- To remove photoresist layer samples are cleaned with acetone isopropyl alcohol and deionized water.

Photolithography steps are the same as the thinning experiment photolithography step. Since, before in the thinning experiment photolithography step is performed successfully any changes are not necessary for this step. In Figure 4.54 images of the samples before and after BOE etching are given.



a) b)

Figure 4.54. a) Image of samples before BOE etching b) Image of the samples after BOE etching photoresist layer is removed.

Samples are ready for the etching step. In the etching based on previous experiments again, KOH is used. Steps for KOH etching are:

- Without any additional process, samples are directly exposed to the KOH solution.
- KOH concentration is 50%, temperature 90 $°C$ Etch time is 2 hours 40 minutes.
- Some of the openings that are created for thinning are broken after the KOH solution.
- Some of the openings are mishandled by the holder and broken off.

KOH step is also the same as in the thinning experiment part. In our previous experiments, it is seen that KOH etching with the same conditions has not resulted in the same way. For the last few minutes of etching should be observed to avoid unexpected results. In Figure 4.55 thinned Si wafers can be seen.

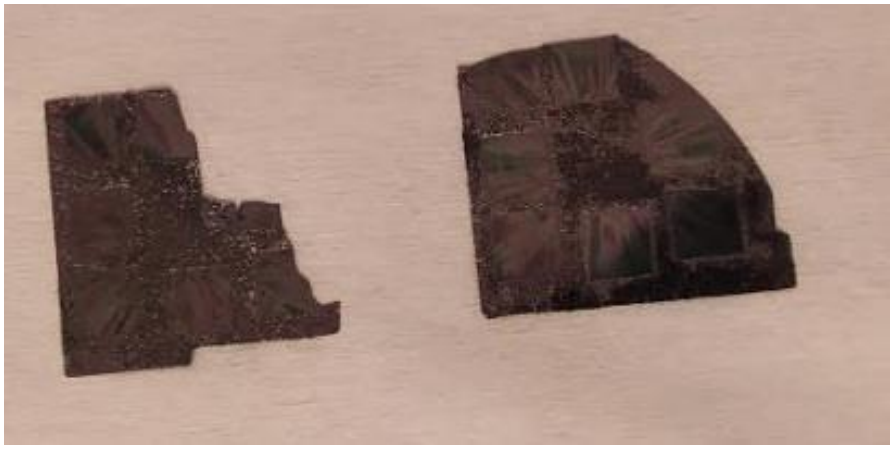


Figure 4.55. Image of thinned Si wafers

In this experiment, some unexpected breakage occurred again during etching but the major part of the samples was still usable in the further process. However, during the drying of the samples right one of the samples was mishandled and shattered. Sample on the left is carried on to the next step which is doping. Steps for doping process are:

- To dope the samples, first desired openings should be created with the help of SOG.
- SOG is coated at 2000 rpm for 60s and cured at 700 °C for 240s.
- Using the photolithography process designed mask is transferred on top of the SOG layer.
- With the help of the BOE solution photoresist mask is transferred to the SOG layer. Etching time is 2 minutes.
- SOD is coated at 2000 rpm 60s and cured at 950 °C for 480s

- Samples are exposed to BOE solution for 3 minutes to remove residue of SOD.

Doping in this experiment is done by partially, unlike thinning experiments. Therefore an extra masking step is required. By forming this mask undesired doping between individual NMOS transistors is prevented. Therefore crosstalk between transistors is prevented. With the doping step, source and drain terminals are created. The next step is to form the dielectric layer. As dielectric layer SOG is designed to be used. To be able to reach doped regions and obtain source and drain terminals for NMOS transistors, openings over doped regions. Placements of these openings are adjusted carefully that the operation of the transistor can be smooth. After required openings are created to obtain contacts for source, drain and gate terminals metal layer is coated with thermal evaporator. Steps for dielectric layer coating and metallization process are:

- SOG is coated at 2000 rpm for 60s and cured at 700 °C for 240s.
- Using the photolithography process designed mask is transferred on top of SOG layer.
- With the help of the BOE solution photoresist mask is transferred to the SOG layer. Etching time is 2 minutes.
- Using the photolithography process again designed mask for metallization is transferred on top of the the SOG layer.
- After photolithography O_2 plasma is applied for cleaner Si surface for ohmic contacts.
- Using thermal evaporator Al and Au is coated however when Al is coated current became uncontrollable and started coated with 3-4nm/s pace. Because of this error photoresist is ruined and bubbles occurred on the surface. The pictures of the final product are given below.

Figure 4.56. Picture of the final ruined product

There were several other experiments to build thin-film NMOS transistors like this. However, in those experiments either etching time was too long and etched all of the Si layer or samples are broken in a way that alignment marks are no longer useful.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

In this thesis single crystal silicon, thin-film transistors are tried to build and evaluated. TFT and MOSFET working mechanisms are examined and explained roughly at first. Then required experiments to be able to produce a thin film MOSFET is done thoroughly. In the MOSFET building process doping is a very significant step. SOD material was crucial in this step. Firstly, thick substrate MOSFETs are built with curing temperature of 150 ˚C. In the IV results of built MOSFET it is seen that for higher V_{GS} values the device is not working properly. To acquire sufficient doping, there were several experiments with SOD material coated with spin coater at different spin speeds. Then samples were cured at RTA oven for different times at 950 ˚C. Results were promising to start to form the thin silicon layer. As given previous works on the topic, releasing the upper silicon layer on the SOI wafer is tried. %49 HF is used to etch the buried oxide layer, thus the upper thin silicon layer will be released. However, HF is started to harm the silicon layer also. After this failure, a more direct approach is pursued. SiNx and SiO2 coated Si wafers are used with KOH. With this process, a doped thin silicon layer is formed and measured. Before moving on to thin-film MOSFET, firstly a traditional MOSFET is built. By building traditional MOSFET it is seen that whether our design is working in the desired way or not. In the measurement phase, it is noticed that the depletion type MOSFET is not suitable to build with our processes. On the other hand, intended depletion type MOSFETs are working as enhancement MOSFETs. Since their designs are not calculated thoroughly, they had a low W/L ratio, high threshold voltage and low on/off ratio. However, these problems can be fixed easily by lowering the oxide thickness between the gate and silicon surface and arranging the design to have a higher W/L ratio. After observing these successful results and potential, the thin-film single-crystal MOSFET process is started. After thinning the silicon layer there are still doping, three photolithography and metallization steps. Although thin silicon films are flexible, the thicker silicon frame that is designed and can be seen in Figure 3.1 was not flexible

enough. Therefore, many of the samples that are thinned are broken in further processing. Since many of the devices that are used required a vacuum to hold samples steady, many of the samples cannot withstand the force of these vacuums and cracked or broken completely. After several tries, just one of the MOSFETs can reach to metallization step and because of a little mistake, that sample was also ruined. In our cleanroom facility, we had some problems and cannot continue processing for more tries. However, it can result from the built traditional thick substrate MOSFETs that thin-film single-crystal functional MOSFETs can be built.

For future work, after achieving single crystal thin film MOSFETs they can be compared with traditionally build ones and other thin film transistor examples. Surface roughness of the KOH etching and Si wafer can also be measured and the effect of it can be discussed. Since transistors are flexible physical limits of the transistors can be tested and how these physical limits affect transistor parameters can also be researched. Finally, if properly working single crystal thin film MOSFETs achieved, they can be incorporated into other devices, such as bendable screens and wearable smart technology, as a driving circuit.

REFERENCES

[1] (n.d.). Retrieved from http://www.sjsu.edu/faculty/watkins/transist.htm

[2] Correia, A. P. P., Cândido Barquinha, P. M., & Goes, J. C. da P. (2016). A Second-Order ΣΔ ADC Using Sputtered IGZO TFTs, 5–16. https://doi.org/10.1007/978-3-319-27192-7

[3] Film, T., & Technology, T. (2013). Thin Film Transistor Technology—Past, Present, and Future.

[4] Yamamoto, Y. (2012). Technological innovation of thin-film transistors: Technology development, history, and future. Japanese Journal of Applied Physics, 51(6 PART 1), 0–12. https://doi.org/10.1143/JJAP.51.060001

[5] Ahn, J. H., Kim, H. S., Lee, K. J., Zhu, Z., Menard, E., Nuzzo, R. G., & Rogers, J. A. (2006). High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates. IEEE Electron Device Letters, 27(6), 460–462. https://doi.org/10.1109/LED.2006.874764

[6] Fortunato, E., Barquinha, P., & Martins, R. (2012). Oxide semiconductor thin-film transistors: A review of recent advances. Advanced Materials, 24(22), 2945–2986. https://doi.org/10.1002/adma.201103228

[7] Lu, N., Jiang, W., Wu, Q., Geng, D., Li, L., & Liu, M. (2018). A Review for Compact Model of Thin-Film Transistors (TFTs). Micromachines, 9(11), 599. https://doi.org/10.3390/mi9110599

[8] Sharma, A., Madhu, C., & Singh, J. (2014). Performance Evaluation of Thin Film Transistors: History, Technology Development and Comparison: A Review. International Journal of Computer Applications, 89(15), 36–40. https://doi.org/10.5120/15710-4603

[9] A. Tripathi, S. Bharadwaj, M. B., & Banerjee, A. (2012). A Publication of the Society for Materials Chemistry, 3(1).

[10] Quevedo-Lopez, M. A., Wondmagegn, W. T., Alshareef, H. N., Ramirez-Bon, R., & Gnade, B. E. (2011). Thin Film Transistors for Flexible Electronics: Contacts, Dielectrics and Semiconductors. Journal of Nanoscience and Nanotechnology, 11(6), 5532–5538. https://doi.org/10.1166/jnn.2011.3425

[11] Plais, F., Huet, O., Legagneux, P., Pribat, D., Auberton-Herve, A. J., & Barge, T. (2002). Single crystalline silicon thin film transistors fabricated on Corning 7059, 170–171. https://doi.org/10.1109/soi.1995.526514

[12] Reiche, M., & Wagner, G. (2003, March). Wafer thinning techniques for ultra-thin wafers. Retrieved from https://electroiq.com/2003/03/wafer-thinning-techniques-for-ultra-thin-wafers/

[13] Zhou, S., Liu, C., Wang, X., Luo, X., & Liu, S. (2011). Integrated process for silicon wafer thinning. Proceedings - Electronic Components and Technology Conference, (May), 1811–1814. https://doi.org/10.1109/ECTC.2011.5898760

[14] Luo, J., & Dornfeld, D. A. (2001). Material removal mechanism in chemical mechanical polishing: Theory and modeling. IEEE Transactions on Semiconductor Manufacturing, 14(2), 112–133. https://doi.org/10.1109/66.920723

[15] Terrell, E. J., & Fred Higgs, C. (2007). Hydrodynamics of Slurry Flow in Chemical Mechanical Polishing. Journal of The Electrochemical Society, 153(6), K15. https://doi.org/10.1149/1.2188329

[16] Ipa, I., Sin, L., The, S. T. S. R. I. E., Rate, E., & Sin, L. (2005). Etching of Silicon. Electrochemistry of Silicon and Its Oxide, 1, 279–351. https://doi.org/10.1007/0-306-47921-4_7

[17] BYU Cleanroom. (n.d.). Retrieved from https://cleanroom.byu.edu/KOH

[18] Westra, K. (2010). KOH and TMAH Etching of Bulk Silicon Recipes , Tricks , What is Possible , and What is Impossible. I Can, (100), 1–3.

[19] Chen, P. H., Peng, H. Y., Hsieh, C. M., & Chyu, M. K. (2001). The characteristic behavior of TMAH water solution for anisotropic etching on both silicon substrate and SiO 2 layer. Sensors and Actuators, A: Physical, 93(2), 132–137. https://doi.org/10.1016/S0924-4247(01)00639-2

[20] Parasuraman S, S., Mr. (n.d.). Lecture 24: Doping. Lecture presented at MM5017: Electronic materials, devices, and fabrication.

[21] Laube, P. (n.d.). Wafer fabrication. Lecture.

[22] Celler, G. K., & Cristoloveanu, S. (2003). Frontiers of silicon-on-insulator. Journal of Applied Physics, 93(9), 4955–4978. https://doi.org/10.1063/1.1558223

[23] Menard, E., Lee, K. J., Khang, D.-Y., Nuzzo, R. G., & Rogers, J. A. (2004). A printable form of silicon for high performance thin film transistors on plastic substrates. Applied Physics Letters, 84(26), 5398–5400. https://doi.org/10.1063/1.1767591

[24] Zhu, Z. T., Menard, E., Hurley, K., Nuzzo, R. G., & Rogers, J. A. (2005). Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates. Applied Physics Letters, 86(13), 1–3. https://doi.org/10.1063/1.1894611

[25]Sun, L., Qin, G., Seo, J. H., Celler, G. K., Zhou, W., & Ma, Z. (2010). 12-GHz thin-film transistors on transferrable silicon nanomembranes for high-performance

flexible electronics. Small, 6(22), 2553–2557. https://doi.org/10.1002/smll.201000522

[26] Zhang, K., Seo, J. H., Zhou, W., & Ma, Z. (2012). Fast flexible electronics using transferrable silicon nanomembranes. Journal of Physics D: Applied Physics, 45(14). https://doi.org/10.1088/0022-3727/45/14/143001

[27] Qin, G., Seo, J. H., Zhang, Y., Zhou, H., Zhou, W., Wang, Y., … Ma, Z. (2013). RF characterization of gigahertz flexible silicon thin-film transistor on plastic substrates under bending conditions. IEEE Electron Device Letters, 34(2), 262–264. https://doi.org/10.1109/LED.2012.2231853

[28] Diab, A., Torres Sevilla, G. A., Ghoneim, M. T., & Hussain, M. M. (2014). High temperature study of flexible silicon-on-insulator fin field-effect transistors. Applied Physics Letters, 105(13), 10–14. https://doi.org/10.1063/1.4897148

[29] Sevilla, G. T., Rojas, J. P., Ahmed, S., Hussain, A., Inayat, S. Bin, & Hussain, M. M. (2013). SILICON FABRIC FOR MULTI-FUNCTIONAL APPLICATIONS Integrated Nanotechnology Lab , King Abdullah University of Science and Technology , Saudi Arabia. 2013 Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, (June), 2636–2639.

[30] H.E.Weste, N., & Harris, D. M. (2010). MOS Transistor Theory. CMOS VLSI Design: A Circuits and Systems Perspective, 67–85. Retrieved from https://www.academia.edu/17649248/CMOS-VLSI-design_A_circuits_and_Systems_Perspective

[31] Poster, O., & Silicon, C. (2012). Wet-Chemical Etching of Silicon, 11–13.

[32] MicroChemicals. (n.d.). Wet-Chemical Etching of Silicon and SiO2, (100). Retrieved from www.microchemicals.com/downloads/application_notes.html%0Ahttps://www.microchemicals.eu/technical_information/silicon_etching.pdf

[33] Yu, A. Y. C. (1970). Electron tunneling and contact resistance of metal-silicon contact barriers. Solid State Electronics, 13(2), 239–247. https://doi.org/10.1016/0038-1101(70)90056-0

[34] Mathiot, D., Lachiq, A., Slaoui, A., Noël, S., Muller, J. C., & Dubois, C. (1998). Phosphorus diffusion from a spin-on doped glass (SOD) source during rapid thermal annealing. Materials Science in Semiconductor Processing, 1(3–4), 231–236. https://doi.org/10.1016/S1369-8001(98)00045-6

[35] Hoarfrost, M. L., Takei, K., Ho, V., Heitsch, A., Trefonas, P., Javey, A., & Segalman, R. A. (2013). Spin-on organic polymer dopants for silicon. Journal of Physical Chemistry Letters, 4(21), 3741–3746. https://doi.org/10.1021/jz4019095

[36] Martinez, J., Moreno, M., Rosales, P., Torres, A., Ambrosio, R., & Murias, D. (2017). Study of the spin on dopant technique as alternative for the fabrication of c-Si solar cells. 2017 IEEE 44th Photovoltaic Specialist Conference, PVSC 2017, 1–4. https://doi.org/10.1109/PVSC.2017.8366574

[37] Giustino, F. (2004). Dielectric effect of a thin SiO2 interlayer at the interface between silicon and high-k oxides. Microelectronic Engineering, 72(1-4), 299–303. doi: 10.1016/j.mee.2004.01.011

[38] Leach, W. M. (2019, August). Ece3050-Analog Electronics Georgia Institute of Technology. Ece3050-Analog Electronics Georgia Institute of Technology. Retrieved from https://leachlegacy.ece.gatech.edu/ece3050/notes/mosfet/mosfet2Rev.pdf