PERFORMANCE AND THERMAL RELIABILITY COMPARISONS OF 2-LEVEL AND 3-LEVEL NPC VOLTAGE SOURCE INVERTERS FOR ELECTRIC VEHICLE DRIVE APPLICATIONS

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ABSTRACT

PERFORMANCE AND THERMAL RELIABILITY COMPARISONS OF 2-LEVEL AND 3-LEVEL NPC VOLTAGE SOURCE INVERTERS FOR ELECTRIC VEHICLE DRIVE APPLICATIONS

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Two-level and multilevel inverters are widely used in electric vehicle drive applications with different switching techniques. Selection of the topology and the switching technique for electric vehicle drives are getting more important with the trend of designing more compact and more efficient drive circuitry. Reliability of semiconductors in power electronics are under investigation in recent years as well. In this thesis, a multidimensional comparison of two common topologies for a 120 kW electric vehicle PMSM (Permanent Magnet Synchronous Machine) drive system is conducted. Two-level topology and three-level NPC (Neutral Point Clamped) type voltage source inverters are compared in terms of output voltage and current quality, thermal performance, efficiency, switching frequency limitation and semiconductor thermal reliability aspects. Also SPWM (Sinusoidal Pulse Width Modulation) and SVPWM (Space Vector Pulse Width Modulation) techniques are under investigation.

Keywords: Two-level Voltage Source Inverter, Three-Level NPC Type Voltage Source

Inverter, Semiconductor Thermal Reliability, Electric Vehicle Traction System, Thermal Analysis

ÖZ

ELEKTRİKLİ ARAÇ MOTOR SÜRÜCÜ UYGULAMALARI İÇİN 2-DÜZEY VE 3-DÜZEY NÖTR KENETLEMELİ GERİLİM BESLEMELİ EVİRİCİLERİN PERFORMANS VE ISIL GÜVENİLİRLİK AÇISINDAN KARŞILAŞTIRILMASI

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Farklı anahtarlama tekniklerine sahip iki seviyeli ve çok seviyeli eviriciler, elektrikli araç tahrik uygulamalarında yaygın olarak kullanılmaktadırlar. Elektrikli araç motor sürücü sistemleri için topoloji seçimi ve anahtarlama teknikleri, daha kompakt ve daha verimli tahrik devreleri tasarlama eğilimiyle daha da önem kazanmaktadır. Yarı iletkenlerin güç elektroniğinde ısıl güvenilirliği de son yıllarda incelenmektedir. Bu tez çalışmasında, elektrikli araçlarda kullanılacak 120 kW sabit mıknatıslı senkron motor sürücü devresi için iki yaygın topolojinin çok boyutlu bir karşılaştırması yapılmaktadır. İki seviyeli topoloji ve üç seviyeli nötr nokta kenetli tip gerilim beslemeli evirici çıkış gerilim ve akım kalitesi, ısıl performans, verimlilik, anahtarlama frekansı sınırlaması ve yarı iletken ısıl güvenilirliği açısından karşılaştırılmıştır. Ayrıca sinüzoidal darbe genişliği modülasyonu ve uzay vektör darbe genişliği modülasyonu teknikleri incelenmektedir.

Anahtar Kelimeler: İki Seviyeli Gerilim Beslemeli Evirici, Üç Seviyeli Nötr Nokta Kenetli Gerilim Beslemeli Evirici, Yarıiletken Isıl Güvenilirliği, Elektrikli Araç Çekiş Sistemi, Isıl Analiz

To my family

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LIST OF ABBREVIATIONS

ABBREVIATIONS

APOD	Alternative Phase Opposition Disposition
BEV	Battery Electric Vehicle
CMC	Common Mode Current
CMV	Common Mode Voltage
CTE	Coefficient of Thermal Expansion
GaNFet	Gallium Nitride Field Effect Transistor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NEDC	New European Drive Cycle
NPC	Nuetral Point Clamped
PD	Phase Disposition
PMSM	Permanent Magnet Synchronous Motor
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
RMS	Root Mean Square
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
VSI	Voltage Source Inverter

WLTP	World Harmonized Light Vehicle Test Procedure

CHAPTER 1

INTRODUCTION

Hybrid electric vehicles, battery electric vehicles and fuel cell electric vehicles have been gaining popularity in recent times. There are many reasons behind this fact. One of them is environmental concerns. In 2009, 25% of the green house gas (GHG) emission was due to transportation sector [5]. Climate change and global warming have been reached a threatening level due to GHG emissions. In [6], it is stated that GHG emmission would be doubled if necessary precautions are not taken. Regarding this issue, integration of electric vehicles (EVs) into the transportation sector would decrease our dependency on fossil fuel based energy sources. EVs use more efficient power trains compared with internal combustion engine vehicles [7]. Also, EVs are able to improve energy security by diversifying energy sources. Especially, integration of EVs to the renewable energy sources are highly promising in order to picture a better near future. Besides, electric mobility will enable us to reshape and restructure our transportation.

Electric drive systems are one of the most important key components in an EV. Therefore, design of more compact, more efficient and more reliable electric drive systems is crucial. This thesis aims to contribute literature by investigating motor drive inverter of battery electric vehicle (BEV) in terms of getting more efficient and more reliable designs.

Two-level voltage source inverters (VSI) are the commercial converter type used in PMSM drives. As semiconductor switches, conventional Si IGBT and diode pairs are used for driving PMSMs in traction applications. However, in recent years, SiC MOSFETs and SiC diodes have been involved in the motor drive market to account for the need in higher switching frequency modulation [8]. As stated in [9], switch-

ing frequency should be at least 9-12 times of the maximum fundamental frequency. However, conventional Si IGBT diode pairs suffer from high switching losses in two-level VSI topology. SiC MOSFET and Si based IGBT diode pair comparison is done for an 80 kW PMSM drive in [8]. Usage of SiC MOSFETs instead of Si IGBT results with 5 percent loss decrease in motor drive. SiC MOSFETs are now preferable with two-level topology due to their lower switching losses, which enables system operation at higher switching frequencies.

Three-level NPC topology is expected to be used at higher switching frequency operations with conventional Si IGBT diode pairs due to lower switching losses. The reasons are as follows: First, blocking voltage requirement of the main switch is halved in three-level topology. Second, switching losses do not linearly change with blocking voltage. An exponent of 1.3, 1.4 is used to calculate even in the same IGBT device [4]. That means switching losses are expected to drop below 50 percent in a 3-level topology, giving us the opportunity for increasing the switching frequency.

In the literature, advantages of three-level inverter over two-level inverter are discussed for PMSM drive applications. Three-level NPC and two-level topologies are compared in terms of output voltage THD, efficiency, and fault tolerance in [10] and in all aspects, three-level NPC topology found to have a superior performance. Similarly, three-level NPC topology is shown to be more compatible with PMSM drives in vehicle traction in terms of current THD, torque ripple, and lower switching losses aspects in [11]. Cost comparison between two-level and three-level topologies is done in [9], where it is shown that three-level NPC topology has a slightly higher initial cost. On the other hand, three-level topology results with a lower operational cost due to its higher efficiency. Although superior performance stated in the literature, manipulation of higher number of switches and floating capacitor balancing are main design challenges of the three-level NPC topology.

Considering the increase in DC bus voltage levels, topology selection is also getting as important as switch selection. Commercially available semiconductor switches have discrete steps of blocking voltage levels. In DC bus voltage levels around 700-900 V, switches with 1200 V voltage blocking capability are required in 2-level VSIs. At this point, semiconductor technologies with lower switching losses are the choice

of the developers. On the other hand, a multi-level VSI may provide solution with conventional semiconductor switches thanks to lower turn-on and turn-off energies compared to two-level topologies.

1.1 Scope of the Thesis

The most commonly used three-phase voltage source inverter topologies that are two-level and three-level NPC type VSIs and switching techniques that are sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) are implemented and examined with the help of numeric analyses. Moreover, a small scale three-level NPC type inverter is implemented and hardware design steps as well as challenges in designing a three-level inverter are addressed.

Results of multidimensional comparisons of the topologies and the switching techniques that are mentioned above in terms of output quality, thermal performance and switching frequency limitations are provided for a 120 kW EV traction system.

Finally, two VSI topolgies are compared in terms of semiconductor thermal reliability point of view under two mission profiles representing two driver characteristics including the driver behavior in lifetime estimation is a novel contribution to the field.

The analyses presented in this study can be summarized as follows:

i. Studying basic principles of two-level and three-level NPC VSI topologies
ii. Building and testing a three-level NPC type inverter.
iii. Analyzing both topologies by means of electrical and thermal characteristics for an electric vehicle drive application
iv. Studying semiconductor losses and thermal modelling of selected topologies
v. Studying methodologies to estimate lifetime of topologies considering thermal reliability of semiconductors

1.2 Thesis Outline

Chapter 2 gives a brief information on trends in both electric machines and voltage source inverter topologies for electric vehicle drive applications. This chapter also includes a general literature review on the performance and reliability improvement of VSIs.

In Chapter 3, fundamentals of the selected VSI topologies and common modulation techniques are explained in details. Also, design steps of a 750 W three-level NPC type topology are discussed. Test results under different load conditions are presented.

In Chapter 4, semiconductor losses of VSIs with Si IGBTs and Si diodes are analyzed. For two-level and three-level NPC type topologies, losses of IGBTs and diodes are analyzed and mathematical approaches to calculate semiconductor losses are given. Additionally, the most common thermal models are explained with the help of electrical and thermal analogies.

In Chapter 5, electric drive system simulation models are constructed with two-level and three-level NPC type topologies. By the help of electro-thermal simulations, a multidimensional comparison of topologies for the same electric drive application is conducted. Semiconductor loss calculations defined in Chapter 4 are used in the electro-thermal simulations.

In Chapter 6, semiconductor thermal reliability fundamentals are discussed and the reasons of semiconductor failures due to thermal stresses are described briefly. Moreover, lifetime estimation methodology of a power semiconductor and flow-chart of lifetime estimation are explained in details. Semiconductor losses methodology defined in Chapter 4 is used to observe thermal stresses of semiconductors. Finally, VSI topologies are compared in terms of their estimated lifetimes for two different mission profiles.

In Chapter 7, a general conclusion is given and suggestions for future studies are included.

CHAPTER 2

STATE OF ART ELECTRIC DRIVES IN VEHICLE TRACTION APPLICATIONS

2.1 Electric Drive Technologies

Electric vehicles have been significantly improved in last decade. At first, hybrid and plug-in hybrid cars have been introduced besides conventional gasoline-based models. These improvements have been followed by battery electric vehicle (BEV) models. In the state of art, there are BEVs in the market with a range of more than 300 miles [12].

Power converters of electric vehicles have to comply with strict requirements because of space and weight limitations. Every part of electrical and mechanical system needs to be designed as compact and light as possible. A lighter weight results in reduced load, so faster acceleration and higher efficiency.

A review of commercial electric vehicle drive systems including electric machine and power electronics is given in [13]. Table 2.1 shows electric drive train of electrified vehicles that have a high market share. The values in the paranthesis represent only the inverter that is boost converters are excluded. In [1], it is stated that power density expectation of an electric vehicle system increases rapidly. Acording to US Department of Energy (DOE), 33 kW/L for a 100 kW traction drive system is estimated by 2025. It is an increment by a factor of 5.5 compared to the state of art. It can be inferred that in the near future electric vehicle drive systems will be much compacter than the today's commercial products.

Table 2.1: Motor drive performances of commercial products [1]

Parameter	2004 Prius (50 kW)	2007 Camry (70 kW)	2008 Lexus (110 kW)	2010 Prius (60 kW)	2012 Leaf (80 kW)	2014 Accord (124 kW)	2016 BMW i3 (125 kW)	2017 Prius (53 kW)
Motor								
Peak power density (kW/L)	3.3	5.9	6.6	4.8	4.2	8.5	9.1	5.7
Peak specific power (kW/kg)	1.1	1.7	2.5	1.6	1.4	2.9	3.0	1.7
Inverter								
Peak power density (kW/L)	4.5 (7.4)	7.4 (11.7)	10.6 (17.2)	5.9 (11.1)	5.7	12.1 (18.5)	18.5	11.5 (21.7)
Peak specific power (kW/kg)	3.8 (6.2)	5.0 (9.3)	7.7 (14.9)	6.9 (16.7)	4.9	9.1 (21.7)	14.1	8.6 (19.0)
Specifications								
DC Voltage	500	650	650	650	375	700	355	600
Current (Arms)	225	282	304	170	442	300	375	160
Number of IGBT	12	18	12	12	18	12	24	6
Total IGBT Si area (mm^2)	1582.8	2165	1959.6	1312	4050	2213	2382	958

In [1], it is also stated that DC bus voltage should be increased in order to achieve higher speeds and more compact designs as well. Increase in DC bus voltage allows designer to reach up higher speeds and result in more compact designs. It can be inferred from [14] that increase in DC bus voltage from 500 to 600/650 V level has a significant effect on the increase of motor speed of Toyota Prius from 6000 rpm to 17000 rpm. Higher DC bus results in lower losses at the inverter side and enables the design of more compact electric drive systems. This is important because another trend in electric motors and drive systems is to increase speed of the motor. In [15], benchmarking of different commercial electric vehicle products are represented. Accordingly, speed rating of the motors varies between 6000 rpm to 14000 rpm.

As cooling technologies, natural cooling with heatsink, forced air cooling and liquid cooling are the most common methodologies in power electronics. For lower power electronics circuitry, natural cooling is widely used with bulky heatsinks. In order to design more compact power converters, forced air cooling could be used to shrink power converter size. On the other hand, in electric vehicle applications, liquid cooling is the most common method. In [15], cooling system of the commercial electric vehicles drive systems are explained. Most of them use heatsink with water-glycol loop as cooling system. Liquid cooling allows more compact design, in terms of volume by sacrificing cost effectiveness.

A general overview of voltage source inverter topologies is given in next section. On the other hand, state of art voltage source inverter for electric vehicle applications is conventional two-level topology due to its simplicity, robustness and easy controllability. Also, conventional Si IGBT and diode pairs are used as power semiconductor switches [1]. In two-level topology, high dV/dt is observed at the switch node of each phase due to swing between 0 and V_{dc}. In order to achieve lower dV/dt at the output and achieve higher efficiency, three-level NPC topology could be a good candidate for near future commercial products.

2.2 Voltage Source Inverter Topologies and Applications

Three-phase voltage source converters can be divided into two main groups. The first one is two-level voltage source converters that are widely used in industry in many applications due to their simplicity and control ease. On the other hand, another major topology group is called multilevel inverters. Multilevel inverters consist of an array of semiconductors and capacitors, which generate output voltage with stepped waveforms. The need to use of multilevel inverters is due to high DC bus voltage levels of medium voltage grid. Power semiconductor blocking voltage specifications are not able to match with DC bus voltage level especially in AC drives of MW ranges. Due to these reasons, multilevel inverters emerged. Level of an inverter is determined by checking the number of possible voltage steps at the switch node of its legs. Basic models of two-level, three-level and multilevel inverters is shown in Figure 2.1.

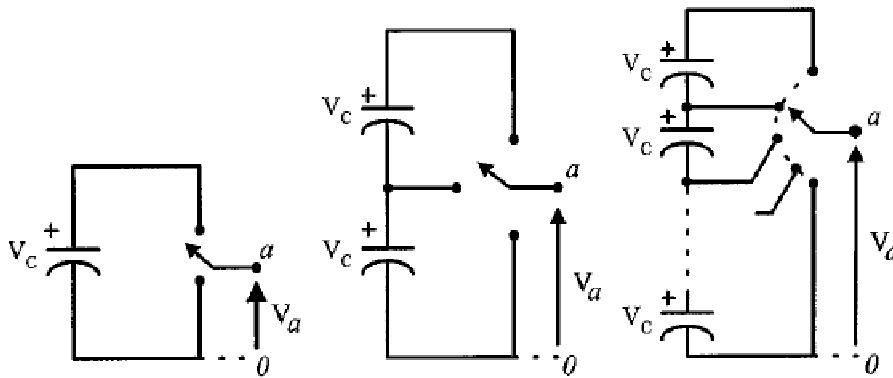


Figure 2.1: One phase leg of inverter with two-level, three-level and n-level node voltages [2]

Voltage source inverters are widely used in high voltage direct current (HVDC) transmission systems, medium-voltage motor drive systems, static compensator (STATCOM) applications, electric traction systems and grid connected energy storage systems. Conventional two-level and three-level topologies are still widely used in most of these applications. On the other hand, multilevel topologies are used for some of the applications above when there are high power, high reliability and high efficiency constraints. Also modular multilevel converters (MMCs) which consist of sub-modules instead of one semiconductor are widely used in the high power appli-

cations as well. In this thesis, only two-level and three-level NPC type converters are investigated. In Chapter 3, detailed information on the selected inverter topologies are given. Information on different multilevel topologies and specific application areas can be found in [16] and [2].

2.3 Modulation Techniques

There are various pulse width modulation (PWM) techniques used to manipulate semiconductors in voltage source inverters. In two-level topology, the most common methods are sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM) and hysteresis current controller based PWM. The first two techniques are discussed in Chapter 3 in details. On the other hand, various modulation techniques can be implemented in multi-level inverters. These switching techniques can be categorized into two main groups as low frequency switching and high frequency switching as shown in Figure 2.2.

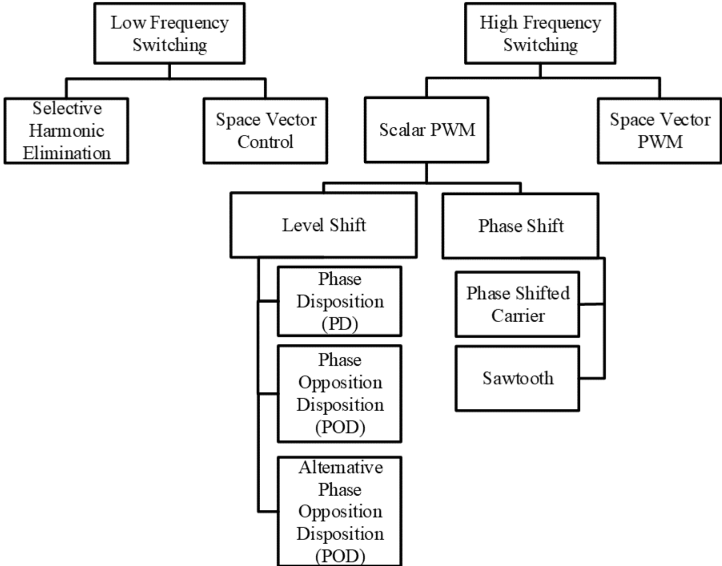


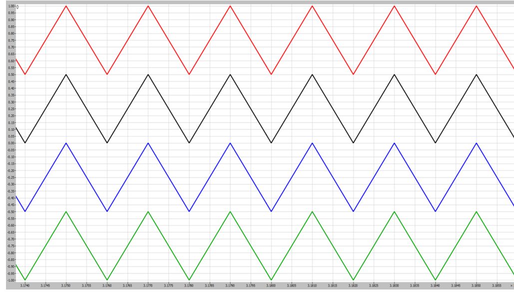
Figure 2.2: Switching techniques for multilevel inverters [3]

In low frequency switching, the first method is selective harmonic elimination in which switching angles are pre-calculated such that desired harmonic component at the output is cancelled. The methodology is explained in details in [17] and [18]. Second low frequency techinque is space vector control method. Space vector control method

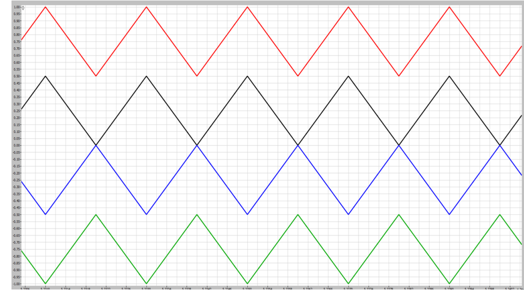
aims to generate output voltage with minimum error with respect to the reference vector. In SVPWM technique, the aim is to generate exactly the same mean voltage of the reference vector at the output. In space vector control method, the aim is just to minimize error between the reference vector and the output voltage. Space vector control method is detailly explained in [3]. Low frequency switching methods decrease switching losses significantly. On the other hand, they have a bad dynamic response.

High switching frequency techniques consist of space vector pulse width modulation (SVPWM) and sinusoidal pulse width modulation (SPWM) techniques. Application of these modulation methods for two-level and three-level NPC type topology are explained in Chapter 3. In SPWM, gate signals are generated by comparing a reference sine wave having fundamental output frequency and carrier signal having switching frequency.

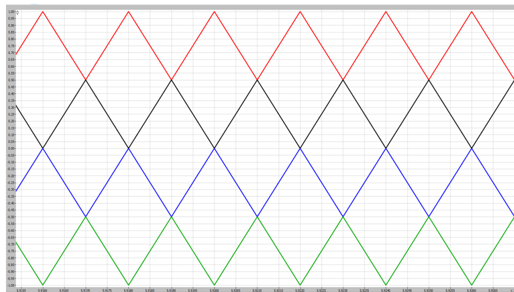
SPWM techniques for MMCs differ by means of carrier signals. Carrier signals of a five-level inverter topology with phase disposition, phase opposition disposition, alternative phase opposition disposition, phase shifted carriers and sawtooth rotation methods are given in Figure 2.3. SVPWM and SPWM with phase disposition method are selected for analyses in the thesis. Selected topologies and switching techniques are detailly explained in the following two chapters.



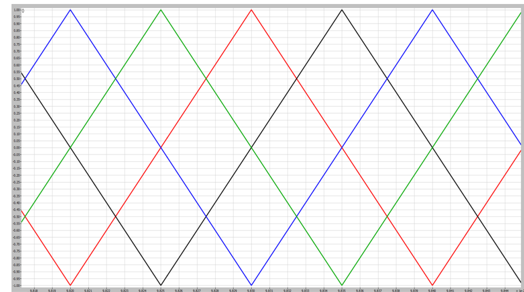
(a) Phase disposition carrier signals



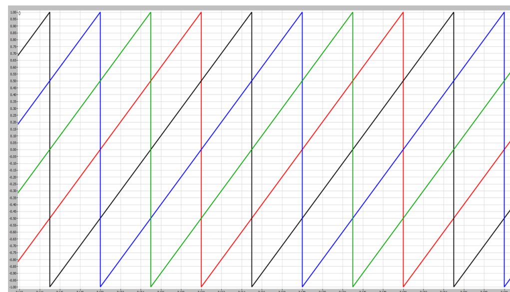
(b) Phase opposition disposition carrier signals



(c) Alternative phase disposition carrier signals



(d) Phase shifted carrier signals



(e) Sawtooth rotation method

Figure 2.3: Scalar PWM carrier signals of a 5-level VSI

CHAPTER 3

TWO LEVEL AND THREE LEVEL NPC TYPE VOLTAGE SOURCE INVERTERS

There are various techniques to generate AC voltage at the output of switch nodes. Sinusoidal PWM, Space Vector PWM, hysteresis controller etc. In this thesis, SPWM and SVPWM methods are considered for two-level and three-level NPC type voltage source inverter topologies since they are the most commonly applied PWM methods.

3.1 Two-level Voltage Source Inverter

A two-level three-phase voltage source inverter is shown in Figure 3.1.

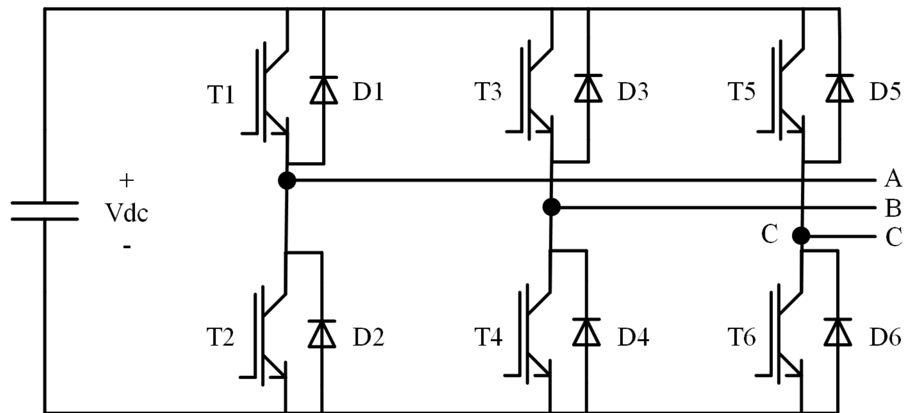


Figure 3.1: Two-level topology

This topology consists of 6 bi-directional switches. Depending on the current and voltage rating of the converter, Si MOSFETs, SiC MOSFETs, GaNFETs and IGBT-diode pairs can be used as main bi-directional switches in two-level inverters. Among them, IGBT-diode pairs are widely used in electric vehicle drive applications. Two

switches in one leg of inverter work complementarily in two-level topology in order to avoid short circuit of DC bus. Thus, Each semiconductor in the topology should block V_{dc} voltage when they are in off state.

3.1.1 Modulation Techniques

SPWM

In SPWM modulated two-level three phase inverter, three reference sine waves 120° shifted wrt. each other are used as reference for each phase. Freuqency of reference sine waves are the same as output frequency. By comparing reference sine waves with the carrier triangle waveforms, gate signals are obtained for upper and lower switches of each leg. Frequency of the carrier signal determines the switching frequency. Carrier signal, three reference signals and node voltages of each leg with respect to DC bus ground are given in Figure 3.2. In the figure, exampilary 50 Hz reference signals and 1 kHz carrier signal are shown.

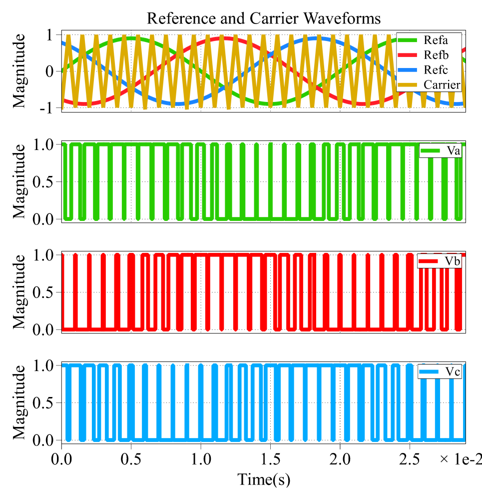


Figure 3.2: Reference and carrier waveforms for two-level SPWM

SVPWM

Space Vector PWM (SVPWM) technique is widely used in many inverter applications. The main advantage of SVPWM is the degree of freedom to place vectors in a

switching period compared with SPWM method. SVPWM also provides a better DC bus utilization. So, due to better DC bus utilization, voltage level of DC bus can be reduced. For two-level inverter topology, 61.2% DC bus utilization can be achieved with SPWM and 70.7% with SVPWM. DC bus utilization corresponds to percent of the ratio between line-line rms voltage at the output of inverter and DC bus voltage value. However; SVPWM technique needs higher computational power due to its nature. In recent years, microcontrollers and DSPs allow designers to implement SVPWM algorithms easily.

SVPWM technique is based on selection of the optimum switching state of the inverter in each switching period. In order to achieve this purpose, three phase reference signals are transformed to $\alpha - \beta$ axis by applying Clarke's transformation using (3.1). Each switching state corresponds to a voltage vector on $\alpha - \beta$ plane and the created vector is called space vector. This vector is created as a combination of $2^3 = 8$ voltage vectors in two-level three-phase topology. Two of them are zero vectors that are represented by 000 and 111 vectors. Space vectors and their switch logic signals are given in Table 3.1.

Table 3.1: Switch logic for corresponding space vectors

		T1,T3,T5			T2,T4,T6		
Vectors		T1	T3	T5	T2	T4	T6
V_0	000	1	1	1	0	0	0
V_1	100	0	1	1	1	0	0
V_2	110	0	0	1	1	1	0
V_3	010	1	0	1	0	1	0
V_4	011	1	0	0	0	1	1
V_5	001	1	1	0	0	0	1
V_6	101	0	1	0	1	0	1
V_7	111	0	0	0	1	1	1

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.1}$$

Then reference vector V_r is defined as in (3.2).

$$\vec{V_r} = V_\alpha + jV_\beta \tag{3.2}$$

In SVPWM algorithm, amplitude $\vec{V_r}$ and phase α of the reference vector is required. These quantities are determined as in (3.3) and (3.4).

$$\mid V_r \mid = \sqrt{V_\alpha^2 + V_\beta^2} \tag{3.3}$$

$$\alpha = tan^{-1}(\frac{V_\beta}{V_\alpha}) \tag{3.4}$$

With magnitude and phase calculation, sector determination is done as in Table 3.2. These vectors are shown in Figure 3.3. It should be noted that zero vectors are equally shared in terms of time.

Table 3.2: Regions and positions of reference vector

Sector	Position of V_r
1	$0^o < \omega t < 60^o$
2	$60^o < \omega t < 120^o$
3	$120^o < \omega t < 180^o$
4	$180^o < \omega t < 240^o$
5	$240^o < \omega t < 300^o$
6	$300^o < \omega t < 360^o$

After this magnitude and phase calculation, the space vectors and their on-times must be calculated. In order to calculate on times for each vector, volt-seconds law is applied as in 3.5. On time calculation of vectors in sector 1 can be done using (3.5) and (3.6). T_s corresponds to switching period, T_0 corresponds to application time of V_0 , T_1 corresponds to application time of V_1 and T_2 corresponds to application time of V_2. Sum of T_0, T_1 and T_2 is equal to switching period T_s. m_a is modulation index defined as in 3.7 in order to simply mathematical formulation for on time calculations.

$$\int_0^{T_s} \vec{V_r} = \int_0^{T_1} \vec{V_1} dt + \int_0^{T_2} \vec{V_2} dt + \int_0^{T_0} \vec{V_0} dt \tag{3.5}$$

$$\vec{V_r} = |V_r| e^{j\alpha}, \vec{V_0} = 0, \vec{V_1} = \frac{2}{3}, \vec{V_2} = \frac{2}{3} e^{\frac{j\pi}{3}} \tag{3.6}$$

$$m_a = \frac{3V_r}{2V_{dc}} \tag{3.7}$$

On time durations of space vectors in all six sectors are given in Table 3.3 as a function of switching period T_s, modulation index m_a and phase of reference vector α. Finally, switching patterns in each sector are given in Figure 3.4 .

Table 3.3: Calculated times and regions in two-level topology

Sector	T_1	T_2	T_0
1	$T_s m_a sin(\frac{\pi}{3} - \alpha)$	$T_s m_a sin(\alpha)$	$T_s - T_1 - T_2$
2	$T_s m_a sin(\frac{2\pi}{3} - \alpha)$	$T_s m_a sin(\alpha - \frac{\pi}{3})$	$T_s - T_1 - T_2$
3	$T_s m_a sin(\pi - \alpha)$	$T_s m_a sin(\alpha - \frac{2\pi}{3})$	$T_s - T_1 - T_2$
4	$T_s m_a sin(\frac{4\pi}{3} - \alpha)$	$T_s m_a sin(\alpha - \pi)$	$T_s - T_1 - T_2$
5	$T_s m_a sin(\frac{5\pi}{3} - \alpha)$	$T_s m_a sin(\alpha - \frac{4\pi}{3})$	$T_s - T_1 - T_2$
6	$T_s m_a sin(2\pi - \alpha)$	$T_s m_a sin(\alpha - \frac{5\pi}{3})$	$T_s - T_1 - T_2$

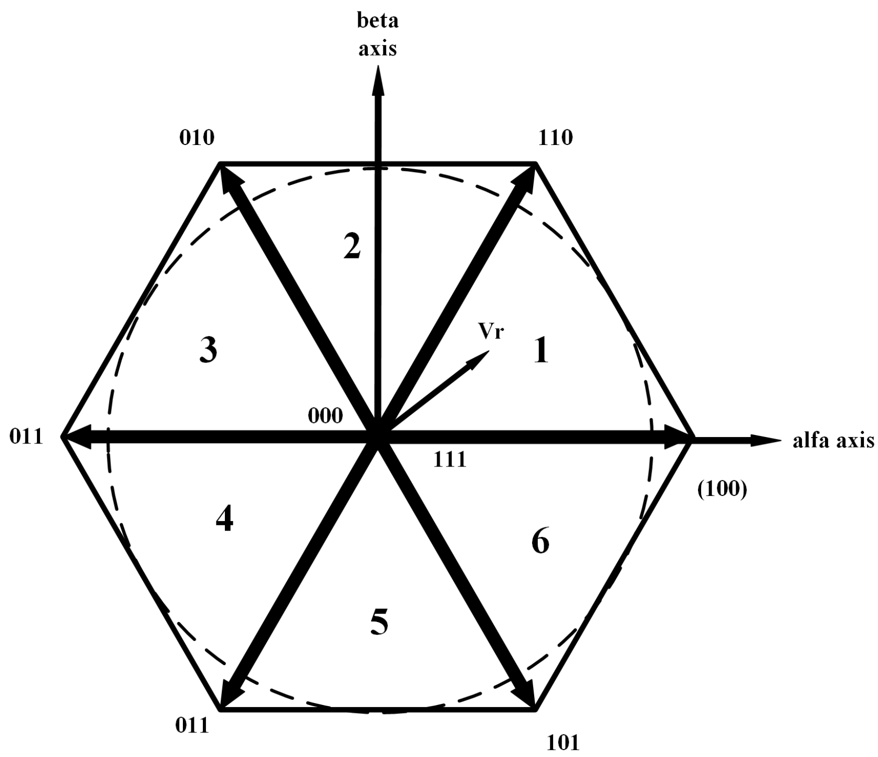


Figure 3.3: Two-level space vectors

(a) Sector 1

(b) Sector 2

(c) Sector 3

(d) Sector 4

(e) Sector 5

(f) Sector 6

Figure 3.4: Switching patterns and on times for each region

3.2 Three-level NPC Type Voltage Source Inverter

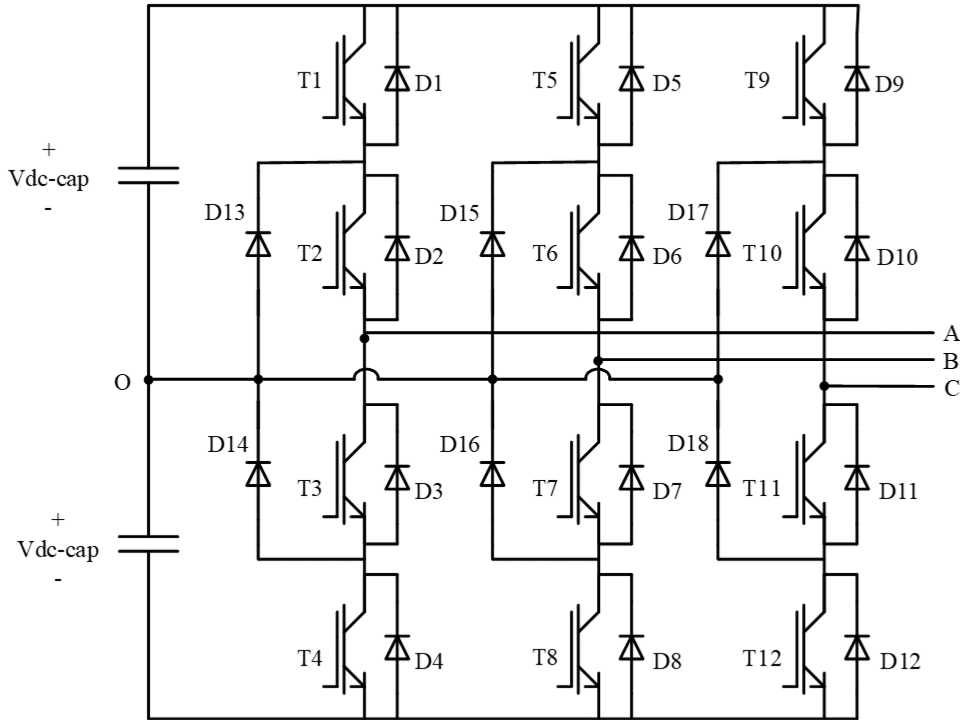


Figure 3.5: Three-level NPC topology

Three-Level NPC type inverter topology was firstly introduced in [19] in 1981. After that the topology is widely used in industry along with T-type three-level inverter topology and two-level topology. In the literature, there are various studies on T-type topology as well. On the other hand, in [20] it is shown that NPC topology can work under higher switching frequencies compared with T-type topology in three-level applications due to its lower losses. Since higher switching frequencies are aimed in this thesis, three-level NPC type topology is selected. In NPC type three-level inverter topology, each leg has four bi-directional switches and two zero potential clamping diodes as shown in Figure 3.5. It should be noted that V_{dc}=2V_{dc-cap}. Diodes are used to clamp different voltage states in each leg. Three different voltage levels that can be obtained in the first leg and corresponding switching patterns are given in Table 3.4.

Table 3.4: Switch pattern and node voltage in one leg

Vout	T1	T2	T3	T4
$0.5V_{dc}$	1	1	0	0
0	0	1	1	0
$-0.5V_{dc}$	0	0	1	1

3.2.1 Modulation Techniques

In modular multilevel converters (MMCs), various switching techniques were studied in the literature. These methods are not only available for three-level NPC type converter , but also applicable for other multilevel converter topologies. A general switching technique review is given in [21] for MMCs. In this study, in order to make a multidimensional comparison, two switching techniques are selected. The first one is SPWM technique with phase disposition method. The second one is SVPWM method by aiming a lower THD at the output current.

SPWM

There are various ways to apply SPWM in three-level topology which were briefly explained in Chapter 2. In this study, SPWM is applied with two different carrier waveforms separated by a DC offset from each other that is called phase disposition method. Carrier waveforms and reference waveforms are shown in Figure 3.6. Phase B and C legs have shifted reference sine waves by 120° wrt. each other. carrier1 is used for upper top switches of each leg (T1, T5, T9). carrier2 is responsible for lower switches (T2, T6, T10). Bottom two switches in each leg works complementarily with top side corresponding switch. For example T_1 and T_3 are complementary switches.

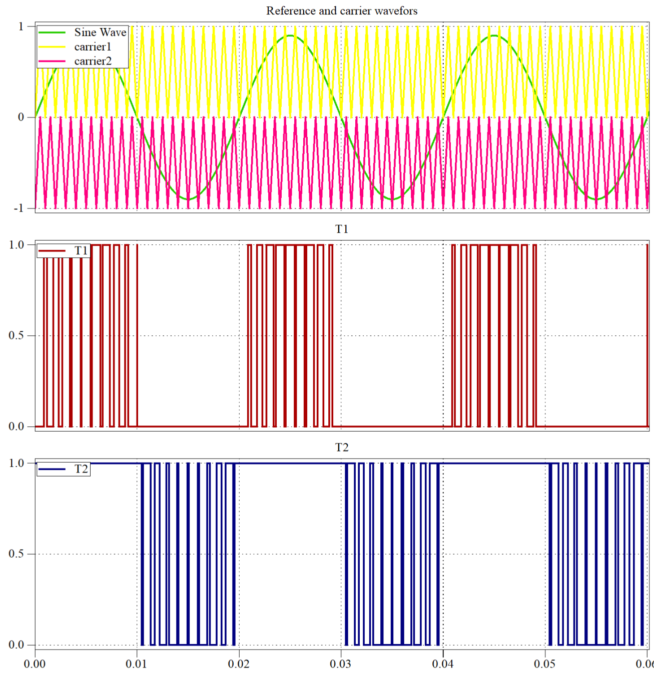


Figure 3.6: Three-level SPWM phase A switching signals

SVPWM

In three level topology there are in total of $3^3 = 27$ space vectors. 24 of them are active vectors from which 12 are short vectors, 6 are medium vectors and 6 are long vectors. Other 3 vectors are zero vectors located in the center. In three level inverter, six main sectors are the same as in two-level case and each sector consists of four sub-sectors. Figure 3.7 and 3.8 show space vectors and four sub-sectors in three level inverter, respectively. Sub-sector representation in Figure 3.8 represents first main sector as in two-level inverter where $0^o < \alpha < 60^o$. Due to the additional degree of freedom, there are many strategies to manage space vectors to generate PWM signals. In this study, symmetrical SVPWM method that is commonly used to achieve a low current THD at the output is used [22]. V_{dc-cap} is defined as voltage of one of the floating capacitors as can be seen in Figure 3.5. Each connection point can attain three different voltage levels in a 3-level VSI; P represents $0.5V_{dc}$, O represents zero potential and N represents -$0.5V_{dc}$ at the switching node of a phase leg as listed in Table 3.5.

Small vectors (POO, ONN, etc.) have magnitude of $V_{dc}/3$. Medium vectors (PON,

Table 3.5: Symbols, corresponding switch states and phase voltages

Symbol	T1	T2	T3	T4	Voltage
P	1	1	0	0	$0.5V_{dc}$
O	0	1	1	0	0
N	0	0	1	1	$-0.5V_{dc}$

OPN, etc.) have magnitude of $(\sqrt{3}/3)V_{dc}$. Large vectors (PNN, PPN, etc..) have magnitude of $2V_{dc}/3$.

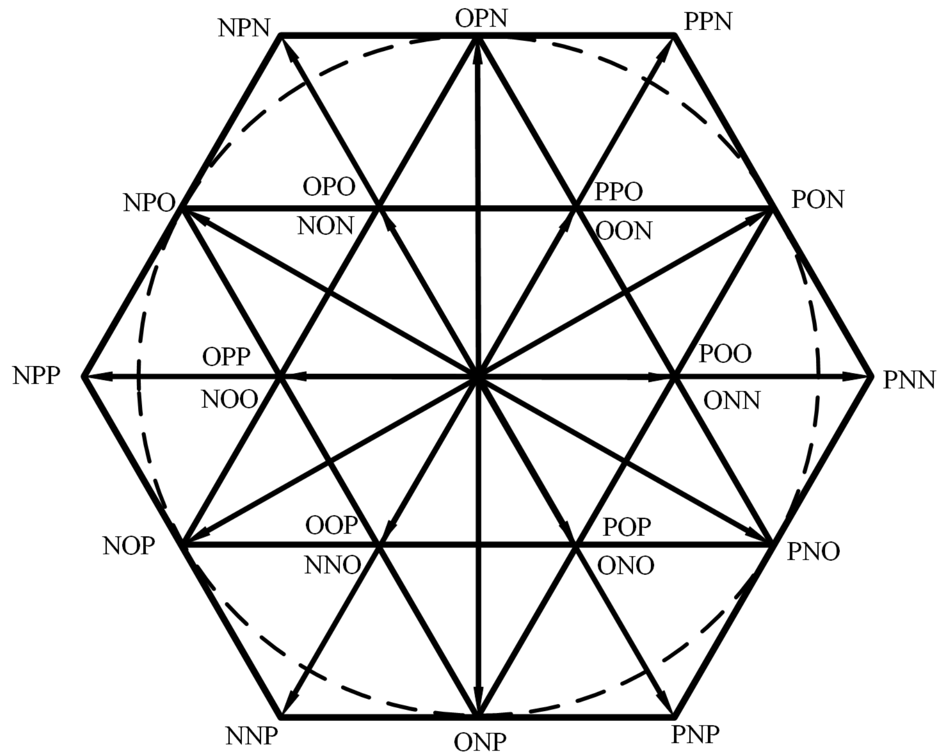


Figure 3.7: Three-level space vectors

Main sector detection is done the same way as in two-level inverter. Sub–sector detection is done with the angle and magnitude of V_r vector. On-time calculation in sector 1 and sub-sector 1 can be carried out using (3.8), (3.9) and (3.10).

$$T_a + T_b + T_c = T_s \tag{3.8}$$

Figure 3.8: Sub-sectors in three-level SVPWM

$$\vec{V_1}T_a + \vec{V_2}T_c = \vec{V_r}T_s,\ T_b = 0 \tag{3.9}$$

$$\frac{2V_{dc}}{3}e^{j0}T_a + \frac{2V_{dc}}{3}e^{j\frac{\pi}{3}}T_c = |\vec{V_r}|T_s \tag{3.10}$$

where,

$$V_\alpha = V_{aref} - 0.5V_{bref} - 0.5V_{cref} \tag{3.11}$$

$$V_\beta = (V_{bref} - V_{cref})\frac{\sqrt{3}}{2} \tag{3.12}$$

$$\alpha = tan^{-1}(\frac{V_\beta}{V_\alpha}) \tag{3.13}$$

Then the on times are calculated for each sub-sector by using the equations as in Table 3.6. Ta, Tb and Tc are on-time of each vector as shown in Figure 3.8. Variable k is defined as:

$$k = \sqrt{3}\frac{|\vec{V_r}|}{V_{dc}} \tag{3.14}$$

Table 3.6: Calculated times and sub-sectors in three-level

S	T_a	T_b	T_c
1	$2ksin(\frac{\pi}{3}-\alpha)$	$T_s-2ksin(\frac{\pi}{3}+\alpha)$	$2ksin(\alpha)$
2	$T_s-2ksin(\alpha)$	$2ksin(\frac{\pi}{3}+\alpha)-T_s$	$T_s-2ksin(\frac{\pi}{3}-\alpha)$
3	$2ksin(\alpha)-T_s$	$2ksin(\frac{\pi}{3}-\alpha)$	$2T_s-2ksin(\frac{\pi}{3}+\alpha)$
4	$2T_s-2ksin(\frac{\pi}{3}+\alpha)$	$2ksin(\alpha)$	$2ksin(\frac{\pi}{3}-\alpha)-T_s$

Detailed PWM patterns of SVPWM for each region and sub-region are given in Appendix A.

3.3 Design, Analysis and Implementation of a 750 W Three-Level NPC Type Inverter

In this section, a three-level NPC type inverter was designed an implemented. The hardware infrastructure of PCB is designed for a 750 W PMSM drive having 350 V_{dc} and 230 V_{rms} line-line voltage parameters. The main purpose of this section is to investigate hardware challenges of three-level NPC type topology. First, design procedure is explained and the critical steps to design a three-level NPC type inverter's PCB are shown in this section. Finally, design challenges of hardware and open loop test results up to half of the rated power are given in this chapter.

3.3.1 Design

As control hardware, F28379D Delfino Experimenter Kit as shown in Figure 3.9 is used from Texas Instruments C2000 family. In order to operate three-level NPC type inverter, at least 12 PWM outputs from the DSP or microcontroller are needed. There-

fore; it can be inferred that one of the most developed DSPs should be used in order to design a three-level NPC type inverter. EPWM peripheral of F28379D is used to manipulate semiconductors of hardware.

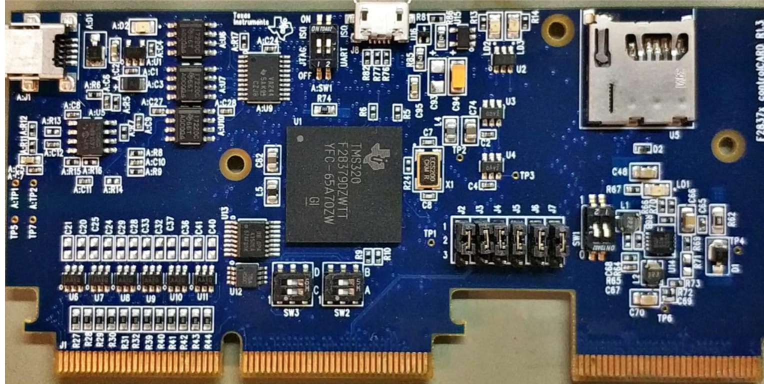


Figure 3.9: F28379D experimenter kit

As the first step, voltage and current rating of hardware are determined. Hardware setup is designed for a PMSM drive rating at 750 W output rating and 350 V dc bus voltage rating. The PMSM has 230 V_{rms} line-line voltage with four pole-pairs.

Desired control method is Field Oriented Control method as used in previous chapters. Therefore; speed sensing is critical for the design. There are various methods of PMSM speed sensing. One of the most common method for speed sensing in PMSMs is incremental encoder method. In this application, power hardware of motor drive circuitry is designed to meet the incremental encoder sensing criterion. Incremental encoder generates square wave pulses as output. Output frequency of sensor is dependent on the speed of the motor. In F28379 DSP module, eCAP (Enhanced Capture Module) captures the rise and fall of the DSP input signal. This peripheral is actually specified to incremental encoder output. With a simple analog circuitry, output of the incremental encoder is connected to the DSP eCAP peripheral easily.

For the Field Oriented Control, phase currents of at least two phases are needed to be sensed. In order to achieve this, hall-effect current sensors are used for each phase. Since output of the hall-effect sensors have high impedance characteristics, they are directly connected to F28379D ADC peripheral inputs. Three-level NPC topology

could face voltage unbalances of floating capacitors due to its nature. In order to avoid such unbalances, floating capacitor voltages should be sensed and with control algorithms undesired unbalances should be avoided. This issue results in increase of both hardware and software complexity. In order to sense floating capacitor voltages, analog sense circuitry was built in the hardware and they are sensed with F28379D ADC peripheral inputs.

The above mentioned issues were implemented in order to prepare PCB board for a closed loop operation while driving the PMSM.

The most critical issue is to construct gate-drive circuitry and power loop construction in power converter design. On the other hand; in three-level NPC topology, each phase leg consists of four bi-directional switches and two clamping diodes. Four bi-directional switches construct a large power loop inductance by nature. In order to avoid such parasitic loop inductance based oscillations, film capacitors, which have good high frequency current capability, are used between high voltage DC positive and center of floating capacitors. Also, by-pass capacitors are added between high voltage DC negative and center of floating capacitors as suggested in [23],[24] and [25].

Another design challenge of a three-level NPC power loop is as follows: Center of floating capacitors are chosen as power ground of the layout. Therefore; digital and analog signals are referenced with regard to center of floating capacitors of DC bus. This application results with a crucial reqirement that all gate drivers should be selected for high side driving. High-side driving can be defined as follows: Source of MOSFET or emitter of IGBT swings between low and high voltages. Therefore; while driving gate of the semiconductor, designer should consider to generate a supply voltage having a reference ground as source or emitter. Therefore; isolated supplies should be generated for each bi-directional semiconductor. In some topologies and switching techniques, this reference voltage generation could be achieved with a method called bootstrap gate driving. Bootstrap gate driving method is simple but maximum on time of the semiconductors are limited. In three level SPWM and SVPWM switching techniques, each switch is completely on or off during half of the fundamental period. Thus it is not a desired application of bootstrap gate driv-

ing. Therefore; total of 12 isolated DC-DC converters are employed for each of the bi-directional semiconductor, which increase complexity of the power hardware.

Selection of switches are important for a power converter. In this application, the main purpose of the design is to build a three-level NPC topology for a specific PMSM. On the other hand, second purpose is to build a generic power converter that can be used in future research activities. For this reason, switches, DC bus capacitors and heatsinks are overdesigned. Although blocking voltage is 175V at this application standard TO-247 packages MOSFETs with 650 V blocking voltages are used as main switches. As clamping diodes SiC diodes are used in order to avoid reverse recovery effect of standard silicon diodes. Clamping diodes have standard TO-220 package. By using industry standard through hole semconductors in the design, an adjustable power board was designed for the future developments.

Three dimensional view of designed PCB's top and bottom layers are shown in Figures 3.10 and 3.11, respectively. Power MOSFETs and clamping diodes are placed at the top side of the PCB. Also, DSP board is placed at the top side. Analog circuitry to sense DC bus voltages and hall effect sensors are placed at the top side. At the bottom side, isolated power supplies for gate driving circuitry are placed.

In this prototype, fan cooling with heatsink is assumed as the cooling solution. Each phase of three-level NPC topology is cooled with one heatsink. Total of six switches are packaged with one heatsink and fan.

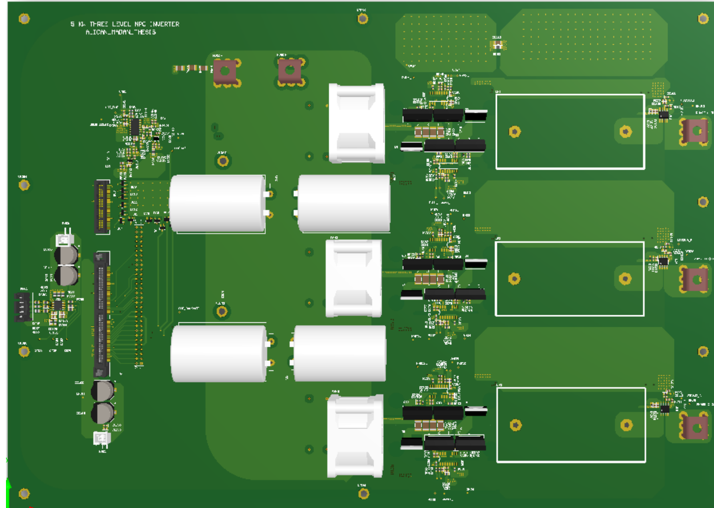


Figure 3.10: Top view of PCB

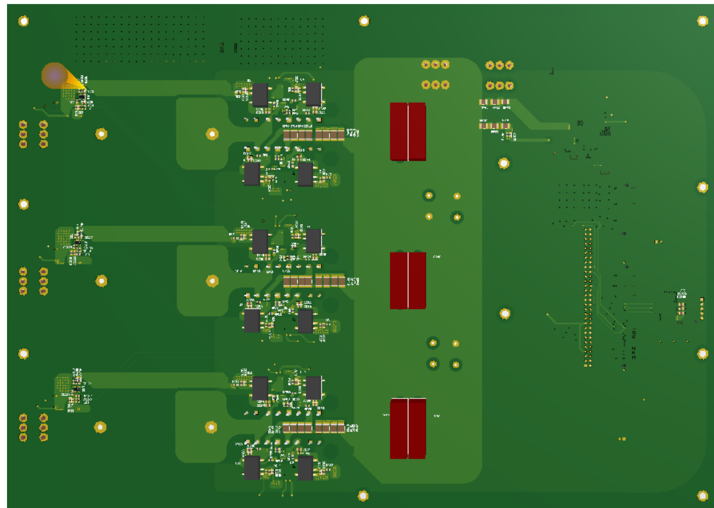


Figure 3.11: Bottom view of PCB

3.3.2 Test Results

In test setup, tests were conducted under 120 W, 240 W and 360 W input power with passive load variations. Resistor bank is adjusted to provide three different output power conditions. Also two different modulation index (m_a) values are used in the tests. An L-C filter is employed at the output of the inverter and resistor bank is used as load. The circuitry schematic in order to conduct tests are given in Figure 3.12.

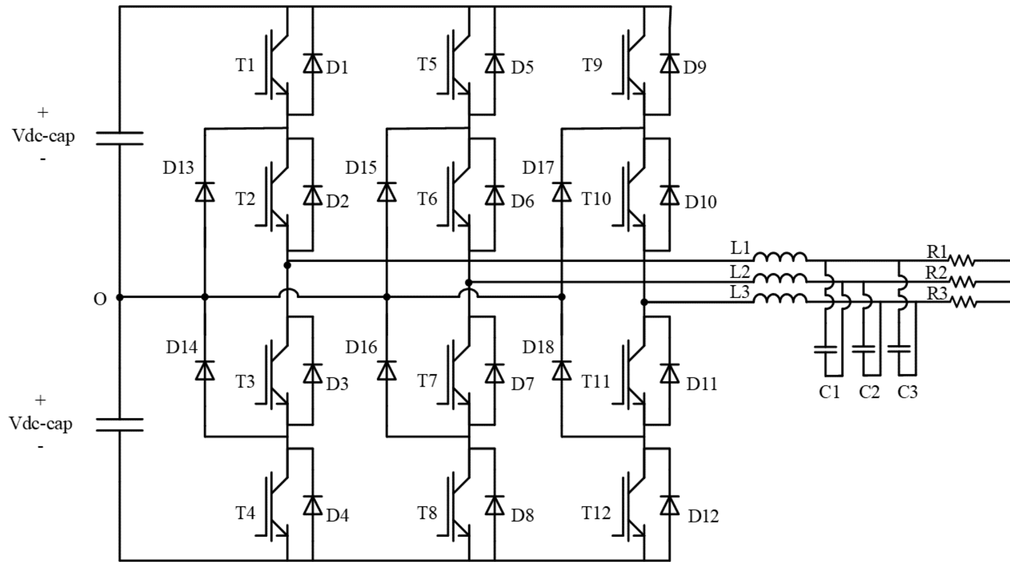


Figure 3.12: Test setup circuitry

Test setup is constructed in the laboratory enviroment. Test setup is shown in Figure 3.13. It consists of the inverter PCB, a high voltage DC source, oscilloscope, a resistor bank. Test parameters are given in Table 3.7

Table 3.7: Hardware test parameters

$V_{dc}(V)$	300
$f_{sw}(kHz)$	25
$f_{out}(Hz)$	50
$R_{load}(\Omega)$	160, 80, 53
$L_1, L_2, L_3(mH)$	2.6
$C_1, C_2, C_3(nF)$	470
m_a	0.8,0.6

In the test procedure, two different observations are done from oscilloscope screen, phase currents and line-line voltages of resistor bank. Since three high bandwidth current probes are not able to be employed in the laboratory environment, line to line voltages of resistor bank for three phases are observed as indicators of phase currents. Six open loop tests are conducted with two different modulation indexes

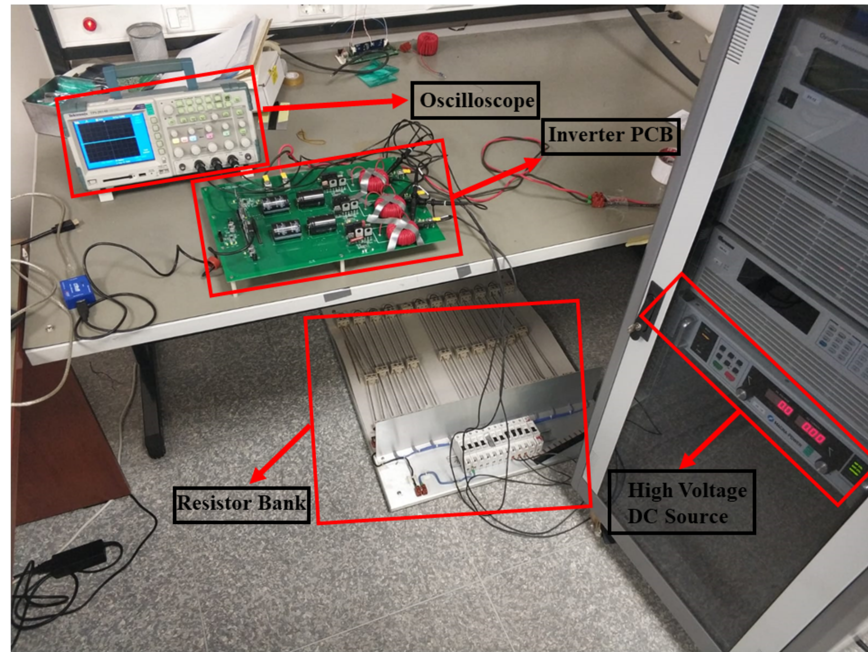


Figure 3.13: Test setup

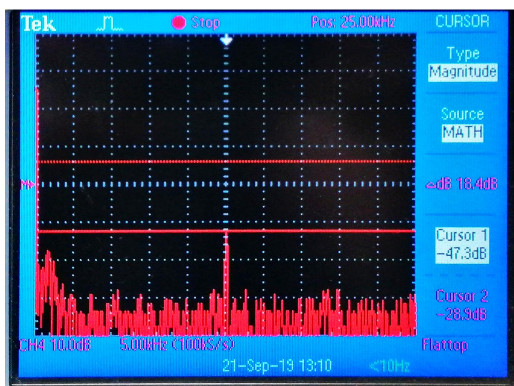
and three loading conditions. Harmonic content of the phase currents and dominant components are also observed in the tests. Open loop phase current waveforms and harmonic content results are given in Figures 3.14 to 3.19.

From the test results, it is clearly seen that fundamental harmonic and switching frequency component is dominant in three-level NPC inverter. Also in every harmonic analysis, it is observed that component at the resonant frequency of the L-C filter is seen at the output. 470 nH capacitor and 2.6 mH inductor filter have resonance at 2.6 kHz since capacitors are delta connected.

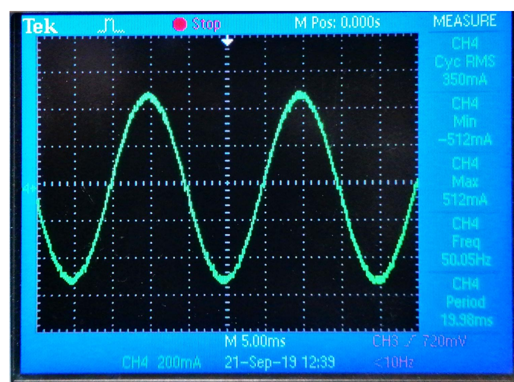
By conducting those tests, hardware is prepared for its real application of PMSM drive. Since tests are conducted with passive balanced loads, unbalance between floating capacitors are not observed. Requirement of isolated power supplies for each semiconductor increases initial cost of the hardware. Also manipulation of 12 controlled bi-directional power semiconductors increases complexity of PWM generation unit. An advanced DSP or microcontroller is needed to use in the hardware. Therefore; three-level NPC topology is not suitable for low power and cost critical applications. On the other hand, halved blocking voltage is one of the major advantages of three-level NPC topology hardware.

Also one of the main advantages of three-level NPC topology is observed in the experiments. Blocking voltage requirement of the semiconductors is half of the DC bus voltage. Drain-source voltage of one MOSFET in the hardware during tun-off is shown in Figure 3.22. As can be seen, the switch need to block 150 V.

In this chapter, the two switching techniques are selected and detailly explained for the two common inverter topologies for electric vehicle drive systems. Also implementation of a threelevel NPC type inverter is detaily explained and test results are given. In the next chapter, semiconductor losses and thermal modelling fundamentals are given for the two topologies. Then multidimensional comparison of the two topologies and two switching techniques are done in the fifth and fourth chapters.

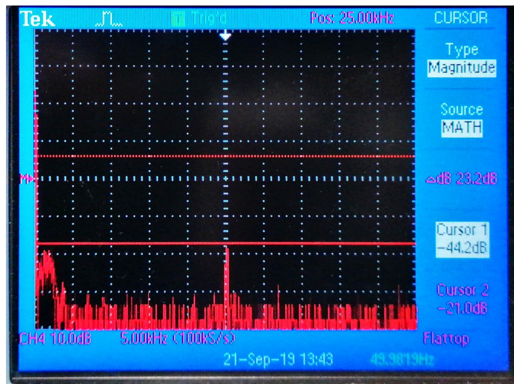


(a) Harmonic content of phase current under $R_{load} = 160\Omega$ and $m_a = 0.6$

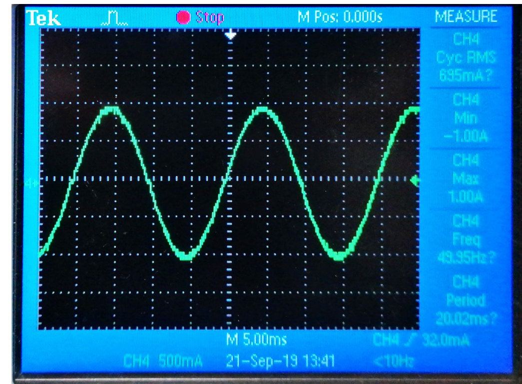


(b) Current waveform with $R_{load} = 160\Omega$ and $m_a = 0.6$

Figure 3.14: Phase current waveform and harmonic spectrum with $R_{load} = 160\Omega$ and $m_a = 0.6$

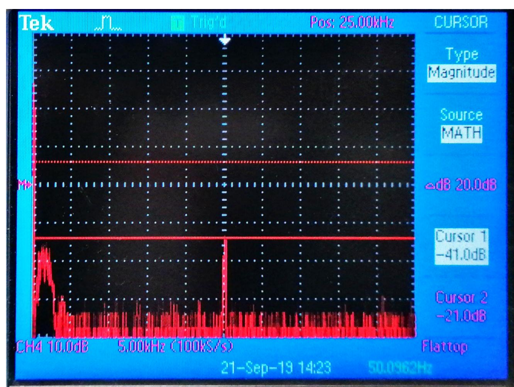


(a) Harmonic content of phase current under $R_{load} = 80\Omega$ and $m_a = 0.6$

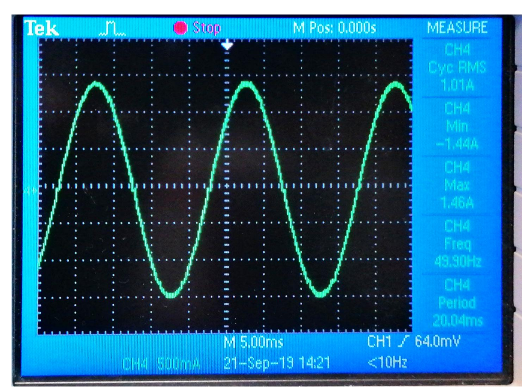


(b) Current waveform with $R_{load} = 80\Omega$ and $m_a = 0.6$

Figure 3.15: Phase current waveform and harmonic spectrum with $R_{load} = 80\Omega$ and $m_a = 0.6$

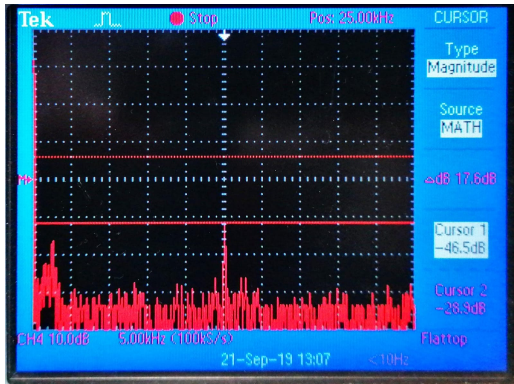


(a) Harmonic content of phase current under $R_{load} = 53\Omega$and $m_a = 0.6$

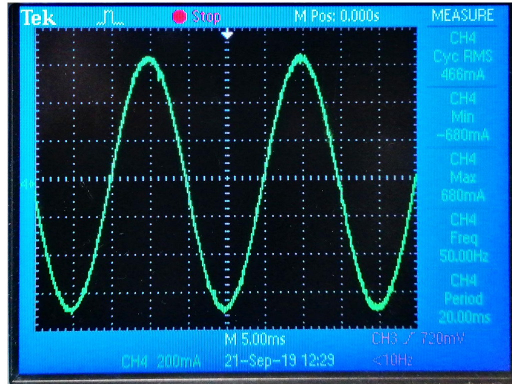


(b) Current waveform with $R_{load} = 53\Omega$ and $m_a = 0.6$

Figure 3.16: Phase current waveform and harmonic spectrum with $R_{load} = 53\Omega$ and $m_a = 0.6$

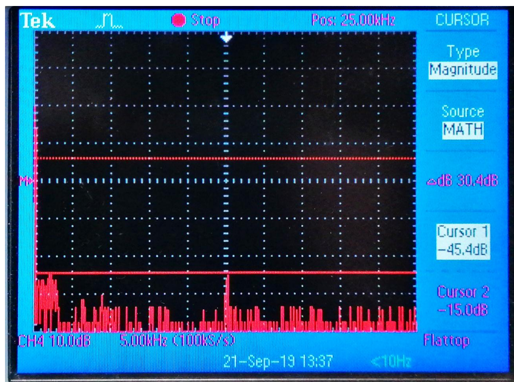


(a) Harmonic content of phase current under $R_{load} = 160\Omega$ and $m_a = 0.8$

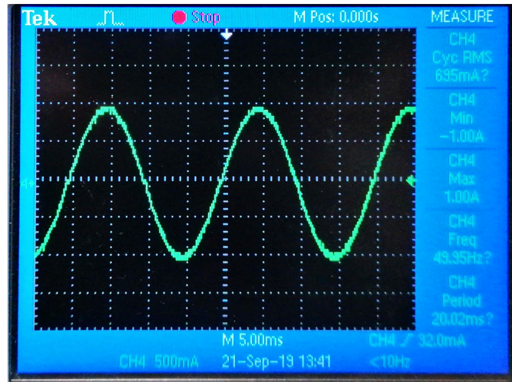


(b) Current waveform with $R_{load} = 160\Omega$ and $m_a = 0.8$

Figure 3.17: Phase current waveform and harmonic spectrum with $R_{load} = 160\Omega$ and $m_a = 0.8$

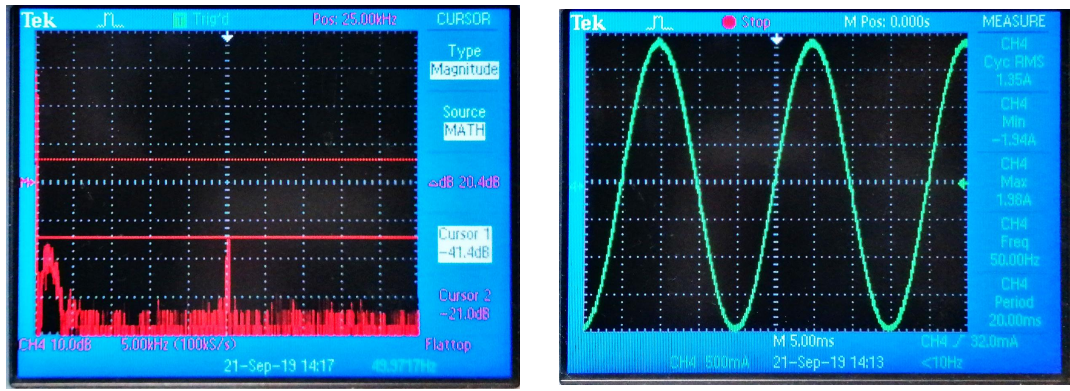


(a) Harmonic content of phase current under $R_{load} = 80\Omega$ and $m_a = 0.8$



(b) Current waveform with $R_{load} = 80\Omega$ and $m_a = 0.8$

Figure 3.18: Phase current waveform and harmonic spectrum with $R_{load} = 80\Omega$ and $m_a = 0.8$



(a) Harmonic content of phase current under $R_{load} = 53\Omega$and $m_a = 0.8$

(b) Current waveform with $R_{load} = 53\Omega$ and $m_a = 0.8$

Figure 3.19: Phase current waveform and harmonic spectrum with $R_{load} = 53\Omega$ and $m_a = 0.8$

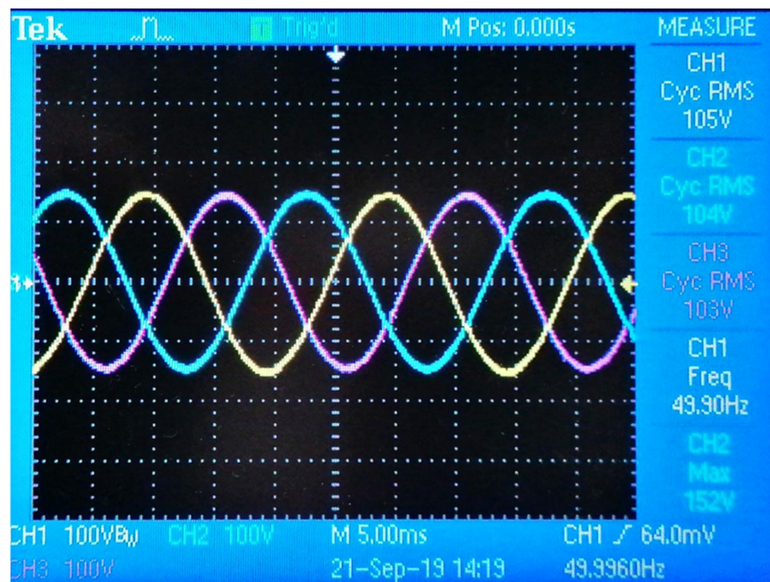


Figure 3.20: Line to line voltages of resistor bank with m_a=0.6 and $R_{load} = 53\Omega$

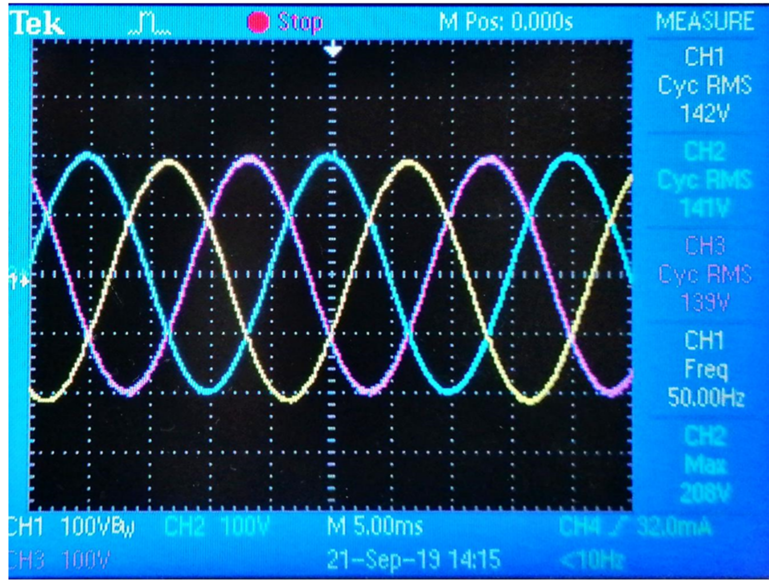


Figure 3.21: Line to line voltages of resistor bank with m_a=0.8 and $R_{load} = 53\Omega$

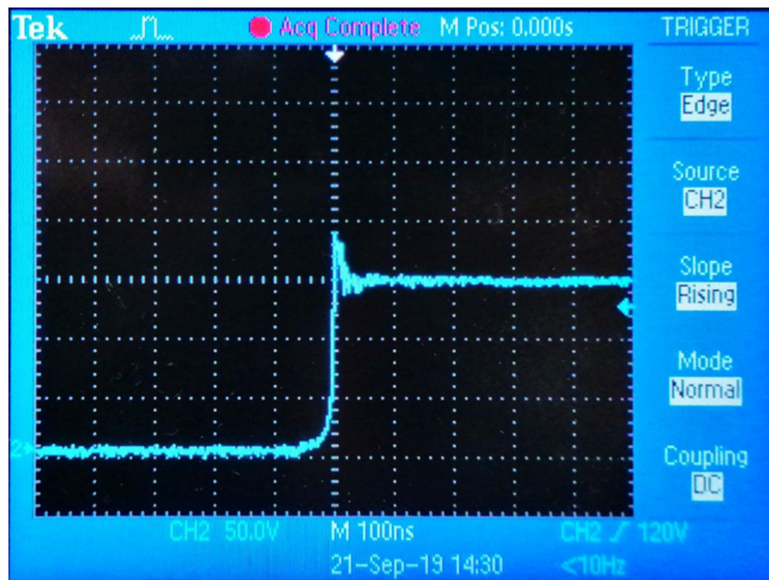


Figure 3.22: Drain-source voltage of MOSFET with 300 V DC bus

CHAPTER 4

SEMICONDUCTOR LOSSES AND THERMAL MODELLING

Main trend in power electronics is designing more compact, more efficient and more reliable converters. Development in semiconductor technologies enabled higher switching frequencies. Higher switching frequencies allow designers to use smaller passive components, thus higher power density converters. Compacter power converters make detailed calculations of thermal management inevitable. Therefore; one of the main challenges in power electronics design is thermal management. Analytical calculations of semiconductor losses in a power converter is the first step of the thermal management. After calculation of semiconductor losses, cooling requirement can be determined and thermal reliability issues can be addressed. Besides, cooling pays a significant role in cost analysis for high power power electronics [26].

4.1 Semiconductor Losses

Semiconductor losses are evaluated for the IGBTs and diodes to compare topologies in terms of different aspects of their thermal performances in two-level and three-level topology.

Mathematical formulations given in this section only show semiconductor losses as average losses. For thermal calculations, power frequency ripple is out of scope of the thesis. In next chapters, different comparisons and calculations are done.

4.1.1 IGBT Losses

IGBT loss calculations are calculated for two-level inverter topology using the equations in [4]. Semiconductor losses are divided into two main groups as conduction losses and switching losses. Total loss of IGBT is sum of conduction loss P_{cond} and switching loss P_{sw}.

$$P_{sw(T)} = f_{sw} E_{on+off} \frac{\sqrt{2}}{\pi} (\frac{I_{out}}{I_{ref}})^{K_i} (\frac{V_{cc}}{V_{ref}})^{K_v} (1 + TC_{ESW}(T_j - T_{ref}) \tag{4.1}$$

$$P_{cond(T)} = (\frac{1}{2\pi} + \frac{mcos(\phi)}{8}) V_{CE0}(T_j) \widehat{I_1} + (\frac{1}{8} + \frac{mcos(\phi)}{3\pi}) r_{ce}(T_j) \widehat{I_1^2} \tag{4.2}$$

IGBT losses in a three-level NPC topology for top and bottom switches are defined in [27]. Losses of uppermost and lowermost IGBTs are as follows:

$$P_{cond(T1,T4)} = \frac{m\widehat{I_{out}}}{12\pi} . \{3V_{CE0}[(\pi - \phi).cos(\phi) + sin(\phi)] + 2r_{ce}\widehat{I}.[1 + cos(\phi)]^2\} \tag{4.3}$$

$$P_{sw(T1,T4)} = f_{sw}.E_{on+off}.(\frac{\widehat{I_{out}}}{I_{ref}})^{K_i}.(\frac{V_{cc}}{V_{ref}})^{K_v}.(\frac{1}{2\pi}[1 + cos(\phi)])(1+ TC_{ESW}(T_j - T_{ref})) \tag{4.4}$$

IGBT losses for middle two switches are defined as follows:

$$P_{cond(T2,T3)} = \frac{\widehat{I_{out}}}{12\pi} . \{V_{CE0}.[12 + 3m(\phi cos(\phi) - sin(\phi)] + r_{ce}.\widehat{I_{out}}.[3\pi - 2m(1 - cos(\phi))^2]\} \tag{4.5}$$

$$P_{sw(T2,T3)} = f_{sw}.E_{on+off}.(\frac{\widehat{I_{out}}}{I_{ref}})^{K_i}.(\frac{V_{cc}}{V_{ref}})^{K_v}.(\frac{1}{2\pi}[1 - cos(\phi)])(1+ TC_{ESW}(T_j - T_{ref})) \tag{4.6}$$

Where,

f_{sw}: Switching frequency

E_{on+off}: Sum of turn-on and turn-off energies of IGBT for I_{out}

I_{out}: RMS value of phase current

I_{ref}: Reference current value for loss calculations in IGBT datasheet

V_{cc}: blocked DC voltage value by IGBT in the application

V_{ref}: Reference voltage value for loss calculation in IGBT datasheet

K_v: Exponents for voltage dependency of switching losses, taken 1.4 for IGBTs

TC_{ESW}: Temperature dependency coefficient of switching losses, taken 0.003 for IGBTs

m: Modulation index

4.1.2 Diode Losses

For two-level topology diode losses are calculated as in [4] as follows:

$$P_{cond(D)} = (\frac{1}{2\pi} - \frac{mcos(\phi)}{8})V_{F0}(T_j)\widehat{I_1} + (\frac{1}{8} - \frac{mcos(\phi)}{3\pi})r_f(T_j)\widehat{I_1^2} \tag{4.7}$$

$$P_{sw(D)} = f_{sw}E_{rr}\frac{\sqrt{2}}{\pi}(\frac{I_1}{I_{ref}})(\frac{V_{cc}}{V_{ref}})^{K_v}(1 + TC_{Err}(T_j - T_{ref}) \tag{4.8}$$

For three-level NPC type inverter, diode losses are calculated as in [27] as follows:

$$\begin{aligned} P_{cond(D5,D6)} = \frac{\widehat{I_{out}}}{12\pi}.\{V_{f0}.[12 + 3m[(2\phi - \pi)cos(\phi) - 2sin(\phi)]] \\ +r_d\widehat{I_{out}}.[3\pi - 4m(1 + cos^2(\phi)]\} \end{aligned} \tag{4.9}$$

$$P_{sw(D5,D6)} = f_{sw}.E_{on+off}.(\frac{\widehat{I_{out}}}{I_{ref}})^{K_i}.(\frac{V_{cc}}{V_{ref}})^{K_v}.(\frac{1}{2\pi}[1 + cos(\phi)])(1+ TC_{ESW}(T_j - T_{ref})) \quad (4.10)$$

$$P_{cond(D1,D4)} = \frac{m\widehat{I_{out}}}{12\pi}.\{3V_{f0}.[-\phi cos(\phi) + sin(\phi)] + 2r_d\widehat{I_{out}}.[1 - cos(\phi)]^2\} \quad (4.11)$$

$$P_{sw(D1,D4)} = f_{sw}.E_{rr}.(\frac{\widehat{I_{out}}}{I_{ref}})^{K_i}.(\frac{V_{cc}}{V_{ref}})^{K_v}.(\frac{1}{2\pi}[1 - cos(\phi)])(1 + TC_{ESW}(T_j - T_{ref})) \quad (4.12)$$

$$P_{cond(D2,D3)} = \frac{m\widehat{I_{out}}}{12\pi}.\{3V_{f0}.[-\phi cos(\phi) + sin(\phi)] + 2r_d\widehat{I_{out}}.[1 - cos(\phi)]^2\} \quad (4.13)$$

$$P_{sw(D2,D3)} = 0 \quad (4.14)$$

From loss calculations for both topologies, it is clearly seen that in two-level topology, a uniform loss distribution among switches is achieved. On the other hand, in three-level NPC type topology, a non-uniform heat generation is observed. Non-uniform heating results in different thermal reliability of each semiconductor. Middle switches of three-level NPC type topology are the most heated semiconductors and operating conditions of these switches must be considered for thermal design.

4.2 Thermal Modeling

Heat propagation occurs in three different ways in a system, that are by conduction, convection and radiation. Conduction is the movement of kinetic energy in materials from higher temperature areas to lower temperature areas through a substance until an equilibrium is reached. In electronic components, thermal analysis are done only by considering heat conduction.

Heat conduction between components is modelled making use of the analogical relation between thermal parameters and electrical parameters. Selected analogy between thermal and electrical parameters are given in Table 4.1.

Table 4.1: Thermal and electrical analogy

THERMAL		ELECTRICAL	
Temperature	T in K	Voltage	U in V
Heat Flow	P in W	Current	I in A
Thermal Resistance	R_{th}	Resistance	R in V/A
Thermal Capacitance	C_{th} in Ws/K	Capacitance	C in As/V

Accordingly, power losses are modelled as current sources and each cooling equipment, semiconductor, interface materials have thermal resistances on the flow path of power losses. Also materials mentioned above have thermal capacitances depending on the material's specific heat as well as its mass and volume. Voltage of the each node in thermal model represents the temperature of that point in the circuitry.

In power electronics, each semiconductor manufacturer publishes thermal resistance and capacitance curves in datasheets. Heatsink manufacturers publish thermal resistance parameters in datasheets too. Hence, thermal models can be created based on manufacturer's data without testing the equipment.

4.2.1 Thermal Equivalent Circuit Models

Two common thermal semiconductor models are the Foster and Cauer models [28]. By the help of these models, analytical calculations can be used to solve for complex electro-thermal systems. Thermal resistances represent resistance to heat flow which creates temperature difference when loss flows into model. Thermal capacitances represent thermal inertia of materials in the models which determine heating and cooling time constants of materials.

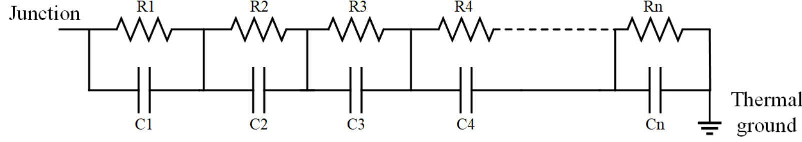


Figure 4.1: Foster model representation

Foster Model

Foster model also called non-grounded capacitor thermal model is shown in Figure 4.1. Thermal ground represents ambient temperature as potential of the node. It is constructed with series connection of parallel R-C networks. Mathematical expression for this model is given in (4.15). In (4.15), Z_{thja} represents thermal impedance of the R-C rungs from junction to ambient. τ_i is the time constant of i_{th} R-C pair in the network. In this model, R-C pairs have no physical meaning. However; this model enables a mathematical simplification in thermal network modeling. Each R-C network has a contribution to the overall system thermal response. Weakness of this model emerges when impulse response of junction temperature is investigated, series capacitances in the model cause unrealistic temperature rise at the nodes. However; experimental extraction of Foster model parameters is easy. Therefore; semiconductor manufacturers mostly give Foster model parameters in the datasheets.

$$Z_{thja} = \sum_{i=1}^{n} R_i(1 - e^{\frac{t}{\tau_i}}) \tag{4.15}$$

Cauer Model

Cauer model also called as grounded capacitor thermal model is shown in Figure 4.2. Thermal impedance of the network is given in (4.15) in s domain. Every node between resistors are grounded through capacitors. Therefore, every node between resistors have physical meaning in this model. Main advantage of the model is that the model can be derived from fundamental laws of heat transfer by conduction. Moreover, this model gives more realistic results when impulse response of junction temperature is under investigation. The main drawback of this model is parameters of each physical layer in the chip must be known. Therefore, in order to construct a

good physically meaningful Cauer model, thermal resistance and capacitance of each layer should be considered. On the other hand, it is possible to convert a thermal network from Foster model to Cauer model. It should be noted that Cauer model that is obtained from Foster model does not have a physical meaning as well.

$$Z_{thja}(s) = \cfrac{1}{sC_1 + \cfrac{1}{R_1 + \cfrac{1}{sC_2 + ... + \cfrac{1}{R_n}}}} \tag{4.16}$$

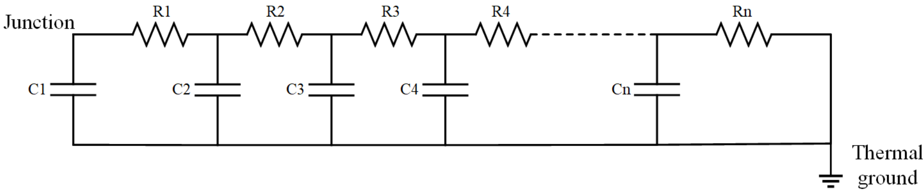


Figure 4.2: Cauer model representation

Comparison of Thermal Equivalent Circuit Models

In Cauer model each node has a physical meaning in terms of temperature, whereas node temperatures do not have a physical meaning in Foster model. R-C rungs can be placed in any order while modelling. However; since Foster model is easy to derive from thermal impedance curve or from experiments, semiconductor manufacturer companies generally give Foster model parameters in datasheets.

Weakness of Foster model is clear when heatsink and thermal interface material are added to the thermal model. Thermal interface materials are generally modeled as thermal resistance only and capacitance of thermal interface material can be ignored due to their low thermal inertia. When a series resistance is added to Foster model, impulse power loss is reflected instantly to the semiconductor case through series capacitors, which is not the case in real system. Heatsink, case of semiconductor and junction of semiconductor are heated with the given order in real life even though an impulse power loss occurs in the semiconductor.

In this thesis, Cauer model is used in the thermal analyses. Three ladder Cauer model of IGBTs and diodes are extracted from datasheet values. Only one thermal resistor is used as thermal interface material. One resistor capacitor pair is used to model heatsink in the analyses.

CHAPTER 5

MULTIDIMENSIONAL COMPARISON OF A 120 KW ELECTRIC VEHICLE DRIVE

A multidimensional comparison of two-level and three-level inverter topologies for a 120 kW PMSM drive is considered in this chapter. Comparison of two topologies with two major switching techniques SPWM and SVPWM are conducted. Conventional Si IGBT diode pairs are used for both topologies from SEMIKRON. DC Bus voltage of the motor drive is selected as 850 V in the design. Therefore; 650 V IGBT diode pair is used for three-level topology while 1200 V IGBT is selected for two-level topology. Comparison is done in terms of output voltage and current quality, junction temperatures and switching frequency limitation aspects. In order to make a reasonable comparison, same heatsinks are assumed in both topologies. The following four cases are analyzed:

- Two-level topology with SPWM
- Two-level topology with SVPWM
- Three-level NPC topology with SPWM
- Three-level NPC topology with SVPWM

First of all, output voltage and current quality are compared at 30 % of rated torque and at different rotational speeds. These operation points are selected to account for a daily drive cycle. This is followed by thermal analysis in Plexim/PLECS simulation platform performed at rated torque and rated speed to analyze the inverter at full load. These electro-thermal simulations are done to calculate junction temperatures of each semiconductor device in the PMSM drive. By limiting the maximum thermal junction

temperature of semiconductors (130^oC), switching frequency limits of each case are explored.

5.1 PMSM Fundamentals

Equivalent circuit model of PMSM consists of two different circuit which are d axis and q axis equivalent circuits. The two equivalent circuit is represented in Figure 5.1 and 5.2. I_d and I_q are the d and q axis currents of PMSM as a result of Park's and Clark's transformation of three phase currents of inverter. R_s represents stator phase resistance. L_d and L_q are the d-axis and q-axis inductances of the motor, respectively. Number of pole pairs are represented as pp. Position of the motor is represented as θ_m. Mechanical speed of the motor is represented as ω_m. ϕ_m' represents the flux linkage due to PMs. ϕ_d and ϕ_q are the corresponding flux linkages of axes. T_e and T_m are electrical torque and mechanical torque, respectively. It should be noted that friction of the motor is ignored in mathematical motor equations. Motor equations that is used in calculations are given in (5.1) to (5.5).

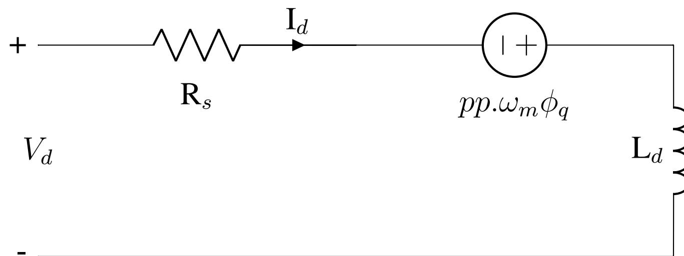


Figure 5.1: d axis equivalent circuit of PMSM

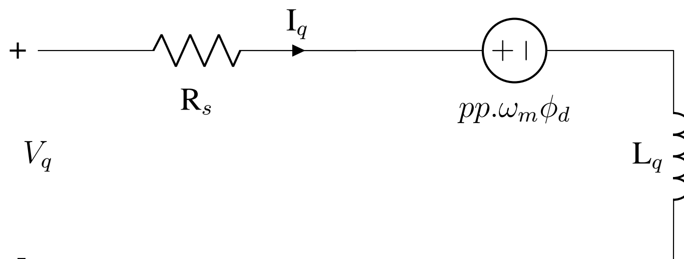


Figure 5.2: q axis equivalent circuit of PMSM

$$\phi_q = L_q I_q \tag{5.1}$$

$$\phi_d = L_d I_d + \phi'_m \tag{5.2}$$

$$T_e = \frac{3}{2}.pp.(\phi_d I_q - \phi_q I_d) \tag{5.3}$$

$$\dot{\omega}_m = \frac{1}{J}(T_e - T_m) \tag{5.4}$$

$$\dot{\theta}_m = \omega_m \tag{5.5}$$

5.2 Semiconductor Module Selection

Main switches should be bi-directional in each topology. Si MOSFET, SiC MOSFET, GANFET, IGBT-Diode pairs could be used as main switch depending on the current, blocking voltage and switching frequency requirements of the design. For the power level of the PMSM in the thesis, conventional IGBT-Diode pairs are widely used in industry. Therefore; IGBT-Diode pairs from SEMIKRON are used in this study. The selected IGBT-Diode modules are given in Table 5.1.

Table 5.1: Selected modules

Topology	IGBT and Diode Module	$V_{CE,max}(V)$
Two-level	SKiiP39GB12E4V1_HPTP	1200
Three-level NPC	SkiM401MLI07E4	650

A 120 kW PMSM drive with the motor and driver parameters given in Table 5.2 is modelled in PLECS software. ω_{rated} and ω_{max} represent rated and maximum mechanical speeds of the motor, respectively.

Table 5.2: PMSM and inverter parameters

Parameter	Value
$V_{dc}(V)$	850
$R_s(m\Omega)$	6.6
$L_d, L_q(\mu H)$	600
ϕ'_m (V.s)	0.222
ω_{rated}(rpm)	4583
ω_{max}(rpm)	12000
pp	3
$I_{phase,rms}$ (A)	177
$f_{sw}(kHz)$	8-12
T_{max}	250

Two-level and three-level NPC VSI topologies are simulated with both SPWM and SVPWM, so in total four cases are analyzed. In order to conduct a fair comparison, controller performance of the motor drives are kept same for all cases. Moreover, as mentioned before the same heatsinks are chosen for both topologies to avoid influence of the size of the cooling system. Analyses are done with different switching frequencies varying between 8-12 kHz. Minimum switching frequency is selected as 8 kHz by considering maximum speed of the electric machine, that is 12000 rpm resulting in 600 Hz fundamental stator frequency. Maximum switching frequency is selected considering the thermal limitation of the two-level topology by setting the maximum junction temperature to 130 ^oC in the designs.

As closed loop operation, field oriented control (FOC) technique is implemented using outer speed and inner current loops. There are many different FOC methods in the literature applied in PMSM motor drive control. Most of them aims to decrease the order of control equations by adding decoupling terms into the control model. In [29],

implementation of decoupling terms are shown. Addition of decoupling terms decrease current overshoots due to cross-coupling terms caused by mutual inductances. Controller performance is out of the scope of this thesis. Therefore; decoupling terms are not used in the controller model of the simulations and the block diagram of closed loop system without cross-coupling terms is given in Figure 5.3. The only aim is to keep controller performance the same for all switching techniques and topologies. In order to compare controller performances, speed is kept constant at rated speed and step load torque change is applied to all four cases. Same controller performances, which are speed regulation and dynamic response are achieved for each topology and each switching technique. An exemplary controller performance of the motor drive is shown in Figure 5.4. Also, topologies are only compared for steady state operations. By this way, effect of controller is mostly excluded from comparison parameters.

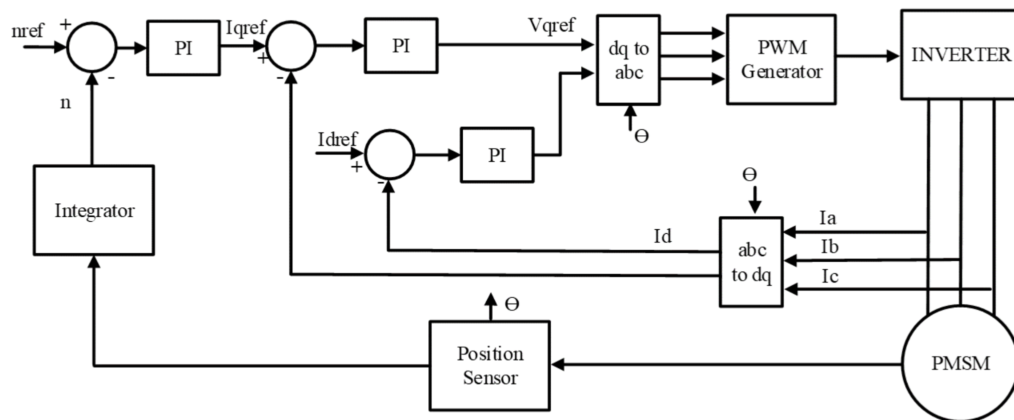


Figure 5.3: FOC block diagram

I_d and I_q currents that are abc to dq transformation outputs are regulated by the inner current control loop. In FOC technique, I_q current is controlled to adjust electrical torque to sustain load torque in a surface mount PMSM, whereas I_d current reference is zero until rated speed is exceeded. In the field weakening region, I_d current reference is adjusted to be able to increase speed of the electric machine.

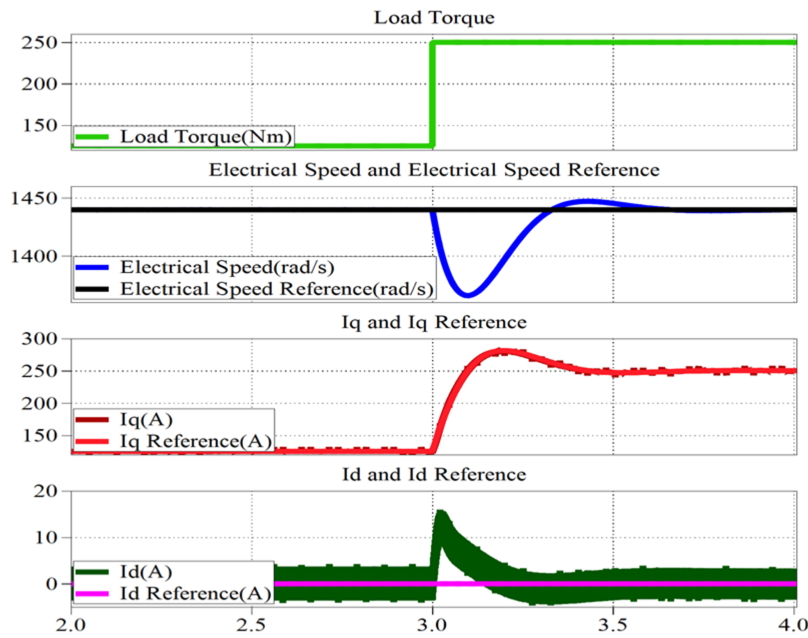


Figure 5.4: Step response of controller

5.3 Electrical Performance Comparison

Current THD analyses are done with constant torque of 75 Nm (30 % of the rated torque). For different speeds of motor, current THDs at different switching frequencies are observed. Current THD values with rated and half of the rated speed is given in Figure 5.5 and Figure 5.6, respectively. Difference between current THD values gets more distinct at higher speed operations and the most distinct operation between cases is observed at rated speed. Three-level NPC topology with SVPWM has superior performance at all motor speeds and switching frequency cases. Three-level topology generates voltage pulses of half of the amplitude of the two-level topology at the output. Therefore; current THD of the three-level topology is expected to be less than two level topology. Moreover, SVPWM has better performance than SPWM in terms of current THD in both topologies, whereas performance difference is more noticeable in three-level topology. Current THD in all cases decrease as switching frequency increases and decrease of output current THD is expected to result in lower core losses in the machine [30].

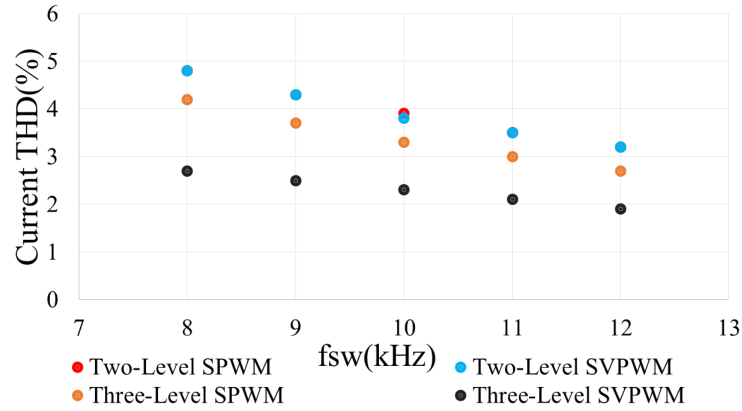


Figure 5.5: Current THD (%) vs. switching frequency at 2291 rpm

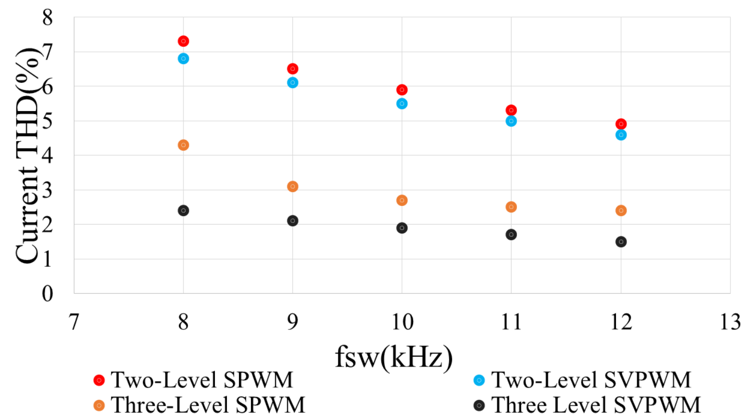


Figure 5.6: Current THD (%) vs. switching frequency at 4583 rpm

5.4 Efficiency and Thermal Performance Comparison

Electro-thermal simulations are carried out at rated speed and rated torque. Both semiconductor modules are assumed directly connected to the heatsink without any thermal interface material. PLECS thermal models calculate loss of a semiconductor by summing energy losses of semiconductors within a switching period. Then averaging them in fundamental cycle of output voltage and current, average loss values of each module are calculated.

Electro-thermal simulation schematic screens are given in Figure 5.7 and Figure 5.8. Same heatsink thermal resistance and capacitance values are used for both topologies having R_{s-a}=0.023 ^{o}C/W as sink-ambient thermal resistance. Since both modules are

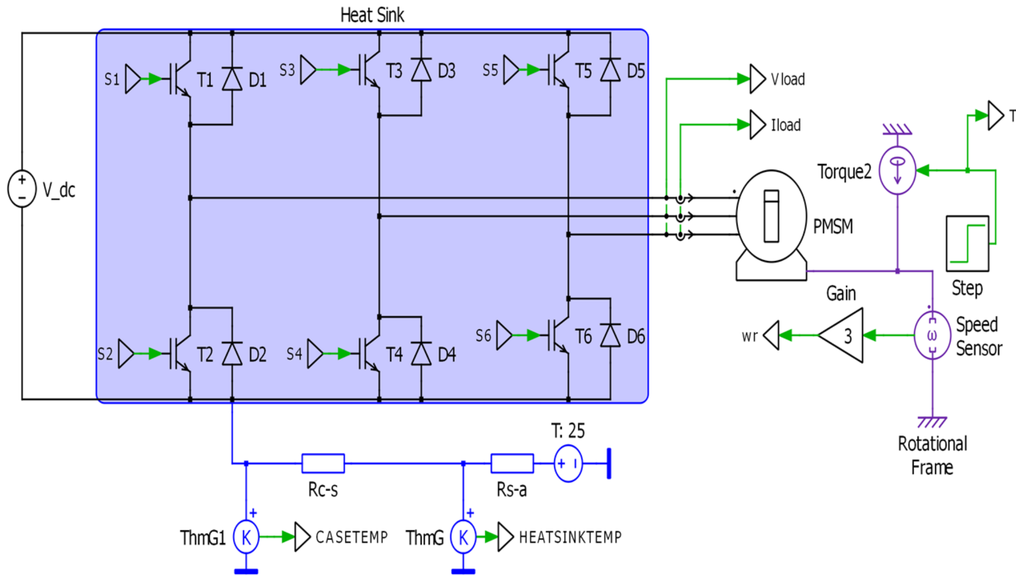


Figure 5.7: Two-level topology electro-thermal model

connected to the heatsink directly, case-sink thermal resistance R_{c-s} is assumed to be zero for each module. Case-heatsink and heatsink-ambient thermal resistances are implemented in the electro-thermal simulation model as in Figure 5.7 and Figure 5.8. IGBT and diode junction-case thermal resistances are derived using datasheet values and SEMISEL design tool. SEMIKRON's WP16_280 heatsink module is used in both designs. Liquid cooling is assumed with a flow rate of 6 l/min. Liquid inside the heatsink is assumed 50% water and 50% glycol for the calculations. Ambient and coolant temperature is set to 25 ^{0}C.

Loss distributions of topologies with SPWM and SVPWM are shown in Figure 5.10. First of all, it is evident that the switching technique does not have a significant effect on thermal performance in both topologies that is conduction losses and switching losses are almost the same. Due to increase in number of switches, conduction losses are almost doubled in three-level topology. On the other hand, switching loss decrease is significant from two-level to three-level topology. In two-level topology, main switches are operating against double V$_{CE}$ voltage stress compared with three-level topology for the same DC bus voltage level. Therefore; switching losses are dominant in two-level topology. Another reason of high switching losses in two-level topology is that the relation between switching losses and blocking voltage is not linear. Dominance of switching losses can be seen in Figure 5.10.

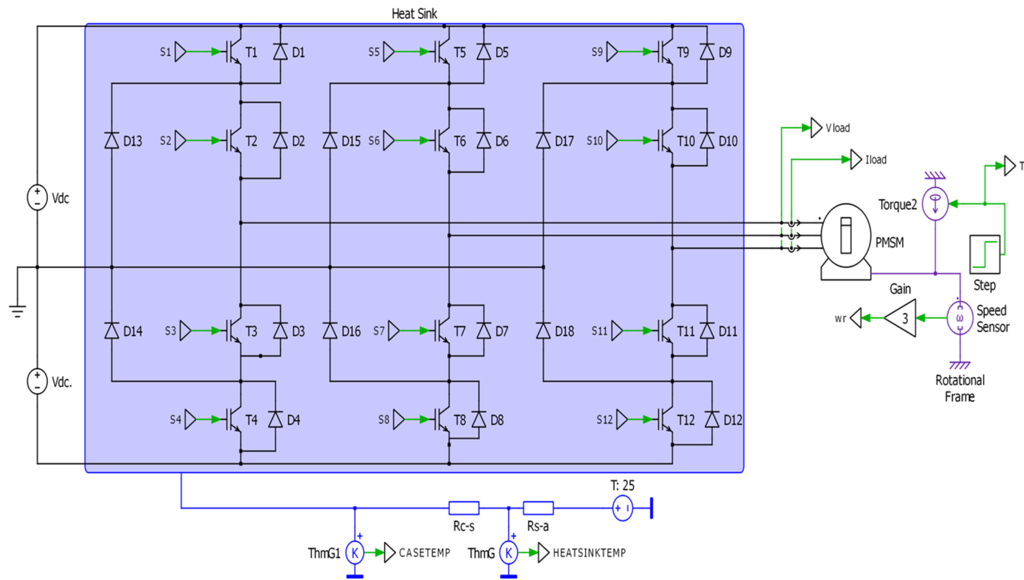


Figure 5.8: Three-level NPC topology electro-thermal model

Two-level topology has higher total losses dominated by switching losses. At 12 kHz switching frequency, maximum junction temperature constraint is reached for two-level topology as can be seen in Figure 5.9.

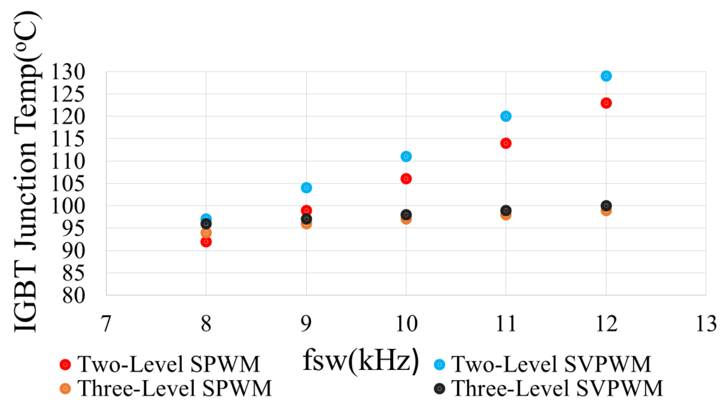
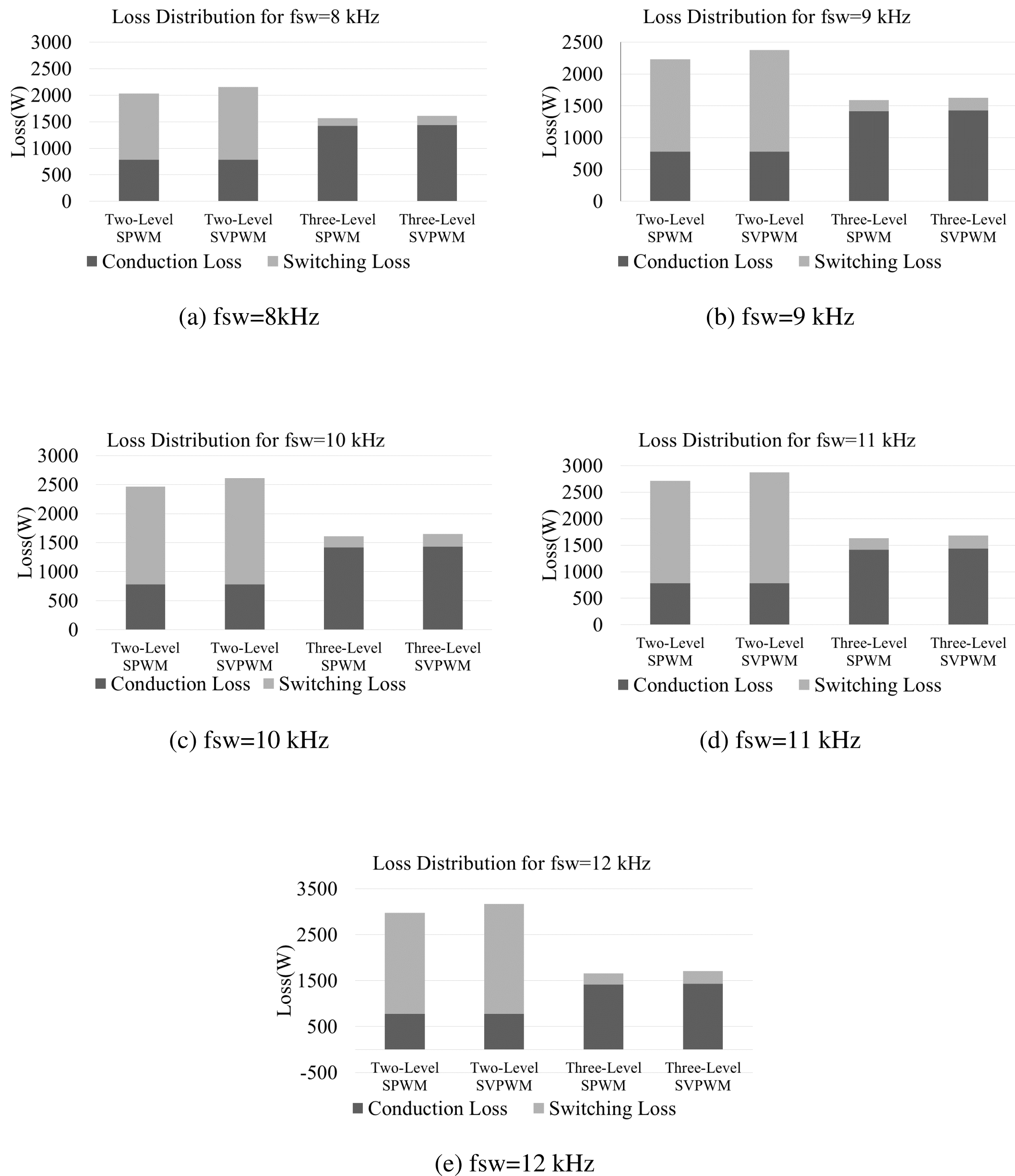


Figure 5.9: IGBT junction temperatures with different switching frequencies

Three-level topology reaches maximum junction temperature of 130 ^{o}C at 22 kHz frequency. That is with the given semiconductors, three-level topology could be used even at f_{sw}=22 kHz although two-level topology is limited at 12 kHz switching frequency. Switching at 22 kHz results with a better output current THD and less torque ripple at the output.

Thermal limitation of inverters are not determined by diodes in this application. Thermal effect of diodes are significant when motor operates at lower power factor values. Inverter operates at a power factor of 0.83 in rated torque and rated speed condition.



(a) fsw=8kHz

(b) fsw=9 kHz

(c) fsw=10 kHz

(d) fsw=11 kHz

(e) fsw=12 kHz

Figure 5.10: Loss distribution with different switching frequencies

5.5 Common Mode Voltage Comparison

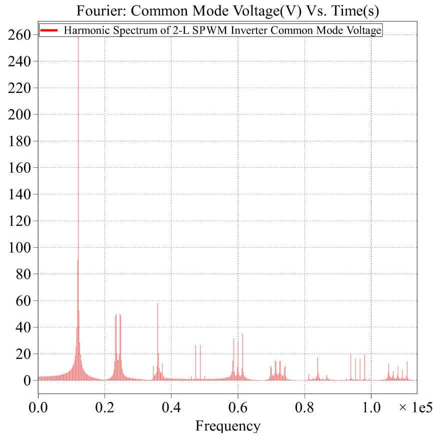
In voltage source inverters, common mode voltage (CMV) is defined as potential difference between star connected load neutral and power ground. On the other hand, voltage between neutral point of the load and floating point of split capacitor DC bus also corresponds to the CMV in a voltage source inverter.

As a result of CMV, common mode current (CMC) flows in both motor and the motor drive. This can result in motor bearing currents and motor failures [31], [32]. Additionally, CMV could result in electromagnetic interferance (EMI) noise, which can affect other electronic circuitry that are fed from the same power supply [33]. In order to avoid these problematic issues, CMV mitigation or decreasing CMC in voltage source inverters have been deeply investigated in the literature. Most of the applied methods include additional passive components such as common mode inductor and capacitor filter components [34], [35], [36]. Some of the methods include active circuitry to mitigate CMV [37]. Other methods propose application of different switching techniques, since switching techniques affect CMV and thus diferent CMC flowing through circuit [38], [39]. CMV is inevitable in voltage source inverters in AC drive applications and mitigation of CMV is crucial. Therefore, CMV performance of the topologies and switching techniques must be considered while designing an AC motor drive.

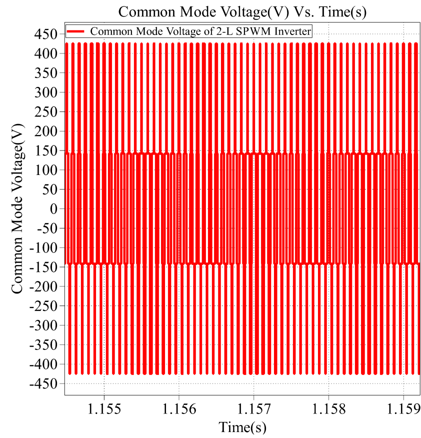
In this part of thesis, each topology and switching technique are compared in terms of CMV. In two-level inverter, split capacitor DC bus is simulated in order to model common mode voltage. Center point of the split capacitors in three-level NPC topology is considered as the power ground in order to simulate CMV. In previous analysis in this thesis, location of the power ground was not crucial. The reason is that all of the previous analysis are done considering differential signals.
When switch node voltages are named as V_a, V_b and V_c for three phases and potential of center of split capacitors is named as V_g, common mode voltage of an inverter is calculated as in (5.6).

$$CMV = \frac{V_{ag} + V_{bg} + V_{cg}}{3} \tag{5.6}$$

Simulation results of two-level and three-level NPC topologies under rated torque and speed operation are given in Figures 5.11-5.14.

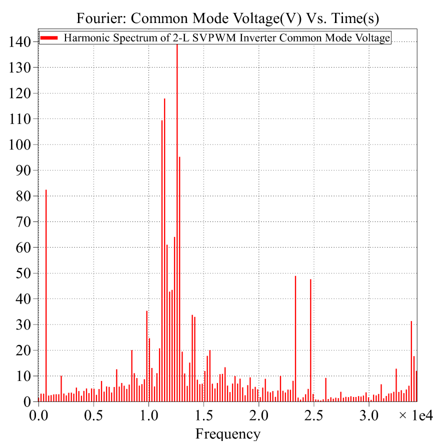


(a) Two-level topology SPWM CMV harmonic content

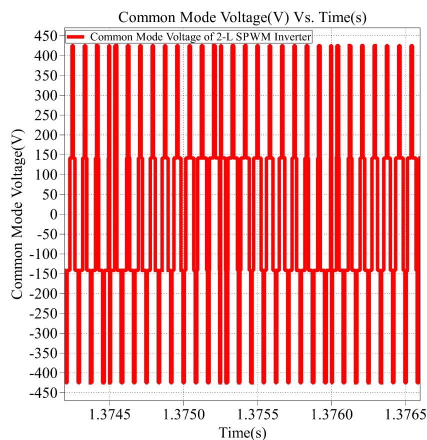


(b) Two-level topology SPWM CMV

Figure 5.11: Two-level topology SPWM CMV and harmonic spectrum

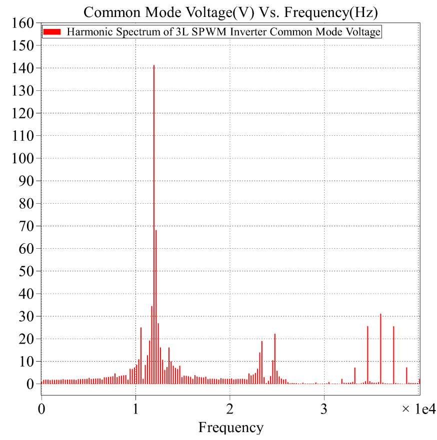


(a) Two-level topology SVPWM CMV harmonic content

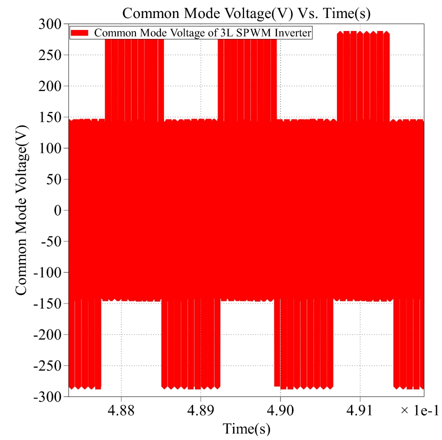


(b) Two-level topology SVPWM CMV

Figure 5.12: Two-level topology SVPWM CMV and harmonic spectrum

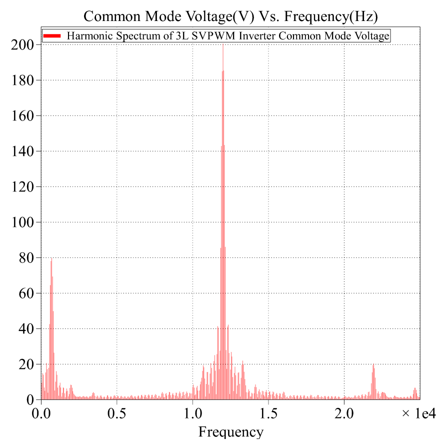


(a) Three-level topology SPWM CMV harmonic content

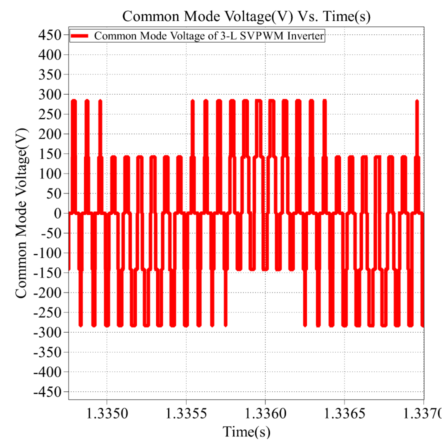


(b) Three-level topology SPWM CMV

Figure 5.13: Three-level topology SPWM CMV and harmonic spectrum



(a) Three-level topology SVPWM CMV harmonic content



(b) Three-level topology SVPWM CMV

Figure 5.14: Three-level topology SVPWM CMV and harmonic spectrum

It is clearly seen that, three level NPC topology has less CMV in terms of magnitude for both of the switching techniques. Comparison is done under 12 kHz switching frequency for both topology and both switching techniques. The only difference in switching techniques is that third harmonic content is not negligible in SVPWM method. However; third harmonic does not have significant effect on EMI perfor-

mance, since fundamental frequency of CMV and resonance frequency due to high dV/dt are the most important factors effecting EMI. When two topologies and two switching techniques are considered, three-level NPC topology has a superior performance in terms of CMV magnitude. Main component of CMV is seen at vicinity of switching frequency of the inverter, where magnitude of CMV of three-level NPC topology is almost half of the two-level topology. Besides, it is clearly seen that switching technique of inverter does not have a significant effect on CMV.

Another important feature of three-level NPC topology in terms of CMV is as follows: CMV fundamental component is at switching frequency. Main component of CMC is proportional with fundamental component of the CMV. On the other hand, CMC path is capacitive especially in AC motor drive applications. Therefore; dV/dt ratio of CMV gains importance since high dV/dt generates higher current during voltage transients. Also CMC flowing during voltage transient of CMV generates much higher frequency current components due to parasitic nature of converter. These currents could result electromagnetic interference issues on the systems especially sharing common power supplies. Therefore; three-level NPC topology has superior performance by considering these currents as well. Lower dV/dt results in a better EMI performance as discussed in [40] and [41].

5.6 Conclusion

A multidimensional comparison of two topologies is done with two different switching techniques. Three-level NPC VSI topology is superior in both thermal performance and output quality point of views. Conduction losses are dominant in three-level topology. However; due to lower collector-emitter blocking voltage requirement, 650V IGBT products can be used in three-level design. Therefore; switching losses have minor effect in three-level topology for the same switching frequencies. For the given semiconductors, two-level topology is limited with 12 kHz switching frequency. On the other hand, three-level topology can reach 22 kHz switching frequency for the same maximum junction temperature limitation. Therefore; three-level topology is superior for applications such that high fundamental frequency is needed. By the help of higher switching frequency, higher bandwidth control performance

could be achieved. However; this inference is valid for conventional Si IGBT diode pairs. With the recent developments in semiconductor technologies, higher switching frequency operation in such power levels with two-level topology is possible as SiC MOSFETs have better switching performance than conventional Si IGBTs [1]. Thermal performance effect of switching techniques is not significant in both topologies. SVPWM has a better output current THD performance compared with SPWM in both topologies. Therefore; SVPWM technique can be preferable due to low THD at the output. Additionally, due to better DC bus utilization, SVPWM can also be preferable in order to decrease DC bus voltage level and switching losses. Although three-level SVPWM is able to achieve a superior performance in all dimensions, three-level topology has some drawbacks. Floating capacitor voltage balancing, manipulation of higher number of switches make three-level topology more challenging compared with two-level topology. Also higher number of switches increases initial cost.

CHAPTER 6

THERMAL RELIABILITY

With the trend of designing more compact, more reliable and more efficient power converters, thermal performance of power electronics equipment has been gaining importance. In the literature, it is stated that most of the power converter failures are due to semiconductors and electrolytic capacitors. Therefore; two weakest components of the power converters are power semiconductors and electrolytic capacitors. Electrolytic capacitor reliability issues have been investigated in the literature [42], [43], [44]. Electrolytic capacitors provide good storage and lower cost in conventional applications. However; they have higher equivalent series resistance values compared with film capacitors. Therefore; thermal stresses could result in failure of electrolytic capacitors in a power converter. On the other hand, film capacitors provide lower series equivalent resistance. Therefore; in reliability critical applications, film capacitors are used instead of electrolytic capacitors [45]. In this thesis, reliability effect of electrolytic capacitors are out of scope. Only semiconductor based reliability results are discussed.

In order to understand thermal reliability issues of a semiconductor, its internal structure should be understood first. In the literature, reliability issues have been mostly studied for high power converters. Therefore; most of the studies have been focused on IGBT thermal reliability issues. In this thesis, a 120 kW PMSM motor drive is under investigation and Si IGBTs and Si diodes are used as semiconductors. Therefore; IGBT module thermal reliability is under investigation in this study as well. IGBT modules consist of different internal layers, which are connected to each other with various methods. Additionally, these are various semiconductor packaging techniques. Reliability of IGBT modules mostly affected by those connection and pack-

aging methods. In Figure 6.1, an IGBT's structural details are shown. In an IGBT, each layer has different thermal expansion coefficient (CTE). Therefore, when an IGBT is heated up or cooled down, different expansions of adjacent layers may damage IGBT structure due to thermo-mechanical stresses in long-term. In the literature, two types of cycling categories in terms of temperature are defined [46]. First one is power cycling [47]. Power cycling is due to power losses of semiconductor under loading condition and has low time constant. Therefore; reasons of power cycle are mission profile or load profile of a power converter. For instance, if a power converter operates in a pulse power application (i.e. elevator motor drive), number of power cycles due to load dependent thermal swings on the semiconductors would be higher. Other cycling term is called thermal cycles. Thermal cycle represents slower changes in the temperatures of IGBT modules. Change of seasons in a year in an open environment can be counted as thermal cycle for a power converter. The main difference between power cycle and thermal cycle is time constants of change of temperature of the semiconductors. Slower changes are counted as thermal cycle and faster changes are counted as power cycle in most of the applications.

In order to analyze reliability of semiconductors under thermal stresses, it is hard to observe a power converter in the field. The reason is as follows: A power converter operates in the field at least for 15 to 20 years until a semiconductor failure occurs. Moreover, there are other reasons such as manufacturing based problems, humidity based problems etc. that can cause failure. Other failure reasons are out of scope of this thesis.

Instead of observing reliability of a semiconductor in the field, researchers have developed a method called accelerated life tests. In accelerated life tests, a general methodology is to test a semiconductor module under power cycles. Junction temperature of semiconductor that is called device under test (DUT) are swinged between known temperatures. These tests are applied to many semiconductors until modules are failed. Lifetime curves are extracted with the light of accelerated tests depending on different parameters. In the literature, methods of power cycling tests are investigated and mathematical approaches are derived in order to calculate lifetime of the semiconductor under different mission profiles.

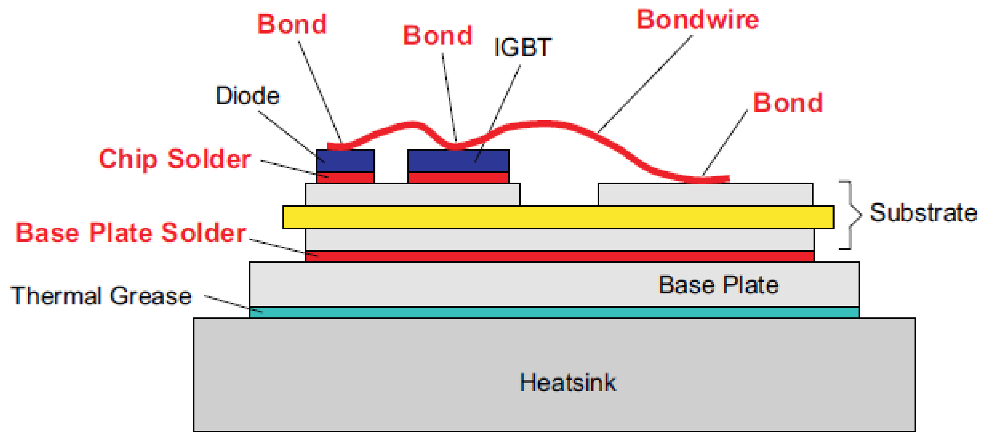


Figure 6.1: IGBT structral details [4]

Real drive cycles are used to make thermal designs in the literature. In [48], thermal design of the inverter was done under FTP-72 drive cycle by assuming 65^oC ambient temperature. Only thermal design was considered in that paper. In [49], lifetime estimation of IGBTs with FTP-75 mission profile is done under 60^oC ambient temperature. Thirty years of lifetime is calculated under this mission profile and assumed thermal constraints.

Semiconductor manufacturers focus on improving connection technique of internal layers where semiconductors mostly fail in life tests. In [46], different power cycle profiles are applied to IGBT modules. Then different failure mechanisms and places are observed with different mean and swing of junction temperatures. In [50], reliability enhancement by not using base plate and using different connection techniques instead of soldering is shown. Trend in IGBT manufacturing is to develop better connection between layers having different thermal expansion coefficients or completely remove connection parts.

The lifetime approach determination flow chart is given in Figure 6.2. In order to calculate lifetime of a semiconductor in power electronics circuit, thermal stresses on the semiconductors must be analyzed for all operation conditions. Mission profile of the semiconductor should be determined. With the mission profile, losses of semiconductor P_{loss} should be calculated. After loss calculation, thermal stresses on the semiconductor should be determined. After extracting junction temperature profile of semiconductor, thermal stress on the semiconductor can be counted with a method

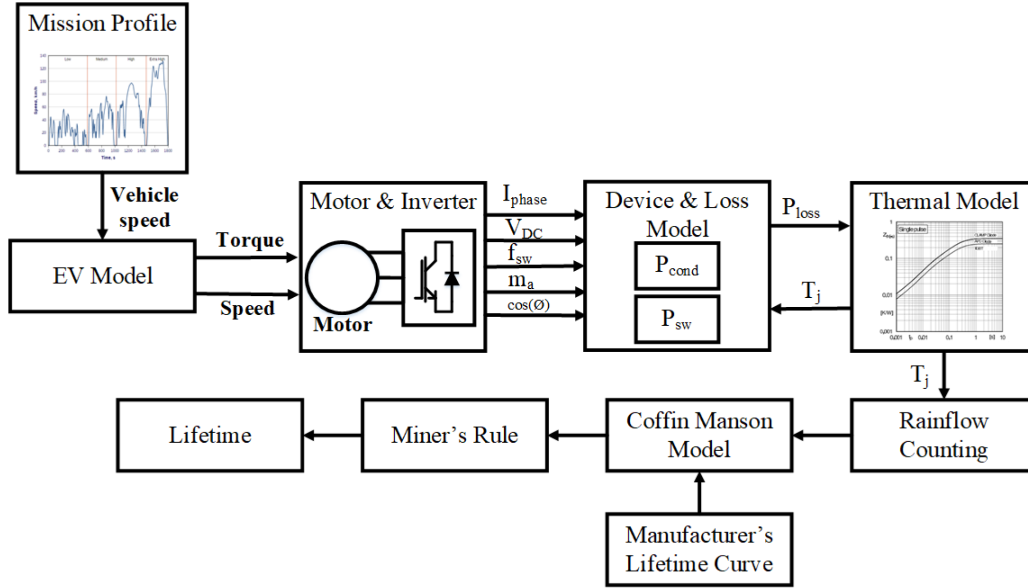


Figure 6.2: Lifetime approach flowchart

called rainflow counting algorithm. After determining thermal swings that the semiconductor faces during operation, degradation of semiconductor is analyzed with the lifetime curve of the semiconductor that is provided by semiconductor manufacturer. The most common method is known as Coffin Manson Law in the literature. In this approach, mean of the junction temperature T_{jm} and temperature swings ΔT_j are the most critical parameters. In recent studies, different parameters affecting lifetime of an IGBT are studied such as on time of power cycles [51], [52] as well, but those are not considered in this study. Finally, with the help of Coffin Manson model and Miner's rule, lifetime of the semiconductor is calculated. Details of the lifetime estimation methodology is explained in the next section.

6.1 Method Overview

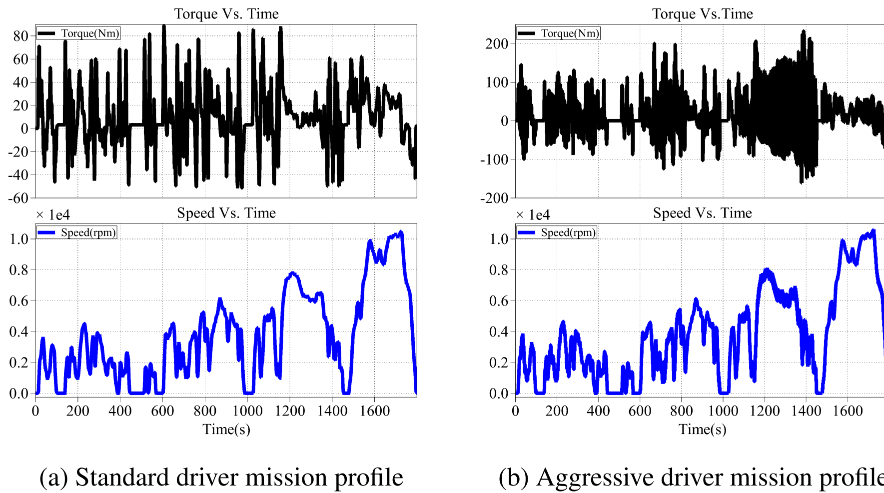
Methodology applied to calculate lifetime of the inverter is as mentioned in Figure 6.2. WLTP mission profile is the input of EV model. EV model generates torque and speed values for the inverter and motor models. Phase current I_{phase}, DC bus voltage V_{DC}, switcing frequency f_{sw}, modulation index m_a and power factor cos(ϕ) are the outputs of motor inverter block. V_{DC} and f_{sw} do not change during the operation. Other parameters are calculated from motor equations and generate input for device

and loss model. Device and loss model block calculates conduction and switching losses of the inverter by the help of mathematical formulations. Output of the block generates input for the thermal model of the inverter. Outputs of thermal model are the junction temperatures of IGBTs and diodes. Device and loss model block also uses junction temperature T_j as input to include variation of semiconductor losses with junction temperature. Junction temperatures are input of the rainflow counting algorithm. Output of rainflow counting algorithm generates input of Coffin Manson model with manufacturer's lifetime curve. Then accumulated damage is calculated with Miner's rule. As a result of the method, lifetime estimation is completed.

6.1.1 Mission Profiles

Mission profiles or load profiles are simply load of a power converter within an operating cycle and depend on the application. Mission profile is one of the most critical inputs of the thermal reliability calculations since it is directly used to generate input for loss calculations. For a wind power, mission profile depends on wind speed of the environment. In [53], reliability analysis of a wind power converter with different wind speed profiles are analyzed. In solar inverters, mission profile of an inverter is determined via solar irradiance of the environment. In [54], reliability analysis methodology of a mission profile based solar inverter is explained. In electric vehicle motor drive applications, mission profiles are based on speed profile of an electric vehicle. Recorded speed curve within a choosen period could be used as a mission profile. For commercial cars there are two main drive cycles in order to measure CO_2 emission rates that are NEDC (New European Drive Cycle) and WLTP (World Harmonized Light Vehicle Test Procedure). In [55], both NEDC and WLTP speed profiles are given and it is stated that WLTP is the more common profile. Speed curve of WLTP is used as a basis of mission profile in thesis. The mission profiles for electric vehicle applications only include speed curves. On the other hand, torque profile that depends on vehicle and driver characteristics is also needed to be able to calculate losses in a motor drive. Therefore; in the thesis, same speed profile under two different torque profiles representing a standard driver and an aggressive driver are used. The difference between two drivers is as follows: Standard driver accelerate and decelerate by applying lower torque. On the other hand, aggressive driver applies

higher torque to the wheel to follow speed reference. The corresponding torque and speed data with respect to time curves are given in Figure 6.3a and Figure 6.3b.



(a) Standard driver mission profile

(b) Aggressive driver mission profile

Figure 6.3: Two different mission profile as drive cycle

For each mission profile, speed curves are almost the same. The main difference between them is torque characteristics. Aggressive driver has higher torque ripples at the motor side to follow speed reference. These huge torque ripples result in ripples at the speed of motor as well.

6.1.2 Electro-thermal Model of Inverter

The thermal model of the two-level topology is shown in Figure 6.4. As can be seen, thermal model of the inverter consists of Cauer R-C rungs of IGBTs and diodes, heatsink R-C pair and thermal interface material if exists. Thermal model of the three-level NPC topology is constructed with the same way with higher number of switches in the model. Input of the thermal model is power loss of each individual semiconductor. Output of the thermal model is node temperatures. Junction temperatures are also used in loss calculations. With the given torque and speed profiles, motor and inverter block generates necessary parameters for loss calculation for the device and loss model and device and loss model takes voltage, current, switching frequency, power factor, modulation index parameters and junction temperatures of semiconductors as input. Device switching model generates semiconductor losses as

output by these inputs as explained in previous chapters.

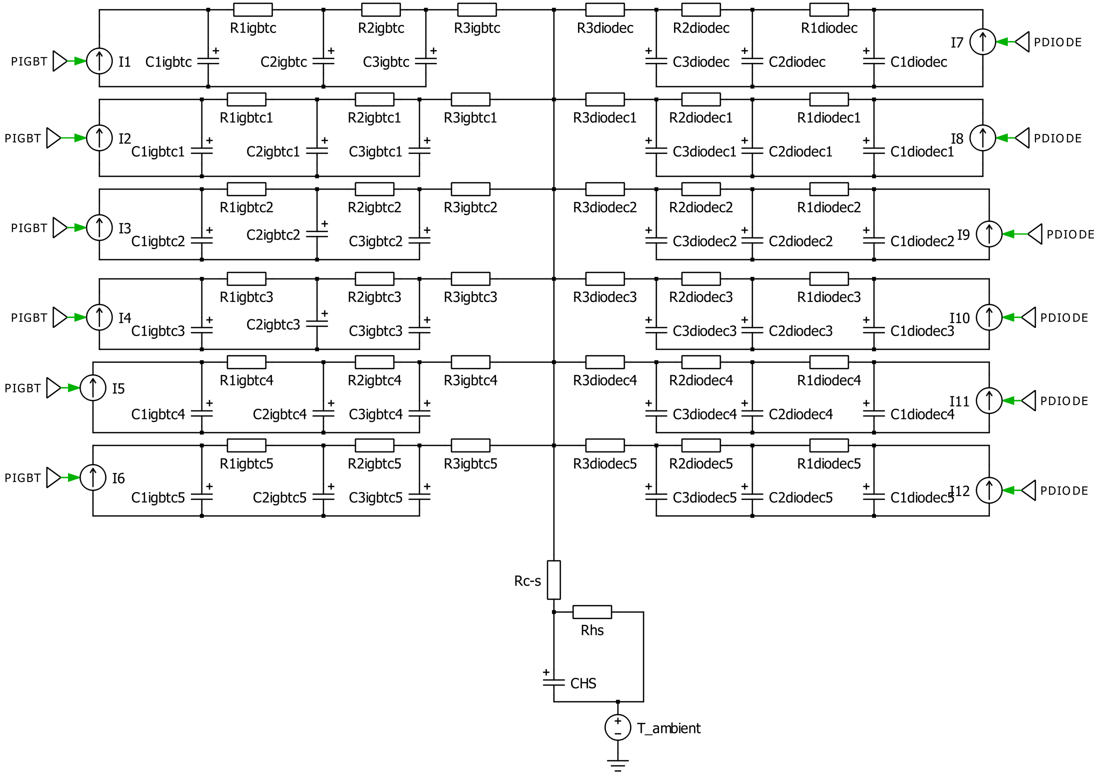


Figure 6.4: Two-level topology thermal model

While computing device switching model, different time constants are valid in terms of losses. First one is switching period of an inverter. Loss ripples at switching period is ignored since temperature changes during switching period are too small and lifetime estimation is not able to cover these small changes, since it is hard to construct a mathematical model for these kind of short thermal ripples experimentally. Second one is output fundamental period. At these frequency, there is also a temperature ripple at semiconductors. These are again too small to effect lifetime of semiconductors. In [4], it is described that switching frequency thermal ripple and fundamental frequency thermal ripple can be ignored. Therefore, as described in previous chapters, DC losses are calculated in order to calculate lifetime of semiconductors. Mission profile torque and speed values are taken as input at a 1 s period and software calculates power losses of semiconductors and junction temperatures.

6.1.3 Rainflow Counting Algorithm

Rainflow counting algorithm is the most common and accepted method to count mechanical stresses on a component [56]. In this analysis, semiconductors are faced with different thermal stresses in terms of junction temperature. This method is used to determine how many thermal cycles a semiconductor faces during operation. As a counting algorithm example, fatigue vs. time graph is given in Figure 6.5.

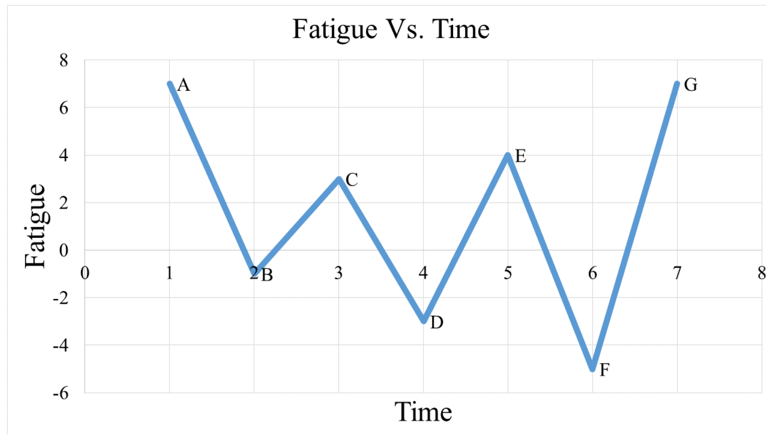


Figure 6.5: Example fatigue profile

Principle of the algorithm can be explained by using the data as below:

1) Y=|A-B| and X=|B-C|. X<Y, so you move to next point, D.

2) Y=|B-C| and X=|C-D|. X>=Y, so |B-C| is counted as one cycle, and points B and C are discarded. Mean of the cycle is 1 and range of the cycle is 4.

3) Y=|A-D| and X=|D-E|. X<Y, so move to the next point, F.

4) Y=|D-E| and X=|E-F|. X>=Y, so |D-E| is counted as one cycle, and points D and E are discarded. Mean of the cycle is 0.5 and range of the cycle is 7.

5) Y=|A-F| and X=|F-G|. X>=Y, so |A-F| is counted as one cycle, and points A and F are discarded. Fewer than three points are left, so the count is complete.

In here there are two half cycles. A-F and F-G are counted as half cycles. Both half cycle has a mean of 1 and range of 12. The cycles causing damage with this fatigue

profile is given in Table 6.1.

Table 6.1: Cycles that cause damage from the fatigue profile

Points	Range	Mean	Cycles
B-C	4	1	1
D-E	7	0.5	1
A-F	12	1	0.5
F-G	12	1	0.5

After a mission profile is applied to the electro-thermal simulation model, thermal stresses on the semiconductors are calculated via electro-thermal simulation tools. Losses are calculated at each step of the electro-thermal simulation using C code and junction temperatures are actively updated. That is, an active calculation of junction temperatures are done via software. Then rainflow couning algorithm decides which temperatures should be counted as thermo-mechanical stresses on the semiconductor module in the C based software.

6.1.4 Coffin Manson Law

Coffin Manson law is the empirical relation between number of cycles to failure and deformaton. The law is the simplest and most common method for estimating lifetime of semiconductors with thermal stresses. Lifetime curves that are obtained from accelerated life testing are supplied by semiconductor manufacturer companies. Generally Coffin Manson model is generated from experimental data by curve fitting. On the other hand, there are other approaches as discussed in [57]. Norris-Landzberg method is an improved verison of Coffin-Manson law that takes frequency of power cycles into account. Bayerer model is more complex than other two. This approach takes t_{on}, T_{jmax}, DC current applied, diameter of bond wire and blocking voltage parameters into account to calculate lifetime of semiconductor. In conclusion, there are various mathematical approaches supplied by semiconductor manufacturer companies to calculate lifetime. In this thesis, simple Coffin-Manson model is used for the selected semiconductors.

The generic expression of Coffin Manson Law is given in 6.1.

$$N_f = \Delta T_j{}^{\delta} e^{\frac{E_a}{kT_m}} \tag{6.1}$$

where,

N_f : Number of cycles to failure.

E_a : Activation energy

k : Boltzman constant

T_m : Mean junction temperature

It can be inferred that for a specific semiconductor, lifetime depends on thermal ripple ΔT_j through device and mean junction temperature. Other parameters are device specific.

6.1.5 Miner's Rule

Miner's rule is seen as a result of Coffin Manson law. With the help of Miner's rule, degradation of a semiconductor or its remaining lifetime with a thermal stress profile can be extracted. A linear accumulation of damage is assumed in Miner's rule. Miner's rule is detailly explained in [58] for mechanical systems. Also for a voltage source inverter, semiconductor accumulated damage as a result of Coffin-Manson law with a real mission profile is calculated in [59].

Mathematical expression of Miner's rule is as in (6.2). RL represents the remaining life of the semiconductor. When RL equals to zero, the device fails. N_i represents the number of ith cycle from output of rainflow counting algorithm. $N_{EOL,i}$ represents how many cycles that the semiconductor is able to withstand with the thermal stress.

$$RL = 1 - \sum_{i=1}^{n} \frac{N_i}{N_{EOL,i}} \tag{6.2}$$

6.2 Thermal Reliability Results

In previous part, work flow of a lifetime calculation was explained in details. In the light of this work flow, mathematical tools are constructed and life cycle of IGBTs in both topologies driven with SPWM at a constant switching frequency of 12 kHz are determined. WLTP (Worldwide Harmonised Light Vehicle Test Procedure) is used as drive cycle. In thermal reliability comparison, switching techniques are not compared. The reason is that switching technique does not have a significant role on overall power losses of semiconductors as discussed in previous chapter.

In previous chapter, only thermal resistance networks are used as electro-thermal models by considering computational power since comparison of models are conducted only for steady state operation. On the other hand, in real mission profiles, thermal capacitances have a significant effect on thermal stress on the semiconductor. It is because of the fact that semiconductor losses are inputted into the electro-thermal models as step functions in every second and temperature response of each semiconductor with respect to time is crucial while analyzing a real mission profile. Therefore, electro-thermal model extraction of two different modules are done analytically. Foster parameter extraction of IGBT-diode pairs are done with a MATLAB based tool via curve fitting. Confirmation of the software was done by checking transient thermal impedance curve given in datasheet of IGBT and diode pair. Cauer thermal model of semiconductors give a more realistic results especially with thermal interface material due to heat conduction. In this comparison, both modules are directly connected to the heatsink. Therefore, Foster or Cauer Models are both acceptable in order to calculate thermal stresses on semiconductors. However; in order to make a general approach for the calculation, Cauer parameters are extracted from Foster model parameters. The transformation method from Foster equivalent circuit to Cauer equivalent is explained in [60]. Another MATLAB code is used to transform Foster model to Cauer model for both modules. Finally, thermal model transformations are checked by comparing transient responses of Foster and Cauer thermal models.

In the literature, 2 to 3 ladder networks are found as sufficient for transient thermal responses as explained in [4]. Three ladder thermal networks are extracted for both SkiM401MLI07E4 and SKiiP39GB12E4V1. Electro-thermal model parameters of

both module is given in Table 6.2 and 6.3.

Heatsink is modelled as one pair of R-C network with a thermal resistance of $R_{s-a} = 0.023^oC/W$. Thermal capacitance of the heatsink is calculated from its mass and material. Heatsink has a mass of 2.2 kg and specific heat of heatsink material that is alumuinium is given as 0.91 J/g.K. Therefore, thermal capacitance of heatsink is calculated as 2002 Ws/K.

Table 6.2: Thermal model parameters of SKiiP39GB12E4V1

(a) Cauer parameters of SKiiP39GB12E4V1

	IGBT	DIODE
R1	0.0213	0.0252
R2	0.1275	0.1513
R3	0.0136	0.0160
C1	0.0494	0.0419
C2	0.9752	0.8208
C3	66.9564	62.0324

(b) Foster parameters of SKiiP39GB12E4V1

	IGBT	DIODE
R1	0.1247	0.0211
R2	0.0193	0.1486
R3	0.0184	0.0228
C1	1.0296	47.7678
C2	0.0519	0.8649
C3	50.2985	0.0441

Table 6.3: Thermal model parameters of SkiM401MLI07E4

(a) Cauer parameters of SkiM401MLI07E4

	IGBT	DIODE
R1	0.0220	0.0650
R2	0.1036	0.1964
R3	0.1206	0.0858
C1	0.1292	0.1294
C2	0.3005	0.3640
C3	1.2802	2.4981

(b) Foster parameters of SkiM401MLI07E4

	IGBT	DIODE
R1	0.1810	0.1237
R2	0.0101	0.1907
R3	0.055	0.0328
C1	1.2136	0.6147
C2	0.1926	1.4682
C3	0.5801	0.1844

Two different mission profiles are extracted for WLTP as explained above. Effect of mission profile on thermal reliability of motor drive is investigated beside topology comparison. Loss calculation of the semiconductors were explained detailly in the

previous parts. From given torque and speed characteristics, current, voltage and power factor values are extracted and DC loss calculations are carried out by using the PLECS simulation tool.

In order to compare two topologies with the test mission profiles, 30 minutes of torque and speed curves are implemented as input to the software. Semiconductor stresses are analyzed seperately. In two level topology, only diodes and IGBTs are analyzed seperately. On the other hand; in three-level NPC topology, two different IGBT thermal profile and three different diode thermal profiles are analyzed. The reason is as follows: In a power semiconductor module, life of the module is determined by the weakest part. Although, one of the semiconductors does not face with high thermal stresses. In two-level topology, loss distribution of all diodes is identical and that is also the case for all IGBTs. On the other hand, in three-level NPC type topology, semiconductors have different thermal stresses. Considering the semiconductor elements in 1st leg, only IGBT 1 and 4, diode 1 and 4, IGBT 2 and 3, diode 2 and 3, clamping diodes 5 and 6 are equally heated. Therefore in two-level topology, motor drive can be seperated into two parts in terms of thermal analysis and in three-level NPC type topology, motor drive is seperated into five parts in terms of thermal analysis.

In thermal simulations, ambient temperature is assumed to be 60 ^oC. While calculating thermal stresses via simulation, thermal steady states are assumed. Therefore, 1800 s WLTP mission profiles are applied to the electro-thermal methods repetitively until thermal steady state is reached. It is seen that thermal steady state is achieved after two or three repetitions. All simulation results are obtained from the fifth cycle. That is simulation results shown in this part represents electro-thermal results of the electric car between 7200 and 9000 seconds time interval.

Lifetime of the semiconductors are determined by assuming that 30 minutes of mission profiles are applied to the motor drive repeatedly until one of the semiconductors are damaged. Calculations are done for IGBTs and diodes seperately. The semiconductor having minimum lifetime determines the lifetime of the motor drive. In order to calculate lifetime of semiconductors, first their lifetime curves were analyzed. For spring contacted IGBT diode modules 'Standard IGBT lifetime curve' is recom-

mended in [4]. Both IGBT modules have spring contacted packages. Therefore, the same Coffin-Manson law parameters are accepted for both of the modules. The life-time curve for both modules are shown in Figure 6.6 for different mean temperatures. By the help of these curves, an Arrhenius relation used to apply Coffin-Manson law was extracted. Coefficients of Arrhenius relation is taken from [61]. A coefficient of 'A' that is Arrhenius term is added to the formulation in addition to Coffin Manson law. This relationship given in (6.3) is to calculate number of cycles to failure of each semiconductor.

$$N_f = A \Delta {T_j}^{\delta} A^{\overline{\frac{E_a}{kT_m}}} \tag{6.3}$$

where,

A : Constant (648000)

E_a : Activation energy (9.89110^{-23})

k : Boltzman constant (1.3810^{-23})

T_m : Mean junction temperature

N_f : Number of cycles to failure

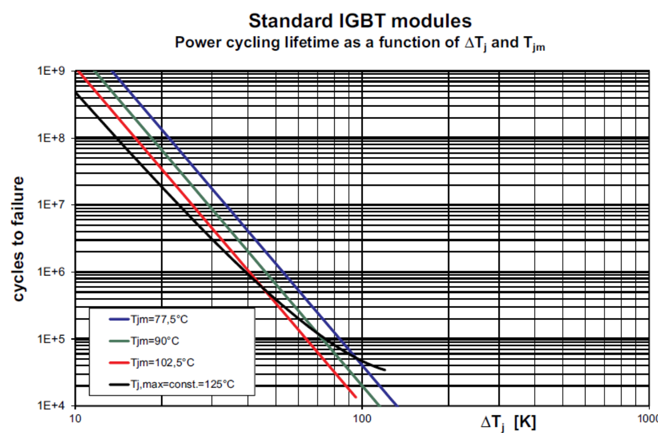
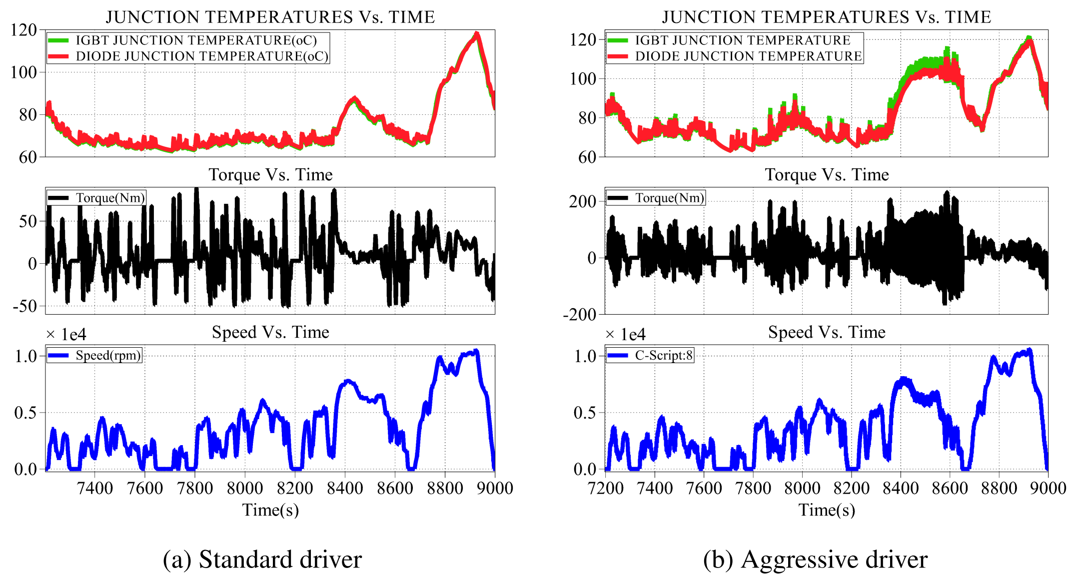


Figure 6.6: Lifetime curve with different mean junction temperatures [4]

Two-Level Topology Results

First analysis is done with two-level topology. Thermal stresses on an IGBT-diode pair and torque, speed curves with respect to time are shown in Figure 6.7a for a standard driver. Two-level topology electro-thermal simulation results with an aggressive driver are given in Figure 6.7b.



(a) Standard driver

(b) Aggressive driver

Figure 6.7: IGBT and diode temperatures of two-level topology

Estimated lifetimes for two-level toplogy for the selected mission profiles are given in Table 6.4. It is clearly seen that driving profile has a crucial impact on lifetime of the semiconductors.

For both of the standard and aggresive driver's profiles, it is clearly seen that absolute maximum and minimum junction temperature peak points do no differ significantly. On the other hand, aggressive driver always applies more torque to follow the speed references. This results in larger torque ripples in the profile. Larger torque ripples result in larger speed ripples in the profile. Aggressive driver's profile draws larger currents from motor drive than standard driver's profile averagely. From the electro-thermal simulation results, it can be inferred that short time constant thermal ripples are more frequent in aggressive driver's profile. The results of Rainflow Counting algorithm shows that number of thermal cycles are much higher in aggressive driver's

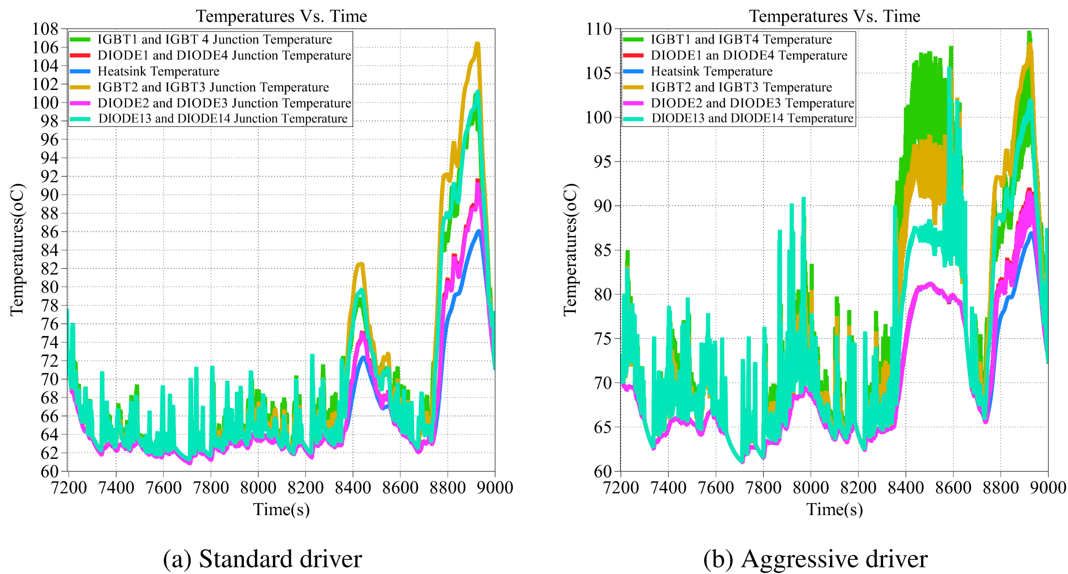
mission profile. Therefore, lifetime of semiconductors with an aggressive driver's profile is shorter.

Table 6.4: Lifetime of IGBT and diode with different mission profiles in two-level topology

Semiconductor	Mission Profile	Lifetime(years)
IGBT	Standard	41.6
Diode	Standard	37.0
IGBT	Aggressive	**16.6**
Diode	Aggressive	25.6

Three-level Topology Results

In three level topology, thermal reliability comparison is more complicated than two-level case. Total of five semiconductor groups should be investigated. Standard and aggressive drivers' thermal profiles are given in Figure 6.8a and Figure 6.8b, respectively.



(a) Standard driver

(b) Aggressive driver

Figure 6.8: Three-levöel topology IGBT and diode temperatures

In Table 6.5, lifetime algorithm results are given, where applied mission profiles and semiconductor's lifetimes can be seen. In standard mission profile, lifetime is determined by inner main switches IGBT 2-3 that are connected to switch nodes of the phase leg. On the other hand; in aggressive driver's mission profile, it is seen that lifetime is determined by IGBT 1-4 that are outer main switches of the leg. Although high time constant temperature swings are similar in each case, small temperature swings having low time constants are more effective in aggressive driver's mission profile and determine the lifetime of the converter.

Table 6.5: Lifetime of IGBT and diode with different mission profiles in three-level NPC topology

Semiconductor	Mission Profile	Lifetime(years)
IGBT 1-4	Standard	296.0
Diode 1-4	Standard	1579.3
IGBT 2-3	Standard	**125.6**
Diode 2-3	Standard	1718.2
Diode 5-6	Standard	288.4
IGBT 1-4	Aggressive	**37.2**
Diode 1-4	Aggressive	1508.8
IGBT 2-3	Aggressive	51.06
Diode 2-3	Aggressive	1633.0
Diode 5-6	Aggressive	70.0

Comparison

For a standard driver profile, three-level NPC type topology looks superior in terms of semiconductor reliability. Estimated lifetime is 125.6 years limited by the inner IGBTs of each leg (IGBT 2-3). Therefore, it would not result in failure in the real application. For two-level topology, 37 years lifetime of diodes look weakest part of the topology for a standard driver. For agressive driver mission profile, 37.2 years lifetime of IGBT 1-4 in the three-level topology is the shortest among semiconductor modules. For two-level topology, 16.6 years lifetime of IGBTs should be considered

as a critical point.

It should be kept in mind that other failure mechanisms of the motor drive system should be considered to estimate lifetime of motor drive.

6.3 Conclusion

In this chapter, a general description of thermal reliability of semiconductors are given. It is stated that for a real mission profile, lifetime estimation of semiconductors were already discussed for different applications in the literature. On the other hand; in this chapter, reliability analysis of electric vehicle drives is conducted by considering driver profiles. By analyzing different profiles, it is implied that absolute maximum and minimum values do not differ significantly. Therefore; heatsink sizing, switching frequency, passive components do not strictly dependent on the driver. On the other hand, aggressive driving result in low time constant thermal ripples at the electrical drive side. Therefore, it is clearly seen that lifetime of semiconductors are highly affected by mission profile of the electric vehicle even both profiles have the same speed curves.

CHAPTER 7

CONCLUSION

Previous studies that focuses on commercial EV products indicate a general trend that more compact, more efficient, cheaper and lighter EV drive systems are needed to be designed for electric vehicles to have a bigger market share. High speed electric machines driven by higher DC link voltages are preferable in order to reach these goals. Although all conventional EV drive systems use two-level topology, three-level NPC topology is seen as a good candidate for near future products due to its better performance at high DC link voltages. Especially, high bandwidth semiconductor products and multi-level topologies would be a perfect match for EV applications. Therefore, this study is carried out to explore advantages and disadvantages of three-level topology in vehicle traction applications.

First of all, two-level and three-level NPC topologies are analyzed with two switching techniques. Three-level NPC type topology is found to have a superior thermal performance and lower common mode voltage. Also, SVPWM technique is advantageous on SPWM by means of output current THD, common mode voltage and DC bus utilization point of views. On the other hand, it is clearly seen that switching technique does not have a significant effect on thermal characteristics of semiconductors. Also, a three-level NPC type topology inverter having rated power of 750 W was designed and tested with resistive load to identify the challenges of multi-level system. In addition to floating DC link voltage and need for isolated gate drivers, three-level system needs to be designed carefully considering computation capability and peripheral facilities of DSP or microcontroller.

Secondly, thermal reliability of semiconductors were explained conceptually. Thermal cycle and power cycle concepts were explained and why power semiconductor

modules are damaged due to thermal stresses was studied. After that, methodology of lifetime estimation of IGBT and diode pairs were explained in details. Using this method, comparison of two-level and three-level NPC type topology in terms of thermal reliability of semiconductors were achieved for two different mission profiles obtained from WLTP drive cycle with standard and aggressive driver profile. Aggressive driver profile results in less lifetime of semiconductors for both topologies. IGBT lifetime in aggressive driver and two-level topology case is estimated as 16.6 years. On the other hand, semiconductor lifetimes are estimated as much longer in other three cases. Therefore; it can be inferred that electric drive failure would occur due to another failure mechanisms in these cases.

Since EV drive systems require more compact power electronics parts, thermal reliability of semiconductors gain more importance. Especially thermal reliability of wide-bandgap power semiconductors will be very critical. All analyses were done with Si IGBT and diodes in the thesis. Therefore, thermal analyses with SiC MOSFETs or GaNFETs would be analyzed for EV applications as a future work. Also commercial GaNFET products block 650 V. Therefore; combination of GaNFETs with three-level NPC type topology would be a great research area for EV drive systems due to increased DC bus voltages. Moreover, efficiency of the overall drive system in the presence of a three-level or multi-level inverter can be investigated to find out the effect of inverter topology on electric machine losses.

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APPENDIX A

THREE-LEVEL NPC SVPWM GATE SIGNALS

PPO Tc/4	POO Ta/4	OOO Tb/2	OON Tc/4	ONN Ta/2	OON Tc/4	OOO Tb/2	POO Ta/4	PPO Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.1: Sector 1, sub-sector 1

PPO Tc/4	POO Ta/4	PON Tb/2	OON Tc/4	ONN Ta/2	OON Tc/4	PON Tb/2	POO Ta/4	PPO Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.2: Sector 1, sub-sector 2

PPO Tc/4	PPN Ta/2	PON Tb/2	OON Tc/2	PON Tb/2	PPN Ta/2	PPO Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.3: Sector 1, sub-sector 3

POO Ta/4	PON Tb/2	PNN Tc/2	ONN Ta/2	PNN Tc/2	PON Tb/2	POO Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.4: Sector 1, sub-sector 4

NON Tc/4	OON Ta/4	OOO Tb/2	OPO Tc/4	PPO Ta/2	OPO Tc/4	OOO Tb/2	OON Ta/4	NON Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.5: Sector 2, sub-sector 1

NON Tc/4	OON Ta/4	OPN Tb/2	OPO Tc/4	PPO Ta/2	OPO Tc/4	OPN Tb/2	OON Ta/4	NON Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.6: Sector 2, sub-sector 2

NON Tc/4	NPN Ta/2	OPN Tb/2	OPO Tc/2	OPN Tb/2	NPN Ta/2	NON Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.7: Sector 2, sub-sector 3

OON Ta/4	OPN Tb/2	PPN Tc/2	PPO Ta/2	PPN Tc/2	OPN Tb/2	OON Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.8: Sector 2, sub-sector 4

OPP Tc/4	OPO Ta/4	OOO Tb/2	NOO Tc/4	NON Ta/2	NOO Tc/4	OOO Tb/2	OPO Ta/4	OPP Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.9: Sector 3, sub-sector 1

OPP Tc/4	OPO Ta/4	NPO Tb/2	NOO Tc/4	NON Ta/2	NOO Tc/4	NPO Tb/2	OPO Ta/4	OPP Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.10: Sector 3, sub-sector 2

OPP Tc/4	NPP Ta/2	NPO Tb/2	NOO Tc/2	NPO Tb/2	NPP Ta/2	OPP Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.11: Sector 3, sub-sector 3

OPO Ta/4	NPO Tb/2	NPN Tc/2	NON Ta/2	NPN Tc/2	NPO Tb/2	OPO Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.12: Sector 3, sub-sector 4

NNO Tc/4	NOO Ta/4	OOO Tb/2	OOP Tc/4	OPP Ta/2	OOP Tc/4	OOO Tb/2	NOO Ta/4	NNO Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.13: Sector 4, sub-sector 1

NNO Tc/4	NOO Ta/4	NOP Tb/2	OOP Tc/4	OPP Ta/2	OOP Tc/4	NOP Tb/2	NOO Ta/4	NNO Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.14: Sector 4, sub-sector 2

NNO Tc/4	NNP Ta/2	NOP Tb/2	OOP Tc/2	NOP Tb/2	NNP Ta/2	NNO Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.15: Sector 4, sub-sector 3

NOO	NOP	NPP	OPP	NPP	NOP	NOO
Ta/4	Tb/2	Tc/2	Ta/2	Tc/2	Tb/2	Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.16: Sector 4, sub-sector 4

POP	OOP	OOO	ONO	NNO	ONO	OOO	OOP	POP
Tc/4	Ta/4	Tb/2	Tc/4	Ta/2	Tc/4	Tb/2	Ta/4	Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.17: Sector 5, sub-sector 1

POP Tc/4	OOP Ta/4	ONP Tb/2	ONO Tc/4	NNO Ta/2	ONO Tc/4	ONP Tb/2	OOP Ta/4	POP Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.18: Sector 5, sub-sector 2

POP Tc/4	PNP Ta/2	ONP Tb/2	ONO Tc/2	ONP Tb/2	PNP Ta/2	POP Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.19: Sector 5, sub-sector 3

OOP Ta/4	ONP Tb/2	NNP Tc/2	NNO Ta/2	NNP Tc/2	ONP Tb/2	OOP Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.20: Sector 5, sub-sector 4

ONN	ONO	OOO	POO	POP	POO	OOO	ONO	ONN
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.21: Sector 6, sub-sector 1

ONN Tc/4	ONO Ta/4	PNO Tb/2	POO Tc/4	POP Ta/2	POO Tc/4	PNO Tb/2	ONO Ta/4	ONN Tc/4
S1								
S2								
S3								
S4								
S5								
S6								

Figure A.22: Sector 6, sub-sector 2

ONN Tc/4	PNN Ta/2	PNO Tb/2	POO Tc/2	PNO Tb/2	PNN Ta/2	ONN Tc/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.23: Sector 6, sub-sector 3

ONO Ta/4	PNO Tb/2	PNP Tc/2	POP Ta/2	PNP Tc/2	PNO Tb/2	ONO Ta/4
S1						
S2						
S3						
S4						
S5						
S6						

Figure A.24: Sector 6, sub-sector 4