Bull. Mater. Sci. (2018) 41:66
https://doi.org/10.1007/s12034-018-1586-2

Influence of Si_3N_4 layer on the electrical properties of Au/n-4H SiC diodes

FATIH YIGITEROL[1], HASAN H GULLU[2,3,4] and ESRA D YILDIZ[1,*]

[1]Department of Physics, Hitit University, 19030 Çorum, Turkey
[2]Central Laboratory, Middle East Technical University, 06800 Ankara, Turkey
[3]Center for Solar Energy Research and Applications (GÜNAM), Middle East Technical University, Ankara 06800, Turkey
[4]Department of Electrical and Electronics Engineering, Atilim University, 06830 Ankara, Turkey
*Author for correspondence (desrayildiz@hitit.edu.tr; desrayildiz@gmail.com)

MS received 18 June 2017; accepted 22 September 2017; published online 16 May 2018

Abstract. In this study, the effect of Si_3N_4 insulator layer on the electrical characteristics of Au/n-4H SiC diode was investigated. The current–voltage ($I-V$), capacitance–voltage ($C-V$) and conductance–voltage ($G/w-V$) measurements were carried out at room temperature condition. Under thermionic emission model, electrical parameters as zero-bias barrier height (Φ_{Bo}), ideality factor (n), interface states (D_{it}), and series (R_s) and shunt (R_{sh}) resistances were estimated from forward bias $I-V$ analyses. The values of n and Φ_{Bo} were about 1.305 and 0.796 eV for metal–semiconductor (MS) rectifying diode, and 3.142 and 0.713 eV for metal–insulator–semiconductor (MIS) diode with the insertion of Si_3N_4 layer, respectively. Since the values of n were greater than the unity, the fabricated diodes showed non-ideal $I-V$ behaviour. The energy distribution profile of D_{it} of the diodes was calculated by taking into account of the bias dependence of the effective barrier height (Φ_e) and R_s. The obtained D_{it} values with R_s are almost one order of magnitude lower than those without R_s for two diodes. According to Cheung's model, R_s were calculated and these values were found in increasing behaviour with the contribution of Si_3N_4 insulator layer. In addition, the J_R-V plot behaviours with linear dependence between $\ln(J_R)$ *vs.* $V^{0.5}$ indicated that the dominant conduction mechanism in the reverse bias region was Schottky effect for both MS and MIS diodes. In the room temperature $C-V$ measurements, different from the results of MIS diode, the values of C for MS diode was observed in decreasing behaviour from ideality with crossing the certain forward bias voltage point (~2.5 V). The decrease in the negative capacitance corresponds to the increase of G/w.

Keywords. MS; MIS; insulator layer; interface states; Si_3N_4 layer; conduction mechanism.

1. Introduction

In recent years, silicon carbide (SiC) structure has attracted considerable attention for photonic and electronic device applications due to unique inherent electrical and high thermal conductivity, indirect wide bandgap (3.0 eV for 6H-SiC and 3.2 eV for 4H-SiC), large critical breakdown of electric field at about 3×10^8 V m^{-1}, high saturation electron drift velocity and high chemical stability [1–4]. Advances in the all aspect of SiC-based devices have directed the researchers because of their potential to compete with Si-based counterparts. Among the wide bandgap semiconductors, it can provide an advantage with its thermally oxidizable characteristic to compose an insulator layer between metal and semiconductor. Therefore, there have been several studies on Schottky barrier height (SBH) characteristics of 6H-SiC [5,6] and 4H-SiC [7,8], in which some of them also developed models to understand the barrier formation in the SiC-based diodes. The formation of barrier height (Φ_B) and interfacial insulator layer in intrinsic or extrinsic origin at metal/semiconductor (M/S) interface, and their inhomogeneity also affect the main electrical parameters [9–14]. This insulating layer generated between semiconductor and metal results in a continuous distribution of interface states, D_{it}, at the interface [9,10]. Although there are many reported works on the electrical characteristics of the MS and MIS (or MOS) devices under the effect of this layer, it is still an open research area to develop a complete understanding [11–23]. Among them, high dielectric constant materials such as Si_3N_4, HfO_2, ZnO_2 and TiO_2 for SiO_2 have attracted attention as an alternative interfacial layer for their applications at M/S interface in electronic structures as MS and MIS devices [18,23–25]. In addition to the high dielectric permittivity characteristic, having low density of D_{it} provides an advantage in device applications. The performance of these devices is characterized by their primary electrical parameters such as σ_B, ideality factor (n), series resistance (R_s) and D_{it}. In general, the $I-V$ plots of MS and MIS diodes are expected to be in linear behaviour on a semi-logarithmic scale at intermediate applied voltage region. On the other hand, it can be deviated from the linearity due to the effect of R_s, D_{it} and interfacial layer when the bias voltage is adequately large

($V \geq 1$ V). The values of R_s and D_{it} can also affect the $C-V$ plots of diodes, and therefore they can cause a bending in $C-V$ plots.

In this study, $I-V$, $C-V$ and $G/w-V$ characteristics of Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes were investigated to determine the effect of insulator (Si_3N_4) layer. Forward and reverse biasing behaviour of diodes were discussed according to Schottky and Poole-Frenkel emission models and device parameters as, n, Φ_B, D_{it} and R_s were also calculated comparatively among these two diodes.

2. Experimental

Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes were fabricated onto a (0001) oriented, 500 μm thick and nitrogen-doped (3.125×10^{16} cm^{-3}) n-type 4H SiC substrates. Before deposition steps, ultrasonic and chemical substrate cleaning procedures by organic solvents of $CHClCCl_2$, CH_3COCH_3 and CH_3OH were applied for 10 min. Following to the cleaning, the surfaces of the SiC substrates were etched in a sequence of H_2SO_4, H_2O_2-HF (20%), HF (20%), a solution of $6HNO_3$:1HF:$35H_2O$ and finally rinsed in 18 MΩ.cm deionized water [26–29]. Then, under 10^{-7} mbar vacuum condition, highly pure (99.999%) Au metal source was thermally evaporated to form ohmic back contacts for the substrates [30]. Substrate temperature in the Au contact deposition was kept constant at 450°C and the final thickness of the contacts was monitored to be around 200 nm. After this process, samples were annealed at 430°C under nitrogen atmosphere to enhance the ohmic contact behaviour. The insulator layer in MIS structure was deposited by magnetron sputtering of a compound Si_3N_4 target at a substrate temperature of 200°C [31]. Finally, MS and MIS diode structures were completed with thermally evaporated dot-patterned Au rectifying contacts in 2 mm diameter and 150 nm thickness, on the front surface of the bare 4H SiC and Si_3N_4 film layer, respectively [32,33]. The schematic diagram of the fabricated Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes is illustrated in figure 1a.

The electrical characterization of these diodes were investigated by room temperature $I-V$, $C-V$ and $G/w-V$ measurements. These measurements were performed by using Keithley 4200 SCS semiconductor characterization system. In addition, the interfacial insulator layer thickness (Si_3N_4) was calculated from measurement of the insulator capacitance ($C_i = C_{ox} = \varepsilon\varepsilon_0 A/d_{ox}$) in the strong accumulation region. Moreover, in order to get a better understanding on the surface morphology of Si_3N_4 layer, atomic force microscopy (AFM) technique was utilized in tapping mode. As seen in figure 1b, Si_3N_4 thin film shows smooth and uniform surfaces; and in addition, the root mean square (RMS) roughness of Si_3N_4 was found to be 0.488 nm.

3. Experimental Results

3.1 *Current–voltage characteristics*

Diode parameters of the fabricated Au/n-4H SiC (MS) and Au/Si_3N_4/n-4H SiC (MIS) diodes were calculated from the room temperature $I-V$ measurements. The experimental forward and reverse bias $I-V$ characteristics of these diodes are presented in figure 2. As seen from this figure, both diode structures show rectifying behaviour with the rectifying ratio (RR) as about 2.2×10^2 and 1.2×10^3 at ±3.8 V for fabricated MS and MIS diodes, respectively. For a MS or MIS diode, the relation between applied forward bias voltage V and resultant current I can be formulated as [9,10,34],

$$I = AA^*T^2 \exp\left(-\frac{q}{kT}\Phi_{Bo}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right], \tag{1}$$

where q is the electronic charge, Φ_{Bo} is the apparent barrier height for zero-bias point at interface, n the ideality factor, k the Boltzmann constant and T the absolute temperature in Kelvin. In this expression, applied voltage, V, was evaluated as the voltage across the diode ($V_D = V - IR_s$) under the effect of R_s. Detailed explanation of diode leakage current can be given as [9],

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right), \tag{2a}$$

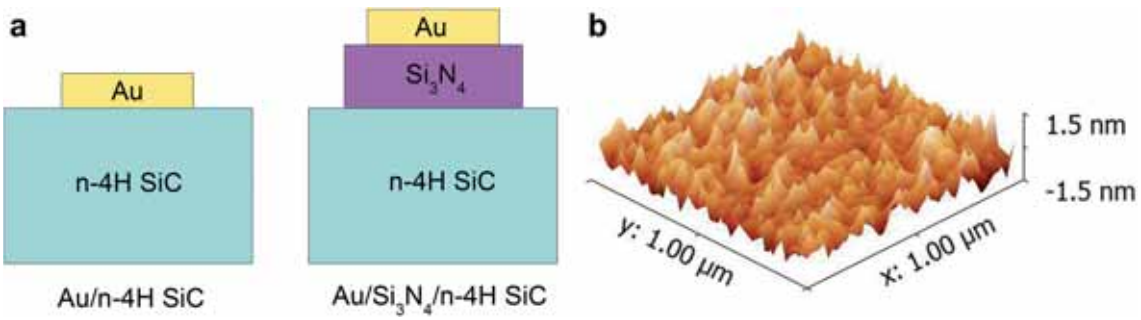

Figure 1. (**a**) The schematic diagram of the Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature and (**b**) AFM image of Si_3N_4 layer.

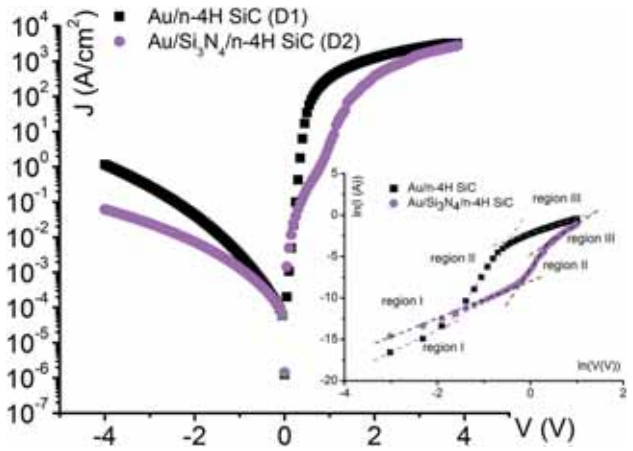

Figure 2. The semi-logarithmic current–voltage and log (I)–log (V) plots of the Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature.

where I_0 is the reverse saturation current due to the minority carriers, A the rectifier contact or diode area, A^* the effective Richardson constant (146 A cm^{-2} K^2 for n-4H SiC [5]).

As observed from figure 2, the $I-V$ curves quite differ from the linearity at high forward bias voltage. This deviation can be attributed to the influences of the presence of insulator layer, density of the interface state D_{it} and the effect of parasitic resistances R_s. In the reverse bias region, the measured current values were observed in increasing behaviour with increase in applied bias voltage and scales up gradually with the reverse bias without any influence of saturation for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes. In this case, non-saturating behaviour of reverse current can be explained in terms of the image force lowering of SBH and the presence of the interfacial insulator layer at M/S interface [9,10,35,36]. Additionally, there is considerable change in the reverse current values with applied bias voltage. As given in figure 2, the magnitude of the leakage current for Au/Si_3N_4/n-4H SiC is lower than Au/n-4H SiC in the reverse bias voltage range of -4 V $\leq$ V ≤ -2.8 V. As a result, Au/Si_3N_4/n-4H SiC diode shows a better RR than Au/n-4H SiC diode due to the decrease in the effects of D_{it} and shunt resistance, R_{sh} [8,36].

From Eq. (1), I_0 values can be extracted from the straight-line intercept of the semi-logarithmic forward biased $I-V$ curve (figure 2) at zero bias voltage point. Additionally, the values of Φ_{Bo} and voltage-dependent effect barrier height (Φ_e) can be obtained from Eq. (2b) and (2c) as [9,10,25]

$$\Phi_{Bo} = kT\ln\left(\frac{AA^*T^2}{I_0}\right) \tag{2b}$$

$$\Phi_e = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s), \tag{2c}$$

where $n(V)$ is the voltage dependent of n, which is the indication of deviation from the ideal TE theory. From Eq. (1), the value of n is calculated from the slope of the linear region of the forward bias ln $I-V$ plot and it can be written as [37],

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right), \tag{3a}$$

Furthermore, the voltage dependent of $n(V)$ can be expressed as [38],

$$n(V) = \left(\frac{q(V - IR_s)}{kT\ln(I/I_0)}\right) \tag{3b}$$

The experimental values of n and Φ_{Bo} of diodes were determined from Eq. (2b) and (3a) as 3.142 and 1.305 for n; and 0.713 and 0.796 eV for σ_{Bo} with and without Si_3N_4 interfacial insulator layer, respectively. The high values of n show that the fabricated Au/n-4H SiC diodes behave as MIS rather than MS structure. The high n values can also be the indication of the presence of an interfacial insulator layer, patches at Au/n-4H SiC interface or wide distribution of low SBHs and distribution of D_{it} at Si_3N_4/n-4H SiC interface [35,36]. Investigation of transport mechanism on the fabricated MS and MIS diodes were detailed by plotting In(I)–In(V) relations given in figure 2. As presented in the inset of figure 2, there are three distinct linear regions for In(I)–In(V) characteristics of both of these diodes as region 1: -3.3 V $<$ V $<$ -1.8 V; region 2: -1.6 V $<$ V $<$ -0.6; region 3: 0 V $<$ V $<$ 1 V for Au/n-4H SiC and region 1: -3.3 V $<$ V $<$ -0.2 V; region 2: -0.25 V $<$ V $<$ 0.3; region 3: 0.4 V $<$ V $<$ 1 V for Au/Si_3N_4/n-4H SiC. At low bias region (region 1), the change in the measured current values are directly related to applied bias voltage as in ohmic contact characteristics for these Schottky barrier diodes (SBDs), independently [38,39]. This behaviour can be the result of the predominance of bulk generated current to the injected free carrier generated current [39–41]. The linearity in the second voltage region (region 2) can be characterized by the mechanism of space charge limited current (SCLC) showing power law dependence of I to V ($I \sim V^m$). This $I-V$ behaviour is related to the increase in injected electrons from electrode to the insulator layer with the increase in voltage. The increase in the number of injected electrons can trigger the saturation of the traps and as a result increase in the space charges [39–41]. Additionally, at strong forward bias region (region 3), the electrons can escape from the traps and contribute to SCLC due to the strong electron injection [39–43].

Parasitic structure resistances (R_i) have a significant role in the performance of the semiconductor devices. In the electrical analysis of these diodes, the values of n and Φ_{Bo} were found to be in increasing behaviour with increase in applied bias voltage mostly for the high bias voltage region under the effect of R_s. In order to estimate this effect of parasitic resistances in these fabricated diodes, R_s and R_{sh} were calculated in the high forward and reverse voltage regions, respectively. According to the parasitic resistance relation as $R_i = dV_i/dI_i$,

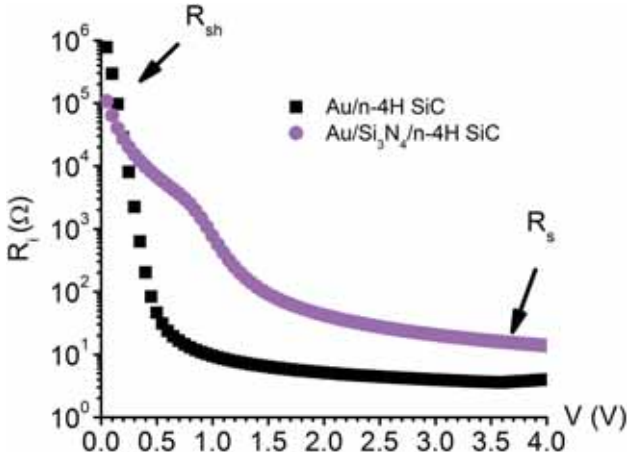

Figure 3. The structure resistance of Au/n-4H SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature.

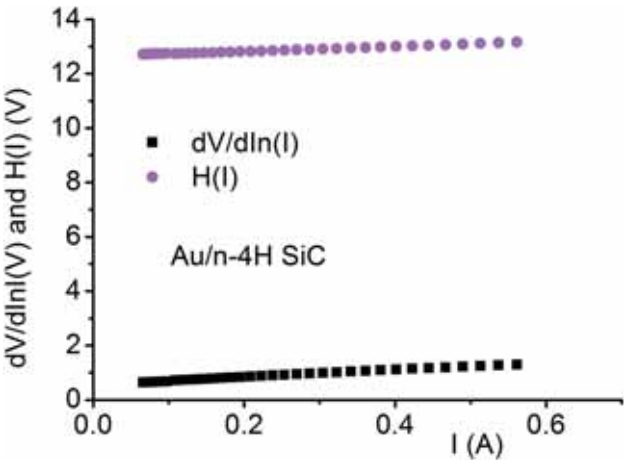

Figure 4. $dV/d(\ln I)-I$ and $H(I)-I$ plots of the Au/n-4H SiC diodes at room temperature.

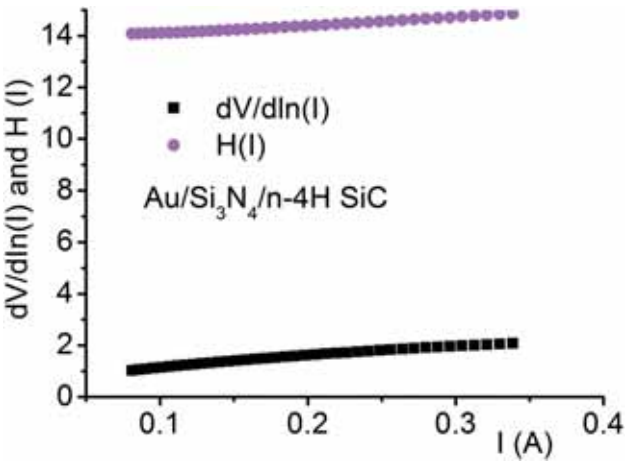

Figure 5. $dV/d(\ln I)-I$ and $H(I)-I$ plots of the Au/Si_3N_4/n-4H SiC diodes at room temperature.

the obtained resistance values are plotted in figure 3. As shown in this figure, at sufficiently high forward bias voltage region, R_s values for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC approach to constant values as 3.79 and 14.83 Ω, respectively. Similarly, at around 0 V reverse bias point, R_{sh} values were found in constant values as 0.77 and 0.10 MΩ for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC, respectively. These observed increase in R_s and decrease in R_{sh} with the contribution of Si_3N_4 insulator layer can be the indication for improvement in the Au/n-4H SiC diode performance.

The values of R_s were also calculated from the forward bias $I-V$ data in the concave curvature region of the $I-V$ plots by using the Cheung and Cheung method [19] as the following expressions,

$$\frac{dV}{d(\ln I)} = n\left(\frac{kT}{q}\right) + IR_s \tag{4}$$

$$H(I) = V + n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_{Bo} + IR_s \tag{5}$$

where the term IR_s is the voltage drop across the R_s in the diodes. The corresponding $dV/d(\ln I)-I$ and $H(I)-I$ plots of the diodes are given in figures 4 and 5, respectively. In these analyses, the slope of the straight line obtained in $dV/d(\ln I)-I$ plots corresponds to the R_s and the y-axis intercept is used to calculate n. As a result of them, the R_s values for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC were found as 4.08 and 2.96 Ω, respectively. In a similar way, the linearity of the $H(I)-I$ plots represented in figures 4 and 5 is related to the R_s values. In addition, by using the n value from the direct analysis of semi-logarithmic $I-V$ relation, Φ_{Bo} can be calculated from the y-intercept of the $H(I)-I$ plots. R_s and Φ_{Bo} values for Au/n-4H SiC diodes with and without Si_3N_4 were found as 3.12, 1.6 Ω and 0.455, 0.457 eV, respectively. As a result, R_s values obtained from $dV/d(\ln I)-I$ and $H(I)-I$ plots are found in a good agreement with each other for both of two fabricated diodes.

The non-ideal $I-V$ characteristics observed at high bias voltages (figure 2) can be evaluated as the continuum of D_{it} in equilibrium with semiconductor, the effects of R_s and interfacial layer [37]. Thus, the distribution of D_{it} can be determined from the forward bias $I-V$ characteristics by using the voltage dependence of Φ_e and n. In addition, under the effect of R_s in the real SBD, Φ_e can be obtained from Eq. (2c) by considering the presence of an interfacial insulator layer (Si_3N_4) and R_s. According to the model proposed by Card and Rhoderick [15], the values of D_{it} can be simplified as,

$$D_{it}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{w_D}\right] \tag{6}$$

where ε_i and ε_s are permittivity of insulator layer and semiconductor, respectively; and w_D is the width of the space

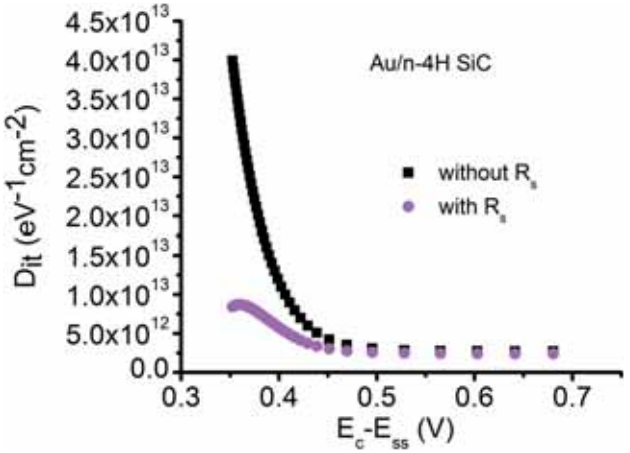

Figure 6. Density of interface states as a function of $E_c - E_{ss}$ of Au/n-4H SiC diodes by taking into account the series resistance in the calculation at room temperature.

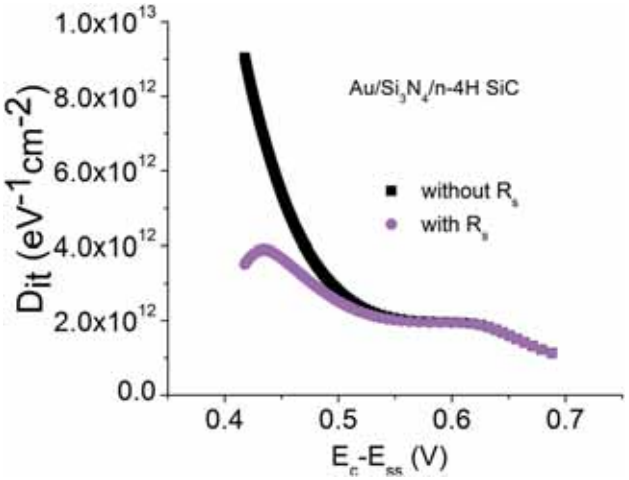

Figure 7. Density of interface states as a function of $E_c - E_{ss}$ of Au/Si_3N_4/n-4H SiC diodes by taking into account the series resistance in the calculation at room temperature.

charge region. For this analysis, the interfacial insulator layer thickness δ was obtained from insulator layer capacitance ($C_{ox} = \varepsilon_i \varepsilon_0 A/\delta$) at 1 MHz frequency.

For n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band of semiconductor E_c can be expressed as [44]:

$$E_c - E_{ss} = q(\Phi_e - V) \tag{7}$$

Therefore, for Au/n-4H SiC diodes with and without Si_3N_4 interfacial insulator layer, the values of D_{it} as a function of $E_c - E_{ss}$ are illustrated in figures 6 and 7, respectively. The exponential increase in the D_{it} from mid-gap towards the bottom of the conductance band were distinctively observed from these figures [15,45–49]. As seen in figure 6, the magnitude of D_{it} for Au/n-4H SiC at $0.36 - E_v$ (eV) changes in the range from 8.557×10^{12} to 2.813×10^{13} eV^{-1} cm^{-2} with the effect of R_s. Additionally, this variation was found in the range from 7.454×10^{12} to 1.763×10^{13} eV^{-1} cm^{-2} at $0.38 - E_v$ (eV) for Au/Si_3N_4/n-4H SiC (figure 7). As a result, the effect of R_s should be discussed in the evaluation of the D_{it} profiles for both of these MS and MIS diodes [49,50]. Since the experimental results showed that the values of D_{it} decreases with contribution of insulator layer to the MS diode and therefore there is a structural improvement with the high dielectric insulator layer.

In the reverse bias region, the exponential dependence of reverse current I_R showed that the current transport characteristics cannot explain by usual diode characteristics. Therefore, Poole-Frenkel or Schottky barrier lowering mechanisms can be evaluated as pre-dominant reverse current transport mechanism for these two diodes. In order to observe the effect of these mechanisms in the reverse conduction region, the current density in the reverse direction $J_R - V$ curves was plotted. As given in figure 8, linear relation between $\ln(J_R)$

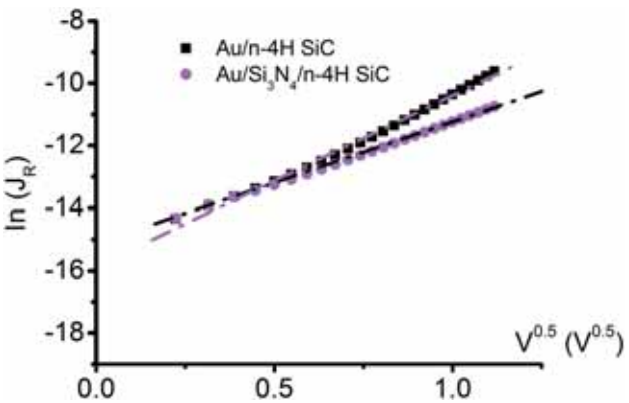

Figure 8. Plots of J_R *vs.* $V^{1/2}$ of the Au/n-type 4H-SiC and Au/Si_3N_4/n-4H SiC diodes in the reverse direction.

and $V^{1/2}$ was observed for the MS and MIS diodes [51–59]. However, Poole-Frenkel conduction and Schottky barrier lowering effect gave the similar appearance in these characteristics plots; it is difficult to specify the dominant effect on the reverse bias $I - V$ characteristics.

The $I_R - V$ expression for the Poole-Frenkel effect is given by

$$I_R = AA^*T^2 \exp(-\Phi_b/kT) \exp[(\beta_{PF} V^{1/2})/(kT d^{1/2})] \tag{8}$$

where β_{PF} is the Poole-Frenkel coefficient expressed by

$$\beta_{PF} = (q/\pi \varepsilon_0 \varepsilon)^{1/2} \tag{9}$$

where ε_0 is the permittivity of free space and ε the relative dielectric constant [51–59]. In this expression, β_{PF} is

Table 1. Experimental and theoretical values of β.

	Experimental values	Theoretical values	
	β ($eVm^{1/2}V^{-1/2}$)	β_{BF} ($eVm^{1/2}V^{-1/2}$)	β_{sc} ($eVm^{1/2}V^{-1/2}$)
Au/n-4H SiC	1.29×10^{-05}	6.85×10^{-05}	3.42×10^{-05}
Au/Si_3N_4/n-4H SiC	2.22×10^{-05}	3.37×10^{-05}	1.73×10^{-05}

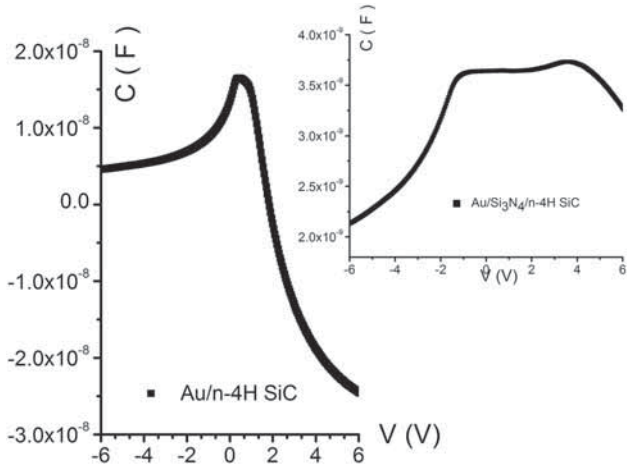

Figure 9. The $C-V$ plot of the Au/n-type 4H-SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature.

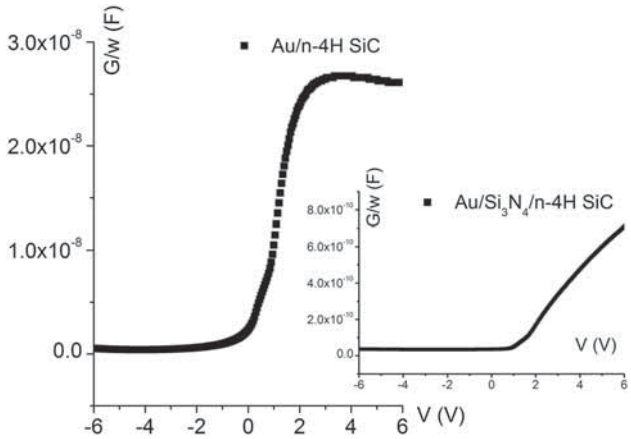

Figure 10. The $G/w-V$ plot of the Au/n-type 4H-SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature.

higher than Schottky coefficient β_{sc} as $\beta_{PF} = 2\beta_{sc}$ [43–51]. The experimental value of β determined from the slope of linear regions in figure 8 is listed in table 1. From the theoretical calculations, β_{PF} was reported as 6.85×10^{-05} and 3.47×10^{-05} $eVm^{1/2}V^{-1/2}$ for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC, respectively. As given table 1, the experimental result of β_{PF} was found in a close approximation to the calculated $\beta_{SC(theorical)}$ value. This result indicated that the reverse current conduction mechanism for these diodes is dominated by Schottky (SC) effect.

3.2 *Capacitance–voltage and conductance–voltage characteristics*

In general, at sufficiently high frequencies ($f \geq 1$ MHz), the D_{it} cannot follow the ac signal and as a result, the contribution of D_{it} capacitance to the measured total capacitance can be neglected [48]. Therefore, the $C-V$ measurements of the diodes were carried out at 1 MHz and the experimental results were given in figure 9. As seen in figure 9, the C values of Au/Si_3N_4/n-4H SiC increases rapidly in the interval of -6.0 and -1 V, whereas there is a slow increase in behaviour between -1 and 4 V and decrease in behavior between 4 and 6.0 V with increase in the reverse bias voltage. In addition, there is an anomalous C peak in the corresponding $C-V$ plot of Au/n-4H SiC at about 0.6 V. In this plot, C values take negative at about 2.0 V. At room temperature condition, such $C-V$ behaviour is known as negative capacitance (NC) [60,61]. Decrease in the values of R_s decrease can be related to the reduction in carrier density in the depletion region of the diode through the introduction of traps and recombination centre associated with the voltage effect. On the other hand, a rapid increase in G/w values with the increase in voltage was observed, as in figure 10, for all fabricated diodes.

The $C-V$ and $G/w-V$ relations of Au/n-4H SiC were figured as a single plot in figure 11. As seen in figure 11, the values of C are relatively higher than G/w in the reverse bias region whereas this behaviour is reversed in the forward bias region. In fact, at about 6.0 V point, C takes a minimum value and on the other hand, G/w reaches to a maximum value with similar to the reported works in the literature [60–63]. The observation of NC, in which the charge on the electrodes decreases with the increment of bias voltage produces, is the indication of an inductive behaviour of this MS diode [60,62]. Based on NC, increase in the injection of minority carriers can be observed only at a forward bias voltage [60]. In this case, the detailed analysis cannot be carried out due to the fact that there is no enough experimental study to define the NC effect [60–63].

From the $C-V$ analysis, the $C^{-2}-V$ plots of the diodes are given in figure 12. From figure 12, in wide range of bias voltage, linear variation of the C^{-2} values with V was observed in both of Au/n-4H SiC (in the interval of -4 to $+0.5$ V)

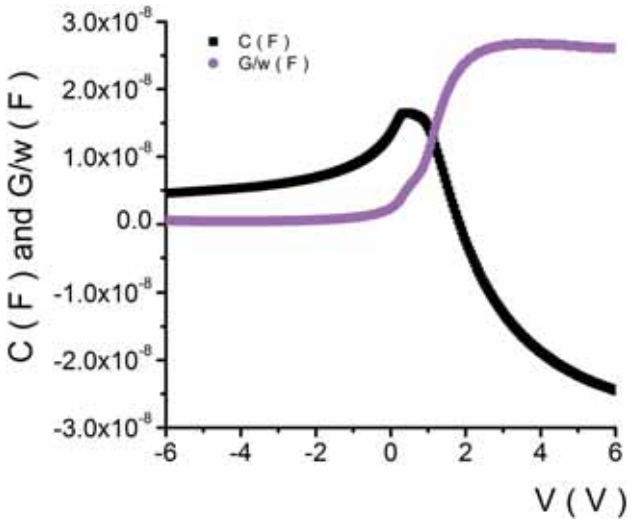

Figure 11. The $C-V$ and $G/w-V$ plot of the Au/n-type 4H-SiC and Au/Si_3N_4/n-4H SiC diodes at room temperature.

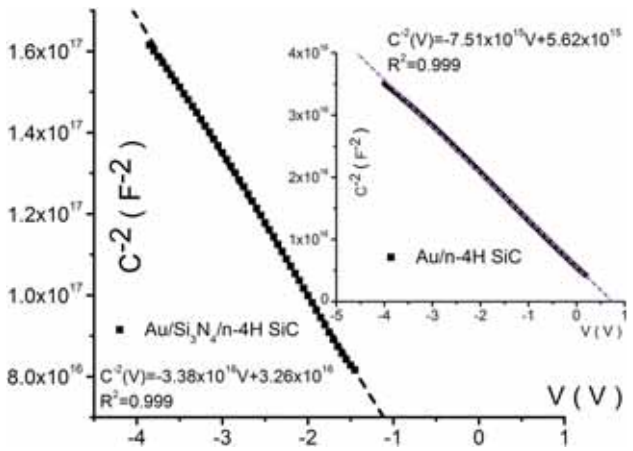

Figure 12. The $C^{-2}-V$ plots of the Au/n-type 4H-SiC and Au/Si_3N_4/n-4H SiC diodes at the frequency of 1 MHz at room temperature.

and Au/Si_3N_4/n-4H SiC (in the interval of -4 to -1 V). The depletion layer capacitance is given as [35],

$$C^{-2} = \frac{2(V_R + V_i)}{q\varepsilon_s N_d A^2}, \tag{10}$$

where V_R is the reverse bias voltage, N_d the doping concentration and V_i the built-in voltage at zero bias. From the extrapolation of the $C^{-2}-V$ plots to the voltage axis, V_i values were obtained as 0.746 and 0.936 V for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC, respectively. In addition, from the slope of $C^{-2}-V$ plots, N_d values for the two diodes were calculated at 1 MHz as 1.96×10^{16} and 1.47×10^{16} cm^{-3}, respectively.

Using the obtained V_i values, the diffusion potential at zero bias can be calculated using following relation [44]:

$$V_d = V_i + \frac{kT}{q} \tag{11}$$

Thus, the values of V_d were obtained as 0.773 and 0.963 V for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC, respectively. The depletion layer width w_D for both of the samples were also investigated from the following equation [17]:

$$w_D = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_d}{qN_d}} \tag{12}$$

and it was found as 1.89×10^{-6} and 1.55×10^{-6} m for Au/n-4H SiC and Au/Si_3N_4/n-4H SiC, respectively.

4. Conclusions

In this study, the electrical characteristics of Au/n-4H SiC diodes were investigated with and without Si_3N_4 interfacial insulator layer. This comparative study of Au/n-4H SiC diodes was carried out by using the room temperature forward and reverse bias $I-V$, $C-V$ and $G/w-V$ measurements. Experimental results showed that these characteristics were strongly affected from the values of R_s, R_{sh}, D_{it} and the interfacial layer. In addition, n and Φ_{Bo} were calculated as 1.305 and 0.796 eV for Au/n-4H SiC, and 3.142 and 0.713 eV for Au/Si_3N_4/n-4H SiC at room temperature, respectively. It was observed that decrease in behaviour of both n and Φ_{Bo} values in the MIS diode as compared with that of the MS could be attributed to the presence of an insulator layer at the Au/n-4H SiC interface. Since experimental n values are greater than unity, $I-V$ behaviour of these diodes was found in deviation from TE theory. This result was attributed to the interfacial insulator layer, D_{it}, formation, Gaussian distribution of barrier height at M/S interface and image force barrier lowering. In addition, the values of R_s and R_{sh} were obtained as 3.79, 0.77 MΩ for Au/n-4H SiC and 14.83, 0.10 MΩ for Au/Si_3N_4/n-4H SiC, respectively. The change in the parasitic resistances shows an improvement in terms of the expectation from the ideal $I-V$ behaviour of the diode structure after the insertion of Si_3N_4. The energy density distribution profiles of D_{it} were extracted from the forward bias $I-V$ data by considering the dependence of BH and the values of both diodes showed an increase in behaviour from the mid-gap towards the bottom of conduction band of n-4H SiC. These values of D_{it} were in high values under the effect R_s for both diodes. The experimental results showed that the values of D_{it} decreases with contribution of insulator layer to the MS diode and there is a structural improvement with this high dielectric insulator layer. According to these results, Au/Si_3N_4/n-4H SiC diode shows a better RR than Au/4n-4H SiC diode due to the decrease in the effects of D_{it} and shunt resistance, R_{sh}.

Furthermore, I_R was interpreted in terms of the two field lowering mechanisms according to Poole-Frenkel and Schottky mechanism. As a result of this analysis, Schottky effect was found to be a most appropriate mechanism to explain the conduction process in reverse direction. Finally, we conclude that the Au/n-4H SiC diodes with Si_3N_4 interfacial insulator layer show better device performance and they are more suitable for this type of device fabrications.

Acknowledgements

This study was partially supported by The Management Unit of Scientific Research Project of Hitit University, under Project Numbers FEF19004.15.010 and FEF19002.15.001.

References

[1] Morkoç H, Strite S, Gao G B, Lin M E, Sverdlov B and Burns M 1994 *J. Appl. Phys.* **76** 363
[2] Masri P 2002 *Surf. Sci. Rep.* **48** 1
[3] Sochacki M, Kolendo A, Szmidt J and Werbowy A 2005 *Solid-State Electron.* **49** 585
[4] Wang S R and Liu Z L 2002 *Curr. Appl. Phys.* **2** 393
[5] Bozack M J 1997 *Phys. Stat. Solid B* **202** 549
[6] Porter L M, Davis R F, Bow J S, Kim M J, Carpenter R W and Glass R C 1995 *J. Mater. Res.* **10** 668
[7] Yakimova R, Hemmingsson C, Macmillan M F, Yakimov T and Janzen E 1998 *J. Electron. Mater.* **27** 871
[8] Schoen K J, Woodall J M, Cooper J A and Melloch M R 1998 *IEEE Trans. Electron. Dev.* **45** 1595
[9] Sze S M 1981 *Physics of semiconductor devices* (New York: Wiley)
[10] Rhoderic E H and Williams R H 1978 *Metal-semiconductor contacts* (Oxford: Clarendon Press)
[11] Lu X, Xu X, Wang N Q, Zhang Q and Lin M C 2001 *J. Phys. Chem. B* **105** 10069
[12] Onganer Y, Sağlam M, Türüt A, Efeoğlu H and Tüzemen S 1996 *Solid State Electron.* **39** 677
[13] Okutan M, Başaran E N and Yakuphanoglu F 2005 *Appl. Surf. Sci.* **252** 1966
[14] Pakma O, Serin N, Serin T and Altındal Ş 2009 *J. Sol-Gel Technol.* **50** 28
[15] Card H C and Rhoderick E H 1971 *J. Phys. D* **4** 1589
[16] Farag A M, Ashery A, Ahmed E M A and Salem M A 2010 *J. Alloys Compd.* **495** 116
[17] Kavasoglu A S, Yakuphanoglu F, Kavasoglu N, Pakma O, Birgi O and Oktik S 2010 *J. Alloys Compd.* **492** 421
[18] Altındal Ş, Kanbur H, Yıldız D E and Parlak M 2007 *Appl. Surf. Sci.* **253** 5056
[19] Cheung S K and Cheung N W 1986 *Appl. Phys. Lett.* **49** 85
[20] Farag A M, Terra F S, Mahmoud G M and Mansour A M 2009 *J. Alloys Compd.* **481** 427
[21] Tataroğlu A and Altındal Ş 2009 *J. Alloys Compd.* **484** 405
[22] Pirri C F, Ferrero S, Scaltrito L, Perrone D, Guastella S, Furno M *et al* 2006 *Microelectron. Eng.* **83** 86
[23] Aydoğan Ş, Çınar K, Asıl H, Çoşkun C and Türüt A 2009 *J. Alloys Compd.* **476** 913
[24] Ejderha K, Yıldırım N, Abay B and Türüt A 2009 *J. Alloys Compd.* **484** 870
[25] Yıldız D E, Altındal Ş and Kanbur H 2008 *J. Appl. Phys.* **103** 124502
[26] Özer M, Yıldız D E, Altındal Ş and Bülbül M 2007 *Solid-State Electron.* **51** 941
[27] Tataroğlu A, Altındal Ş and Bülbül M 2005 *Microelectron. Eng.* **81** 140
[28] Aydın S B K, Yıldız D E and Kanbur Çavuş H 2014 *Bull. Mater. Sci.* **37** 1563
[29] Yıldız D E and Dökme İ 2011 *J. Appl. Phys.* **110** 014507
[30] Benkovska J, Stuchlikova L, Buc D and Caplovic L 2012 *Phys. Stat. Sol. A* **209** 1384
[31] Vila M, Prieto C, Miranzo P, Osendi M I and Ramirez R 2002 *Surf. Coat. Technol.* **151-152** 67
[32] Tataroğlu A and Pür Z 2013 *Phys. Scr.* **88** 015801
[33] Tataroğlu A 2013 *Chin. Phys. B* **22** 068402
[34] Card H C and Rhoderick H C 1973 *Solid-State Electron.* **16** 365
[35] Hudait M K and Krupanidhi S B 2001 *Mater. Sci. Eng. B Solid* **87** 141
[36] Wener J H and Güttler H 1991 *J. Appl. Phys.* **69** 1522
[37] Schroder D K 1998 *Semiconductor material and device characterization* (London: Wiley)
[38] Wagle S and Shirodkar V 2000 *J. Phys.* **30** 380
[39] Zang Z X, Pan X J, Wang T, Xie E Q and Jia L 2009 *J. Alloys Compd.* **467** 61
[40] Bengi A, Aydemir U, Altındal Ş, Özen Y and Özçelik S 2010 *J. Alloys Compd.* **505** 628
[41] Wang H, Shen X N, Su X J, Wang Z, Shang S X and Wang M 1997 *Ferroelectrics* **195** 233
[42] Güllü Ö, Aydoğan S and Türüt A 2008 *Microelectron. Eng.* **85** 1647
[43] Zhang S X, Kundaliya D C, Yu W, Dhar S, Young S Y, Salamanca-Riba L G *et al* 2007 *J. Appl. Phys.* **102** 013701
[44] Güllü H H, Bayrakli Ö, Yildiz D E and Parlak M 2017 *J. Mater. Sci. Mater. Electron* **28** 17806
[45] Hudait M K and Krupanidhi S B 2001 *Mater. Sci. Eng. B* **87** 141
[46] Ma T P 1989 *Semicond. Sci. Technol.* **4** 1061
[47] Hughes G W 1997 *J. Appl. Phys.* **48** 5357
[48] Akkal B, Benemara Z, Boudissa A, Bouiadjra N B, Amrani M, Bideux L *et al* 1998 *Mater. Sci. Eng. B* **55** 162
[49] Çetinkara H A, Türüt A, Zengin D M and Erel Ş 2003 *Appl. Surf. Sci.* **207** 190
[50] Soylu M, Al-Hartomy O A, Al Said S A F, Al-Ghamdi A, Yahia I S and Yakuphanoğlu F 2013 *Microelectron. Reliab.* **53** 1901
[51] Arslan E, Bütün S and Ozbay E 2009 *Appl. Phys. Lett.* **94** 142106
[52] Soylu M, Yahia I S, Yakuphanoglu F and Farooq W A 2011 *J. Appl. Phys.* **110** 074514
[53] Gould R D 1996 *Coord. Chem. Rew.* **156** 237
[54] Reis F T, Mencaraglia D, Saad S O, Seguy I, Oukachmih M, Jolinat P *et al* 2003 *Synth. Met.* **138** 33
[55] Harrell W R and Gopalakrishnan C 2002 *Thin Solid Films* **405** 205
[56] Frenkel J 1938 *Tech. Phys. USSR* **6** 685

[57] Frenkel J 1938 *Phys. Rev.* **54** 647
[58] Harrell W R and Frey J 1999 *Thin Solid Films* **352** 195
[59] Arslan E, Şafak Y, Altındal Ş, Kelekçi Ö and Özbay E 2010 *J. Non-Cryst. Solids* **356** 1006
[60] Uslu H, Altındal Ş, Polat I, Bayrak H and Bacaksız E 2011 *J. Alloys Compd.* **509** 5555
[61] Jones B K, Santana J and McPherson M 1998 *Solid State Commun.* **107** 47
[62] Ershov M, Liu H C, Li L, Buchanan M, Wasilewsk Z R and Jonscher A K 1998 *IEEE Trans. Electron. Dev.* **45** 2196
[63] Wu X, Yang E S and Evans H L 1990 *J. Appl. Phys.* **68** 1104