FULLY AUTONOMOUS INTERFACE CIRCUIT FOR THERMOELECTRIC ENERGY HARVESTING IN WEARABLE AND IoT APPLICATIONS

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Approval of the Board of Graduate Programs

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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ABSTRACT

FULLY AUTONOMOUS INTERFACE CIRCUIT FOR THERMOELECTRIC ENERGY HARVESTING IN WEARABLE AND IoT APPLICATIONS

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M.S. Sustainable Environment and Energy Systems Program

Supervisor : Assoc. Prof. Dr. Ali Muhtaroglu

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IoT and wearable electronics are building blocks of the current and future monitoring technologies with numerous applications such as environmental monitoring, precision agriculture, healthcare, transportation and logistics, and smart buildings. Powering the IoT smart nodes is costly due to the existence of billions of these nodes in the technology roadmaps, and is not environmental friendly due to the use of chemical batteries with toxic substances. Eliminating batteries is therefore highly desirable. Fully integrated solutions with sufficient output power capacity for batteryless IoT applications are rarely targeted in the literature. In this thesis, a novel fully autonomous interface circuit for energy harvesting from thermoelectric devices is introduced, which provides considerably increased output power with maximum power point tracking capability at 1 V regulated voltage level. The circuit is composed of a DC-DC converter based on charge pump and LC-tank oscillator with a digital MPPT block, and an LDO regulator. A novel MPPT algorithm is proposed that refrains from disconnecting the circuit form the TEG, and is compatible with varying input and load conditions. Based on the measurement results, the circuit start-up voltage is as low as 170 mV. The output power attains 500 μW, which is the state of the art in the literature for a fully integrated design, and thus meets the real time demand of IoT nodes for sensing, signal processing and wireless data transmission in duty cycle mode and some GHz range. The peak efficiency based on post-layout simulations is 36%, which reduces to 20% due to fabrication mismatches. The discrepancies between simulations and measurements are fully characterized as part of the research, and are modeled to enable design improvements in the future. The MPPT algorithm reaches up to 98% accuracy when the internal resistance of the thermoelectric generator is between 30 Ω to 100 Ω, which is a typical range for a number of tiny TEGs in series.

Keywords: DC-DC converter, energy efficiency, charge pump circuit, LC tank oscillator, Maximum Power Point Tracking, MPPT, batteryless sensors, wearable sensors.

ÖZET

GİYİLEBİLİR VE IOT UYGULAMALARINDA TERMOELEKTRİK ENERJİ HASATI İÇİN TAMAMEN ÖZERK ARAYÜZ DEVRESİ

Hamed Osouli Tabrizi

Yüksek Lisans, Sürdürülebilir Çevre ve Enerji Sistemleri

Danışman: Doç. Dr. Ali Muhtaroğlu

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IoT ve giyilebilir elektronik cihazlar, çevresel izleme, hassas tarım, sağlık, ulaşım ve lojistik, ve akıllı binalar gibi sayısız uygulama ile mevcut ve gelecekteki izleme teknolojilerinin yapı taşlarıdır. IoT akıllı düğümlerine güç vermek, teknoloji yol haritalarında bu düğümlerin milyarlarca olmasına bağlı olarak maliyetlidir ve zehirli maddeler içeren kimyasal bataryaların kullanılmasından dolayı çevre dostu değildir. Bataryaları ortadan kaldırmak bu nedenle çok arzu edilir. Bataryasız IoT uygulamaları için tamamen entegre, yüksek çıkış gücü üreten çözümler literatürde nadiren ele alınmıştır. Bu tezde, termoelektrik cihazlardan enerji hasadı için maksimum güç noktası takip (MGNT) özelliği ile 1 V regüle voltaj ve önemli ölçüde artırılmış çıkış gücü sağlayan yeni ve tam otonom bir arayüz devresi önerilmiştir. Devre, şarj pompası ve LC-tank osilatöre dayalı bir DA-DA dönüştürücü ile bir dijital MGNT bloğu ve bir doğrusal regülatörden (LDO) oluşur. Devrenin termoelektrik jeneratör (TEJ) ile bağlantısını kesmeden çalışan, değişken giriş ve yük koşullaıyla uyumlu uyumlu yeni bir MGNT algoritması önerilmiştir. Ölçüm sonuçlarına göre devre başlatma voltajı 170 mV'a kadar inmektedir. Çıkış gücü tam entegre bir çip için literatürde en gelişmiş teknoloji olan 500 μW seviyesine kadar çıkmakta, ölçüm, sinyal işleme ve görev döngüsü modunda ve bazı GHz aralıklarında kablosuz veri iletimi için gerekli olan gerçek zamanlı güç talebini karşılayabilmektedir. Yonga yerleşim sonrası simülasyonlara dayanan en yüksek verimlilik %36'dır; fabrikasyon uyumsuzlukları dolayıslıyla bu değer ölçümde %20'ye düşmektedir. Bu uyumsuzluklar gelecekteki tasarım geliştirmelerini mümkün kılmak için ölçümle karakterize edilmiş ve modellenmiştir. MGNT algoritması, TEJ iç direnci 30 Ω ila 100 Ω arasında olduğunda % 98'e kadar doğruluk oranına ulaşabilmektedir. Bu direnç aralığı, seri bağlanmış bir dizi küçük TEJ için tipiktir.

Anahtar Kelimeler: DA-DA dönüştürücü, enerji verimliliği, şarj pompa devresi, LC tank osilatörü, Maksimum Güç Noktası Takibi, MGNT, bataryasız sensörler, giyilebilir sensörler.

DEDICATION

To my wife

For her unconditional love, patience and inspiration.

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I want to thank all my SEES program professors for providing a solid background to understand the current sustainability issues all over the world and the necessity to confront these problems both globally and locally.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

C	Capacitance (pF)
P	Power
I	Current
F	Frequency
η	Efficiency (%)
η_{min}	Minimum bound for the MPPT Efficiency (%)
MEMS	Micro-Electromechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
Low_Vt	Low threshold voltage
V_{in}	İnput voltage
V_t	Threshold voltage
gm	Transconductance
W	Width (μm)
L	Inductor (nH)
V_{DD}	Source voltage
R_S	Series resistance
R_P	Parallel resistance
C_S	Series capacitance
C_P	Parallel capacitance
P_T	Total power
V_{PP}	Peak-to-peak voltage
TE	Thermoelectric

CHAPTER 1

1 Introduction

1.1 Ambient energy harvesting for IoT smart nodes

“Internet of things” (IoT) has recently gained a lot of focus, and has been a promising framework in design and development of miniaturized batteryless sensors and actuators equipped with wireless data transmission capabilities such as WiFi or Bluetooth. “Smart nodes”, the building blocks of IoT, are embedded systems that enable sensing and data transmission in ubiquitous networks to monitor parameters of interest in any environment such as residential and industrial areas, forests, oceans, deserts, etc. [1] The accumulated big data in these sensor networks finds way to the internet to be shared and processed in cloud, paving the way for numerous emerging applications, some of which are summarized in Figure 1.1. A general block diagram of an IoT smart node is illustrated in Figure 1.2. Miniaturization becomes considerably important for applications such as wearable electronics for health care. In fact a newly emerged trend is using IoT in health care applications to achieve 24-hour low cost health monitoring. This will be the backbone of future healthcare system. This includes animal health care monitoring and animal consensus.

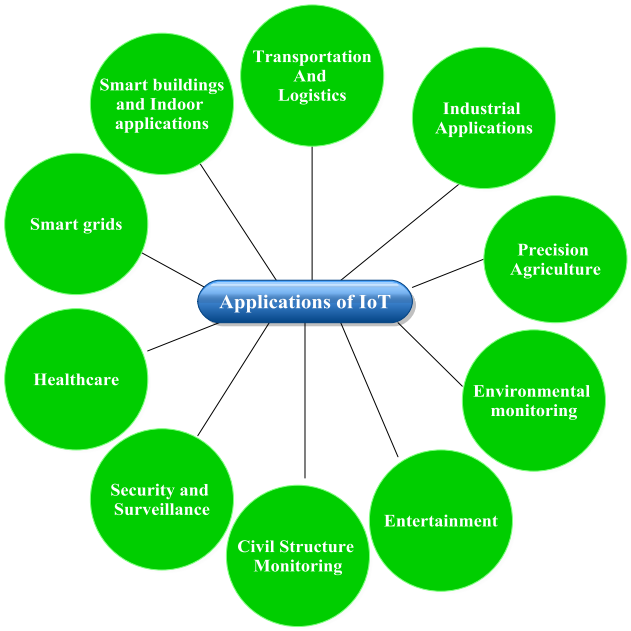


Figure 1.1. Applications of IoT [6].

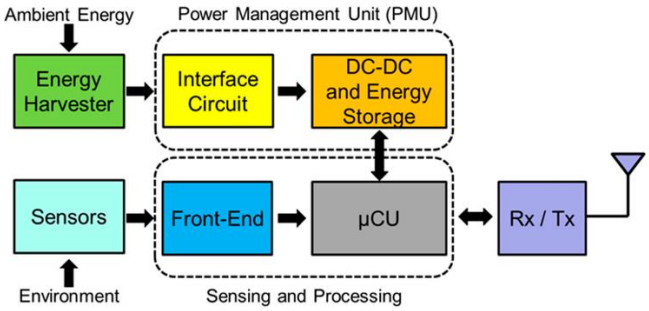


Figure 1.2. Block diagram of an IoT smart node [7].

To this end, billions of these smart nodes will be integrated into the environment. The estimated minimum number of IoT device usage at 2020 is 50 billion [2]. Miniaturization of these nodes therefore is of significant importance. Current smart nodes are typically large and battery powered [3]. Some of the most commonly used examples are: i) Arduino Yun - 6.8cm × 5.4cm hardware platform [4], ii) Raspberry Pi - 8.5cm × 5.6cm single board computer [5], and iii) BeaglBone Black – low power 6.5cm × 7.6cm single board computer [6]. These single board computers are equipped with wifi or LAN communication protocols, and usually require AAA batteries for their proper operation, which adds to the dimensions and the weight. The weight of an AAA type battery is typically between 10 to 20 grams. The size and weight specifications of the current IoT nodes is a barrier for widespread deployment. The size and weight should be reduced tens of times in magnitude, and tiny energy harvesting elements with cm^2 or smaller footprint should replace the batteries. Empowering these nodes using batteries is a big challenge in terms of network lifetime and reliability, and environmental issues. Use of batteries significantly increases the system cost (including maintenance and battery replacement) and size, and reduces portability. Use of batteries is impractical in some applications such as implantable sensors and remote environmental monitoring systems, since battery replacement is expensive, time consuming, and inconvenient. However, problems like environmental pollution, size and cost increase still remain unsolved with the rechargeable batteries [7]. CMOS integrated circuits and MEMS are fundamental technologies utilized in the implementation of low-cost IoT smart nodes. The rapid growth in the CMOS technology brings about chip size reduction, lower cost and ultra-low power consumption, based on which micro-scale ambient energy harvesting has been made feasible.

Ambient energy harvesting plays an important role in confronting the battery and power problems. The state of the art in micro-scale energy harvesting achieves complete elimination of the battery from the sensor nodes making them much smaller and more

environment friendly [8], [9]. There are many types of ambient energy that can be scavenged. Thermoelectric, vibration, solar, electromagnetic and ambient RF are among the attractive and promising sources in the literature [10]. In Chapter 2, micro scale energy harvesting from some of the widely used ambient energy sources are briefly introduced. However, the main focus and objective of this thesis is on thermoelectric energy harvesting for IoT and wearable applications.

Wearable electronics is an emerging area under the paradigm of internet of things that aims at creating wearable sensors and actuators for healthcare monitoring, athletic performance evaluation, and security applications. Opportunity exists to power wearable sensor nodes using energy harvesting from body heat and body movement. Wireless Body Area Network (WBASN) connects wearable electronic nodes that enable monitoring human body variables such as temperature, blood pressure, glucose, ECG, EEG, EMG signals for 24 hours. The majority of these wearable electronic devices are wireless due to inconvenience of wiring. Making wearable devices batteryless is highly desirable due to size reduction and convenience. A thermoelectric generator (TEG), which converts temperature gradients to electric power, can be used to achieve batteryless operation. For example, the wearable temperature sensing system introduced in [11] relies on energy harvested from 2 TEGs. An integrated system presented in [12] measures ECG signals and transmits the data wirelessly to the sink node using power from thermoelectric generators.

1.2 Energy requirements of the IoT and wearable smart nodes

A typical IoT smart node is composed of an embedded processing unit, different sensors and wireless data transmission unit. The typical power consumption of state of the art ultra-low power microcontrollers are found to be no less than 20 μA/MHz for active mode [13]–[15]. This is equal to 20 μW/MHz power consumption. For a typical 10 MHz microcontroller 200 μW power will be required for the active mode operation. The power requirement of wireless data transmission is in the range of some hundred mW without duty cycle that can decrease to some hundred μW by duty cycling thanks to the wake up radio technology [16]. Adding the required power for sensing, the overall minimum required power consumption for an IoT node is hundreds of μWs. However, most fully integrated energy harvesting solutions in the literature achieve only some tens of μW at best, which is not sufficient for continuous operation of these nodes. There are two types of sensor nodes deployed for wearable electronics: On-body and off-body. Thermoelectric energy harvesting typically targets the on-body sensor types since the hot plate of the TEG should be in contact with the

body, a good temperature regulator. The power consumption requirement for this type of node is in the range of some hundred μWs [17] as well.

1.3 The necessity of the interface circuits

An energy harvesting actuator cannot be directly connected to a sensor node as a power supply due to the following considerations:

- The harvester's output voltage varies with environmental (temperature) conditions.
- The output voltage level of the harvester can be well below the required supply voltage to power the electronic circuits within the sensor node.
- The generated voltage from some harvesters, such as those that use mechanical vibration energy, is AC, whereas the load voltage is required to be DC.
- Both harvester's output resistance and sensor load are variable, which leads to inefficient power transfer between the harvester and the load when the output impedance of one does not match the input impedance of the other.

Figure 1.3 demonstrates the general view of the harvester interface circuit elements. An interface circuit typically performs some or all of voltage regulation, Maximum Power Point Tracking (MPPT), voltage boost and rectification functions. There are many considerations around the design of interface circuits as discussed in section 1.4

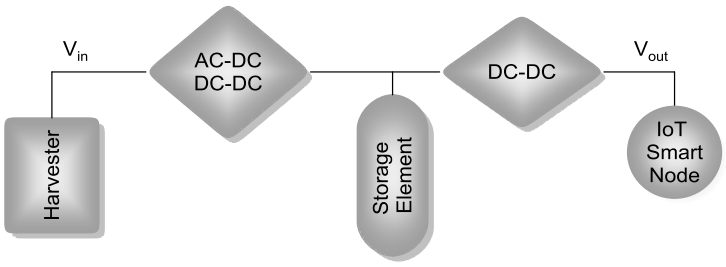


Figure 1.3. Harvesting microsystem composed of harvester and interface circuit [11].

1.4 Important considerations in the design of interface circuits

Figure 1.4 demonstrates the design considerations for the interface circuits. The design space has many parameters due to the following facts:

1- Different energy sources have inherently different characteristics
2- Electric properties of harvesters such as their output impedance and their equivalent circuit models are different.

3- In IoT and wearable applications, the load is highly dynamic since a combination of sensing, signal processing and wireless data transmission tasks take place at different instances that require very different amount of power.

Output power and efficiency should be maximized by the interface circuits. Although related, these two parameters can be treated differently. This means in some energy harvesting systems the efficiency may be low due to the losses, but power requirement of the sensor node may be met. On the other hand, maximizing the efficiency brings about increase in the output power by minimizing the system losses for a given input power, but if the input power is reduced, for example due to impedance mismatches, this may be misleading.

Output Power	MPP tracking Efficiency	Minimum start up voltage
Single source / Hybrid	Input voltage range	Output voltage ripple
Power Conversion Efficiency	Target output voltage	Voltage Conversion Ratio (VCR)

Figure 1.4. The design space of interface circuits.

The efficiency of the overall system should be calculated considering the overall input power available from the source and the total power delivered to the load. However, due to the difficulty of calculating such efficiency value, many studies in the literature mainly focus only on the efficiency of their designed interface circuit rather than the overall system. Multiplication of the harvester efficiency by the interface circuit efficiency can be a good approximation for the overall system efficiency.

Due to varying output resistance of the harvesters, maximum power point tracking is an essential block in the design of interface circuits. The MPPT circuits track the output impedance of the harvesters. The accuracy of MPPT blocks can be varying due to the implemented algorithms with different errors in tracking the exact maximum power point. Introduction of MPPT unit to the system increases the loss due to the power consumption of

the unit itself. Therefore, minimizing the power consumption should also be considered in the design of this block.

Tiny ambient energy harvesters typically provide low output voltage due to their miniature size. This voltage can be well below the threshold voltage of the MOSFET transistors in the interface circuit, forcing them to operate in the subthreshold region. This can dramatically reduce the efficiency of the interface circuit. Thermoelectric micro-generators are known to provide very small output voltage in the range of tens of mVs to hundreds of mVs. Design of interface circuits that can deliver suitable power and efficiency from as low voltage as possible can be a real challenge. In some designs a separate sub-block called "cold-startup" is utilized which is active only during the startup. The minimum voltage with which the system can start power conversion thus becomes an important design parameter.

Target output voltage, target output power and output voltage ripple are the design parameters imposed by the application circuits. For designing a general purpose interface circuit, one practical option can be making the circuit configurable for different load requirements.

1.5 Objective of the thesis

The goal of this work is the design of a fully integrated, self-starting, ultra-low voltage interface circuit with high output power and maximum power point capability for energy harvesting from thermoelectric generators, mainly for wearable electronics under the paradigm of Wireless Body Area Sensor Network (WBASN) applications. To this end, the output power of the fully integrated circuit should reach hundreds of μW while maintaining the maximum power delivery to the load. The minimum start up voltage also must be less than 200 mV which is a typical available voltage from TEGs connected to the body for a wearable sensor node of roughly 20 cm^2 size. The circuit is implemented in 180 nm standard CMOS technology without using any off-chip components. This study includes the following tasks:

- Study the characteristics of the DC-DC converter previously designed by our research group for variable input voltage;
- Propose a circuit design to make the charge pump reconfigurable with variable number of stages to achieve MPPT,

- Propose a novel MPPT algorithm to eliminate the interruption associated with the open circuit measurement required by the algorithms present in the literature,
- Design and implement the digital maximum power point tracking circuit,
- Design and implement the interface circuit with regulated output voltage,
- Layout and send the test chip for fabrication with configurable number of stages,
- Validation of the test chip with and without MPPT.

Achieving these objectives will provide us with an energy harvesting interface circuit that can meet the real time power demand of IoT nodes existing in the literature such as the node with multiple sensors proposed in [18] for environmental monitoring. This IoT node is composed of CO, CO_2, UV, temperature and humidity sensors and employs an ATmega328p micro controller. By elimination of the power hungry CO_2 sensor and replacing the microcontroller with the one with 1 V supply, the node's required power for sensing and signal processing which is reported to be 1 mW can be met by the solution proposed in this thesis. Another example of such nodes is the falling detection IoT node introduced in [19]. Another circuit can be found in [20] where a wearable sensing for continuous monitoring of ECG and PPG signals are proposed.

1.6 Thesis Contributions

In this thesis a fully integrated autonomous interface circuit is proposed which has about two times higher output power and about half the minimum input voltage performance, compared the state of the art proposed in the literature for fully integrated solutions. The minimum start up voltage has also been maintained as low as 170 mV which is within the range of output voltage of the tiny TEGs when connected to the body. A novel MPPT algorithm is proposed that guarantees continuous operation of the application circuits without using any battery or energy storage element. The optimized DC-DC converter is fabricated and tested. Parasitic elements added during the fabrication procedure are also identified and modeled that creates an opportunity for further optimization of the chip layout. A comparison table that summarizes the contribution is present at the end of chapter 7. When compared with interface circuits which are not fully integrated, our circuit performs similarly, however full integration for IoT devices is necessary because of considerable cost and size benefits. On the other hand when fully integrated designs are considered, our approach performs significantly better in terms of output power. This is mainly because in our approach the LC-tank oscillator output resistance and the charge pump input resistance are optimized to

match. In addition, the start up voltage is also low because of using LC-tank oscillator front-end. A novel MPPT algorithm is introduced and implemented for maximum output power delivery under varying ambient and load conditions, which doesn't exist in the literature.

1.7 Thesis outline and Roadmap

The main focus of the thesis is the design a circuit level implementation of the MPPT block for the previously proposed DC-DC converter based on LC-tank and charge pump circuit. The MPPT algorithm design and implementation is completely novel for this type of DC-DC converters. Cadence software suit [21] has been used as the CAD tool for all the simulations and layout drawings. Cadence is one of the mostly used commercial tools in the design of Analog and digital VLSI circuits that uses many technology library information from chip manufacturers including UMC 180 nm technology [22], which is the technology used to fabricate this chip. However, similar to all automated design tools, it has some deficiencies in accurately modeling the manufacturing variations. Due to this factor, a discrepancy has been observed between the post layout simulation results and the measurement results, which is explained in detail in chapter 7.

The remaining part of the thesis is organized as follows:

Chapter 2 discusses background information on different energy harvesting techniques. Chapter 3 is the literature review on the DC-DC converter design for thermoelectric energy harvesters. Basic principle of voltage step-up DC-DC converter is described in chapter 3 including the different types of LC-tank oscillators as subcircuit blocks. The advantages and the drawbacks of the existing low voltage interface circuits for the thermoelectric generators are also discussed in this chapter.

In chapter 4, characteristics of the LC-tank Charge Pump DC-DC converter are studied considering variable input voltage for MPPT. The proposed MPPT algorithms in the literature are reviewed, and a novel MPPT algorithm alternative is introduced.

Chapter 5 demonstrates the circuit level implementation of the interface sub-blocks and their verification using simulation results. In addition, a comprehensive comparison between the interfaces reported in the literature and the proposed design is provided.

The comparison of the validation data from the fabricated test-chip, pre-silicon simulation, and the model based analytical results are presented in Chapter 6.

The conclusions from this work and possible design improvements as future steps are discussed in Chapter 7.

CHAPTER 2

2 Background

2.1 Common energy harvesting techniques

The amount of energy available from tiny energy harvesters is in the range of some tens of μW per unit. The only exception is photovoltaic solar energy harvesting, which can reach up to some hundred mW/cm^2 in the presence of outdoor sunlight. Table 2.1 demonstrates the characteristics of some of the available energy sources [10]. The utilization of energy harvesting blocks in a system will only be practical when the overall harvested energy is more than the energy consumption of the single block in a given timeframe. All of the energy sources in Table 1 can be harnessed for IoT and wearable applications depending on the environment. Thermoelectric is a suitable type of energy for wearable electronics, where body heat can be used as a reliable source of energy to be harnessed. Energy harvesting techniques are elaborated in the following sections.

Table 2.1: Ambient energy and characteristics of micro-power generators [10].

	PV Solar	Thermoelectric	Piezoelectric vibration	Electromagnetic Vibration	Ambient RF
Power density	Outdoor: 100 mW/cm^2 Indoor: < 100 μW/cm^2	50-100 μW/cm^2 per ºC	10-200 μW/cm^3	1-2 μW/cm^3	0.0002-1 μW/cm^2
Output voltage	0.5 V Max	10-100 mV	10-20 V (open ckt)	Few 100 mV	3-4 V (open ckt)
Availability	Lighted environment	Surfaces with ΔT	Hz-kHz Vibration	Hz vibration	Vicinity to radiation sources
Pros	High Power Density Well Developed Technology	Non intermittent / Less intermittent than alternatives	High Voltage Well Developed Technology	Well Developed	Antenna can be integrated Widely Available
Cons	Intermittent Highly dependent on light	Low Voltage Need ΔT	Highly Variable output, Large Area, High output impedance	Bulky, Low power density, Low output Voltage	Very sensitive to the distance from the RF source

2.1.1 Solar energy harvesting

Solar energy is one of the most abundant sources of energy available for IoT nodes, and can be harvested using tiny photovoltaic cells integrated to sensor nodes. A photovoltaic cell is usually modeled as a current source with a highly varying output impedance with changing illumination conditions. Therefore, use of interface circuits that enable maximum power point tracking is mandatory to increase efficiency. Photovoltaic cells can typically provide voltages above 300 mV when exposed to high intensity of light. The amount of current, however, is in the range of some micro amps for the tiny cells. The outdoor output voltage is typically high enough to be used as the input voltage of the fully integrated DC-DC converters that use MOSFETs. For indoor applications, however, the output voltage and current of the cell can dramatically drop. The building blocks of a smart node based on solar energy harvesting is depicted in Figure 2.1. Photovoltaic cells have the property to convert incident light into electricity under the concept of charge separation of two materials with different conduction mechanism [23]. These materials are composed of p-type and n-type semiconductors, which enable the flow of charge. Despite abundance of sunlight, solar harvester output power is very intermittent due to variations in solar radiation. Figure 2.2 (a) depicts the typical electrical model of solar PV cell. Figure 2.2 (b) shows sample miniature PV cells for micro-scale solar energy harvesting.

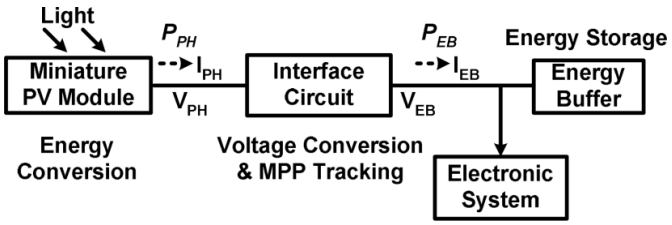


Figure 2.1. The building blocks of a smart node based on solar energy harvesting [12].

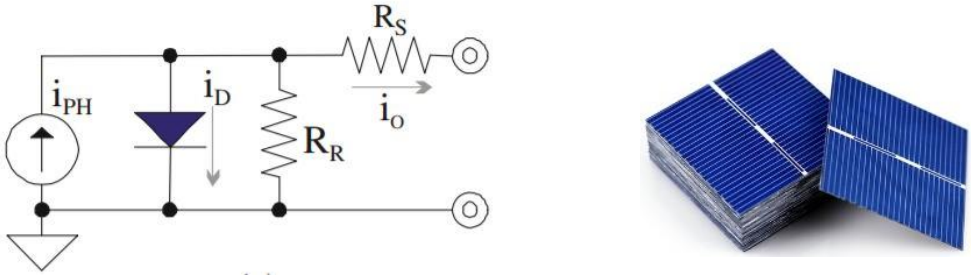


Figure 2.2. (a) Typical one diode PV cell model [11]. (b) Sample miniature PV cells for micro-scale solar energy harvesting 22 mm × 17 mm TSPV, 1 mW at MPP.

Due to variations at the source, an energy storage element such as a battery or a super capacitor is necessary to prevent system power outage. Some examples of interface circuit design for solar energy harvesting in IoT applications can be found in [24] [25] [26]. Figure 2.3 demonstrates the block diagram of a typical boost converter used as the interface circuit for micro-scale solar energy harvesting.

In this circuit the duty cycle of the pulse at the gate of the NMOS switch is dynamically altered based on the measured power output of the solar cell to adjust the effective input impedance of the load in order to find the new maximum power point.

2.1.2 Thermoelectric energy harvesting

Thermoelectric energy harvesters utilize the Seebeck effect to convert thermal energy into electric energy. Figure 2.4 (a) illustrates a schematic of a thermoelectric generator and Figure 2.4 (b) shows a tiny TEG for micro-scale energy harvesting.

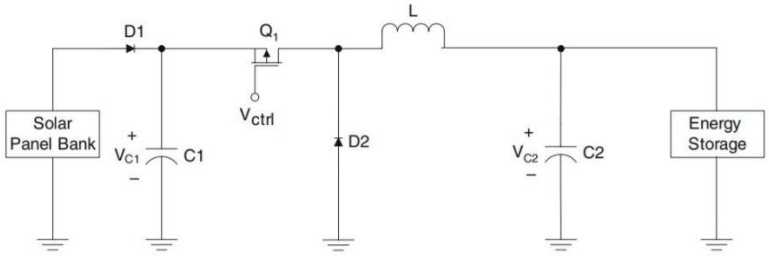


Figure 2.3. Block diagram of an interface circuit for solar energy harvesting [13].

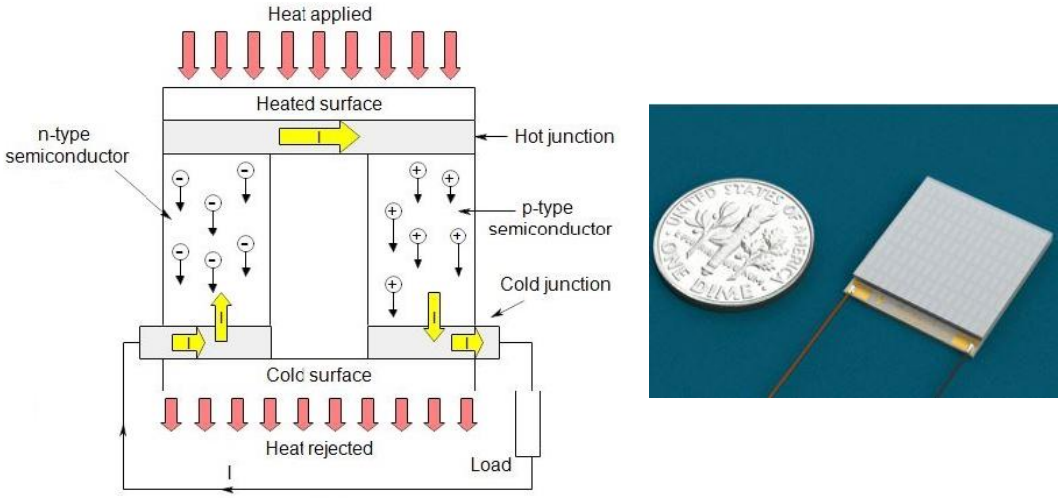
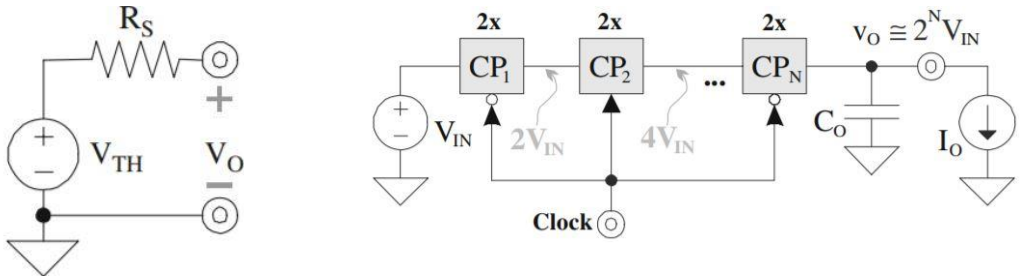


Figure 2.4. (a) Thermoelectric generator based on the seebeck effect (b) tiny TEG for micro-scale energy harvesting, 16 mm ×16 mm TEG, 0.2 mW at MPP [24].

Thermoelectric generators offer considerable miniaturization since there is no moving part in them as opposed to the vibration and electromagnetic energy harvesters, which makes them ideal options for small scale energy harvesting if temperature difference is present in the application [27]. In fact, thermoelectric generators consist of numerous thermocouples which are connected in a matrix of series and parallel connections. The number of series thermocouples determine the output voltage and the number of parallel thermocouples determine the output current level [24]. The thermopiles of the thermocouple consist of p-type and n-type semiconductors to generate the voltage drop across the p-n junction due to the different mobility of charge carriers that are stimulated and flow from high temperature terminal to low temperature terminal. The generated voltage is proportional to the temperature difference ($V=\alpha.\Delta T$). The proportionality constant (α) is the Seebeck coefficient of the thermoelectric material. The Seebeck coefficient is a measure of the magnitude of an induced thermoelectric voltage in response to a temperature difference across that material given in volts per kelvin (V/K). [28] The highest Seebeck coefficient among undoped semiconductors belongs to selenium with 900 μV/K and the third highest is for silicon with 440 μV/K at room temperature. Doping increases the Seebeck effect considerably. Since the highest observed Seebeck coefficient is limited to at most hundreds of microvolts per Kelvin [29], large temperature gradient is necessary to generate mV output at small scale area. Due to the limited Seebeck coefficient of the thermoelectric generators, the output voltage of the thermocouple is in the range of 20-400 mV for the typical miniature size thermoelectric generators (TEG) for some K temperature difference between the hot and the cold plates [30]. Figure 2.5 (a) illustrates the typical model used for thermoelectric energy harvesters. Designing the interface circuits for the TEGs should include voltage step-up and cold start-up. Cold start up is a term in thermoelectric energy harvesting, used when the minimum voltage required for the circuit to start voltage boost up is very low, i.e. a less than MOSFETs threshold voltage.. A schematic block diagram of



(a) *(b)*

Figure 2.5. (a) TEG model, (b) A typical Interface circuit for voltage boost up based on charge pump [11].

an interface circuit based on charge pump for thermoelectric energy harvesting is depicted in Figure 2.5 (b). The functionality of the charge pump (CP) based interface circuit is explained in detail in section 2.2.

2.1.3 Piezoelectric energy harvesting

Piezoelectric material can be used to convert the kinetic energy of mechanical movements present in the environment into electrical energy. In Figure 2.6 the block diagram of the typical setup for piezoelectric energy harvesting is provided. The conversion can be described through the mass-spring motion model. The piezoelectric material connected to a cantilever generates AC voltage. The amplitude of the generated voltage is proportional to the substrate stress. An electrical equivalent model of piezoelectric energy harvesters is illustrated in Figure 2.7. There is an output capacitance in the model which is typically some nF for tiny piezoelectric materials. Piezoelectric harvesters typically have high output impedance. Therefore, in their interface circuit design, high input impedance should be fulfilled to get the maximum power from the source. In addition, in contrast to solar and thermoelectric sources, piezoelectric materials generate AC signal. Therefore, use of full bridge rectifiers together with the voltage boosters are very popular in the interface circuits. The boost converters for this application typically require inductors in the order of tens of μHs which are impractical to be integrated inside a chip [10]. A typical interface circuit for piezoelectric energy harvesting is based on a negative to positive converter circuit followed by a boost converter. Figure 2.8 illustrates an interface circuit for the piezoelectric energy harvesters. In this circuit the AC voltage generated by the piezoelectric module is being rectified by the rectification block. The accumulated energy charges the piezoelectric capacitance, Cp. A control circuitry detects the maximum voltage and turns on S2 as soon as voltage reaches its maximum that results in charging the inductor. When the inductor reaches its maximum current which is detected by a current

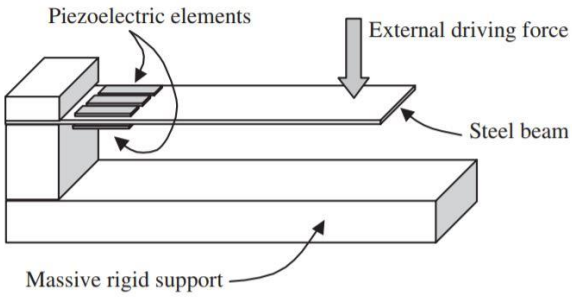


Figure 2.6. Schematic of the typical setup for piezoelectric energy harvesting [19].

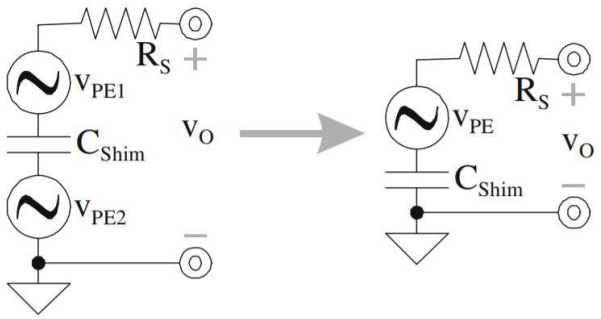


Figure 2.7. Circuit equivalent model for the piezo electric harvester [11].

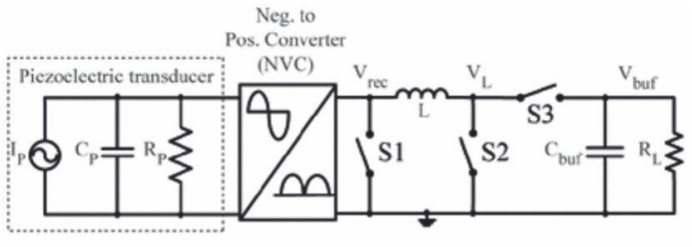


Figure 2.8. Schematic of a SECE interface for piezoelectric energy harvesters.

sensor, the control circuitry turns S2 off and S1 and S3 on. At this point the energy charged in the inductor is dissipated on the load. Detecting the maximum voltage and current levels adds significant control circuitry and makes the piezoelectric energy harvesting complicated, which can be considered as its drawback.

2.1.4 Electromagnetic (Vibration) energy harvesting

In addition to piezoelectric conversion, Faraday's Law offers another method for energy harvesting from movement, and is abundantly found in applications such as human motion. According to this law, when a coil moves in the vicinity of a magnetic field, electric current can flow through it. The printed coils and permanent magnets are utilized for the micro-scale harvesting techniques. The converted output voltage depends on the magnetic field strength, number of turns of the coil and the rate of change of the flux (the last one is a function of displacement length and frequency). These critical parameters limit on-chip integration in typical environments. A novel batteryless interface circuit design for electromagnetic energy harvesting is presented in [31]. Figure 2.9 demonstrates the 2 cm × 3.5 cm cylindrical harvester with 2 magnets embedded in the cylinder. The movement of the moving magnet creates electric current in the coil. The AC current generated in the coil is fed to a novel interface circuit that has rectification circuit composed of a passive and active AC-DC converters for higher efficiency. The DC voltage then is fed to a DC-DC converter to

provide the required voltage for the application. Figure 2.10 shows the block diagram of the system.

2.1.5 Ambient RF energy harvesting

RF sources are widely distributed and can be found abundantly in most environments nowadays. Some common sources are wireless radio and TV broadcasting antennas, and cellular towers. In applications where the density of the ambient radio frequency waves is high enough, the RF energy harvesting can be promising due to relatively simple interface circuits and integrated antennas. A typical block diagram of an RF energy harvesting system is shown in Figure 2.11. There are many challenges associated with RF energy harvesting such as design optimization of the antenna to cover a wide bandwidth of RF signals and dealing with the highly variable input power of the signals.

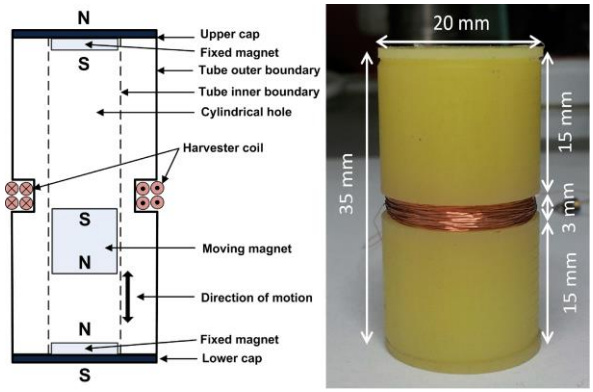


Figure 2.9. Electromagnetic energy harvester [21].

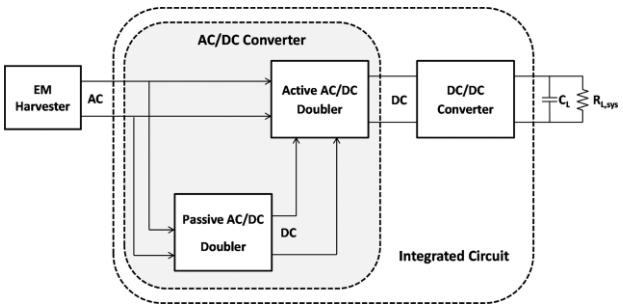


Figure 2.10. The integrated interface block diagram of the electromagnetic energy harvester [21].

Despite these challenges, RF energy harvesting has gained a lot of attention in WSNs due to the existence of a sink node in such networks that is usually connected to the grid for long range communication, and therefore can provide sufficient RF power for the nodes of the sensor network that needs harvesting [32].

2.1.6 Hybrid energy harvesting

Each energy source comes with its limitations and strengths. More than one source of energy can found in the majority of the applications. For instance in WBASN there are many sources available such as body heat, body movement, solar and RF.

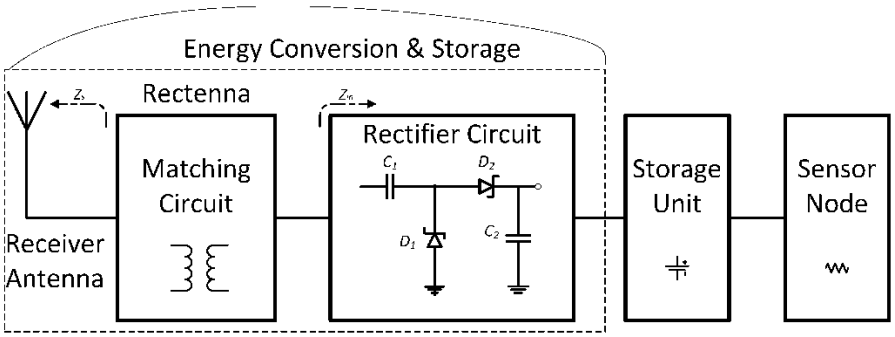


Figure 2.11. RF energy harvesting circuit components [22].

Using hybrid energy harvesting circuits, which allow utilization of multiple energy sources, can improve system reliability, efficiency and output power to meet the demands of the load without the necessity for a storage element such as a battery or a supercapacitor. An ideal hybrid energy harvesting system can offer higher output power which in turn can increase the wireless communication range of IoT nodes when multiple sources are available. Such a system must turn into a single source energy harvesting whenever only one source of energy is available. Considering the inherent features of different sources of energy, the design of such an interface circuit is complicated and will continue to be a hot research topic. Figure 2.12 demonstrates the general block diagram of a hybrid system in the presence of only a single source. A system in [33] is introduced that uses solar and RF sources in IoT application. It is reported that the addition of the RF energy harvester to the indoor solar system has increased the robustness of the system toward rapid light intensity changes. A piezo-electromagnetic system is introduced in [34] that utilizes piezo electric and electromagnetic sources together. It is reported that the introduction of the hybrid system has

increased the bandwidth that leads to higher output power in a larger range of oscillation frequencies. In [35] a hybrid system that uses RF and Thermal energy sources for active RFID tags is introduced. Based on the simulation results maximum of 80% increase is achieved in the output power.

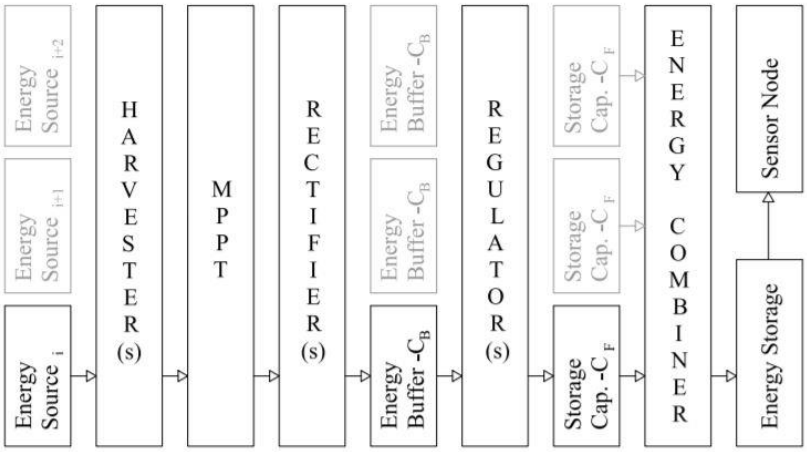


Figure 2.12. Block diagram of a hybrid energy harvesting system when only a single source is present [24].

Thermoelectric generators are suitable candidates for the applications where temperature difference is present. Smart home, industrial and healthcare applications are some examples. Indoor and outdoor solar energy harvesting is typically promising for many applications however some type of energy storage elements should be utilized to get the most of solar energy. Precision agriculture and environmental monitoring can be two examples for solar energy harvesting application. In transportation and logistics as well as healthcare applications energy electromagnetic and piezo electric energy harvesting can be promising due to the presence of some type of movement.

2.2 Efficiency and output power of the interface circuits

Power efficiency is one of the important characteristics of the interface circuits to evaluate their feasibility of use. Due to very stringent power budget in the low power energy harvesting, higher efficiency is highly desired to minimize the energy losses and transfer the maximum power to the load. The power efficiency (η) of an interface circuit can be expressed as (2.1).

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{V_{out}.I_{out}}{V_{in}.I_{in}} \times 100\% \quad (2.1)$$

where P_{out} is the output power and P_{in} is the input power. Power is defined as multiplication of current and voltage. The output power itself is a very important factor imposed by the application circuits requiring a minimum amount that should be met. If the output power requirement of an application cannot be met with a specific energy harvesting circuit, high efficiency will no longer be important. In such scenarios use of a storage device such as battery becomes inevitable. Some WSN protocols with duty cycling are recently introduced that can tolerate such stringent power budgets [36]. However, these techniques reduce network throughput by putting nodes to sleep for a considerable fraction of time.

For fully integrated solutions, minimizing chip area is another factor related to cost. To facilitate the optimization methods, a good circuit model is necessary to implement with theoretical expressions. In ultra-low power energy harvesting applications, the output of the energy harvester is limited to at most couple of hundreds of mV, typically less than the threshold voltage of the MOSFET. As a result, design of a fully integrated interface circuit for micro-scale energy harvesting with high efficiency, high output power, MPPT and cold start up is a real challenge.

CHAPTER 3

3 Related work on TE Energy Harvesting Interface Circuits

3.1 Introduction

Thermoelectric generators (TEG) are suitable for applications in which creating temperature gradient is feasible. A wide range of examples can be found in industry, home applications and transportation. The applications of TEGs in the past, were limited to industrial cases such as energy harvesting from chimney, forges, hot parts of different machines and airplane or car's engines. TEGs are reliable devices that can be miniaturized. Further miniaturization of the TEGs and fabrication of flexible TEGs have paved the way towards using them in the newly emerging IoT smart nodes and WBASN nodes. TEGs typically have very high output current compared to other counterparts with the same size and dimensions. However, their ultra-low output voltage is a drawback. To confront this problem DC-DC boost converters are used to boost up the voltage to a desired level. There are two types of DC-DC converters:

- *Conventional boost converter with one switching transistor*

  Inductors are used as temporary energy storage elements in this type of DC-DC converters. There is a switching element that receives a pulse with varying duty cycle. The output DC voltage level is a function of duty cycle. These conventional boost converters offer high power efficiency and output power. However, the inductor size necessary for these converters is in the range of some μH, which cannot be achieved by on chip inductors. The cost associated with necessary external inductor is the main disadvantage associated with this converter architecture.

- *Charge pump based boost converter*

  In the charge pump based boost converter, capacitors are used as temporary energy storage to boost DC voltage level from one stage to the other. Therefore, the higher stages can achieve higher voltage. The main advantage of charge pumps is the ease of integration. Charge pump structure requires two out of phase pulses which are typically generated by ring oscillators. Large capacitors are used in this type of boost converter which are subject to large energy dissipation when used in switching circuits. In addition, larger capacitors require larger area on the chip, which in turn

increases the chip size and cost. However, for a fully integrated solution, optimization of the charge pump structure seems to be the only way to achieve voltage boost up.

Full integration of interface circuits brings about significant cost and area saving for the wearable micro power electronic applications. Therefore, fully integrated solutions are more desirable and in some cases such as implant sensors in WBAN are inevitable. Considering the above mentioned types of boost converters, charge pump based converter is the only suitable type for fully integrated solutions provided that a good optimization is performed to achieve high efficiency and output power. One of the main challenges associated with the charge pump based converters is the reduced output power for ultra-low input voltage levels specifically when the voltage is below the threshold voltage of MOSFET gates. Charge pump based DC-DC converter circuits consist of high performance, MOSFETs with typical threshold voltage of couple of hundreds of millivolts when low V_t devices are used. Low V_t devices are known to have high power consumption due to leakage. Therefore the size of these devices should be optimized for minimum power consumption. In order to increase the output power of an interface circuit, higher current is necessary for a given target voltage. This in turn is a challenging requirement since the size of circuit elements should grow, and the use of low V_t devices should be considered that lead to higher leakage and thus higher power loss. One way to solve threshold voltage problem is use of on-chip inductors. However, integration of inductors can typically lead to inductors with lower quality factors. In the following sections, a comparative study of charge pump based interface circuits has been provided. The introduction of LC-tank oscillators as the clock source for charge pump circuits and our research group's optimization methods on this solution is discussed in detail. Maximum power point problem definition for TEG energy harvesting and the features of the optimized charge pump with LC-tank and variable input voltage is introduced.

3.2 Charge pump based DC-DC converters

The block diagram of a thermoelectric energy harvesting system for a smart IoT node using charge pump based DC-DC converter is illustrated in Figure 3.1. The output of the energy harvester is connected to both the charge pump circuit and the oscillator. The circuit consists of two basic sub-blocks: oscillator and the charge pump. The oscillator circuit generates the necessary non-overlapping signals for the switching mechanism of the charge pump capacitors. The oscillation amplitude plays an important role in the voltage conversion ratio.

In an ideal scenario, when there is zero loss, the output voltage of each stage of the charge pump is the addition of previous stage voltage and oscillation amplitude.

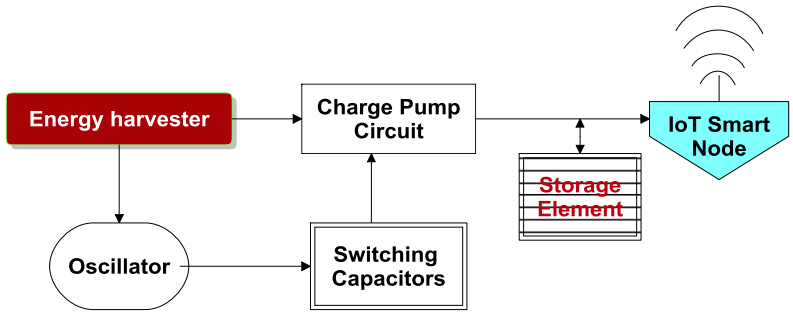


Figure 3.1. The block diagram of a charge pump based DC-DC converter for energy harvesting applications.

The function of the Charge pump circuit is to boost up the input voltage into high DC level while transferring charge from one stage to another through the switching mechanism. The capacitors used as the energy switching elements in this circuit are relatively large. The use of storage element, such as small rechargeable battery or a super capacitor, is necessary to reduce ripples and supply the load if the output power is not sufficient. This is the scenario assumed in this thesis to design batteryless interface circuit. For the cases that the output power is not sufficient to meet the real time demand of an application circuit, duty cycling of the power should be considered by first charging the storage capacitance and then connecting the charged capacitor to the load. The charge pump circuit topology used in our thermoelectric interface is illustrated in Figure 3.2. Each stage of the charge pump is composed of two cross-coupled NMOS and PMOS pairs with two capacitors. The two non-overlapping clock signals drive the charge pump switches to accumulate the charges in capacitors and transferring to the next stage. Once CLK_1 is low and CLK_2 is high (Vin), N_1 is on while N_2 and P_1 are off. Then C_1 will accumulate charges to achieve V_{in} voltage drop across it. The opposite phase of the clock signal switches on N_2, while N_1 and P_2 are switched off. C_2 will start to be charged from the charge pump input voltage. The configuration of fully charged C_1 with clock voltage in series, achieves $2V_{in}$ at the drain of N_3 and N_4 nodes. In the same manner after each stage, the voltage of the previous stage is added to the maximum voltage of the oscillation signal. Consider the ideal case without attenuation of the oscillation signal and zero voltage drop at the switching MOSFETs. Under these conditions, the output voltage of the n^{th} stage for an n-stage charge pump and oscillation amplitude V_{osc} can be described as (3.1).

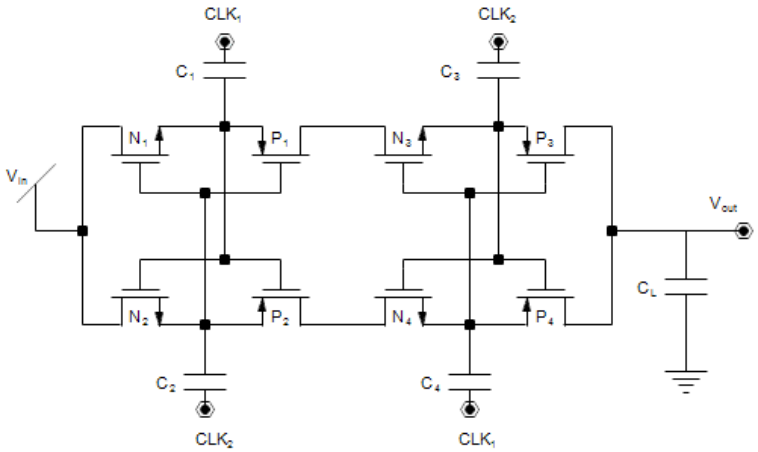


Figure 3.2. Dual-phase charge transfer cross-connected charge pump [37].

$$V_n = V_{in} + n \times V_{osc} \tag{3.1}$$

where V_{in} is the input voltage of the charge pump from TEG, V_n is the voltage of nth stage, V_{osc} is the oscillation amplitude and n is the number of stages. Important performance metrics of a DC-DC converter in ultra-low power energy harvesting applications are power efficiency, output power, and minimum startup voltage. The area minimization is another important factor for fully integrated solutions.

The dual charge transfer branch charge pump used by our team is the state of the art latest version of the Dickson charge pump [38]. The added advantage of this design is its switching activity twice per clock cycle and therefore twice power delivery for every clock. In previous topologies, the switching activity is only once per cycle. In [37], [39]–[41] some optimizations to the Dickson charge pump are reviewed, such as minimized voltage ripple at each stage, reduced start-up voltage, and increased efficiency.

3.3 Oscillator circuit for the DC-DC converter design

Non-overlapping pulses are essential in the operation of the charge pump based DC-DC converters. Oscillators are used to generate these signals. High efficiency, voltage multiplying oscillator circuits are necessary for the appropriate operation of the charge pump. There are two types of oscillators typically used, ring oscillators and LC-tank oscillators. The most common example for the CMOS oscillator is the ring oscillator, which is popular among DC-DC converter designers as a clock generating circuit. A ring oscillator is simple and easy to integrate. The frequency can be controlled through the bias current. On

the other hand, LC-tank based oscillators are commonly used in microelectronic telecommunication applications since they can typically offer higher frequency band of oscillation. Integrated LC-tank oscillators require larger area compared to ring oscillators due to on-chip inductors. However, LC-tank oscillators can start oscillating with much lower voltages than ring oscillators. In addition ring oscillator's oscillation amplitude is limited to rail-to-rail, while LC-tank oscillators can easily go beyond the supply range due to the presence of inductors. Threshold voltage of CMOS technology is a serious limitation for ring oscillator's output power when exposed to ultra-low voltages. In section 3.3.1 and 3.3.2 these two types of oscillators are reviewed.

3.3.1 Ring oscillators

Figure 3.3 depicts the topology of ring oscillators. Ring oscillators are composed of odd number of cascaded inverter stages. The voltage swing of an ideal ring oscillator is 0-V_{DD}.

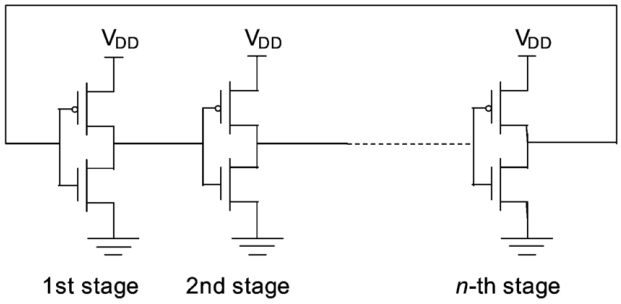


Figure 3.3. Topology of the ring oscillator circuit (odd n).

Oscillation frequency is a function of the inverter propagation delay under unit load condition, and the number of inverter stages. If the propagation delay of a single inverter is t_d, the oscillation frequency can be calculated as (3.2):

$$f = \frac{1}{2.N.t_d}. \tag{3.2}$$

Small area and ease of integration are the two main advantages of ring oscillators in most of the charge pump based DC-DC converters presented in the literature [42]–[45]. On the other hand, there are several drawbacks associated with ring oscillators, which makes them challenging to use for TEG interface circuits. These disadvantages are as follows:

1. Ring oscillators, which can drive high output current and power, cannot sustain oscillations at typical micro-TEG voltages below the threshold voltage of the MOSFETs.

2. Required large and numerous number of buffer circuits to enhance the current deliverability of the ring oscillator topology leads to high dynamic and static power dissipation.
3. Subthreshold oscillator circuits can work around threshold voltage limitations, but both frequency and output power suffers with subthreshold circuit design.

LC-tank oscillators have been proposed by our research group in [46]–[50] as alternatives to ring oscillators to overcome cold start up problem, and boost output power as discussed in detail in section 3.4.

3.3.2 LC-tank oscillators

On-chip LC-tank oscillators are usually used in telecommunication circuits. There are many topologies proposed in the literature [51], [52]. LC-tank oscillators are typically implemented in CMOS technology using two cross-coupled NMOS transistors that create necessary negative resistance for the oscillation to be sustained. In terms of using LC-tank oscillators for energy harvesting purpose, design topologies with minimum number of elements are desirable since addition of components results in higher dynamic and static power losses. On-chip inductors typically have higher ohmic resistance than discrete inductors causing lower quality factor. Optimized designs are necessary to benefit from the advantages of fully integrated solutions. The required switching frequency for charge pump based DC-DC converters are hundreds of MHz for the continuous charge delivery with minimum ripple at output. This frequency range can be obtained with on-chip capacitors with pF range and integrated inductors with nH range for the fully integrated LC-tank oscillator circuits.

3.4 Use of on-chip LC-tank oscillators for fully integrated DC-DC Converters

In [53] one of the first fully integrated interface circuits for micro-scale energy harvesting from thermoelectric generators is proposed. This solution is a charge pump based DC-DC converter with a current measurement sensor and power management circuit to track maximum power point. The oscillator used in this circuit is a ring oscillator. The drawback of the proposed circuit is its very high input resistance in the range of some kΩ which makes it impractical for typical miniature TEGs with output resistances of some tens of ohms. In addition, due to threshold voltage problem, the start-up voltage is 500 mV which is available only with very large TEGs. The first reported circuit that uses LC-tank oscillator together with a charge pump can be found in [54]. The topology of the circuit proposed in this paper is shown in Figure 3.4. In this topology, an LC-tank oscillator is used, which has a doubled

oscillation amplitude compared to input voltage. The main motivation in replacing ring oscillators with LC-tank oscillators in this paper is that LC-tank oscillators can reach oscillation amplitudes higher than V_{DD}. This is the main requirement in overcoming the threshold voltage limitation with very small input voltages in the range of <200mV. In addition, LC-tank oscillators provide the two non-overlapping signals with 180^o phase shift by design, which is essential for the functionality of the charge pump.

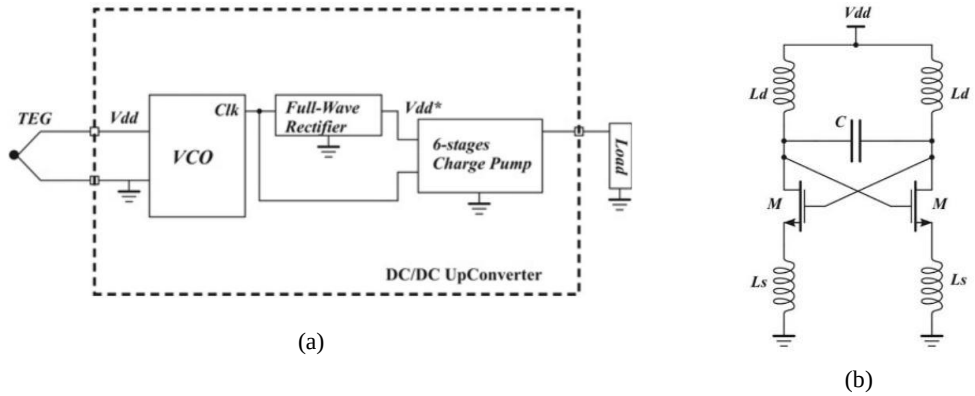
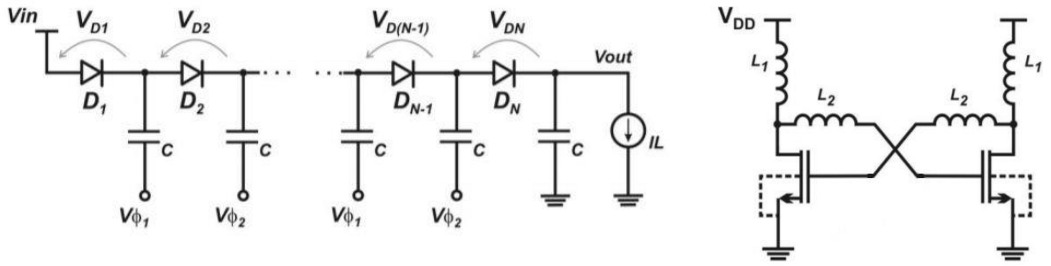


Figure 3.4. (a) DC-DC converter topology using LC-tank oscillators first proposed in [47], (b) VCO Circuit.

Cascade buffers are not required to improve current drive in LC-tanks, as compared to ring oscillators. In this topology a rectifier is utilized to provide the charge pump with the required DC voltage rectified from the oscillator signals. Two non-overlapping signals are used to feed the charge pump capacitors. The oscillator used in this topology has four inductors, and is based on transformer feedback between the foot and the leg inductors. The W/L ratio of the cross-coupled NMOS transistors in UMC 180 nm technology is 3500. The size of the diodes used in the rectifier are W=800 μm and L=800 nm. A capacitor of 1 nF is also used that occupies 500 μm × 200 μm. This topology is therefore not area efficient. Furthermore, the results are reported only based on simulation. The peak efficiency is 20% with 100 mV input and 10 kΩ load resistance. The maximum output power is 180 μW at 125 mV input voltage.

In [55] a similar topology is investigated that offers lower start-up voltage compared to [54]. The enhanced swing ring oscillator (ESRO) using 4 inductors is utilized as the oscillator of the charge pump based DC-DC converter. The oscillator and the charge pump circuit used in this topology is shown in Figure 3.5. The behavior of this oscillator is also described using mathematical equations of phase and voltage gain. In this paper a Dickson charge pump topology is used. Even though the state of the art 83 mV start-up voltage is achieved without the need to use start-up circuits, the maximum efficiency of the overall converter is 1%. The

idea of using on-chip transformers to boost up voltage swing of the oscillator with minimum start-up voltage is proposed in [56]. The oscillation amplitude in this LC-tank structure, in which inductors form the secondary coil of a transformer with the winding turn ratio of N, is $2NV_{in}$.



(a) (b)

Figure 3.5. (a) The DC-DC converter topology using initially proposed LC-tank oscillators, (b) VCO circuit [55].

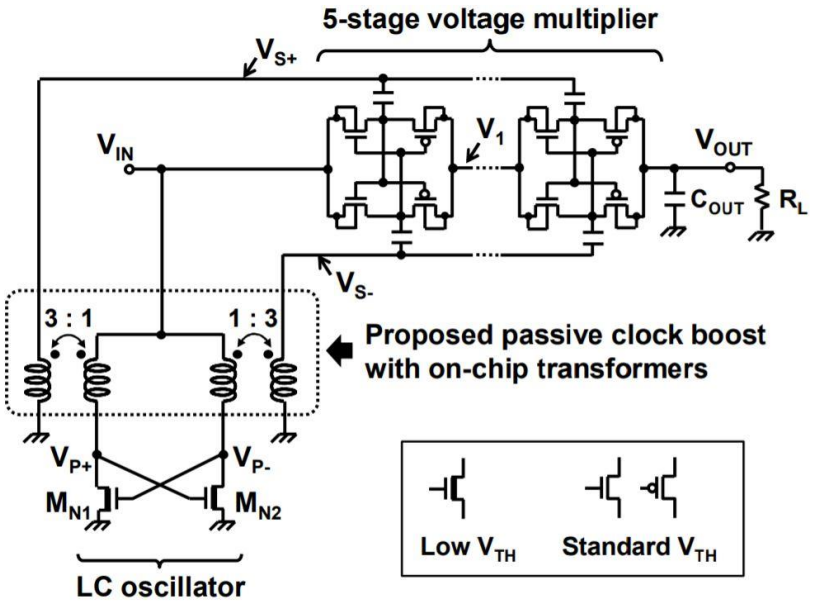


Figure 3.6. The circuit schematic of the fully integrated DC-DC converter proposed in [56].

This voltage conversion ratio (VCR) is the highest for a fully integrated implementation in the literature. The circuit implemented in this paper is demonstrated in Figure 3.6.VCR of this structure can be calculated using equation (3.3) for an ideal scenario, which neglects the leakage and parasitic elements:

$$V_{out} = V_{in} + n \times 2 \times N\, V_{in} \tag{3.3}$$

where n is the number of charge pump stages and N is the transformer winding ratio. In fully integrated solutions, high winding ratio cannot be reached. In this work, a 5 stage charge pump and 2 transformers with winding ratio of 3 are used.

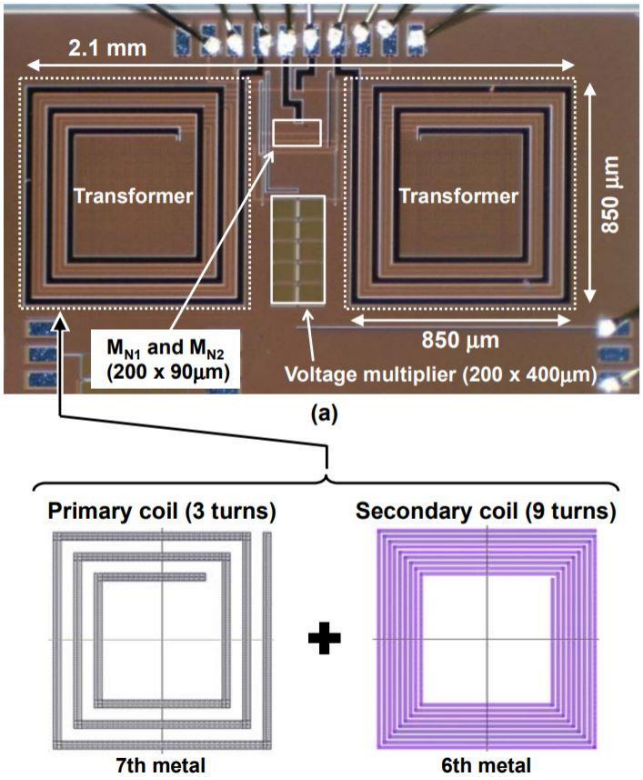
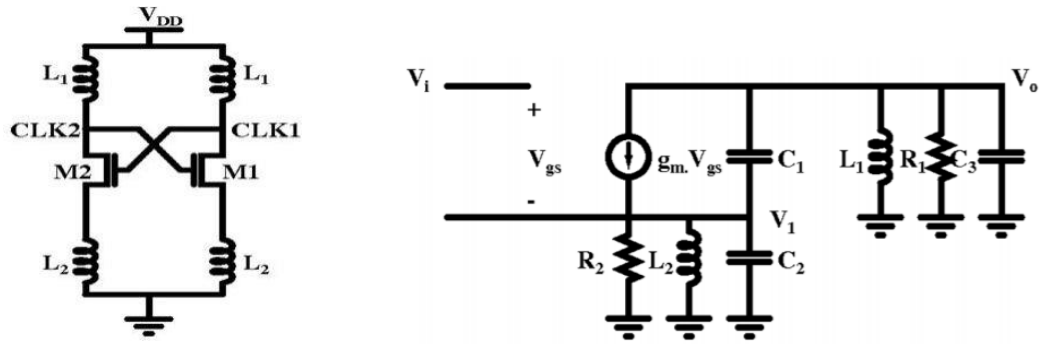


Figure 3.7. The chip micrograph of the circuit proposed in [56] and implemented in 65 nm technology.

Therefore, a VCR of 30 is expected with output target voltage of 1 V. The chip micrograph is shown in Figure 3.7 which shows the implementation of on-chip transformer. There are some drawbacks associated with this topology even though the theoretical VCR seems appealing. Efficiency optimization method is lacking. The calculated efficiency is less than 3% due to the high losses associated with on-chip transformers. Another important drawback is low output power. In this topology the maximum power of 10 µW is reached with 1 MΩ load when the input voltage is 120 mV, for which the output voltage reaches 770 mV. Due to this current delivery limitation, the VCR significantly decreases to 4.7 with a 1 MΩ load from the theoretical 30 for open circuit. Our research group has been developing solutions and design optimization methods to increase the output power of the DC-DC converter and at the same time improve the minimum start up voltage and the efficiency of the system. In [46], a new LC-tank oscillator topology was proposed that runs the dual charge transfer

branch charge pump. The optimization of the circuit to increase efficiency has been done based on the oscillator's half-circuit model. Figure 3.8 demonstrates the proposed LC-tank topology and the corresponding half circuit model. In this paper the parasitic elements of L_1 and L_2 inductances are extracted using 3D Planar Electromagnetic Field Solver Software.



(a) (b)

Figure 3.8. (a) The proposed LC-tank topology and (b) the corresponding half circuit model for optimization [46].

Using the half circuit model and with the target oscillation frequency of 1 GHz, the necessary g_m value and therefore the optimum oscillator cross coupled NMOS transistor sizes are obtained for the maximum voltage swing. By optimization on the oscillator elements, the efficiency of 22% is reported for the fabricated chip. The maximum output power is reported to be 31 μW while the minimum start up voltage is 150 mV.

In [47], [48] a novel model based optimization method is proposed. In this study the LC-tank oscillator and the charge pump circuit are redesigned so that the output impedance of the oscillator matches with the input impedance of the charge pump circuit. Figure 3.9 (a) depicts the oscillator circuit topology with minimum number of elements. The enhanced model of the LC-tank considering all parasitic elements is shown in in Figure 3.9 (b), where R_P, R_{DS}, R_A, C, and C_A refer to the parallel resistance of inductor L, oscillator NMOS drain to source resistance, the resistance between M1 drain and M2 drain, parallel capacitance of the inductor, and capacitance between M1 drain and M2 drain respectively. The gate capacitance is small compared to charge pump capacitors. Therefore, in the series structure $C + 2C_A$ is dominant. In order to increase the oscillation amplitude, large inductors are desirable. Therefore, in this research the largest achievable standard inductors are chosen within the layout area constraint for low cost fabrication. In UMC 180 nm technology this limit is 14 nm. Oscillation frequency and the power consumption of this oscillator topology can be calculated using Equation (3.4) and (3.5):

$$f_0 = \frac{1}{2\pi\sqrt{L(C+2C_A)}} \tag{3.4}$$

$$P_T = \left(V_{PP}/2\sqrt{2}\right)^2 \left[\frac{1}{R_{DS}} + Cf_0\right] \tag{3.5}$$

$$C + 2C_A = C_0 + C_{P1} \tag{3.6}$$

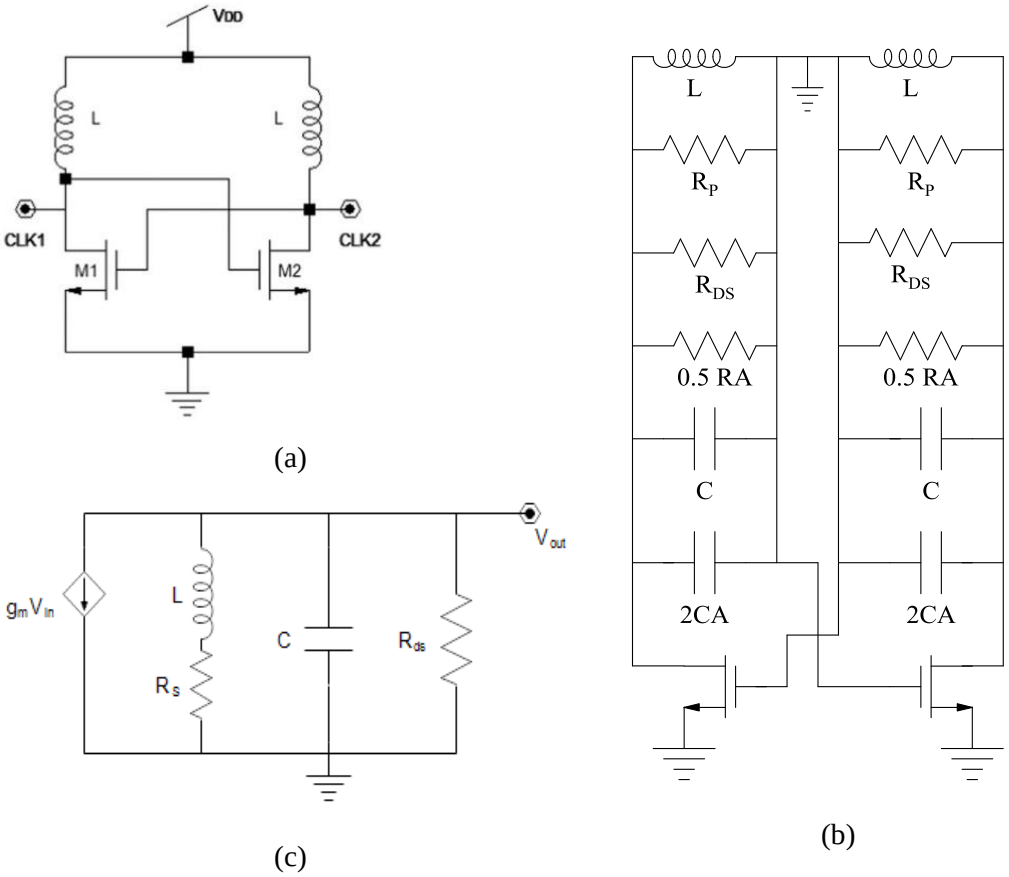


Figure 3.9. (a) The oscillator circuit topology with minimum number of elements, (b) circuit model of the LC-tank and the cross coupled NMOS transistors that create the negative resistance necessary to sustain the oscillation, and (c) simplified model of the oscillator [49].

where f_0 is the oscillation frequency, L, C and R_s are the inductance, equivalent capacitance and the series resistance of the inductor, respectively. P_T is the total power dissipation which is the addition of static power dissipation on the R_{DS} and the dynamic power dissipation due to switching. Since R_{DS} << R_P and R_A the dominant static power dissipation accrues in the NMOS transistors. For the optimization purpose, equation 3.6 is necessary where C_0 is the LC-tank coupled with charge pump capacitance and C_{P1} is the equivalent parallel capacitance of the charge pump capacitors, C_n. Figure 3.10 illustrates the charge pump

circuit topology for a three stage charge pump. To better understand the functionality of the charge pump, ON and OFF paths in a 3 stage charge pump at the instant that $CLKn = high$ and $CLKn + 1 = low$ is illustrated in Figure 3.11. Capacitors of the first stage are charged to V_{DD} when the clock pulse is low. Later when the clock pulse becomes high, the capacitance of the next stage is charged.

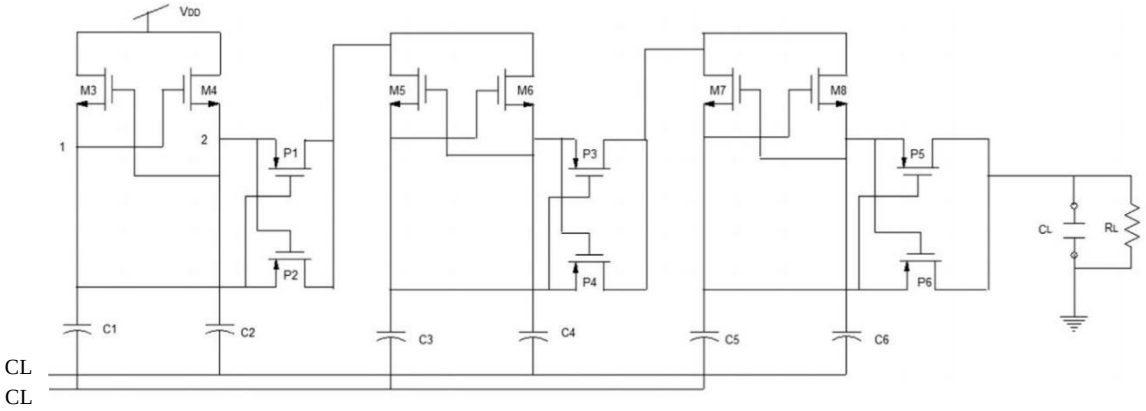


Figure 3.10. The charge pump circuit topology for a three stage charge pump used in [49].

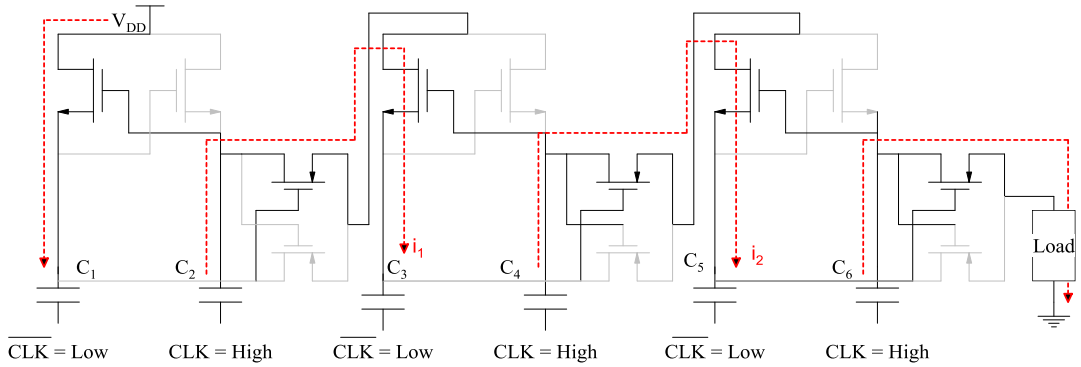


Figure 3.11. ON and OFF paths in a 3 stage charge pump at the instant that CLKn = high and CLKn + 1 = low.

The voltage to which the capacitance will be charged is given in (3.7):

$$VC_{n+1} = VC_n + V_{clk} \tag{3.7}$$

where VC_{n+1} is the voltage of the charge pump capacitance of stage n+1, VC_n is the voltage of the charge pump capacitance of stage n and V_{clk} is the oscillation amplitude of the clock signal. In order to do the model based design optimization to deliver maximum power to the output, a half circuit model of the oscillator connected to the charge pump is introduced in [49]. Figure 3.12 illustrates the equivalent circuit model for the n stage DC-DC converter. All the charge carrying MOSFETs are represented by resistors. R_P represents the equivalent resistance of the PMOS while R_M is equivalent resistance of the NMOS. R_L represents the

load resistance. These correspond to the ON resistances of these devices. The impedance of the charge pump network can be written as in equations (3.8-3.12):

$$Z_1 = (R_{P1} + R_{N3}) - j\left({}^{1}/_{\omega C_1} + {}^{1}/_{\omega C_4}\right) \tag{3.8}$$

$$Z_2 = (R_{P3} + R_{N5}) - j\left({}^{1}/_{\omega C_3} + {}^{1}/_{\omega C_6}\right) \tag{3.9}$$

$$Z_{n-1} = \left(R_{P(2n-3)} + R_{N(2n-1)}\right) - j\left({}^{1}/_{\omega C_{2n-3}} + {}^{1}/_{\omega C_{2n}}\right) \tag{3.10}$$

$$Z_n = \left(R_{P2(n-1)} + R_L\right) - j\left({}^{1}/_{\omega C_{2n-1}}\right) \tag{3.11}$$

$$Z_{CP} = {}^{1}/_{\sum_1^n \left({}^{1}/_{Z_n}\right)} \tag{3.12}$$

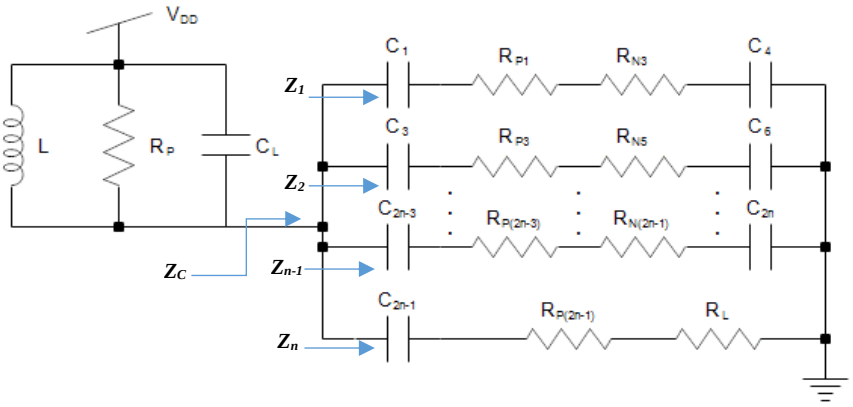


Figure 3.12. The half circuit model proposed for the model based design optimization to deliver maximum power [49].

When the charge pump connects to the LC-tank oscillator, the charge pump capacitance will be seen by the oscillator. Therefore, C_{P1} in (3.6) can be described by (3.13). C_0 can then be described by (3.14). Equation (3.15) shows the g_m required to sustain oscillation, which determines the size of cross coupled NMOS transistors of the LC-tank oscillator.

$$C_{P1} = \frac{-(R_N^2C^2 + LC_0 - LC) + \sqrt{(R_N^2C^2 + LC_0 - LC)^2 + 4LCC_0}}{2L} \tag{3.13}$$

$$\frac{R_s(C_0 + C_{P1})}{L} = \frac{n-1}{(R_P + R_N) - j\left({}^{1}/_{\pi C}\right)} + \frac{1}{(R_L + R_N) - j\left({}^{1}/_{2\pi C}\right)} \tag{3.14}$$

$$g_m = \frac{R_S}{R_S^2 + {}^{L}/_{(C_0 + C_{P1})}} \tag{3.15}$$

where C , R_N , R_p represent first stage charge pump capacitance and ON NMOS resistance respectively. It is worth stating that the NMOS and PMOS transistors used in other stages

have the same size of stage one. In addition, the value of the charge pump capacitance used in all stages are also same. In order to solve the optimization problem, output voltage and power equation are given in (3.16) and (3.17). The output equation is a recursive equation with V_0= 0 V.

$$V_n(t) = \left(\frac{1}{\sqrt{2}} V_{pp}\, e^{\frac{-t}{C(R_P+R_L)}} + V_{n-1}\right) \times e^{\frac{-t}{C_s(R_P+R_L)}} \times \left(1 - \frac{R_P}{(R_L+R_P)}\right) \tag{3.16}$$

$$P_n(t) = \frac{V_n^2}{R_L} + \frac{V_{pp}^2}{8}\left[\frac{1}{R_{DS}} + C_L f_0\right] + \left(\frac{V_{pp}}{2\sqrt{2}} - V_{DD}\right)^2 C f_0 + n\frac{V_{pp}^2}{8} C f_0 \tag{3.17}$$

where V_{pp} is the peak-to-peak oscillation amplitude. The model based optimization of this structure can be achieved by the following stages:

1- Choosing Maximum L to increase the oscillation amplitude, the largest achievable inductance value in standard UMC180 nm technology is 14 nm.
2- Based on the output target voltage, choose the number of stages. Higher number of stages lead to higher output voltages and increase power losses at the same time.
3- Select charge pump MOSFET sizes considering the MOSFET resistance and capacitance curves in the specified technology.
4- Choose a value for charge pump capacitance C.
5- Calculate C_0 and C_{P1} using equations (2.11) and (2.12).
6- Calculate required g_m using (2.13).
7- Calculate V_{pp} considering (2.15) and $\frac{dP_n}{dC} = 0$.
8- Based on the gm and Vpp determine the size of LC-tank NMOS transistors.

With this model based optimization, considerable increase is achieved in the output power delivery and cold start-up voltage and efficiency in a fully integrated DC-DC converter. There are not much fully integrated DC-DC converters for ultra-low voltage energy harvesting reported in the literature. Table 3.1 shows a comparison between the measurement results of the DC-DC converter proposed in [49] and state of the art fully integrated DC-DC converters for thermoelectric energy harvesting in the literature. All reported data in this table are from measurement results. The circuit proposed by our research group demonstrates superior output power capacity while maintaining an ultra-low start up voltage of 170 mV. The efficiency based on post layout simulations was 34%, but due to significant process variation in V_t of both NMOS and PMOS charge pumps the efficiency has dropped. This mismatch will be covered in details in chapter 6 where

experimental results are discussed. With this state of the art output power and ultra-low voltage start up, the proposed chip can be utilized as a reliable source for batteryless IoT and wearable applications.

Table 3.1. Comparison between the DC-DC converter previously proposed by our research group and state of the art fully integrated DC-DC converters for thermoelectric energy harvesting in the literature.

Ref.	Proc. (nm)	Min. input (v)	Output (v)	Power output (µW)	Maximum efficiency (%)	Area (mm^2)
[57]	65	0.10	1.2 @ 0.14 V input & 1 MΩ load	10@ 0.12 V input	33@ 0.10 V input & 1 MΩ load	2.13
[58]	130	0.08	1.0 @ 0.08 V input & 1 MΩ load	1 @ 0.08 V input	24 @ 0.08 V input & 1 MΩ load	-
[59]	250	0.6	1.2 @ 0.6 V input & 14 kΩ load	140 @ 1.5 V input	76 @ 1.5 V input & 14 kΩ load	1.96
[60]	55	0.22	1.9 @ 0.22 V input & 345 kΩ load	11 @ 0.22 V input	37.4 @ 0.22 V input & 345 kΩ load	0.74
[61]	120	0.07	1.25 @ 0.07 V input & 92 kΩ load	17 @ 0.07 V input	58 @ 0.07 V input & 92 kΩ load	0.6
[62]	250	0.5	1.2 @ 1.2 V input & 14.4 kΩ load	120 @ 1.2 V input	83 @ 0.07 V input & 14.4 kΩ load	-
[63]	180	0.14	5.2 @ 0.35 V input & 520 MΩ load	4 @ 0.45 V input	50 @ 0.45 V input & 300 MΩ load	0.069
Measurement results for the chip proposed by our research group in [49]	180	0.17	2.4 @ 0.33 V input & 10 KΩ load	900 @ 0.32 V input	25 @ 0.22 V input & 2 kΩ load	1.98

3.5 Maximum power point tracking in thermoelectric harvesting circuits

Maximum power point tracking is known as the act of adjusting the input resistance of the interface circuit to match with the output resistance of the source (thermoelectric device). A thermoelectric generator can be modeled as a voltage source with a series resistance. V_{TEG} is the open circuit voltage of the thermoelectric generator and R_{TEG} is the output resistance. Figure 3.13 shows the first order model of the TEG connected to the power management system. TEGs are composed of array of thermocouples. The number of series connections determine the open circuit voltage per Kelvin, while the number of arrays in parallel dictates the short circuit current. Three different category of TEG devices has been introduced in the

literature. Among these, which are described in Table 3.2, thin film TEGs and CMOS compatible TEGs are recent research areas [64].

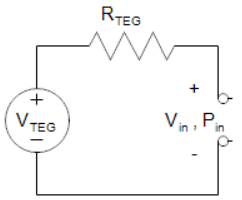


Figure 3.13. First order model widely accepted for thermoelectric generators.

Table 3.2. Comparison of Three different category of TEG devices [57].

Type	Conventional TEG	Thin Film TEG	CMOS Compatible TEG
Size	10.54 cm^2	11.4 mm^2	16 mm^2
Power Density	3μ $W/K^2/cm^2$	143μ $W/K^2/cm^2$	0.026μ $W/K^2/cm^2$
Open Circuit Voltage	2.4 $mV/K/cm^2$	1.23 $V/K/cm^2$	12.5 $V/K/cm^2$
Internal Resistance	0.5 Ω/cm^2	2632 Ω/cm^2	1.5 G Ω/cm^2
Thermocouple Density	$12/cm^2$	$4738/cm^2$	$29375/cm^2$

The temperature difference is very limited for wearable and IoT applications. A typical range of 0.5 K < ΔT < 10 K temperature difference is expected across the TEG for energy harvesting from body heat [64], which results in high variations in power output and effective output impedance. Therefore, maximum power point tracking is usually an essential part of energy harvesting form TEGs for maximum power output. MPPT provides impedance matching between the interface circuit and the TEG device. Alternatively, it can be perceived as adjusting the input voltage of the interface circuit to half of TEG open circuit voltage. The necessity of MPPT is the major difference between DC-DC converters in energy harvesting systems and the ones used in common power conversion applications. Typically the maximum power point tracking method for thermoelectric generators involves measurement of the open circuit voltage and adjusting the interface circuit's input voltage to half of the measured open circuit voltage [65]–[72].

In [65] a complex mechanism is implemented to adjust the input voltage of the converter to half open circuit voltage. To this end a switching circuit disconnects the converter from the TEG and the open circuit voltage is sampled using an ADC. The difference between the sampled open circuit voltage and input voltage is translated to a digital value in a digital block and is used to alter the switching frequency of the transformer that is used in the input path. In [67] a single-inductor dual-input dual-output (SIDIDO) is implemented. The

equation of switching frequency of the converter and the input impedance is given. A switching mechanism regularly connects and disconnects the TEG and each time the open circuit voltage and the input voltage are sampled using a sample and hold circuitry. These two voltages are then compared and the result adjusts the direction of an up/down counter. The output of the counter is then used to adjust the duty cycle of the switching pulse. The similar sample and hold mechanism to measure open circuit TEG voltage and Vin is utilized in other references two. This mechanism not only affect real time power delivery to the load that requires bulky storage devices to compensate but also significantly adds to the complexity and the number of system components. Therefore we have tried to avoid this mechanism.

Maximum power point tracking for the charge pump based DC-DC converters can be achieved by altering the voltage conversion ratio, oscillation frequency or the size of the charge pump capacitance[25] [73]. In [74] the oscillation frequency is adjusted based on the comparison of the open circuit TEG voltage and Vin which is obtained based on the same sample and hold mechanism. The oscillation frequency is altered by adjusting the input voltage of the ring oscillator. In [25] a current sensor is utilized that measures the load current to adjust the oscillation frequency, number of stages and the flying capacitance values to reach to the maximum power point. This method used output power measurement to do maximum power point tracking which avoids disconnecting the circuit from TEG, however, using current sensor and 3-D maximum MPPT has significantly increased the complexity of the system. Figure 3.14 depicts a schematic diagram of charge pump based DC-DC converters with maximum power point tracking capability. For the charge pump based DC-DC converters that use ring oscillators, the input impedance can be described by a closed form equation of (2.16) [73]

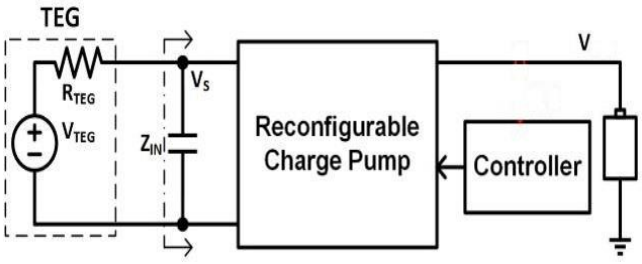


Figure 3.14. Schematic diagram of charge pump based DC-DC converters with maximum power point tracking capability.

$$Z_{in} = \frac{1}{(VCR)^2} \sum_{i \in caps} \frac{(a_{c,i})^2}{f_0 \times C_i} \tag{3.18}$$

where $a_{c,i}$ represents the charge multiplier, f_0 is the switching frequency, C_i is the used capacitor value, and *VCR* is the conversion ratio of the charge pump. Equation 3.18 introduces the elements that can be used to adjust the input impedance of the charge pump based DC-DC converter. The charge multiplier is typically not tunable unless a tunable capacitor is utilized, which requires larger chip area. The switching frequency and conversion ratio are usually the two parameters that are used to tune the converter input impedance. There is significant difference between charge pumps with ring oscillators and charge pumps with LC-tank oscillators in that the voltage swing amplitude and the oscillation frequency of ring oscillator do not change with change of the load or the number of stages of the charge pump, whereas such changes in load can substantially affect the parameters in LC-tank oscillator. The reason is the loading effect of the charge pump on the LC-tank oscillator as discussed in detail in Section 4.1. This is due to the fact that the LC-tank oscillator effective output impedance is significantly higher than the output buffering stage of a typical ring oscillator. Therefore, effective input impedance of a charge pump based DC-DC converter is highly nonlinear due to the change in oscillation characteristics. These effects are explained in detail in chapter 4. Because of the above mentioned differences, conventional algorithms cannot be used for charge pump based DC-DC converters with LC-tank oscillator. In this thesis a novel MPPT algorithm is introduced which will be explained in chapter 4.

3.6 Output voltage regulation for batteryless applications

The latest trend in ambient energy harvesters is achieving autonomous power management systems that can supply enough output voltage and power to meet the real time demands of application circuits without the need for batteries or other energy storage elements such as super capacitors [75]–[78]. In applications with an energy harvester to charge a battery, output voltage regulation is less stringent due to the fixed voltage of the battery. However, in applications for which the energy harvesting circuit is being directly used to empower the application circuitry, regulation is essential. Minimal design that can fulfill output voltage regulation while having very small energy consumption overhead is low-dropout regulators (LDO). LDOs can regulate voltage even if the supply voltage is very close to the desired output voltage. A block diagram of this regulator is shown in Figure 3.15.

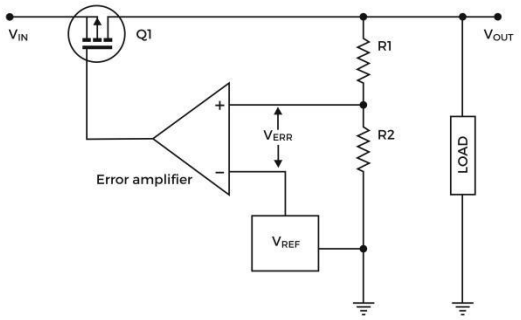


Figure 3.15. The block diagram of a typical low-dropout regulator.

This topology is based on the op-amp output feedback. The output voltage is sensed via op-amps noninverting input and the reference voltage is applied to the inverting input. If the output voltage drops a negative differential voltage will be sensed by the op-amp. Therefore the op-amp output voltage will drop significantly due to op-amps large gain. This in turn will turn on the PMOS shown by Q1 in the picture and the output voltage will be increased when the V_{IN} to V_{OUT} path is closed. On the other hand, if V_{OUT} goes higher that the regulation voltage, the differential voltage will be positive that will act in the opposite direction and will open the Q1 switch. The V_{IN} to V_{OUT} path will be open leading to decrease in the output voltage.

With the advances in the CMOS technology miniaturization the required supply voltage for consumer electronics is rapidly decreasing. Many applications circuits can run with 1 V which is the target voltage of the voltage regulator implemented in this thesis.

CHAPTER 4

4 Fully Autonomous Interface Circuit Design for Thermoelectric Energy Harvesting

4.1 Input-output characteristics of the optimized charge pump based DC-DC converter with LC-tank oscillator

Design of fully integrated micro scale energy harvesters for wearable electronics and IoT applications is a challenging task due to multiple requirements such as cold start-up, high output power, and high efficiency. In addition, smart sensor nodes in such applications are typically highly dynamic since a combination of three major tasks of sensing, signal processing and wireless data transmission takes place at every instance. On the other hand, the ambient condition is also highly varying. Usually cold plate of the TEGs in wearable electronics is prone to highly variable temperature profile, and thus the temperature gradient varies. Considering these factors, an autonomous system is required to auto-adjust itself to ensure maximum power delivery to the load for a wide range of variations. For the inductive boost regulators, this is typically achieved by measuring the TEG open circuit voltage periodically and adjusting the effective input impedance of the inductor by changing the switching frequency of the converter. For a system with a regulated output, this can be perceived as a simpler output voltage regulation problem considering the fact that the autonomous power management system is responsible to provide the desired output voltage level for a wide input voltage range, when the load is fixed. Based on the promising results from the optimized charge pump based DC-DC converter with LC-tank oscillator as presented in Table 3.1, the converter is further investigated to implement MPPT block to make it fully autonomous and self-sufficient for batteryless applications.

4.2 Reconfigurable charge pump

Number of stages is a key factor in determining the voltage conversion ratio (VCR) of a charge pump based DC-DC converter. It also has an inverse relation with the input impedance of the charge pump as described by equation (3.18). On the other hand, higher number of stages bring about higher dynamic and static power dissipation. Therefore, changing the number of stages affects the efficiency, output power and input impedance of the system all at the same time. There is another nonlinear effect in LC-tank driven charge pump circuits that does not exist in ring oscillator driven charge pumps. Increasing the number of stages increases the load on the oscillator and hence decreases the oscillation amplitude. Figure 4.1 demonstrates the LC-tank small signal model. In this model, charge

pump is shown as an admittance connected to the LC-tank. Voltage gain transfer function based on the small signal model is given in equation (4.1).

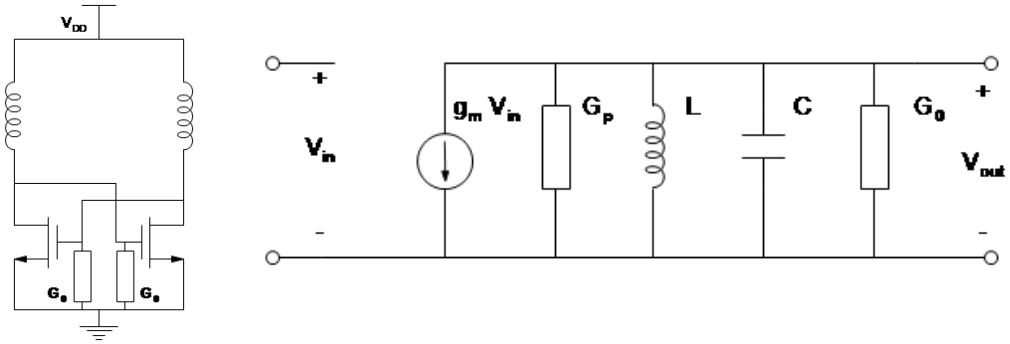


Figure 4.1. LC-tank small signal model with Charge pump modeled as the load. [71]

$$\frac{V_{out}}{V_{in}} = -g_m\left(\frac{G_p + G_0}{\left(G_p + G_0\right)^2 + \left(\frac{1}{L\omega} - C\omega\right)^2} + \frac{\frac{1}{L\omega} - C\omega}{\left(G_p + G_0\right)^2 + \left(\frac{1}{L\omega} - C\omega\right)^2}\, j\right) \tag{4.1}$$

where g_m represents NMOS transconductance, G_p models the parasitic conductance of both the inductor and the capacitor, G_0 models the charge pump load, L and ω are the inductance and oscillation frequency respectively. C represents the NMOS gate-drain and drain-source capacitance. The phase shift $\emptyset$ between V_{out} and V_{in} is described by equation (4.2). Oscillation condition requires that $\emptyset = \pi$. By applying the oscillation condition ω can be calculated as (4.3).

$$\emptyset = \pi - \tan^{-1}\left(\frac{\frac{1}{L\omega} - C\omega}{G_p + G_0}\right) \tag{4.2}$$

$$\omega = \frac{1}{\sqrt{LC}} \tag{4.3}$$

By applying the result obtained in (4.3), to (4.1) the voltage gain of oscillation will be simplified to (3.4). In addition, start-up condition requires greater-than-unity gain [79], which gives the minimum oscillation start-up condition described by (4.5)

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m}{G_p + G_0} \tag{4.4}$$

$$g_m > G_p + G_0 \tag{4.5}$$

It is worth emphasizing that g_m and G_0 values depend on V_{DD}, which is the output voltage of the TEG in this topology, but G_p which is modeling the L and C non-ideality, is almost constant. g_m of a MOSFET transistor is given by the well-known simplified equation in (4.6). From (4.4) it can be seen that the oscillation amplitude decreases if admittance of the charge pump increases (input impedance decreases), which is the case with increase in the number of stages as described earlier in (3.12).

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \tag{4.6}$$

In order to achieve a charge pump structure with adjustable number of stages, an innovative circuit is proposed. The proposed topology is depicted in Figure 4.2.

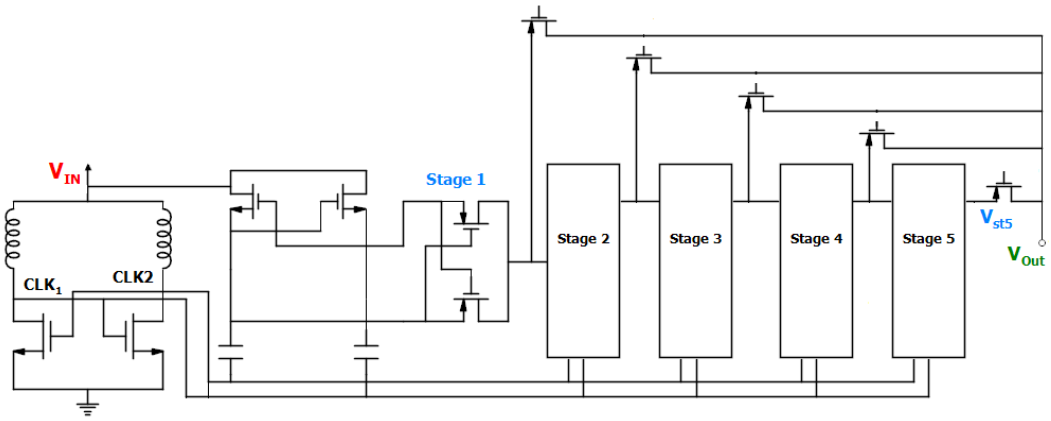


Figure 4.2. The proposed topology to create a charge pump with variable number of stages.

In this topology, large PMOS switches are used to control the path to the output. Only one PMOS switch can be ON at a time. For example when the gate voltage of stage 3 PMOS is low and all other stage PMOS gate voltages are high, the topology becomes a 3 stage charge pump. Since the path is designed to carry considerable amount of current, the PMOS switches are chosen and designed to be large and low Vt to minimize voltage drop. The drawback of these large low Vt PMOS switches is the increase in leakage. This topology offers minimum number of switches which is essential to minimize leakage. The size of these elements are given in chapter 6. Another unique feature of this topology is that the output voltage of all stages are maintained while MPPT is in progress. This is because of connectivity of clock signals and the output of the previous stage in all of the stages. This feature proves useful to overcome the problem of not having a reliable V_{DD} which is necessary to empower control circuitry. The control circuitry is composed of digital MPPT block, the comparator and the regulator circuits. The MPPT circuitry is digital with minimum power consumption. Vst5 is the output of stage 5 which is used as the supply

voltage for all digital blocks, and for the biasing circuitry of the op-amp and the comparator. These blocks will be discussed in detail in section 4.4.

4.3 Maximum power point for the charge pump based DC-DC converter with LC-tank oscillator

Charge pump circuit's voltage conversion ratio has direct relation with the number of stages. However, due to the loading effect of the charge pump on the oscillation amplitude of the LC-tank oscillator, analyzed in section 4.2, this is not a linear relation. Instead due to higher loading effect and decrease in

the oscillation amplitude, the output voltage will also decrease. In fact for a fixed value of load and input voltage, there is a specific number of stages that leads to the maximum output voltage which will be maximum output power for the fixed load. Maximum input power that can be delivered to the interface circuit can be defined as (4.7) when the input impedance of the interface circuit is equal to the output resistance of the TEG.

$$P_{in,MAX} = \frac{(V_{TEG})^2}{4\,R_{TEG}} \tag{4.7}$$

Figure 4.3 illustrates the block diagram of the energy harvesting system with respect to the first order TEG model. Z is defined by equation (2.10). Using TEGs with smaller R_{TEG} increases the maximum input power. However, due to the smaller thermocouple density in TEGs with lower R_{TEG}, higher temperature gradient (ΔT) is required to reach the minimum start-up voltage. From equation (4.7) the maximum input power only depends on V_{TEG} and R_{TEG} and therefore is fixed for any given ΔT. Power efficiency of the system is the amount of power that can be delivered to the load via a power management system over the maximum extractable power, calculated using (4.8).

$$\eta = \frac{P_{out}}{P_{in,max}} = \frac{\frac{{V_{out}}^2}{R_L}}{\frac{(V_{TEG})^2}{4\,R_{TEG}}} = \left(\frac{V_{out}}{V_{TEG}}\right)^2 \times \left(\frac{4\,R_{TEG}}{R_L}\right) \tag{4.8}$$

From equation (4.8) maximizing the output power will maximize efficiency for a given ΔT. In other words, if V_{out} is maximized for any given V_{TEG} and R_L the output power and thus the efficiency will be maximized. Changing the number of stages not only changes the output voltage but also affects the input impedance of the interface circuit and leads to a maximum power point. It is worth emphasizing that maximizing the output power is really

the ultimate goal when doing maximum power point tracking in circuits. For the inductive boost converters, this can be achieved by maximizing the input power of the converter by adjusting the input impedance of the converter to match with the output impedance of the power source.

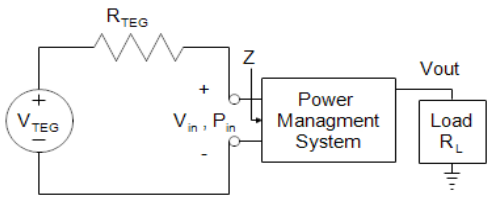


Figure 4.3. The block diagram of the energy harvesting system with respect to the first order TEG model.

However, due to change in efficiency of the charge pump based DC-DC converters with change in their input voltage for ultra-low voltage range, matching the input impedance with output impedance of the power source alone will not guarantee the maximum output power. Instead the output power itself should be maximized for any pair of V_{TEG} and R_L. Furthermore, as discussed in section 3.6, voltage regulation is an essential requirement for batteryless applications. Therefore, any voltages higher than the target voltage will be regulated down to the target voltage. Therefore, reaching the target voltage with minimum number of stages is desirable due to minimizing the power loss in multiple stages and to minimize the load of charge pump on the oscillator.

Based on the above discussion, a novel MPPT algorithm is proposed, which refrains from disconnecting the converter from the source for continuous operation, and instead uses output voltage comparison with the reference value. Maximum power point tracking (MPPT) algorithms in the literature are typically based on measuring the TEG open circuit voltage V_{OPEN} for impedance matching. This method has two drawbacks. First, it requires disconnecting the converter from the TEG. This results in delivering no power to load during V_{OPEN} measurement and considerable voltage drop for high load which can be a serious problem for baterryless or storageless applications. Second, maximum power point tracking by input impedance matching is applicable when the efficiency of converter remains constant for all impedance values, such as in inductive boost converters. The efficiency of the charge pump based DC-DC converters when performing in ultra-low voltage, close to the CMOS threshold voltage, is highly dependent on the input voltage. The efficiency drops

substantially when the input voltage drops. Therefore, the maximum power point tracking should be considered as directly maximizing the output power. Thus, in our proposed algorithm, search for maximum power point is based on the two following rules, first to deliver the required voltage, and second to minimize power losses:

1- Search for the stage that can generate the target output voltage
2- Minimize the number of stages while maintaining the output target voltage

The novel proposed MPPT algorithm is illustrated in Figure 4.4. In this flowchart, the paths in black demonstrate the search for the stage that generates output target voltage and the green path corresponds to reducing the number of stages to achieve the output target voltage with the minimum number of stages. In the proposed algorithm MPPT starts from stage 5. This is because of very low input voltages at cold-start up. Then the output voltage is compared to the target voltage, 1 V in our design. If the output voltage is less than the target voltage then the number of stages will be decreased by one. Decreasing the number of stages can lead to stages with higher output voltage as a result of decrease in the loading effect on the oscillator and increase in the input impedance of the charge pump that leads to higher input voltage. After each stage reduction, checking the condition of meeting the target voltage is repeated. If a stage can be found for which the target voltage is fulfilled, then that stage will be chosen and MPPT is still ON. Then starting from the stage that generates the output target voltage the algorithm tests if the target voltage can be achieved with a smaller number of stages. At the end the lowest number of stages will be locked, and MPPT will be turned OFF.

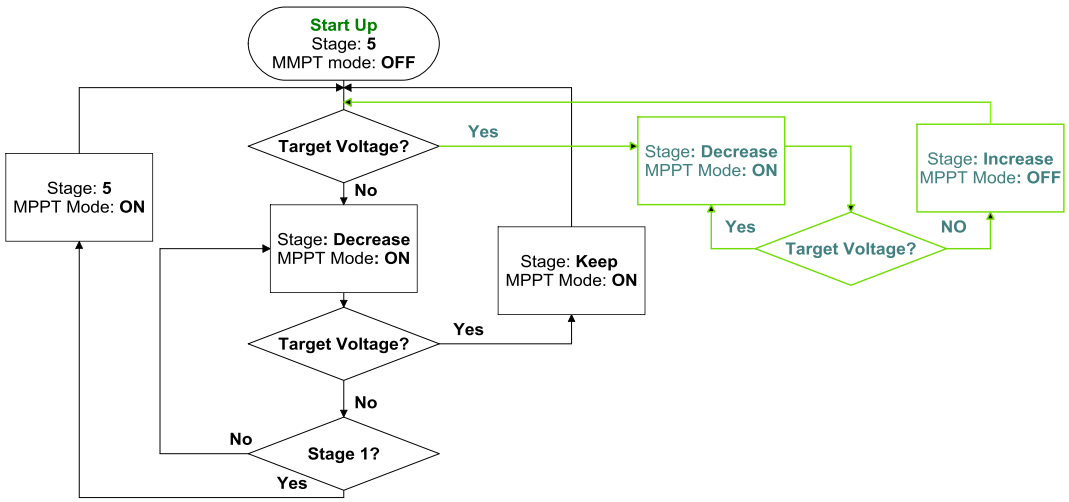


Figure 4.4. The proposed novel MPPT algorithm for charge pump based DC-DC converters with LC-tank oscillator.

It is possible that due to very heavy load or very small ΔT no stage can be found to supply the output with the target voltage. In this case the algorithm will keep searching until finding a new stage. The MPPT block turns on again searching for the maximum power point when the voltage drops to bellow the target voltage and the so called procedure will be repeated. This is done by a mechanism that initializes the MPPT block. This circuit is explained in section 4.5.

4.4 MPPT implementation

4.4.1 Logic design of the MPPT finite state machine

A finite state machine (FSM) is designed to implement this algorithm. This state machine is a mealy machine with one hot design approach for higher robustness towards glitches and noise. The state diagram of the proposed MPPT algorithm is given in Figure 4.5. The input of this state machine is a binary signal coming from a comparator, shown in blue in Figure 4.5. The signal is high if the output target voltage is reached and is low otherwise. In order to make the FSM simpler, the DC-DC converter structure with only one stage is neglected since the output voltage cannot reach the 1 V target voltage unless the input voltage is larger than 600 mV which is not a realistic scenario with tiny TEGs in WBASN applications. This has reduced the MPPT search to stages 2 to 5. The outputs of the FSM, shown in black in Figure 4.5, are the state signals S2:S3:S4:S5 which directly open or close the PMOS switches illustrated in Figure 4.2.

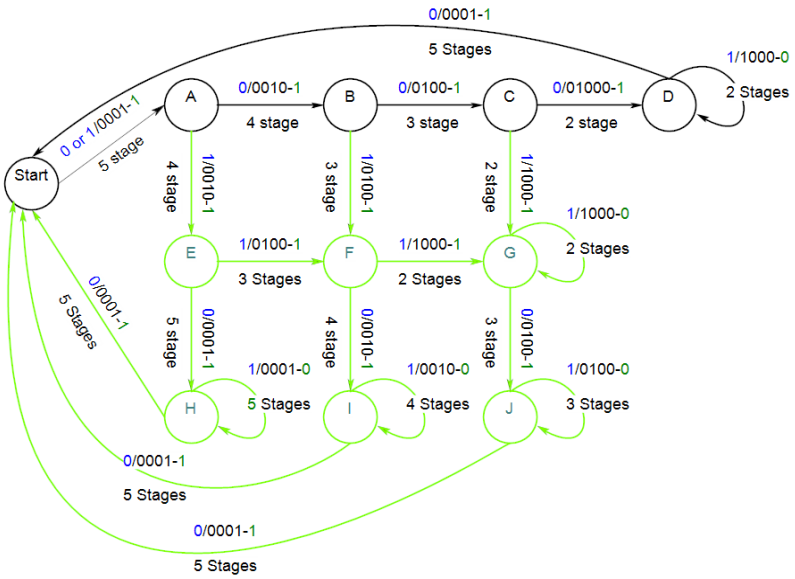


Figure 4.5. The state diagram of the proposed MPPT algorithm.

Table 4.1 . State table of the proposed FSM.

S	S	S^+ ($A^+B^+C^+D^+E^+F^+G^+H^+I^+J^+S^+$)		S2		S3		S4		S5		FSM_ON	
	(ABCDEFGHIJS)	0	1	0	1	0	1	0	1	0	1	0	1
Start	00000000001	00000000010	00000000010	0	0	0	0	0	0	1	1	1	1
A	00000000010	00000000100	00000100000	0	0	0	0	1	1	0	0	1	1
B	00000000100	00000001000	00001000000	0	0	1	1	0	0	0	0	1	1
C	00000001000	00000010000	00010000000	1	1	0	0	0	0	0	0	1	1
D	00000010000	00000000001	00000010000	0	1	0	0	0	0	1	0	1	0
E	00000100000	00100000000	00001000000	0	0	0	1	0	0	1	0	1	1
F	00001000000	01000000000	00010000000	0	1	0	0	1	0	0	0	1	1
G	00010000000	10000000000	00010000000	0	1	1	0	0	0	0	0	1	0
H	00100000000	00000000001	00100000000	0	0	0	0	0	0	1	1	1	0
I	01000000000	00000000001	01000000000	0	0	0	0	0	1	1	0	1	0
J	10000000000	00000000001	10000000000	0	0	0	1	0	0	1	0	1	0

Neglecting Stage 1 which is only useful for very high input voltages:

$$A^+ = \overline{Out_{CP}}\ \&\ (D) + Out_{CP}\ \&\ (A) \tag{4.9}$$

$$B^+ = \overline{Out_{CP}}\ \&\ (E) + Out_{CP}\ \&\ (B) \tag{4.10}$$

$$C^+ = \overline{Out_{CP}}\ \&\ (F) + Out_{CP}\ \&\ (C) \tag{4.11}$$

$$D^+ = Out_{CP}\ \&\ (H + D + E) \tag{4.12}$$

$$E^+ = Out_{CP}\ \&\ (F + I) \tag{4.13}$$

$$F^+ = Out_{CP}\ \&\ (J) \tag{4.14}$$

$$G^+ = \overline{Out_{CP}}\ \&\ (H) + \ Out_{CP}\ \&\ (G) \tag{4.15}$$

$$H^+ = \overline{Out_{CP}}\ \&\ (I) \tag{4.16}$$

$$I^+ = \overline{Out_{CP}}\ \&\ (J) \tag{4.17}$$

$$J^+ = S \tag{4.18}$$

$$S^+ = \overline{Out_{CP}}\ \&\ (A + B + C + G) \tag{4.19}$$

$$S2 = H + Out_{CP}\ \&\ (D + E) \tag{4.20}$$

$$S3 = I + \overline{Out_{CP}}\ \&\ (D) + Out_{CP}\ \&\ (A + F) \tag{4.21}$$

$$S4 = J + \overline{Out_{CP}}\ \&\ (E) + Out_{CP}\ \&\ (B) \tag{4.22}$$

$$S5 = S + C + \overline{Out_{CP}}\ \&\ (A + B + F + G) \tag{4.23}$$

$$MPPT\_ON = \overline{Out_{CP}\ \&\ (A + B + C + D + G)} \tag{4.24}$$

Another output is required to deactivate the FSM when the MPP is found. This output signal is indicated in the state diagram in green and FSM is active when it is high. The state machine is composed of 11 states. The states are coded based on one hot approach from start=00000000001 until J=10000000000. The State table is given in. Equations (4.9) to (4.18) are extracted from table and are describing equations of our MPPT FSM.

4.4.2 The circuit for implementing the finite state machine

The block diagram of the MPPT unit is shown in

Figure 4.6 (a). The FSM Core block is the circuit level realization of equations (4.9) to (4.24). This circuit is composed of 11 flip-flops and the necessary combinational circuit. The initialization signal is an active low signal that initiates the state of the machine to "Start" in the start-up as shown in Table 4.1. The initialization occurs whenever the voltage of stage 5 drops to lower than 350 mV which means either the load is too heavy or the TEG input voltage is too small. The circuit that generates this signal is explained in section 4.5.4. Activating or inactivating the MPPT circuit is fulfilled using a clock gating block which also helps to reduce the power consumption when the MPPT block is off. The block which is shown in

Figure 4.6 (b) generates the input clock signal if the enable signal is high. The enable signal is high if $MPPT_{ON}$ is high. After initialization, the state of the machine is Start, therefore $MPPT_{ON}$ is high. When $MPPT_{ON}$ is low, the system finishes and MPP is found. Output voltage drop after an MPP is found, triggers a new MPPT search since the $\overline{\mathrm{Out}_{\mathrm{Comp}}}$ signal becomes high. It is worthwhile to note that after each successful MPPT cycle, the state of the FSM becomes "Start", to be ready for another MPP tracking if the block becomes activated by the $\overline{\mathrm{Out}_{\mathrm{Comp}}}$.

4.4.3 Subthreshold FSM

In low speed digital circuits, proper functionality can be achieved at low power consumption, if the circuit operates in the subthreshold region. Subthreshold region offers ultra-low power consumption but reduced speed. MPPT for TE energy harvesting offers a good application for subthreshold circuits, since the temperature gradient transitions occur with a much larger time constant than a typical MOSFET switching in the circuit.

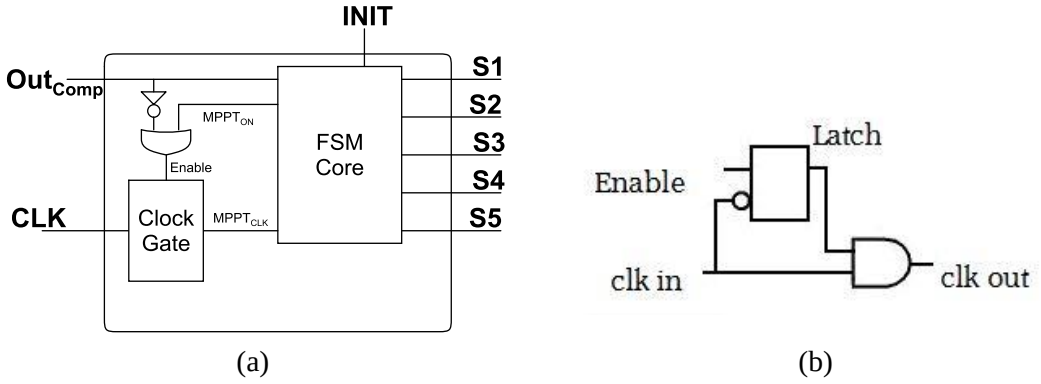


Figure 4.6. (a) Block diagram of the MPPT circuit (b) Clock gating block.

Typically it is tolerable for energy harvesting systems if the MPPT takes hundreds of milliseconds [66]. The convergence speed of the MPPT found in the literature is in the range of some hundreds of milliseconds to tens of seconds [70]. To further reduce the power consumption of the FSM unit, the FSM circuit discussed in 3.4.2 has been further modified to push it to operate in subthreshold region. Adding head and foot transistors that are active in subthreshold region is a well-known method to limit the current of the paths and push the circuit to the subthreshold region. By adding head and foot transistors, both static and dynamic power consumption will be decreased due to the decrease in current. The general block diagram of the implemented circuit is shown in Figure 4.7. The topology shown in Figure 4.7 is implemented for all flip-flop blocks and the combinational circuits.

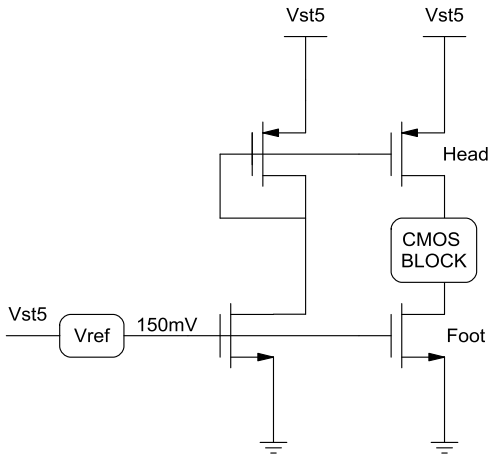


Figure 4.7. Pushing the CMOS block to operate in subthreshold region using Foot and Head MOSFETs.

4.5 The fully autonomous power management system

Figure 4.8 depicts the block diagram of the proposed power management system. The circuit is composed of the reconfigurable charge pump based DC-DC converter with LC-tank oscillator shown in Figure 4.2, the MPPT block, the comparator and the voltage regulator. V_{st5}, is used as the supply node to power all control circuitry since it provides sufficiently high voltage even when V_{TEG} is at the minimum. The MPPT block implements the MPPT algorithm which was discussed in detail in section 4.4. When the TEG output voltage reaches the minimum start-up voltage, the initialization circuit sets the output of the FSM to stage 5 for high voltage boost, and activates the MPPT block. Each MPPT block output is connected to the output select pin of multiplexers (MUX). The input of these multiplexers are output of stage 5, V_{st5}, or output of the op-amp, V_{reg}.

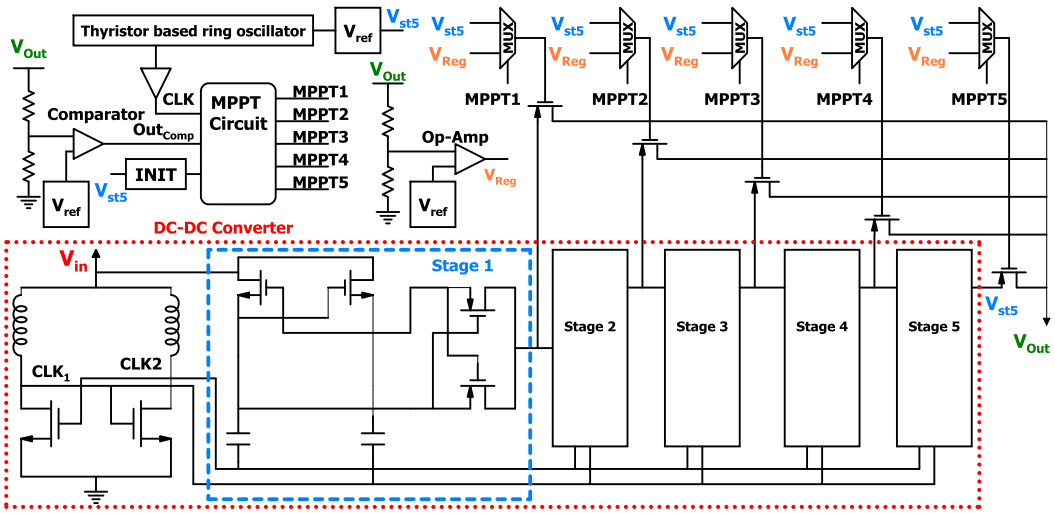


Figure 4.8. The schematic of the overall fully autonomous integrated power management system.

When the $MPPT_n$ signal is high V_{reg} becomes selected. In this case stage n will be open and the op-amp circuit together with the PMOS switches create a low dropout regulator that regulates output voltage to 1 V. If the MPPTn (n=2,3,4,5) signal is low, V_{st5} becomes selected that turns the PMOS off since the PMOS gate voltage will be higher than or equal to PMOS source voltage. Since stage one is not considered as mentioned in section 4.4.1, the system has only 4 MUXs.

4.5.1 Ultra-low power control circuitry

As discussed earlier in chapter 3, it is necessary to consider power consumption of the circuit in the design of power management circuits. Typically analog blocks are power hungry because of bias circuits. Therefore, minimum bias current is targeted in the design of Op-Amp and the Comparator block. This in turn reduces the gain and slew rate of these gates. The slew rate is compensated via buffer circuits, typically 2 minimum size back to back inverters. The power consumption of the digital blocks, FSM for instance, is not considerable. For most of the design units power consumption was reduced to sub-micro watt. A detailed comparison of this work with the state of the art in the literature is presented in chapter 5.

Another important consideration in this circuit is using a supply node with variable voltage, based on the voltage of V_{st5}. No voltage regulator is used to help minimize power consumption. As shown in Figure 4.8, V_{st5} is directly used as the supply node which adds to the complexity of the blocks as will be discussed in the following sections.

4.5.2 Ultra-low power voltage reference circuit

Voltage reference circuit can be a large block consisting of many MOSFETs, and bias circuitry. Bandgap voltage references are commonly used in integrated circuits, which are the combination of circuits with current proportional to absolute temperature (PTAT) and current complementary to absolute temperature (CTAT). A constant voltage with respect to temperature and supply voltage variations can be achieved by combining PTAT, in which the current increases with increase in temperature, and CTAT, in which the current decreases with increase in temperature, and then feeding the combined current to a constant load. There are many voltage reference circuits introduced in the literature which are typically composed of high number of devices biased in the active region and thus are power hungry [80]–[85]. In order to reduce the power consumption, some voltage reference circuits are recently proposed that act in the subthreshold region [86]–[96]. The power consumption of these subthreshold voltage references are less than some tens of nW. The main drawback of these circuits is their very low output. A subthreshold voltage reference circuit with minimum number of elements is proposed in [97] which is composed of only 2 NFET with different threshold voltages (2T voltage reference). The proposed circuit and the corresponding MOSFET sizes in different CMOS technologies are shown in Figure 4.9. The operation of this circuit is based on the threshold voltage difference of the two NFETs. This

circuit is chosen for its ultra-low power consumption, reliability and robustness toward a high range of power supply variation with as low as 0.5 V. A thick oxide NFET is proposed to be used in the paper. However, in the standard CMOS UMC 180 nm technology we have used low Vt NMOS instead of thick oxide NMOS without changing the use of native NMOS to keep using standard components and reduce the cost. The output voltage reference of the proposed circuit reaches 330 mV. However, higher voltage levels is required for the comparator in order to decrease the effect of process variations of the big poly resistors in the voltage divider. Therefore, the circuit is modified by adding more stages as cascoded to M2 transistor. By increasing the number of cascoded transistors the output voltage level increases. By adding 5 identical transistors as M2 the output voltage reaches around 700 mV. Supply voltage of this voltage reference circuit is V_{st5} which is necessary to reach 0.75 V at a minimum. This voltage is easily achievable by a 170 mV input even for a heavy load scenario.

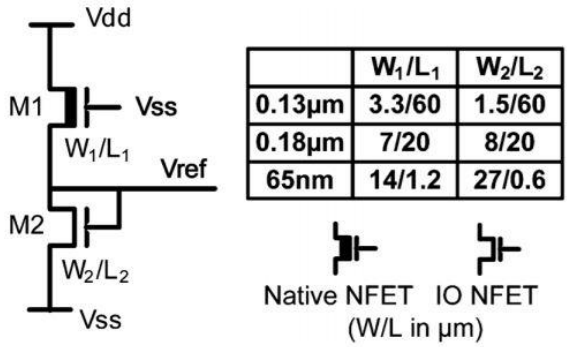


Figure 4.9. Ultra-low power voltage reference proposed in [89].

4.5.3 Ultra-low power low-frequency clock generator circuit

Use of ring oscillator for FSM clock generation has some drawbacks. 1) The oscillation signal is a sinusoid signal with ultra-low drive current because of biasing MOSFETs in the subthreshold region. Therefore, a large buffer is required to create a square wave signal with acceptable driving current. Large buffers increase the dynamic power loss. 2) The presence of glitches that can be produced in the output of the buffer. Since our circuit is implementing an FSM and more than hundred µs is required between each stage change for to reach steady state, these glitches can adversely affect the functionality of the FSM. On the other hand, thyristor-based ring oscillators can provide ultra-low frequency clock signal. In addition, thyristor based ring oscillators are very suitable for our application due to their ultra-low power consumption and the generated square wave clock signal. [98] Figure 4.10 demonstrates a conventional CMOS thyristor. The thyristor will be turned off if Ptrig is

precharged to Vdd and Ntrig is predischarged to ground. Ptrig or Ntrig can both be triggering nodes. For simplicity we assume Ptrig to be the triggering node. Until Ptrig is discharged down to Vdd - Vt, M1 conducts less than the subthreshold current. Once M1 is turned on, Ntrig voltage will start growing and Ptrig voltage will start decreasing even more. This strong positive feedback mechanism in this turn-on operation provides a very quick flipping of the state. Due to this very quick flip, the power consumption will be considerably reduced due to reduction in both dynamic and static power loss since there is no current flow directly from Vdd to ground. The quick flop also results in a square wave pulse with very small rise and fall time. A delay element can be built with this CMOS thyristor and a control current source for triggering the thyristor. Figure 4.11 (a) depicts the typical delay element created by the CMOS thyristor gate shown in Figure 4.9. Figure 4.11 (b) illustrates a block diagram of a three stage thyristor based ring oscillator. In chapter 5, simulation based verification is provided for the oscillator. The circuit topology shown in Figure 4.11 is utilized as the clock generator for the MPPT gate. All NMOS and PMOS transistors used in this circuit are minimum size native elements. The capacitance used are MIMCAP type with 15 μm × 15 μm with capacity of 229.5 fF. The output frequency of the oscillator is 5 kHz. This means every MPPT stage change will take place in approximately 200 μs which is sufficient for the signals to stabilize. The high dependency of the oscillation frequency to Vdd is a drawback for this oscillator. To overcome this problem, we have proposed an innovative solution. The proposed circuit in which the 2T voltage reference is used as supply voltage for the thyristor based oscillator is shown in Figure 4.12. The drive current of the 2T voltage reference circuit is some pA, because of operating in the subthreshold region. The thyristor based oscillator sinks some tens of pA in the transition. Therefore a capacitor is used to store the energy during the two pulses.

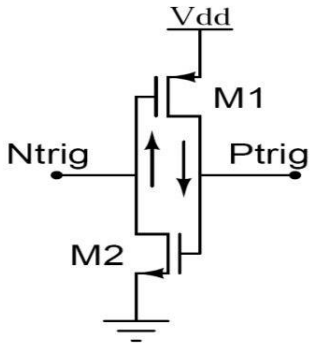
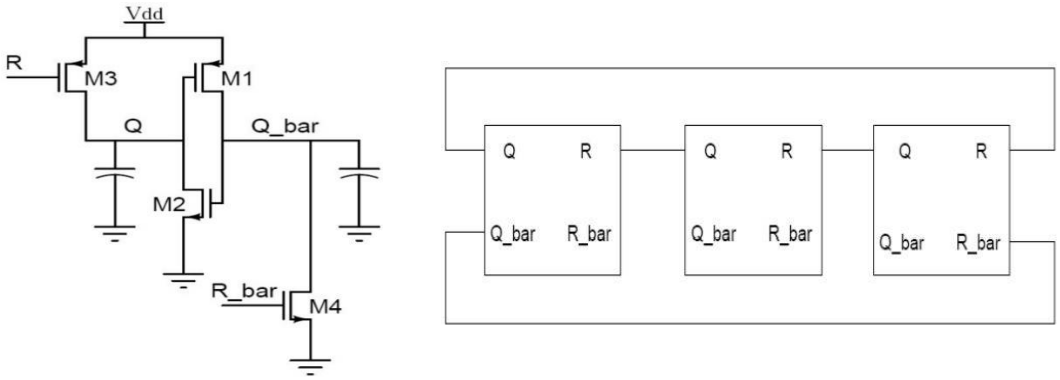


Figure 4.10. A conventional CMOS Thyristor block.



(a) (b)

Figure 4.11. (a) A typical delay element created by the CMOS thyristor gate, (b) block diagram of a three stage thyristor based ring oscillator [99].

The capacitor is a MIMCAP of size 70 µm × 70 µm with capacity of 4.9 pF. The voltage swing of the tyristor based oscillator therefore will be equal to the reference voltage (700 mV). To convert this voltage to the Vst5 level a "level shifter" circuit is utilized. The level shifter supply voltage is Vst5 . Level shifter topology is shown in Figure 4.13. IN shown in this figure is the input pulse with lower amplitude. When IN is low (Vss), MN1 is off and MN2 is on, since MN2 will see the inverted IN (VddL). Since MN2 is ON, voltage of the OUT will be low (Vss). Therefore MP1 will be ON, making the voltage of N1 high (VddH) and MP2 will be OFF. On the other hand, when IN is high (VddL) MN1 will be ON and MN2 will be OFF. Since MN1 is ON, voltage of N1 Node will be low (Vss) and MP2 will be ON making the Voltage of OUT high (VddH). In the following level shifter circuit all MOSFETs are minimum size.

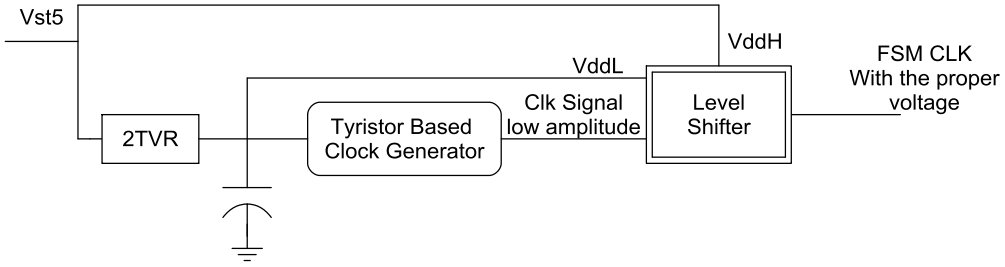


Figure 4.12. The proposed circuit topology for ultra-low power FSM clock generator.

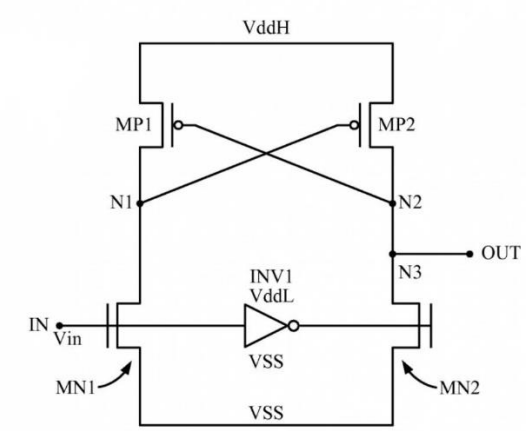


Figure 4.13. Voltage level shifter.

4.5.4 Ultra-low power initialization circuit

One of the important challenges in the design of energy harvesting interface circuits is the start-up condition. Control circuitry will not be activated until their supply voltage reaches to a specific level. To overcome this problem in our circuit topology we need the FSM to be initialized at 5 stage mode to get a high voltage in the beginning of the conversion. Considering this, the FSM initialization signal should be an active low signal, which sets the output of the FSM to stage “start” with output at stage 5. To this end flip-flops of two different types of SET and RESET are used. The necessary low signal that initiates the FSM is generated using the circuit topology depicted in Figure 4.14.

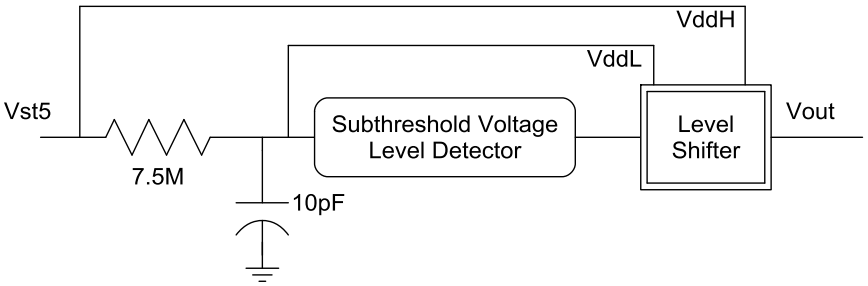
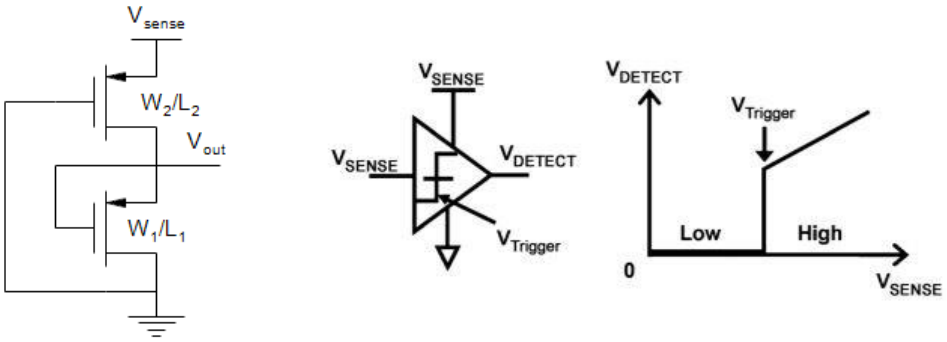


Figure 4.14. Initialization circuit that generates the required pulse for initializing the FSM.



(a) (b)

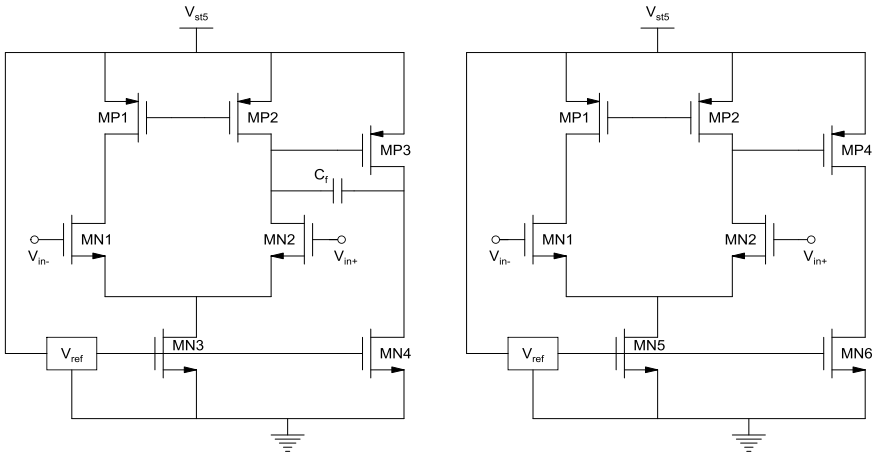
Figure 4.15. (a) The voltage level detector circuit, (b) Input-output characteristic [100].

$$V_{Trigger} = \frac{mkT}{q} ln\left(\frac{W_1}{W_2} \times \frac{L_2}{L_1}\right) \tag{4.25}$$

In the start-up when the voltage of Vst5 rises, the RC circuit starts charging the capacitor. The subthreshold voltage detector circuit [100] which is shown in Figure 4.15, triggers when the voltage reaches $V_{Trigger}$. Due to the high time constant of the RC circuit, the low signal lasts for tens of microseconds which is enough to initialize the FSM circuit. Once the level detector is triggered, the output of the circuit will be high. The use of the level shifter block guarantees the proper voltage level equal to Vst5 for the output of the initialization circuit. The trigger voltage is given in (4.25). In this circuit if V_{sense} is less than $V_{Trigger}$ then V_{out} is low, otherwise it will be equal to V_{sense}. In this circuit the trigger voltage is designed to be 350 mV, W2/L2 = 240 nm/10 µm, and W1/L1 = 75 µm/180 nm.

4.5.5 Ultra-low power op-amp and the comparator circuits

The Op-Amp circuit is shown in Figure 4.16. The bias current is considerably reduced by decreasing the bias voltage to 250 mV to minimize the power consumption. The op-amp circuit is composed of a differential amplifier and another amplifier stage with a feedback capacitor. The comparator circuit is shown in Fig 3.16 and is the same op-amp circuit except for the feedback capacitor. Elimination of the feedback capacitor enables output's rapid change which is required in the comparator circuits to quickly differentiate the compared signal level as higher or lower than the reference voltage.



(a) (b)

Figure 4.16. (a) Op-Amp circuit (b) Comparator circuit

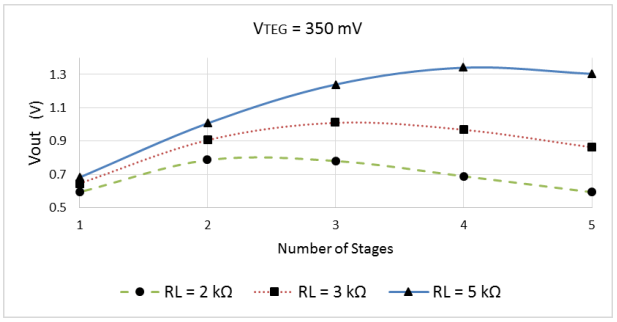
Chapter 5 focuses of verification of the circuit blocks that were present in this chapter by simulating all the circuits in Cadence CAD environment. All the blocks are implemented in UMC 180 nm technology.

CHAPTER 5

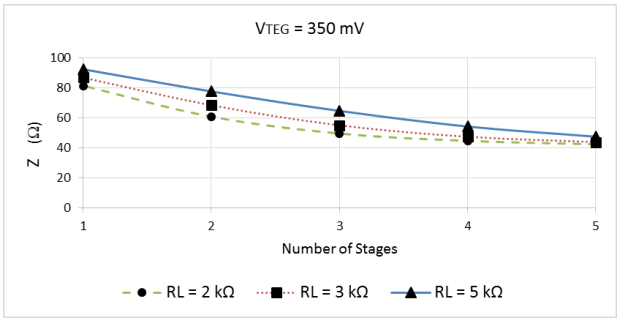
5 Circuit Verification

5.1 Simulation results for the optimized charge pump based DC-DC converter

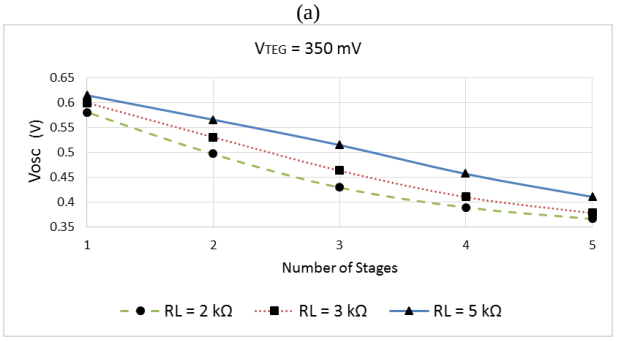
The charge pump based DC-DC converter has been simulated for different varying input voltages and output loads. The minimum start-up voltage for the DC-DC converter is 150 mV. The LC-tank starts oscillating for the input voltages as low as 130 mV, however, it is not enough to reach 1 V at the output. The upper limit for the input voltage is imposed by the CMOS technology. In CMOS 180 nm technology, maximum tolerable voltage limit is around 3.3 V. In IoT applications, the load, which is an embedded system with sensing, signal processing and wireless communication capability, can be highly varying depending on the mode of operation of the smart node. The highest load corresponds to wireless data transmission. Typically one or more mWs of power is required for short range wireless data transmission. For sensing and data processing, some hundreds of μWs would be sufficient with an ultra-low power signal processing and sensing units [101]. Figure 5.1 illustrates the behavior of our charge pump based DC-DC converter based on the post layout simulation results. The R_{TEG} value can vary for different products. 40 Ω is a typical value for tiny TEGs that can harvest around 350 mV from body heat and is used in the simulations shown in Figure 5.1 [102]. Figure 5.1(a) shows that the output voltage will not linearly increase with the increase in the number of stages due to the loading effect on the LC-tank as discussed in Chapter 4. Instead there is one stage that provides maximum output voltage. Based on the equation (2.16) and the discussion in chapter 4, the input resistance is expected to decrease as the number of stages increase. This is depicted in Figure 5.1(b). As a result, the input voltage also declines as the number of stages increases, which is illustrated in Figure 5.1(c). Oscillation amplitude is also demonstrated in Figure 5.1(d). As discussed in Chapter 4, increase in the number of stages raises the load on LC-tank oscillator, reducing its voltage swing. The two above mentioned effects prevent further boosting of the output voltage by increasing the number of stages. In other words, for a given V_{TEG} and R_L, there is only one stage that provides maximum output voltage. Figure 5.1(e) illustrates the input power of the interface circuit. Based on equation (3.8) the input power has a maximum value, which is only dependent on the V_{TEG} and R_{TEG}, and can be achieved when the input resistance of the interface circuit is equal to R_{TEG}. Based on the input resistance values shown in Figure 5.1(b), these values converge to $R_{TEG} = 40\Omega$ with 5-stage charge pump. Therefore, the input power reaches the maximum achievable input power with 5 stages. On the other hand, the output power is illustrated in Figure 5.1(f) and shows maximum power point is achieved



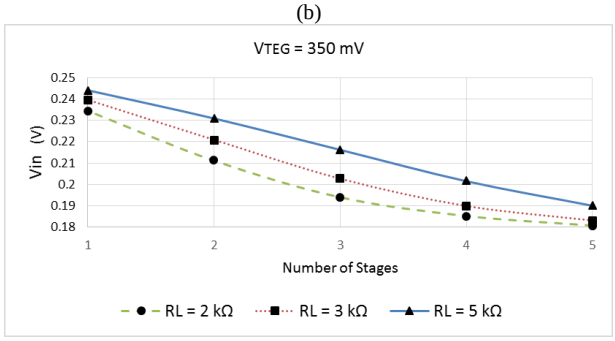
(a)



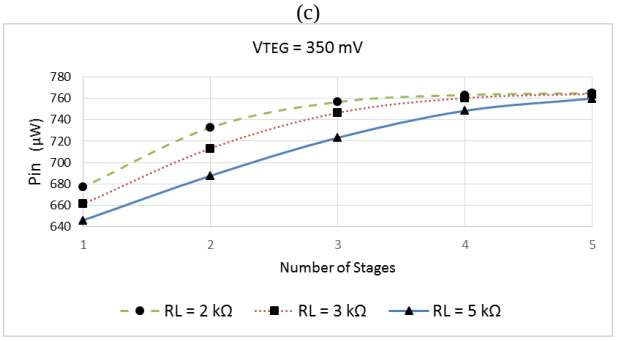
(b)



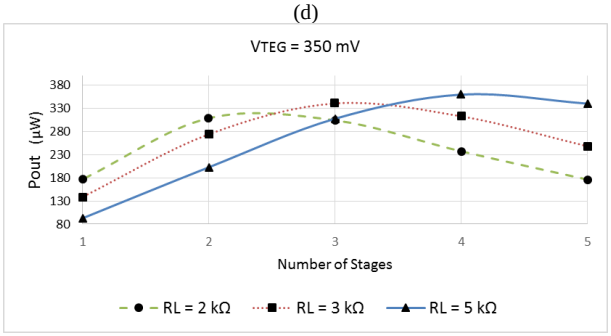
(c)



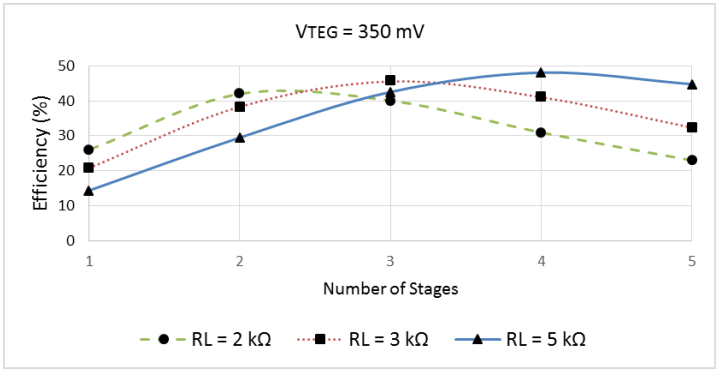
(d)



(e)



(f)



(g)

Figure 5.1. Simulation results of the behavior of the DC-DC converter for varying load and fixed Source voltage. (a) For each load there is one stage which provides maximum output voltage. (b) Input impedance of the system decreases as number of stages increases. (c) As number of stages increases charge pump loading reduces the oscillation amplitude. (d) For a fixed VTEG, Vin has inverse relation with number of stages. (e) Input power is maximum in

stage 5 since Z=RTEG (f) output power is maximum in different stages due to the variable efficiency of the charge pump and the output voltage.

Maximum output power point is what we are tracking. Output power is maximized with 2 stages, 3 stages and 4 stage for 2kΩ, with different number of stages for different loads. The efficiency curve is depicted in Figure 5.1(g), which shows the maximum efficiency is achieved at the same stage that maximum output is achieved. This is the end-to-end efficiency which was defined in equation (1.1) and differs from the maximum power point efficiency defined in equation (3.8). 3kΩ and 5kΩ load. (g) The stage that maximizes the output power also maximizes the efficiency. Furthermore, Figure 5.1 demonstrates the effect of increasing the load on the behavior of the charge pump. Based on the model presented in Figure 3.12 and equations (2.9) and (2.10), increase in RL increases the impedance of the nth branch, which leads to the overall increase in the input impedance. In Figure 5.1(b) the input resistance increases by increasing RL. The same effect explains the Vin increase with increase in RL. On the other hand, increase in impedance decreases G_0 in equation (3.4) and leads to higher gain and higher oscillation. This is reflected in Figure 5.1(c) where oscillation amplitude increases with increase in the load for a fixed number of stages. The increase in the oscillation amplitude significantly affects Vout. Therefore in Figure 5.1(a), for a fixed number of stages higher output voltage is obtained.

Figure 5.1 indirectly verifies the MPPT algorithm proposed theoretically in Chapter 4. Figure 5.1(f) clearly shows that 3 stage charge-pump results in the maximum power point for the load of 3 kΩ. It is worth emphasizing that output higher than 1 V will be regulated.

Figure 5.2 depicts the simulation results with a fixed load and varying V_{TEG}. The trend of the curves are similar to the curves obtained in Figure 5.1 with more linear nature. Figure 5.2 (a) shows that by increasing the V_{TEG}, V_{out} increases for a fixed number of stages and a fixed load. This is similar to increasing R_L as demonstrated in Figure 5.1 (a). The input resistance has inverse relation with V_{TEG}. This is expected due to the variable R_{on} of the MOSFETs of the converter. Increase in V_{TEG} decreases the R_{on} of the MOSFETs therefore decreasing R_{Pn} and R_{Nn} in equations (2.6) to (2.10), thus decreasing the overall input resistance as illustrated in Figure 5.2(b). With decrease in the input resistance, V_{in} also decreases as shown in Figure 5.2(d). In addition, the oscillation amplitude is directly related to the input voltage from equation (3.4) as depicted in Figure 5.2(c). Since the oscillation amplitude directly affects the output voltage, in Figure 5.2(a), with increase in V_{TEG}, V_{out} increases for a fixed number of stages. The input power also has direct relation with the input voltage, which

explains the input power increase with increasing the V_{TEG} demonstrated in Figure 5.2(e). The output power increasing trend is also a result of output voltage increase. Similar to the increase in R_L effect for any given V_{TEG} with a fixed R_L there is a stage that generates maximum output voltage that leads to maximum output power and maximum efficiency as depicted in Figure 5.2(f) and Figure 5.2(g).

5.2 Simulation Results for the circuit blocks

5.2.1 FSM clock generator

As described in section 4.5.3 tyristor based oscillator is used to generate the necessary clock for the FSM due to its ultra-low power consumption, low frequency and rectangular pulse waveform. The frequency of the pulse is highly variable with the supply voltage similar to all VCOs. In addition, the input current of the oscillator is in the order of μA at flipping instance for a few ns. Figure 5.3 demonstrates the simulation results for the thyristor based oscillator circuit proposed for the FSM Clock. The output current of the voltage reference circuit is only some nAs, since the circuit is operating in subthreshold region. The circuit sinks high current only when flipping, and the oscillation frequency is low. Therefore, a capacitor is used that charges up to the V_{ref} by the reference voltage circuit. In Figure 5.3, V_1 is the voltage of the capacitor. The input current curve of the tyristor based oscillator is shown as I_{Tyr}. The oscillation amplitude then is adjusted to match Vst5 by means of a level shifter circuit described in section 4.5.3.

5.2.2 The ultra-low power circuit that generates the initialization signal

In order to initialize our FSM circuit in the beginning of the MPPT tracking, we need a low level signal that lasts for at least 30 us for a reliable initialization of the flip-flops. To do this, a circuit is proposed that takes advantage of an RC circuit's time constant and a level detector circuit as discussed in detail in section 4.5.4. Figure 5.4(a) shows the circuit and Figure 5.4(b) illustrates the corresponding signals. The level shifter is triggered when V_1

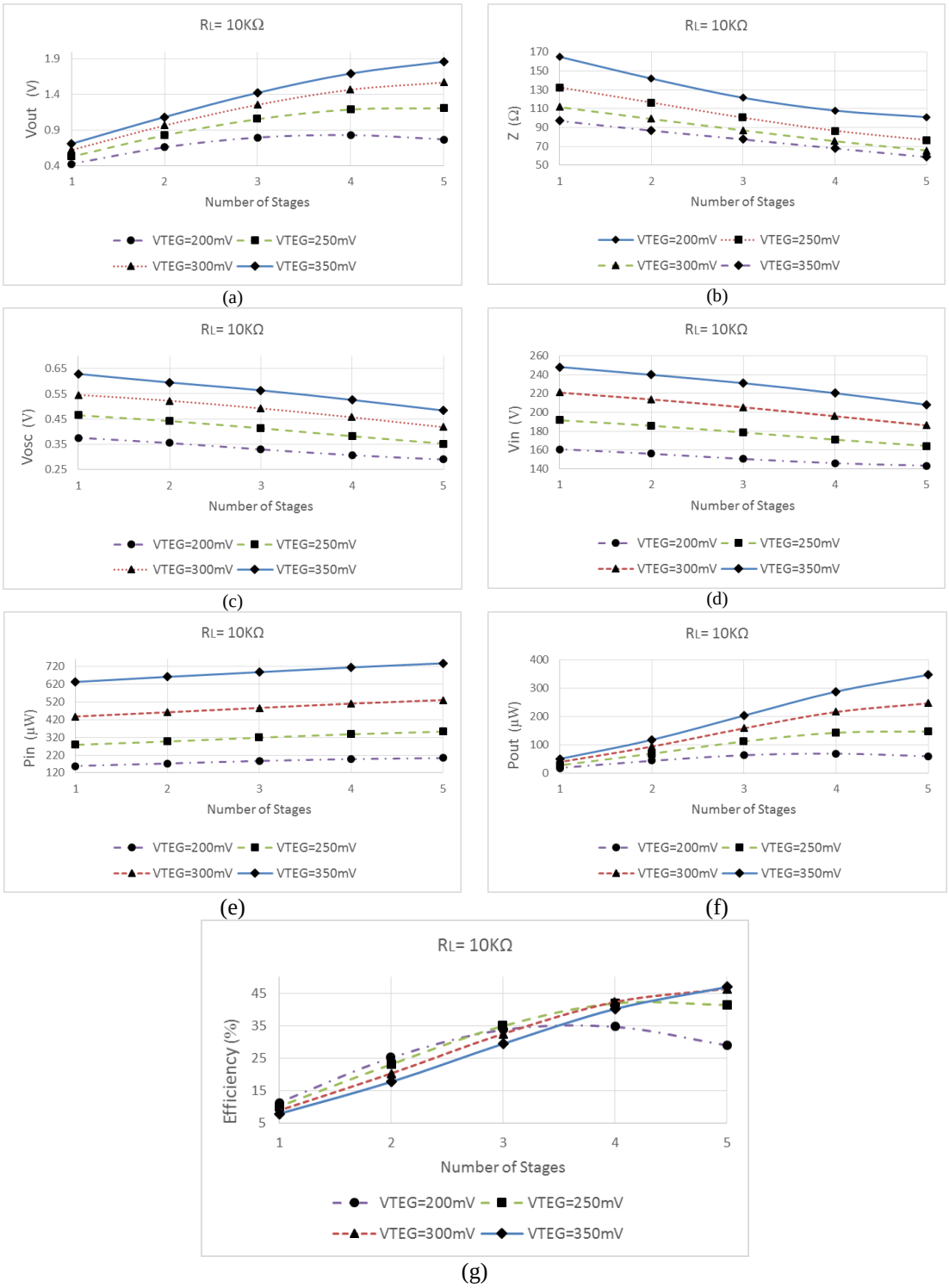
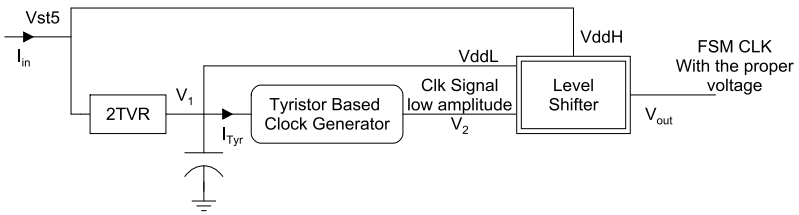


Figure 5.2. Simulation results for the proposed power management system behavior with a fixed load and varying V_{TEG}. (a) For different V_{TEG} there is one stage which provides maximum output voltage. (b) Input impedance of the system decreases as the number of stages increases.

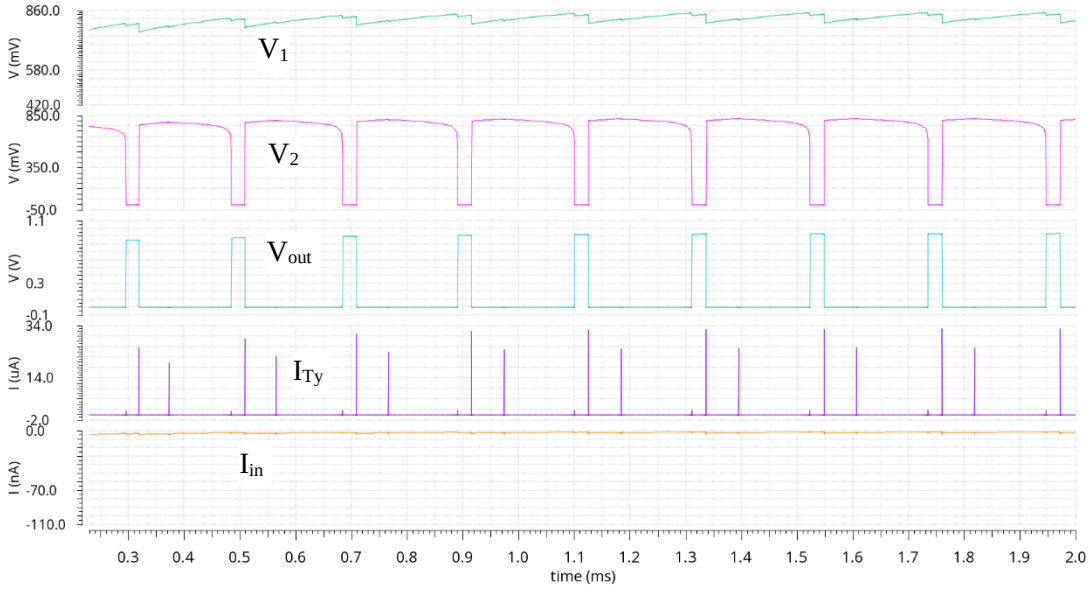
reaches 350 mV. The output of the level detector is fed to a voltage level shifter to adjust the amplitude to Vst5.

5.3 Simulation results for the fully autonomous system with MPPT

By applying the proposed MPPT algorithm to the scenario investigated in Figure 5.1, the search for maximum power point will start with 5 stages. Figure 5.5 demonstrates the simulation results for the full autonomous system analysis with the MPPT block with the same scenario as in Figure 4.1. In (a) starting from 5 stages, since the output voltage with a 3 kΩ load is less than 1 V, the number of stages will be decremented. 1 V target will not be reached with 4 stages, and hence the number of stages will again be decremented to 3 when the 1 V output can be fulfilled. At this stage MPPT is still active and is looking for the minimum number of stages that can create 1 V output to increase efficiency. Therefore, the number of stages will again be decremented to 2. However, the 1 V target voltage cannot be achieved with 2 stages. Thus, the algorithm increments the number of stages to 3. The MPPT still stays active to sense any change in the V_{TEG} level or load. At this state the target voltage is still achieved, so the MPPT is deactivated and the number of stages is locked on 3 which also corresponds to the maximum efficiency point. In (b), the load is increased to 5 kΩ. Stages 3 to 5 will provide target 1 V. At the beginning the algorithm will start with 5 stages. Even though the target voltage is achieved, the number of stages will be decremented searching for the maximum efficiency.

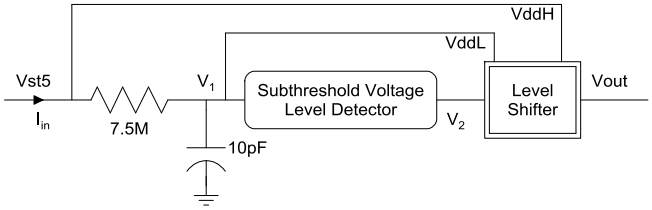


(a)

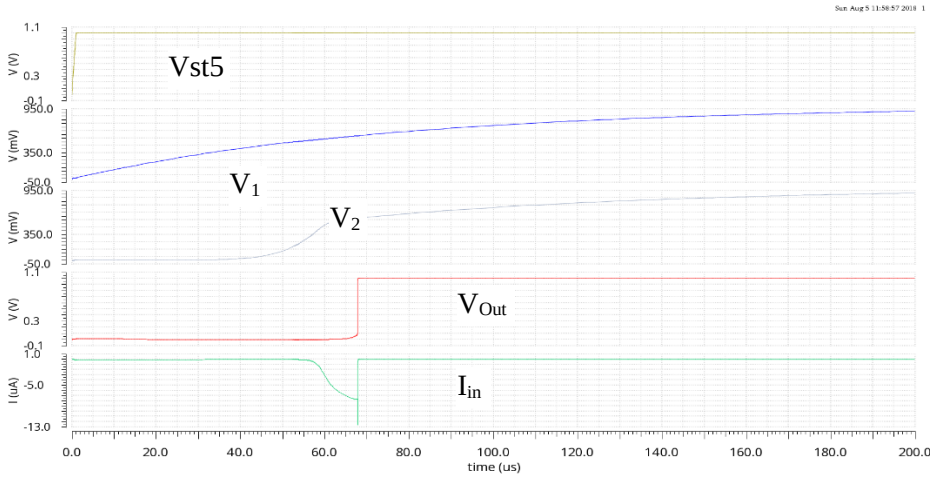


(b)

Figure 5.3. (a) The circuit for the FSM clock generator using a voltage reference block (copied from Figure 4.12). (b) The circuit's corresponding waveforms.



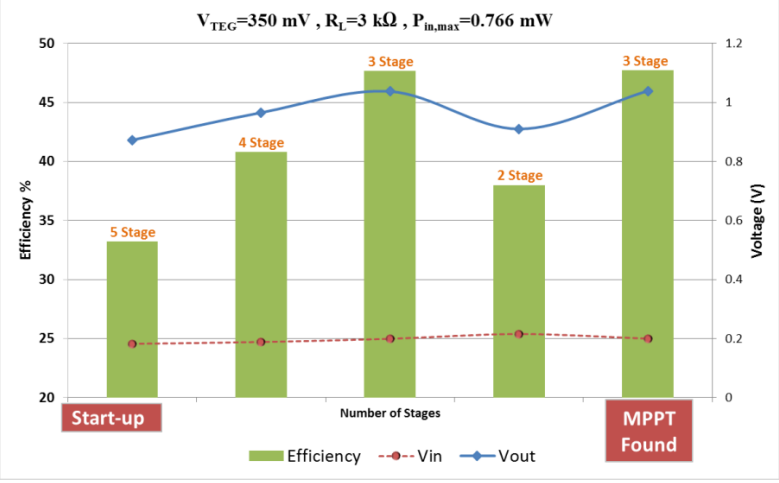
(a)



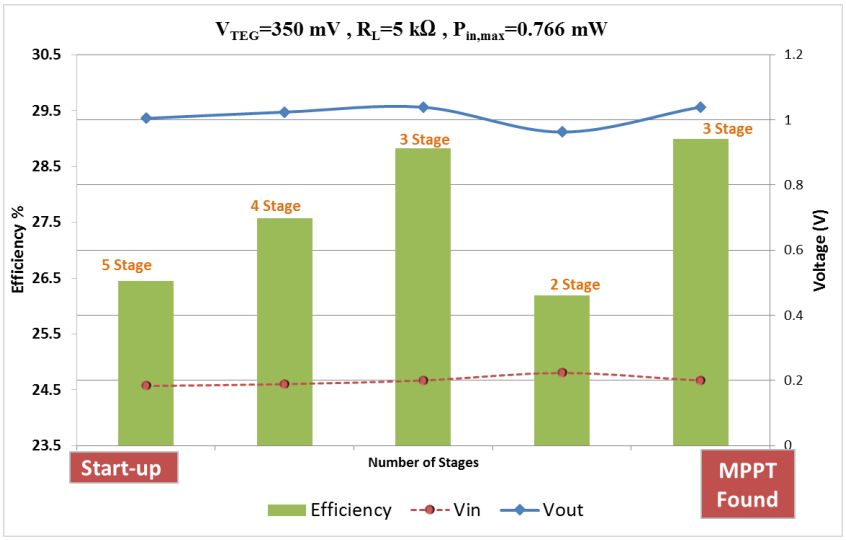
(b)

Figure 5.4. (a) The proposed circuit for the FSM initialization signal (copied from Figure 4.14), and (b) the circuit's corresponding waveforms.

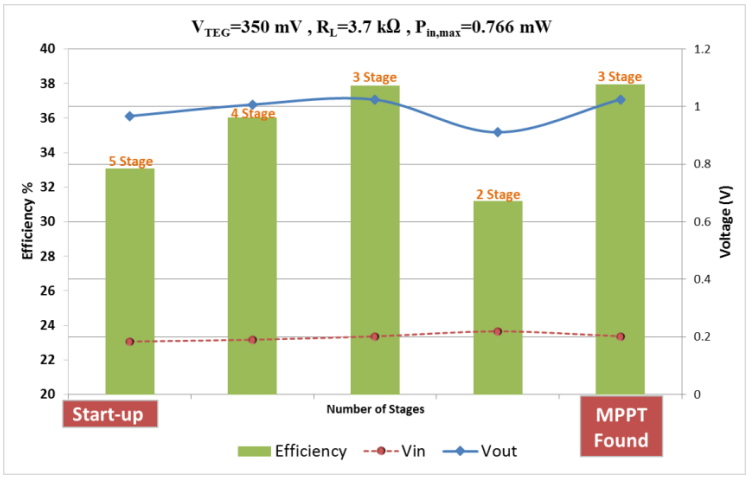
With all stages except 2, the 1 V target voltage will be achieved. Therefore, the MPPT will increment the number of stages and will be locked on 3. Hence, maximum power point with minimum loss which corresponds to maximum efficiency will be achieved with the minimum number of stages, which is 3. Another simulation is shown in (c) where R_L is 3.7 kΩ and stages 3 and 4 provide target 1 V. In the beginning the algorithm starts with 5 stages. Since the target voltage will not be achieved, the number of stages will be decremented searching for the stage that fulfills the target voltage. With stage 4 the target voltage is reached; therefore the number of stages is decremented to 3 searching for the maximum efficiency. With 3 stages 1 V target voltage will again be achieved. Therefore, the MPPT will decrement the number of stages to 2. With 2 stages the output voltage is less than 1 V, so the number of stages will be incremented and MPPT will be locked on 3. Therefore, maximum power point with minimum loss which corresponds to maximum efficiency will be achieved with minimum number of stages, which is 3. In (d) V_{TEG} is decreased to 240 mV with 10 kΩ load in analogy to the scenario in Figure 4.2. Number of stages is decremented in the beginning since the target voltage cannot be achieved. 3 stages cannot provide 1 V target voltage; therefore the algorithm is locked on stage 4 for the maximum efficiency. In (e) a scenario is simulated where the input voltage is high enough that all stages provide 1 V target voltage. Therefore, the number of stages are decremented starting from 5 stages in the beginning to search the number of stages with maximum efficiency. When the number of stages reaches 2, it cannot be decremented anymore. Therefore, the number of stages is locked on 2 that leads to maximum efficiency. It is worth to mention that there is less than 10% offset in the output voltage of the regulator in the following scenarios due to decreased bias current of the op-amp to meet the ultra-low power criteria that has led to reduced gain.



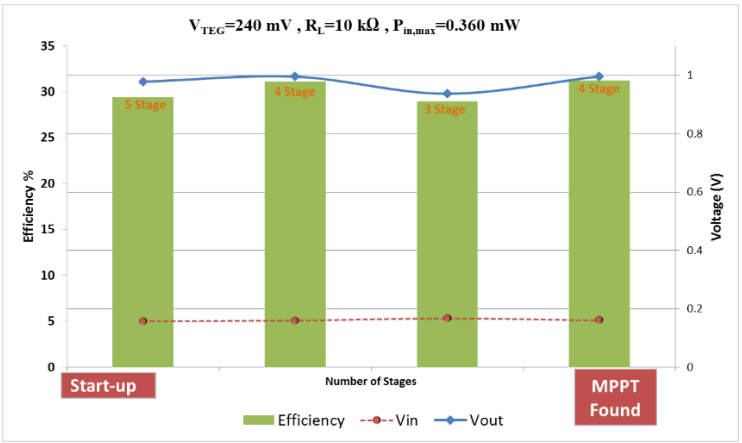
(a)


V_{TEG}=350 mV , R_L=5 kΩ , $P_{in,max}$=0.766 mW
Efficiency %
Voltage (V)
Number of Stages
5 Stage
4 Stage
3 Stage
2 Stage
3 Stage
Start-up
MPPT Found
Efficiency
Vin
Vout

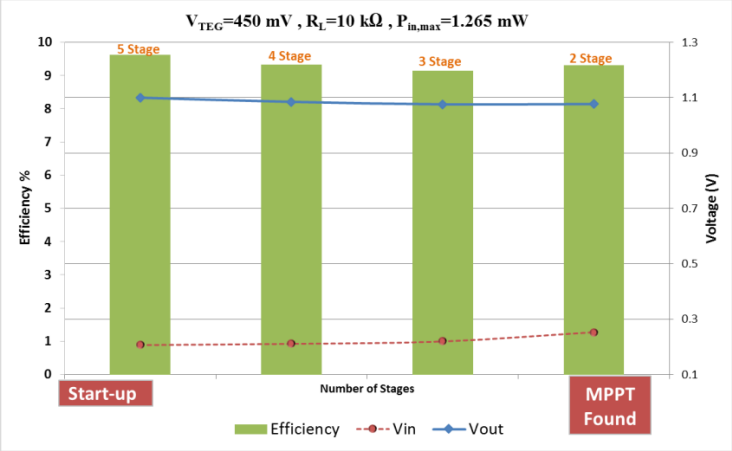
(b)


V_{TEG}=350 mV , R_L=3.7 kΩ , $P_{in,max}$=0.766 mW
Efficiency %
Voltage (V)
Number of Stages
5 Stage
4 Stage
3 Stage
2 Stage
3 Stage
Start-up
MPPT Found
Efficiency
Vin
Vout

(c)


V_{TEG}=240 mV , R_L=10 kΩ , $P_{in,max}$=0.360 mW
Efficiency %
Voltage (V)
Number of Stages
5 Stage
4 Stage
3 Stage
4 Stage
Start-up
MPPT Found
Efficiency
Vin
Vout

(d)



(e)

Figure 5.5. Simulation results for the fully autonomous system with (a) V_{TEG}=350 mV and R_L = 3 kΩ (b) V_{TEG}=350 mV and R_L = 5 kΩ (c) V_{TEG}=350 mV and R_L = 3.7 kΩ (d) V_{TEG}=240 mV and R_L = 10 kΩ (e) V_{TEG}=450 mV and R_L = 10 kΩ.

Since the op-amps drive large PMOS switches, gain is important, but the offset is tolerable in order to achieve low power. Even though the op-amp bias current is limited, the largest share of the power consumption is dedicated to the LDO circuit as shown in Figure 5.6.

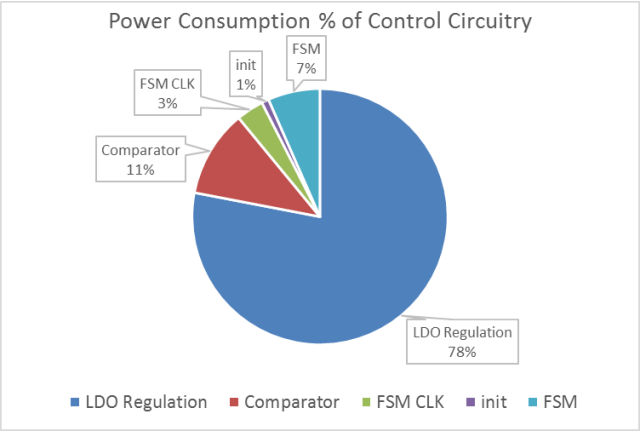


Figure 5.6: The histogram of the power consumption of different blocks of the fully autonomous system.

Figure 5.6 shows the percentage of the power consumption of the control circuitry. The most power consuming block is the low drop-out regulator. Since the output of the Op-Amp should turn large PMOS switches ON and OFF, a high gain is necessary to drive these switches. Therefore, the bias current of the Op-Amp has to be high. It is approximately 8

times higher than the comparator. The overall power consumption of the control circuitry is approximately 3% of the input power.

CHAPTER 6

6 Design validation

6.1 Introduction

This chapter presents the first test chip layout and validation of the fully integrated DC-DC converter with proposed MPPT capability. The validation is performed on the optimized layout for the DC-DC converter with a configurable charge pump to select the number of stages. Fully automated features such as voltage regulation and MPPT are implemented using external components. The pre-layout simulations, post-layout simulations, and experimental results for the fabricated test chip are presented with a comparative analysis. 180 nm standard CMOS technology is used in cadence environment for post-layout simulations including C-parasitic, RLC-parasitic extracted simulations.

6.2 Test chip design and layout

An overview of the circuit interface is illustrated in Figure 6.1. Large PMOS size has been used for stage switching to minimize voltage drop. The voltage at the end of each stage is high unlike the input voltage with ultra-low voltage range. PMOS is known to be suitable to pass high voltage levels without Vt drop. There is no internal capacitance at the output node to decreases the chip area. Instead loads like sensors or MCUs in wearable or IoT applications typically come with their inherent capacitance of some nF.

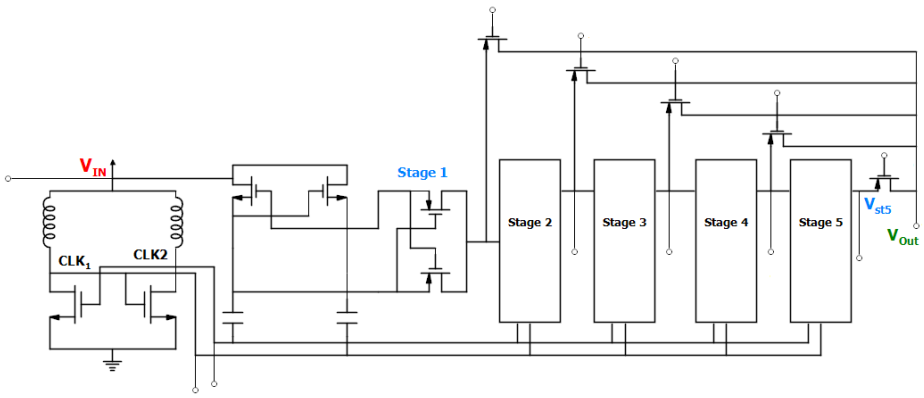


Figure 6.1. Block diagram of the fabricated test chip.

The full system layout is depicted in Figure 6.2, including PAD connections. (A) refers to the reconfigurable five stage charge pump with the corresponding capacitors. (B) is the LC-tank cross coupled NMOS pair for the oscillator switching mechanism. (L)s represent the oscillator inductors which occupy 0.6 mm^2 of the layout area. All the capacitors and

inductors are shielded with the ground connected wire line to prevent the magnetic and capacitive coupling effects.

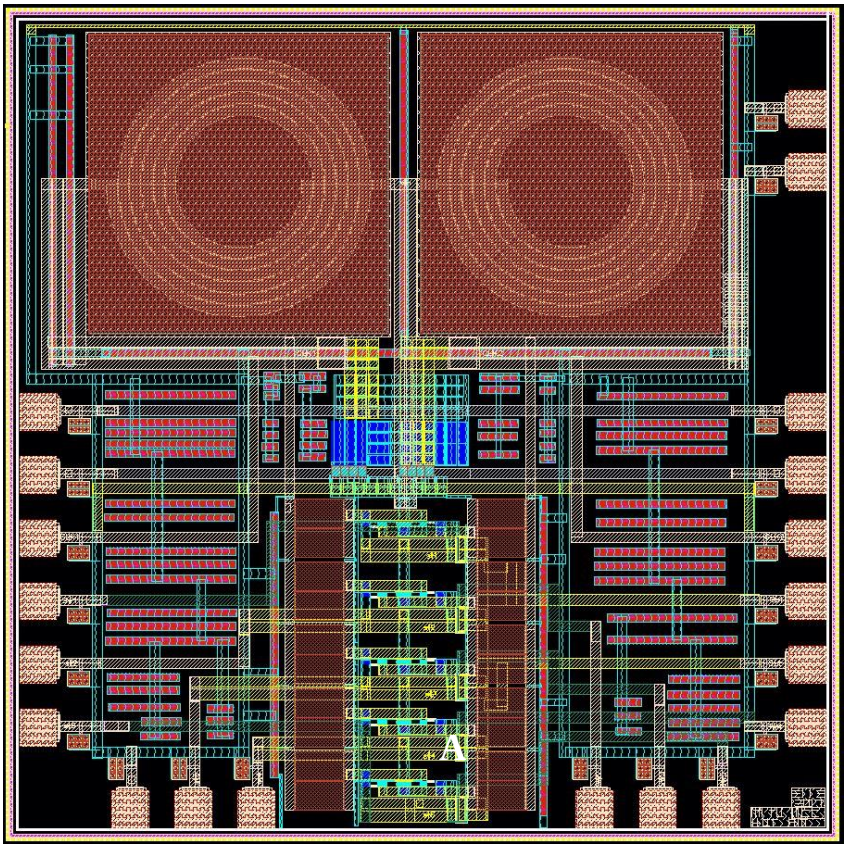


Figure 6.2. Chip layout photo with PAD connections.

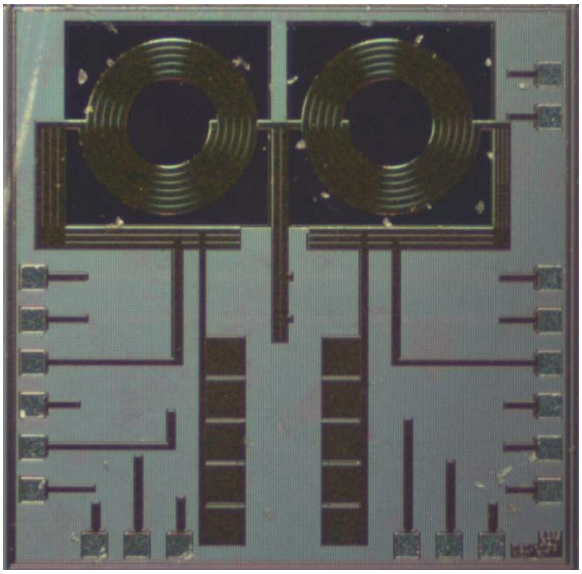


Figure 6.3. Die micrograph.

The system consists of 20 pins including 3 ground connecting pins, 4 input pins, 2 output pins, and corresponding switch pins for selecting between stages and the pins for the output voltage of each stage. The die micrograph of the fabricated chip is illustrated in Figure 6.1. The design parameters of the implemented circuit components are depicted in Table 6.1.

Table 6.1. Design parameters of the full system.

Component	parameters	UMC_18_CMOS cell name
LC-tank NMOS	W/L = 380 µm/240 nm Multiplier[1] = 4 Number of Fingers = 20	N_LV_18_MM
LC-tank inductors	Inductance = 14 nH Width = 20 µm Width = 5.5 Diameter = 238	L_SLCR20K_RF
Charge pump NMOS	W/L = 190 µm/240 nm Multiplier = 1 Number of Fingers = 10	N_LV_18_MM
Charge pump PMOS	W/L = 150 µm/240 nm Multiplier = 1 Number of Fingers = 10	P_LV_18_MM
Charge pump capacitors	C = 10 pF Number of Fingers = 10 Width= 55 µm Length= 90.51 µm	MIMCAPS_MM
Output switch- PMOS	W/L = 225 µm/240 nm Multiplier = 1 Number of Fingers = 5	P_LV_18_MM

[1] Multiplier in the layout is technique that allows repeating the same finger pattern for more efficient use of layout

The design layout effective area is 1525 µm × 1525 µm including PAD connections. The LC-tank based oscillator occupied 1200 µm × 574 µm of area while 608 µm × 472 µm is for the reconfigurable charge pump. The design layout has been implement in QFN 48 package for the performance characterization in laboratory environment. The bonding diagram and

pin description of fabricated IC is illustrated in Figure 6.4 and Table 6.2, for design validation.

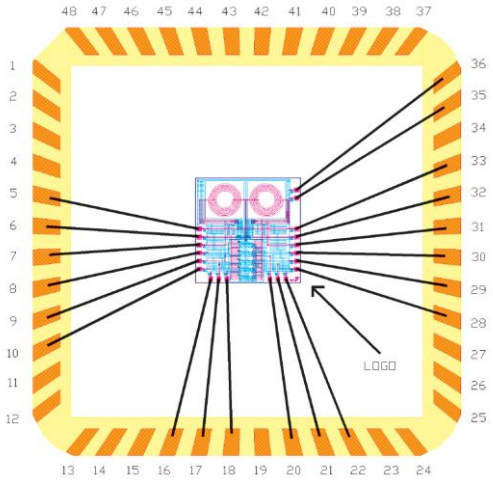


Figure 6.4. The bonding diagram of the fabricated IC.

Table 6.2. Pin description of the fabricated IC.

Pin name	Description	Pin number
Vin	Input connecting to TEG	5
Vin	Input connecting to TEG	6
CLK1	Oscillator Output 1 (Can be used for ex Inductor)	7
SW1	Gate of PMOS Switch stage 1	8
St2	Output Voltage of Stage 2	9
St5	Output Voltage of Stage 5	10
GND	Ground	16
St3	Output Voltage of Stage 3	17
St4	Output Voltage of Stage 4	18
SW2	Gate of PMOS Switch stage 2	20
SW3	Gate of PMOS Switch stage 3	21
SW5	Gate of PMOS Switch stage 5	22
SW4	Gate of PMOS Switch stage 4	28
Out	Output Of the Chip	29
Out	Output Of the Chip	30
CLK2	Oscillator Output 2 (Can be used for ex Inductor)	31
Vin	Input connecting to TEG	32
Vin	Input connecting to TEG	33
GND	Ground	35
GND	Ground	36

6.3 Experimental setup for system validation

The chip with QFN 48 package is soldered on a PCB for system validation in laboratory environment. A power supply is used for DC-DC converter input to emulate TE module output in a real system. PMOS switch gates are tied to stage 5 when it is necessary to turn them off. The input current is measured with a digital multimeter (Fluke 8846A) and oscillation signals are detected with an oscilloscope (Tektronix MSO 3034) using probes with 500 MHz bandwidth. The test setup is illustrated in Figure 6.4.

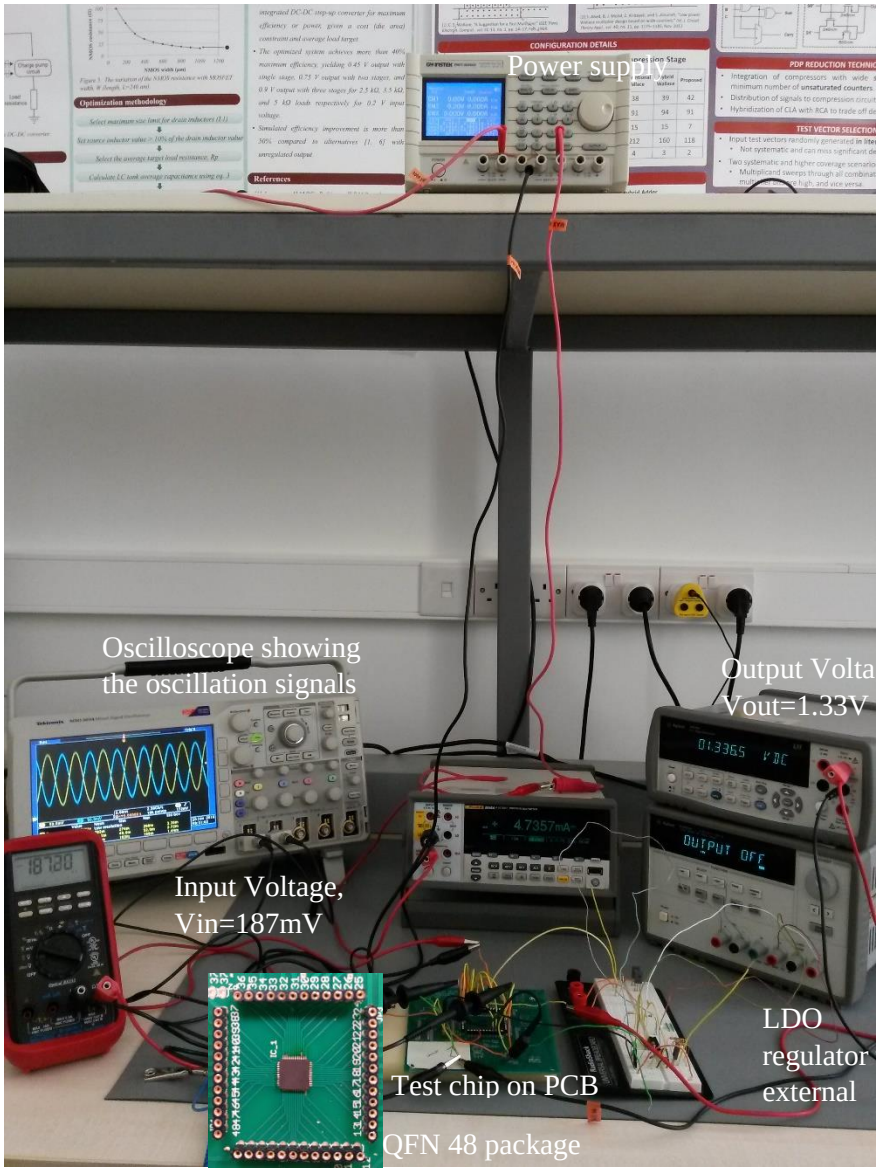


Figure 6.5 . Experimental setup for the system validation.

6.4 Characterization

6.4.1 Post-layout simulations with parasitic extraction (RLC)

To characterize the test chip for different conditions, three important paramters are taken into account, which are Input current (Iin), open circuit stage voltage (Vst5, Vst4, Vst3, Vst2), and oscillation frequency. These parameters have been characterized with an input voltage range, at no-load and loaded conditions. Figure 6.6 depicts post layout simulation results for stage voltages from 2 to 5 with respect to variable input voltage and no load condition. Input current and the oscillation frequency for the same conditions as mentioned above are illustrated in Figure 6.7.

6.4.2 Discrepancy between post-layout simulations and measurement data

During the validation procedure discrepancy was revealed between the Post-layout simulations and Measurement data. This means some aspects of the parasitic elements hasn't been extracted in the RLC post layout simulation. In fact there is not much could be done on this part since we have performed the most comprehensive parasitic extraction in the RLC format. These mismatches are shown in Figure 6.8 and Figure 6.9 respectively for varying input voltage and no load condition.

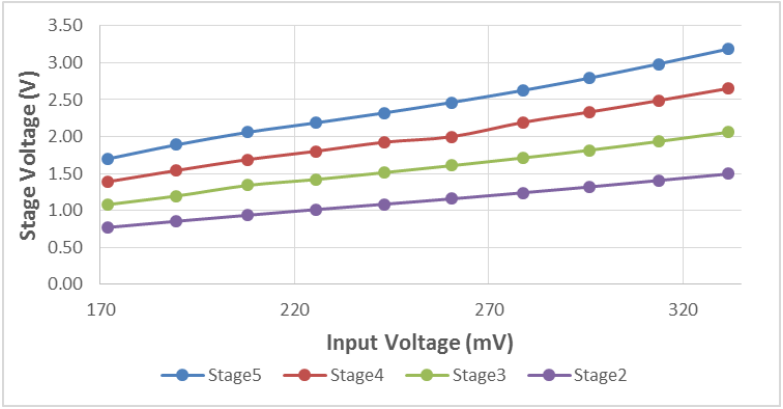


Figure 6.6. Post layout simulation results for output voltage from different stages with respect to varying input voltage and no load condition.

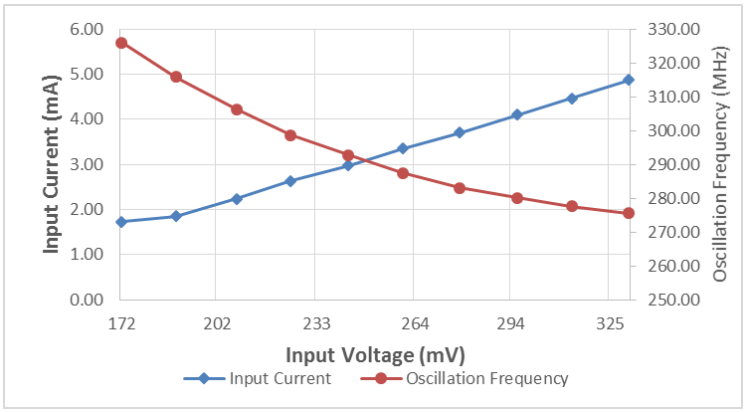


Figure 6.7. Post layout Simulation results for the input current and oscillation frequency with respect to varying input voltage and no load condition.

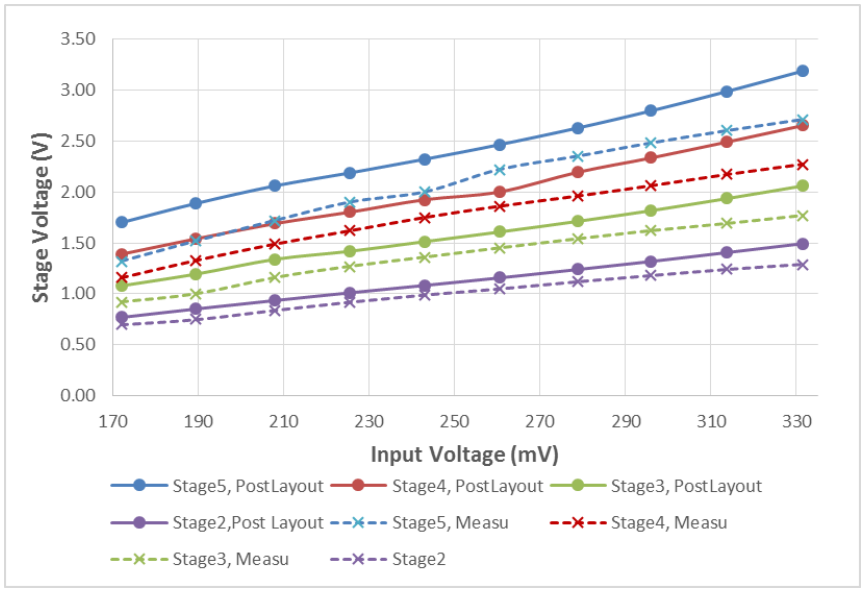


Figure 6.8. Stage voltages for post-layout simulations versus measurements.

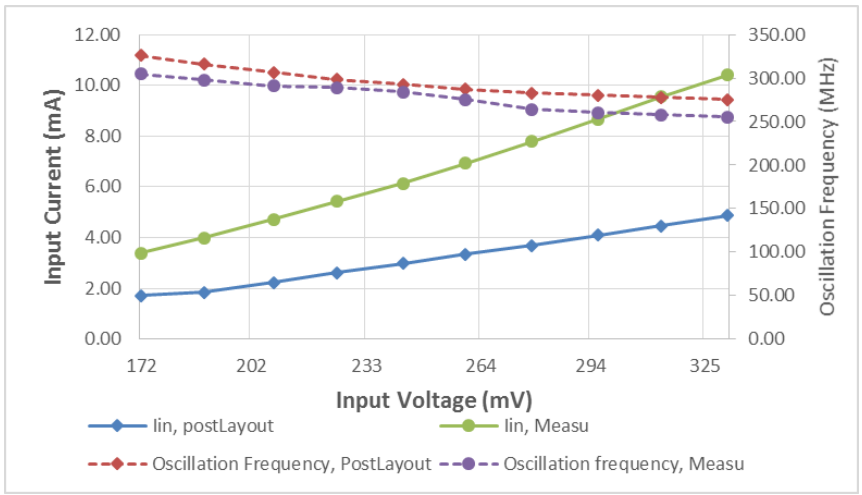


Figure 6.9. Oscillation frequency and input current for post-layout simulation versus measurements.

6.4.3 Model correlation with measurement

Despite optimization in the LC-tank oscillator's path to minimize the path resistance, the resistance of the inductor is slightly higher than that in the post layout simulations based on the direct measurement results by multimeter from Vin and CLK pins. However, adding only this parameter is not sufficiently reducing the discrepency. Large low-Vt (LVT) NMOS transistors used both in the LC-tank oscillator and the charge pump have also been investigated for any discrepancy from the simulation condition. Two clock pins have been considered in the design for this purpose. The pins enable direct access to the cross coupled NMOS structure to study its DC and AC characteristics. In addition, the effect of added RC from the oscilloscope probe together with the

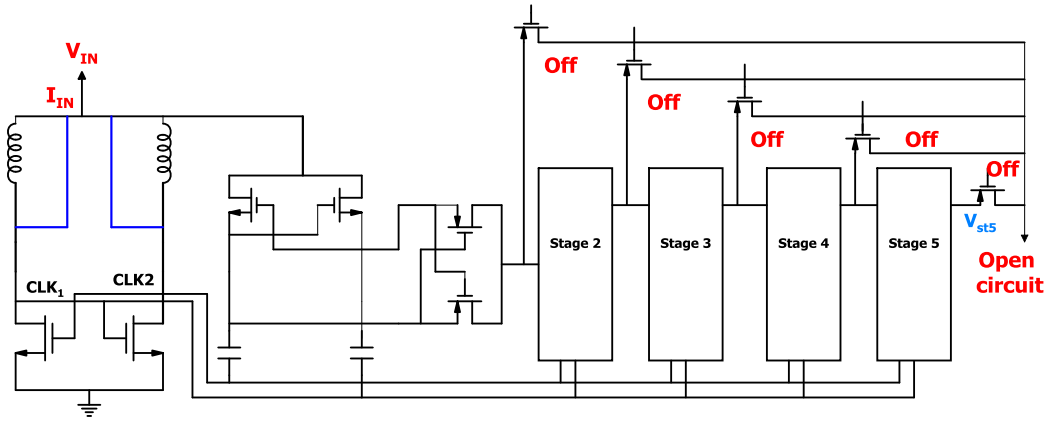


Figure 6.10. The variation of 5-stages DC-DC converter output voltage with load resistance.

pin-to-pad and on chip route resistance need to be taken into account. Such loading causes attenuation of the clock signal. The circuit to study the DC behavior of NMOS cross coupled transistors is shown in Figure 6.10. In this circuit the oscillation will be suppressed and the inductors will be shorted. The measured I-V curve for two test chips is illustrated in Figure 6.11. The circuit in Figure 6.10 is composed of two large NMOS transistors with gate and drain tied to each other. The expected curve should look more like a diode I-V curve. However, this curve is linear that requires a series resistance in the path. In addition to that, comparing simulation results with the measurement result leads to the conclusion that the Vt for the measurement results is less than that in the simulation. The higher series resistance is a result of pin-to-pad and the routing resistance. Although negligible in many circuits, it become crucial when some Ohms appear in the LC-tank oscillator circuit.

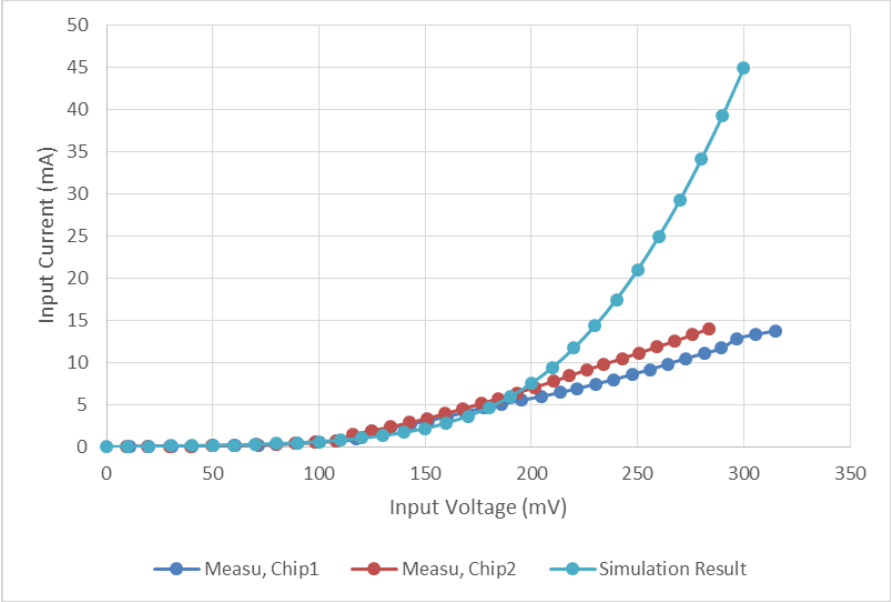


Figure 6.11. I-V curve of the circuit shown in fig. 5. 10.

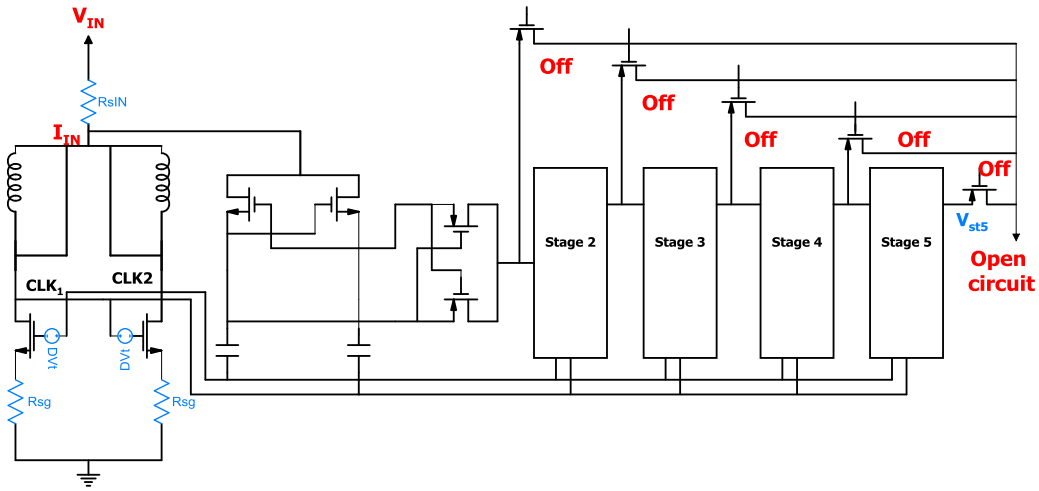


Figure 6.12. The proposed model for the DC analysis of fabricated NMOS mismatch with the simulated results.

The pin-to-pad resistance that comes with package is 0.1 Ω [103]. In addition the package parasitic capacitance and inductance are about 2 nH and 0.4 pF respectively. To quantify the resistance values and the Vt difference, the circuit in Figure 6.12 is used for simulation. The results of the simulation is then used for curve fitting. Simulation results of the DC analysis and the curve fitting are summarized in Figure 6.13. The path resistance for the chip 1 is higher than chip 2. For the chip 1, the best fit can be achieved by RsIN= 6 Ω , Rss=4 Ω and DVt=-60 mV which means Vt of the NMOS transistors of the chip is 60 mV less than that in the simulation. These values for the chip 2 are RsIN=6 Ω , Rss=2 Ω and DVt= -70 mV. The

more complete model for that covers mismatch is composed of Vt difference in the NMOS transistors of the charge pump as well as the overall extra capacitance of the NMOS gates due to package and wide POLY layer of the gate, and series resistance of the inductor. This model is depicted in Figure 6.14. RsIn represents the resistance of the Vin path, the Rs is the extra resistance in series with the inductor, DVt is the Vt difference between the chip and the post layout simulations for the oscillator NMOS transistors, Rsg is the ground path resistance, DVtCH is the Vt difference of the NMOS transistors in the charge pump and finally Cg represents the higher capacitance of the gate of the NMOS transistors.

6.5 Validation of the model resistance values by on-chip measurements

Detailed correlation analysis of the model, simulation, and experimental results has been performed. On chip resistance measurements are performed to validate the matching values used in simulation. Three paths are of interest based on the proposed modified model. These paths are resistance seen between two Vin pins, the resistance between Vin and CLK pin, and the resistance between two GND pins. Figure 6.15. demonstrates the location of the pin on the layout. Table 6.3 summarizes the resistance measurement results. The GND-to-GND measurement 3.49 Ω, which is considered in the modified model by Rsg. Vin-to-Vin measurement demonstrates that there is a resistance in the Vin path of about 4Ω.

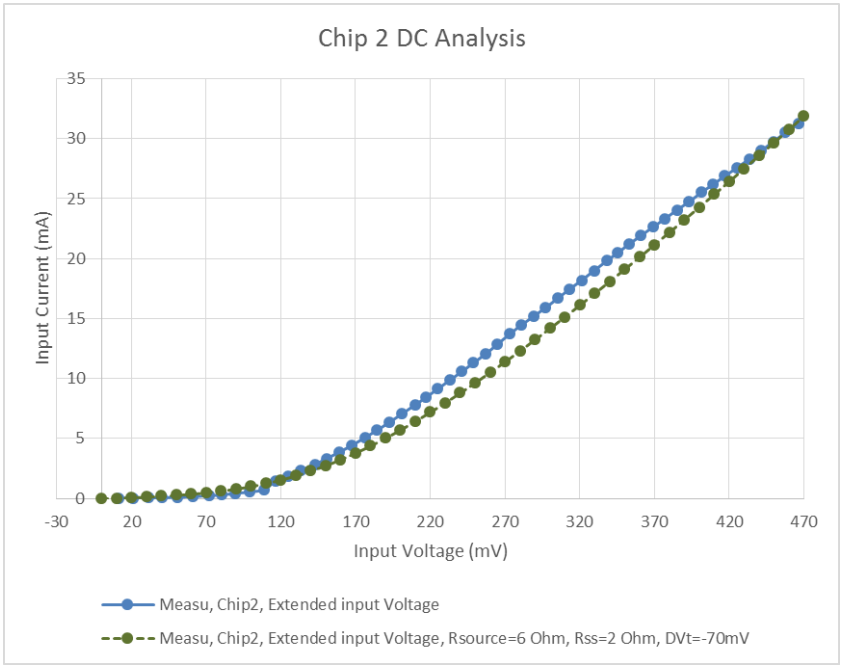


Figure 6.13. The variation of 3-stage DC-DC converter output voltage with load resistance.

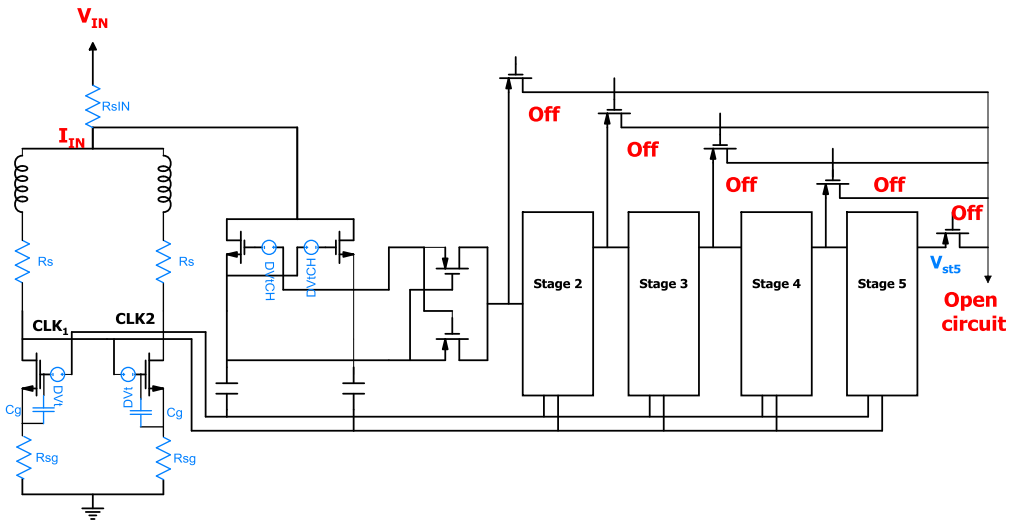


Figure 6.14. The modified model that identifies the parasitic elements that describe measurement data and post layout simulation discrepancy.

Vin-to-CLK measurement indicates about 8Ω resistance. However, this resistance is not fully because of the parasitic resistance of the inductor; CLK pin and path, and Vin pin and path are also included. Therefore, Rs in the modified model is estimated to be around 2 Ω. These parasitic resistances cause lower oscillation amplitude than expected in the simulation, and higher power consumption due to drawing high current from power source. The value of the gate capacitance can be found from the measurement results of the oscillation frequency. Based on this, an additional 2.5 pF capacitance is also added to the model.

6.6 Correlation between the model and circuit validation with and without load

Figure 6.16. Shows the simulation results for stages obtained from the modified model and the measurement results in the no-load scenario. Based on the results there is a match between simulation and measurement results. Figure 6.17 demonstrates the comparison of the input current with respect to the input voltage change with the modified model, post layout simulation results and the measurement results in the no-load scenario. The modified model shows improvement in this curve as well. However, since there is still discrepancy present in the input current figure, further investigation should be done to find other parasitic values. Figure 6.18 depicts the comparison of oscillation frequency of the modified model and the measurement results. To illustrate the effect of the oscilloscope on the oscillation signal a circuit equivalent model of the probe is added to the simulation. This model is shown in Figure 6.19.

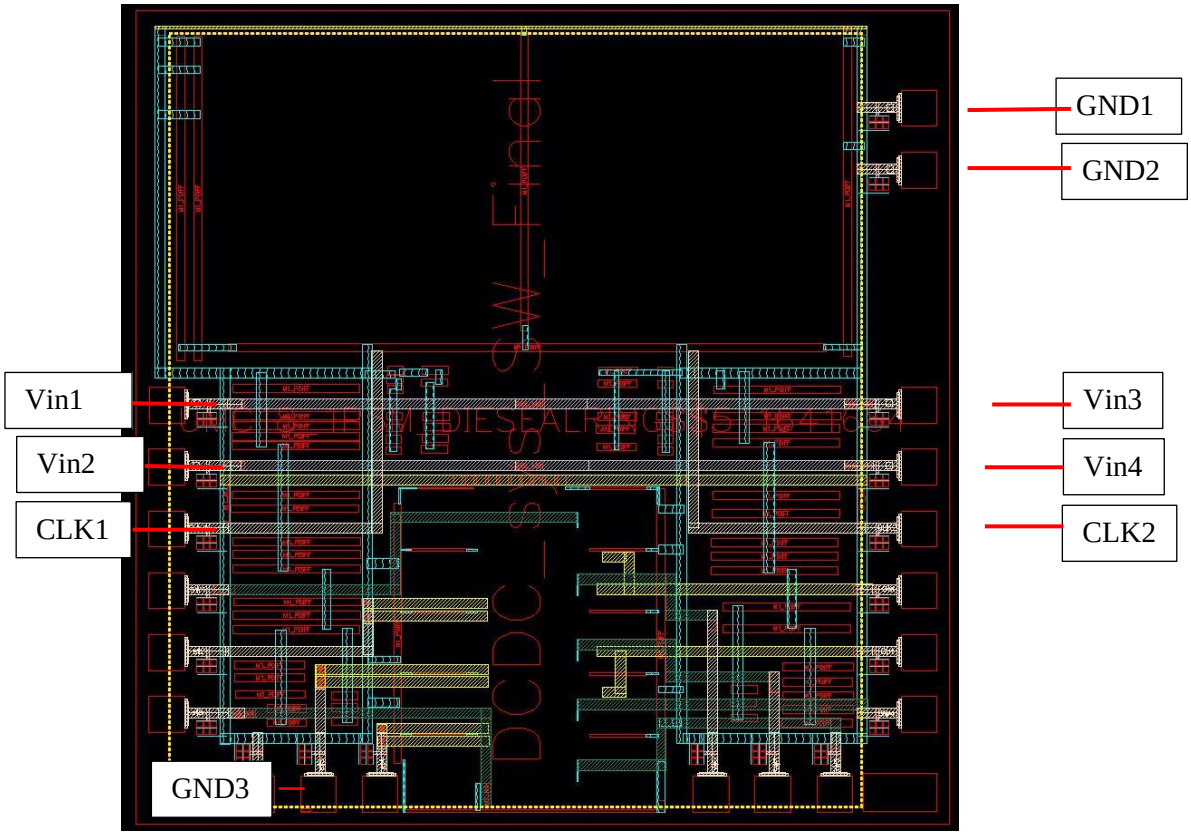


Figure 6.15. Location of the pins used for resistance measurement on the layout.

Table 6.3. On chip resistance measurement results.

GND1 -> GND3	3.49 Ω (The Ground path resistance + Pin to pad and Via resistances)
Vin1 -> Vin3	3.89 Ω (a metal line of 1363um length and 20um width + 2 pad to pin resistances + Vias)
Vin1 -> Vin2	3.96 Ω
Vin2 -> Vin3	3.95 Ω
Vin1 -> CLK1	7.98 Ω
Vin3 -> CLK2	7.95 Ω

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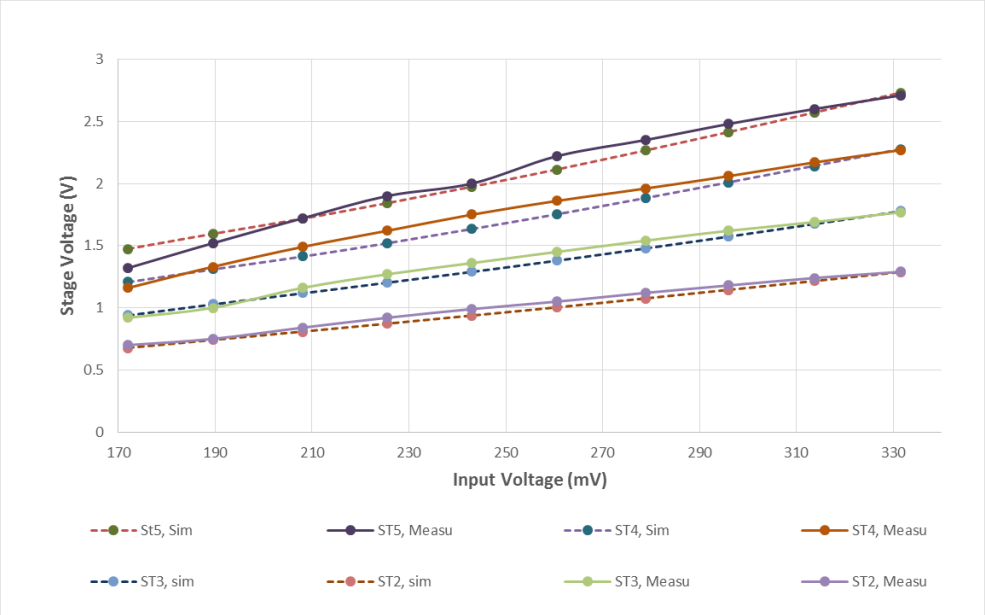


Figure 6.16. The comparison of the output voltage of the stages with respect to the input voltage change against the modified model no-load scenario.

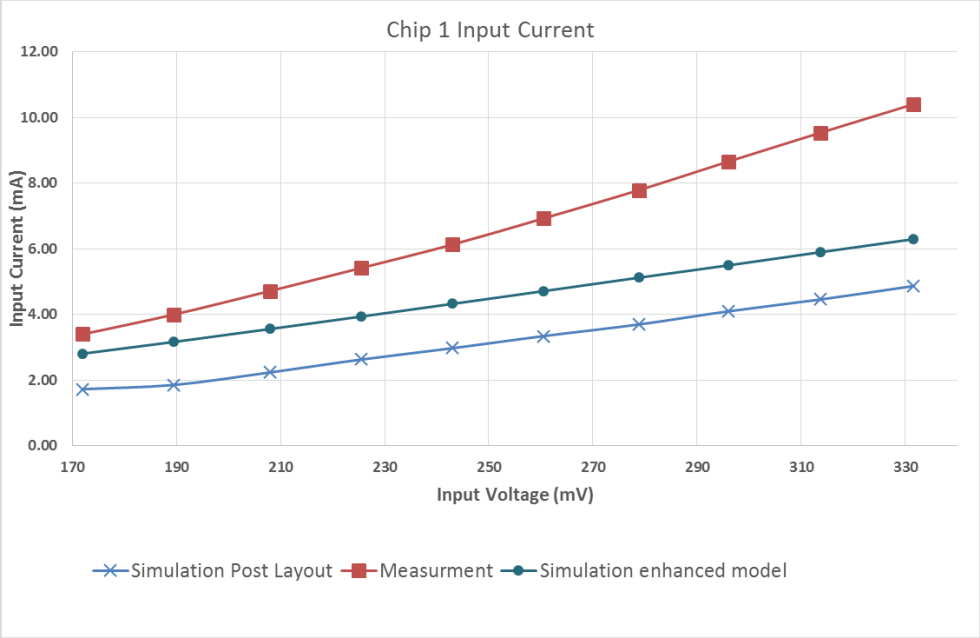


Figure 6.17. The comparison of the input current with respect to the input voltage change against the modified model no-load scenario.

Figure 6.20 demonstrates the comparison of the output voltage of the stages between simulation of the modified model and measurement results for a load of 5 kΩ. Figure 6.21 compares the input current between simulation of the modified model and measurement results for the same load. For low voltages there is a significant mismatch. Figure 6.20

indicates that further parasitic elements must be in the charge pump due to the fact that this measurement is with load and therefore current passes through different stages of the charge pump.

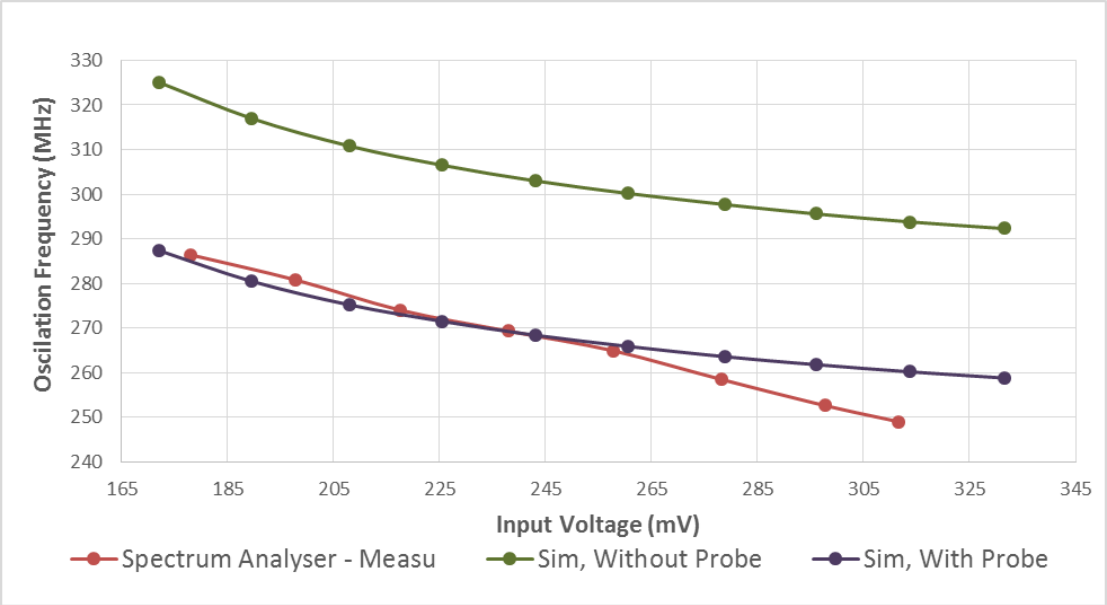


Figure 6.18. Comparison of oscillation frequency of the modified model and the measurement results.

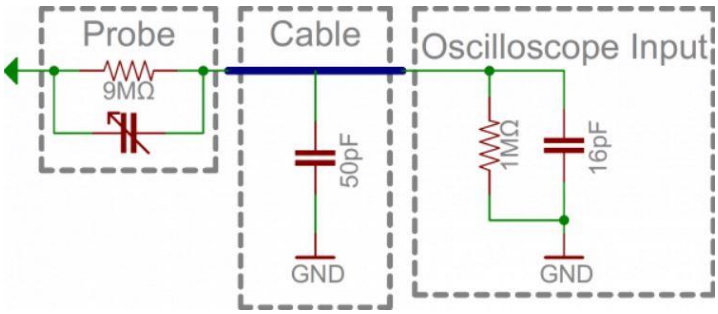


Figure 6.19. The oscilloscope probe model [104].

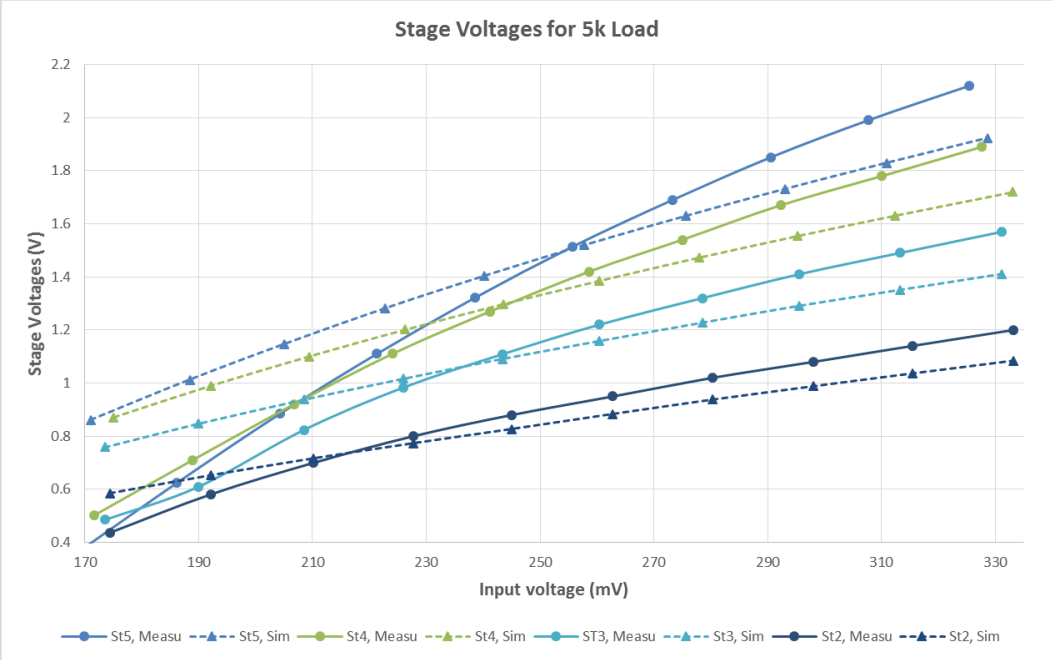


Figure 6.20. Comparison of the output voltage of the stages between simulation of the modified model and measurement results for 5 kΩ load.

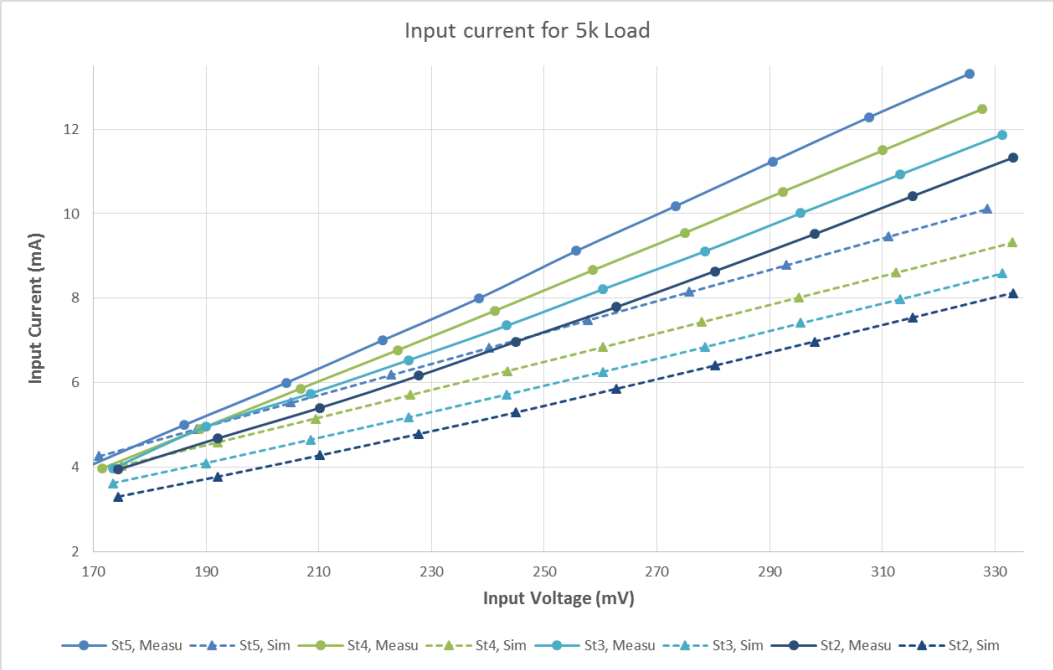


Figure 6.21. Comparison of the input current between simulation of the modified model and measurement results for 5 kΩ load.

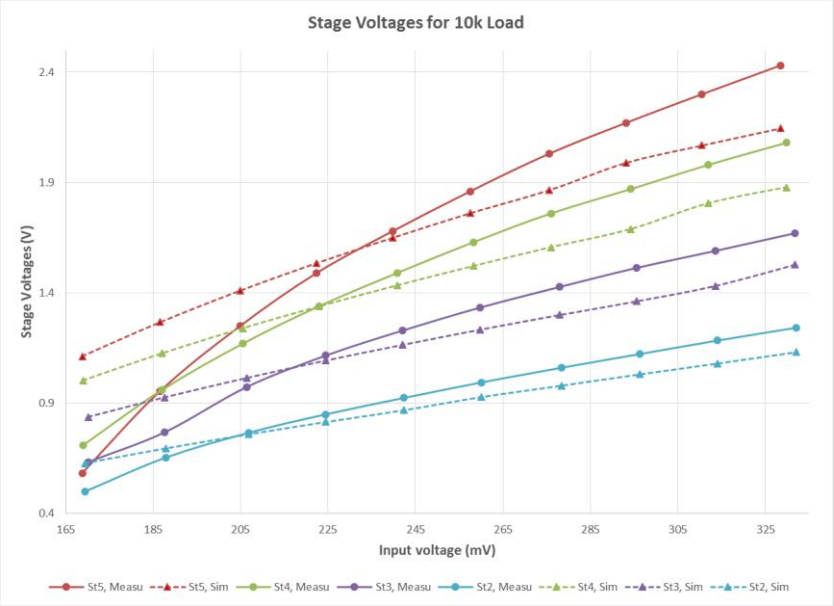


Figure 6.22. Comparison of the output voltage of the stages between simulation of the modified model and measurement results for 10 kΩ load.

Figure 6.22 demonstrates the comparison of the output voltage of the stages between simulation of the modified model and measurement results for a load of 10kΩ. Figure 6.23. compares the input current between simulation of the modified model and measurement results for the same load. The same discrepancy that indicates further parasitic elements in the charge can be observed for 10k load too.

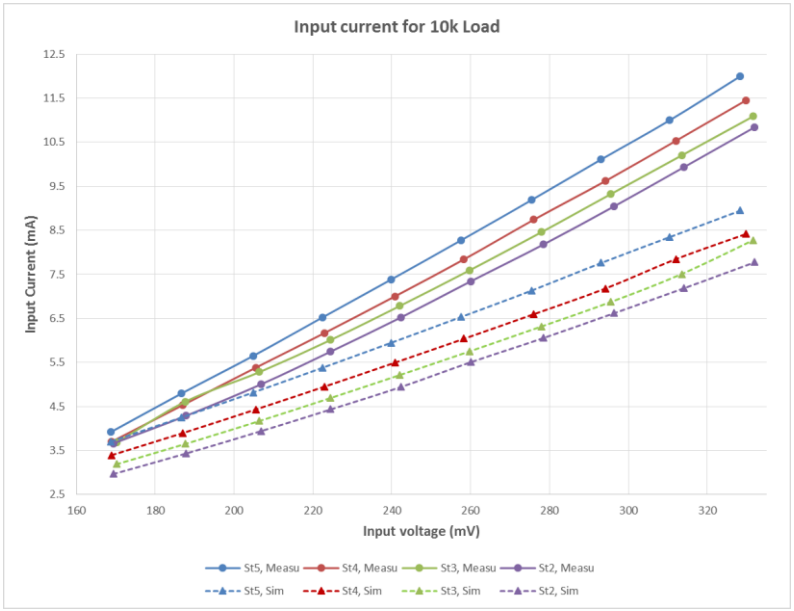


Figure 6.23. Comparison of the input current between simulation of the modified model and measurement results for loads of 10kΩ.

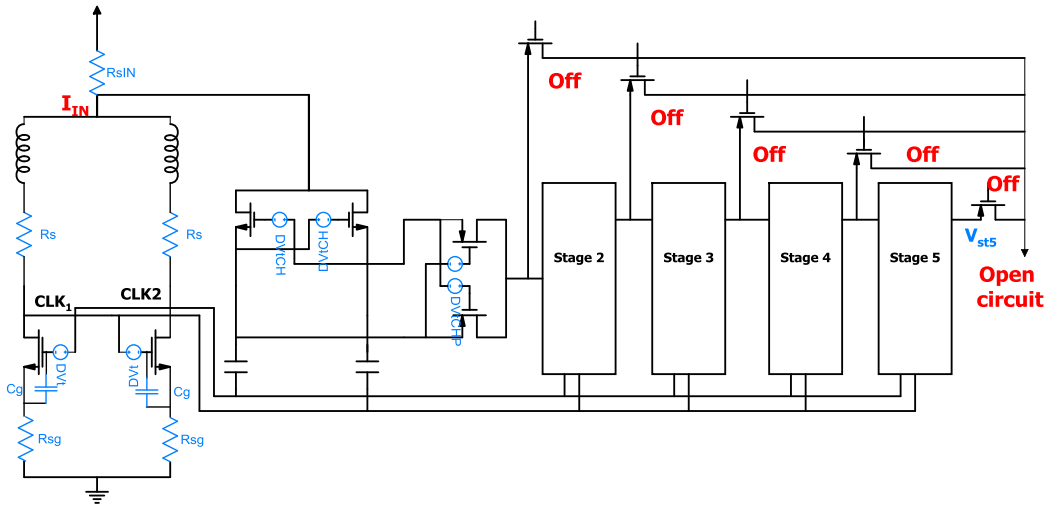


Figure 6.24. The final model elements that describe the discrepancy between the post layout simulation and the fabricated chip.

Another source of discrepancy is the difference in the Vt of the PMOS transistors. By adding a voltage source to the gate of the charge pump PMOS transistors similar to the ones added to the NMOS transistors, and doing curve fitting, a difference of 140 mV is identified through comparison of the stage voltage outputs. Figure 6.24 demonstrates the final model that explains the discrepancy between the post layout simulations and the fabricated chip. Figure 6.25 demonstrates that the stage output voltages match between the measurement data and the final model after addition of the Vt difference to the charge pump PMOS model. Even though at this stage the model is acceptable for further improvements, the increasing mismatch between measurement and simulations data in Figure 6.25 as the number of stages increase can be an indication for some other parasiticics such as resistance in the path between the stages or leakage of the large flying capacitors or MOSFETs. Table 6.4 summarizes the parasitic values of the modified model that results in a match between simulation and measurement results.

6.7 The fabrication data provided by the manufacturer

After modeling the discrepancy the fabrication company was asked to provide details about the parasitic elements and range of process variation. For 1.8 V LVT NMOS devices, the Vt from Table 6.5 can vary from 100 mV to 340 mV with a typical value of 220 mV. The simulation results show that cadence assumes Vt to be around 160 mV for these devices which is extrapolated based on the larger sizes given in Table 6.1 (LC-tank NMOS is 380/0.24 and Charge pump NMOS is 190/0.24). Based on the measurement results Vt of the

LC-tank NMOS must be around 100 mV and charge pump NMOS should be around 120 mV. This is very close to the minimum value specified in

Table 6.6.

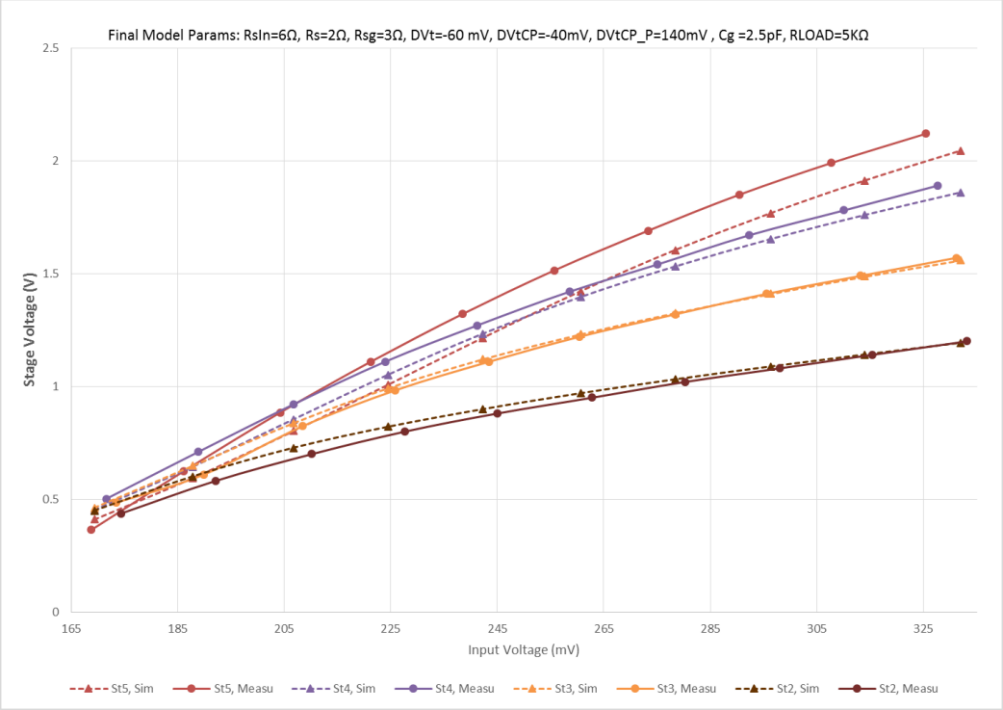


Figure 6.25. Stage output voltages match between the measurement data and the final model.

Table 6.4. Parasitic values of the modified model that results in a match between simulation and measurement results.

	RsIN (Ω)	Rs (Ω)	Rsg (Ω)	DVt (mV)	DVtCH (mV)	DVtCHP(mV)	Cg (pF)
Chip1	6	2	3	-60	-40	140	2.5

For LVT PMOS also according to the simulation we find 140 mV discrepancy. Based on the datasheet typical value is -220 mV, with maximum -340 mV. In an analogy to NMOS which is pushed to the minimum side due to size, large PMOS transistors seem to be pushed to the minimum side, having Vt around -340 mV instead of typical -220 mV. Table 6.5 demonstrates the resistance values. The values are given in Ω/sq for the N+ Poly which is the material used in a large size to build the large LC-tank NMOS transistors and in m Ω/sq for the metals. The measured resistance values demonstrated in Table 6.3 are roughly in accordance with the values in Table 6.5 since the length of the metals has reached some hundreds of μm. Another resistance source which can significantly add to the path resistance

is the use of VIAs. These VIAs have huge resistance. Even though all VIAs used in the layout are matrixes composed of hundreds of VIAs, they will contribute to the path resistance. In addition significant leakage values are shown in

Table 6.7. For instance for the LC-tank NMOS transistors 29.4 nA/μm × 380 μm = 11 μA is considerable and will dissipate significant current and power.

Table 6.5. The fabrication resistance values at 25^{O}C provided by the manufacturer of the chip as per our request.

Device	Min	Typ	Max	unit
N+ Poly Sheet (w = 0.18 μm)	2	8	12	Ω/sq[1]
Metal 1 Sheet (w = 0.24 μm)	45	77	115	mΩ/sq
Metal 2 Sheet (w = 0.28 μm)	30	62	95	mΩ/sq
Metal 3 Sheet (w = 0.28 μm)	30	62	95	mΩ/sq
Metal 4 Sheet (w = 0.28 μm)	30	62	95	mΩ/sq
Metal 5 Sheet (w = 0.28 μm)	30	62	95	mΩ/sq
Metal 6 Sheet (w = 0.44 μm)	25	41	55	mΩ/sq
Mvia1 (0.28 × 0.28 μm^2)	2	6.5	9.5	Ω/mvia
Mvia2 (0.28 × 0.28 μm^2)	2	6.5	9.5	Ω/ mvia
Mvia3 (0.28 × 0.28 μm^2)	2	6.5	9.5	Ω/ mvia
Mvia4 (0.28 × 0.28 μm^2)	2	6.5	9.5	Ω/ mvia
Mvia5 (0.28 × 0.28 μm^2)	2	6.5	9.5	Ω/ mvia

[1] Ohms per square is the unit of surface resistivity across any given square area of a material

Table 6.6. The fabrication threshold voltage values at 25^{O}C provided by the manufacturer of the chip as per our request.

Device / Vt	Min	Typ	Max	unit
Low Vt NMOS	0.1	0.22	0.34	V
Low Vt PMOS	-0.1	-0.22	-0.34	V

Table 6.7. The fabrication leakage current values at different temperatures provided by the manufacturer of the chip as per our request.

Device / leakage	25^{O}C	85^{O}C	125^{O}C	unit
Low Vt NMOS	29.4	142	330	nA/μm
Low Vt PMOS	12.4	82	188	nA/μm

6.8 Measurement results for the system with MPPT and output regulation

We have used the fabricated test chip to study the behavior of the autonomous chip. To do so, an external op-amp is used to implement the LDO regulator. The MPPT mechanism is then implemented by manually changing the number of stages. 3% power consumption overhead of the control circuitry is considered to achieve realistic results for the fully integrated autonomous chip. Figure 6.26. demonstrates the measurement results for the V_{TEG} = 350 mV, R_{TEG}=40 Ω and R_L = 4 kΩ . Due to the process variations and the discrepancy between the fabricated model and the post layout simulations described in earlier sections the efficiency and power output is decreased compared to simulation results in chapter 5. In Figure 6.26 starting from 5 stages the target 1 V is achieved and the number of stages is decreased to 4 where the target voltage is also met. With 3 stages the output voltage is less than 1 V therefore 4 stages are configured as the MPP. In Figure 6.27 the input voltage is increased and the output voltage for the stages 5 to 3 is the target voltage. The stage with the maximum efficiency is therefore stage 3.

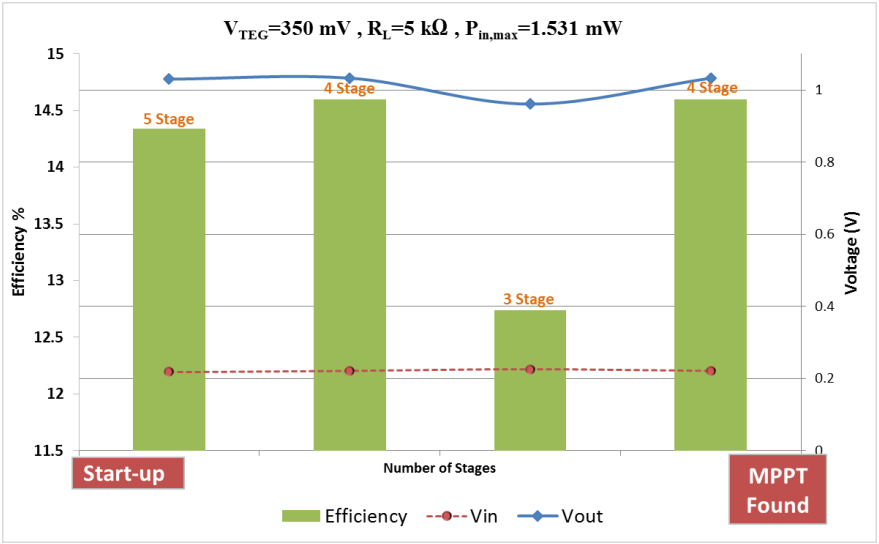


Figure 6.26. Measurement results for the autonomous system with V_{TEG}=350 mV and 5 kΩ load.

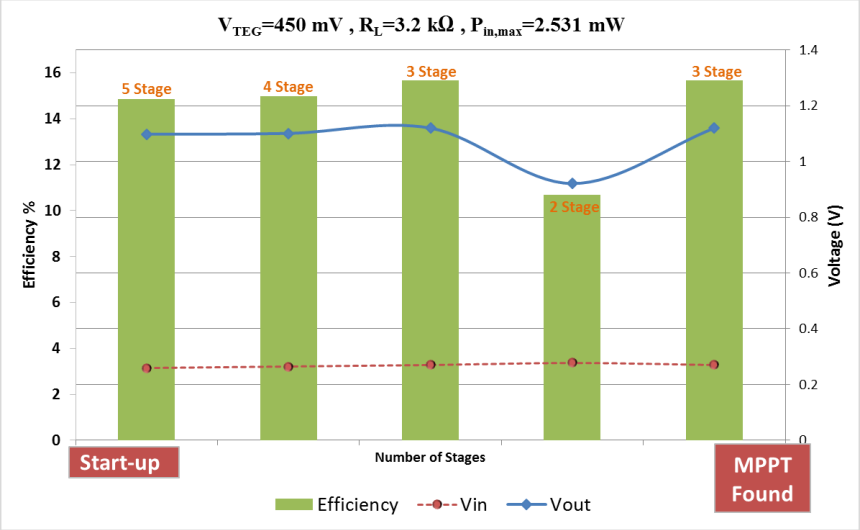


Figure 6.27. Measurement results for the autonomous system with V_{TEG}=450 mV and 3.2 kΩ load.

6.9 Measurement results for the DC-DC converter with the real TEG

The measurement results are performed using 2 TEG modules shown in Figure 6.28. This TEG module has 10 Ω internal resistance with 18 mV/K output voltage based on the measurement results. By configuring them in series, 10 ^{O}C temperature difference is necessary. The measured open circuit voltage and short circuit current values are 350 mV and 53 mA. For real wearable applications however a TEG module with higher power density should be utilized due to lower temperature difference availability when connected to the body. Figure 6.29 demonstrates the setup to provide the temperature difference. The chiller and the heater used to heat up the hot plate and to cool down the cold plate is shown in Figure 6.30. Measurement results are shown in Figure 6.31. The results prove that TEG modules are able to provide enough input power to the interface system that the measurement results do not change when using a real TEG instead of the ideal voltage supply with a series resistance to model R_{TEG}.

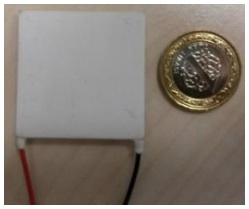


Figure 6.28. The 4 mm × 4 mm TEG Module.

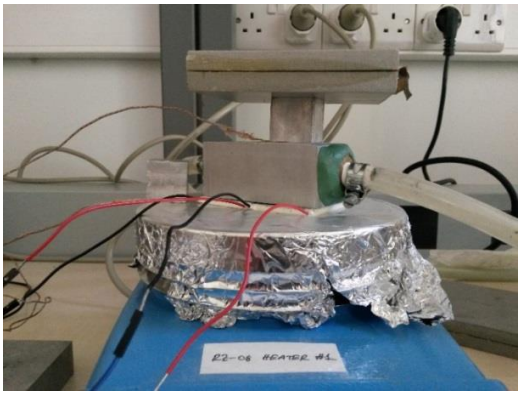
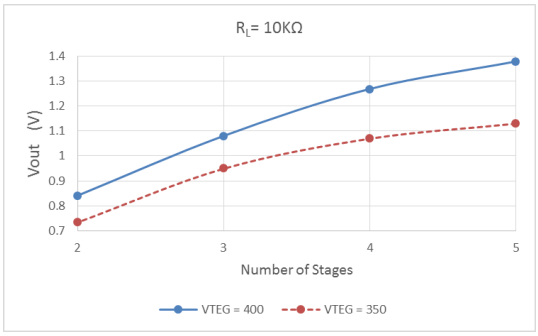
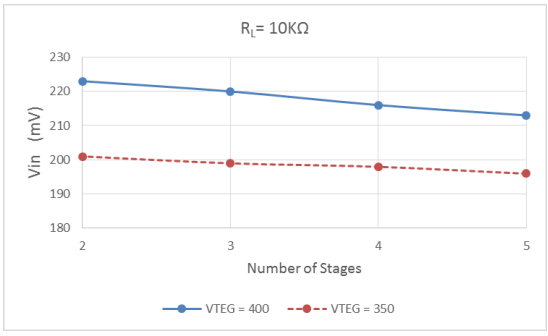


Figure 6.29. The TEG set-up to provide the necessary temperature difference.

Figure 6.30. The cooler and heaters used for TEG cold and hot palates.



(a)



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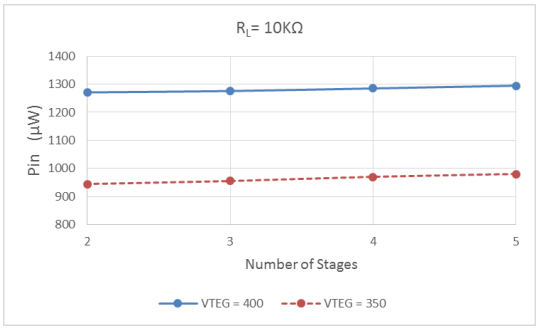

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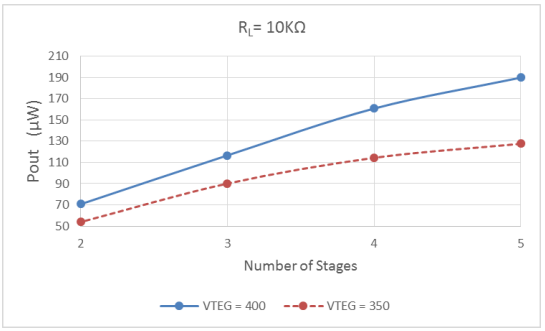

(d)

Figure 6.31. Measurement results of the fabricated chip for (a) output voltage , (b) input voltage (c) input power (d) output power of different stages with 10 kΩ load and V_{TEG}=350 mV.

CHAPTER 7

7 Thesis Conclusion

In this thesis, a new fully autonomous interface circuit for energy harvesting from thermoelectric generators for IoT and wearable applications is introduced. The thesis is built upon a DC-DC converter based on a charge pump and LC-tank oscillator previously introduced by our research group. The proposed autonomous circuit is capable of maximum power point tracking and output voltage regulation with considerably increased output power that makes is suitable to use in batteryless application with varying ambient condition and highly dynamic loads. The characteristics of the charge pump based DC-DC converter with LC-tank oscillator is studied to design and implement MPPT circuit. A novel MPPT algorithm is introduced that refrains from disconnecting the interface circuit from the application circuit making continuous power delivery possible for fully batteryless applications. The design is validated with pre and post layout simulations. The previously suggested DC-DC converter's topology is changed to have a reconfigurable number of stages necessary for the MPPT algorithm and then fabricated. Based on the post layout simulation results and the measurement results, some on chip parasitic elements are identified and a new model for the discrepancies is introduced. Based on the simulation results the chip is excellent for its output power, simplicity of the MPPT algorithm and minimum start up voltage compared to the state of the art fully integrated circuits in the literature. Table 7.1 shows the comparison of this research to the state of the art the literature. Based on Table 7.1, simulation results for the presented circuit has high output power capacity, which is comparable with the state of the art non-fully-integrated solutions in [74], [105]. Our solution also doesn't require a separate subsystem for startup since the LC-tank oscillator can start oscillating from voltages as low as 150 mV, which is comparable to the state of the art chips in the literature like the one introduced in [106]. Our solution offers regulated output voltage which is necessary for the elimination of the battery. In addition, the new MPPT algorithm refrains from disconnecting the system from TEG for open circuit measurement, and thus provides continuous output. The area is larger than other fully integrated solutions because of use of inductors which are bulky on-chip elements, but lead to much lower cost compared to solutions with discrete components. Measurement results revealed a drop in efficiency and the minimum start up voltage compared to the simulation results. This discrepancy was modeled and the parasitic elements in the fabrication process was discussed in detail in Chapter 6.

Table 7.1. Comparison of the current work with state of the art in the literature.

Reference	Process	Maximum Output Current	Separate Start Up Unit	Min V_{in} for start-up	Regulated V_{out}	Peak End to End efficiency	Fully Integrated	Off chip (L+C+R)	Chip Area	MPPT Mechanism
[74]	0.13 µm	500 µA	Yes	270 mV	1 V	64%	NO	0+1+2	0.835 mm^2	N[1], F[2], C[3] OCM[4]
[105]	65 nm	730 µA	Yes	80 mV	NO (0.7 V – 1 V)	73%	NO	4+2+0	0.51 mm^2	PWM Modulation
[107]	0.13 µm	900 µA	Yes	250 mV	1.8 V	80%	NO	0+7+2	NA	PWM Modulation
[70]	65 nm	358 µA	Yes	65 mV	1.8 V	65%	NO	1+2+0	1.96 mm^2	PWM Modulation
[25]	65 nm	300 µA	Yes	350 mV	1 V	83% @ vin=0.5 V	YES	NA	0.54 mm^2	N[1], F[2], C[3] OCM[4]
[106]	0.18 µm	5 µA	No	140 mV	NO (2.2 V – 5.2 V)	50% @ vin=0.45 V	YES	NA	0.86 mm^2	NA
[108]	0.18 µm	20 µA	No	500 mV	1.8 V	72 %	YES	NA	1.69 mm^2	N OCM
[73]	0.18 µm	16 µA	Yes	450 mV	3.3 V	81 %	YES	NA	3.2 mm^2	N OCM
This Work	0.18 µm	500 µA	No	150 mV[5] 170 mV[6]	1 V	47 % [5] 20% [6]	YES	NA	2.25 mm^2	N, Continuous

1 Charge pump number of stages

2 Oscillation frequency

3 Charge pump capacitance

4 Open circuit voltage measurement

5 Simulation Results

6 Measurement results

7.1 Future work

Based on the model that explains the discrepancy between the post layout simulations and the measurement results, the next fabrication run can be optimized in order to minimize the effect of the parasitics. In order to increase the power capacity of the system, interface circuits for energy harvesting from hybrid sources will be investigated based on the current topology. Using flexible TEGs, a wearable prototype will be built to measure different body signals.

Appendix I: Publications on Thesis

1- Tabrizi, Hamed Osouli, H. M. P. C. Jayaweera, and Ali Muhtaroğlu. "A fully integrated autonomous power management system with high power capacity and novel MPPT for thermoelectric energy harvesters in IoT/wearable applications." Journal of Physics: Conference Series. Vol. 1052. No. 1. IOP Publishing, 2018.

2- Tabrizi, Hamed Osouli, H. M. P. C. Jayaweera, and Ali Muhtaroğlu. "Fully integrated 98mV start up DC-DC converter for energy harvesting in batteryless IoT/Wearable devices." Electrical and Electronics Engineering (ELECO), 2017 10th International Conference on. IEEE, 2017.

3- Jayaweera, H. M. P. C., Hamed Osouli Tabrizi, and Ali Muhtaroğlu. "Fully integrated ultra-low voltage DC-DC converter with voltage quadrupling LC tank oscillator for energy harvesting applications." Electrical and Electronics Engineering (ELECO), 2017 10th International Conference on. IEEE, 2017.

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