EFFICIENT INTEGRATED DC-DC CONVERTERS FOR ULTRA-LOW VOLTAGE ENERGY HARVESTERS

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Approval of the Board of Graduate Programs

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ABSTRACT

EFFICIENT INTEGRATED DC-DC CONVERTERS FOR ULTRA-LOW VOLTAGE ENERGY HARVESTERS

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M.S. Sustainable Environment and Energy Systems Program

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The self-starting on-chip fully integrated ultra-low voltage DC-DC converters for energy harvesting applications presented in literature generally have low efficiency and output power capacity. Any improvement in DC-DC converter circuits in terms of energy efficiency, output power, self-starting modes, and voltage gain will contribute significantly to the widespread application of energy harvesters. Two novel fully integrated, self-starting, ultra-low voltage DC-DC converter topologies and model based optimization methodologies for these converters are studied in this thesis for efficient micro-power energy harvesting applications. According to the pre-layout simulations in standard UMC 180nm CMOS technology, the proposed 3-, 4-, and 5-stage DC-DC converter with voltage doubling LC oscillator can achieve 47.9%, 51.5%, 51.7% efficiency, and deliver 343 μW at 1.02 V output, 385 μW at 1.39 V output, and 454 μW at 1.65 V output respectively for 0.2 V input. The voltage quadrupling LC tank coupled DC-DC converter with 4 and 3 stages can achieve 33% and 31% efficiency while delivering 1193 μW at 2.18 V output, and 778 μW at 1.77 V output respectively for 0.2 V input. The measurements from the fabricated test chip for the first topology indicate major deviations from the simulations, i.e. the measured simulation peak efficiency is < 7% at 0.2 V input. Comprehensive design validation and analysis is presented for the discrepancy, which results in post-layout simulations of a new model that can be correlated to silicon observations. The fixes to the design and layout have been taped out as part of a second revision of the test chip to overcome the problems. The post-layout simulations for the new design achieve a peak efficiency of 41.5% at 1.54 V output, and 41% at 1.27 V output with 5 and 4 stages respectively for 0.2 V input. The theoretical analysis and optimization methods presented in this thesis are verified through simulations in Cadence environment.

Keywords: DC-DC converter, energy efficiency, charge pump circuit, LC tank oscillator.

ÖZ

ULTRA-DÜŞÜK VOLTAJLI ENERJİ TOPLAYICILARI İÇİN ETKİN ENTEGRE EDİLMİŞ DC-DC DÖNÜŞTÜRÜCÜLER

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Literatürde sunulan enerji toplama uygulamaları için kendi kendine çalışan tam entegre ultra düşük voltajlı DC-DC dönüştürücüler, genellikle düşük verimlilik ve çıkış gücü kapasitesine sahiptirler. DC-DC dönüştürücü devrelerinde enerji verimliliği, çıkış gücü, kendiliğinden çalışma modları ve voltaj kazanımı açısından sağlanabilecek herhangi bir gelişme, enerji toplayıcı uygulanmalarının yaygınlaşmasına önemli ölçüde katkıda bulunacaktır. Bu tezde, verimli mikro güç enerji toplama uygulamaları için, iki özgün tam entegre, kendi kendine çalışan, ultra-düşük voltajlı DC-DC dönüştürücü topolojileri ve modüle dayalı optimizasyon metodolojileri incelenmiştir. Standart UMC 180 nm CMOS teknolojisindeki düzen öncesi simülasyonlara göre, önerilen 3-, 4- ve 5-aşamalı LC osilatörlü voltaj katlama DC-DC dönüştürücüsü için sırasıyla, % 47.9, % 51.5, % 51.7 verimlilik sağlanabilir ve 0.2 V giriş için sırasıyla 1.02 V çıkışta 343 µW, 1.39 V çıkışta 385 µW ve 1.65 V çıkışta 454 µW sağlayabilir. 4 ve 3 kademeli DC-DC dönüştürücüye bağlanan voltaj dört katına çıkartan LC tankı, sırasıyla % 23 ve % 31 verimlilik elde edilirken, 0.2 V giriş için sırasıyla 2.18 V çıkışta 1193 µW ve 1.77 V çıkışta 778 µW alınmıştır. İlk topoloji için imal edilen test yongasından alınan ölçümler, simülasyonlardan büyük sapmalara işaret etmektedir, diğer bir değişle, ölçülen simülasyon pik verimi, 0.2 V girişinde < %7'dir. Kapsamlı tasarım geçerliliği ve analizi, tutarsızlık için sunulmuştur; bu, silikon gözlemleriyle ilişkilendirilebilen yeni bir model sonrası düzen simülasyonuna neden olmuştur. Tasarım ve yerleşimdeki düzeltmeler, sorunların üstesinden gelmek için test yongasının ikinci revizyonunun bir parçası olarak kaydedilmiştir. Yeni tasarım için düzen sonrası simülasyonlar, 5 ve 4 aşamalarda 0.2 V giriş için sırasıyla, 1.54 V çıkış için % 41.5 ve 1.27 V çıkış için % 41 pik verimleri elde edilmiştir. Bu tezde sunulan teorik analiz ve optimizasyon yöntemleri, Cadence ortamında simülasyonlarla doğrulanmıştır.

Anahtar kelimeler: DC-DC dönüştürücü, enerji verimliliği, Şarj pompa devresi, LC tank osilatörü.

DEDICATION

To my loving wife, Parents, Brother, Sister, and My supervisor

For their unconditional assistance and inspiration.

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NOMENCLATURE

C	Capacitance (pF)
P	Power
I	Current
f	frequency
η	Efficiency (%)
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
Low_Vt	Low threshold voltage
V_{in}	İnput voltage
V_t	Threshold voltage
gm	Transconductance
W	Width (μm)
L	Inductor (nH)
V_{DD}	Source voltage
R_S	Series resistance
R_P	Parallel resistance
C_S	Series capacitance
C_P	Parallel capacitance
P_T	Total power
V_{PP}	Peak to peak voltage
TE	Thermoelectric

CHAPTER 1

1 INTRODUCTION

1.1 Background

The concept of smart cities under the paradigm of "sustainable development" boosts up the use of wearable electronic devices especially for communication, health care, and security applications as well as Internet of Things (IoT) applications. Along with the enhancement of consumer electronics (CE) and machine-to-machine (M2M) technology, the wireless interconnection of portable devices, which is one pillar of IoT, has become ubiquitous to increase efficient utilization. According to CISCO and several other organizations, the estimated minimum number of IoT device usage at 2020 is 50 billion [1]. The majority of IoT devices and consumer electronics including wearable electronic devices are wireless due to inconvenience and expense of wiring. Examples include wireless sensor networks with thousands of sensor nodes like WiseNet developed by CSEM [2] and others discussed by Yang [3] and Wagle [4]. However, an individual wireless device requires a temporary power reservoir such as a button cell battery. As a result, there are a number of ultra-low power wireless sensor protocols like ad-hoc networks [5] and intelligent sensor systems [6] in order to minimize the power consumption and utilize the battery usage.

In the past few decades, the evolution of batteries in terms of higher power density has made them more feasible for use in mobile electronic applications. Use of batteries may significantly increase system cost (including maintenance and replacement cost), however, and may be impractical in some of the implantable, portable and wireless system applications. Battery replacement is expensive, time-consuming, and inconvenient. Examples include on-body sensor nodes used for the chronic disease monitoring and treatments such as pacemakers [7], implantable pressure sensors [8], wireless transmission for the analysis [9], and thousands of smart sensor node networks for the IoT applications [10]. On the other hand, different sub-circuits in an electronic system require different voltage levels for proper operation. The size and weight of the consumer electronic device increase in proportion to the number of batteries. In addition, the short lifespan of rechargeable batteries in mobile electronic devices (range of 2-4 years) results in an exponentially increasing amount of e-waste [11].

Despite the evolutional enhancement in quality of life through the technological advancement, the disproportional abundance of waste electronic and electric equipment (E-waste) emerges

as the fastest growing waste issue in the world [12], [13]. Computer related discarded appliances including IoT devices, and mobile electronic devices have been the dominant e-waste components during last decades due to their short lifespan. E-waste includes appliances that comprise of batteries, power cords, printed circuit boards with lead (Pb) soldering, and wires. Small scale batteries consist of different toxic materials and chemicals. The improper disposal or recycling can cause to seep or disintegrate these toxic compounds into the environment including heavy metals like Lithium, Nickel, lead, copper, and Cadmium, and toxic pollutants like $LiClO_4$, $LiPF_6$ and $LiBF_4$ [14], [11]. But currently, 90% of discarded lithium-ion batteries which are used in consumer electronics (CE) are disposed to the environment without proper recycling as e-waste [15]. The discarded battery related hazards can be significant in next few years due to the massive abundance of mobile electronic applications. For instance, in 2014, China's (world largest lithium-ion battery manufacturer and consumer) estimated lithium-ion battery export is 1.32 billion which represents a 16.8% increase compared to the previous year [16]. Open burning of PCBs and PWBs (printed wire board) which are the major components of electronic devices [17] and wires has contributed to release hazardous chemicals, which potentially caused environmental pollution including the river water, air, and soil of the burning area [18]. The manufacturer to end-user transportation and recycle process also contributed to the fossil fuel combustion which causes the environmental pollution. Therefore, a global effort is ongoing in size reduction combined with low power consumption in order to enhance the lifespan and minimize the environmental hazard. Reduction of power consumption benefits systems by lowering battery size and minimizing the emission of greenhouse gasses due to the use of fossil fuels for grid power generation and transportation. Implementation of fully integrated circuit architecture leads to size reduction of the system and to elimination of wires, PCBs and PWBs in microelectronics. Therefore, smart device revolution along with sustainable developments triggers the necessity for integrated, lightweight, green-power solution with long lifetime as an alternative to the monolithic batteries.

One feasible green energy replacement for the battery is energy harvesting from ambient sources to directly power electronic devices (self-powering). As the development of very large scale integration (VLSI) technology allows downscaling of the power consumption and area of the integrated circuit devices, small-scale energy harvesting techniques become feasible in powering smart electronic devices. Furthermore, micro- to milli-power harvesting systems allow elimination of grid connection and rechargeable batteries to advance the energy autonomy of mobile electronic devices [19].

1.2 Common energy harvesting techniques

There are several types of promising small scale energy harvesting techniques including solar, kinetic, thermal, fuel cell, bio mass, piezoelectric, and electromagnetic. Solar, thermoelectric, kinetic, and electromagnetic energy harvesting are four most common small-scale ambient energy scavenging techniques developed in last few decades. The source for the ambient energy harvesting depends on the application. For example, the human body is the most usual energy harvesting source for the wireless body area network (implantable sensor node). The kinetic and thermal are the usual kind of techniques used in human body generated power for mobile applications [20] e.g. wearable sensor networks and computing microchips.

The solar or photovoltaic energy emerged as a viable technique due to the successful ongoing research effort on sustainable green energy solutions for the increasing energy demand. Photovoltaic cells have the property to convert incident light into electricity through charge separation of two materials with different conduction mechanism [21]. These two materials are composed of P-type semiconductor and N-type semiconductor, which enable charge flow in one direction as shown in Figure 1.1(a). Because solar cells work as a flux sensitive voltage limited current source [22]. The power density of a typical solar cell in outdoor at noon is 15 mW/cm^2 [22] and is limited to several tens of $\mu W/cm^2$ (typically 10 $\mu W/cm^2$ [23]) for the indoor applications due to the limited solar flux density. Summing voltage through series connection of the solar cells makes high output voltage feasible. But the necessary area is also increased with the number of solar cells. Despite the availability and ease of access, solar energy harvesting has poor energy security. Due to the dramatic variation of the source power, an energy storage reservoir such as a battery or a super capacitor is necessary to prevent a power failure.

Thermoelectric energy harvesting technique uses the phenomena of Seebeck effect to convert thermal energy into electrical energy. The pyroelectric materials have the property to generate an electrical charge with the temperature gradient. There have been a number of ongoing successful research efforts to implement large scale thermoelectric energy harvesting techniques. For example, waste thermal energy of vehicle exhaust and industrial processes can generate electrical energy using thermoelectric harvesting technique [24]. The lack of moving parts in the thermoelectric generators along with reliability and scalability make them ideal for small scale energy harvesting [25]. The thermoelectric generator consists of a series array of thermocouples [26] which generate voltage difference across the two terminals due to the temperature gradient as shown in Figure 1.1. (b).

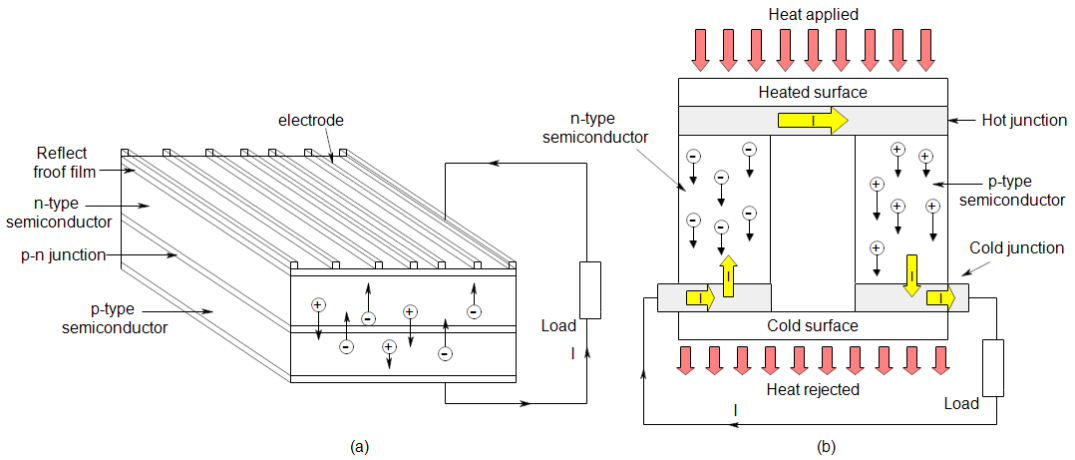

Figure 1.1. (a) Solar cell for photovoltaic, and (b) thermocouple for thermoelectric, energy harvesting.

The thermopiles of the thermocouple consist of p-type and n-type semiconductors to generate a voltage drop across the p-n junction due to the different mobility of charge carriers, which are stimulated and flow from high-temperature terminal to low-temperature terminal. The generated voltage is proportional to the temperature difference ($V=\alpha.\Delta T$). The proportionality constant (α) is the Seebeck coefficient of the thermoelectric material. Despite the inverse proportionality between Seebeck coefficient with conduction electron density, the highest Seebeck coefficients have been observed in semiconductors. Since the highest observed Seebeck coefficient is limited to at most hundreds of microvolts per Kelvin [27], a large temperature gradient is necessary to generate tens and hundreds of milli-Volts in small area. Recent development of the microelectronic technology utilizes the feasibility to fabricate the micro-technological thin film substrate thermoelectric generators. The first micro-technological thermoelectric generator was fabricated by Rowe and co-workers with the leg dimension of 4.5 mm x 20 µm x 0.4 µm and 530 µV/K Seebeck coefficient [28]. Due to the limited Seebeck coefficient of the thermoelectric generators, the output voltage of the thermocouple is in the range of 20-400 mV at most for typical environment conditions [29]. The temperature gradient of the thermoelectric generator is a function of the ambient temperature. Therefore, voltage boost up converter with temporary energy receiver is essential for the system applications.

The energy extracted from the mechanical movement in the environment can be converted into electrical energy through kinetic energy harvesting techniques. The most commonly available form of environmental kinetic energy is vibration, which can be converted into electrical energy using piezoelectric, electrostatic and electromagnetic, techniques [30]. The electromagnetic harvesting method is commonly used in macro scale wind and hydro

generators. The environmental kinetic energy is used to rotate the coil, which is placed in the magnetic field to induce current on the coil following Faraday's law. Printed coils and permanent magnets are utilized for the micro scale harvesting techniques. Converted output voltage level depends on the magnetic field strength, number of turns of the coils and rate of change of the flux (rotational speed of the mass/spring). Piezoelectric materials can generate an electric charge when the substrate is squeezed or stretched [31] as shown in Figure 1.2. (a). The generated voltage is proportional to the substrate stress. The oscillator system connected to the piezoelectric material cantilever generates AC voltage with irregular amplitude. Electrostatic energy harvesting mechanism is based on varying the capacitance of a fully charged capacitor, as illustrated Figure 1.2. (b). Change in capacitance produces a voltage across the capacitor terminals to keep the voltage or charge of the capacitor constant. The utilization of on-chip MEMS variable capacitors makes electrostatic converter more attractive compared to electromagnetic methods due to the lack of bulky inductors. However, it is necessary to have a temporary power reservoir such as a battery for the initialization of the capacitor charge.

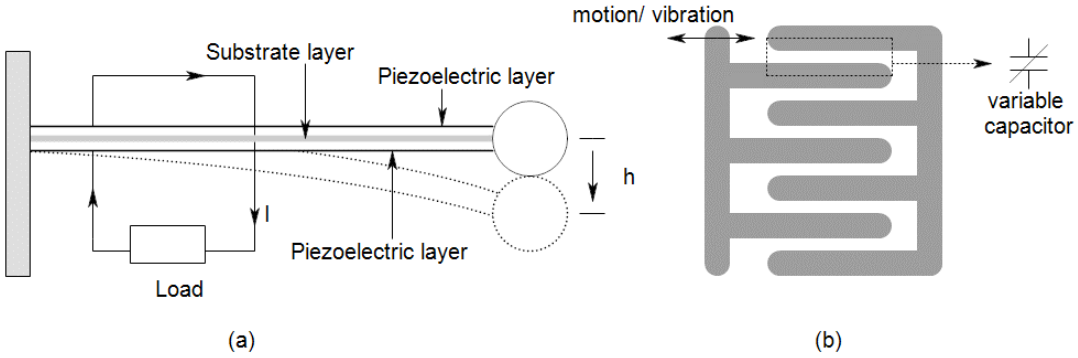

Figure 1.2. (a) Piezoelectric energy harvester, (b) electrostatic energy harvester, to convert kinetic energy into electrical energy.

The vibration of the permanent magnet attached spring can be used to generate the electromagnetic electricity as illustrated in Figure 1.3. (a). The rate of change of magnetic flux through the inductive coil generates the electric current through the coil, following the Faradays law.

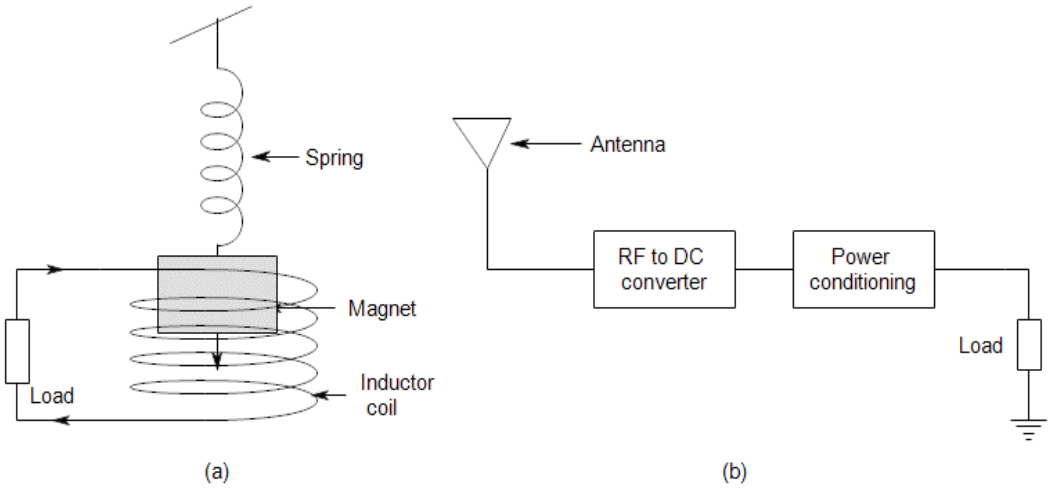

Figure 1.3. (a). Electromagnetic vibration energy harvester, (b) RF energy harvester.

The current environment consists of billions of electromagnetic waves due to the development of wireless communication and broadcasting. RF wave harvesters contain three main components to harvest electrical energy as shown in Figure 1.3. (b): Antenna to receive the high-frequency EM waves, AC to DC converter to convert the captured signals into electric current, and voltage step-up converter with the regulator to boost up the voltage for the usable range.

1.3 Problem associated with the energy harvesting techniques

The common phenomena of the ambient energy harvesting system are the infinite lifetime compared to the environmental hazardous short lifetime batteries as illustrated in Table 1.1.

Table 1.1. Power density comparison of energy sources used for energy harvesting.

Energy harvesting mechanism		Power density-one year lifetime	Power density-ten year lifetime
Solar-outdoor [32]		30 - 5 mW/cm^2	30 - 5 mW/cm^2
Solar-indoor [33]		13- 88 µW/cm^2	13- 88 µW/cm^2
Vibration	Piezoelectric [34]	1500 µW/cm^3 @ 10 m/s^2 acceleration	1500 µW/cm^3 @ 10 m/s^2 acceleration
	Electrostatic [35]	133 µW/cm^3 @ 1.3 kHz	133 µW/cm^3 @ 1.3 kHz
Thermal [36]		60 µW/cm^3 @ 5 ^{0}C gradient	60 µW/cm^3 @ 5 ^{0}C gradient
Batteries [31]	non-rechargeable	45 µW/cm^3	3.5 µW/cm^2
	rechargeable	7 µW/cm^3	0

But there are three common adverse characteristics of the ambient energy harvesters which have to be taken care of in mobile applications.

- The harvester output is unregulated.
- The generated output power is interrupted and not continuously steady state.
- The average output power is limited in the range of at most few tens of mW, and the output voltage is typically at most couple of hundreds of mV.

Since the harvester output is a function of the corresponding environment parameter (e.g. ambient temperature for the thermoelectric generator), the energy harvester cannot be used for direct powering of the electronic devices. For example, a small scale thermoelectric generator '1MD02-035-03TEG' with the hot side at 35 ^{0}C and at 55 ^{0}C generates 0.07 V, 1 mW and 0.24 V, 10 mW optimum output respectively while cold side is at 27 ^{0}C. Any reduction in the hot side temperature causes a corresponding drop in the output voltage and possible shut down of the electronic device. Therefore, the harvester output is often connected to a small temporary storage used in mobile applications such as capacitors, super capacitors, and small rechargeable batteries. But the harvester output is too low to charge these components up to the required voltage levels. The minimum sink voltage for the typical rechargeable battery is around 1 V [37] which can be 4-10x of the output voltage level of the micropower harvester. The monocrystalline silicon solar cell 'TG18.5 BR' has 500 mV output at outdoor applications with a light intensity of 100 mW/cm^2 [38]. But the output voltage of the typical single solar cell is limited to at most 200 mV in dark office environment [39] The small scale (centimeter range) piezoelectric device generates alternative voltage with milliwatt range at typical ambient conditions [40]. Hence the AC to DC converter is necessary for kinetic energy harvesting application for the mobile electronic powering. The RF energy harvester also needs an AC-DC converter for the electronic applications. But the typical output voltage level of these single stage AC-DC converters is limited to 200 mV at ambient conditions. The output voltage level of these converters can be boosted up using stages of charge pumps, which decrease the efficiency of the system. Low efficiency leads to increase in power dissipation and causes heating problems, which are important in implantable microelectronic applications. Therefore, a power management unit is necessary between harvester interface and the electric load as shown in Figure 1.4.

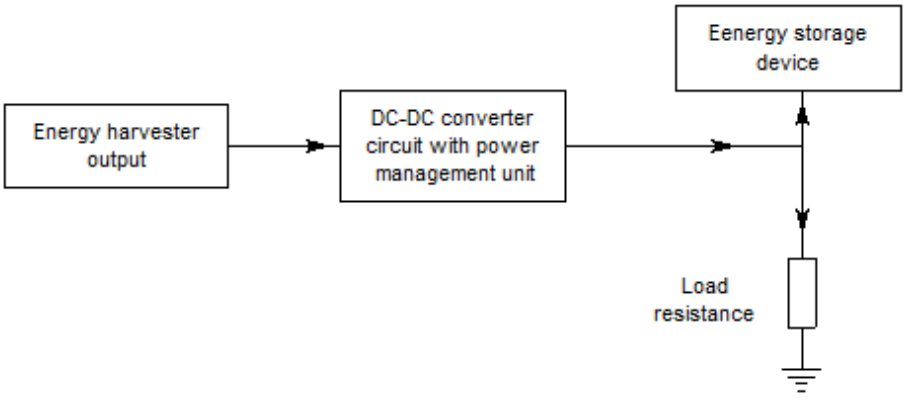

Figure 1.4. Block diagram of the energy harvester interface.

Employing the energy management unit of the energy harvester array through a direct current to direct current (DC-DC) converter offers voltage boost up method to generate the DC voltage to drive the load. Therefore, an integrated DC-DC converter enhances the mobile electronic application by reducing the battery area or even completely replacing the battery from energy harvester prototype. But the existing low voltage DC-DC converters are relatively low in performance; few high-performance implementations are built from discrete components such as bulky inductors and capacitors and are usually limited in charge delivery at a low input voltage and poor output characteristics at low load resistance.

1.4 DC-DC converters

DC-DC converters are widely used in almost all portable electronic devices like laptops, MP3 players, mobile phones, and other wearable electronic devices. The smart electronic devices comprise of several sub-circuits with different operational load voltage. Therefore, the DC-DC converter circuits are used to convey the necessary voltage level for the load resistance from the main power reservoir like a battery or an energy harvester. A good commercial DC-DC converter should satisfy the following requirements;

- Low cost
- Good steady state performance (constant output voltage for ripple input)
- Minimum start-up conditions
- Ability to self-start

As all other smart devices, the DC-DC converter should be lightweight, small in scale, high in efficiency, low in cost, to be competitive in the market. As a result, the best solution in terms of economy is integrated design with high efficiency. The steady state performance is the output characteristics of the DC-DC converter with the different conditions at the inputs. A

good design should deliver maximum power and maximum output voltage level for the given conditions. The output variation should be minimal. The output characteristic variation like efficiency, charge delivery, output level for different load conditions, should be within a specific range for the considerable range of input. Availability of minimum start-up condition with self-starting capability increases the number of possible microelectronic applications.

DC-DC converters are categorized into two groups according to the conversion direction of the design: Step up converters and step down converters. The step down DC-DC converters are commonly used for electronic applications that recharge batteries through the grid connection. Examples include the standard 12 V laptop battery step down to 5 V to power USB ports and keyboard through the step-down converter. The requirement and popularity of the step-up DC-DC converter arises with switching the source from grid power to the sustainable green power for the smart applications. Hence, DC boost up converters are popular in energy harvester applications due to the limited source voltage. There are few step-up converter applications available in past generation portable electronic devices. For example, a 3 V battery operates portable radio which has an audio amplifier with 5 V supply for the proper operation. In order to have a long battery life, the efficiency of the DC-DC converter should be high to minimize the power losses in addition to avoiding heating problems.

There are two fundamental types of DC-DC voltage converters. The first type is linear conversion based on the voltage divider using the array of resistors also known as linear regulators. The block diagram of the linear voltage converter is shown in Figure 1.5. Variable resistor (R) can be replaced with a MOSFET in the linear region for on-chip integration. The feedback with control system adjusts the variable resistor to keep output at a constant voltage regardless of the load variation. The main drawbacks of this linear DC converter are the significant power dissipation and the fact that it achieves only step down conversion. Therefore, the efficiency of the linear DC converter depends on the variable resistor and the current through the feedback loop. The current through the feedback loop is low and the power dissipation of the controller is small. The advantage of area reduction and cost benefit compared to the distinctive battery usage results in wide usage of the linear DC converters for different electronic circuit applications.

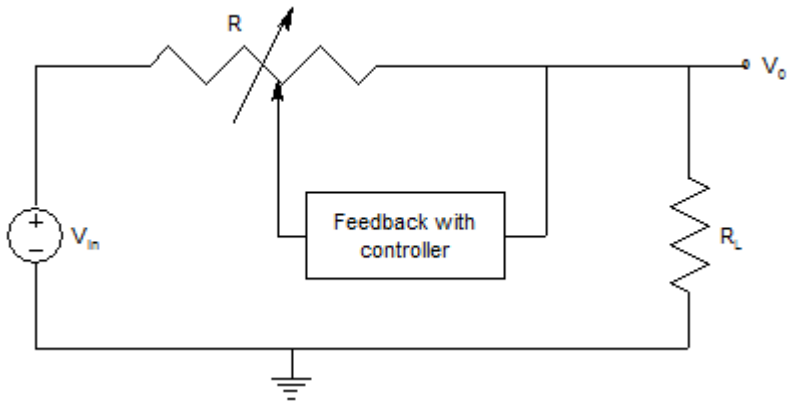

Figure 1.5. Block diagram of linear DC converter.

The second type is switch mode DC converters, which are nonlinear. Unlike the linear DC converters, the switch mode DC-DC converters consist of switches, energy storage devices like capacitors and inductors as shown in Figure 1.6. The switches are an extension of the control unit of the DC-DC converter, which regulates the energy accumulation in temporary storage devices and then feeds them into the load. MOSFETs are used as switches to improve the integration and performance of the conversion in terms of switching speed and energy loss. Depending on the temporary energy storage devices used, the switch mode DC-DC converters can be categorized into two groups: The first type consists of only capacitors as the energy storage device, the second type consists of both capacitors and inductors as energy storage devices. The first type is smaller in scale compared to the second type due to the lack of bulky inductors. The main advantage of the switch mode DC-DC converter is the possibility of achieving both up conversion and down conversion using proper controller unit implementation and topology adjustments according to the application. In addition, the switched mode DC-DC converter efficiency is higher than the linear DC converters due to lack of large resistance in series with the load. Through proper selection of device parameters and switching frequency according to the application goal, the converter can be implemented as a low cost, fully integrated module with the lightweight and small scale to satisfy the economic requirement of the market. Using temporary energy storage devices, like capacitors, together with switching mechanism minimizes the output variation due to the effect of noise and input variations. Therefore, the switch mode DC-DC converter can achieve high steady state performance. Implementing a feedback loop with control unit can improve the dynamic characteristics of the converter. Therefore, the switch mode DC-DC converters are more advanced compared to the typical linear DC-DC converters.

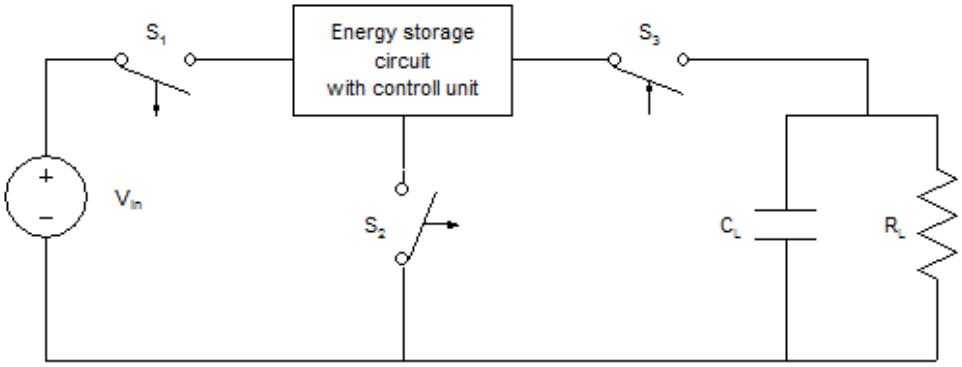

Figure 1.6. Block diagram of the switch mode DC-DC converter.

1.5 DC-DC converter efficiency

Power efficiency is one of the main characteristics of the electronic devices to evaluate the feasibility of use for the applications. In low power energy harvesting, high efficiency is necessary to minimize the energy losses and transfer the maximum power to the load. The power efficiency (η) of DC-DC converter can be expressed as,

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \times 100\%, \quad (1)$$

where P_{out} is the output power and P_{in} is the input power. The input power can be expressed as the product of source current (I_{in}) and the source voltage (V_{in}) while output power is the product of sink current (I_{out}) and sink voltage (V_{out}). The main lossy component in the linear DC-DC converter is the variable resistor. If the feedback loop current is negligible, the efficiency of the linear DC converter can be simplified as the ratio of output voltage and input voltage. Due to the buck conversion property, the efficiency is low in linear DC converter. The efficiency of the switching DC-DC converter is a function of the circuit component parameters, switching frequency, and input voltage. Because in high-speed, low-cost integrated DC-DC converter, switches are implemented with MOSFETs, and they have a finite resistance which contributes to the energy loss. The internal resistance of the inductor also plays a part in the energy loss as a function of the square of current through the inductor multiplied with the self-resistance of the inductor. The capacitor energy loss is a function of operational frequency (f), capacitance (C), and the voltage change across the capacitor (V), as,

$$P_{Cap.\ loss} = CV^2 f. \quad (2)$$

In order to achieve a good design, proper optimization is necessary with consideration of efficiency, power delivery, and circuit area. To facilitate the optimization, a good circuit model is essential. There are few research papers presented in the literature to address the design optimization of the DC-DC converter to increase the performance. In applications with low input voltage, however, the performance of the MOSFET switches decreases. Especially in ultra-low power energy harvesting applications, the output of the energy harvester is limited to at most couple of hundreds of mV, typically less than the threshold voltage of the MOSFET. As a result, most of the published research implementations and design architectures in regards to the DC-DC converters are less applicable for the low voltage operation. Even when such designs function, the efficiency is drastically small compared to the theoretical predictions or analysis. Hence, highly efficient, novel DC-DC converter topology with design optimization methodology is necessary for the ultra-low voltage sources such as small energy harvesters.

1.6 Objectives of the thesis

The goal of this work is to design a fully integrated, self-starting, highly efficient, ultra-low voltage step-up DC-DC converter with high output power capacity for energy harvesting applications. The circuit is implemented in 180 nm standard CMOS technology with only on-chip circuit components. A comprehensive list of objectives of the thesis is as follows:

- Study and recognize the main drawbacks of the existing DC-DC converter circuits.
- Implement a fully integrated oscillator design, which can self-start at the input voltage (V_{in}) of 0.2±50% to generate two out-of-phase periodic signals with amplitude $\geq 2\times V_{in}$.
- Implement a DC-DC converter based on an integrated charge pump circuit to deliver maximum output voltage and power.
- Propose and implement novel methods to model the DC-DC converter in order to analytically optimize and enhance the performance in terms of efficiency and output power. Validate the model based results with circuit simulations with extracted parasitics in UMC 180 nm process technology.
- Layout, fabricate, and validate a DC-DC converter test chip to characterize performance with different input voltage levels and load resistances. Analyze the discrepancy between simulations and measurements for further improvement of circuits and associated models.

Design of voltage regulators and maximum power point tracking (MPPT) control circuits are not within the scope of this thesis.

1.7 Thesis outline

The remaining part of the thesis is organized as follows: The basic principle of the voltage step-up DC-DC converter is described in chapter 2 including charge pump circuit techniques for integrated voltage step-up, and different types of oscillator circuits to stimulate charge-pumps. A literature review to identify advantages and drawbacks of the existing low voltage oscillators and charge pumps is also discussed in this chapter.

Chapter 3 discusses two different novel LC tank oscillator designs, and features of these oscillators. A model based analysis is presented for the working principles, oscillation frequency and power efficiency calculations. Simulation results are presented for the verification of the model.

In chapter 4, two fully integrated DC-DC converter designs are presented, which are optimized for energy harvesting applications with higher power at ultra-low input voltage levels, compared to other solutions in the literature. The detailed model based analysis is also provided to determine the variation of clock frequency with circuit component parameters. Model based power consumption analysis the DC-DC converter topology with voltage doubling LC tank is also presented in this chapter. An optimization methodology is presented for high power delivery under the constraint of design area, and the model is verified through simulation results.

Chapter 5 presents the proposed test chip design and layout of the multi-stage DC-DC converter. The comparison of the measurements, simulations, and model based analytical results is presented. Based on major deviations observed in measurements due to previously ignored parasitic effects, a re-built model with more accurate layout parameters is used for post-layout simulation results to match silicon results.

Conclusions and future work are presented in Chapter 6.

CHAPTER 2

2 BACKGROUND

2.1 Introduction

Smart low power wearable electronic systems and smart IoT applications are the current trend of new generation. Most often, the small scale batteries are the power source for such tiny circuits and dominate the volume of the package [41]. As a result, the power source (typically a battery) is a critical factor for portability and lightweight of the device. The small button cell batteries like 'Duracell DA 13 (features - 7.9 mm×5.4 mm, 290 mAh)' and 'Duracell DA 675 (features – 11.6 mm×5.4 mm, 290 mAh)' are currently used for portable micropower applications like wearable wireless medical devices. However, the individual output voltage of these small battery cells is limited to a maximum of 1.4 V, which is below the operational voltage of most micro power loads (most of the standard microcontrollers operate in a range of 1.8 V to 3.6 V) [41]. In the majority of circuit designs, the power requirement of different sub-circuits in main hardware is different and impossible to feed on the main battery without a power management unit. Use of discrete batteries for each sub-circuit is impractical as they increase the cost of product, size, and weight. Therefore, utilizing energy harvesting coupled with voltage boost up unit for direct powering or recharging the main battery is an essential need for the next generation of microelectronic portable and smart devices. The problem associated with energy harvesting is the generated low voltage at ambient conditions, which is on the order of a couple of hundreds of millivolts, and which is not sufficient to fulfill the load voltage requirement. Therefore, the harvester output voltage has to be boosted up to a certain voltage level to compensate the load power requirement. Switch mode DC-DC converters are utilized to boost low DC input into a higher level of DC voltage. The problem related to the DC-DC converter is the sharp performance degradation for the lower input voltage. The on-chip micro scale DC-DC converter circuits consist of low power MOSFETs with operating threshold voltage of couple of hundred of millivolts, but usually, the ambient energy harvester output is below the threshold voltage of the common and economical standard CMOS fabrication process, like 180 nm technology. As a result, through the evidence of previous works, self-starting, high performance, fully integrated, ultra-low voltage DC-DC converter implementation is a big challenge.

There are two types of switch mode DC-DC converters, categorized according to the energy storage element.

- Capacitive based DC-DC converters

  Capacitors are the temporary energy storage elements in capacitive based DC-DC converters. The function of these capacitors is to store and deliver charge from one stage to next stage, according to a switching mechanism. Therefore, the DC-DC converter voltage gain has a positive relationship with capacitor size and converter stages, but large capacitors cause a significant amount of energy dissipation. Large capacitors need large space on the chip, which is critical in the fully integrated process. Hence, an optimization methodology is necessary for the on-chip capacitive based DC-DC converter architecture to achieve the design goal.

- Inductive based DC-DC converters

  Inductors are the temporary energy storage elements in inductive based DC-DC converters. They also boost up the DC supply by integrated switching mechanism. Advanced inductor based DC-DC converters consist of many capacitors and inductors to store energy in the form of charge and magnetic field, respectively. The essential large area for the inductors is the main disadvantage of inductive based DC-DC converter architecture. For the best DC output with minimum ripple, the operational switching frequency is necessary to be at least in MHz range. As a result, inductance should be within the range of a couple of tens of nH while capacitance in pF range. Perhaps the connectors of the discrete inductors generate significant capacitance and inductance in Pico and Nanoscale, respectively. Due to the advances in integration, tolerance in component parameters, cost, area, and lightweight, the on-chip inductors are more reliable for the ultra-low voltage DC-DC converter design.

Integration of inductors and capacitors are critical for the feasibility of on-chip DC-DC converter design in micro-scale area with significant cost saving for the wearable micro power electronic applications. Unlike RF integrated inductors, the inductance of the DC-DC converters should be much larger and have lower self-resistance. For the best performance, the parasitic capacitance and the inductance of on-chip inductors and capacitors should be minimum. As a result, designing on-chip inductors and capacitors for the DC-DC converter is a big challenge.

2.2 DC-DC converter fundamentals

Figure 2.1 illustrates the block diagram of a conventional switched mode DC-DC converter for low voltage energy harvesting applications. The output voltage of the energy harvester is varied with the ambient condition. Therefore, the energy storage capacitor is necessary to prevent the voltage ripple at the input terminal of the DC-DC converter. The DC-DC converter consists of two sub-circuits: Oscillator circuit and charge pump circuit. The oscillator circuit generates the necessary clock signals to drive the switching MOSFETs. The clock signal can work as a charge source for the energy storage elements. The advanced oscillators are feasible with high gain amplitude oscillations. They boost up the DC-DC converter output and achieve high efficiency with fewer circuit components. The DC-DC converter output is parallel connected with the load resistance and energy storage devices such as small rechargeable batteries or supercapacitors. The energy storage device is necessary to secure the power requirement of the load in case of the failure of energy harvester in unexpected critical environmental condition. Once the load is inactive, the energy storage device will charge and store energy for compensating power failure.

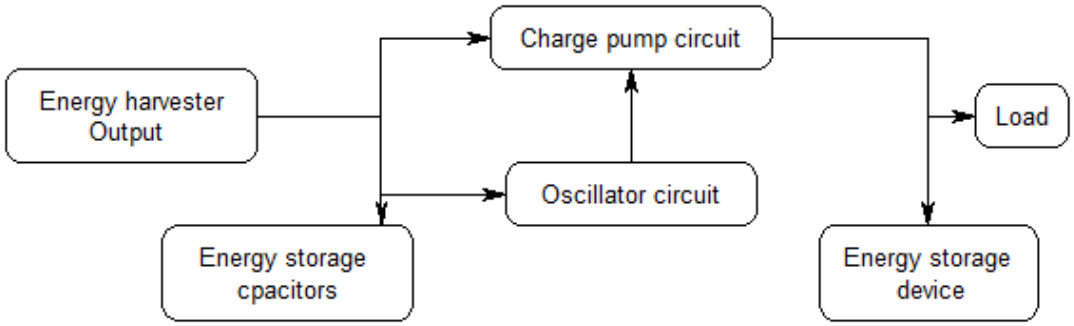

Figure 2.1. The block diagram of a switch mode DC-DC converter for energy harvesting applications.

Power efficiency, minimum start-up voltage, high power output, response to input voltage variation, output voltage ripple, and area are the basis for evaluating the performances of DC-DC converter topology. In general, the efficiency and on-die area are the most important parameters of the on-chip micro power DC-DC converters. This is because a highly efficient design has minimum power dissipation and maximum load power for a given input. If the power dissipation is high, even with sufficient output power, the design should employ a cooling system to prevent heating. The area downscaling increases the feasibility of DC-DC converter usage in applications like body area network and IoT.

The switch mode DC-DC converter consists of energy storage devices and switching mechanism for energy accumulation as illustrated in Figure 2.2. Once S1 and S2 are grounded and connected to the source voltage, respectively, the charge will flow through the energy storage device and accumulate energy on it. Most often, fully integrated or partially integrated capacitors are the temporary energy storage elements for the DC-DC converter. As a result, there is always an energy loss, which is proportional to the switching frequency of the DC-DC converter. The opposite state of S1 and S2 switches make the series connection of source, energy storage device, and load capacitor as depicted in Figure 2.3. In the case of the capacitor as the temporary storage device, neglecting the losses, the load capacitance can be charged to Vout = 2×Vin. The high-speed switching is necessary for DC voltage at the output node. Therefore, switches are replaced from MOSFETs for higher performance of the DC-DC converter. The switches are driven by a pair of clock signals with optimal frequency for minimum ripple at the output.

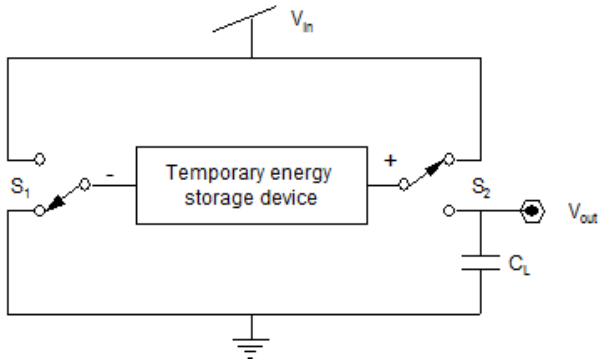

Figure 2.2. Energy accumulation of the energy storage device in the DC-DC converter.

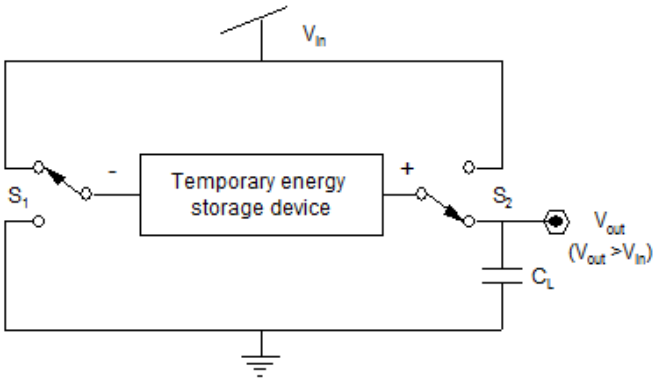

Figure 2.3. The energy transferring from energy storage device to load capacitor of the DC-DC converter.

2.3 Switch mode charge pump topologies for DC-DC converter design

The development of the microelectronic architecture with integrated CMOS design has increased the attention to different charge pump topologies to enhance the performance in ultra-low voltage applications. The enhanced versions of basic charge pump topologies are used for the DC-DC converter applications. The schematic of the Cockcroft-Walton charge pump circuit, which is one of the primary charge pump circuits, consists of capacitors and switches as shown in Figure 2.4. Once S_1 and S_2 switches are connected to ground and node 2, respectively, C_1 and C_4 will accumulate charge from the source voltage (V_{in}). When the switches change the state, C_2 and C_4 will be parallel to each other; each of them will charge to V_{in} /2. Then, S_1 and S_2 switches are connected to ground and node 2, respectively, C_4 and C_5 will charge to Vin and V_{in}/4 respectively. Finally, V_{out} will reach $3V_{in}$ after several switching states if all the charge pump capacitors are identical. This charge pump topology is low in efficiency at a given load condition, compared to the alternative charge pump topologies. The charge pump performance is adversely proportional to the charge pump stages.

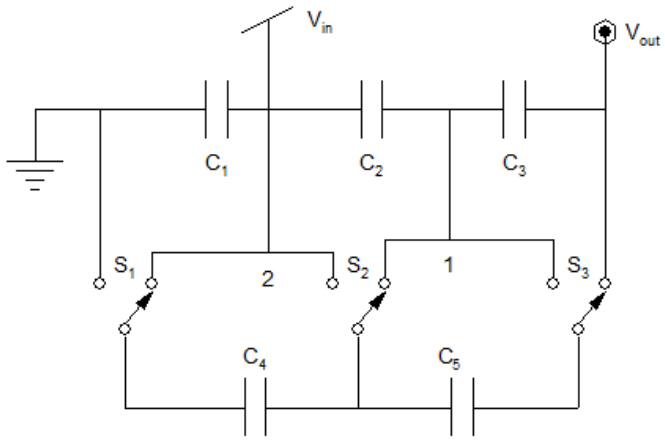

Figure 2.4. Cockcroft-Walton charge pump.

Two phase cascade voltage doubling charge pump is another basic charge pump which consists of dual capacitors and switches in each stage as shown in Figure 2.5. The configuration of S_1 ground and S_2 source connection allows accumulating energy on C_1 in the form of charge. The opposite connection of switches makes the series array of the source, C_1, and C_2. Therefore, C_2 will reach $2V_{in}$ for the ideal capacitors. Similarly, fully charge C_2 is the source of C_3 capacitor. C_3 will charge to V_{in} (if C_2= C_3) when S_3 is grounded and S_2 and S_4 are connected to V_{in} and C_2, respectively. Opposite switching states allow C_3 in series with C_L, C_1, and V_{in} to achieve $V_{out} = 4V_{in}$. For the ideal circuit components, the peak voltage at S_2 and V_{out}

is $2\times V_{in}$ and $4\times V_{in}$, respectively. Therefore, the voltage gain of the N stage two-phase cascade voltage doubling charge pump is 2N. In CMOS process, switches are replaced with MOSFETs that are controlled for high-speed switching to achieve minimum ripple at output nodes. The leakage current of the charge pump is the main drawback of the design. The parasitic capacitance also contributes to decreasing the voltage gain of the topology.

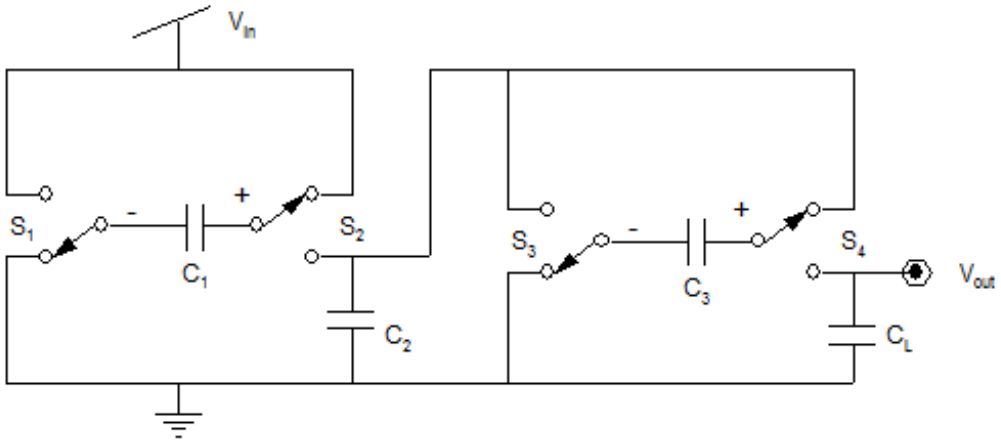

Figure 2.5. Two-stage of two phase cascade voltage doubler charge pump circuit [42].

Makowski proposed a dual phase charge pump topology; each stage consisting of a single capacitor and three switches as illustrated in Figure 2.6. The N stage charge pump is composed of N+1 capacitors and 3N+1 switches. S_2, S_3, S_4, and S_7 switches are operated synchronously while S_1, S_5, and S_6 are opposite. Once S_2, S_3 are closed, and S_1, S_5 are open, C_1 capacitor accumulates energy from the source and reaches V_{in}. Then, S_2, S_3 open and S_1 turn-off to achieve $2V_{in}$ at the output of the first stage. Simultaneously S_5, S_6 turn-off, and S_4 will open. Therefore, first stage output works as a source for the second stage. Similarly, two switches in each stage have the same operation while others switch in opposite direction. Hence, an antiphase dual clock system can be replaced in CMOS architecture to drive the MOSFET switches. The maximum voltage gain of the N stage of Makowski charge pump is N+1. Makowski topology requires the least number of capacitors to achieve the given voltage gain compared to the other existing topologies [43]. The charge pump stages for a given voltage gain can be calculated using the Fibonacci number described in [43], but determination of the switching frequency, capacitor sizes, and switched MOSFET parameters for the maximum efficiency is critical. Despite the high voltage gain, the Makowsky topology has low efficiency compared to the Dickson charge pump circuit [44].

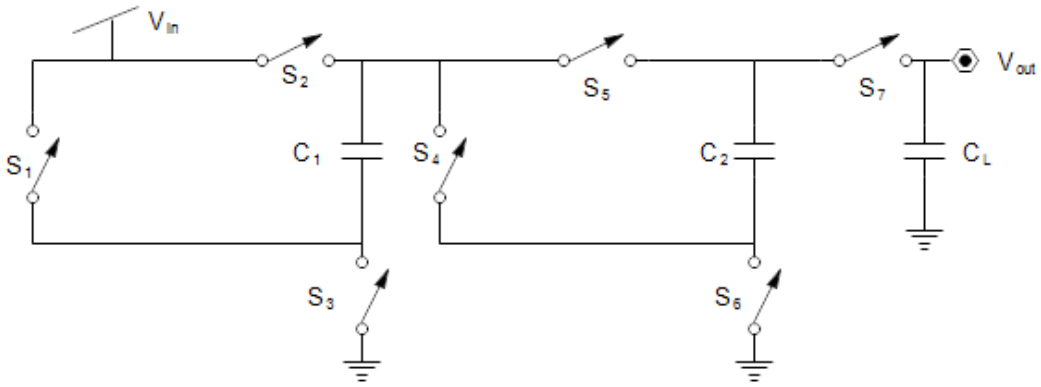

Figure 2.6. Makowski charge pump topology.

The three-stage of the voltage step-up ladder charge pumps circuit consists of 9 switches and three capacitors as shown in Figure 2.7. The switches S_2, S_4, and S_7 are synchronized, and are switched off-phase with the other switches. Once S_2, S_4, and S_7 open, then C_1 and C_2 capacitors will charge from the source voltage. When S_2, S_4, and S_7 are off, the flying capacitors are in series with each other and V_{in}. Therefore, the output is the summation of the voltage across all flying capacitors and the source. The N stage ladder circuit can achieve a maximum gain of 2N at open circuit condition.

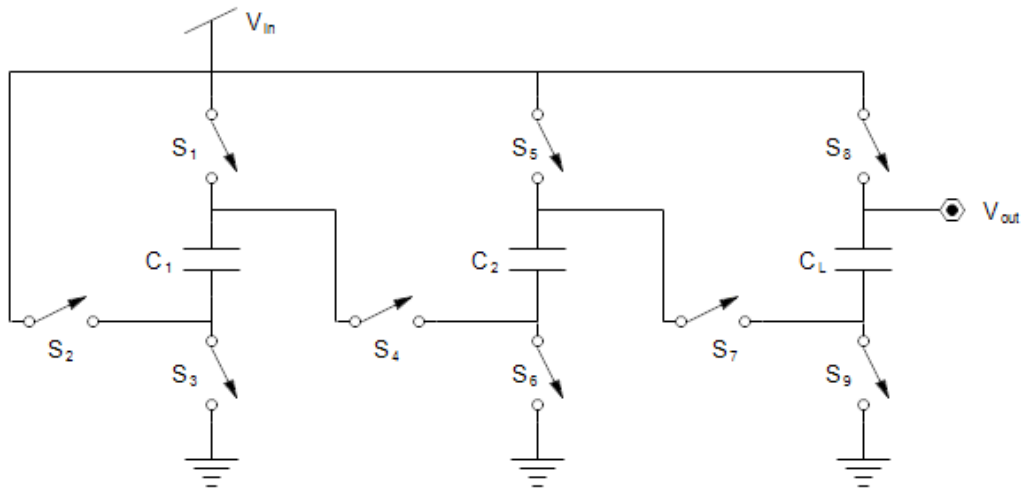

Figure 2.7. The voltage step-up ladder charge pump architecture [45].

Unlike the other existing switch mode charge pump topologies, the dual phase cascade DC output voltage double charge pump has the minimum ripple output at each stage. Each stage of the circuit consists of six switches and two capacitors to maintain the DC output and voltage gain at each stage.

Two-stage of dual phase cascade DC output charge pump topology has four output switches as depicted in Figure 2.8. The operation of the S_1 switch is opposed to the S_2 while S_1 and S_2 are synchronous with S_4 and S_3 respectively. Once S_1 and S_2 are open and closed correspondingly, S_6 and S_5 will connect to ground and V_{in} respectively. Therefore, the charge will flow through the C_2 capacitor and accumulate energy on it. Then switch S_1 will be turned off while S_2 is open. At the same time, the grounded S_5 will allow the accumulation of charges on the C_1 capacitor. Simultaneously, the voltage at the node-2 will reach to $2V_{in}$ due to the series connection of fully charged C_2 and V_{in}. At this time the switch S_3 will turn-on while S_4 is turned-off to achieve $2V_{in}$ at the output (node-3) of the first stage. At the opposite configuration of the switches, the series connection of Vin and fully charged C_1 allows the $2V_{in}$ at the output of the first stage. Simultaneously, C_2 will start to accumulate energy on it. As a result, the node-3 is at DC voltage throughout the operation of the switching mechanism. The output switches in each stage reduce the leakage current and back-flow current in the system. Therefore, the charge deliverability and efficiency are higher than the other charge pump topologies.

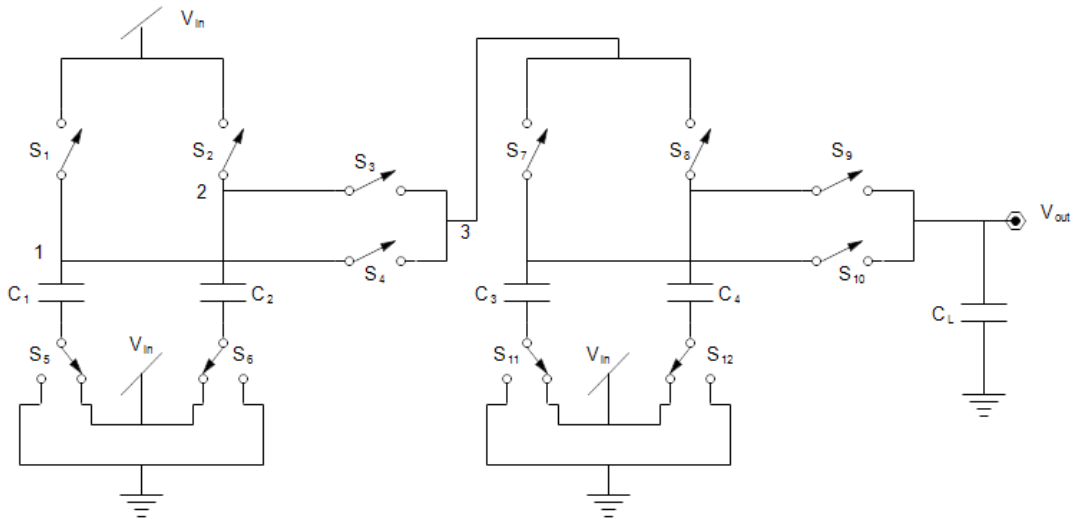

Figure 2.8. Two-stage of dual phase cascade DC output voltage doubler charge pump circuit.

2.4 CMOS charge pump circuits for DC-DC converter applications

CMOS charge pump circuits are used for low power memory devices and analog electronic devices like flash memories, DRAM, EEPROM, etc. [46]. Cockcroft and Walton have proposed the first charge pump topology for high power electronic applications [47]. This design consists of mechanical switches to operate the charge transferring between corresponding capacitors on each stage. In 1976, Dickson proposed an advanced version of

charge pump design to overcome the problem associated with Cockcroft-Walton type charge pump topology [48]. The diode connected clock mechanism is used in Dickson charge pump to prevent the back flow. The 3-stage Dickson charge pump circuit consists of 4-diodes and 6-capacitors as illustrated in Figure 2.9. CLK_1, CLK_2 refer to the clock signals which are identical and out of phase with each other. C_1, C_2, and C_3 capacitors are charged and discharged in accordance with the clock operation. Since the diode current is unidirectional, each capacitor is charged by the previous stage capacitor except the first stage capacitors, to deliver charge from stage to next stage. Therefore, any higher stage voltage is larger than the previous stage voltage.

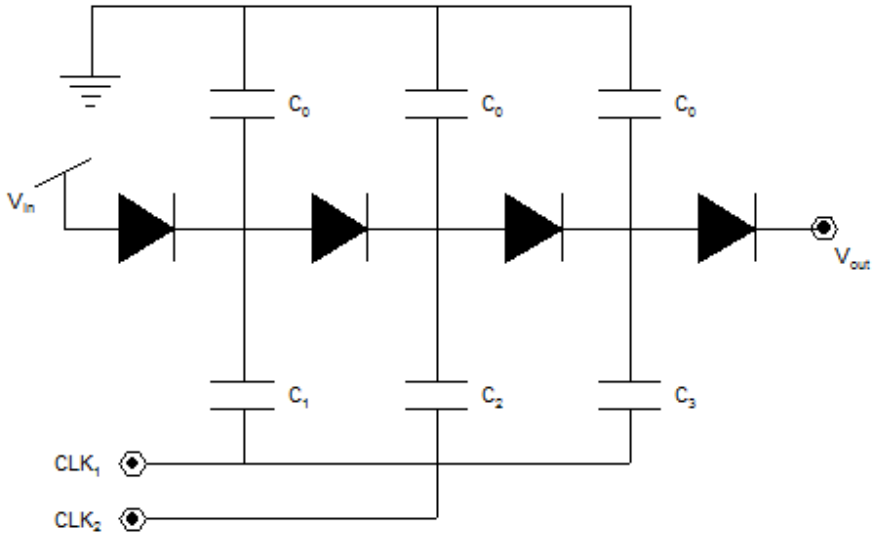

Figure 2.9. Dickson charge pump circuit with diode switches.

The N stage diode connected Dickson charge pump output is given by:

$$V_{out} = V_{in} + \frac{C}{C+C_0}.N.V_{CLK} - (N+1)V_D, \quad (3)$$

where V_{out}, V_{in}, C, C_0, N, V_{CLK}, and V_D respectively refer to charge pump output voltage, charge pump source voltage, charge pump capacitance ($C = C_1 = C_2 = C_3$), stray capacitance, number of stages, clock amplitude voltage, and conducting voltage drop of the diode. The forward bias voltage drop in each stage is the main drawback of this diode connected charge pump structure. The stray capacitors are adversely affecting the voltage gain of the charge pump circuit. However, larger charge pump capacitors are necessary for higher voltage gain. Due to the forward bias voltage drop and the high leakage current, the diode connected Dickson charge pump model is not feasible for ultra-low voltage applications. The replacement of diodes and stray capacitors from MOSFETs and parasitic capacitance of each junction utilize the

feasibility of ultra-low voltage application [49]. In standard CMOS technology, the threshold voltage of the MOSFETs are much smaller than the diode forward bias voltage and within the ultra-low voltage range depending on the advance of the technology. Figure 2.10 illustrates the NMOS implementation of the Dickson charge pump topology for microelectronic applications. The output of the NMOS connected Dickson topology is given by:

$$V_{out} = V_{in} + \frac{C}{C + C_S}.N.V_{CLK} - (N+1)V_t, \tag{4}$$

where Vt is the threshold voltage of the NMOS and C_S is the parasitic capacitance of each stage formulated by the clock coupling capacitor and NMOSs parasitic at the junction. The threshold voltage of the standard CMOS MOSFET is [50]:

$$V_t = V_{t0} + \gamma\sqrt{2.|\varphi_F| + V_{SB}} - \sqrt{2.|\varphi_F|}, \tag{5}$$

where, V_{t0}, φ_F, V_{SB}, and γ, respectively refer to the intrinsic threshold voltage, surface potential, source-bulk potential difference, and the body effect coefficient. Typically, in low-cost CMOS process, the body of the NMOS is grounded. The source-bulk voltage increases the threshold voltage and voltage drop at each stage of the charge pump. The leakage current is subjected to the significant impact of the voltage gain and efficiency of the charge pump. As a result, the Dickson's charge pump topology is not suitable for the ultra-low voltage applications.

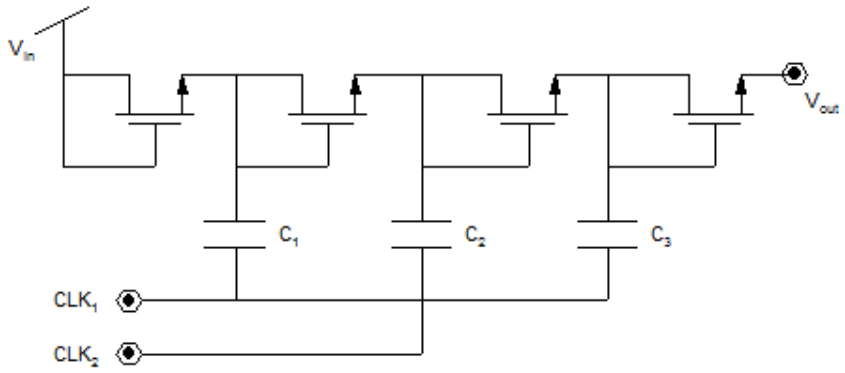

Figure 2.10. Dickson charge pump with NMOS switches.

As a first integrated charge pump topology, an extensive research attention is given to improving the performance of Dickson charge pump architecture. The voltage doubling and tripling charge pump circuits presented in [51] analyze the dynamic models of the Dickson charge pump topology taking the parasitic effects into account. The simple dynamic model for the N-stage Dickson charge pump is presented in [52] to implement a mathematical analysis to estimate the required area for the given number of stages. The power consumption during

boosting of the Dickson charge pump is analyzed in [53] along with the optimization of the number of stages to achieve the minimum rising time. Dickson charge pump power consumption optimization methodology and validated results in CMOS 350 nm CMOS process are presented in [54]. Area optimization of the Dickson topology to achieve the given performance has been presented in [55]. Authors in [56] and [57] presented the theoretical analysis of the switched capacitors used in Dickson charge pump for the DC-DC converter applications and frequency optimization methodology for a given load condition to maximize the performance of the dual phase Dickson topology. However, the majority of these Dickson charge pump improvements are limited to the charge pump applications operating beyond the ultra-low voltage level. Therefore, different switching mechanisms and structured switched based charge pump topologies are proposed in recent decades to overcome the issues of the Dickson charge pump architecture.

Several developed switch mode CMOS charge pump circuits are presented to enhance the low voltage performance by eliminating the limitations of the threshold voltage. Wu and Chang reported the four-stage charge pump [58] known as 'NCP-2 charge pump'. The main advantage of this circuit is the lack of threshold voltage effect during the charge transfer process. The two stages of the NCP-2 charge pump circuit consisted of NMOSs and capacitors as shown in Figure 2.11. The N stage of the NCP-2 charge pump consists of 3N +2 NMOS, N number of PMOS and N+1 capacitors excluding load capacitance. The CLK_1 and CLK_2 are two identical out of phase signals for the clock requirement of the circuit. Once CLK_1 is low, C_1 will charge to V_{in} and voltage at node 1 is at source voltage. When CLK_1 is high, the node 1 reaches to $2V_{in}$ due to the series connection of C_1 and CLK_1. Therefore, the node 1 is at V_{in} and $2V_{in}$ during the full cycle of the clock generation while node 2 oscillates between $2V_{in}$ and $3V_{in}$ during the entire period of the clock signal. Since the maximum voltage difference between two consecutive stages is $2V_{in}$, circuit MOSFETs suffer the high voltage overstress on the gate oxide [59]. Besides, the NCP-2 charge pump NMOSs are lower the voltage gain due to the body effect issue as NMOSs work as diode connected MOSFETs. However, the large output voltage ripple and the energy losses in each stage are the disadvantages of NCP-2 charge pump for ultra-low voltage applications.

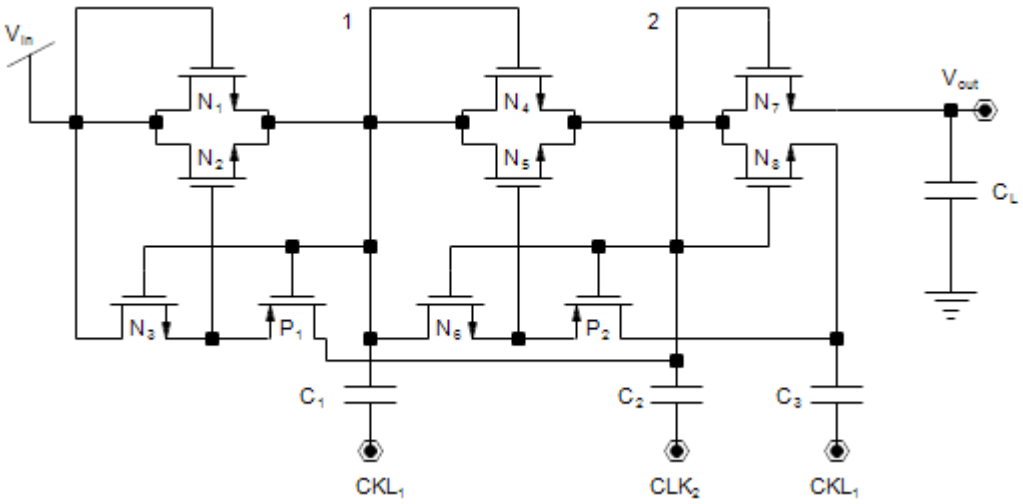

Figure 2.11. A two stage NCP-2 charge pump.

The dual-charge transfer branch charge pump presented in [59] solved the threshold voltage drop issue with the charge pump MOSFETs. The main advantage of this design is completely on and off MOSFETs operation. These fully functioning MOSFETs minimize the leakage current on the system. The two-stage charge pump circuit is shown in Figure 2.12. Each stage of the charge pump consists of two cross-coupled NMOS pair and PMOS pair with two capacitors. The two antiphase clock signals drive the charge pump switches to accumulate the charge on capacitors and transfer to the next stage with high efficiency. Once CLK_1 is low and CLK_2 is high, N_1 is on while N_2 and P_1 are off, C_1 will accumulate charge and reach to source voltage. The opposite configuration of the clock signals allows to switch on N_2 when N_1 and P_2 are switched off. Therefore, the series connection of source and C_2 allows accumulating energy on C_2 capacitor. Simultaneously, node 1 achieves $2V_{in}$ thanks to the series connection of charged C_1 and clock signal. Simultaneously, P_1 is on and allows to transfer the charges to the second stage. Node 2 voltage oscillates in between V_{in} and $2V_{in}$ during the full period of the oscillation and opposes to the node 4. However, the maximum voltage difference between two consecutive stages is $2V_{in}$. Therefore, the MOSFETs suffer from the high voltage overstress on the gate oxide.

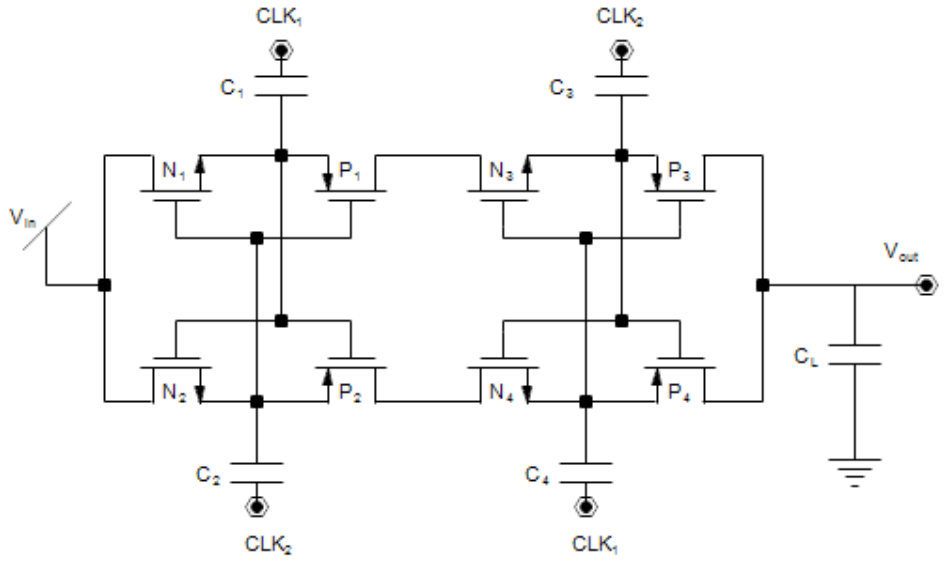

Figure 2.12. Dual charge transfer branch MOSFET cross connected charge pump.

To achieve better voltage gain and low start-up voltage Bhalerao and his research group [46], [59] presented the enhanced charge pump for minimizing the voltage ripple at each stage output. As a fact of better performance, several strategies are presented in the literature to enhance the performances of the MOSFET cross connected charge pump design. The switched body bias mechanism and adaptive dead-time techniques are presented in [60] to enhance the efficiency of the charge pump. However, the added circuits consumed more power and reduced the voltage gain of the charge pump. Apart from that, the adaptive dead-time circuit and body-biasing circuit occupied a large area, which is critical in fully integrated circuit design. Chen and his research group [61] presented forward body biasing technique to improve the efficiency of low voltage charge pump circuit, but the power converter efficiency is poor. Additionally, the NMOS body biasing fabrication process is expensive.

2.5 Oscillator circuit for the DC-DC converter design

Oscillator circuits generate a periodic time varying signal (clock signal), which is essential for the charge pump applications in DC-DC converter designs. In microelectronic CMOS process, charge pump switches are replaced by the MOSFETs switches. The oscillator is the controlling unit of these MOSFETs, but also works as a source for the flying capacitors. An efficient, low phase noise, and high gain clock system is necessary for the proper operation of the charge pump. Most high-frequency oscillators can be viewed as a feedback loop with frequency selective circuit as shown in Figure 2.13.

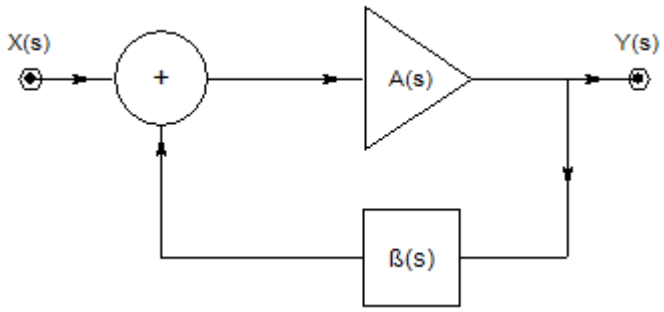

Figure 2.13. Basic block diagram of an oscillator [62].

The closed loop transfer function (*Y(s) / X(s)*) of the oscillator is given by,

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1-[A(s).\beta(s)]}, \tag{6}$$

where A(s) refers to amplification stage transfer function and β(s) refers to feedback stage transfer function. Since there is no output for the zero input of the oscillator, $A(s).\beta(s) = 1$ for $X(s) = 0$. For constant amplitude and frequency oscillations, the closed loop transfer function should be a purely real number. Furthermore, the phase shift in the loop should be an integer multiplication of 2π. These two necessary conditions are known as Barkhausen stability criteria. There are two types of oscillators according to the shape of the oscillations; Square wave oscillators and sine wave oscillators. The ring oscillator is a popular CMOS square-wave oscillator used for DC-DC clock generator circuit. LC tank and RC tank based oscillators are the commonly used sine wave generators in microelectronic applications. Unlike the CMOS square wave oscillators, the sine wave generators require a large on-die area.

2.5.1 Ring oscillator circuit

Ring oscillators consist of an odd number of inverters. The input and output terminals are short-circuited to generate the necessary feedback loop for continuous oscillation. The inverter is the delay cell of the CMOS ring oscillator circuit. A large number of inverter cells are necessary for low-frequency operation. Due to the odd number of inverters, the oscillator first stage inverter input is in the same phase with the last inverter output. As a result, the phase shift of the feedback loop is zero and follow the Barkhausen criteria. Each stage of the CMOS ring oscillator consists of N-channel MOSFET and P-channel MOSFET as illustrated in Figure 2.14. The ideal amplitude of the oscillator is V_{in}, which is the inverter output.

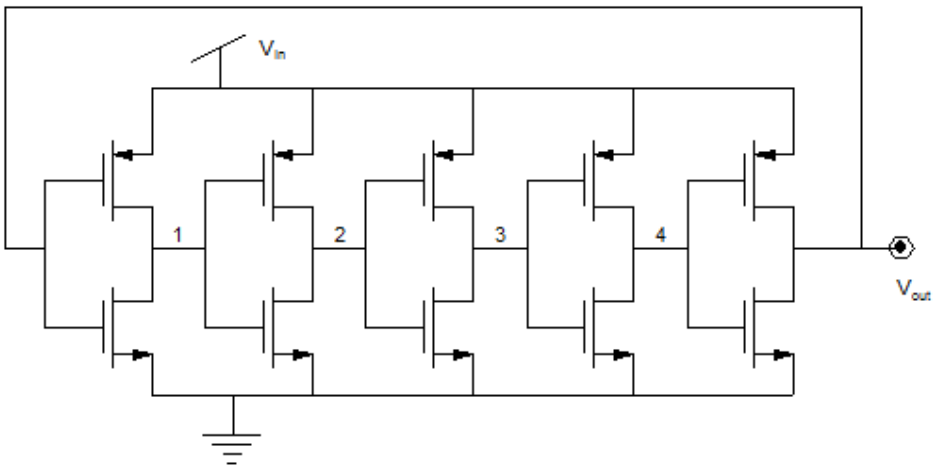

Figure 2.14. A five stage CMOS ring oscillator.

An oscillation frequency is a function of the number of inverter cells and the delay of a unit cell. If the delay of the single inverter is t_d (summation of the low to high and high to low propagation time), and total delay for the N stages is $N.t_d$. The single clock cycle consists of two half cycles. Therefore, oscillation period is given by $2.N.t_d$. Hence, the oscillation frequency is,

$$f = \frac{1}{2.N.t_d}. \tag{7}$$

According to the frequency equation, the number of stages is inversely proportional to the frequency. Therefore, the high-frequency ring oscillators occupy less circuit area due to the small MOSFETs. As a result, the majority of existing DC-DC converter circuits [63], [64], [57] use ring oscillators as the clock generator circuit. However, there are several disadvantages associated with the ring oscillators regarding the fact that:

1. The clock amplitude is limited by the source voltage;
2. Oscillation failure at low voltage operation (below the CMOS threshold voltage),
3. Frequency is inversely proportional and varies significantly with the oscillator delay cells across environmental conditions,
4. The array of buffer circuits is necessary for dual phase clock signal applications.

The drastic reduction of oscillator performance deteriorates the use of ring oscillator for the ultra-low voltage DC-DC converter applications. As an alternative, the CMOS inverter delay cells in ring oscillator architecture can be replaced with differential delay stages as shown in Figure 2.15. An odd number of oscillators gives the swap output feedback loop. These types of differential oscillators are known as source coupled logic (SCL) based oscillators.

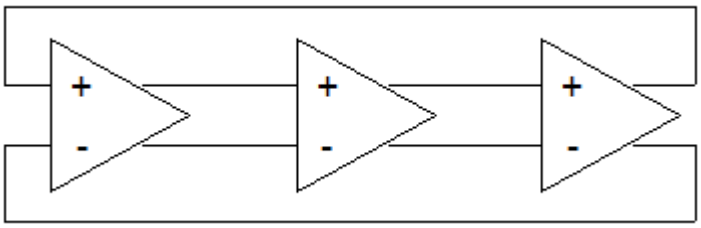

Figure 2.15. Differential delay cell ring oscillator.

There are several types of differential cells presented in the literature for the ring oscillator applications. A conventional CMOS SCL differential cell is composed of NMOS source coupled differentail pair as shown in Figure 2.16 [65].

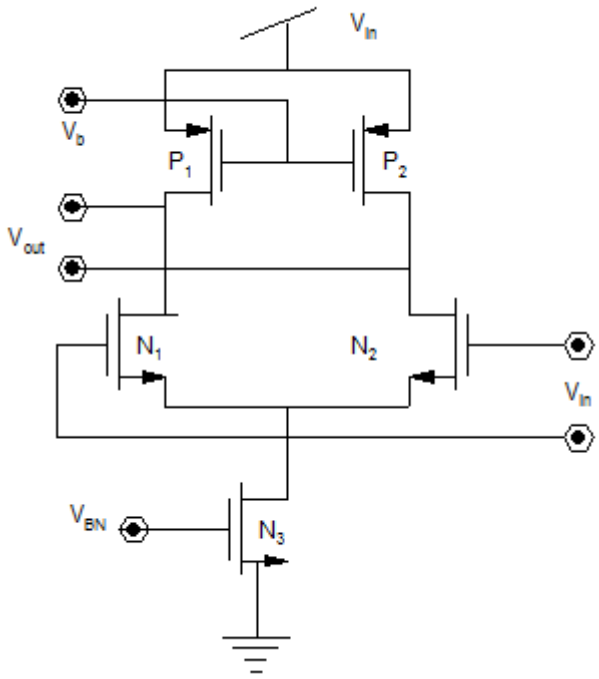

Figure 2.16. A conventional SCL differential cell.

The P-type MOSFETs function as load resistors with a suitable bias voltage (V_b) to control the branch current which is proportional to the frequency of the oscillator. Since the differential cells work in the current domain, the high-speed operation allows oscillating in the high-frequency range. However, the differential delay cell is complex to design, requires large area due to five MOSFETs, and requires bias voltage, which are the main drawbacks of this design. Source coupled logic subthreshold ring oscillators are often utilized for ultra-low voltage applications due to their advantages in regards to the following:

1. The clock signal is less sensitive to the source voltage ripple;
2. Low noise immunity at high-frequency operation,
3. Can use even or odd number of delay cells,
4. Possible to operate at subthreshold voltage.

The peak oscillation amplitude is equal to the oscillator source voltage. In ultra-low voltage applications, the ring oscillator does not function as an amplitude boost circuit. Hence, the clock amplitude is limited to the source voltage and may not be able to drive the charge pump MOSFETs. For example, the typical source coupled logic subthreshold ring oscillator fails to oscillate at a low voltage such as 0.1 V, which is below the threshold voltage of the 180 nm CMOS process. In addition, a subthreshold ring oscillator has a limited current drive, which means its current output has to be enhanced through a power-wasting buffer before it can effectively drive a charge pump.

2.6 LC tank oscillators

LC tank oscillators are composed of one or more inductors and capacitors to sustain continuous oscillations through resonant operation. In single port paradigm, the oscillator can be represented as two one-port networks interconnected as a single port network as shown in Figure 2.17 [62]. The L_p, $C_{p,}$ and R_p are the ideal inductance, ideal capacitance and parallel resistance, which represent the real losses of the tank. For the continuous oscillations, the real losses (real part of the resonator impedance = R_p) should be compensated from the active network.

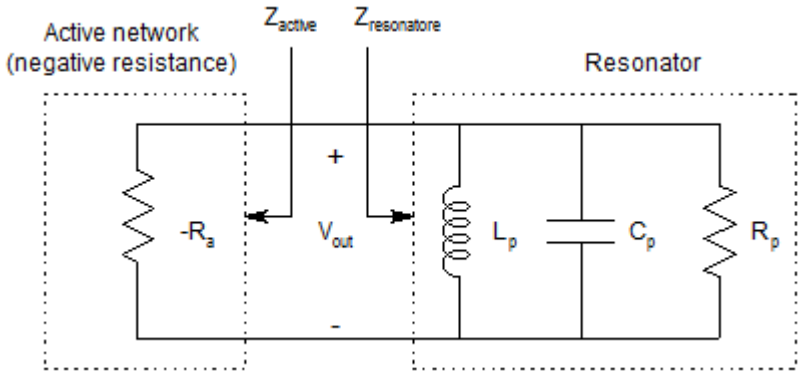

Figure 2.17. An oscillator as a two port network.

The resonator impedance is,

$$Z_{resonator} = \frac{\omega^2 L^2 R}{R^2(1-\omega^2 LC)^2 + \omega^2 L^2} + j\left[\frac{\omega L R^3(1-\omega^2 LC)}{R^2(1-\omega^2 LC)^2 + \omega^2 L^2}\right]. \quad (8)$$

At resonance, the resonator impedance should be a real number. Therefore, the resonant frequency f_0 is given by,

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \quad (9)$$

and average power loss of the LC tank is given by,

$$P_0 = \frac{V_p^2}{2R_p}, \quad (10)$$

where V_p is the peak amplitude of the oscillation. However, in practice, there are some energy losses due to the parasitic capacitance, parasitic resistance and parasitic inductance of the circuit components and connection terminals. Large inductors and capacitors decrease the frequency of the oscillator as in equation (9). However, required switching frequency of the charge pump MOSFETs is above several hundreds of MHz for the continuous charge delivery with minimum ripple at the output. Therefore, CMOS on-chip capacitors with pF range and integrated inductors with nH range can feasibly be employed for the LC tank oscillator circuit. In CMOS technology, the essential negative resistance of the active network is implemented using the cross-coupled NMOS or PMOS pair according to the current mirror principle.

The recent development in CMOS integrated spiral inductor technology reveals the feasibility of fully integrated LC tank based oscillator architecture. There are many existing LC tank topologies feasible for the DC-DC converter applications. The scheme of the PMOS monolithic LC tank based VCO consists of cross coupled PMOS pair as depicted in Figure 2.18 [66]. A 0.48 pF capacitance (C_L) and 2.4 nH inductance (L_1) yields 2.4 GHz oscillation frequency and -105 dBc/Hz phase noise in 180 CMOS standard process. The DC power consumption of the design is 13.5 mW for 1.5 V input voltage (V_{in}). The oscillator can achieve a frequency tuning range of 90 MHz thanks to the variation in frequency control voltage V_C. The cross-coupled PMOS pair (M_3 and M_4) provide the necessary negative resistance to compensate the real loss of the oscillator. The differential output with anti-phase two sinusoidal oscillation is the main advantage of this oscillator design for the DC-DC applications. However, the oscillations are not sustained in the ultra-low voltage applications due to the threshold voltage of the PMOS. In addition, the oscillation amplitude is limited to unit gain, which limits the delivered current.

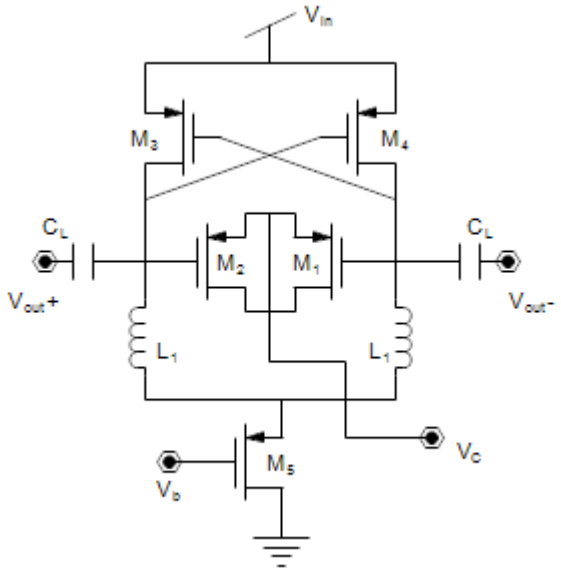

Figure 2.18. PMOS LC tank based VCO [66].

The LC tank base oscillator with both NMOS and PMOS cross-coupled pair was presented in [67] to operate around 1 V source voltage and achieve sinusoidal differential oscillations with 1.56 GHz frequency and low jitter. The scheme of the oscillator is shown in Figure 2.19. The main advantage of this design is feasibility to drive the load requirement of anti-phase dual phase signals without buffer circuits. However, the limited output current and the failure to operate at ultra-low voltage level are the disadvantages of the circuit.

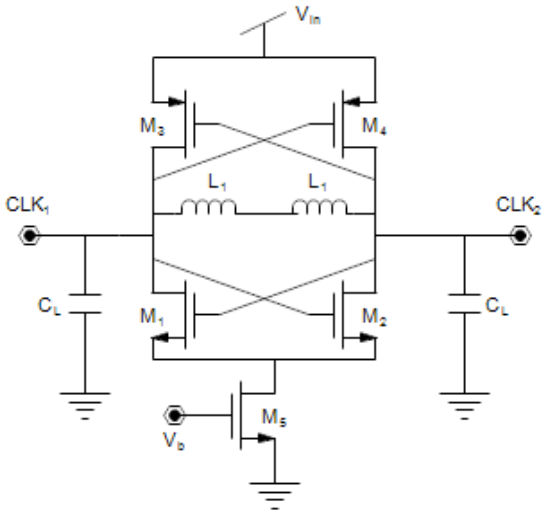

Figure 2.19. Differential complementary oscillator with cross coupled NMOS and PMOS pair.

K. Kwok and H. C. Luong [68] presented a transformer feedback voltage control oscillator in standard CMOS process for ultra-low voltage operation. The oscillator is composed of four

inductors, and a cross-coupled NMOS pair as shown in Figure 2.20. The oscillator can achieve -128.6 dBc/Hz phase noise at 1 MHz frequency offset for the center frequency of 1.4 GHz and self-starting oscillations voltage as low as 0.35 V in 180 nm CMOS process. Hence, the main advantage of the design is the capability to sustain oscillation under the threshold voltage of the CMOS technology. The implemented coupling technique provides voltage doubling, which is an advantage for the application in ultra-low voltage DC-DC converter. However, the required additional area for the four integrated inductors is a disadvantage for the wearable microelectronic applications.

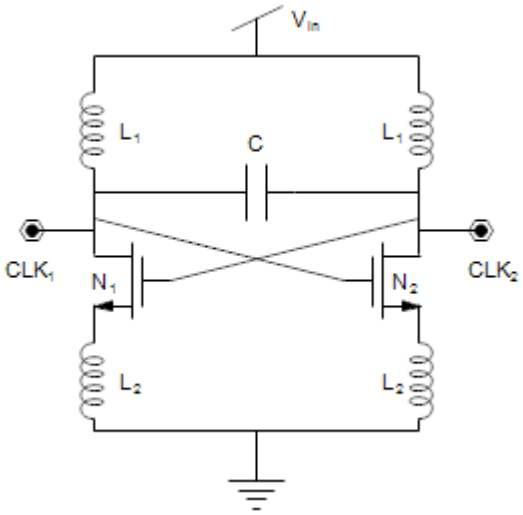

Figure 2.20. Transformer feedback VCO.

Few publications presented performance enhancing techniques for the transformer feedback LC tank based oscillator architecture. For example, Hsieh and Lu [69] introduced capacitive feedback and body-biasing techniques to improve the performance of transformer feedback VCO. The employment of the capacitive feedback system enhances the oscillator amplitude gain. Frequency tuning capability is an advanced option in this design. The increase in the size of the capacitors leads to increasing the power consumption drastically affected by the efficiency of the application. The extremely high-frequency transformer feedback VCO presented in [70] can achieve 24 GHz at 0.38 V input and -96 dBc/Hz phase noise at 1MHz offset. The implemented four capacitors and added two MOSFETs lead to an increased power consumption and the output amplitude. Difficulty in feeding the control voltage discourages the use of this design for the applications such as DC-DC converters for the micropower harvesting.

Perhaps, most of the LC tank oscillators presented in the literature suffer from low oscillation purity at ultra-low voltage operation. Minimum startup voltage is above the threshold level of

the MOSFETs, and significant power consumption exists due to capacitor and inductor losses. To improve the performance of the LC resonator architecture, a forward body bias technique is introduced in [69], [71], and [72] together with capacitive feedback. Techniques such as current reuse with bottom series coupling, and VCO core current control are utilized to improve the LC tank performance in terms of amplitude gain, phase noise and low power consumption at low voltage operation. Despite the filtering techniques proposed in [73] to enhance the phase noise performance, the added MOSFETs contribute to power dissipation and reduce the voltage gain. Even with the large area requirement of the on-chip spiral inductor design, the LC tank based oscillators are often used for the ultra-low voltage DC-DC converter applications due to its advantages in regards to:

1. The ability of sustain oscillations even below the threshold voltage of the CMOS technology;
2. Amplitude amplification,
3. Good charge drivability,
4. Dual phase oscillations,
5. Lack of buffer circuits.

In this thesis, to achieve high performance at low input voltage, the LC tank based oscillator topology is implemented. The LC tank half-circuit model and analysis with charge pump topology to generate the clock signal for the DC-DC converter circuit design in CMOS 180 nm standard process is also presented.

2.7 DC-DC converter modeling and optimization

High performance DC-DC converter circuits could benefit from maximum energy transfer at critical conditions in energy harvesting applications. Minimum chip area is necessary for microelectronic wearable applications like implantable sensors. Early charge pump based DC-DC converters prioritized high-frequency clock signaling to achieve higher performance with lower die area [74]. Practically, the output current decreases beyond a critical switching frequency due to partial charging and discharging of the capacitors in the DC-DC converter [75]. The implementation of LC tank based oscillators to stimulate charge pumps potentially requires dedication of a higher percentage of the die area to the oscillator design [76]. Meanwhile, the larger charge pump capacitors increase the charge storage capability, which causes increase in the output power [77]. The bulky capacitors lead to enlarging the chip area which is critical in DC-DC converter applications. As a result, it is necessary to obtain the circuit parameters which provide the maximum efficiency under the constraints of the given application. However, the power efficiency of most existing fully integrated ultra-low voltage

DC-DC converters has been less than 25% when they are used with step-up conversion applications at low load conditions [78], [79]. An optimization method to obtain a higher performance in such a fully integrated LC tank based DC-DC converter system with ultra-low voltage input is lacking.

In order to achieve maximum efficiency, the impact of the switching resistance on the output impedance of charge pump is discussed in [80] and [81]. Tanzawa [82] proposed a simulation method to define the optimal switching frequency, number of charge pump stages and circuit component parameters for the Dickson charge pump topology. [83] proposed a model-based methodology of optimizing Dickson charge pump topology to maximize the output current under the constrain of area. However, model-based analysis or optimization method for the cross-coupled charge pump, which is the most commonly used charge pump for ultra-low voltage DC-DC converter application, is lacking in the literature.

There are few available publications regarding to the LC tank oscillator modeling for frequency calculations and circuit parameter estimations. A half-circuit model of the transformer VCO is proposed by [68], which consists of two resonator circuits as shown in Figure 2.21. The model employed the parallel combination of an ideal capacitor, inductor, and resistor. An analytical expression for the oscillation frequency is derived using the transfer function of the VCO. The minimum NMOS transconductance is also derived using the model based transfer function. However, this work does not analyze power consumption or optimization methodology.

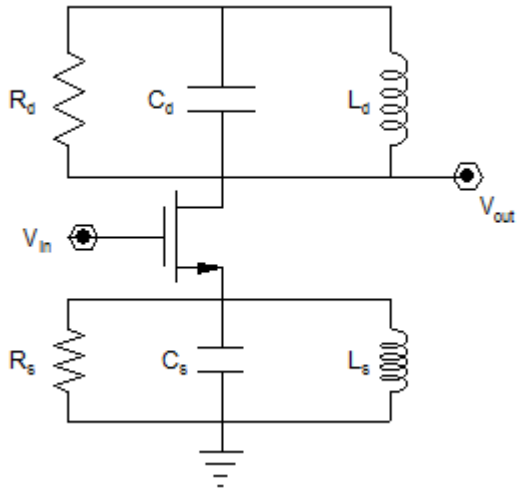

Figure 2.21. Half-circuit model for the transformer feedback VCO.

Machado and Schneider [84] presented a simplified half-circuit model for inductive load ring oscillator circuit to determine the minimum startup voltage. An analytical expression for the oscillation frequency, transfer function, and minimum startup voltage is derived using simplified half circuit model. However, the frequency behavior of the charge pump connected LC tank oscillator has not been analyzed in the literature.

In this thesis, a model based optimization of the DC-DC converter with charge pump connected LC tank oscillator is presented. The goal is to achieve maximum efficiency in the design. The analytical model is verified using standard 180 nm CMOS technology using Cadence IC simulations. Design, modeling, and analysis of a novel LC tank oscillator are presented in the next chapter to enhance the performance of the fully integrated ultra-low voltage DC-DC converter in terms of maximum efficiency and power capacity at low input voltage.

CHAPTER 3

3 PROPOSED OSCILLATOR ARCHITECTURE

3.1 Introduction

This chapter introduces a detailed description of the proposed oscillator architecture with a model based circuit analysis. Two novel LC tank oscillator topologies are presented: Voltage doubling LC tank oscillator, and voltage quadrupling LC tank oscillator. The objective of the proposed LC tank oscillators is to generate oscillations at ultra-low input voltage with high output voltage amplitude, low phase noise, frequency stability, and high oscillation purity. Amplification of ultra-low input voltage with high power capacity is necessary to efficiently drive the charge pump MOSFETs. Circuit design and frequency equations are derived using a simplified half circuit model. The oscillator is implemented in 180 nm standard CMOS technology in CAD environment to verify the model predictions.

3.1.1 Negative resistance generator

Negative resistance (or negative conductance) is necessary to compensate for the real losses associated with the real components (positive conductance) of the oscillator impedance. Current mirror technique is implemented in differential NMOS cross-coupled pair as illustrated in Figure 3.1. (a). The corresponding small signal circuit representation of M_2-NMOS is shown in Figure 3.1. (b). According to Figure *3.1*.(b), I_0 is,

$$I_0 = \frac{-g_m V_{DD}}{2} + \frac{V_{DD}}{2R_{ds}}, \tag{11}$$

where I_0, g_m, V_{DD}, and R_{ds} are M_2 drain current, NMOS transconductance, oscillator input voltage, and drain to source resistance of ON M_2 respectively. However, the input resistance (r) of NMOS cross-coupled pair is,

$$r = \frac{V_{DD}}{I_0} = \frac{2}{-g_m + {}^{1}/_{R_{ds}}}. \tag{12}$$

For the large NMOS in UMC 180 nm CMOS process, $g_m >> 1/R_{ds}$. Therefore, the NMOS cross-coupled pair provides a negative input resistance and can be simplified as,

$$r = \frac{-2}{g_m}. \tag{13}$$

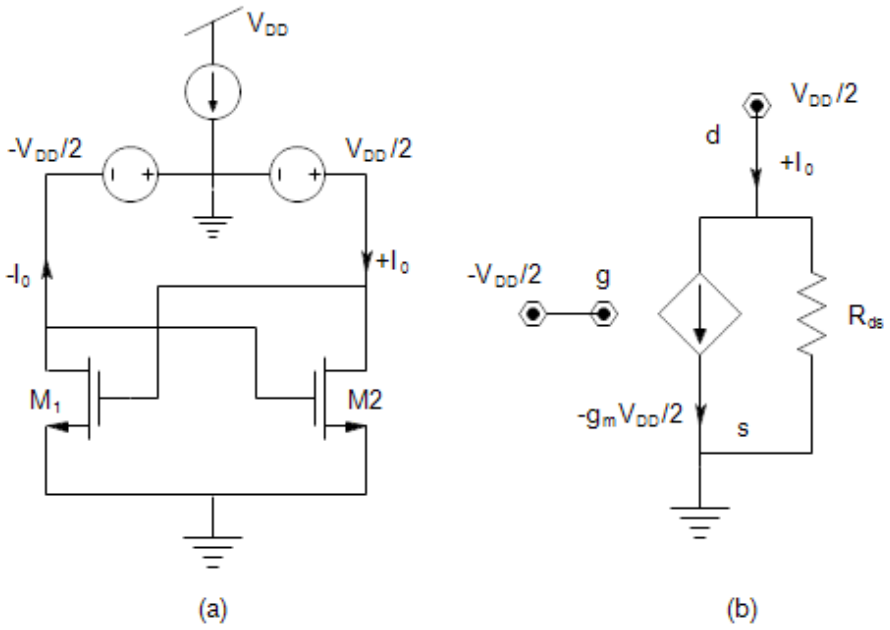

Figure 3.1. (a). Differential cross coupled NMOS pair, (b). M2 NMOS at differential state.

3.1.2 LC tank real losses

Self-resistance of inductors, capacitors, and NMOSs causes real losses in LC tank oscillator. When the NMOS is fully switched ON, the corresponding energy loss is negligible. Therefore, the series resistance of the inductor (R_S) and the capacitor (R_{CS}) cause real losses, and can be transformed into parallel resistance for small signal half circuit model analysis to make the easy of calculations as depicted in Figure 3.2.

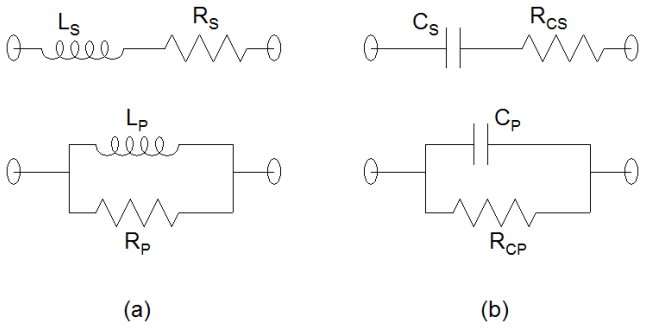

Figure 3.2. The series-parallel combination of (a) LR circuit, (b) CR circuit.

According to Figure 3.2. (a), series and parallel LR circuit impedance (Z_{LR}) at ω frequency is given by:

$$Z_{LR} = R_S + j\omega L_s = \frac{\omega^2 L_P^2 R_P}{R_P^2 + \omega^2 L_P^2} + j\frac{\omega L_P R_P^2}{R_P^2 + \omega^2 L_P^2}, \quad (14)$$

where R_P, and L_P are the equivalent parallel resistance of series resistance R_S and parallel inductance of series inductance L_S, respectively. Solving real and imaginary components of equation (14), the relation of the series and parallel resistance can be written as:

$$R_P = \frac{\omega^2 L_S^2}{R_S}. \tag{15}$$

According to Figure 3.2. (b), impedance (Z_{CR}) of series and parallel CR circuit at ω frequency is,

$$Z_{CR} = R_{CS} + {}^{1}/_{j\omega C_s} = \frac{R_{CP}}{1 + \omega^2 C_P^2 R_{CP}^2} - j\frac{\omega C_P R_{CP}^2}{1 + \omega^2 C_P^2 R_{CP}^2}, \tag{16}$$

where R_{CS} and R_{CP} are the series resistance with capacitor C_S, the equivalent parallel resistance of series resistance R_{CP} and equivalent parallel capacitance to series capacitance Cs respectively. Equating the real component of series and parallel impedance,

$$R_{CS}(1 + \omega^2 C_P^2 R_{CP}^2) - R_{CP} = 0. \tag{17}$$

Equating the imaginary component of series and parallel impedance,

$$1 + \omega^2 C_P^2 R_{CP}^2 - \omega^2 C_s C_P R_{CP}^2 = 0. \tag{18}$$

From equation (17) and (18), the parallel resistance (R_{CP}) can be written as,

$$R_{CP} = R_{CS} + \frac{1}{\omega^2 C_S^2 R_{CS}}. \tag{19}$$

In the utilized process technology (UMC 180nm CMOS), the R_S and R_{CS} values are limited to < 10 Ω for a typical inductor in nH range, and a capacitor with pF range. Equation (15) and (19) thus illustrate that $R_{CP} >> R_P$ for the low-frequency conditions since $\omega^2.C_S^2.R_{CS} << 1$. Therefore, parallel resistance of the inductor (R_P) is dominant in the LC tank, and R_{cp} can be neglected for $R_{cp} \,||\, R_p$ configuration. The LC tank oscillator can thus be represented as a parallel combination of a pure inductor, capacitor, and resistance as shown in Figure 3.3. The power loss (P_r) due to inductor self-resistance can expressed as,

$$P_R = I_0^2 R_s, \tag{20}$$

where I_0 is the average current through the inductor.

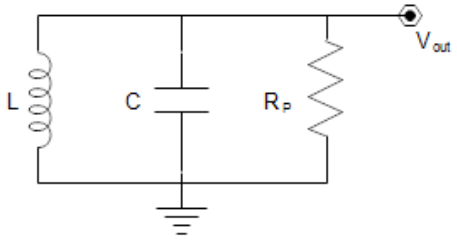

Figure 3.3. LC tank oscillator with ideal components.

Energy loss associated with LC tank inductor (P_L) and capacitor (P_C) can be expressed as,

$$P_L = fLI_0^2, \tag{21}$$

$$P_C = \frac{C\omega\left(V_{PP}/2\sqrt{2}\right)^2}{2\pi}, \tag{22}$$

where V_{PP} is the peak voltage across the capacitor. Therefore, total loss (P_T) is,

$$P_T = \left(V_{PP}/2\sqrt{2}\right)^2\left[\frac{1}{R_{DS}} + \frac{C\omega}{2\pi}\right] + I_0^2(R_s + fL), \tag{23}$$

where R_{DS} is the average drain to source resistance of NMOS off stage. For an LC tank operating with an ultra-low voltage input, nH inductors and pF capacitors, the inductor current is less than 1 mA, and the power consumption of the inductor is negligible for a typical on-chip inductor with resistance < 10 Ω. Therefore the total power consumption of LC tank can be simplified as,

$$P_T = \left(V_{PP}/2\sqrt{2}\right)^2\left[\frac{1}{R_{DS}} + \frac{C\omega}{2\pi}\right]. \tag{24}$$

3.1.3 Oscillator phase noise

Low phase noise is one of the main criteria of oscillator design in many low power applications such as wireless, wired communication, charge pump clock signals, data converters, and sensors, among others. The low noise oscillator is an advantage for any clocked system in terms of performance. A general expression for the oscillator phase noise is given by Leeson's formula as equation (25):

$$L(\Delta\omega) = 10\,log\left\{\frac{2FkT}{P_{sig}}\left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\right\}, \tag{25}$$

where T is the temperature in Kelvin, ω_0 is the oscillation frequency, Q is the tank quality factor, $\Delta\omega$ is offset from the carrier, P_{sig} is the signal power, F is a constant (noise factor) and k is the Boltzmann constant. Higher signal amplitude, subject to high output power, leads to lower phase noise according to equation (25). The active devices contribute to phase noise with increasing noise factor in equation (25) and as a result the LC tank oscillator has low phase noise due to the minimum number of active devices and high amplitude.

3.2 Voltage doubling LC tank oscillator

3.2.1 Basic operation of oscillator

The proposed voltage doubling LC tank oscillator consists of two inductors and a single cross-coupled NMOS pair as shown in Figure 3.4. This is an enhanced version of LC tank topology proposed in [85]. The parasitic capacitance of the inductor and NMOS is utilized to enhance the oscillator amplitude while reducing the power consumption. The identical inductors (L_1=L_2) and N-type MOSFETS (M_1=M_2) cause the symmetrical behavior to generate two identical oscillations with 180^0 phase offset with respect to each other. V_{DD} is the input voltage of the LC tank oscillator, which is assumed to be a constant DC voltage with minimum ripple.

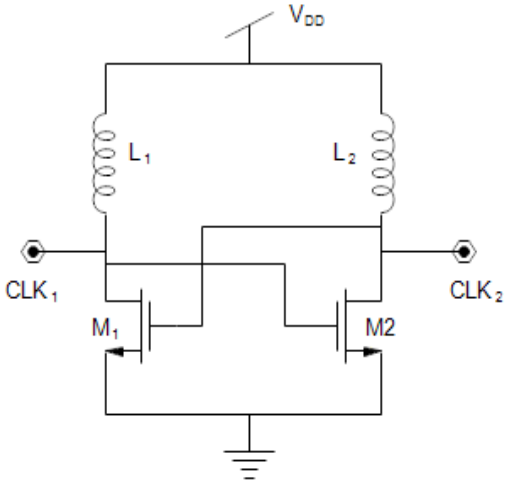

Figure 3.4. Voltage doubling LC tank oscillator.

The voltage doubling LC tank oscillator working principle is analyzed using the simplified half-circuit model as depicted in Figure 3.5. A capacitor stores energy in the form of electrical charge, which generates a voltage across it. An inductor stores energy in its magnetic field, depending on the current through it. The inductor peak current with fully discharged C_1 capacitor leads to transfer of input voltage (V_{DD}) to CLK_2 in Figure 3.5. If N_2 is OFF and C_1 is fully charged as shown in Figure 3.5. (a), the current will start to flow through the

inductor while reducing the CLK_2 voltage. This current accumulates energy in the form of magnetic flux in L_1. Eventually, C_1 has discharged, and the voltage across it reaches zero. However, the current will continue to flow as shown in Figure 3.5. (b) because the current through an inductor cannot change instantaneously. Now the voltage at CLK_2 is equivalent to V_{DD}. The current starts to charge the capacitor in opposite polarity to its initial state. If N_2 is ON just after the start of capacitor charging, the capacitor will directly connect to the ground and charge V_{DD} instantly. Once the magnetic field has dissipated, the current through the inductor will be zero as illustrated in Figure 3.5. (c). Then, the current will start to flow in the opposite direction through the inductor due to the voltage across it (in case of the charged capacitor in parallel). Since N_2 is still ON, the current will be sourced by the input power source. This inductor current is stored as energy in the form of the magnetic field at L_1. Once N_2 is off, C_1 starts to discharge through L_1. The fully discharged C_1 allows the peak current on L_1 inductor as shown in Figure 3.5. (d). Therefore, the inductor will store energy from charged C_1 capacitor and input source (V_{DD}) simultaneously. At this instant, the voltage at CLK_2 is V_{DD}. The zero voltage across the C_1 capacitor causes the current through L_1 to stop, but L_1 resists change in its current, so the reduction of current is gradual. Therefore, current will continue in the same direction but will decrease as the L_1 magnetic flux discharges through the C_1 capacitor. This inductor current will charge the C_1 capacitor to $< 2V_{DD}$, and $> V_{DD}$, which will result in $> 2V_{DD}$ at CLK_2 as illustrated in Figure 3.5. (e). Then the cycle will begin again, with the reverse current through the inductor. Drain to source resistance of switched ON M_2 and load current will decrease CLK_2 peak voltage. The oscillator output transition depends on CMOS threshold voltage as illustrated in Figure 3.6.

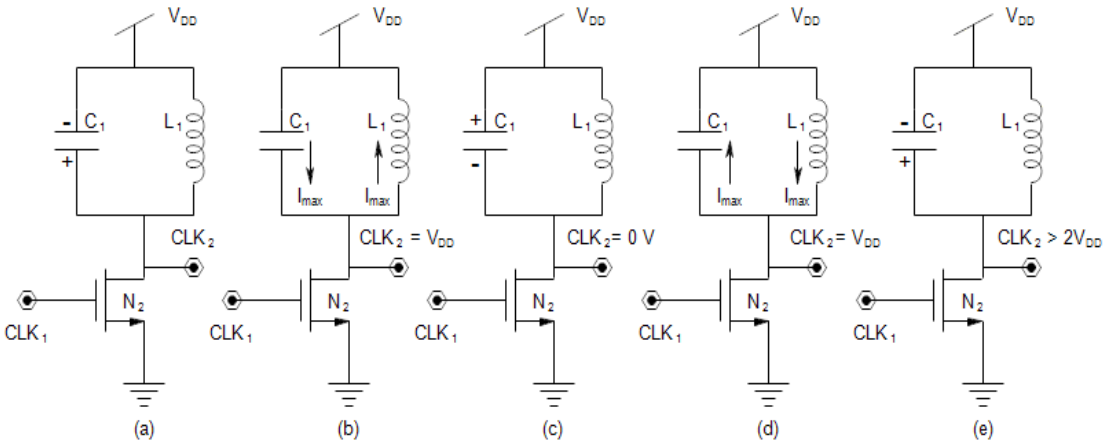

Figure 3.5. Half circuit analysis for the voltage doubling oscillator.

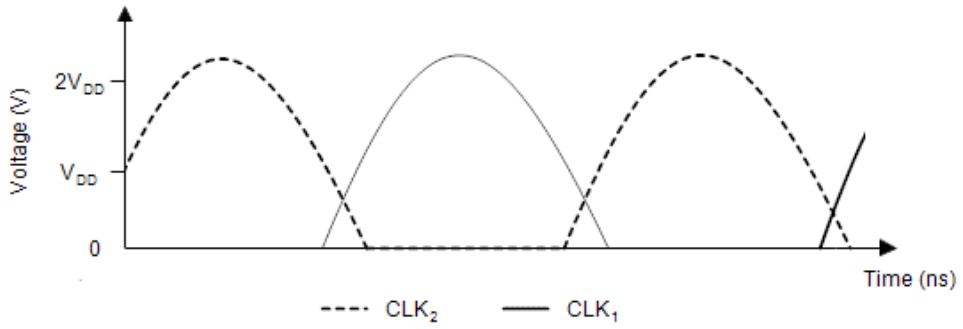

Figure 3.6. Voltage doubling LC tank output wave form.

3.2.2 Model based circuit analysis

The small signal half-circuit model of the LC tank oscillator is composed of a parallel combination of capacitor and inductor as illustrated in Figure 3.7. Inductor self-resistor is represented as a series resistance (R_S) and inductor L. Since V_{out} is an alternative voltage, self-resistance of capacitor C is infinitesimal, and can be ignored. Drain to source voltage at switched OFF NMOS is represented as R_{dc} (R_{ds} >>). From Kirchhoff first law,

$$-g_m V_{in} = V_{out}\left(\frac{1}{R_P} + \frac{1}{R_S + j\omega L} + j\omega C\right). \tag{26}$$

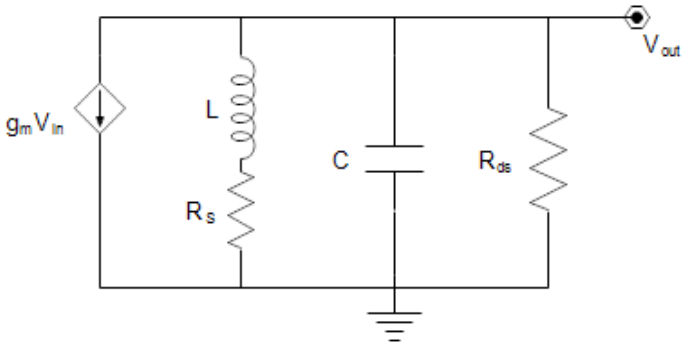

Figure 3.7. Small signal half-circuit model of the LC tank oscillator.

Transfer function of the half-circuit model from equation (16),

$$\frac{V_{out}}{V_{in}} = \frac{-g_m}{\frac{R_S^2+\omega^2L^2+R_SR_P}{R_P(R_S^2+\omega^2L^2)} + j\frac{R_S^2C\omega - L\omega(1-\omega^2LC)}{R_S^2+\omega^2L^2}}, \tag{27}$$

where g_m represents the NMOS gate transconductance. The phase shift α between V_{out} and V_{in} can be calculated from (26) as,

$$\alpha = \pi - \tan^{-1}\left[\frac{R_S^2 C\omega - L\omega(1-\omega^2 LC)}{R_S^2 + \omega^2 L^2}\right]. \quad (28)$$

For the full wave oscillations with out of phase CLK_1 and CLK_2 in Figure *3.4*, the phase shift is π. Thus, the oscillation frequency ω calculated from (28) is,

$$\omega = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{R_S^2 C}{L}}. \quad (29)$$

The minimum close loop gain should be unity for the continuous oscillations. Therefore, the minimum condition for the oscillations from equation (27) is,

$$g_m \geq \frac{1}{R_P} + \frac{R_S}{R_S^2 + \omega^2 L^2}, \quad (30)$$

but $1/R_P$ is negligibly small because $R_P >> 1$,

$$g_m \geq \frac{R_S}{R_S^2 + \omega^2 L^2}. \quad (31)$$

Substituting ω from equation (28),

$$g_m \geq \frac{R_S C}{L}. \quad (32)$$

Larger MOSFETs (W/L ratio) increase the transconductance of the NMOS but increase the current consumption of the design. Therefore, optimal W/L ratio is necessary for low power consumption while operating in ultra-low voltage domain.

3.2.3 Characteristics of UMC 180 CMOS process

Table 3.1. shows the design parameters of the voltage doubling LC tank oscillator. NMOS multiplier represents the number of parallel NMOSs used in a cross-coupled pair for higher transconductance. This parallel combination increases the parasitic capacitance and decreases the active resistance of the MOSFETs. The NMOS channel length causes more current and decreases the oscillation amplitude. Therefore, the minimum channel length of the Low-Vt NMOS in UMC 180 CMOS process is used for the cross-coupled NMOS pair. The maximum spiral width and capacitance available in UMC 180 CMOS are used for minimizing the inductor self-resistance and oscillations, respectively.

Table 3.1. Voltage doubling LC tank parameters.

Component	parameters	UMC_18_CMOS cell name
M_1 & M_2	W/L = 400 µm/240 nm 1<Multiplier <11	N_LV_18_MM
L_1 & L_2	Inductance = 14 nH Width = 20 µm Turns = 5.5 Diameter = 238 µm	L_SLCR20K_RF

Change of NMOS multiplier causes variation in the LC tank capacitance. As discussed in the simplified half-circuit analysis, the oscillation amplitude increases with the LC tank capacitance (NMOS multiplier) as illustrated in Figure 3.8. The rate of increase decreases with the multiplier due to the increase in time constant of the charging and discharging cycle.

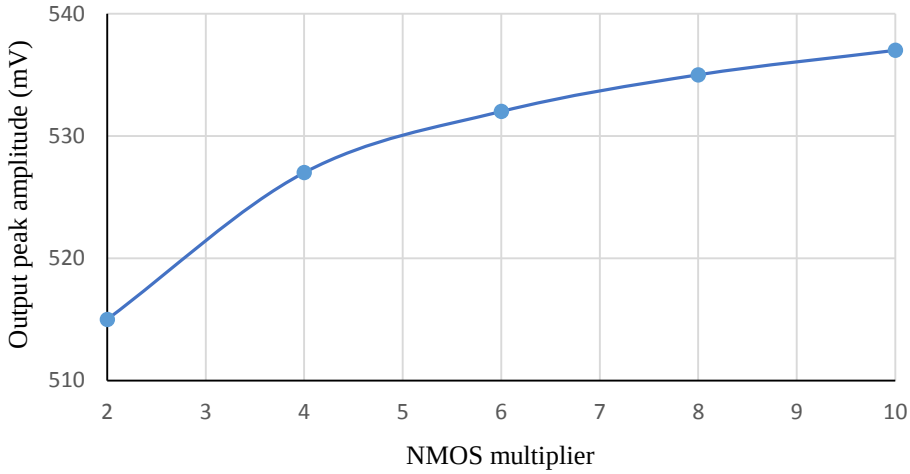

Figure 3.8. The variation of oscillator peak amplitude with NMOS multiplier.

LC tank frequency response is shown in Figure 3.9, where model analysis is validated against simulation results. The oscillator frequency inversely changes with the tank capacitor. Therefore, NMOS size is utilized as a frequency selecting parameter for the oscillator. The oscillator with 14 nH inductors can achieve at least 40% tuning range from tank capacitors. The simulation and model based calculation results indicate increasing power dissipation with tank capacitance as illustrated in Figure 3.10. Since the simulation results are similar to model based calculations, the model can be considered as a good theoretical method to estimate the circuit parameters of the LC tank according to the application requirement.

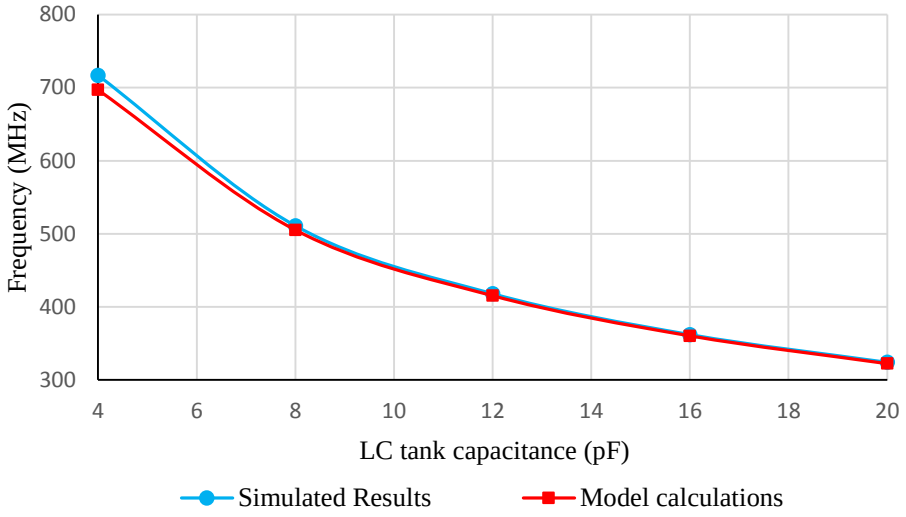

Figure 3.9. The variation of the oscillation frequency with LC tank capacitance.

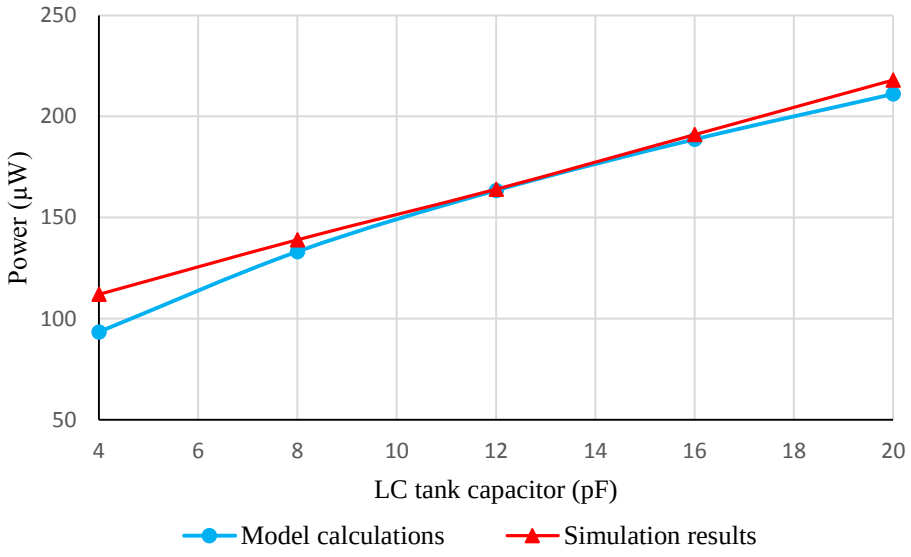

Figure 3.10. The variation of LC tank power consumption with tank capacitance.

The higher oscillator clock amplitude is an advantage for the DC-DC converter to achieve the expected step-up conversion with a minimum number of circuit components. Additionally, low phase noise and high oscillation purity minimize the losses in regards to the leakage of the MOSFET switches. A novel voltage quadrupling LC tank oscillator is presented next to achieve output clock with higher amplitude and lower phase noise for the DC-DC converter applications.

3.3 Voltage quadrupling LC tank oscillator

3.3.1 Basic operation

The voltage quadrupling LC tank oscillator can generate a sinusoid signal output with at least quadrupled peak-to-peak amplitude compared to the input DC voltage supply. Apart from the high gain, the oscillator consists of desirable characteristics such as low phase noise and frequency stability. These objectives are met through two synchronously operating LC oscillators (primary and secondary) controlled by a cross-coupled switch pair. As illustrated in Figure 3.11, the controlling switches are implemented as CMOS N-channel MOSFETs (NMOS). V_{DD} is the input supply voltage in the figure. CLK_1 and CLK_2 represent two output sinusoid signals with 180^0 phase offset with respect to each other. The negative resistance of the cross-coupled differential NMOS pair compensates the real losses from the passive components. C_0 is the optional capacitor, which can be implemented through the parasitic capacitance from the inductors and switches of the primary oscillator in Figure 3.11. The parallel combination of the C_2 with L_2 form the secondary LC tank.

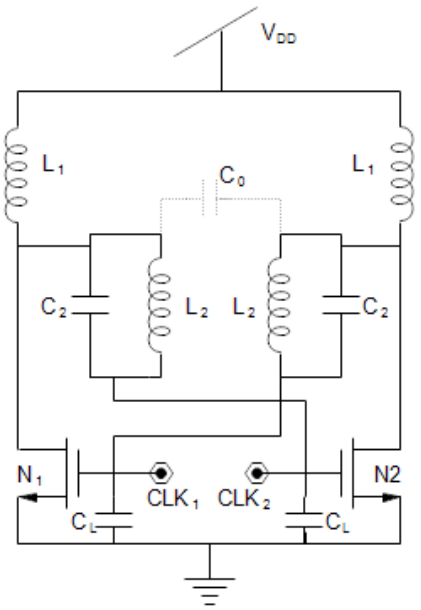

Figure 3.11. Voltage quadruple LC tank based oscillator.

The primary LC tank oscillator operation is similar to the voltage doubling LC tank. In the voltage quadrupling LC tank, a large voltage swing is observed at the gate node instead of the drain node of NMOS. NMOS drain voltage swings between 0 V and 3 V_{DD} according to the on-off state of the MOSFET.

The secondary LC tank operation is analyzed using an array of the half-circuit models as shown in Figure 3.12. Since CLK_1 (oscillator output node) and node A have different zero-crossing as illustrated in Figure 3.13.(a), the peak current through the L_2 inductor does not coincide with the L_1 peak current, as depicted in Figure 3.13.(b). The current from N_2 drain to primary LC tank inductor is assumed negative in the figure, while current from N_2 drain to C_2 and L_2 is positive. The L_2 peak current is synchronized with the C_2 peak current, but it is opposite in direction as illustrated in Figure 3.13.(b). The zero voltage across the capacitor C_2 due to fully discharged state causes it to start charging. At this instant voltage at node A and node CLK_1 are equal (ground). The simultaneous zero current through L_2 and C_2 results in the minimum voltage at the output. Once, N_2 is off and both C_L and C_2 are fully charged as shown in Figure 3.12.(a), the voltage at node A < CLK_1. C_2 and C_L will then discharge through L_2 and R_L while accumulating magnetic energy in L_2. Since C_2 is discharging, this current will not flow into the primary LC tank. The fully discharged C_2 and C_L conduct the maximum L_2 current while delivering zero voltage at node A and CLK_1 as in Figure 3.12.(b). Then L_2 starts to contribute to the current in the same direction and starts to charge the capacitors. Since N_2 is switched on, some portion of the current flows through NMOS, and sinks to the ground. Finally, capacitors charge as shown in Figure 3.12.(c), and create the minimum voltage at CLK_1 ($\leq -2V_{DD}$). Then C_2 starts to discharge through L_2 inductor while C_L is charging as shown in Figure 3.12.(d), and simultaneously the primary LC tank capacitor is fully charged, which result in L_1 inductor current flowing through L_2 due to the negative voltage at CLK_1 with respect to the ground connection in NMOS drain. The fully discharged C_L and C_2 stop the current loop while the grounded voltage at node A is conveyed to CLK_1. Since the inductor resists the change in current, L_2 starts to discharge the magnetic energy by producing current in the same direction. This current will start to charge the capacitors, but the current through C_2 capacitor will sink to ground due to N_2 ON condition (A = 0V) as shown in Figure 3.12.(d). Once voltage increases at CLK_1, the most of the current starts to flow through the load and C_2 current will reduce since N_2 is switched off as shown in Figure 3.12.(e). Therefore, C_L current will be maximum and will increase CLK_1 voltage. The increase in CLK_1 voltage with respect to node A decreases the C_L current and allows increase of C_2 current in the same direction again. Once C_L is fully charged (C_L current is zero), the voltage at CLK_1 is at maximum as shown in Figure 3.12.(f) with secondary peak current through the C_2 as illustrated in Figure 3.13.(b). Then C_L and C_2 start to discharge through L_2 inductor while reducing the voltage at CLK_1. This loop will continue until disconnection at the external power source (V_{DD}). The voltage across C_2 capacitor varies from $-2V_{DD}$ to $2V_{DD}$ with respect to node A as shown in Figure 3.13.(c). When CLK_1 voltage peaks, C_2 voltage is $\leq 2V_{DD}$ and $\geq V_{DD}$ according to C_2

capacitance. Higher C_2 capacitance will produce higher CLK_1 voltage due to lower impedance and higher time constant, compared to lower C_2 capacitance value. On the other hand, increase in C_L causes reduction the peak CLK_1 voltage, resulting in reduction in the current through C_2.

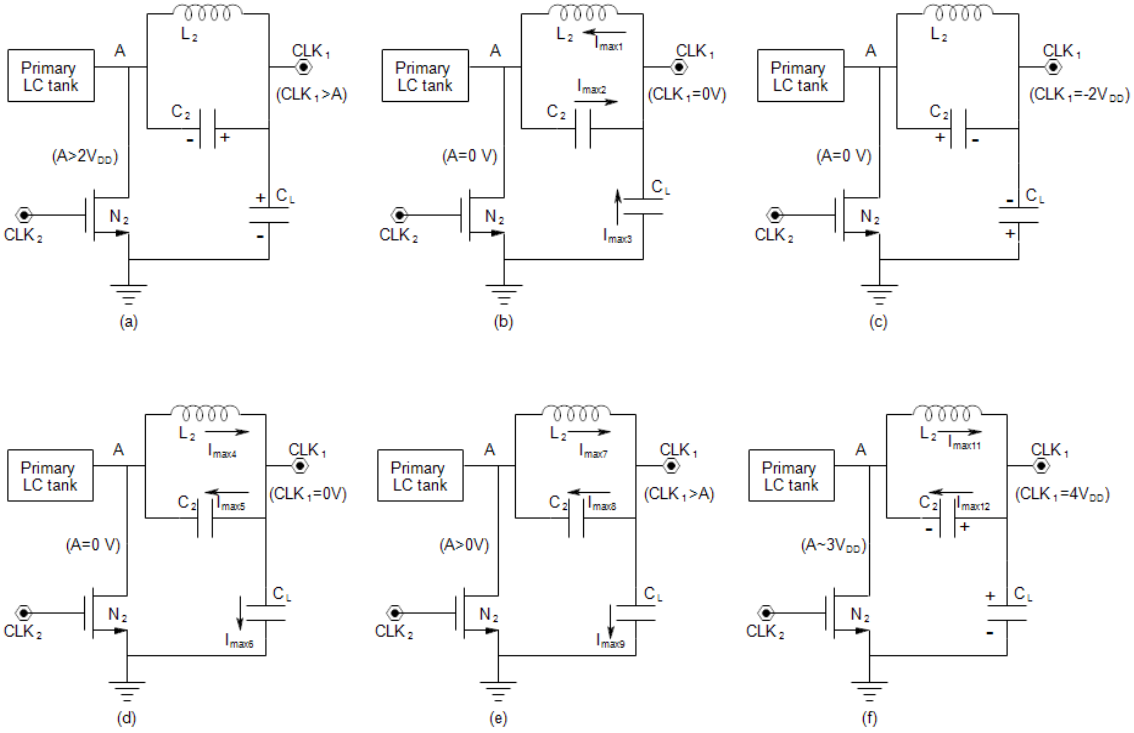

Figure 3.12. Half circuit analysis for the secondary oscillator.

3.3.2 Modal based circuit analysis

The simplified small-signal half circuit model is shown in Figure 3.14 for the frequency analysis. The primary LC tank is modeled with L_1 inductor and C_1 capacitor. C_1 is the sum of parasitic capacitance between the drain of the NMOS and ac ground. R_{P1} is the parallel resistance of the L_1 inductor. The parallel combination of L_2 and C_2 form the secondary LC tank. Self-resistance of L_2 is represented with R_{S2}. C_L is the effective capacitance between CLK node (output) and ac ground, comprising of the sum of load capacitance, NMOS gate capacitance, and L_2 and C_2 node capacitance values.

The ratio of the output voltage (V_O) and the NMOS drain voltage (V_X), according to the model shown in Figure 3.14, is:

$$\frac{V_0}{V_x} = \frac{(1-\omega^2 C_2 L_2)\left(1-\omega^2 L_2(C_2+C_L)\right)+\omega^2 R_{s2}^2 C_2(C_2+C_L)}{\left(1-\omega^2 L_2(C_2+C_L)\right)^2+\omega^2 R_{s2}^2(C_2+C_L)^2}. \quad (33)$$

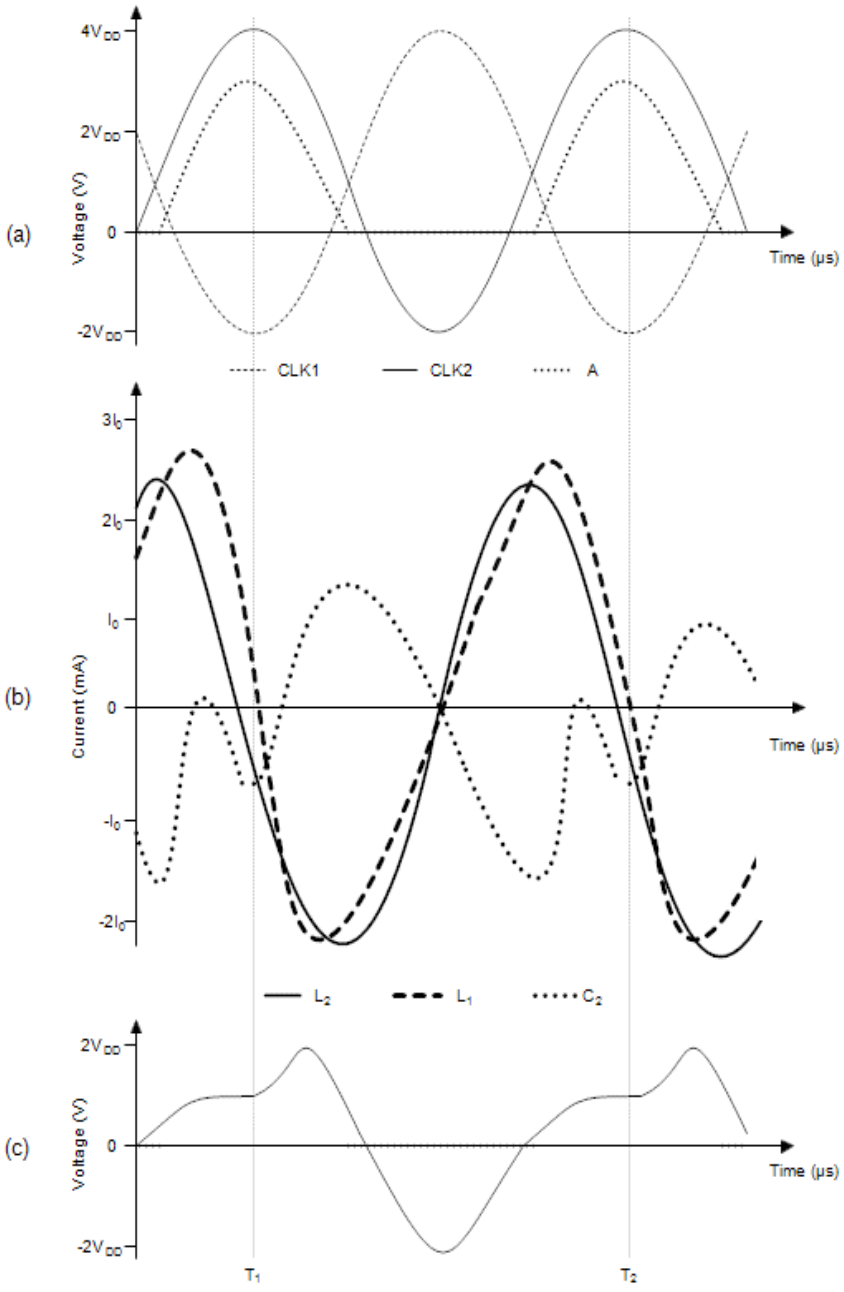

Figure 3.13. The characteristic curves for the voltage quadrupling LC tank.

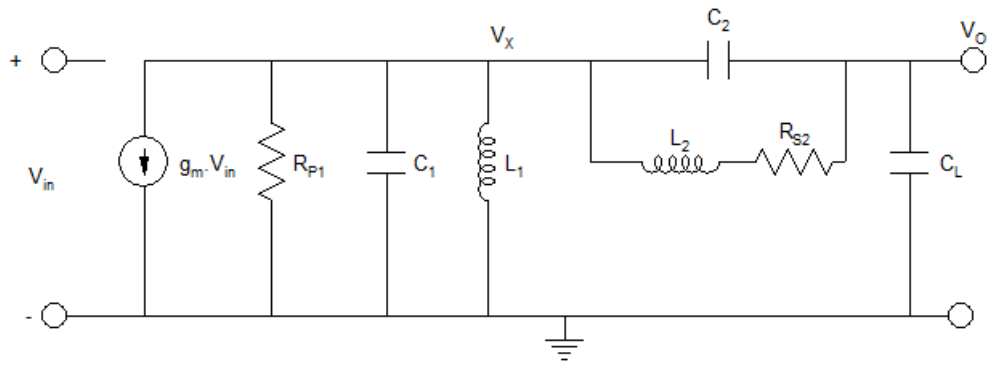

Figure 3.14. Simplified small-signal half-circuit model of the voltage quadrupling LC tank oscillator.

Given the following simplifying assumptions:

$$\left(1-\omega^2 \mathrm{L}_2(C_2+C_L)\right)^2 \gg \omega^2 \mathrm{R}_{\mathrm{S2}}^2(C_2+C_L)^2, \tag{34}$$

$$(1-\omega^2 C_2 L_2)\left(1-\omega^2 L_2(C_2+C_L)\right) \gg \omega^2 R_{s2}^2 C_2(C_2+C_L)\ , \tag{35}$$

equation (23) can be rewritten as:

$$\frac{V_0}{V_x}=\frac{(1-\omega^2 C_2 L_2)}{1-\omega^2 L_2(C_2+C_L)}. \tag{36}$$

The output voltage (V_O) of the LC tank must be higher than V_X, for all positive V_X. Therefore,

$$\omega^2 < \frac{1}{(C_2 L_2 + C_L L_2)}\ . \tag{37}$$

The transfer function of the voltage quadrupling LC tank oscillator, according to the model shown in Figure 3.14, is:

$$\frac{V_0}{V_{in}}=\frac{-g_m}{\frac{(1-\omega^2 C_2 L_2-\omega^2 C_L L_2)}{(1-\omega^2 C_2 L_2) R_{p1}}+j\left\{\frac{(1-\omega^2 C_2 L_2-\omega^2 C_L L_2)}{(1-\omega^2 C_2 L_2)}\left(\omega C_1-\frac{1}{\omega L_1}\right)-\omega C_L\right\}}\ , \tag{38}$$

where g_m represents the NMOS gate transconductance. The phase shift α between V_O and V_{In} can be calculated from (38) as,

$$\alpha=\pi-tan^{-1}\left\{\frac{\left(1-\omega^2 L_2(C_2+C_L)\right)}{\left(\frac{1}{\omega}-\omega C_2 L_2\right)}\left(C_1-\frac{1}{\omega^2 L_1}\right)-C_L\right\}. \tag{39}$$

For full wave oscillations with out of phase CLK_1 and CLK_2 in Figure *3.11*, the phase shift is π. Thus, the oscillation frequency ω calculated from equation (39) is,

$$\omega^4\left\{L_1 L_2[C_1 C_2+C_L(C_1+C_2)]\right\}-\omega^2 b+1=0, \tag{40}$$

$$\omega^2 = \frac{b \pm \sqrt{b^2 - 4L_1L_2[C_1C_2 + C_L(C_1 + C_2)]}}{2L_1L_2[C_1C_2 + C_L(C_1 + C_2)]}, \tag{41}$$

$$b = L_1C_1 + L_2C_2 + C_L(L_1 + L_2)\ . \tag{42}$$

Equation (40) yields two positive solutions for ω. ω must satisfy the equation (36) for high gain operation. Therefore,

$$\omega = \sqrt{\frac{b - \sqrt{b^2 - 4L_1L_2[C_1C_2 + C_L(C_1 + C_2)]}}{2L_1L_2[C_1C_2 + C_L(C_1 + C_2)]}}. \tag{43}$$

Based on equation (37), the required transconductance (g_m) to sustain the oscillation is given by:

$$g_m \geq \frac{(1 - \omega^2C_2L_2 - \omega^2C_LL_2)}{R_{p1}(1 - \omega^2C_2L_2)}. \tag{44}$$

From equation (30), the necessary condition to sustain oscillation is:

$$b^2 \geq 4L_1L_2[C_1C_2 + C_L(C_1 + C_2)]\ . \tag{45}$$

3.3.3 Characteristics of UMC 180 CMOS process

The design parameters of the voltage quadrupling LC tank oscillator is shown in Table 3.2. NMOS multiplier is the number of parallel N-type MOSFETs, a mechanism to decrease the drain to source resistance of M_1 & M_2 and change the tank capacitance. For the continuous oscillations, the transconductance of M_1 & M_2 should satisfy the minimum requirement of equation (33). The oscillation amplitude variation with tank capacitance is depicted in Figure 3.15. Similar to a voltage doubling LC tank, an increase of primary resonator capacitance decreases the amplitude of voltage quadrupling LC tank. However, the secondary resonator capacitance increases the oscillation peak amplitude since it increases the time constant. The output waveforms are sinusoidal and the amplitude is symmetrical across the input voltage range of the LC tank.

The simulated voltage quadrupling oscillator frequency variation with primary and secondary LC tank oscillator is depicted in Figure 3.16 and Figure 3.17, respectively along with the model results. Different NMOS multiplier values are used to change the primary LC tank capacitance of the voltage quadrupling oscillator with 14 nH inductor, and 25 pF secondary capacitor. For the Figure 3.17, the NMOS multiplier is 3 and the total primary LC tank capacitance is 11.15 pF. Both primary and secondary LC tanks capacitors lead to a decrease in the oscillation

frequency and achieve more than 25% frequency tuning range. However, the model calculations bit higher than the simulation frequency. The reason for this discrepancy is the neglecting some small parasitic capacitance, approximations and simplification made in calculations.

Table 3.2. Voltage quadrupling LC tank parameters.

Component	Parameters	UMC_18_CMOS cell name
M_1 & M_2	W/L = 600 µm/240 nm 2 < Multiplier < 15	N_LV_18_MM
L_1 & L_2	Inductance = 14 nH Width = 20 µm Turns = 5.5 Diameter = 238 µm	L_SLCR20K_RF
C_0	6 pF < C < 12 pF	MIMCAPS_MM
C_2	10 pF < C < 40 pF	MIMCAPS_MM

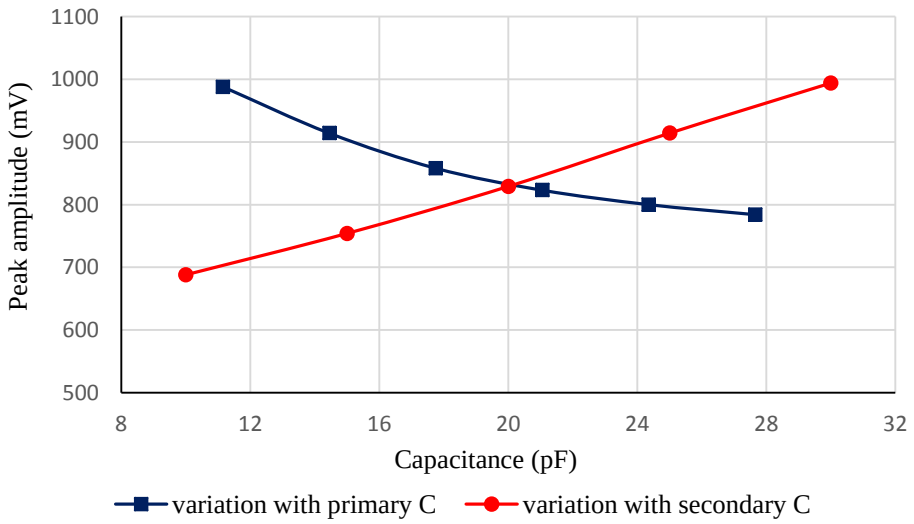

Figure 3.15. The variation of peak amplitude with LC tank capacitors.

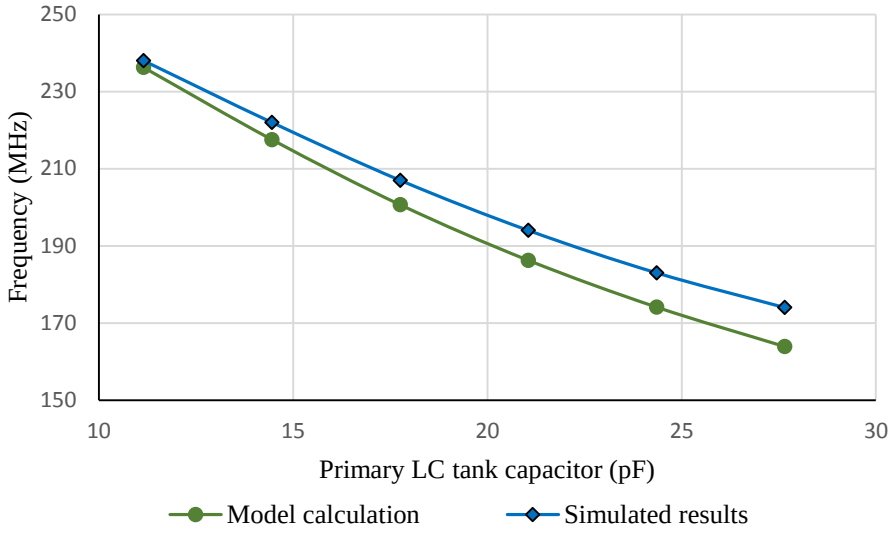

Figure 3.16. The variation of oscillation frequency with primary LC tank capacitance.

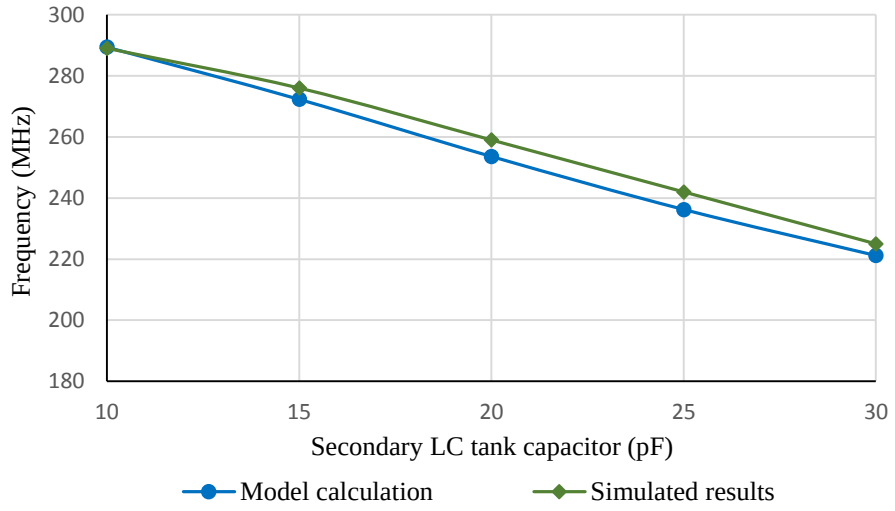

Figure 3.17. The variation of oscillation frequency with secondary LC tank capacitor.

Since the simulation results are similar to model base calculations, the model can be considered a justified theoretical method to determine the circuit component values of the LC tank according to the application requirement.

The LC tank coupled DC-DC converter design and model are presented in the next chapter along with the model based optimization methodology.

CHAPTER 4

4 PROPOSED DC-DC CONVERTER ARCHITECTURE

4.1 Introduction

This chapter introduces a detailed description of proposed DC-DC converter architecture with model based circuit analysis. Voltage doubling and quadrupling LC tank based oscillators are implemented as a clock generating circuit for the charge pump topology. The objective of the proposed DC-DC converters is to generate a high output voltage from the ultra-low input voltage with higher efficiency and higher output power capacity for energy harvesting applications. Two novel optimization methodologies have been proposed to improve the efficiency of a DC-DC converter for a given range of load conditions. Model based frequency analysis of the charge pump connected voltage doubling LC tank based oscillator is presented. The DC-DC converter is implemented in 180 nm standard CMOS technology in CAD environment to verify the model based analysis.

Figure 4.1 depicts the architectural block diagram of the proposed DC-DC converter. The system consists of two main sub-circuit blocks. Fully integrated LC tank oscillator is used as a self-starting clock generating circuit. The LC tank oscillator generates two out-of-phase clock signals. The charge pump is used to step up the ultra-low input DC voltage into higher DC voltage according to the load requirement. For the desired input voltage and load condition, the required voltage gain can be achieved using a proper number of charge pump stages.

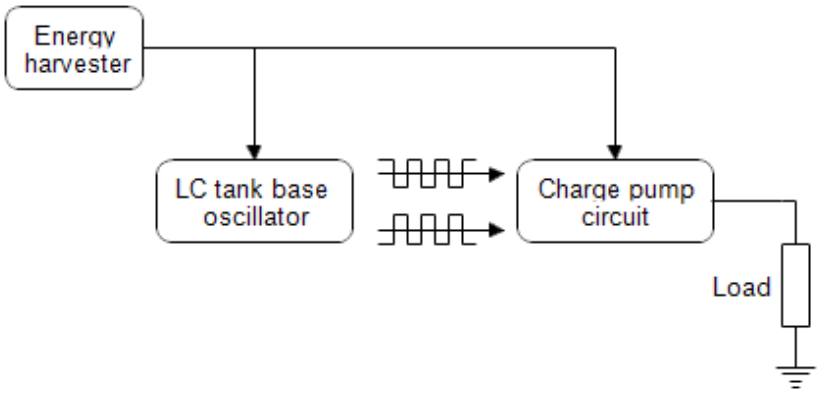

Figure 4.1. Block diagram of proposed DC-DC converter.

4.2 Charge pump circuit

The NMOS cross-coupled charge pump topology proposed by [46] has been enhanced with suitable parameters and Low-Vt MOSFETs to step up the ultra-low input voltage. A three-stage version of the cross-coupled MOSFET charge pump is depicted in Figure 4.2. The CLK_1 and CLK_2 clock signals are driven from the voltage doubling or quadrupling LC tank oscillators with $2V_{DD}$ or $4V_{DD}$ peak-peak amplitude respectively, and a frequency in the range of hundreds of MHz. Each N-channel MOSFET in the cross-connected pair charges the corresponding capacitor at opposite clock phase while the P-channel MOSFET devices take turns to transfer charge to the next stage.

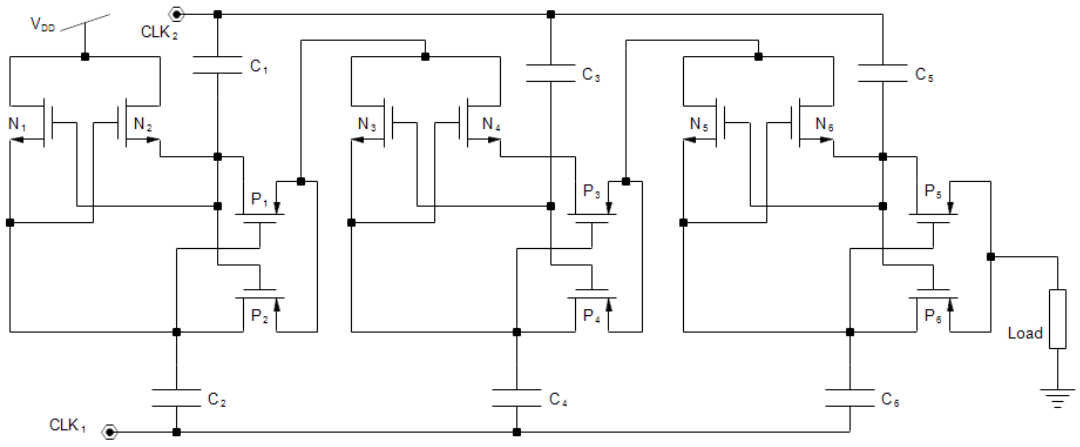

Figure 4.2. Cross-coupled MOSFET charge pump.

Once CLK_1 is high and CLK_2 is low, N_2 and P_1 will switch on and off, respectively allowing C_1 to charge V_{DD} while N_1 is off and P_2 is turned on. If the peak amplitude of CLK_1 is $2V_{DD}$, N_1 drain voltage reaches $3V_{DD}$ at the peak of CLK_1 because of the series connection of fully charged C_2 (V_{DD}) and CLK_1. Since P_2 is switched on, P_2 source terminal will achieve $3V_{DD}$ as the charges transfer from N_1 drain to P_2 source. During the opposite configuration of the clock signals, (CLK_1 low and CLK_2 high) N_2 and P_1 will turn off and on, respectively. Since C_1 is in series with CLK_2, the voltage at P_1 drain and source terminal is $3V_{DD}$. Turned on N_1 charges C_2 capacitor while P_2 blocks the charge transfer through PMOS. Therefore, P_1 source (= P_2 source, which is the output of the first stage and also the input of the second stage) voltage is at $3V_{DD}$ during the entire duration of the clock period. The same charge transfer process repeats itself in the subsequent stages. Therefore, each stage can achieve a stable step-up voltage during the operation of the clock signal.

4.3 DC-DC converter architecture with voltage doubling LC tank

A fully integrated DC-DC converter circuit consists of the resonator and coupled charge pump as illustrated in Figure 4.3 with only two stages of charge pump for clarity. The oscillator output nodes are connected to charge pump capacitors for the stimulation of charge transfer. Lack of buffer circuits between the charge pump and the oscillator is the main advantage in this topology, in addition to the high amplitude of voltage at each charge pump capacitor and stable DC voltage at each output stage of the charge pump. For the ultra-low input voltage range (typically less or equivalent to the threshold voltage value of the UMC 180 nm CMOS standard process), oscillation amplitude should be larger than the threshold voltage of MOSFETs for proper operation of the DC-DC converter. Optimal charge pump capacitors and MOSFET sizes are necessary to enhance performance, and minimize reverse current and switching losses. Larger MOSFETs cause higher sinking current and device capacitance, but small MOSFETs add to ON resistance, which causes resistive energy loss and voltage drop across each MOSFET. Therefore, an optimal MOSFET size is necessary for efficient DC-DC converter circuits. Smaller capacitors are unable to store sufficient charge to transfer into the next stage during the half cycle of the clock signal. However, larger capacitors cause energy losses proportional to the capacitance and will not fully discharge during the half-clock cycle. Therefore, capacitor size is one of the critical parameters to improve efficiency by minimizing the losses, and to sustain DC-DC converter voltage gain. The DC-DC converter has to be optimized as a whole with the clock generation, because the LC tank oscillator frequency is a function of NMOS drain capacitance, which increases with the charge pump coupling.

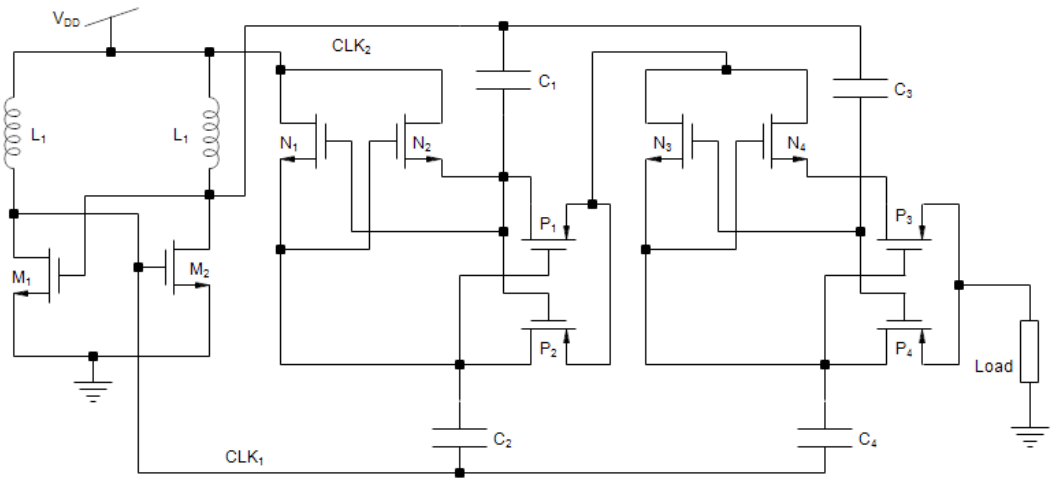

Figure 4.3. Two stage DC-DC converter with voltage doubling LC tank oscillator.

4.3.1 Charge pump coupled LC tank oscillator frequency

NMOS cross-coupled LC tank oscillator frequency is a function of the total capacitance of the cross-coupled NMOS drain. Therefore, the charge pump coupled LC tank oscillator frequency is a function of flying capacitors. Each charge pump capacitor is in series with at least a single MOSFET. The charge carrying MOSFET can be modeled as a series resistance with a capacitor. The equivalent parallel resistance (R_{CP}) and capacitance (C_P) of the series resistance (R_{CS}) and capacitance (C_S) can be derived using series parallel impedance transformation as shown in Figure 4.4.

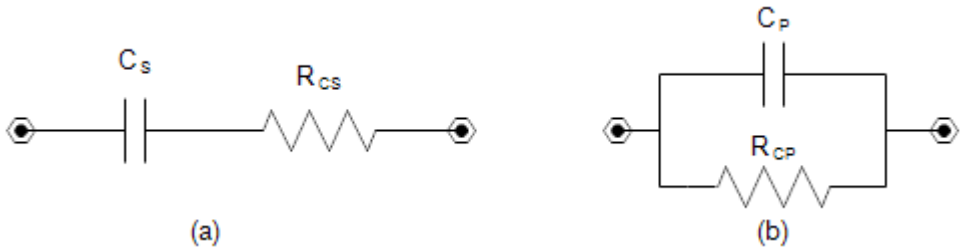

Figure 4.4. Series and parallel RC circuit.

By equaling the series RC impedance with parallel RC impedance at ω frequency,

$$R_{CS} + \frac{1}{j\omega C_S} - \frac{R_{PR}}{1 + j\omega C_P R_{PR}} = 0. \tag{46}$$

Solving equation (46), equivalent parallel capacitance (C_P) can be given as,

$$C_P = \frac{C_S}{1 + (\omega C_S R_{CS})^2}. \tag{47}$$

According to the equation (47), parallel capacitor is a function of series resistance and decreases with the increase in the series resistance of the capacitor. The variation of the equivalent parallel capacitance of a capacitor with the series resistance is depicted in Figure 4.5 for 400 MHz operation. The equivalent parallel resistance is inversely proportional to the series capacitance. Therefore, the added stages of charge pump capacitors affect the frequency less compared to the first stage capacitors.

A single stage DC-DC converter and enhanced LC tank model for the single stage DC-DC converter is illustrated in Figure 4.6.(a) and (b) respectively. R_{DS}, $R_{P,}$ and R_A refer to NMOS drain to source average resistance at turn-off condition, the equivalent parallel resistance of the inductor series resistance, and resistance between M_1 and M_2 drain respectively. The capacitance between M_1 and M_2 drain terminal is modeled as C_A, while C is the total

capacitance between NMOS drain terminal and virtual ground. C consists of the parasitic capacitance of NMOS, inductor, and charge pump capacitance, at the drain, and corresponding parallel capacitance (C_P) of charge pump capacitors.

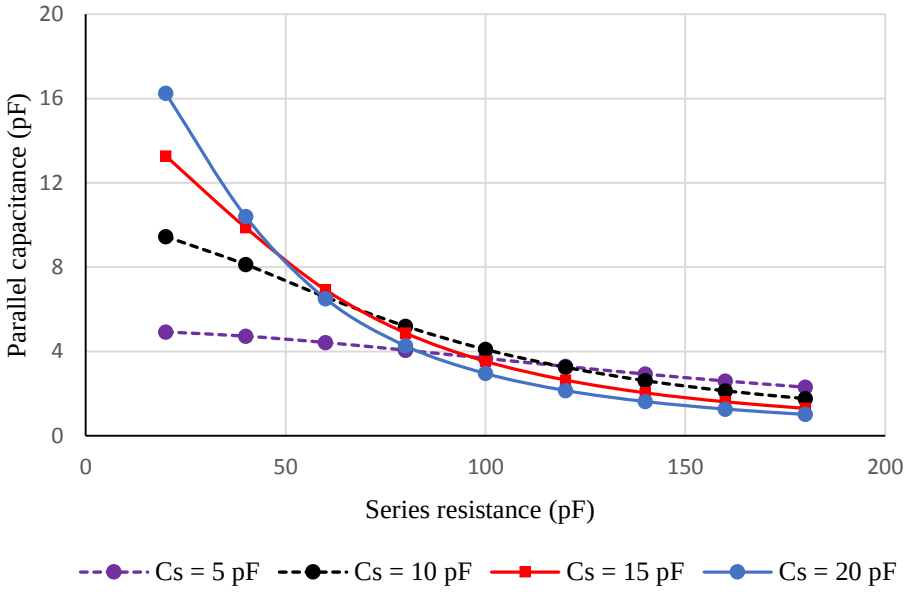

Figure 4.5. The variation of parallel capacitance with series resistance for different series capacitance.

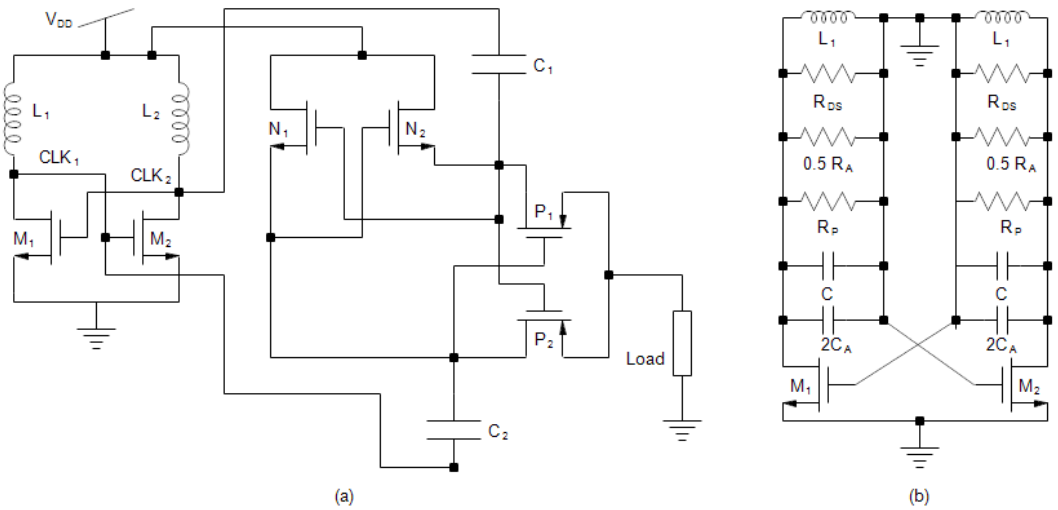

Figure 4.6. (a) Single stage DC-DC converter, (b) enhanced LC tank model for the single stage DC-DC converter.

For the inductor with small self-resistance, the charge pump coupled LC tank oscillator frequency (f_0) can be represented as,

$$f_0 = \frac{1}{2\pi\sqrt{L(C + 2C_A)}}. \tag{48}$$

But the total capacitance, $C + 2\,C_A$ can be rewritten as $C_0 + C_{P1}$, where C_0 is the LC tank capacitance corresponding to the resonator frequency without coupled charge pump, and C_{P1} is the parallel capacitance of charge pump capacitor C_1. Therefore, f_0 can rewrite as,

$$f_0 = \frac{1}{2\pi\sqrt{L(C_0 + C_{P1})}}. \tag{49}$$

From equation (48) and (49), the C_{P1} is given by,

$$C_{P1} = \frac{-(R_{CS1}^2 C_{S1}^2 + LC_0 - LC_S) + \sqrt{(R_{CS1}^2 C_{S1}^2 + LC_0 - LC_S)^2 + 4LC_{S1}C_0}}{2L}, \tag{50}$$

where C_{S1}, R_{CS1} represent first stage charge pump capacitance and ON NMOS resistance respectively. The average resistance of ON NMOS can be extracted from Cadence tool, which is a function of MOSFET size and UMC technology. The variation of NMOS resistance with MOSFET width is depicted in Figure 4.7, for UMC 180 nm CMOS process and 240 nm length.

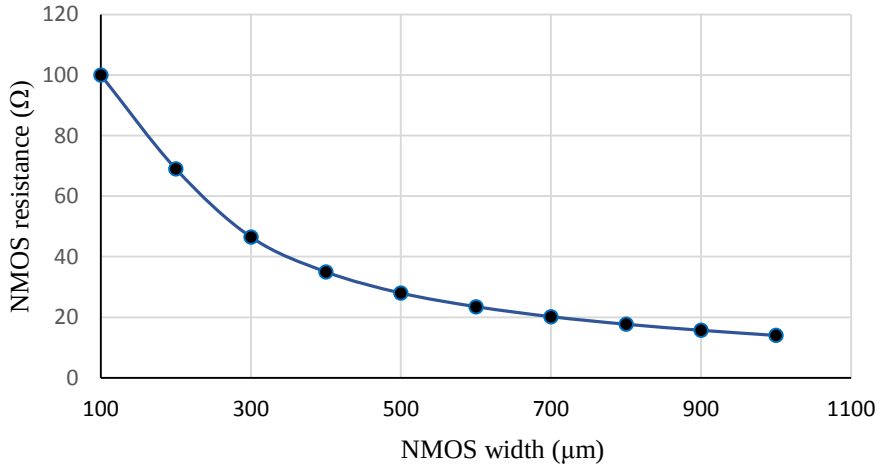

Figure 4.7. Variation of NMOS resistance with NMOS width (L = 240 nm).

The variation of charge pump coupled LC tank oscillation frequency with charge pump capacitance is illustrated in Figure 4.8, along with model validations. The clock frequency decreases with the increase in charge pump capacitance, and then starts to increase as the

parallel resistance is decreased for higher values of capacitance in series with the NMOS resistance. The reason for the small discrepancy between the model and simulation frequency is the change of average active resistance of the MOSFET with leakage current which is not included in the model.

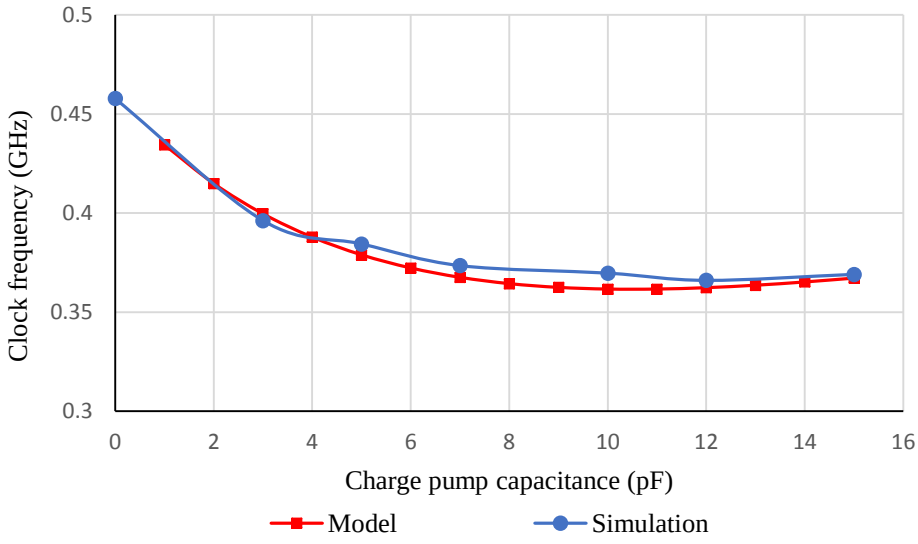

Figure 4.8. The variation of clock frequency with charge pump capacitance.

4.3.2 DC-DC converter model

The lumped element half circuit model of the n-stage DC-DC converter is illustrated in Figure 4.9. The charge pump MOSFETs are represented by individual resistors. The MOSFET capacitance is negligible compared to the charge pump capacitors. Each charge carrying path consists of two resistors and two capacitors except for the last stage. The last stage has a single charge pump capacitance and two resistors including the load resistance. While the LC tank NMOS drain is at the higher voltage phase, the drain to source resistance is high compared to parallel resistance paths, and can thus be ignored. In small signal AC analysis, the tank MOSFET resistance is in parallel with the inductor parallel resistance R_P (LC tank parallel resistance), and is much larger than the tank parallel resistance. C_L refers to the charge pump coupled LC tank parallel capacitance including LC tank capacitance and corresponding parallel capacitance from the charge pump.

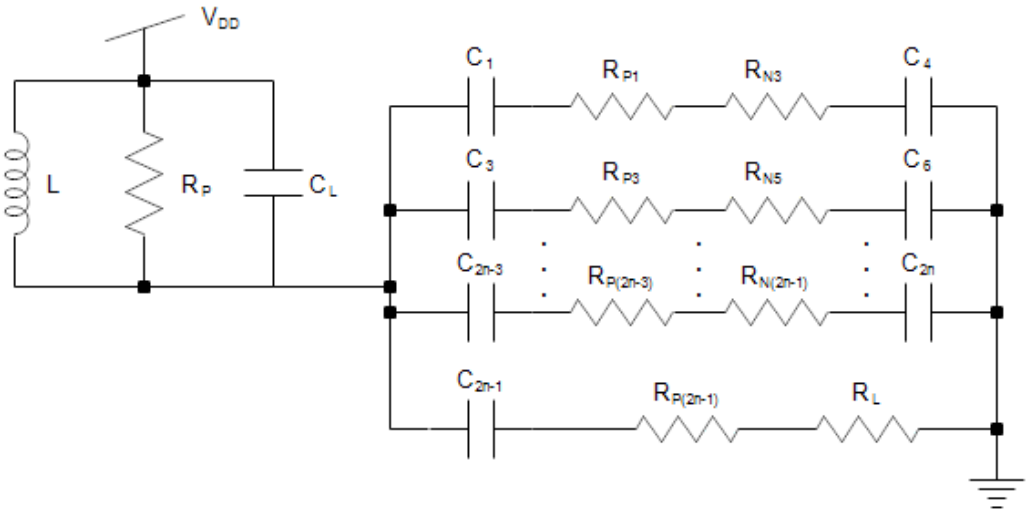

Figure 4.9. The lumped element half circuit model of the n-stage DC-DC converter.

The impedance of the each charge carrying path network can be written as,

$$Z_1 = (R_{P1} + R_{N3}) - j\left({}^{1}/_{\omega C_1} + {}^{1}/_{\omega C_4}\right), \tag{51}$$

$$Z_2 = (R_{P3} + R_{N5}) - j\left({}^{1}/_{\omega C_3} + {}^{1}/_{\omega C_6}\right), \tag{52}$$

$$Z_{n-1} = \left(R_{P(2n-3)} + R_{N(2n-1)}\right) - j\left({}^{1}/_{\omega C_{2n-3}} + {}^{1}/_{\omega C_{2n}}\right), \tag{53}$$

$$Z_n = \left(R_{P2(n-1)} + R_L\right) - j\left({}^{1}/_{\omega C_{2n-1}}\right), \tag{54}$$

where, Z_n is the n^{th} charge carrying path of charge pump impedance, n = 1, 2, …, n. The total impedance of the charge pump network is,

$$Z_{CP} = {}^{1}/_{\sum_1^n \left({}^{1}/_{Z_n}\right)}. \tag{55}$$

The effective impedance decreases with increasing number of charge pump stages (n). The model based calculations of three-stage of the charge pump impedance variation with charge pump capacitance (identical capacitors for all stages) are depicted in Figure 4.10, for 10 pF resonator capacitor and 4 kΩ load resistance. For the large charge pump capacitors, the impedance response has low variation compared to the smaller charge pump capacitors due to the corresponding variation of frequency. However, the impedance increases with MOSFET resistance.

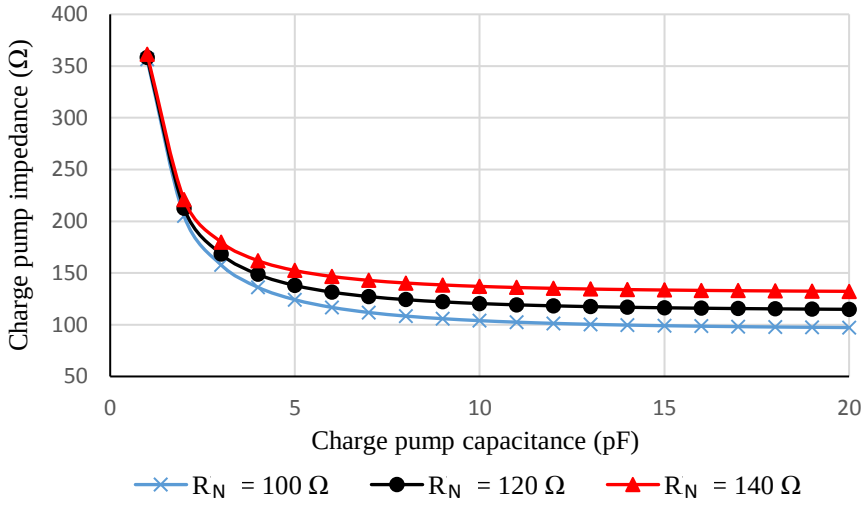

Figure 4.10. The variation of charge pump impedance with charge pump capacitors.

4.3.3 DC-DC converter optimization

Optimal device parameters are essential to achieve high performance at ultra-low voltage, micro-power electronics such as ambient energy harvesting devices. Therefore, novel model based optimization methods have been implemented to enhance the performance of the DC-DC converter in efficiency, circuit area, and charge drivability.

4.3.3.1 Simplified half circuit model for impedance matching

Since the DC-DC converter consists of a charge pump driven by an LC tank circuit, charge pump impedance (Z_{CP}) should be equal to resonator impedance at the operating frequency (ω), to achieve maximum power transfer. The governing equation for the lumped element half-circuit model for the n-stage charge pump coupled LC tank can be written as,

$$R_P = {1}\Big/{\sum_1^n \left({1}/{Z_n}\right)}. \tag{56}$$

Substituting oscillation frequency from equation (49), equation (56) can be rearranged as,

$$\frac{L}{R_s(C_0 + C_{P1})} = {1}\Big/{\sum_1^n \left({1}/{Z_n}\right)}. \tag{57}$$

For the circuit design convenience, the NMOSs, PMOSs, and capacitors are selected as identical for all stages resulting in this relation:

$$\frac{R_s(C_0 + C_{P1})}{L} = \frac{n-1}{(R_{P1} + R_{N1}) - j\left({}^{2}/_{\omega C_{P1}}\right)} + \frac{1}{(R_L + R_{N1}) - j\left({}^{1}/_{\omega C_{P1}}\right)}. \quad (58)$$

As described earlier, the lower ON resistance of the charge pump MOSFETs leads to reduced losses. Increasing MOSFET width increases parasitic capacitance as shown in Figure 4.11 for the low voltage UMC 180 nm CMOS process at 240 nm minimum channel length, in addition to increasing leakage current. The increased switching capacitance of the MOSFETs increases the dynamic power dissipation while the leakage current increases the static power dissipation. Therefore, 90-120 µm NMOS width is the optimal range for the DC-DC converter circuit because of the low capacitive and leakage effect, and low active resistance.

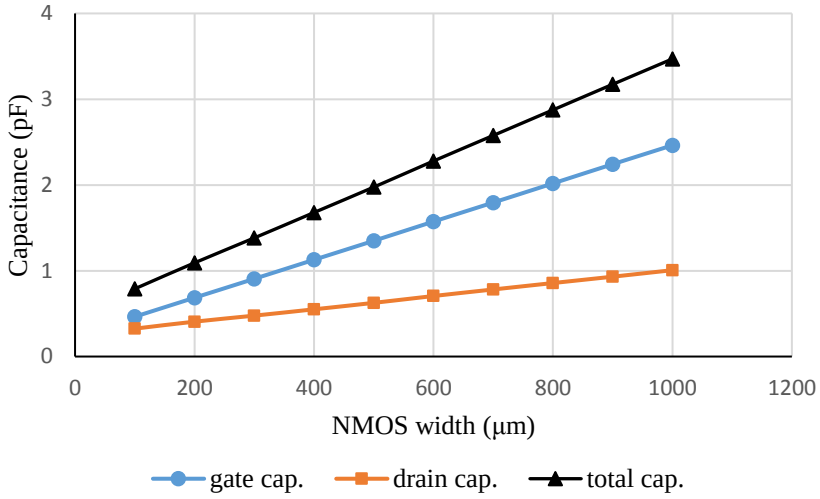

Figure 4.11. The variation of NMOS capacitance with NMOS width.

4.3.3.2 Simplified half circuit model for power calculations

The lumped element half circuit of n-stage DC-DC converter model consists of L, R, C components as illustrated in Figure 4.12 for the power analysis. Similar to impedance matching half-circuit model, all the charge carrying MOSFETs are represented with individual resistors. The capacitance of the cross-coupled N-channel MOSFETs is accounted for the power dissipation calculations. The first-stage charge carrying NMOS connected capacitor (C_2) is modeled with an equivalent parallel capacitor, which is in parallel with an oscillator capacitor (C_L). The selection of the charge pump MOSFETs is similar to the impedance matching technique.

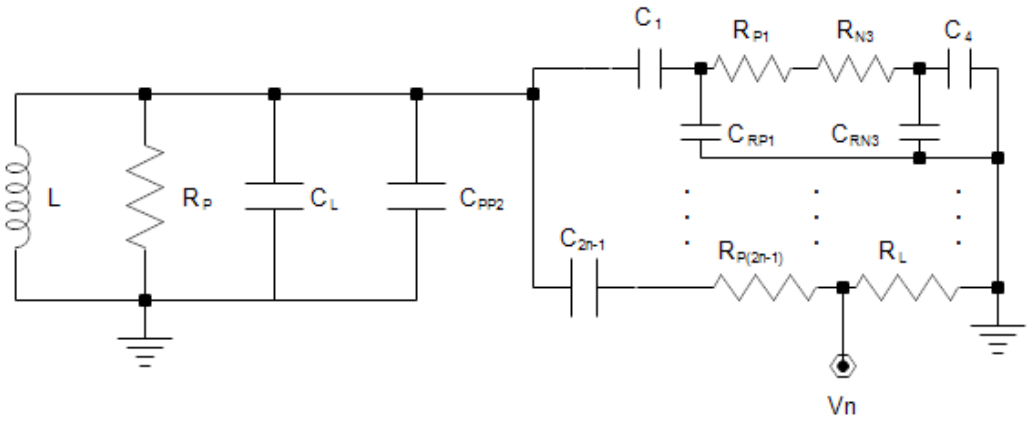

Figure 4.12. Half circuit model of a DC-DC converter for power analysis.

For the clock signal with peak amplitude of V_{pp}, the output voltage of n-stage DC-DC converter is,

$$V_n = \left(\frac{1}{\sqrt{2}} V_{pp}\, e^{\frac{-t}{C_1(R_{P2}+R_L)}} + V_{n-1}\right) \times e^{\frac{-t}{C_1(R_{P2}+R_L)}} \times \left(1 - \frac{R_{P(2n-1)}}{(R_L + R_{P(2n-1)})}\right), \qquad (59)$$

where V_0 is the DC-DC converter source voltage (V_{DD}) and t represents the half period of DC-DC converter clock signal. The output power of the DC-DC converter is,

$$P_n = \frac{V_n^2}{R_L}, \qquad (60)$$

The total power consumption of the single-stage DC-DC converter is the summation of output power, LC tank power consumption, and power consumption of charge pump capacitors, the power dissipation of charge pump MOSFET parasitic capacitors and charge carrying resistors. However, the power consumption due to the MOSFET resistance is negligible given the current flow in the order of several hundreds of micro-Amps flowing through the MOSFETs. The charge pump capacitors are able to preserve a roughly constant voltage across, except the first stage capacitors. Therefore, only the first stage charge pump capacitors account for the power dissipation and are modeled as parallel capacitors with LC tank capacitor. The total power consumption of the DC-DC converter is,

$$P_{nt} = P_n + \frac{V_{pp}^2}{8}\left[\frac{1}{R_{DS}} + \frac{C_L \omega}{2\pi}\right] + \left(\frac{V_{pp}}{2\sqrt{2}} - V_{DD}\right)^2 \frac{C_{1P}\omega}{2\pi} + \sum_{n=1}^{n} \frac{V_{pp}^2}{16\pi} C_n \omega\,, \qquad (61)$$

Where C_n ($C_n = C_{RPn} + C_{RNn}$) is the summation of the parasitic capacitance of charge pump NMOS and PMOS, but for the high current through the load, the power consumption of the last stage PMOS should be accounted for the total power of the DC-DC converter.

4.3.3.3 Optimization methodology

The oscillation amplitude is a critical parameter for DC-DC converter performance. Therefore, to implement the maximum quality factor and parasitic capacitance for the resonator the first step is to select the maximum inductor size according to the available on-die area. The maximum inductor width decreases the internal resistance of the inductor. The self-resistance of the inductor (R_S) and inductor parasitic capacitance can be extracted from the corresponding CMOS technology. A number of charge pump stages should be selected according to the output voltage using the rough estimation of voltage gain of 3+1.5(n-1) where n is the number of stages. The next step is to determine the relationship between C_0 and C_{P1} using equation (58) for the known load resistance, number of stages, and charge pump MOSFET resistors. The charge pump N-channel MOSFETs should be determined using the characteristic curves to give the low resistance and low capacitance. PMOS size is selected according to the mobility of the technology to keep similar rising and falling time of NMOS and PMOS. Then C_1 is calculated in terms of C_0 by substituting C_{P1} in equation (50). The half-period time of the DC-DC converter is calculated in terms of L and C_0 by substituting relation of C_0 and C_1 in equation (49). The optimal charge pump capacitance for maximum output power can be calculated by substituting above relation into equation dP_n/dC_1. C_0 and C_{P1} can be calculated using the optimal C_1. Required minimum transconductance (g_m) of LC tank NMOS is calculated using equation (62). The minimum MOSFET channel length (L_{MOS}) is determined using equation (63) for the proper operation under the low voltage. V_{gs}, V_t, W, K_P refer to MOSFET gate to source voltage, the threshold voltage of MOSFET, MOSFET width, and a constant for the CMOS technology, respectively. Then LC tank NMOS capacitance is determined by simulations or standard equations. Equation (58) is reused to calculate the charge pump optimal capacitance.

$$g_m \geq \frac{R_S}{R_S^2 + {}^{L}/_{(C_0 + C_{P1})}}, \tag{62}$$

$$L_{MOS} = \frac{(V_{gs} - V_t)\, W\, k_p}{g_m}. \tag{63}$$

Similarly, the input to output power transfer equation can be used to determine the optimal device parameters to achieve maximum efficiency in a given device area. The design parameters of the optimized DC-DC converter are illustrated in Table 4.1, in reference to Figure 4.3. In order to achieve a large MOSFET width such as 100 μm, the fingered layout is

preferred in UMC 180 CMOS process. Maximum width is used for inductor metal to minimize the self-resistance of the inductor.

Table 4.1. The design parameters of voltage doubling LC tank connected DC-DC converter.

Component	parameters	UMC_18_CMOS cell name
M_1 & M_2	W/L = 400 µm/240 nm Multiplier = 5	N_LV_18_MM
L_1 & L_2	Inductance = 14 nH Width = 20 µm Turns = 5.5 Diameter = 238 µm	L_SLCR20K_RF
charge pump NMOS	W/L = 100 µm/240 nm Multiplier = 1	N_LV_18_MM
charge pump PMOS	W/L = 150 µm/240 nm Multiplier = 1	N_LV_18_MM
charge pump capacitors	C = 10 pF	MIMCAPS_MM

4.3.4 Model verification by simulations

According to the model based analysis, the resonator impedance is equal to the charge pump impedance at 11 pF of charge pump capacitance and 2 kΩ of load resistance as illustrated in Figure 4.13. However, the charge pump impedance and LC tank impedance are close to each other in the 6-15 pF range of charge pump capacitances. The optimal charge pump capacitance slightly increases with the increase of load resistance at 10 kΩ impedance as illustrated in Figure 4.14. The higher charge pump capacitors allow increasing the efficiency and power output of the DC-DC converter while sinking more power into the DC-DC converter. However, the larger capacitors occupy significant on-die area. Charge pump capacitors of value < 5pF reduce the design area but decrease the design efficiency and power delivery. According to the model calculations, the optimized DC-DC converter input impedance is < 200 Ω. Therefore, this DC-DC converter is suitable for the thermoelectric energy harvesting applications as the thermoelectric harvester output impedance is < 10 Ω [86], [87].

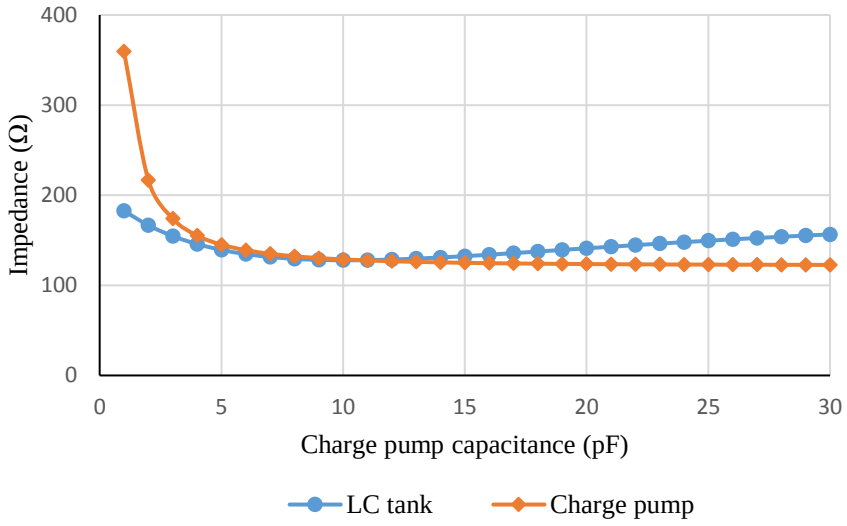

Figure 4.13. The variation of impedance with charge pump capacitance at 2 kΩ load.

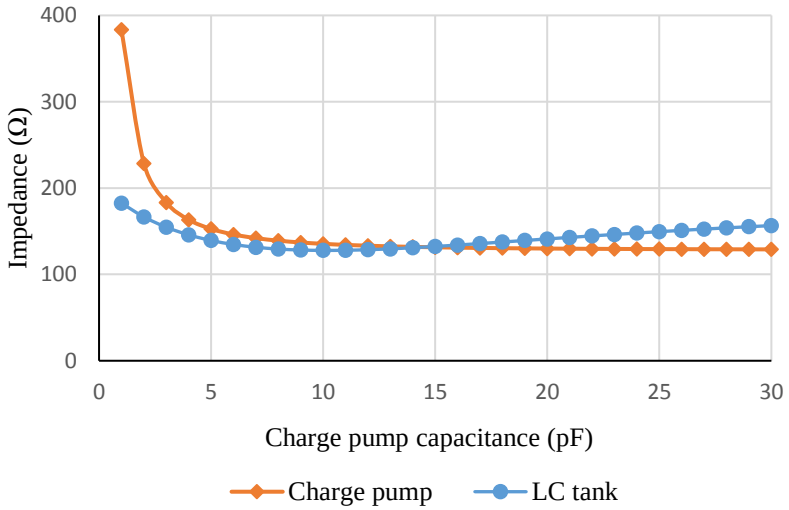

Figure 4.14. The variation of impedance with charge pump capacitance at 10 kΩ load.

The simulated DC-DC converter output voltage is depicted in Figure 4.15 along with the model results for the 1-3 stages at 10 pF charge pump capacitance and 14 nH oscillator inductance. The output voltage increases with the DC-DC converter stages. However, the minimum load condition for the steady state output increases with the charge pump stages. This is because the additional charge pump stages cause decrease of charge pump impedance. Therefore, higher load resistance is necessary to increase charge pump impedance and match with the LC tank impedance for proper operation.

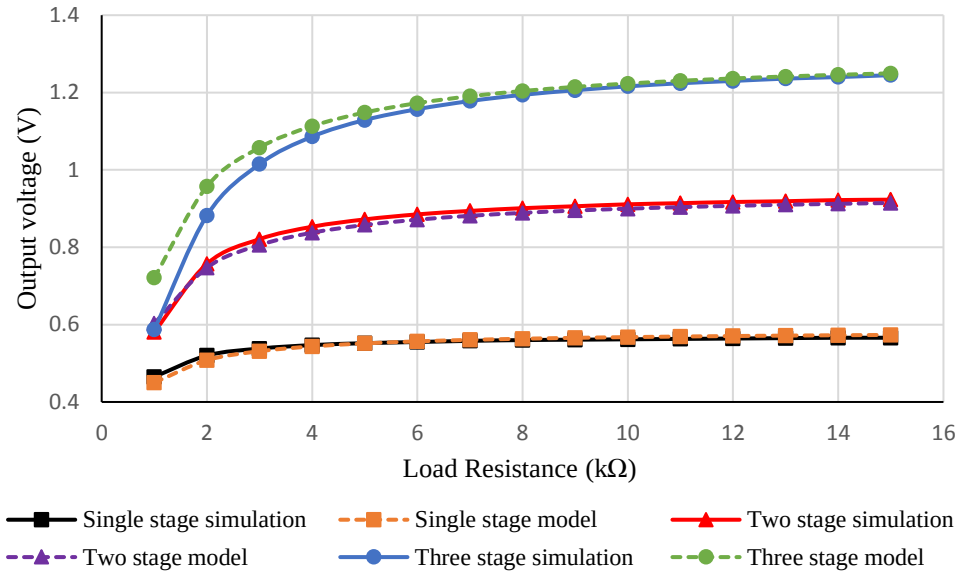

Figure 4.15. The variation of output voltage with load resistance for 1-3 stages.

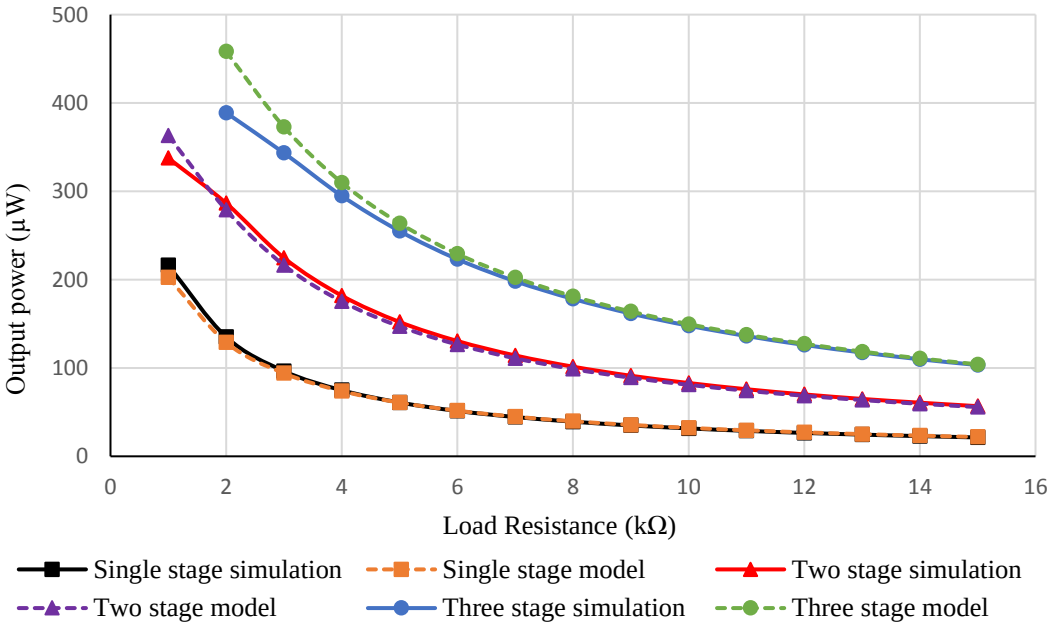

Figure 4.16. The variation of output power with load resistance for 1-3 stages.

The output power characteristics of the DC-DC converter is inversely related with the load resistance as illustrated in Figure 4.16. The added charge storing capacitors increase the output and input power of the DC-DC converter. In addition, the DC-DC converter is failing or partially operates at low load resistance because the oscillator is unable to deliver the necessary high load current. As a result, the simulation observations have some discrepancy with model based calculations at low load conditions (before they reach the steady state condition). The

optimized DC-DC converter can achieve > 48% peak efficiency for each stage as shown in Figure 4.17. According to the model analysis, the equivalent charge pump impedance and LC tank impedance should achieve 50% peak efficiency. The lower load resistance decreases the charge pump impedance and improves the peak efficiency. The DC-DC converter fails to operate at the condition of LC tank impedance > charge pump impedance. Therefore, the curves are starting from the operating DC-DC converter load resistance at the ultra-low input. However, the maximum amplitude of the power efficiency curve is shifted to the right-hand side with increasing DC-DC converter stages. Since the charge pump stages are parallel to each other, each stage contributes to a decrease in the charge pump impedance. Therefore, load resistance should increase with the charge pump stages for impedance matching. This observation validates and proves the accuracy of the model results.

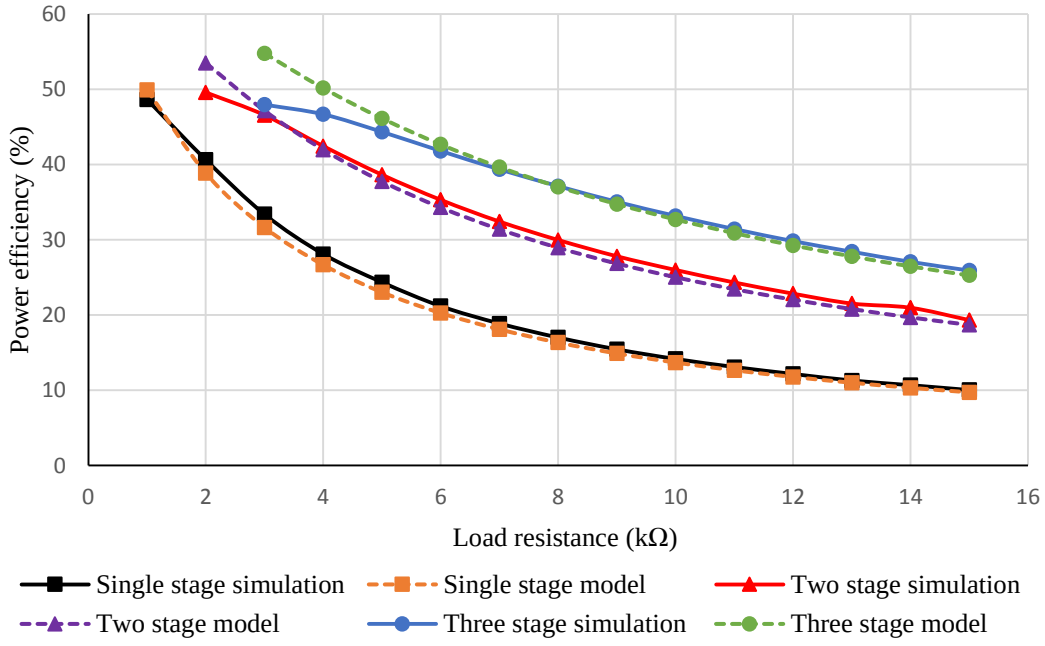

Figure 4.17. The variation of power efficiency with load resistance for 1-3 stages.

The optimized 4-stage and 5-stage DC-DC converter can achieve 1.5 V and 1.8 V at 8 kΩ and 9 kΩ respectively for 0.2 V input voltage as depicted in Figure 4.18. The 4-stage and 5-stage converters yield 51 % and 51.7 % maximum efficiency for 5 kΩ and 6 kΩ loads, respectively at 0.2 V input as illustrated in Figure 4.19. However, peak efficiency decreases with the reduction of input voltage to 31% at 0.15 V input. The efficiency variation decreases with the increase of the DC-DC converter stages. Therefore, the change of gradient decreases with increasing of the DC-DC converter stages. The maximum efficiency and maximu power of the DC-DC converter is yield for the low load resistance such as > 1 kΩ and < 10 Ω. Therefore, the present DC-DC converter is suitable for the low input impedance load applications like

biomedical pressure sensors [88], parallel set of temperature sensors [89], micro power voice band audio codec [90], and parallel array of micro power sensosors. The active load resistance of the sensor network is rapiedly change with the number of active sensors. Therefore, the optimizations should follow for the average load resistance according to he application environment.

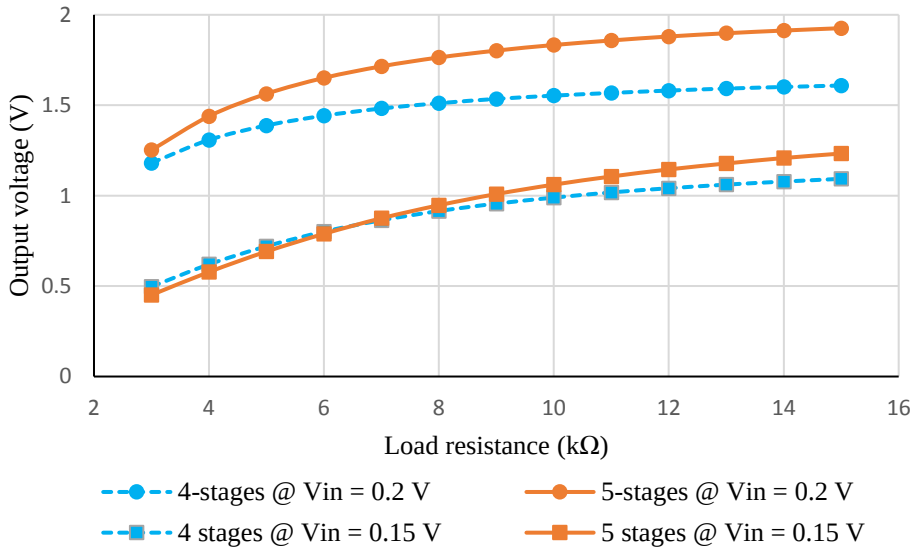

Figure 4.18. Variation of output voltage with load resistance for 4 & 5 stages @ 0.2 V, 0.15 V inputs.

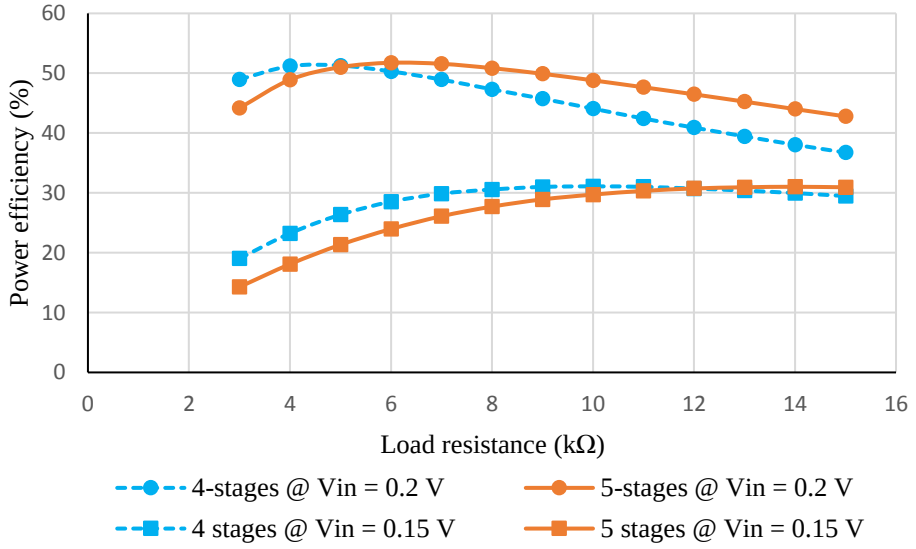

Figure 4.19. Variation of power efficiency with load resistance for 4 & 5 stages @ 0.2 V, 0.15 V inputs.

4.4 Voltage quadrupling LC tank coupled DC-DC converter architecture

A fully integrated DC-DC converter is illustrated in Figure 4.20 with only two stages of a charge pump for clarity. The output nodes of the LC tank based oscillator are coupled with charge pump capacitors without any buffer circuits. The higher clock amplitude of the oscillator enables fewer number of DC-DC converter stages for any target output voltage and power. The required additional area for the bulky inductors is the main drawback of this design while the lower impedance of the LC tank makes it feasible to operate with lower load resistance, and deliver higher output current.

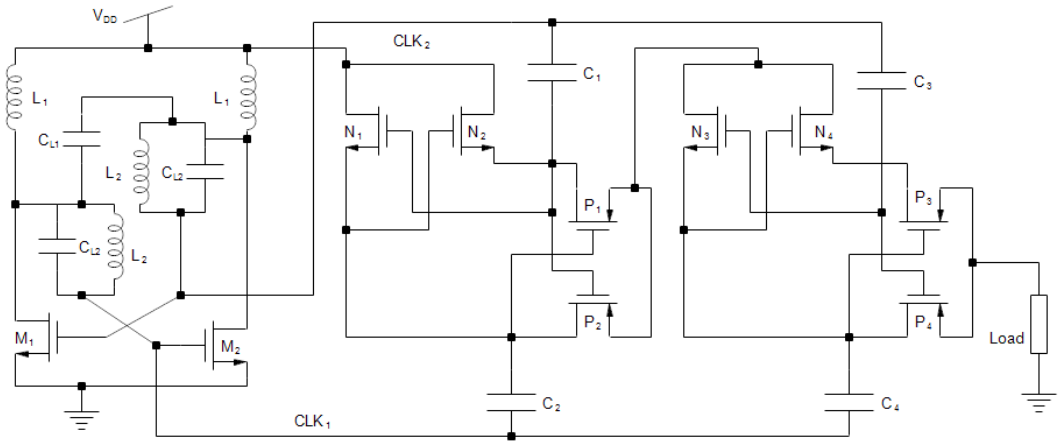

Figure 4.20. Two stages of the DC-DC converter with voltage quadrupling LC tank.

The DC-DC converter oscillation frequency variation with the charge pump capacitors is not significant but can be modeled as a corresponding equivalent parallel capacitor of a series capacitor. Since the charge pump capacitors are clock coupled, they adversely affect the oscillation amplitude. However, the secondary resonator capacitor (C_{L2}) causes higher amplitude while consuming additional power. For the rough estimation of power consumption, the capacitor associated energy loss can be calculated in a similar way to the voltage doubling LC tank. Since the power consumption of the LC tank is significant, the minimum LC tank circuit parameters which give the lowest energy losses should be used for the DC-DC converter efficiency. However, the larger secondary resonator oscillator capacitance is an advantage for the high output power requirement with low input voltage when input power is available in the application. The impedance matching technique helps to improve design performances like efficiency and optimal power output under a specific/some application criterion.

4.4.1 Simplified half-circuit model for impedance matching

The lumped element half-circuit model of n-stage of the DC-DC converter with voltage quadrupling LC tank is depicted in Figure 4.21. The charge pump MOSFETs are modeled as a series resistance with parasitic capacitance ignored. Primary LC tank of the voltage quadrupling LC tank oscillator is modeled as a parallel inductor (L), resistor (R_P) and capacitor (C_{L1}). R_P, C_{L1} represents the equivalent parallel resistance of L_1 inductor and the total capacitance between LC tank NMOS drain terminal and AC ground. Secondary LC tank is modeled as C_{L2} capacitor parallel with the series combination of L_2 inductor and self-resistance of the inductor (R_S). C_{O1} is the total capacitance at LC tank NMOS gate terminal referenced to AC ground, including the corresponding equivalent parallel capacitance of the first stage charge pump capacitor.

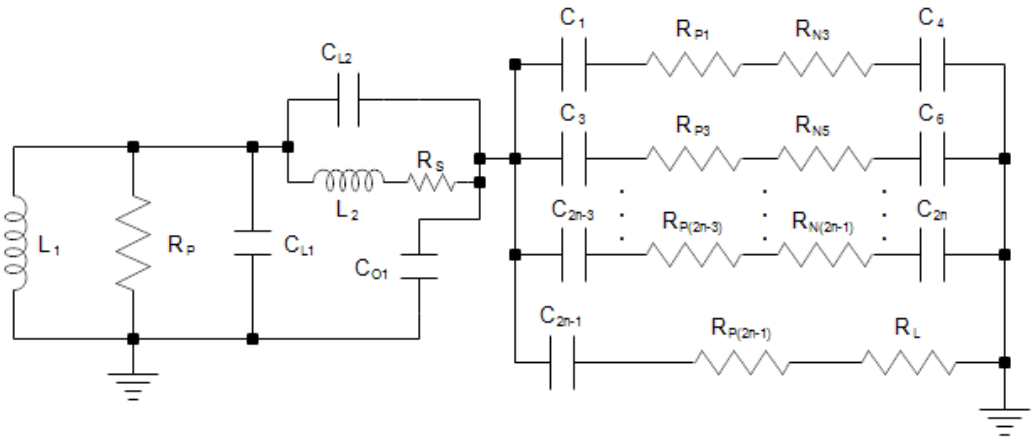

Figure 4.21. The lumped element half circuit model of the n-stage DC-DC converter with voltage quadrupling LC tank.

The n-stage of charge pump impedance is given in equation (55). The primary (Z_{LC1}) and secondary (Z_{LC2}) resonator impedance are given by,

$$Z_{LC1} = \frac{j\omega L_1 R_P}{R_P(1-\omega^2 L_1 C_{L1}) + j\omega L_1}, \tag{64}$$

$$Z_{LC2} = \frac{j\omega L_2 + R_S}{(1-\omega^2 L_2 C_{L2}) + j\omega C_2 R_S} \ . \tag{65}$$

The total impedance of voltage quadrupling LC tank which couples to the charge pump is,

$$Z_{LC} = \frac{Z_{LC1} + Z_{LC2}}{j\omega C_{O1}\,(Z_{LC1} + Z_{LC2}) + 1}. \tag{66}$$

4.4.2 Optimization methodology

The selection of charge pump MOSFETs and oscillator inductors is similar to the voltage doubling LC tank coupled DC-DC converter optimization process. After selection of inductors and charge pump MOSFET parameters, the characteristics of the components are determined by simulation method or standard work sheet. DC-DC converter frequency does not significantly vary with charge pump capacitor values. Therefore, charge pump capacitors can be ignored in oscillation frequency calculations in equation (43). Since the expected theoretical output peak amplitude of the LC tank is $4V_{DD}$ and NMOS gate amplitude is $3V_{DD}$ as explained in chapter 3, the equation (36) and equation (42) provide the relation between C_{L1}, C_{L2}, and C_L. Another relation between C_{L1}, C_{L2}, and C_L can be determined by applying the minimum conditions in Equation (45). For the continuous oscillations, the minimum requirement is to compensate the real losses of the resonator from negative resistance created by the cross coupled NMOS pair. Therefore, the real component of the charge pump impedance can substitute the absolute negative resistance of the NMOS cross coupled pair ($1/g_m$) in equation (44), and determines another relationship for capacitors. This impedance matching allows achieving maximum efficiency for the system. For the desired load condition, equation (55) and (66) can be used to derive other equations for the DC-DC converter (equating imaginary component of charge pump and tank impedance, and similarly real components). Now the derived four equations can be used to determine the unknown values of four capacitors. Then minimum transconductance of NMOS can be calculated from equation (44) by substituting the capacitor values and other circuit parameters. After characterizing the NMOS process parameters using simulations, the NMOS gate capacitance and drain capacitance are extracted and substituted into the equations. Similarly, the parallel charge pump capacitor in frequency equation should be included to recalculate the exact values of capacitor sizes by following the same procedure.

The design parameters of the optimized DC-DC converter are illustrated in Table 4.2, referring to the Figure 4.20. The voltage quadrupling LC tank parallel resistance is less than that of the voltage doubling oscillator. Therefore, the optimized charge pump NMOS is larger in voltage quadrupling LC tank for the large transconductance. The larger NMOS causes more current and increases the power dissipation as a drawback for the design; the higher current reduces the power efficiency. Hence, voltage quadrupling LC tank design provides a tradeoff between output power capacity and voltage, and efficiency.

Table 4.2. The design parameters of voltage quadrupling LC tank connected DC-DC converter.

Component	parameters	UMC_18_CMOS cell name
M_1 & M_2	W/L = 600 µm/240 nm Multiplier = 5	N_LV_18_MM
L_1 & L_2	Inductance = 14 nH Width = 20 µm Turns = 5.5 Diameter = 238 µm	L_SLCR20K_RF
C_{L1}	C = 6 pF	MIMCAPS_MM
C_{L2}	C = 10 pF	MIMCAPS_MM
charge pump NMOS	W/L = 100 µm/240 nm Multiplier = 1	N_LV_18_MM
charge pump PMOS	W/L = 150 µm/240 nm Multiplier = 1	N_LV_18_MM
charge pump capacitors	C = 10 pF	MIMCAPS_MM

4.4.3 Simulation results

The output voltage dependency of 2-4 stages of the DC-DC converter is depicted in Figure 4.22, for secondary resonator capacitor of 10 pF and 25 pF at 0.2 V input voltage. Despite the oscillator peak amplitude increase with secondary LC tank capacitance, the secondary capacitor is inversely related to the DC-DC converter output voltage. The larger secondary LC tank capacitors increase the time constant. As a result, the charge transfer from one stage to next is decreased, which causes the output power to decrease with C_{L2} as illustrated in Figure 4.23. DC-DC converter output voltage increases with number of stages, as expected. The minimum load resistance for the steady state output increases as the number of stages increases. However, the DC-DC converter fails to operate at low load conditions, the load resistance for the steady state operation is increased with the DC-DC converter stages.

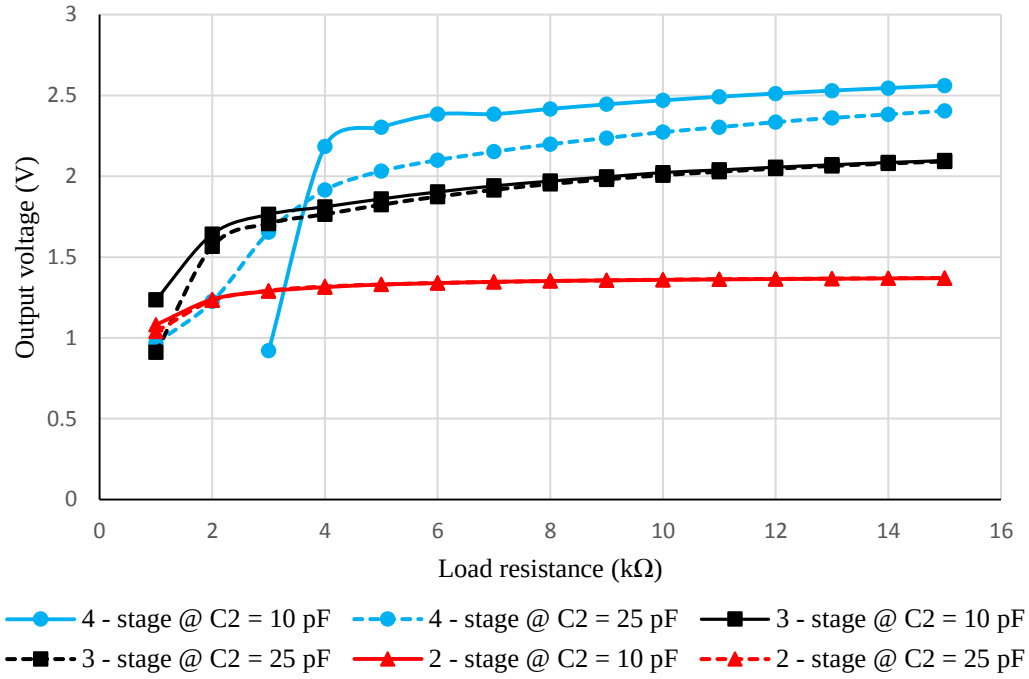

Figure 4.22. The variation of output voltage with load resistance and secondary resonator capacitor value for 2-4 stages.

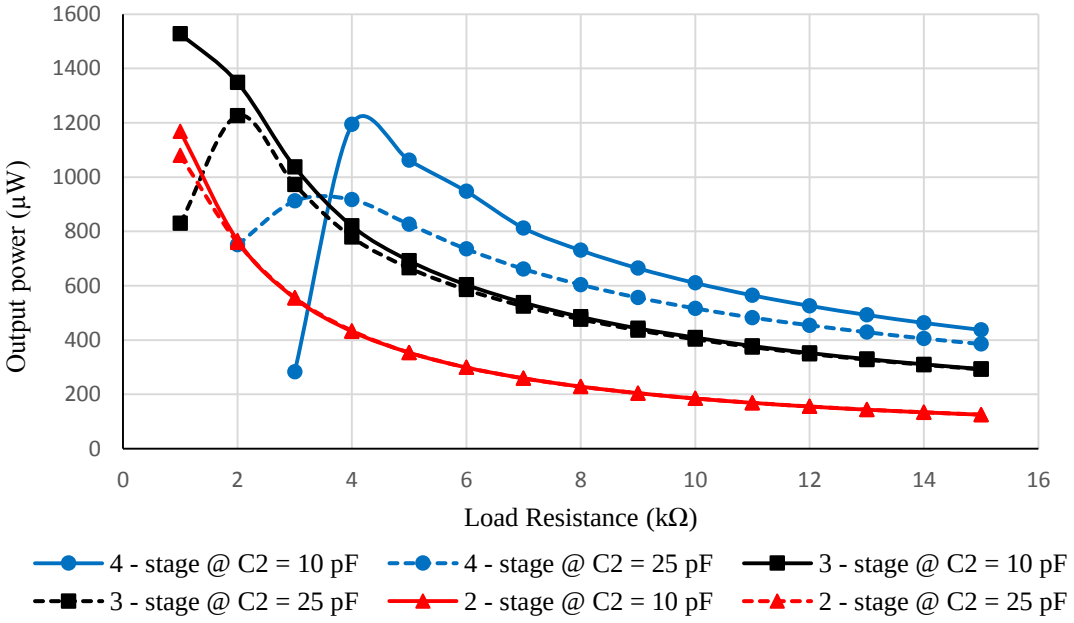

Figure 4.23. The variation of output power with load resistance for 2-4 stages.

The optimized 2-4 stages DC-DC converter can achieve efficiencies of 43% at 1 kΩ load, 40% at 2 kΩ, and 34% at 4 kΩ load, respectively as depicted in Figure 4.24. Since the power consumption of the LC tank is significant, DC-DC converter efficiency decreases with the load resistance after steady state operation due to the output power decrease. The maximum

efficiency of the DC-DC converter is obtained for a finite load condition which creates the equivalent charge pump impedance with oscillator impedance. For the low load resistance, the charge pump impedance is less than the oscillator impedance. Therefore, oscillator is unable to drive the charge pump, and the efficiency, output power, and output voltage are lower than the peak values. For large load resistors, charge pump impedance is greater than the oscillator impedance and the output voltage increases with load resistance. However, the large load resistors limit the load current and cause the decrease of output power and efficiency.

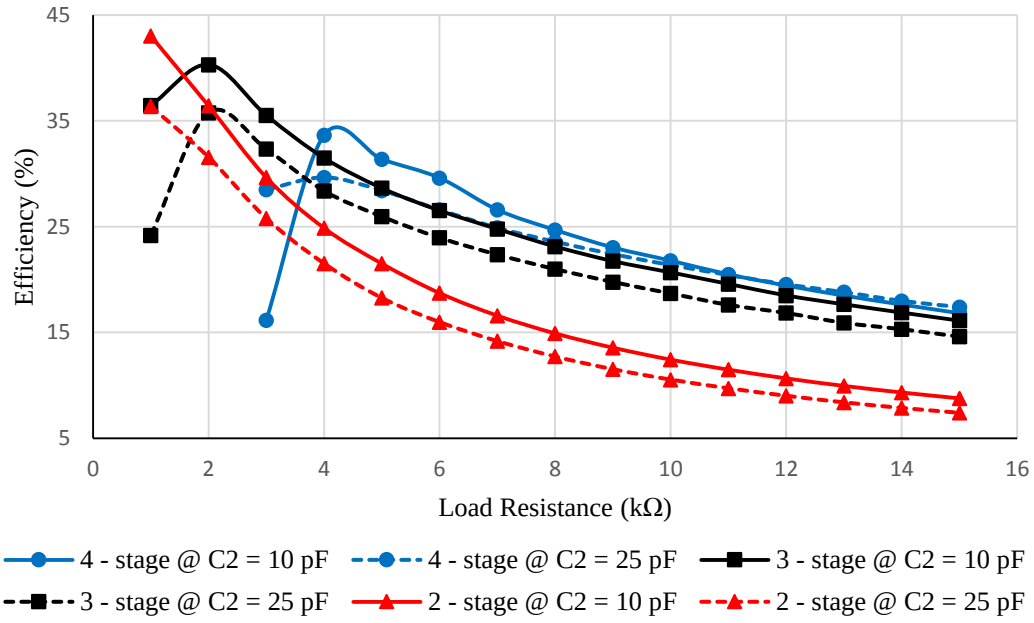

Figure 4.24. The variation of efficiency with load resistance for 2-4 stages.

The high power transfer capacity and high voltage gain are the main advantage of this design even for large load resistors. But the required circuit area for the additional bulky inductors and high voltage ripple at MOSFET terminals are the main drawbacks of this high gain DC-DC converter topology.

The multi stage DC-DC converter design, modeling, and layout design are presented in next chapter. Simulation results and experimental results are provided for the model validation.

CHAPTER 5

5 DESIGN VALIDATION

5.1 Introduction

This chapter presents validation results from the fully integrated DC-DC converter test chip utilized to characterize the circuit performance in the laboratory environment. The test chip consists of a DC-DC converter with voltage doubling LC tank oscillator, and external switching mechanism for the number of charge-pump stages. The design is implemented in 180 nm standard CMOS technology in CAD environment. Pre- and post-layout simulations, and experimental results for the fabricated IC are presented in the following sections.

Chapter 5 is organized as follows: System block diagram, optimal circuit parameters, and layout design are presented in Section 5.2. Section 5.3 discusses the experimental setup for the system validation. Pre- and post-layout simulations as well as the experimental results from the fabricated test chip are discussed in Section 5.4. The post-layout simulation is initially completed by ignoring the parasitic resistance and then includes the parasitic resistance to show the variation of design efficiency and step-up performance with parasitic resistance. Section 5.5 describes the discrepancy between experimental results and measurements. Then the analytical explanation for the discrepancy is presented by taking parasitic resistance into account, and is validated using post-layout simulations. The self-resistance of the on-chip inductor is analytically estimated, and then validated using experimental curves. Section 5.6 presents the performance enhanced DC-DC converter design, layout, and post-layout simulations. Silicon performance for the newly proposed DC-DC converter is estimated based on model analysis to present an error range. Section 5.7 summarizes the performance comparison of the ultra-low voltage DC-DC converters available in the literature along with the proposed design.

5.2 Test chip design and layout

The test circuit interface consists of switching mechanism and DC-DC converter as illustrated in Figure 5.1. The DC-DC converter is coupled with an ultra-low voltage power source like micro scale thermoelectric energy harvester for the input power. The circuit is composed of four basic blocks including voltage doubling oscillator and 3-5 stage charge pump circuits. Each charge pump sub-block is connected to input and output switches for stage selection depending on load requirements. N-channel MOSFETs are used as input switches. Unlike the

ultra-low input voltage, the output is larger than the MOSFET threshold voltage. Therefore, transmission gates are used for output switches. Smoothing capacitors are integrated to minimize the input and output voltage ripple.

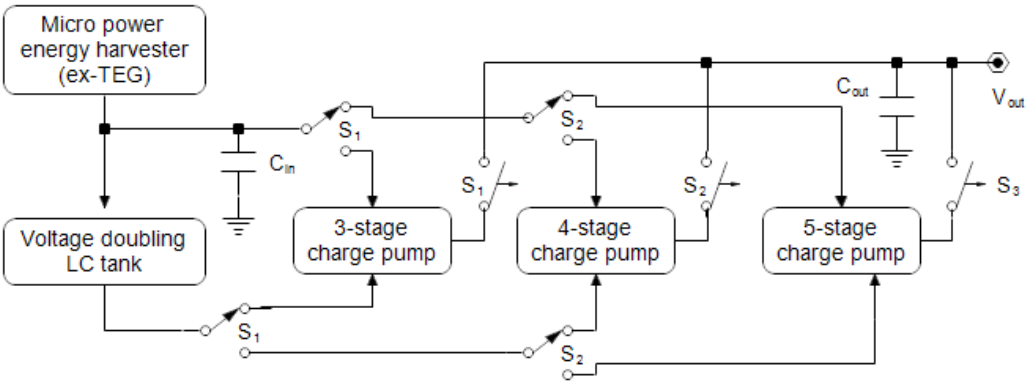

Figure 5.1. Block diagram of full chip design.

Full system layout is composed of DC-DC circuit topology and PAD connections as depicted in Figure 5.2. A, B, and C refer to the five-stage, four-stage, and three-stage charge pumps respectively, with corresponding capacitors. D is the LC tank cross-coupled NMOS pair for the oscillator switching mechanism. L represents the oscillator inductors, which occupy a relatively large area. The input and output smoothing capacitors are represented as E and F respectively. All the capacitors and inductors are shielded with ground to prevent magnetic and capacitive coupling effects. The system consists of 14 pins including ground connection, input, output, and DC-DC converter stage select pins. The layout picture of the LC tank NMOS pair is depicted in Figure 5.3. The design parameters of the circuit components are selected as in Table 5.1.

The design layout fits in an area of 1525 µm × 1525 µm including PAD connections. The LC tank oscillator occupies 0.79 mm^2 of the area while 0.23 mm^2 is used for the 5-stage charge pump. The design is packaged in QFN 48 for performance characterization in a laboratory environment. The bonding diagram and pin description of the fabricated IC are illustrated in Figure 5.4 and Table 5.2 respectively for design validation.

5.3 Experimental setup for system validation

QFN 48 package has been soldered on a test PCB for system validation in the laboratory environment. The 3-input power supply is used for the DC-DC converter input and stage selection switch controls. The output voltage is measured using a digital oscilloscope with a

10 MΩ probe. The test setup is depicted in Figure 5.5. The signal from the 5-stage DC-DC converter is shown in Figure 5.6 with negligible ripple.

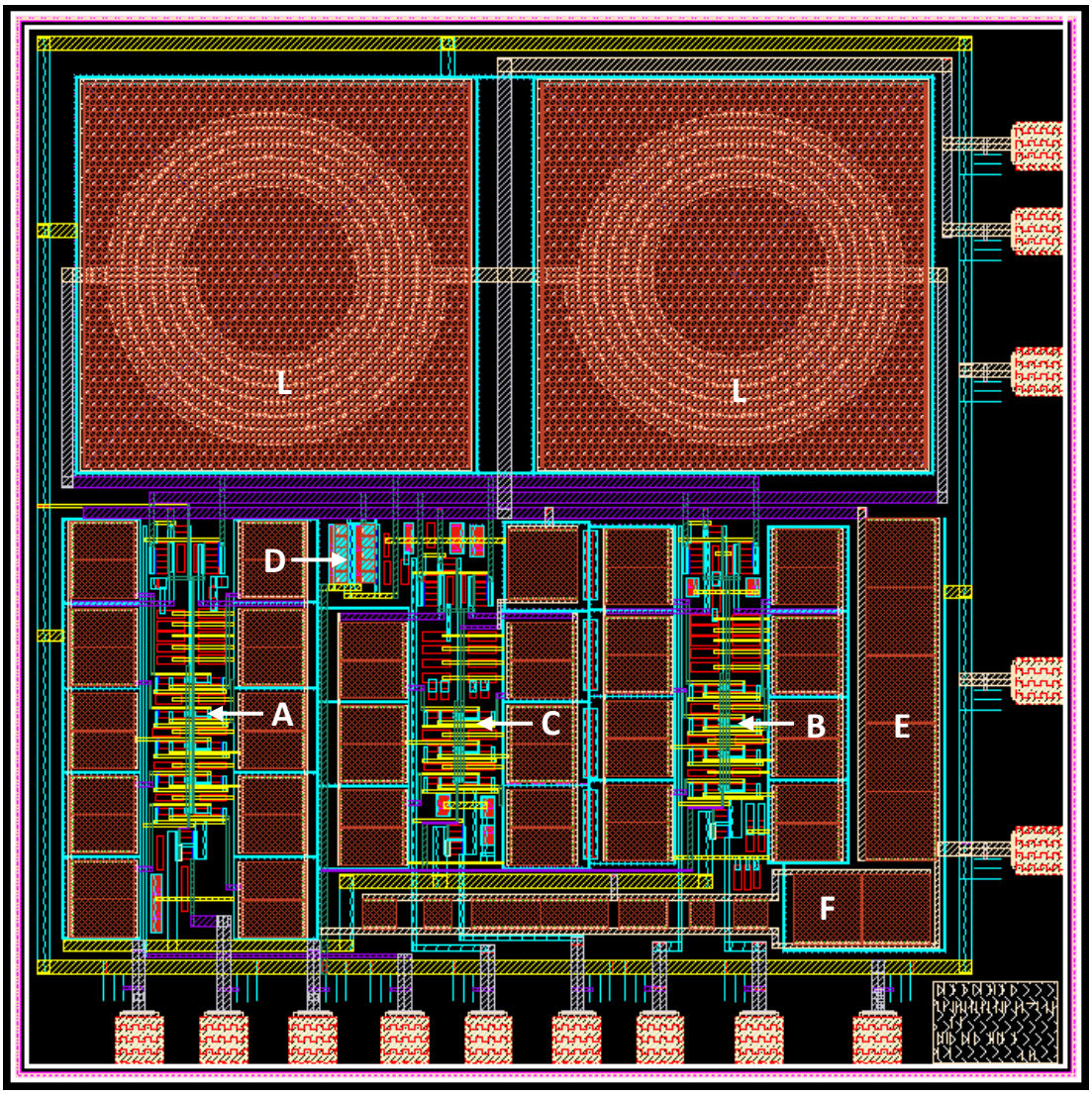

Figure 5.2. Test circuit layout with PAD connections.

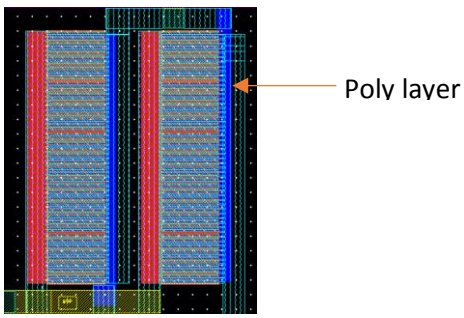

Figure 5.3. LC tank NMOS cross-coupled pair.

Table 5.1. Design parameters of the full system.

Component	parameters	UMC_18_CMOS cell name
LC tank NMOS	W/L = 400 μm/240 nm Multiplier = 5	N_LV_18_MM
LC tank inductors	Inductance = 14 nH Width = 20 μm Turns = 5.5 Diameter = 238 μm	L_SLCR20K_RF
Charge pump NMOS	W/L = 190 μm/240 nm Multiplier = 1	N_LV_18_MM
Charge pump PMOS	W/L = 150 μm/240 nm Multiplier = 1	N_LV_18_MM
Charge pump capacitors	C = 10 pF	MIMCAPS_MM
Input switch- NMOS (for clock signal)	W/L = 190 μm/240 nm Multiplier = 5	N_LV_18_MM
input switch- NMOS (for charge pump input)	W/L = 190 μm/240 nm Multiplier = 2	N_LV_18_MM
Output switch- NMOS	W/L = 190 μm/240 nm Multiplier = 2	N_LV_18_MM
Output switch- PMOS	W/L = 190 μm/240 nm Multiplier = 2	N_LV_18_MM
Input smoothing capacitor	C = 60 pF	MIMCAPS_MM
Output smoothing capacitor	C = 40 pF	MIMCAPS_MM

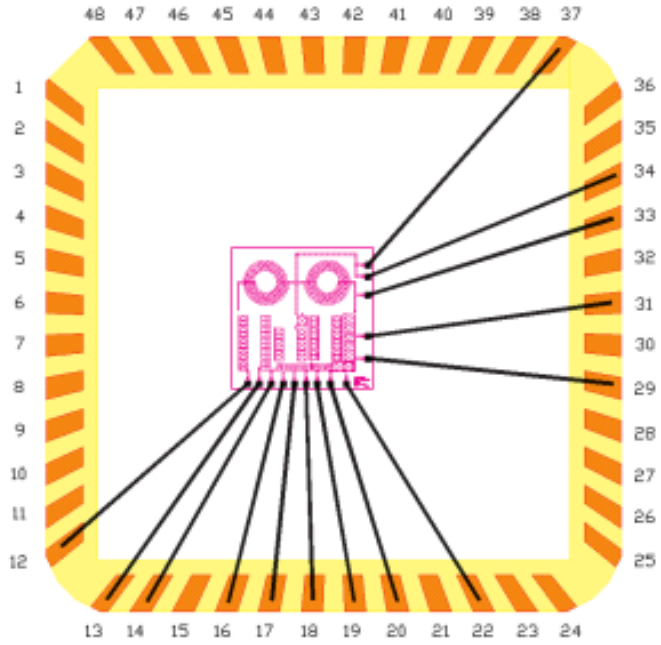

Figure 5.4. The bonding diagram of the fabricated IC.

Table 5.2. Pin description of the fabricated IC.

Pin number	Pin name	Description
34, 37	V_{in}	System input
12, 14	V_{out}	System output
16	V1	5-stage select NMOS switch
13	V2	5-stage select PMOS switch
19	V3	4-stage select NMOS switch
20	V4	4-stage select PMOS switch
17	V5	3-stage select NMOS switch
18	V6	3-stage select PMOS switch
22, 29, 31, 33	gnd	Ground connection

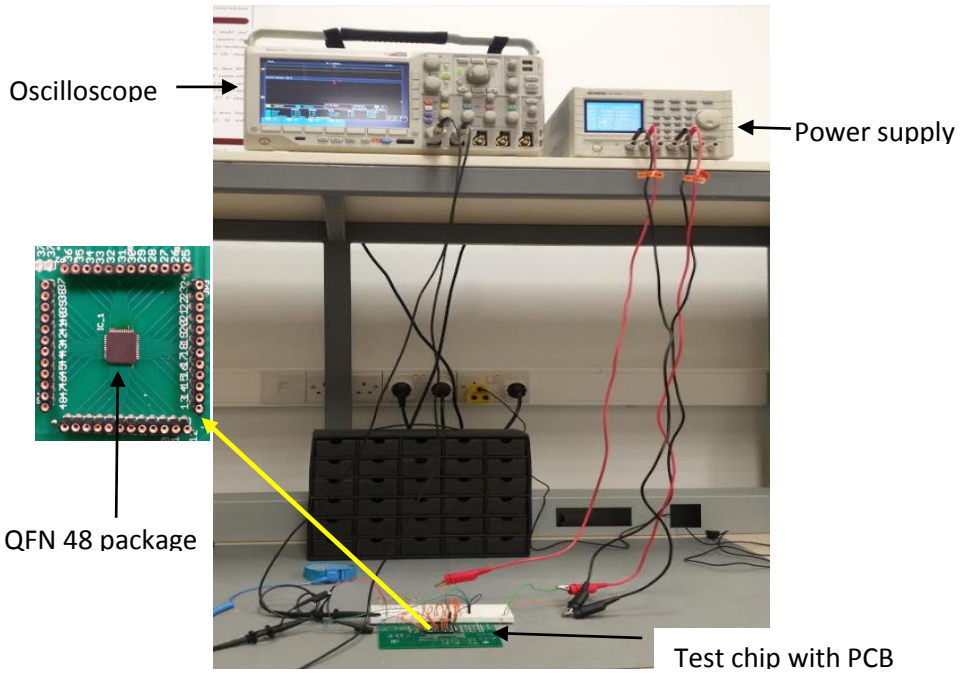

Figure 5.5. Experimental setup for the system validation.

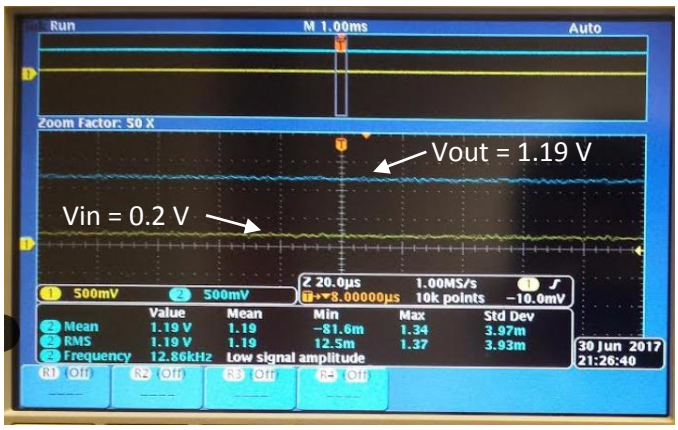

Figure 5.6. The screen shot of oscilloscope output for the 5-stage DC-DC converter.

5.4 Characterization

5.4.1 Post-layout simulations with parasitic capacitance extraction

According to the parasitic capacitance extracted post-layout simulations, 5- stage DC-DC converter can achieve 1.9 V output at 0.2 V input as illustrated in Figure 5.7. The 4-stage and 3-stage DC-DC converters can achieve 1.55 V and 1.27 V respectively at 14 kΩ load resistance. The 3- stage, 4- stage, and 5- stage of DC-DC converters reached peak efficiency of 46% at 3, 4, and, 6 kΩ load resistance respectively as illustrated in Figure 5.8. 5-stage has the maximum range of load resistance of efficiency greater than 35% compared to the rest.

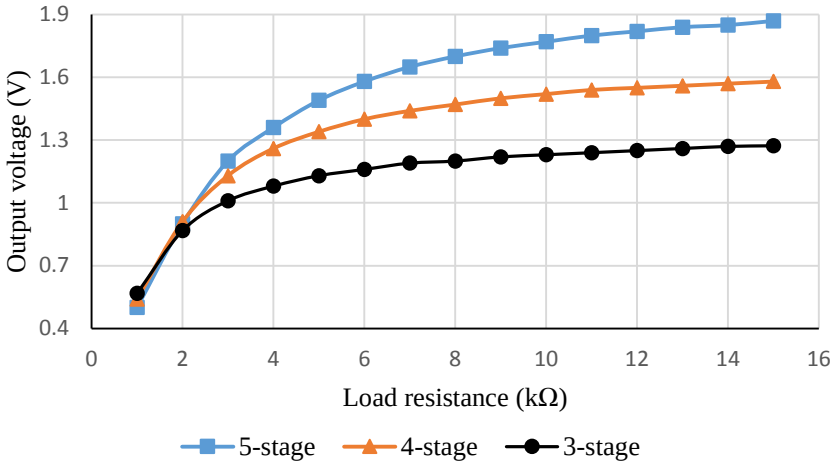

Figure 5.7. The variation of system output with load resistance (only C extraction).

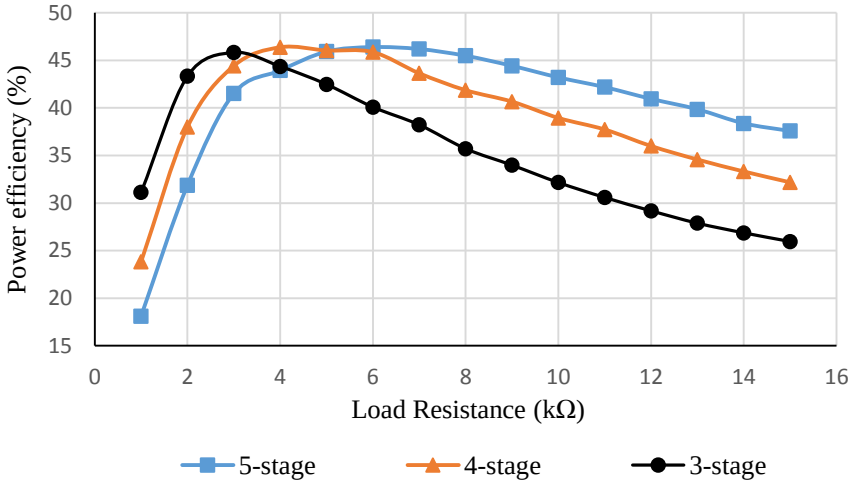

Figure 5.8. The variation of system efficiency with load resistance (only C extraction).

5.4.2 Post-layout simulations with parasitic LRC extraction

The output voltage and power efficiency of LRC-extracted simulation results are much lower than the pre-layout and C-extracted simulations for 0.2 V input, as illustrated in Figure 5.9 and Figure 5.10 respectively. This discrepancy is caused by the parasitic resistance of LC tank cross coupled NMOS pair, which reduces the oscillation amplitude. The LC tank performance is sensitive to the series resistance of the inductor and NMOS. In fact, the amplitude of LC tank output decreased, and the power consumption increased due to the additional parasitic resistance. The characteristic of the DC-DC converter is analyzed using experimental results to enhance the theoretical model.

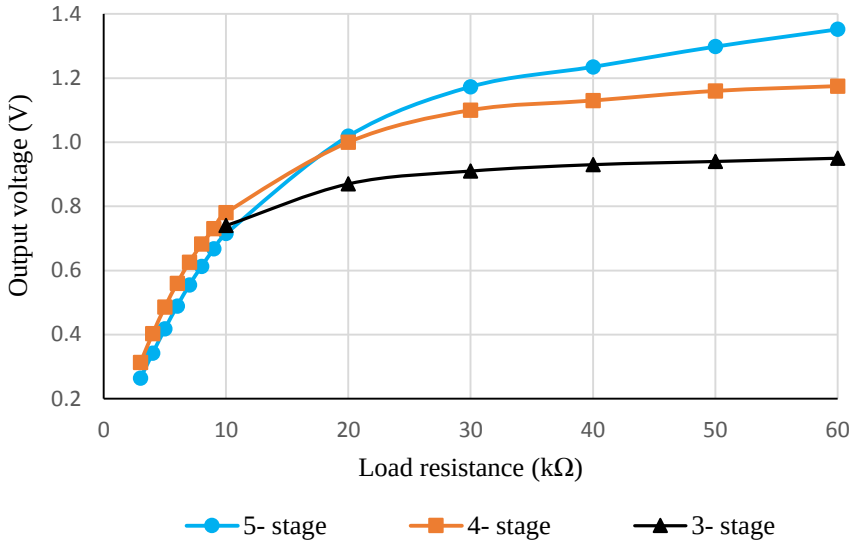

Figure 5.9. The variation of system output with load resistance (LRC extraction).

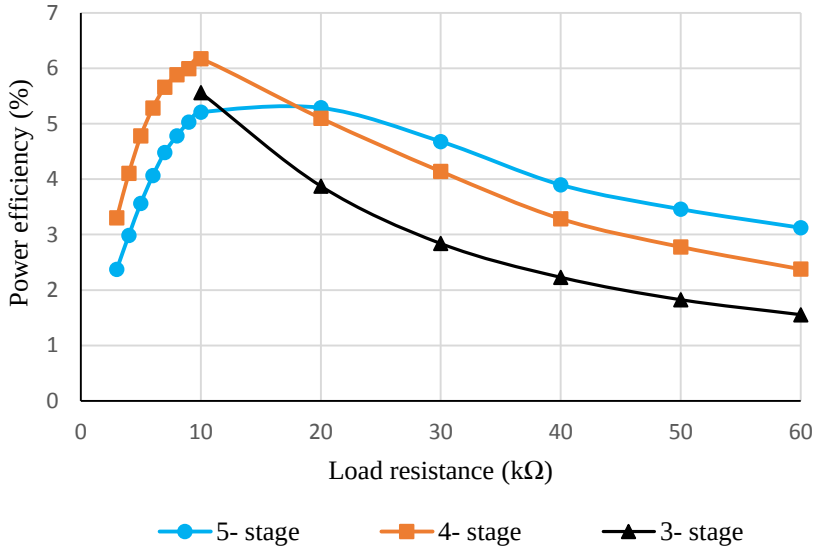

Figure 5.10. The variation of system efficiency with load resistance (LRC extraction).

5.4.3 Experimental results

The voltage characteristic curves of the 5-stage DC-DC converter are significantly lower compared to the pre-layout simulation as depicted in Figure 5.11. The circuit can achieve 1.5 V at a load resistance of 10 kΩ and 0.35 V input voltage, 20 kΩ load and 0.30 V input. For 0.2 V input, the open circuit output can reach 1.2 V, which is far less than the expected result. The 5-stage peak power efficiency is limited to 5.6% for the 0.35 V input as depicted in Figure 5.12. However, the peak efficiency is increased and decreased with the input voltage and load resistance, respectively.

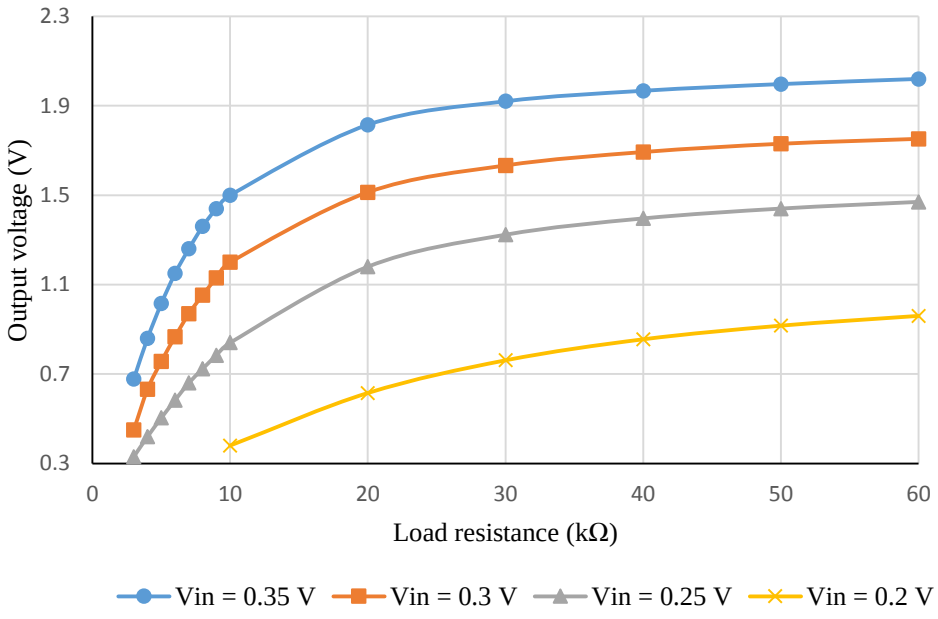

Figure 5.11. The variation of 5-stage DC-DC converter output voltage with load resistance.

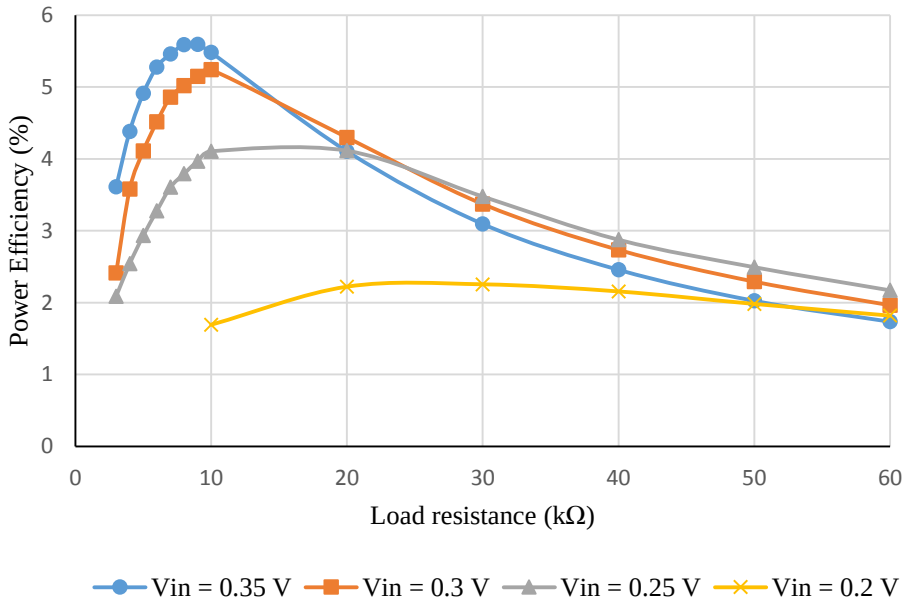

Figure 5.12. The variation of 5-stage DC-DC converter efficiency with load resistance.

The 4-stage DC-DC converter yields 1.42 V, 1.43 V, and 1.19 V output voltage at 10 kΩ, 20 kΩ, and 30 kΩ load resistance for 0.35 V, 0.30 V, and 0.25 V inputs respectively as illustrated in Figure 5.13. Similar to the 5-stage DC-DC converter, the 4-stage DC-DC converter peak efficiency is less than 6%. The efficiency decreases with lower input voltage and higher load resistance as illustrated in Figure 5.14.

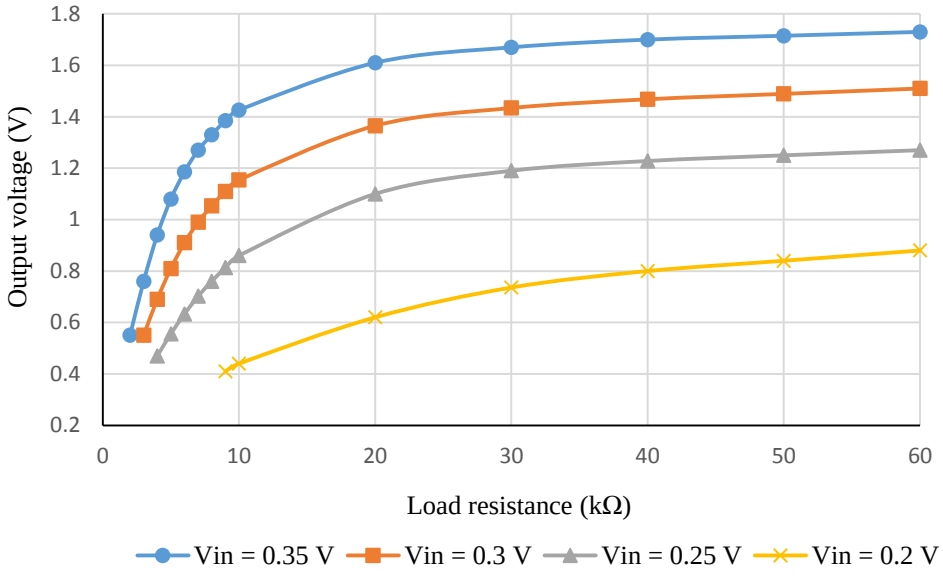

Figure 5.13. Variation of 4-stage DC-DC converter output voltage with load resistance.

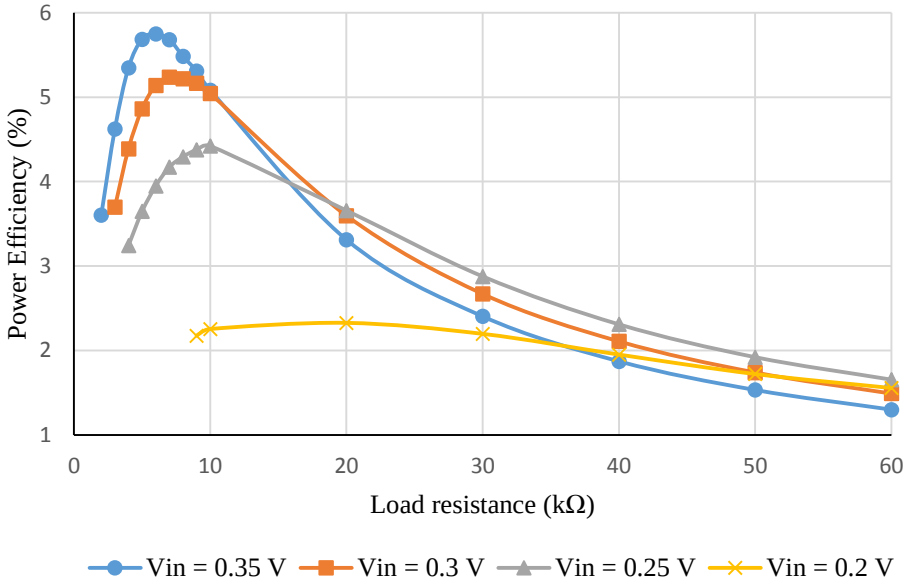

Figure 5.14. Variation of 4-stage DC-DC converter efficiency with load resistance.

Three-stage DC-DC converter output voltage variation with load resistance for different input conditions is illustrated in Figure 5.15. For low load resistance < 3 kΩ, the 0.2 V input is not sufficient for proper operation of the system due to the failure of the oscillator. 3-stage DC-DC converter efficiency decreases with load resistance as illustrated in Figure 5.16.

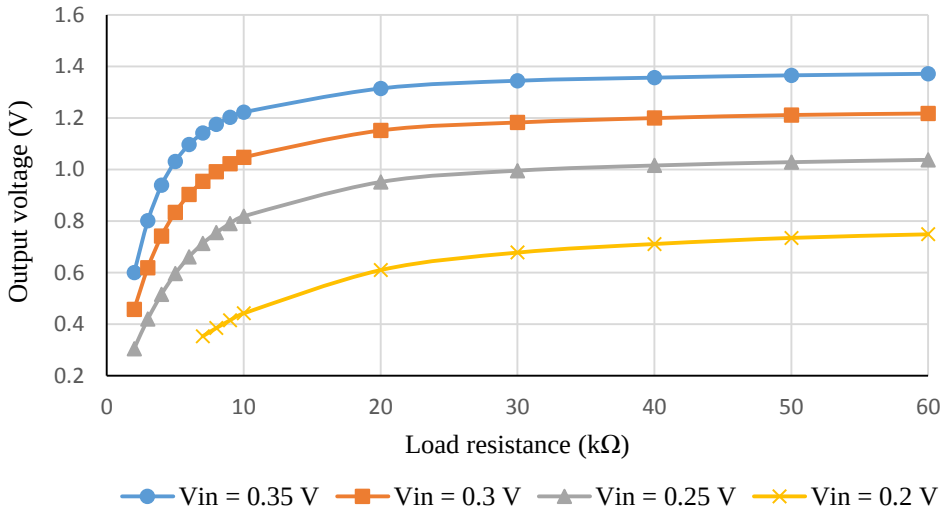

Figure 5.15. Variation of 3-stage DC-DC converter output voltage with load resistance.

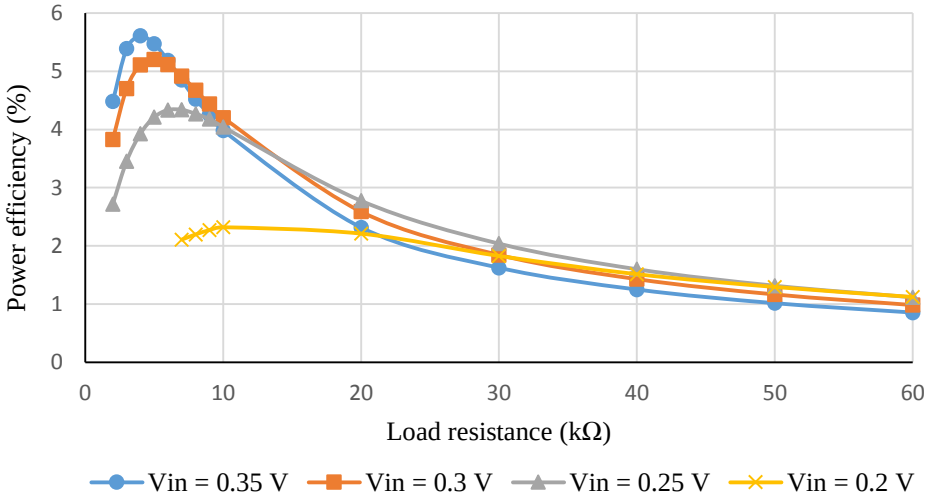

Figure 5.16. Variation of 3-stage DC-DC converter efficiency with load resistance.

Three- stage efficiency is lower than the efficiency with higher number of stages at higher load condition. However, efficiency increases with input voltage; for example, 0.35 V input achieves 5.6% peak efficiency while 0.2 V input only achieves 2.3% efficiency. According to the experimental results, the fabricated chip has lower efficiency compared to the simulation results. RC extracted and LRC extracted post-layout simulation results are identical to each other and closer to the experimental results, and follow a similar trend as illustrated in Figure 5.17 and Figure 5.18. However, the pre-layout simulation results are equal with the C-extracted post-layout simulation output voltage and efficiency. Therefore, the DC-DC converter performance is independent of the parasitic capacitor. The results indicate that parasitic resistance and actual metal resistance causes significant energy loss and

performance reduction. Therefore, a comprehensive analysis and model validation is presented for performance enhancements in the following section.

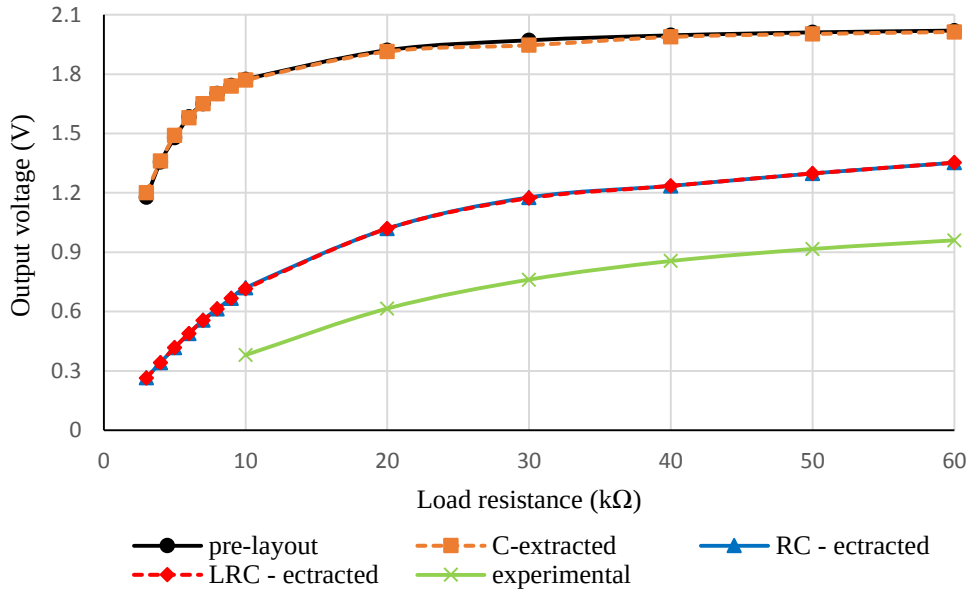

Figure 5.17. Variation of 5-stage DC-DC converter output voltage with load resistance for pre-layout simulation, post-layout simulation (C-extracted, RC-extracted, and LRC-extracted), and experimental measurement at 0.2 V input.

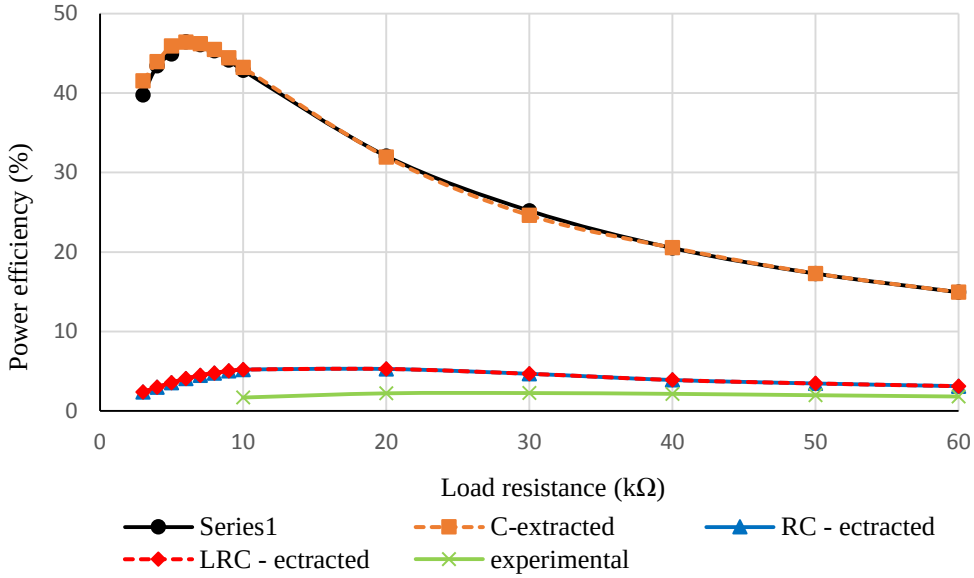

Figure 5.18. Variation of 5-stage DC-DC converter efficiency with load resistance for pre-layout simulation, post-layout simulation (C-extracted, RC-extracted, and LRC-extracted), and experimental measurement at 0.2 V input.

5.5 Correlation across the model, simulations, and experimental results

Detailed correlation analysis across model, simulation, and experimental results have been completed using test chip observations. The model based calculations are similar to the pre-layout and parasitic C-extracted post-layout simulations in Cadence environment. However, the LRC-extracted post-layout simulation output voltage and frequency are lower than the pre-layout results. The parasitic resistance of LC tank cross-coupled NMOS is the main source of this performance reduction. Since the LC tank NMOS consists of parallel MOSFETs (NMOS-multiplier) for the required transconductance, the Poly layer significantly increases the parasitic resistance. In addition, the parasitic resistance from the contact resistance between Poly layer and the metal layers is significant. Therefore, the pre-layout simulation amplitude is higher than the post-layout parasitic R-extracted oscillation amplitude. This difference is increased due to the weak contact at the MOSFET gate and small pitch of the poly layers.

The fabricated IC with switched off charge pump circuit sinks 3.70 mA for 0.2 V input which is expected to be < 1.0 mA from pre-layout simulations, and < 2 mA from post-layout simulations. Parasitic resistance of the MOSFETs and self-resistance of silicon on-die inductor cause this additional power consumption while decreasing the oscillation amplitude. According to the analysis, there should be about 14 Ω additional resistance in fabricated IC compared to the pre-layout simulations.

5.5.1 Model correction for post-layout simulations

The parasitic resistance is modeled as a resistance which is in series with the CMOS device. For example, the LC tank NMOS gate parasitic resistance is modeled as a series resistance with NMOS gate terminal. This additional resistance generates a voltage divider at the gate, and leads to decreased oscillation amplitude. As a result, the charge-pump clock amplitude drastically decreases with the increase of parasitic resistance. Different sizes of Poly layers are used to validate the amplitude reduction regarding the parasitic resistance. The variation of the DC-DC converter oscillation amplitude with the inductor series resistance (resistance between NMOS drain and inductor) can be observed by incorporating an external resistor into the design. The amplitude of the fabricated DC-DC converter has a linear response with inductor series resistance at 0.2 V input as illustrated in Figure 5.19. Despite the small variation of the oscillation frequency, the current consumption of the LC tank has a significant increase in post-layout simulations due to the presence of parasitic resistance. This increasing current can be explained through the LC tank parallel resistance model. Parallel resistance is inversely proportional to the series resistance. Since oscillation frequency and resonator inductance

variation are insignificant with parasitic resistance, the resonator parallel resistance decreases significantly with the increase of series resistance. Therefore, the LC tank power consumption can be written as,

$$P_T = \left(V_{PP}/2\sqrt{2}\right)^2 \left[\frac{2}{R_{PL}} + \frac{C\omega}{2\pi}\right], \tag{67}$$

where R_{PL} is the total parallel resistance of the resonator. Increasing fingering of parallel NMOS decreases R_{PL}, and increases the power consumption of the LC tank, but the decreasing oscillation amplitude decreases the power consumption. The parasitic resistance effect on charge pump MOSFETs is not significant because of the low channel width compared to the LC tank NMOS. However, the amplitude downscaling decreases the charge pump power consumption. The decrease of the capacitive losses is smaller compared to the LC tank resistive losses. Therefore, power consumption of the DC-DC converter is significantly increased due to the additional power loss to the oscillator parallel resistance.

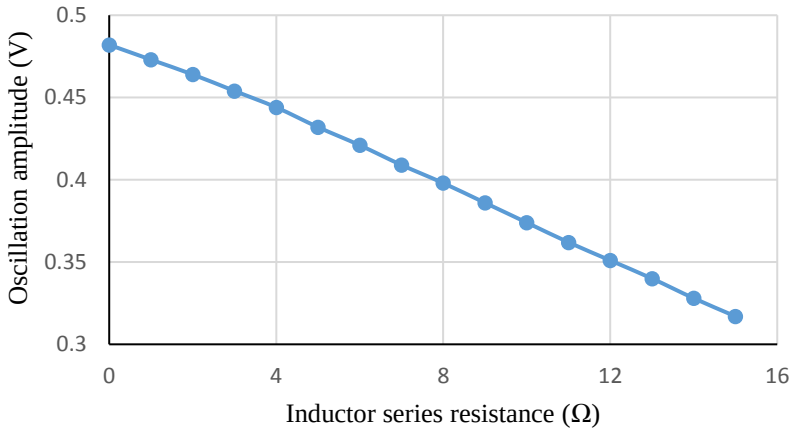

Figure 5.19. The variation of DC-DC converter oscillation amplitude with inductor series resistance.

According to model based analysis, the total parasitic resistance between inductor and NMOS drain (model as R) except the self-resistance of the inductor in the post-layout circuit is approximately 9 Ω. However, there is a 5 Ω additional resistance available in fabricated silicon design. This additional resistance is mainly from the silicon resistance of on-chip inductor, which is known as the true self-resistance of the inductor (including contact resistances inside the inductor design). The model analysis can be used to minimize the parasitic resistance in layout design and enhance the performance using optimization. The optimization process is similar to section 4.3.3, including additional power consumption of parallel resistance. The post-layout simulation results are presented for the new model validation below.

5.5.2 Verification by Simulation

The post-layout simulation, experimental, and model based analyzed output voltage response of the fabricated 3-stage DC-DC converter at 0.2 V input is shown in Figure 5.20. The corresponding efficiency variation is depicted in Figure 5.21. R is the total parasitic resistance between NMOS drain and LC tank inductor. According to the analysis, the fabricated IC contains 5 Ω additional inductor-series resistance compared to the parasitic extracted layout design. The on-chip metal inductor and metal connections of the MOSFET and inductor contribute for this additional resistance, which depends on the CMOS fabrication process.

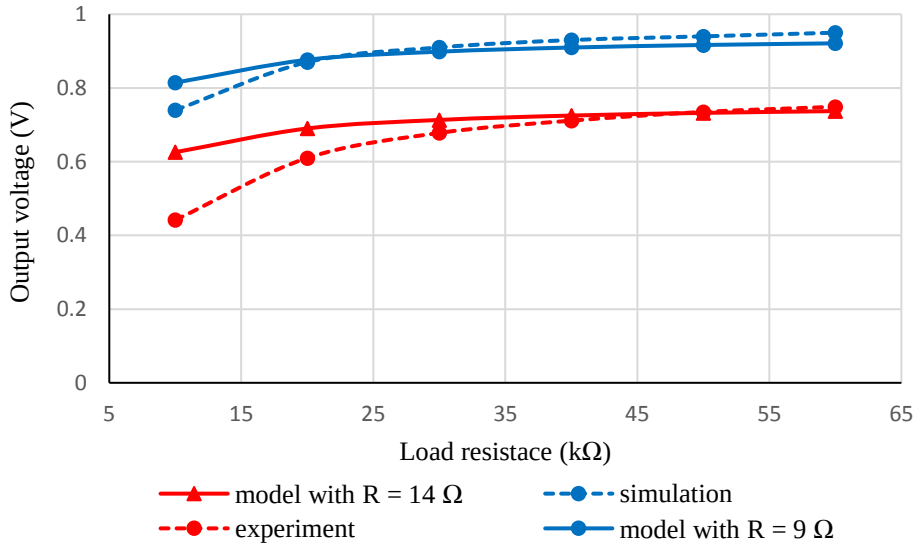

Figure 5.20. The variation of 3-stage DC-DC converter output voltage with load resistance (simulation, experiment, and model results).

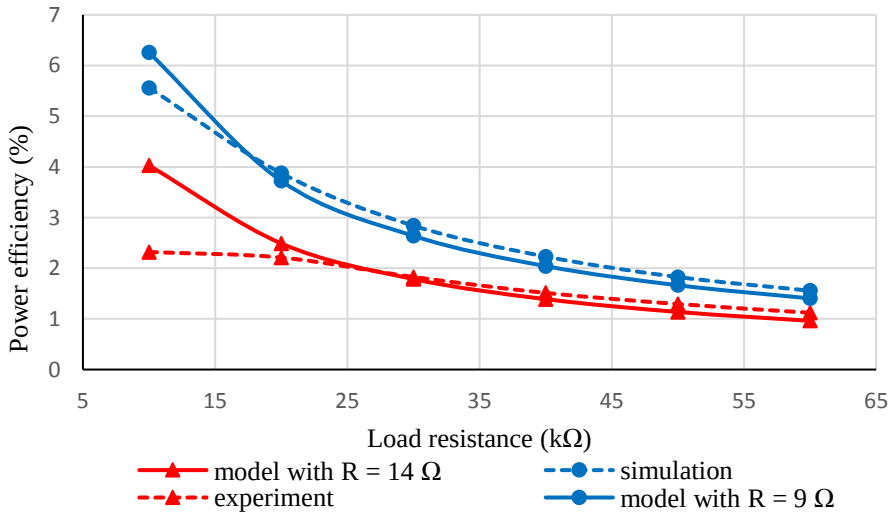

Figure 5.21. Variation of 3-stage DC-DC converter efficiency with load resistance (simulation, experiment, and model results)

The measured power efficiency and output voltage response of the fabricated 3-stage DC-DC converter along with the model results at 0.25 V input is depicted in Figure 5.22 and Figure 5.23 respectively. The variation of MOSFET resistance with load current and small parasitic components are the reason for the small discrepancy between model results and experimental results.

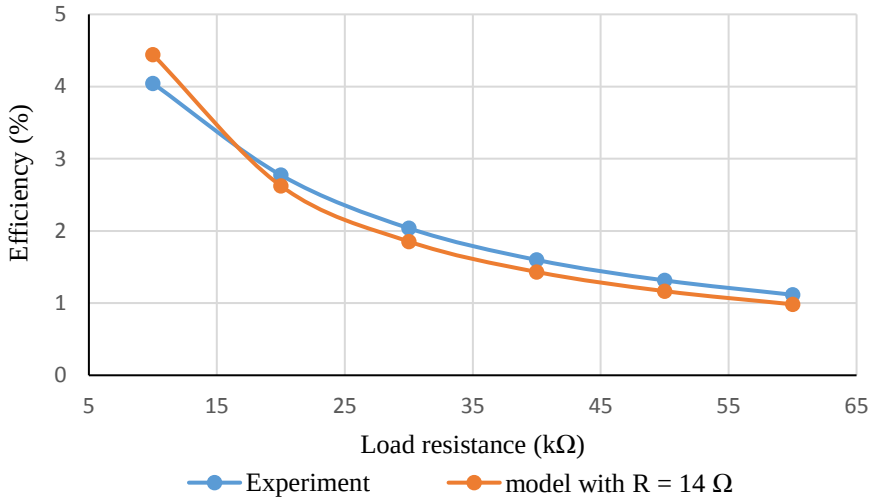

Figure 5.22. The variation of 3-stage DC-DC converter output voltage with load resistance at 0.25 V input (post-layout simulation and model results).

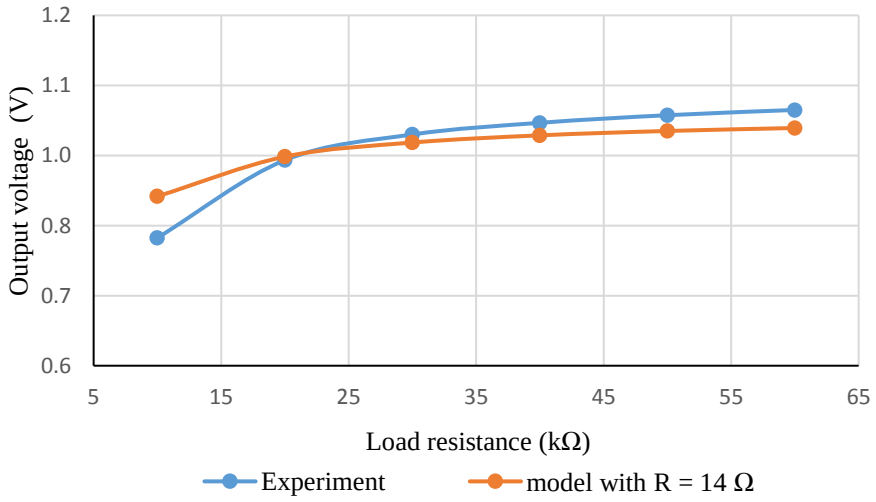

Figure 5.23. The variation of 3-stage DC-DC converter efficiency with load resistance at 0.25 V input (post-layout simulation and model results).

The optimized LC tank consists of four parallel N-channel MOSFETs with 400 µm channel-width and 240 nm channel-length in UMC 180nm CMOS Low_Vt process. When a small Poly layer in layout design is introduced to increase the parasitic resistance in the model, the output voltage variation of the RLC-extracted post-layout simulations is similar to the model results

as illustrated in Figure 5.24. 3-stage DC-DC converter achieves 1.15 V for 15 kΩ load resistance at 0.2 V input. The simulated efficiency response of the DC-DC converter with load resistance is similar to model calculations as depicted in Figure 5.25. According to the post-layout simulation results, 3-stage DC-DC converter maximum efficiency is 31.3 % and the converter delivered 190 µW output power for 4 kΩ load resistance at 0.2 V input (is not shown in the graph). The simulation results are parallel with the model calculations of a DC-DC converter for the proper working range of load resistance.

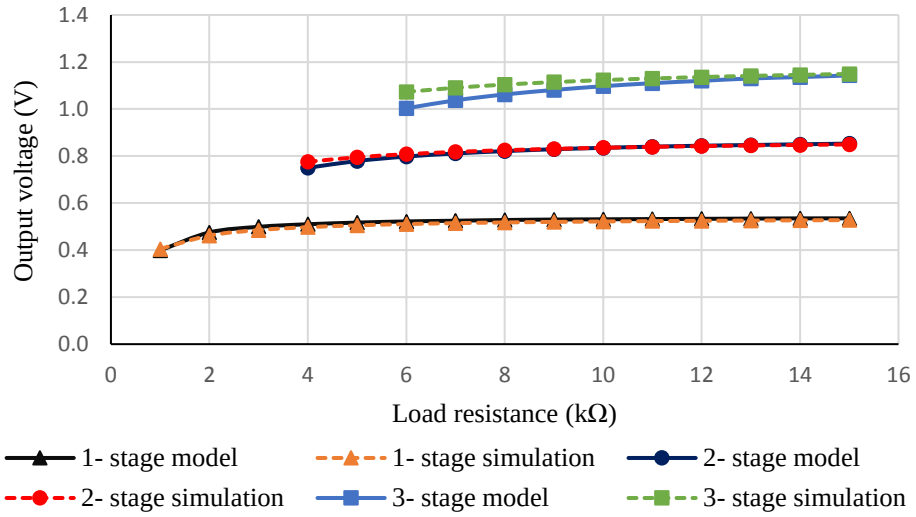

Figure 5.24. The variation of DC-DC converter output voltage with load resistance at 0.2 V input (small Poly layout).

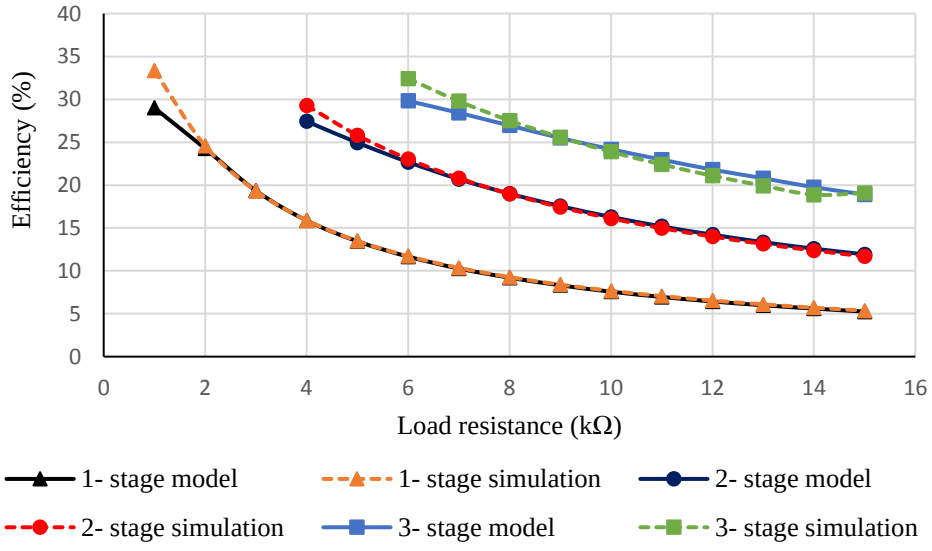

Figure 5.25. The variation of DC-DC converter power efficiency with load resistance at 0.2 V input (small Poly layout).

Similar circuit parameters are implemented into layout design with larger Poly layer connection to observe the trend of characteristic curves and validate the model calculations. The NMOS gate with large poly connection recovered an oscillation amplitude that matched the original pre-layout simulation amplitude. However, the current consumption is greater than the pre-layout simulation due to the none-zero parasitic resistance that is not included in the pre-layout model. Figure 5.26 illustrates the output voltage variation of 1-3 stage DC-DC converter with load resistance for 0.2 V input. 1-3 stage DC-DC converter steps 0.2 V up to 0.55 V, 0.88 V, and 1.19 V respectively. The reduction of parasitic resistance increases the power efficiency and achieves around 40% peak efficiency as depicted in Figure 5.27.

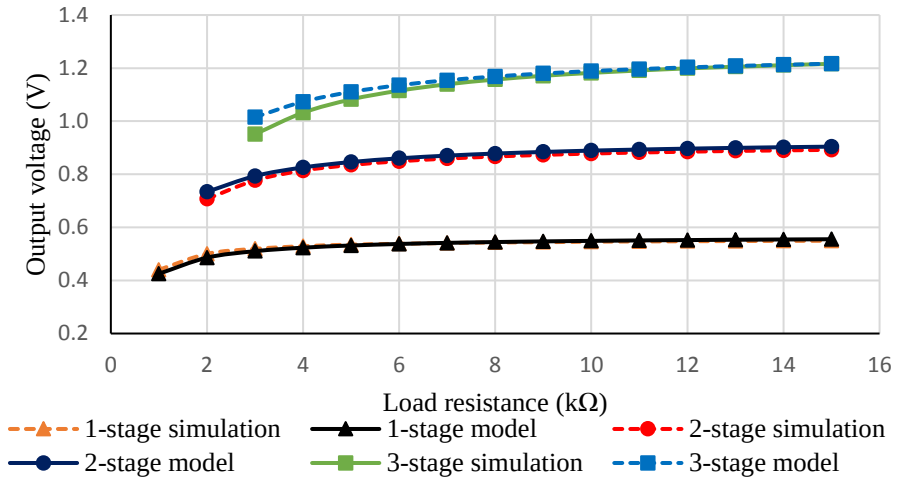

Figure 5.26. The variation of DC-DC converter output voltage with load resistance for 0.2 V input (large Poly layout).

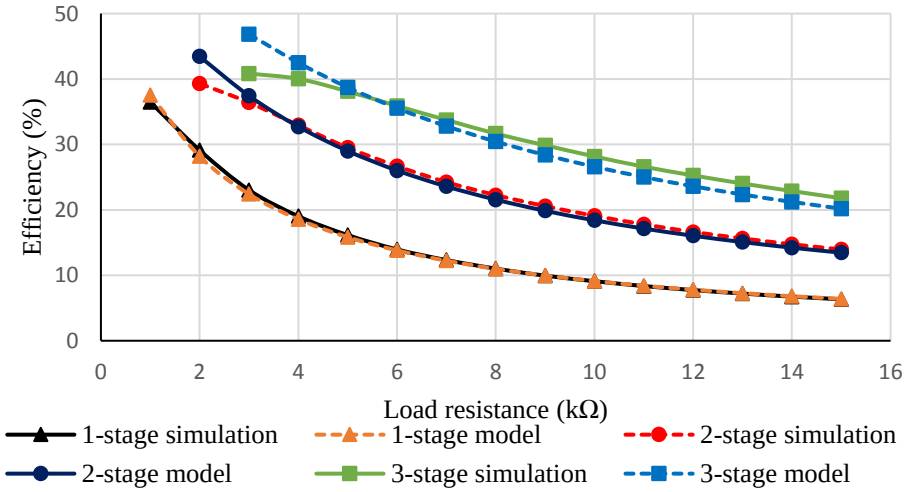

Figure 5.27. The variation of DC-DC converter power efficiency with load resistance for 0.2 V input (large Polly layout).

5.6 Enhanced multi-stage DC-DC converter

To achieve higher performance, LC tank oscillator MOSFET parasitic effect should be decreased and the number of switching MOSFETs should be minimized. The LC tank parallel resistance is inversely proportional to the inductor series resistance, but the parasitic resistance increases the inductor series resistance. As a result, the LC tank parallel resistance decreases with increasing the parasitic resistance. Therefore, the required transconductance (g_m) of the LC tank oscillator NMOS is less than the pre-simulation calculations. To achieve this, optimized circuit components are used for the DC-DC converter design, and a single NMOS is used as a stage selection switch for the multi stage DC-DC converter. The full system consists of an LC tank oscillator, four-stage charge pump with an optional additional stage that is selected through an NMOS switch, as shown in Figure 5.28.

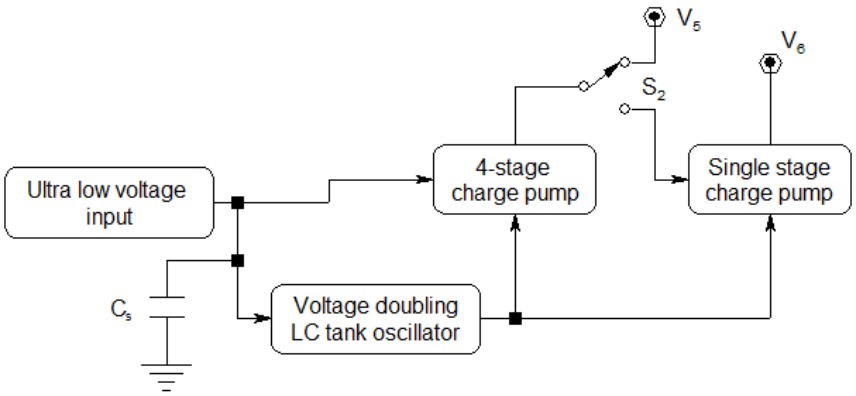

Figure 5.28. Block diagram of multi stage DC-DC converter.

Figure 5.29 and Figure 5.30 illustrate the LRC extracted output voltage and efficiency variation of 4-5 stage DC-DC converter with load resistance for 0.2 V input. The 4-5 stage DC-DC converter steps 0.2 V into 1.27 V, 1.47 V and yields 41%, 41.5% peak efficiency with 320 µW, 358 µW output power, respectively. The time taken for the steady state output voltage is < 200 ns. However, the load resistance of the peak efficiency increases with the DC-DC converter stages. Similarly, although the output voltage increases with load resistance, the efficiency decreases as charge pump impedance increases compared to the LC tank impedance.

Figure 5.31 and Figure 5.32 illustrate the output voltage and power efficiency of 5-stage DC-DC converter LRC-extracted simulation results and model verification. According to the model analysis, the model with 2 Ω resistance is matched with the post-layout simulation

output voltage and efficiency. The pre-layout simulation is matched with model results without this additional 2 Ω resistance.

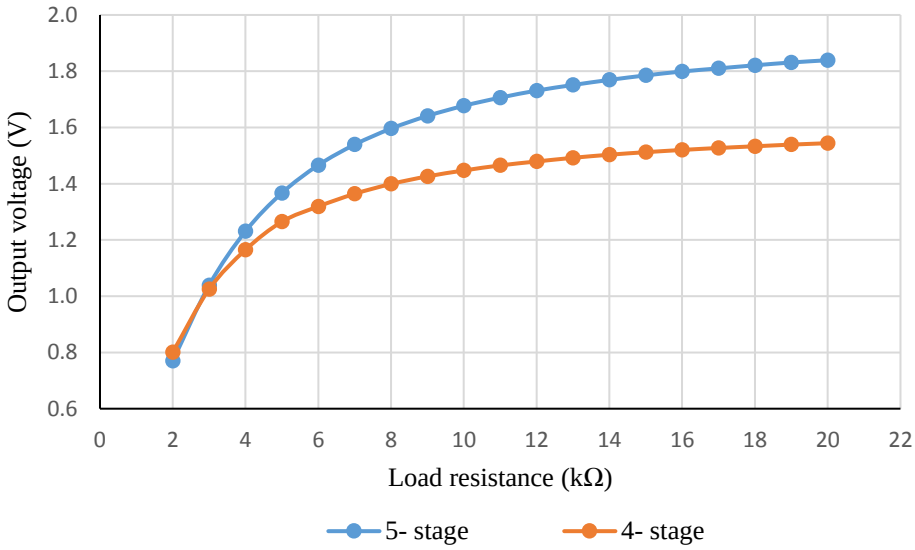

Figure 5.29. The variation of output voltage with load resistance of enhanced design.

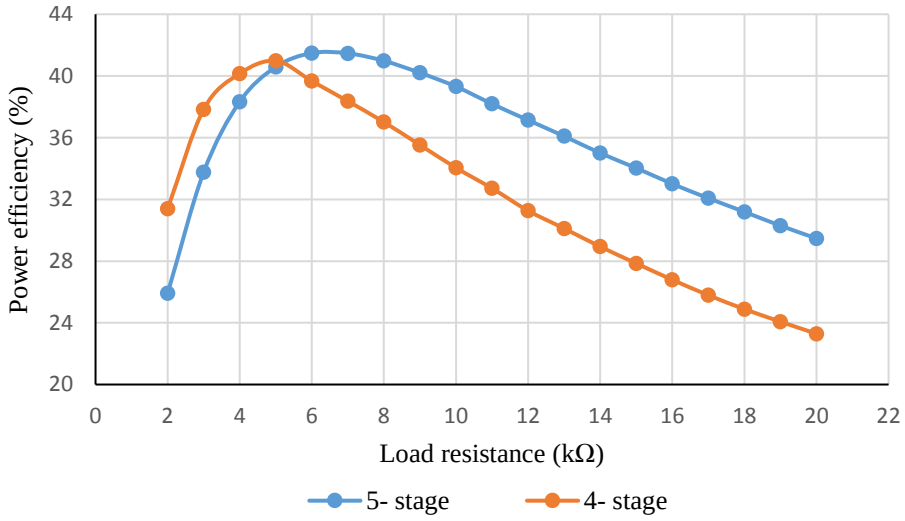

Figure 5.30. The variation of power efficiency with load resistance for enhanced design.

In the model, this resistance represents the parasitic resistance of the NMOS which is series with the inductor. There is a small discrepancy between post-layout simulation and model results. This is because the frequency and active resistance of the MOSFET are varying with the load resistance, and are ignored in model calculations. The expected peak efficiency of the 5-stage DC-DC converter is 40% at similar silicon fabrication environment compare to the fabricated design. Because, according to the model analysis, the fabricated on-chip inductor

consists of 5 Ω additional resistance compare to the RLC-extracted post-layout design and is a constant for similar parameters. But, this silicon resistance can be decreased according to the fabrication process and environment. Therefore, the 5-stage DC-DC converter peak efficiency is expected to be 40.0 ± 1.5 % for 1.53 ±0.01 V output at 7 kΩ load and 0.2 V input.

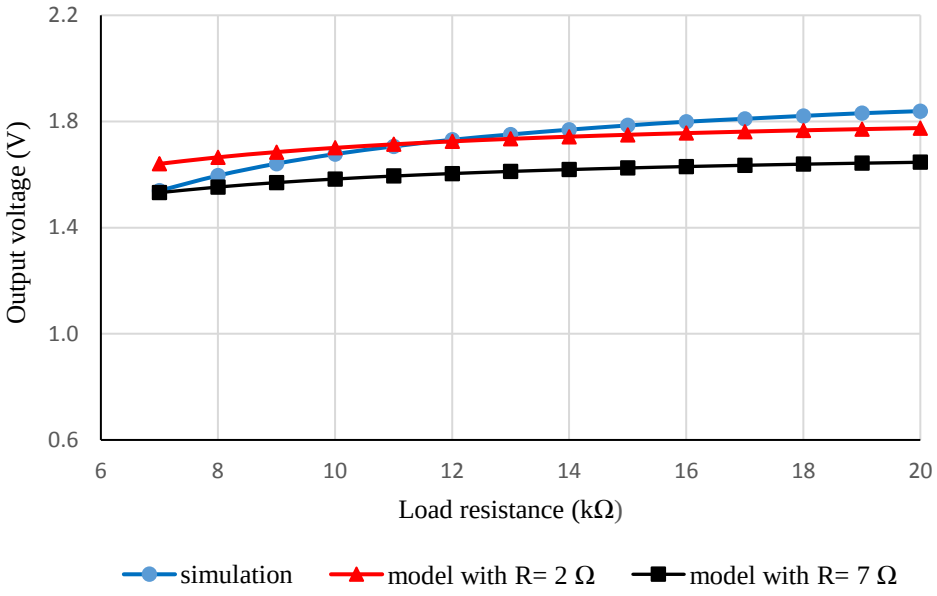

Figure 5.31. The 5-stage DC-DC converter output voltage variation with load resistance at 0.2 V input (simulation and model results).

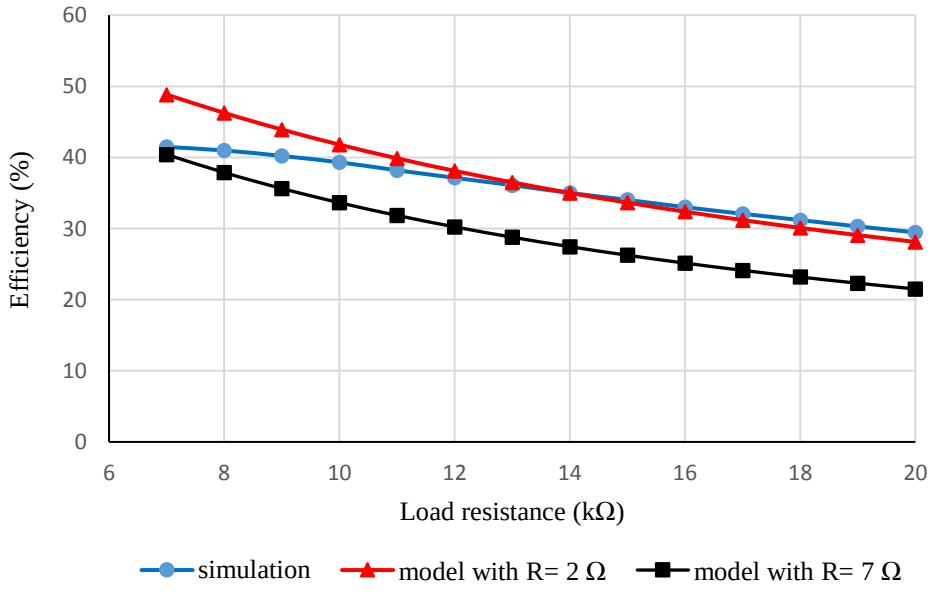

Figure 5.32. The 5-stage DC-DC converter efficiency variation with load resistance at 0.2 V input (simulation and model results).

The 4-stage DC-DC converter peak efficiency can be presented as 39 ± 2 % for 1.2 ±0.1 V output at 5 kΩ load and 0.2 V input as illustrated in Figure 5.33 and Figure 5.34. The 4-stage DC-DC converter is expected to achieve > 200 ± 10 µW load power for > 27± 1% at <10 kΩ load and 0.2 V input. The full-chip layout of the second design is shown in Figure 5.35.

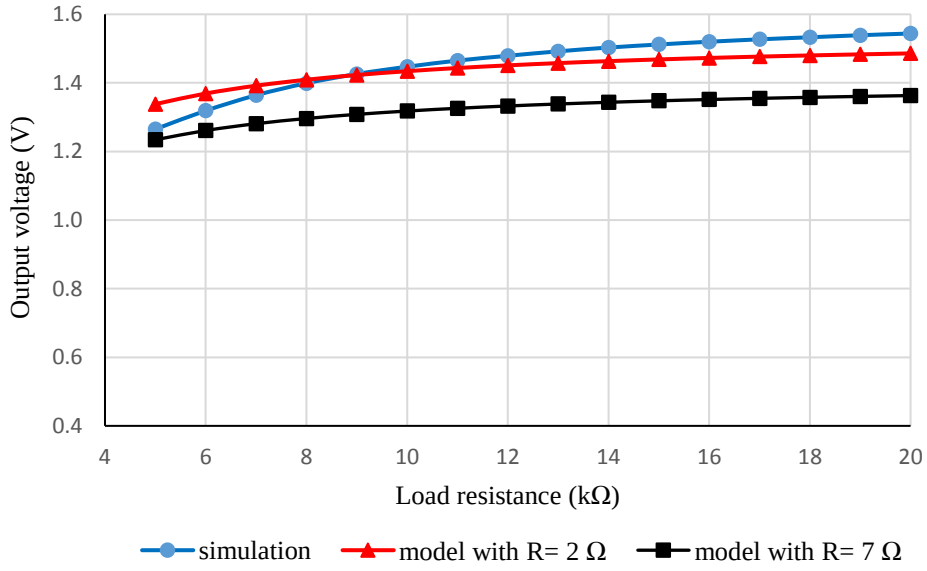

Figure 5.33. The 4-stage DC-DC converter output voltage variation with load resistance at 0.2 V input (simulation and model results).

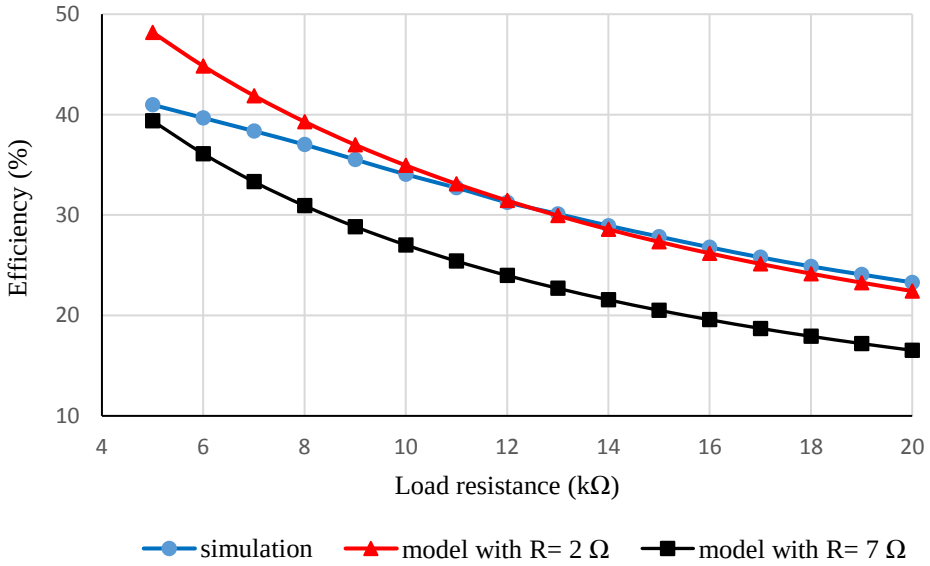

Figure 5.34. The 4-stage DC-DC converter efficiency variation with load resistance at 0.2 V input (simulation and model results).

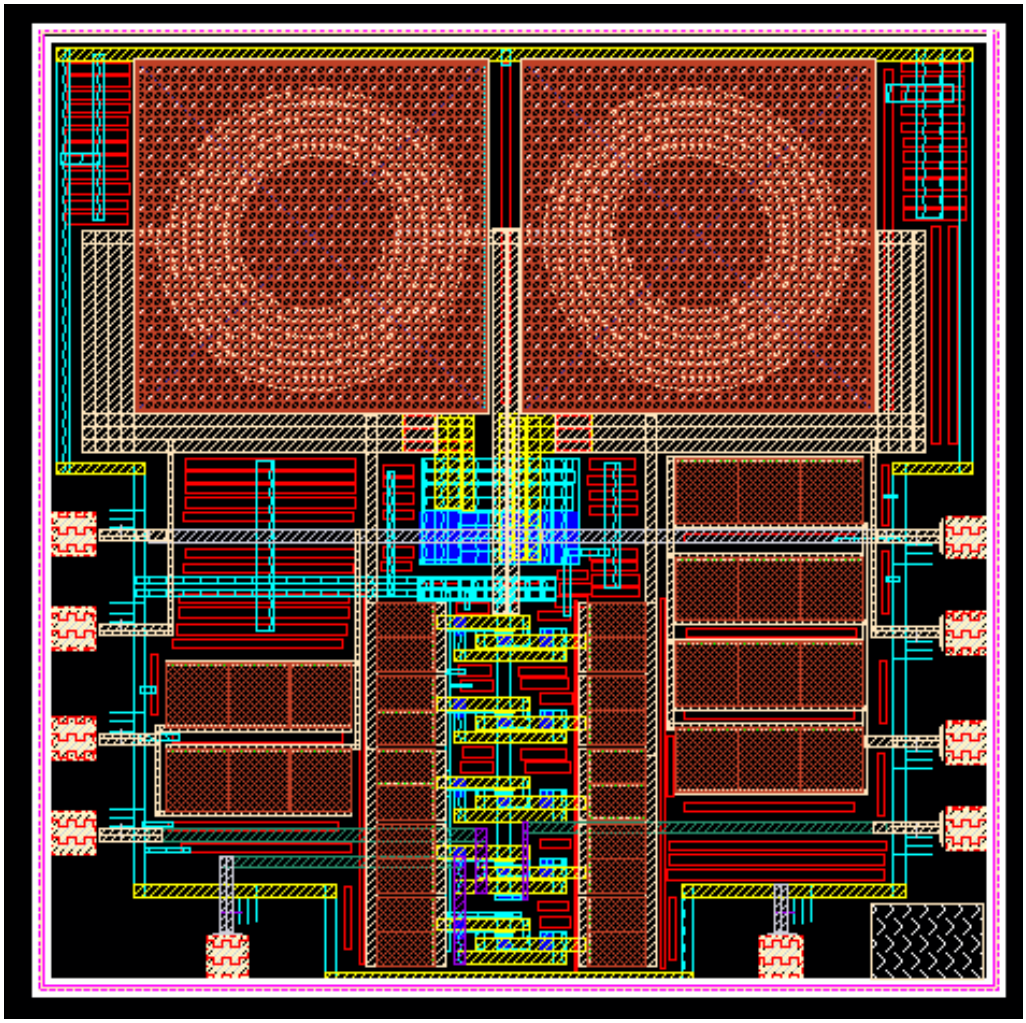

Figure 5.35. Die layout photo of enhanced circuit with PAD connections.

Metal-6 layer is used to design the inductor in UMC 180nm CMOS process and the minimum sheet resistance of the Metal-6 sheet is 25 mΩ/sq. The used inductor consists of 20 µm width and 5152 µm total average length. Therefore, the total metal resistance is 6.4Ω, ignoring the contact resistance. However, the model predicts that 7 Ω total resistance is available in the inductor. Therefore, this calculation validates the accuracy of the model results.

5.7 Performance comparison with literature

Table 5.3 summarizes the performance comparison of the ultra-low voltage DC-DC converters available in the literature. The proposed DC-DC converter (enhanced multistage DC-DC converter) performance is better than most of the alternative ultra-low input DC-DC converters available in the literature. Extremely high output power and high efficiency at low load

condition are the main advantages of this design. However, the proposed design occupies a larger on-die are because of two bulky inductors.

Table 5.3. Comparison with ultra-low voltage DC-DC converters in literature.

Ref.	Proc. (nm)	Min. input (v)	Output (v)	Power output (μW)	Maximum efficiency (%)	Area (mm^2)	Off chip component
[78]	65	0.10	1.2 @ 0.14 V input & 1 MΩ load	10@ 0.12 V input	33@ 0.10 V input & 1 MΩ load	2.13	None
[91]	180	0.20	1.2 @ 0.20 V input & 10 kΩ load	146 @ 0.20 V input	36 @ 0.20 V input & 10 kΩ load	-	2-inductors
[92]	130	0.15	0.619 @ 0.18 V input & 10 kΩ load	11 @ 0. 18 V input	34 @ 0.18 V input & 10 kΩ load	0.066 for only charge pump	6-caps
[76]*	180	0.15	1.6 @ 0.20 V input & 40 kΩ load	63 @ 0.20 V input	35 @ 0.2 V input & 40 kΩ load	1.15 for 5-stage	None
[93]	180	0.15	1.7 @ 0.25 V input & 60 kΩ load	55 @ 0.25 V input	15.5 @ 0.25 V input & 60 kΩ load	0.88 for 5-stage	None
[94]	180	0.15	2.0@ 0.14 V input & 100 kΩ load	40@ 0.20 V input	20 @ 0.20 V input & 10 kΩ load	-	None
This* work	180	0.15	1.8 @ 0.2 V input & 16 kΩ load	358 @0.2 V input	41.5 @ 0.2 V input & 6 kΩ load	1.24 for 5- stage	None

(*-simulation results)

CHAPTER 6

6 THESIS CONCLUSION

In this thesis, two non-identical DC-DC converter topologies have been designed for ultra-low voltage applications with high power capacity such as ambient thermal energy harvesting with low temperature gradient across many thermoelectric transducers. Both DC-DC converters are capable of self-starting at as low input voltage as 0.2 V, and boost up to a higher DC voltage level according to the number of stages. To achieve high performance using minimum integrated chip area, new optimization methods have been utilized and validated using Cadence environment. The proposed circuit characteristics are summarized in Table 6.1, for 4- stage DC-DC converter design.

Table 6.1. Summary of the implemented circuits.

DC-DC converter with	Type	V_{in} min. (V)	V_{out} @ Vin = 0.2 V	Pout (μW) @ Vin = 0.2 V	Max. effi. (%)
voltage doubling LC tank (design 1)	Pre- layout	0.11	1.5 @ 9 kΩ load	425	46
	Post-layout	0.17	0.9 @ 20 kΩ load	52	8
	experimental	0.18	0.8 @ 40 kΩ load	19	2.33
voltage doubling LC tank (design 2)	Pre- layout	0.11	1.45 @ 10 kΩ load	455	48
	Post-layout	0.15	1.447 @ 10 kΩ load	350	41
	Expected experimental	0.15	1.32 ± 0.13 @ 10 kΩ load	310 ± 20	39 ± 2
voltage quadrupling LC tank	Pre- layout	0.20	2.47@ 10 kΩ load	1193	33.6

According to the pre-layout simulation results, the DC-DC converter with voltage doubling LC tank can yield 50% peak efficiency for load resistance < 10 kΩ, which is verified through model calculations. Post-layout simulation results prove worse, as a result of the presence of parasitic resistance, which significantly contributes to power consumption of the LC tank, and drastically reduces the oscillation amplitude. Experimental efficiency is lower than the simulation results due to the silicon on-die self-resistance of the inductor. The discrepancy

between the pre-layout, post-layout and experimental observations are analytically explained and then model to enhance the performance of the DC-DC converter. In addition, the design layout effect on the DC-DC converter is analyzed based on model calculations.

The pre-layout simulation efficiency of the first design is lower than the optimized 4-stage DC-DC converter as explained in chapter 4 due to the stage control MOSFET switches. However, the post-layout results are drastically reduced compared to the pre-layout results because of the parasitic resistance. The first design is used as a test bench for the model validation and is rebuilt to enhance the accuracy. The silicon on-die inductor self-resistance and the MOSFET gate parasitic resistance are estimated using model analysis. Different layout design for the unique circuit parameters is used to observe characteristics of DC-DC converter variation with layout parasitic. These observations are used as a test bench to validate the model analysis. According to the model, the total resistance of 9Ω is available in series with an inductor in post-layout apart of the self-resistance, and additional 5Ω is available in silicon on-die design. The second design is an enhanced version of the first to maximize the efficiency and output power capacity of the system. According to the LRC-extracted post-simulation results, the 4-stage DC-DC converter can yield 41% peak efficiency and 340 μW load power at 0.2 V input. The 5-stage DC-DC converter embedded in second design can step 0.2 V up to 1.47 with 41.5% peak efficiency for 15 kΩ load resistance. According to model analysis, the silicon on-chip 5 stage DC-DC converter peak efficiency can be expected to be in the range of 40.0 ± 1.5 % for 1.54 ± 0.01 V output at 7 kΩ load and 0.2 V input. Similarly, 4-stage DC-DC converter is expected to yield a peak efficiency of 39 ± 2 % for 1.2 ± 0.1 V output at 5 kΩ load and 0.2 V input.

The DC-DC converter with voltage quadrupling LC tank has lower efficiency than the system with voltage doubling oscillator due to the high power consumption of the voltage quadrupling oscillator. However, voltage gain and output power of the DC-DC converter with voltage quadrupling LC tank are significantly higher than the previous one. The four stage of the DC-DC converter can boost 0.2 V into 2.5 V with 525 μW load power for 12 kΩ load resistance. At 0.2 V input, peak efficiency of 33.6% is observed, with capacity of delivering 1194 μW output power to 4 kΩ load resistance. This comes at an area increase of 80% compared to the design with voltage doubling LC tank.

6.1 Future work

According to the analysis, the DC-DC converter characteristics drastically change with the parasitic resistance of the CMOS components. Post-layout simulations prove the feasibility of higher efficiency DC boost converter in UMC 180nm CMOS technology. Hence, the priority is to minimize the differences between pre-layout and post-layout simulation results through the enhancement of the design along with the theoretical model based analysis. The other comprehensive list of future studies is listed below:

1. Voltage quadrupling LC tank based oscillator coupled DC-DC converter layout can be designed and fabricated to observe the output power and efficiency.
2. Fully integrated inductor can be re-designed to improve the efficiency and output voltage of the DC-DC converter. The internal resistance should be smaller than the UMC inductor available in Cadence.
3. Integrated regulator and maximum power point tracking system can be implemented with stage switching mechanism to yield steady output voltage and best efficiency at varying input and output conditions.

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