LOW VOLTAGE INTEGRATED CHARGE PUMP CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

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Approval of the Board of Graduate Programs

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This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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ABSTRACT

LOW VOLTAGE INTEGRATED CHARGE PUMP CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

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Two different low voltage integrated charge pump circuit topologies are studied in this thesis for energy harvesting applications. The circuits are implemented in 0.18 μm standard CMOS technology without the use of off-chip magnetic components and non-standard processes, and are thus suitable for low profile (small and low cost) system-on-chip applications. In the first proposed design, operation at low input voltage (~240 mV) is achieved with a 5-stage subthreshold first stage oscillator, which improves the first stage efficiency by 28%. The 50 mV hysteretic on-off decision by a comparator at the second stage enables bursts of charge-pumping to a standard DC voltage, and thus improves full system efficiency by 2%. The system has been validated in application to generate 1.5 V output with 4% peak efficiency and 0.24 V input voltage. The simulation-validation correlation has been presented in detail. The second proposed system has been developed with fully integrated inductors at the first stage in order to improve the efficiency obtained in the previous design. The system can successfully convert 0.2 V up to 1.5 V with 22% efficiency based on simulations. The generated output power is 31 μW which is 94% higher than that of the previous design. The inductors are modeled using 3D Planar Electromagnetic Field Solver Software incorporating the losses associated with the silicon based spiral inductors. At the ultra-low voltage range of interest, the regulators are estimated to have lower cost and improved efficiency compared to the alternatives reported in literature including the 90 nm two-stage charge pump design previously reported by our team.

Keywords: Charge pump, thermoelectric energy harvesting, integrated inductors, SOC

ÖZ

ENERJİ HASADI UYGULAMALARI İÇİN DÜŞÜK VOLTAJLI ENTEGRE ŞARJ POMPASI DEVRELERİ

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Bu tezde, enerji hasadı uygulamaları için iki farklı düşük voltajlı entegre şarj pompası devre topolojisi çalışılmıştır. Devreler, çip dışı manyetik bileşenler olmaksızın 0.18 um standart CMOS teknolojisi ile yapılmıştır; bu şekilde düşük profilli (küçük ve düşük maliyetli) çip üzeri sistemler için uygundur. Sunulan ilk tasarımda düşük giriş voltajlı (~240 mV) işlem, 5 safhalı eşik altı ilk kademe osilatörü ile gerçekleştirilmiştir. Bu yaklaşım ilk kademenin verimliliğini %28 artırmıştır. 50 mV değerindeki kompratör histeresis aralığı ikinci safhadaki açma-kapama kayıplarını azaltır ve böylece tüm sistem genelinde %2 verimlilik artışı sağlar. Sistemde 0.24 V giriş voltajıyla 1.5 V çıkışın %4 verimlilikle sağlandığı uygulamalar ile doğrulanmıştır. Simülasyon-doğrulama ilişkisi detaylı olarak sunulmuştur. İkinci ileri sürülen tasarım, ilk kademede tamamen entegre bazlı indüktörler ile, ilk tasarımdaki enerji verimliliğini artırmak amaçlı tasarlanmıştır. Sistem 0.2 V girişi 1.5 V'a kadar %22 verimlilikle başarılı bir şekilde çevirmiştir. Üretilen çıkış gücü 31 uW olup bir önceki tasarıma göre %94 daha fazladır. İndüktörler 3B Düzlemsel Elektromanyetik Alan Çözücü yazılımı ile modellenmiş ve silikon bazlı spiral indüktörlerden kaynaklanan kayıplar dikkate alınmıştır. Tamamlanan tasarımlar, ultra düşük voltaj çerçevesinde, alternatiflerine göre daha düşük maliyet ve daha yüksek verimliliğe sahiptir.

Anahtar Kelimeler: Şarj pompası, termoelektrik enerji hasadı, entegre indüktör, SOC

DEDICATION

To my Wife, Parents and Brother

For their unconditional support, trust and encouragement.

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NOMENCLATURE

A	Gain of the amplifier
A_m	Metal area (m^2)
C	Capacitance (pF)
I_{in}	Input current (µA)
I_{out}	Output current (µA)
L	Inductance (nH)
Low-Vt	Low threshold voltage
MOSFET	metal–oxide–semiconductor field-effect transistor
n	Subthreshold slope factor
NMOS	N-type metal-oxide-semiconductor
Nom-Vt	Nominal threshold voltage
P_{in}	Input power (µW)
PMOS	P-type metal-oxide-semiconductor
P_{out}	Output power (µW)
Q	Quality factor of the inductor
R_L	Load Resistance (kΩ)
R_p	Parallel resistance (Ω)
R_s	Series resistance (Ω)
T	Temperature (^{0}C)
TE	Thermoelectric
U_T	Thermodynamics voltage
V_{GS}	Gate to Source voltage of MOSFET
V_{SD}	Source to drain voltage of MOSFET
V_t	Threshold voltage of the MOSFET
Zero-Vt	Zero threshold voltage
η_{eff}	Efficiency (%)

CHAPTER 1
INTRODUCTION

As worldwide energy demand increases, conventional energy resources will be replaced by new technologies to make the energy future sustainable [1].On the other hand, the penetration of small electronic equipment to daily life increases at a fast pace, while new applications require more advanced functions, higher performance and lower power operation, along with reduced size. Small portable devices become ubiquitous with applications like distributed wireless sensor nodes for structural health monitoring, embedded sensors in automotive industry such as tire pressure monitoring systems, MP3 players, and other military systems. Improvements in microelectronics and MEMS technology lead to reduces size in portable devices, opening up room for new applications in wearable devices such as watches, glasses, and clothes. Batteries have traditionally been used as the main power source for these systems. The usage of batteries adds undesirable weight and volume, as well as requiring regular replacement [2].

For applications which require thousands of sensor nodes distributed in a large area, it is impossible to replace the batteries as soon as the source is depleted. Even if it is possible, their replacement cost poses major obstacle for such applications. Furthermore, in some applications such as implanted medical devices, replacements of batteries are impossible. Therefore, using batteries as the power source of these systems is impractical with their large dimensions and short lifespan [3]-[4].

The size of the electronic circuits and their energy requirements has been drastically reduced in recent decades, which opens up the possibility to harvest energy from the environment to power electronic circuits. However, the voltage generated from low power energy harvesters, such as small thermoelectric generators, individual solar cells, micro-bio fuel cells is in the order of few tens of millivolts to a couple of hundreds of millivolts at most, and is less than the voltage required for most state-of-the-art integrated circuit loads [5].In addition, the voltage generated from energy harvesters varies with time. Therefore, voltage step-up (boost) circuit technologies, which can regulate a widely varying and low voltage sources, are critical in order to make low voltage energy scavenging feasible. However, low-voltage operation of a circuit is challenging because of the following three reasons [6]:

1. The standard low-power CMOS technologies have a minimum MOSFET threshold voltage around 250 mV, which is typically higher than the voltage generated from the micro-power energy harvesters.
2. The noise on the power supply, ground lines and from the substrate often causes errors in the circuits.
3. The leakage current and the power dissipation of the interface circuit need to be minimized in order to generate positive power.

Due to these challenges, most of the DC-DC converters present in the literature contain discrete magnetic components such as large inductors, and transformers [7]. These circuits cannot easily be integrated for system-on-chip applications, and thus require larger space and investment. There are very limited numbers of papers published in terms of fully integrated DC-DC converters which can start up with ultra-low voltages in 100 – 250 mV range, without using any discrete components. Most of these papers provide simulation data and do not provide insight into validation and testing, which is inhibitive in enabling the industry to integrate low-voltage thermoelectric energy harvesting ubiquitously.

This thesis aims to design and validate ultra-low voltage charge pump based DC-DC converters for the voltage generated from energy harvesters with DC output, and mainly focuses on micro-thermoelectric harvesting problem. In this chapter, a brief introduction to energy harvesting systems and interface electronics for thermoelectric micro-power generators is provided. Section 1.1 introduces the types of general harvesting techniques, and their applications. Section 1.2 and 1.3 explain the operation principle of thermoelectric energy harvesters, and their applications. Section 1.4 describes general interface electronics used for thermal energy based harvesters. Finally, Section 1.5 and 1.6 present the objective and outline of the thesis by considering main goals and expected achievements at the completion of the thesis. The chapter ends with a summary.

1.1 Common Energy Harvesting techniques and their applications

Energy Harvesting, also known as Energy Scavenging, is the method of converting ambient energy to electrical energy, which can then be used to power electronic devices. The most well-known ambient energy sources for micro-power generation are light, heat, and vibration.

The power densities for various energy sources for 1-year and 10-year life time are shown in Table 1-1.

Table 1-1. The power densities for various energy sources [4]-[8]

Source	Conditions	Power density 1-year life time	Power density 10-year life time
Vibration	$1ms^{-2}$	100 $\mu W/cm^3$	100 $\mu W/cm^3$
Solar	Outdoors	7500 $\mu W/cm^2$	7500 $\mu W/cm^2$
Solar	Indoors	100 $\mu W/cm^2$	100 $\mu W/cm^2$
Thermal	$\Delta T=5^{\circ}C$	60 $\mu W/cm^2$	60 $\mu W/cm^2$
Batteries (Lithium)	Non-rechargeable	89 $\mu W/cm^3$	7 $\mu W/cm^3$
Batteries (Lithium)	Rechargeable	13.7 $\mu W/cm^3$	0 $\mu W/cm^3$
Fuel Cells (methanol)	-	560 $\mu W/cm^3$	56 $\mu W/cm^3$

According to Table 1-1, the power densities for natural energy sources stay constant over time. On the other hand typical energy sources like batteries have better performance than the energy harvesting sources for a fixed term, and degrade in performance with time. Dead batteries create environmental pollution if not recycled properly, which is another disadvantage of battery usage.

Due to above reasons, there is a strong research interest in energy harvesting. A wide range of applications are targeted for the harvesters, including distributed wireless sensor nodes for structural health monitoring, embedded and implanted sensor nodes for medical applications, recharging the batteries of large systems, monitoring tire pressure in automobiles, powering unmanned vehicles, mobile computing applications, and domestic security systems.

Photovoltaic energy harvesting is most commonly used method which converts the solar energy into electrical energy by using solar panels. This has been a very common practice used in many low power consumable electronics such as calculators, parking meters, weather stations, telephone boxes and traffic information systems [4]. Recent developments in photovoltaic technology enable extension of the application to notebooks as well [9].

The vibration energy harvesting can convert ambient mechanical energy into electrical energy. The kinetic energy can be found as form of vibration, random displacements or

forces, and can be converted to electrical energy using piezoelectric, electromagnetic, and electrostatic mechanisms [4]. Piezoelectric materials contain dipole which can create electrical voltage when subjected to a mechanical force. Conversely, when the electric field is applied, the material can be deformed due to the rotation of the dipole. Therefore, piezoelectric materials are used in a variety of commercial sensor and kinetic energy harvesting applications. The electromagnetic transduction is based on the Faraday's low of electromagnetic induction. This type of system can be found in bicycle dynamos, Seiko kinetic watches. The electrostatics generators are third most common method of kinetic energy harvesting. The system consists of charge variable capacitors and changes its capacitance due to the applied vibration. Due to the basics equation of Q=CV the output voltage or charge variation is generated by keeping constant either charge or voltage, respectively [4]-[10].

The thermoelectric (TE) based energy harvesters are third most common method of energy harvesting method, and it is main application area chosen in this thesis for the development of DC-DC converters. Converting thermal energy through thermoelectric devices into electricity is called thermoelectric energy harvesting, and can be found in many industrial applications like powering wireless sensors for structural buildings, sensors for engine health monitors, sensors for battlefield surveillance, and reconnaissance, as well as medical sensors and implants.

1.2 Principle of thermoelectric devices

The seebeck effect in a thermoelectric couple produces a voltage when the component is exposed to a temperature gradient. Figure 1-1 shows the basic schematic of the thermoelectric generator which consists of many thermoelectric couples (n- and p-type thermoelectric materials). The thermoelectric couples are connected electrically in series and thermally in parallel to make up a thermoelectric module.

When a temperature difference is applied across two junctions, the mobile charge carrier will move from hot end to cold end which creates a net charge at cold end. The net charge at the cold end will produce an electrostatic potential (voltage), and is given by,

$$V = \alpha \Delta T \tag{1}$$

where $\Delta T = (T_H - T_C)$ is the temperature difference between two junctions and T_H and T_C represent the hot and cold temperature values. α is the relative seebeck coefficient and its unit is $V.K^{-1}$ [4]-[10].

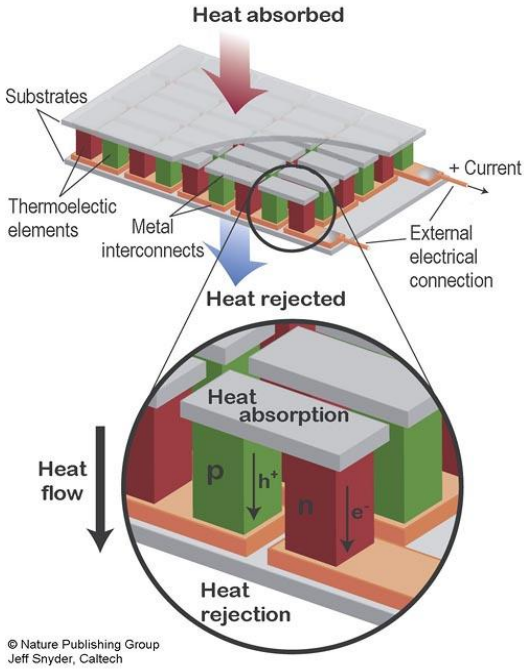

Figure 1-1. Schematic of a thermoelectric generator [11]

The seebeck coefficient in metals and metal alloys are few to tens of $\mu V.K^{-1}$, and is much higher in semiconductors which can be up to 1000 $\mu V.K^{-1}$. The conversion efficiency of a thermoelectric device is dependent on a dimensionless parameter called thermoelectric figure of merit (ZT),

$$ZT = \frac{\alpha^2.\sigma.T}{\lambda} \tag{2}$$

where λ is thermal conductivity and σ is electrical conductivity. According to Equation (2), a good thermoelectric materials should have a large seebeck coefficient to generate high voltage with large electrical conductivity to minimize the joule heating and low thermal conductivity to retain the temperature gradient between hot and cold junctions. The maximum ZT value can be obtained with bismuth telluride (Bi_2Te_3) and antimony telluride (Sb_2Te_3), and useful

power can be generated even with small temperature difference under 10°C. These materials are thus suitable for applications with low temperature gradient around 10°C [4]-[12].

The equivalent circuit for thermoelectric generator is shown in Figure 1-2.

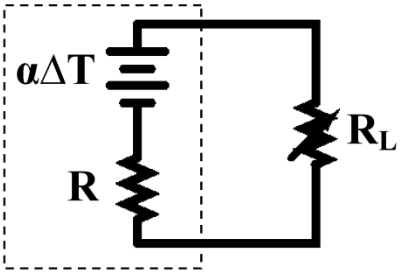

Figure 1-2. The equivalent circuit for thermo electric generator

The thermoelectric converter can be viewed as a thermal battery with generated voltage, $V=\alpha\Delta T$. Electrical voltage across the load is given by,

$$V = \alpha\Delta T\left(\frac{R_L}{R+R_L}\right) \tag{3}$$

where R_L and R are the load resistance and internal resistance of the thermoelectric converter.

The electrical power delivered to the load is given by:

$$P = \frac{s}{(1+s)^2}\frac{(\alpha\Delta T)^2}{R} \tag{4}$$

where $s=R_L/R$ is the ratio between load resistance and device internal resistance.

1.3 Application of thermoelectric energy harvesting

Seiko Thermic wristwatch is a microelectronic application example of thermoelectric energy harvesting, and is shown in Figure 1-3. It uses the human body as thermal energy source and converts the heat into electrical energy by using 10 thermoelectric modules which can generate sufficient microwatts required to operate the mechanical motion in the watch.

According to Moore's Law, the number of transistors on integrated circuits doubles approximately every two year. As the number of transistors increases, the reduction in power of a unit circuit becomes increasingly important [6].On the other hand the enhancement of integration and the shrinking of the device feature size lead to smaller and more sophisticated devices. Thus, more devices can be integrated within the same area as before, leading to a higher package density. With higher package density, the self-heating of the semiconductor devices and the interconnect lines become significant factors. The chronological evolution of selected microprocessors in terms of transistor integration density per die (a) and the observed power loss density per die (b) is shown in Figure 1-4 [14].

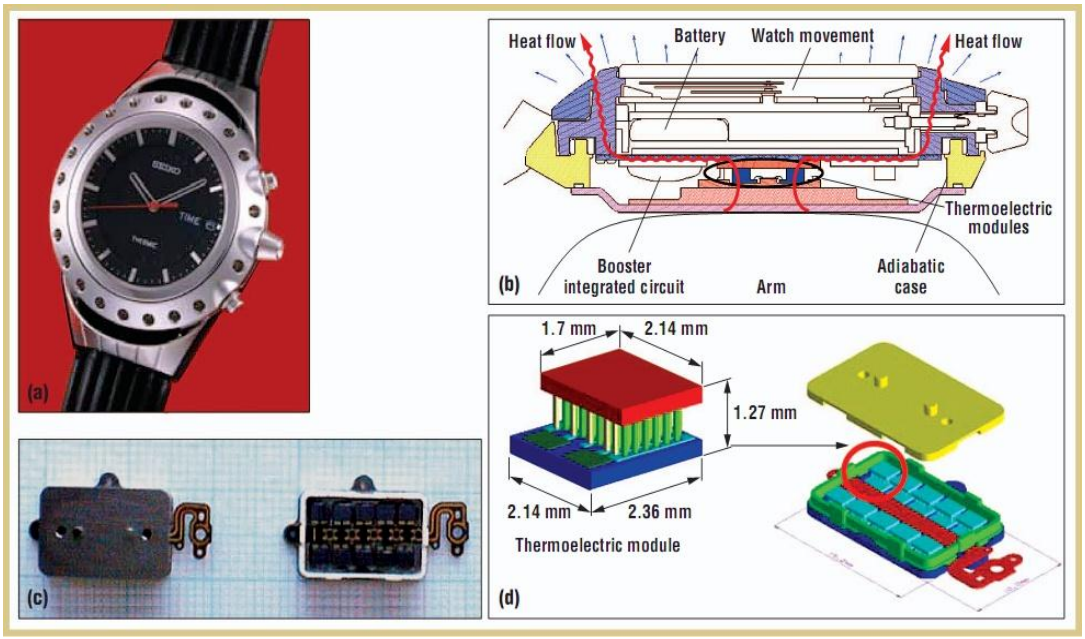

Figure 1-3. The Seiko Thermic wristwatch: (a) the product; (b) a cross-sectional diagram; (c) thermoelectric modules; (d) a thermopile array [13]

These problems cause researchers to find thermoelectric energy scavenging opportunities in Note book computers. Ali Muhtaroglu et al.[9] showed that the battery life extension can be achieved by scavenging waste heat from processors or other significant components in the computer's chipset by integration of Thermoelectric generators parallel with photovoltaic arrays. The integration of thermoelectric converter into a notebook computer is empirically investigated by [12].The results indicate that up to 1.26 mW/cm^3 of power can be harvested by using appropriate thermoelectric converter in surrounding area of the heat pipe in a large

notebook under realistic high activity scenarios. To use this harvested power in mobile computer application, fully integrated DC-DC converter is required which can work in µW power range and supply at least 1 V regulated voltage with at least 1 µW power [15].

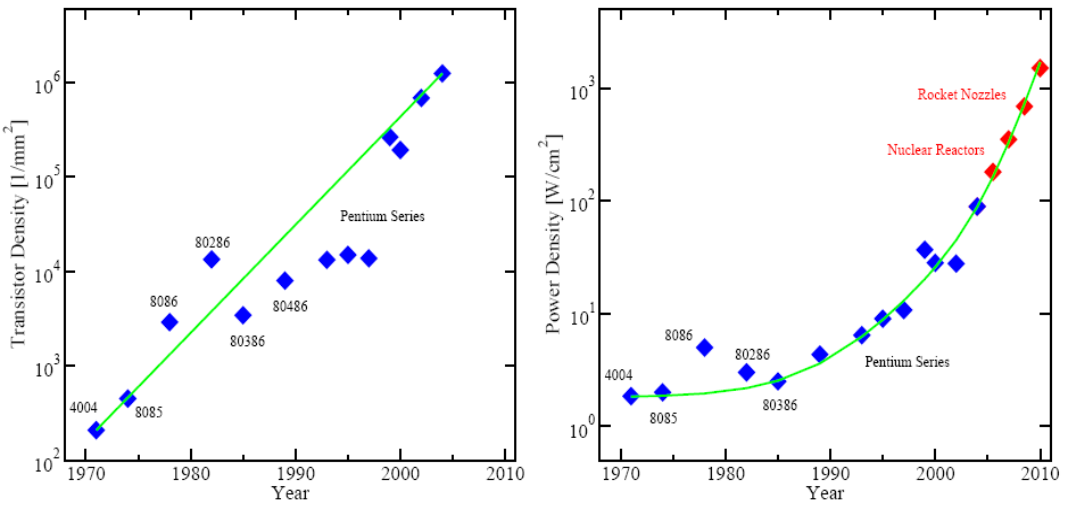

Figure 1-4. The chronological evolution of selected microprocessors in terms of transistor integration density per die (a) and the observed power loss density per die (b) [14]

1.4 Common interface circuit architecture for thermoelectric energy harvesting

When the voltage generated from thermoelectric device is not sufficient, power management systems are needed to power loads. The block diagram in Figure 1-5 depicts basic interface circuit architecture for thermoelectric energy harvesting system.

Figure 1-6 shows the interface circuit architecture proposed by [19], which is used for thermoelectric energy harvesting. The operation of the circuit can be explained as follows: When the output voltage drops below the V_{ref}, the comparator enables the oscillator which can provide 50% duty cycle square wave in order to control M1.When the clock signal is high, the input current increases and charges the inductor. When the clock signal is low, one-shot circuit activates the PMOS M2 and boosts the output voltage to the required level. The frequency control block is used to provide correct switching time for the circuit. The described circuit architecture can operate from input voltages ranging from 20 mV to 250 mV while supplying a regulated 1 V at the output with approximately 50% efficiency. However, it requires an external 4.7 µH power inductor and two 0805 SMD filter capacitors, and is not

suitable for full chip integration. Also, it required external supply to charge the output capacitor initially in order to start up the converter [19].

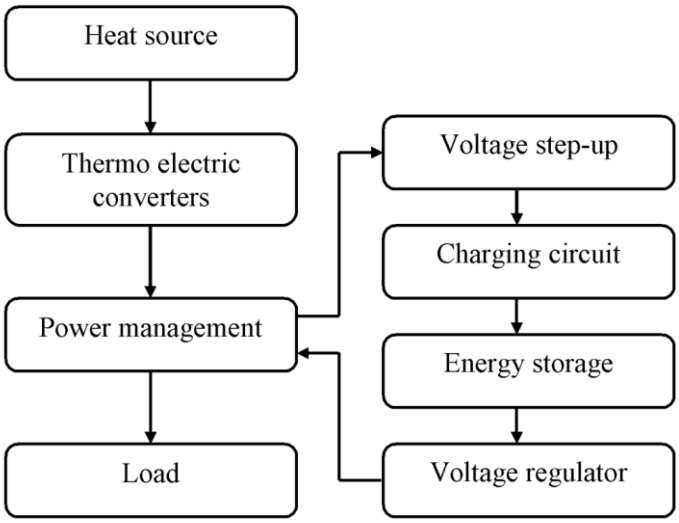

Figure 1-5. The block diagram basic interface circuit architecture of thermoelectric energy harvesting system [4]

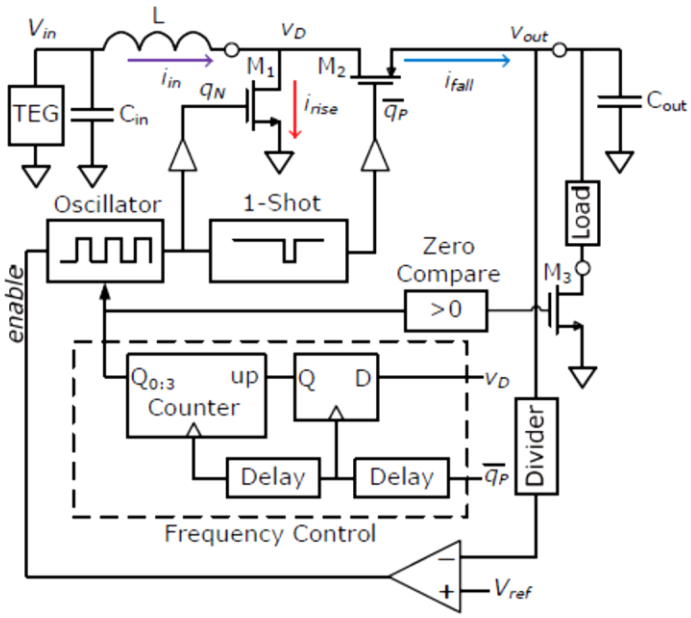

Figure 1-6. Boost converter circuit block diagram proposed by [19]

Off-the-shelf components, such as LTC 3108, are also available for ultra-low voltage step-up and power management [20]. The basic block diagram of the LTC3108 is shown in the Figure 1-7.

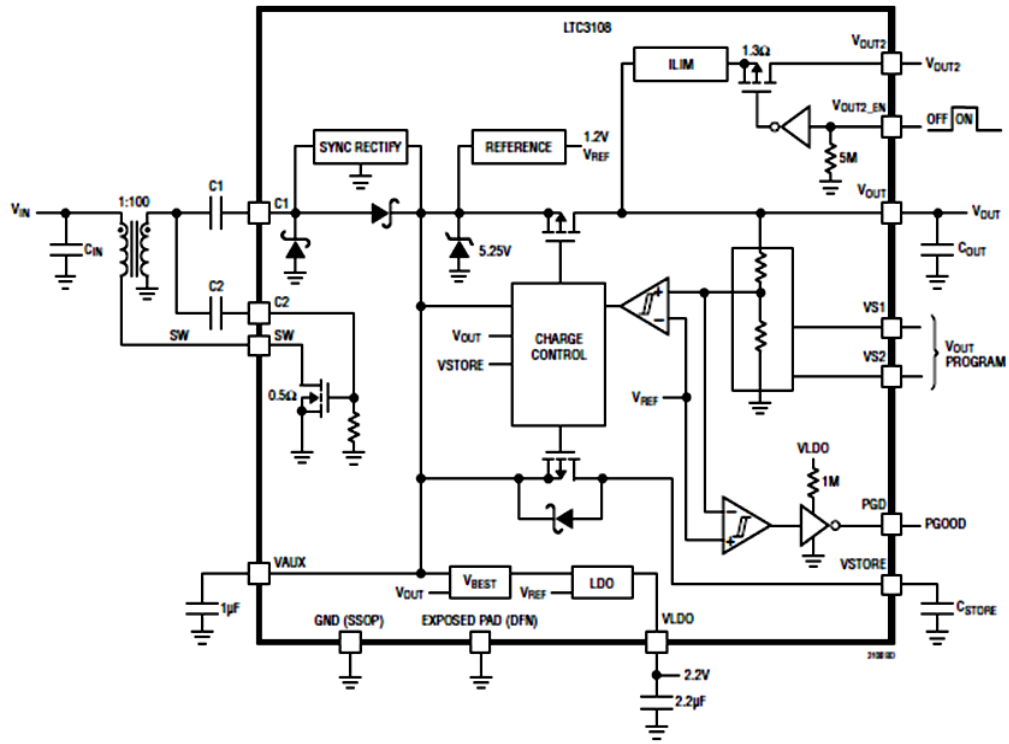

Figure 1-7. The basic block diagram of the LTC3108 [20]

It uses NMOS switch to form resonant step-up oscillator and step-up transformer to boost the voltages as low as 30 mV.When the input voltage reaches to its steady state, the voltage at the secondary coil and the V_{GS} (Gate to source voltage) of the NMOS switch are also increasing. Then, the voltage of the primary coil starts to decrease, which changes the current direction at both coils. This will create an oscillation. The stepped-up AC voltage from the secondary coil is rectified, and used to charge the auxiliary capacitor (VAUX). This auxiliary capacitor is used to provide a stable supply for the IC, and minimizes the ripple at the output voltage. Once it exceeds the 2.5V, the main V_{out} is allowed to start charging. The main output voltage on V_{out} is charged from the VAUX supply, and is user programmed to one of four regulated voltages (2.35 V, 3.3 V, 4.1 V and 5 V) using the voltage select pins VS1 and VS2.

The circuit can startup with input voltage as low as 20 mV. The system cannot work in large input voltage range with the same transformer. The system has 11% efficiency at the input voltage of 0.2 V [21]. However, the initial step-up requires an external transformer; therefore, the complete system cannot be integrated into a single chip.

Similarly, large numbers of boost converter based DC-DC converter topologies which contain external magnetic components such as inductors or transformers are available in the literature. There is an absence of thermoelectric energy harvesting systems with fully-integrated charge pump based DC-DC converters and low cost power conversion circuits that convert low input voltages to a usable output voltage (in 1 V and 1 μW power range), which can then be used to power up small loads, such as temperature sensors [22], utilized in context aware systems.

1.5 Objective of the Thesis

The aim of this thesis is to design and implement low voltage, low power, and fully integrated charge pump circuits for energy harvesting applications. The circuit validation is carried out using a thermoelectric converter as a power source. A comprehensive list of objectives of this thesis is as follows:

1. Study and specification of the blocks required for the integrated low voltage power conversion circuit architecture for thermoelectric energy harvesters.

2. Design and implementation of fully-integrated and self-starting charge pump circuit design. The proposed design converts the DC voltage generated by thermoelectric energy harvester with fully-self powered topology, which does not need any external battery. It has lower cost and compared to the implementations reported in literature, and higher validated efficiency than commercial alternatives. The DC-DC converter block efficiently boosts and regulates the output voltage to 1 V voltage with > 1 μW output power.

3. Implementation of a test platform for the fabricated interface electronics, validation, and comparison of performance against simulations with resistive loads, and using off-the-shelf TE modules as power supplies. TETECH model TE-17-0.6-1.0P(6mm x 6mm) [23] has been chosen as the TE harvester due to the ease of availability, and small size.

4. Design and implementation of an alternate integrated interface circuit using small integrated inductors and charge-pumps for ultra-low voltage applications with higher converter efficiency than that of the initial design that has charge-pumps only.

1.6 Thesis outline

The remaining part of the thesis consists of 6 chapters. Chapter 2 describes the basics principle of the charge pump circuits, clock generating circuits for charge pumps, and different types of regulation circuits required for the proposed low voltage charge pump based DC-DC converters. Literature review of fully integrated low voltage charge pump circuit designs are also included in this chapter. Lastly, fully integrated DC-DC converter topologies with inductors are discussed at the end of the chapter.

Chapter 3 introduces the design and simulation results of the fully-integrated low voltage charge pump based DC-DC converter for energy harvesting application, which was designed in UMC 180 nm CMOS technology. The theory of each of the blocks utilized in the designed system is explained in detail in this chapter, and design considerations for these blocks are provided.

Chapter 4 presents the experimental results obtained from the fabricated circuit in UMC 180 nm technology. The simulation-validation correlation has been presented in detail. The fully-integrated structure of the overall circuit is one of the main considerations of the system. The performance of the circuit is measured with a thermoelectric converter, and results are presented in the same section. The problems encountered with the fabricated chip are analyzed, and possible solutions are provided.

Chapter 5 provides the design and simulation results of the fully-integrated DC-DC converter with inductors in the first stage, which can overcome a fundamental problem identified with the previous design.

Chapter 6 finalizes the thesis by summarizing the achievements obtained from two alternate designs, and outlines the further study areas.

1.7 Summary of the chapter

In this chapter, different types of energy harvesting systems and their applications are introduced. The operation principle of thermoelectric energy harvesters and their applications are explained in detail. General interface electronics used for thermal energy based harvesters are briefly discussed. Also, the objective and outline of the thesis is presented by considering main goals and expected achievements at the completion of the thesis.

CHAPTER 2
BACKGROUND AND PREVIOUS WORK

2.1 Introduction

The main purpose of the energy harvesting systems is to utilize the ambient energy sources to power an applicable load. However, the voltage generated from energy harvesters is in the order of few tens of millivolts to a couple of hundreds of millivolts. This voltage has to be converted into a standard voltage which can be broadly used for other applications. The integrated power management circuits typically rely on standard CMOS technology that has higher MOSFET threshold voltage, in 250-400 mV range, depending on the technology, which is higher than the voltage range available from micro-power generating harvesters. Therefore, the key challenge is to develop a solution to startup from ultra-law voltages and provide regulated output voltage without using any discrete magnetic components. DC-DC converters convert the unregulated DC input into regulated DC output. There are two types of switching DC-DC converters[8]:

1. Inductive-based DC-DC converters
   This type of converters use a modulation technique to charge the inductor and boost the DC voltage by transferring the charge on the inductor onto the output capacitor. The operation of an inductive-based DC-DC converter used for thermoelectric energy harvesting system was explained in detail in section 1.4.
2. Capacitive-based converters
   Capacitive-based converters use a switching scheme which can transfer the charge between the capacitors by shifting DC voltage levels at each stage. Ideally higher stages can achieve higher boost voltage. There are mainly two types of capacitive based converters, charge pump based converters and switched capacitor DC-DC converter.

The block diagram of a typical charge pump based DC-DC converter for thermoelectric energy harvesting is shown in Figure 2-1. The voltage generated by the thermoelectric energy harvesters fluctuates; hence first stage of the system requires a storage element (Energy storage-1) to enable the charge pump circuit once the input voltage level reaches to an appropriate DC voltage.

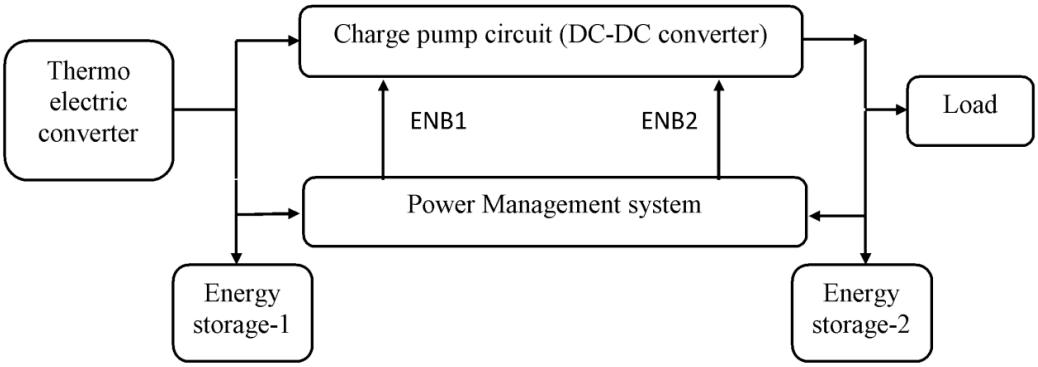

Figure 2-1. The block diagram of a typical charge pump based DC-DC converter for thermoelectric energy harvesting

The second stage of the system is a charge pump circuit that boosts the input voltage into appropriate DC voltage and stores it in Energy storage-2. Energy storage-2 can supply the required voltage for the load with minimum ripple. Once the output reaches the required voltage, the power management circuit will disable the charge pump circuit in order to save charge on Energy storage-1.

2.2 Charge pump circuit

The charge pumps are used to generate high voltage from low voltage. Charge pumps use capacitors as energy storage elements and pump the charges towards the output using switches to generate high DC voltage from the low DC voltage. These circuits can be found in flash memories, EEPROM, DRAM, etc [24]. The charge pump can be operated in a closed loop system by utilizing a regulator to keep the output voltage in a desired level. The basic block diagram of the charge pump operation circuit is shown in the Figure 2-2.

Initially, the output voltage of the pump is zero and the feedback system will enable the charge pump. The voltage regulator consists of a comparator to enable or disable the charge pump. It compares the value of the output voltage with the reference voltage in order to turn on or off the charge pump. After, enabling of the charge pump, the output voltage will be raised to the regulated voltage level. As soon as the output voltage reaches the regulated voltage, the voltage regulator turns off the charge pump. If the load is capacitive, the charge pump output should remain constant for long time. Practically, due to the load power consumption, leaking of output DC current, capacitive coupling from nearby signals and current dissipation in the

voltage regulator, the output of the charge pump will discharge with time. This causes the output voltage to go below the regulated level, which results in enabling of the charge pump by the voltage regulator, and the process keeps on repeating [7].

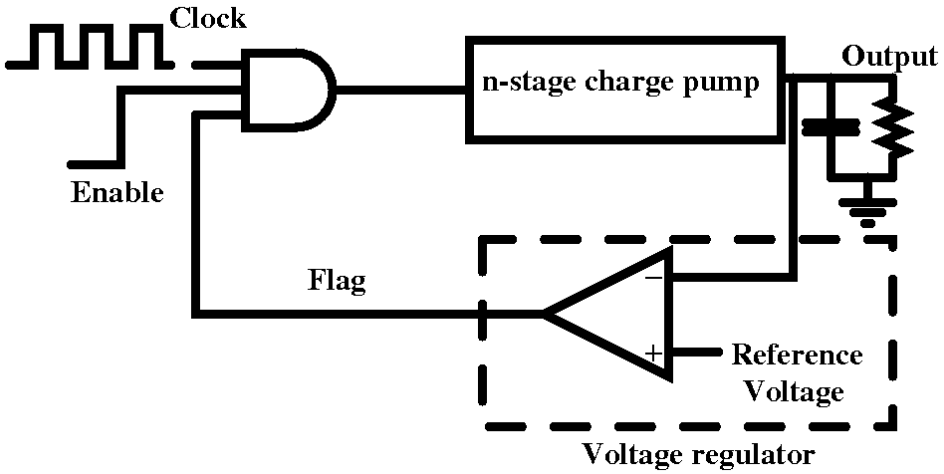

Figure 2-2. The basic block diagram of the charge pump based circuit [7]

Most charge pump circuits consist of Dickson topology. The conventional Dickson charge pump consist of capacitors interconnected by diodes and fed by two opposite phase clocks. In CMOS technology the diodes are replaced by diode-connected MOSFETs [7]. Figure 2-3 represents the MOSFET implementation of the Dickson charge pump.

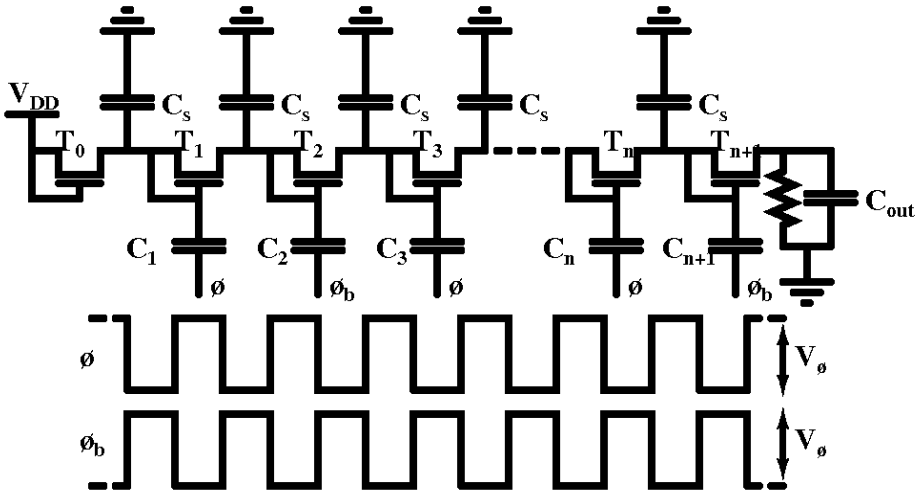

Figure 2-3. Dickson charge with diode-connected MOSFET [7]

Two out of phase clocks ϕ and ϕ_b with amplitude V_ϕ are capacitively coupled to alternate nodes. During each half of the clock cycle, the voltage at every other node is increased, pumping the packet of charge along the diode connected MOSFET chain. The difference between the voltages of n^{th} and $(n+1)^{th}$ is given by:

$$V_{n+1} - V_n = V_\Phi^1 - V_t - V_L \tag{5}$$

where V^1_ϕ is the voltage swing at each node, V_t is the threshold voltage of the MOSFET, and V_L is the voltage drop per stage due to the load current I_{load}. Due to parallel connection between stray capacitance, C_s and a clock coupling capacitance, C, the value of V_ϕ is reduced to V^1_ϕ as,

$$V_\Phi^1 = \left(\frac{C}{C + C_s} \right) V_\Phi \tag{6}$$

If the clock frequency is f, then the average load current can be written as follows:

$$I_{out} = f(C + C_s)V_L \tag{7}$$

Substituting for V^1_ϕ from (2) and for V_L from (7) and (6) into (5) gives,

$$V_{n+1} - V_n = \left(\frac{C}{C + C_s} \right) V_\Phi - V_t - \frac{I_{out}}{f(C + C_s)} \tag{8}$$

For N stages, the equation can be written as follows,

$$V_{out} = V_{dd} + N\left(\left(\frac{C}{C + C_s} \right) V_\Phi - V_t - \frac{I_{out}}{f(C + C_s)} \right) \tag{9}$$

An additional isolating diode connected MOSFET with the threshold voltage V_t is required to prevent the reverse current from the load. Then the equation (9) can be modified as follows:

$$V_{out} = V_{dd} + N\left(\left(\frac{C}{C + C_s} \right) V_\Phi - V_t - \frac{I_{out}}{f(C + C_s)} \right) - V_t \tag{10}$$

The threshold voltage of the NMOS transistor can be represented as follows:

$$V_t = V_{t0} + \gamma\left(\sqrt{\Phi s + V_{sb}} - \sqrt{\Phi_s}\right) \tag{11}$$

where ϕ_s is the surface potential at threshold, γ is the body effect coefficient, and V_{sb} is the source to body voltage bias.

In general, the bulk terminal of the MOSFET T_n is connected to the ground. According to equation (11) $V_{t,n}$ (threshold voltage of the n^{th} MOSFET) increases as the voltage at the each pumping node increases. This is called "body effect", and causes the voltage gain per stage to decrease as the number of stages increases [7]. Figure 2-4 represents the variation of V_t versus V_{sb}. For low voltage applications, threshold voltage and body effect coefficient become significant. Therefore, the voltage gain at each pumping stage and the maximum output voltage become much smaller with lower supply voltage. Therefore, the conventional Dickson charge pump cannot be used in low voltage applications, and new charge pump architectures are required in order to overcome these problems.

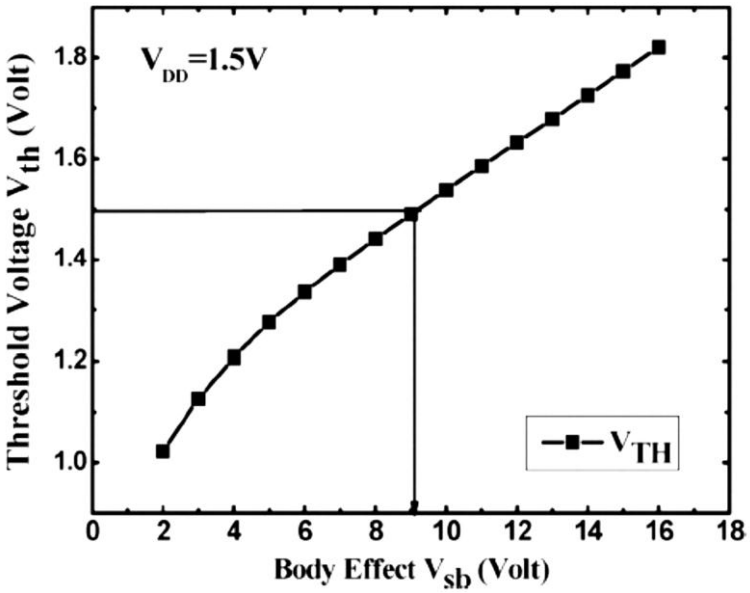

Figure 2-4. Variation of V_t with NMOS V_{sb} voltage [25]

2.3 Different charge pump architectures for low voltage application

By eliminating the body effect, the MOSFET circuits can be used for low voltage applications with acceptable efficiency. To enhance the pumping efficiency by reducing the body effect,

several circuit topologies were proposed. Wu and Chang [26] have proposed the NCP-2 charge pump in order to overcome the problems associated with Dickson charge pump. The proposed circuit topology is depicted in Figure 2-5. This circuit uses four charge transfer switches (CTS), each of which is controlled by MN's and MP's. The CTS are used to transfer the charges from one stage to another without suffering the problem of V_{th} voltage drop. The NCP-2 charge pump can boost the 1.2 V input voltage to 3.5 V. The efficiency of the charge pump and the measured results are not provided by the author.

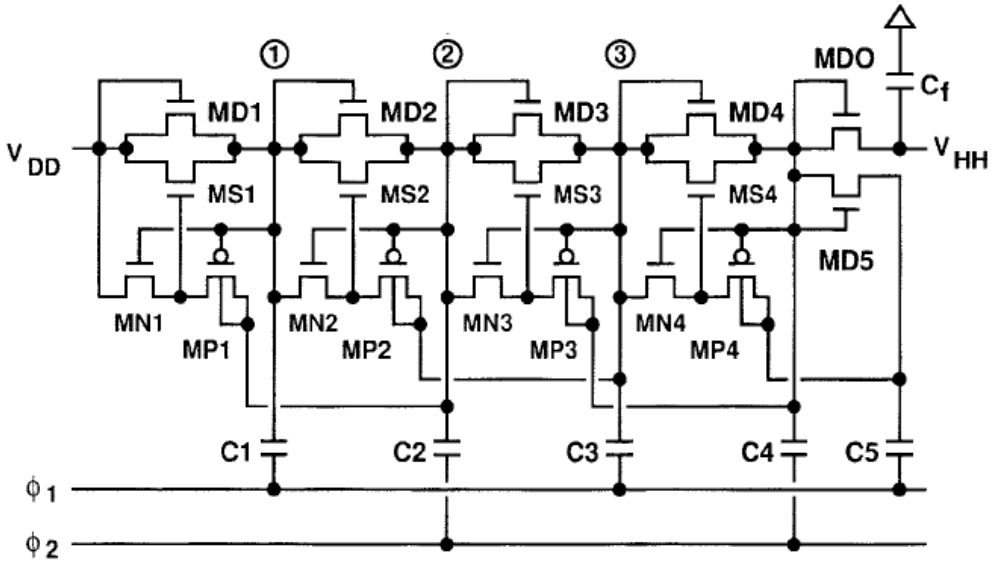

Figure 2-5. A four stage NCP-2 charge pump [26]

The output stage of the NCP-2 charge pump is a diode connected NMOS transistor, and this leads to reduction of the output voltage due to a body effect and hence not suitable for low voltage application.

Wang et al.[25] introduced a charge pump circuit which employs a novel charge transfer switch (CTS) control scheme that combines backward control and forward control. The four stage charge pump circuit, shown in the Figure 2-6, can start at 1.5 V, and provides 6.3 V output. MD1-MD4 are all diode connected MOSFETs, while MS1-MS3 and MS4-MS5 are NMOS CTS's and PMOS CTS's respectively. The operation of the first and second stages is the same as the NCP-2 charge pump circuit. The efficiency of the charge pump and the measured results are not provided by the author.

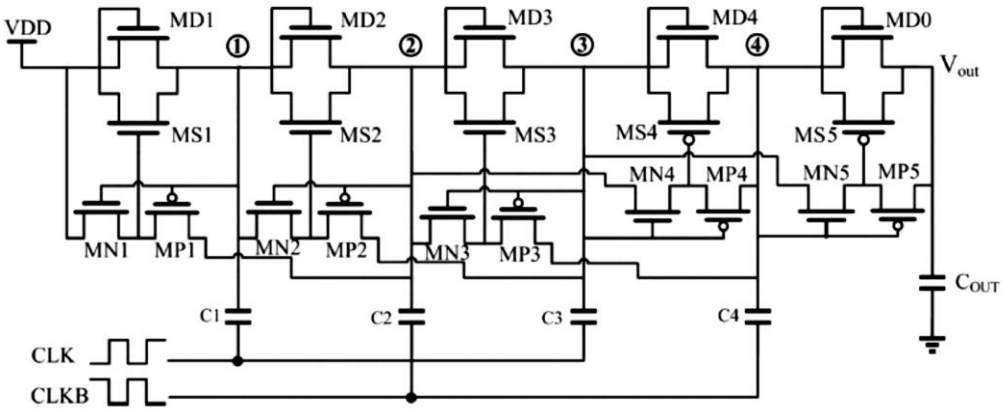

Figure 2-6. The charge pump circuit with CTS control scheme [25]

The charge pump topology introduced by Mishra et al.[27] can start up from 0.12 V input voltage, and generate 0.28 V output with 23% efficiency. For the input voltages of 0.18 V and 0.25 V, the generated output voltages are 0.75 V and 1.2 V respectively with 1 MΩ load resistance. The proposed topology by Mishra et al. is shown in the Figure 2-7.

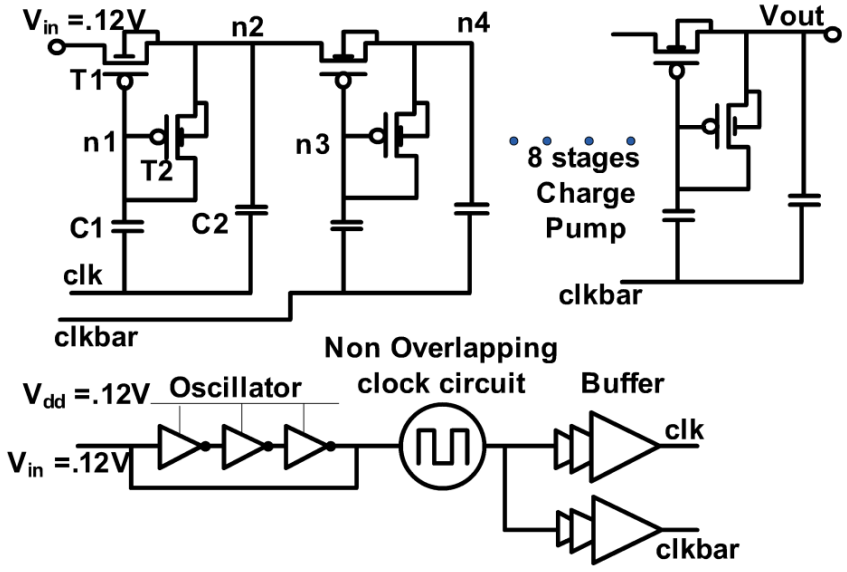

Figure 2-7. The schematic of the proposed topology by Mishra et al. [27]

Usage of C1 capacitor and T2 PMOS will help to improve gate source voltage (V_{gs}) of the T1 which can reduce the overall resistance of the circuit. The system was fabricated using 0.18µm technology and occupied an area of 0.69 mm^2.

The output voltage degradation was observed at ultra-low input voltages such as 0.12 V due to the very low current driving capability of PMOS transistors. Larger area and low driving capability are disadvantages with the described system.

Bhaleraoet al.[24] proposed a circuit which can be used for low voltage application around 0.9 V to 2.1 V. This circuit is an extended version of NCP-2 charge pump which is proposed by [26]. This version consists of cross connected NMOS cells and it pumps charge for entire duration of the clock period. The Figure 2-8 represents the charge pump circuit with cross connected NMOS cells. The circuit shows remarkable improvement at the output voltage compared to previously reported charge pump circuits. A modified and optimized version of this design has been implemented in 0.18 µm CMOS process and explained in the next chapter.

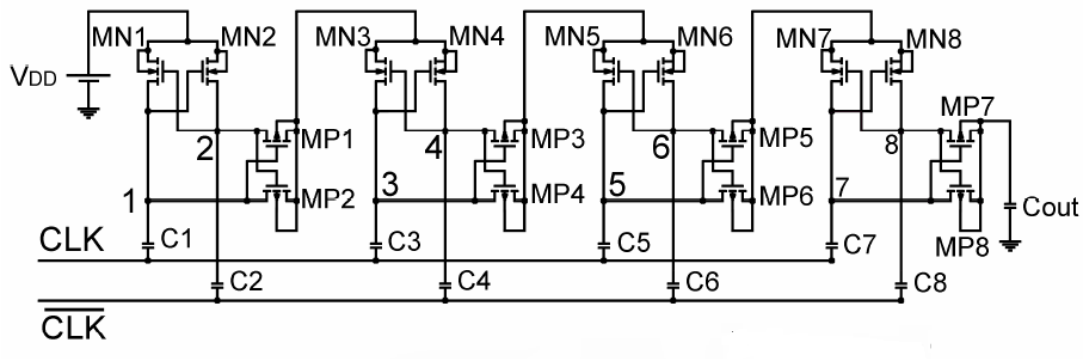

Figure 2-8. Charge pump circuit with cross connected NMOS cells [24]

In addition to the stand-alone charge pump designs, there are full DC-DC converter system design approaches with charge pump components. For example Chen et al.[28] proposed a circuit which can start with 0.18 V input voltage, and provide 0.74 V output with 6 mA output current. The circuit is fabricated in 65 nm technology. There are two stages in the system as shown in Figure 2-9. The first stage uses forward body biasing technique in the voltage doubler based charge pump circuit. Each body of NMOS is biased with the next stage output and each body of PMOS is biased with the input voltage of previous stage in order to reduce the threshold values of the MOSFETs. The charge pump can start at 0.18 V input and boosts the voltage to 0.5 V. This voltage is used to power the clock generator circuit, which provides an 80% duty cycle CLK with 0.5 V amplitude to the boost converter in order to boost the input to a higher output voltage. The circuit consists of an off-chip component (large discrete

inductor) which avoids the full integration of the design. Author doesn't provide the overall efficiency associated with the full system. Also, the body biasing technique on NMOS will require a special process for manufacturing, and hence carry a higher cost.

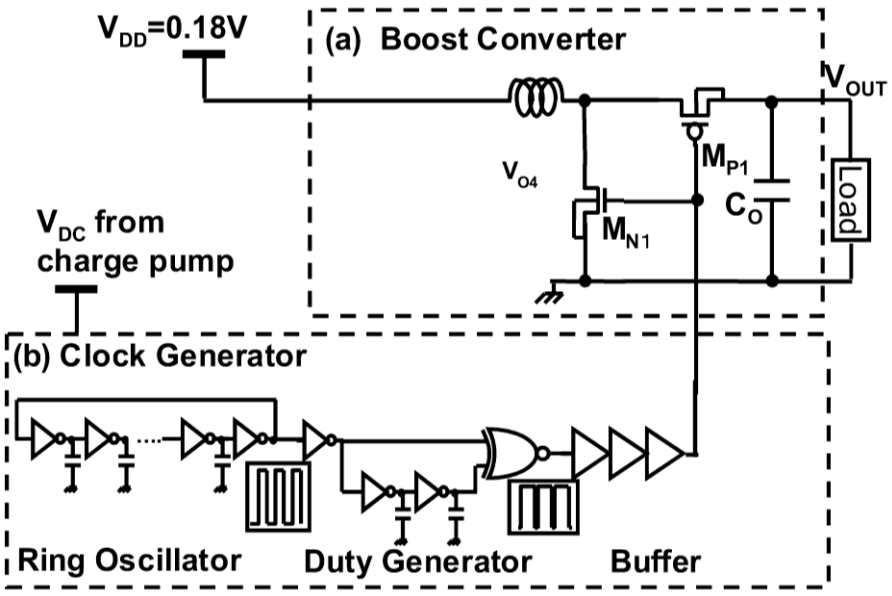

Figure 2-9. The block diagram of the proposed system by Chen et al. [28]

Kappelet al.[29] proposed a low voltage charge pump starting at 135 mV for thermal energy harvesting which can generate 0.65 V output while loaded by its own control unit. The proposed circuit by Kappel et al. [29] was fabricated in 130 nm process with an active area of 0.168 mm^2, and is shown in Figure 2-10. After applying a voltage to the input, the output node is pre-charged through the bypass diode. When V_{out} is lower than V_{in} , the supply selector select the input voltage as a input. Once the output voltage reaches to a higher value, the circuit drives from the output. This will require large output capacitor, in nF or µF range at the output, in order to supply current to the main circuit. The requirement of the off chip component will prevent the circuit to be used in on chip applications. The V_{sense} capacitor voltage unit monitors the inner voltage of the pumping stage and makes sure that the charge is fully transferred to the next stage. This also controls the frequency of the circuit, when it operates in higher voltage. Therefore, the control unit helps this circuit to work in wide range of input voltages (0.135 V-1.2 V). The 4 x tree charge pump topology proposed by [30] is utilized in the system as shown in Figure 2-11, which is modified to provide $8xV_{in}$ ideal output

voltage. The usage of tree charge pump topology helps to reduce the area consumption by capacitors as compared to the alternate architectures.

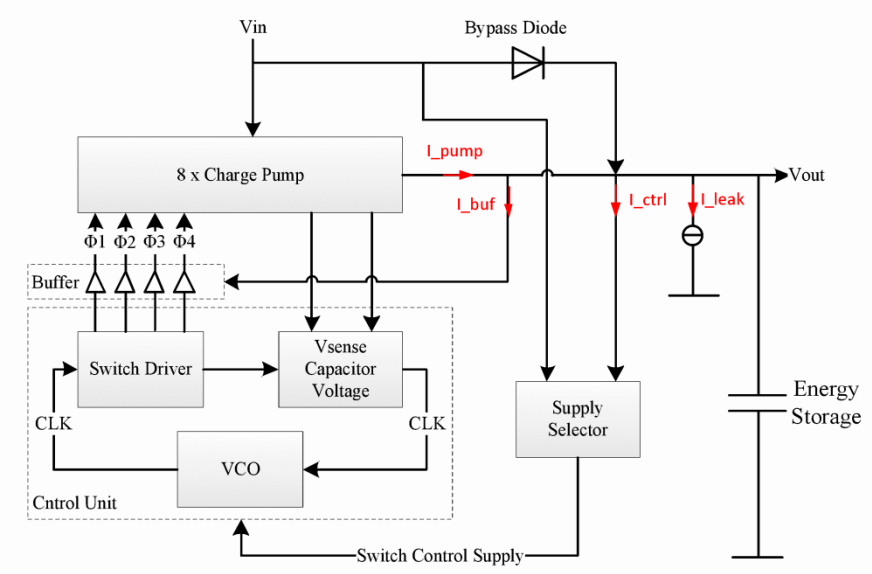

Figure 2-10. The block diagram of the proposed system by Chen et al. [29]

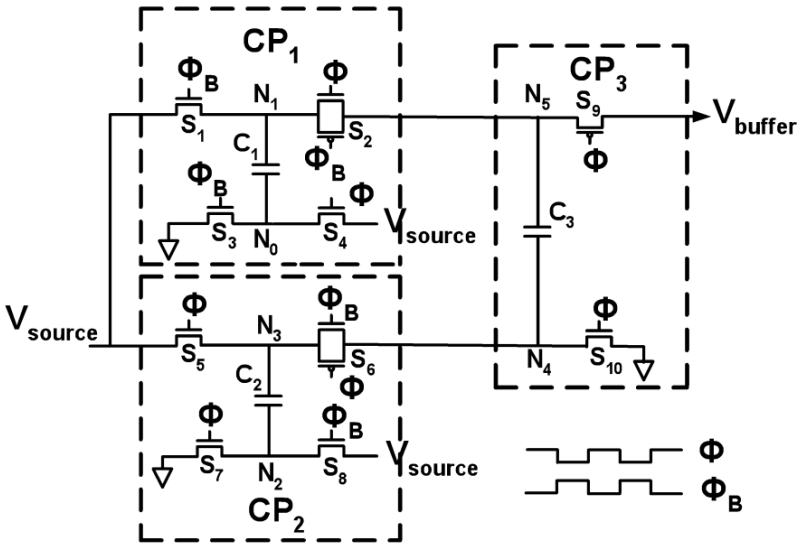

Figure 2-11. The 4 x tree topology charge pump proposed by Lu et al. [30]

Even though the circuit was reported to start with 0.135 V input, the characterization of the circuit with an external load was carried out with input voltages of 0.2 V and 0.25 V. Output

voltages of 0.65 V and 1 V can be generated at 1 µA load with the input voltages 0.2 V and 0.25 V respectively. Precharge phase causes delays, and prevents the circuit from responding quickly to any changes in the input voltage, which is a disadvantage of this system.

Recently published paper by Kim et al. [31] has introduced a charge pump based circuit which can convert 0.18 V input up to an unregulated voltage of 0.619 V at no external load condition. The design is depicted in Figure 2-12. The circuit uses SW-G (Switch conductance enhancement) enhancer circuit, which contains 2-phase negative charge pump to control the two series switches in the voltage doublers. The circuit has 34% efficiency at the input voltage of 0.18 V. Even though the efficiency is high compare to the other designs, the circuit cannot deliver high output voltage at ultra-low input voltages.

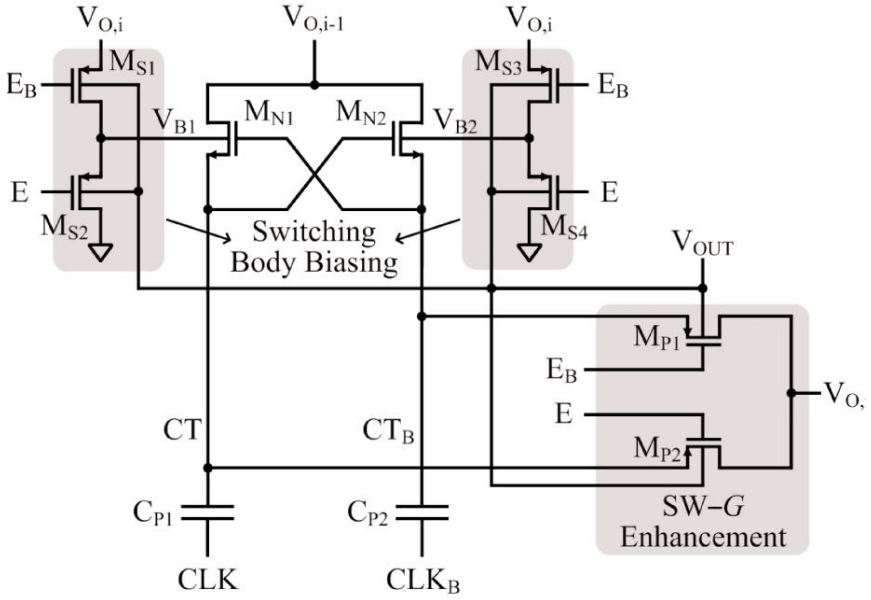

Figure 2-12. Unit Charge pump circuit with switching body biasing and conductance-enhanced dual-series switch [31]

The low output voltage levels are acceptable and possibly beneficial for low power digital operation. It does not provide sufficiently high supply voltage, however, required for analog subsections of the standard 1 V systems [15]. In addition, 10 nF pumping capacitors used in the proposed design require a very large area for integration, and higher cost if the capacitors are discrete. The paper [11] proposes a switching body bias technique to control the body of

the NMOS in the charge pump in order to enhance the efficiency of the circuit. This type of integration typically requires special processing which increases manufacturing costs.

The inductorless DC-DC converter presented in [15] is capable of starting with input voltage as low as 270 mV without any external excitation, and provides 0.81 V unregulated output voltage. However, it requires 0.40 V input voltage in order to generate 1.4 V regulated output. The requirement of the higher input voltage is main disadvantage of this system. It is desirable to further reduce the low voltage limit to open up the application of such circuits to systems with thermoelectric micro-modules.

A novel interface circuit topology was presented in 90 nm by our group [21] with power management, which started up from input voltage as low as 0.2 V based on simulations, and generated 2.3 V with 12% of maximum efficiency as shown in the Figure 2-13. Comparative analysis was also performed with a commercial low voltage DC-DC converter (LTC3108) to identify the relative advantages and disadvantages of the integrated approach. The operation of the circuit can be explained as follows.

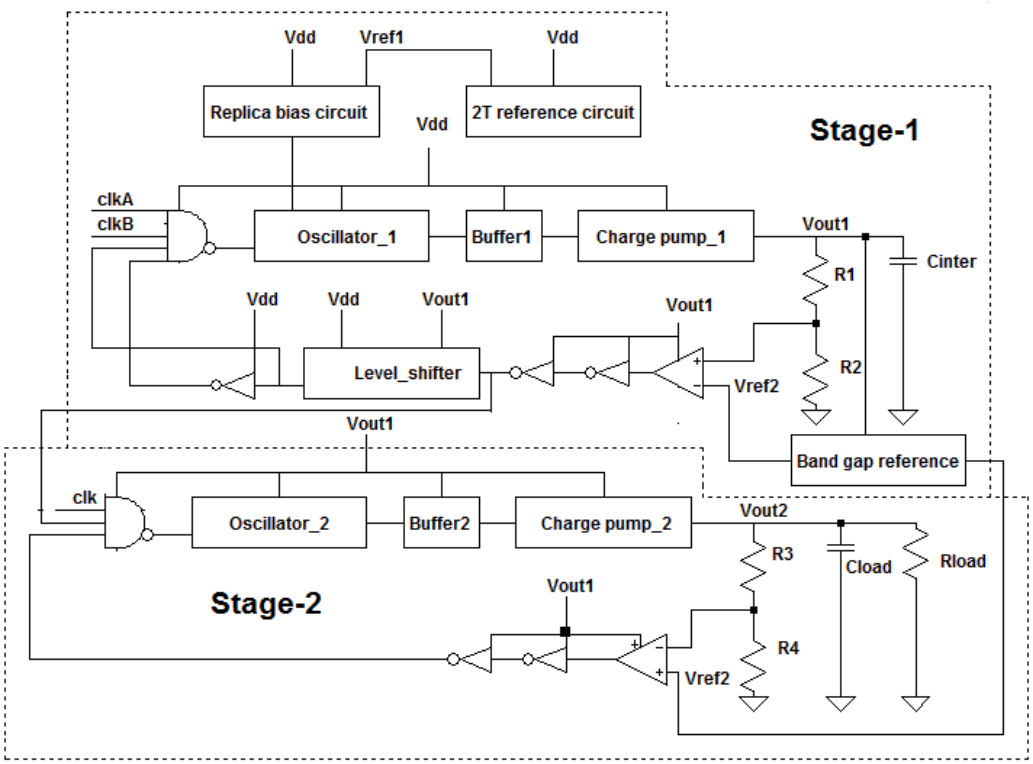

Figure 2-13. The proposed interface circuit topology presented by our group [21]

The system is operated in closed-loop to regulate the output voltage. The voltage regulator consists of a comparator, which enables or disables the charge pump depending on the output voltage level. The level shifter in the circuit provides 0 V and 0.2 V when the output voltages of the pump are 0 V and 0.5 V. The clkA and clkB represent the differential clock output signals, generated from subthreshold source couple based oscillator. Initially, the output voltage of the pump at 1st stage is zero, hence the regulator enables the charge pump. It compares the value of the output voltage with the reference voltage in order to turn on or off the charge pump. After enabling the charge pump, output voltage rises to the regulated voltage of 0.5 V. As soon as the output voltage reaches the regulated voltage, the voltage regulator turns off the charge pump in the 1st stage and turns on the 2nd stage. When the output voltage of the charge pump of 2nd stage reaches to its regulated voltage of 2.3 V, then the voltage regulator turns off the charge pump of the 2nd stage, starts the 1st stage and repeats the process [21].

The efficiency of the proposed circuit and LTC3108 were analyzed using same load range of 500 kΩ - 5000 kΩ. For the proposed circuit, the input power is approximately 15.5 μW while the output power is in the range of 0.8-1.3 μW (efficiency 12%). The input and output power of the LTC3108 are in the range of 8-9 mW and 1-11 μW (efficiency 0.12%). Since the efficiency of LTC3108 is low for the large load resistances, it is simulated again under the small load resistance conditions (6kΩ to 20kΩ), and observed 11% of maximum efficiency for the input voltage of 0.2 V [21]. The first charge pump stage required relatively large capacitors (90 pF) and MOSFETs for on-chip integration to compensate for the high MOSFET threshold values, which led to large area requirement, and hence higher cost. The system contained two back-to-back independently regulated stages, which led to frequent on/off behavior at the second stage, resulting in efficiency drops. These disadvantages of the proposed system will lead us to propose a new charge pump topology as explained in the next chapter.

2.4 Fully integrated DC-DC converters with inductors

There is very limited number of papers available in the literature for integrated DC-DC converters with inductors for ultra-low voltage applications. Bassi et.al [32] presented a fully-integrated DC–DC converter for thermal energy harvesting which can start from the input voltage low as 0.14 V. The proposed converter is shown in Figure 2-14. The clock generating

circuit proposed by [33] is used by replacing the transformer with four planer inductors with sizes of 15.5 nH x 2 and 3.3 nH x 2.The modified charge pump circuit proposed by [33] is used by replacing PMOS switches with diode connected NMOS switches in order to maximize efficiency.

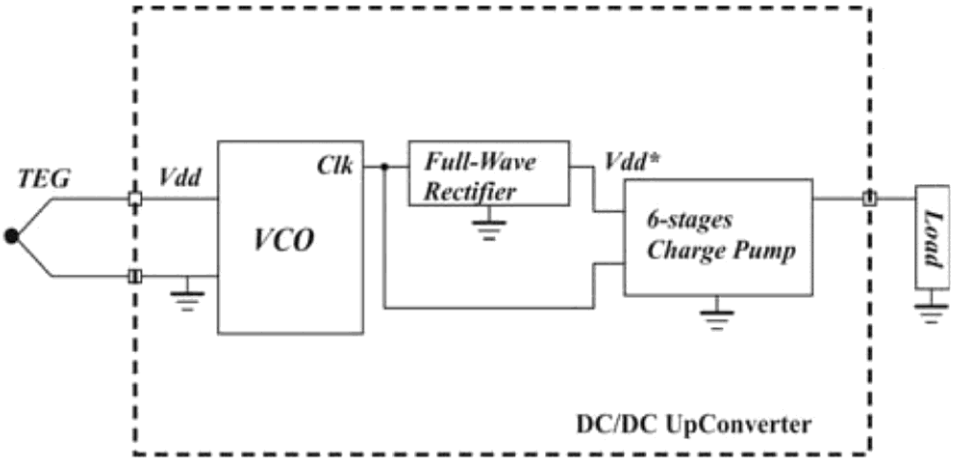

Figure 2-14. The first DC-DC converter proposed by Bassi et.al [32]

The full wave rectifier is used to generate input voltage to the charge pump. The final sizes of the NMOS's in the charge pump circuit is W= 800 μm and L = 800 nm. The integrated capacitor of 1 nF is used as a buffer. The converter can generate 1.28 V output from 0.2 V input with 19.8% efficiency. Requirement of large area is the main disadvantage of this converter. In addition, the paper does not provide any details of the inductor modeling and associated parasitic values used during the simulation. The validation results are also not provided by the author. Due to the missing information and data, the efficiency may not be accurate.

Hernandez et al.[34] presented a fully integrated boost converter that allows energy extraction from low voltage thermoelectric generators. The converter uses a 22 nH integrated metal-track inductor, and provides a 1.1 V regulated output voltage from 30 0mV of input voltage and 45% of maximum efficiency in normal operation. The proposed boost converter by Hernandez et al. [34] is shown in Figure 2-15.In order to start the boost converter, C_{OUT} capacitor (1200 pF) must be pre charged up to 0.75 V. A charge pump circuit with 10 stages (based on the Dickson charge pump topology) is utilized to pre-charge C_{OUT} until the control

circuit can operate. This is the start-up mode of the circuit. After C_{OUT} is charged up to 0.75 V, the circuit will work in normal operation and the charge pump circuit will be disabled. Then the oscillator will start and provide a 10 MHz 50% duty-cycle square signal that controls a short pulse generator circuit. A 4 ns (T_{ON}) pulse is generated for each rising or falling edge of the oscillator signal which controls M_N. During T_{ON}, M_N transistor remains turned on and charges the inductor. Once T_{ON} has elapsed, the discharge current of the inductor charges C_{OUT} capacitor through D_1 Shockley diode resulting in a boost of the output voltage [34]. The circuit can operate with a wide range of inputs from 0.3 V to 0.8 V, which is an advantage of this system, and occupies0.63mm^2. The measured results are not provided by the author.

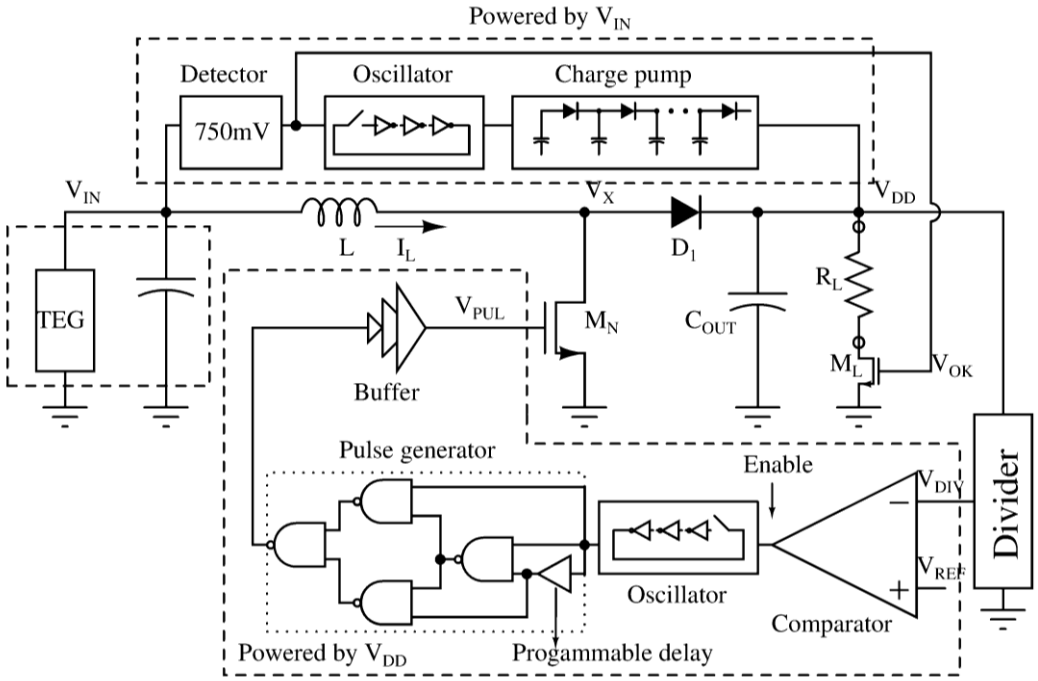

Figure 2-15. The proposed boost converter by Hernandez et al. [34]

There is very limited amount of validation, and plenty of simulation data present in the literature. For example, [21], [24], [25], [32], [34], [35], and [36] on low voltage charge pump based DC-DC converters only provide simulations, which is inhibitive in enabling the industry to integrate low-voltage thermoelectric energy harvesting ubiquitously. This thesis is able to fill the gap in the literature by introducing fully integrated charge pump based DC-DC converters with detailed simulation-validation correlation.

2.5 Clock generating circuits

Oscillators are the integral part of the charge pump circuit. In order to operate the charge pump properly, the clock should have appropriate frequency, amplitude and charge drive capability. An oscillator can be described as positive feedback system and it amplifies its own noise at certain frequency [37].

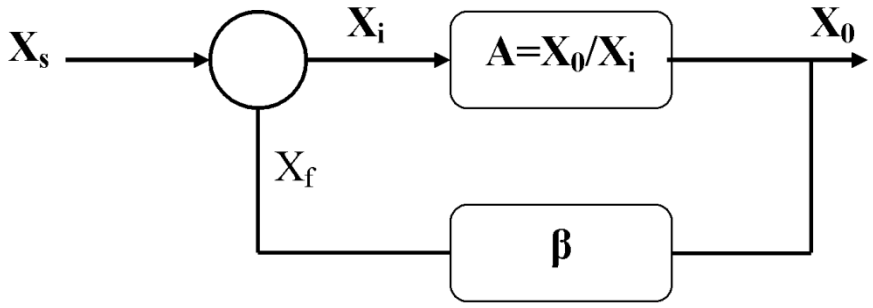

Figure 2-16. Feedback diagram for an oscillator [37]

$$X_0 = AX_i = A(X_s + X_f) = A(X_s + \beta X_0) \tag{12}$$

$$A_f = \frac{X_0}{X_s} = \frac{A}{1 - A\beta} \tag{13}$$

If $A\beta=1$ $A_f \rightarrow \infty$ which means $X_s \rightarrow 0$, the oscillation can happen without any input signal.

In order for steady oscillation to occur, the circuit must satisfy with Barkhausen criteria;

1. $A\beta=1$
2. $\angle A\beta = 0^0 \text{ or } 2\pi$

These conditions are necessary but may not be sufficient to ensure oscillation.

2.5.1 Ring oscillator circuit

Most of the fully integrated charge pump based DC-DC converters presented in the literature, such as [15], [29] and [38], used traditional ring oscillators as their clock generator. The ring oscillator consists of odd number of inverting gates, connected in a ring pattern. A NAND

gate replaces one of the inverters to enable the oscillation. The frequency of the oscillation can be expressed as follows:

$$f = \frac{1}{N(t_{phl} + t_{plh})} \tag{14}$$

where t_{phl} is the signal propagation delay through an inverter stage from high to low state, and t_{plh} is the signal propagation delay form low to high state. N is the number of stages of the oscillator. For properly sized gate t_{phl}=t_{plh}, Therefore equation (14) can be rewritten as follows:

$$f = \frac{1}{2NT_D} \tag{15}$$

where T_D is the propagation delay which is equal to t_{phl} and t_{plh}. Figure 2-17 represents a seven stage ring oscillator.

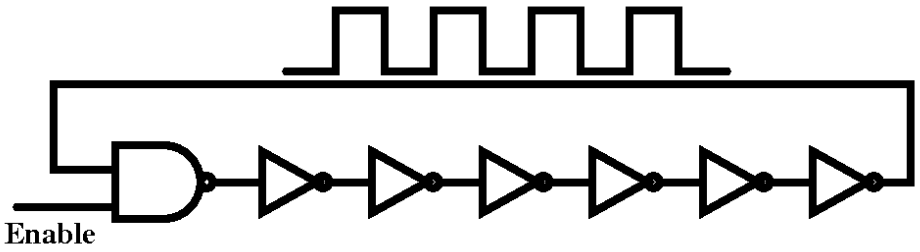

Figure 2-17. A seven-stage ring oscillator [7]

When the ring oscillator is used for the ultra-low voltage application with input voltage around 0.1-0.2 V several problems arise. Power dissipation and dependency of the voltage swing on input voltage for example lead to poor performance for the charge pump circuit in low voltage applications.

2.5.2 Source-couple based oscillator

Source-coupled logic (SCL) circuits are widely used in high frequency applications. In an SCL gate, the logic operation takes place mainly in current domain. Therefore the speed of

operation can be inheritably high. The logic network consists of NMOS source-couple differential pairs. The tail bias current I_{ss} is controlled by the NMOS as shown in the Figure 2-18. The output load resistance (R_L) converts the branch current back to the voltage domain in order to drive the subsequent SCL gates [39].

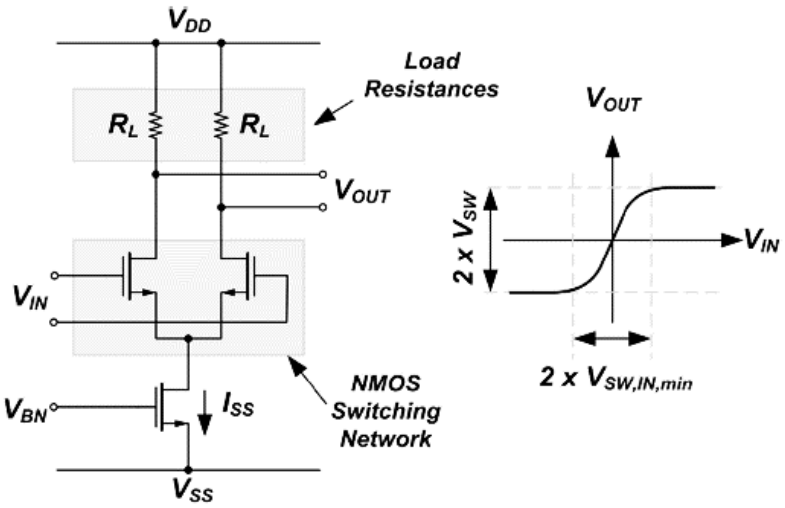

Figure 2-18. A conventional SCL-based inverter/buffer circuit [39]

The load resistances can be implemented using PMOS devices biased in triode region. Figure 2-19 depicts the oscillator design based on the SCL.

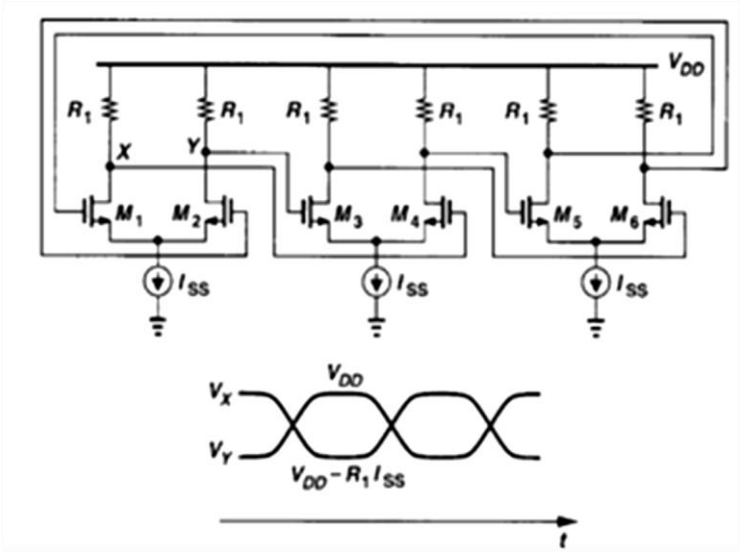

Figure 2-19. Source-couple based oscillator [40]

To implement very low power systems, it is necessary to minimize the power dissipation in the circuits. This topology also has the same problem when it comes to the ultra-low voltage application. At very low input voltages, such as 0.2 V, the conventional SCL circuit design fails to provide any oscillation. Therefore, it needs to be modified to work in the subthreshold region. Tajalliet al. [39] and Wang et al.[41] have introduced the potentials of subthreshold oscillator circuits as an alternative solution for implementing ultra-low-power digital systems. From the approach introduced by Tajalliet al. [39], the power consumption and maximum speed of operation can be adjusted linearly through the tail bias current of each gate over a very wide range, thus efficiently decoupling the decision of output voltage swing from power dissipation and delay. A modified and optimized version of this design has been implemented to generate the clock for the proposed charge pump circuit in 0.18 µm CMOS process, and is explained in the next chapter.

2.5.3 LC tank based oscillators

The dominant portion of the power is dissipated at the clock drivers for most of the low power charge pump based circuits. The LC oscillators can remove the drivers and can reduce the power consumption of the overall clock distribution. Therefore, fully integrated resonant clocking has become an interesting research area recently. However, in order to recover energy from the oscillator efficiently, the inductors with high quality factors are needed.

The resonant based oscillator has an LC tank which acts as frequency selective element. The typical schematic of the LC oscillator is shown in Figure 2-20. The resistive loss of the tank (labeled R_p) should be compensated with negative resistance (labeled–R_a) which provides the energy into the tank [37].

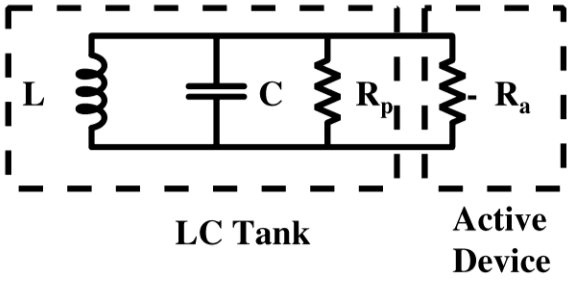

Figure 2-20. Schematic of the LC oscillator [37]

The stable oscillation can be obtained when the energy loss is equal to the energy provided by the active device.

The effective impedance ($Z(j\omega)$) of the LC oscillator can be expressed as:

$$Z(j\omega) = \frac{1}{\frac{1}{j\omega L} + j\omega C + \frac{1}{R_p}} \tag{16}$$

At resonance, $Z(j\omega)$ value is real, and satisfies the phase condition of the Barkhausen criteria. Therefore, the frequency of the resonance (f_0) is given by,

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{17}$$

The magnitude condition can be satisfied by setting $R_p / R_a \geq 1$.

If a voltage V_E is applied across the LC tank, the average power dissipated by the LC tank is given by [37]:

$$P_{avg} = \frac{V_E^2}{2R_p} \tag{18}$$

Differential type LC oscillators are very popular in RF designs due to their simple topology and good phase noise performance [42] due to differential implementation. As monolithic inductors have appeared in CMOS technologies in the past decade, the design of integrated LC oscillators have become an active research area [43].

Hansson et al.[44] presented an on chip differential resonant clock oscillator, which directly drives 2x896 flip-flops without intermediate buffers. The oscillator works in 1.56 GHz frequency at 1 V supply voltage, and is shown in Figure 2-21.Even though it can generate a clock signal with 1.2 nH inductor, and minimum width NMOS and PMOS, larger inductance and widths of MOSFETS are required when the circuit is powered by ultra-low supply voltage, such as 0.2 V. This leads to higher area requirement on die, and is one of the disadvantages of the system for low voltage system on chip application.

The inductive based ring oscillator proposed by Machado et al.[45] can generate oscillation at 53 mV which makes the topology suitable for energy harvesting applications such as DC-DC converters operating from very low voltages. However, 100 nH total inductance is required to generate the clock signal, without any boost in amplitude.

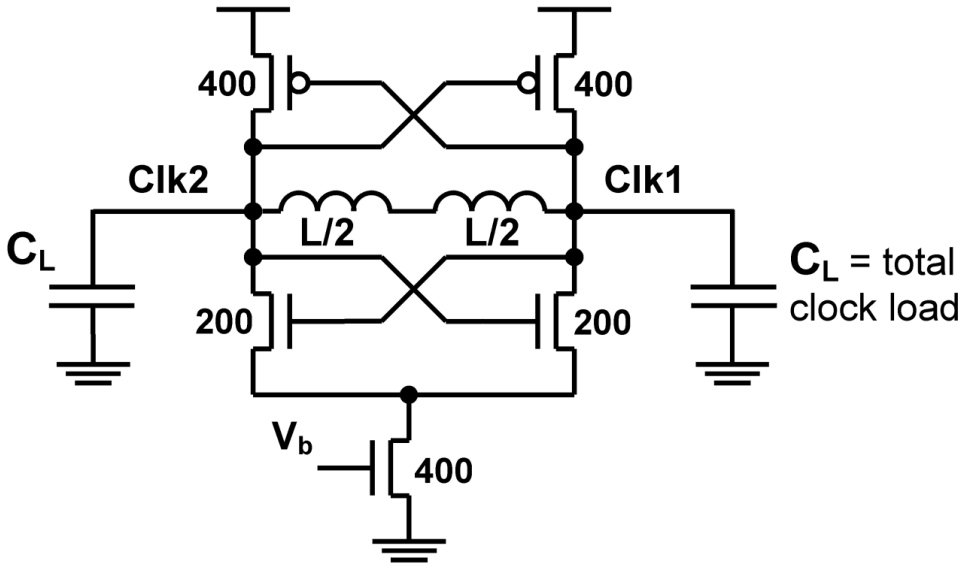

Figure 2-21. Differential complementary oscillator proposed by Hansson et al. [44]

Schematic diagram of an N stage inductive ring oscillator is shown in Figure 2-22.

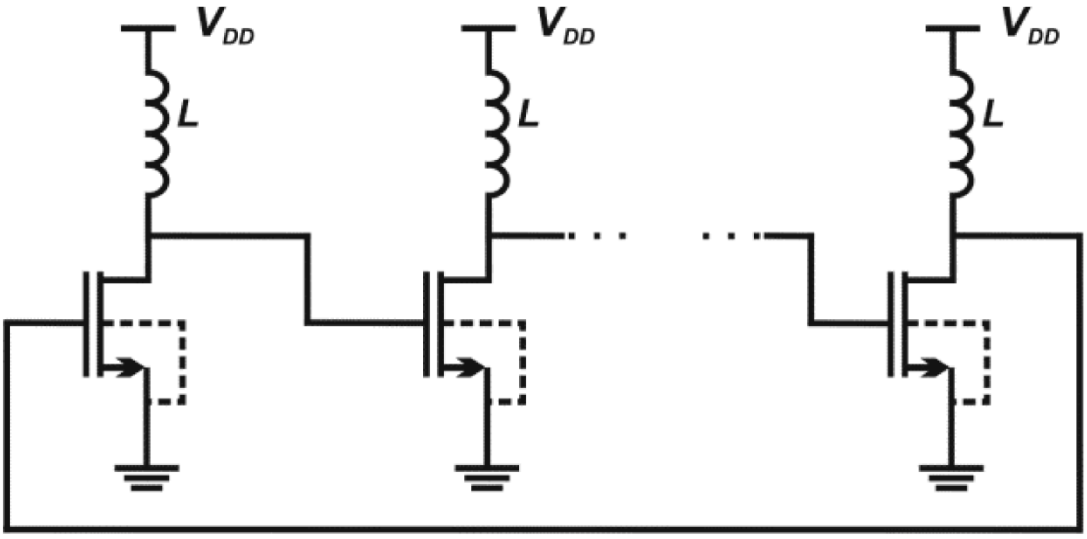

Figure 2-22. Schematic diagram of an N stage inductive ring oscillator [45]

Even though, the topology can generate the clock at 53 mV by utilizing zero-Vt NMOS transistors, it cannot switch on the MOSFET's in the charge pump circuit due to lower amplitude of the clock which is far below the threshold value of the MOSFETs in the typical CMOS technology. This is a disadvantage of this topology. The leakage current will also be significant if zero-Vt NMOS transistors are utilized in the charge pump.

Kwok and Luong [46] proposed an ultra-low-voltage high-performance CMOS voltage controlled oscillator (VCO) using transformer feedback which can generate a clock signal at 0.35 V with 1.4 GHz frequency and 1.46 mW power consumption. The proposed transformer-feedback VCO design is shown in Figure 2-23.

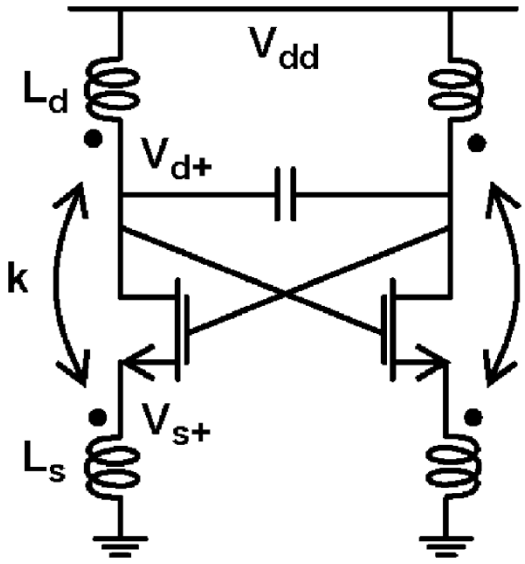

Figure 2-23. Transformer-feedback VCO design proposed by Kwok and Luong [46]

The transformer's primary coil with self-inductance L_d is connected to the drain to create an LC tank. The secondary coil has self-inductance L_s. The coupling between two coils is k. The main advantage of this circuit is that the drain voltage could swing above the supply voltage and the source voltage could swing below the ground potential due to the transformer feedback, which makes the design a suitable clock generator for the charge pump that works in ultra-low input voltages. However, design and analysis of an integrated transformer in standard CMOS technology is not an easy task due to the limited support in the computer aided design software, such as Cadence. It consumes a lot of time to optimize a design of a

transformer which can work at ultra-low voltage input value (below 0.35 V) which is a disadvantage of this design.

Hsieh and Lu [47] introduced a modification to the work by Kwok and Luong [46] and were able to replace the transformers in the design with the capacitive feedback. The designed oscillator can generate 1.4 GHz frequency at 0.35 V with 1.5 mW power consumption. The schematic of the proposed VCO topology by Hsieh and Lu is shown in Figure 2-24.

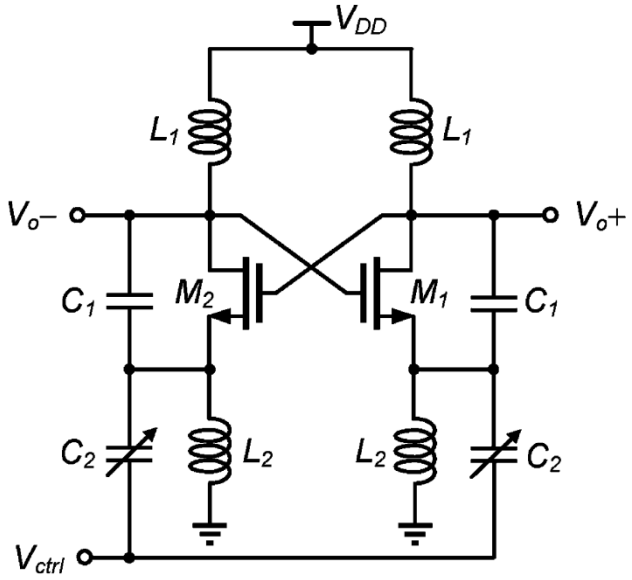

Figure 2-24. The schematic of the proposed VCO topology by Hsieh and Lu [47]

A modified and optimized version of the designs in [46] and [47] has been implemented to generate the clock for the second proposed charge pump circuit design in 180 nm CMOS process, which is explained in chapter 5.

2.6 Pump regulation design

As previously discussed, pump regulation is very important especially when it comes to the ultra-low power application. The resistor divider feedback is common as shown in Figure 2-25. However, the basic design has several issues. Among them, power consumption is important since this research is focused on low voltage, low power applications. Also, the process corner variation in poly resistors in 180 nm technology should be considered. Post layout Monte Carlo simulation can be run in order to identify the process variation.

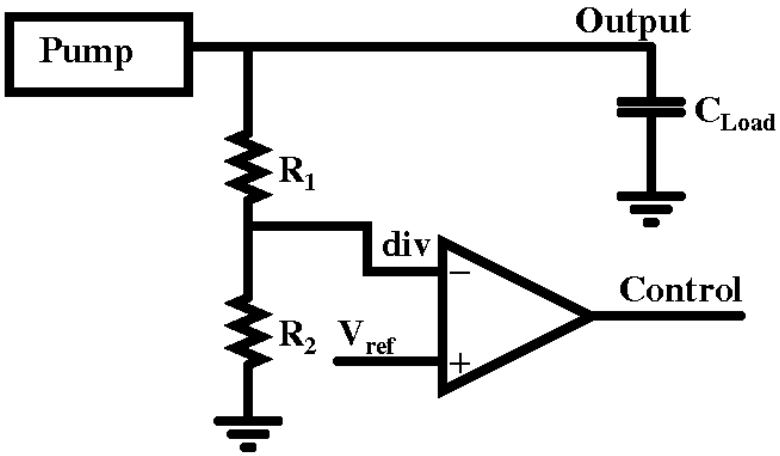

Figure 2-25. Resistive divider feedback control [7]

The output of the circuit is given by the following equation:

$$V_{output} = V_{ref}\left[1 + \frac{R_1}{R_2}\right] \tag{19}$$

The capacitive divider method is another common type of regulation method used for pump regulation. Atypical capacitive divider circuit is shown in the Figure 2-26.

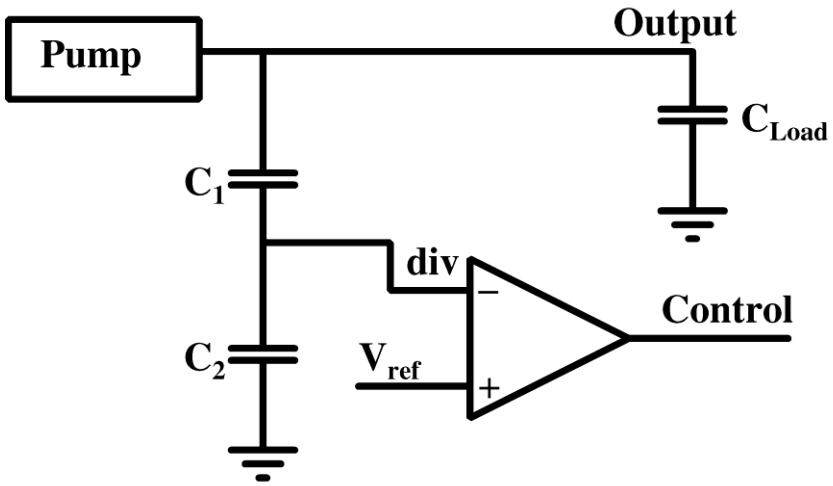

Figure 2-26. Capacitive divider feedback control [7]

The output of the circuit is given by the following equation;

$$V_{output} = V_{ref}\left[1 + \frac{C_2}{C_1}\right] \tag{20}$$

There are few disadvantages with using capacitive divider in the regulation system. First, capacitance may shift with the process variation or biasing voltage. Secondly, the capacitive divider is based on charge conservation on middle node in between two capacitors. So, any leakage current or subthreshold current would make conservation of the charge invalid and cause the regulation level on output to be off [7].

Low dropout regulator (LDO) is a simplest inexpensive way to regulate an output voltage that is powered from a higher voltage input. Figure 2-27 shows basic block diagram of a LDO circuit.

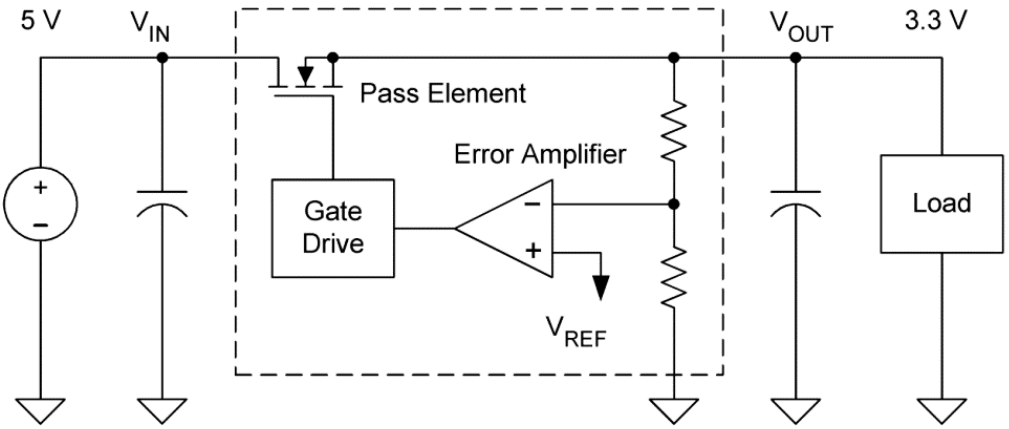

Figure 2-27. The basic block diagram of a LDO circuit [48]

The input voltage is applied to a pass element which can be MOSFET (NMOS or PMOS) or BJT (Bipolar junction Transistor) (NPN or PNP) type transistor. The output voltage is sensed by error amplifier and is compared with the reference voltage. The amplifier output drives the pass element's gate to the appropriate operating point to ensure that the output is at the correct voltage. The pass element operates in the linear region to reduce the input voltage to the

required output voltage value [48]. Each of the above circuits has to be evaluated for pump regulation as part of the system design.

2.7 Summary of the chapter

In this chapter, the required blocks for a typical fully integrated thermoelectric based energy harvesting interface electronics has been reviewed. The fundamentals of the charge pump circuit are explained. Detailed description of different charge pump architectures for low voltage application has also been introduced. The ultra-low voltage fully integrated charge pump based DC-DC converter systems in literature with and without integrated magnetic components have been presented. The theory and design of each block is explained with the help of state-of-the-art designs in the literature. Also important parameters of each block for low voltage and low power applications have been discussed.

CHAPTER 3
PROPOSED FULLY-INTEGRATED LOW VOLTAGE CHARGE PUMP CIRCUIT WITHOUT MAGNETIC COMPONENTS

3.1 Introduction

The previous chapter introduced fundamental theory associated with the charge pump circuits, design architectures of previous charge pump based DC-DC converters, and associated building blocks of the system. The designing of low voltage charge pump circuit to generate 1 V regulated voltage with 1 µW power is challenging due to low input voltage levels from the energy harvesters. Two basic challenges are efficient conversion of DC voltage into a stable DC power source to drive a realized load while keeping the required area (cost) at a minimum value.

Chapter 3 is organized as follows: The theory, design, and simulation results are presented for the blocks of a low voltage charge pump circuit without magnetic components, which is designed in 0.18 µm CMOS technology. Section 3.2 explains general overview of the proposed energy harvesting system by introducing each sub-block. Section 3.3 focuses on the design and simulation results of the first stage of the system, which includes the charge pump design, the subthreshold oscillator design. The section discusses the advantage of using the subthreshold oscillator over the ring oscillator traditionally used in previous systems. Section 3.4 describes the second stage of the system which includes the ring oscillator design, charge pump circuit design and hysteresis comparator design. The uses of hysteresis control and low-Vt transistors in the second stage are justified, as improvements in the system as compared to previously reported designs. Section 3.5 presents the voltage regulator circuit, which includes three sub-blocks as a sub-threshold voltage reference, a low power voltage divider, and a low power comparator. The circuit is designed to stabilize 1 V output voltage with 1 µW power for input voltages larger than 0.17 V. Finally, Section 3.6 includes the overall performance of the system as evaluated by simulations including minimum input startup voltage, output voltage under load, and efficiency. The chapter ends with a summary.

3.2 Energy Harvesting IC Overview

Figure 3-1 shows the overview of the proposed interface circuit (IC) for energy harvesting applications, designed in UMC 0.18µm CMOS technology which is the improved work of the previous design [21] reported by our team. All sub-blocks of the system is designed and implemented on a single chip, which offers a fully integrated system that is powered with a thermoelectric energy harvester.

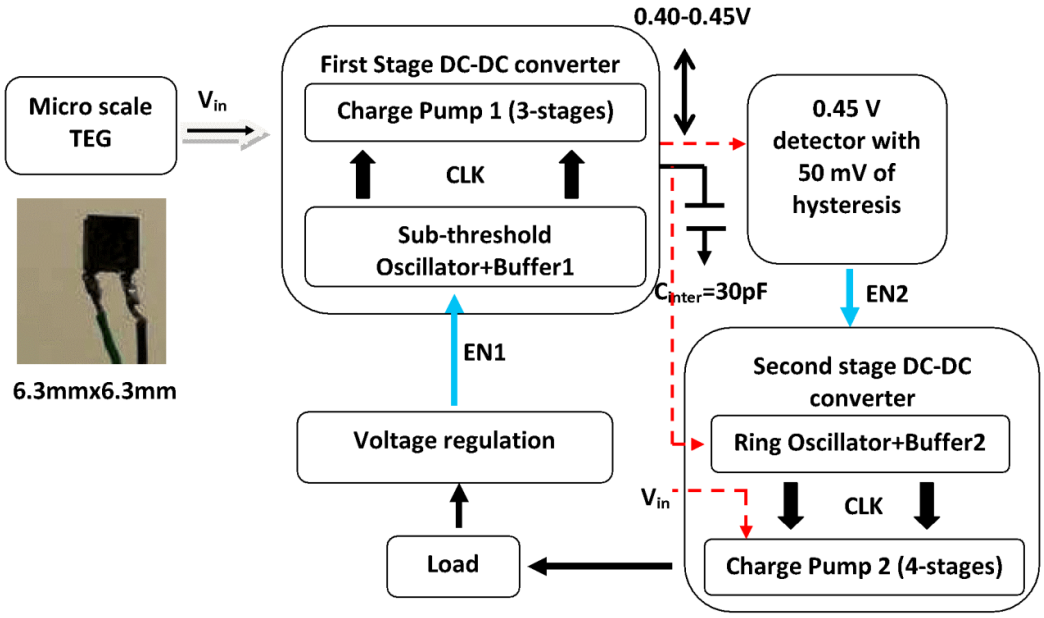

Figure 3-1. Block diagram of the proposed DC-DC converter

The first stage consists of a subthreshold oscillator with a buffered differential clock output that drives a three-stage charge pump circuit. The second stage contains a traditional ring oscillator as the clock generator to drive a four-stage charge pump. The hysteresis comparator is introduced between the two stages in order reduce the oscillatory on-off behavior at the second stage. The regulation is made up of a comparator, level shifter and a subthreshold NAND gate for selectively enabling the clock to the charge-pump.

The simulation waveforms are provided in Figure 3-2 to clarify the operation of the circuit. The comparator enables (EN1) the subthreshold oscillator when the output drops below 1 V. The subthreshold oscillator provides 2.5MHz, 50% duty cycle clock, CLK1 to the charge pump when the input voltage is 0.17 V. The charge pump at the first stage boosts the input

voltage up to 0.45 V. After reaching 0.45 V, the hysteresis comparator enables (EN2) the ring oscillator in the second stage. The enable signal holds until first stage output drops to 0.4 V. While this process repeats, 4-stage charge pump in the second stage steps up 0.45 V from the first stage to 1 V output.

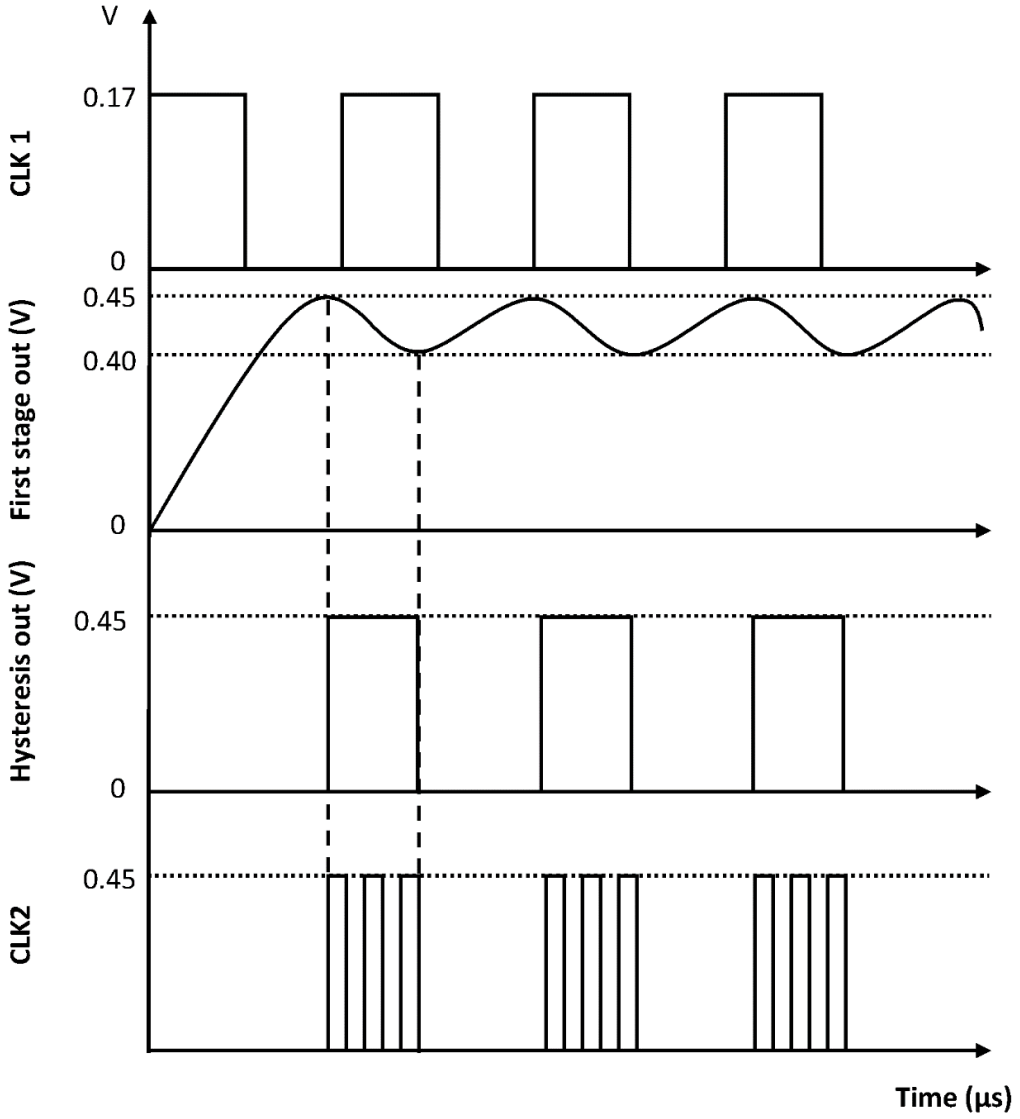

Figure 3-2. Waveforms to describe operation at V_{in}=0.17 V

The integrated (small) intermediate capacitor is used to store the charge from the first stage, and acts as a voltage source for the second stage. The hysteresis comparator is used to provide reasonable enable time for the second stage, and also helps to deliver a square wave clock (CLK2) with 2.2 MHz as shown in Figure 3-2. Without hysteresis, additional power

consumption would occur due to the frequent on-off switching in the second stage. The input of the two charge pumps are connected to the 0.17 V input voltage, so that the charge coming out from the first stage is used only for the ring oscillator, driver buffer, and the regulation circuit. This scheme improves the efficiency of the second stage. Although the choice of a larger intermediate capacitor would have improved the enabled time for the second stage, the tradeoff is increased initial circuit start-up time, and cost. The sub-circuits in each stage are explained in the following sections.

3.3 The First stage

3.3.1 Subthreshold source-coupled oscillator

Most of the fully integrated charge pump based DC-DC converters presented in the literature[15],[29],[38] used traditional ring oscillators as their clock generator. However, a typical ring oscillator has large variation over process, temperature and supply voltage deviations, and can change its frequency more than 30% over the typical operating condition [7]. The differential clock signal coming from the traditional ring oscillator has significant phase overlap between clocks due to the additional inverter. This overlap leads to the requirement of separate circuits to generate non-overlapping clocks. The power consumption of these additional circuits is significant when the circuit is working with ultra-low input voltages.

A five-stage subthreshold source-coupled logic (STSCL) based oscillator proposed in [39] has been utilized in this work with modifications, as the clock generating circuit, and is able to operate on low input voltages from energy harvester. Subthreshold source-coupled oscillator with replica bias circuit is depicted in Figure 3-3. The current going through M5 is controlled by the current mirror M6 and M7 as shown in Figure 3-3.

The active load resistances are implemented using PMOS devices (M1 and M2). The active output resistance converts the branch current back to differential voltage pair in order to drive the subsequent subthreshold source-coupled logic gates. To maintain a desired voltage swing at very low voltages and current values, it is necessary to have large resistance as;

$$R_L = \frac{V_{sw}}{I_{ss}} \tag{21}$$

where R_L is the PMOS resistance, V_{sw} is the voltage swing across the load, and I_{ss} is the tail bias current.

When the oscillator is working in the subthreshold region, the tail bias current is in the range of nA. According to Equation (21), the load resistance should be in the range of hundred MΩ in order to obtain the required output voltage swing. The regular PMOS load used in traditional source-couple based (SCL) inverter, with body connected to source and bias in the triode region, cannot be utilized, since the required channel length of the PMOS would be impractically large [49]. This leads to use of an alternate PMOS load proposed by [39], which provides higher resistance, and enables a higher output swing at very small bias current. The modified PMOS load, with drain connected to body, provides a high-resistance path to the applied V_{SD} (source-to-drain voltage) due to reversed-biased diode between n-well and the p-substrate, as shown in Figure 3-4.

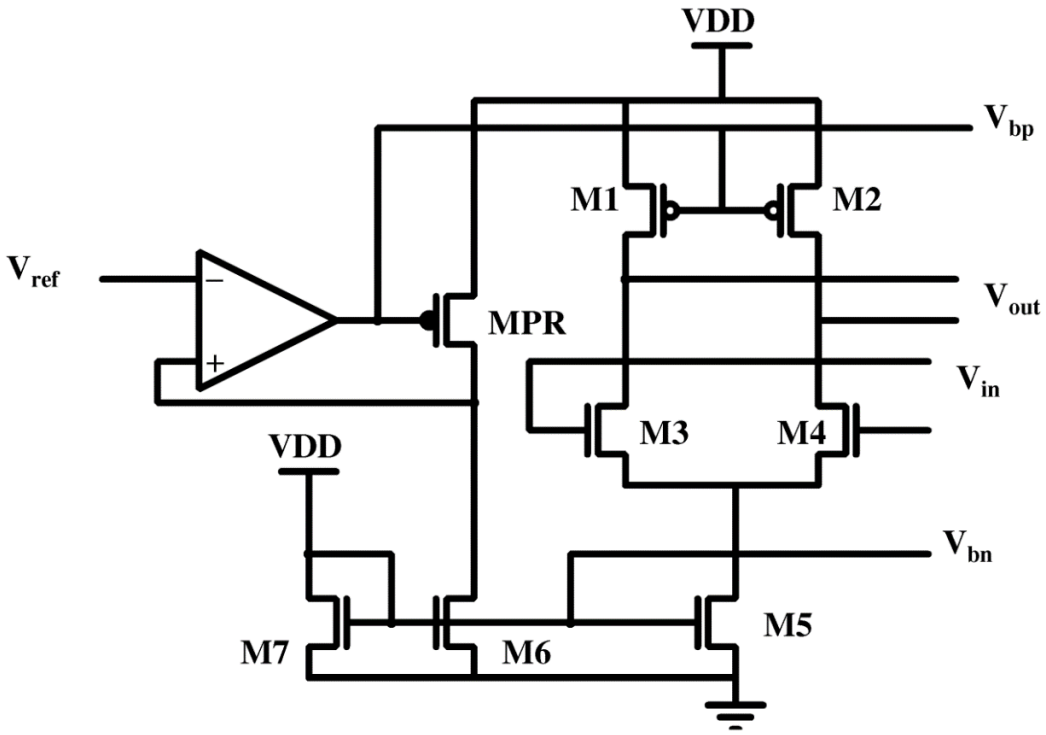

Figure 3-3. The subthreshold source-coupled oscillator [39]

The equation for the equivalent resistance can be obtained using EKV model [41], and is given by:

$$R_{SD} = \frac{nU_T}{I_{SD}} \times \frac{\exp\left(V_{SD}/U_T\right)-1}{\left(n-1\right)\exp\left(V_{SD}/U_T\right)+1} \tag{22}$$

where n is the subthreshold slope factor, U_T is the thermodynamics voltage, V_{SD} is the source to drain voltage of the PMOS and I_{SD} is the source to drain current of PMOS.

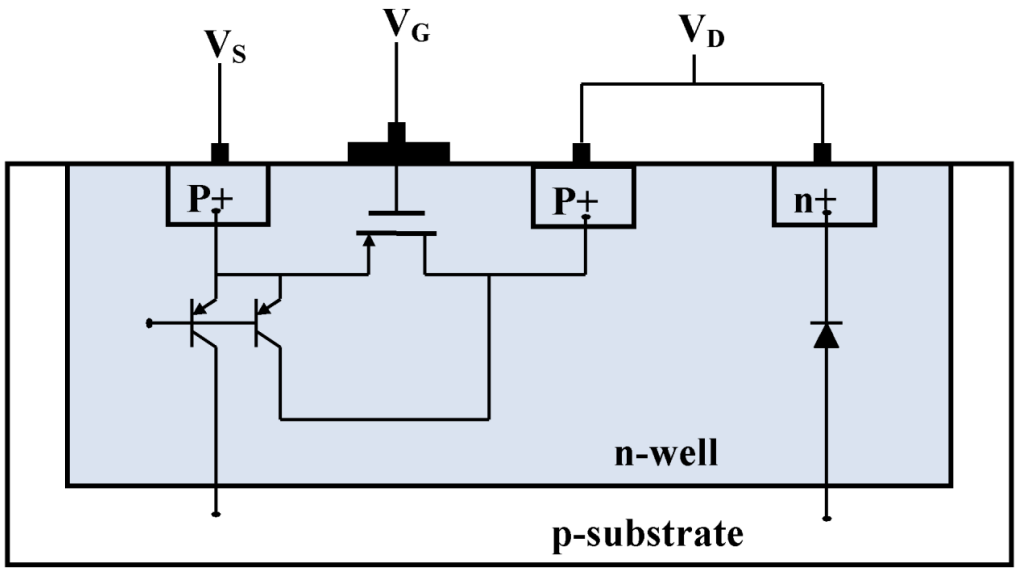

Figure 3-4. Cross-section view of the PMOS load device, showing the parasitic components that contribute to its operation in subthreshold region [39]

The generated frequency (f_{Max}) can be tuned by changing the bias voltage of the replica bias circuit, and is given by:

$$f_{Max} = I_{ss} / \ln 2.N.V_{SW}C_L \tag{23}$$

where N is the number of stages, and C_L is the load capacitance. Table 3.3 shows the design parameters of the subthreshold source-coupled oscillator with replica bias circuit.

In order to operate the STSCL gates properly, a simple single-stage differential amplifier with small gain and offset is sufficient, as provided in Figure 3-5.The current source, M5 in the figure, is driven by V_{DD}, when the amplifier is used in the replica bias circuit, and is connected

to V_{bn} (Figure 3-3) to serve the comparator function. The device sizes of the differential low-gain amplifier are depicted in Table 3-1.

A reference voltage of 0.14 V is required in order to maintain a steady minimum voltage swing at the STSCL gates. The modified 2T reference topology proposed by [51] is used for this purpose, and will be explained in detail in 3.5.1. Simulations have been carried out to quantify the advantage of subthreshold oscillator over ring the oscillator in the first stage of the system as shown in Figure 3-6.

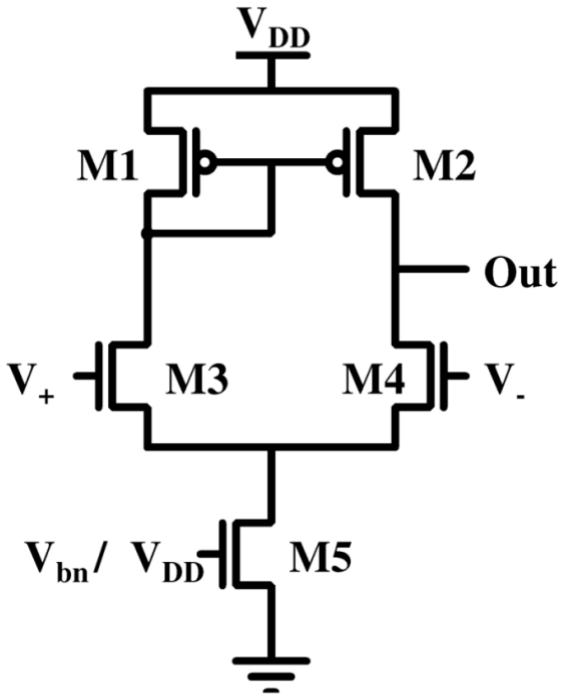

Figure 3-5. Simple differential low-gain amplifier [50]

Table 3-1. The device sizes of the differential low-gain amplifier

Name	W(µm)/L(µm)	Device type
M1,M2	0.5/0.18	Nom-Vt
M3,	1/0.18	Nom-Vt
M4	1.5/0.18	Nom-Vt
M5	0.24/2	Low-Vt

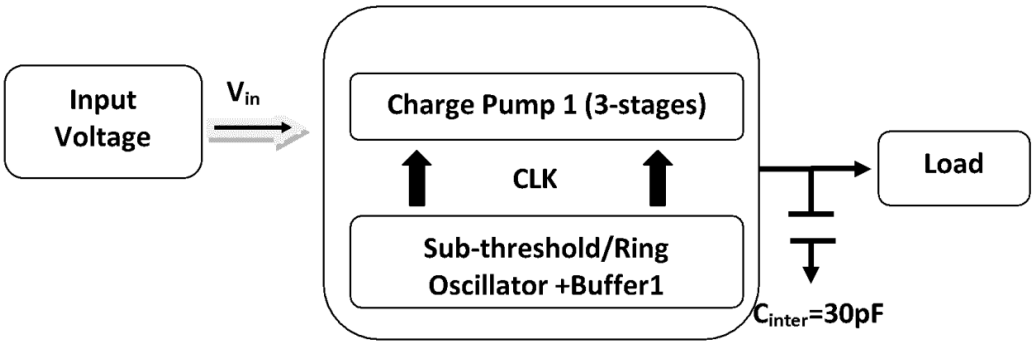

Figure 3-6. The first stage of the system

The simulated device sizes are depicted in Table 3-2.

Table 3-2. The design parameters of the transistors in Subthreshold oscillator and Ring oscillator

Component Name	Name	W(µm)/L(µm)	Device type
Subthreshold Oscillator	M1,M2	3/3	Low-Vt
	M3,M4	0.24/0.24	Low-Vt
	M5,M6,M7	0.24/2	Low-Vt
	MPR	0.7/0.24	Low-Vt
Ring oscillator	PMOS and NMOS size of the inverter	PMOS-0.48/0.24 NMOS-0.24/0.24	Low-Vt

The efficiency of the first stage with 5- stage subthreshold oscillator, 5-stage ring oscillator and 75-stage ring oscillator is shown in the Figure 3-7 for 0.17 V input voltage. Even though the frequency generated from the ring oscillator is higher (14.9 MHz) than that of the subthreshold oscillator (3.3 MHz), the ring oscillator based system suffers efficiency drop due to the inefficient charge transfer. The frequency of the stand-alone subthreshold oscillator is higher (3.3 MHz) than that of the subthreshold oscillator (2.5 MHz) in the full system with the same input voltage, due to the missing delay of the regulation block. In order to obtain a 3.3 MHz frequency from the ring oscillator, 75 stages are required. Hence the ring oscillator based design requires a larger area. The subthreshold design can overcome the drawbacks of the traditional ring oscillator, and is thus suitable for ultra-low voltage applications.

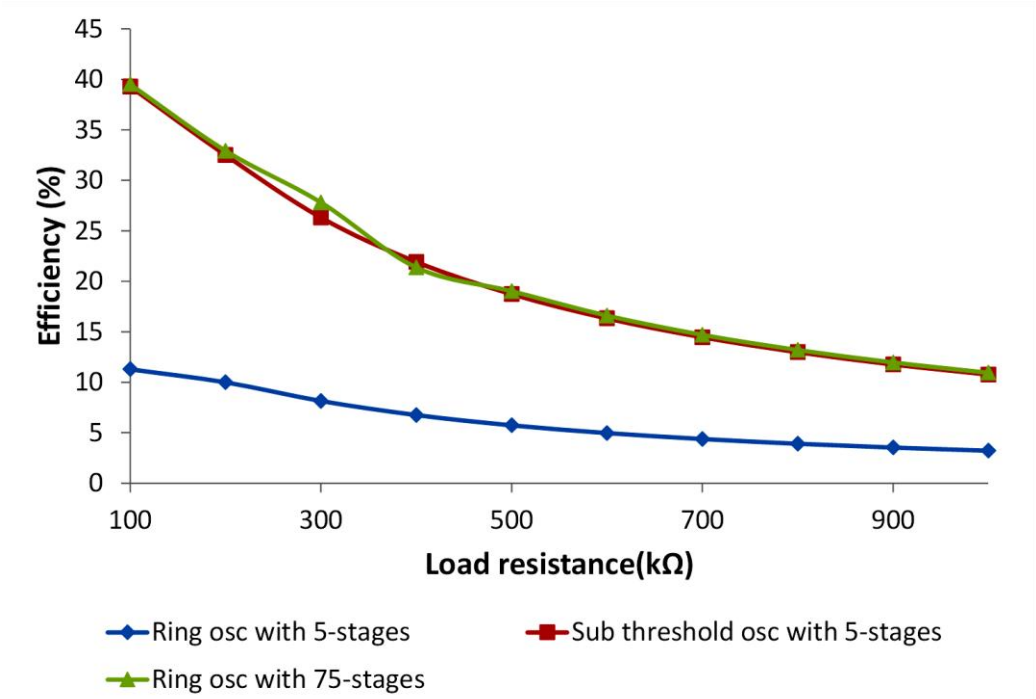

Figure 3-7. The simulated efficiency of the first stage of the system with subthreshold oscillator and 5 and 75 stages of Ring oscillator at V_{in}=0.17 V

3.3.2 Charge pump circuit

The circuit topology proposed by [24] has been adapted for the charge pump with modifications as shown in Figure 3-8.Low-Vt MOSFETs available in 0.18 µm have been utilized to accommodate the low voltage input requirement in this application.

The operation of the circuit can be explained as follows: When the clock signal CLKB is low and CLKA is high, the MN1 is turned on and charge is transferred to node 1. Then, the voltage at node 1 becomes V_{DD}. At the same time, MN2 is turned off and the voltage at node 2 becomes $2V_{DD}$. At this time transistor MP1 is turned on while MP2 is off. Hence, the voltage at output of first stage becomes $2V_{DD}$. When CLKB is high and CLKA is low, voltage at node 1 is $2V_{DD}$ and voltage at node 2 is V_{DD}. The transistor MN2 is on, and transfers the charge into node 2, while MN2 is turned off. At the same time, transistor MP2 is turned on while MP1 is off, and hence the ideal voltage at output of the first stage is $2V_{DD}$ for the entire duration of time. Similar analysis can be extended to the following stages. This is the main advantage of this circuit.

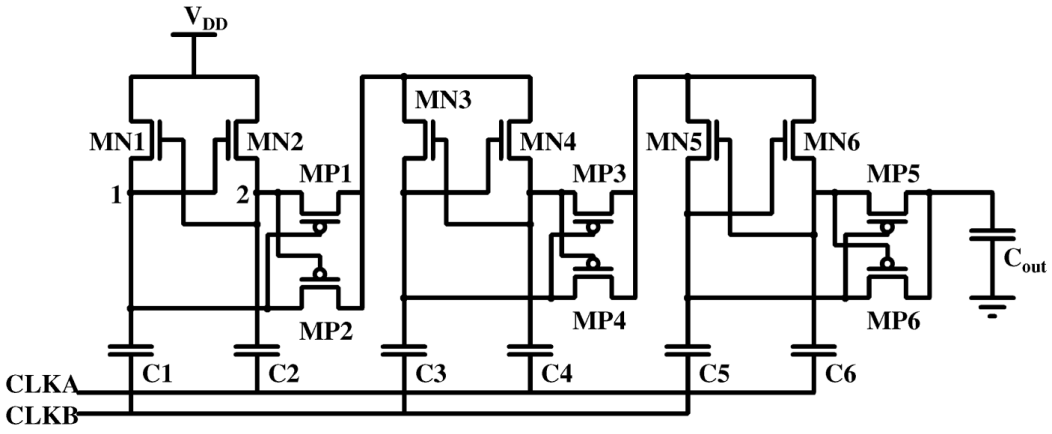

Figure 3-8. Charge pump circuit with cross connected NMOS cells [24]

3.4 The Second stage

3.4.1 Ring oscillator and the Charge pump circuit

The second stage consists of a 4-stage charge pump, and traditional ring oscillator along with the NAND gate to control the oscillator as shown in Figure 3-9.

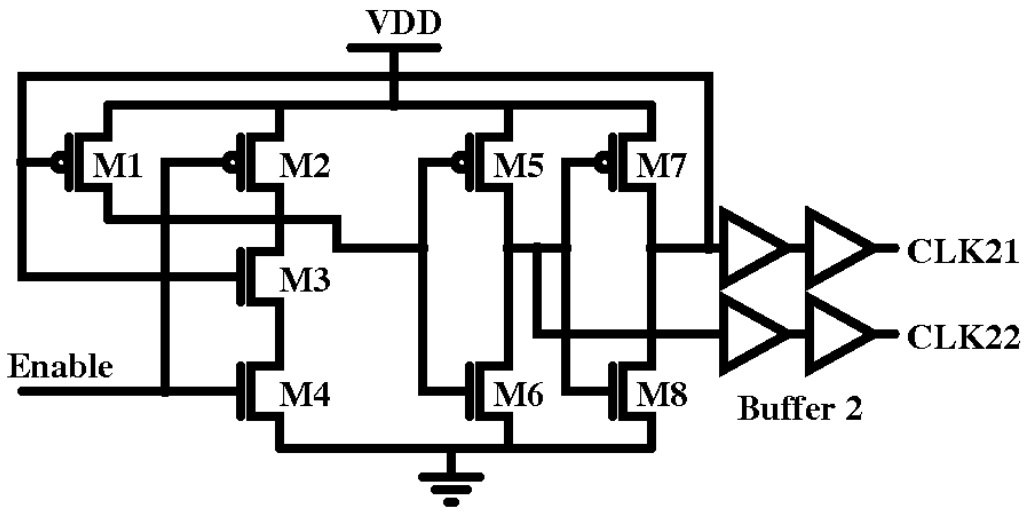

Figure 3-9. The controlled ring oscillator in the second stage

The second stage works on a clock with higher amplitude (0.4 V - 0.45 V) compared to the first stage. Figure 3-10 shows the efficiency of the full system when the second stage consists

of Low-Vt versus Nom-Vt MOSFETs with input voltage at 0.17 V. According to the result, usage of Low-Vt MOSFETs can boost the efficiency of the system up to 18% compare to that of Nom-Vt based charge pump, due to lower threshold operation.

Table 3-3. Size of the transistors of the charge pump and the buffer circuit

Name	Wp(µm)/Wn(µm)	Type of the transistor
Buffer1(4-stage)	16/8,48/24,144/72,432/216	Low-Vt
Charge pump1(3-stage)	160/80	Low-Vt
Buffer2(2-stage)	1/0.5,3/1.5	Low-Vt
Charge pump 1(4-stage)	0.48/0.24	Low-Vt
NAND Gate	1/1	Nom-Vt
Ring Oscillator	1/0.5	Nom-Vt

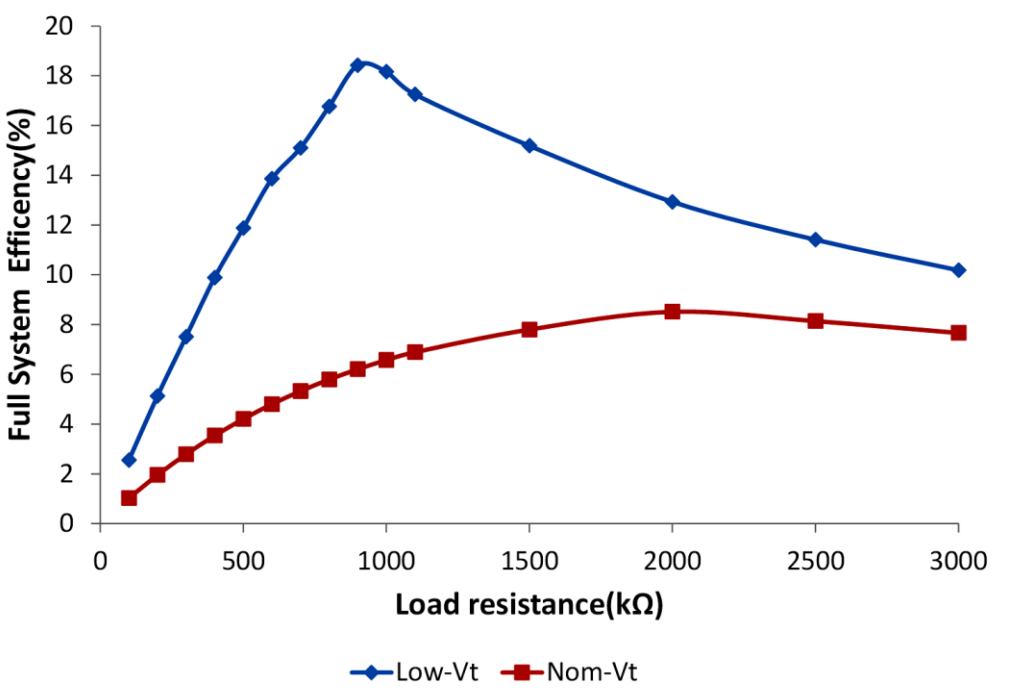

Figure 3-10. The simulated efficiency of the full system when the second stage charge pump consists with Low-Vt or Nom-Vt MOSFETs at V_{in}=0.17 V

The ring oscillator consists of Nom-Vt MOSFETs in order to reduce the leakage current. The architecture of the charge pump is the same as in Figure 3-8. Size of the transistors of the

charge pumps, buffer circuits and ring oscillator is depicted in Table 3-3 where all the lengths were set to minimum value.

3.4.2 The hysteresis comparator

The second stage is controlled by the hysteresis comparator in Figure 3-11. The control is outlined in Figure 3-2. The function of the hysteresis comparator can be explained as follows [52]:

$$V_{out}=1 \text{ when } V_p>V_n+V_{hyst+} \tag{24}$$

$$V_{out}=0 \text{ when } V_p<V_n-V_{hyst-} \tag{25}$$

where V_{hyst+} and V_{hyst-} are up and down hysteresis voltage values respectively. The hysteresis voltage is introduced by M5 and M6. When $V_p>V_n$, M6 and M9 are off, M7 and M5 are on, and I_{total} will flow through them. Up hysteresis voltage value can be determined by using the following conditions:

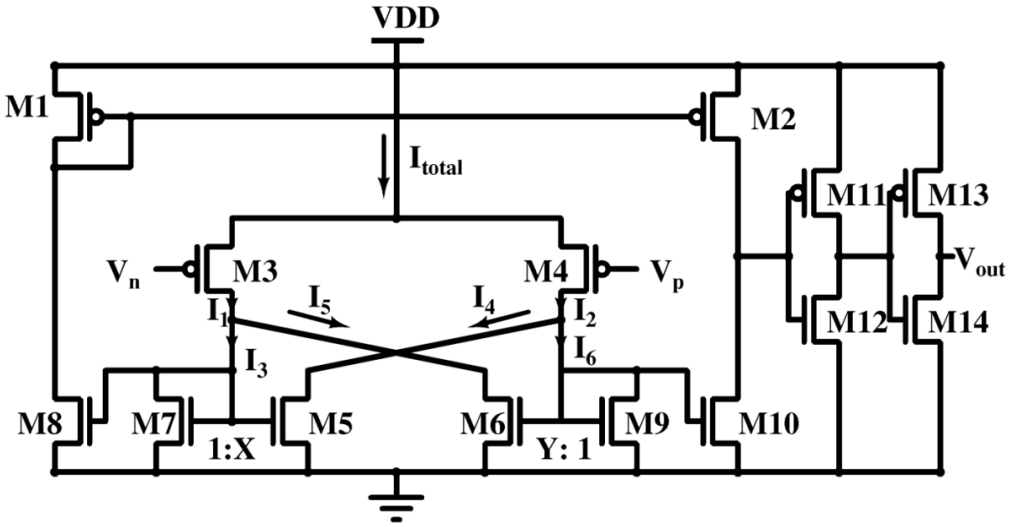

Figure 3-11. The hysteresis comparator [52]

$$I_{total}=I_1+I_2=I_3+I_4+I_5+I_6 \tag{26}$$

$$I_5=I_6=0, I_2=I_4=XI_3, I_3=I_1 \tag{27}$$

$$V_{hyst+} = \left|V_p - V_n\right| = \left|V_{gsM4} - V_{gsM3}\right| \tag{28}$$

$$V_{hyst+} = \sqrt{\frac{2I_{total}}{\mu C_{ox}(W/L)}} \times \frac{(\sqrt{X}-1)}{\sqrt{X+1}} \tag{29}$$

where X is the ratio between I_4 and I_3.Down hysteresis voltage can be derived in a similar manner.

Table 3-4. The design parameters of the hysteresis comparator

Name	W(µm)/L(µm)	Device type
M1,M2,M7,M8,M9,M10,M12,M14	0.24/0.18	Nom-Vt
M3,M4	0.24/0.24	Low-Vt
M5,M6,M11,M13	0.48/0.18	Low-Vt

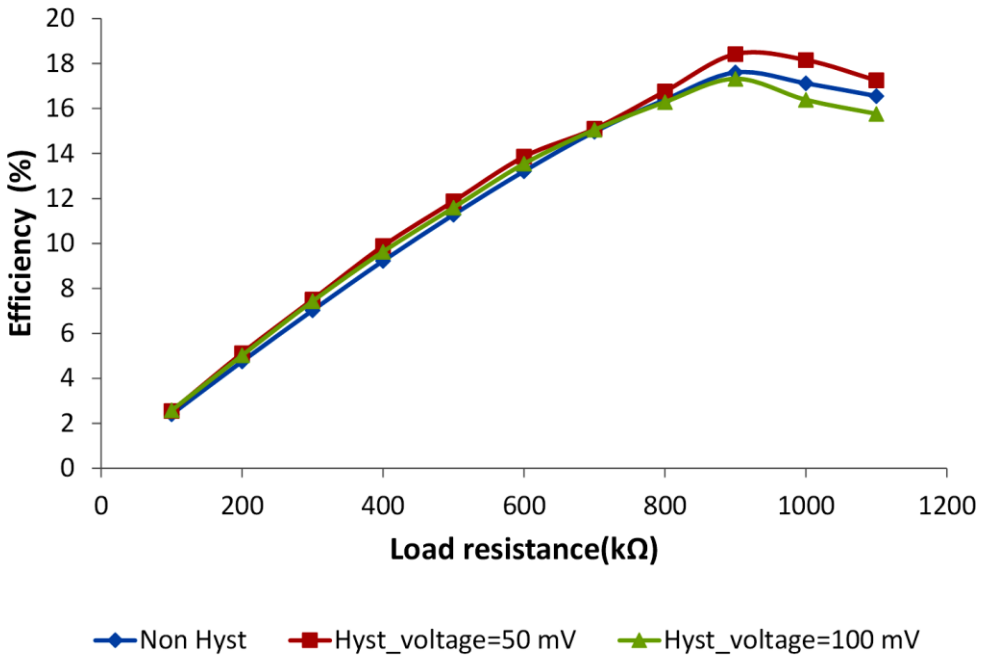

Figure 3-12. The simulated efficiency of the full system with different hysteresis voltages at V_{in}=0.17 V

Optimization analysis is shown in Figure 3-12 for the hysteresis band. According to the simulation result, the 50 mV hysteresis is suitable for the proposed DC-DC converter, and it has 3% and 2% higher efficiency compared to the system with 100 mV band and 0 mV (non-hysteretic) band respectively. The design parameters of the hysteresis comparator are shown in Table 3-4.

3.5 Voltage Regulation

The regulation is made up of the comparator, level shifter and the subthreshold NAND gate for enabling the clock to the charge-pump in a closed-loop system. The complete voltage regulation system is depicted in Figure 3-13. Diode-connected P-type MOSFETs are used as resisters in resistive divider network instead of highly resistive poly resistors in order to reduce the errors due to the process variation.

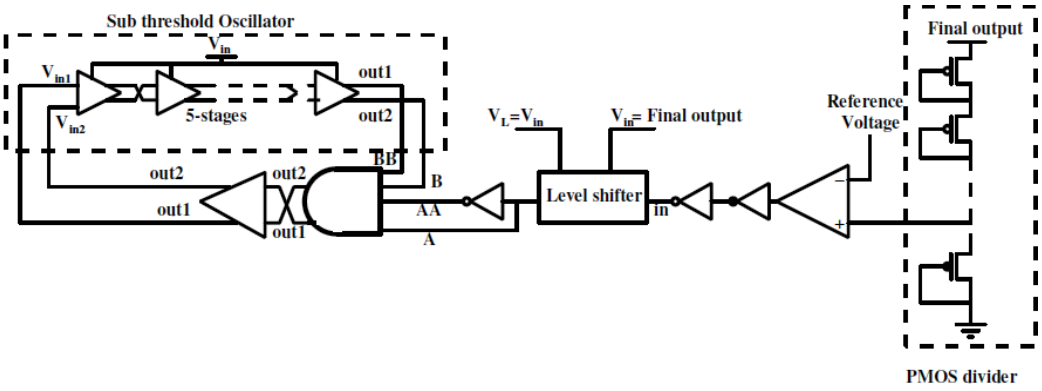

Figure 3-13. Voltage regulation in the proposed system

The output of the resistor divider circuit is given by the following equation;

$$V_{out} = V_{ref}\left[1 + R_1 / R_2\right] \tag{30}$$

Since the clock generation circuit in the 1st stage has differential input, the conventional NAND gate can't be used in the regulation system. The utilized AND gate is depicted in Figure 3-14. The V_{bn} and V_{bp} are generated from the replica bias circuit at subthreshold source-coupled oscillator. The differential two input AND gate and inverter are used to create the NAND function. Both are working in subthreshold region to minimize the power

consumption of the circuit. Therefore, the level shifter is needed to shift the voltage range and provides 0 V and 0.2 V when the output voltages of the pump are 0 V and 1 V respectively.

The operation of the proposed subthreshold AND gate can be explained as follows: Assuming inputs A and B are high when the inputs AA and BB are low, the current through M3 and M6 increases while the current through M5 and M7 decreases. Therefore, the voltage at Out2 increases while the voltage at Out1 decreases, and creates the AND function. The amplifier utilized in the replica bias circuit is reused here as a comparator to regulation system to regulate the final output to 1 V.

The level shifter used in this design is shown in Figure 3-15.The working principle of the level shifter circuit can be explained as follows: When the V_{in} is high, and then the M2 and M3 are switched on while the M1 and M4 are switched off. Then the output goes to V_L. When the V_{in} is low, M2 and M3 are switch off while the M1 and M4 are switched on. Then the output goes to zero [53].

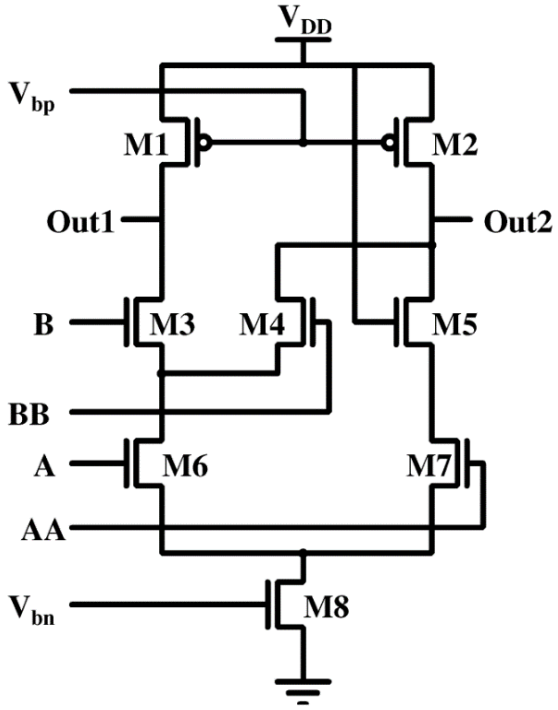

Figure 3-14. Subthreshold AND gate [39]

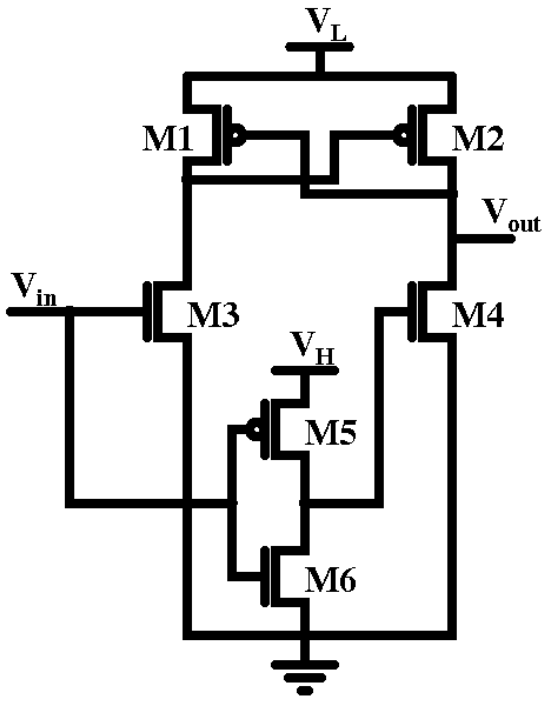

Figure 3-15. The level shifter circuit

The design parameters of the AND gate and level shifter circuits are shown in Table 3-5.

Table 3-5. The design parameters of the AND gate and level shifter circuits

Design Name	Name	W(µm)/L(µm)	Device type
AND gate	M1,M2	3/3	Low-Vt
	M3,M4,M5,M6,M7	0.24/0.24	Low-Vt
	M8	1/0.24	Low-Vt
Level shifter	M1	0.48/0.24	Nom-Vt
	M2	0.48/0.24	Low-Vt
	M3	0.24/0.24	Nom-Vt
	M4	3/0.24	Low-Vt
	M5	0.48/0.18	Nom-Vt
	M6	0.24/0.18	Nom-Vt

3.5.1 Reference voltage generators

Two different reference voltages are required for the proposed system: A reference voltage of 0.14 V (Ref1) is required at the replica bias circuit in order to maintain the constant gate voltage of the PMOS load devices. In addition, a reference voltage of 0.29 V (Ref2) is required for the comparator in order to maintain the accurate regulation in both stages. The 2T reference circuit proposed by [51] is used to generate both reference voltages with modifications, as depicted in Figure 3-16.

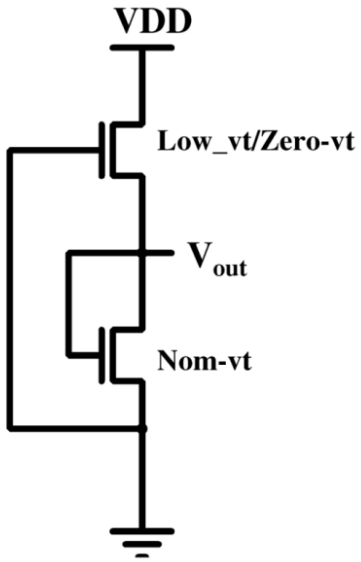

Figure 3-16. The 2T reference circuit [51]

The two required reference voltages can be generated by using device options with different threshold at the top portion of this circuit. The sizes of the transistors in two reference circuits (Ref1 and Ref2) are depicted in Table 3-6.

Table 3-6. Size of the transistors of the two reference circuits

Name	W(µm)/L(µm)	Type
Ref1	0.7/15	Low-Vt
	2/20	Nom-Vt
Ref2	0.7/15	Zero-Vt
	2/20	Nom-Vt

The output voltage V_{ref} can be modeled by Equation (31), the subthreshold current equation [51]. Both devices are working in the weak inversion region.

$$I_{DS} = (n-1)\mu C_{ox} \frac{W}{L} U_T^2 \exp\left(\frac{V_{gs} - V_t}{nU_T}\right)\left(1 - \exp\left(\frac{-V_{ds}}{U_T}\right)\right) \tag{31}$$

where, n is the subthreshold slope factor, μ is the effective carrier mobility, C_{ox} is the gate oxide capacitance, U_T is the thermodynamic voltage, V_t is threshold voltage of the MOSFET, and V_{gs} and V_{ds} are gate to source and drain to source voltages of the MOSFET. Setting the current through M1 and M2 equal, V_{ref} can be obtained as,

$$V_{ref} = \frac{n_1 n_2}{n_1 + n_2}\left(V_{t2} - V_{t1}\right) + \frac{n_1 n_2}{n_1 + n_2} U_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_1}{\mu_2 C_{ox2} W_2 L_1}\right) \tag{32}$$

MOSFETs that make up the 2T voltage reference were sized to have non-minimum L in order to generate voltage and temperature compensated reference voltage while maintaining low power consumption in nW range.

In UMC process the corner options are named: “nom”, which means typical conditions, “ss” which means slow conditions for both NMOS and PMOS devices, “ff” which means fast conditions for both NMOS and PMOS transistors, “fnsp” means fast N type MOSFET and slow P type MOSFET and “snfp” means slow N type MOSFET and fast P type MOSFET. Process corner analysis is carried out for both reference voltage generators at different voltage levels in order to assess the impact of process variation during high volume manufacturing. The process corner analysis and the temperature variation of the reference voltage generator at the subthreshold oscillator (Ref1) are shown in Figure 3-17 and Figure 3-18 respectively. The reference voltage (Ref1) variation during the process variation is in the range of ±17 mV. As the temperature is swept from 0°C to 100°C, the change at the reference voltage (ref1) is in the range of ±4 mV. The process corner analysis and the temperature variation of the reference voltage generator at regulation block (Ref2) are shown in Figure 3-19 and Figure 3-20.The reference voltage (Ref2) variation with process is in the range of ±16 mV. As the temperature has been swept from 0°C to 100°C the change at the reference voltage (Ref2) is in the range of ±4 mV. Therefore, both reference generators can generate voltage and temperature compensated steady reference voltage.

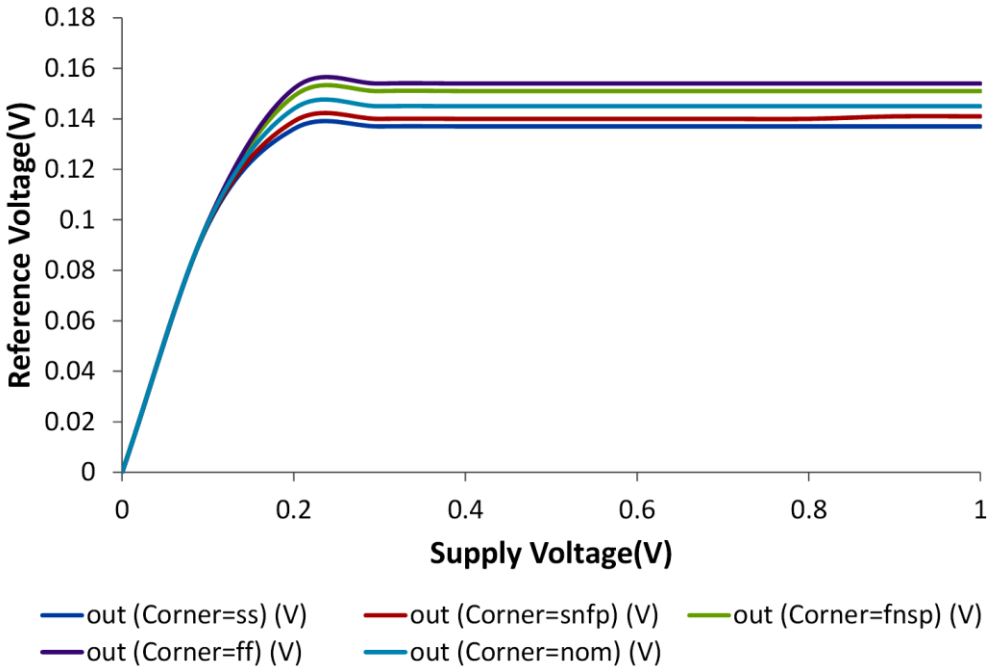

Figure 3-17. Change of the reference voltage (Ref1) with the supply voltage

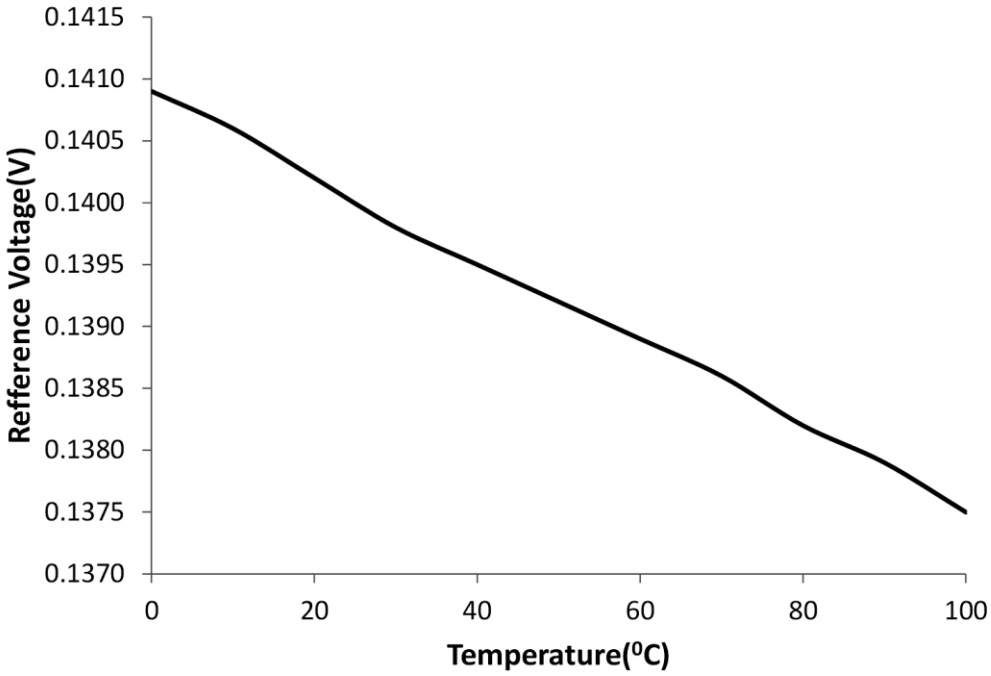

Figure 3-18. Change of the reference voltage (Ref1) with the temperature

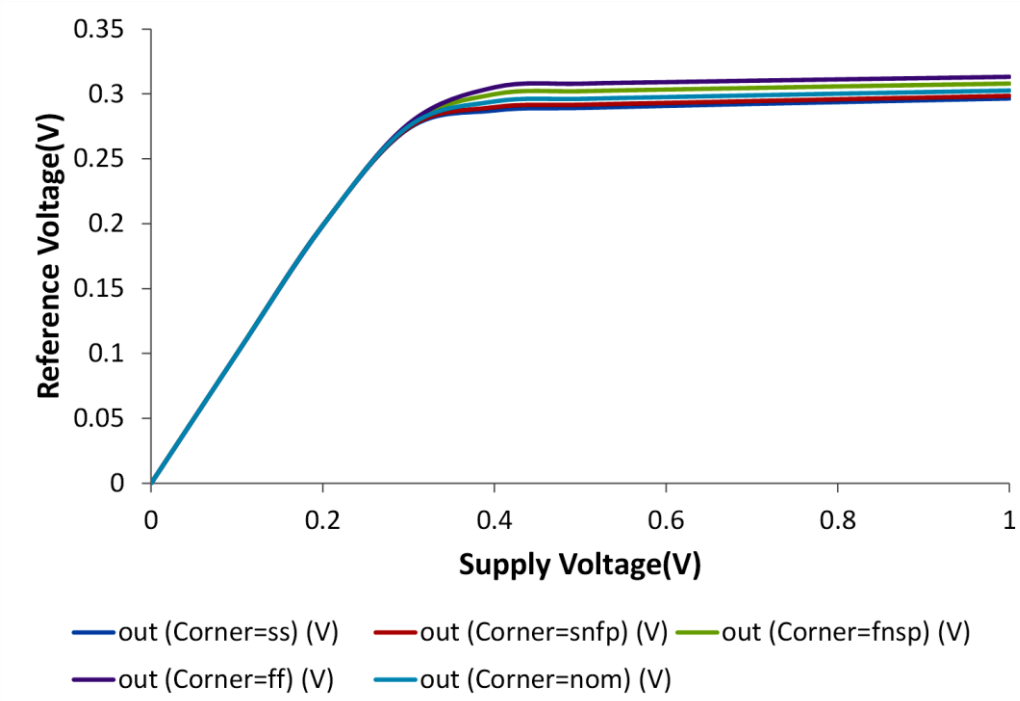

Figure 3-19. Reference voltage (Ref2) change with supply voltage

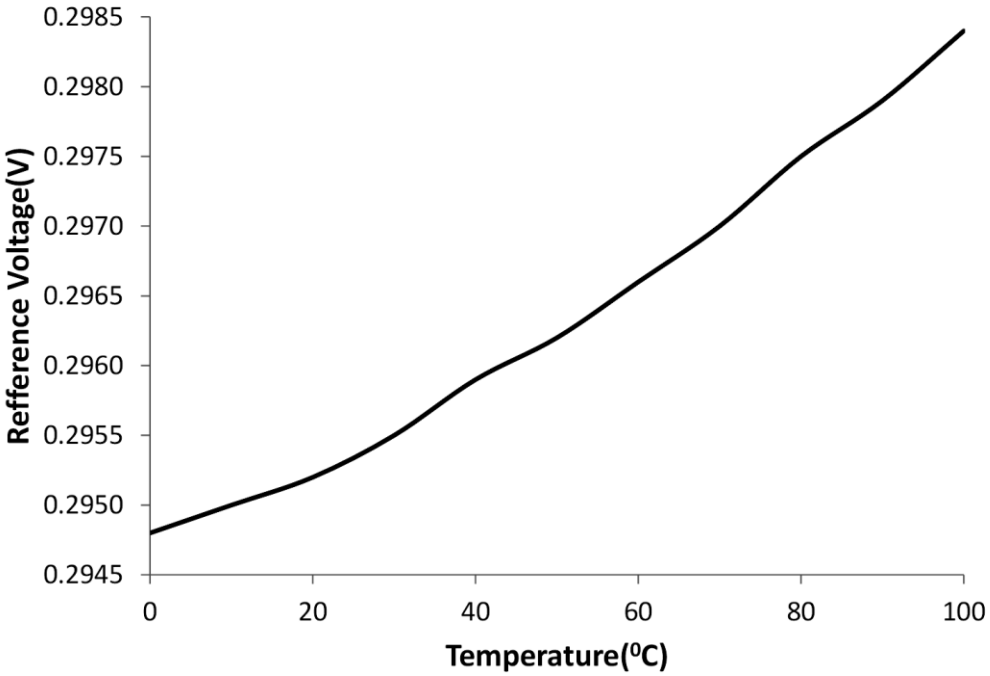

Figure 3-20. Reference voltage (Ref2) change with temperature

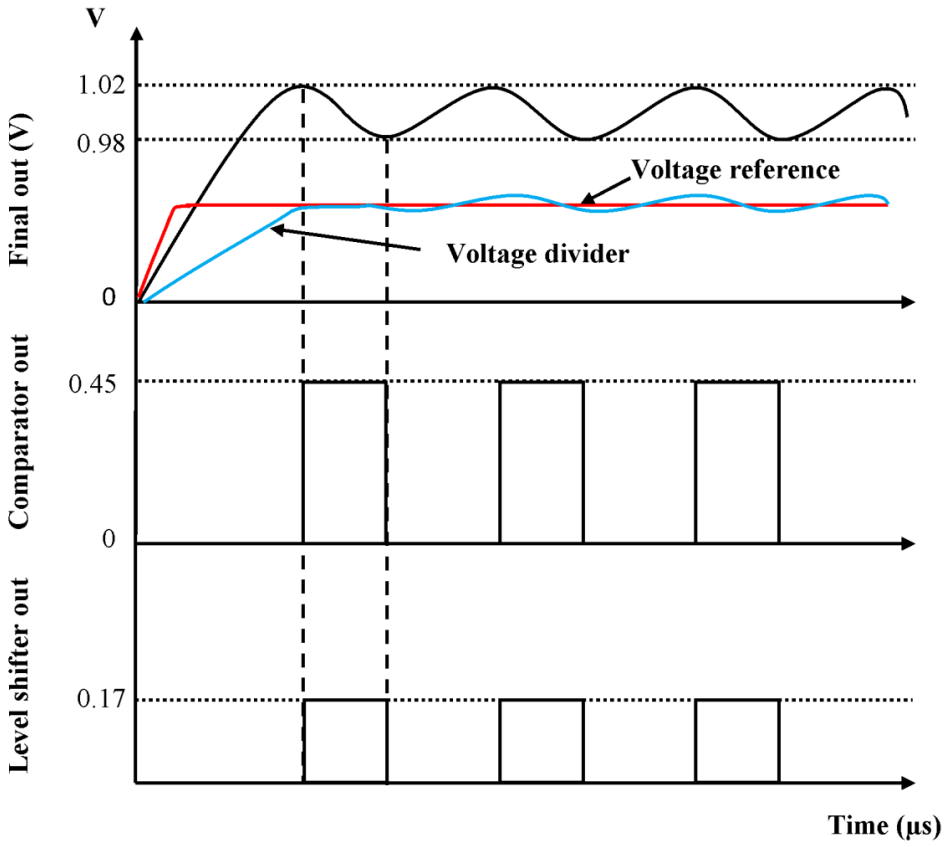

Figure 3-21. The simulation result of the regulator block at V_{in}=0.17 V

Figure 3-21 presents the simulation result of the regulator block, which demonstrates the operation principle. As explained earlier, the voltage reference and voltage divider outputs are compared with the comparator. At low supply voltages the reference voltage is higher than that of the divided output voltage. Hence the comparator gives low voltage which means the oscillator is working with full power. When the supply voltage reaches the desired value (1 V for this work), the divider output starts to exceed the reference voltage. Hence, the comparator output provides a high signal to the level shifter, which then shifts the voltage level to the supply value of 0.17 V in this case, and fed into the subthreshold oscillator through the subthreshold NAND gate in order to stop the oscillation. The final output voltage ripple is acceptable since it is within ±2% voltage range.

3.6 Full system simulation

The proposed interface design in 0.18 μm CMOS UMC technology has been verified using Cadence simulations.

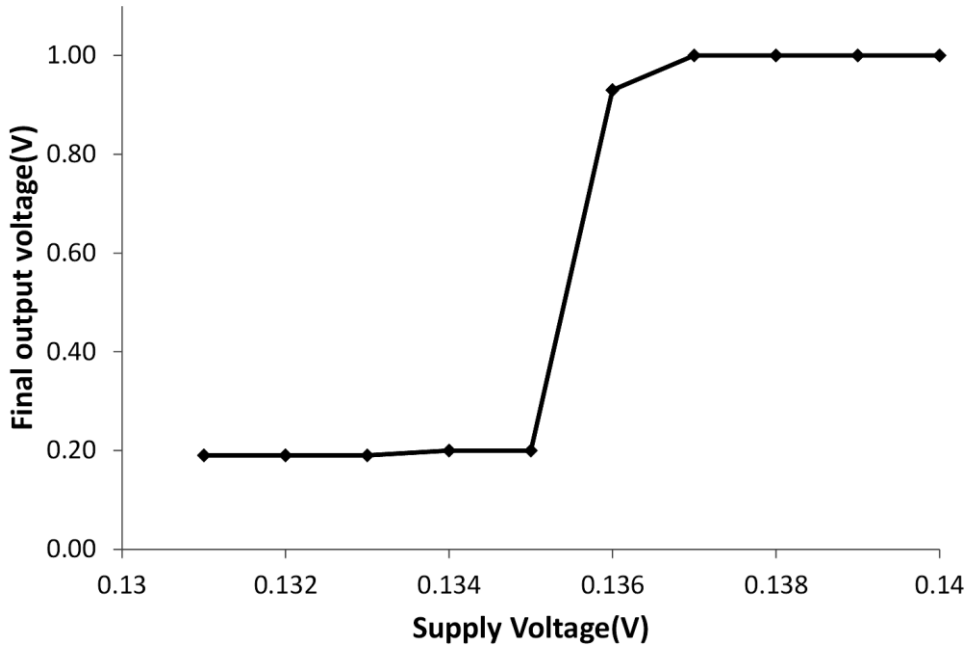

Figure 3-22. Simulated output voltage of the proposed system for different supply voltages

The startup condition of the circuit is verified by measuring the output voltage loading with its own power management circuit for different input voltages as shown in Figure 3-22.According the results the proposed system is able to start with 0.136 V input voltage, and generates 0.93 V without any external load resistance.

The system can only generate 1 V with 1 μW power at 0.17 V and therefore the characterization of the proposed system is carried out for the input voltages of 0.17 V or higher. The efficiency of the proposed circuit has been analyzed using the load resistance range of 200 kΩ - 1500 kΩ with different input voltages. The efficiency with different load and input voltage values is depicted in Figure 3-23.The corresponding output of the proposed circuit is shown in Figure 3-24.

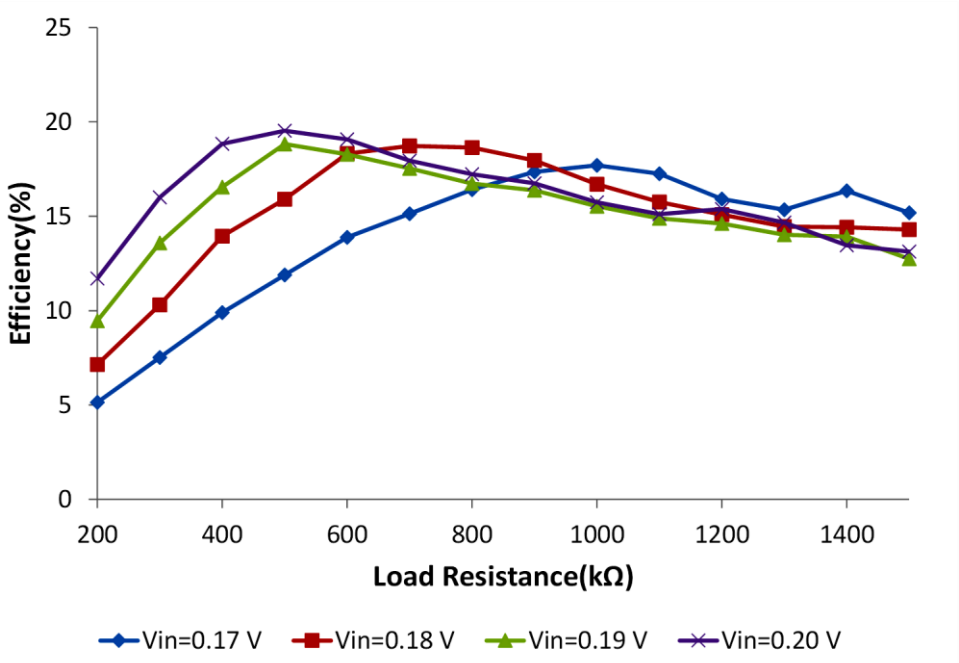

Figure 3-23. Efficiency of the proposed circuit versus varying load, and different input voltage values

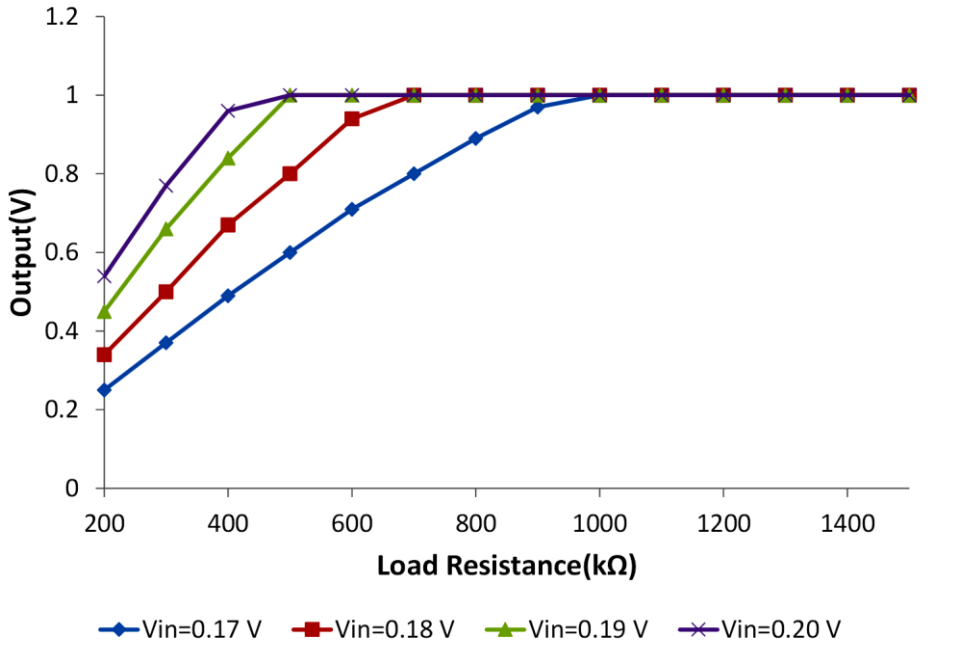

Figure 3-24. Final output voltage of the proposed circuit versus varying load, and different input voltage values

According to Figure 3-23 and Figure 3-24, the proposed system can achieve 20% efficiency with input voltage of 0.2 V. It also generates required 1 V output over a wide range of load resistances. However, the circuit can also be started up with an input voltage as low as 0.17 V based on the simulations, and generates 1 V with 18% of maximum efficiency in this condition. The proposed system can generate more than 35% power compared to the previous work [21] due to improvements. The peak efficiency has been increased from 12% to 18%, while start up voltage is reduced to 0.17V [22].

3.7 Summary of the chapter

Table 3-7 shows a summary circuit performance comparison to literature with circuits which do not contain any magnetic components.

Table 3-7. Performance comparison of this work against literature

	[15]	[21]	[27]	[29]	[31]	This work
Process (nm)	130	90	180	130	130	180
Input (mV)	400	200	120	135	180	170
Output (V)	1.4 V Regulated at 400 mV	2.3 V Regulated at 200 mV	0.28 V unregulated at 120 mV	0.65 V** unregulated at 135 mV	0.62 V Unregulated at 180 mV	1 V regulated
External Components	No	No	No	No	Pump capacitors	No
Startup	Self	Self	Self	Self	Self	Self
Area (mm^2)	0.42	-	0.69	0.168	0.06	0.32
Efficiency	58% at 400 mV	12% at 200 mV	23% at 120 mV	N/A	34% at 180 mV	18% at 170 mV

(**The generated output voltage without any external load)

In this chapter, the theory, design and simulation results of the proposed fully integrated low voltage charge pump based DC-DC converter for energy harvesting applications has been presented. The demonstrated architecture includes a complete system for energy harvesting applications, and has been designed in UMC 0.18 µm CMOS technology. The operation

principles and performance of each of the sub-blocks are demonstrated with simulations. The proposed system can generate steady 1 µW power output for the input voltage as low as 0.17 V with 18% efficiency. The circuit avoids off-chip and large on-chip magnetic components, non-standard processes, and is thus suitable for ultra-low voltage low profile system-on-chip applications.

CHAPTER 4

TEST CHIP LAYOUT, EXPERIMENTAL RESULTS AND DESIGN VALIDATION

This chapter presents the planning and layout of the test chip utilized to validate the system design from Chapter 3, experimental measurements the test structures, and comparative analysis between experimental and simulation results. The simulation-measurement correlation has been presented in detail. The fabricated IC has also been tested under realistic application conditions using an off-the-shelf thermoelectric module, which is also discussed in this chapter. Finally, possible solutions are suggested for the miscorrelations between validation and simulation results.

Section 4.1 describes testability design in the IC, including the full layout of the system. Section 4.2 explains the PCB design and the current measurement method of the Test IC. Section 4.3 presents the efficiency analysis of the system during the validation. Section 4.4 depicts the experiment setup of the test IC including the voltage generation setup. The measurement results of the Test IC are presented in the section 4.5.Finally Section 4.6 contains a detailed analysis of correlation between simulation validation results. The chapter ends with a summary.

4.1 Testability circuit

Testability circuits are required on the test chip in addition to the full system integration in order to characterize the performance of each sub block. For this purpose, 13 different circuits including the main system were implemented, along with 42 pads to be used as test interface.

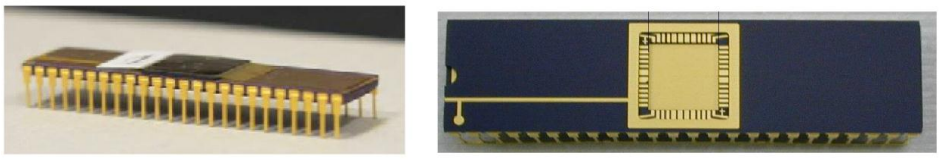

Figure 4-1. (A) Fabricated IC, (B) top view of an DIL48 package with pads [54]

The test chip was packaged in DIL 48 as shown in Figure 4-1, in order to enable simple test interface, and use of breadboards if the test PCB (Printed Circuit Board) had problems.

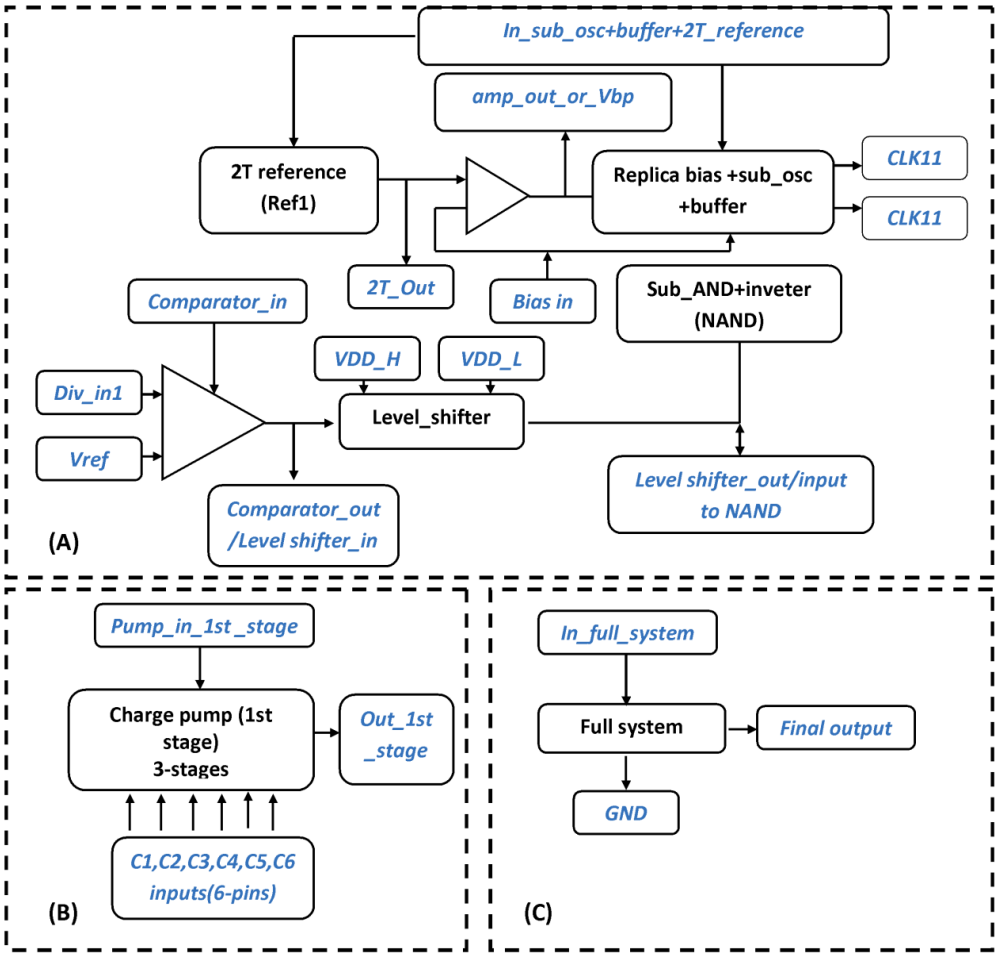

Figure 4-2. Testability circuit block diagram for (A) first stage including voltage regulation circuit, (B) first stage charge pump, (C) complete system

The testability circuits used for the first stage and the full system are shown in Figure 4-2. The pin names are shown in italic bold blue color letters for clarity. All the sub-circuit blocks are shown in bold black letters. The testability circuit used for the second stage including the separate subthreshold oscillator circuit block is shown in Figure 4-3. The testability I/O signal abbreviations and the corresponding pin numbers on the Test IC is listed in Table A-1 of APPENDIX A.

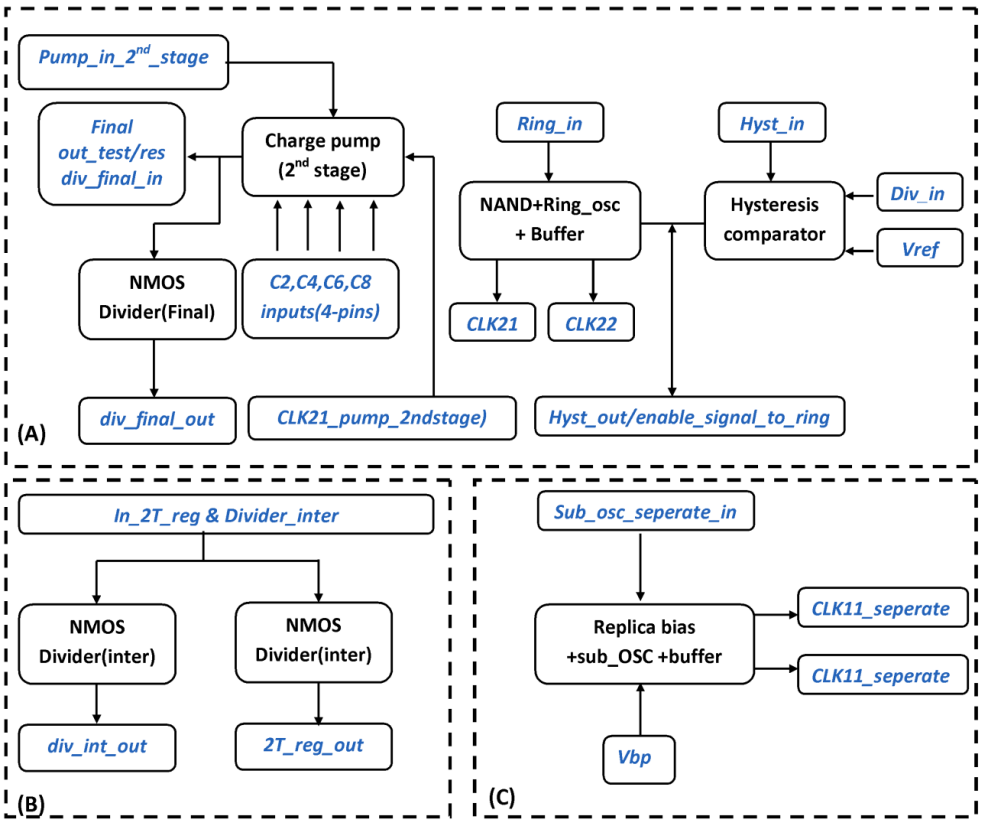

Figure 4-3. Testability circuit block diagram for (A) second stage, (B) final stage reference generator and resistive divider, (C) separate subthreshold circuit block

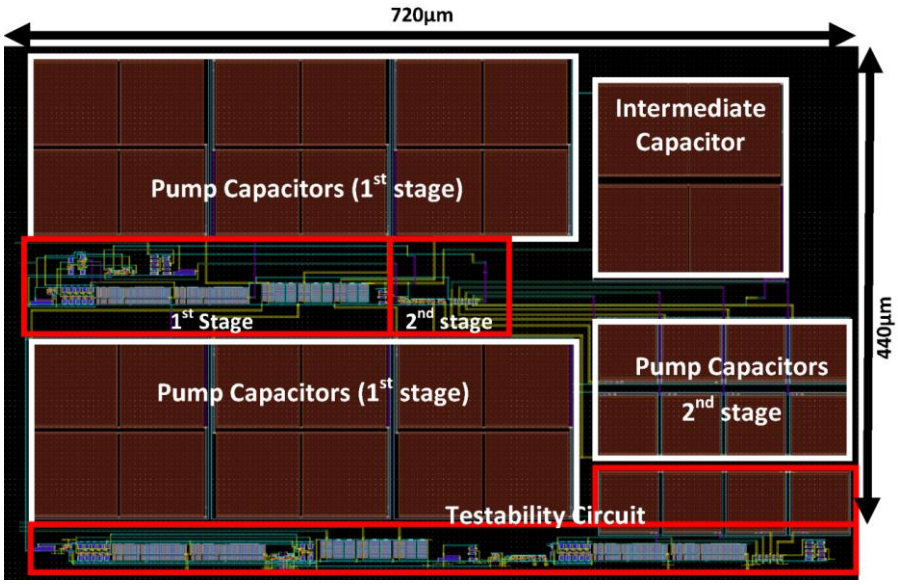

Figure 4-4. Layout of the proposed system

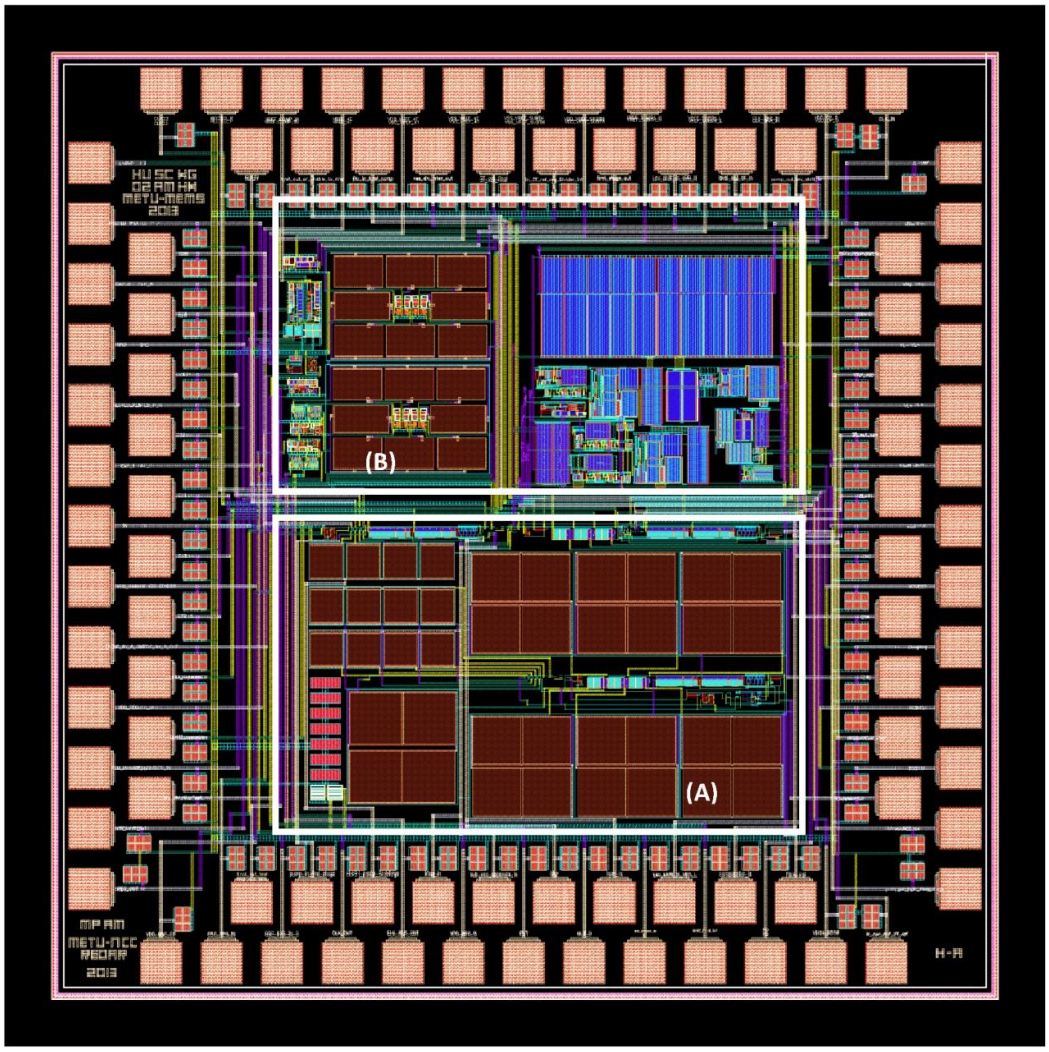

Figure 4-5. Overall die photo with PAD connection: (A) The proposed system (B) other circuits unrelated to this thesis.

Figure 4-4 depicts the full system layout including testability circuits for detailed characterization of the system, and the sub-blocks. The area occupied by the circuit is 740 µm x 440 µm. Figure 4-5 shows the overall die photo with the PAD connections. The die consists of proposed thermoelectric harvester interface electronic circuit with redundant sub circuits for testability (bottom half), and other circuits unrelated to this thesis (top half).

4.2 PCB design and the current measurement method

4.2.1 PCB design

The usage of a PCB for testing the test chip helps to minimize the effects of parasitic contact and wiring resistances. A test PCB was designed to get more precise results from the chip. Figure 4.7 presents the PCB designed using EAGLE Layout Editor 6.4.0 [55], which was then fabricated using an external vendor. The test PCB includes pin headers so that external components, such as load resistors and capacitors, can be mounted and swapped.

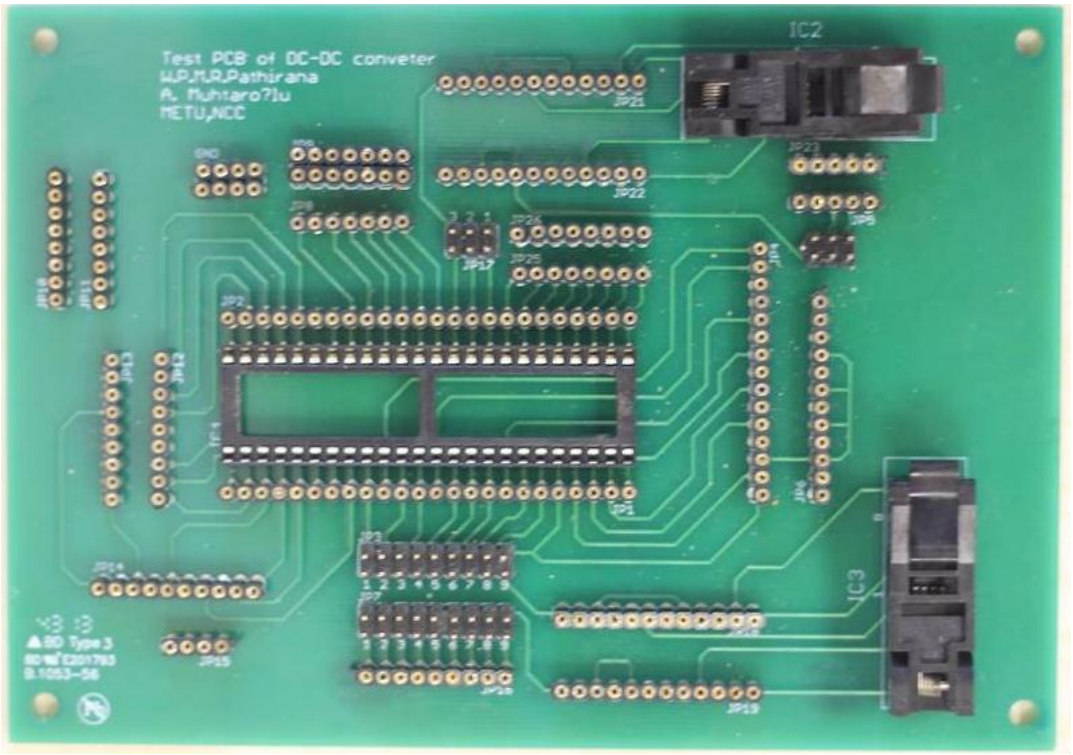

Figure 4-6. Designed test PCB for the UMC 0.18 µm chip

4.2.2 The current measurement technique

The expected current consumption by each sub-block is shown in Table 4-1.According to the Table 4-1 the current measurement will range from pA to µA. Moreover, there will be noise on the current measurement because of the frequent on-off behavior during regulation. Since traditional ammeters cannot be used to measure the pA to nA range current, LTC2050IS8PBF

sense amplifier [56] is used for the accurate power characterization of the system by measuring small voltage drop across current-sense resistors on power lines.

Table 4-1. Expected current consumption of the each sub-block

Pin name	Average expected current(µA)
sub_osc_seperate_in	30
pump_in_2nd_stage	3.2
Ring_in	3.3
hyst_in	0.18
VDD_L	$31x10^{-6}$
comparator_in	0.0044
in_osc_buf_2T_ref	30
pump_in_first_stage	6
in_full_system	40
VDD_H	0.002
first_stage_out	6
in_2T_ref_reg_Divider_int	0.02

The schematic diagram used for the current sensing is shown in Figure 4-7.

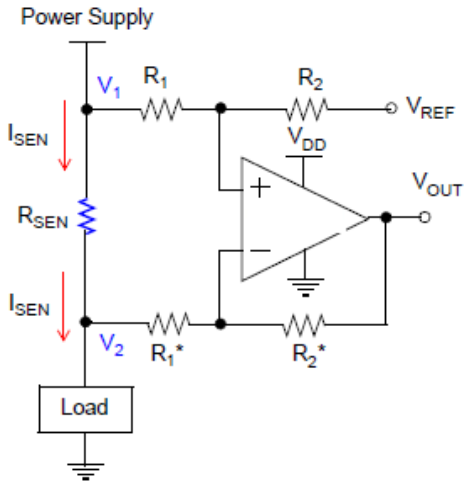

Figure 4-7. The op-amp configuration for high-side current sensing [57]

Assuming that current flow in upper branch (through R_1) and lower branches (through R_1*) are I_1 and I_2 respectively, the equation for I_1 and I_2 can be written as follows *(R_1=R_1*, R_2=R_2*)*:

$$I_1 = \frac{V_1 - V_x}{R_1} = \frac{V_x - V_{ref}}{R_2} \tag{33}$$

$$I_2 = \frac{V_2 - V_x}{R_1} = \frac{V_x - V_{out}}{R_2} \tag{34}$$

where V_x is the voltage at positive and negative terminal of the amplifier assuming that the amplifier has high input impedance.

From (33) and (34)

$$V_{out} = (V_2 - V_1)\frac{R_2}{R_1} + V_{ref} \tag{35}$$

The offset voltage should be calibrated before an accurate measurement can be completed. This is done by setting V_1 and V_2 nodes to ground or V_{DD}. It was measured around 165 mV for 1024 MΩ/1 MΩ gain ratio. The top view of the LTC2050IS8PBF is shown in Figure 4-8.

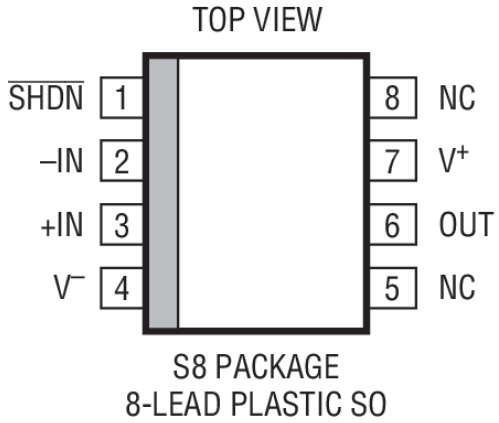

Figure 4-8. Top view of the LTC2050IS8PBF [56]

The resistor values used for current sensing, and the corresponding pin numbers are depicted in Table 4-2.

Table 4-2. Resistor values used for current sensing, and the corresponding pin numbers

Pin number at the IC	Description
7	Positive supply of the op-amp (+5V)
4	Negative supply of the op-amp (GND)
3	Positive input (R6) (1027 MΩ)
3	Positive input (R5) (1 MΩ)
6	output
2	Negative input (R3) (1027 MΩ)
2	Negative input (R4) (1 MΩ)
	Sense resistors (10.2 Ω)

Using Equation (35) and Table 4-2, the input current can be calculated by through:

$$I_{in}(\mu A) = \frac{\left(V_{out}(mV) - V_{off}(mV)\right)}{10.2 \times 1027} \times 1000 \tag{36}$$

where I_{in} is the input current in the circuit, V_{out} is the output of the amplifier, and V_{off} is the offset voltage value of the amplifier. Digit Precision Multimeter (8846A, 6.5) was also used to verify the subset of the measurements taken from the current sense amplifier in the µA current range.

4.3 Efficiency analysis

The proposed system works in nW to µW power range. Therefore, the voltage drop along the power line is important for the efficiency calculation. The power delivery resistance along the V_{DD} line of test chip layout can be calculated using the data obtained from Figure C-1.

The approximate length of the different metal line and the number of via's of the test chip layout is depicted in Table 4-3.

Table 4-3. Approximate length of the different metal lines and the number of vias on these routes

Name	Length of the metal line or number of via's
M1	450 µm
M2	50 µm
M3	22 µm
M4	170 µm
M5	150 µm
Via1(M1 to M2)	4
Via2(M2 to M3)	4
Via3(M3 to M4)	6
Via4(M4 to M5)	36
Via5(M5 to M6)	64

The resistance values of metal lines and via's can be obtained by:

$$R_{ME}(\Omega) = \frac{R_{\square}}{\frac{W}{0.24\mu m}} \times \frac{L}{0.24\mu m} \tag{37}$$

$$R_{Via}(\Omega) = \frac{Single\ via\ resis\tan ce}{Number\ of\ vias} \tag{38}$$

where R_{ME} and R_{Via} is the resistance coming from the metal lines and the vias respectively. $R_{\square}$ is the sheet resistance value in Ω/sq. The total resistance coming from different metal lines and from via's of the test chip layout is close to 48 Ω (typical resistance values are used).

The resistance value of the bond wire is depicted in Figure C-2. The bond wire length can be obtained approximately from Figure C-3. Since the full system input is pin 20, maximum distance of the bond wire will be 2.4+ (.595/2) inch=6.9 cm. Therefore, resistance from the bond wire is approximately 3 Ω (0.19 Ω/0.45 x6.9=3 Ω).

Therefore, for the worst case scenario, the power delivery resistance of about 60 Ω had to be accounted for the test-chip power line layout, and the low cost DIP package used in the experiment.

The total efficiency of the proposed circuit (η_{eff}) can be calculated through:

$$\eta_{eff}(\%) = \frac{P_{out}}{P_{in}} = \frac{(V_{out} / R_L) \times V_{out}}{(V_{in} - I_{in} * R_{IC}) * I_{in}} \times 100 \quad (39)$$

where V_{out} is the output voltage of the proposed system, R_L is the load resistance, I_{in} is the input current going to the system, and R_{IC} is power delivery resistance of the IC which in this case is approximately 60 Ω.

4.4 Experiment setup of the test IC

4.4.1 Controlled voltage generation setup

The controlled voltage generation setup from the TE module has been presented in Figure 4-9 and Figure 4-10.

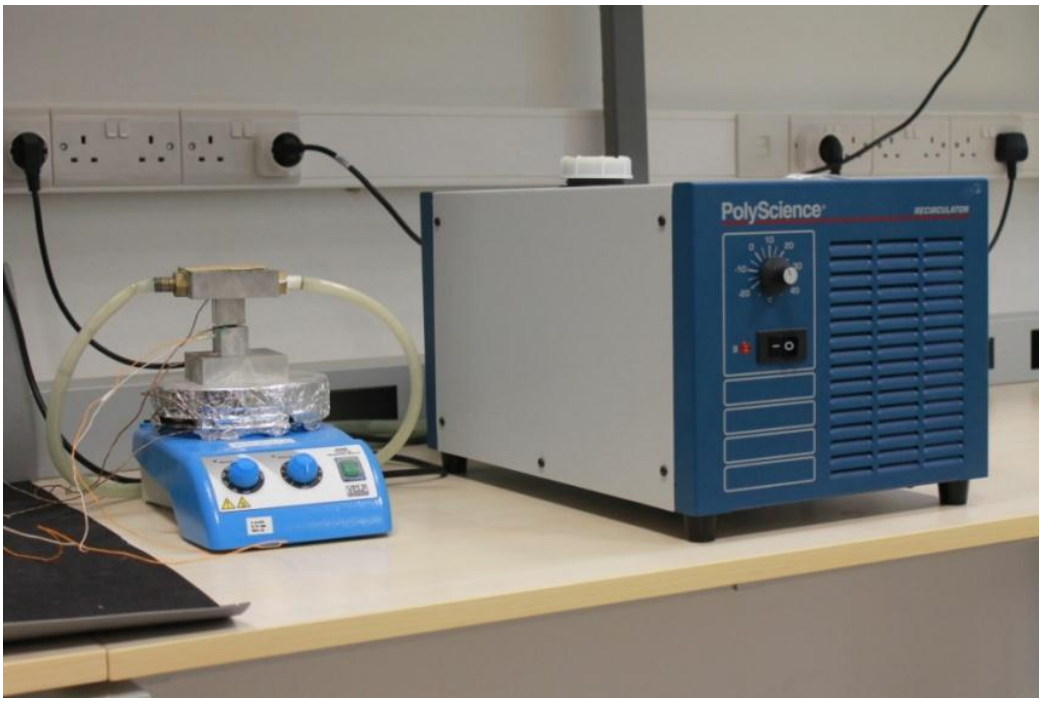

Figure 4-9. Controlled voltage generation setup from the TE module

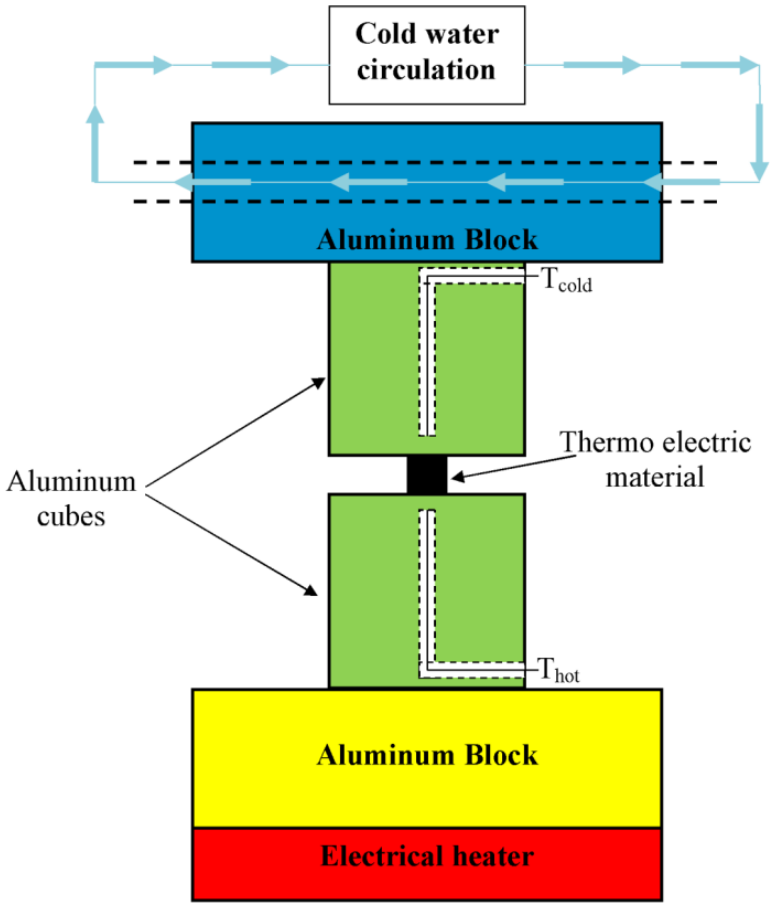

Figure 4-10. Block diagram of the TE module setup with temperature control

The thermoelectric material is located between the aluminum cubes. TETECH model TE-17-0.6-1.0P (6 mm x 6 mm) has been chosen as the TE harvester. The thermocouples used in the temperature measurement were placed in narrow channels in contact with surface of the small cubes. The lower aluminum block temperature was set using an electrical heater, while the upper block was designed to provide a regulated heat sink using a chiller. Stable 0.24 V input can be generated with 50°C temperature difference.

4.4.2 The complete experimental setup for system validation

The complete experimental setup for the system validation is depicted in the Figure 4-11. The input for the test system is generated from the TE module. The digital thermo meter is used to monitor the temperature difference between the hot and cold side of the TE module in order to generate the stabilized voltage. The probe resistance of 10 MΩ is used as the load to the

test setup. The minimum voltage of the startup and the output voltage are monitored through the digital oscilloscope, and the oscilloscope output is shown in Figure 4-12.

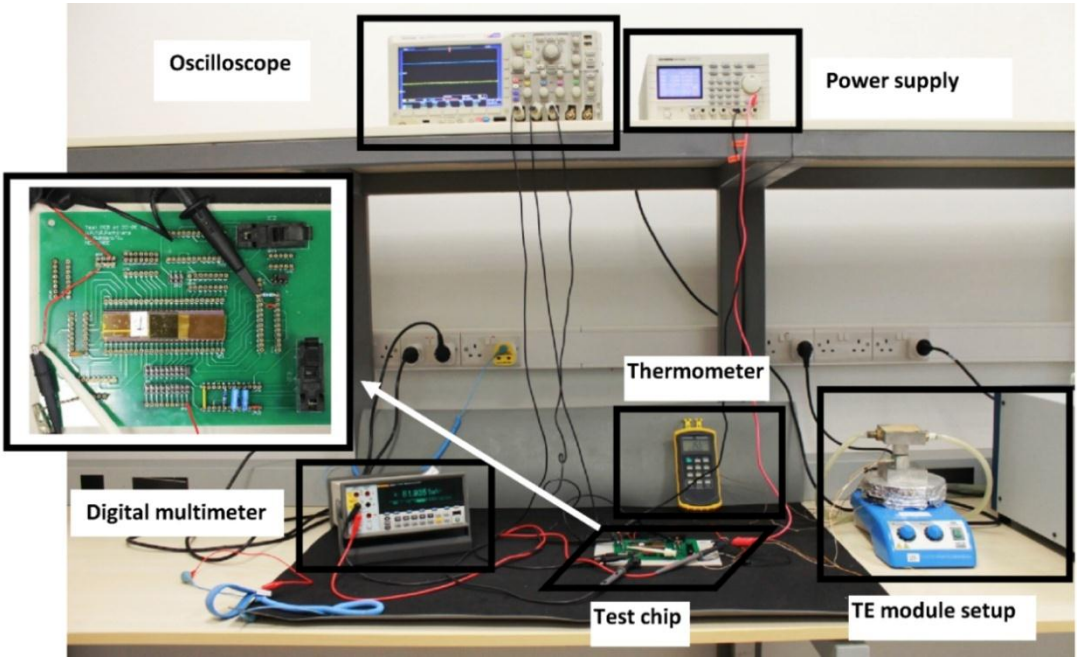

Figure 4-11. Complete experimental setup for system validation

4.5 Validation of the full system

The oscilloscope output of the full system with 10 MΩ is shown in Figure 4-12.Regulated voltage moved from simulated 1 V to 1.5 V in measurement, and the minimum startup voltage was 0.24 V instead of 0.17 V in simulation.

The efficiency of the proposed circuit has been analyzed using the load resistance range of 497 kΩ - 10,000 kΩ with different input voltages. The efficiency with different load and input voltage values is depicted in Figure 4-13.The corresponding output of the proposed circuit is shown in Figure 4-14.According to Figure 4-13 and Figure 4-14 the proposed system can achieve maximum 5% efficiency with input voltage of 0.26 V.

Post-layout simulation was carried out to identify the efficiency value at different corners at 0.24 V input. The maximum simulated efficiency at different corners for the input voltage of 0.24 V (output voltage regulated to 1 V) is shown in Figure 4-15.

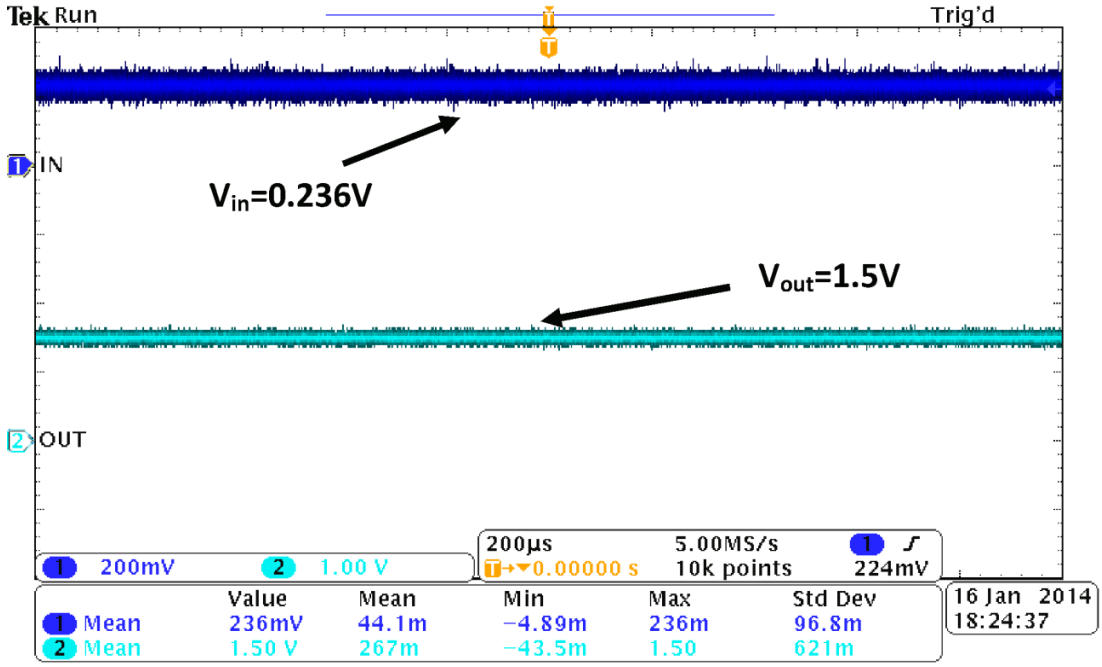

Figure 4-12. The oscilloscope output with 10 MΩ

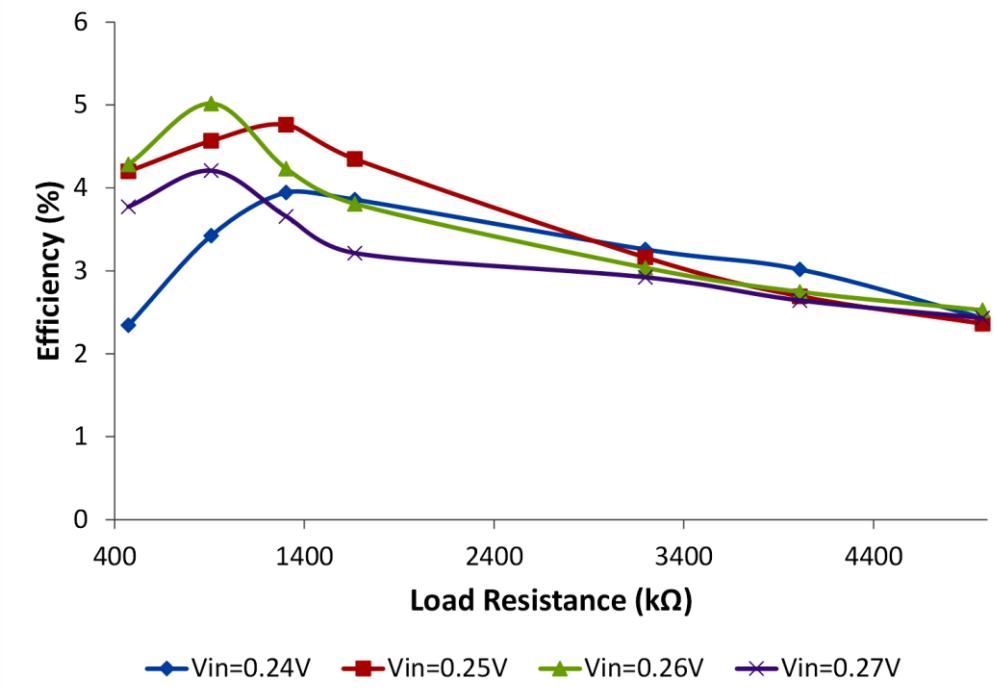

Figure 4-13. Measured efficiency of the proposed system at V_{in} =0.24 V, 0.25 V, 0.26 V and 0.27 V

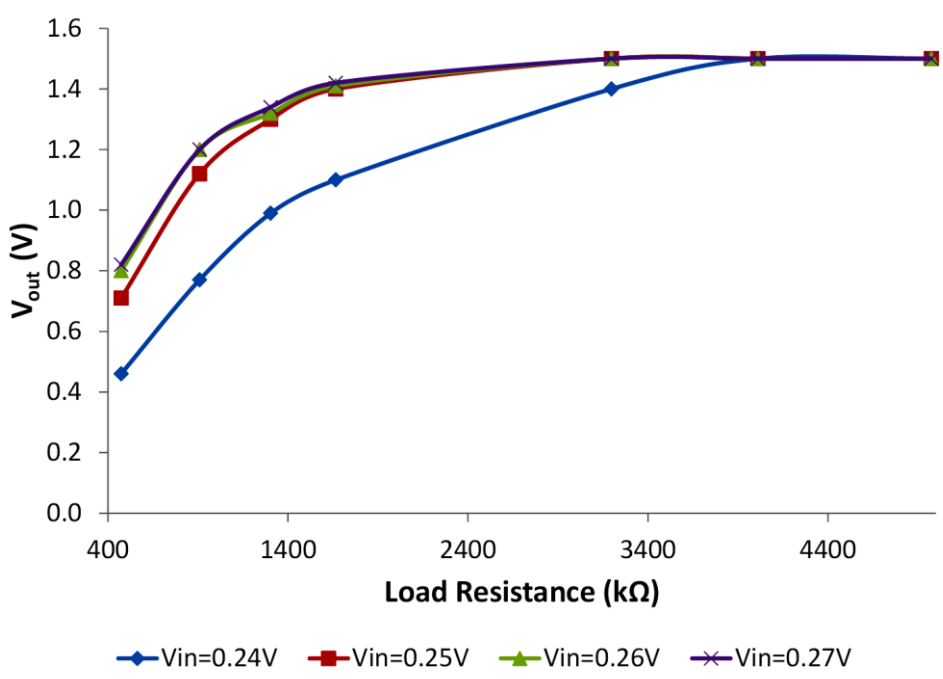

Figure 4-14. Measured output voltage of the proposed system at V_{in} =0.24 V, 0.25 V, 0.26 V and 0.27 V

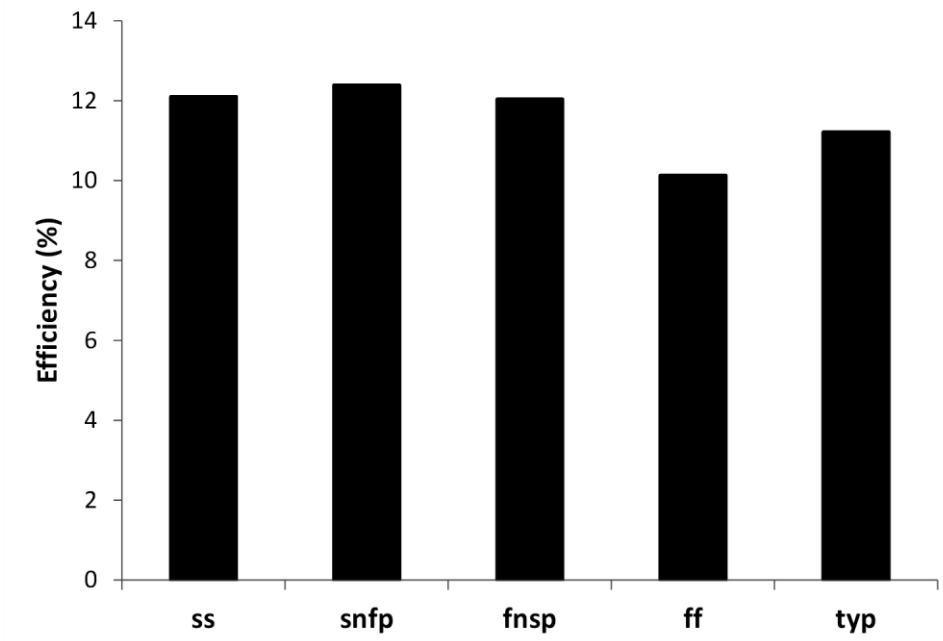

Figure 4-15. Maximum simulated efficiency at different corners for the input voltage of 0.24 V and output regulated voltage of 1 V

4.6 Correlation between simulation and validation results

4.6.1 Process corner identification

According to the results from the Figure 4-15, 10% or higher efficiency is expected even in the worst process corner. Therefore, the reason behind the discrepancy between simulated and measured results should be further investigated.

The process corner of the test chip can be obtained by looking at the current vs. supply voltage and frequency vs. supply voltage of the standard ring oscillator at the second stage. According to Figure 4-16 and Figure 4-17, test chip is very close to the typical region rather than snfp condition. Therefore, simulations at typical condition were considered in any comparison made for the sub-blocks and the full system.

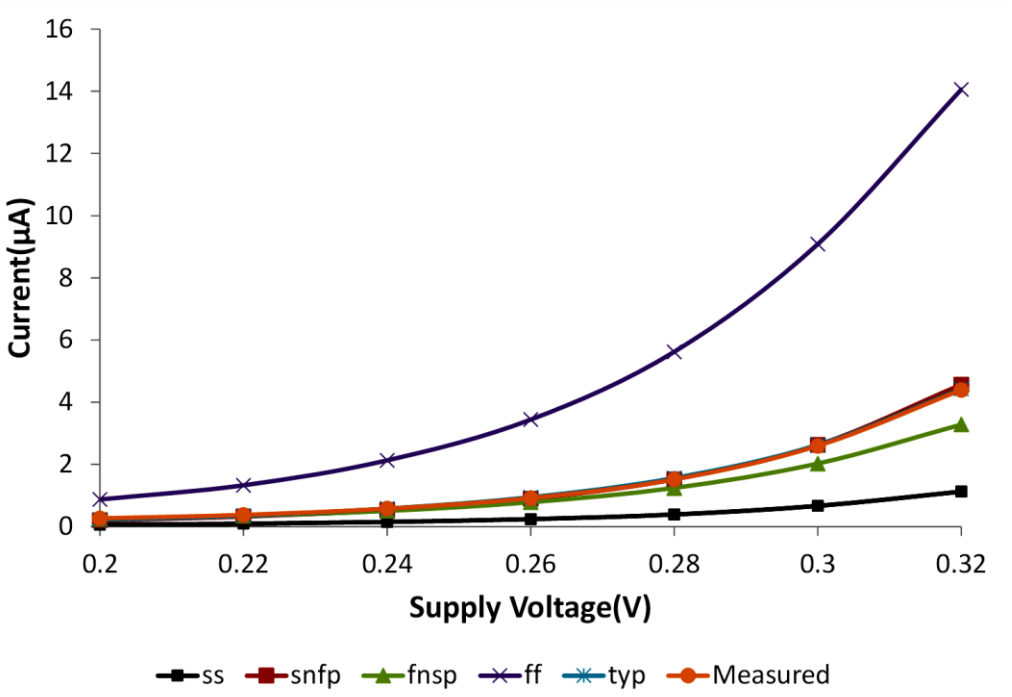

Figure 4-16. The current vs. supply voltage for the ring oscillator at different simulation corners and the measured values

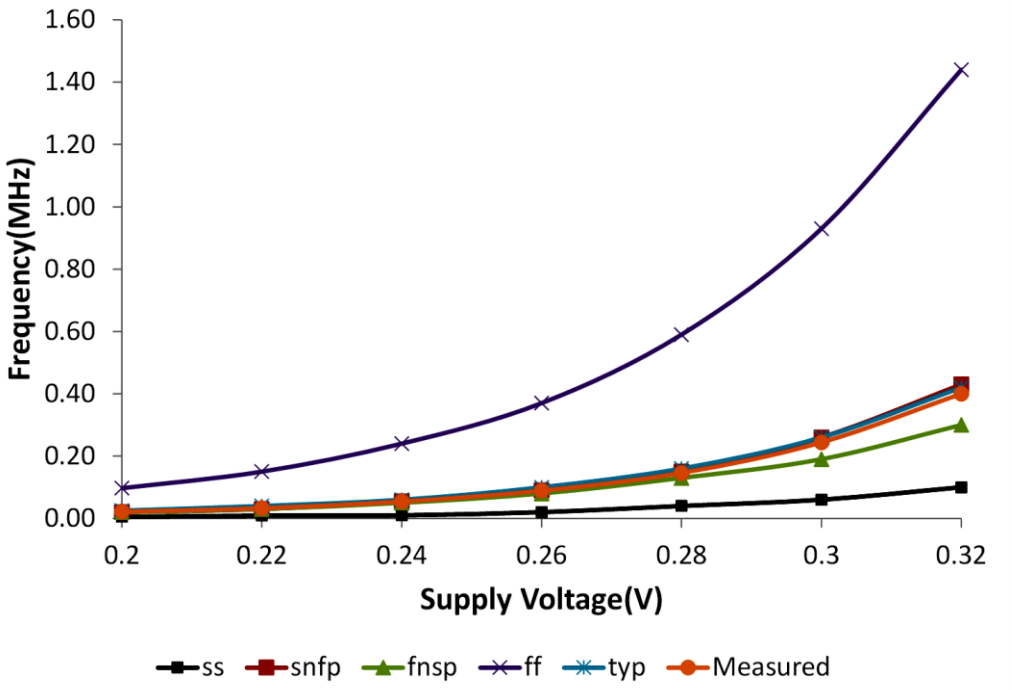

Figure 4-17. Frequency vs. supply voltage for different simulation corners and the measured values

4.6.2 The variation of the minimum input voltage

The testability circuit was used in order to investigate the minimum startup voltage limit of the full system. The first stage of the system was constructed on the test PCB board by connecting the charge pump and the subthreshold oscillator externally. The first stage charge pump on the testability circuit doesn't have integrated capacitors due to the limited area requirement and therefore they were connected externally for the testing purpose. It is also noted that, the full system functionality cannot be obtained by connecting the second stage of the system to the first stage using external wires due to the power losses associated with the wires.

Ref1 voltage was supplied by an external voltage source. Fig. 19 and Fig. 20 present the measured versus simulated results at input voltages of 0.18 V, 0.2 V, and 0.24 V for the first stage of the converter output voltage, and efficiency against the load resistance respectively.

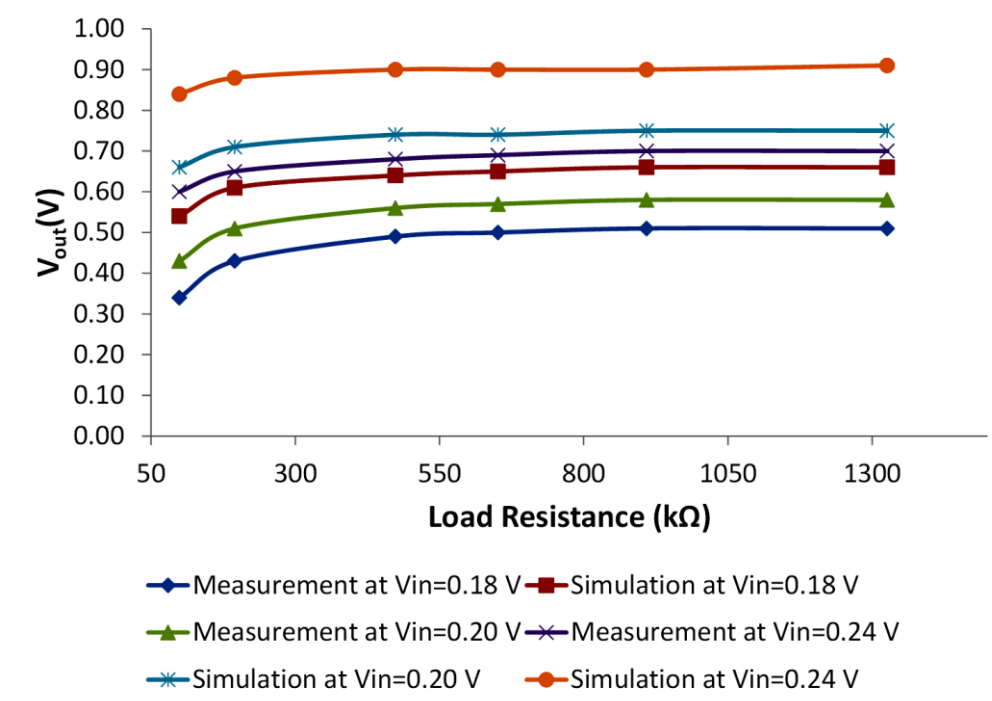

Figure 4-18. Measured vs. simulated output at V_{in}=0.18 V, 0.20 V and 0.24 V

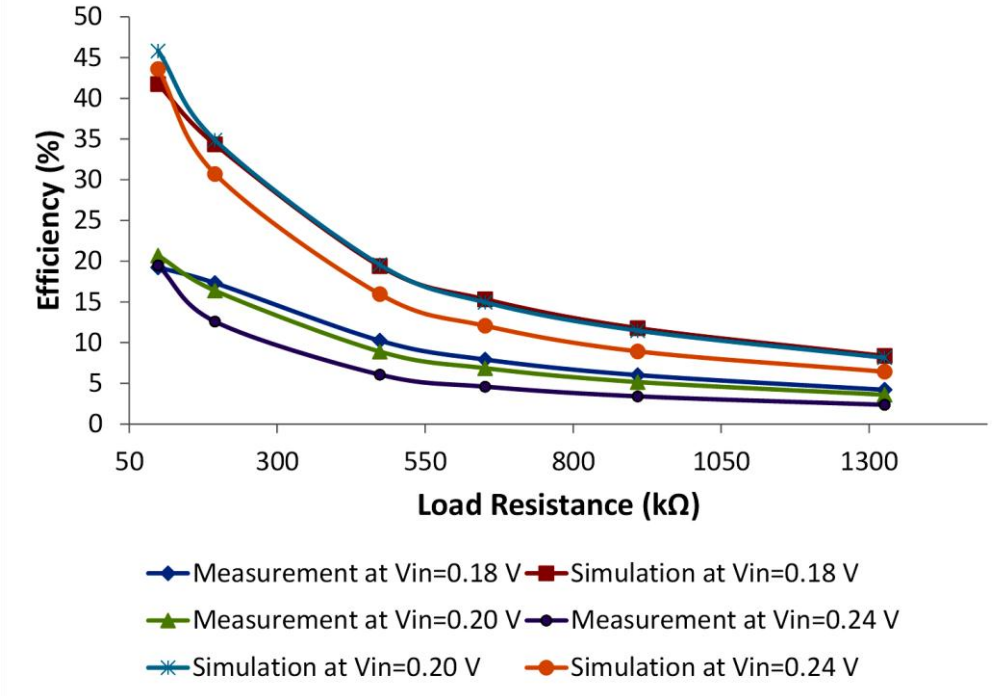

Figure 4-19. Measured vs. simulated efficiency at V_{in}=0.18 V, 0.20 V and 0.24 V

According to the results, the first stage of the converter can start up at 0.18 V, and can generate 0.5 V with 8% measured efficiency. It has been confirmed that the performance difference in minimum startup voltage between the first stage and the full system is due to mismatches between low-Vt and nom-Vt NMOS device types in 2T references in the subthreshold oscillator (Ref1).

4.6.3 The variation of the system output voltage

The reason for the variation of the output voltage was investigated by comparing the two reference generators. The variations of the reference voltages (Ref 1 and Ref 2) as well as oscilloscope probe resistance of 10 MΩ were characterized, and had to be considered to establish correlation between simulations and measurements. Comparison of the reference voltage between pre-silicon simulation and post-silicon measurement for different input voltages is provided in Figure 4-20 and Figure 4-21.

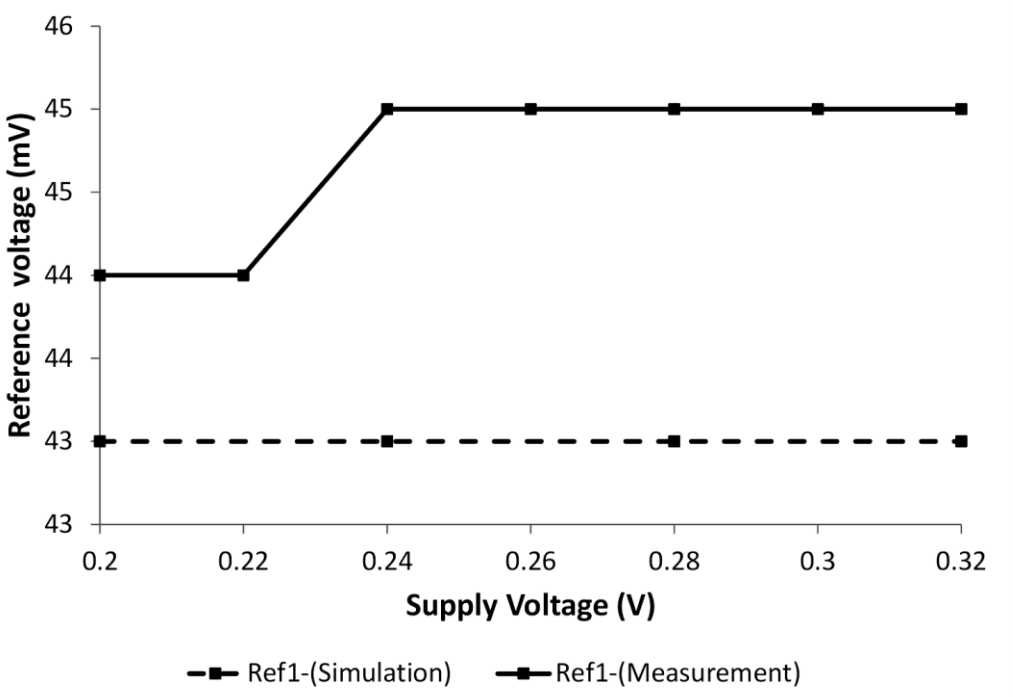

Figure 4-20. Ref1 pre-silicon simulation and post-silicon measurement for different input voltages (10 MΩ output load resistance is used to model the oscilloscope probe resistance)

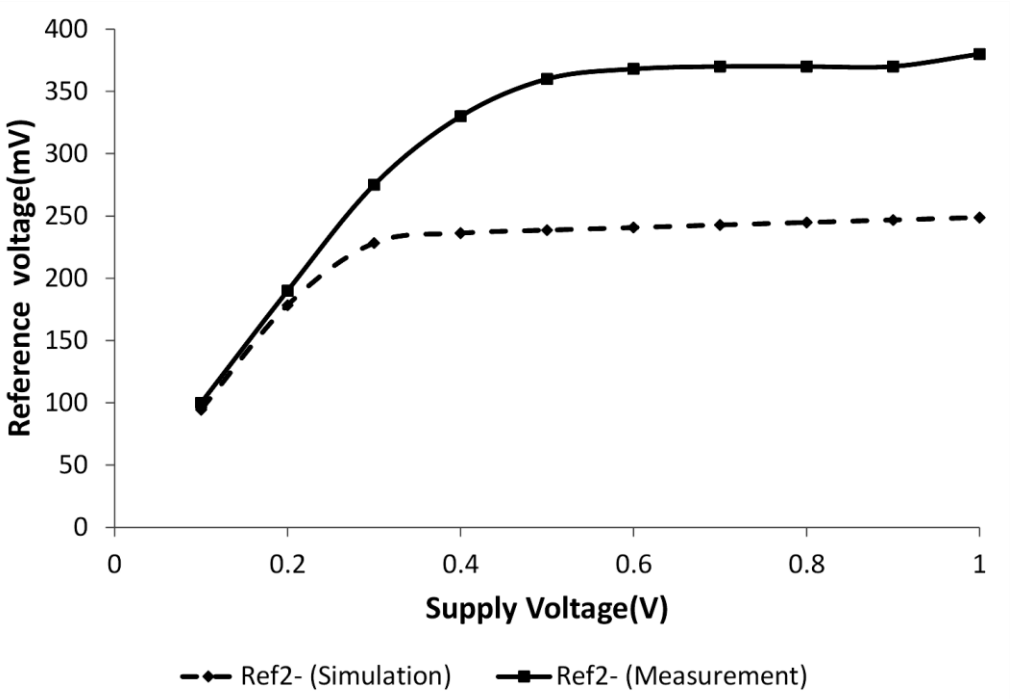

Figure 4-21. Ref2 pre-silicon simulation and post-silicon measurement for different input voltages (10 MΩ output load resistance is used to model the oscilloscope probe resistance)

The expected output voltage 0.14 V cannot be measured accurately due to low driving capability of reference voltage generator. Therefore, the measurement indicated 0.045 V output in the presence of oscilloscope probe resistance. However, the result presented in section 4.6.2 confirmed that the minimum startup failure comes from mismatches between low-Vt and nom-Vt NMOS device types in 2T references in the subthreshold oscillator.

Regulated voltage moved from simulated 1 V to 1.5 V in measurement, and the minimum startup voltage was 0.24 V instead of 0.17 V in simulation. According to the results presented in section 4.6.2 and 4.6.3, the shift is due to mismatches between low-V_t and nom-V_t NMOS device types in 2T references in the subthreshold oscillator (Ref1), subthreshold oscillator devices and zero-V_t and nom-V_t NMOS device types at voltage regulation system (Ref2).

As a result, the frequency of the subthreshold oscillator reduces from 5 to 2.8 MHz, while the second stage startup voltage moves from 0.4 V to 0.6 V approximately at the input voltage of 0.24 V. The final regulation voltage also moves to 1.5 V, since the same reference circuit is used for both comparators.

4.6.4 Leakage current estimation

The discrepancy between the simulated and measured efficiency of the converter is further investigated by measuring the leakage current of the two oscillators. The leakage current of the two oscillators is estimated using the following equation by plotting the $I_{dynamics}$ *vs. frequency*:

$$I_{Dynamic} = C(V_{dd}\, f) + I_{leakage} \tag{40}$$

where $I_{dynamics}$ is the dynamic current of oscillator, C is capacitive load, V_{dd} is input voltage, f is the frequency and $I_{leakage}$ is the leakage current of the oscillator.

The calculated leakage current of the subthreshold and regular clock generator with buffer circuits are depicted in Table 4-4. The estimated leakage of the subthreshold oscillator is higher due to the large buffer circuit as expected, but it is also higher than the simulated value.

Table 4-4. Leakage in the subthreshold and regular clock circuits

Components	V_{in} (V)	Meas. $I_{leakage}$(μA)	Sim. $I_{leakage}$(μA)
Subthresholdosc+buffer	0.24	8	3
Ring osc+ buffer	0.6	1	0.1

4.6.5 Correlation between the simulated and measured efficiency

Detailed correlation studies between simulation and measurements identified device variations from target in both I_{ON} and I_{OFF}. Power delivery resistance of about 60 Ω had to be accounted for the limited test-chip power layout, and the low cost DIP package used in the experiment. Similarly, variations of the reference voltages (Ref 1 and Ref 2) and subthreshold oscillator and oscilloscope probe resistance of 10 MΩ were considered to establish correlation between simulations and measurements.

The efficiency of the system was characterized by introducing the changes obtained from the sections 4.6.1, 4.6.2, 4.6.3 and 4.6.4.Figure 4-22 and Figure 4-23 present measured versus simulated results at 0.24 V input voltages for converter output voltage and efficiency respectively against the load resistance.

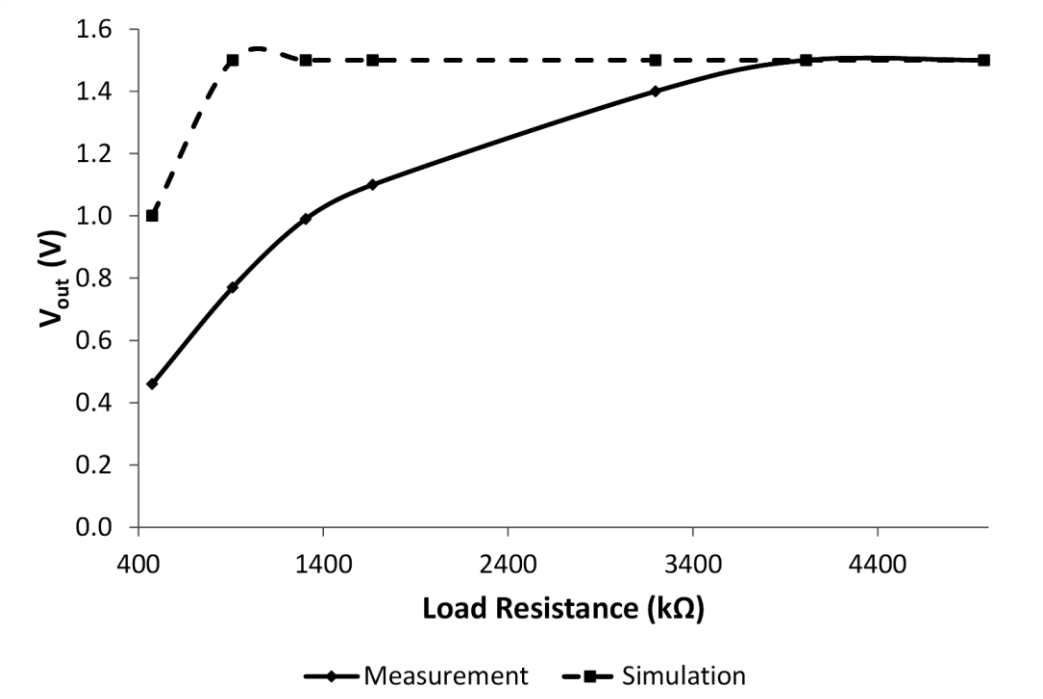

Figure 4-22. Measured vs. simulated output at V_{in} =0.24 V

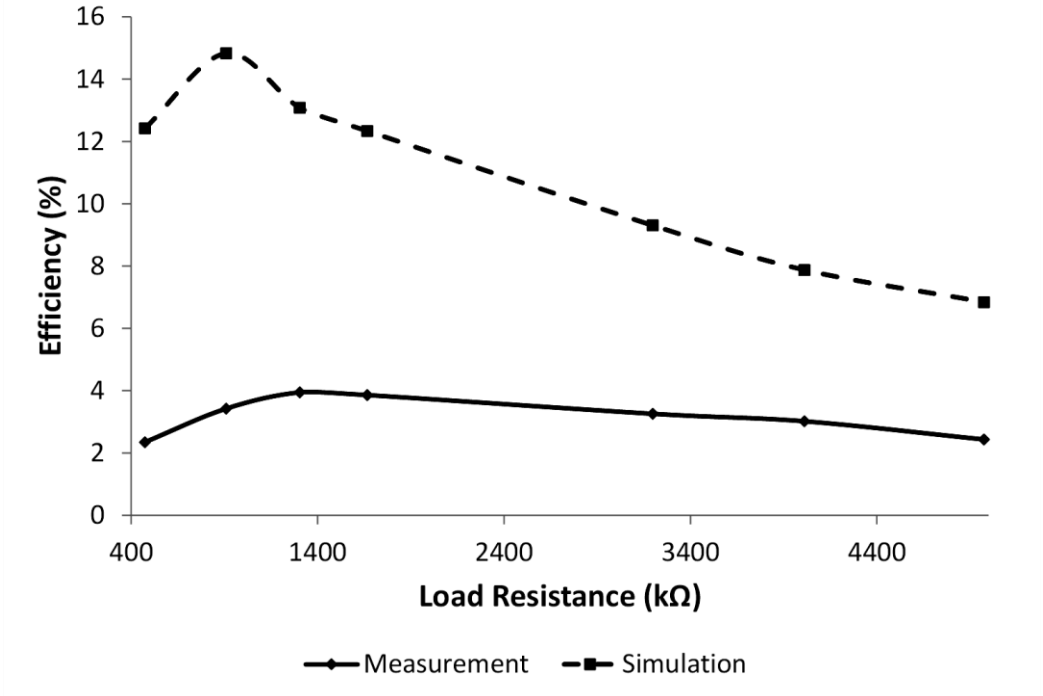

Figure 4-23. Measured vs. simulated system efficiency at V_{in}=0.24 V

Table 4-5 lists the input power (P_{in}), output power (P_{out}), and the total leakage power ($P_{Leakage}$) of the system.

Table 4-5. Power consumption (V_{in} =0.24 V, Load resistance=473 kΩ)

	P_{in}(μW)	P_{out}(μW)	$P_{leakage}$(μW)	Efficiency (%)
Measured	19.05	0.45	2.52	2.35
Simulated	17.00	2.11	0.78	12.42

The experimental efficiency of the system can be recalculated by taking measured excess leakage into account as:

$$\eta_{without\ Leakage}(\%) = \frac{\left(P_{out(Meas)} + \left(P_{Leakage(Meas)} - P_{Leakage(sim)}\right)\right)}{P_{in(Meas)}} \times 100\% \qquad (41)$$

where $\eta_{withoutLeakage}$ is the efficiency without the excess leakage, $P_{out(meas)}$ is the measured output power, $P_{Leakage(Meas)}$ is the measured leakage power of the system, $P_{Leakage(Sim)}$ is the simulated leakage power of the system, and $P_{in(Meas)}$ is the measured input power of the system.

The adjusted efficiency of the full system at 0.24 V input voltage and 473 kΩ load resistance is simulated as12.42% and measured as 11.5%. The efficiency of the first stage at 0.24 V input voltage and 473 kΩ load is simulated as 16% and measured as 14%. The 2% difference between the correlated and simulated efficiencies for the first stage of the system can be expected due to the uncalculated losses associated with the external connection on the PCB board. The leakage of the low-V_t devices in 0.18 μm technology is evidently significant for ultra-low voltage system, and it is higher than the expected values at the intended voltage range.

According to the measurement results, the performance of the proposed DC-DC converter is highly dependent on Ref1. To mitigate the dependency of the Ref1 on the converter, the diode connected PMOS resistive divider network can be used instead of Ref1.According to the simulation results, the same efficiency can be obtained with the resistive divider circuit. However, the resistive divider circuits are still prone to the process variation. Therefore, interdigitated layout can be introduced to resistive divider network as well as the differential

subthreshold oscillator in order to minimize the process variation. The comparative analysis of the layout options was left to another study.

According to the results in the Table 4-1, it is obvious that the maximum current consumption has occurred from the clock buffer in the first stage, and it is around 75% of the total current consumption. Therefore, removing the clock buffer can significantly improve the overall efficiency of the system.

The new alternative charge pump based DC-DC converter with fully integrated LC tank oscillator is proposed to remove the intermediate clock buffer. Detail of the proposed new alternative DC-DC converter is discussed in the next chapter.

4.7 Summary of the chapter

In this chapter, the planning and layout of the test chip utilized to validate the system design has been presented. Comparative analysis between experimental and simulation results has been presented. The system has been validated in application to generate 1.5 V output with 4% peak efficiency and 0.24 V input voltage. The simulation-validation correlation has been presented in detail. Finally, possible solutions are suggested for the miscorrelations between validation and simulation results.

CHAPTER 5
PROPOSED ALTERNATIVE FULLY-INTEGRATED LOW VOLTAGE CHARGE PUMP CIRCUIT WITH MAGNETIC COMPONENTS

Chapter 5 is organized as follows: The theory, design, and simulation results are presented for the blocks of a low voltage charge pump circuit with integrated inductors in 0.18 µm CMOS technology. Section 5.1 provides general overview of the proposed energy harvesting system by introducing each sub-block. Section 5.2 focuses on the oscillator design and the working principle of the same. Section 5.3 introduces the integrated inductor design, modeling of the associated losses, and design parameters. The proposed oscillator modeling and validation are presented in Section 5.4. Section 5.5 explains the design of the charge pump circuit, 2T reference generator, and regulator design. The circuit is designed to stabilize 1.5 V output voltage with 31 µW output power for an input voltage as low as 0.2 V. Section 5.6 includes the overall performance of the system as evaluated by simulations, including minimum input startup voltage, output voltage under load, and efficiency. Finally, Section 5.7 and 5.8 describe the system layout with testability structures. The chapter ends with a summary.

5.1 System architecture of the proposed system

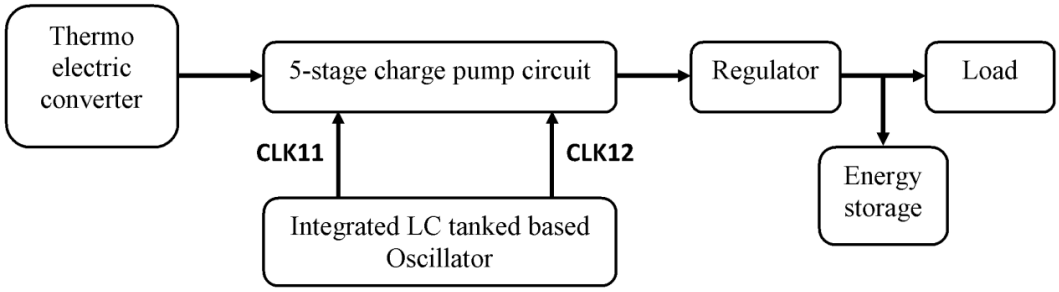

Figure 5-1. The block diagram of the proposed system

Figure 5-1 shows the overview of the proposed interface circuit (IC) for energy harvesting applications, designed in UMC 0.18 µm CMOS technology, which is an improved work over the previous design provided in Chapter 3. All sub-blocks of the system are designed and

implemented on a single chip, which offers fully integrated system that is powered with thermoelectric energy harvester.

The clock generated from the oscillator is directly fed into the charge pump circuit without using any intermediate clock buffers. This improves the system efficiency significantly compare to that of the previous designs presented by our teams [21]-[22]. The sub-circuits in each stage are outlined in the following sections.

5.2 Oscillator design

The proposed oscillator design is shown in Figure 5-2. This is the modified version of the oscillator design proposed by [46]. The tail current transistor in a conventional cross-coupled oscillator is replaced by on-chip inductors, in order to reduce the required supply voltage, and to eliminate the additional noise contribution [47]. The inductor design is the most critical part of the oscillator design, and will be explained in detail in section 5.3.7. The proposed oscillator modeling and validation are presented in detail in section 5.4.

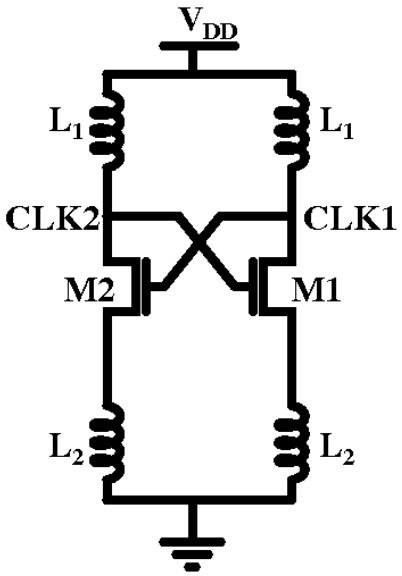

Figure 5-2. The proposed oscillator design

The expected waveforms for CLK1, CLK2, I_{L1} and dI_{L1}/dt at input voltage (V_{DD} in Figure 5-2) value of 0.2 V is shown in Figure 5-3. The proposed oscillator can generate a clock signal

with 1 GHz frequency at 0.2 V. The intuitive analysis of the proposed oscillator can be explained as follows:

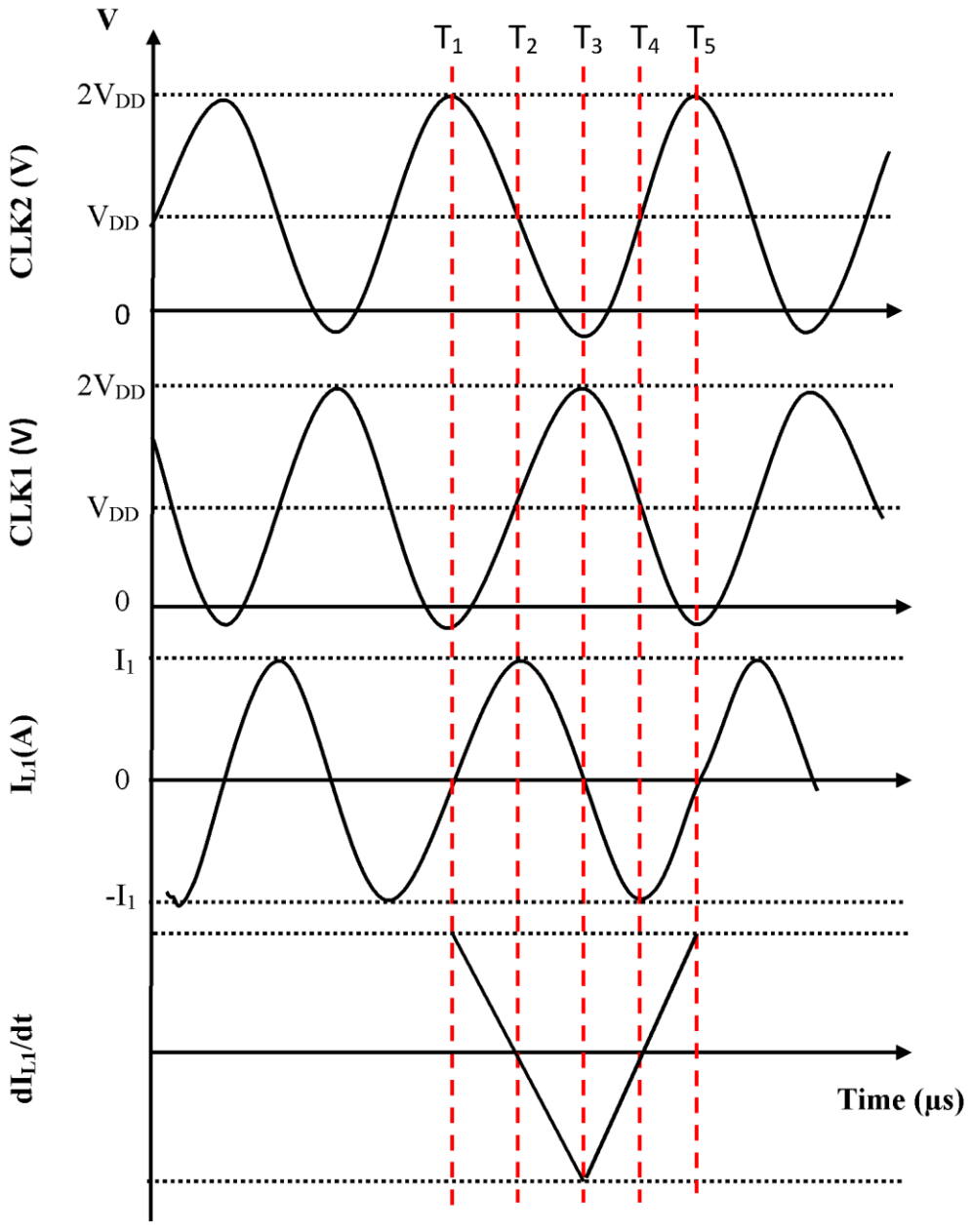

Figure 5-3. Expected waveforms for CLK1, CLK2, I_{L1} and dI_{L1}/dt

When CLK2 goes from $2V_{DD}$ to V_{DD} ($T_1 \rightarrow T_2$), current going through the inductor L_1 is increased as V_{gs} (gate source voltage) of M1 is close to $2V_{DD}$ at T_1. During this time, I_{L1} is

thus increasing and $dI_{L1}/dt > 0$. But dI_{L1}/dt is decreasing with time. Therefore, V_D (V_D is the voltage at drain of M1) will reach to V_{DD} in order to have a voltage drop of 0 V across the inductor L_1 (V_L=0 V at T_2, where V_L is the voltage drop across the inductor L_1). At the same time, CLK1 goes from negative voltage value of $V_{negative}$to V_{DD}. When CLK2 goes from V_{DD} to $V_{negative}$ (T_2 to T_3), current going through the inductor L_1 starts to decrease as V_{gs} of M1 goes to zero. Also, $dI_{L1}/dt < 0$ and its magnitude increases with time. So the CLK1 increases beyond the V_{DD} supply voltage level of the oscillator, and reaches $2V_{DD}$. The inductor acts as a battery and generates approximately V_{DD} voltage, across the inductor and pushing the drain voltage of M1 go to a voltage closer to $2V_{DD}$.

During the time period from T_1 to T_3, V_s (source voltage of M1) will follow the same voltage waveform with lower amplitude due to the voltage drop across M1. Conceptual voltage waveforms of M1 drain and source voltages of are shown in Figure 5-4.

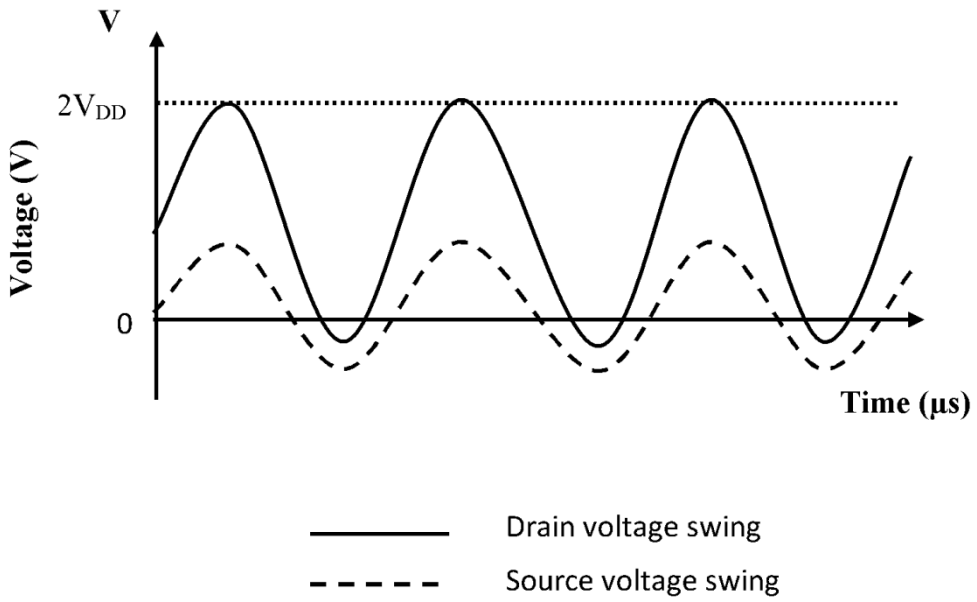

Figure 5-4. Conceptual voltage swing of M1 drain and source voltages

From T_3 to T_4, $dI_{L1}/dt < 0$ and its magnitude decreases with time. Therefore, V_D will reach V_{DD} in order to set the voltage drop across the inductor L_1 is 0 V (V_L=0 V at T_4).

From T_4 to T_5, $dI_{L1}/dt > 0$ and its magnitude increases with time. At the same time, V_{gs} of M1 becomes high, and the MOSFET is switched on. The voltage at node B (CLK1) should go

beyond the ground voltage and reach negative voltage value of $V_{negative}$ due to the loading of L_2.

5.3 Integrated inductor design

5.3.1 Introduction

An inductor is a passive element designed to store energy in the form of magnetic flux. The typical inductor consists of a wire loop or coil. The inductance of the coil depends on the conductor total length of the coil and the magnetic properties of the material around which the coil is wound. If current is allowed to pass through an inductor, the generated voltage across the inductor is given by [58],

$$V_L = L \times \frac{di}{dt} \tag{42}$$

where L is the inductance of the inductor, and di/dt is the rate of change of the current.

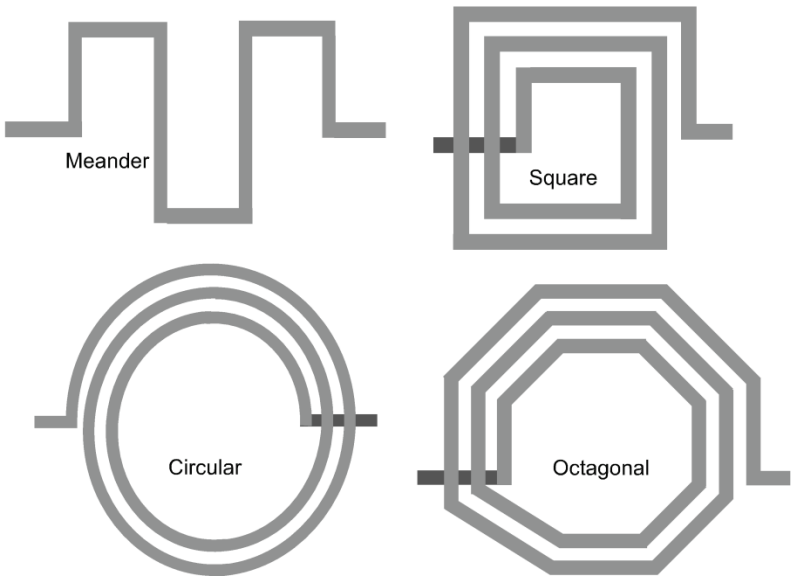

Figure 5-5. Planar inductor structures [59]

In silicon technology, conventional 3-D inductor design is a difficult task due to the limited metal layers in the process. On the other hand, inter metal dielectric between metal layers create large overlap capacitance, which reduces the maximum usable frequency and the

quality factor. Therefore, the planar spiral inductors created using top metal layer are popular in silicon technologies [37]. A planar spiral inductor can be laid out in numerous ways as shown in the Figure 5-5.

The spirals should ideally be laid out as circular if possible, since this creates a larger perimeter for the same radius, and yields higher inductance and quality factors compared to the other inductor geometries. However, circular inductor is rarely employed in integrated circuits due to an inherent limitation in mask generation. Therefore, Octagonal or Square type planar inductors are commonly used due to their flexible geometric structure [60].

5.3.2 Inductance and Quality factor of an inductor

The exact inductance value of a planar spiral inductor can be accomplished using 3D Planar Electromagnetic Field Solver Software. The other simpler method to find the inductance is using Greenhouse theory. According to Greenhouse theory, the overall inductance L_T of a monolithic inductor is given by [37],

$$L_T = L_0 + M_+ - M_- \tag{43}$$

where L_0 is the self-inductance of individual segments, M_+ is the total sum of positive mutual inductance between adjacent segments, M_- is the total sum of negative mutual inductances between segments.

The efficiency of an inductor is determined by its quality factor (Q), which is given by,

$$Q = 2\pi \times \frac{E_s}{E_L} \tag{44}$$

where E_S and E_L are stored electromagnetic energy and dissipated energy in a cycle respectively.

Assuming the losses only come from the series resistance (R_s) of the metal winding of an isolated inductor, the equation (44) can be rewritten as follows [61],

$$Q = 2\pi \times \frac{P_S \times T}{P_L \times T} = \omega \times \frac{0.5 \times L \times I_{rms}^2}{0.5 \times R_s \times I_{rms}^2} = \frac{\omega \times L}{R_s} \tag{45}$$

where P_S and P_L are the stored and dissipated power respectively, I_{rms} is the root mean square current flowing through the inductor and T is period of the cycle.

5.3.3 Loss mechanism in Silicon based spiral inductors

Losses in Silicon based spiral inductors mainly come from the metallization resistive loss and substrate loss. The losses associated with Silicon based inductor can be explained using Faraday's law (Equation (46)) and Ampere's low (Equation (47)).

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{46}$$

$$\nabla \times \vec{B} = \mu \cdot \vec{J} + \mu \cdot \varepsilon \cdot \frac{\partial \vec{E}}{\partial t} \tag{47}$$

5.3.4 Metallization resistive loss

Inductors are generally implemented using metal layers, and are prone to resistive losses due to finite conductivity. Aluminum(Al) with conductivity of 2.5 x 10^7 $\Omega^{-1}m^{-1}$ is used in conventional Si processes [62]. At lower frequency, DC resistance is significant and can be calculated using,

$$R = \rho \frac{l}{A_m} \tag{48}$$

where ρ is the resistivity of the metal, l and A_m are length and cross sectional area of the metal.

However, at higher frequencies, the induced electromotive force causes a non-uniform current distribution in the conductor. The current will reside at the conductor surface, which reduces the effective cross sectional area of the conductor. This is called the skin effect, and is directly proportional to the operating frequency [37].

Skin depth δ is defined as,

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{49}$$

where f is the frequency, σ is the conductivity, and μ is the permeability of the metal conductor respectively.

This suggests that, at higher frequencies δ decreases, increasing the resistance of the conductor. The skin resistance of the conductor (R_{skin}) can be defined as,

$$R_{skin} = \frac{1}{\sigma\delta} = \sqrt{\frac{\pi f \mu}{\sigma}} \tag{50}$$

The resistive loss can be minimized by increasing the metal thickness. This is especially true of silicon based spiral inductors [37].

At higher frequency, eddy currents are also generated in the inner conductors of the spiral, and increase the non-uniformity of the inductor current. This phenomena is called current crowding and can be explained using Figure 5-6.

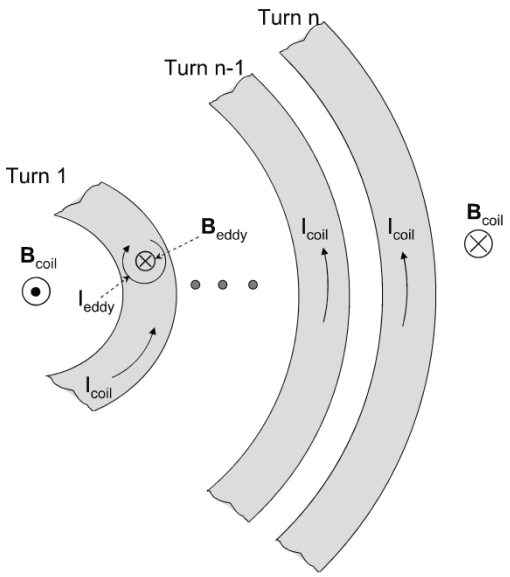

Figure 5-6. Section of an n-turn circular inductor with the fields and the eddy currents [59]

The I_{coil} and B_{coil} represent the current in the inductor and associated magnetic flux respectively.

If the inner radius of the inductor is small, the B_{coil} will pass through the inner turns. According to Faraday's and Lenz's laws, the transient nature of the magnetic field induces an electric field which, in turn is responsible for circular eddy currents in the inner turns. The generated magnetic field (B_{eddy}) due to these eddy currents reduces the total magnetic field and reduces the inductance value at high frequencies. According to Figure 5-6, the eddy current will add to the I_{coil} on the inner side (left edge) and subtract from I_{coil} on the outer side (right edge) of the conductor. Therefore, the current density will be higher on the inner side than on the outer side, which result a non-uniform current in the metal turns of the spiral inductor [59]-[62]. To minimize this effect it is necessary to use a hollow coil.

5.3.5 Substrate loss

Silicon based spiral inductors are usually fabricated using top and second highest metal layers. The inductor is located on top of inter metal die electric layer, which is made of silicon dioxide and the silicon substrate. These layers will couple though a parasitic capacitor, which degrades the self-resonant frequency of the inductor. The current flowing through the lossy capacitor generates ohmic losses and adversely affects the quality factor of the inductor. Therefore, the losses due to the lossy capacitor can be modeled as a grounded resistor in series with a capacitor as shown in Figure 5-7.

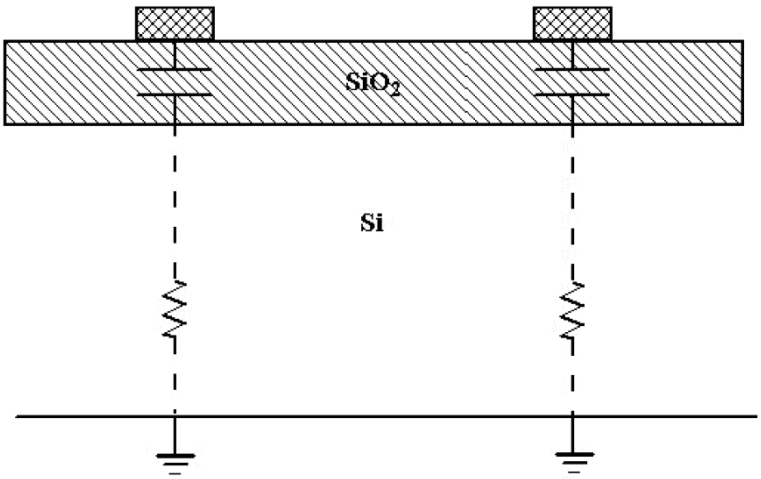

Figure 5-7. Substrate related capacitive losses [62]

Capacitive losses can be minimized by decreasing the area of the metal lines which, in turn serves to increase the series resistance as well as the self-inductance of the inductor. According to Faraday's law, the time-varying magnetic field induces an electric field in the substrate. The resulting electric field creates an image current that is limited to the substrate, and flows in a direction opposite to the inductor current as shown in Figure 5-8. These eddy currents contribute to larger substrate related losses in CMOS integrated inductors [62].

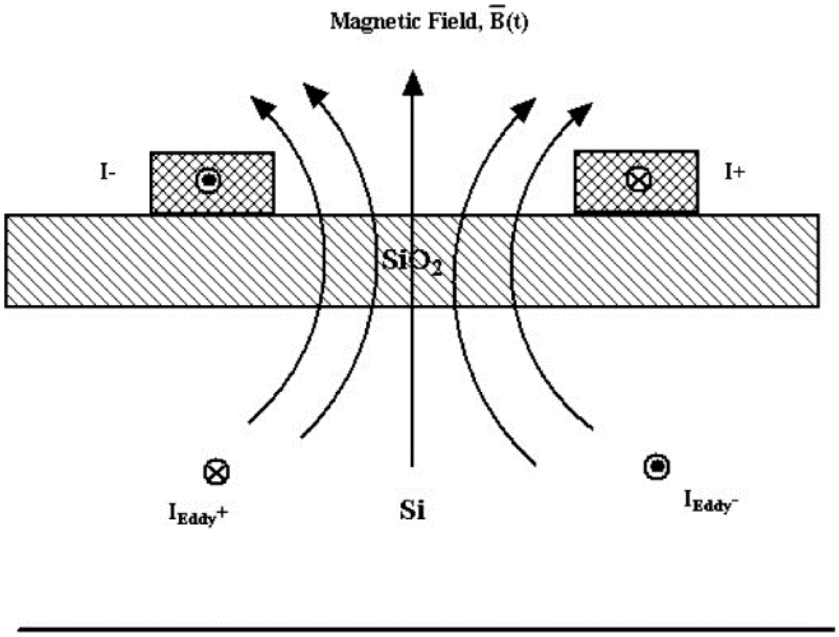

Figure 5-8. Generation of substrate currents on planar inductors [62]

5.3.6 Modeling of the inductor

The usage of on-chip inductors is limited due to the unavailability of a precise inductor model. A simple lumped lower order model can be developed in order to characterize the inductor with minimum number of discrete components [63].

The resulting π-equivalent model for two port inductor is shown in Figure 5-10. L and R_s are self inductance and the series DC resistance of the inductor (skin effects and current crowding is neglected), R_{sub} is used to model the ohmic losses in the substrate, C_L is the capacitive coupling between two metal lines in the inductor, C_{ox} models the area capacitance between the inductor and substrate, and C_{sub} is used to characterize the capacitance in the substrate.

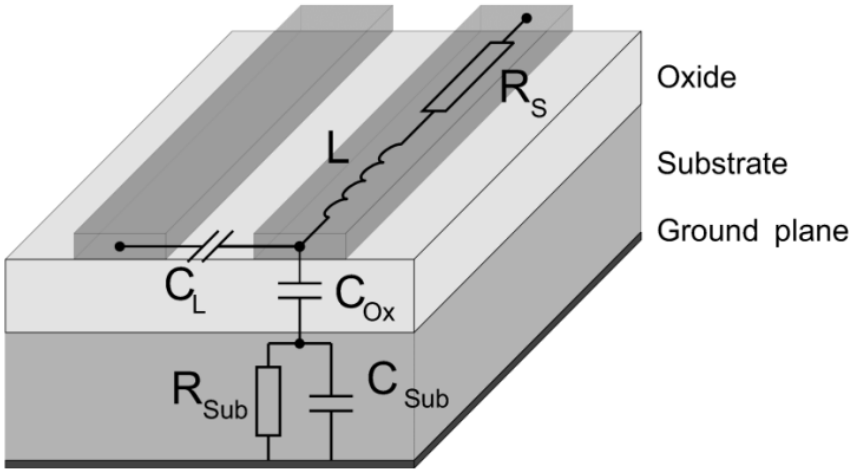

Figure 5-9. Inductor cross-section and parasitic components [63]

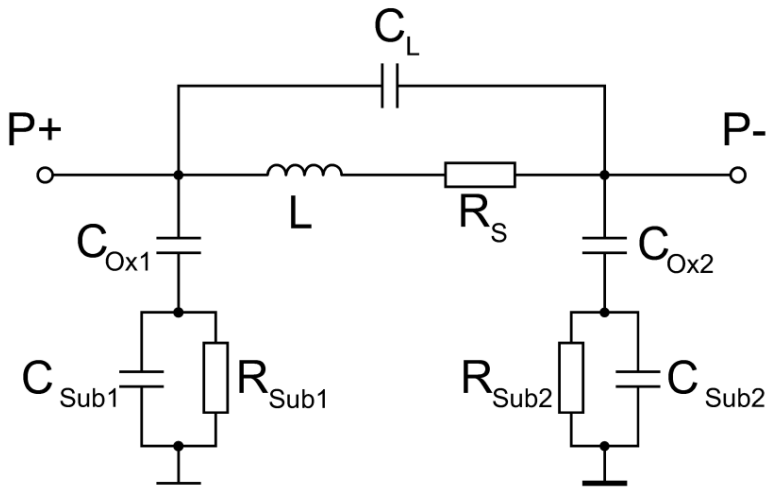

Figure 5-10. The π-equivalent model for two port inductor [63]

5.3.7 Proposed inductor design and modeling

Silicon based inductor layout design is not an easy task due to the limited support from CAD software like Cadence. The manual design of planar inductor will result in design rule violation (DRC) errors. Therefore, "*The Spiral Inductor Assistant software for Sonnet*"(freeware software)[64] is used to design the layout of the inductor, and "*SONNET*

Suites Professional Release 14.54 (3D Planar Electromagnetic Field Solver Software)"[65] is used to model the inductor and extract its inductance, quality factor and series resistance.

The DC-DC converter proposed by [32] utilizes an oscillator design with four planar inductors of 15.5 nH and 3.3 nH. If UMC 0.18 µm technology is used, the design of only four inductors will require an area of more than 0.99 mm^2, so is high in cost. The proposed inductor design utilizes two center-tap differential inductors with L_1 (0.73*0.63 mm^2) and L_2 (0.46*0.34 mm^2) between port 1 and port 2 at 1 GHz frequency (assume port 3 is open circuit), and require total area of 0.61 mm^2 which is approximately 38% area reduction. The design methodology of the inductor is shown in Figure 5-11.

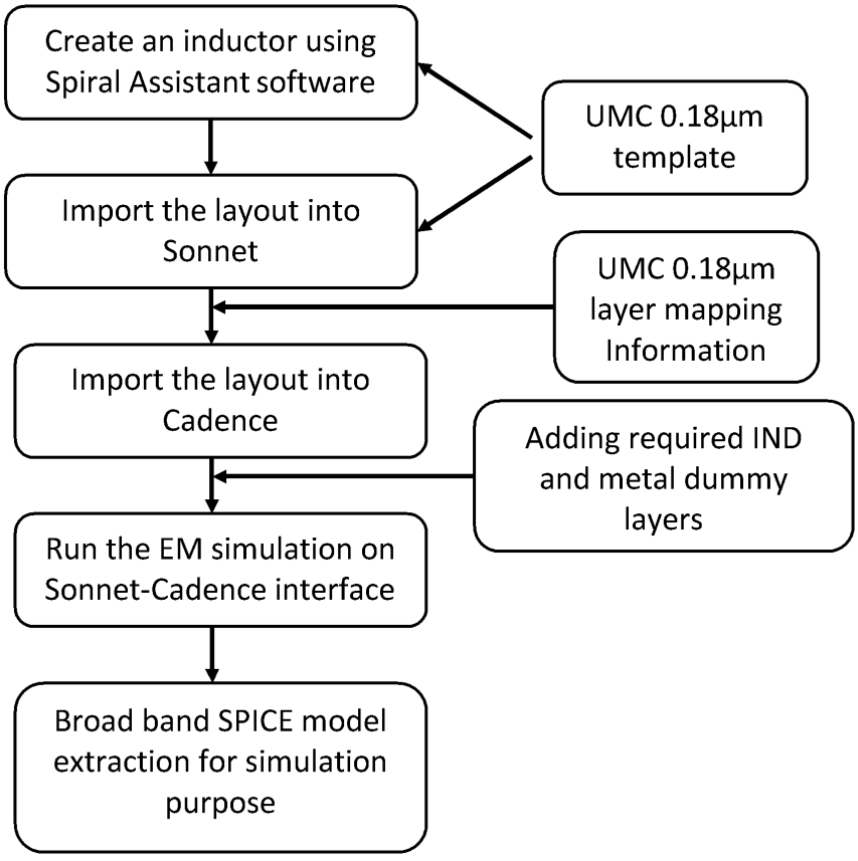

Figure 5-11. Design methodology of the integrated center-tap differential inductor

The layout of the center-tap inductor of L_2 is shown in Figure 5-12.

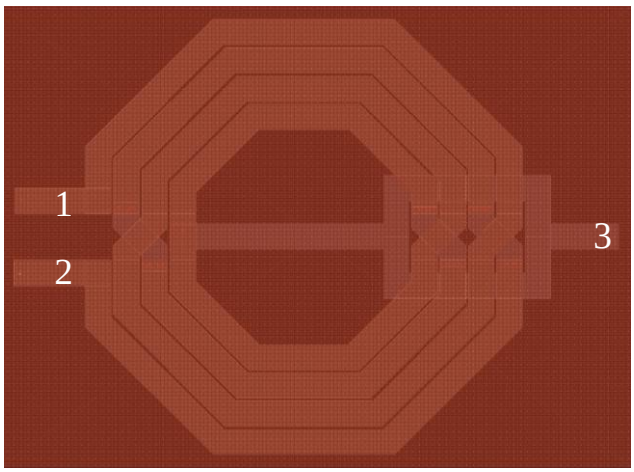

Figure 5-12. The layout of the L_2 center-tap inductor

The inductance between port 1 and 3 (or between port 2 and 3) is required in order to carry out the oscillator modeling.

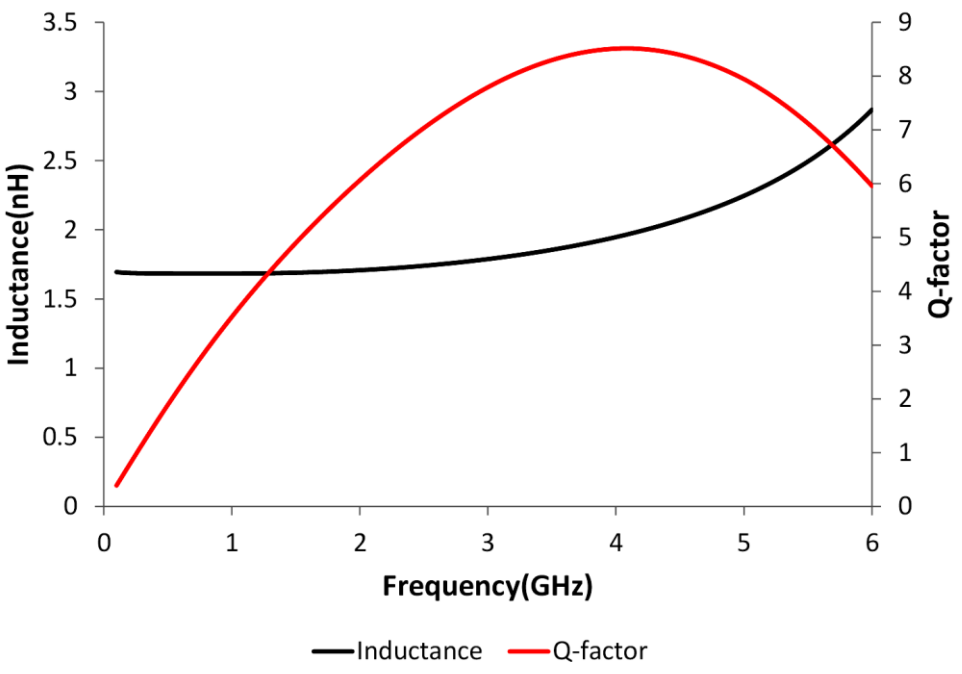

Figure 5-13. The inductance value and Quality factor of L_2 between port 1 and port 3 at different frequencies

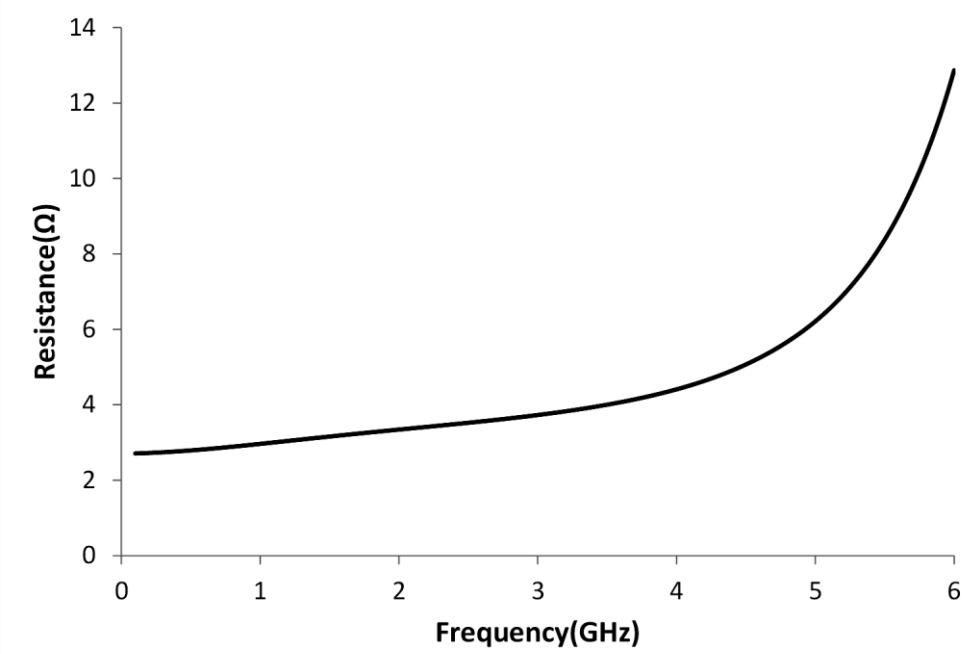

Figure 5-14. The series resistance value of L_2 between port 1 and port 3 at different frequencies

The simulated values of the inductance, quality factor (Q-factor) and series resistance between port 1 and port 3 are depicted in Figure 5-13 and Figure 5-14 for L_2 inductor. Similar graphs can be obtained for L_1 inductor as well.

The simulated values of the inductance (L_{13}), series resistance (R_{s13}) and the Quality factor (Q_{13}) of the two inductors between port 1 and 3 are given in Table 5-1.

Table 5-1. Simulated values of L_{13}, R_{s13} and Q_{13} of the two inductors between port 1 and 3 at 1 GHz

Inductor	L_{13} (nH)	R_{s13} (Ω)	Q_{13}
L_1	15	13.6	5.8
L_2	1.6	2.96	3.5

The inductor is designed using UMC 0.18 µm technology with 20KA Aluminum Top Metal 6 and Metal 5 layers in order to generate high Q value [66]. The width of the metal inductor is 19 µm.

5.4 The proposed oscillator modeling and validation

Figure 5-15 shows the parasitic components of the LC oscillator, considering the symmetry of oscillator model.

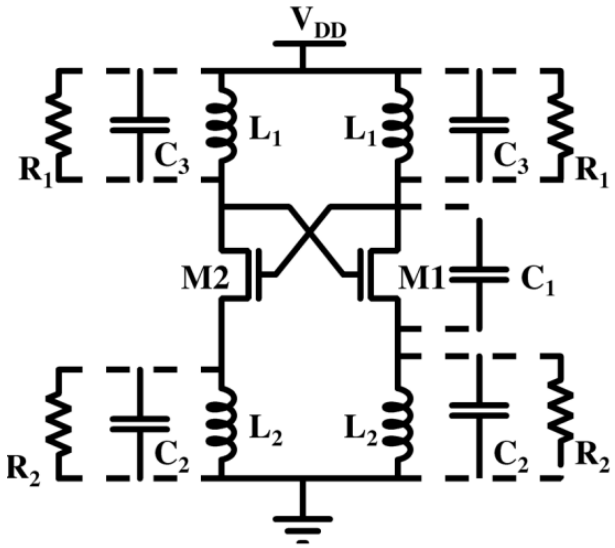

Figure 5-15. The proposed oscillator design with parasitic components

L_1 and L_2 are the self-inductance of the inductors between port 1 and port 3 (or port 2 and port 3). C_2 and C_3 are the total parasitic capacitances of the inductors L_2 and L_1 respectively. R_2 and R_3 are the parallel resistances of the inductors L_2 and L_1 respectively, and C_1 is the total parasitic capacitance of the M1.

The series parallel transformation of the impedance of a LR circuit can be used to derive parallel resistance values of L_1 and L_2. Figure 5-16 shows series and parallel LR circuits.

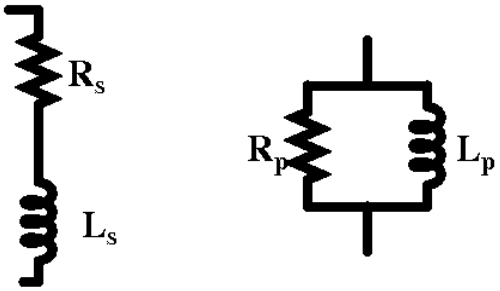

Figure 5-16. Series and parallel LR circuits

If the impedance of the parallel circuit is equivalent to that of the series circuit, then the circuits are equivalent and can be written as,

$$Z_{par}=Z_{ser} \text{ or } \frac{R_p sL_p}{R_p + sL_p} = R_s + sL_s \tag{51}$$

Taking an imaginary part of the equation,

$$R_s sL_p + R_p sL_s = R_p sL_p \tag{52}$$

If $R_p>>>>R_s$ equation (52) becomes $L_s=L_p$

By substituting the values into the real part of the equation (51);

$$R_p = \frac{(\omega L)^2}{R_s} \tag{53}$$

The calculated values for R_1 and R_2 are ~2440 Ω and ~77 Ω respectively at oscillation (where *f=1 GHz*).

In order to derive the startup conditions and the oscillation frequency, the equivalent half-circuit of the proposed oscillator is used, and is shown in Figure 5-17.

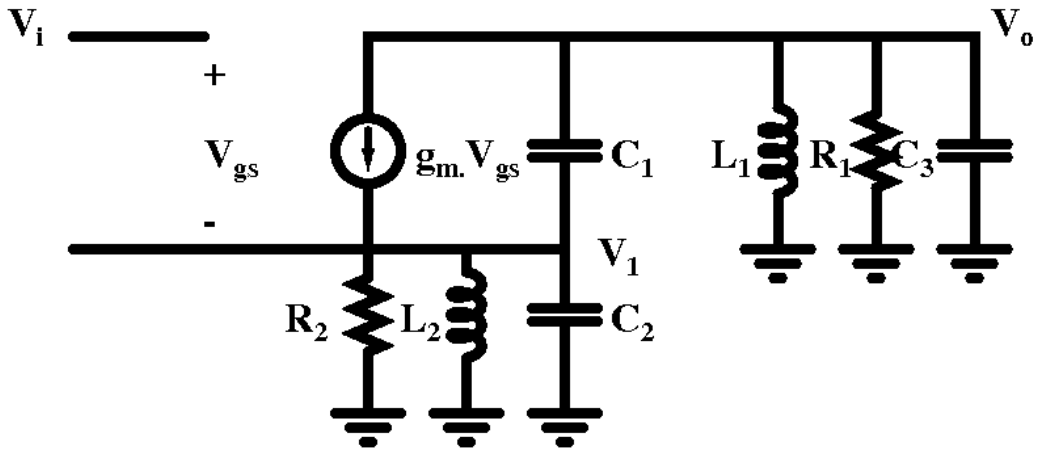

Figure 5-17. Half-circuit model of the proposed oscillator

Using Kirchhoff's Current Law (KCL), the current at the V_1 node can be written as follows,

$$\frac{V_1}{R_2}+\frac{V_1}{L_2 s}+V_1 C_2 s+(V_1-V_0)c_1 s=g_m V_{gs} \tag{54}$$

$$\frac{V_0}{R_1}+\frac{V_0}{L_1 s}+V_0 C_3 s+(V_0-V_1)c_1 s=-g_m V_{gs} \tag{55}$$

From (54) and (55)

$$\underbrace{V_1\left[\frac{1}{R_2}+\frac{1}{L_2 s}+C_2 s\right]}_{A}=-\underbrace{V_0\left[\frac{1}{L_1 s}+\frac{1}{R_1}+C_3 s\right]}_{B} \tag{56}$$

From (56) to (55);

$$\frac{V_0}{V_i}=\frac{-g_m}{\left[B+C_1 s+\frac{B}{A}g_m+\frac{C_1 B s}{A}\right]} \tag{57}$$

where $V_{gs}=V_g-V_1=V_i-V_1$

To sustain oscillation $\frac{V_0}{V_i}=-1$

By using this condition into (57), and considering the real part of the equation, the final equation can derived as follows,

$$a\omega^4+b\omega^2+c=0 \tag{58}$$

where,

$$a=(C_3 L_1 R_1)(C_2 L_2 R_2)+(C_1 R_1 L_1)(C_2 L_2 R_2)+L_2 R_2 L_1 R_1 C_1 C_3$$

$$b=-(L_1 L_2+C_3 L_1 R_1 R_2+C_2 L_2 R_2 R_1-g_m L_1 R_1 L_2+C_1 R_1 L_1 R_2+g_m L_2 R_2 L_1+C_2 L_2 R_2 R_1)$$

$$c = R_1 R_2$$

L_1, L_2 can be found using the inductor model in sonnet and parallel transformation can be used to find the R_1 and R_2(equation 2); g_m (transconductance of M1) can be found approximately using the following equation at 0.2 V,

$$g_m = \frac{2I_D}{V_{gs} - V_{th}} \tag{59}$$

where I_D=392 μA, V_{gs}=0.4 V, V_{th}=0.25 V.

The calculated transconductance of M1 is (g_m) approximately 5 mA/V. C_1 is around 100 fF, and can be extracted from the layout. Since the frequency of the oscillation is 1 GHz at 0.2 V, the estimated values of C_3 and C_2 can be obtained by solving the equation (58) using a numeric solver, such as "*Excel Solver*". The estimated values for the C_3 and C_2 are 1.68 pF and 0.4 pF respectively.

The model can be validated using well known equation of the LC tank based oscillator. The frequency of the LC tank based oscillator is given by (17). The frequency of the oscillation will be decided by the values of L_1 and C_3 [67].

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{15\times10^{-9}\times1.68\times10^{-12}}} = 1GHz \tag{60}$$

5.5 Charge pump design, reference voltage design and regulator design

The 5-stage charge pump utilized in the previous design (Chapter 3) is used in the proposed DC-DC converter. The proposed regulator design is depicted in Figure 5-18.

At the beginning, the voltage at the node, ResDiv is lower than the node 2Tout, and M4 is switched on. The comparator output ampout keeps M6 switched on until the node Vreg reaches the regulated output voltage of 1.5 V. LDO (Low Drop Out) MOSFEET, M6 (PMOS) width is set to 100 μm in order to minimize the voltage drop across the drain and source of M6. 2T reference voltage generator and comparator are the same as the ones described in

Chapter 3 with an improved layout design in order to reduce the effect of the process variation. Detailed layout information of the system is given in section 5.7.

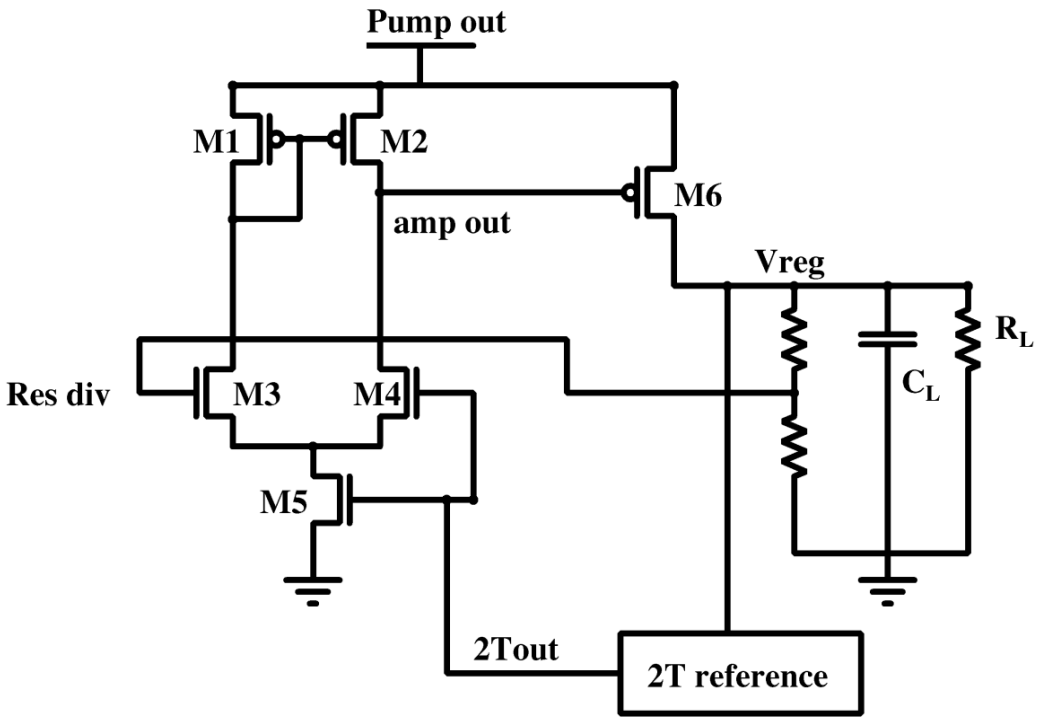

Figure 5-18. Proposed regulator design

5.6 System simulation

The proposed interface design in 0.18 μm UMC technology has been verified using Cadence. The startup condition of the circuit is verified by measuring the output voltage, loaded with own power management circuit for different input voltages. The result is illustrated in Figure 5-19.According to the results, the proposed system is able to start with 0.122 V input voltage, and generates 0.97 V without any external load resistance. The efficiency of the proposed circuit has been analyzed using the load resistance range of 20 kΩ - 150 kΩ with different input voltages. The efficiency calculations with different load and input voltage values are depicted in Figure 5-20. The output voltage of the proposed system with different load and input voltage values is shown in Figure 5-21.

According to Figure 5-20 and Figure 5-21, the proposed system can achieve 22% efficiency with an input voltage of 0.2 V. It also generates required 1.5 V output voltage over a wide

range of loads. However, the circuit can also be started up with an input voltage as low as 0.15 V based on the simulations, and generates 1.3 V with 12.5% of maximum efficiency in this condition.

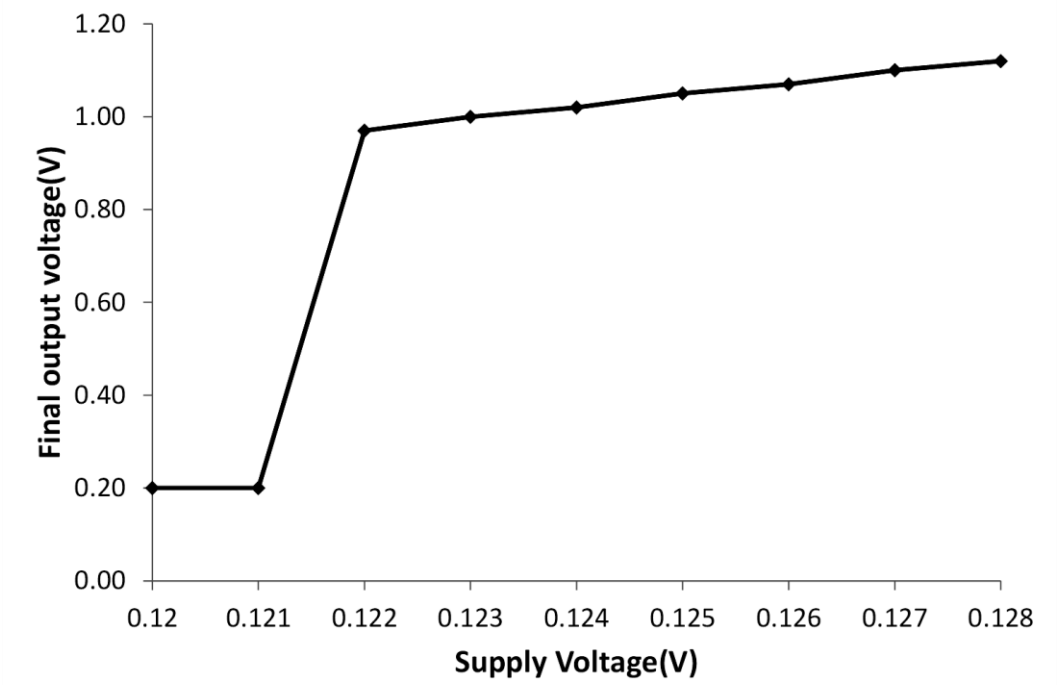

Figure 5-19. Final output voltage for different input voltages, using own power management circuit as load

The proposed system can generate more than 96% and 94% of power compared to the previous works of [21] and [22] due to improvements. The peak efficiency has been increased from 12% to 22% for design 1 [21] and 20% to 22% for design 2 [22], while minimum start up voltage is reduced to 0.122 V [22]. Area of the proposed system is increased by 64% compared to that of the previous design while reducing the minimum startup voltage by 10% (simulated).

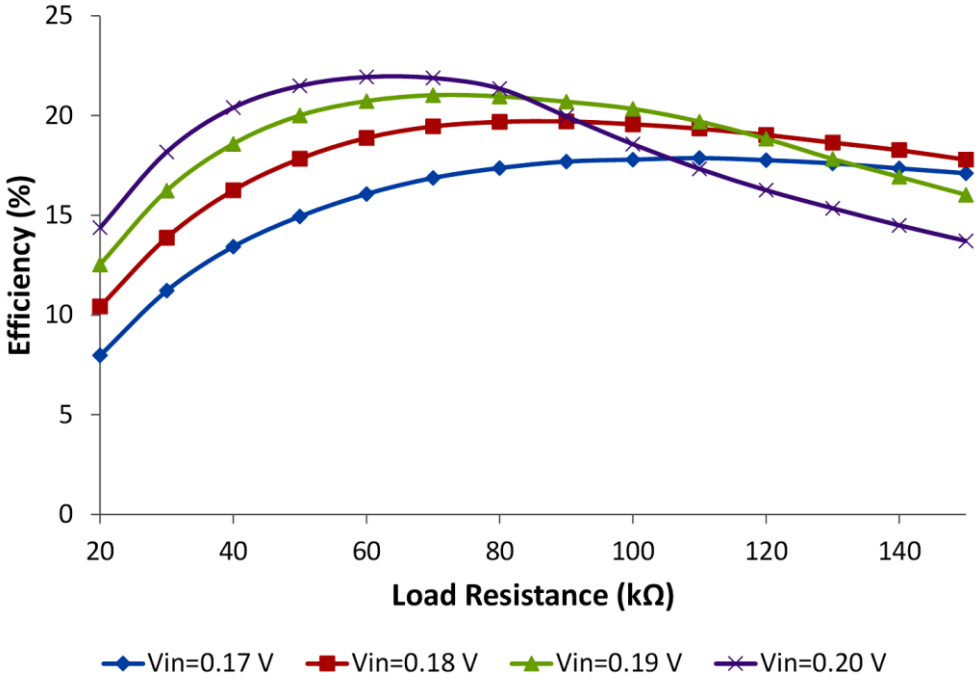

Figure 5-20. System efficiency with different load and input voltage values

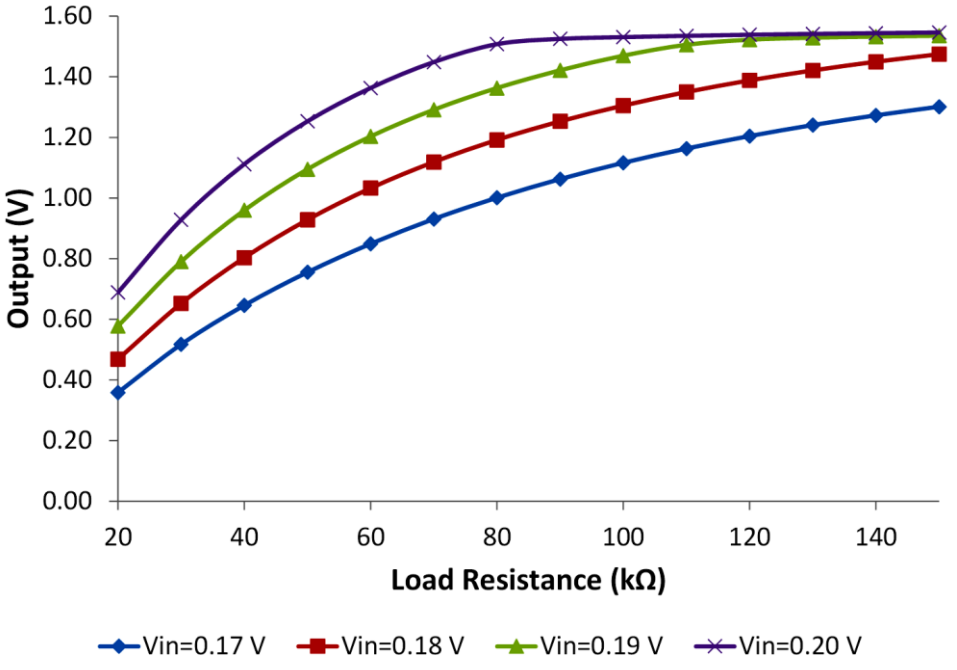

Figure 5-21. Output voltage of the proposed system with different load and input voltage values

5.7 Full system layout

Testability circuits are required on the test chip in addition to the complete system, in order to characterize the performance of each sub block. For this purpose, 9 different circuits including the main system were implemented, along with 26 pads to be used as test interface. The area requirement for the full system is 0.83 mm×1.06 mm (0.88 mm^2). The proposed testability circuit is shown in Figure 5-22.

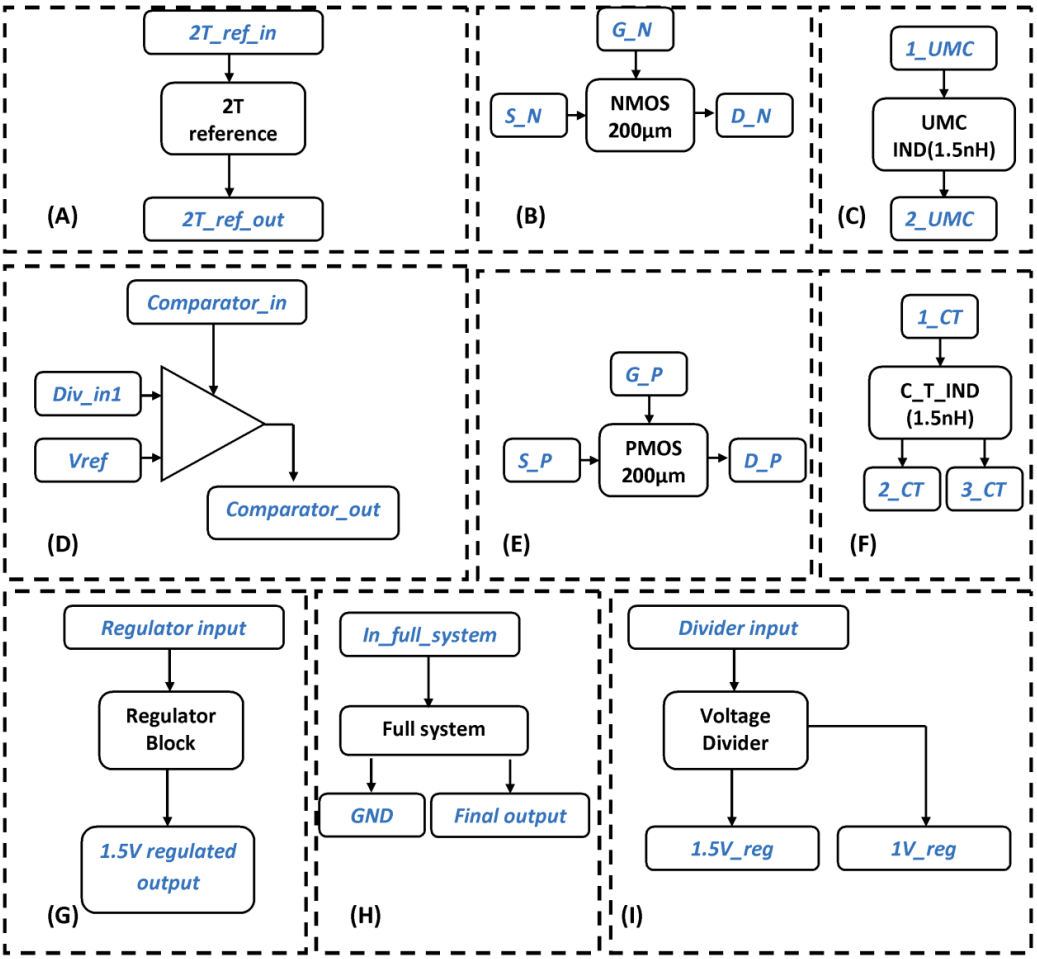

Figure 5-22. The proposed floor plan for the DC-DC converter (a) 2T reference; (b) stand-alone NMOS, (c) UMC 0.18µm standard inductor, (d)comparator, (e) stand-alone PMOS, (f) user created center-tap differential inductor, (g) regulator block, (h) full system, (i) voltage divider.

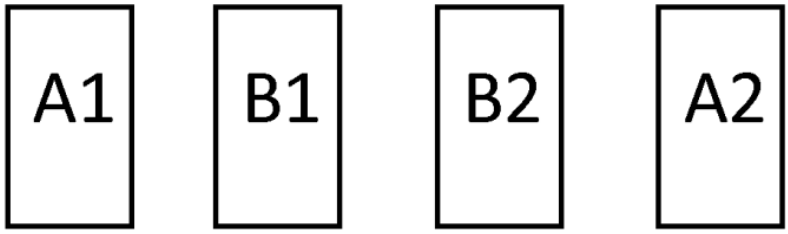

Figure 5-23. The proposed inter-digitization method

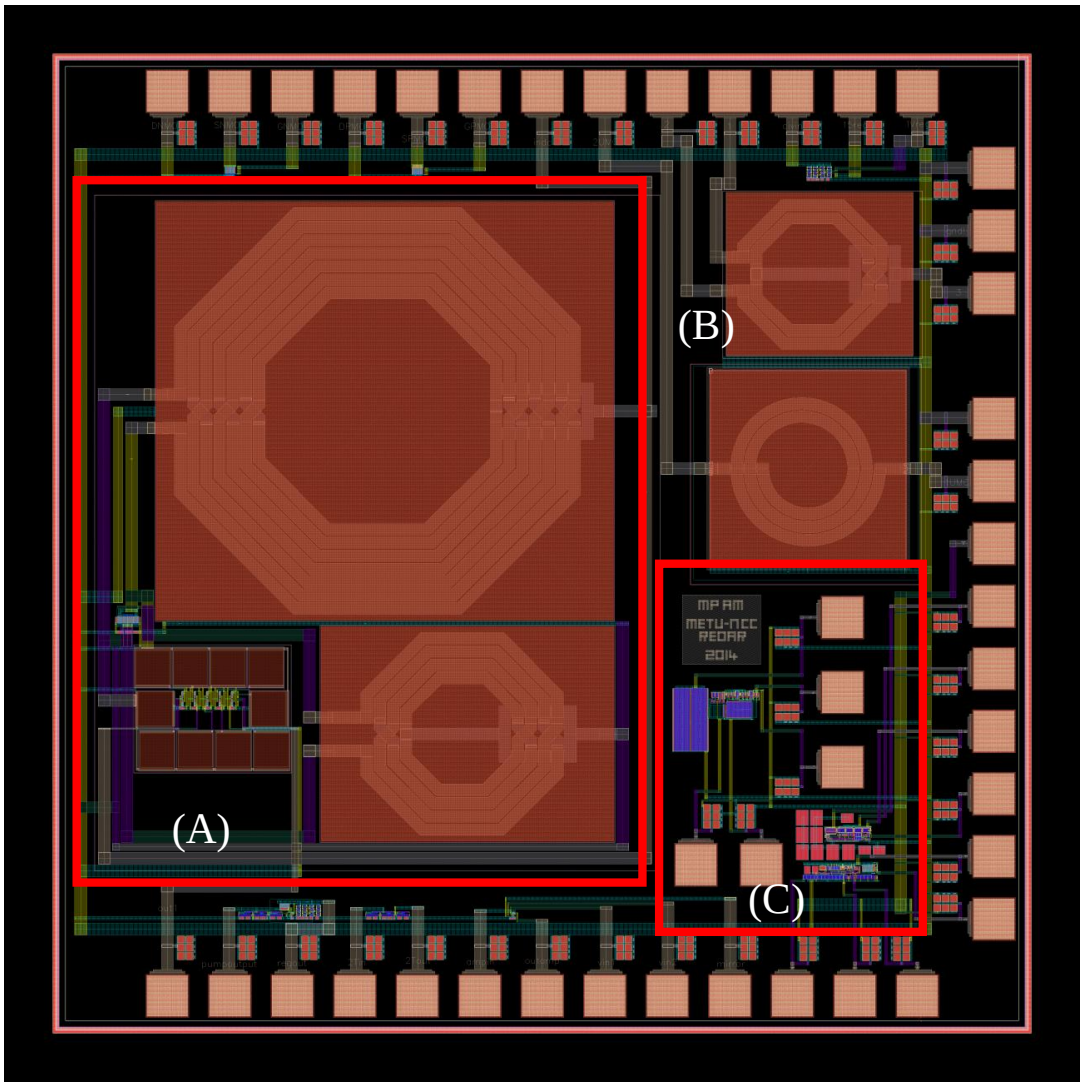

Figure 5-24. Overall die micrograph with the PAD connection: (A) Proposed system, (B) testability circuit, (C) other circuits unrelated to this thesis.

The inter-digitization technique with common centroid method is used to design the differential NMOS pair on the oscillator, and the differential amplifier in the regulator block in order avoid the effect on the process variation. The proposed inter-digitization method is shown in the Figure 5-23.

Dummy MOSFETs have been placed in 2T reference and PMOS based voltage divider in order to minimize the faults associated with the fabrication. The full system layout with the test structure is shown in the Figure 5-24. The testability I/O signal abbreviations on the Test IC are listed in Table B-1 in APPENDIX B.

The system has been sent for fabrication, but experimental results will not be included in this thesis due to time constraints.

5.8 Summary of the chapter

In this chapter, theory, design, and simulation results of the proposed improved fully integrated DC-DC converter with integrated inductors has been presented. Table 5-2 shows a summary circuit performance comparison with circuits in the literature that contain magnetic components.

The demonstrated architecture includes a complete system for energy harvesting applications, and has been designed in UMC 0.18µm CMOS technology. The LC tank based oscillator design is the critical part of the proposed system, and is explained in detail including integrated inductor design. SONNET 3D Planar Electromagnetic Field Solver Software is used to characterize the designed inductors.

The circuit is able to generate stable output voltage of 1.5 V, with 31 µW output power for input voltage of 0.2 V. The proposed system can generate more than 96% and 94% of power compared to the previous work due to improvements. Area of the proposed system is increased by 64% compare to that of the previous design while reducing the minimum startup voltage by 10%. The proposed design area is 28% larger than that of the design of [34] whereas the minimum start up input voltage is 59% less than that of [34].

Table 5-2. Performance comparison of this work against literature

	[5]	[18]	[28]	[32]	[34]	This work
Process (nm)	130	350	65	180	180	180
Input (mV)	20	35	180	200	300	200
Output (V)	1 V Regulated at 20 mV	1.8 V Regulated at 35 mV	0.74 V Unregulated at 180 mV	1.23 V Unregulated at 200 mV	1.1 V Regulated at 300 mV	1.5 V Regulated at 200 mV
External Components	inductor	inductor	inductor	1 nF capacitor	1.2 nF capacitor	No
Startup	650 mV External	Mechanical Switch	self	self	Pre charging required	Self
Area (mm^2)	0.12	1.6	-	-	0.63	0.88
Efficiency at same input voltage	52% at 20mV	58% at 35mV	-	19.8% at 200mV	45%** at 300mV	22% at 200mV

(**The efficiency provided here is only for the boost converter and it was calculated after pre charging the output capacitor to 0.75V (the detail provided in Section 2.4)).

CHAPTER 6
CONCLUSION

6.1 Thesis conclusion

In this thesis, two different fully-integrated low voltage self-starting charge pump based DC-DC converters have been designed, and implemented for energy harvesting applications. The goal of the designed interface electronics is to efficiently step up the low voltage generated by the thermoelectric energy harvester to a stable standard DC output voltage. The proposed first system (system with no magnetic components) has 4% maximum measured efficiency and can supply constant output voltage of 1.5 V with a supply voltage as low as 0.24 V, as validated using a 6 mm x 6 mm TE micro-module. Simulation-to-measurement correlation studies have been reported in detail, for the first time to our knowledge in such a low-voltage micro-power generator topology. Problem areas and enhancements have been identified in order to attain simulated efficiency target of 18% with 0.17 V input and 1 V output. A significant learning out of the validation process is that technologies, which are accurately targeted and characterized at nominal voltage ranges, may not provide sufficient predictability at ultra-low voltage ranges for energy harvesting applications. Part of the obtained results from this work has been presented in conferences such as ICEAC 2012 and THERMINIC 2013.

The second proposed system has been developed with fully integrated magnetic components. The proposed system is the improved work of the previous design and it can start up with low voltage as low as 0.122 V without any external load. The system can successfully convert 0.2 V up to 1.5 V (31 µW output power) with 22% efficiency based on simulation. The inductor is modeled using 3D Planar Electromagnetic Field Solver incorporating the losses associated with the silicon based spiral inductors. The LC tank based oscillator used in the design is explained in detail, and is verified. The full system required 0.88 mm^2 area. The usage of center-tap differential inductors in the oscillator topology achieved 38% of area reduction, compared to the usage of separate four inductors. However, area of the proposed system is increased by 64% compare to that of the previous design while reducing the minimum simulated startup voltage by 10%. The expected simulated efficiency improvement of the

design is 9% compare to the previous design. The full system design has been submitted for fabrication. The validation for the second system cannot be obtained due to time constraints.

6.2 Future work

The experimental and simulation results have provided sufficient evidence that the implemented circuits in 180 nm provide unique solutions for small, fully-integrated on-chip supplies with TE input. Therefore, it opens a door for future research areas in energy harvesting interfaces. A comprehensive list of future studies is listed below:

[1]. The validation of the second proposed system can be carried out and compared with the simulation results.

[2]. The smaller package (QFN package instead of DIL package) can be used in order to reduce the parasitic effect associated with package.

[3]. An on-chip sensor with suitable operating parameters compatible with the proposed systems can be added on the same chip with smaller package. Then the total system can be mounted on a TE harvester to have a completely integrated sensor system. A feasible example for this sensor is a temperature sensor.

[4]. The hybrid input interface circuit can be developed with another energy harvesting topology, such as photovoltaic (PV) energy harvesters in order to enhance the power output and the overall efficiency of the system.

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APPENDIX A

THE DETAIL DESCRIPTION OF THE PIN ABBREVIATION OF TESTABILITY STRUCTURE

Table A-1. The detail description of the pin abbreviation of testability structure and the corresponding pin number of the IC

Block Name	Pin Number	Pin name	Description
Full system	20	In_full_system	Full system input
	17	Final_out	Output of the final system
	43	GND	Ground connection
2T reference circuit	18	in_sub osc+buffer+2T_reference	Total input for 2T reference, buffer, subthreshold oscillator, subthreshold NAND
	26	2T_out_osc	Output of 2T reference
Buffer+ subthreshold oscillator	21	amp_out_or_Vbp	Output of the amp or Vbp(If amp is not working we can give the bias voltage until osc start working(0-0.2)
	25	CLK11	Clock output of subthreshold oscillator
	28	CLK12	Clock output of subthreshold oscillator
Level_shifter	33	VDD_H	Level shifter high voltage input(0.4-0.5V)(First stage out)
	15	VDD_L	Level shifter low voltage input(0.2V=V_{dd})
	31	comp_out/lev_shifter_in	Comparator output from the regulation system or input of the level shifter (initial value is 0V)

	32	Level shifter_out/input to NAND	Level shifter output (initial value is 0)
Comparator at the final regulation	16	comparator_in	V_{dd} of the comparator(0.4-0.5V)(First stage output)
	29	Div_in1	input from the voltage divider(positive in)
	30	Vref	Reference voltage(negative in)(0.3V)
Charge pump at First stage	19	pump_in_first_stage	Input the first stage charge pump
	34	first_stage_out	Output of the charge pump/As a whole output of the first stage
	48,12,24,23,22	C1,C2,C3,C4,C5,C6	External capacitors
Charge pump at Second stage and Resister divider Circuit	9	pump_in_2nd_stage	Input the second stage charge pump
	8	Final out_test/resdiv_final_in	Output of the charge pump/As a whole output of the system/resistor divider input
	47,46,45,44	C2,C4,C6,C8	External capacitors
	10	CLK21_pump_2ndstage	CLK input for the internal capacitors of the charge pump
	5	res_div_final_out	Resistor divider output
Ring oscillator+Buffer+NAND+ Hysteresis Comparator	11	Ring_in	Input for the ring oscillator(Output of the first stage)
	40,41	CLK21,CLK22	CLK output of the ring osc
	39	hyst_out_or_enable_signalto_ring	Enable signal for ring osc (Initial value 0.5V)
	14	hyst_in	V_{dd} of Hysteresis Comparator
	38	Div_in	Divider input for the Hysteresis Comparator(positive)

2T reference and the voltage divider at the intermediate section	35	In_2T_reg &Divider_inter	The input for both 2T reference and the voltage divider at intermediate stage
	36	2T_reg_out	Output of 2T reference at the regulation(0.3V)
	37	res_div_inter_out	Output of the voltage divider at the intermediate section
Separate subthreshold oscillator	12	sub_osc_seperate_in	Input for separate subthreshold oscillator
	3	CLK11_seperate	CLK output
	4	CLK12_seperate	CLK output
	13	Vbp	Bias voltages for the PMOS(6mV)

APPENDIX B

THE DETAIL DESCRIPTION OF THE PIN ABBREVIATION OF TESTABILITY STRUCTURE FOR NEW SYSTEM

Table B-1. The detail description of the pin abbreviation of testability structure and the corresponding pin number of the IC

Block Name	Pin name	Description
2T reference circuit	2T_ref_in	Total input for 2T reference
	2T_ref_out	Output of 2T reference
NMOS (200µm)	S_N	Source of the NMOS
	G_N	Gate of the NMOS
	D_N	Drain of the NMOS
PMOS (200µm)	S_P	Source of the PMOS
	G_P	Gate of the PMOS
	D_P	Drain of the PMOS
Comparator at the regulation	comparator_in	V_{dd} of the comparator
	Div_in1	input from the voltage divider(positive in)
	Vref	Reference voltage(negative in)(0.3V)
UMC IND	1_UMC	First port of the UMC 018µm inductor
	2_UMC	second port of the UMC 018µm inductor
C_T_IND	1_CT	First port of the centre tap inductor
	2_CT	Second port of the centre tap inductor
	3_CT	Third port of the centre tap inductor
Regulator Block	Regulator input	Input for the regulator blcok
	1.5V regulated output	1.5V regulated output
Voltage divider	Divider input	The input for the PMOS divider
	1.5V_reg	1.5V regulated output connection
	1V_reg	1V regulated output connection

APPENDIX C

RESISTANCE VALUES OF THE METAL LINES AND THE DIL-48 PACKAGE

6. Resistances:

6.1 Salicide and Metal Resistances	Min.	Typ.	Max.	Unit
N-Well sheet resistance on field (*1) (W = 20 um)	350	415	450	Ohm/sq
Note(*1): 1. for width effect: RsNW= 408*W/(W-0.32) Ohm/sq, W: resistor width 2. The resistance variation is dependent on the width of N-Well resistor. To decrease the resistance variation (3s ≤ 10%), the N-Well resistor width should be larger than 2.0 um.				
N+ sheet resistance (W= 0.24 um)	2	8	13.5	Ohm/sq
P+ sheet resistance (W= 0.24 um)	2	8	13.5	Ohm/sq
N+ sheet resistance between two Poly lines (*2) (S= 0.34 um)	8	20	50	Ohm/sq
P+ sheet resistance between two Poly lines (*2) (S= 0.34 um)	8	20	50	Ohm/sq
Note(*2): The Poly spacer of 0.08 um per side has been taken into account for resistance calculation.				
N+ Poly sheet resistance (W= 0.18 um)	2	8	12	Ohm/sq
P+ Poly sheet resistance (W= 0.18 um)	2	8	12	Ohm/sq
Metal1 sheet resistance (W= 0.24 um)	45	77	115	mOhm/sq
Metal2 sheet resistance (W= 0.28 um)	30	62	95	mOhm/sq
Metal3 sheet resistance (W= 0.28 um)	30	62	95	mOhm/sq
Metal4 sheet resistance (W= 0.28 um)	30	62	95	mOhm/sq
Metal5 sheet resistance (W= 0.28 um)	30	62	95	mOhm/sq
MMC Metal sheet resistance (W=0.6um)	7	11.5	16	Ohm/sq
Metal6 sheet resistance (W= 0.44 um)	25	41	55	mOhm/sq
(*3)optional 20KA Metal6 (W= 1.2 um)	10	20	30	mOhm/sq
(*4)optional 12kA Metal6 (W= 0.8 um)	10	23	36	mOhm/sq
N+ contact resistance (0.24*0.24 um^2)	5	15	19.5	Ohm/cont
P+ contact resistance (0.24*0.24 um^2)	5	15	19.5	Ohm/cont
N+ Poly contact resistance (0.24*0.24 um^2)	5	12	17	Ohm/cont
P+ Poly contact resistance (0.24*0.24 um^2)	5	12	17	Ohm/cont
Mvia1 resistance (0.28*0.28 um^2)	2	6.5	9.5	Ohm/mvia
Mvia2 resistance (0.28*0.28 um^2)	2	6.5	9.5	Ohm/mvia
Mvia3 resistance (0.28*0.28 um^2)	2	6.5	9.5	Ohm/mvia
Mvia4 resistance (0.28*0.28 um^2)	2	6.5	9.5	Ohm/mvia
Mvia5 resistance (0.28*0.28 um^2)(Metal6 to Metal5)	2	6.5	9.5	Ohm/mvia
Mvia5(*3) resistance (0.28*0.28 um^2)(Metal6 to MMC)	2	10	20	Ohm/mvia

Figure C-1. Resistance values of the each metal layers [66]

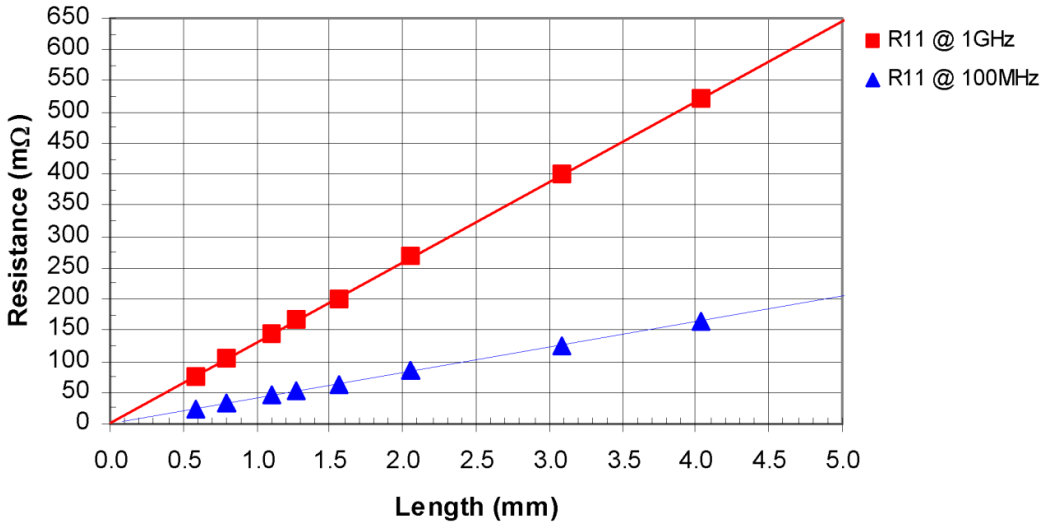

Figure C-2. Gold Bond wire Partial Self Resistance (mΩ) (1 mil Diameter) [68]

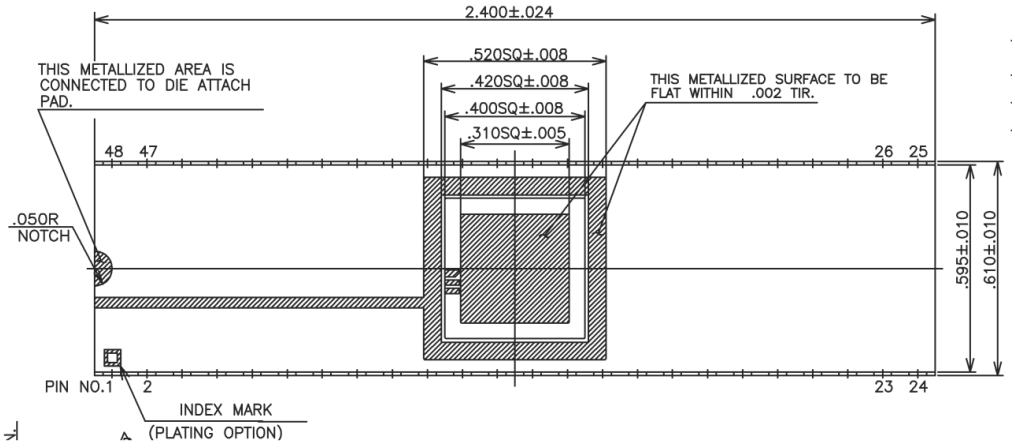

Figure C-3. The DIL-48 package plan [69]