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AN UNCOOLED MICROBOLOMETER INFRARED DETECTOR IN ANY STANDARD CMOS TECHNOLOGY

D.S. Tezcan*, F. Koçer*, and T. Akin*,**
*Middle East Technical University, Dept of Electrical and Electronics Engineering, Ankara, Turkey
** TUBITAK-BILTEN, Middle East Technical University, Ankara, Turkey
Phone: +90 (312) 210-2369 Fax: +90 (312) 210-1261 e-mail: tayfun-akin@metu.edu.tr

ABSTRACT

This paper reports a new microbolometer structure with the CMOS n-well layer as the active element. The n-well structures are suspended and thermally isolated by post-etching of fabricated and bonded CMOS chips, while the n-well regions are protected from etching by the electrochemical etch-stop technique in a TMAH solution. The characterization results of the fabricated chips show that the n-well has a TCR value of 0.50%/K at 300K in a commercial 0.8μm CMOS process. Detailed thermal simulations in ANSYS were performed to obtain an optimized structure. These results and calculations show that it is possible to implement a microbolometer structure with a responsivity of 4000 V/W and a detectivity of $1.2x10^9$ $cmHz^{1/2}/W$ with a thermal time constant of 3.2 msec. This approach is very cost-effective to produce large focal plane arrays in CMOS for uncooled infrared imaging with reasonable performance.

INTRODUCTION

Uncooled infrared detectors have recently gained wide attention for infrared imaging applications, due to their advantages such as low cost, low weight, low power, large spectral response, and long term operation. One of the most famous approaches for uncooled infrared imaging is to use microbolometer structures, where infrared radiation increases the temperature of a material, causing a change in its resistance [1-4]. There are efforts to implement microbolometers using many different materials. The most widely known and used material is vanadium oxide (VO_x), due to its high temperature coefficient of resistance (TCR) of about 2-3%/K and its low temperature process. There are 320x240 pixel VO_x microbolometer arrays, where each pixel occupies an area of 50μmx50μm [1]. The main drawback of VO_x is that it is not a standard material in IC fabrication processes. An IC compatible microbolometer material is the amorphous silicon carbide (SiC) [2], which has a high TCR value of around 4-6%/K. However, the amorphous SiC requires high temperature annealing to achieve stability of microstructures, which is not suitable for post-CMOS processing, i.e., it is difficult to merge it with a CMOS process for monolithic implementation with readout circuitry. Another IC compatible micro-bolometer material is the polycrystalline silicon-germanium (poly SiGe), which has a TCR value of 2-3%/K [3]; but its process temperature is also high for post-CMOS processing. A low temperature and IC compatible approach is to implement microbolometers using metal films such as platinum (Pt) [4], but metals have very low TCR in general, limiting their performance.

This paper reports a new microbolometer structure, which uses the CMOS n-well layer as the active material. The n-well layer has a TCR of 0.5-0.75%/K, which is the highest among various CMOS process layers, and this TCR is adequate for many infrared applications. We believe that n-well microbolometer will allow easy implementation of low cost and highly reproducible CMOS integrated microbolometer focal plane arrays for infrared imaging with a reasonable performance.

N-WELL MICROBOLOMETER STRUCTURE

Figure 1 shows the schematic cross-sectional view of the n-well microbolometer that can be obtained with any CMOS process. Infrared radiation heats the absorption layer on the thermally isolated n-well region, increasing its temperature, which in turn results in a change in its resistance related to its TCR. The bulk silicon under the n-well is etched away to reduce the thermal conductance and to increase the responsivity of detectors. This thermally isolated suspended structure is obtained by front-end bulk etching of fabricated CMOS dies, while using the electrochemical etch-stop technique to prevent the etching of the n-well [5].

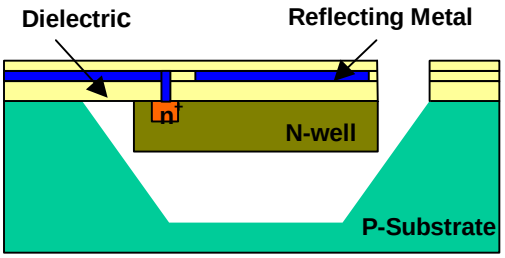

Figure 1. Schematic cross-section of the n-well microbolometer that can be obtained with any CMOS process.

Figure 2 shows the layout of an n-well microbolometer pixel, which measures 50x50μm^2. The n-well layer is surrounded by an opening area that allows silicon to be exposed for etching from the front side of the wafer. The openings are formed by placing the various CMOS layers on top of each other, including active, contact, via, and passivation opening layers, so that there is no need for any post-CMOS lithography step [6]. Electrical contact to the n-well layer is obtained using CMOS interconnect layers through the support arms.

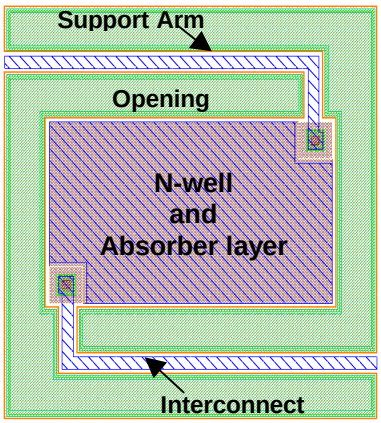

Figure 2. Layout of an n-well microbolometer pixel, which measures 50μmx50μm.

The performance of the n-well microbolometer is affected from a number of design parameters and material characteristics, including pixel size, fill factor, opening width, support arm width, interconnect layer on the support arms, and the absorber layer. In this study, the pixel size is selected as 50μmx50μm to be compatible with high-resolution imagers. This small size reduces the fill factor of the detector, since there is a minimum size requirement for the openings and arm widths. The support arms should be as long as possible and as thin as possible to reduce their thermal conductance. In addition, the materials on the support arms should have low thermal conductivity. The dielectric layer on the support arms, which protects the etching of the interconnect layer, has a very low thermal conductivity. However, the interconnect layer has a very high thermal conductance, and it determines the overall thermal conductance of the support arm.

There are two alternatives for interconnect layer: the metal and the polysilicon. The advantage of the metal layer is that it has a low electrical resistivity, reducing its noise contribution. However, the metal layer has a high thermal conductivity. In contrast, the polysilicon layer has high electrical resistivity, but low thermal conductivity. In this research, microbolometers with both type of interconnects are designed and evaluated, as will be explained later.

Another important consideration in the design is the absorbing layer. Since silicon is transparent to infrared radiation, an absorber layer is necessary on top of the n-well layer. There are detailed studies on the characterization of various absorber structures that can be formed using standard CMOS processes by placing various layers on top of each other [7, 8].

In this study, we have used oxide-metal1-passivation layers on top of the n-well as the absorber layer. Figure 3 shows the infrared absorption simulation result of the sandwich layer in our design obtained by using the Kidger Optics software. These results show that the absorptance is mostly in the 10-12μm band and reaches to 36% at 10.5μm wavelength, and the average absorptance is about 33% in the 8-14μm band.

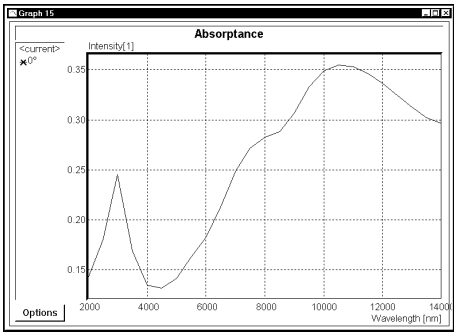

Figure 3. Absorptance of passivation-metal-oxide sandwich simulated by Kidger Optics software.

PERFORMANCE EVALUATION AND OPTIMIZATION

We have performed detailed thermal simulations using finite element modeling in the ANSYS program as well as analytical calculations in order to evaluate the performance of the n-well bolometers and to optimize the structure. Two different 0.8μm CMOS processes are considered for evaluation of test structures: MOSIS AMI and CMP AMS processes. Table 1 summarizes the typical process parameters for the various layers on these two processes. Table 2 shows thermal conductivity and heat capacity values of various CMOS layers used in thermal simulations in the ANSYS program.

Figure 4 shows the steady-state thermal ANSYS simulation result for the n-well microbolometer in the AMI process, where the interconnect layer is Metal1. This analysis is performed by assuming an input heat power of 2500W/m^2, which corresponds to 2.5μW power drop on the absorber area. This power increases the n-well temperature from 20°C to 20.75°C, suggesting that the total thermal conductance of the arms is 3.3x10^{-6}W/K. The thermal time constant of the structure is found to be

0.6msec, which is very low compared to other detectors. When the same structure is simulated with the polysilicon interconnect layer, the temperature increase becomes 5.28°C, suggesting that the thermal conductance of the arms decreases to 0.47×10^{-6}W/K, i.e., polysilicon interconnects provide a better thermal isolation. However, the thermal time constant for this structure increases to 5.3msec.

Table 1. Typical process parameters for the various layers on MOSIS AMI and CMP AMS 0.8 μm CMOS processes.

0.8 μm CMOS Process Parameters	Typical Values	
	MOSIS AMI	CMP AMS
Passivation Thickness (μm)	1	1
Total Oxide Thickness (μm)	0.5	2
Metal-1 Thickness (μm)	0.6	0.6
Poly Si Thickness (μm)	0.4	0.4
N-well Depth (μm)	3	3.5
N-well Sheet Resistance (Ω/sq)	900	1200
TCR of N-well (%/K)	0.75*	0.65

*TCR is measured 0.50%/K in the fabricated chip and 0.50%/K is used in the ANSYS simulations.

Table 2. Thermal conductivity and heat capacity values used in ANSYS simulations.

	Thermal Conductivity (W/mK)	Heat Capacity (J/cm^3K)
Nwell	140	1.63
Oxide	1.3	1.05
Nitride	1.5	2.7
Poly	18	1.6
Metal	181	Negligible

Considering the improvement on the thermal conductance, a second structure was designed with poly interconnects and sent to an AMS 0.8μm CMOS process for fabrication. Its pixel size is again selected as 50μmx50μm, but the fill factor in this design became 25%, due to the pixel select circuitry necessary for a focal plane array implementation. The ANSYS simulations show that the thermal time constant is 3.2msec and the temperature rise in the n-well is 2.34°C, suggesting that the total thermal conductance is 0.67×10^{-6}W/K.

Table 3 summarizes the performance simulation and calculation results of the two n-well micro-bolometers in AMI and AMS processes. The detector with polysilicon interconnect provides better performance, resulting in a responsivity of 4000 V/W, a D* of 1.2×10^{9}cmHz$^{1/2}$/W, and a thermal time constant of 3.2msec. It should be noted here that only the Johnson noise is considered for calculations since it is expected to be dominant for the n-well microbolometer. The responsivity, *R*, values are found using the following equation [3],

$$\Re = \frac{h a V_{app}}{G} \frac{R_b R_l}{(R_b + R_l)^2}$$

where, α is the TCR, G is the thermal conductance, η is the absorptance, R_b and R_l are the bolometer and load resistance, respectively, and V_{app} is the applied DC bias. R_l is selected to be equal to R_b and V_{app} is selected as 5 V.

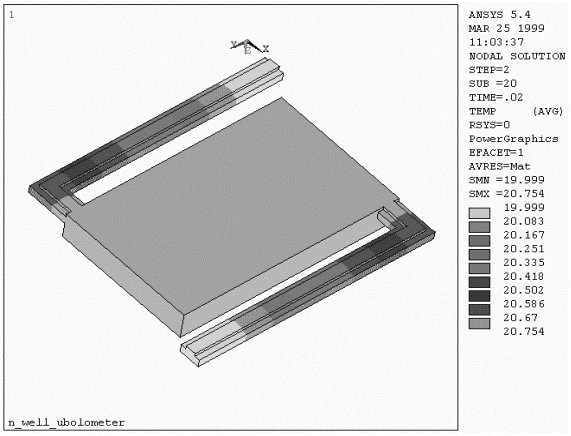

Figure 4. Steady-state thermal ANSYS simulation result for the n-well microbolometer.

Table 3. Performance simulation and calculation results of two n-well microbolometers

	MOSIS AMI	CMP AMS
Pixel Size (μm^2)	50x50	50x50
Fill Factor	40%	25%
Interconnect Material	Metal	Poly
Resistance @ 300K (kΩ)	1.33	4.43
Thermal Conductance (W/K)	3.3×10^{-6}	0.67×10^{-6}
Heat Capacitance (J/K)	2×10^{-9}	2.14×10^{-9}
Thermal Time Constant(msec)	0.6	3.2
Responsivity (V/W)	625	4000
D* (cmHz$^{1/2}$/W)	4.2×10^{8}	1.2×10^{9}

RESULTS AND DISCUSSION

N-well microbolometers with different sizes and structures were designed and sent to fabrication in two 0.8μm CMOS processes to verify their performance. The first chip was sent to MOSIS AMI process, and the second one is recently sent to CMP AMS process. Post-CMOS etching and measurement are performed on the first chip. The post-CMOS etching details are given in somewhere else [5], and it will not be repeated here in detail. Shortly, the etching is done at 80°C in a 10% TMAH solution. During the front-end bulk etching, etching of the aluminum pads is prevented by dissolving 36g/l silicon in the solution.

Figure 5 shows the SEM of the single pixel 50μmx50μm n-well microbolometer with a fill factor of 40% realized in the first chip. Figure 5 shows that the structure is suspended, i.e., the TMAH solution can etch through small openings of 4 μm. It should be noted here that the structure remains flat, suggesting that the composite passivation and interconnect layer on the arms are stress compensated. The TCR of n-well in this process was measured as 0.50%/K at 300K using a cryostat.

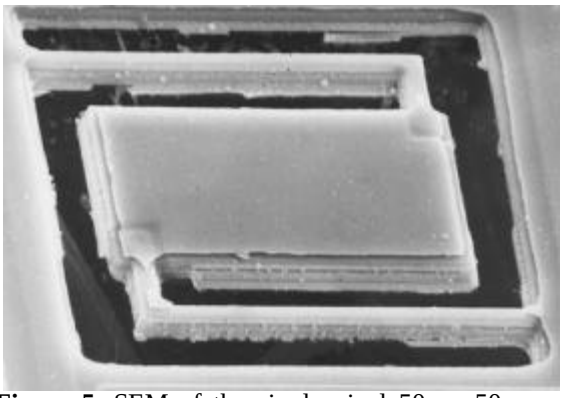

Figure 5. SEM of the single pixel 50μmx50μm n-well microbolometer with a fill factor of 40% realized in MOSIS AMI 0.8 μm CMOS Process.

The TCR of the n-well layer is low compared to that of the materials in the state-of-the-art detectors; however, n-well microbolometer performance is still comparable to other microbolometers, as shown in Table 4. It can be noticed that VO_x microbolometer has the highest responsivity, however, this responsivity cannot be utilized fully in 30 Hz frame rate applications due to its high thermal time constant. On the other hand, the n-well microbolometer is expected to have six times lower thermal time constant, even with the polysilicon interconnects, resulting in a comparable performance. The performance of the n-well microbolometer can be further improved with different structures, support arms, and absorbers.

Table 4. Comparison of the n-well microbolometer with the state-of-the-art microbolometers.

	Responsivity (V/W)	D* ($cmHz^{1/2}/W$)	Thermal Time Constant (msec)
VO_x[1]	$250x10^3$	$0.5\ x10^9$	20
SiC[2]	$4.8x10^3$	$0.8\ x10^9$	Not Available
Poly SiGe[3]	$28x10^3$	$2.26x10^9$	7.8
Metal (Pt)[4]	$1x10^3$	$0.05x10^9$	3
N-well *	$0.625\ x10^3$	$0.42\ x10^9$	0.6
N-well**	$4x10^3$	$1.2x10^9$	3.2

* The values are for the n-well bolometer structure with metal interconnects in the AMI process

** Expected performance of the n-well microbolometer with polysilicon interconnects in the AMS process.

CONCLUSIONS

This paper reports a new microbolometer structure that can be obtained in any standard CMOS process. The structure uses the n-well layer as the active element, which provides a TCR value of 0.50-0.75%/K depending on the process. The n-well layer is thermally isolated from the bulk-silicon by post-CMOS etching in TMAH solution together with electrochemical etch-stop. Detailed thermal simulations were performed using ANSYS program to optimize the structure and to estimate the performance. The simulation and fabrication results show that it is possible to implement low cost uncooled microbolometer in CMOS technology, where the detector can achieve a performance comparable to state-of-the-art microbolometers.

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