10
CMOS-based Thermal Sensors

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Abstract

This chapter presents various CMOS-based thermal sensors, including thermal radiation sensors, thermal converters, and thermal flow sensors. Two thermal radiation sensor approaches are described in detail: thermopiles and microbolometers. Thermopile-based uncooled infrared imaging arrays are relatively simple to implement and are low cost; however, their performances are limited. They typically have small responsivity (5–15 V/W), moderate noise equivalent temperature difference (NETD) values ($\sim$ 500 mK), large pixel sizes (pixel pitch of 100–400 μm), and small array sizes (typically 16×16 and 32×32). Microbolometer type uncooled infrared detectors have shown impressive developments in recent years. They are more expensive than thermopiles, however, much cheaper than cooled photon detectors, while approaching to their performances. Currently, there are microbolometer infrared cameras in the market with array sizes of 320×240, pixel sizes of 25 μm×25 μm, and NETD values smaller than 30 mK. There are also 640×480 format microbolometer array demonstrations with NETD values smaller than 50 mK. Efforts are continuing to reduce the prices of uncooled infrared detectors to widen their use in many commercial applications. CMOS-based thermal converters are used for true root mean square (RMS) voltage and ac signal measurements, independent of signal waveform. There are sensors reported to operate up to 1.2 GHz with a linearity error of less than 1%. Thermal flow sensors are used to measure the movement of a fluid (liquid or gas) by measuring either physical deflection, or heat loss, or pressure variation. Demonstrated sensors include a mass flow sensor that operates over the 1cm/s to 5m/s range and a wind sensor that can measure wind speeds up to 38 m/s.

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Thermal sensors; uncooled infrared detectors; microbolometers; thermopiles, infrared detectors; radiation sensors; flow sensors; thermal converters; thermal flow sensors.

10.1 Introduction

There are a number of thermal sensors based on the CMOS process, including thermal radiation sensors, thermal converters, thermal flow sensors, thermal pressure sensors, thermal acceleration sensors, resonant position sensors, chemical sensors, and sensors for determining thermal properties of materials [1]. Some of these sensors have already been covered in the previous chapters, including pressure sensors (see Chapter 6), acceleration sensors (see Chapter 3), chemical sensors (see Chapter 7), and sensors for determining thermal properties of materials (see Chapter 2). This chapter will summarize the state of the art in three CMOS-based thermal sensors, namely thermal radiation sensors, thermal converters, and thermal flow sensors. Section 10.2 will introduce thermal radiation sensors, explaining the differences between the cooled photon detectors and uncooled thermal infrared detectors. Two uncooled infrared detector approaches will be described in detail: thermopile-based radiation sensors and microbolometers. State-of-the-art in these approaches will be presented. Section 10.3 will summarize the work on thermal converters implemented with CMOS technology together with post-CMOS micromachining. Finally, Section 10.4 will summarize the state-of-the-art on CMOS thermal flow sensors.

10.2 Thermal Radiation Sensors

Infrared radiation is part of the electromagnetic spectrum with wavelengths above the visible spectrum, ranging from 1 μm to several tens of μm [2]. Detectors that can sense infrared radiation are called infrared detectors, while ensembles of in-

frared detectors in two-dimensional arrays are often called focal plane arrays (FPAs). Infrared detectors are used in many military and commercial applications such as night vision, mine detection, reconnaissance, fire fighting, medical imaging, and industrial control. Detectors for infrared imaging are sensitive in two regions of the infrared spectrum where the infrared transmission is allowed by atmosphere: the 3–5 μm wavelength region (mid wave infrared, MWIR) and the 8–12 μm wavelength region (long wave infrared, LWIR).

There are basically two types of detectors that can sense infrared radiation. The first type is photon detectors [3, 4], where the absorbed infrared photons generate free electron–hole (E–H) pairs, which are then collected by the application of an electric field for electronic processing. The second type of infrared detectors is known as thermal detectors [2], where the energy of the absorbed infrared photon raises the temperature of the detector, and the temperature-induced change in an electrical parameter is measured with the help of suitable circuitry.

Photon infrared detectors are fast, and their sensitivities are much higher than for thermal detectors, with noise equivalent temperature difference (NETD) values as low as 7–20 mK. However, the number of thermally generated E–H pairs at room temperature is much larger than the infrared-induced E–H pairs, which makes their use for infrared imaging impossible, unless they are cooled to cryogenic temperatures, i.e., 77 K or below. For this purpose, special and expensive coolers are used, increasing the size, cost, and operating power of the detector systems or cameras. Commonly used cooled (or photon) infrared detectors are fabricated using indium antimonide (InSb) [5], mercury cadmium telluride (HgCdTe or MCT) [6, 7], or quantum well infrared photodetector (QWIP) [8–10] technologies. InSb detectors are used in the 3–5 μm wavelength range, while MCT and QWIP can be used in both 3–5 and 8–12 μm wavelength ranges. The fabrication of these detectors involves complicated processing steps, owing the known difficulties of handling low-bandgap materials required for the detection of low-energy infrared photons. Therefore, the cost of the photonic detectors and infrared cameras using these detectors is very high (typically $50 000–150 000), finding application areas only in expensive weapon platforms, in astronomical observation instruments or in special medical instruments, where the performance is the primary issue. On the other hand, infrared cameras using thermal detectors are small in size, consume less power and are less expensive (typically $8000–15 000 for 320×240 arrays), making them the ideal choice for applications which require high unit numbers with relatively lower performance. There are continuing efforts to decrease the cost of uncooled detectors to much lower values (such as $50–500) while achieving reasonable performance. The next section explains the principles of thermal detectors.

10.2.1
Thermal (Uncooled) Infrared Detectors

Thermal or uncooled infrared detectors sense the change in an electrical parameter with change in the device temperature related to the amount of absorbed infrared energy. Therefore, the thermal detection mechanism is an indirect means of infra-

red detection, and the response times of these detectors are longer than those of photon detectors. In most cases, the signal-to-noise ratio and detectivity of the uncooled thermal detectors are lower than those of cooled photon detectors. Therefore, the performance of thermal detectors is in general lower than that of cooled photon detectors. It should be mentioned that photon detectors are usually implemented as linear arrays (such as 240×1 or 240×4) that are scanned optically, while thermal detectors are implemented as 2-D staring arrays (such as 320×240). Since the electrical bandwidth of staring arrays is much lower than that of scanned arrays, it is possible to improve the signal-to-noise ratio of the thermal detectors when operated in staring arrays. Further, it is easier to fabricate staring arrays using thermal detectors than arrays that use cooled photon detectors. Furthermore, at scanning speeds close to the TV frame rate (30 frames/s), the performance degradation of the thermal detectors due to their relatively longer thermal time constants can be minimized by proper detector design. Considering these factors, although cooled detector arrays still provide better performance, the performance difference between thermal and cooled photonic detectors becomes smaller than expected by just comparing them on a pixel basis [2].

The most important advantage of thermal detectors is that they can operate at room temperature without requiring any complex and expensive cooling equipment. The resulting infrared imaging systems utilizing uncooled detector technology have much smaller size, lower cost, lower power consumption and extended operation durations. Owing to these advantages, uncooled detectors are used in many military and commercial applications, such as night vision, mine detection, driver night vision enhancement, fire fighting and industrial control applications. Wide application areas have made uncooled infrared technology a highly requested technology, and there is a worldwide effort to implement high-performance and low-cost uncooled infrared detector arrays. There are already infrared cameras on the market using 320×240 format detector arrays with 50×50 μm and 25×25 μm pixel sizes and with noise equivalent temperature differences (NETD) better than 30 mK [11–13]. The uncooled technology has also demonstrated uncooled FPAs with a 640×480 array format with 25×25 and 28×28 μm pixel sizes and NETD values lower than 50 mK [14–17]. The target of uncooled technology is to fabricate detectors with less than 25×25 μm pixel size and with NETD values better than 10 mK [2], i.e., performances similar to that of cooled detectors. Therefore, as the uncooled technology develops, many other infrared imaging systems that currently use cooled infrared detector arrays may start using uncooled detector arrays. The cooled photonic detectors, on the other hand, may find future application areas in more sophisticated and expensive infrared imaging platforms requiring even higher performance with added new features such as multi-spectral and/or multi-color infrared radiation sensing capability, possibly achieved using the rapidly developing QWIP technology.

10.2.2 Types of Thermal (Uncooled) Infrared Detectors

There are two major types of thermal radiation sensors based on post-CMOS fabrication approaches (see Chapter 1): thermopile sensors and microbolometers. Thermopile sensors are mostly based on bulk micromachining of the CMOS-processed wafers, whereas microbolometers are mostly based on surface micromachining of the CMOS-processed wafers. There are also recent examples of microbolometers which are implemented with post-CMOS bulk micromachining. Additional types of thermal detectors include electro-junction devices, where the absorbed infrared energy causes bending of a surface micromachined cantilever beam, changing the capacitance of the pixel [18, 19].

Most of the advances in thermal or uncooled infrared technology have been achieved with microbolometer technology. Although this technology is already much cheaper than photon detector technology, the fabrication and system costs are still high for many commercial applications, resulting in a worldwide effort to decrease further the cost of uncooled technology to enter the low-cost, high-volume markets where the system costs of $50–500 are required. Apart from decreasing cost of detector fabrication, there are other key issues to achieve these system costs, including wafer level vacuum packaging of the detectors, their wafer level testing, and the use of low-cost infrared optics. The following sections provide further details on the CMOS-compatible thermal radiation sensors.

10.2.2.1 Thermopile-based Radiation Sensors

Thermoelectric detectors are formed using thermocouples, whose operation principle is based on the Seebeck effect. Fig. 10.1 shows a schematic of a thermocouple. When two pieces of different materials A and B are joined and heated at one end, there will be a self-generated potential difference between the two other ends of the structures depending on the difference of the two material's Seebeck coefficients and the temperature difference between the hot and cold end points.

The output voltage of a thermocouple, V_{AB}, is given as [20–23]

$$V_{AB} = \alpha_{AB}\Delta T_{hot-cold} = (\alpha_A - \alpha_B)(T_{hot} - T_{cold}) \quad (1)$$

where α_A and α_B are the Seebeck coefficients of the two different materials, α_{AB} is the Seebeck coefficient of the thermocouple, T_{hot} and T_{cold} are the temperatures of the hot and cold junctions, respectively, and $\Delta T_{hot-cold}$ is the temperature difference between the hot and cold junctions. The output voltage of a single thermocouple is usually not sufficient; therefore, a number of thermocouples are connected in series to form a so-called thermopile. Fig. 10.2 shows a thermopile that is constructed by series connection of five thermocouples. The thermopile can be used as an infrared detector if the thermocouples are placed on a suspended dielectric layer and if an absorber layer is placed close to or on top of the hot contacts of the thermopile. Fig. 10.3 shows a perspective view of this arrangement.

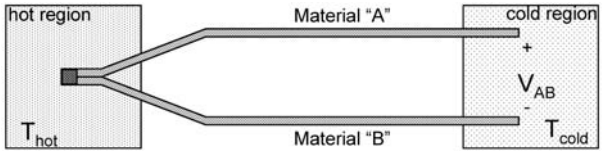

Fig. 10.1 Schematic of a thermocouple. The self-generated voltage V_{AB} at the open ends of the thermocouple is called the Seebeck voltage

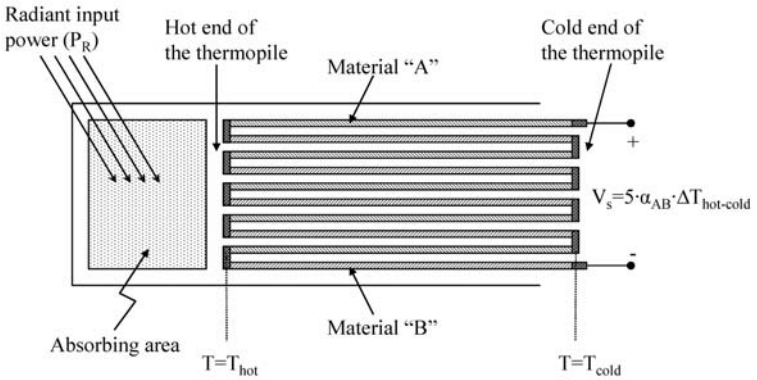

Fig. 10.2 Thermopile consisting of five series-connected thermocouples. The thermopile can be used as an infrared detector if the thermocouples are placed on a suspended and thermally insulating dielectric layer and if an absorber layer is placed close to the hot contacts of the thermopile

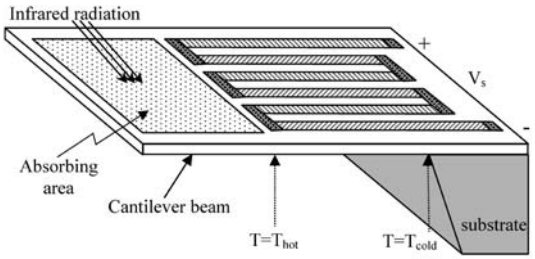

Fig. 10.3 Perspective view of a thermopile that can be used as an infrared detector. Thermocouples are placed on a dielectric cantilever beam and an absorber layer is placed on the tip next to the hot junction

An important factor for obtaining a large output voltage from a thermopile is to obtain a high thermal isolation in order to maximize the temperature difference between hot and cold junctions, $\Delta T_{hot-cold}$, for a specific absorbed power. To achieve this thermal isolation between hot and cold junctions, the thermocouples are often placed on top of dielectric diaphragms where the silicon underneath is removed to increase the thermal resistance. Of course, the layers that are used for

Tab. 10.1 Seebeck coefficients and thermal conductance values of various materials [ref.?]#Q5#

Material	*Seebeck coefficient (at 273 K) (μV/K)*	*Thermal conductance (W/K m)*
Aluminum	–1.7 [a)]	237
Chromium	18.8	
Gold	1.79	318
Copper	1.70	
Platinum	–4.45	
Nickel	–18.0	90
Bismuth	–79 [b)]	
Antimony	43 [b)]	
p-Type silicon	300 to 1000 [a)]	149
n-Type polysilicon	–200 to –500 [a)]	

a) At 300 K.
b) Averaged over 0 to 100 °C.

the thermocouples also contribute to the thermal conduction between the hot and cold junctions, and their contribution to the thermal conduction should be minimized for better performance (see figure of merit).

Thermopiles can be constructed using semiconductors and/or metals. Tab. 10.1 lists Seebeck coefficients and thermal conductance values of various materials. Since the Seebeck coefficients of semiconductors are larger than that of metals, semiconductor thermopiles are more responsive than their metal counterparts [20–30]. The Seebeck coefficient of semiconductor materials depends on the variation of the Fermi level of the semiconductor with respect to temperature; therefore, for semiconductor thermopiles, the magnitude and sign of the Seebeck coefficient can be adjusted by adjusting the doping type and doping level. The following equation can be used to estimate the Seebeck coefficient of silicon as a function of its electrical resistivity at room temperature [21]:

$$\alpha_s = \pm 0.216 \times 10^{-3} \ln(\rho/\rho_0) \tag{2}$$

where ρ is the resistivity of silicon in ohm cm and $\rho_0 \approx 5 \times 10^{-4}\ \Omega$ cm. Here, α_s is given in V/K, and a positive sign is selected for p-type silicon, whereas a negative sign is selected for n-type silicon. Equation 10.2 suggests that the Seebeck coefficient of a semiconductor increases in magnitude with increased resistivity, and therefore, with decreased doping level. However, a thermopile material with very low electrical resistivity is not necessarily the best choice for a particular infrared detector, as the Seebeck coefficient is only one of the parameters influencing its overall performance. The next section explains the parameters that are important for selection of a material for thermopiles.

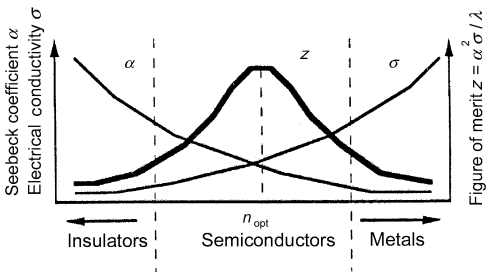

Fig. 10.4 Thermoelectric properties of metals, semiconductors and insulators [33]

Figure of Merit for Thermocouples

An ideal thermocouple material for infrared detector applications should have a very high Seebeck coefficient, a very low thermal conductance, and very low noise. These parameters are usually conflicting, and a figure of merit, z, is defined for the performance of a particular thermocouple material [31, 32]:

$$z = \frac{\alpha^2}{\rho\kappa} \tag{3}$$

where α is the Seebeck coefficient, κ is the thermal conductivity, and ρ is the electrical resistivity. The figure of merit for a thermocouple increases if materials with high Seebeck coefficients (α) and low thermal conductivities (κ) are used. Other than these two parameters, the electrical resistivity (ρ) should also be taken into account when choosing a thermocouple material, since Johnson noise is generated by the finite electrical resistance of the thermocouple structure. The Johnson noise, which is also called thermal noise, limits the minimum detectible temperature difference with the thermocouple. The Johnson noise voltage (V_N) for a resistor is defined as follows:

$$V_N = \sqrt{4kT\Delta f R_{el}} \tag{4}$$

where k is Boltzmann's constant (1.381×10^{-23} J/K), T is the temperature in K, Δf is the bandwidth in Hz, and R_{el} is the electrical resistance in Ω. For a thermocouple, a low amount of Johnson noise voltage is required. To decrease the Johnson noise, the electrical resistance, R_{el}, should be decreased. Since R_{el} is proportional to ρ, the thermocouple materials should be chosen from low-resistivity materials. However, as mentioned previously, a lower ρ value also gives a lower Seebeck coefficient. Therefore, an optimum point needs to be determined considering all these parameters based on the figure of merit defined above. Fig. 10.4 shows a graph for the visual interpretation of the figure of merit concept [33]. As can be seen, an optimum value for the figure of merit is achieved for semiconductors at a specific doping level n_{opt}. This doping value is around 10^{19} cm^{-3} for both single-crystal silicon and polysilicon materials.

Tab. 10.1 also lists the thermal conductance values of some of the materials used in CMOS thermopiles. It should be noted that when the number of thermo-

couples is increased to obtain a high output voltage, it also increases the thermal conduction between the hot and cold junctions and the series electrical resistance (and therefore the Johnson or thermal noise). This means that increasing the number of thermocouples does not necessarily increase the performance after a certain number of thermocouples and that care should be taken when determining the optimum number of thermocouples for a thermopile.

Equation 10.3 is valid for a single thermocouple material. The figure of merit for a thermocouple constructed with two different materials, A and B, having a relative Seebeck coefficient α_{AB}, is defined as follows [31–34]:

$$z = \frac{\alpha_{AB}^2}{\left(\sqrt{\rho_A \kappa_A} + \sqrt{\rho_B \kappa_B}\right)^2} \tag{5}$$

where ρ_A and ρ_B are electrical resistivity of the materials A and B, respectively, in Ω m, and κ_A and κ_B are the thermal conductivity of the materials A and B, respectively, in W/m K.

There are a number of materials that provide very high figures of merit, such as Bi–Te, Bi–Sb–Te, and Pb–Te, and there are thermopile arrays that use some of these materials [35, 36]; however, these materials are not readily available in a CMOS technology. In a CMOS technology, polysilicon is readily available, but polysilicon has a small figure of merit compared with the above materials. Furthermore, in a standard CMOS process, there is only one type of polysilicon (usually n-type), and the other material used to make a thermopile is usually aluminum, which has a very low Seebeck coefficient. Although n-polysilicon/aluminum thermopiles are widely used to implement thermopiles in a standard CMOS process, there are also other options, as described in the next section.

Thermocouple Options in CMOS

There are limited number of layers available as thermocouple materials in CMOS technology. If a standard CMOS process is used for making thermocouples, doping levels, thickness values, and thermal conductivity values of these layers cannot be changed. One should consider the available layers and their thermocouple parameters and decide among various thermocouple options. Fig. 10.5 shows perspective views of four different thermocouple options and approaches used for implementing thermopiles in standard CMOS processes. The most widely used approach is n-poly/aluminum thermopiles [27, 37–39]. Although aluminum has a very low Seebeck coefficient, this approach is used widely, as it is easy to implement with post-CMOS processes. The approach in Fig. 10.5 (b) is better in terms of Seebeck coefficient, as the p^+-active layer, i.e., the p^+-source/drain implantation, provides a higher Seebeck coefficient than n-poly [40, 41]. However, the p^+-active layer is protected inside an n-well during etching and this reduces the thermal isolation between the hot and the cold junction, reducing the overall performance of the thermopile. The third approach, shown in Fig. 10.5 (c), is very attractive, as it provides relatively very high thermocouple coefficients, α_{AB}, with the use of p-poly/n-poly thermocouples [22, 26, 28, 29, 42]

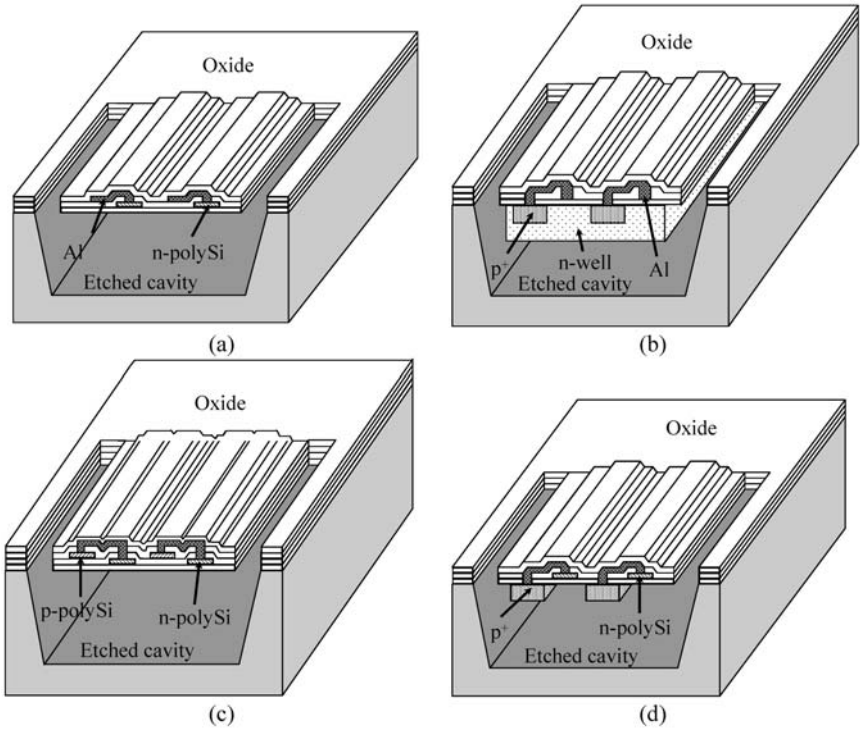

Fig. 10.5 Perspective views of four different approaches used for implementing thermopiles in standard CMOS processes: (a) n-poly/aluminum; (b) p^+-active/aluminum; (c) p-poly/n-poly; (d) n-poly/p^+-active

and is easy to implement during post-CMOS processes [similar to Fig. 10.5 (a)]. However, p-poly is not available in most of the standard CMOS processes, and therefore, implementing p-poly/n-poly thermocouples is not possible in most of the standard CMOS processes. The fourth approach, shown in Fig. 10.5 (d), uses n-poly/p^+-active thermocouples [30], maximizing the overall thermocouple Seebeck coefficient. Post-CMOS fabrication steps are slightly more complicated than (a) and (c); however, it can be implemented in any standard n-well CMOS process. Fig. 10.6 shows an SEM photograph of a semiconductor thermopile structure implemented using 20 n-poly/p^+-active thermocouples in a standard n-well CMOS process [30].

Absorber layers are necessary for thermal detectors, as silicon and most of the detector materials are transparent to infrared radiation. There are various layers in literature that are used as absorber layers, such as Gold Black, Titanium, and Titanium Nitride. However, it is also possible to use the standard layers in CMOS as absorbers [43, 44], where it is possible to obtain absorbance of 30–70% in 8–12 μm wavelength regions.

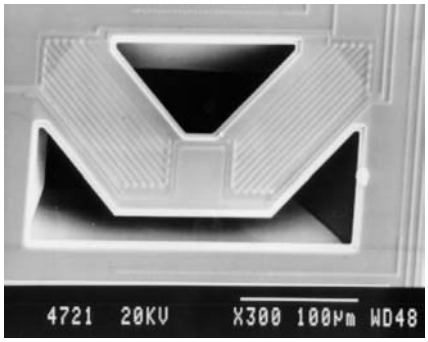

Fig. 10.6 SEM photograph of a semiconductor thermopile structure implemented using 20 n-poly/p^+-active thermocouples (10 on each arm) in a standard n-well CMOS process [30]. The structure measures 325 µm× 180 µm in a 1.2 µm CMOS process.

Thermopile Imaging Arrays

Thermopiles are widely used as single elements in a number of applications, mostly as single-point detectors, but array implementations of thermopiles are limited, mainly owing to the large pixel size required for implementing each thermopile pixel. There are some successful focal plane array (FPA) implementations merged with CMOS readout electronics [26–29, 42].

Researchers at the University of Michigan demonstrated a 32×32 FPA implemented with 32 n-poly/p-poly thermocouples on dielectric diaphragms [26]. The pixel size is 375 µm×375 µm with an active area of 300 µm×300 µm, i.e. with a fill factor of 64%. The FPA has a responsivity of 15 V/W and a D^* of 1.6×10^7 cm/Hz$^{1/2}$/W. The etching is mainly done from the back side of the wafers, but small etch-cavities are also placed on the front-site of the wafers to achieve heat sinks between the pixels, to prevent the heating of the cold junction and to achieve thermal isolation between adjacent pixels. The process is based on an in-house 3 µm CMOS process, but it is customized to accommodate dielectric window deposition and to implement n-poly and p-poly thermocouples.

Researchers at ETH Zurich also developed thermal imager FPAs using bulk micromachining of CMOS processed wafers [27, 28]. The group first demonstrated a 10×10 FPA with 12 n-poly/aluminum thermocouples that provide a Seebeck coefficient of 108 µV/K. The pixel size is 250 µm×250 µm. The FPA has a measured responsivity of 5.83 V/W and a D^* of 1.5×10^7 cm/Hz$^{1/2}$/W. The noise-equivalent-temperature difference (NETD) of the FPA is reported to be 530 mK with a low-cost polyethylene Fresnel lens. The FPA is fabricated by back-side etching of the CMOS wafers and stopping at large dielectric diaphragms. The thermal isolation between pixels is achieved by using 25 µm thick and 80 µm wide gold lines on top of the membrane. The group also achieved a 16×16 FPA with the same approach [22] and demonstrated thermal images, as shown in Fig. 10.7.

An interesting array implementation uses post-CCD surface micromachining to implement a 128×128 thermopile array [29]. Each thermopile pixel in the array has 32 pairs of p-type polysilicon and n-type polysilicon thermocouples, and the pixel size is 100 µm×100 µm with a fill factor of 67%. The reported NETD for this array is 0.5 K with f=1 optics. Although these performances are very good for

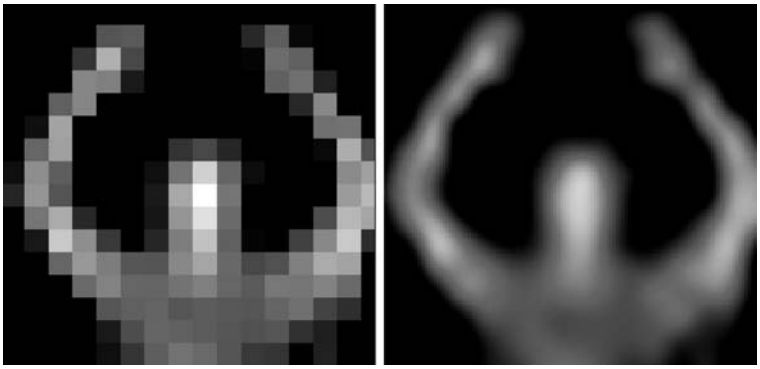

Fig. 10.7 Thermal image of a person, acquired with a 16×16 thermal imager developed at ETH Zurich: (a) unprocessed image; (b) the same image after cubic spline interpolation between pixels. After [22] with permission of the author

a thermopile FPA, the FPA requires vacuum packaging for operation, increasing its cost. Further, CCD technology is not as widespread a technology as CMOS.

Another example of large-format FPA with thermopiles was recently presented by the Nissan Research Center [42]. The FPA has a 120×90 format, and it is monolithically integrated with a CMOS process. Each detector consists of two pairs of n-poly/p-poly thermocouples with a pixel size of 100 μm×100 μm, and front-end bulk-etching is used to thermally isolate the detectors. With vacuum packaging and a precisely patterned Au-black absorbing layer, the detectors provide a responsivity of 3900 V/W after amplification of 2000 V/W. The thermopiles are monolithically integrated with a 0.8 μm CMOS process, but seven special processes are added to the CMOS process, making it a custom-made CMOS process.

The uncooled infrared detectors implemented with thermopiles have an important advantage, as they do not require temperature stabilizers, owing to their inherent differential operation between hot and cold junctions [23]. However, the temperature gradient in the thermopile array may cause significant offsets; therefore, spatial variation in the array temperature should be minimized by careful array design. In one application it has been reported that the heat generated by the on-chip preamplifiers causes noticeable offset in the thermopile outputs [22]. Furthermore, the responsivity of the thermopiles is very low, of the order of 5–15 V/W, and the pixel sizes in these devices are large, such as 250 μm×250 μm, limiting their use for large format detector arrays. Furthermore, these detectors require extra processing for thermal isolation between pixels, such as processing steps to obtain silicon islands [22, 26] or electroplated gold lines [22, 23]. Although there are successful implementations of CMOS thermopile arrays, their low responsivity values and large pixel sizes limit their performance and application areas. These limitations prevent the use of thermopiles for infrared imagers that require large FPAs, and the attention on uncooled infrared detectors has shifted to microbolometers.

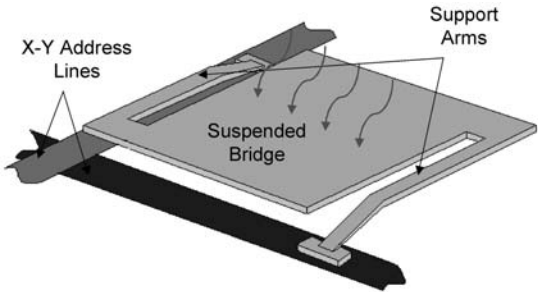

Fig. 10.8 Simplified perspective view of a microbolometer structure obtained using surface micromachining techniques. After [2]

10.2.2.2 **Microbolometers**

One of the most widely used approaches for uncooled infrared imaging is to use resistive microbolometers implemented using surface micromachined bridges on CMOS-processed wafers [14, 46–55]. Fig. 10.8 shows a simplified perspective view of a microbolometer structure obtained using surface micromachining techniques [2]. Infrared radiation increases the temperature of a material on the thermally isolated and suspended bridge, causing a change in its resistance related to its TCR value. The performance of resistive microbolometers depends on both the temperature sensitive layer along with its thermal isolation and the quality of the readout circuit.

The surface micromachining technique allows the deposition of temperature-sensitive layers with very small thickness, very low mass, and very good thermal isolation on top of bridges over the readout circuit chips. With the removal of the sacrificial layers between the bridge structures and readout circuit chip, suspended and thermally isolated detector structures are obtained, assuming vacuum packaging. There are a number of uncooled infrared cameras on the market with pixel sizes of 50 μm×50 μm and array formats of 320×240, and these cameras provide a noise equivalent temperature difference (NETD) better than 100 mK. At the research level, there are uncooled detector FPAs with pixel sizes as small as 25 μm×25 μm allowing very large format FPAs such as 640×480 to be implemented. The goal is to reach NETD values lower than 10 mK for these large-format FPAs. Therefore, as the uncooled technology develops, many other infrared imaging systems that currently use cooled infrared detector arrays may start to use uncooled detector arrays.

Today's achievements on uncooled infrared technology were initiated by the US Department of Defense in the 1980s, when it gave large classified contracts to both Honeywell and Texas Instruments (TI) to develop two different uncooled infrared technologies [2]. Texas Instruments concentrated on pyroelectric technology [45], whereas Honeywell concentrated on microbolometer technology [46, 47], and they both successfully developed uncooled infrared 320×240 format FPAs. These technologies were unclassified in 1992, and since then many other companies have started working in this technology. These companies include Raytheon [11, 15, 48], BAE (formerly Honeywell) [14], DRS (formerly Boeing) [17, 49], Sarcon [18, 50], Indigo [51, 52], and InfraredVision Technologies [53] in the USA, INO in Canada [54], ULIS in France [55, 56], NEC [57, 58] and Mitsubishi [59–61] in Ja-

pan, QuinetiQ [62], in the UK, and XenICs in Belgium [63]. There are also many research institutions working on microbolometer-based uncooled infrared arrays, such as LETI LIR in France [64, 65], IMEC in Belgium [63, 66], University of Texas, Arlington [67–69] and University of Michigan [70] in the USA, KAIST in Korea [71, 72], and METU in Turkey [73–77].

The main advantage of microbolometers over pyroelectric infrared detectors is that they can be monolithically integrated with a CMOS readout circuit. Most of the microbolometers use resistive approaches combined with surface micromachining technology, i.e., the microbolometers are formed using a material with high temperature coefficient of resistivity (TCR) deposited on a suspended and thermally isolated bridge, as shown in Fig. 10.8.

There are efforts to implement resistive surface micromachined microbolometers using many different materials, such as vanadium oxide (VO_x) [11–17, 46–49, 51–54, 57, 58, 80], amorphous silicon (a-Si) [55, 56, 64, 65, 81], polycrystalline silicon-germanium (poly-SiGe) [63, 66], yttrium barium copper oxide (YBaCuO) [59, 67–69], and metal films [62, 71, 72, 78, 79].

Vanadium oxide is the most widely used material, and it has a high TCR value of 2–3%/K. The main drawback of VO_x is that it is not compatible with a CMOS line and requires a separate fabrication line after the CMOS process to prevent contamination of the CMOS line. In addition, VO_x exhibits large $1/f$ noise due to its non-crystalline structure, limiting its performance. Nevertheless, there are a number of companies fabricating large-format and very high-performance FPAs based on VO_x under license from Honeywell, including Raytheon (formerly Hughes), DRS (formerly Boeing and Rockwell), BAE (formerly Lockheed Martin and Loral), Indigo Systems, InfraredVision Technology, and NEC. Currently, there are large-format FPAs such as 640×480 available with a pixel pitch of 28 or 25 μm using a conventional simple deck structure. Some companies have managed to reduce the pixel pitch to 25 μm for their 640×480 and 320×240 FPAs with the use of double deck structures, first presented by researchers at KAIST [71, 72] in 1998. Fig. 10.9 shows a cross-sectional view of a double deck structure, which is used to obtain a high fill factor in a smaller pixel area [71, 72].

Outstanding performance has been demonstrated with the uncooled technology, with performances close to those of cooled infrared detectors at much lower cost. Fig. 10.10 shows an image taken by the camera developed by Raytheon based on their 640×480 pixel VO_2 FPA, showing excellent resolution and image quality [80]. However, the cost of detectors are still very high for many commercial applications.

Another material that is used successfully to implement high-format FPAs is a-Si, which is a CMOS line compatible material. Detectors with a-Si have been developed by CEA/LETI and transferred to ULIS to implement large-format FPAs such as 320×240 with a pixel pitch down to 35 μm while providing an NETD of 36 mK [55]. Fig. 10.11 (a) shows SEM photographs of an a-Si surface micromachined microbolometer detector array from the top, and Fig. 10.11 (b) shows a zoomed view of the pixel support arm structure [55]. This figure shows that it is possible to implement very thin layers with a-Si, allowing short arms to be made. Raytheon is also developing a-Si-based uncooled infrared FPAs [81].

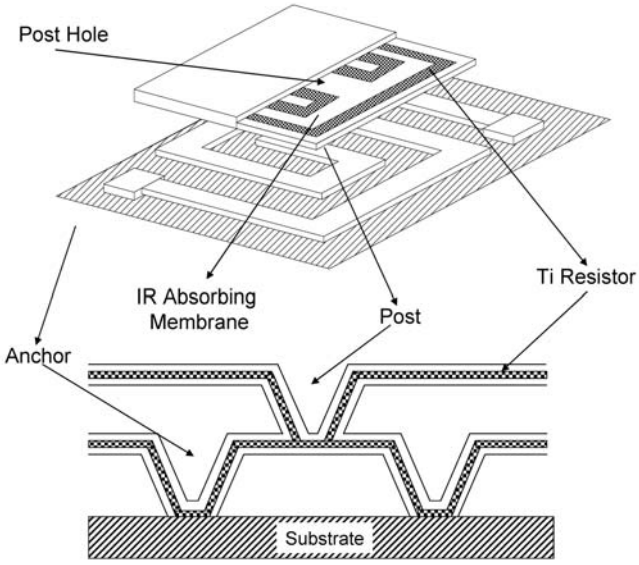

Fig. 10.9 Cross-sectional view of a double deck structure, which is used to obtain a high fill factor in a smaller pixel area. After [72]

Fig. 10.10 An image taken by the camera developed by Raytheon based on their 640 × 480 pixel VO_2 FPA, showing excellent resolution and image quality. After [80]

Poly-SiGe is also used for uncooled resistive microbolometers, as it provides a TCR of 2–3%/K. This material was developed by IMEC, Belgium, and subsequently the technology was transferred to XenICs, Belgium. This material needs to be deposited at high temperatures; therefore, it is not easy to integrate with CMOS. A large effort

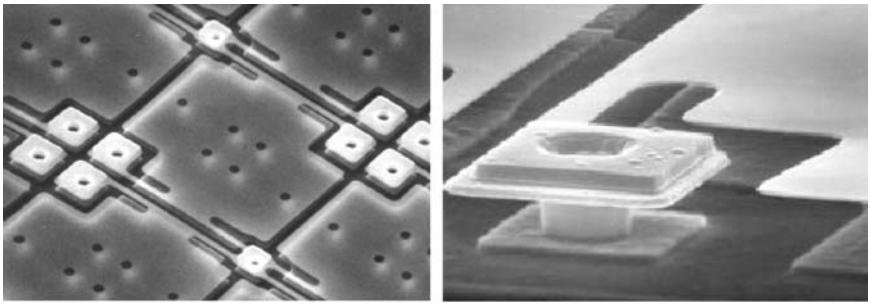

Fig. 10.11 SEM photographs of a-Si surface micromachined microbolometer detectors: (a) top view; (b) zoomed view of the pixel support arm structure [55]

was made to decrease the deposition temperature to a level that allows its monolithic integration with CMOS. Another problem is the internal stress of the deposited films, making the deposited films buckle. Nevertheless, XenICs has managed to develop 200×1 and 14×14 detector arrays [63]. However, this material exhibits high $1/f$ noise owing to its non-crystalline structure, and it also requires complicated post-CMOS processing to reduce the effects of residual stress.

Another high-TCR material that is used for resistive microbolometer development is YBaCuO [59, 67–69]. This material is attractive as it is deposited at room temperature, and it has low $1/f$ noise. There are efforts at the research level to implement YBaCuO detectors in various substrates, mainly at the University of Texas, Arlington [69], and formerly at Southern Methodist University [67, 68]. A large-format FPA implementation using YBaCuO has been demonstrated by Mitsubishi. A 320×240 format FPA with a 50 μm pitch was demonstrated, and this FPA provides an NETD of 80 mK [59].

There are also efforts to implement resistive microbolometers using metals with the motivation that they are CMOS compatible and their deposition does not require any high-temperature process. However, metal microbolometers have low performance due to the low TCR values of metal films. The most widely used metal for resistive microbolometers is titanium, which has a reported TCR of 0.26%/K when deposited as a thin film [72]. QinetiQ (UK) is currently developing resistive microbolometers [62] based on titanium, where the array size is selected as 64×64 for commercial applications with a pixel size of 75×75 μm. Since the production is done in a commercial CMOS foundry (XFAB), the production costs for these detectors are predicted to be below $100; however, the performance of the detectors is relatively low and the detectors heat up by about 10–20 °C when biasing them to read out their resistance change, decreasing their dynamic range. The use of metals does not bring much advantage compared with post-CMOS processes, and therefore, it is very difficult for metal microbolometers to compete with high-TCR and CMOS line compatible materials, such as a-Si.

All of the surface micromachined resistive bolometers require post-CMOS material deposition and etching steps, as well as a number of high-precision lithography

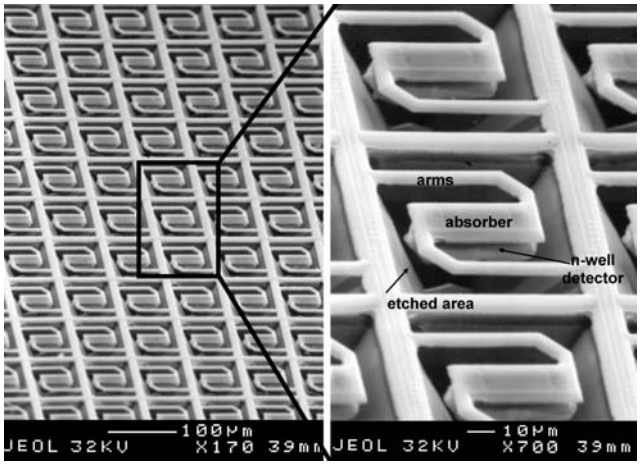

Fig. 10.12 SEM photograph of a fabricated and post-processed array die verifying that all n-well structures are suspended and none of the support arms are broken. The suspended structures remain flat without any extra stress-reducing process steps after CMOS fabrication

steps. An alternative to these approaches was proposed by METU [73], where a resistive microbolometer FPA was demonstrated using the CMOS n-well as the bolometer material, which has a moderate TCR of 0.5–0.7%/K. Fig. 10.12 shows an SEM photograph of a fabricated and post-processed array die verifying that all n-well structures are suspended, and none of the support arms are broken. The suspended structures remain flat without any extra stress-reducing process steps after CMOS fabrication. The pixel size is 80 μm×80 μm, and the fill factor is only 13% owing to large openings required to access silicon for etching after the CMOS process. In addition, the effective pixel TCR is reduced to 0.26%/K owing to the diode implemented within each pixel for easy readout and to the use of polysilicon in the arms to achieve larger thermal isolation. These limitations prevent the implementation of larger FPAs with this approach. The same group demonstrated later that it is possible to reduce the pixel size to 40 μm×40 μm while increasing the fill factor to 44% [74]. The performance of the detectors is increased by implementing the microbolometers using suspended diodes, instead of resistors.

Fig. 10.13 shows the post-processing steps used for implementing (a) resistive-type and (b) diode-type n-well microbolometers. In resistive n-well microbolometers, a number of layers of the CMOS process are removed by proper design in order to obtain openings to the silicon substrate for subsequent post-CMOS bulk etchings while using electrochemical etch-stop in TMAH. This approach requires the openings in the arms to be more than 10 μm to allow etching of the extra metals in these openings, especially in sub-micron CMOS technologies. A different approach is used for diode microbolometers, as shown in Fig. 10.13 (b), to reach silicon for post-CMOS anisotropic wet etching. Here, an additional RIE (reactive ion etching) step is included before the bulk micromachining. During RIE,

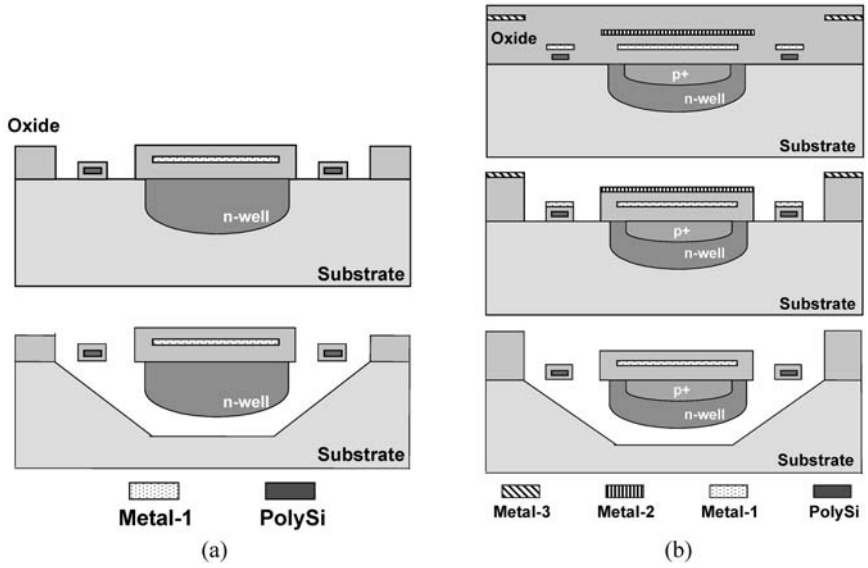

Fig. 10.13 The post-processing used for implementing (a) resistive-type and (b) diode-type n-well microbolometers [74]

CMOS metal layers are used as etch masks to eliminate any critical lithography step after CMOS [101] while achieving narrow etch openings of about 1.2 μm between the support arms. After RIE, the masking metal layers are removed, and then, the bulk silicon underneath the detector is removed while protecting the n-well layer using an electrochemical etch-stop technique in TMAH. This approach was used to implement 64×64 [75] and 128×128 [77] FPAs using a commercial 0.35 μm CMOS process. Fig. 10.14 shows SEM photographs of the fabricated de-

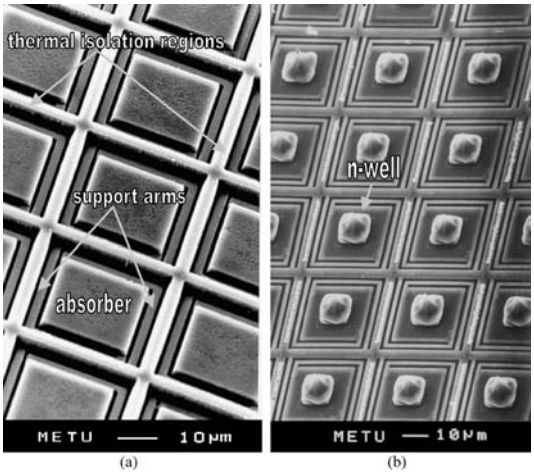

Fig. 10.14 SEM photographs of the fabricated detector array pixels after post-CMOS processing: (a) top view; (b) bottom view after removing pixels from the substrate using a sticky tape [75, 76]

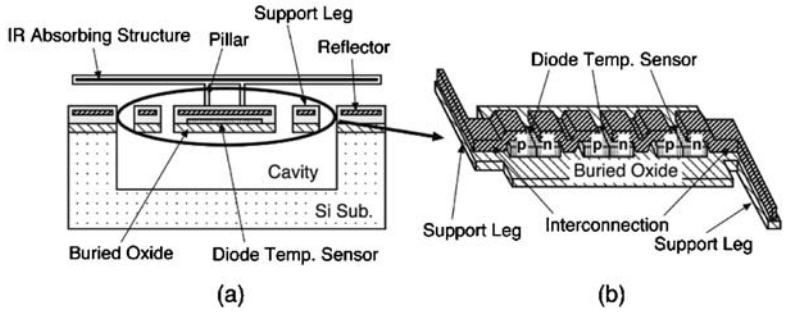

Fig. 10.15 SOI diode microbolometer: (a) schematic of the detector cross-section and (b) schematic of SOI diode-array pixels [28]. Reproduced with permission from the author

tector array pixels after post-CMOS processing: (a) top view and (b) bottom view after removing pixels from the substrate using a sticky tape [75, 77]. The expected NETD values for these arrays are 0.8 and 1 K for 64×64 and 128×128 arrays, respectively, but it is expected to reduce the NETD values to 0.3 K, which is sufficient for a number of low-cost infrared imagers. In comparison with CMOS thermopiles, this approach seems attractive as it allows the implementation of a much smaller pixel and much higher FPA format, while providing similar NETD performances. The performance of diode-based CMOS microbolometers can be increased by connecting a number of suspended diodes in series.

Series-connected diode microbolometers were successfully developed by Mitsubishi using a custom SOI CMOS technology [60]. Fig. 10.15 (a) and (b) show a schematic of the detector cross-section and schematic of SOI diode-array pixels, respectively. Arrays consisting of 320×240 FPA pixels are based on suspended multiple series diodes with 40 μm×40 μm pixel sizes on silicon on insulator (SOI) wafers. The reported NETD value is 120 mK for *f*/1 optics at a scanning rate of 30 frames per second (fps). The pixel structure and the fabrication process of the diode detector FPAs have been changed to increase the fabrication yield. Fig. 10.16 shows the modified fabrication steps and final cross-sectional view of the diode microbolometer, where deep trench etching and trench filling steps are added to remove the silicon underneath the detectors using XeF_2 gas, while still keeping the silicon between the pixels to prevent thermal cross talk. Fig. 10.17 shows an SEM view of the recent SOI diode pixels developed by Mitsubishi [61]. These pixels also utilize high fill factor absorbing structures and this allows the pixel size to be reduced without compromising the performance. The recent work of this group shows that it is possible to obtain an NETD of 87 mK with a 320×240 FPA, while the pixel size is reduced to 28 μm×28 μm [61]. Although this approach provides very uniform arrays with very good potential for low-cost, high-performance uncooled detectors, its fabrication is based on a dedicated in-house SOI CMOS process. Since these detectors cannot be implemented in a standard CMOS process, it would be difficult to reduce their costs to the limits that ultra-low-cost applications require. For ultra-low-cost applications, the best approach would be to implement the detector arrays together

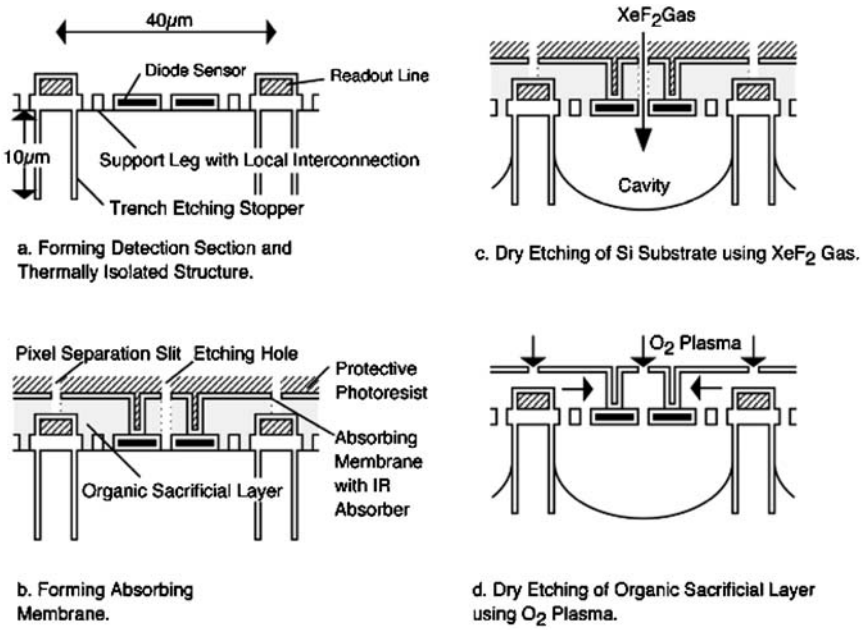

Fig. 10.16 Modified fabrication steps and final cross-sectional view of the SOI diode microbolometer, where deep trench etching and trench filling steps are added to remove the silicon underneath the detectors using XeF_2 gas, while still keeping the silicon between the pixels to prevent thermal cross talk. Reproduced with permission from the author

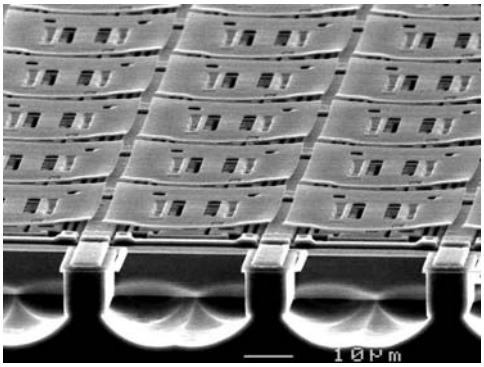

Fig. 10.17 SEM view of the recent SOI diode pixels developed by Mitsubishi. Reproduced with permission from the author

with their readout circuitry fully in standard CMOS, with some simple post-CMOS micromachining steps [75, 77].

Other than detector fabrication costs, there are other factors that affect the cost of uncooled or thermal infrared detector FPAs, including the need for thermoelectric cooler (TEC) use, vacuum packaging, and optics. Uncooled infrared detectors based on thermopiles do not need the use of TEC, as the detectors respond to the difference between the hot and cold junctions, where the cold junction is usually at am-

bient temperature. However, microbolometers require the use of TEC, as they also respond to ambient temperature variations. TEC stabilizes the detector temperature to a fixed level around room temperature, and the bolometer resistance only increases with the absorbed heat. This increases the cost of microbolometers. There are recent approaches to eliminate the use of TEC in microbolometers by changing the bias used during the readout of the microbolometer resistance [82, 83]. Differential readout techniques also reduce the need for TEC use [77].

Another issue with microbolometers is self-heating. For reading of the microbolometer resistor or diode, a current is passed through the pixel, and this causes the pixel to heat. There are various approaches to reduce this effect, including differential reading. Vacuum operation is another issue that increases costs. Vacuum operation is very important, especially for surface micromachined microbolometers, as the separation between the substrate and the detector is only 2–2.5 μm. A vacuum environment for the detectors is usually created on a package level, i.e., by vacuuming the package through a small hole and then sealing the hole that is used for pumping air out. This is a costly approach, and recently efforts have been concentrated on vacuum packaging the detectors with wafer level vacuum packaging approaches [84, 85]. Nevertheless, no detector FPA that is vacuum packaged at the wafer level has yet been reported. A satisfactory solution to this bottleneck will be one of the key elements for cost reduction of uncooled infrared detectors. The cost of infrared optics is a further major issue for low-cost infrared imaging applications, and there are continuing efforts to develop low-cost infrared optics with the use of plastics and molding [86], along with the investigation of other low-cost optic materials [87]. There are also efforts to develop microoptical components that can be used together with FPAs to increase their performance [88].

10.3 Thermal Converters

Thermal converters are used for true root mean square (r.m.s.) voltage and AC signal measurements [89–97]. The basic measurement principle of thermal converters is to convert the electrical signal to a heat power and measure the dissipated power as the temperature elevation of a (micromachined) structure with a temperature sensor. This technique allows the true r.m.s. measurement of the signal, independent of the signal waveform. Implementation of such a sensor using CMOS and MEMS technologies provides a number of advantages. First, MEMS techniques allow the heat-generating resistors to be placed on thermally isolated regions, which allows the achievable temperature elevation per dissipated heating power to be maximized. On the other hand, the use of microstructures enables the thermal time constants to be reduced, yielding increased signal bandwidth. The ability to implement these structures in a CMOS process enables one to put readout circuitry together with the sensor, allowing the implementation of precision measurement techniques. Implementing thermal converters with CMOS and MEMS technologies also allows their cost to be reduced.

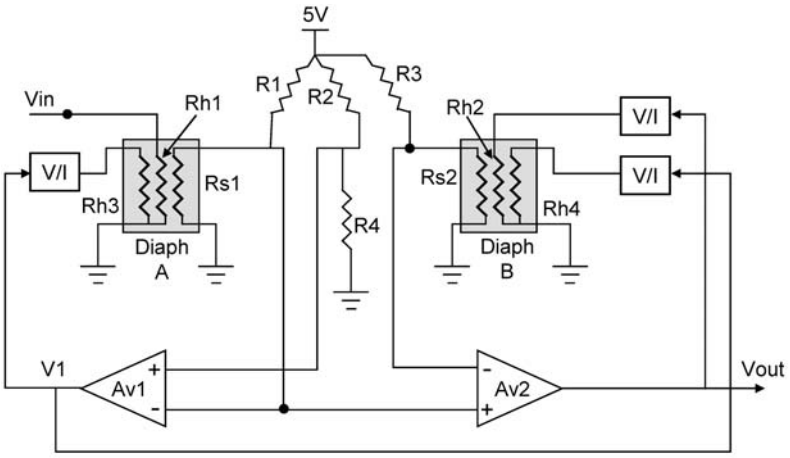

Fig. 10.18 Circuit diagram of the thermal r.m.s. converter developed at the University of Michigan. After [90]

There are various approaches to co-integrate thermal r.m.s. converters with CMOS technologies [89–97]. Devices developed by the US National Institute for Standards and Technology (NIST) use a polysilicon resistor as the heater and thermocouples as the sensor element, with both elements placed on a dielectric diaphragm suspended using front-side bulk micromachining of CMOS-fabricated chips [89]. The bandwidth of the implemented devices is limited to about 100 kHz owing to the relatively large diaphragms of 2×4 mm [89].

A different approach pursued at the University of Michigan utilizes a differential readout mechanism together with a feedback circuit to obtain higher performance in terms of sensitivity and bandwidth and to decrease the influence of ambient temperature variations [90]. Fig. 10.18 shows the circuit diagram of the device. There are two thermally isolated diaphragms and a feedback circuit to keep the temperature of both diaphragms the same and about 20 °C above the ambient temperature. In each diaphragm, there are three resistors, two of which are made with polysilicon and used as heating resistors and one made with gold and used as a temperature sensor. One of the heating resistors (Rh1) on diaphragm A is connected to the unknown AC input signal, while the other heating resistor (Rh3) is driven by the feedback circuit (V_1). Similarly, one of the heating resistors (Rh2) in diaphragm B is connected to the output voltage (V_{out}) generated by the circuit, and the other (Rh4) is connected to the V_1 signal. The V_1 signal is used to keep the temperatures of each diaphragm at a constant value of about 20 °C above ambient regardless of the input signal. The output voltage of the second feedback loop, V_{out}, is the true r.m.s. value of the unknown input signal. If the input signal V_{AC} is zero, then V_{out} is zero. If there is an AC signal on V_{in}, a DC signal V_{out} that provides the same heating power is generated by the circuit, as the feedback circuit forces the temperatures of diaphragms A and B to be the same. Meanwhile, the voltage V_1 is decreased to compensate for the extra heatings from V_{in}

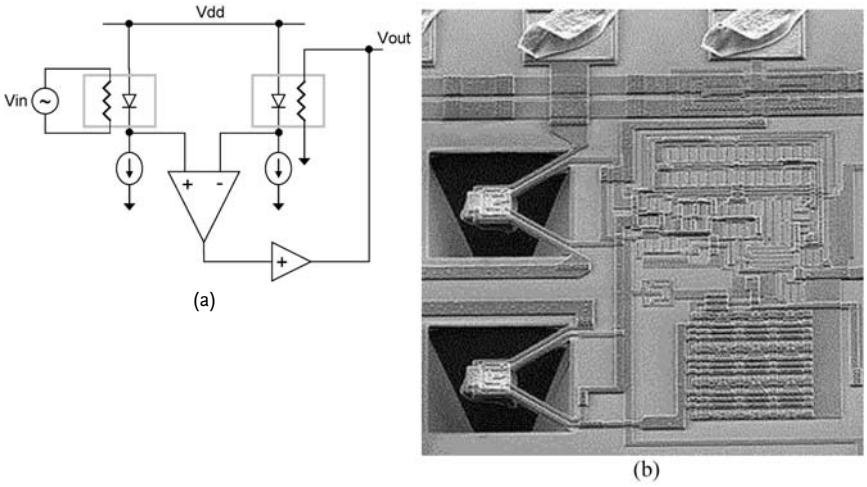

Fig. 10.19 Thermal r.m.s. converter developed at Stanford University: (a) circuit diagram; (b) SEM photograph showing the CMOS circuitry and the suspended n-well structures holding the heater resistors and sensor diodes [91, 92]

and V_{out} on each diaphragm. This approach allows one to obtain true r.m.s. values of input signals up to 20 MHz signal bandwidths with a non-linearity less than 1%. The device measures 3×3.5 mm and is fabricated using a custom 3 µm CMOS process in combination with back-side bulk micromachining, releasing a dielectric membrane with a thermal resistance of 7000 K/W.

The thermal converter developed at Stanford University uses a similar concept compared to the University of Michigan device in terms of keeping the temperatures of two thermally isolated regions the same, where one region is heated with an unknown input AC signal and the other region is heated with a known DC output signal [91, 92]. However, there are a number of differences in the implementation. Fig. 10.19 (a) shows the circuit diagram of the thermal r.m.s. converter developed by Stanford University. The temperature sensors are implemented with diodes that are suspended and thermally isolated from the substrate. These suspended microstructures also have heating resistors. When an unknown AC signal is applied to the heating resistor of the microstructure A, the temperature of that region is increased by an amount proportional to the r.m.s. power of the AC signal. The feedback circuitry now generates a DC output voltage, V_{out}, that provides a similar power to the microstructure B to raise its temperature to a value similar to that of microstructure A. Therefore, the r.m.s. value of V_{in} is given by V_{out}. Fig. 10.19 (b) shows the fabricated device, where the suspended diode structures are implemented by post-CMOS anisotropic etching from the front of the wafer using TMAH (see also Chapter 1) in combination with an etch-stop technique at the CMOS n-wells. The suspended diode structures provide a high thermal resistance of 37 000 K/W and a low thermal time constant of 5 ms, resulting in a good overall performance. The device has a packaging limited 415 MHz bandwidth, a

60 dB dynamic range, 1% nonlinearity, and 1 mW power dissipation, while occupying a small area of only 400 μm×400 μm.

Substantial work on thermal converters has also been conducted at ETH Zurich [93–96]. A number of devices have been developed with the same basic idea, i.e., a polysilicon resistor on a dielectric diaphragm is used as the heating resistor connected to the unknown AC input signal and thermopiles are used as temperature-sensing elements. The dielectric diaphragms are obtained using either front-side bulk micromachining or back-side bulk micromachining of standard CMOS-fabricated wafers. One of the fabricated devices is reported to provide a linearity error of less than 0.1% below 400 MHz and less than 1% up to 1.2 GHz [93].

Thermal converters to measure even higher frequency microwave signals have also been implemented with post-CMOS bulk micromachining approaches. One such device is implemented using thermocouples in a standard CMOS process. The aluminum/polysilicon thermocouples are suspended using post-CMOS etching with XeF_2 dry etching first, followed by an EDP etch [97]. The fabricated device is reported to operate up to 20 GHz with a non-linearity of ±0.16%, while having a dynamic range of 40 dB and a sensitivity of 5.32 V/W.

10.4 Thermal Flow Sensors

Flow sensors are used to measure the movement of a fluid. They have a wide variety of application areas including biomedical, environmental monitoring, automotive, and process control. There are different techniques to realize a flow sensor depending on the application [1, 98–100], including measuring physical deflection, heat loss, and pressure variation. This section will summarize the state of the art on CMOS-based thermal flow sensors.

Thermal flow sensors measure the fluid flow by measuring the convective heat transport due to the liquid/gas flow [1]. There are three main categories of thermal flow sensors, depending on their operation principles [98]: anemometers, calorimetric flow sensors, and time-of-flight flow sensors.

An anemometer is a device measuring the heat loss due to liquid flow. Generally, anemometers have a single element, which is heated, while its temperature is measured. Owing to the external flow, the heater element temperature, and hence its resistance, change. By monitoring this change, the flow rate can be measured. MEMS-based anemometers employ thermally isolated thin films as the heating element. This heating element is located on a membrane or microbridge to achieve good thermal isolation and high sensitivity. Anemometers can operate in three different modes: constant current, constant temperature, or constant power.

Calorimetric flow sensors and time-of-flight flow sensors require two or more elements. Fig. 10.20 shows the operation principle of a calorimetric flow sensor. In this type of flow sensor, a heating element, such as a polysilicon resistor, heats the fluid. There are two resistive thermometers located on both sides of the heater. In MEMS implementations, these thermometers can be made of thermopile,

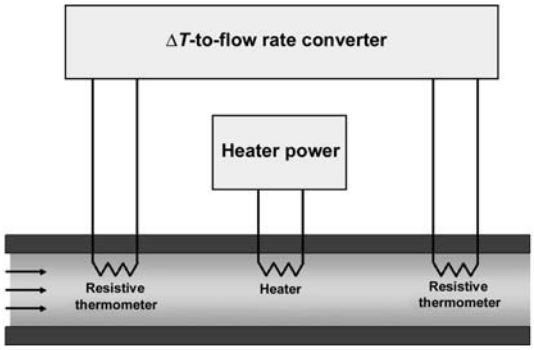

Fig. 10.20 Schematic view of a calorimetric flow sensor. After [98]

polysilicon resistors or p–n junction diodes. Depending on the flow rate and direction, hence, a temperature difference between the thermometer readings develops giving a measure of the flow rate.

In time-of-flight sensors, a heat pulse is applied to the fluid, and its delay is measured by a temperature sensor located at a different position. This type of flow sensors is more accurate in determining the velocity of the flow [99].

Honeywell developed a microfabricated (but not CMOS integrated) air-flow sensor in 1987 [102] to measure gas velocity, mass flow or differential pressure using the constant-heater-power-mode calorimetric approach. This device measures the temperature difference between upstream and downstream resistors as shown in Fig. 10.20. The sensor is commercially available in a package with a flow inlet employing a dust filter.

Another thermal flow sensor operating in the constant-heater-power-mode was developed at the University of Michigan in 1992 [103, 104]. In this work, an integrated mass-flow sensor with on-chip CMOS interface electronics is presented. This device is an intelligent sensor which is capable of measuring flow velocity, direction, gas type, temperature, and pressure. Fig. 10.21 shows the sensor structure. The sensor operates over the 1 cm/s to 5 m/s range.

Another packaged, miniaturized flow sensor microsystem was reported by Mayer et al. [105] in 1997. The reported system includes a thermal CMOS flow sensor with on-chip power management, signal conditioning, and A/D conversion. Fig. 10.22 shows a schematic view of the system. The flow sensor is based on a membrane made of dielectric layers of the CMOS process. Gate polysilicon is used as the heating resistor and a temperature difference due to heat loss is measured by integrated polysilicon-based thermopiles. The chip consumes 3 mW of power and can measure wind speeds up to 38 m/s with a dynamic range of 65 dB. Fig. 10.23 shows different gas sensors with a similar idea developed by the same group [105–111].

Fig. 10.24 shows a commercial gas flow meter developed by ABB [112], which utilizes the CMOS-based flow sensor developed by Sensirion in Switzerland [113]. The flow sensor is composed of a closed membrane with temperature sensors sandwiched between stress-free dielectric layers. An integrated resistor provides

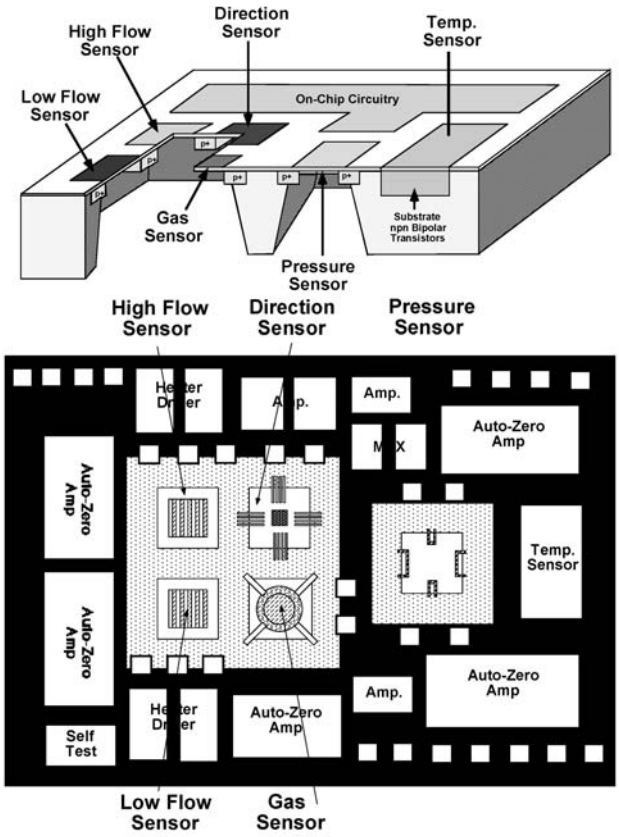

Fig. 10.21 Integrated mass-flow sensor developed at the University of Michigan. After [103]

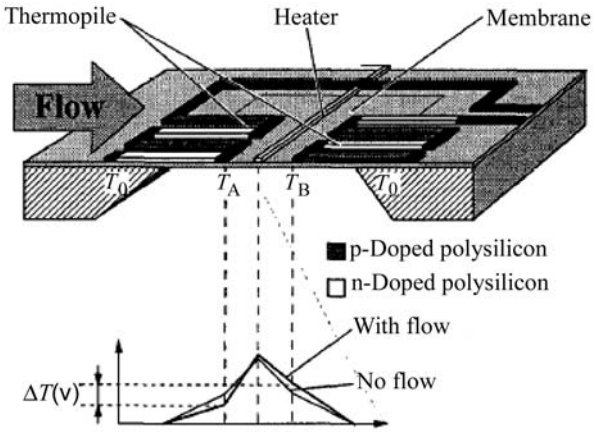

Fig. 10.22 Schematic view of the micromachined thermal flow sensor developed by ETH Zurich. After [105]

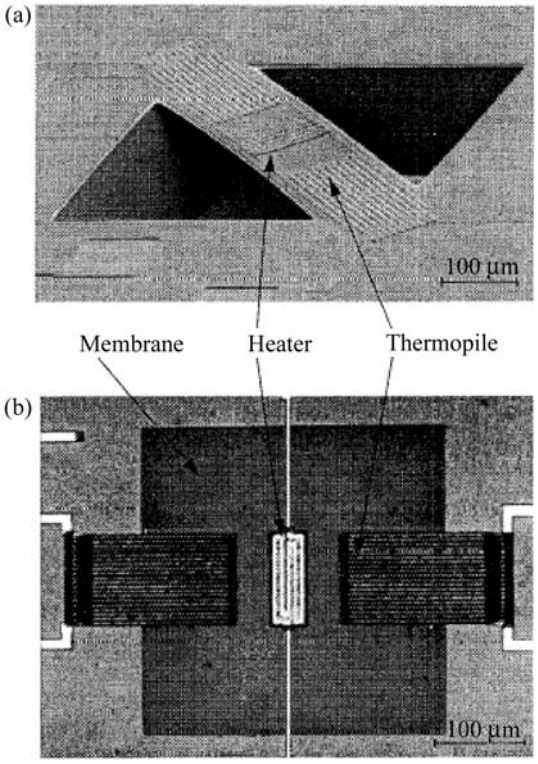

Fig. 10.23 (a) SEM photograph of a microbridge CMOS gas flow sensor. (b) Optical micrograph of a membrane CMOS gas flow sensor developed by ETH Zurich. After [107]

Fig. 10.24 A commercial gas flow meter developed by ABB, which utilizes the CMOS-based flow sensor developed by Sensirion. After [112]

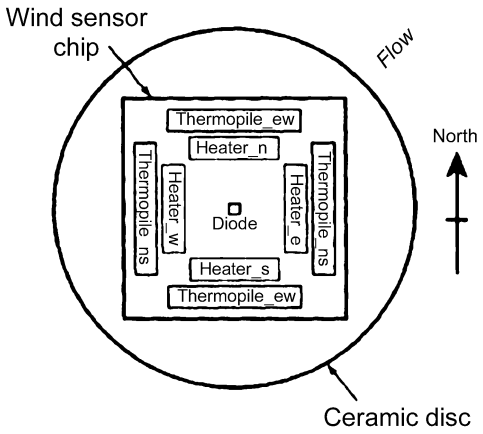

Fig. 10.25 Schematic view of the two-dimensional wind sensor. After [114]

the heating power. The sensors measure the temperature of the gas before and after it flows over the heater and this gives a measure for the gas flow.

A smart wind sensor was reported by Delft University, combining thermal flow sensor and sigma–delta interface electronics on a single chip [114–116]. This chip is capable of measuring wind speed and direction with an accuracy of ±4% and ±2°, respectively, over the range 2–18 m/s. Fig. 10.25 shows the schematic layout of the CMOS wind sensor. It consists of a square silicon substrate on which four heaters, four thermopiles and a diode have been integrated. Each thermopile consists of 12 p^+-diffusion/Al thermocouples and has an estimated sensitivity of 6 mV/K. Heaters are made of polysilicon resistors.

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