HIGH SPEED TWO FRAME VIDEO DATA ACQUISITION SYSTEM

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By

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ABSTRACT

HIGH SPEED TWO FRAME VIDEO DATA ACQUISITION SYSTEM

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A 19 MHz sampling rate digitizer is designed as an expansion unit for IBM-AT microcomputer bus, for acquisition of video signals generated by medical imaging systems. Two successive frames of image data are sampled and stored for post processing in the computer.

System is designed as a general purpose frame grabber and a flexibility is given with user defined options and some special purpose units such as compander amplifier.

Key words: Fast A/D conversion, frame grabber, microcomputer interfacing.

Scientific Code: 609.01.04

ÖZET

YÜKSEK HIZLI, İKİ ÇERÇEVE GÖRÜNTÜ VERİSİ AKTARMA SİSTEMİ

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Medikal sistemlerce üretilen görüntü sinyallerini IBM-AT kişisel bilgisayarına aktaracak 19MHz örnekleme hızı olan bir analog-sayısal dönüştürücü, bilgisayara genişleme ünitesi olarak tasarlanmıştır.

Sistem, genel amaçlı bir görüntü yakalayıcı olarak tasarlanmış ve kullanıcı tarafından tanımlanan seçenekler ve sıkıştırıcı yükselteç gibi bazı özel ünitelerle daha esnek bir yapı kazandırılmıştır.

Anahtar sözcükler: Hızlı Analog Sayısal Dönüşüm, Görüntü Yakalayıcı, Mikrobilgisayar Arabağlaşım.

Bilim Alanı Kodu: 609.01.04

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CHAPTER 1

INTRODUCTION

In medical imaging systems, sometimes, complex image processing techniques are required for accurate characterization of tissues of the human body. Computers and their peripherals offer the users a wide variety of image processing techniques with higher precision and less noise than the analog systems. In recent years, there had been a significant improvement in digital data acquisition and image processing hardware and software for more accurate medical diagnosis.

The aim of this study is to design a high speed data acquisition system to store samples of video signals which carry two dimensional image information, for post processing in the microcomputer.

Two years ago, another data acquisition study "Image Data Acquisition System" had been carried out[1]. A 26.65MHz sampling rate digitizer is designed to acquire ultrasound RF signals and video signals. One frame of ultrasound signals or video data is acquired by the system and transferred to the host computer by asynchronous serial communication protocol RS-232C.

This study covers the design and implementation of

a high speed image data acquisition add-on card for the IBM-AT microcomputer. The device is installed on an expansion slot of the microcomputer which is directly connected to the computer's bus. This is an efficient way for the computer to acquire data if speed and less hardware requirement considerations are taken into account.

In chapter 2, information about video signals are given. The flash analog to digital converter and the function and the characteristic of the input companding stage are briefly explained.

The designed hardware and software to acquire the data and the design constraints are explained in chapter 3. The hardware is explained in blocks with related circuit and timing diagrams.

The results achieved and comments on further studies are discussed in chapter 4.

Appendix A includes the software designed to transfer and process the data acquired in the computer. In Appendix B, the circuit diagrams, circuit's layout, printed circuit board layouts, parts list are given. Data sheets of some special components used in the system can be found in Appendix C and information about the IBM-AT bus is given in Appendix D.

CHAPTER 2

ACQUISITION OF VIDEO SIGNALS AT HIGH SAMPLING RATES

2.1. VIDEO SIGNALS

In recent years, a rapid growth is observed in medical imaging systems. Present technology use four basic techniques for medical imaging: X-Rays, ultrasound, nuclear science and Magnetic Resonance Imaging.

In X-Ray imaging, a very high frequency elctromagnetic energy is employed. This energy is transmitted through the body to form an image. The transmitted energy is received by a TV camera to form the image on a monitor. The gray levels of the image formed is proportional to the absorption of energy within the tissues.

In this study, a system for acquisition of two successive frames of image data obtained by a TV camera is developed.

2.1.1. Video Camera Signals

There are two major techniques of scanning used by video cameras: interlaced scanning or non-interlaced

scanning. Interlaced scanning scans the odd number of lines in one field and even number of lines in the second field forming one frame of two dimensional image data. Non-interlaced scanning scans all lines in one field to form one frame of image data. We can also group video signals, according to the polarity of black and white levels, as positive video signals or negative video signals [2]. One line of a positive video signal is given in figure 2.1.a and illustration of interlaced scanning and non-interlaced scanning can be seen in figure 2.1.b.

The system is designed to record positive and interlaced signals to the microcomputer IBM-AT PC.

2.2 MEMORY CONSIDERATIONS

System requires a temporary storage unit since the data acquisition speed is too high for any computer to handle. Therefore an average size of memory to store one frame of image data should be calculated.

A standard TV camera scans 625 lines in one frame. Scan of one line takes 64 microseconds. 10.24 microseconds of this period is reserved for synchronization pulses and data is given in 53.76 microseconds. Therefore, the number of samples taken

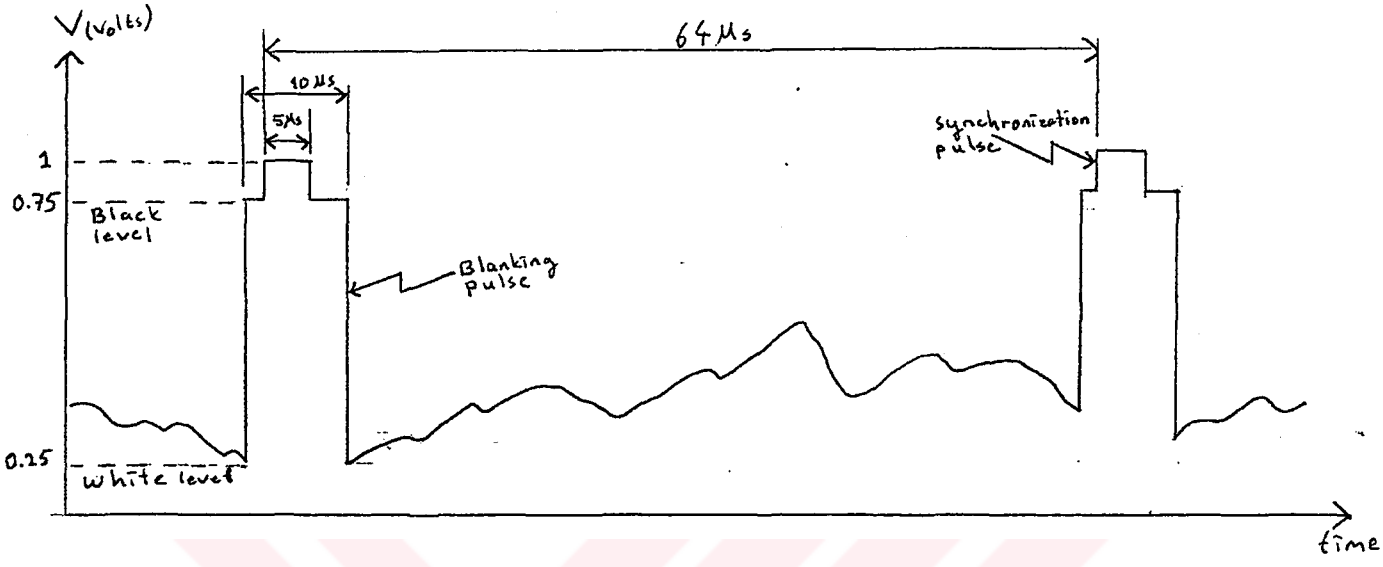
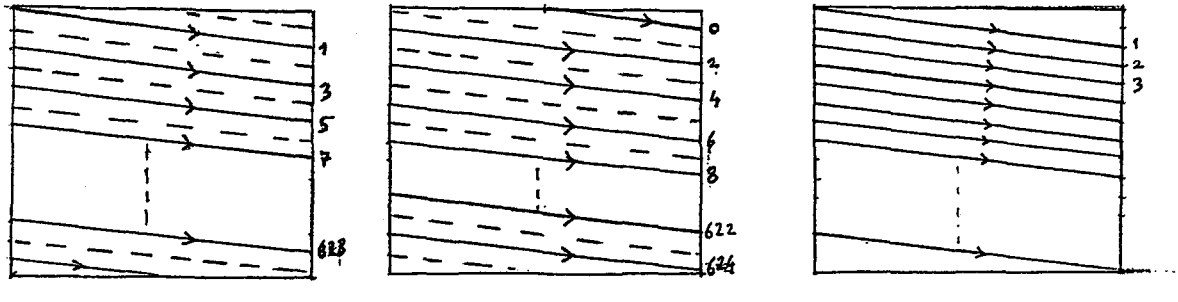


Figure 2.1.a. One Line of Positive Video Signal.



Odd Field Even Field Non-Interlaced Scanning

Interlaced Scanning

Figure 2.1.b.

from one line is given as:

53.76microseconds/52nanoseconds=1033 samples,

Then, number of samples taken from one frame of image data can be calculated as:

1033samples/line * 625lines/frame = 645625samples/frame

Here it is assumed that the edges of the image usually contain no useful data. Hence, a resolution of 900samples/line and 580lines/frame would be sufficient which requires a 512KByte of memory. This resolution is sufficient since IBM-AT monitor has a resolution of 720 column*400 row pixels (picture elements) at best.

2.3. FAST ANALOG TO DIGITAL CONVERSION

The function of the fast analog to digital (A/D) conversion unit is to convert the analog video signals into 8 bit digital words at 19 mega samples per second (MSPS) rate.

The flash A/D converter embodies the fastest known technique for converting a continuous voltage into discrete digital codes and does not require a sample and hold circuit at the input. In an n-bit flash A/D converter 2^n comparators are packed. A single convert signal controls the conversion operation of the analog signal, V_{in}. The conversion is achieved by encoding the comparator outputs when a 'convert' command is received.

TRW-TDC1048, a 20MSPS flash A/D converter is used for conversion of video signals and it is capable of converting an analog signal with full power frequency components up to 10 MHz into 8-bit digital words with 1/2 least significant bit accuracy. It has TTL compatible digital inputs and outputs and can be connected to give either true or inverted outputs in binary or offset two's complement coding [3]. The TDC1048 flash ADC consists of a comparator array, encoding logic and output latches. Functional block diagram is given in figure 2.2 and timing diagram is given in figure 2.3.

2.3.1 Interface Circuit

The interface circuit at the input of the A/D converter contains a companding amplifier, a buffer amplifier, a limiter and a reference voltage generator as shown in figure 2.4.

The companding amplifier provides an increase in dynamic range comparable to 10-bit resolution with an 8-bit system. It is basically a transistor differential amplifier pair, implemented using a hybrid transistor array[4]. Its transfer function is given by the formula:

$$V_{in} = (kT/q) \ln (I_2/(I_s - I_2)) + R_e (2I_2 - I_s)$$

ɔnal Block Diagram

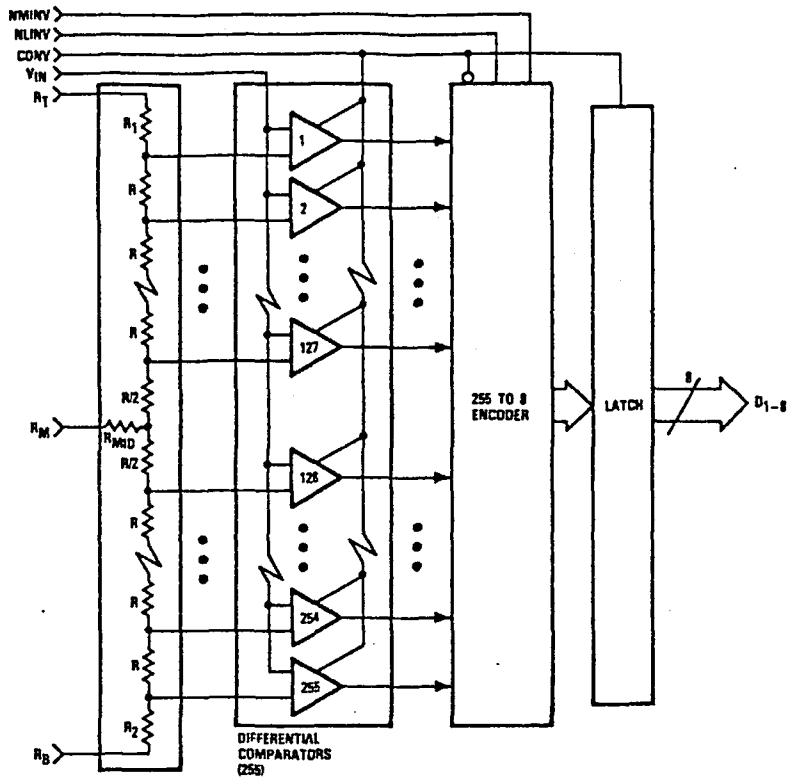


Figure 2.2. Block Diagram of the A/D Converter Unit.

Diagram

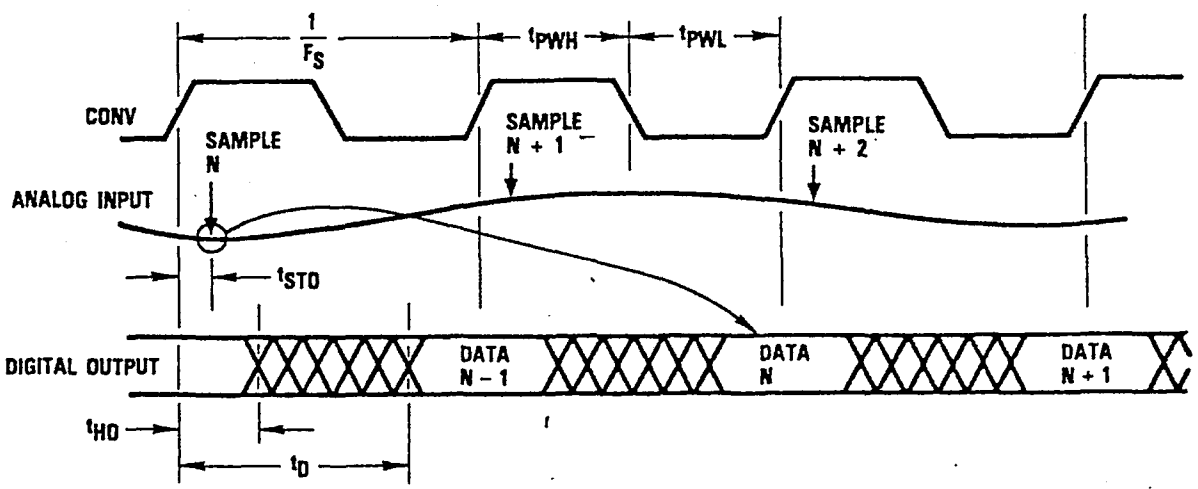


Figure 2.3. Timing Diagram of the A/D Converter

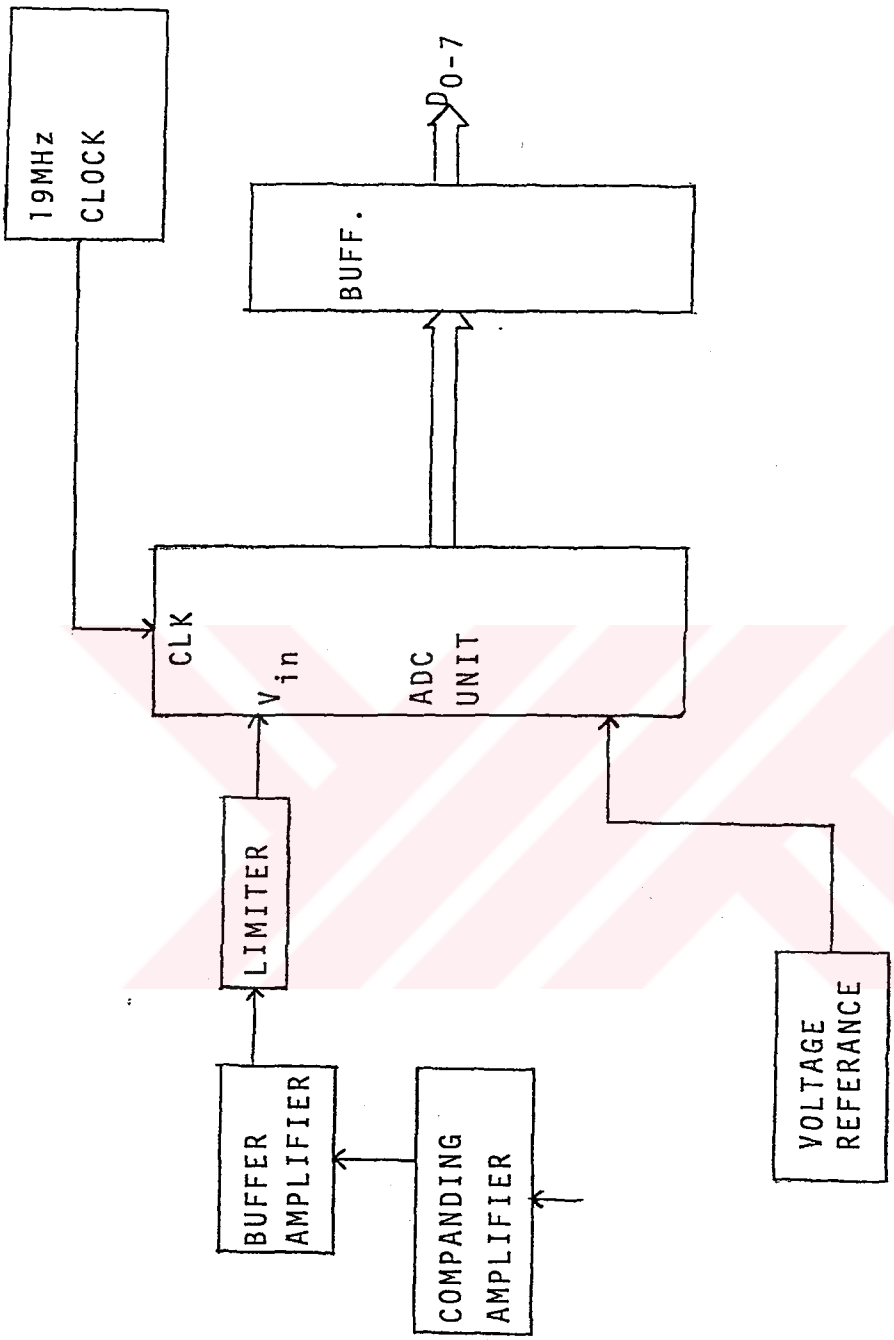


Figure 2.4. A/D Converter Interface Circuit Block Diagram.

Here V_{in} is the input voltage, k is Boltzmann constant, T is temperature in Kelvin, q is charge in Coulombs, I_2 is the collector current of the second (non-inverting) transistor, I_s is the quiescent bias current and r_e is the emitter resistance.

During the design, it is tried to fit this characteristic to a logarithmic curve which is expressed as:

$$I_2 = (I_s/2) + a \ln(1 + b (q V_{in}/(k T))$$

by changing the circuit parameters.

Precise logarithmic characteristic is obtained by a further software conversion. The reason for choosing a differential pair is its large bandwidth. With a logarithmic amplifier it is not possible to get such a large bandwidth. The logarithmic curve and the transfer curve of the amplifier is given in figure 2.5.

The companding amplifier together with the buffer amplifier match the 1V p-p 75 Ohm video output to the A/D converter input. The limiter circuit is used to protect the A/D converter input from input levels higher than the specified level. Voltage reference circuit provides an adjustable voltage of about -2 volts.

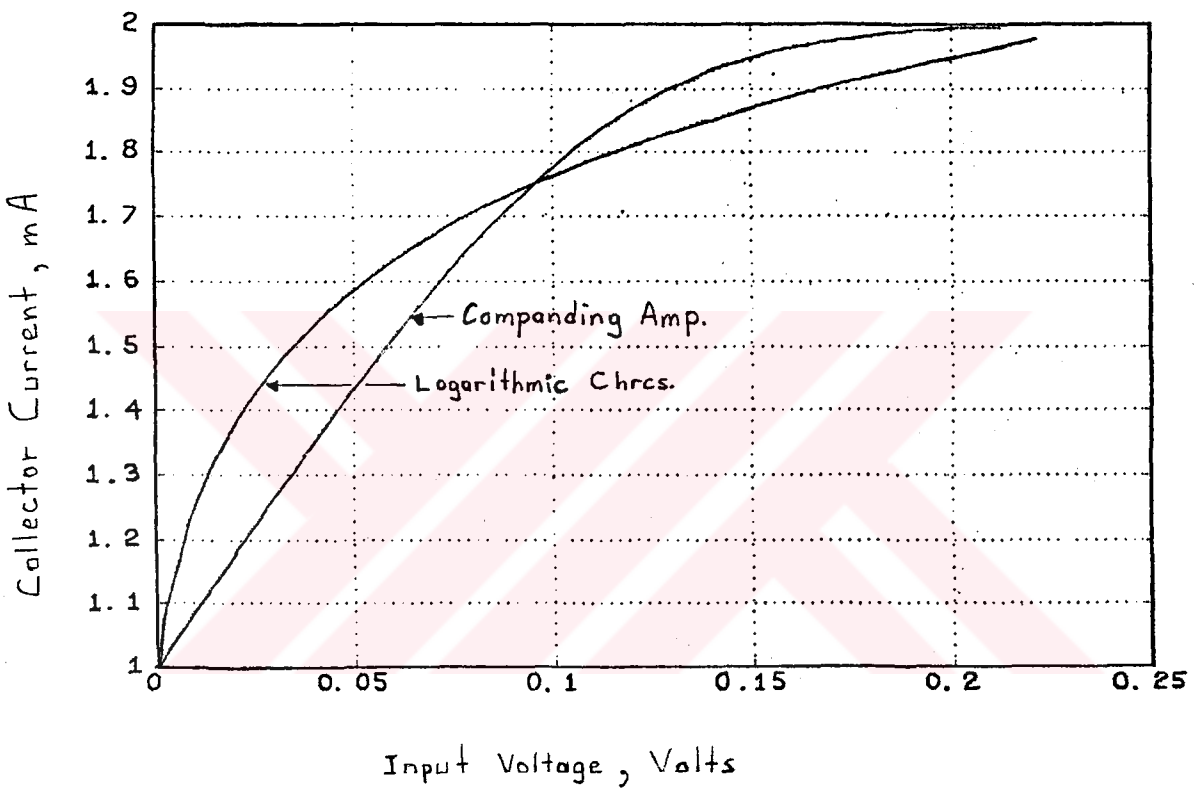


Figure 2.5. The Logarithmic Curve and the Characteristic Curve of the Companding Amplifier.

CHAPTER 3

ACQUISITION OF THE DATA

System is designed to interface a video camera to the IBM-AT PC. One read cycle takes about 750 nanoseconds for a microcomputer with 6 MHz system clock. The fast A/D converter generates a byte of data at every 52 nanoseconds. Therefore, additional circuit is required to acquire data at this speed and then transfer this data to the host computer for long-term storage and post-processing.

The data acquisition unit is installed directly to the computer's bus through its expansion slot. Hence, operations for acquiring data are controlled mainly by the computer itself. A detailed block diagram of the system is given in figure 3.1.

3.1 DECODING AND CONTROL UNIT

Two main blocks control the data acquisition operation: decoder unit for decoding instructions from the microcomputer and a control unit generating signals for memory operations.

Upon receiving the start command from the computer,

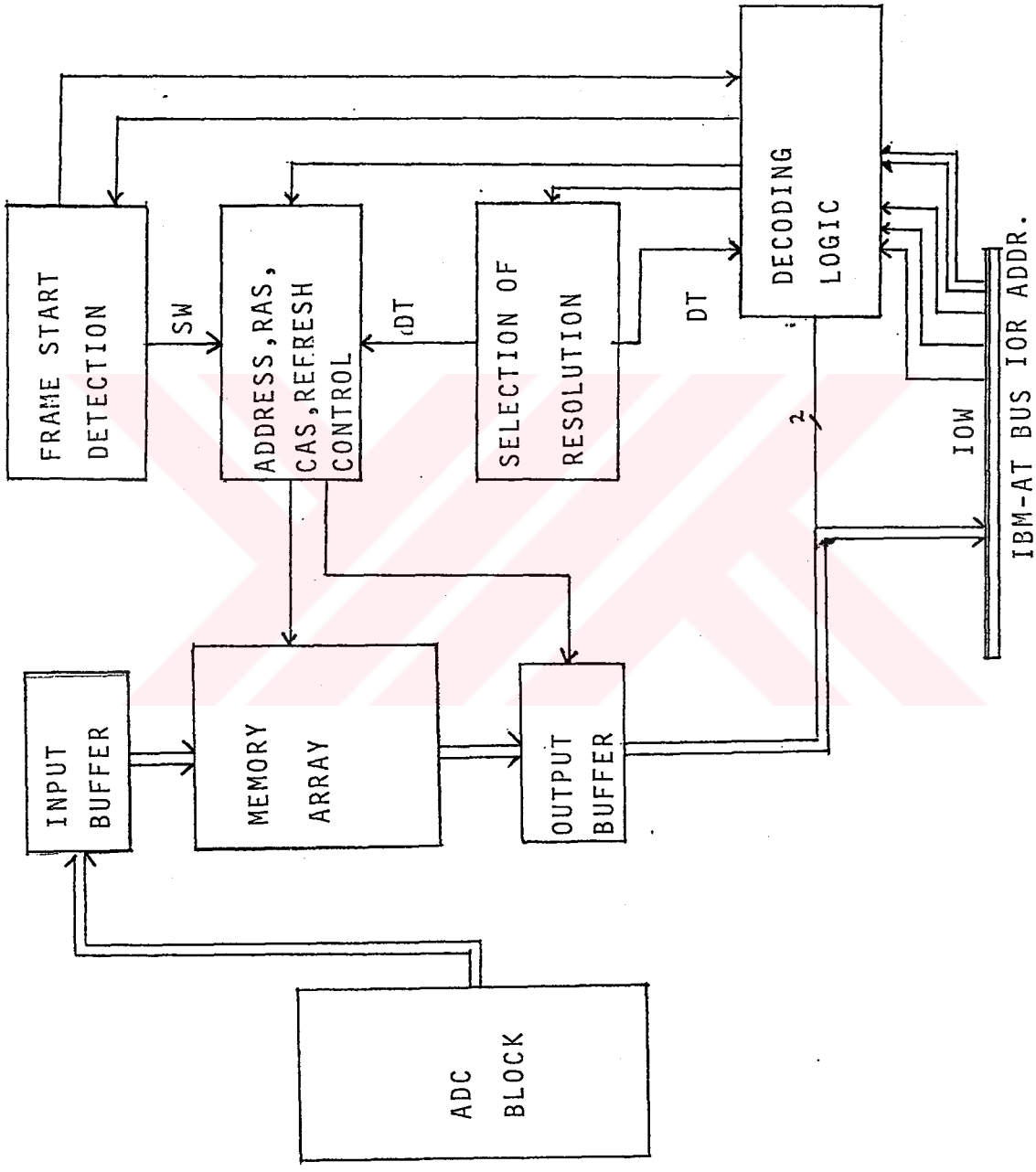


Figure 3.1. Block Diagram of the Data Acquisition System.

circuit waits for the start of a new frame of image data. With the start of the first odd field of a frame, clock circuit is enabled for storage of acquired data into the temporary memory. When two frames of image data are stored, system informs the computer that data is available. Then, data transfer to harddisk is performed under the control of the computer.

3.1.1. Decoder Unit

A microcomputer performs many input and output (I/O) operations during the execution of a program. The computer generates related address, data and other control signals for every I/O operation of its central processing unit (CPU). Therefore, each unit must decode instructions related to itself and must not respond to other instructions [5].

The system decodes instructions between the addresses 100_{hex} to $17F_{hex}$ where the most significant five bits are used to enable the system and bit_4, bit_5 and bit_6 are used to decode six different instructions [6]. Least significant four bits of the address data are not used to simplify the decoding logic.

The decoding block consists of a two input AND gate, a quad two input OR gate and a 3 to 8 decoder.

The circuit diagram is given in figure 3.2. This block generates six different signals for the control of operations performed by the system. The INIT signal initializes the system counters and flip-flops before data acquisition operation starts. The START signal enables the hardware which detects the start of a frame. RAS signal sends the strobe signal for memory in read cycles.The signal CHK checks whether the system is in read mode and whether any refreshing of memory takes place. For read operations, a read buffer (RB) signal is generated which is sent to another decoding logic that enables the memory output buffers sequentially to send data to the microcomputer. The last signal generated is the FRS signal which selects the block of memory from which data is to be read.

3.1.2. Memory Control Unit

In interlaced scanning systems, a new frame of image data starts with the scan of odd field. Therefore, to acquire a complete frame of image data, start of odd field must be detected. With the start of odd field, memory operations are enabled to store data coming from the A/D converter unit.

The resolution of TV cameras vary considerably from one camera to another. The compatibility of the system

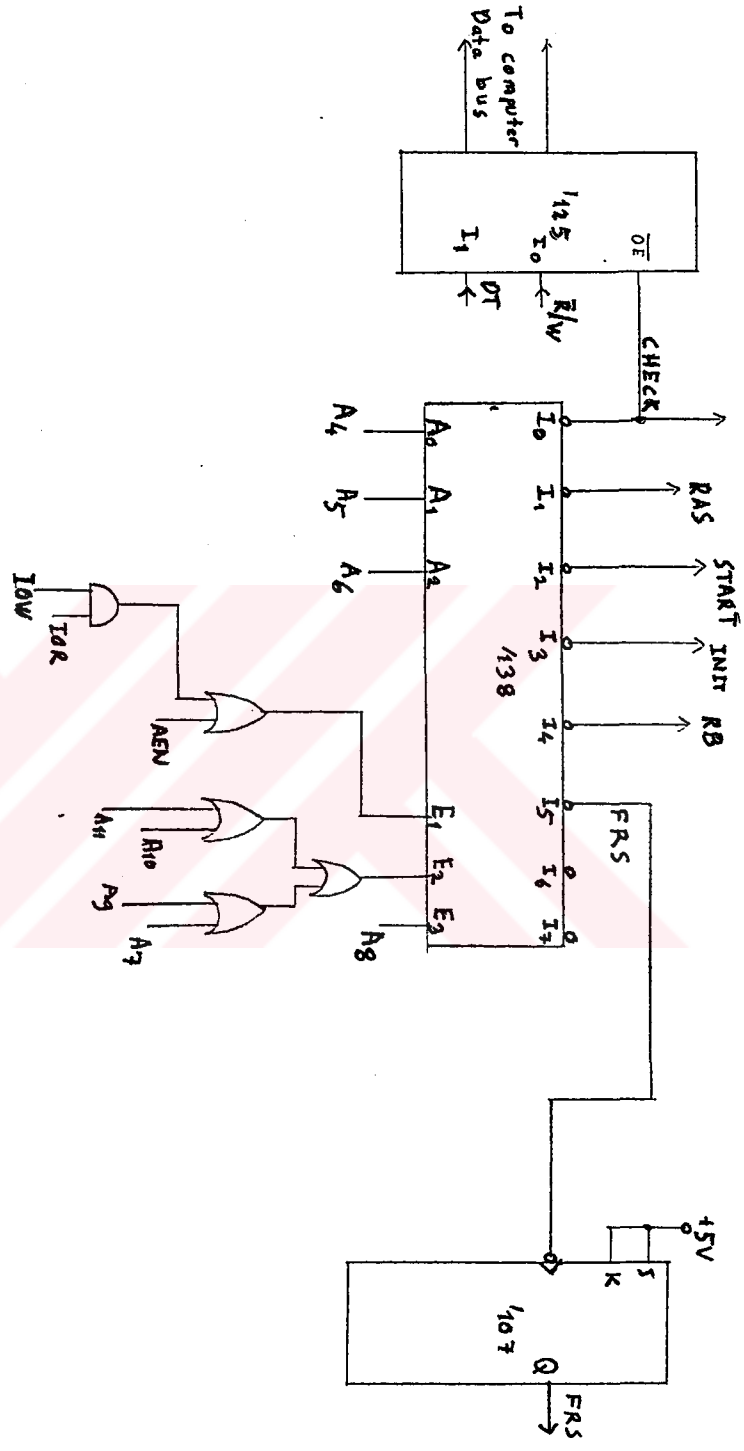


Figure 3.2. Block Diagram Of The Decoding Logic.

with different type of cameras is also taken into account during the design. The size of data to be recorded is selected by the user. Any desired window from the image can also be chosen.

Dynamic memory devices used for temporary storage of data need addressing, address strobe, read/write and refreshing signals for regular operation. These signals are generated by the memory control hardware.

3.1.2.1 Frame Start Detection

A TV camera generates equalization and horizontal synchronization pulses for sychronous operation with the monitor. Equalization pulses, together with the vertical synchronization pulses synchronize the start of fields while horizontal synchronization pulses set the start of each scan of line [2]. These pulses are illustrated in figure 3.3.

The designed hardware has three control signals (CTRL1, CTRL2, CTRL3) to detect the duration of each synchronization pulse and the time interval between two successive synchronization pulses. These signals are generated by monostable multivibrator circuits (74LS123) which are triggered by the synchronization pulses. CTRL1 is a 4 microseconds active low pulse and CTRL2 is a 6

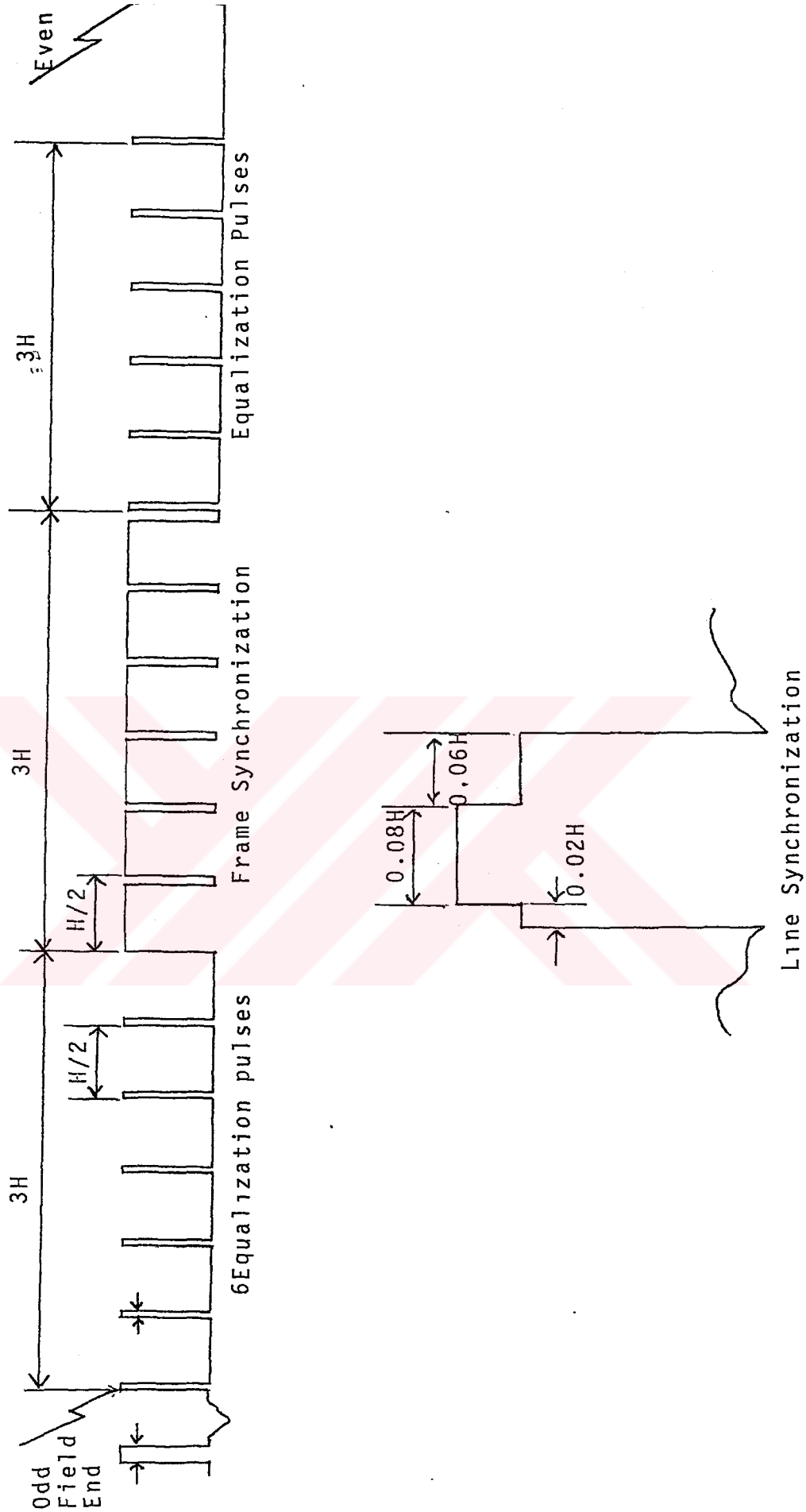


Figure 3.3. Equalization and Line Synchronization Pulses

microseconds active high pulse which are triggered by the rising edge of the horizontal synchronization pulse. CTRL3 is a 30 microseconds active low pulse triggered by the rising edge of the CTRL1 signal.

For regular operation of this system, the synchronization pulses are seperated from the video signal. A voltage referance generating circuit and a voltage comparator circuit are used to seperate the synchronization pulses and generate the SYNC signal compatible with the TTL logic levels.

Three flags are affected with the control signals CTRL1, CTRL2, CTRL3 and SYNC pulses. These flags are named as duration detector (DD), half period (HP) and odd field (OF). DD flag determines the duration of the last synchronization pulse. If CTRL1 and CTRL2 are both high during the high to low transition of a SYNC pulse, which means that the duration of this pulse is between 4 microseconds and 6 microseconds, then the DD flag is set to high logic level. This flag will be zero if the duration of the SYNC pulse is not between 4 microseconds and 6 microseconds. Therefore this flag is set only if the pulse is a 5 microseconds horizontal synchronization pulse. HP signal determines whether the time interval between the last two SYNC pulses is 32 microseconds (half period) or not. If the SYNC pulse is high during

the low to high transition of the CTRL3 signal, then the HP flag is set. Odd field starts with a 5 microseconds synchronization pulse 32 microseconds after a 3 microseconds equalization pulse. Therefore HP flag is still high while DD flag goes from low to high. OF flag is set with the low to high transition of the DD flag if HP is high during this transition, and cleared if HP is low during this transition (start of even field).

The circuit diagram of this block is given in figure 3.4 and related timing diagram is given in figure 3.5.

3.1.2.2. Selection Of Resolution

The problem of circuit's compatibility with different camera resolutions is handled by adjusting the size of data to be stored. The number of lines to be recorded from each frame and the number of samples to be recorded from each line can be selected. This option also enables the system to choose any window from the image that will be acquired.

An eight-bit counter counts the number of points sampled from each line of video data. This counting operation is reset with each line synchronization pulse. It starts with the falling edge of each line synchronization pulse and ends with the rising edge of

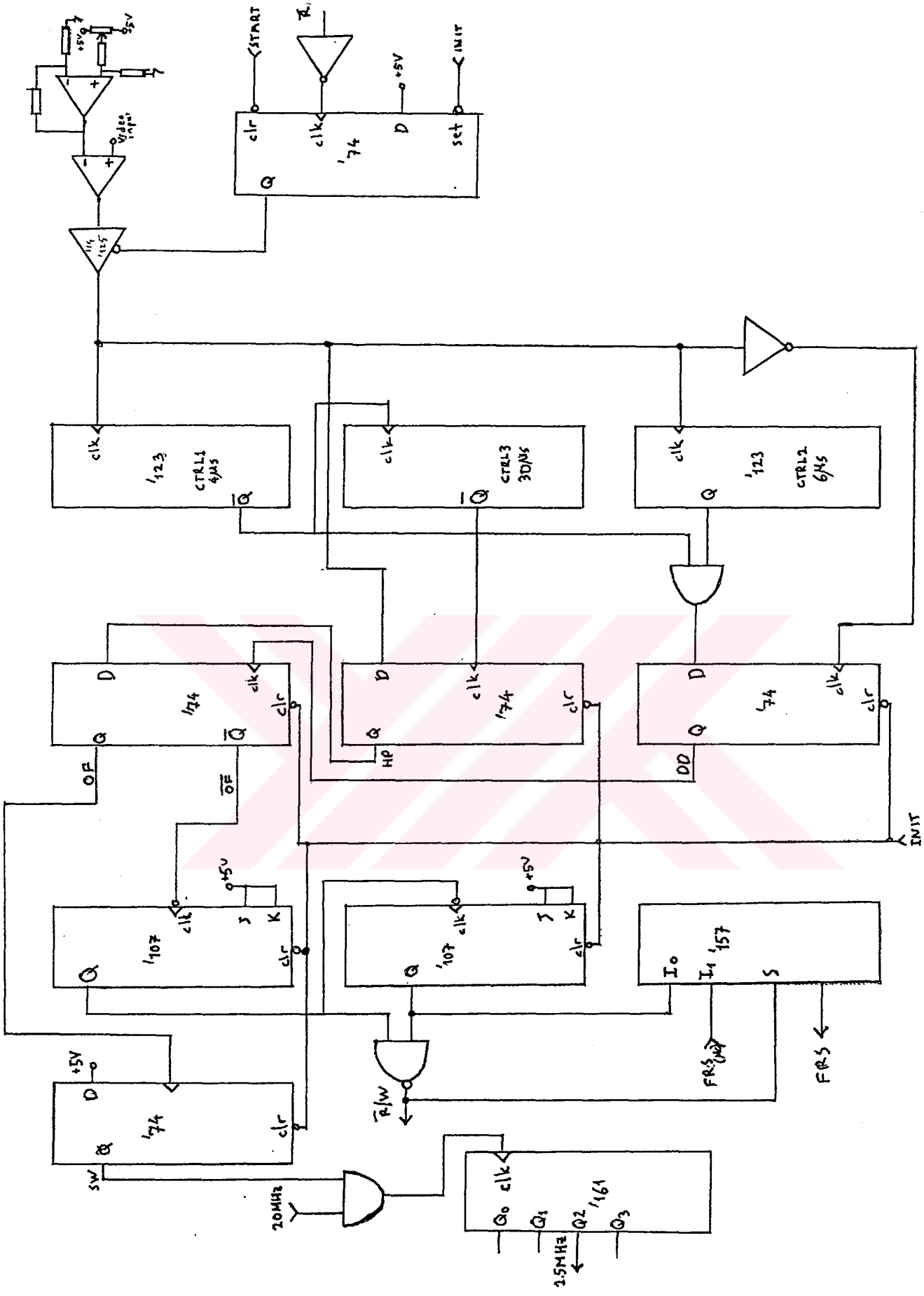


Figure 3.4. Circuit for Frame Start Detection.

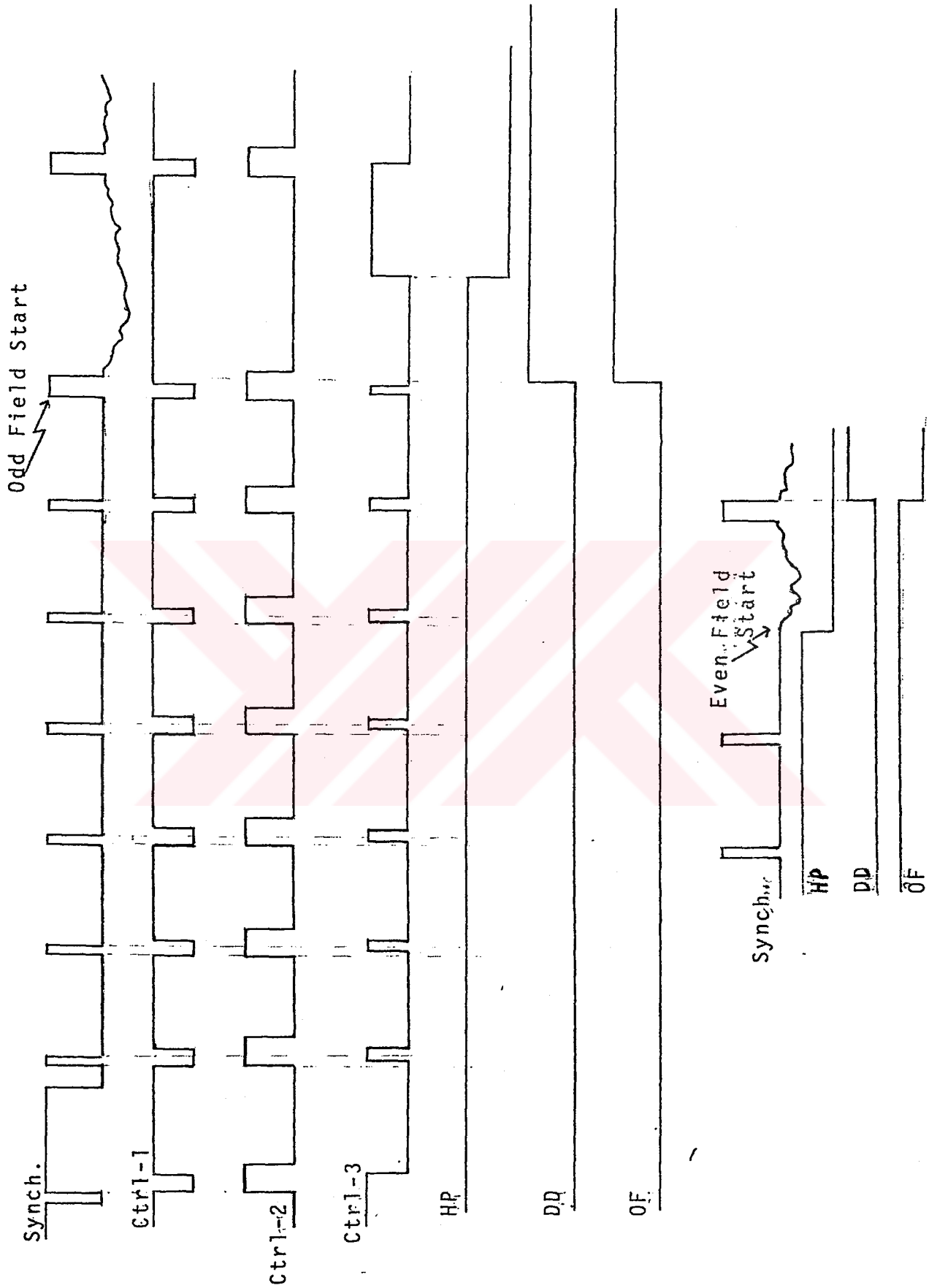


Figure 3.5. Timing Diagram For the Frame Start Detection.

the next line synchronization pulse. For synchronization of this sampling window with the memory control logic, counters are triggered by 1/8 of the system clock frequency. Hence, the counters count the number of sampled points normalized with eight. To generate a sampling window for each line of video data, the value of the point after which recording should start and the value of the point after which the recording should stop are set by two DIP switches. During the scan of each line, the value from the sample counter is continuously compared with the data set by the first DIP switch by a ten-bit magnitude comparator to detect the beginning of the sampling window. The output of the magnitude comparator goes to high logic level when the value of the sample counter output and the DIP switch setting are equal. Therefore a pulse is generated by the magnitude comparator when the sample counter output reaches the value set by the first DIP switch. Similarly the value of the sample counter output is compared with the value set by the second DIP switch by another ten-bit magnitude comparator to detect the end of the sampling window. A second pulse is generated by the second magnitude comparator. The comparator outputs are connected by an OR gate to the clock input of a toggle flip-flop whose output generates the high level signal to form the line sampling window.

A very similar system with 10 bit line counter,

magnitude comparators, a combinational logic circuit and DIP switches is designed to select the lines to be sampled from each field. The counter is reset with the start of each field and triggered with the horizantal synchronization pulses. Therefore it counts the lines scanned within each field. The DIP switches set the number of lines after which recording should start and stop. A window for sampling lines from each field of image data is generated by the same comparator and toggle flip-flop circuit as in line sampling circuit. The generated field window and the line window signals are given to the input of an AND gate to form a two dimensional window on a two dimensional image data. The circuit diagram of this system is given in figure 3.6 and the timing signals are given in figure 3.7.

This configuration provides a resolution of maximum 2048 points from one line and 1024 lines from a field of image data. But it is not possible to obtain these maximum values at the same time, the overall memory capacity should also be taken into account while choosing the resolution.

3.1.2.3 Memory Control Hardware

For temporary storage of data, a 1MByte memory array is used. This array is implemented with dynamic

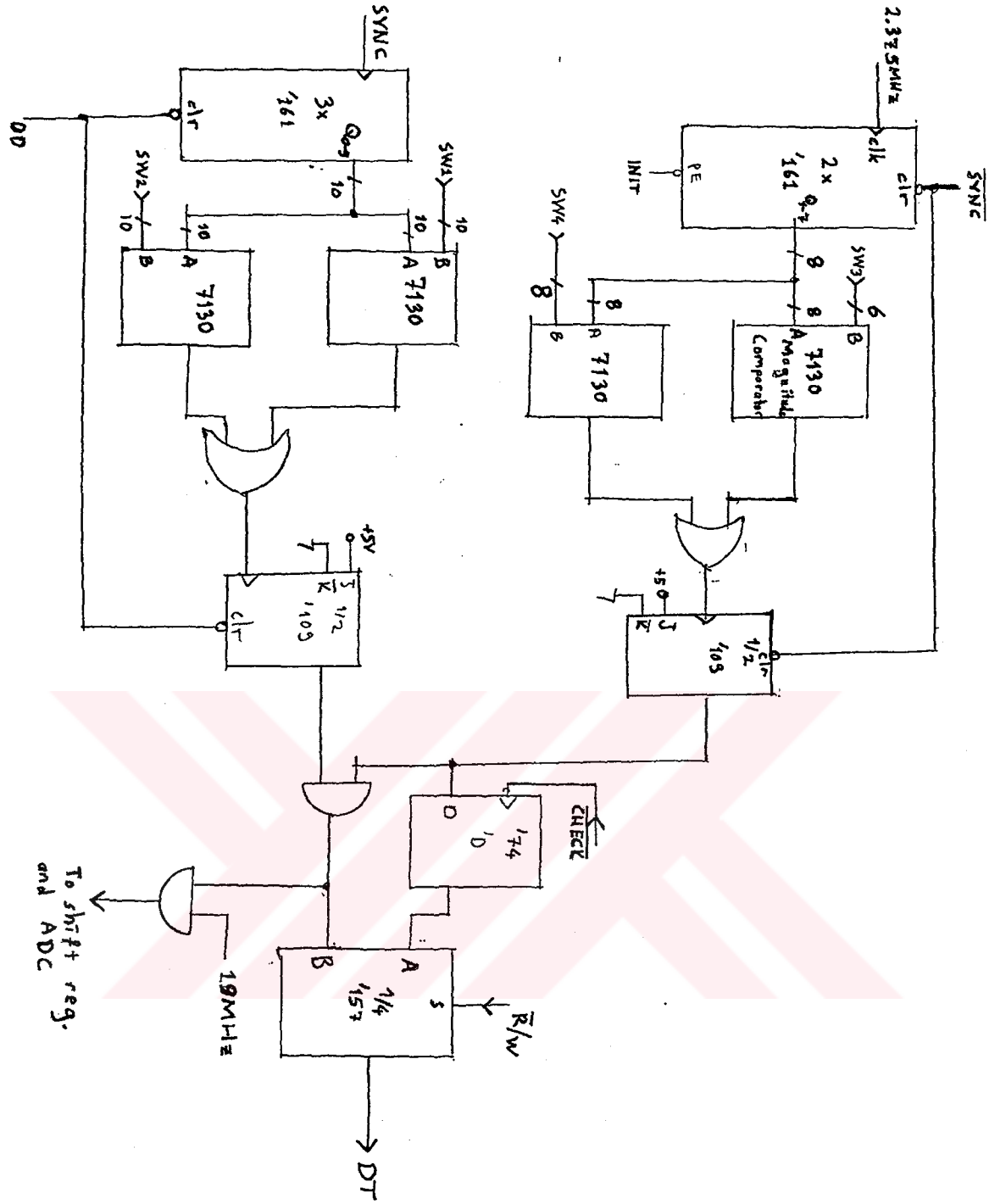


Figure 3.6. Circuit for Selection of Resolution.

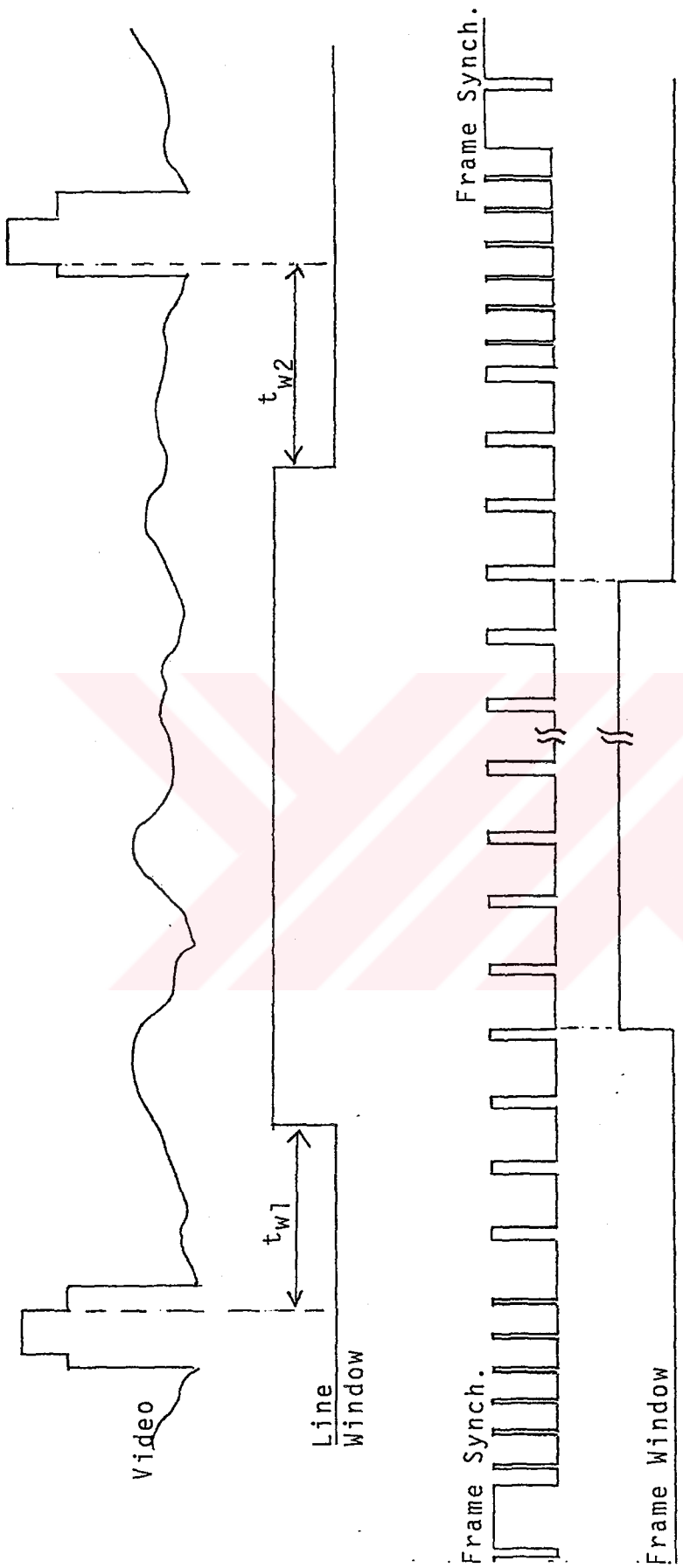


Figure 3.7. Timing Diagram of the Sampling Windows.

RAM devices. These chips are smaller in dimensions and faster when compared to the standard static RAM chips.

Dynamic memories store data in a row and column orientation. 16 address bits are required to decode one of the 65536 cell locations within the 64K*4Bit DRAM. 8 of these address bits decode row address while the other 8 decode column address.These addresses are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, namely the row address strobe (RAS), latches 8 row addresses into the chip while the second clock, the column address strobe (CAS) sequentially latches 8 column addresses into the chip [7].

1MByte memory array is arranged as two 512KByte blocks for storing two sucessive frames of image data. each 512KByte block is arranged as 8 banks of 64 KByte memories. Data is written to and read from the 8 banks at the same time. This provides sufficient time for the memory chips to access data during write cycles and faster reading for the computer during read cycles.

This system generates the strobe signals (RAS, CAS), the read/write mode selection signal (W), the memory output enable signal (OE) and the frame select signal (FRS). In write cycles, the 2.375 MHz RAS signal

is obtained from the third bit of a four bit counter which divides the 19 MHz system clock by eight and the address counters are triggered by the 2.375 MHz clock AND'ed with the sampling window. In read cycles, RAS is sent by the computer and address counters are triggered by the rising edge of this signal. These signals are multiplexed by 2 to 1 multiplexers and given to the system according to the mode of operation. The CAS signal is obtained by giving some delay to the RAS signal using buffers as delay elements. The R/W signal of the system is inverted to generate the W signal for the memory array. During read and write operations, a signal is generated to select the memory block to which data would be written or read from. This signal,namely FRS selects the first block if the first frame is being recorded or read and selects the second block if second frame is being processed. A two bit counter counts the start of each odd field after the START signal is received. Second bit of this counter determines the value of the FRS signal. The counter outputs are also given to the input of a NAND gate to generate the R/W signal of the system.

Dynamic memory devices must be refreshed at every 4 milliseconds otherwise they lose the data stored in them. For refreshing an 8-bit address counter and a tri-state octal latch is used. During write cycles

refreshing is performed within the time interval when there is no recording process being held, that is, outside the sampling window. During read cycles, a window is generated by the system. Computer sends RAS signal and eight successive data are transferred to the output buffers of the memory. The computer then sends a check (CHK) signal and refreshing starts if the line window signal is low during the high to low transition of CHK.If refresh takes place, the computer reads the data in 8 buffers and waits for the end of refresh otherwise it continues to read the data, sending signals in the same order. This brings more efficient use of time because the computer can read data during refresh cycles. The circuit diagram of the memory control hardware is illustrated in figure 3.8.

3.2. MEMORY BUFFERS AND MEMORY ARRAY

Since data sampling rate is too fast for any personal computer to handle, a temporary data storage unit is needed for acquisition of data at 19MHz wihout any loss of data. Later this data is transferred to the microcomputer for long term storage and post processing.

The memory array is formed with dynamic RAM devices of 64K*4Bit organization. 32 chips are used to form 1MByte of memory. These devices have a minimum access time of 120 nanoseconds which is slower than the

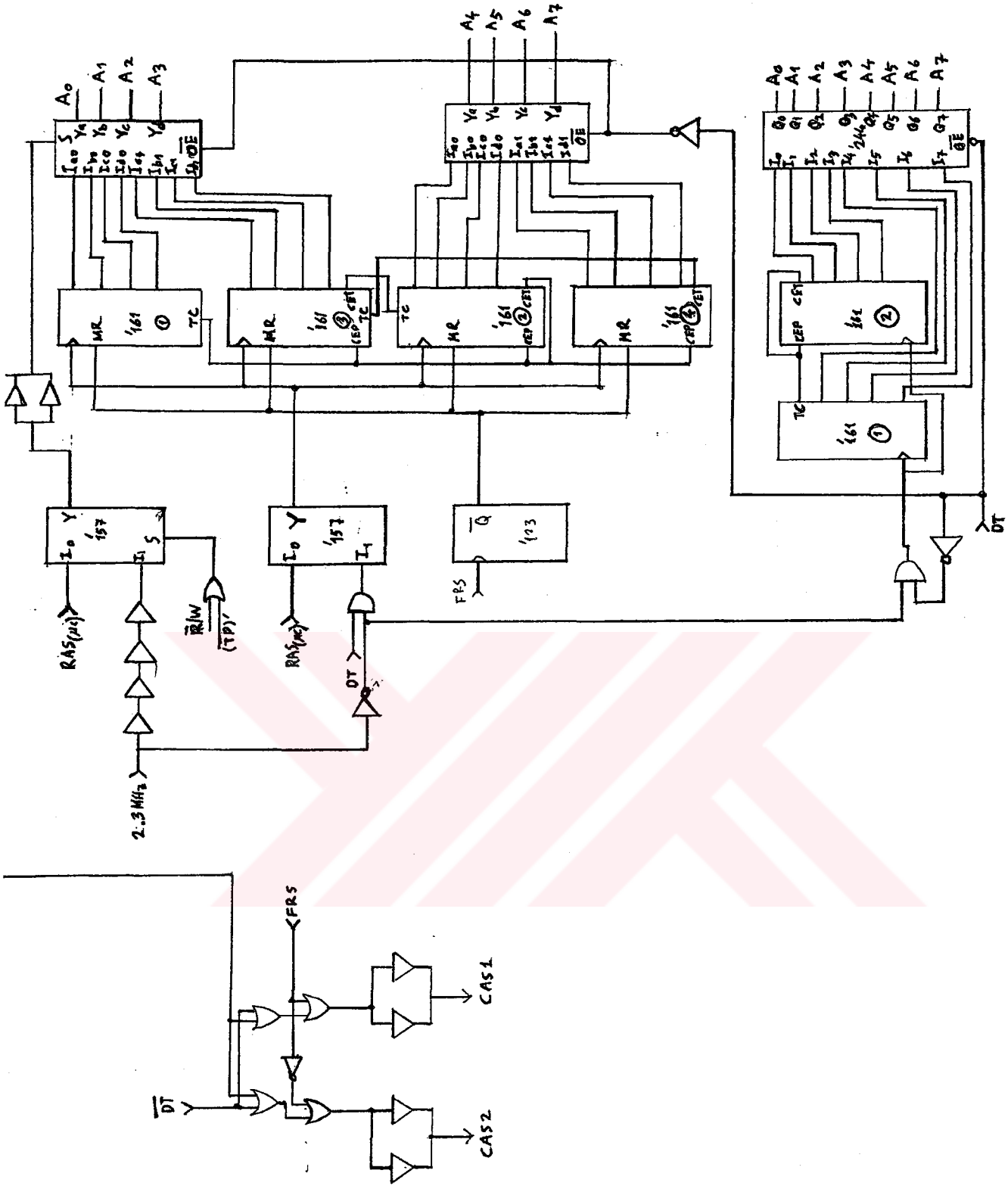


Figure 3.8. Memory Control Hardware.

sampling rate of the system. Hence an additional buffer circuit must be used to decrease the speed of data during storage without any loss in data acquisition rate and data sampled.

3.2.1 Memory Input Buffer

A memory input buffer is designed to decrease the speed of data sampled for storage into the memory while achieving 19MHz data acquisition rate.

The memory input buffer packs eight consecutive data and transfer them to the memory at a rate eight times less than the data input rate. Each block of memory is organized as eight banks, therefore eight consecutive data are written into the same address location of each bank at the same time [1]. This is illustrated in figure 3.9.

$Bank_0$	$Bank_1$	$Bank_2$	$Bank_3$	$Bank_4$	$Bank_5$	$Bank_6$	$Bank_7$
$D_{0,n}$	$D_{0,n+1}$	$D_{0,n+2}$	$D_{0,n+3}$	$D_{0,n+4}$	$D_{0,n+5}$	$D_{0,n+6}$	$D_{0,n+7}$
$D_{1,n}$	.....	.....	.....	.....	.....	.....	$D_{1,n+6}$
$D_{2,n}$	.....	.....	.....	.....	.....	.....	$D_{2,n+6}$
$D_{3,n}$	.....	.....	.....	.....	.....	.....	$D_{3,n+6}$
$D_{4,n}$	.....	.....	.....	.....	.....	.....	$D_{4,n+6}$
$D_{5,n}$	.....	.....	.....	.....	.....	.....	$D_{5,n+6}$
$D_{6,n}$	.....	.....	.....	.....	.....	.....	$D_{6,n+6}$
$D_{7,n}$	$D_{7,n+1}$	$D_{7,n+2}$	$D_{7,n+3}$	$D_{7,n+4}$	$D_{7,n+5}$	$D_{7,n+6}$	$D_{7,n+7}$

$D_{0,n}$: Least significant bit of nth data
$D_{7,n+7}$: Most significant bit of $(n+7)^{th}$ data

Figure 3.9. Memory Input Data Configuration

The memory input buffer consists of eight 8-bit serial to parallel shift registers and eight tri-state octal D flip-flops. Each one of the 8-bit data output of the A/D conversion unit is connected to the input of an 8-bit serial to parallel shift register and shifted by the clock of the A/D converter. When eight successive data bytes are stored in the shift registers, they are transferred to the memory through eight octal D flip-flops. Circuit diagram and the timing diagram of the memory buffer are given in figure 3.10 and 3.11 respectively.

3.2.2. Memory Array

The memory array serves to store the samples of two successive frames of video signals. It is organized as 2 blocks of 512KByte (64K*8bit and 2*8banks) capacity. The block diagram of the memory array is given in figure 3.12.

The memory buffer outputs are written, at the same time, into the eight memory banks of a 512Kbyte block which is selected by the FRS signal. This operation is performed at a rate of 2.375MHz. When a frame of image data is stored in the first block, second block is selected for storage of the second frame.

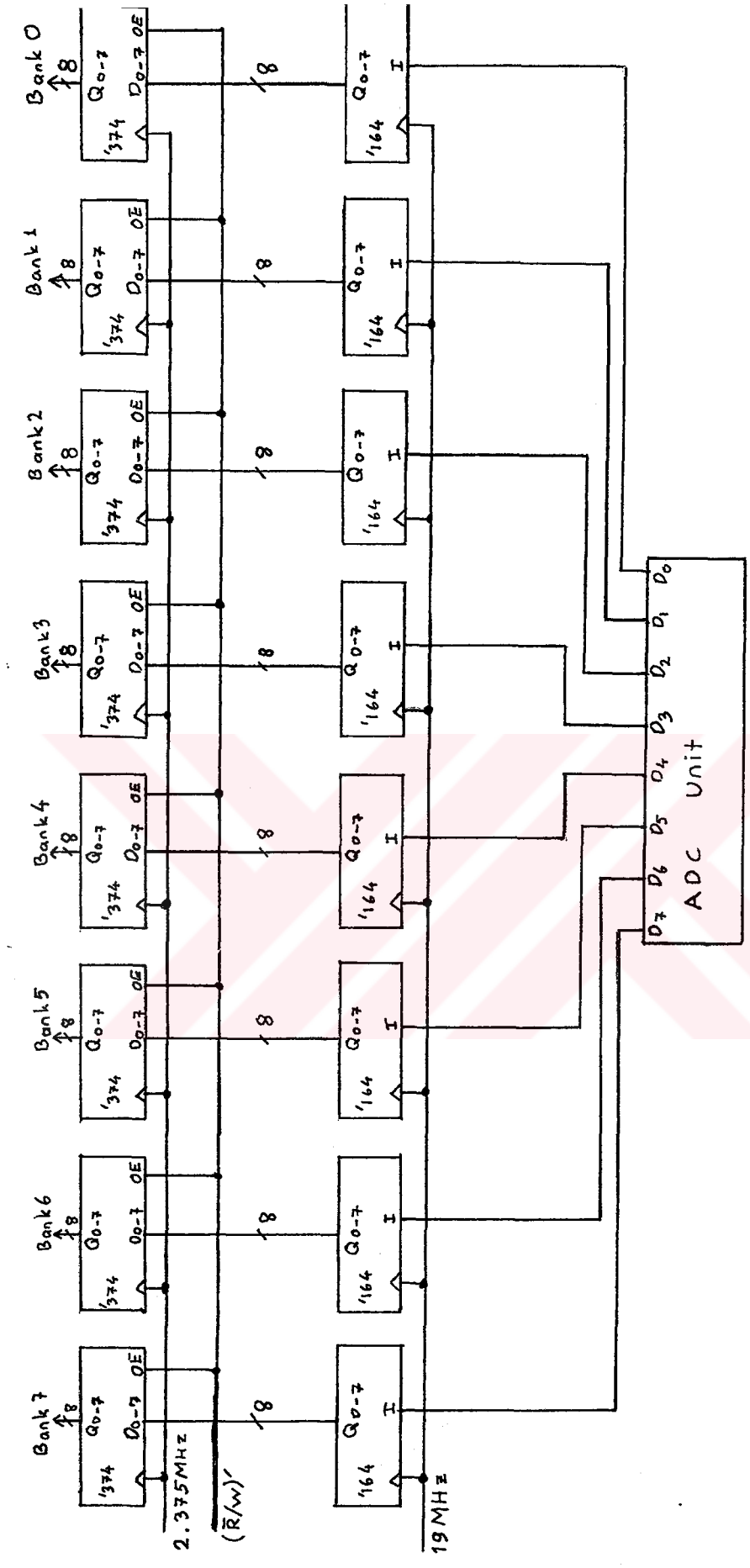


Figure 3.10. Circuit Diagram of the Memory Input Buffer.

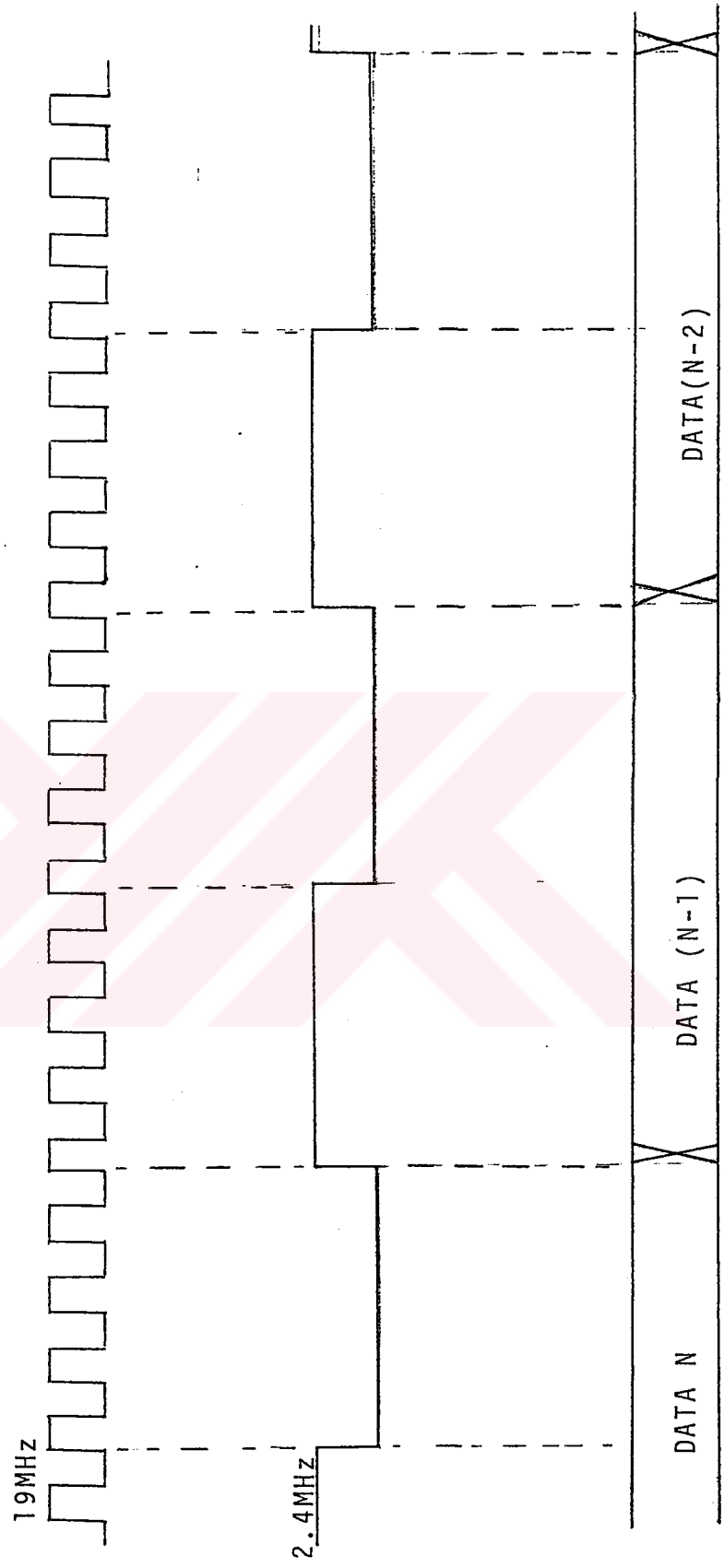


Figure 3.11. Timing Diagram of the Memory Input Buffer.

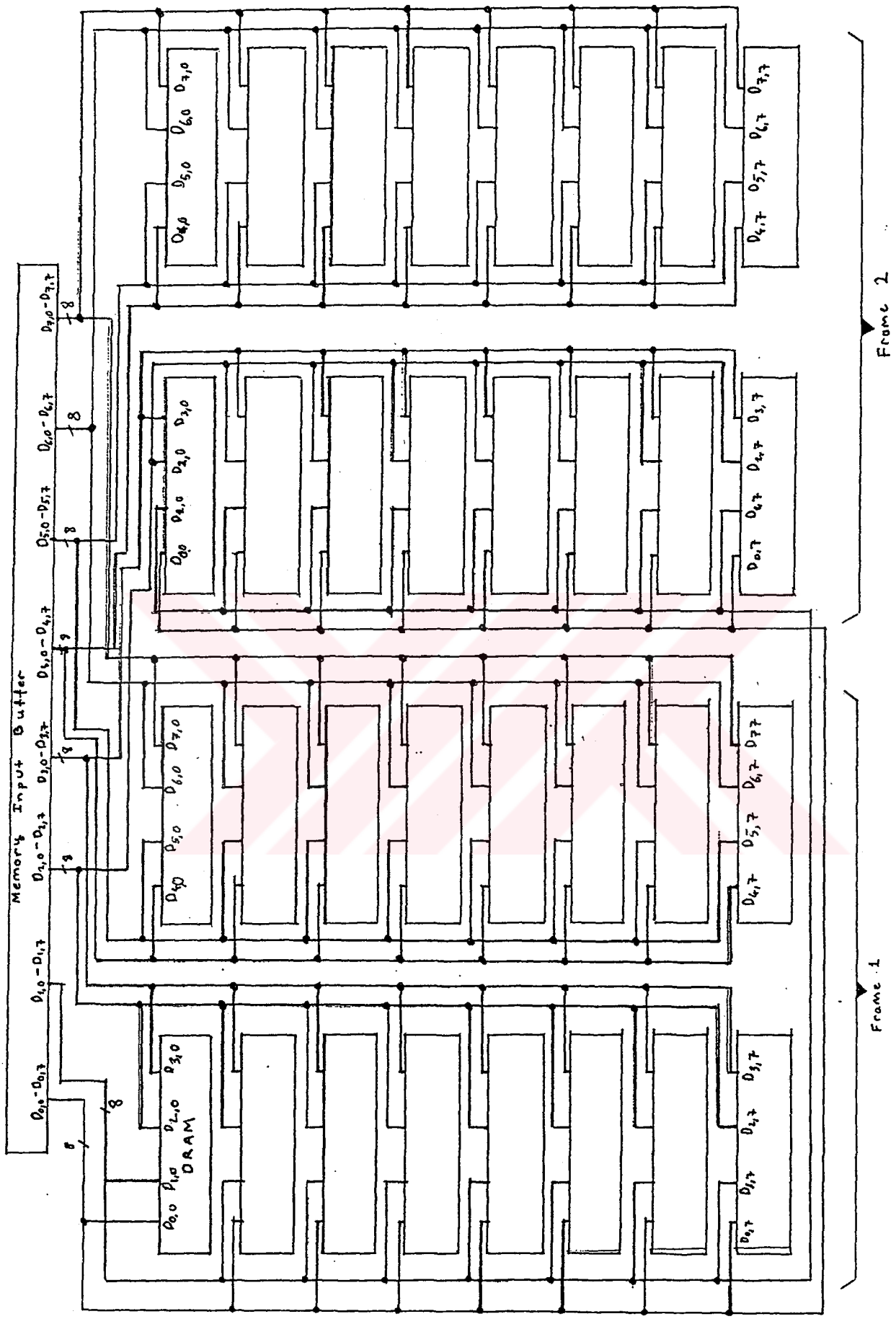


Figure 3.12. Memory Array.

In one of the memory banks, $BANK_n$, the address location m contains the $(m*8+n)^{th}$ byte of the data sequence which are generated by the flash A/D converter.

The RAS signal and the address bits are sent to the two blocks at the same time. Only CAS is disabled by the FRS signal. This provides an opportunity to refresh the other block while writing to or reading from or refreshing one of the blocks.

In read cycles, data is transferred to eight output buffers from eight banks of a block in the same manner as in write cycles. Then data is read by the computer sequentially from these buffers.

3.2.3 Memory Output Buffers

The computer performs read operation by sending a single address. Memory addressing is performed by the address counters of the system which are triggered by the RAS signal sent by the computer. Output buffers are loaded with eight successive data from eight banks of a block at the same time with the rising edge of the RAS signal. Then a decoding logic, whose circuit diagram is given in figure 3.13, sequentially enables the eight output buffers with the RB signal sent by the computer.

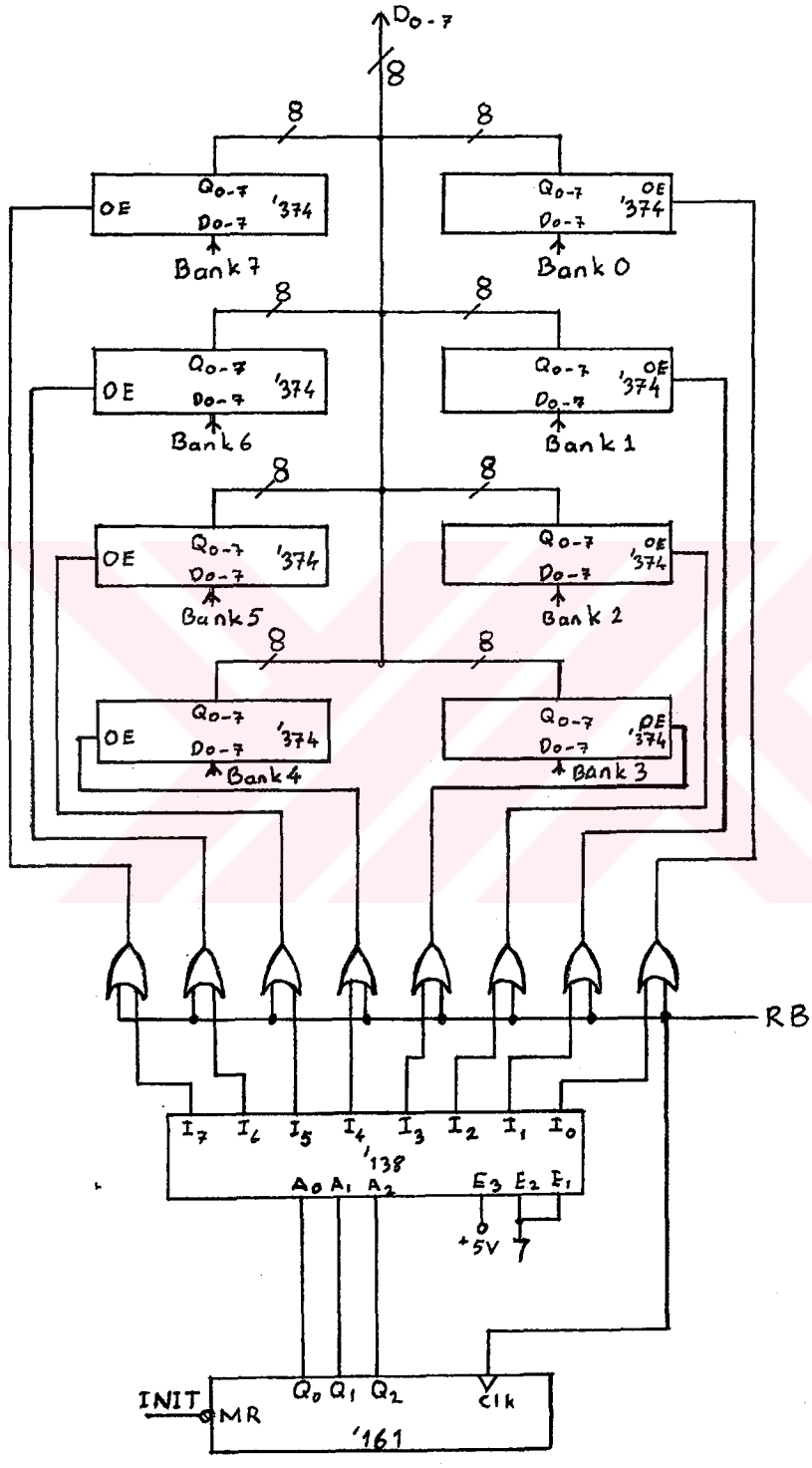


Figure 3.13. Memory Output Buffers Decoding Logic.

The decoding logic employs a four bit counter, a 3 to 8 decoder and eight two input OR gates. The counter is triggered by the RB signal and the counter outputs are connected to the decoder. Each output of the decoder is connected to an OR gate together with the RB signal. Each OR gate output enables the output buffers sequentially to release the data to the computer's data bus during that read cycle.

3.3. DATA ACQUISITION AND FRAME DISPLAY SOFTWARE

A software is needed for the acquisition of the data from the designed hardware and for processing this data in the computer.

Two programs are written for this purpose. The first program acquires the data from the temporary memory of the system and the second one display this data on the IBM-AT monitor.

3.3.1. Data Acquisition Software

This program generates necessary codes for system initialization and to start data acquisition. Then the computer waits for the system to finish the acquisition of data. When the circuit goes into the read mode the computer starts reading the data. During reading, the

refresh cycles of the system memory is also checked. The data read is arranged as a screen matrix according to the selected dimensions of the image data acquired. This matrix is saved onto the hard disk for post processing.

The program is written in Pascal programming language [8] and listing is given in Appendix A.

3.3.2. Frame Display Software

In this work, as a demonstration of the operation of this system, a software is developed to display the image acquired by the designed hardware.

The resolution of the monitor of IBM-AT is at most 720 columns by 348 rows with the Hercules graphics card and 640 columns by 200 rows with the CGA graphics card. The screen matrix formed by the data acquired is generally larger than the resolution of the monitor of IBM-AT. Therefore, an averaging technique must be used to decrease the size of the screen matrix for plotting on the computer's monitor. The second point is that IBM-AT monitor has no gray level with the Hercules or CGA graphics cards. The software must define gray levels to form the image if the monitor of the microcomputer used has no gray level. There are, however, a wide variety of graphics cards for IBM-AT microcomputer, which have higher resolution and have gray levels. With these

graphics cards, it is possible to obtain an image without loss of resolution.

Averaging is done by assigning the average value of points in a region to the point in the center of that region. To obtain gray levels, a 3*3 pixel (picture element) is defined and according to the intensity of light, points are plotted in that pixel. Nine points define white level while no points define the black level. This gives ten gray levels on the monitor.

CHAPTER 4

RESULTS AND CONCLUSIONS

A microcomputer based high speed image data acquisition device is designed and implemented to store two successive frames of image data for use in medical imaging systems.

Major problems faced during the design were the limited size for the printed circuit board, limited power supply capacity and the rate of data acquisition which can not be handled by any memory device in the market except for some special cache memory devices. But these devices have low capacity and therefore it would not be practical to use these devices for a 1MByte memory array.

The problem of the size of the printed circuit board is solved by mounting the circuit on two seperate printed circuit boards. The first board contains the control hardware while the second board contains the memory buffers and the memory array. The memory board is mounted on the control board by connectors.

Dynamic RAM chips have smaller size than the standard static RAM chips. They also have lower power consumption. Hence using dynamic memory devices brought

a solution to size problem and the power supply problem. But dynamic RAM chips have low access time when compared to the data acquisition rate. This is compensated using a special buffer configuration that is explained in chapter 3.

The computer can supply limited amount of power to its expansion slots[6]. Therefore minimum amount of power consumption constraint must be considered during the design. For this purpose, low power shottky (LS) chips are used for the whole design.

Another problem arouse in the design of the input companding amplifier. Conventionally, a logarithmic amplifier should be used since it has a simpler and more definite transfer characteristic. In addition to that X-Ray sources generate signals in which the information carried is exponentially related to the medium properties through which the energy is passed. But it is a very difficult task to implement a logarithmic amplifier with a bandwidth about 10MHz. To solve this problem, a transistor differential amplifier is designed whose transfer characteristic is kept close to a logarithmic curve by adjusting the circuit parameters. Further corrections are made with the software to get ideal logarithmic response.

REFERENCES

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[2] Harold, E.E, "Television Broadcasting: Equipment, Systems and Operating Fundamentals", pp. 260-269, Howard W. Sams & Co., Inc., Indianapolis, 1971.

[3] TRW VLSI Databook,1985.

[4] Clarke, K.K., Hess, D.T., "Communication Circuits: Analysis and Design", pp. 114-120, Addison Wesley, 1971.

[5] Stone, H.S., "Microcomputer Interfacing" Addison Wesley, 1982.

[6] IBM-AT Technical Reference Manual, 1984.

[7] Hitachi IC Memory Databook, 1988.

[8] Turbo Pascal Version 3.0 Reference Manual, 1985.

[9] Philips Data Handbook, TTL Logic Series, 1986.

[10] Hitachi IC Memory Products, 1986.

APPENDICES

APPENDIX A

SYSTEM SOFTWARE

In this part, the program listing of the data acquisition software and the display software are given. These programs are written for demonstration purposes and they can handle 120 KByte of data (400 * 300 samples).

A.1. DATA ACQUISITION SOFTWARE

```
{        THIS PROGRAM GENERATES NECESSARY CODES        }
{       TO COMMUNICATE WITH THE DESIGNED SYSTEM        }

program datatake;

  type  imgp =^img;
        img = record
        imagearr:array[1..400,1..150] of byte;
        end;
  var imp1,imp2,imp3            :imgp;
      image                     :file of img;
      frs,a,b,c,d,p,maxx,maxy   :integer;
      ch,check,ok               :byte;
      start,init                :char;

BEGIN
     new(imp1);
     new(imp2);
     new(imp3);
     port[$120]:=0;  {                        }
     port[$100]:=0;  {  FOR ADDRESS COUNTER   }
     port[$100]:=0;  {     INITIALIZATION     }
     repeat
       writeln('PRESS I FOR INITIALIZATION');
       readln(init);
     until((init='i') or (init='I'));

     port[$150]:=0;        {INITIALIZE THE SYSTEM}

     repeat
       writeln('PRESS S FOR START');
       readln(start);
     until ((start='s') or (start='S'));
     port[$120]:=0;        {SEND THE START COMMAND}
     writeln(' WAITING FOR END OF RECORDING');
     repeat
          check:=port[$160];
     until (1 and check)=0;    {CHECK FOR END OF RECORDING}

     frs:=1;
     writeln('INPUT THE NUMBER OF COLUMNS');
     readln(maxx);
     writeln('INPUT THE NUMBER OF ROWS');
     readln(maxy);
     for frs:=1 to 2 do
```

```
          begin
CLRSCR;
          writeln('RECORDING STARTED');
          port[$100]:=0;
               b:=1;
      repeat check:=port[$160] until (2 and check)=2;
               while b<=maxy do
                  begin
                    a:=1;
                      while a<=maxx do
                       begin
                        for p:=1 to 100 do frs:=1;
                        port[$110]:=0;          {send ras}
                        imp1^.imagearr[a,b]:=port[$140];
                        imp1^.imagearr[a+1,b]:=port[$140];
                        imp1^.imagearr[a+2,b]:=port[$140];
{SEND BUFFER}           imp1^.imagearr[a+3,b]:=port[$140];
{READ SIGNAL}           imp1^.imagearr[a+4,b]:=port[$140];
{TO READ ODD}           imp1^.imagearr[a+5,b]:=port[$140];
{FIELD      }           imp1^.imagearr[a+6,b]:=port[$140];
                        imp1^.imagearr[a+7,b]:=port[$140];
                        a:=a+8;
                       end;
                     b:=b+1;
                   end;
                   port[$100]:=0;   {send frs}
                 end;
  b:=1;
               while b<=maxy do
                  begin
                    a:=1;
                      while a<=maxx do
                       begin
                        for p:=1 to 100 do frs:=1;
                        port[$110]:=0;          {send ras}
                        imp2^.imagearr[a,b]:=port[$140];
                        imp2^.imagearr[a+1,b]:=port[$140];
{READ EVEN}             imp2^.imagearr[a+2,b]:=port[$140];
{FIELD    }             imp2^.imagearr[a+3,b]:=port[$140];
                        imp2^.imagearr[a+4,b]:=port[$140];
                        imp2^.imagearr[a+5,b]:=port[$140];
                        imp2^.imagearr[a+6,b]:=port[$140];
                        imp2^.imagearr[a+7,b]:=port[$140];
                        a:=a+8;
                       end;
                     b:=b+1;
                   end;
for b:=1 to maxy do
   for a:= 1 to maxx do
    begin
imp3^.imagearr[a,b]:=(imp1^.imagearr[a,b]+imp2^.imagearr[a,b]) div 2;
    end;
        assign(image,'image.dat');
        rewrite(image);
        write(image,imp3^);
```

```
      close(image);

    Writeln('DATA TRANSFER IS COMPLETED');
    dispose(imp3);
    dispose(imp2);
    dispose(imp1);
END.
```

A.2. FRAME DISPLAY SOFTWARE

```
    {THIS PROGRAM READS THE DATA ACQUIRED BY THE                }
    {DIGITIZER HARDWARE AND PLOTS IT ON THE COMPUTER'S          }
    {MONITOR                                                    }


{$i typedef.sys}
{$i graphix.sys}
{$i kernel.sys}

type  dtp = ^dataarr;
      dataarr  = record
          data:array[1..400,1..150] of byte;
      end;

var
  dd,dav                                  : dtp;
  m,n,xc,yc,i,j,k,l,mm,nn,sum,m1,n1 : integer;
  datafile                                : file of dataarr;
  inten                                   : real;
  maxi,mini                               : byte;

BEGIN

   assign(datafile,'image.dat');
   reset(datafile);
   new(dd);
   new(dav);
   read(datafile,dd^);
maxi:=0;
mini:=255;
mm:=2;
nn:=2;
for j:=1 to 400 do            {FIND MAXIMUM AND MINIMUM     }
   for i:=1 to 140 do         {VALUES OF THE ACQUIRED DATA  }
       begin
           if dd^.data[j,i]>maxi then maxi:=dd^.data[j,i];
           if dd^.data[j,i]<mini then mini:=dd^.data[j,i];
       end;
writeln('MAXIMUM=    ',maxi);
writeln('MINIMUM=    ',mini);
  for m:=1 to 199 do
     for n:=1 to 74 do
       begin
         sum:=0;
         for k:=2*m-1 to 2*m+1 do       {TAKE THE AVERAGE    }
           for l:=2*n-1 to 2*n+1 do   {TO DECREASE THE SIZE}
                   sum:=sum+dd^.data[k,l]; {OF DATA         }
```

```
      dav^.data[m,n]:=sum div 9;
    end;

INITGRAPHIC;

    for j:=1 to 199 do        {DEFINE GRAY LEVELS AND}
       for i:=1 to 74 do      {PLOT ON THE MONITOR    }
         begin
                            if (dav^.data[j,i]<>0) then
                 begin

                 inten:=((dav^.data[j,i]-mini)/(maxi-mini))*10;
            xc:=3*j;
            yc:=3*i;
 if inten>1 then
    begin
    dp (xc,yc);
   if inten>2 then
      begin
      dp (xc-1,yc-1);
     if inten>3 then
        begin
        dp (xc+1,yc+1);
       if inten>4 then
          begin
          dp (xc-1,yc+1);
         if inten>5 then
            begin
            dp (xc+1,yc-1);
           if inten>6 then
              begin
              dp (xc-1,yc);
             if inten>7 then
                begin
                dp (xc+1,yc);
               if inten>8 then
                  begin
                  dp (xc,yc-1);
                 if inten>9 then
                    dp (xc,yc+1);
    end;
      end;
        end;
          end;
            end;
              end;
                end;
                  end;
                    end;

     repeat until keypressed;
```

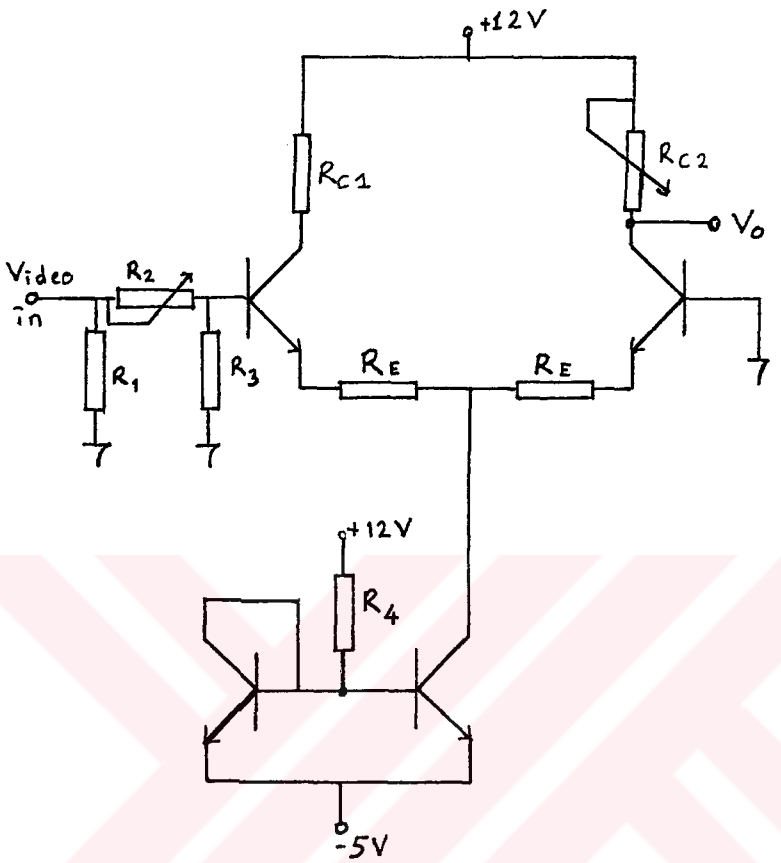
```
        LEAVEGRAPHIC;
        dispose(dav);
        dispose(dd);
        close (datafile);

END.
```

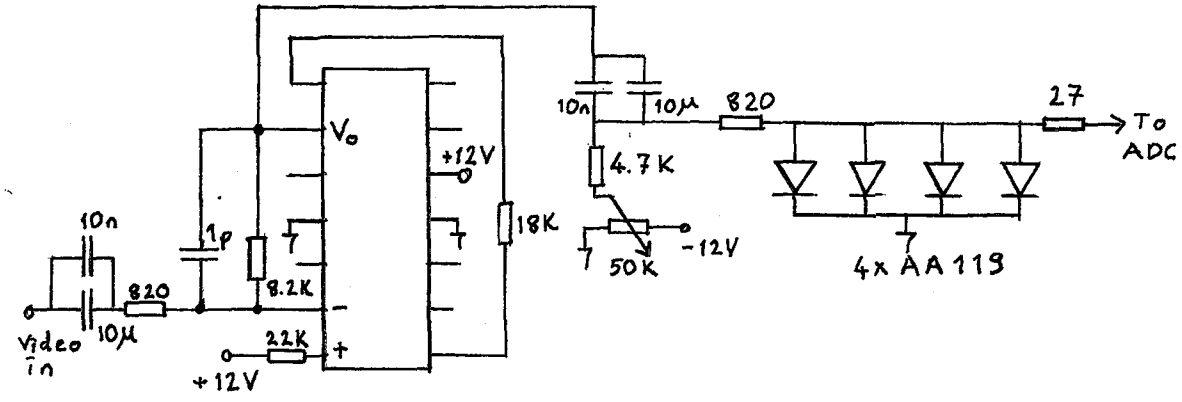
APPENDIX B

CIRCUIT DIAGRAMS AND LAYOUTS

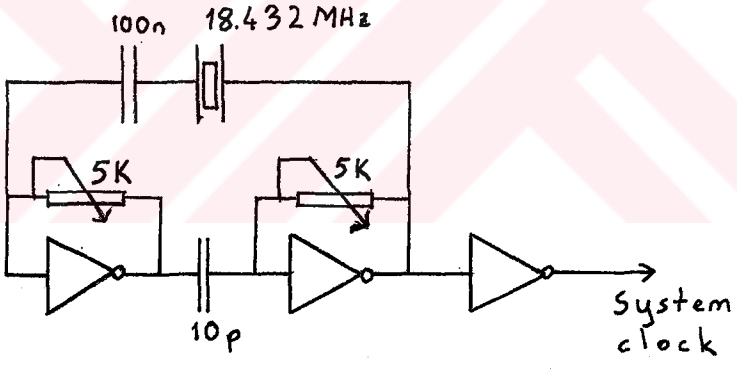
In this section, circuit diagrams which are not given in the other sections are included together with the circuit layouts and parts list. In these diagrams, DC coupling capacitors are not shown.



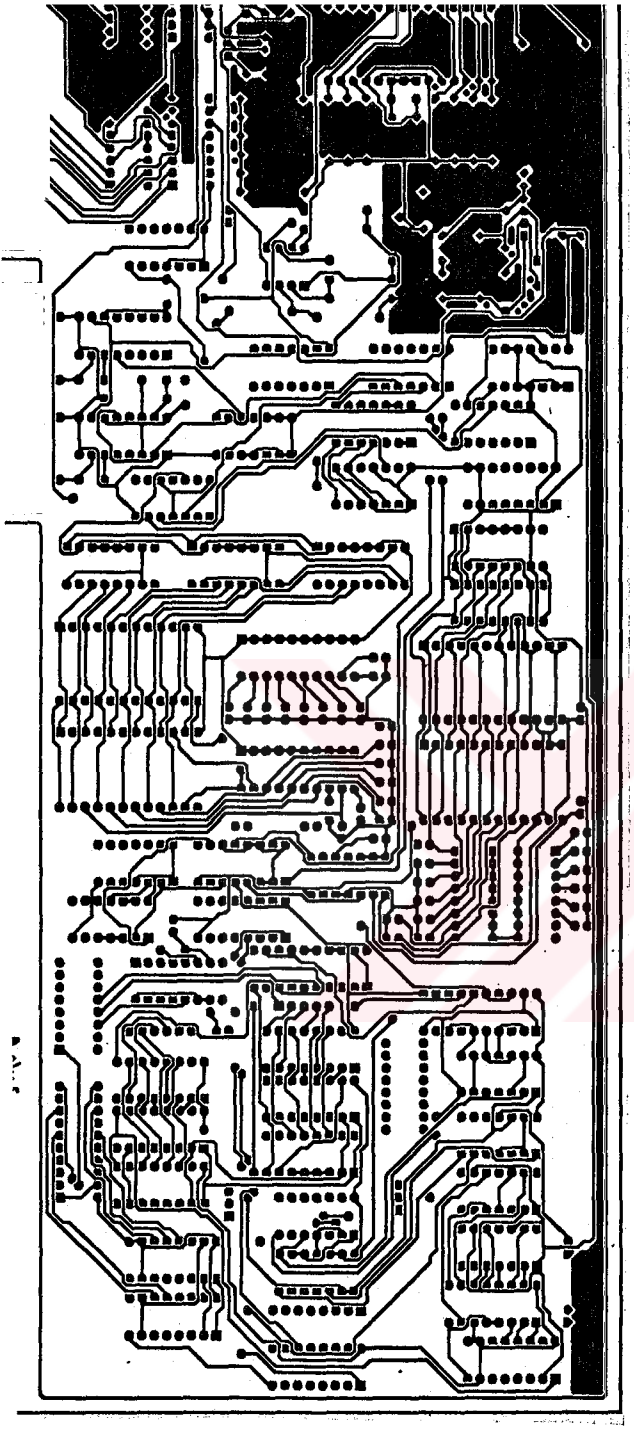
Input Compander Amplifier

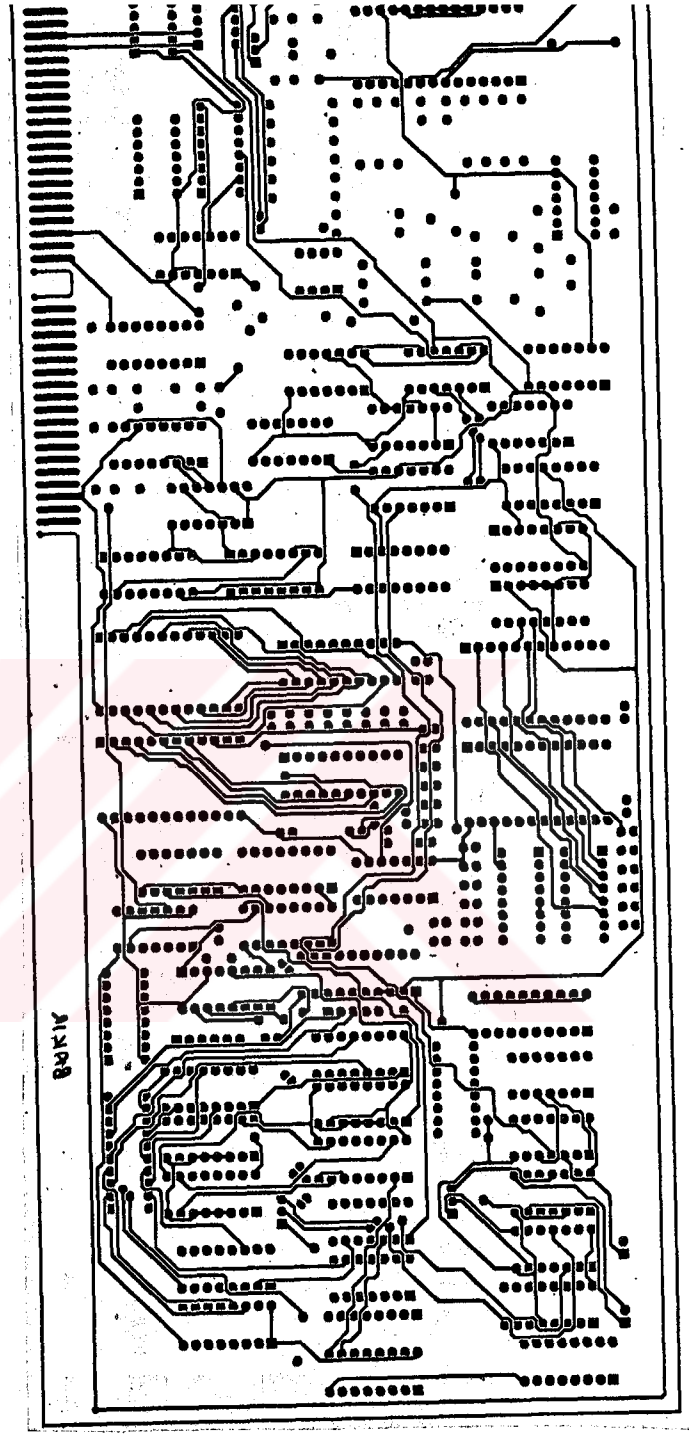


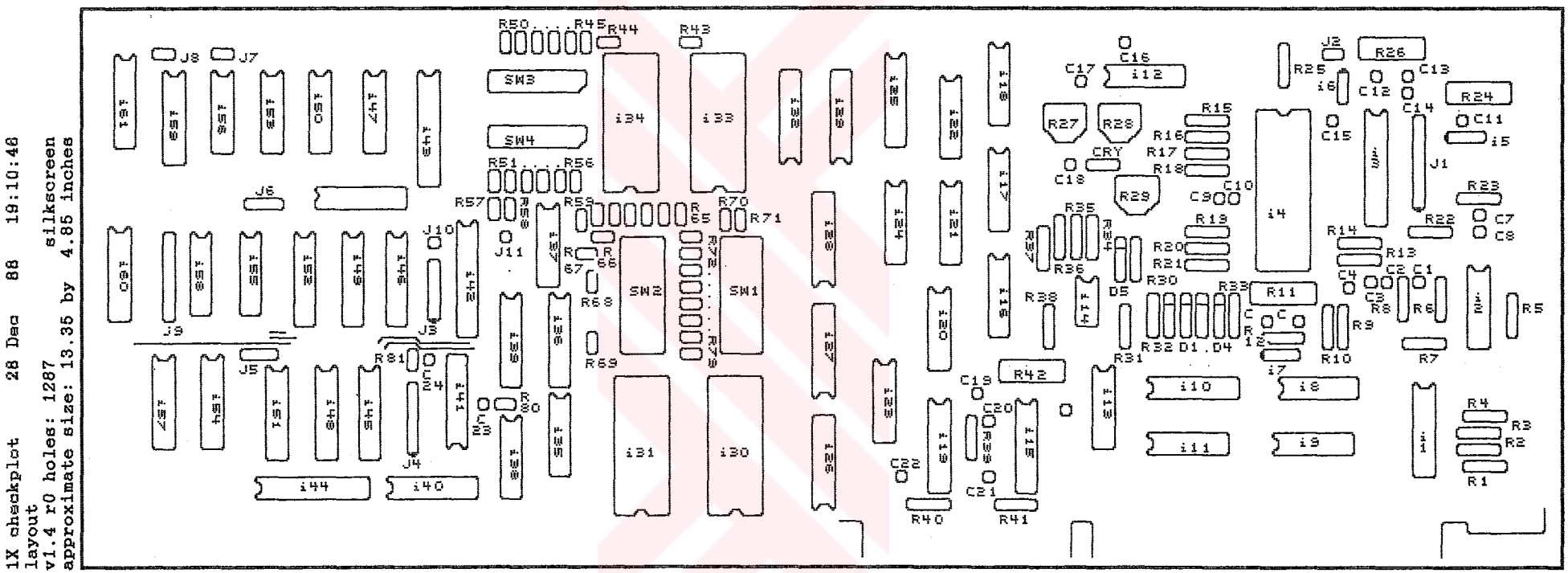
ADC Block Analog Input Buffer Amplifier



System Clock Generator







8.4.1. Control Board Layout

B.4.2. Control Board Parts List

Symbol	Type	Description
I1	CA 3127	High frequency NPN transistor array
I2	LM 359	High frequency Norton current amplifier
I3	74LS374	Octal D flip flops with tri-state output
I4	TDC1048	8-Bit flash A/D converter
I5-7	LM337T	Negative voltage regulator
I8	74LS08	Quad two input AND gate
I9	74LS125	Quad tri-state latch
I10	74LS138	3 to 8 decoder
I11	74LS32	Quad two input OR gate
I12	74ALS04	Hex inverter
I13	74LS107	Dual negative edge triggered J-K flip flop
I14	LF353	Dual FET input op-amp
I15	74LS123	Dual retriggerable monostable multivibrator
I16	74LS125	Quad tri-state latch
I17	74LS74	Dual edge triggered D flip flop
I18	74LS08	Quad two input AND gate
I19	74LS123	Dual retriggerable monostable multivibrator
I20	74LS08	Quad two input AND gate
I21	74LS00	Quad two input NAND gate
I22-23	74LS74	Dual edge triggered D flip flop
I24	74LS107	Dual negative edge triggered J-K flip flop
I25-29	74LS161	Four bit binary counter
I30-31	DM7130	Ten bit magnitude comparator
I32	74LS161	Four bit binary counter

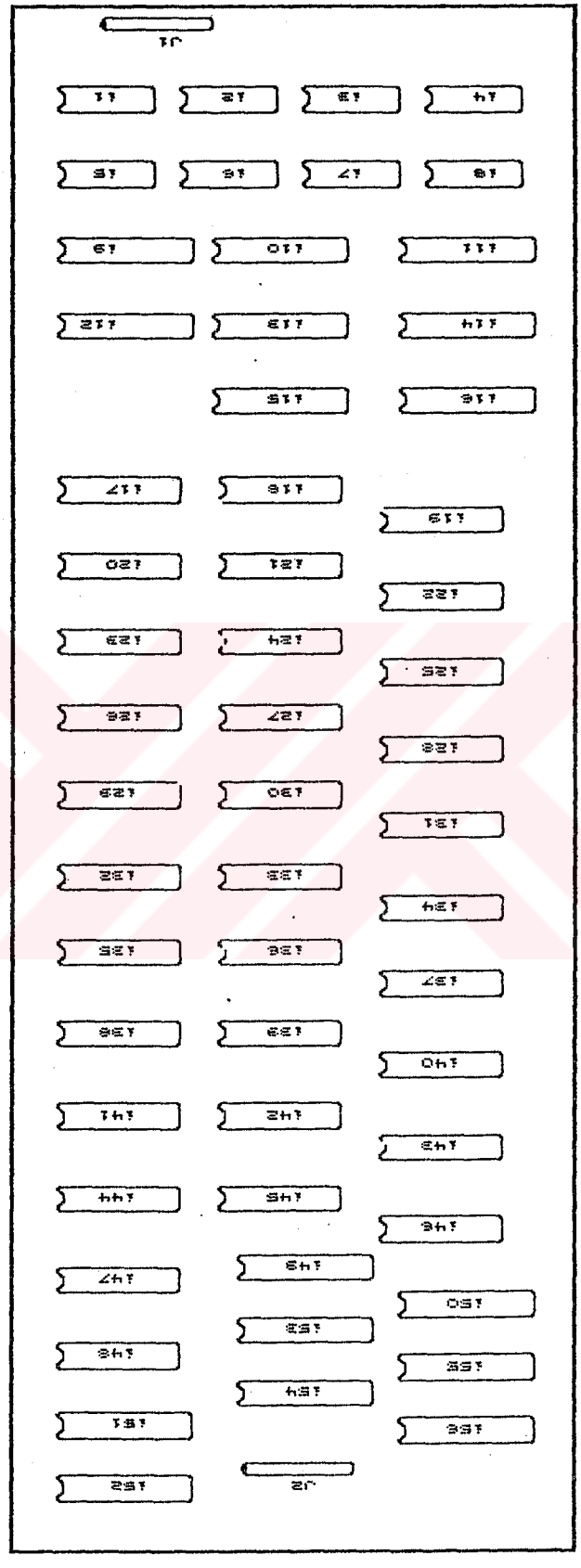
Symbol	Type	Description
I33-34	DM7130	Ten bit magnitude comparator
I35	74LS74	Dual edge triggered D flip flop
I36	74LS109	Dual positive edge triggered J-K flip flop
I37	74LS32	Quad two input OR gate
I38	74LS00	Quad two input NAND gate
I39-40	74LS157	Quad 2 to 1 multiplexer
I41	74LS123	Dual retriggerable monostable multivibrator
I42-44	74LS244	Octal buffers tri-state
I45-46	74LS257	Quad 2 to 1 multiplexer with tri-state output
I47	74LS32	Quad two input OR gate
I48-49	74LS161	Four bit binary counter
I50	74LS32	Quad two input OR gate
I51-52	74LS161	Four bit binary counter
I53	74LS32	Quad two input OR gate
I54	74LS161	Four bit binary counter
I55	74LS08	Quad two input AND gate
I56	74LS32	Quad two input OR gate
I57	74LS161	Four bit binary counter
I58	74LS00	Quad two input NAND gate
I59	74LS138	3 to 8 decoder
I60	74LS157	Quad 2 to 1 multiplexer
I61	74LS161	Four bit binary counter
SW1-2		Ten bit DIP switch
SW3-4		Eight bit DIP switch
J1-11		Pin connectors
R1,R4		27 Ohm resistor

R2	5 KOhm potentiometer
R3	820 Ohm resistor
R5	22 KOhm resistor
R6	5 KOhm potentiometer
R7	22 KOhm resistor
R8	820 Ohm resistor
R8	820 Ohm resistor
R9	820 Ohm resistor
R10	2.2 KOhm resistor
R11	100 KOhm potentiometer
R12	4.7 KOhm resistor
R13-21	2.7 KOhm resistor
R22	1.5 KOhm resistor
R23	1.2 KOhm resistor
R24	1.2 KOhm potentiometer
R25	120 Ohm resistor
R26	10 KOhm potentiometer
R27-29	10 KOhm potentiometer
R30	1 KOhm potentiometer
R31	1.2 KOhm resistor
R32	27 Ohm resistor
R33	820 Ohm resistor
R34	1.2 KOhm resistor
R35-38	820 Ohm resistor
R35-39	820 Ohm resistor
R40	4.7 KOhm resistor
R41	5.1 KOhm resistor

R42		50 KOhm potentiometer
R43-44		3.9 KOhm resistor
R45-79		47 KOhm resistor
R80-81		8.2 KOhm resistor
C1		10nF capacitor
C2		10 microfarad capacitor
C3-4		10 microfarad capacitor
C5		1 microfarad capacitor
C6		0.1 microfarad capacitor
C7		0.1 microfarad capacitor
C8		1 microfarad capacitor
C9		0.1 microfarad capacitor
C10		1 microfarad capacitor
C11		1 microfarad capacitor
C12		1 microfarad capacitor
C13		0.1 microfarad capacitor
C14		2.2 microfarad capacitor
C15		2.2 microfarad capacitor
C16		2.2 microfarad capacitor
C17		10 picofarad capacitor
C18		0.1 microfarad capacitor
C19		0.1 microfarad capacitor
C20		4.7 microfarad capacitor
C21		4.7 nanofarad capacitor
C22		2 nanofarad capacitor
C23		1.2 nanofarad capacitor
C24		1 nanofarad capacitor
D1-4	AA119	Germanium diodes

D5	1N4148	Silicon diode

1X checkplot 31Kamhoc4plot01:12:36 Jan 80 01:12:36
b:layo2
v1.4 r0 holes: 1354 silkscreen
approximate size: 12.05 by 4.20 inches



8.5.1. Memory Board Layout

B.5.2. Memory Board Parts List

Symbol	Type	Description
I1-8	74LS164	8-bit serial to parallel shift register
I9-16	74LS374	Octal D flip flops with tri-state output
I17-48	HM50464	64K*4 bit DRAM
I49-56	74LS374	Octal D flip flops with tri-state output

APPENDIX C

DATA SHEETS

In the following pages, data sheets of the flash A/D converter TRW-TDC 1048 and the dynamic memory components HM50464 are given. The information about other components used in the design can be found in their related manuals mentioned in the references section.

TDC1048

Monolithic Video A/D Converter
8-bit, 20MSPS

The TRW TDC1048 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28 lead package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

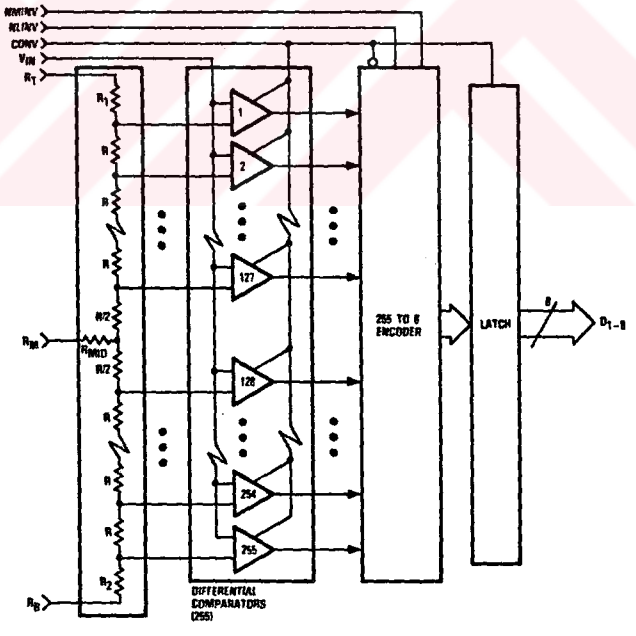
Features

- 8-Bit Resolution
- 20MSPS Conversion Rate
- Low Power Consumption, 1.6W (Worst Case)
- Sample-And-Hold Circuit Not Required
- Differential Phase 1 Degree
- Differential Gain 2%
- 1/2 LSB Linearity
- TTL Compatible
- Selectable Output Format
- Available In 28 Lead DIP, CERDIP, Or Contact Chip Carrier
- Evaluation Board - TDC1048E1C

Applications

- Low-Cost Video Digitizing
- Radar Data Conversion
- Data Acquisition
- Medical Imaging

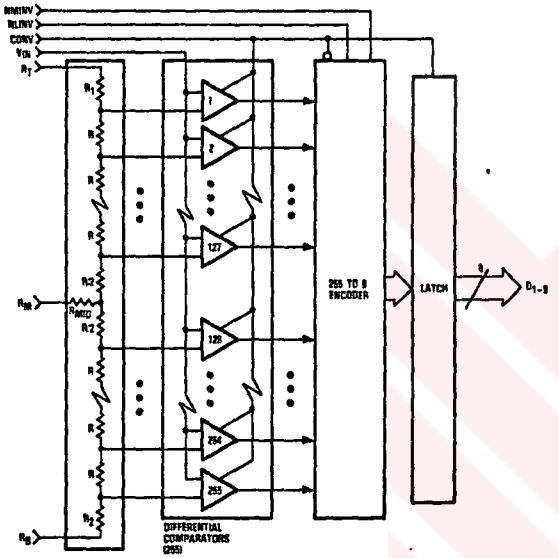
Functional Block Diagram



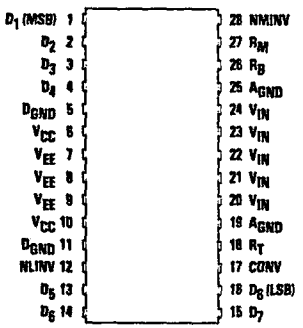
LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

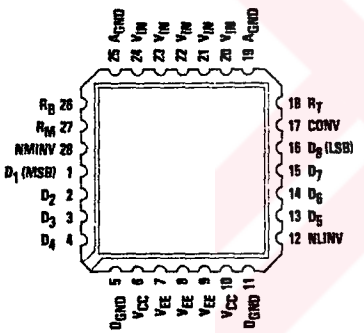
Functional Block Diagram



Pin Assignments



28 Lead DIP – J6 Package
28 Lead CERDIP – B6 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1048 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1048 operates from two supply voltages, +5.0V and -5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the -5.2V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J6, B6, C3 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 6, 10
V_{EE}	Negative Supply Voltage	-5.2V	Pins 7, 8, 9
D_{GND}	Digital Ground	0.0V	Pins 5, 11
A_{GND}	Analog Ground	0.0V	Pins 19, 25

Reference

The TDC1048 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = -2.0V.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a nonlinear transfer function. The circuit shown in Figure 5 will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance seen at this node is approximately 220 Ohms, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and noise introduced at this point will degrade the quantization process.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an automatic gain control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz.

Name	Function	Value	J6, B6, C3 Package
R_T	Reference Resistor (Top)	0.0V	Pin 18
R_M	Reference Resistor (Middle)	-1.0V	Pin 27
R_B	Reference Resistor (Bottom)	-2.0V	Pin 26

D

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding table on page 121. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J8, B6, C3 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 28
NLINV	Not Least Significant Bit INVert	TTL	Pin 12

Convert

The TDC1048 requires a convert (CONV) signal. A sample is taken (the comparators are latched) within 15ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1048 is taking input sample N + 2.

Name	Function	Value	J8, B6, C3 Package
CONV	Convert	TTL	Pin 17

Analog Input

The TDC1048 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1048 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All five analog input pins must be connected together.

Name	Function	Value	J8, B6, C3 Package
V_{IN}	Analog Signal Input	0V to -2V	Pins 20, 21, 22, 23, 24

Outputs

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LSI unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J8, B6, C3 Package
O_1	MSB Output	TTL	Pin 1
O_2		TTL	Pin 2
O_3		TTL	Pin 3
O_4		TTL	Pin 4
O_5		TTL	Pin 13
O_6		TTL	Pin 14
O_7		TTL	Pin 15
O_8	LSB Output	TTL	Pin 16

Figure 1. Timing Diagram

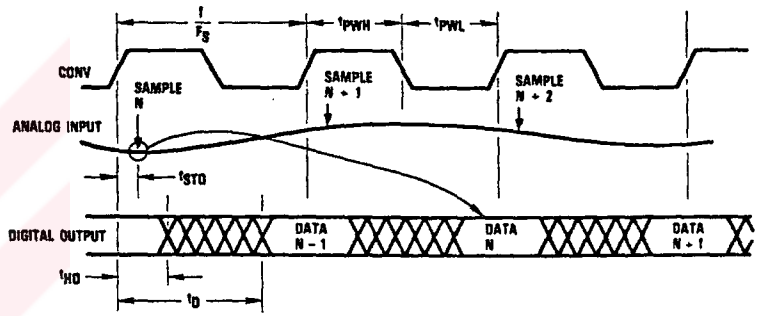


Figure 2. Simplified Analog Input Equivalent Circuit

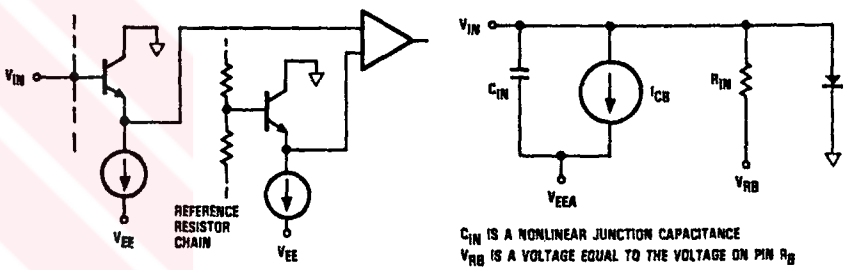


Figure 3. Convert Input Equivalent Circuit

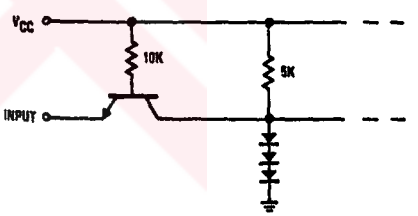
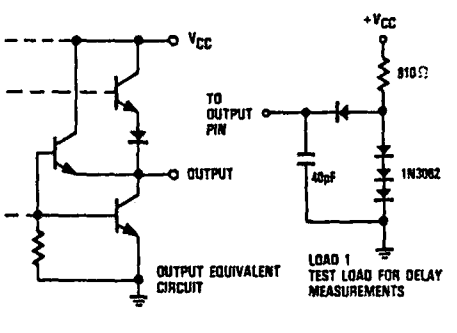


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V[2]
Applied current, externally forced	−1.0 to +8.0mA[3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input[1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		35		40	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		−260			mA
		T_A = 70°C		−185			mA
		T_C = −55°C to 125°C				−320	mA
		T_C = 125°C				−180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35		45	mA
R_{REF}	Total Reference Resistance		67		50		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}		100		100	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		200		550	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V					
		CONV		−0.4		−0.4	mA
		NMINV, NLINV		−0.8		−0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		−30		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
CS	Code Size		25	175	25	175	% Nominal
E_{OT}	Offset Error Top	V_{IN} = V_{RT}		+45		+45	mV
E_{OB}	Offset Error Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Offset Error Temperature Coefficient			±20		±20	µV/°C
BW	Bandwidth, Full Power Input		7		5		MHz
t_{TR}	Transient Response, Full Scale			20		20	ns
SNR	Signal-to-Noise Ratio	20MSPS Conversion Rate, 10MHz Bandwidth					
	Peak Signal:RMS Noise	1.248MHz Input	54		53		dB
		2.438MHz Input	53		52		dB
	RMS Signal:RMS Noise	1.248MHz Input	45		44		dB
		2.438MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase Error	F_S = 4 x NTSC		1.0		1.0	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		2.0		2.0	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20MSPS Conversion Rate	36.5		36.5		dB

Output Coding

Step	Range −2.0000V FS 7.8431 mV STEP	Range −2.0480V FS 8.000 mV STEP	Binary True NMINV = 1 NLINV = 1	Binary Inverted 0 0	Offset Two's Complement True 0 1	Offset Two's Complement Inverted 1 0
000	0.0000V	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	−0.0080V	0000001	1111110	1000001	0111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

Notes:

1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logical "1" and tied to ground for a logical "0"
2. Voltages are code midpoints when calibrated by the procedure given below

Calibration

To calibrate the TDC1048, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_T is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 254 and 255.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 6.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1048. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. All five V_{IN} pins are connected close to the device package, and the buffer amplifier feedback loop should be closed at that point. The buffer has a gain of minus two, increasing a 1 Volt p-p video input signal to the recommended 2 Volt p-p input for the A/D converter. Proper decoupling is recommended for all systems, although the degree of decoupling shown may not be needed. A variable capacitor permits buffer optimization, by either step response or frequency response. This may be replaced with a fixed value capacitor, as determined by the layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.

Figure 5. Typical Reference Midpoint Adjust Circuit

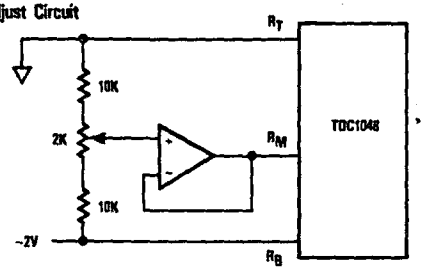
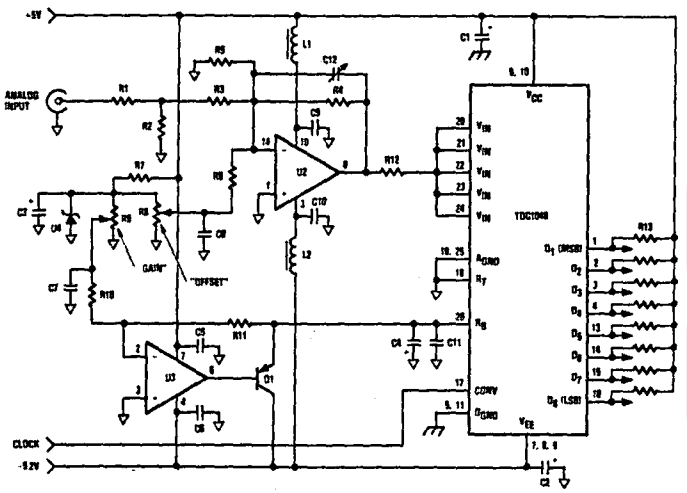


Figure 6. TDC1048 Typical Interface Circuit



Parts List

Resistors

R1	0.0 Ω	1/4W	5%
R2	80.7 Ω	1/4W	5%
R3	1K Ω	1/4W	5%
R4	2K Ω	1/4W	5%
R5	220 Ω	1/4W	5%
R6	2K Ω	1/4W	5%
R7	1K Ω	1/4W	5%
R8	2K Ω	1/4W	Multiturn Pot
R9	2K Ω	1/4W	Multiturn Pot
R10	10K Ω	1/4W	5%
R11	20K Ω	1/4W	5%
R12	27 Ω	1/4W	5%
R13	2.2K Ω	SIP	5%

Capacitors

C1-C4	10μF	25V
C5-C11	0.1μF	50V
C12	1-8pF	variable

Integrated Circuits

U1	TRW TDC1048
U2	HA-2539-5 op-amp
U3	uA741C op-amp
U4	LM313 reference

Transistors

Q1	2N2907

Inductors

L1, L2	Ferrite beads

$$R2 = \frac{1}{\frac{2V_{Range}}{V_{REF}\,Z_{IN}} - 0.001} \qquad R1 = Z_{IN} - \frac{1000\,R2}{1000 + R2}$$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1048J6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead DIP	1048J6C
TDC1048J6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead DIP	1048J6G
TDC1048J6F	EXT-T_C = -55°C to 125°C	Commercial	28 Lead DIP	1048J6F
TDC1048J6A	EXT-T_C = -55°C to 125°C	High Reliability [1]	28 Lead DIP	1048J6A
TDC1048C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1048C3C
TDC1048C3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1048C3G
TDC1048C3F	EXT-T_C = -55°C to 125°C	Commercial	28 Contact Chip Carrier	1048C3F
TDC1048C3A	EXT-T_C = -55°C to 125°C	High Reliability [1]	28 Contact Chip Carrier	1048C3A
TDC1048B6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead CERDIP	1048B6C
TDC1048B6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead CERDIP	1048B6G

Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

Note:

1. Per TRW document 72231757

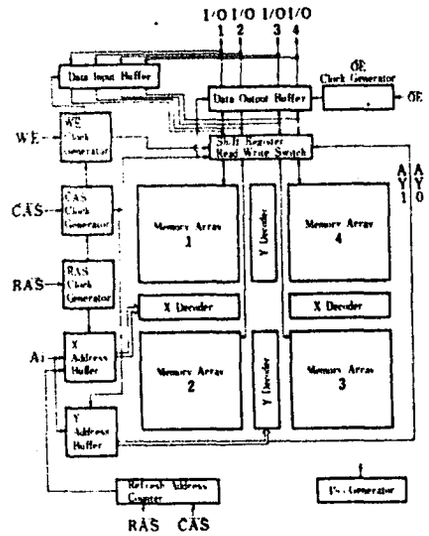
D

-Word x 4-bit Dynamic Random Access Memory

TURES

- mode capability
  - 5V (±10%)
  - ip substrate bias generator
- power: 350 mW active, 20 mW standby
- speed: Access Time 120ns/150ns/200ns
- data controlled by $\overline{CAS}$ or $\overline{OE}$
- compatible
- refresh cycles . . . . . 4 ms
- riations of refresh . . . . . $\overline{RAS}$ only refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
  - Hidden refresh

OCK DIAGRAM



$A_0 \sim A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1 ~ I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$ (Row)	Refresh Address Inputs

HM50464P Series

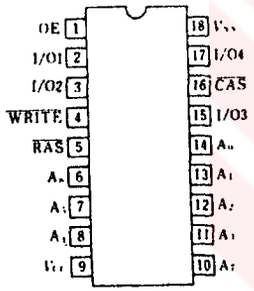
(DP-18)

HM50464CP Series

(CP-18)

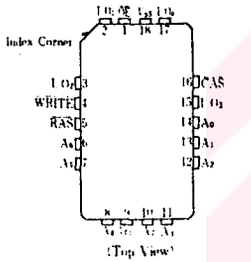
■ PIN ARRANGEMENT

● HM50464P Series



(Top View)

● HM50464CP Series



(Top View)

Supply Voltage relative to V_{SS}	V_{CC}	[illegible]	
Operating Temperature (Ambient)	$Topr$	0 to +70	°C
Storage Temperature (Ambient)	$Tstg$	−55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	$Iout$	50	mA

■ RECOMMENDED DC OPERATING CONDITION (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464P CP-12		HM50464P CP-15		HM50464P CP-20		Unit
		min.	max.	min.	max.	min.	max.	
Operating Current (t_{RC} = min.)	I_{CC1}	–	83	–	70	–	55	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Disable)	I_{CC2}	–	4.5	–	4.5	–	4.5	
Refresh Current ($\overline{RAS}$ only refresh, t_{RC} = min.)	I_{CC3}	–	62	–	53	–	42	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Enable)	I_{CC5}	–	10	–	10	–	10	mA
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min.)	I_{CC6}	–	69	–	58	–	45	mA
Operating Current (Page mode, t_{PC} = min.)	I_{CC7}	–	57	–	48	–	37	mA
Input Leakage Current (0 < Vin < 7V)	I_{LI}	−10	10	−10	10	−10	10	μA
Output Leakage Current (0 < $Vout$ < 7V, Dout = Disable)	I_{LO}	−10	10	−10	10	−10	10	μA
Output High Voltage ($Iout$ = −5 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V
Output Low Voltage ($Iout$ = 4.2 mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the outp condition.

■ CAPACITANCE (V_{CC} = 5V ±10%, Ta = 25°C)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	$CI1$	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	$CI2$	–	10	pF	1
Output Capacitance	Data In/Data Out	CI/O	–	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464P/CP-12		HM50464P/CP-15		HM50464P/CP-20		Un
		min.	max.	min.	max.	min.	max.	
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	30	–	40	–	50	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	

(to be c

ommand Set-up Time	t_{WCS}	0		[illegible]		[illegible]		ns	[illegible]
ommand Hold Time	t_{WCH}	40	-	45	-	55	-	ns	
ommand Hold Time referenced to RAS	t_{WCR}	100	-	120	-	155	-	ns	
ommand Pulse Width	t_{WP}	40	-	45	-	55	-	ns	
ommand to RAS Lead Time	t_{RWL}	40	-	45	-	55	-	ns	
ommand to CAS Lead Time	t_{CWL}	40	-	45	-	55	-	ns	
Set-up Time	t_{DS}	0	-	0	-	0	-	ns	9
Hold Time	t_{DH}	40	-	45	-	55	-	ns	9
Hold Time referenced to RAS	t_{DHR}	100	-	120	-	155	-	ns	
ommand Set-up Time	t_{RCS}	0	-	0	-	0	-	ns	
Command Hold Time referenced to CAS	t_{RCH}	0	-	0	-	0	-	ns	
Command Hold Time referenced to RAS	t_{RRH}	10	-	10	-	10	-	ns	
h Period	t_{REF}	-	4	-	4	-	4	ms	
Write Cycle Time	t_{RWC}	305	-	360	-	450	-	ns	
to WE Delay Time	t_{CWD}	100	-	125	-	160	-	ns	8
to WE Delay Time	t_{RWD}	160	-	200	-	260	-	ns	8
charge Time	t_{CPN}	50	-	60	-	80	-	ns	
-up Time (CAS before RAS refresh)	t_{CSR}	10	-	10	-	10	-	ns	
old Time (CAS before RAS refresh)	t_{CHR}	120	-	150	-	200	-	ns	
recharge to CAS Hold Time	t_{RPC}	0	-	0	-	0	-	ns	
Time from OE	t_{OAC}	-	30	-	35	-	45	ns	
ut Buffer Turn-off Delay referenced to OE	t_{OFF2}	-	30	-	40	-	50	ns	
Data-in Delay Time	t_{ODD}	30	-	40	-	50	-	ns	
old Time referenced to WRITE	t_{OEH}	25	-	20	-	40	-	ns	
Mode Cycle Time	t_{PC}	120	-	145	-	190	-	ns	
Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	-	60	-	80	-	ns	
Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	-	245	-	310	-	ns	

otes)

. AC measurements assume t_T = 5ns.

ssume that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

. Measured with a load circuit equivalent to 2TTL loads and 100pF.

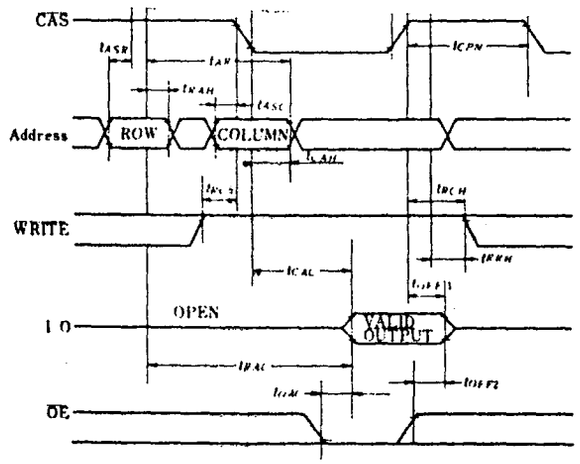
. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).

. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not ferenced to output voltage levels.

$_{IH}$ (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

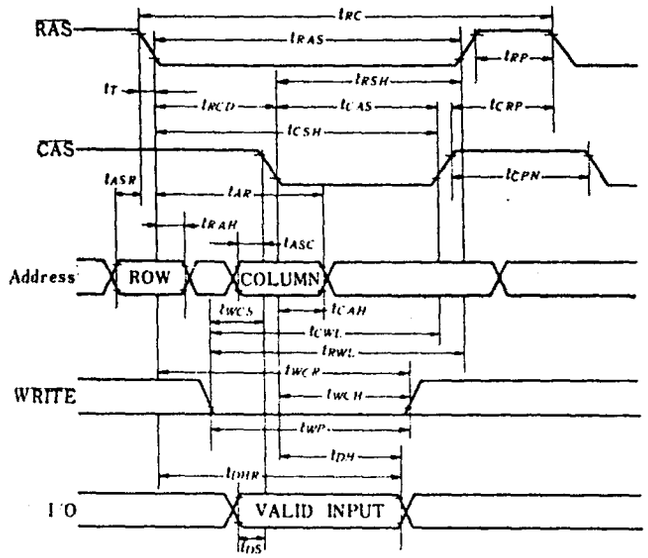
. Operation with the t_{RCD} (max) limit insures that $_{AC}$ (max) can be met; t_{RCD} (max) is specified as reference point only, if t_{RCD} is greater than the ecified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.

8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 CAS before RAS refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, OE must disable output buffers prior to applying data to the device.

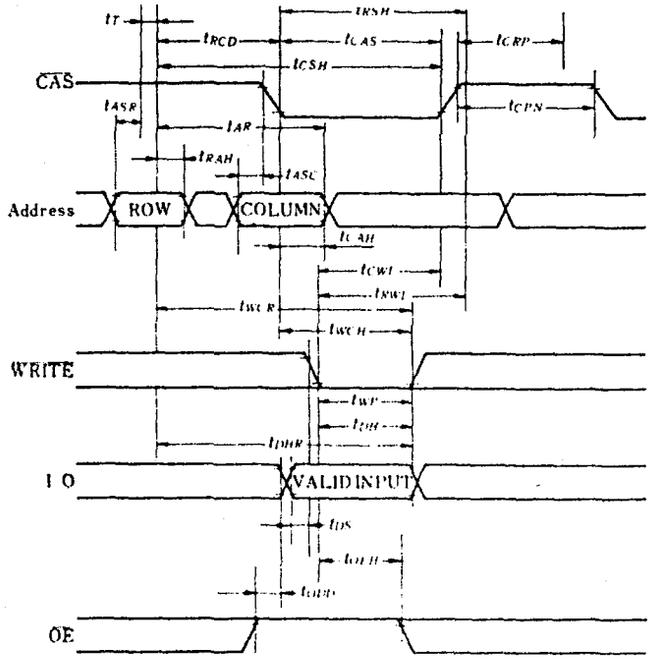


• ▭ : Don't

• **EARLY WRITE CYCLE**

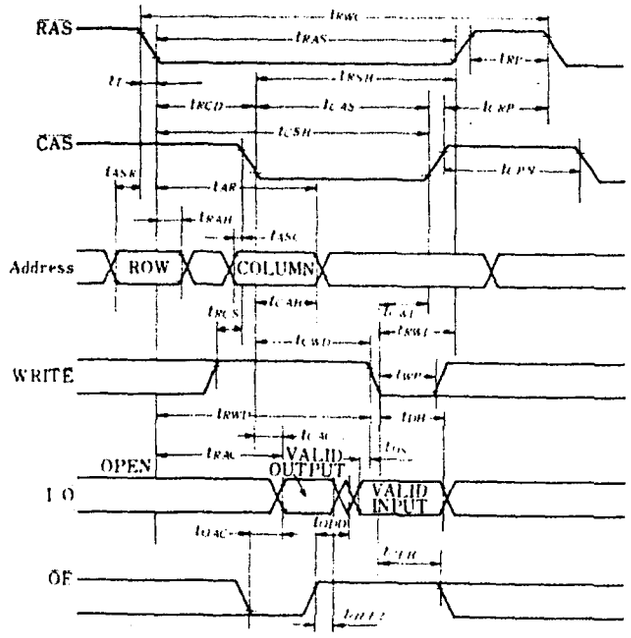


• $\overline{OE}$: Don't
• ▭ : Don't

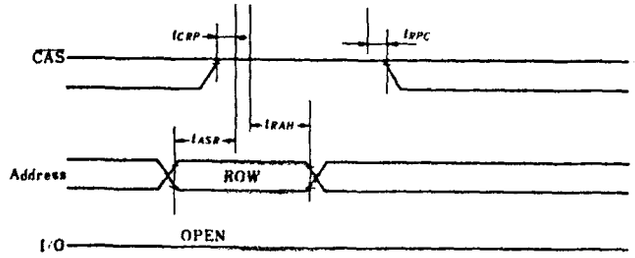


• ▭ : Don't care

READ MODIFY WRITE CYCLE

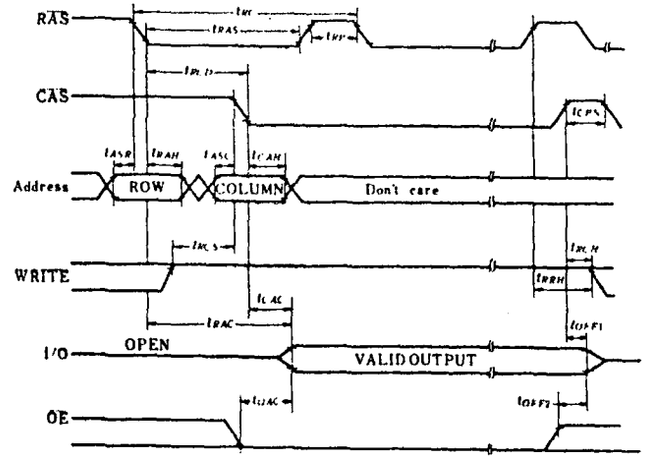


• ▭ : Don't care

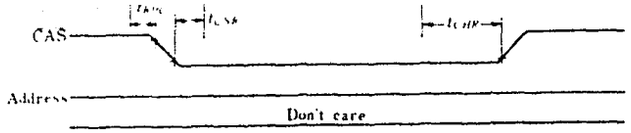


• $\overline{OE}$, $\overline{WE}$: Don't
• ▭ : Don't ca

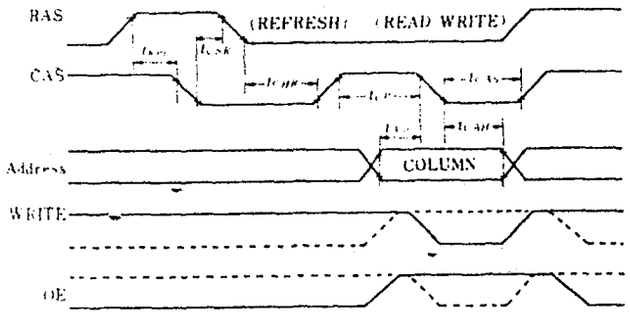
• **HIDDEN REFRESH CYCLE**



• ▭ : Don't

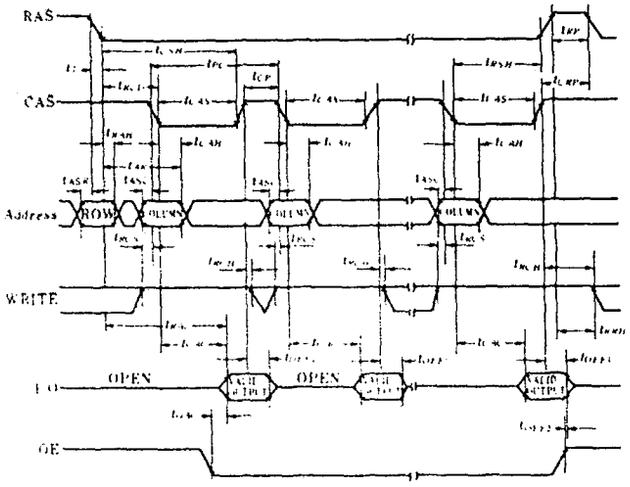


COUNTER TEST

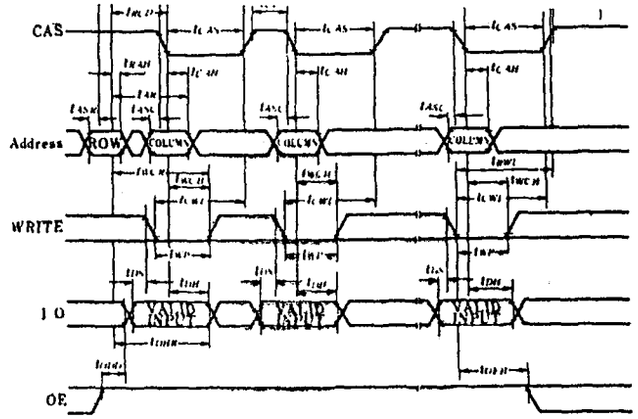


* [ ] : Don't care

PAGE MODE READ CYCLE

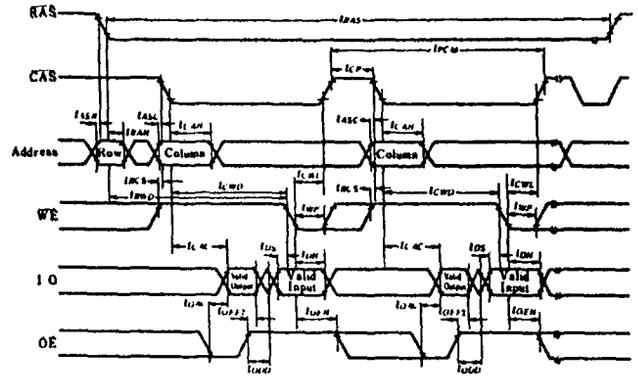


* [ ] : Don't care



* [ ] : Don't ca

• PAGE MODE READ MODIFY WRITE CYCLE



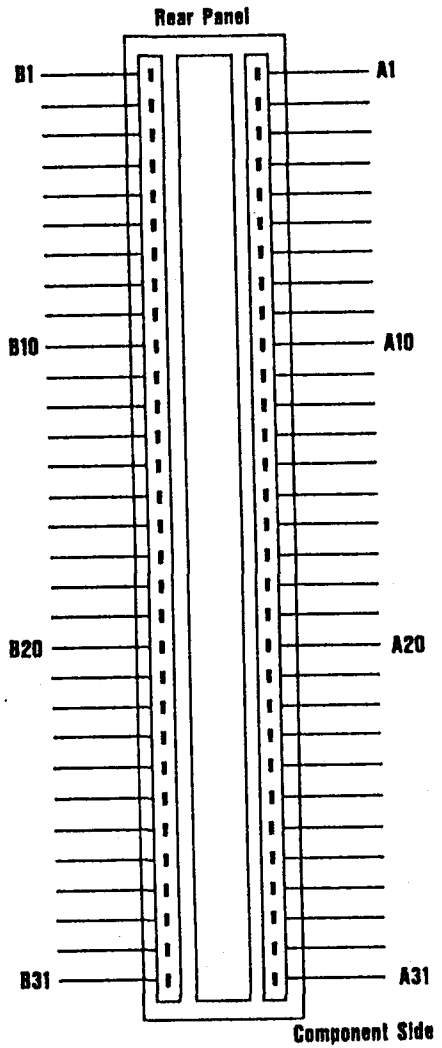
* [ ] : Don't care

APPENDIX D

IBM-AT BUS INFORMATION

This section gives the connector configuration, memory and I/O address mapping of the IBM-AT bus together with the signal descriptions.

The following figure shows the pin numbering for I/O channel connectors J1 through J8.



I/O Channel Pin Numbering (J1-J8)

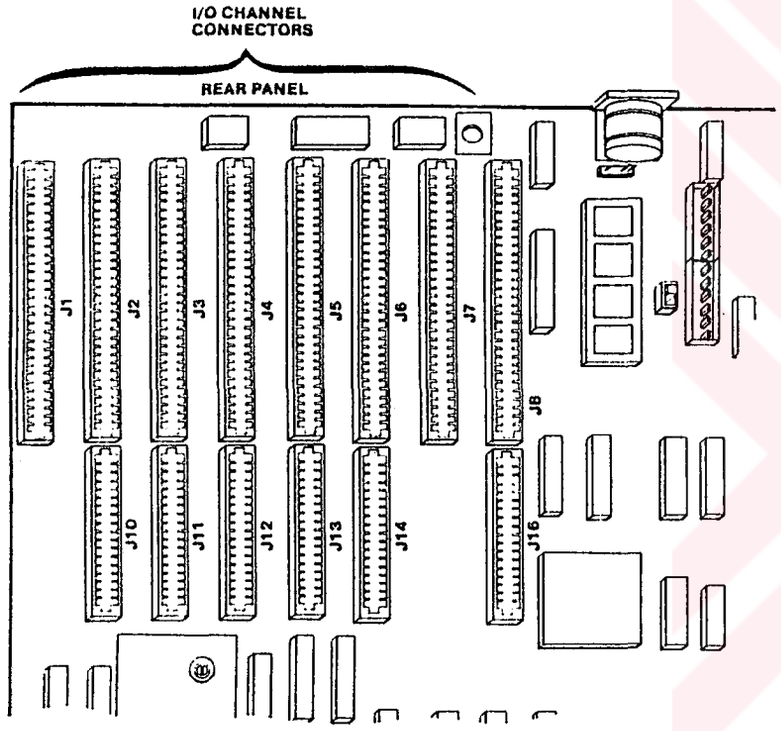
The following figures summarize pin assignments for the I/O channel connectors.

I/O Pin	Signal Name	I/O
A 1	-I/O CH CK	I
A 2	SD7	I/O
A 3	SD6	I/O
A 4	SD5	I/O
A 5	SD4	I/O
A 6	SD3	I/O
A 7	SD2	I/O
A 8	SD1	I/O
A 9	SD0	I/O
A 10	-I/O CH RDY	I
A 11	AEN	O
A 12	SA19	I/O
A 13	SA18	I/O
A 14	SA17	I/O
A 15	SA16	I/O
A 16	SA15	I/O
A 17	SA14	I/O
A 18	SA13	I/O
A 19	SA12	I/O
A 20	SA11	I/O
A 21	SA10	I/O
A 22	SA9	I/O
A 23	SA8	I/O
A 24	SA7	I/O
A 25	SA6	I/O
A 26	SA5	I/O
A 27	SA4	I/O
A 28	SA3	I/O
A 29	SA2	I/O
A 30	SA1	I/O
A 31	SA0	I/O

I/O Channel (A-Side, J1 through J8)

I/O Pin	Signal Name	I/O
B 1	GND	Ground
B 2	RESET DRV	O
B 3	+5 Vdc	Power
B 4	IRQ 9	I
B 5	-5 Vdc	Power
B 6	DRQ2	I
B 7	-12 Vdc	Power
B 8	OWS	I
B 9	+12 Vdc	Power
B 10	GND	Ground
B 11	-SMEMW	O
B 12	-SMEMR	O
B 13	-IOW	I/O
B 14	-IOR	I/O
B 15	-DACK3	O
B 16	DRQ3	I
B 17	-DACK1	O
B 18	DRQ1	I
B 19	-Refresh	I/O
B 20	CLK	O
B 21	IRQ7	I
B 22	IRQ6	I
B 23	IRQ5	I
B 24	IRQ4	I
B 25	IRQ3	I
B 26	-DACK2	O
B 27	T/C	O
B 28	BALE	O
B 29	+5 Vdc	Power
B 30	OSC	O
B 31	GND	Ground

I/O Channel (B-Side J1, through J8)



I/O Channel Signal Description

The following is a description of the system board's I/O chann signals. All signal lines are TTL-compatible. I/O adapters sh be designed with a maximum of two low-power Shottky (LS) loads per line.

SA0 through SA19 (I/O)

Address bits 0 through 19 are used to address memory and I/(devices within the system. These 20 address lines, in addition LA17 through LA23, allow access of up to 16Mb of memory. SA0 through SA19 are gated on the system bus when 'BALE high and are latched on the falling edge of 'BALE.' These signals are generated by the microprocessor or DMA Controll They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

LA17 through LA23 (I/O)

These signals (unlatched) are used to address memory and I/C devices within the system. They give the system up to 16Mb addressability. These signals are valid when 'BALE' is high. LA17 through LA23 are not latched during microprocessor cy and therefore do not stay valid for the whole cycle. Their pur is to generate memory decodes for 1 wait-state memory cycles These decodes should be latched by I/O adapters on the falli edge of 'BALE.' These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

CLK (0)

This is the 6-MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanosecor The clock has a 50% duty cycle. This signal should only be us for synchronization. It is not intended for uses requiring a fixe frequency.

RESET DRV (0)

'Reset drive' is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (I/O)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. D0 is the least-significant bit and D15 is the most-significant bit. All 8-bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The 16-bit devices will use D0 through D15. To support 8-bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

BALE (0) (buffered)

'Address latch enable' is provided by the 82288 Bus Controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with 'AEN'). Microprocessor addresses SA0 through SA19 are latched with the falling edge of 'BALE.' 'BALE' is forced high during DMA cycles.

-I/O CH CK (I)

'-I/O channel check' provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

I/O CH RDY (I)

'I/O channel ready' is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ 14 through 15 (I)

Interrupt Requests 3 through 7, 9 through 12, and 14 through 15 are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). Interrupt 13 is used on the system board and is not available on the I/O channel. Interrupt 8 is used for the real-time clock.

-IOR (I/O)

'-I/O Read' instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

-IOW (I/O)

'-I/O Write' instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

These signals instruct the memory devices to drive data onto the data bus. '-SMEMR' is active only when the memory decode is within the low 1Mb of memory space. '-MEMR' is active on all memory read cycles. '-MEMR' may be driven by any microprocessor or DMA controller in the system. '-SMEMR' is derived from '-MEMR' and the decode of the low 1Mb of memory. When a microprocessor on the I/O channel wishes to drive '-MEMR', it must have the address lines valid on the bus for one system clock period before driving '-MEMR' active. Both signals are active LOW.

-SMEMW (O) -MEMW (I/O)

These signals instruct the memory devices to store the data present on the data bus. '-SMEMW' is active only when the memory decode is within the low 1Mb of the memory space. '-MEMW' is active on all memory read cycles. '-MEMW' may be driven by any microprocessor or DMA controller in the system. '-SMEMW' is derived from '-MEMW' and the decode of the low 1Mb of memory. When a microprocessor on the I/O channel wishes to drive '-MEMW', it must have the address lines valid on the bus for one system clock period before driving '-MEMW' active. Both signals are active low.

DRQ0-DRQ3 and DRQ5-DRQ7 (I)

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with 'DRQ0' having the highest priority and 'DRQ7' having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding 'DMA Request Acknowledge' (DACK) line goes active. 'DRQ0' through 'DRQ3' will perform 8-bit DMA transfers; 'DRQ5' through 'DRQ7' will perform 16-bit transfers. 'DRQ4' is used on the system board and is not available on the I/O channel.

-DACK0 to -DACK3 and -DACK5 to -DACK7 (O)

-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are active low.

AEN (O)

'Address Enable' is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

-REFRESH (I/O)

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

T/C (O)

'Terminal Count' provides a pulse when the terminal count for any DMA channel is reached.

SBHE (I/O)

'Bus High Enable' (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use 'SBHE' to condition data bus buffers tied to SD8 through SD15.

-MASTER (I)

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a '-DACK'. Upon receiving the '-DACK', an I/O microprocessor may pull '-MASTER' low, which will allow it to

control the system address, data, and control lines (a condition known as *tri-state*). After '-MASTER' is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

-MEM CS16 (I)

'-MEM 16 Chip Select' signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA17 through LA23. '-MEM CS16' should be driven with an open collector or tri-state driver capable of sinking 20 mA.

-I/O CS16 (I)

'-I/O 16 bit Chip Select' signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. '-I/O CS16' is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

OSC (O)

'Oscillator' (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

0WS (I)

The 'Zero Wait State' (0WS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, '0WS' is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, '0WS' should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. '0WS' is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

The following figure is an I/O address map.

Hex Range	Device
000-01F	DMA controller 1, 8237A-5
020-03F	Interrupt controller 1, 8259A, Master
040-05F	Timer, 8254.2
060-06F	8042 (Keyboard)
070-07F	Real-time clock, NMI (non-maskable interrupt) mask
080-09F	DMA page register, 74LS612
0A0-0BF	Interrupt controller 2, 8259A
0C0-0DF	DMA controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1

I/O Address Map

Note: I/O addresses, hex 000 to 0FF, are reserved for the system board I/O. Hex 100 to 3FF are available on the I/O channel.

At power on time, the non-maskable interrupt (NMI) into the 80286 is masked off. The mask bit can be set and reset with system programs as follows:

Mask On Write to I/O address hex 070, with data bit 7 equal to a logic 0