DEDICATED TO MY LOVELY MOTHER AND FATHER

REAL-TIME DUAL-ENERGY X-RAY DIGITAL SUBTRACTION IMAGING SYSTEM

A MASTER'S THESIS

in

Electrical and Electronics Engineering

Middle East Technical University

By

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Approval of the Graduate School of Natural and Applied Sciences.

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ABSTRACT

REAL-TIME DUAL-ENERGY X-RAY

DIGITAL SUBTRACTION IMAGING SYSTEM

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A special hardware is designed for on-line real-time subtraction of images obtained by a coronary-angiography system.

The developed subsystem samples video signals carrying 2-D contrast information in 8-bit resolution at a rate of 15MHz. Two 512x512 image matrices are formed for two frames obtained at two different X-Ray energies. Then, these images are subtracted and composed with synchronization pulses after digital to analog conversion to visualize the subtracted image on a TV monitor. It is also capable of freezing images on the monitor.

Key Words: Real-Time, Digital Subtraction, X-Ray absorption properties of radio-opaque materials.

Scientific code: 609.01.04

ÖZET

GERÇEK-ZAMANLI ÇİFT-ENERJİLİ X-IŞINLI SAYISAL ÇIKARMALI GÖRÜNTÜLEME SİSTEMİ

ÖZDEMİR, Haldun

Yüksek Lisans Tezi, Elektrik ve Elektronik Müh. Bölümü.

Şubat 1990, 105 sayfa

Bu çalışmada, bir koroner-anjiyo sistemi tarafından elde edilen görüntüleri gerçek zamanlı olarak çıkarmak için özel bir donanım tasarlandı.

Gelistirilen alt-sistem, iki boyutlu görüntü bilgisi taşıyan video işaretlerini 15MHz.' de 8-bit çözümlemeyle örnekler. İki değişik X-ışını enerji seviyesinde elde edilen iki çerçeve görüntü için iki adet 512x512 boyutunda görüntü matrisi oluşturulur. Daha sonra bu görüntüler çıkarılır ve sayısal-analog dönüsümden sonra, bir TV monitörüne aktarılmak üzere eşleme işaretleriyle birleştirilir. Sistem aynı zamanda, monitörde bir çerçeve görüntüyü dondurma özelliğine de sahiptir.

Anahtar Kelimeler: Gerçek-zamanlı, Sayısal Çıkartma, Radyo-opak maddelerin X-ışını soğurma özellikleri.

Bilim alanı kodu: 609.01.04

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Table Page

CHAPTER 1

INTRODUCTION

During the last decade, highly developed medical imaging systems are increasingly used in medical practice. This is due to the requirements for better image information in medical diagnosis. Characterization of the organs and tissues becomes easier and more accurately done by digital image acquisition and processing techniques.

The aim of this study is to design an on-line real-time system that subtracts two subsequent images taken at two different X-Ray energies by a Coronary-Angiography System, SIEMENS PANDOROS OPTIMATIC. It is difficult to obtain images of the heart, because of its motion and shadowing effects. The shadows of the bones and the other soft tissues obscure the vessels. Therefore, catheterization sessions take longer time to obtain satisfactory images.

The major part of this study covers the design and implementation of a high speed(flash) analog to digital conversion unit, two memory arrays for storing two images, a control unit for kVp adjustment and a composite video signal generator unit after digital subtraction of two memory array outputs.

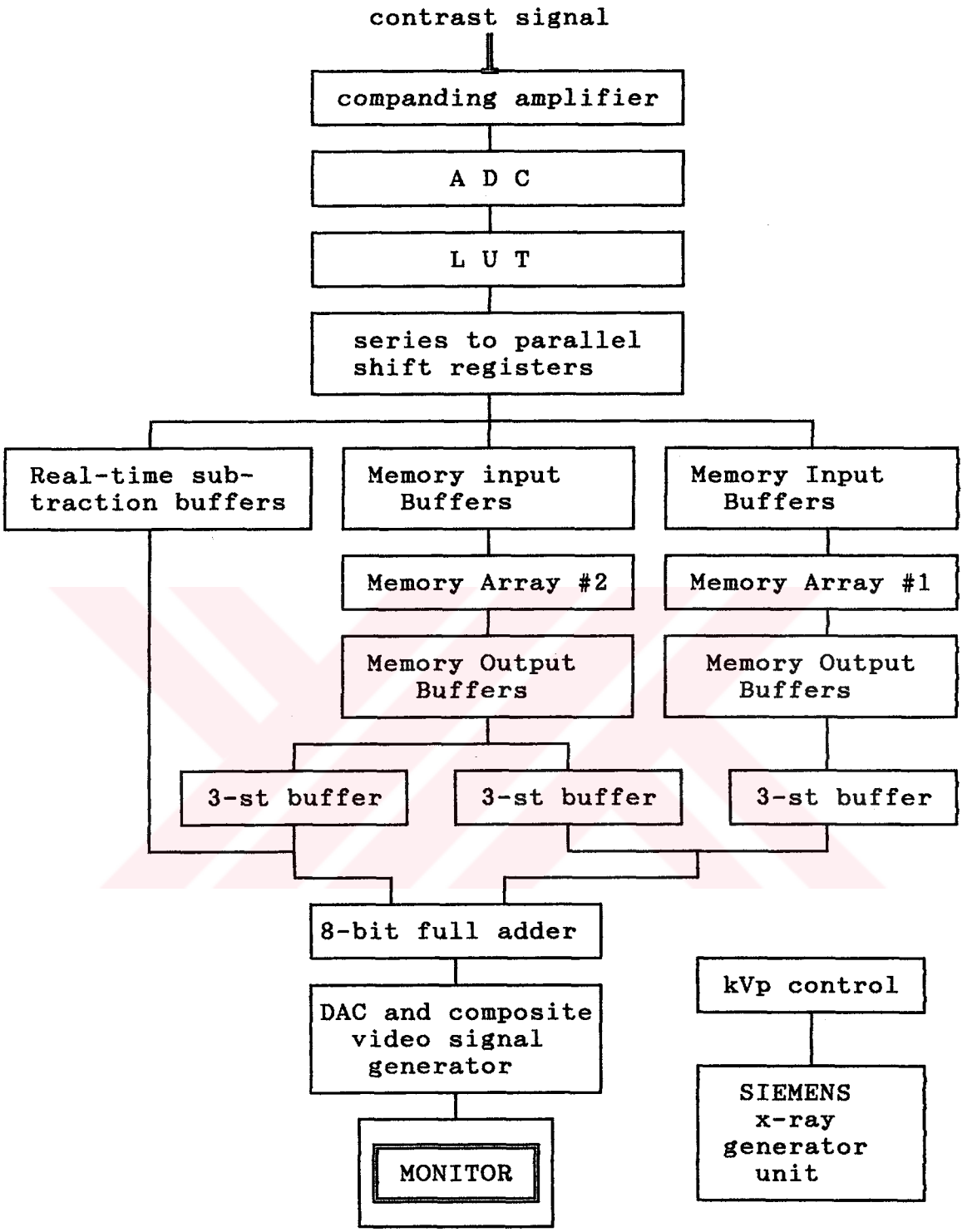


Figure 1.1. Functional block diagram of the real-time dual-energy x-ray digital subtraction imaging system.

The basic components of the system are Flash Analog to Digital Convertor, fast access time static RAM's and a Flash Digital to Analog Convertor. The functional block diagram of the developed hardware is given in Figure 1.1.

The contrast signal at the output of the video camera is given as an input to the companding amplifier. Then a fast analog to digital converter generates 8-bit digital words at every 66.66 nanoseconds. Look-up-Table(LUT) converts the companded data into exact logarithmic words. After data speed is decreased by eight by means of series to parallel shift registers, the information is written into memory arrays by means of memory input buffers. While a data set belonging to a frame is written into a memory array, it is added with the other memory array contents at the same time. Finally, the subtracted data is converted into analog signal by means of a fast digital to analog converter and composed with synchronozation pulses to generate composite video signals to visualize the images on a TV monitor. KVp control unit triggers SIEMENS x-ray generator unit for dual-energy.

A brief description of the Coronary Angiography Imaging System, the theoretical background for the dual energy X-Ray digital subtraction imaging and the design constraints of the needed hardware are discussed in Chapter 1.

The information about the video camera output signals, fast analog to digital conversion in 8-bit resolution, fast digital to analog conversion and composite video signal generation are explained in Chapter 3.

In Chapter 4., the designed hardware and the design constraints are presented. Each block of the hardware is described and related timing and circuit diagrams are given.

The obtained results and comments on further studies are given in Chapter 5.

CHAPTER 2

DUAL-ENERGY X-RAY DIGITAL SUBTRACTION IMAGING

2.1. DIAGNOSTIC IMAGING

Diagnostic imaging requires devices to generate physical energy(as in x-ray or ultrasound examinations), to acquire diagnostic information, to record this information and to display it for diagnostic interpretation. In particular, equipment for cardiovascular examinations must be improved in order to meet the current demand for systems which are able to provide functional as well as morphological information.

Cardiovascular diagnosis has improved remarkably as a result of advances in technology and engineering. The development of large capacity x-ray tubes and generators, and high sensitivity image intensifiers has led to the practical realization of high-speed cine-angiography. In addition, the development of safer contrast media has made less invasive cardiovascular imaging techniques possible.

Angiography, which provides a high quality spatial resolution, suffers from the disadvantage of invasiness. A catheter must be inserted into a vessel. Digital Subtraction Angiography(DSA) was initially developed to overcome this problem. Furthermore, DSA permits vascular structures to be enhanced and examined in isolation,

eliminating distracting background shadows from neighboring bones and soft tissue. In diagnostic imaging, an important goal is to extract only those signals containing essential diagnostic information. DSA is developed to meet this requirements.

The basic aim of this study is to improve diagnostic precision making use of an imaging technique called K-Edge imaging.

2.1.1 Coronary Angiography.

X-rays for medical purposes have been employed all over the world widely since W.C.Roentgen discovered its existance in 1895. However, X-rays have been used in cardiovascular diagnosis for no more than two decades.

The coronary angiography system that we use is in the Cardiology Department of Turkish Advanced Specialization Hospital(TYIH). A photograph of the examination room is given in Figure 2.1.

A functional block diagram of a coronary angiography system is illustrated in Figure 2.2.[1].

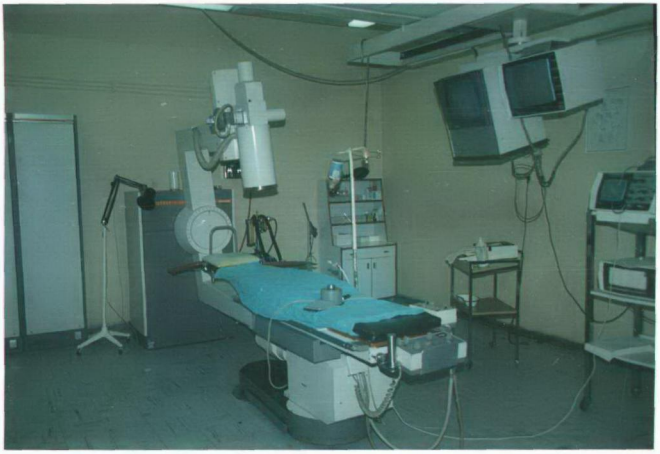
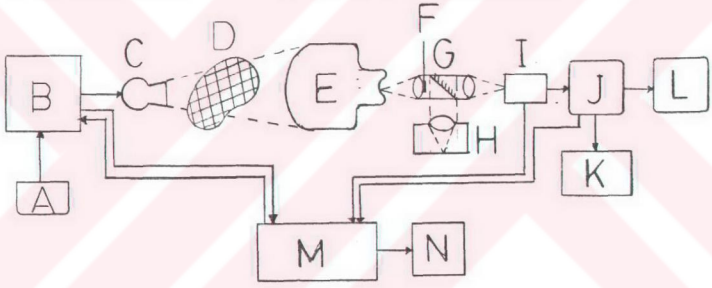


Figure 2.1. Coronary Angiography Examination Room.



A:control console, B:X-ray generator and control unit, C:x-ray tube, D:patient, E:image intensifier, F:photo multiplier, G:mirror, H:cine-camera, I:TV camera, J:electronic control system, K:video recorder, L:monitor 1, M:Dual energy x-ray DSA system, N:monitor 2.

Figure 2.2. Functional Block Diagram of Coronary Angiography System.

Its operation is as follows: After the patient is prepared for the operation, a tubular wire called catheter is inserted from the arm of the patient until it reaches the entrance of a coronary artery. When fluoroscopy button is pressed, a rectified high voltage is applied to the x-ray tube(C) by the x-ray generator(B) to produce x-ray beams. These beams fall on the patient. Some part of its energy is exhausted by absorption and scattering. The spatial energy distribution from the patient is a two dimensional shadow pattern corresponding to the internal structures of the body. An image can then be formed by means of an image intensifier tube .

The visible image at the output of image intensifier is then acquired by the TV camera to obtain image signals for monitoring and recording by cine-camera and/or video-recorder. The optimum contrast density at the output of TV camera is adjusted automatically by means of photo-multiplier.

X-ray images give remarkably good differentiation among bones, soft tissues and gas-filled structures. But, soft tissues do not have very much inherent x-ray contrast, so contrast agents are often given to patients to improve the image quality. These contrast agents are commonly made up of barium or iodine, which have relatively high x-ray attenuation[2].

2.2. K-EDGE IMAGING

2.2.1. Production of X-Ray Beams.

A high speed electron can convert some or all of its energy into an x-ray photon when it strikes an atom and,thus we need to speed up electrons to produce x-rays. Trying to speed up an electron in air is difficult. It is therefore necessary to eliminate most of the electrons and this is done by using a glass bulb(x-ray tube)[2].

The main components of a modern x-ray unit are (1) a source of electrons-a filament, or cathode; (2) an evacuated space to speed up the electrons; (3) a high positive potential to accelerate the electrons; and (4) a target or anode, which the electrons strike to produce x-rays(Figure. 2.3). In an x-ray tube, the number of electrons accelerated toward the anode depends on the temperature of the filament, and the maximum energy of the x-ray photons produced is determined by the accelerating voltage-kilovolt peak(kVp). For example, an x-ray tube operating at 80 kVp will produce x-rays with a spectrum of energies up to a maximum of 80 kilo electronvolts(one keV is the energy an electron gains or loses in going across a potential difference of 1000 Volts. One keV=$1.6*10^{-16}$ Joules). The kVp used for an x-ray study depends on thickness of the patients and the type of study being done[2]. For coronary angiography, x-rays from 25 kVp to 110 kVp are used.

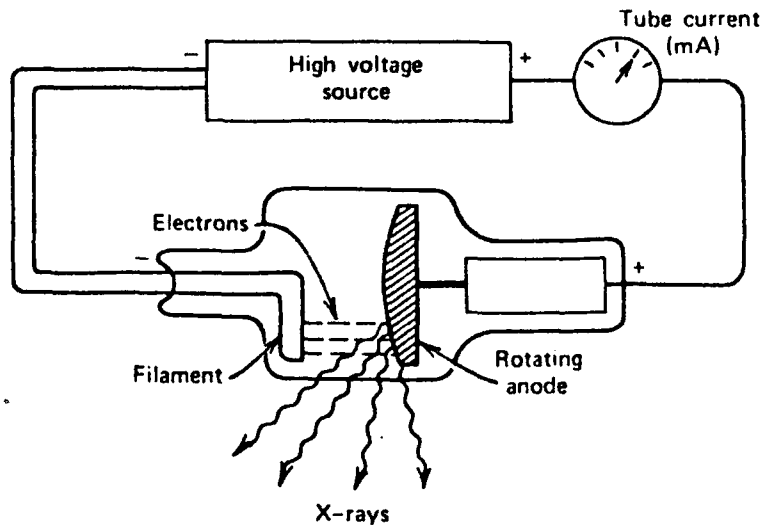


Figure 2.3. An x-ray unit.

Sometimes a fast electron strikes a K-electron in a target atom and knocks it out of its orbit. The vacancy in the K-shell is filled almost immediately when an electron from an outer shell of the atom falls into it, as indicated schematically in Figure 2.4, and in this process, a characteristic K x-ray photon is emitted. An x-ray photon is emitted when an electron falls from the L level to the K level is called a K_α characteristic x-ray. The ray emitted when an electron falls from the M shell to the K shell is called a K_β x-ray.Since the energies of the electrons in the various shells of an atom are precisely determined by nature, an electron falling from an outer shell to an inner shell will produce an x-ray with an energy characteristics of that atom[2]. Table 2.1 gives the energies of the K_α x-rays of several elements. The K-edge is explained in the next section.

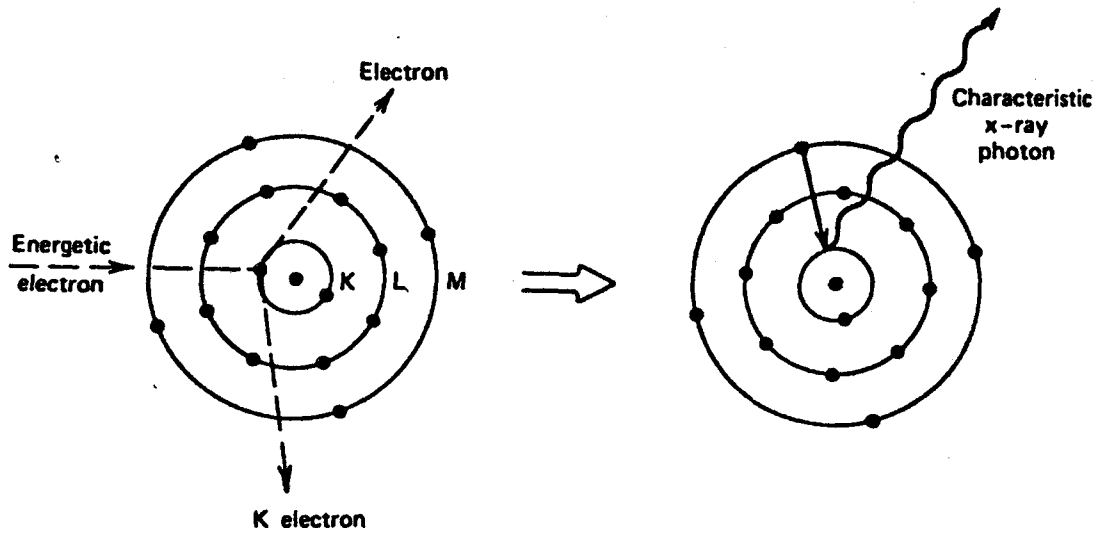


Figure 2.4. Generation of x-rays.

Element	K_α (keV)	K-Edge(keV)
Aliminum	1.5	1.6
Calcium	5	6
Copper	8	9
Molybdenum	17.5	20
Iodine	28	33
Tungsten	59	70
Lead	75	88

Table 2.1 Approximate Energies of the K_α X-Rays and K-Edge for several elements.

The spectrum of x-rays generated by a modern x-ray generator is shown in Figure 2.5. The spikes represent the characteristic x-rays[2].

2.2.2. How X-Rays are Absorbed.

X-rays are not absorbed equally well by all materials, if they were they would not be very useful in diagnosis. Heavy elements such as Calcium, are better absorbers of x-rays than light elements such as Carbon, Oxygen and

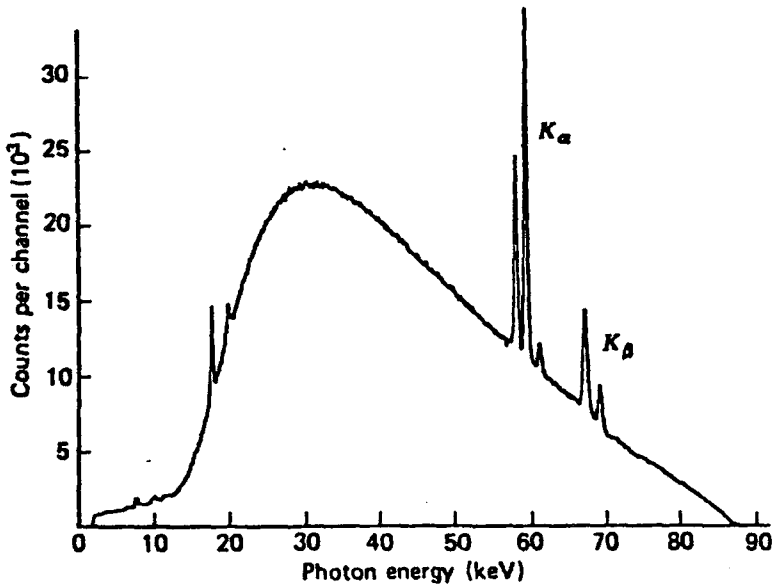


Figure. 2.5. The spectrum of x-rays produced by an x-ray generator.

Hydrogen, and as a result, structures containing heavy elements, like bones, stand out clearly. The soft tissues-fat,muscles and tumors- absorbe about equally well and are thus difficult to distinguish from each other on an x-ray image[2].

The attenuation of an x-ray beam is the reduction in its energy by the absorption and scattering of some of the photons in the beam. An x-ray beam passed through a block of matter, (Figure 2.6.), can be described by the equation:

$$I=Io\ \exp(-\mu x) \qquad (2.1.)$$

where Io is the incident intensity of the monoenergetic x-ray beam, I is the transmitted intensity of the x-ray beam, x is the path length through the element and μ is the linear attenuation coefficient of the element. The linear

attenuation coefficient is dependent on the energy of the x-ray photons; as the beam becomes harder, it decreases.

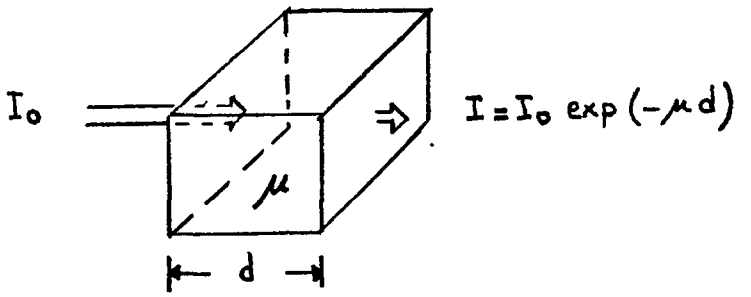


Figure 2.6. X-ray transmission through a matter.

The mass attenuation coefficient μ_m is used to remove the effect of density when comparing attenuation in several materials:

$\mu_m = \mu/d$, where d is density of material.

Therefore Eqn. 2.1. can be rewritten as:

$$I = Io \exp(-\mu_m (dx)) \qquad (2.2)$$

The quantity dx is in grams per centimeter squares and is sometimes called the area density. The mass attenuation coefficient emphasizes that the mass is primarily responsible for attenuating x-rays[2].

Figure 2.7 shows the mass attenuation coefficient of fat, muscles, bone, iodine and lead as a function of x-ray energy. Note that on a gram-for-gram basis, iodine is a better absorber than lead from about 30 to 90 keV. This phenomenon is due to the photoelectric effect[2].

The photoelectric effect is one way x-rays lose energy in the body. It occurs when the incoming x-ray photon transfers all of its energy to an electron which then

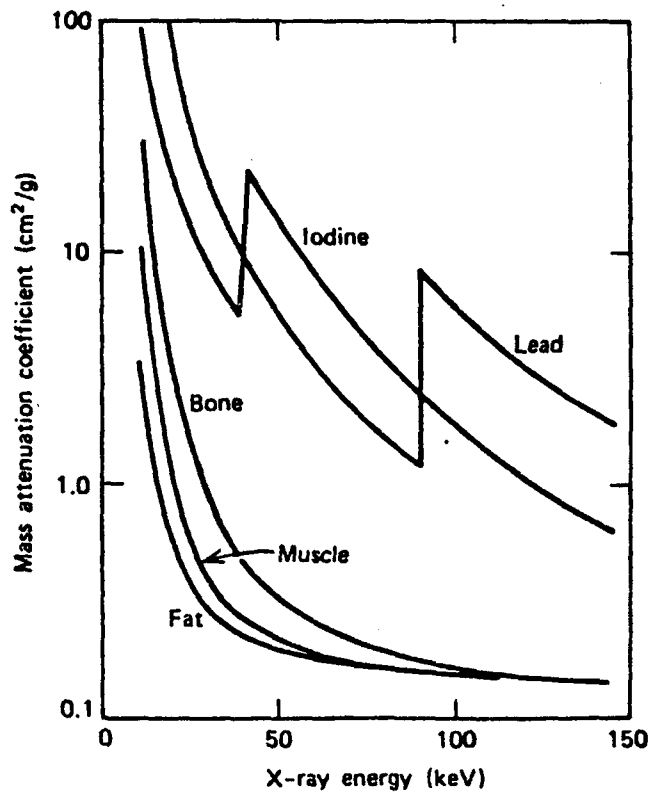


Figure 2.7. Mass attenuation coefficients of some materials.

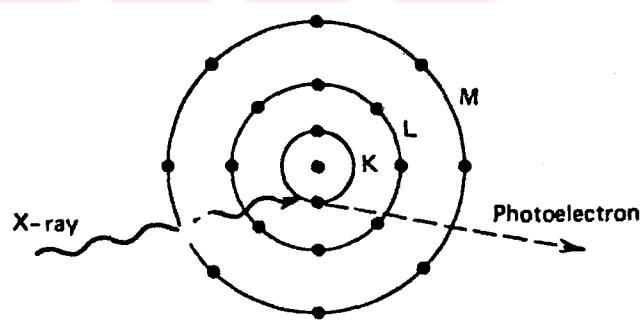


Figure 2.8. An illustration of how x-rays lose energy.

escapes from the atom (Figure 2.8). The photoelectron uses some of its energy(the binding energy) to get away from the positive nucleus and spends the remainder ripping electrons off(ionizing) surrounding atoms[2].

The photoelectric effect is more apt to occur in the intense electric field near the nucleus than in the outer levels of the atom, and it is more common in elements with high Z(atomic number) than in those with low Z. Of course, for a given electron to be liberated, its binding energy must be lower than the energy of the x-ray. The binding energy of a K electron in iodine is 33 keV, while that in lead is 88 keV, and from 33 to 88 keV an x-ray photon can release a K electron from iodine but not from lead. When the energy of the x-ray is just slightly greater than the binding energy, the probability that the photoelectric effect will occur increases greatly, and this accounts for the sharp rises in the curve for iodine at 33 keV and in the curve for lead at 88 keV. These sharp rises are called K-edges. The elements in bone, muscle and fat have K-edges, but they are at such low energies(~6 keV for calcium) that they do not appear in Figure. 2.7. The K-edge energies for some common elements are given in Table 2.1.[2].

2.2.3. K-Edge Imaging Methodology.

In the K-edge imaging methodology, x-ray absorption properties of radio-opaque materials- contrast agents used during the catheterization sessions- are utilized. They have

abrupt changes at special x-ray energies. For example, the mass attenuation coefficient for iodine which is a mostly used contrast agent, jumps from 6.5 cm^2/grams to 36 cm^2/grams around and x-ray energy level of 33 keV, Fig. 2.7.

For this purpose, a special hardware is designed to subtract two images obtained at two different x-ray energy levels at either side of K-edge. That is, one image is obtained at an energy level just below the K-edge energy and the subsequent image is obtained just above the K-edge energy. Afterwards, these are subtracted.

The only contribution to the resultant image is due to iodine. The mass attenuation coefficient of the other tissues and bones do not have remarkable changes within this short energy interval. It is expected that, although a small amount of radio-opaque material is used, a higher quality contrast information than that of conventional film-radiography can be obtained.

2.3.LOGARITHMIC AMPLIFICATION(COMPANDING AMPLIFIER)

As mentioned before, the x-ray intensity dependence on the attenuation coefficient is exponential. Assume a monoenergetic x-ray beam of energies E_1 and E_2, passes through a beampath containing arbitrary amounts of tissue t, bone b and Iodine i. Then the Equation 2.2 can be rewritten for two different energies as:

$$I_1 = I_{o1} \exp[-(\mu_{t1} t + \mu_{b1} b + \mu_{i1} i)] \quad (2.3a)$$

$$I_2 = I_{o2} \exp[-(\mu_{t2} t + \mu_{b2} b + \mu_{i2} i)] \quad (2.3b)$$

where μ_t, μ_b and μ_i are mass attenuation coefficients for tissue, bone and Iodine respectively. If I_1 is x-ray energy intensity on image intensifier for an energy E_1 slightly below K-edge energy and I_2 is for an energy E_2 slightly above K-edge energy, it is obvious that; in order to be able to subtract two contrast signals properly a logarithmic amplification of I_1 and I_2 is needed.

After logarithmic amplification we obtain:

$$\mu_{t1} t + \mu_{b1} b + \mu_{i1} i = \ln(I_{o1}/I_1) \quad (2.4a)$$

$$\mu_{t2} t + \mu_{b2} b + \mu_{i2} i = \ln(I_{o2}/I_2) \quad (2.4b)$$

Furthermore, assuming that $\mu_{t1}=\mu_{t2}$ and $\mu_{b1}=\mu_{b2}$ based on reasoning stated in 2.2.3 and also $I_{o1}=I_{o2}$. Hence, after subtraction of 2.4a and 2.4b, one gets:

$$\mu_{i1} i - \mu_{i2} i = \ln(I_{o1}/I_1) - \ln(I_{o2}/I_2) \quad (2.5)$$

After further simplification, Eqn. 2.5 can be written as:

$$\mu_{i1} - \mu_{i2} = (1/i)[\ln(I_2) - \ln(I_1)] \quad (2.6)$$

However, what we obtained in Equation 2.6 is not the actual situation due to the nonlinearities existing in attenuation coefficients and beam hardening of x-rays.

A differential amplifier, (Figure 2.9), is designed to meet the requirements using matched transistor pairs,(Appendix E1.). It is not so easy to obtain a perfect logarithmic characteristics using discrete devices. So an amplifier having a characteristics close to logarithm is realized. Circuit analysis of the amplifier is as follows:

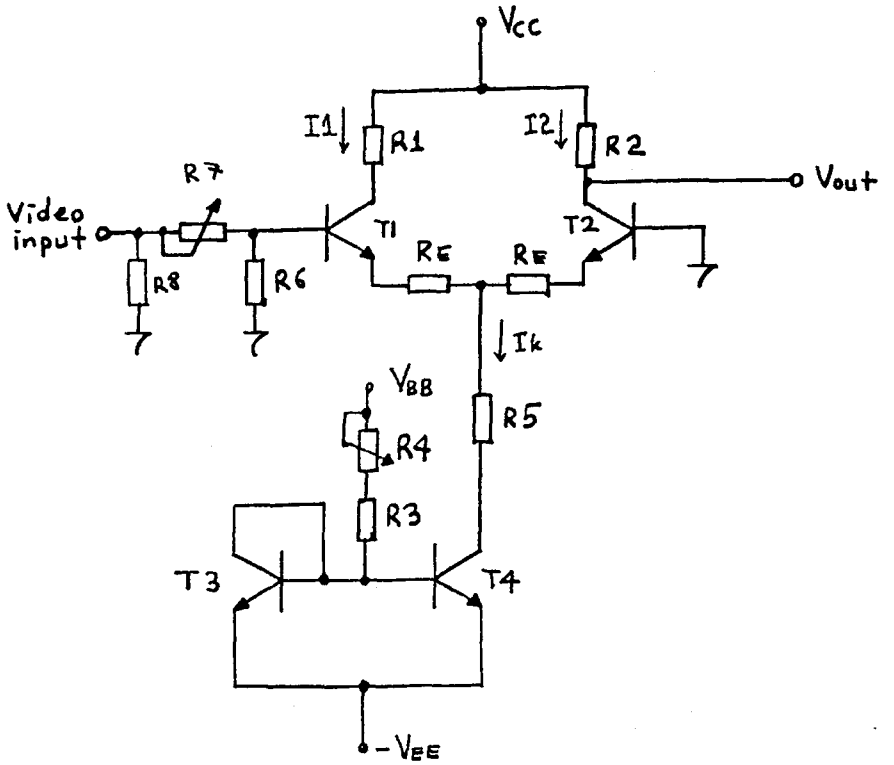


Figure 2.9. Companding Amplifier.

KVL in the input side can be written as:

$$-V_{in} + V_{be1} + I_1 R_E = V_{be2} + I_2 R_E \qquad (2.7)$$

and $$I_1 + I_2 = I_k \qquad (2.8)$$

$$I_1 = I_{o1} \exp(V_{be1}\, q/kT) \qquad (2.9a)$$

$$I_2 = I_{o2} \exp(V_{be2}\, q/kT) \qquad (2.9b)$$

where, q is charge in Coulombs, k is Boltzman constant, T is temperature in Kelvin and I_{o1}, I_{o2} are reverse saturation currents of Base to Emitter junction of diodes of T_1 and T_2 respectively. Dividing 2.9a by 2.9b we get:

$$\frac{I_1}{I_2} = \frac{I_{o1}}{I_{o2}} \exp\left[\frac{q}{k\,T}\,(V_{be1} - V_{be2})\right] \qquad (2.10)$$

Since all transistors are on the same substrate in the same chip, it can be assumed safely that $I_{o1} = I_{o2}$. Then Eqn. 2.10 can be rewritten as:

$$\frac{I_1}{I_2} = \left[\frac{q}{k\ T}\ (V_{be1}-V_{be2})\right] \qquad (2.11)$$

Taking natural logarithms of both sides of Eqn. 2.11, one gets:

$$V_{in} = \frac{k\ T}{q}\ \ln\left[\frac{I_1}{Ik-I_1}\right] + R_E\ (2I_1 - Ik) \qquad (2.12)$$

Equation 2.12 is the nonlinear characteristic equation of the companding amplifier(we call it so, since it compands the input signal). In fact, it can easily be shown that the I_1 versus V_{in} curve has tangent hyperbolic characteristics[3]. What we want to obtain at the end is a logarithmic relation in the form of:

$$I_1 = \frac{Ik}{2} + a\ \ln\left[1 + b\ \frac{q\ V_{in}}{k\ T}\right] \qquad (2.13)$$

The Equations 2.12 and 2.13 are solved together to obtain maximum input dynamic range and maximum bandwidth. A computer simulation program typed in Appendix F. is written in a packet program called MATLAB. As a result, it is found out that R_E=30 ohms, Ik=2 mA, a=0.28 and b=3.7. Figure 2.10 shows the plot of this solution.

It is obvious that, in order to obtain the exact logarithmic relation in Equation 2.13, a Look-up-Table(LUT) is to be used after digitization of signal at the companding amplifier output. By means of LUT, 256 points will be converted into new exact logarithmic values.

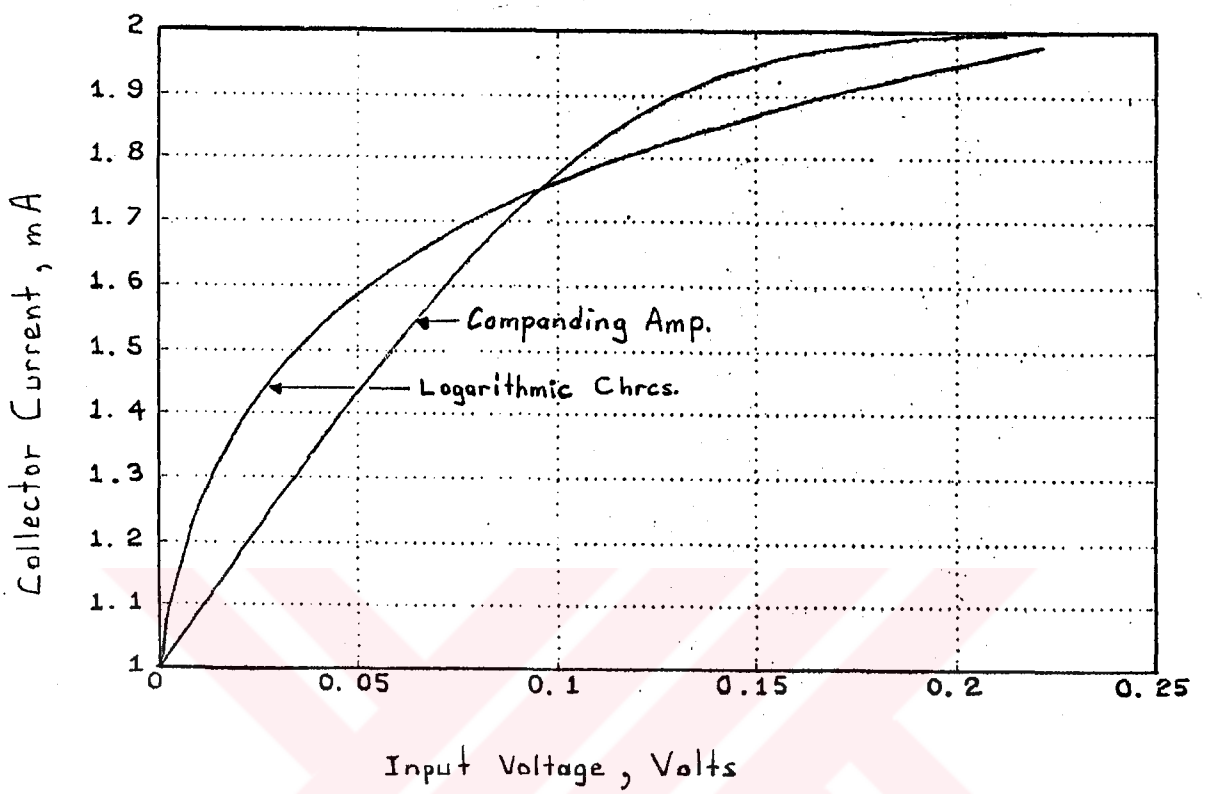


Figure 2.10. Computer Simulation Results for RE=30 ohms, Ik=2 mA, a=0.28 and b=3.7. Collector current versus input voltage plot of Equation 2.12 and 2.13.

CHAPTER 3

FAST SAMPLING OF VIDEO SIGNALS

3.1. VIDEO SIGNAL

In application of x-ray imaging systems, a very high frequency and voltage electromagnetic energy is transmitted through the human body and a video camera is employed to obtain visible images. The signal at the output of the video camera is called " video signal ". This signal is the composition of the image and the horizontal and vertical synchronization information. The video camera output is normally connected to a monitor to visualize the image.

3.1.1. Video Camera Output.

A real-time imaging system should produce sequences of images at a rate fast enough(with a frame rate up to 25 frames per second) to follow the movements of the organs. Video-cameras used in on-line imaging systems are either of 25 frames per second or 30 frames per second. The one we use is a 25 frames/sec. and realizes interlaced scanning. Interlaced scanning means that the 625 lines in a frame are scanned in two seperate time intervals: first 312.5 odd numbered lines, secondly the remaining 312.5 even numbered lines. The aim of this type of scanning is to reduce the overall bandwidth. Every 312.5 even or odd lines form a field. A frame is composed of two fields. A sample line is illustrated in Figure 3.1.

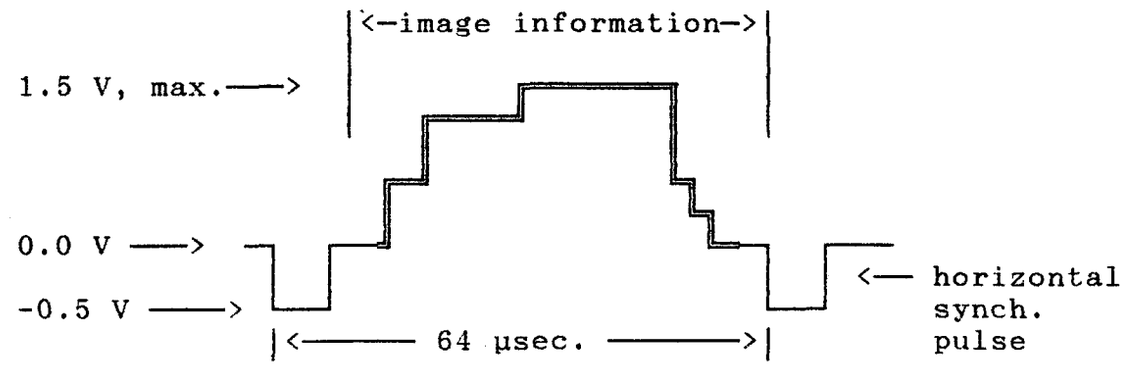


Figure 3.1 A sample line of a composite video signal.

3.2. ANALOG TO DIGITAL CONVERSION

A flash analog to digital converter(ADC) is employed for sampling of video signals at a rate of 15.0 Mhz. It does not require a sample and hold circuitry at the input stage. In a flash ADC, conversion is achieved by a single convert pulse. At each "convert" command the outputs of the comparators inside the ADC unit are encoded and conversion is realized[4].

The major aim is the sampling of the continuous time signals at a fastest rate. TRW-TDC 1048, a 20 MSPS(Mega samples per second) ADC with 1/2 LSB accuracy is used[4]. Its digital output is TTL compatible. The TDC 1048 flash ADC is composed of a comparator array, encoding logic and output latches, Figure 3.2.

The TDC 1048 converts analog signals within the range $V_{RB} \leq V_{IN} \leq V_{RT}$. V_{RB} is the voltage applied to the bottom of the reference resistor chain and V_{RT} is the voltage applied

to the top of the reference resistor chain. The nominal voltages for V_{RT} and V_{RB} are 0.00 and -2.00 Volts respectively[4].

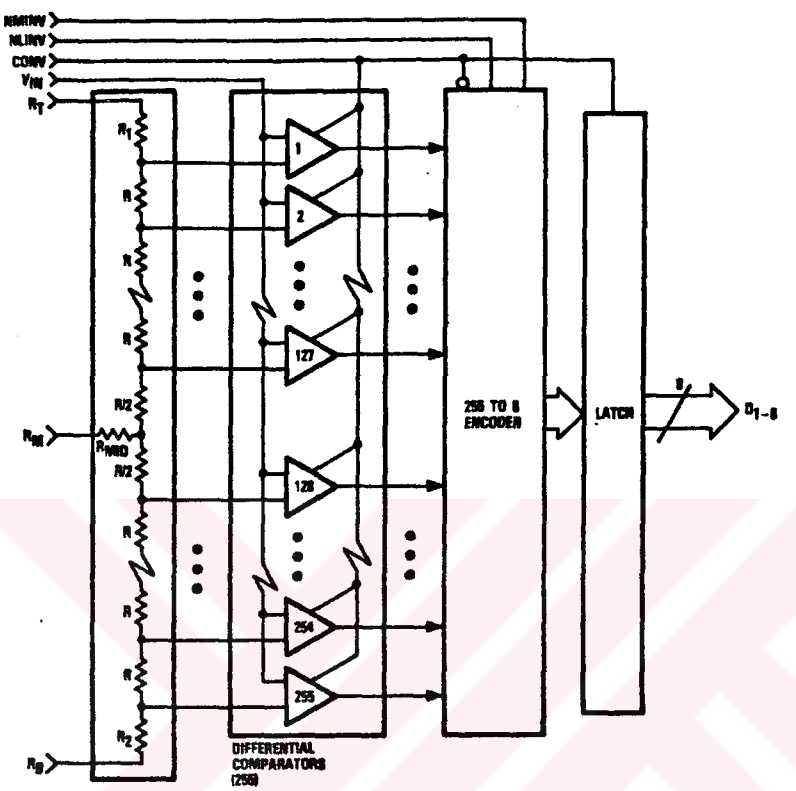


Figure 3.2.Functional block diagram of flash ADC.

The ADC unit is triggered by a convert signal(CONV) at 15.0 Mhz. A sample is taken within sampling time offset(tsto), during the rising edge of the CONV signal, (Figure 3.3.). The coded result is transferred to the output latches with the next rising edge of CONV signal. The output hold the previous data for a time, The output hold time(t_{HO}). The data is valid after a minimum delay time (t_D), after the rising edge of the CONV signal[4].

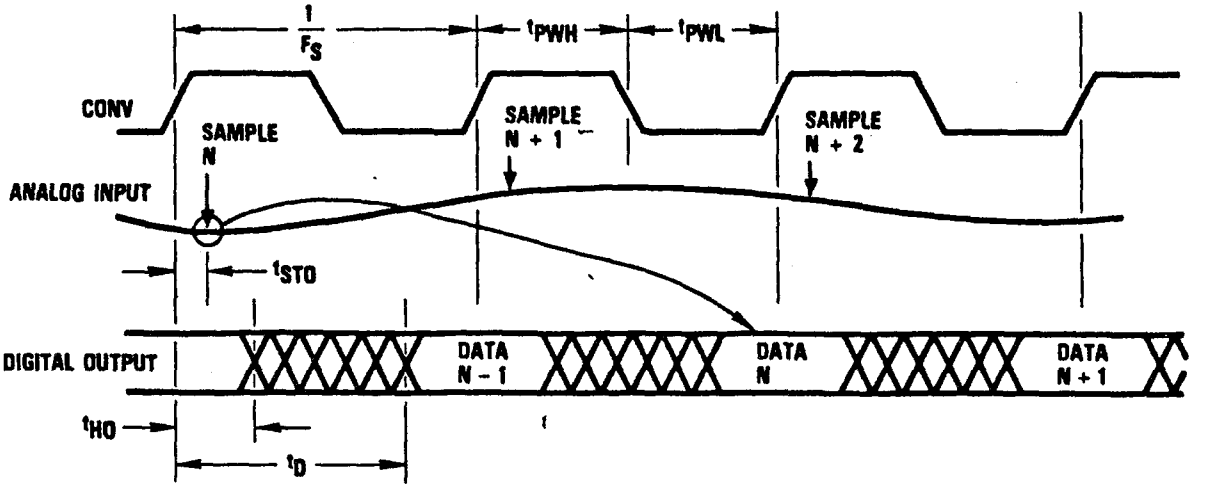


Figure 3.3. Timing diagram of A/D conversion.

3.2.1. ADC Interface Circuit.

The interface circuit,Fig.3.4, includes a companding amplifier explained in Chapter 2., a wide-bandwidth buffer amplifier, reference voltage generator, limiter at the input and the latch buffer at the output of the Flash ADC.

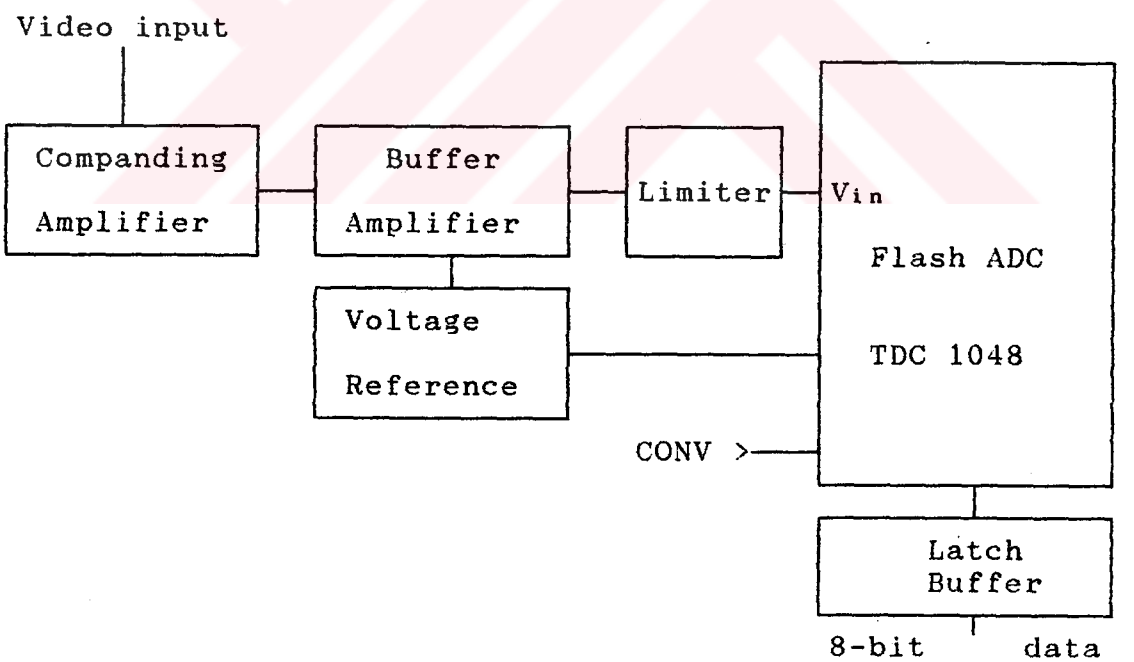


Figure 3.4. Block diagram of ADC and peripherals.

The buffer amplifier matches the video signal at the input to the ADC. Its gain is adjusted so that the voltage at the output is in the range of 0 to -2 Volts in accordance with the input specification of the ADC employed. The limiter circuit protects the ADC from input voltages higher than 0.5 Volts. Voltage reference circuit provides -2 V. for V_{RB} input of ADC. CONV signal is provided by the clock generation and control circuit-explained in the next Chapter. A detailed circuit diagram of ADC board is given in Figure 3.5

3.3. DIGITAL TO ANALOG CONVERSION

A flash Digital to Analog Converter(DAC) is used after digital subtraction of two images. TRW-TDC 1016, a 20 MSPS DAC is employed. Its 10-bit digital input is TTL compatible. The analog output is between 0 V. and -2 V. with a 75 ohms of output impedance[4]. Since our data is 8-bit, the output of the DAC swings from 0 to -255 mV[4].

3.3.1. Composite Video Signal Generation.

The analog signal at the output of DAC is composed with synchronization pulses to generate a composite video signal. This signal is coupled to a TV monitor to visualize The subtracted image, Figure 3.6.

The synchronization and blanking pulses are taken directly from the video signal control boards of the angiography system, SIEMENS PANDOROS OPTIMATIC, Appendix B.

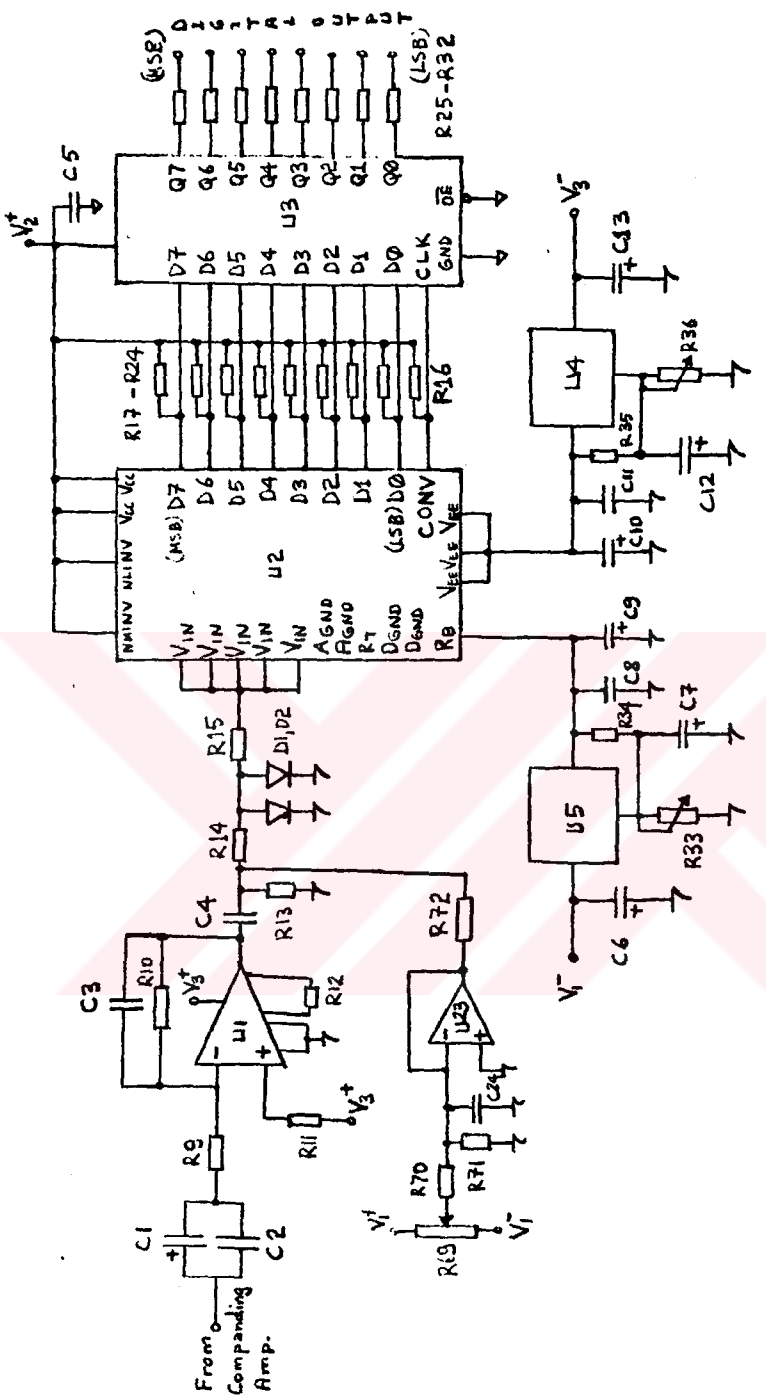


Figure 3.5. Circuit diagram of ADC board.

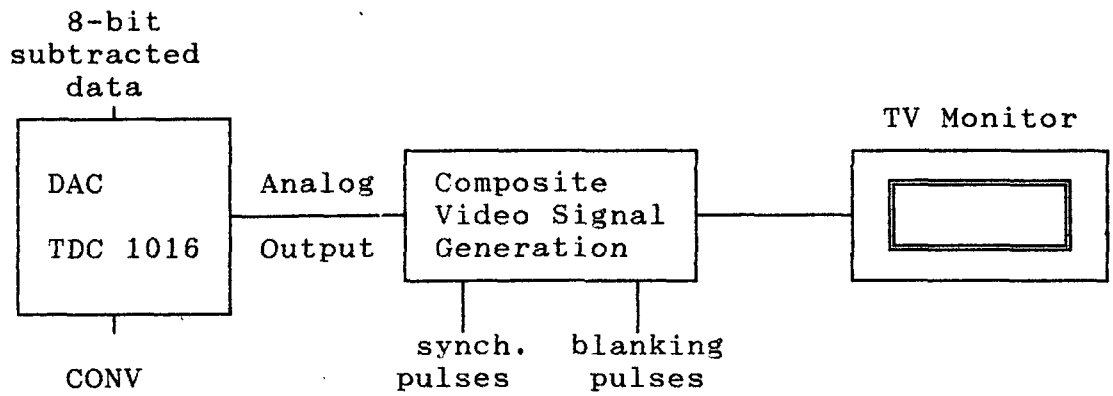


Figure 3.6. Block diagram of the composite video signal generation board.

Composite video signal generator board circuit diagram is given in Figure 3.7. The circuit operation is as follows: The image information signal at the output of DAC is terminated by a 75 ohm input impedance inverting buffer amplifier of adjustable gain. The signal at the output of buffer amplifier is gated by the blanking signal, then, added by the synchronization pulses. Finally, a composite video signal of 75 ohm output impedance is generated for monitoring. An illustration of how composite video signal is generated is given in Figure 3.8.

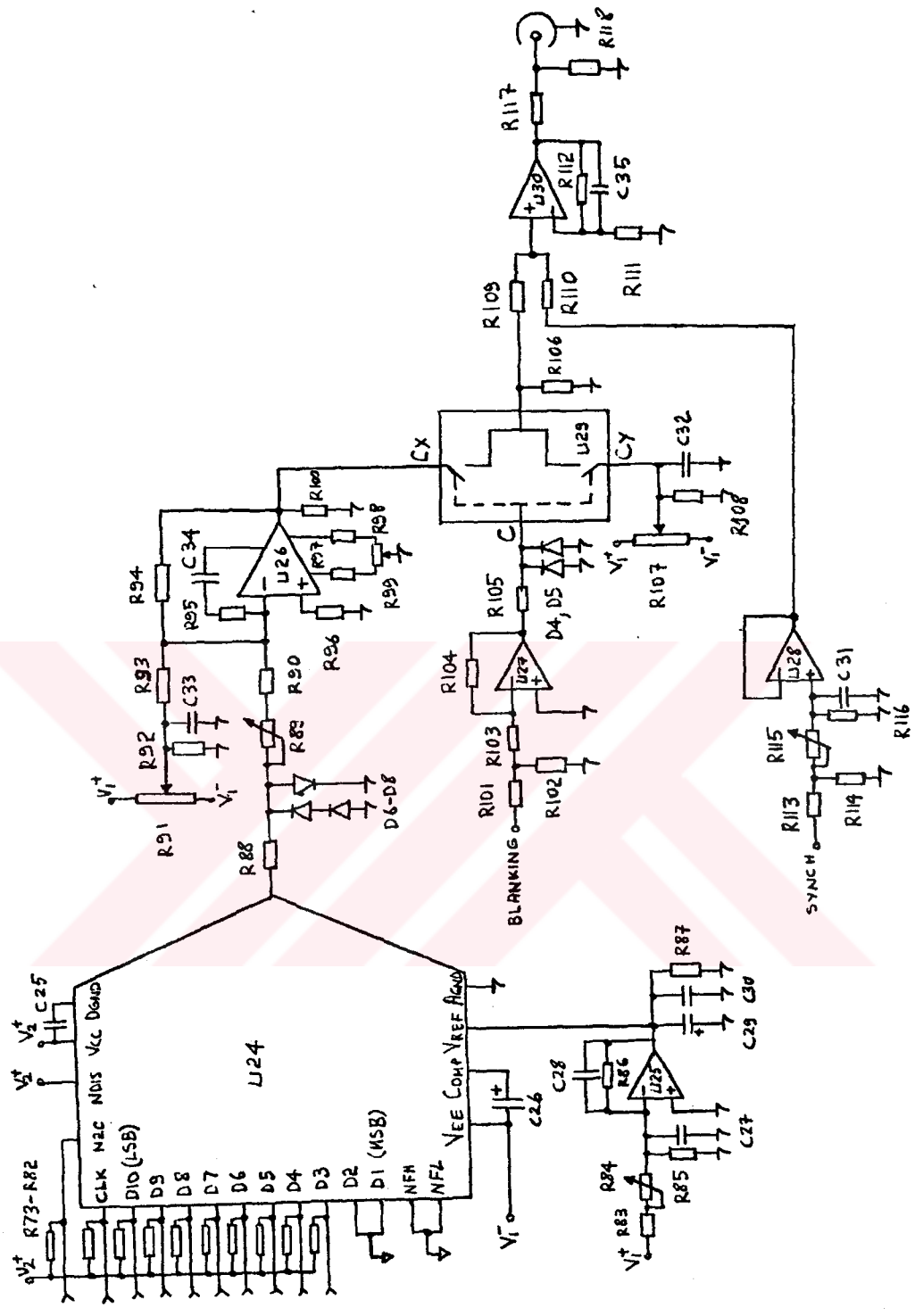


Figure 3.7. Circuit diagram of composite video signal generation board.

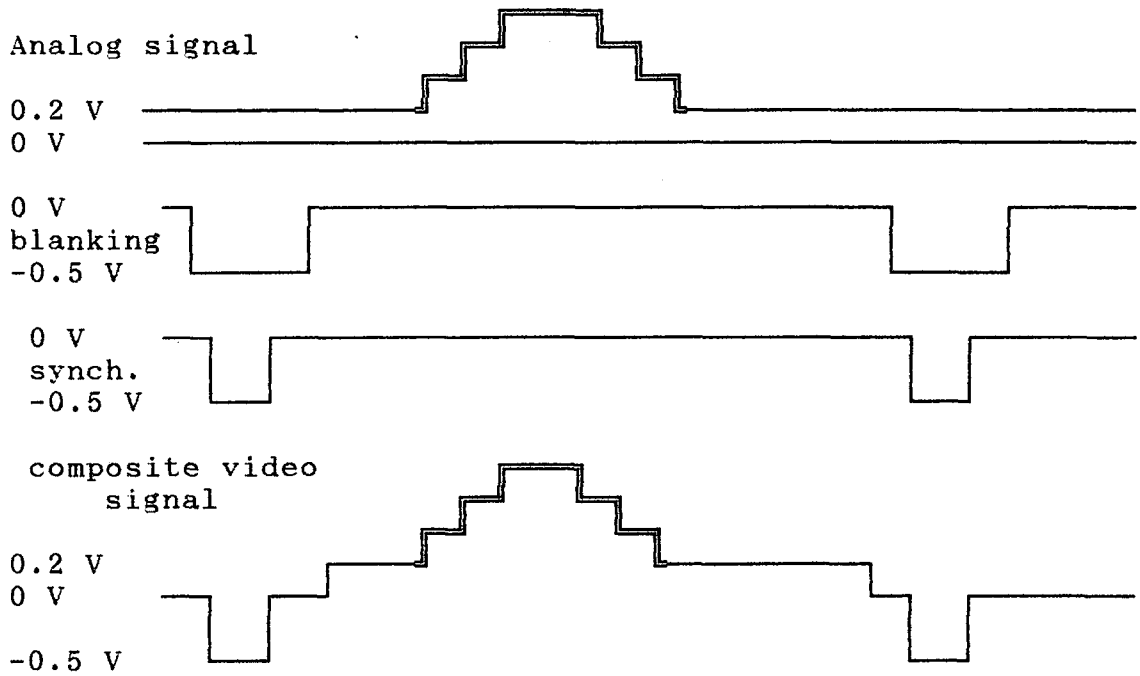


Figure 3.8. Illustration of composite video signal generation.

CHAPTER 4

DATA ACQUISITION AND DIGITAL SUBTRACTION

The functional block diagram of the designed hardware is given in Figure.1.1. In this Chapter, the main digital control circuits for data acquisiton and digital subtraction of images are explained. Complete timing and circuit diagrams of memory read/write, real-time clock generation and subtraction circuits are also explained and given.

4.1. LOOK-UP-TABLE(LUT)

A LUT is required to convert the data companded by the companding amplifier into true logarithmic data. This may be achieved using an EPROM(Electrically Programmable Read Only Memory). The data speed generated by ADC is 66.66 nsec. This speed is considerably below the access time of the EPROMS's available in the market. It is decided that Bipolar TTL Cash-Memories can be used, Appendix E2. The conversion table given in Appendix C. is written into an ordinary EPROM. Then, whenever the power is turned on or system is reset, this information in EPROM is rewritten into Bipolar TTL Buffer Memories. The digital data from ADC board is directed to the address inputs of these buffer memories. With every new data from ADC, the data at the corrsponding memory location is read out as true logarithm of the input.

The block diagram of LUT is given in Figure 4.1.

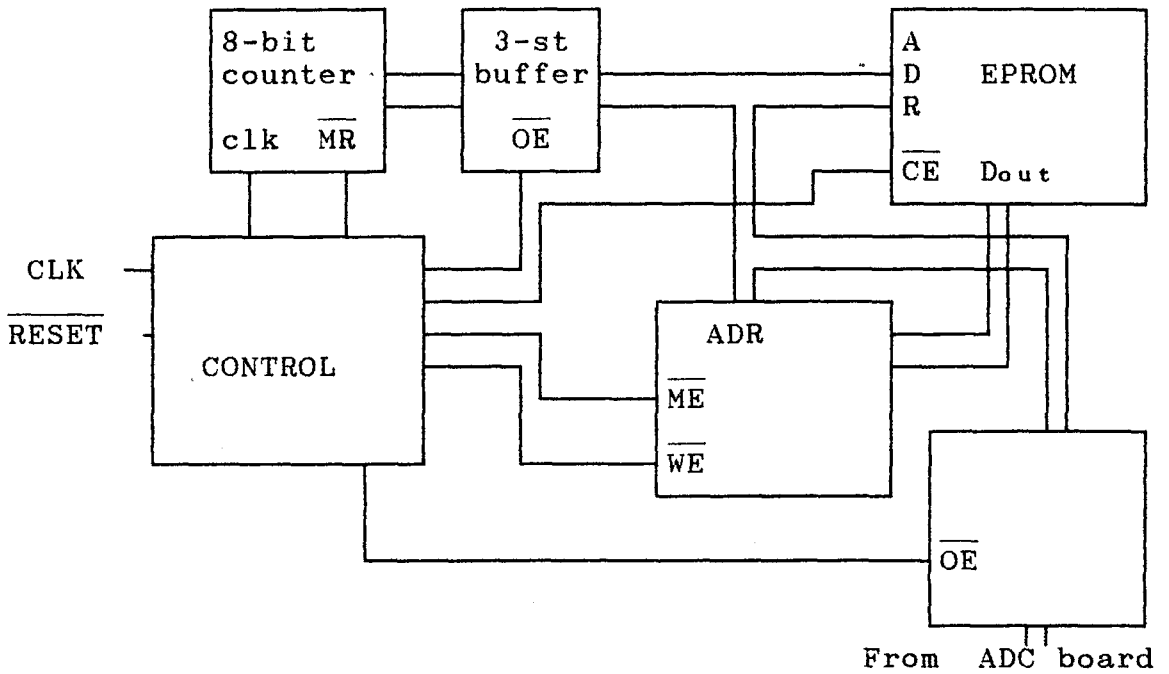


Figure 4.1. Functional block diagram of LUT.

The detailed circuit and timing diagrams are in Figure 4.2 and 4.3. respectively. After power is turned on or reset button is pressed, Q2 output of U31 is set with the rising edge of CLK. Then, $\overline{OE}$(TP2) of U16 is reset and $\overline{OE}$(TP3) of U14 is set by the first falling edge of TP1. The first byte at address 00 is read from EPROM and written into bipolar memories while $\overline{WE}$ is low. 8 of these fast-access-time(less than 40 nsec.) memories are combined to form a memory array of 256 words x 8-bit. Each of them is organized in 256 words x 1-bit manner. Data input of each memory is connected to one of the data outputs of EPROM seperately as shown in Figure 4.4. After 256 bytes data is stored into memories, TP2 is set and TP3 is reset to allow data from ADC to reach the address bus of memories. The data at the memory indicated by the data at the address bus from ADC is read out at every 66.66 nsec.

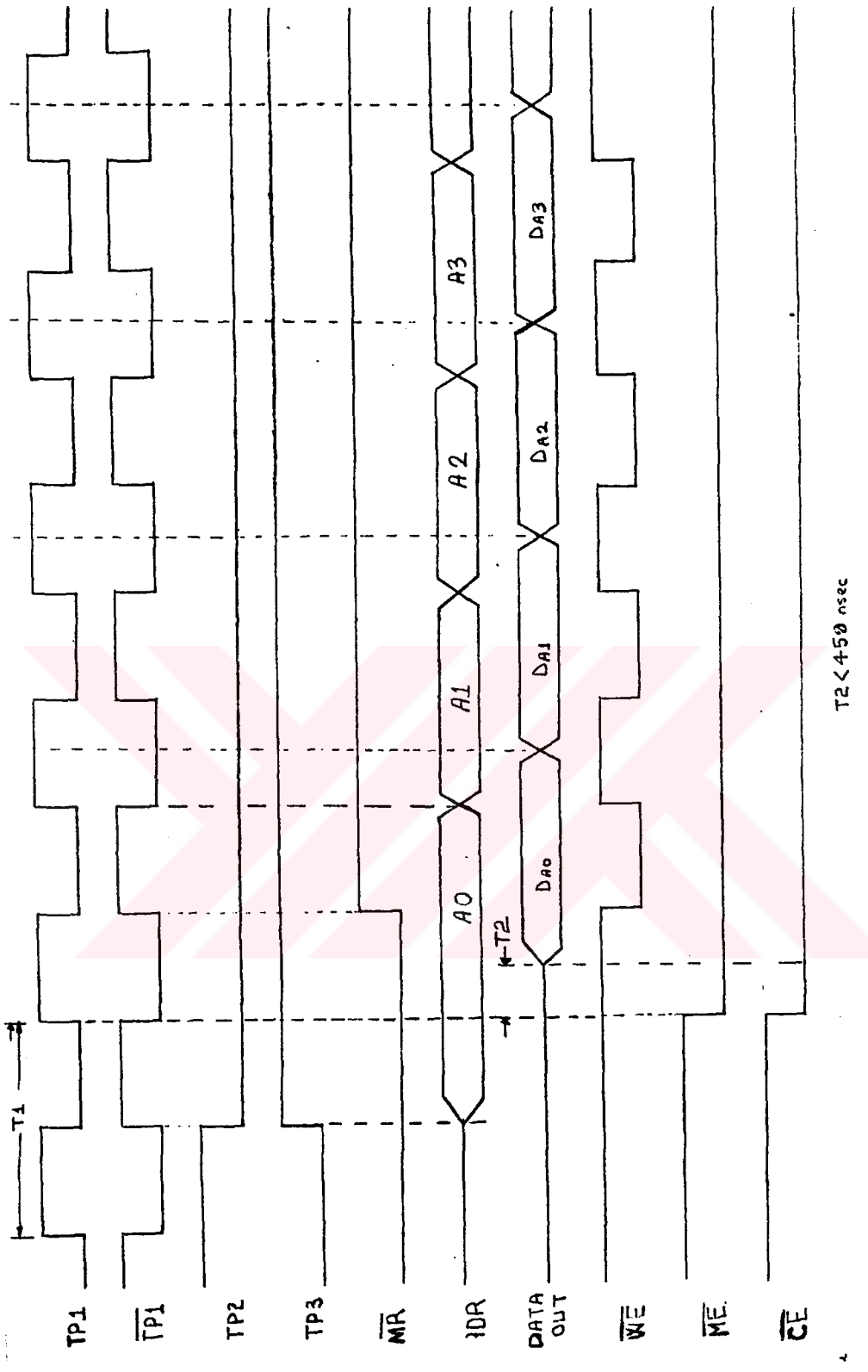


Figure 4.2. Timing diagram of LUT.

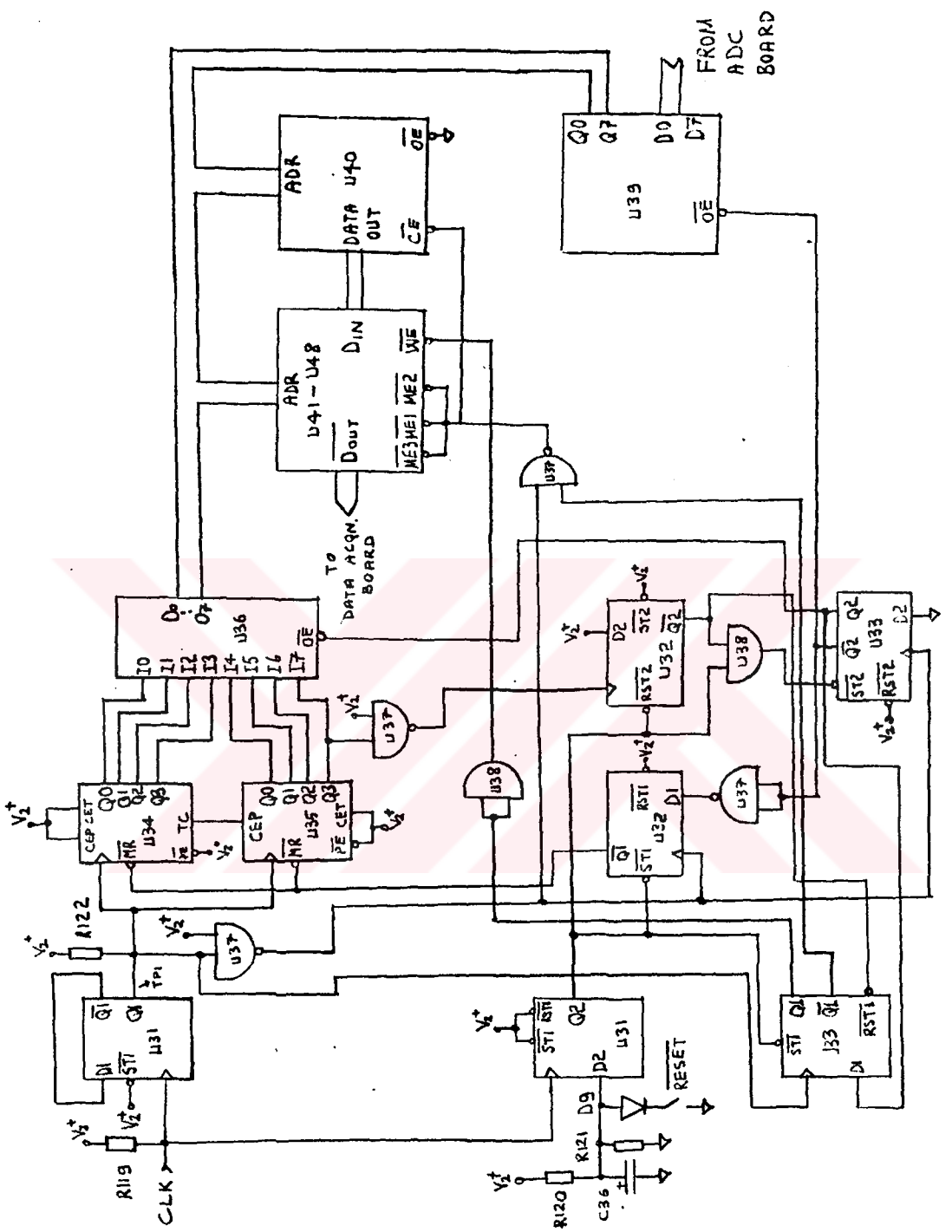


Figure 4.3. Circuit diagram of LUT board.

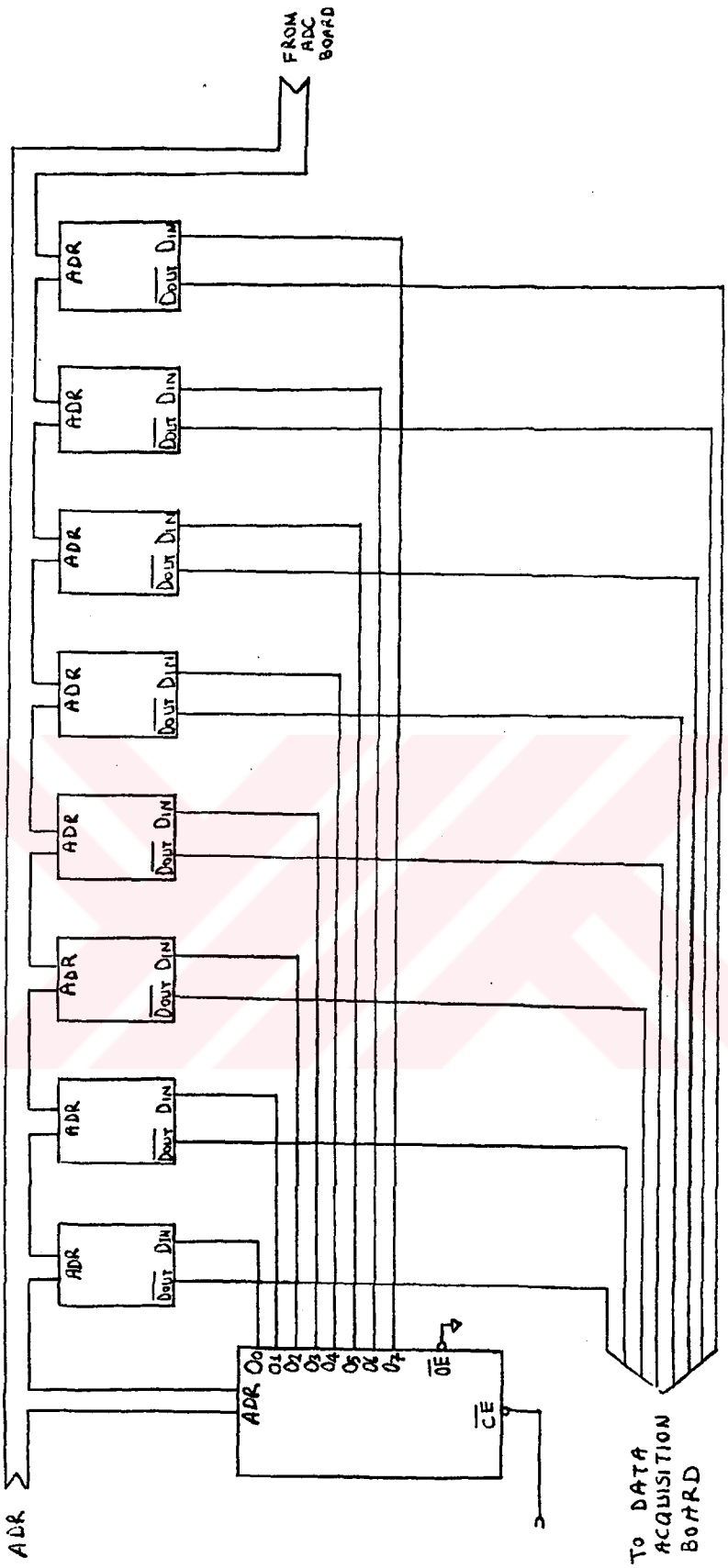


Figure 4.4. LUT details.

4.2. HIGH SPEED DATA ACQUISITION.

The data is generated by the ADC at every 66.66 nsec. This data speed is too fast for the large storage capacity solid state memories available in the market. Bipolar TTL Memories with access time less than 30 nsec. are also available. Yet, they have low storage capacities. The speed of the data, hence, should be decreased. Serial input to parallel output shift registers are used to achieve this goal. Transparent 3-state latches employed as memory input and output buffers and series to parallel shift registers can be thought together as "memory buffer". Address generation and memory read/write control functions are achieved by an on-board control circuit.

The functional block diagram of the data acquisition board is given in Figure 4.5. It is necessary to implement two's complement of one frame of image data, in order to be able to subtract to images. Two's complement control and implementation circuit shown in figure 4.6 achieves this task. It takes two's complement of the high-energy-image, image obtained above the K-Edge.

4.2.1. Memory Buffer.

The circuit diagram of the memory buffer is given in Figure 4.7. Each bit of the 8-bit data is fed to the serial input of one of the eight series to parallel shift registers, U74-U81. At every (66.66 x 8) nanoseconds, data

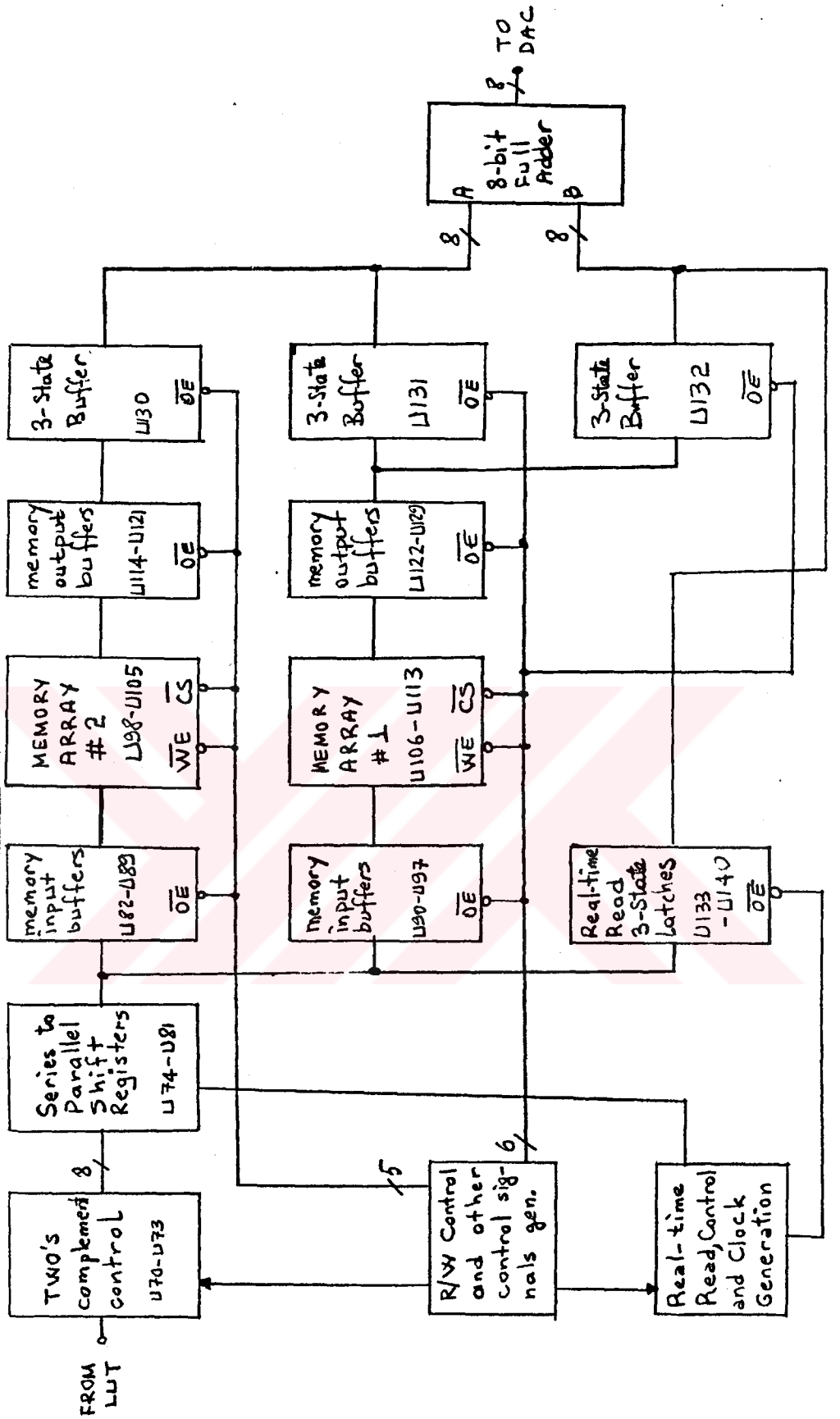


Figure 4.5. The functional block diagram of the data acquisition board.

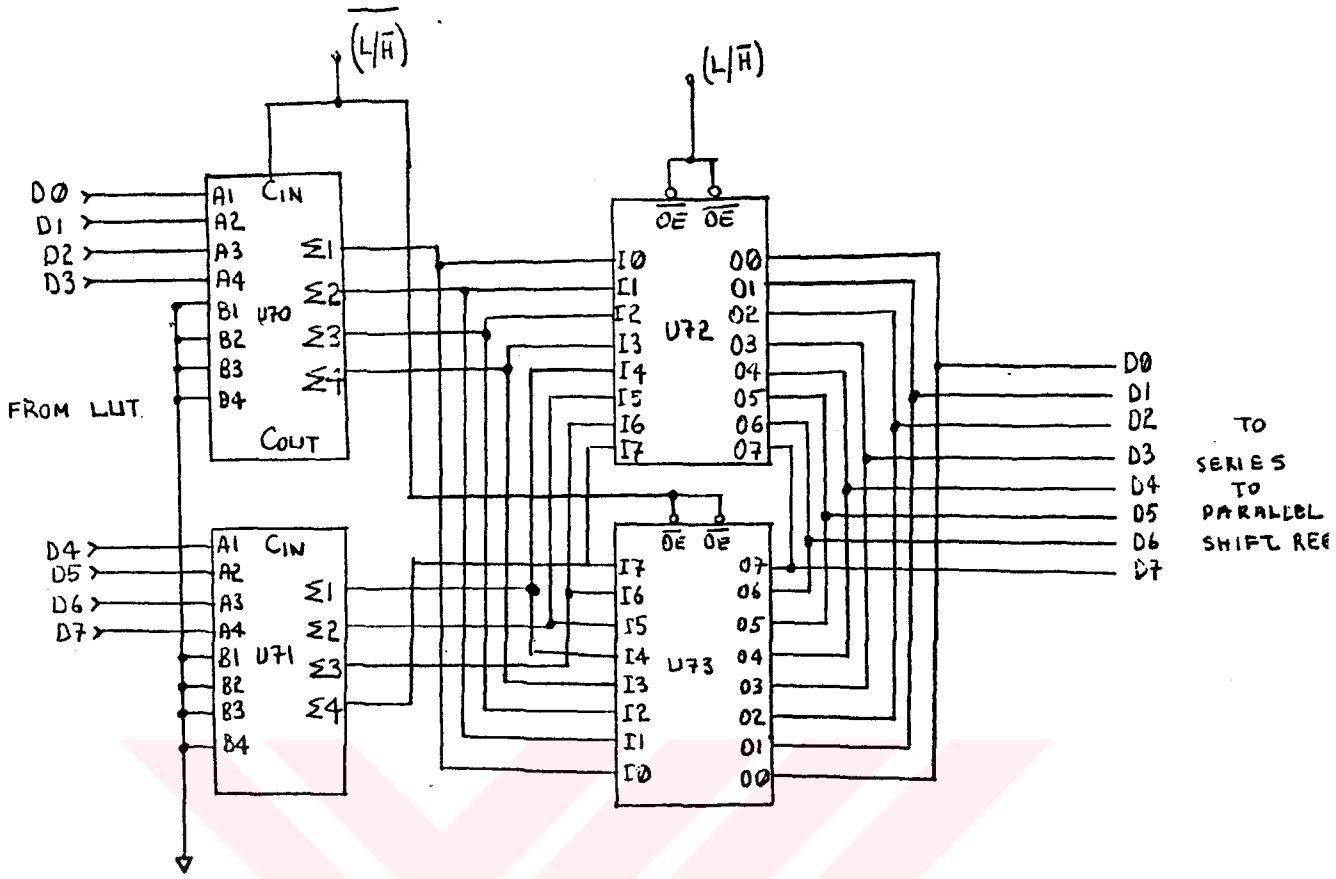


Figure 4.6. Circuit diagram of two's complement control and implementation unit.

at the output of U74 is composed of the least significant bits of the last 8-bytes data. Similarly, U81 contains the most significant bits. Q7 output of U74 contains the least significant bit of the first byte of the eight consecutive bytes. Similarly, Q7 output of U81 contains the most significant bit. The output of the shift registers are connected to the input of the transparent latches in a way that, latches numbered from U82 to U89 contain one byte of eight sequential data in dereasing significance. In other

words, U82 contains the first byte of the eight consecutive bytes and U89 contains the eighth byte of them, as explained in Figure 4.8. Memory output buffers, U114-U121 are enabled only during memory read operation.

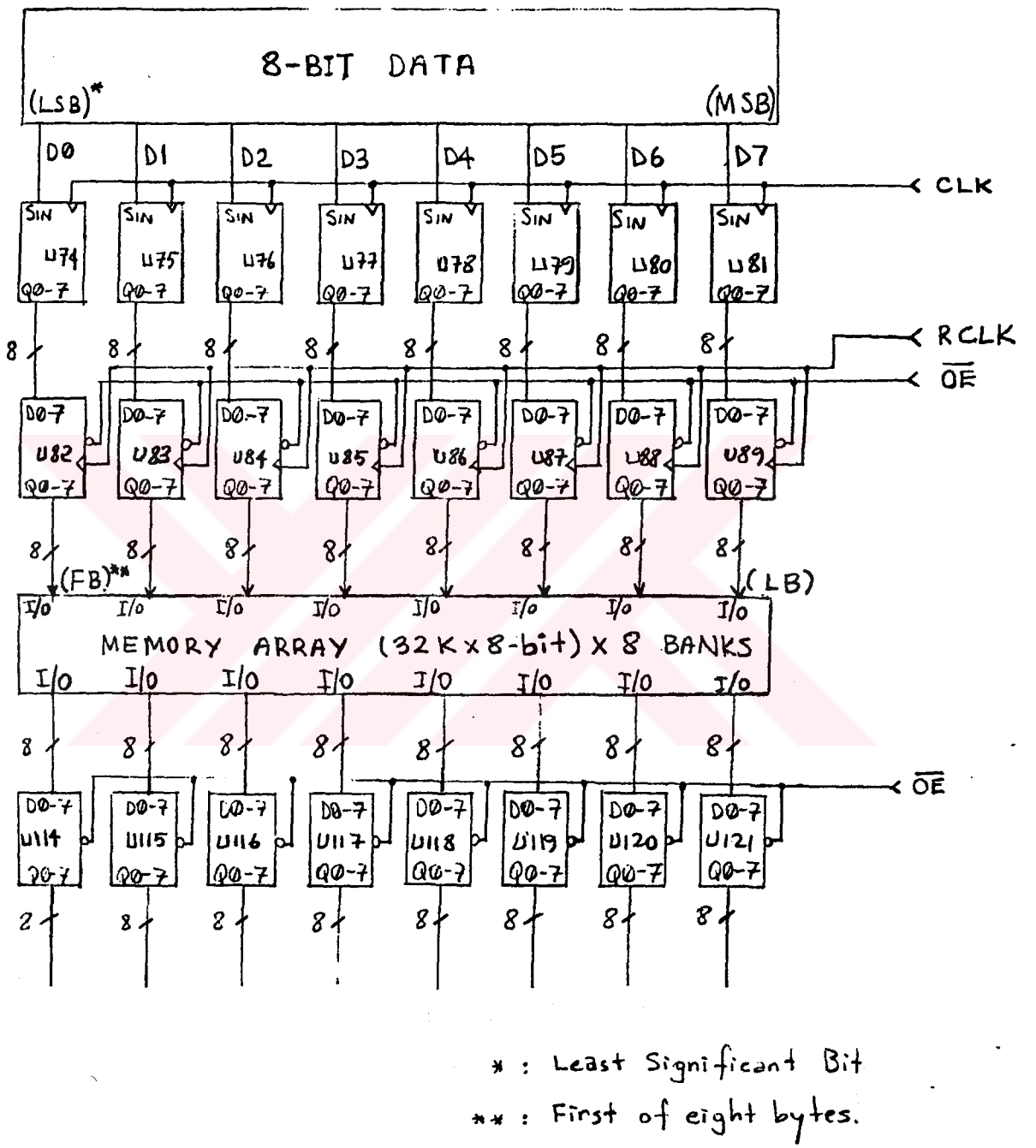


Figure 4.7. Memory buffer.

```
U74,Q7–U82,D0  U75,Q7–U82,D1  ..............  U81,Q7–U82,D7
U74,Q6–U83,D0  U75,Q6–U83,D1  ..............  U81,Q6–U83,D7
     .              .          ..............       .
     .              .          ..............       .
     .              .          ..............       .
U74,Q0–U89,D0  U75,Q0–U89,D1  ..............  U81,Q0–,U89,D7
```

Figure 4.8. Memory buffer connections.

4.2.2. Memory Array.

Two memory arrays are organized to store the samples of two subsequent frames of video signals. 32 Kbytes static RAM's are used in 8-banks to obtain an array of 256 Kbytes, as shown in Figure 4.9.

There are 625 lines in a frame of video signal. The scanning time for a single line is 64 µsec. ADC takes samples at every 66.66 nsec. Therefore, it is possible to take 512 samples from each line, (512x512=256 Kbytes) memory locations are necessary- which is the memory capacity of the most of the modern imaging systems.

Memory arrays are organized in page mode. That is, outputs of eight memory buffers are written into eight different memories at the same address location and at the same time.

Hitachi HM62256, 256KwordsX8-bit static RAM's are used. Address pins, chip select($\overline{CS}$) and write enable($\overline{WE}$) strobes of eight memory chips are connected together.Read cycle 2.

and write cycle 2. are chosen for their simplicity to imply. Output enable($\overline{OE}$) is always kept low[5].

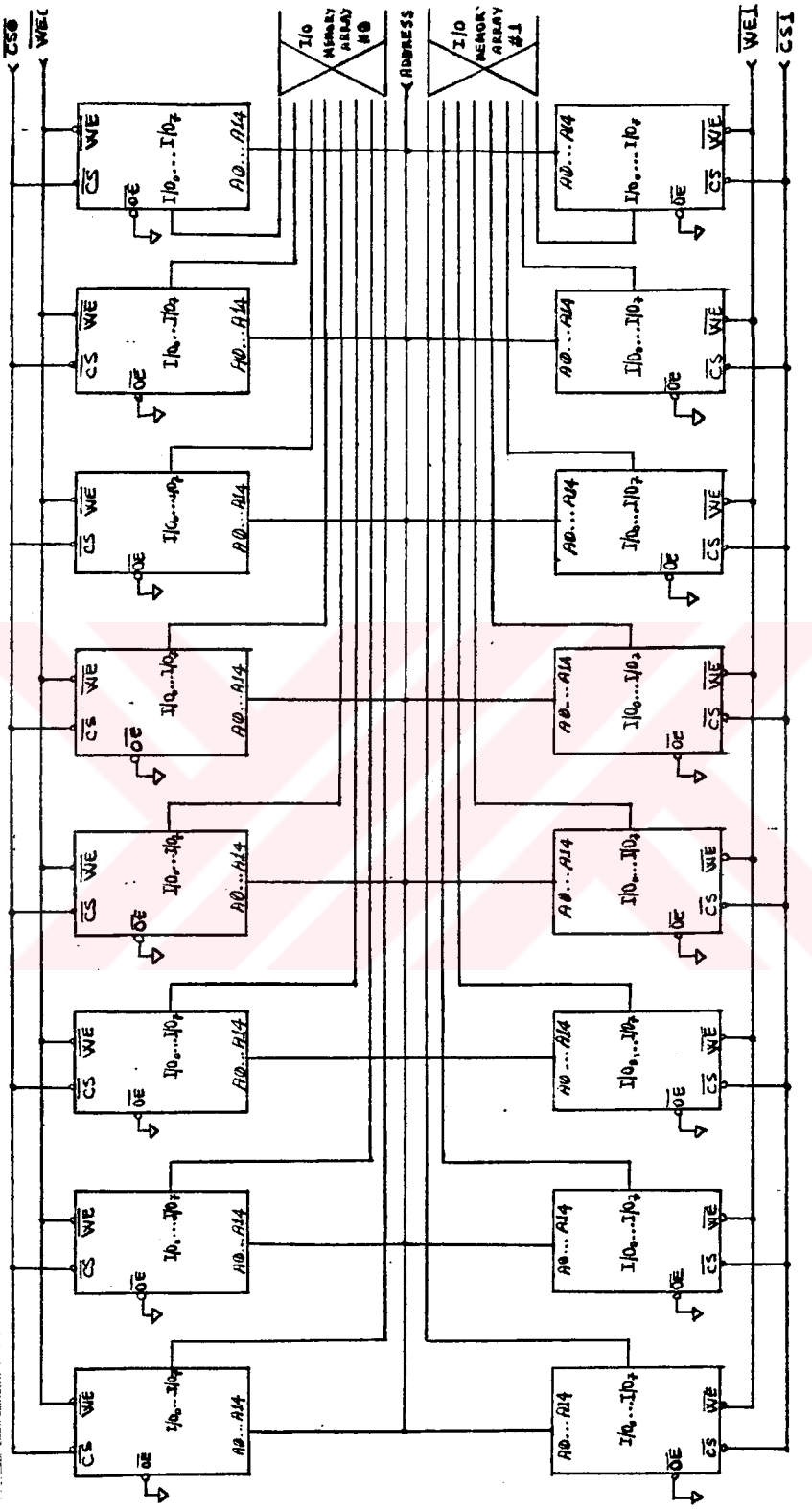


Figure 4.9. Circuit diagram of memory array.

4.2.3. Control Strobe Signals Generation.

Control signals required for memory read/write, enabling the memory input buffers, obtaining frozen images and x-ray generator energy level selection are generated by this unit.

The complete circuit diagram of the video signal control board is given in Figure 4.10. Synchronization pulses are taken directly from the test point "S" on the video control board I in VIDEOMED N, Appendix B. The synch. pulses at this test point swings between 0V and -5V. It is first attenuated to a reasonable level in order not to load the test point and then amplified by an inverting amplifier using U6. Then, it is fed to an AND gate to increase fan-out

Timing diagram showing synchronization pulses and how Even/$\overline{\text{Odd}}$(E/$\overline{\text{O}}$) field strobe is obtained is given in Figure 4.11. What is called, vertical synch. pulses, take place between points A and B, C and D[6]. The scanning of an even field ends at point A and the scanning of an odd field starts at point B. Point C is the end point of an odd field and point D is the starting point of an even field. The monostable U7 generates two pulses of duration of 4 µsecs. at $\overline{\text{Q1}}$ output and of 6 µsecs. at $\overline{\text{Q2}}$ output of U7 with every rising edge of synch. pulses. These are applied to the clock inputs of D flip-flops in U8. The signal at TP2 is set low whenever vertical synch. pulses are faced, otherwise remaining high. TP2 is low with two different durations: one

is 15x32 μsecs. and the other is 16x32 μsecs. The monostable U9 generates negative going pulses of duration of 15.5x32 μsecs. at every falling edge of TP2. This is fed to clock input of D flip-flop U11. Even/$\overline{\text{Odd}}$ field strobe is obtained at Q1 output of U11. Point E indicates the beginning of an odd field and point F indicates that an even field starts.

Field data window strobe(FDW) is generated during every field. There is an adjustable delay at the beginning of every field, as shown by T1 in Figure 4.12. JK flip-flop U13 is set high on the falling edge of TP4 indicating that it is time to start data acquisition from the related field. FDW strobe is reset after 256 lines are sampled. An 8-bit synchronous counter determines the width of the field data window.

One of every two consecutive frames is belonging to an image obtained at low energy and the other at high energy. Low/$\overline{\text{High}}$(L/$\overline{\text{H}}$) strobe is obtained at Q1 output of U17. The width of its low duration part is modified due to the reasons discussed in Chapter 5.

When it is required to obtain a frozen image on the monitor, $\overline{\text{FREEZE}}$ control is set low. $\overline{\text{FREEZE LOCK}}$($\overline{\text{FL}}$) strobe is reset on the next rising edge of [L/$\overline{\text{H}}$]$_1$. When $\overline{\text{FL}}$ is low, no data is written into any of the memory arrays. Two memory arrays are read out together continuously until $\overline{\text{FL}}$ is high. Timing diagram of the FREEZE operation is given in Fig.4.13.

X-ray generator unit determines the energy level of the x-rays it produces according to the reference voltages produced by the x-ray generator regulator unit. Reference voltages between -1.25V and -7.5V fit energy levels between 25 kVp and 150 kVp. In the control circuit given in Figure 4.14. a negative reference voltage is generated when $[L/\overline{H}]_2$ strobe is low. A reference voltage more negative than the previous one is generated to produce high energy x-rays. While $[L/\overline{H}]_2$ is high, the reference voltage at C_Y input of analog multiplexer U22 is transmitted to the output. And, as $[L/\overline{H}]_2$ is low, reference signal at C_X input is transmitted to the output. Various x-ray energies can be obtained by the user adjusting R53 and R56. When KEdge Imaging Switch is closed, reference voltage produced by our system is applied to x-ray generator unit through B_X channel of analog mux. and subsequently a buffer amplifier. On the other hand, when S_1 is open, x-ray generator unit is controlled by the x-ray generator regulator unit, already existing in the angiography system(See Appendix D. for details of the modification made in the system).

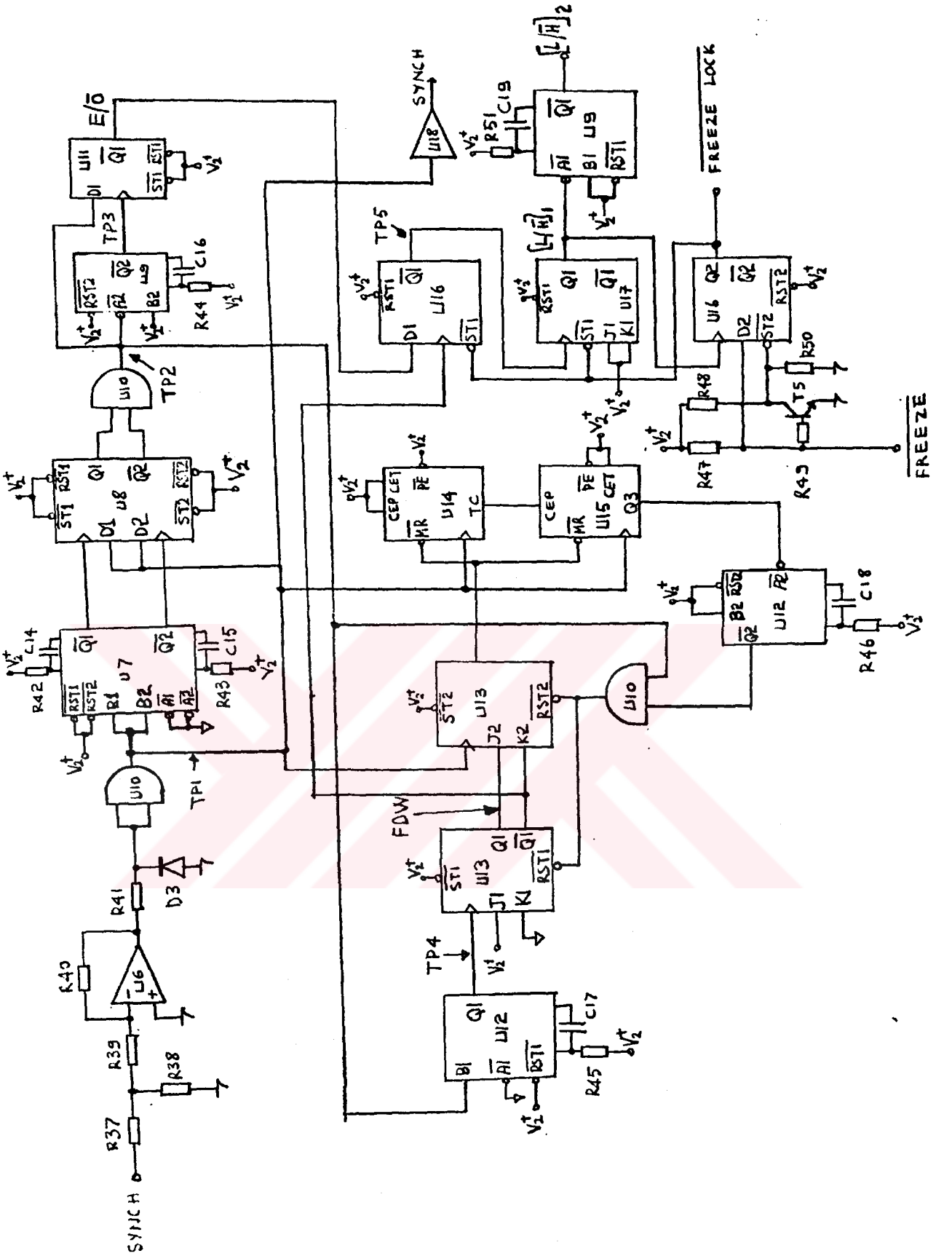


Figure 4.10. Circuit diagram of video signal control board.

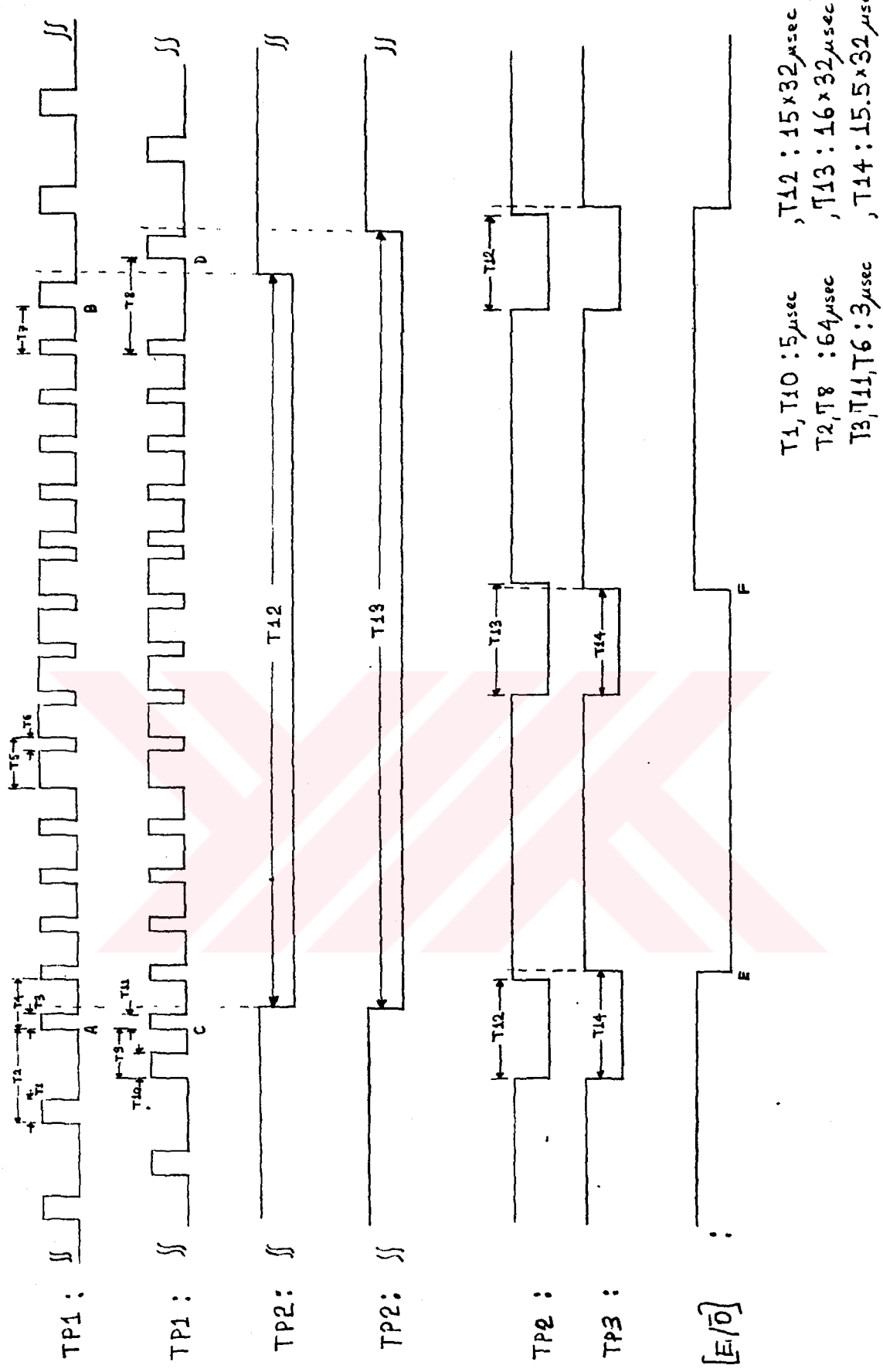


Figure 4.11. Timing diagram of Even/$\overline{\text{Odd}}$ field seperation.

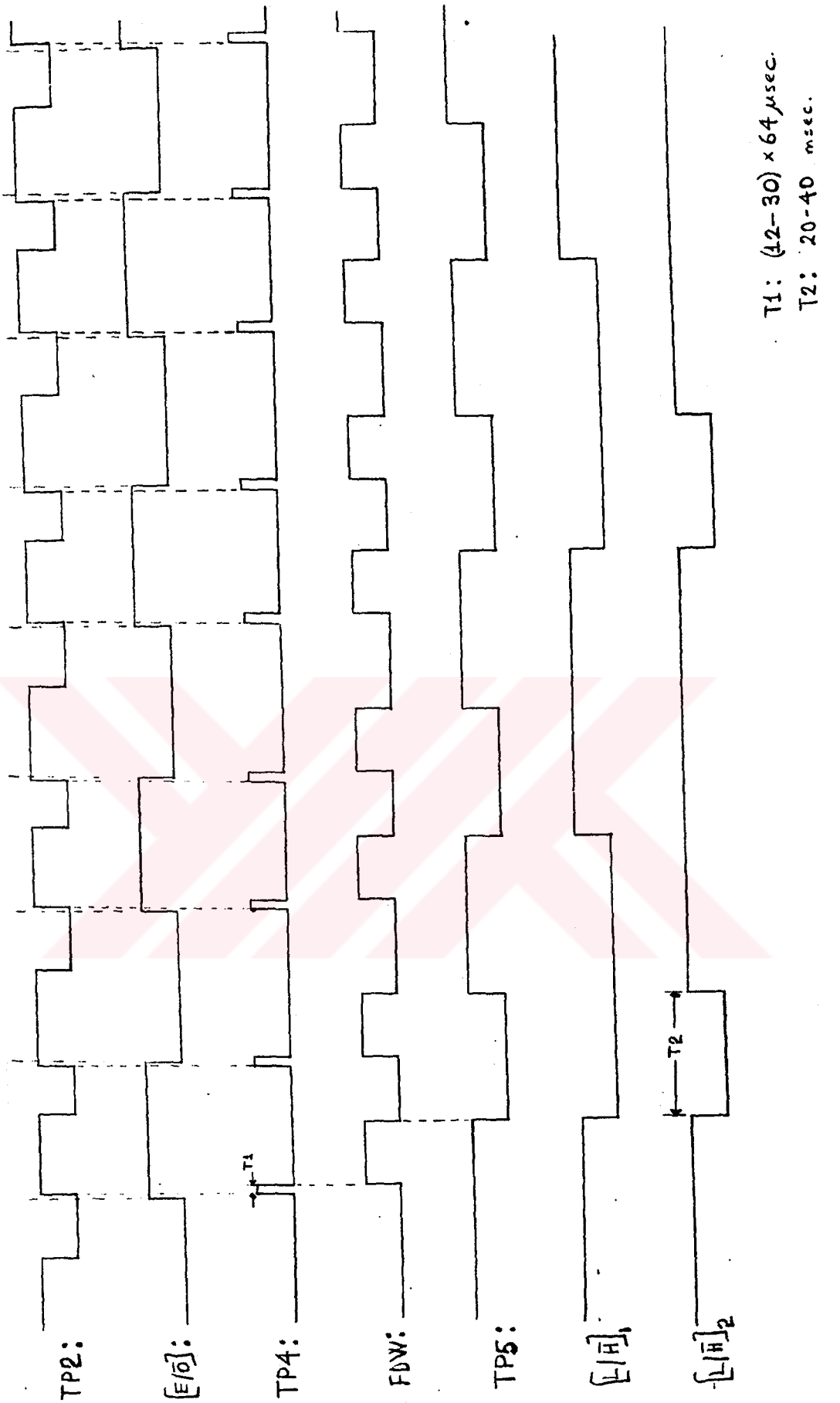


Figure 4.12. Timing diagram of Low/$\overline{\text{High}}$ strobe generation.

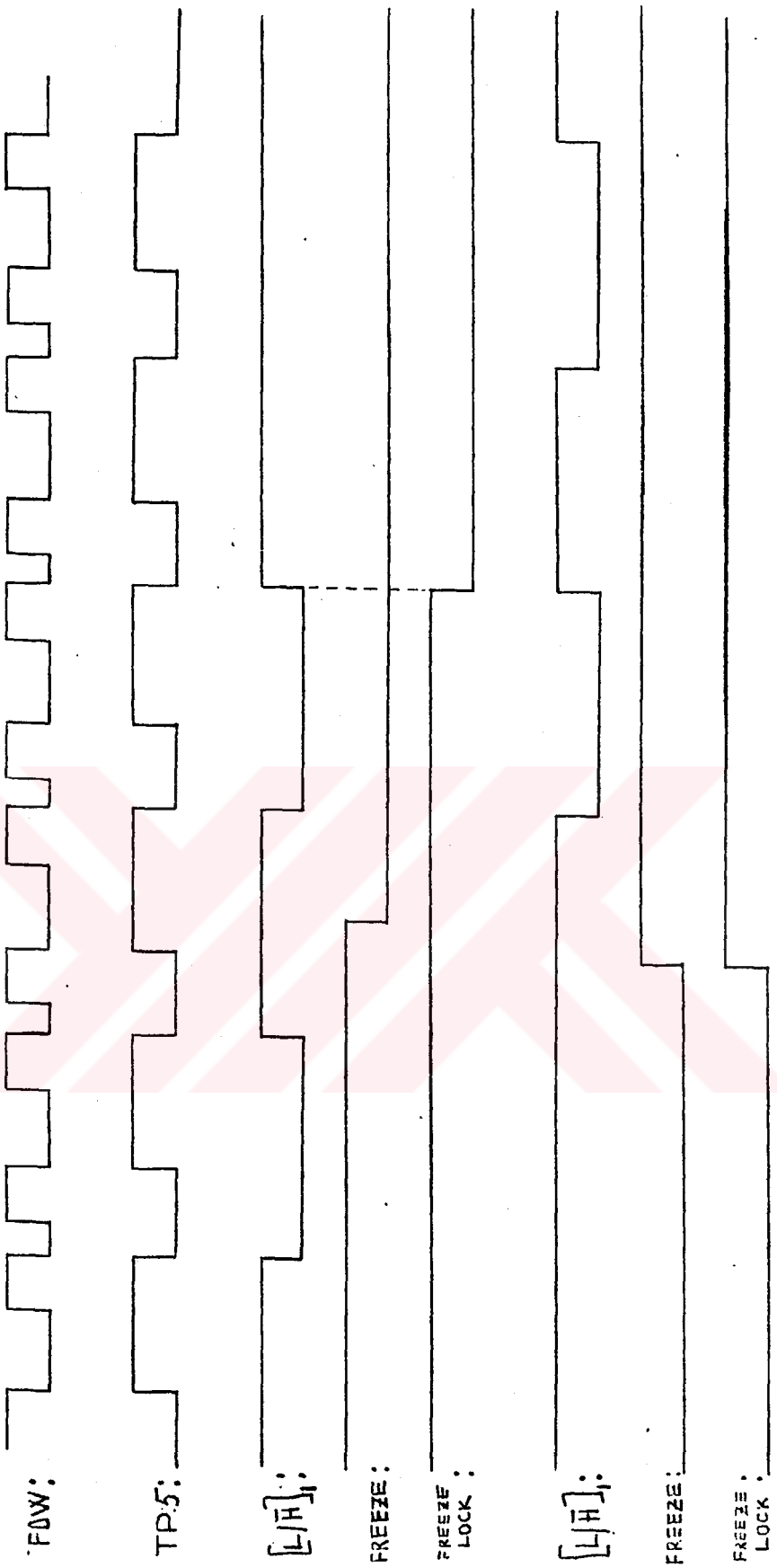


Figure 4.13. Timing diagram of FREEZE operation.

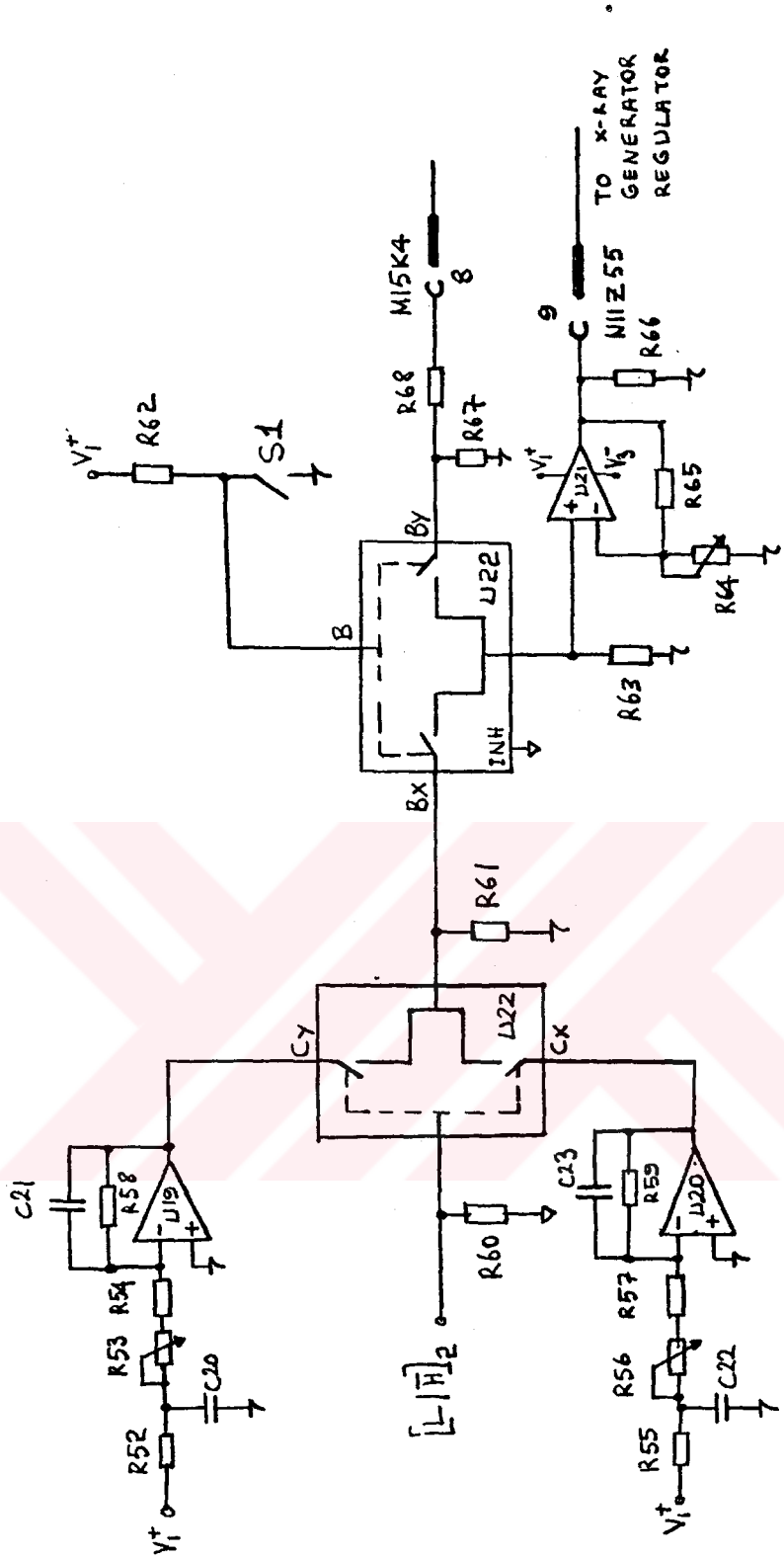


Figure 4.14. Circuit diagram of x-ray generator control board.

4.2.4 Real-Time Read Control and Clock Generation.

A crystal oscillator of 15.000 MHz. is used to obtain the main clock of the whole circuit, Figure 4.15. Then it is divided by eight to drive the memory input/output buffers and memory read/write control circuit. U68 and U69 both 3 to 8 decoders. They are connected to the output enables inputs of real-time-read buffers(U133-U140) and memory output buffers (U114-U129) to achieve real time subtraction. These buffers are enabled one by one at every 66.66 nsecs. And, then their outputs are added by an eight-bit full adder. When FL strobe is low, U69 is disabled. Consequently, U133-U140 are disabled. Two memory output buffer arrays, U114-U121 and U122-U129 are continued to enable until FREEZE operation is ended.

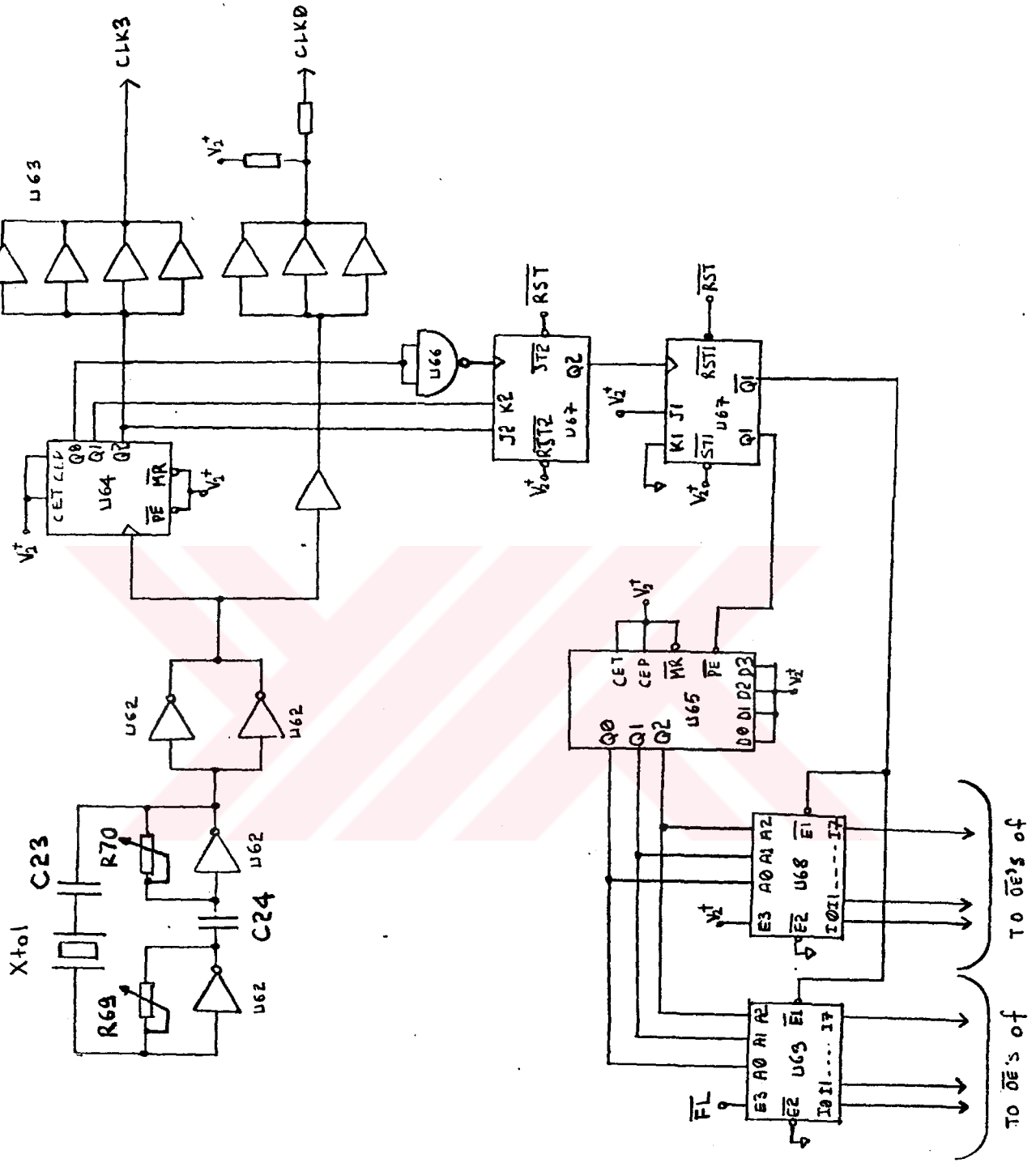


Figure 4.15. Circuit diagram of real-time read control and clock generation.

4.2.5. Memory Read/Write.

Storing the samples of video signals into the memory arrays are achieved by memory write control circuit. The circuit diagram is given in Figure 4.16. The operation of the circuit can be explained as follows: After FDW is set high, Line Data Window(LDW) is set high on the rising edge of TP1 which may be called line delay. Its duration at low is adjustable. After LDW is set high with the rising edge of CLK3, Synchronous counters U55 and U56 start counting until the width of LDW at high reaches (512 x 66.66) nanoseconds. In other words, it stops after 512 samples are stored into memory.

Timing diagram of memory write operation is given in Figure 4.17. With every rising edge of CLK3, Q1 output of U53 is set low. Subsequently, $\overline{CS}$, $\overline{WE}$ and finally $\overline{OE}$ of memory input buffers are set low. After data appears at the output of memory input buffers, it is stored into the memory location indicated by the address counter. Then, $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ are all set high, completing the memory write operation.

When $\overline{FL}$ is set low, $\overline{CS}$ is kept low and $\overline{WE}$ is kept high so that two memory arrays are read out continuously.

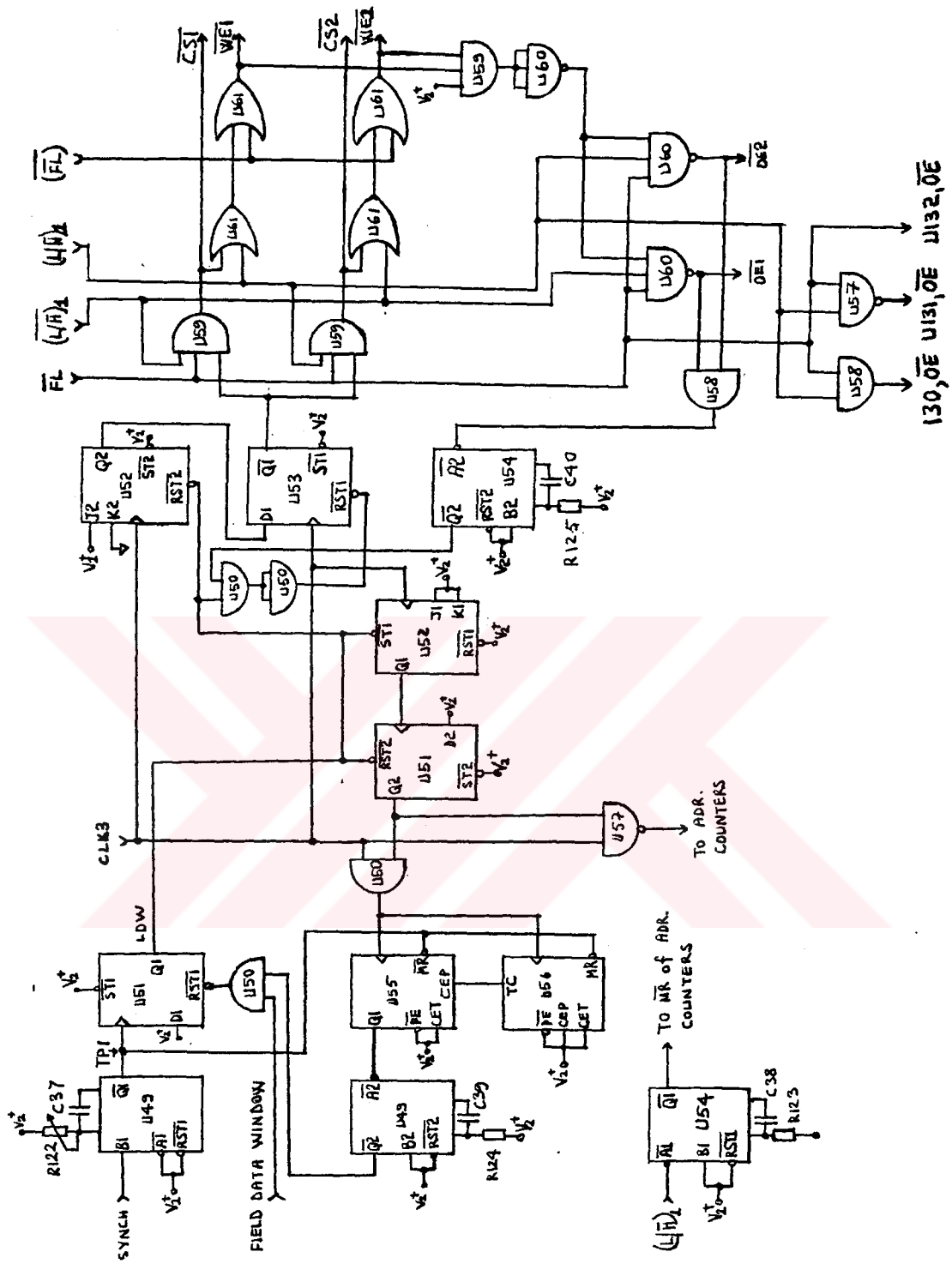


Figure 4.16. Circuit diagram of memory read/write control board.

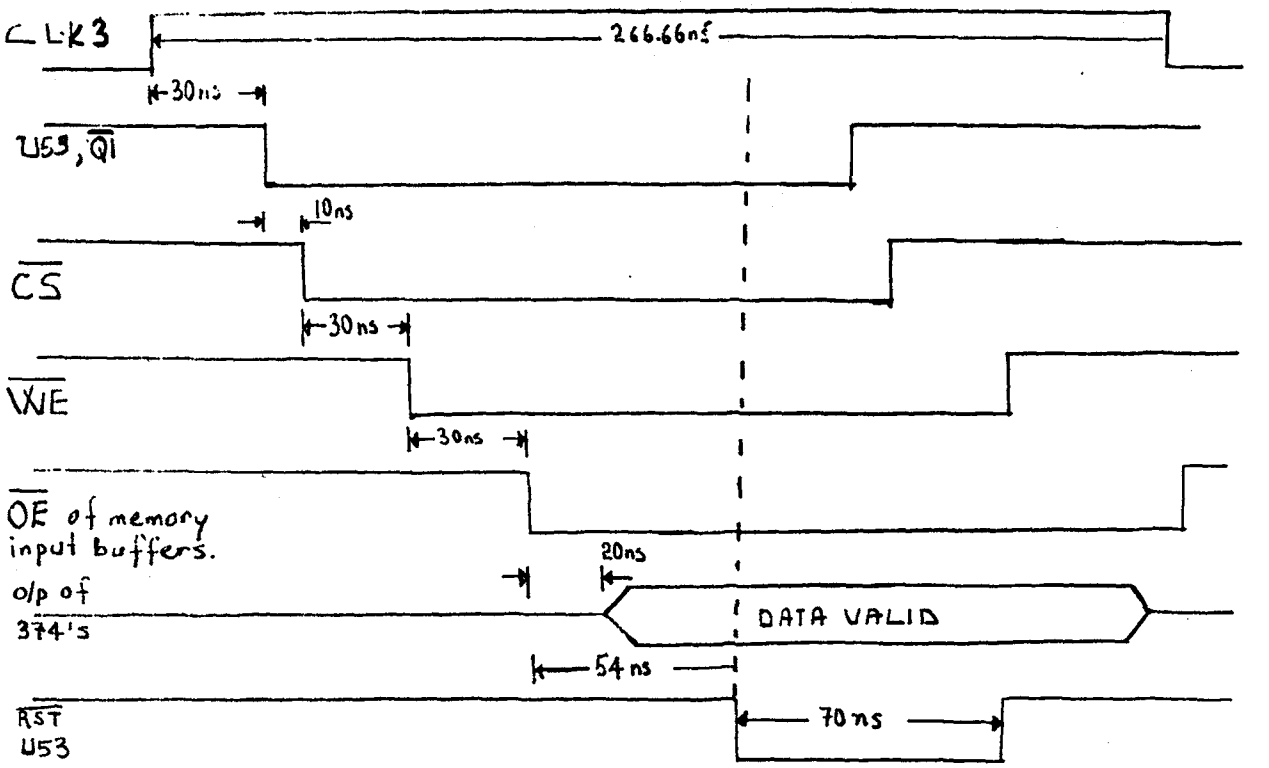


Figure 4.17. Timing diagram of memory write operation.

CHAPTER 5

RESULTS AND CONCLUSIONS

A real-time dual-energy x-ray digital subtraction angiography system is designed and implemented to operate with a coronary angiography system, already existing in TYIH. The device triggers x-ray generator for two different x-ray energies:one is below K-edge and the other is above K-edge. Then, it takes samples of the video signals carrying two dimensional contrast information at a rate of 15 MHz. This data is stored into two memory arrays of 256 Kbytes each. Finally, a composite video signal is generated to observe the subtracted images on a TV monitor.

This subsystem can be operated with any angiography system having a DC-regulated x-ray generator. Presently, it is not possible to use this system as a general video digitizer. signals. It can accept only negative signals as illustrated in Figure 3.1. An inverting video amplifier at the input stage should be included in the future models.

It is easy to use the developed device during catheterization sessions. While normal session is continued, it is possible to observe subtracted images immediately after a push-button named KEIS(K-Edge Imaging Switch) is pressed after switch S4 is set for manual mode(See Appendix D. for details). And, the normal operation can be returned

whenever mentioned switches are set to previous positions. It is planned to control the switch S4 together with KEIS. This will provide one-touch operation.

Another feature of the system is that it is capable of freezing subtracted images on the monitor. Thus, the surgeon can record images which are valuable in diagnosis.

It can be argued that the only disadvantage of the dual-energy imaging is the exposure of the patient to high x-ray energy. This problem can be overcome by shortening the high energy pulse interval. That is why $[L/\overline{H}]_2$ signal in 4.2.3. is applied to x-ray generator control unit instead of $[L/\overline{H}]_1$ signal. The width of low duration part of $[L/\overline{H}]_2$ can be adjusted.

What we obtained in Equation 2.6. means that the subtracted image is contributed by only the Iodine concentration in the vessel. But, as also stated in 2.3, the actual image contains information about other tissues and bones as well. This causes some artifacts in the image,which can be solved by image processing techniques after subtracted data is acquired by a suitable computer.

One major problem is faced during the design of PCB layouts. Since the system works at 15 MHz., it is cumbersome to arrange the locations of components. For the future

designs, a rack system consisting of EURO-CARDS must be considered.

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[10] R.E. Alvarez, R.A.Lehmann, A.Macowski, W.R.Brody, "Limitations to accuracy in digital fluoroscopy", Digital Radiography, vol. 314, pp.196-209, 1981.

[11] R.Schittenhelm, " Imaging systems for digital radiography: present status and future prospects ", Electromedica 54, pp. 72-81, 1986.

[12] Gerald L. Hansen, "Introduction to solid-state television systems "; Prentice-Hall Inc., 1969.

[13] Clyde N. Herrick, " Television theory and servicing: black/white and color ", Reston Publishing Company,Inc., 1976.

[14] Henry W. Ott, "Noise reduction techniques in electronic systems ", John Wiley & Sons, 1976.

[15] Charles Kittel, " Introduction to solid state physics", John Wiley & Sons, 1986.

[16] Philips Data handbook, TTL Logic Series, 1986.

[17] MATLAB User's guide.

APPENDICES

APPENDIX A.

LIST OF PAPERS PUBLISHED BY THE AUTHOR

[1] H.Özdemir, Z. İder, H. Köymen, Gerçek-zamanlı çift-enerjili x-ışınlı sayısal çıkarmalı görüntüleme, ODTÜ EEMB 30.yıl sempozyumu, sayfa 21-23, 8-10 Şubat, 1989 Ankara.

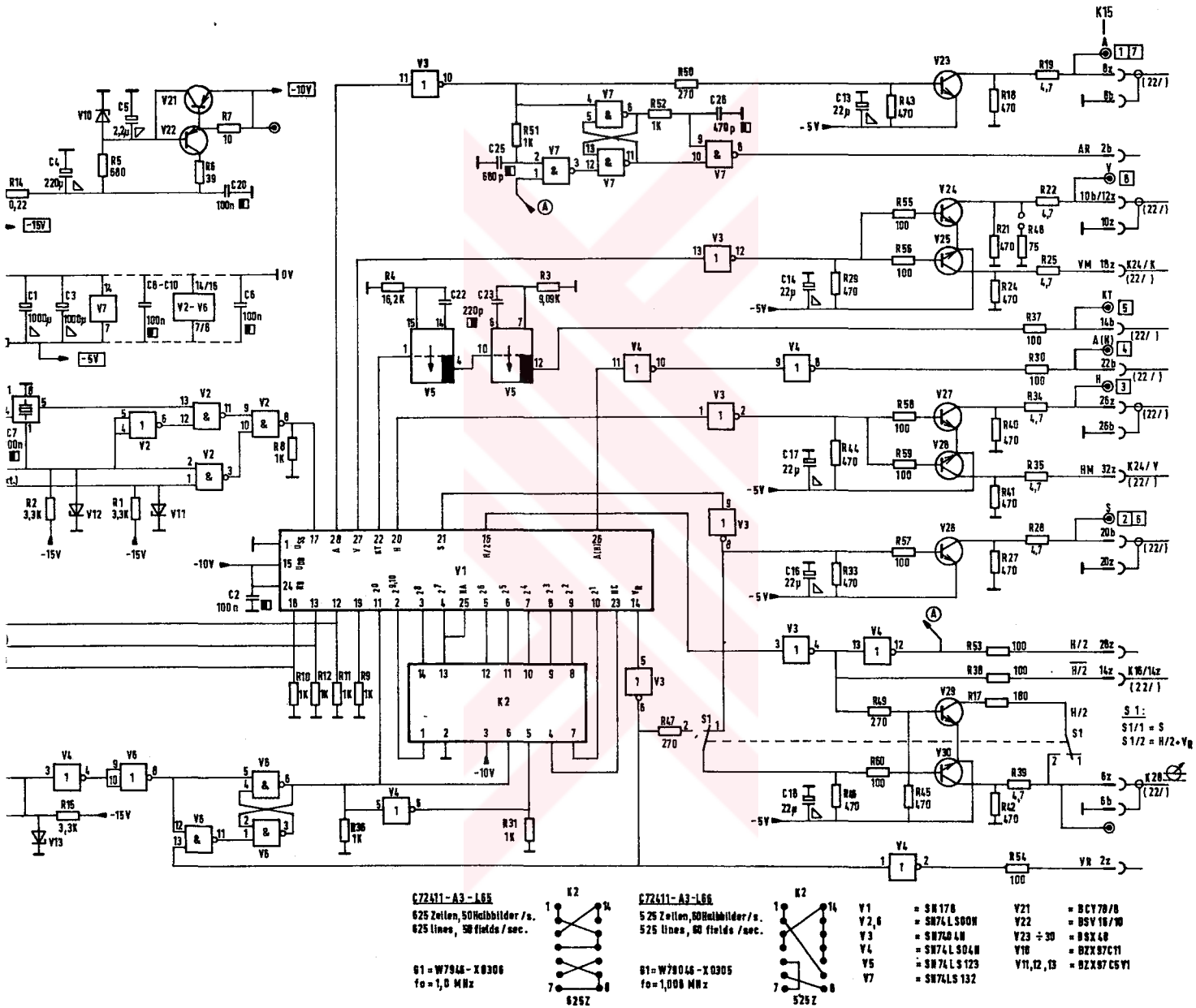
[2] H.Özdemir, H.Köymen, " Real-time dual-energy x-ray digital subtraction imaging ", Proceedings V. Medirerranean conference on medical and biological engineering ", pp.340-341,Sep. 1989.

APPENDIX B

CIRCUIT DIAGRAM OF VIDEO SIGNAL GENERATOR BOARD IN " SIEMENS PANDOROS OPTIMATIC " CORONARY ANGIOGRAPHY SYSTEM.

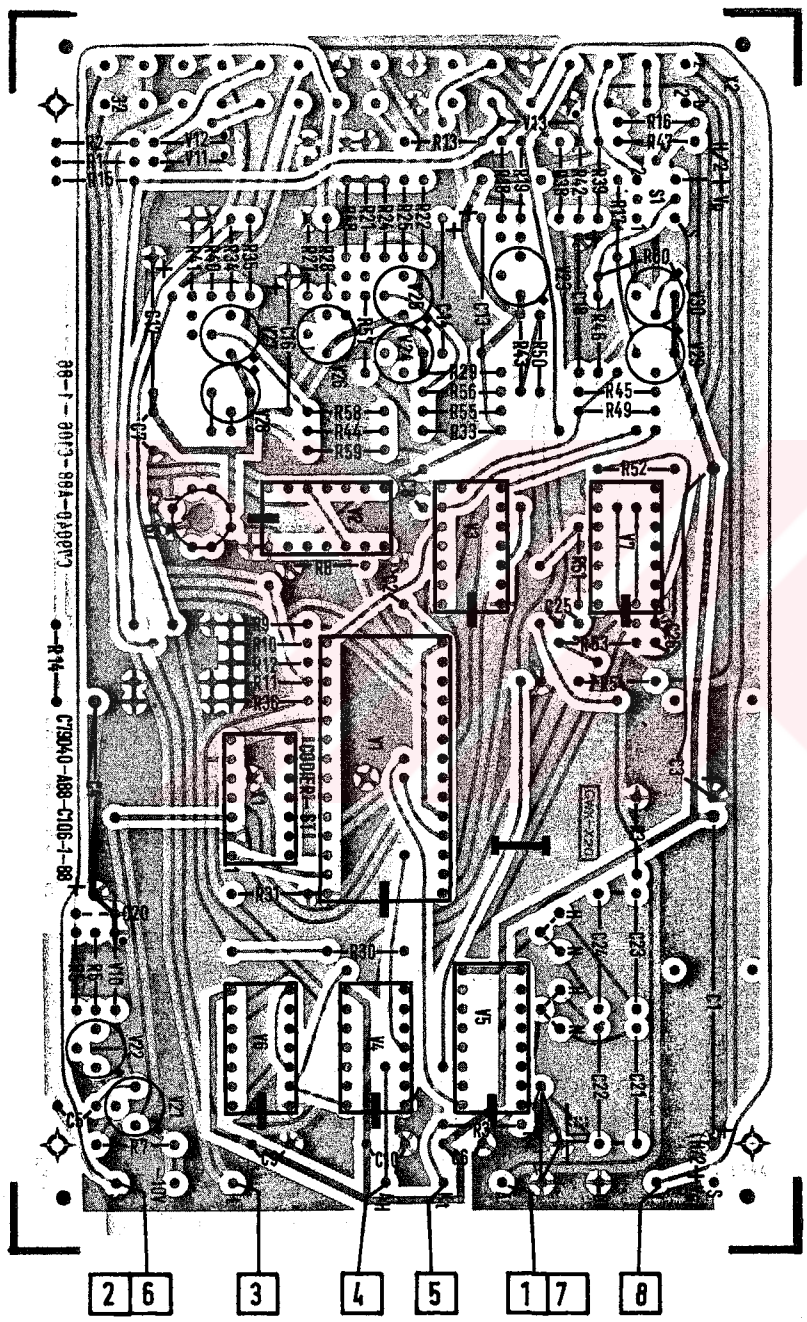
The " Blanking " and " Synchronization " pulses are available on Video Signal Generation Board existing in the angiography system as test points. These signals are used directly by the subsystem. Blanking and Synchronization pulses are available at test points A and S, respectively.

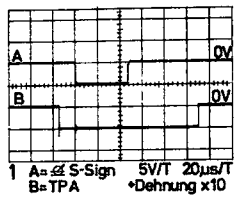
Circuit diagram and a photo of related board is given in the following pages.


K15
-10V
-15V
0V
-5V
V1
V2
V3
V4
V5
V6
V7
V10
V11
V12
V13
V21
V22
V23
V24
V25
V26
V27
V28
V29
V30
K2
S1
S1/1 = S
S1/2 = H/2+V_R
H/2
H/2
AR 2b
V 6
10b/12z
10z
VM 18z
K24/K
KT 5
14b
A(K) 4
22b
H 3
26z
26b
HM 32z
K24/V
S 2 6
20b
20z
H/2 28z
H/2 14z
K16/14z
6z
K28
6b
VR 2z
(22/1)
C72411-A3-L65
625 Zeilen, 50 Halbbilder/s.
625 lines, 50 fields/sec.
61 = W7946-X0306
fo = 1,0 MHz
C72411-A3-L66
525 Zeilen, 60 Halbbilder/s.
525 lines, 60 fields/sec.
61 = W7946-X0305
fo = 1,008 MHz
625Z
525Z
V1 = SN 178
V2,6 = SN74LS00N
V3 = SN7400N
V4 = SN74LS04N
V5 = SN74LS123
V7 = SN74LS132
V21 = BCY78/8
V22 = BSV16/10
V23 ÷ 30 = BSX60
V10 = BZX97C11
V11,12,13 = BZX97C5V1

/IDEOMED N, Zentrale: Platte I
C.C.U : board I

C72411-A3-L65...L66-1-98
Juni 1980





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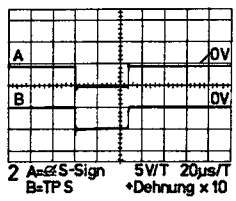
B=TPA +Dehnung x10



2 A=⊿S-Sign 5V/T 20µs/T
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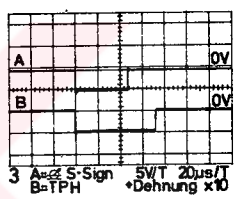

3 A=⊿S-Sign 5V/T 20µs/T
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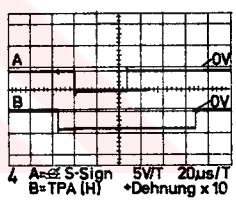
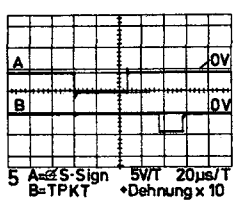


4 A=⊿S-Sign 5V/T 20µs/T
B=TPA (H) +Dehnung x 10



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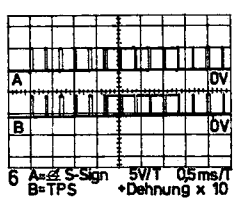
B=TPKT +Dehnung x 10



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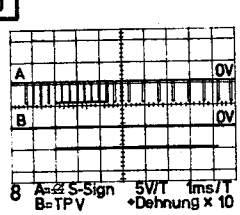
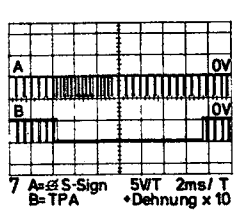
B=TPS +Dehnung x 10



8 A=⊿S-Sign 5V/T 1ms/T
B=TPV +Dehnung x 10



7 A=⊿S-Sign 5V/T 2ms/ T
B=TPA +Dehnung x 10

APPENDIX C.

LUT CONVERSION DATA

Data to be written into EPROM on LUT board is listed below.

A	D	A	D	A	D	A	D	A	D	A	D	A	D
00	FF	27	E7	4E	CE	75	B6	9C	9C	C3	7F	EA	55
01	FF	28	E6	4F	CE	76	B5	9D	9C	C4	7E	EB	53
02	FE	29	E5	50	CD	77	B5	9E	9B	C5	7E	EC	51
03	FE	2A	E5	51	CC	78	B4	9F	9A	C6	7D	ED	4F
04	FD	2B	E4	52	CC	79	B3	A0	9A	C7	7C	EE	4D
05	FC	2C	E3	53	CB	7A	B3	A1	99	C8	7B	EF	4C
06	FC	2D	E3	54	CA	7B	B2	A2	98	C9	7A	F0	4A
07	FB	2E	E2	55	CA	7C	B1	A3	98	CA	79	F1	47
08	FA	2F	E2	56	C9	7D	B1	A4	97	CB	78	F2	45
09	FA	30	E1	57	C9	7E	B0	A5	96	CC	77	F3	43
0A	F9	31	E0	58	C8	7F	B0	A6	96	CD	76	F4	40
0B	F8	32	E0	59	C7	80	AF	A7	95	CE	76	F5	3D
0C	F8	33	DF	5A	C7	81	AE	A8	94	CF	75	F6	3A
0D	F7	34	DE	5B	C6	82	AE	A9	93	D0	74	F7	37
0E	F6	35	DE	5C	C6	83	AD	AA	92	D1	73	F8	33
0F	F6	36	DD	5D	C5	84	AC	AB	92	D2	72	F9	2F
10	F5	37	DD	5E	C4	85	AC	AC	91	D3	71	FA	2A
11	F5	38	DC	5F	C4	86	AB	AD	90	D4	70	FB	24
12	F4	39	DB	60	C3	87	AA	AE	90	D5	6F	FC	1D
13	F3	3A	DB	61	C3	88	AA	AF	8F	D6	6E	FD	12
14	F3	3B	DA	62	C2	89	A9	B0	8E	D7	6D	FE	01
15	F2	3C	D9	63	C1	8A	A8	B1	8D	D8	6C	FF	00
16	F1	3D	D9	64	C1	8B	A8	B2	8D	D9	6B		
17	F1	3E	D8	65	C0	8C	A7	B3	8C	DA	69		
18	F0	3F	D8	66	BF	8D	A6	B4	8B	DB	68		
19	EF	40	D7	67	BF	8E	A6	B5	8A	DC	67		
1A	EF	41	D6	68	BE	8F	A5	B6	8A	DD	66		
1B	EE	42	D6	69	BE	90	A4	B7	89	DE	65		
1C	EE	43	D5	6A	BD	91	A4	B8	88	DF	64		
1D	ED	44	D5	6B	BC	92	A3	B9	87	E0	63		
1E	EC	45	D4	6C	BC	93	A3	BA	87	E1	61		
1F	EC	46	D3	6D	BB	94	A2	BB	86	E2	60		
20	EB	47	D3	6E	BA	95	A2	BC	85	E3	5F		
21	EA	48	D2	6F	BA	96	A1	BD	84	E4	5D		
22	EA	49	D1	70	B9	97	A0	BE	83	E5	5C		
23	E9	4A	D1	71	B8	98	9F	BF	83	E6	5B		
24	E8	4B	D0	72	B8	99	9E	C0	82	E7	59		
25	E8	4C	D0	73	B7	9A	9E	C1	81	E8	58		
26	E7	4D	CF	74	B7	9B	9D	C2	80	E9	56		

APPENDIX D

MODIFICATIONS IN SIEMENS ANGIOGRAPHY SYSTEM

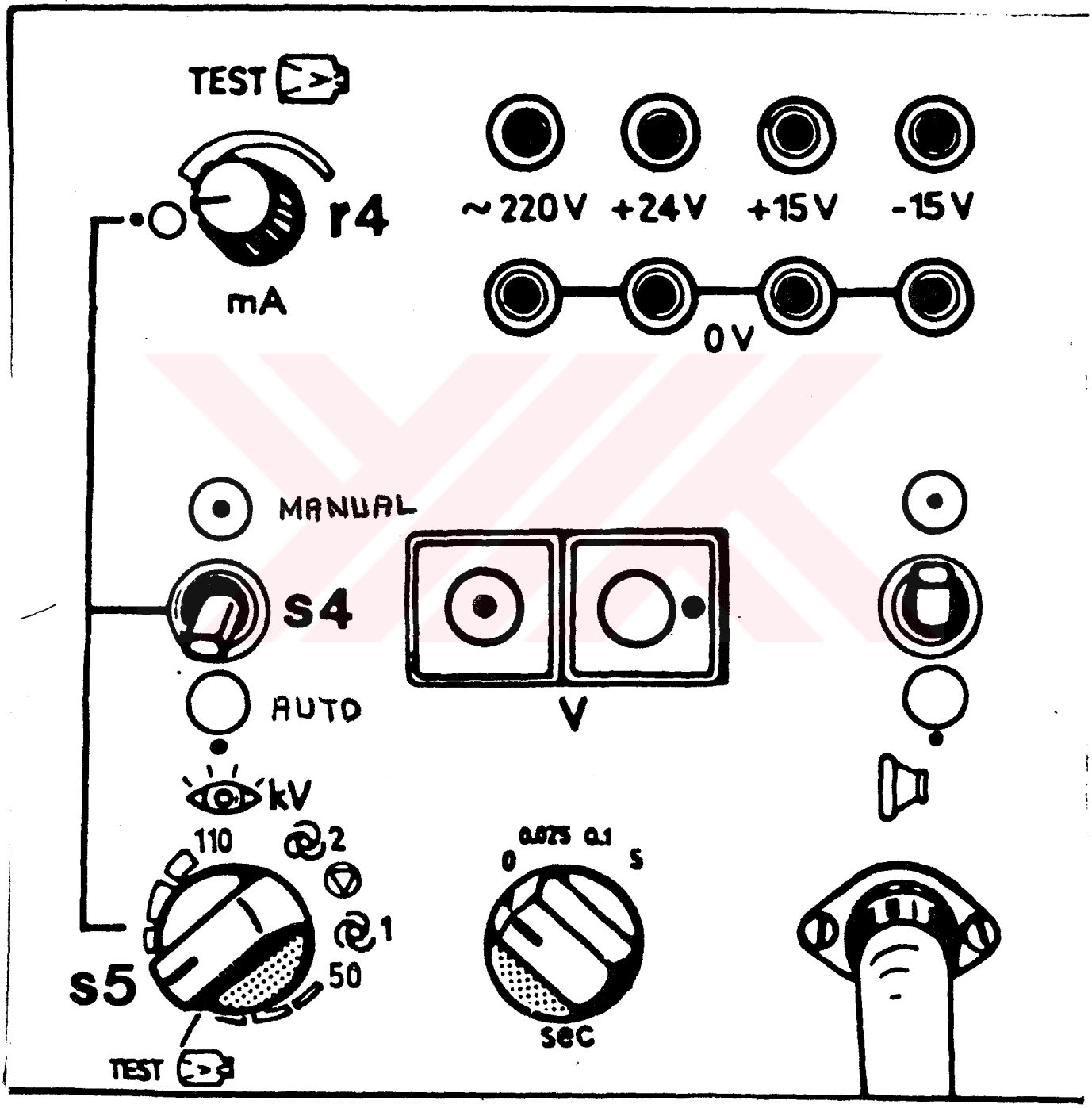
During K-Edge Imaging the modifications listed below should be done:

1. Switch S4 on panel M15 is positioned for adjusting x-ray generator manually.

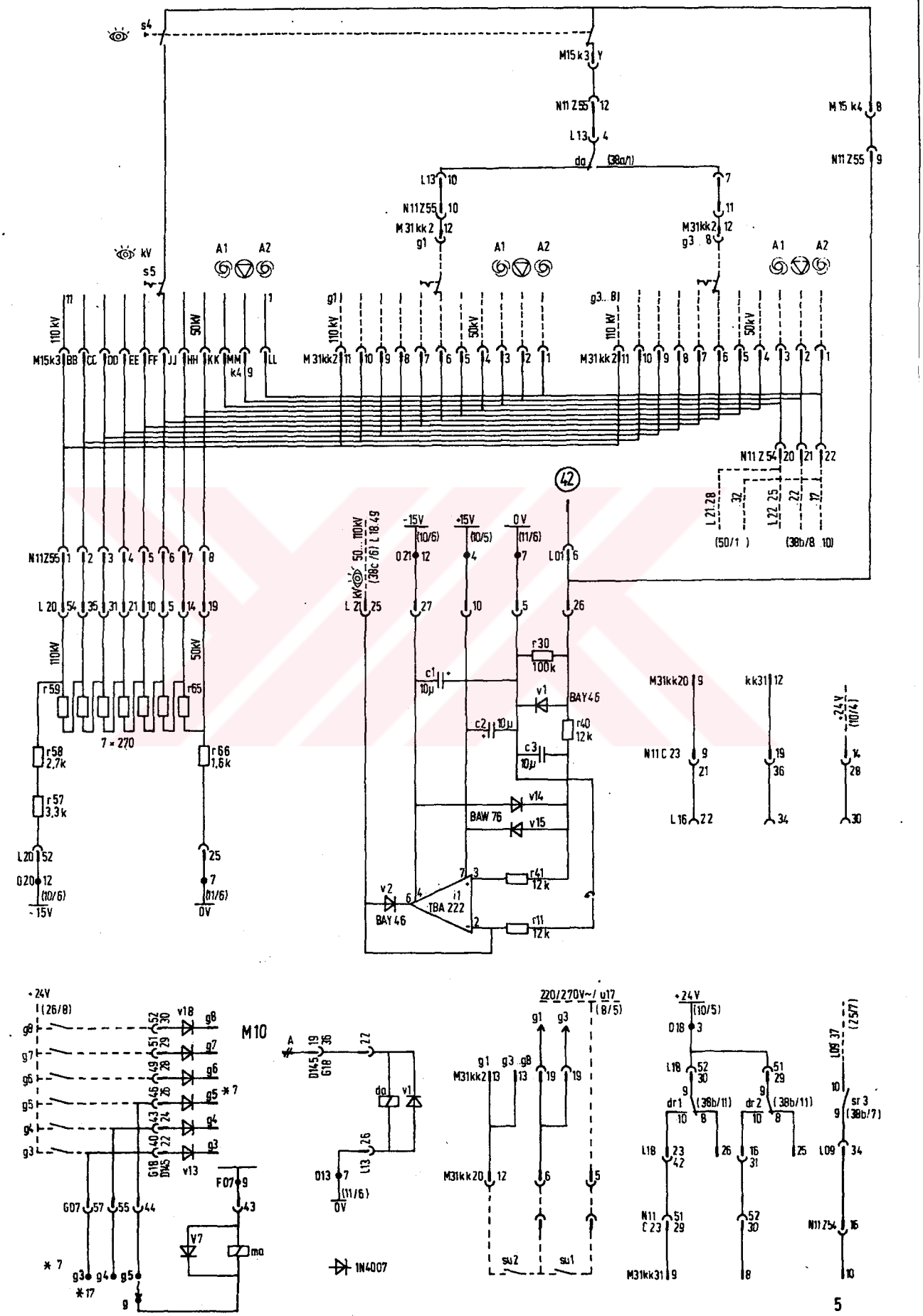
2. Cable connected to pin number 8 in connector k4 on panel M15 is disconnected. Then, it is reconnected to the subsystem. And, the related cable from the subsystem is connected to pin number 8 in connector k4 on panel M15.

A schematic diagram of front side of panel M15 and its circuit diagram is given in the following pages. A photo of panel M15 is also given.

Schematic diagram of front side of panel M15



Circuit diagram of M15 panel



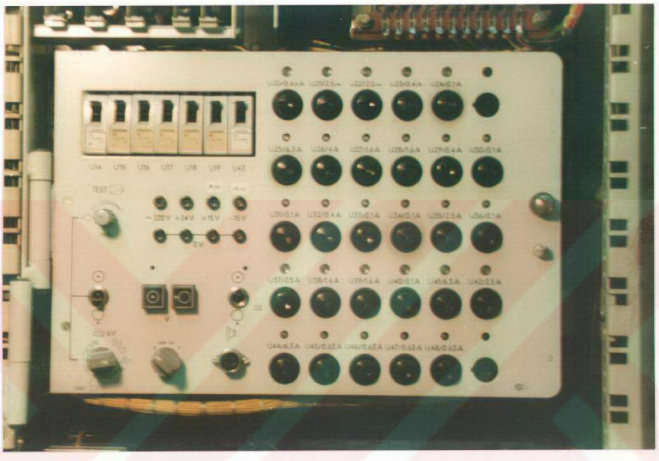


Photo of front side of M15 panel

APPENDIX E

DATA SHEETS

Data sheets of CA3127 and 82S16 are given in the following pages.

CA3127

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.) at 100 MHz*
- *Five independent transistors on a common substrate*

RCA-CA3127* consits of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127 useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

The CA3127 is supplied in the 16-lead dual-in-line plastic package (E suffix), 16-lead dual-in-line frit-seal ceramic package (F suffix), and is also available in clip form (H suffix). It operates over the full military temperature range of -55 to +125° C.

*Formerly RCA Dev. No. TA6206.

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

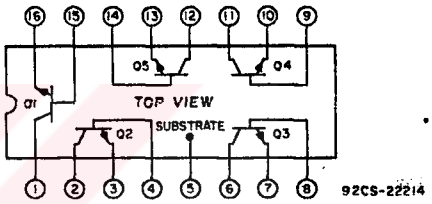


Fig. 1 — Schematic diagram of CA3127.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:

Any one transistor	85 mW
Total Package:	
For T_A up to 75° C	425 mW
For T_A > 75° C Derate Linearly at	6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating	-55 to +125° C
Storage	-65 to +125° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265° C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	20 V
Collector-to-Substrate Voltage, V_{CIO}*	20 V
Collector Current, I_C	20 mA

*The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

CA3127

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\ \mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible cap or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\ k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration, f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	kΩ
Input Capacitance	$V_{CE} = 6$ V	–	3.7	–	pF
Output Capacitance	$I_C = 1$ mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

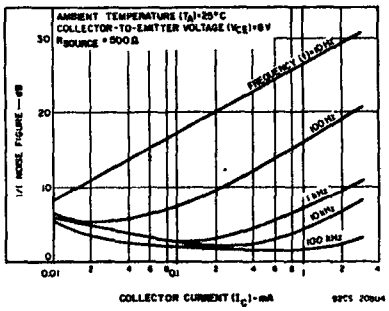


Fig. 2 – 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

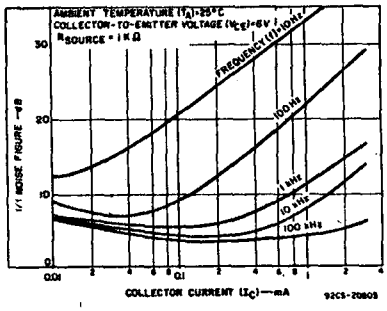


Fig. 3 – 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

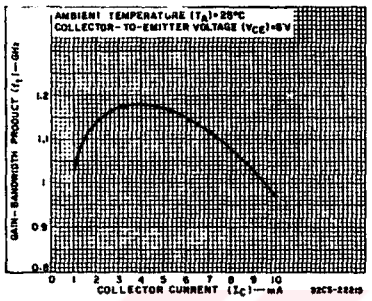


Fig. 4 – Gain-bandwidth product as a function of collector current.

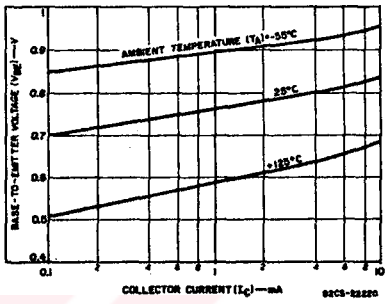


Fig. 5 – Base-to-emitter voltage as a function of collector current.

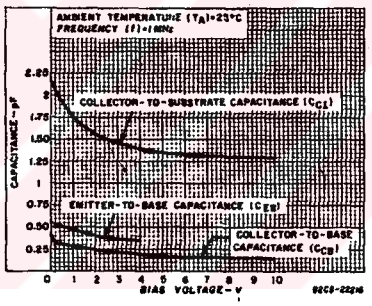


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.018	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

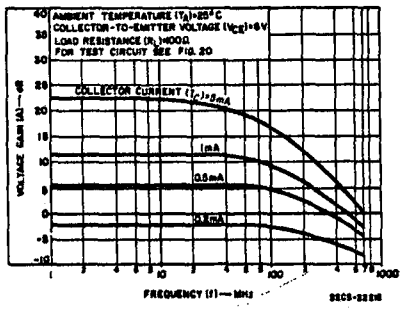


Fig. 7 – Voltage gain as a function of frequency at R_L = 100 Ω.

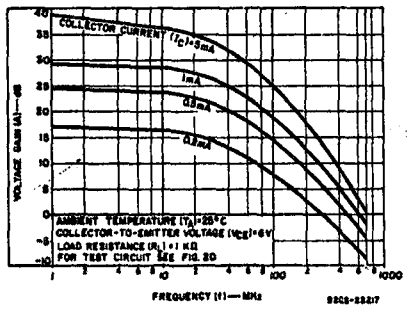


Fig. 8 – Voltage gain as a function of frequency at R_L = 1 kΩ.

CA3127

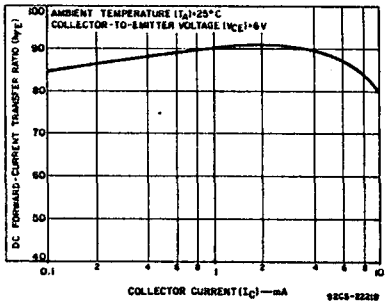


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

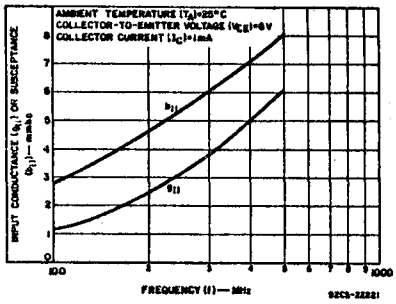


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

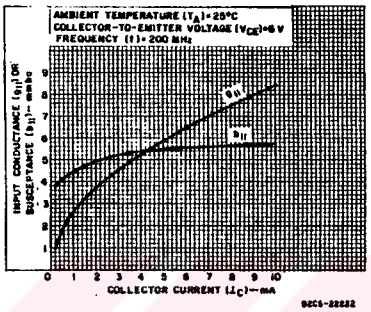


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

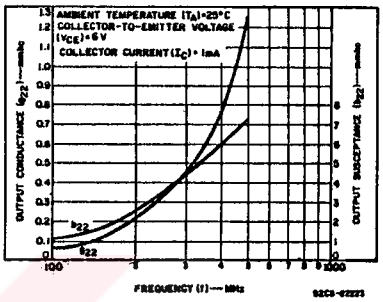


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

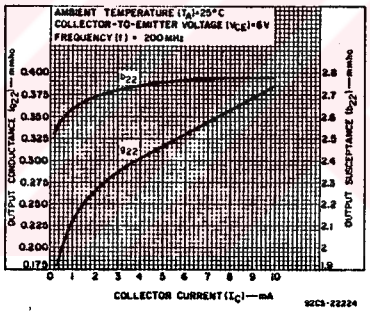


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

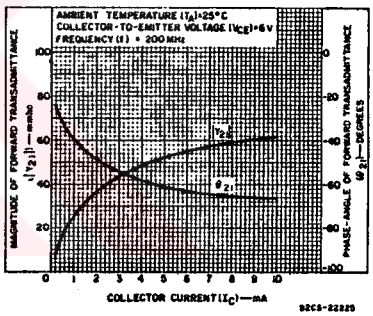


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

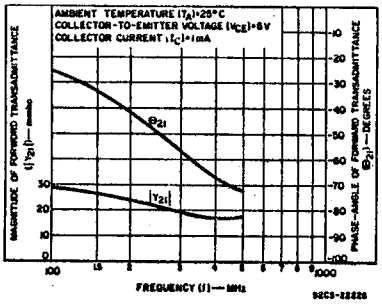


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

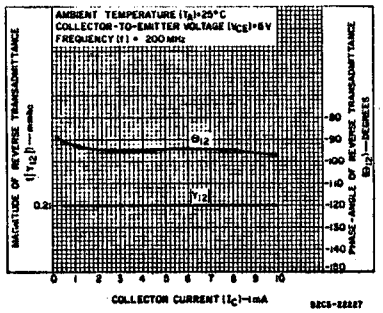


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

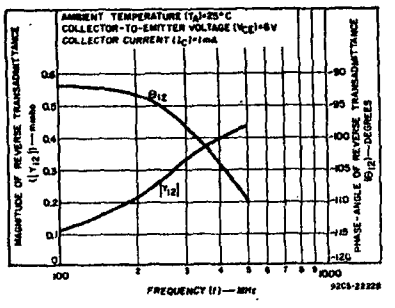


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

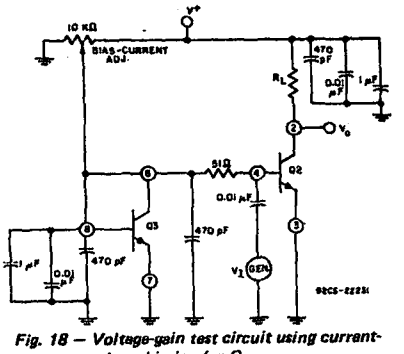
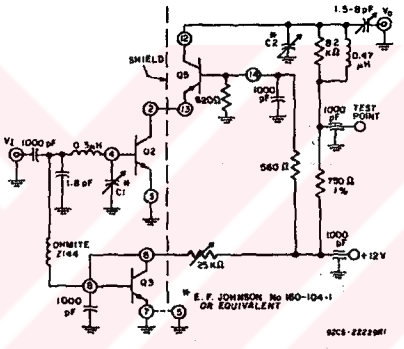


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

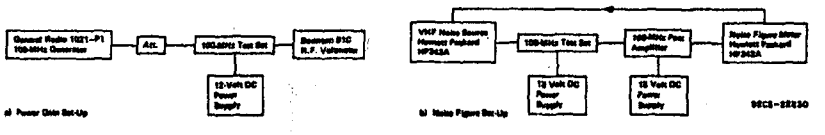


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

ESCRIPTION

e 82S16/116 and 82S17/117 are read/te memory arrays which feature either en collector or tri-state output options for imization of word expansion in bused anizations. Memory expansion is further anced by full on-chip address decoding, hip enable inputs and pnp input transis-s which reduce input loading to 25μA for igh level, and −100μA for a low level.

ring Write operation, the logical state of output of both devices follows the com-ment of the data input being written. This ture allows faster execution of Write-ad cycles, enhancing the performance of stems utilizing indirect addressing des, and/or requiring immediate verifi-ion following a Write cycle.

th devices have fast read access and te cycle times, and thus are ideally suited igh-speed memory applications such as che, buffers, scratch pads, writable con-l stores, etc.

devices are available in the commercial nperature range (0°C to +75°C) and are ecified as N82S16/116/17/117, F or N. e 82S16 and 82S17 are also available in military temperature range (−55°C to 25°C) and are specified as S82S16/17.

EATURES

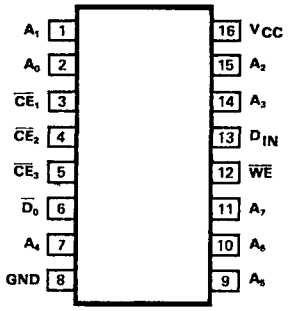
Address access time:
82S116/117: 40ns max
Write cycle time:
82S116/117: 25ns max
Power dissipation: 1.5mW/bit typ
Input loading:
N82S116/117: −100μA
Output follows complement of data input during Write
On-chip address decoding
Output option:
82S16/116: Tri-state
82S17/117: Open collector
Schottky clamped
TTL compatible

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

F,N PACKAGE*



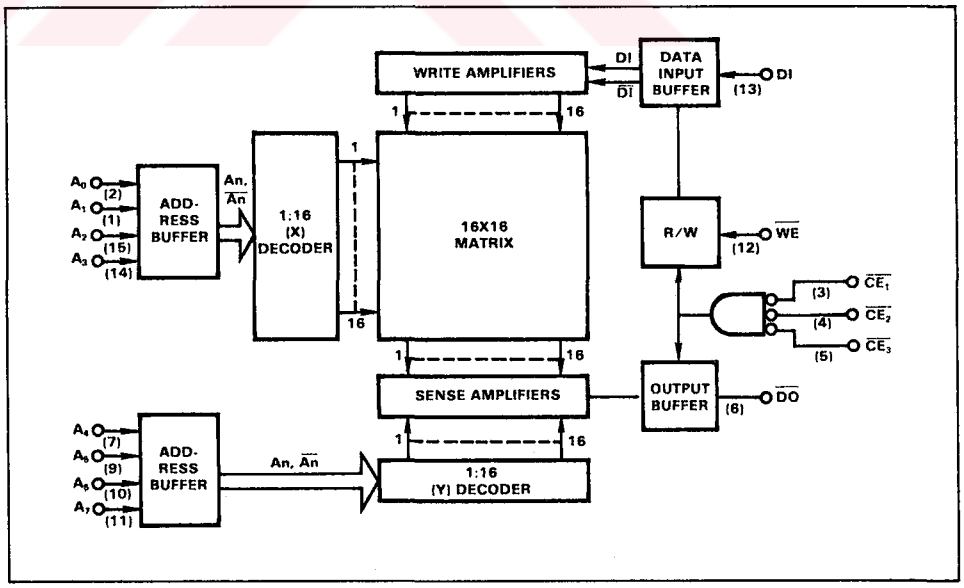
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_{OUT}	High (82S17)		
V_O	Off-state (82S16)		
	Temperature range		°C
T_A	Operating		
	S82S16/17	−55 to + 125	
	N82S16/17, N82S116/117	0 to +75	
T_{STG}	Storage	−65 to +150	

ELECTRICAL CHARACTERISTICS

N82S116/117, N82S16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S16/17: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S16/17/116/117			S82S16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage[2]	V_{CC}= Min							V
V_{OH}	High (82S16/116)[4]	I_{OH} = −3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = Max							mA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−250	
	Output current								
I_{OLK}	Leakage (82S17/117)[6]	V_{OUT} = 5.5V		1	40		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S16/116)[6]	V_{OUT} = 5.5V		1	40		1	50	μA
		V_{OUT} = 0.45V		−1	−40		−1	−50	
I_{OS}	Short-circuit (82S16/116)[7]	V_{CC} = Max, V_O = 0V	−20		−70	−20		−70	μA
I_{CC}	V_{CC} supply current	V_{CC} = Max		80	115		80	120	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

ECTRICAL CHARACTERISTICS

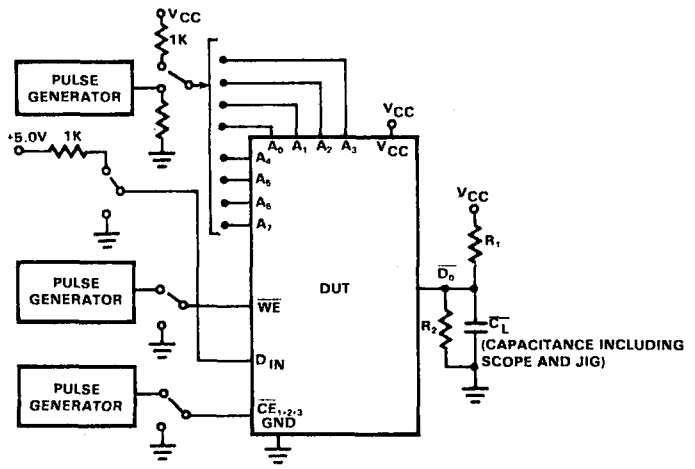
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S116/117, N82S16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S16/17			N82S116/117			S82S16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max	
Access time												ns
Address				40	50		30	40		40	70	
Chip enable				30	40		15	25		30	40	
Disable time	Output	Chip enable		30	40		15	25		30	40	ns
Valid time	Output	Write enable		30	40		30	40		30	55	ns
Setup and hold time												ns
Setup time	Write enable	Address	20	5		0	-5		20	5		
Hold time			5	0		0	-5		10	0		
Setup time	Write enable	Data in	40	30		25	15		50	40		
Hold time			5	0		0	-5		10	0		
Setup time	Write enable	$\overline{CE}$	10	0		0	-5		10	0		
Hold time			5	0		0	-5		10	0		
Pulse width												ns
Write enable[8]			30	15		25	15		40	20		

cal values are at V_{CC} = 5V, T_A +25°C.
age values are with respect to network ground terminal.
ich input one at the time.
ed with a logic low stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
ed with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
ed with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
on of the short-circuit should not exceed 1 second.
neasured with the write enable and memory enable inputs grounded, all other inputs at 4.5V.
e output open.
um required to guarantee a Write into the slowest bit.

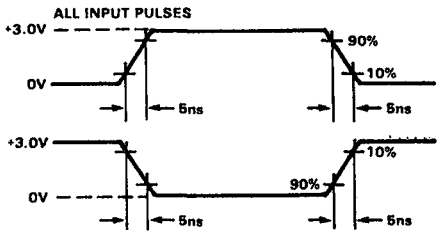
LOAD CIRCUIT

LOADING CONDITION



VOLTAGE WAVEFORM

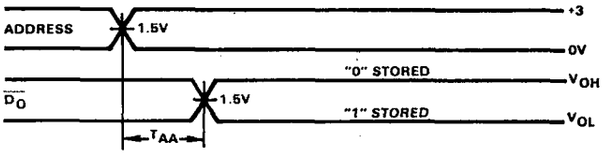
INPUT PULSES



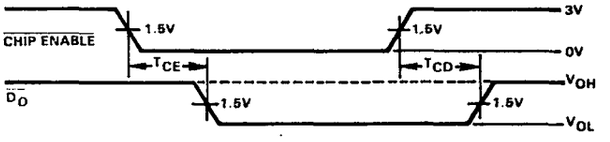
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

'IMING DIAGRAMS

READ CYCLE

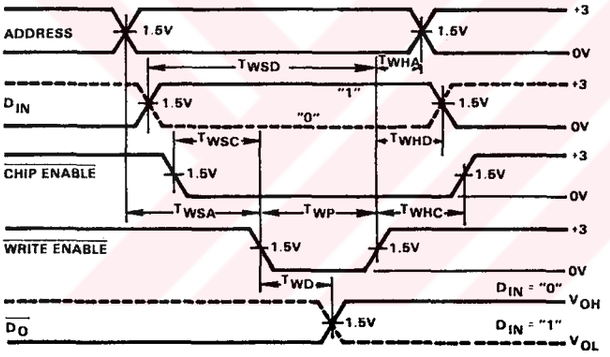


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state.

T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

APPENDIX F

COMPANDING AMPLIFIER SIMULATION PROGRAM

```
echo off:
clear;
clc;
ik=input('Ik (mA)=  ');
re=input('RE=  ');
a=input('a=  ');
b=input('b=  ');
g=2;
x1=ik/2:(ik/2)/255:2*.9999;
n=size(x1);
for j=1:n(2);
l(j)=j;
i=x1(j);
v1(j)=26e-3*log(i/(ik-i))+re*1e-3*(2*i-ik);
x2(j)=ik/2+a*log(1+b*v1(j)/.026);
y1(j)=-(x1(j)-ik*.5)*g;
y2(j)=-(x2(j)-ik*.5)*g;
end;
plot(v1,x1,v1,x2);
xlabel('input,Volts');
ylabel('coll. current,mA');
title('collector current vs. i/p. voltage');
grid;
pause;
plot(v1,y1,v1,y2);
title('ADC i/p signal vs. input signal');
xlabel('input, Volts');
ylabel('ADC i/p, Volts');
grid;
pause;
pause;
clc;
c=input('continue iteration ? (1/0)');
if c<1,clc,break,end;
else if c=1
tez;
end.
```

APPENDIX G

CIRCUIT DIAGRAMS

Complete circuit diagrams of all units are given in the text wherever mentioned. The circuit diagram of power supply board is merely given here.

Power supplies employed in the system are named as V_1^+, V_1^-, V_2^+, V_3^+ and V_3^-:

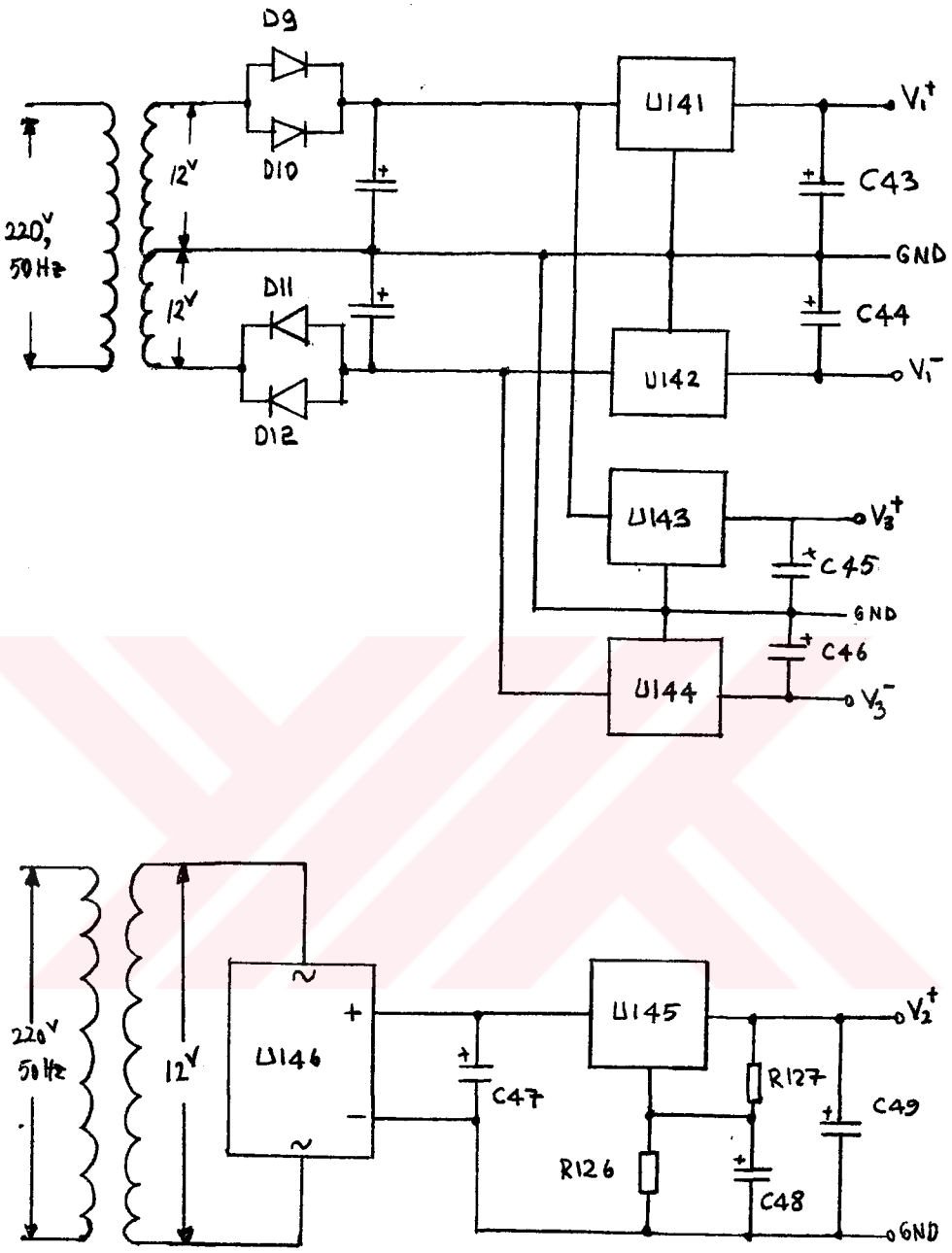
V_1^+ : +5V, 1.5A for analog parts,

V_1^- : -5V, 1.5A for analog parts,

V_2^+ : +5V, 3A for digital parts,

V_3^+ : +12V, 1.5A for analog parts,

V_3^- : -12V, 1.5A for analog parts.



POWER SUPPLY

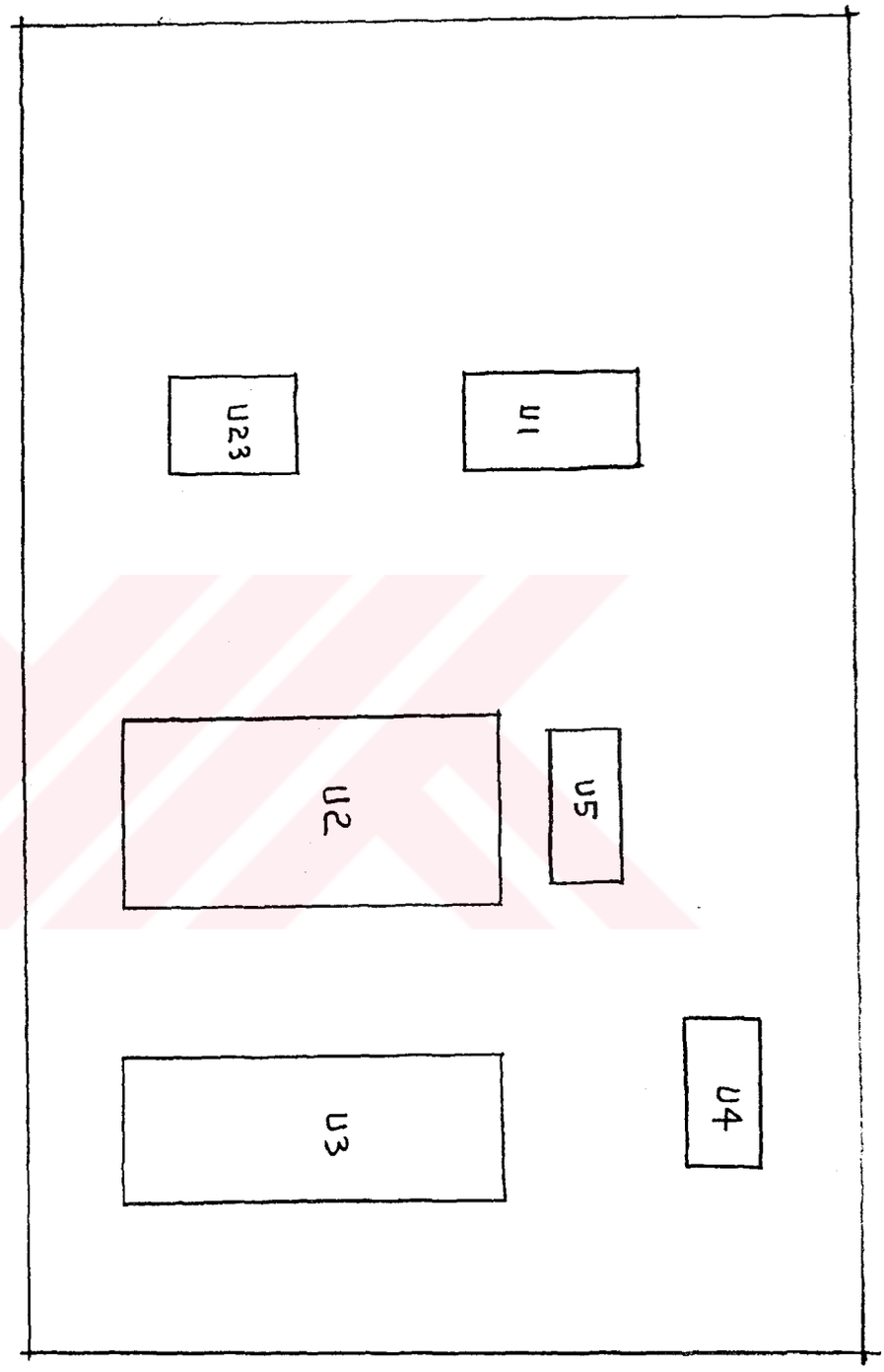
APPENDIX H

LAYOUTS

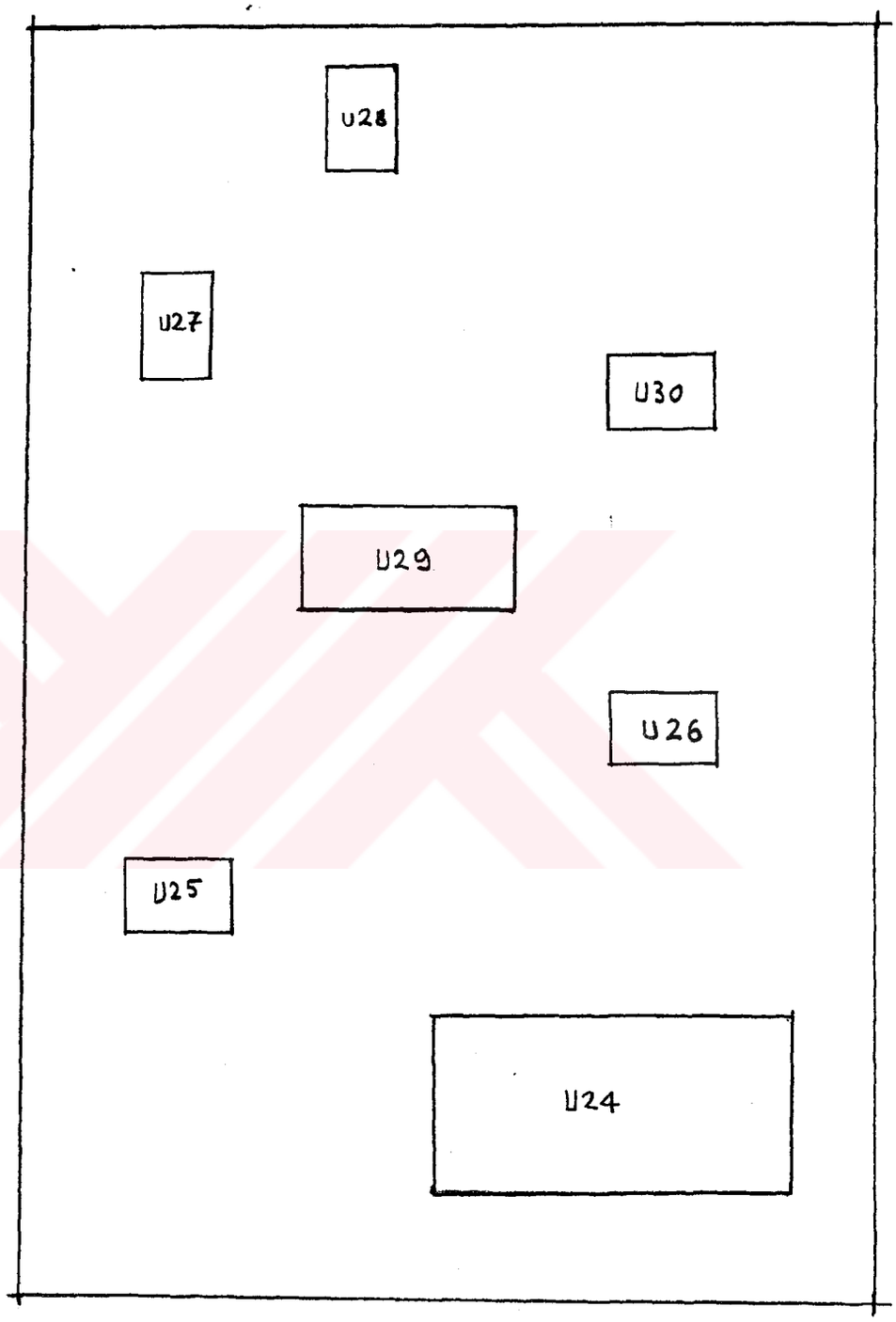
Layouts of all boards are given in the order of appearance.

The resistors and capacitors are not shown, only the Integrated circuits are given.

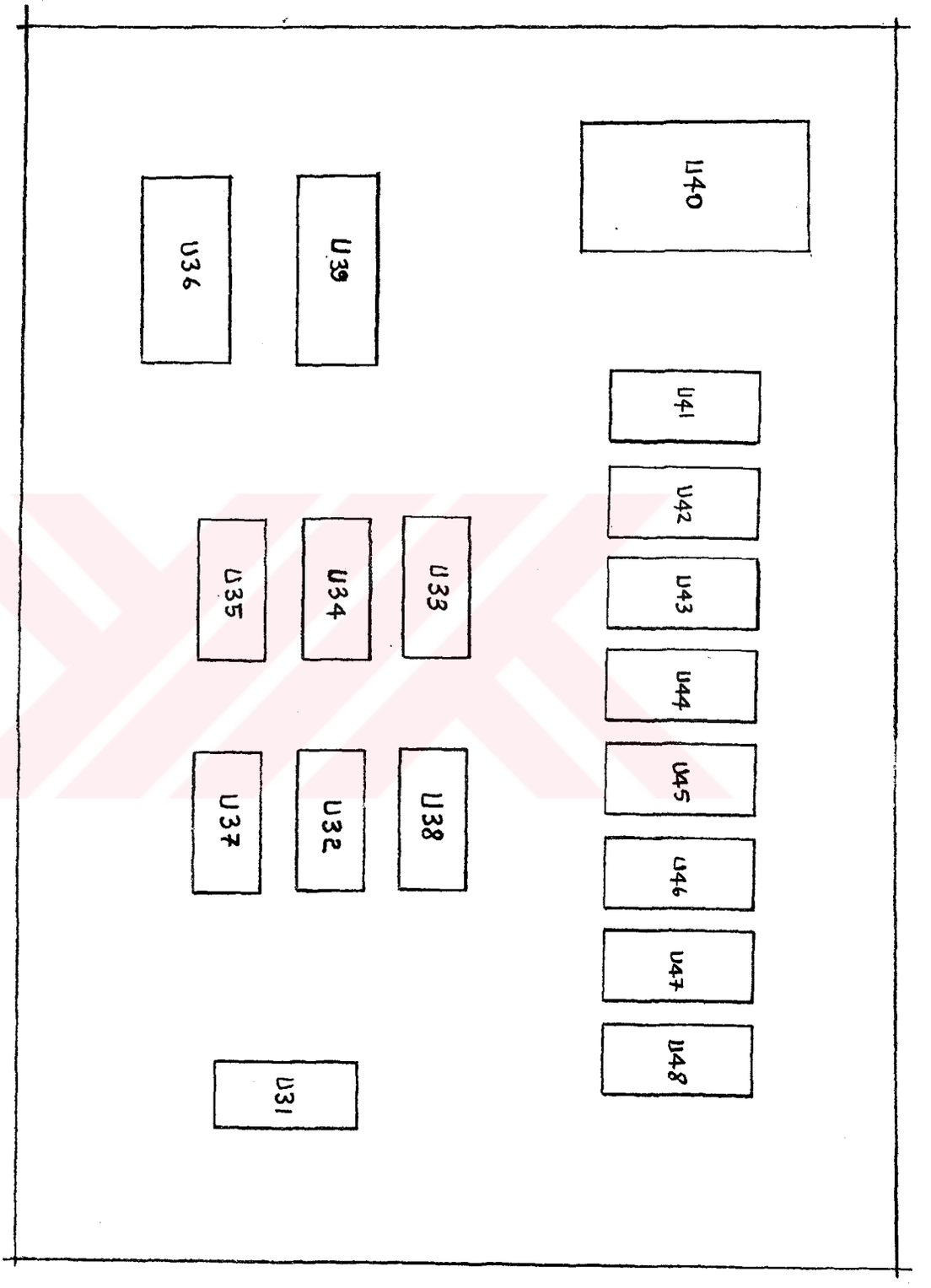
ADC board layout



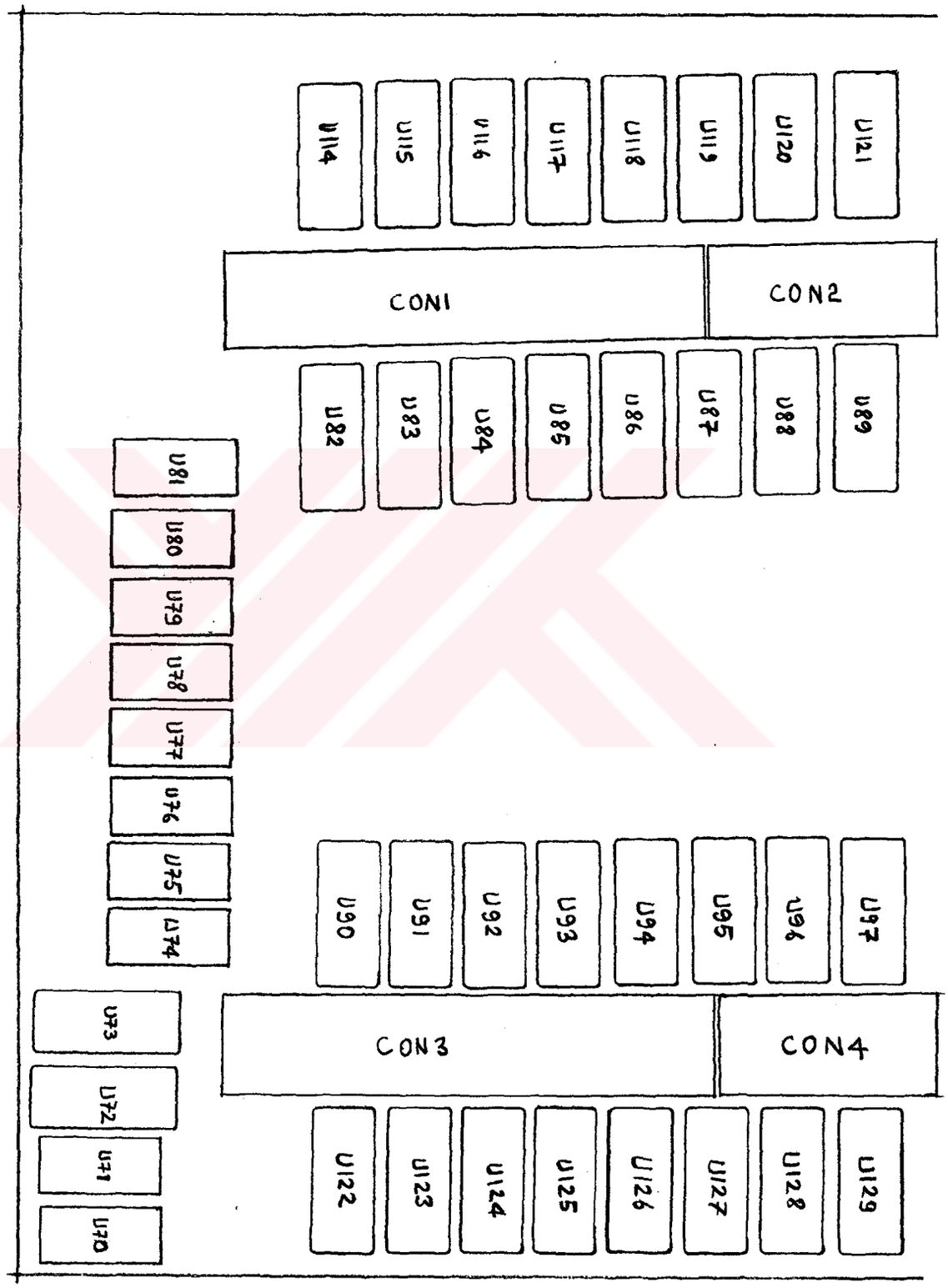
Composite video signal generator board layout



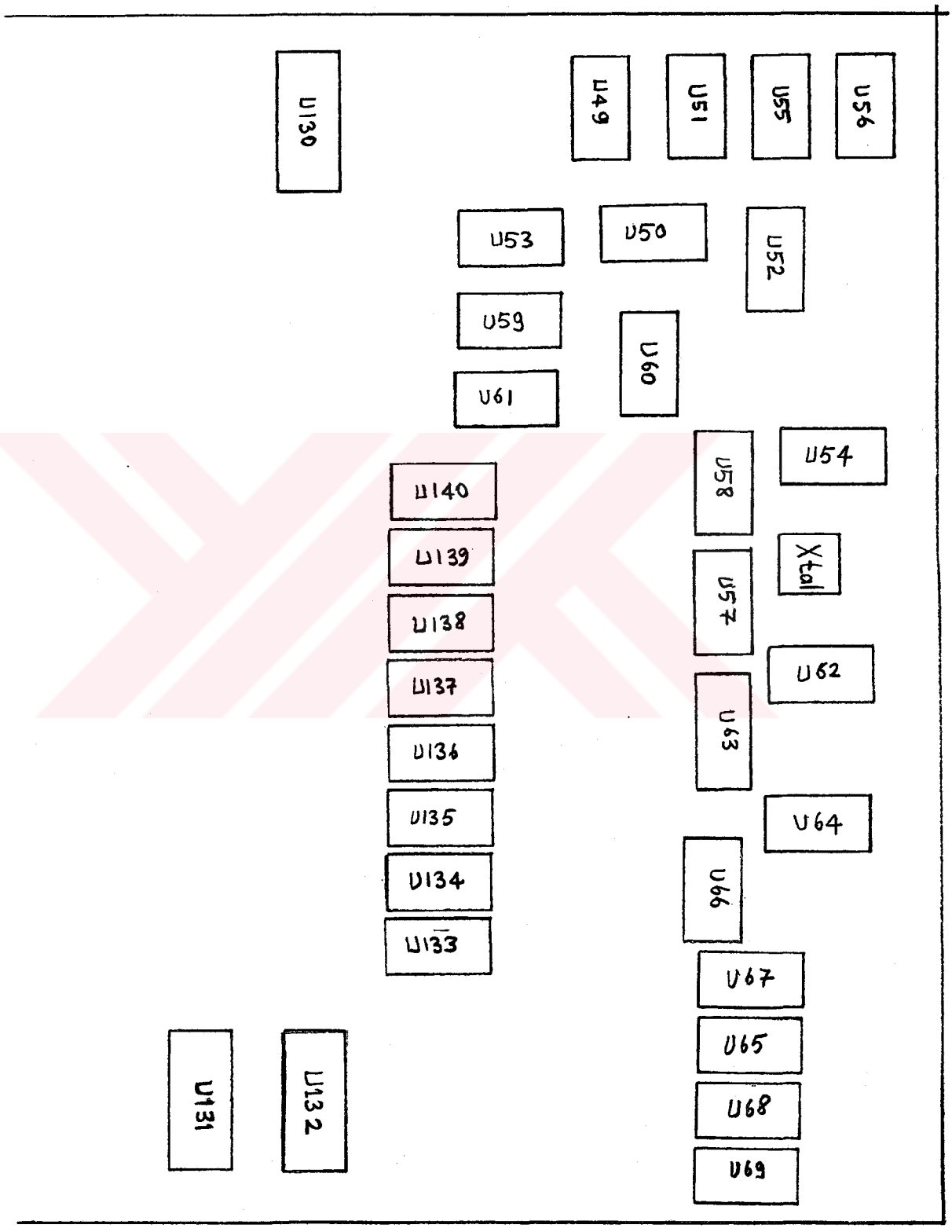
LUT board layout



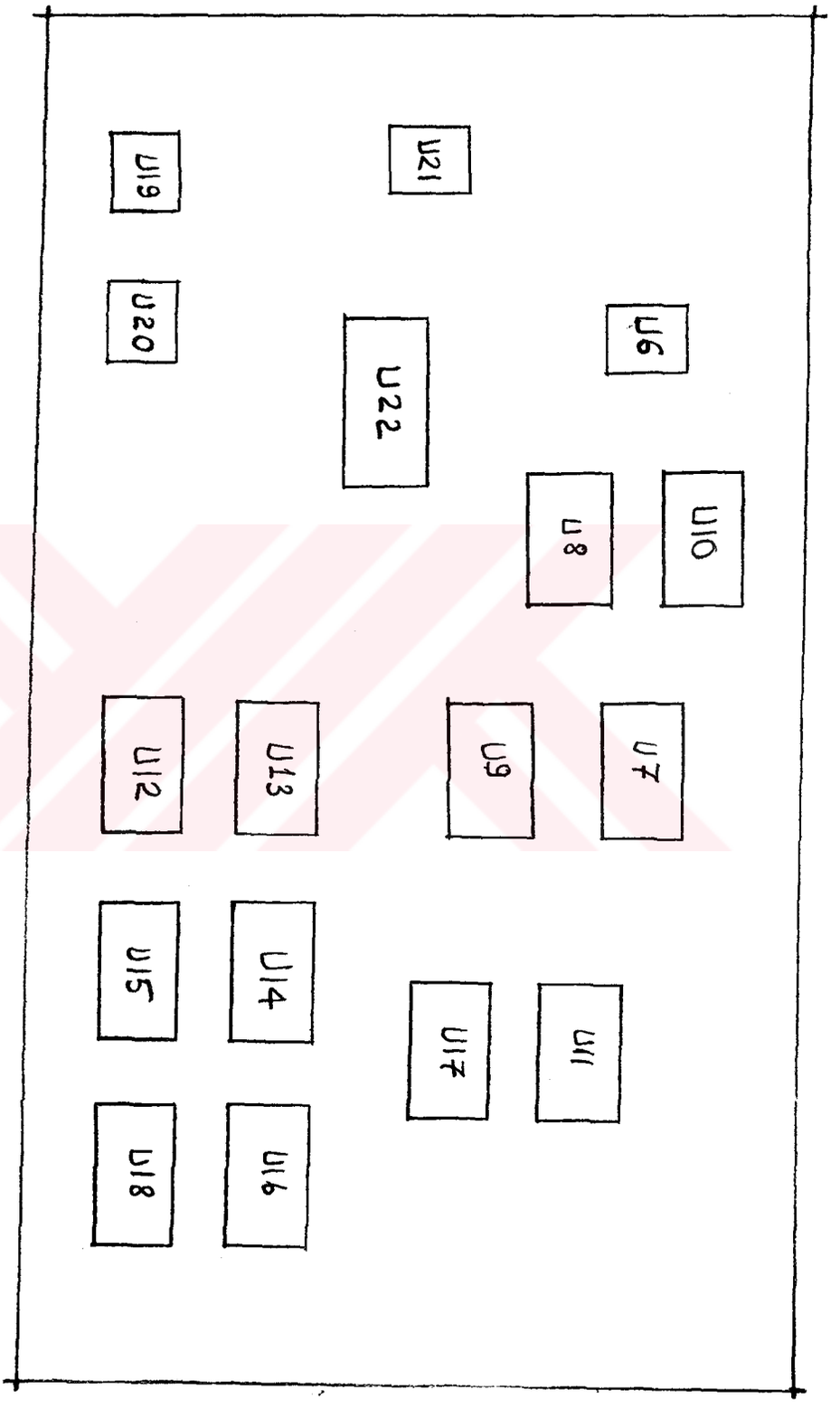
Data acquisition board layout



Data acquisition board layout (continued)



Video signal and kVp control board layout



APPENDIX I

PART LISTS

Lists of components employed to implement the system are given in this part.

I.1. Companding Amplifier Board Part List.

Symbol	Type	Description
T1,T2,T3,T4	all in CA3127	High-Frequency NPN Transistor Array
R1	820 ohms	.25W,carbon resistor
R2,R4,R7	10K	.25W,multiturn trimpot
R5	1 ohm	.25W,carbon resistor
R6	82 ohms	.25W,carbon resistor
R8	75 ohms	.25W,carbon resistor

I.2. ADC Board Part List.

Symbol	Type	Description
U1	LM359	Dual, High speed, Programmable Current Mode(Norton) Amplifiers
U2	TDC-1048	20 MSPS Flash ADC
U3	74LS374	Octal D Flip-Flop, 3-State
U4,U5	LM337	3-term.adjustable volt. regulator
U23	LF351	Wideband JFET input OPAMP
D1,D2	1N4148	Silicon Switching Diode
R69	4K7	.25W,trimpot
R70	1K	.25W,carbon resistor
R71	680	.25W,carbon resistor
R72	33K	.25W,carbon resistor
R9	820 ohms	.25W,carbon resistor
R10	8K2	.25W,carbon resistor
R11,R12	20K	.5W,carbon resistor
R13,R14, R25-R32	33 ohms	.25W,carbon resistor
R16	1K5	.25W,carbon resistor
R17-R24	2K2	.25W,carbon resistor
C1	.010µF	50V,ceramic capacitor
C2	100µF	16V,electrolytic capacitor
C3	4p7F	63V,ceramic capacitor
C4,C5,C8, C11,C24	.1µF	50V,ceramic capacitor
C6,C7,C9, C10,C12,C13	10µF	16V,electrolytic capacitor

I.3. Composite Video Signal Generation Board Part List

Symbol	Type	Description
U24	TDC-1016	20 MSPS 10-bit DAC
U25	LF351	Wideband JFET input OPAMP
U26,U30	LM318	Wideband OPAMP
U27,U28	LF356	Monolithic JFET input OPAMP
U29	4053	Triple 2-channel analog MUX.
D4-D8	1N4148	silicon switching diode
R84,R115	50K	.25W,multiturn trimpot
R89,R91,R107	10K	.25W,multiturn trimpot
R73-R82,R118	2K2	.25W,carbon resistor
R83,R85		
R101,R102	22K	.25W,carbon resistor
R86,R103,R106		
R116	12K	.25W,carbon resistor
R87,R90	100ohms	.25W,carbon resistor
R92,R108	150ohms	.25W,carbon resistor
R109.R112	10K	.25W,carbon resistor
R97,R98	27K	.25W,carbon resistor
R99	4K7	.25W,trimpot
R88,R117	68ohms	.25W,carbon resistor
R96,R100	1K	.25W carbon resistor
R110	39K	.25W carbon resistor
R111	6K8	.25W carbon resistor
R104	100K	.25W carbon resistor
R95	3K	.25W carbon resistor
R93	2K5	.25W carbon resistor
R94	5K1	.25W carbon resistor
R105	20ohms	.25W carbon resistor
C25,C27,C30		
C31,C32,C33		
C34	.1µF	50V,ceramic capacitor
C28	.015µF	63V,ceramic capacitor
C35	5p6F	63V,ceramic capacitor
C26	22µF	16V,solid tantal. cap.

I.4. LUT Board Part List

Symbol	Type	Description
U31-U33	74LS74	Dual D-type flip-flop
U34,U35	74LS161	Synch. 4-bit binary counter
U36,U39	74LS244	Octal buffer, 3-St.
U37	7400	Quad 2-input NAND gate
U38	74LS08	Quad 2-input AND gate
U40	2716	2K, 8-bit EPROM
U41-U48	82S16	256-bit bipolar RAM, 256x1
D9	1N4148	silicon switching diode
R120	62K	.25W,carbon resistor
R121	180K	.25W,carbon resistor
R119	1K5	.25W,carbon resistor
C36	1000µF	16V,electrolytic capacitor

I.5. Data Acquisition Board Part List

Symbol	Type	Description
U70,U71	74LS283	4-bit full adder with fast carry
U72	74LS240	Octal inverter buffer, 3-St.
U73	74LS244	Octal buffer, 3-St.
U74-U81	74LS164	4-bit ser.-in par.-out shift reg
U114-U129, U133-U140	74LS374	Octal D-flip-flop, 3-St.
U130-U132	74LS244	Octal buffer, 3-St.
U98-U113	HM62256	32768-word X 8-bit high speed static CMOS RAM

I.6. Video Signal Control Board Part List

Symbol	Type	Description
U6	LF356	
U7,U9,U12	74LS123	Dual retriggerable monostable multivibrator
U8,U11,U16	74LS74	Dual D-type flip-flop
U14,U15	74LS161	Synch. 4-bit binary counter
U10	74LS08	Quad 2-input AND gate
U13,U17	74LS76	Dual J-K flip-flop
U18	74LS125	Quad 3-state buffers
T5	BC237	NPN silicon transistor
D3	1N4148	Silicon switching diode
R37,R38,R40	39K	.25W,carbon resistor
R39	2K2	.25W,carbon resistor
R41	82ohms	.25W,carbon resistor
R42,R48	1K	.25W,carbon resistor
R43	1K5	.25W,carbon resistor
R44,R45	10K	.25W,carbon resistor
R46	2K2	.25W,carbon resistor
R47,R50	5K1	.25W,carbon resistor
R49	12K	.25W,carbon resistor
R51	200K	.25W,multiturn trimpot
C14,C15	.015	50V,ceramic capacitor
C16	.2µF	50V,porcelain capacitor
C17	.1µF	50V,ceramic capacitor
C18	.033µF	50V,ceramic capacitor
C19	.47µF	50V,ceramic capacitor

I.7. X-Ray Generator Control Board Part List

Symbol	Type	Description
U19,U20	LM741	General purpose OPAMP
U21	LF356	Monolithic JFET input OPAMP
U22	4053	Triple 2-channel Analog MUX.
R53,R56	100K	.25W,linear potentiometer
R54,R57	2K2	.25W,linear potentiometer
R64	2K2	.25W,trimpot
R52,R55,R58		
R59,R61	12K	.25W,carbon resistor
R60,R65,R66	1K	.25W,carbon resistor
R62	2K2	.25W,carbon resistor
R63	15K	.25W,carbon resistor
R67	470ohms	.25W,carbon resistor
R68	220ohms	.25W,carbon resistor
C20,C22	.15µF	50V,ceramic capacitor
C21,C23	.0082	50V,ceramic capacitor

I.8. Real-Time Read Control and Clock Generation Board

Part List

Symbol	Type	Description
U62	74LS04	Hex inverter
U63	74LS244	Octal buffer,3-St.
U64,U65	74S161	Synch.4-bit binary counter
U66	74LS00	Quad 2-input NAND Gates
U67	74F112	Dual J-K flip-flop
U68-U69	74S138	1-of-8 decoder/demultiplexer
Xtal		15.000 MHz. crystal oscillator
R69,R70	10K	.25W,multiturn trimpot
C23	.1µF	50V,ceramic capacitor
C24	12pF	68V,ceramic capacitor

I.9. Memory Read/Write Control Board Part List

Symbol	Type	Description
U49,U54	74LS123	Dual retriggerable monostable multivibrator
U50,U58	74LS08	Quad 2-input AND gate
U51,U53	74LS74	Dual D-type flip-flop
U52	74LS76	Dual J-K flip-flop
U57	74LS00	Quad 2-input NAND gate
U59	74LS11	Triple three-input AND gate
U60	74LS10	Triple three-input NAND gate
U61	74LS32	Quad 2-input OR gate
R122	50K	.25W,multiturn trimpot
R123-R125	10K	.25W,carbon resistor
C37	.0056µF	50V,ceramic capacitor
C38,C39	330pF	50V,ceramic capacitor
C40	1p5F	50V,ceramic capacitor

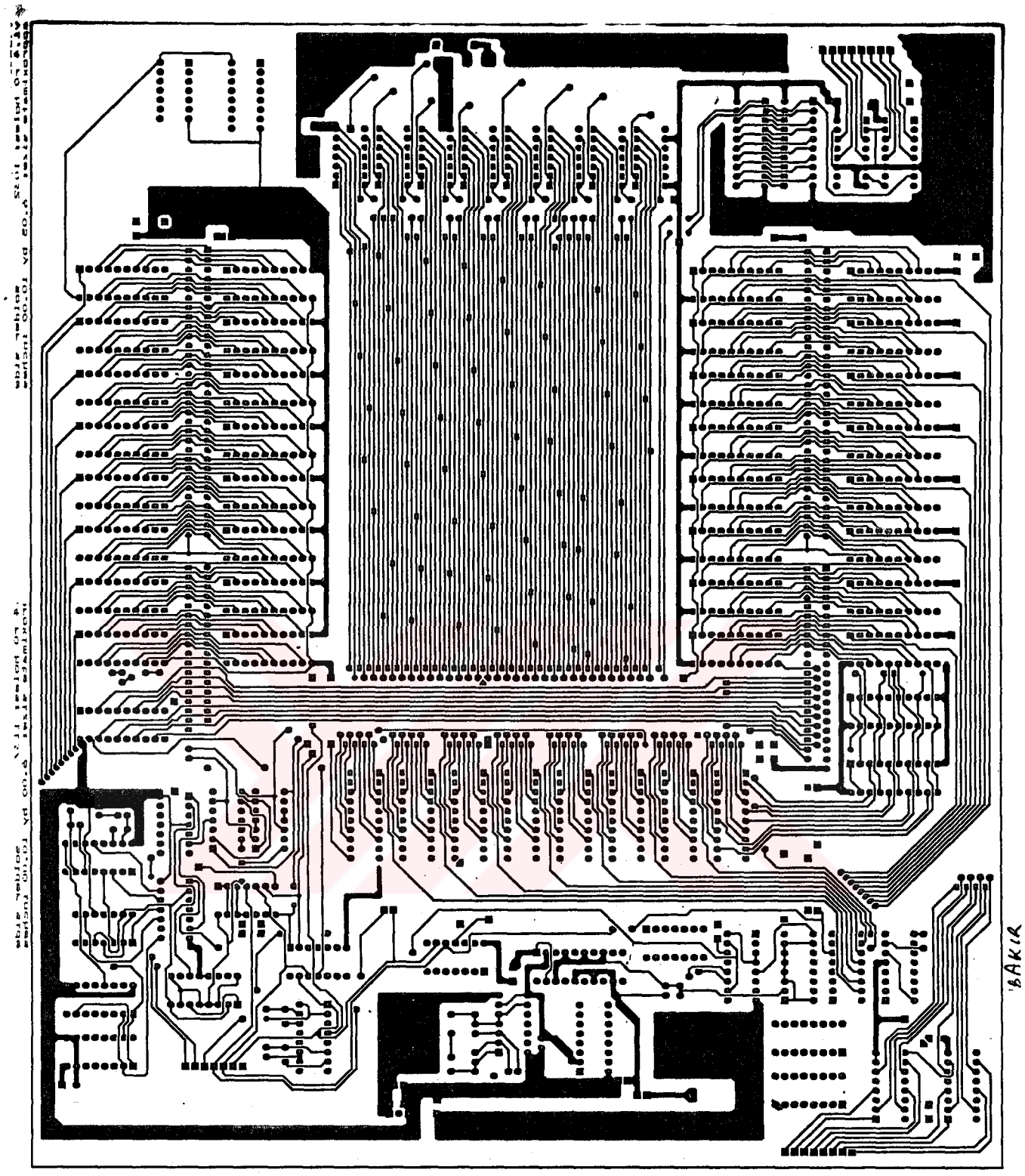
I.10. Power Supply Board Part List

Symbol	Type	Description
U141	LM7805	+5V, 3-terminal voltage regulator
U142	LM7905	-5V, 3-terminal voltage regulator
U143	LM7812	+5V, 3-terminal voltage regulator
U144	LM7912	-5V, 3-terminal voltage regulator
U145	LM350	3-term. adjustable volt.regulator
U146	B80C3200	bridge diode
D9-D12	1N4001	PN junction silicon diode
R126	820 ohms	.25W, carbon resistor
R127	220 ohms	.25W, carbon resistor
C41,C42, C47	4700µF	25V,elctrol+ytic capacitor
C43-C46	10µF	16V,electrolytic capacitor
C48,C49	10µF	16V,electrolytic capacitor

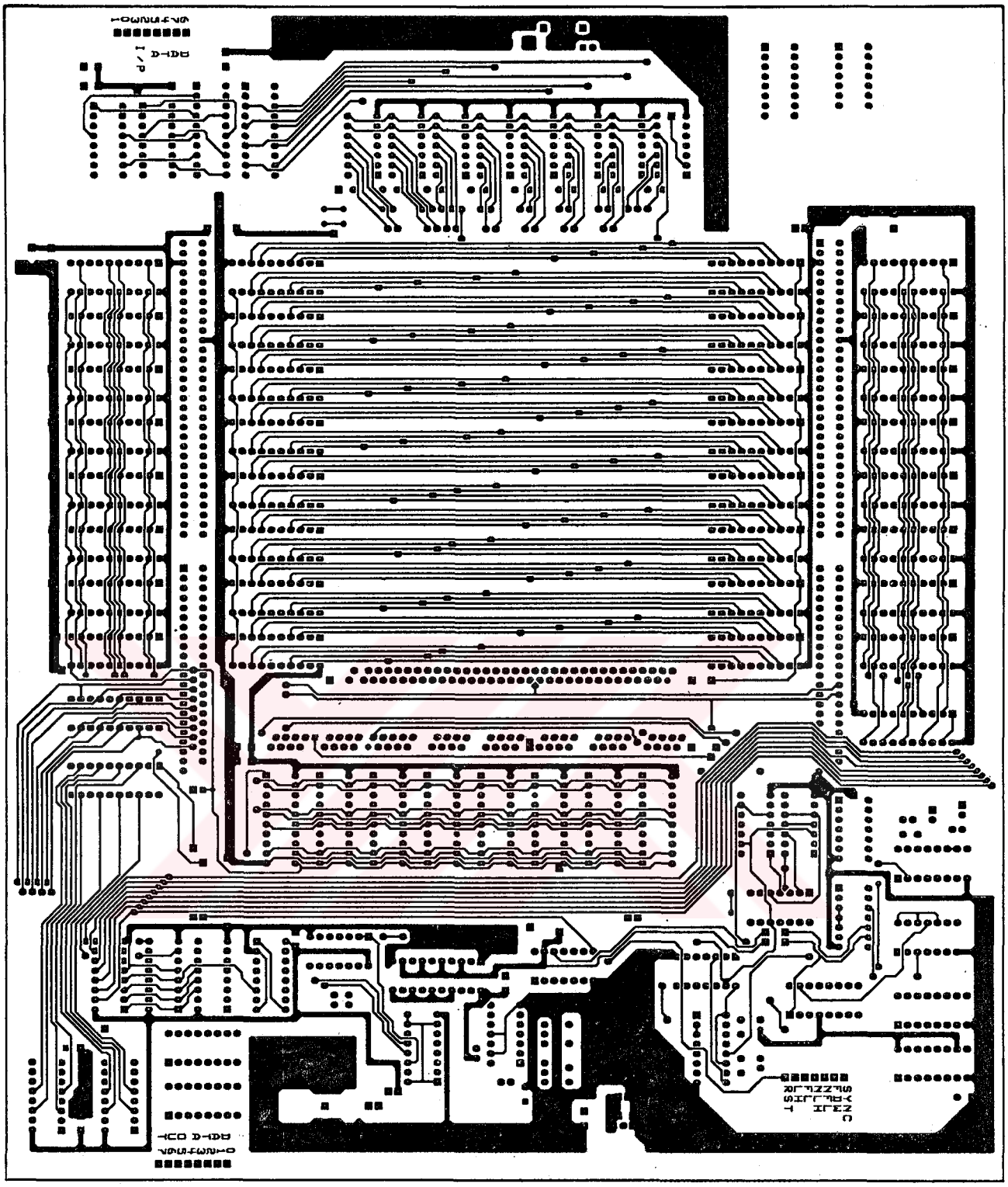
APPENDIX J

FILMS OF PRINTED CIRCUIT BOARDS

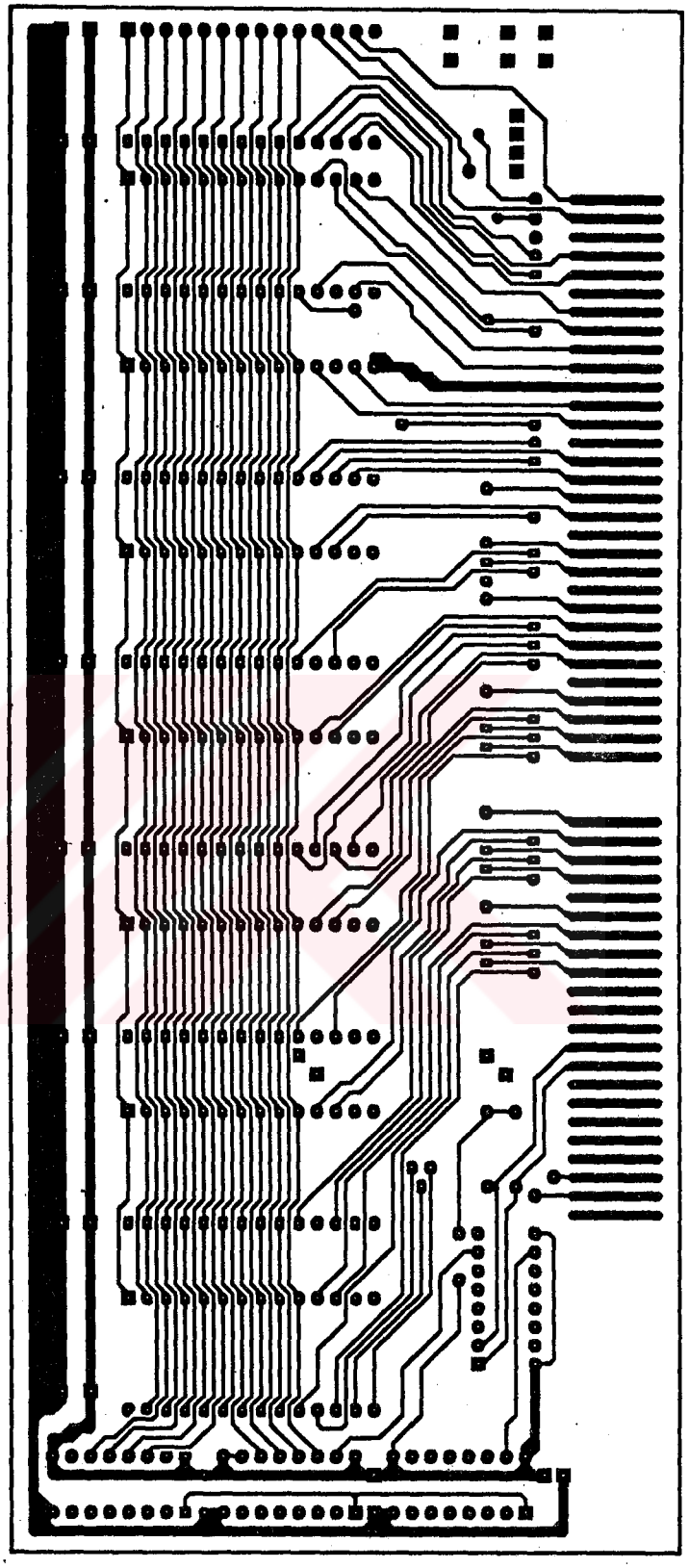
Most of the circuits are constructed on WIRE-WRAP cards. The rest(Companding amplifier, LUT, Memory Array and Data Acquisition) are realized on PCBs. These are given in the following pages.



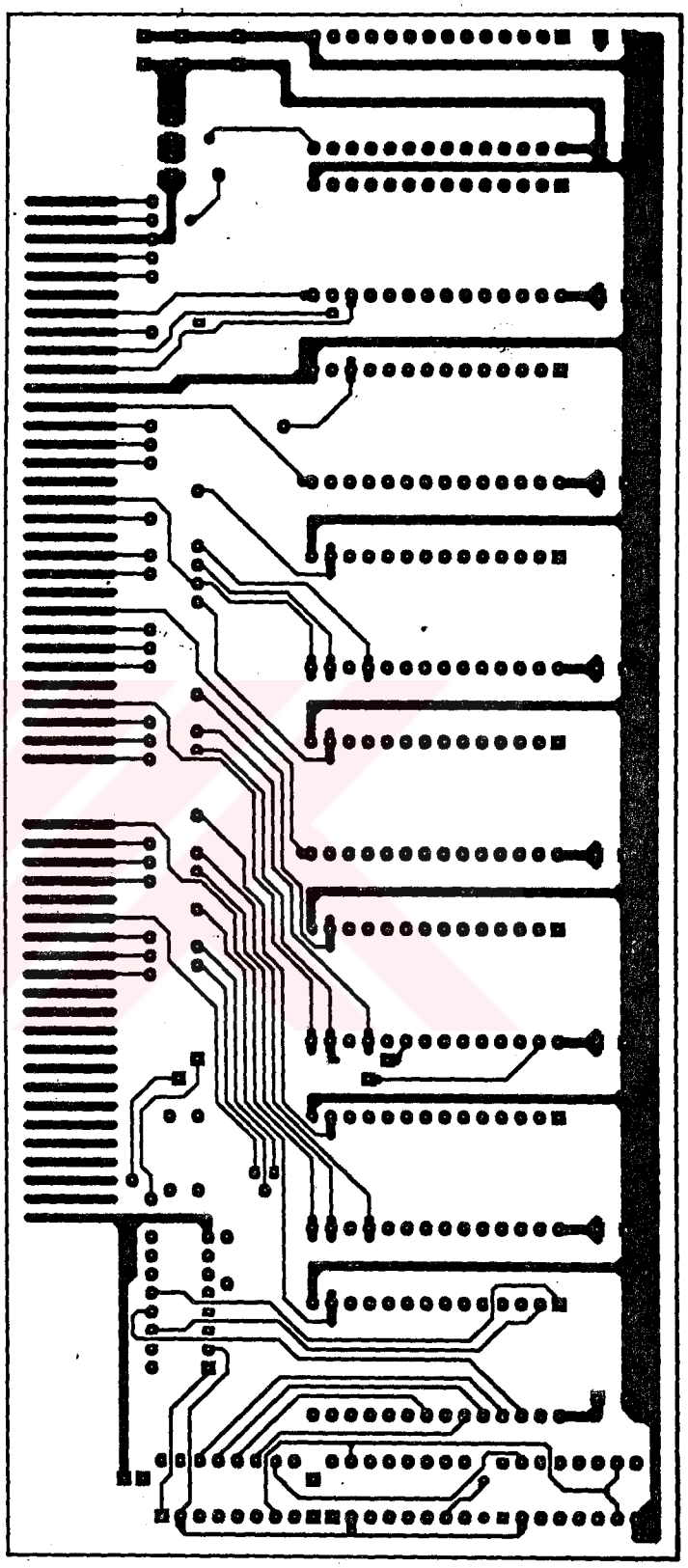
Solder side of Data Acquisition Board, Scale factor=0.647



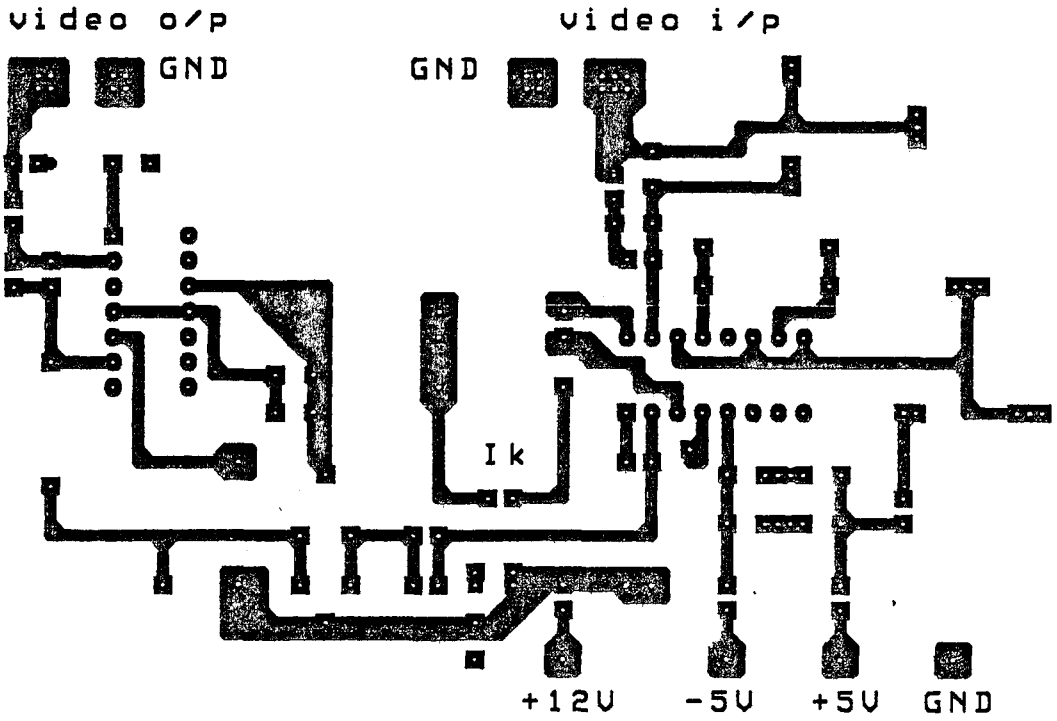
Component side of Data Acquisition Board, Scale factor=0.647



Solder side of Memory Array Board, Scale factor=1

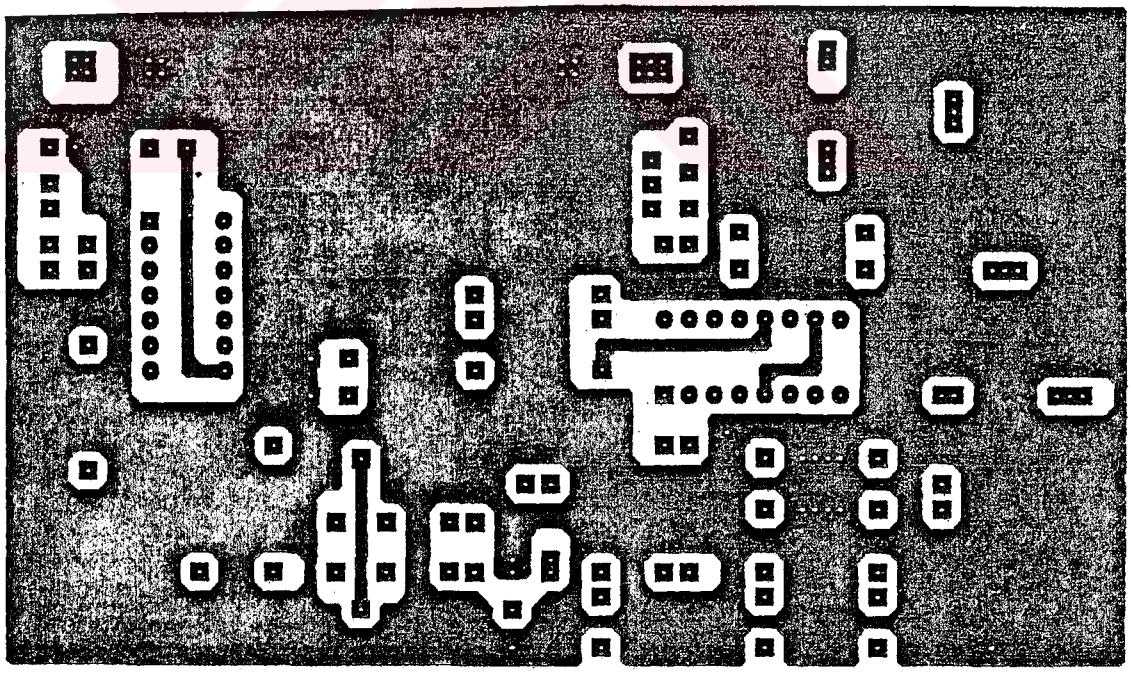


Component side of Memory Array Board, Scale factor=1



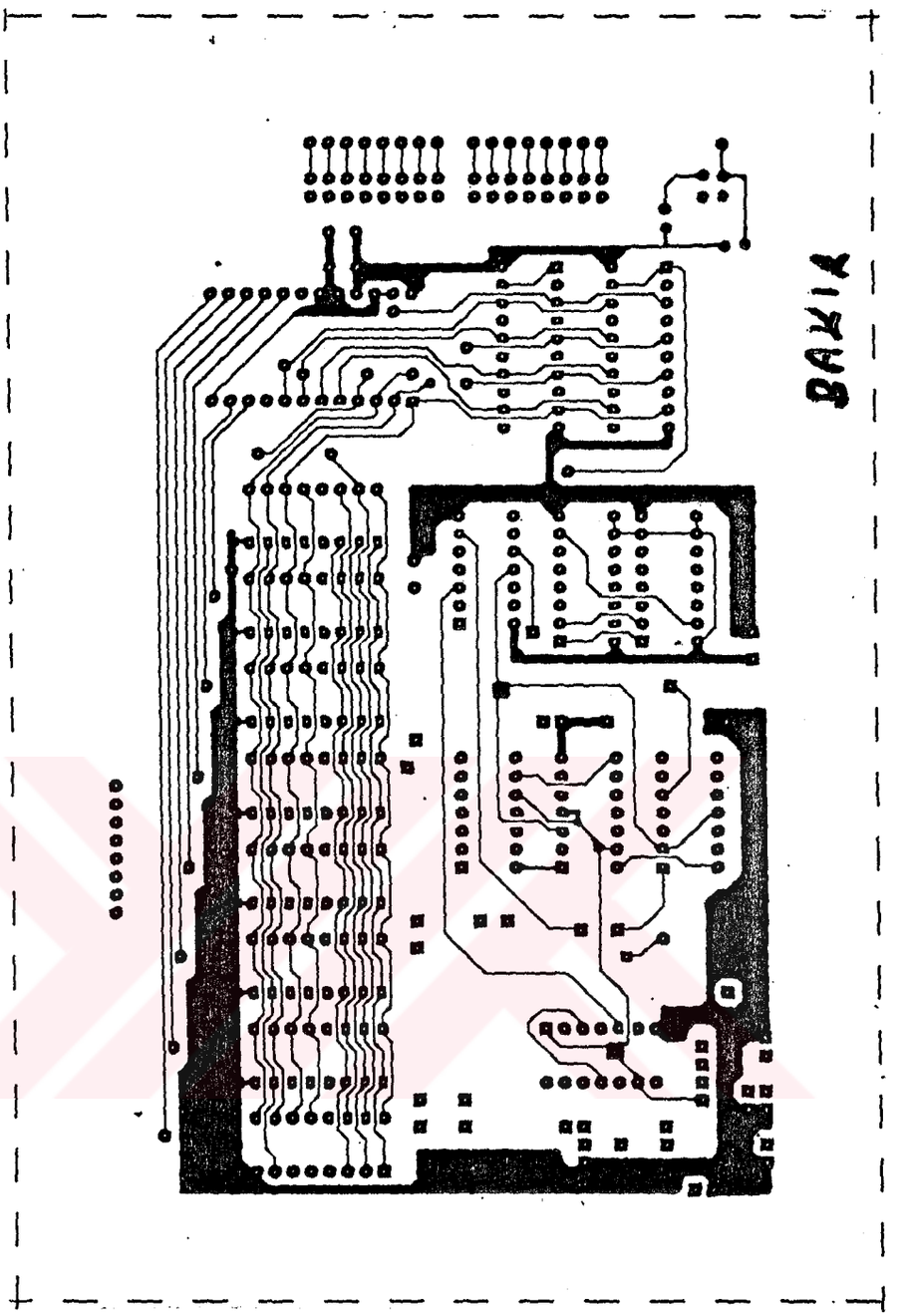
Companding amplifier and ADC input buffer, component side.

scale factor=1.294

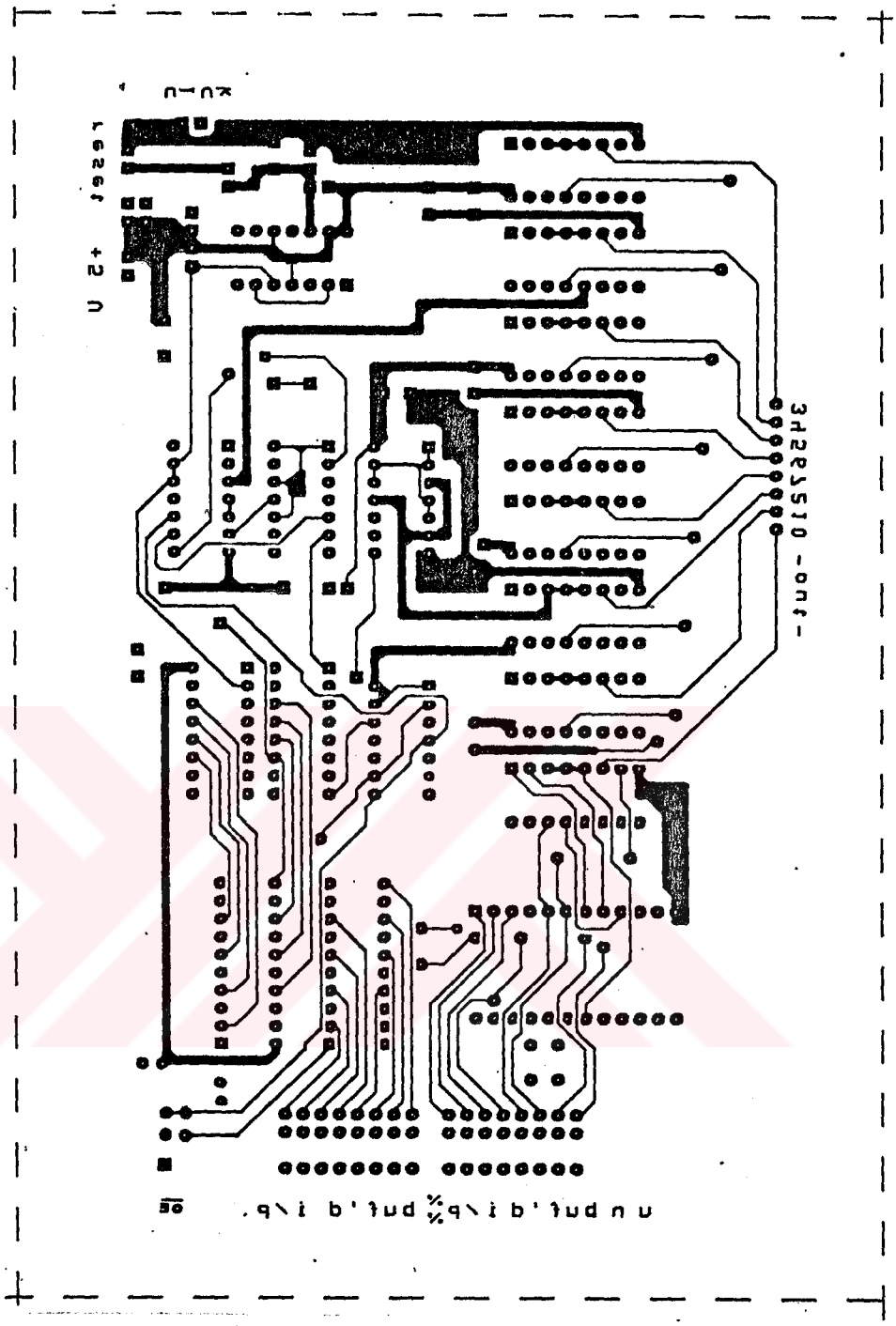


Companding amplifier and ADC input buffer, solder side.

scale factor=1.294



Solder Side of LUT Board Scale Factor = 1



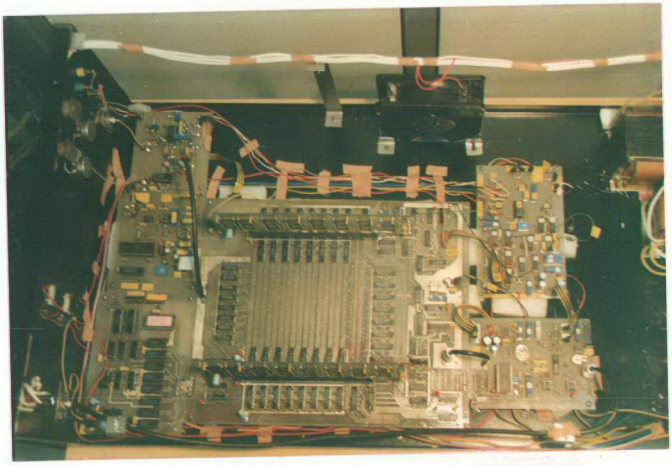
Component Side of LUT Board Scale Factor = 1

APPENDIX K

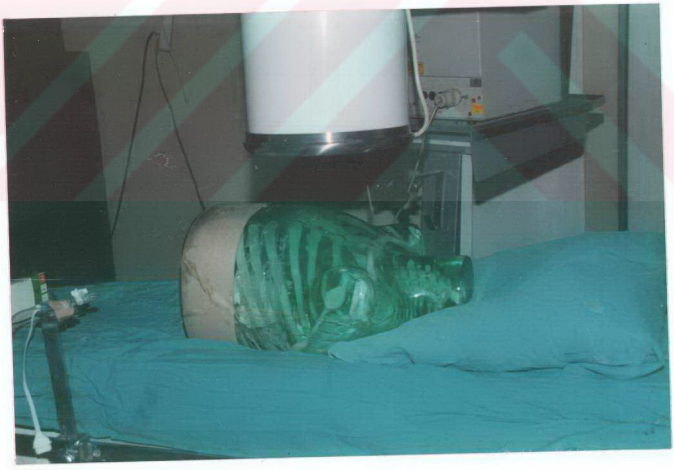
PHOTOGRAPHS OF THE SUBSYSTEM

Photographs of the developed hardware and the images which are obtained by this system are presented in this section.

Front panel of K-Edge Imaging System

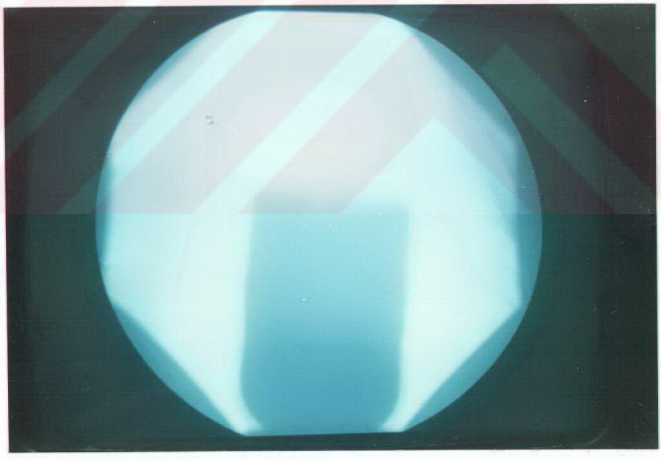


Inside of the K-Edge Imaging System

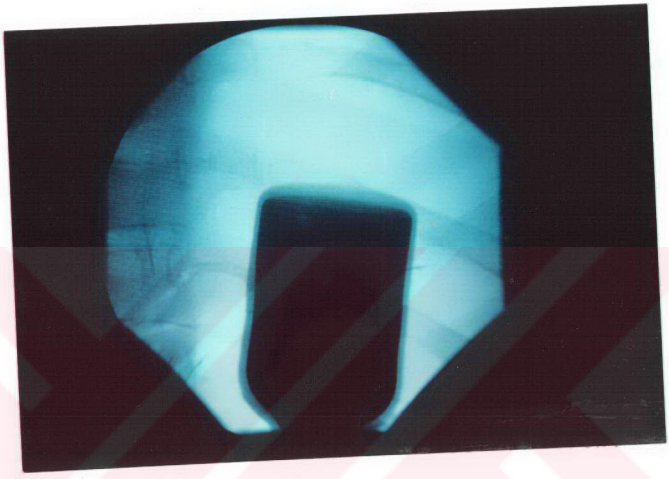


Thorax Phantom and TV camera

Thorax Phantom and radio-opaque material



Subtracted Image of Thorax Phantom and radio-opaque material



Normal X-Ray Fluoroscopy Image of Thorax Phantom and radio-opaque material