IMPROVED CONTACT RESISTIVITY METHODS BASED ON COX-STRACK AND 4 POINT PROBE

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ABSTRACT

IMPROVED CONTACT RESISTIVITY METHODS BASED ON COX-STRACK AND 4 POINT PROBE

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Contact resistivity (ρ_c) of metal-semiconductor or conductive layer-semiconductor in the solar cells can limit their performance if not treated with care. It is, therefore, of great importance to be able to accurately measure ρ_c for its optimization purposes. Many methodologies have been developed for this purpose. In this thesis, various methods for extracting ρ_c are investigated. Namely, Transfer Length, Cox and Strack, four-point probe methods are discussed in detail. Cox and Strack and four-point probe methods are further extended with analytical formulations to simplify the fabrication of test samples and increase the speed of extracting ρ_c. Good agreement (relative error < 10 % for extended Cox and Strack; < 1.9 % for extended four-point probe) between the derived analytical formulations for the proposed methods and finite element method simulations is achieved. Furthermore, ρ_c of experimentally fabricated test samples determined using classic and improved methodologies is reported with good agreement between the two. Finally, a simulation study is performed to determine the optimum dimensions of the front metal grid design to be utilized in the fabrication of the solar cells.

Keywords: Contact Resistivity, Solar Cells, Front Grid Metal Design, Characterization

ÖZ

COX-STRACK VE 4 NOKTALI PROB TEKNİKLERİNE DAYALI GELİŞTİRİLMİŞ TEMAS DİRENCİ ÖLÇME YÖNTEMLERİ

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Metal-yarı iletken veya iletken-yarı iletken tabakaları arasında oluşan temas direnci (ρ_c) eğer iyileştirimez ise güneş pillerinin verimini düşürür. Bu sebeple, temas direncini doğru bir şekilde ölçmek, bu iyileştirmeyi yapmak yüksek verimli güneş pilleri için hayati bir öneme sahiptir. Bu amaçla geliştirilen birçok yöntem bu tezin konusu olmuştur. Ayrıca, bu yöntemlerden bazıları olan transfer uzunluğu (Transfer Length Method, TLM), Cox ve Strack, dört noktalı prob (four-point probe, 4PP) yöntemlerine ayrıntılı bir şekilde yer verilmiştir. Cox ve Strack yöntemi ve dört noktalı prob yönteminin analitik formülleri açılarak test numunelerinin üretimi basitleştirilmiş, temas direncini bulma kolaylaştırılmıştır. Önerilen yöntemler için türetilen analitik formülasyonlar ve sonlu elemanlar yöntemi simülasyonları arasında Cox ve Strack methodu için % 10 dan, dört noktalı prob için ise % 1,9 dan küçük bir fark gözlemlenmiştir. Ayrıca, klasik ve geliştirilmiş metodolojiler kullanılarak belirlenen temas direnci ve üretilmiş test numunelerden ölçülen temas direncinin uyumlu olduğu tespit edilmiş ve sonuçları bu tezde raporlanmıştır. Son olarak, simülasyon çalışmaları ile güneş pillerinin imalatında kullanılacak ön metal ızgara tasarımının optimum boyutları belirlenmiştir.

Anahtar Kelimeler: Temas Direnci, Güneş Pilleri, Ön Metal Izgara Tasarımı, Karakterizasyon

To my family

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ABBREVIATIONS

TLM	Transfer Length Method
SCS	Standard Cox and Strack Method
ECS	Extended Cox and Strack Method
4PP	Four-point probe
S4PP	Standard four-point probe method
E4PP	Extended four-point probe method
3D	Three dimensional
FEM	Finite element method
a-Si	Amorphous silicon
c-Si	Crystalline silicon
CL	Conductive layer
TCO	Transparent conductive oxide
ITO	Indium tin oxide
IR	Infrared
FGO	Front grid optimization

CHAPTER 1

INTRODUCTION

The quality of the metal-semiconductor interfaces is the crucial parameter in building electronic devices as it can be one of the significant sources of heat and noise. Therefore, significant effort has been put into optimizing such interfaces. One parameter that needs refinement is contact resistivity (ρ_c), a source of unwanted losses in the devices. Various methodologies to determine ρ_c indirectly have been proposed since it is not possible to measure it directly. This thesis is aimed to analyze some of the most widely used methods and provide modifications to increase their accuracy and ease their use. Improvements to the classical methods for determining ρ_c are presented with numerical and experimental verifications. It should be noted that this work is constricted only to the field of silicon solar cells and was motivated by the need to engineer the interfaces with low ρ_c. However, discussed methodologies are not restricted to the said field and can be utilized in other areas of electronics.

1.1 Metal-semiconductor contacts and contact resistivity

Metal-semiconductor contact was first invented in 1874 by Braun [1], [2]. At the time, its working principles were not well understood, and it was used with no supporting theoretical background. In the late 1930s, however, Schottky has put together the theory behind the rectifying behavior of metal-semiconductor interfaces [3]. Since then, the interest and use of these contacts have widely increased due to the well-established theory at hand, which was simultaneously strengthening as new milestones were achieved in electronics. According to Schottky's theory, depending on the energy barrier height established when metal and semiconductor are brought together, the contact can have either a rectifying (significant energy barrier height) or an ohmic (small energy barrier height) behavior. Note that ohmic contacts can be also be formed when the barrier height is significant, but the space charge region is narrow (due to high energy band bending), which allows charge carriers to tunnel [4], [5]. While the former class of the contacts has many uses, the focus of this work is on the ohmic contacts.

For almost every microelectronic device, the contact to the semiconductor is achieved through the metal. It naturally follows that these contacts should have ohmic behavior and should not introduce any losses to the device's output performance. However, due to the inherent resistance present between the metal and the semiconductor, heat losses and noise are inevitable in the system. This resistance is referred to as contact resistance, and it can be imagined as an additional resistance connected in series between the semiconductor and metal. According to Berger [6], it originates from the difference in the work functions of the metal and semiconductor and unwanted residues on the surface of the semiconductor. Furthermore, Schroder [1] implies that the surface quality (density of defect states, dangling bonds, etc.) can influence the behavior of the metal-semiconductor interfaces and affect the contact resistance. Since the contact resistance depends on the geometry of the contact, namely the contacted region area, it is more convenient to characterize the contact in terms of the contact resistivity (ρ_c) measured in $\Omega.\text{cm}^2$.

1.2 Solar cells and contact resistivity

Being one source for degradation in the performance, in most cases, the ρ_c of the metal-semiconductor interfaces in electronic devices should be minimized. ρ_c plays a crucial role in improving the heat dissipation in Gunn oscillators [7],[8], tunnel diodes [9], high cut-off frequency varactors, devices utilizing a high electric field [10]. In addition to these electronic devices, ρ_c should be treated with care in the photovoltaic devices, the solar cells. To better understand the role of ρ_c in solar cell operation, it is worth discussing the performance parameters of the solar cells.

1.2.1 Contact resistivity in solar cells

The current density (J) and voltage characteristics of an ideal solar cell can be modeled by a single diode equation:

$$J(V) = J_{\mathrm{sc}} - J_0 (e^{(V + J(V) R_{series} / (n V_{\mathrm{th}})} - 1) \qquad 1.1$$

where J_{sc} is the short-circuit current density under zero bias and illumination, J_0 is the dark saturation current, R_{series} is the series resistance (Ω.cm^2), V_{th} is the thermal voltage ($V_{\mathrm{th}} = \frac{k_{\mathrm{B}} T}{q}$, where k_{B} is the Boltzmann constant, T is the temperature in K and q is the charge) and n is the ideality factor. The standard performance parameters of a solar cell, besides the J_{sc} in 1.1, are the open-circuit voltage (V_{oc}), the fill factor (FF), and the efficiency (η). The FF is defined as:

$$\mathrm{FF} = \frac{V_{mpp} J_{mpp}}{V_{\mathrm{oc}} J_{\mathrm{sc}}} \qquad 1.2$$

where V_{mpp} and J_{mpp} are the voltage and the current density at the maximum power point. Note that FF can also be represented visually by dividing the area of a rectangle formed by J_{mpp} and V_{mpp} (blue rectangle in Figure 1.1) by the area formed by J_{sc} and V_{oc} (pink rectangle in Figure 1.1). Furthermore, η is defined as the maximum power output of the solar cell divided by the input power:

$$\eta = \frac{V_{mpp} J_{mpp}}{P_{in}} \qquad 1.3$$

Or in terms of V_{oc}, J_{sc} and FF:

$$\eta = \frac{V_{\mathrm{oc}} J_{\mathrm{sc}}\, \mathrm{FF}}{P_{in}} \qquad 1.4$$

where P_{in} is the input power.

R_{series} term in Eq. 1.1 is the summation of the resistive sources present in the solar cell. Typically, these sources include the vertical resistivity of all materials present in the solar cell, the resistance arising from the metal grid, and the contact resistance of the interfaces. To avoid dependence on the area of a device, R_{series} is reported in Ω.cm^2 (via normalization with the area of the device). It is expected that with a larger R_{series}, the η of a solar cell will degrade. This can be observed in the inset of Figure 1.1, where *J-V* curves for $R_{series} = 0$ and $R_{series} = 4\ \Omega$.cm^2 were generated using Eq. 1.1. As R_{series} is increased from 0 to 4 Ω.cm^2, η drops linearly from 18.3 % to 14.0 %. The drop in the performance occurs due to the significant degradation of the FF when R_{series} is increased.

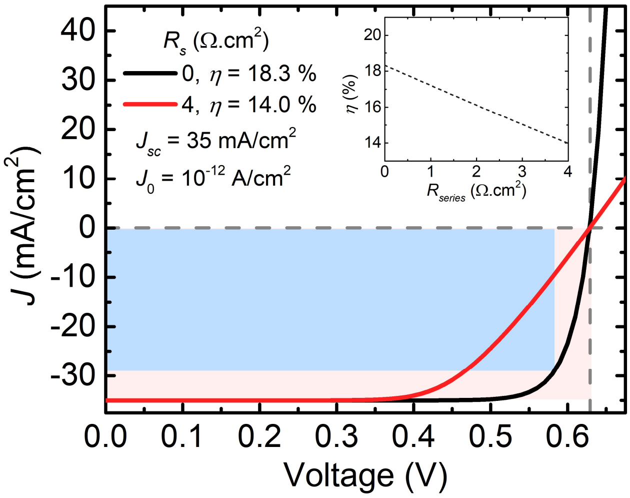

Figure 1.1. *J-V* characteristics calculated using 1.1 for $R_{series} = 0$ and 4 Ω.cm^2. The inset demonstrated the efficiency versus R_{series}.

Therefore, it is of utmost importance to keep R_{series} low enough to ensure high-performing devices. For example, from Figure 1.2, where the efficiency of a silicon solar cell is calculated for various rc and saturation currents, it can be seen that for $\rho_c < 0.3\ \Omega$.cm^2, it strongly depends on the passivation quality (saturation current density) rather than on ρ_c. It can also be noted that for $\rho_c > 1\ \Omega$.cm^2, efficiency is limited by large ρ_c. [11]

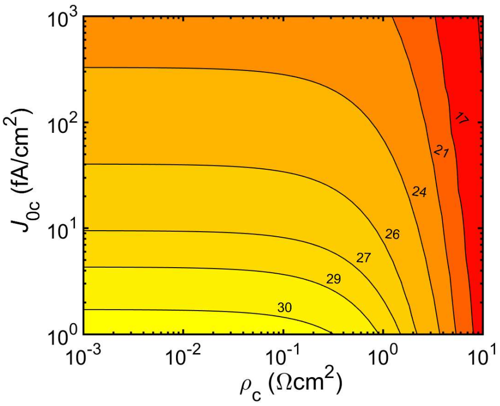

Figure 1.2. Efficiency versus contact resistivity (ρ_c) and saturation current density (J_{0c}) calculated ($J_{sc} = 43.8$ mA/cm^2). [11]

Note that, while correlating the losses in FF to large R_{series} is sufficient for the scope of this work, in non-ideal circumstances, FF can also be severely affected by high J_0 and ideality factor [12].

Since R_{series} can have a detrimental effect on the output power of a solar cell, it is crucial to identify the resistive sources that limit the performance. Typically, it is straightforward to calculate the bulk's contribution to R_{series} since its resistivity is usually known. However, it is the ρ_c of the interfaces that requires careful investigation. Generally, resistive interfaces exist between metal and semiconductor. However, it is also possible to have resistive interfaces between the materials in the solar cells if layers other than the crystalline silicon (c-Si) are used (usually, these materials bring the advantage of maintaining the high performance of the devices while keeping the fabrication costs low). There is no direct way to measure the ρ_c of interfaces since the interface is considered a surface. Therefore, numerous indirect methods have been proposed to extract this parameter.

1.3 Outline

The main purpose of this thesis is to review the widely used methodologies and investigate the improvements developed for the classic methods of extracting ρ_c. The analysis of these improvements is performed in three steps: derivation of analytical formulations, verification with the numerical simulations, and experimental demonstration of the accuracy of the modifications. Chapter 2 presents a detailed overview of the classical methods with the proposed improvements. Chapter 3 outlines the simulation tools that were used to verify the validity of the methods. Chapter 4 describes the experimental procedures for fabricating the test samples used in the third stage of this work. Results and discussions on the advantages, disadvantages, and further possible enhancements of the analyzed methods are presented in Chapter 5. Finally, Chapter 6 summarizes the main highlights of this work. In parallel to the discussion of ρ_c extraction with various methods, there is a mention of the simulation study performed for optimizing the design of the front metallization grid utilized in the solar cells. The methods, simulation setup, and results are presented in Chapters 2, 3, and 4, respectively.

CHAPTER 2

METHODOLOGY

Determining ρ_c is beneficial not only in photovoltaic applications but also in the development of transistors, sensors, etc. Throughout time, several methods for extracting ρ_c of the desired interfaces have been developed. Some of these methods have become an indispensable tool in the development of solar cells with novel topologies. In this chapter, some of the classic and some of the newer methods are presented. Additionally, the need to optimize the metal grid for the solar cells' front surface is discussed, and the utilized methodology is presented.

2.1 Transfer Length Method (TLM)

Transfer Length Method (TLM) is one of the most widely used methods to extract ρ_c. It was originally proposed by Schockley in 1964 [13] and relies on the sequential measurements of the resistance between the rectangular fingers in the designated TLM test structure, shown in Figure 2.1b. The metal fingers are usually deposited through a shadow mask or using photolithography. The measured resistance (*R*) of each neighboring pair of fingers is plotted versus the corresponding separation (*d*) between them. An example *R* versus *d* curve is illustrated in Figure 2.1a. From the slope and zero intercepts of this curve, ρ_c can be calculated solving a set of simple equations:

$$R_{\mathrm{sh}} = Z\frac{\Delta R}{\Delta d} \qquad 2.1$$

$$R_{\mathrm{c}} = \frac{\rho_c}{L_{\mathrm{T}}L} \qquad 2.2$$

$$L_{\mathrm{T}} = \sqrt{\frac{\rho_c}{R_{\mathrm{sh}}}} \qquad 2.3$$

where Z and L are the length and width of the fingers, respectively, R_{c} is the extrapolated resistance value when $d = 0$, R_{sh} is the sheet resistance of the test sample, and L_{T} is the transfer length (distance from the edge of the finger where voltage drops to $1/e$ of its maximum value).

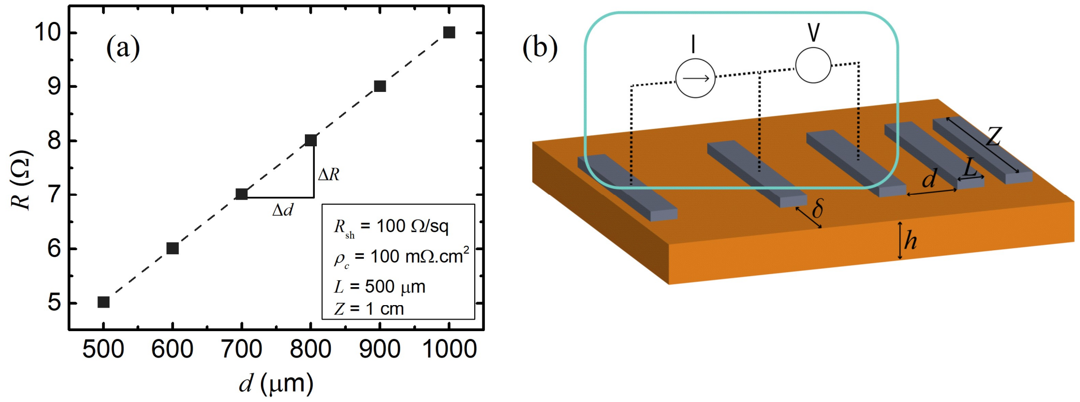

Figure 2.1. (a) An example of R versus d of a TLM test sample with the parameters specified in the inset. (b) Schematic of a TLM test sample. Encircled region demonstrates the contact end resistance (R_{CE}) measurement setup (described in the next section).

Although this method is quite popular, there are certain assumptions made for the equations 2.1-2.3 that might lead to erroneous results if not treated with care. These assumptions are:

- R_{sh} of the material is assumed to be constant throughout the test sample,
- metal fingers are thick enough to avoid the effect of metal's resistivity on the measured R,
- the thickness of the layer underneath the fingers is much smaller than d,
- Z and width of the sample are equal to each other ($\delta = 0$).

The presented list of assumptions poses difficulty in universally applying TLM approach. Therefore, extensive work has been done in addressing these assumptions to allow simpler and more feasible utilization of TLM. In the following, each assumption is addressed individually with its brief description and possible ways of correcting the result.

2.1.1 Non-uniform R_{sh}

One potential issue arising in applying TLM is the assumption that R_{sh} is homogeneous throughout the test sample. In reality, during the formation of the metal contacts, the underlying region might undergo some physical changes[14],[15], resulting in different R_{sh} underneath them. To account for non-uniform R_{sh}, [16] proposed the following approach. In addition to the standard measurement procedure of TLM, making an additional measurement (Figure 2.1b) of "end resistance" (R_{CE}) and using the following set of equations provides more reliable ρ_c.

$$R_{\mathrm{c}} = \frac{R_{\mathrm{SK}} L_{\mathrm{T}}}{Z} \coth(L / L_{\mathrm{T}}) \qquad 2.4$$

where $L_{\mathrm{T}} = \sqrt{\dfrac{\rho_c}{R_{\mathrm{SK}}}}$ and R_{SK} is the modified sheet resistance underneath the metal fingers $\qquad$ 2.5

$$R_{\mathrm{CE}} = \frac{\rho_c}{L_{\mathrm{T}} Z} \frac{1}{\sinh(L / L_{\mathrm{T}})} \qquad 2.6$$

$$\frac{R_{\mathrm{c}}}{R_{\mathrm{CE}}} = \cosh(L / L_{\mathrm{T}}) \qquad 2.7$$

Hence, using Eq. 2.4, 2.5, and 2.7, L_{T} can be found, and thus ρ_c determined from Eq. 2.6.

2.1.2 Effect of thin metal fingers

Guo et al. [17] have reported that there is a non-ideal current distribution within the metal fingers in the presence of the non-negligible line resistance (R_{line}). R_{line} can significantly contribute to the measured R when it is large, or in other words, the thickness of the deposited metal or metal's conductivity is low. This behavior was confirmed using numerical simulations, and based on the current distribution profile, a corresponding correction factor was proposed. Application of this correction factor requires the knowledge of the R_{line} of the metal fingers. Once R_{line} is known, corrected measured resistance ($R_{\text{cor.line}}$) is calculated as:

$$R_{\text{cor.line}} = R - \frac{R_{\text{line}} Z}{6} \qquad 2.8$$

Then using corrected resistance values, one can proceed to ρ_c estimation using the aforementioned procedures, i.e., perform fitting to $R_{\text{cor.line}}$ versus d curve and determine ρ_c from the fitted parameters.

2.1.3 Effect of thick test samples

Another crucial aspect in TLM is the assumption that the layer (or substrate) under the contact fingers is thin enough ($h << d$) to ensure that current is reaching the bottom of the sample. However, in some cases, one might desire to measure ρ_c of the interfaces on the thick layers/substrates. In this case, the current might not reach the bottom of the sample affecting measured R. Two extreme cases of full and partial vertical spreading of current are demonstrated in Figure 2.2.

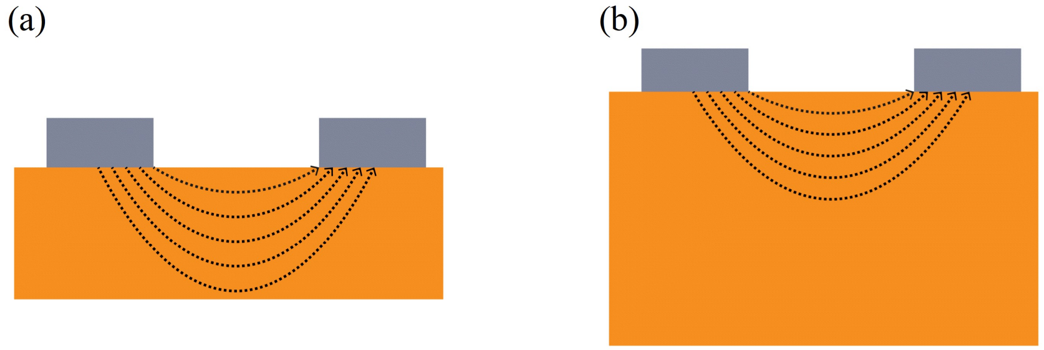

Figure 2.2. Vertical spreading in TLM structures. (a) Full spreading of current in a thin layer ($h << d$). (b) Partial spreading of current in the thick layer ($h \sim d$).

One possible solution, although not preferable, is to utilize a larger separation of the fingers. However, this approach might be unpractical due to sample size limitations and, additionally, with larger d, the contribution of ρ_c to R becomes smaller, making it more difficult to distinguish since R is dominated by R_{sh} of the layer. Therefore, a solution was proposed by Eidelloth and Brendel [18]. Using a method of images, they arrived at an analytical formulation that considers the non-ideal current distribution in thick samples and thus leads to a more accurate determination of ρ_c. One can refer to the original publication [18] for a more detailed presentation of the formulas, and here the final result is presented. The proposed approach consists of calculating the geometrical correction factor (G) using Eq. 2.9 and solving for ρ_c in Eq. 2.10.

$$G = 1 + \sqrt{(G_{\text{1D-TLM}} - 1)^2 + (G_{\text{CM}} - 1)^2} \qquad 2.9$$

$$G = \frac{R_c}{m} / \frac{\rho_c h}{\rho_{\mathrm{b}} L} \qquad 2.10$$

where, $G_{\text{1D-TLM}}$ and G_{CM} could be found in [18], m is the slope of R versus d curve, h is the thickness of the layer, and ρ_{b} is the resistivity of the layer.

2.1.4 Effect of uncut edges

Another assumption in TLM is that current travels only perpendicularly to the longer edge of the fingers without spreading sideways. To achieve this behavior experimentally, the edges are isolated (or cleaved) by laser or using photolithography. However, these steps can be quite imprecise (edge isolation with a laser) or time-consuming (lithography), which necessitates another correction. Without these additional steps, i.e., without edge isolation, the current spreads sideways, shown in Figure 2.3, consequently affecting the results. It should be further noted that if classical TLM theory were applied to the structures without isolated edges, calculated ρ_c would be overestimated due to the increase of fitted R_c. This result can be counter-intuitive due to the assumption that current can have more paths to travel. However, the current spreading through uncut edges becomes more significant for larger d, reducing the measured R. The lower R values at higher d's decrease the slope of the fitted curve, which in turn increases the y-intercept, i.e., R_c. So, in this case, not only the ρ_c is overestimated, but also an inaccurate R_{sh} is determined.

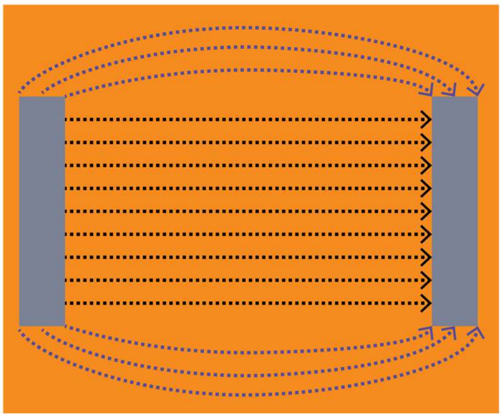

Figure 2.3. The current path from one finger to another in a TLM sample with uncut edges. Blue dashed arrows demonstrate the current that spreads inside the uncut edges, black arrows represent the typical current path in a cleaved TLM sample.

Chor and Lerdworatawee [19] have come up with yet another way to account for the effects of non-isolated edges. It suggests that using R_{CE} and parallel resistance term ($R_{//}$) one can arrive at the corrected R. $R_{//}$ is the resistance of the uncut edges, which is calculated by the method of images and it is given by:

$$R_{//} = 2R_{\mathrm{sh}} \frac{K(k_0)}{K(k_0^{'})} \qquad 2.11$$

$$\text{where, } k_0 = \frac{\tanh(\frac{d\pi}{4\delta})}{\tanh(\frac{(d+2L)\pi}{4\delta})} \text{ and } k_0^{'} = \sqrt{1-k_0^2} \qquad 2.12$$

where δ is the width of the non-isolated edge, and $K(x)$ is the complete elliptic integral of the first kind with the modulus x.

Then using R_{CE} and $R_{//}$, the total resistance is corrected as follows:

$$R' = \frac{2R_{\mathrm{CE}}(-2R_{\mathrm{CE}} + R_{//}/2) - R_T(-2R_{\mathrm{CE}} + R_{//}/2) - R_{//}R_{\mathrm{CE}}}{R_T - 2R_{\mathrm{CE}} - R_{//}/2} \qquad 2.13$$

where, R_T is the resistance of the structure with non-isolated edges.

Finally, ρ_c is calculated by performing fitting on the curve of the corrected resistance (R') given by Eq. 2.13 versus d. Note that the total resistance of the structure in Figure 2.3 can be calculated as:

$$R = 2R_{\mathrm{CE}} + [2(R_c - R_{\mathrm{CE}}) + R_{\mathrm{sh}}d/Z]//[R_{//}/2] \qquad 2.14$$

where, $[x_1]//[x_2]$ represents parallel combination of x_1 and x_2 resistors.

2.2 Cox and Strack Method (CS)

In addition to TLM, another widely used method for extracting ρ_c is named after Cox and Strack (CS) [20]. Similar to TLM, this method relies on the variation of the measured R with the size of the contact. Unlike the TLM structures, however, the CS structures utilize circular metal electrodes of various diameters and are contacted from top and bottom, as shown in Figure 2.4b. ρ_c is extracted from the fitted parameters of the R versus electrode radius (b) curve, shown in Figure 2.4a.

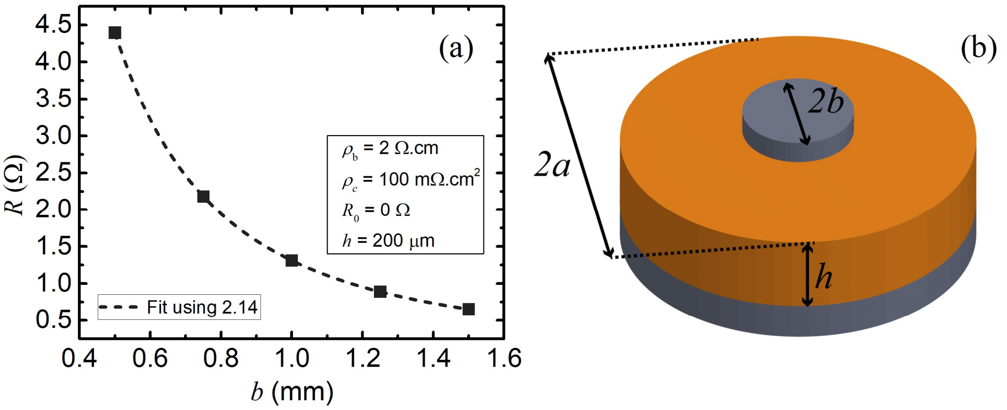

Figure 2.4 (a) An example of R versus b of a CS test sample with the parameters specified in the inset (a is assumed to be infinite). The dashed line shows the fitted curve using 2.15. (b) Schematic of a CS test sample. Grey regions represent the electrodes.

The relation between obtained R versus b is given by:

$$R = \frac{\rho_b}{2b\pi}\arctan\left(\frac{2}{b/h}\right) + \rho_c + R_0 \qquad 2.15$$

where R_0 is the residual resistance of the backside contact, which is independent of the contact diameter. Note that the backside contact should have an ohmic behavior and preferably low ρ_c (lower than the ρ_c of the front side) to eliminate additional sources of potential errors.

Standard CS method (SCS) can be directly applied to metal-semiconductor or metal-insulator-semiconductor interfaces without any additional deposition steps [21],[22]. However, it is also possible to insert a conductive layer (CL) between the metal and the semiconductor (this kind of interface is usually analyzed in the development of solar cells with passivating heterocontacts [23]). For this analysis, the SCS method necessitates confinement of the CL under the metal contact. This limitation arises from the analytical formulation given in Eq. 2.15, which assumes a confined CL structure. As a result, fabrication of the test samples might require additional time-consuming steps such as photolithography or reactive ion etching to form the confined CL. It is possible to avoid these steps if the particular CL can be sputtered or thermally evaporated [e.g., sputtered indium tin oxide (ITO)]; in these cases, the desired pattern can be achieved through a shadow mask. However, when the use of the shadow mask is not possible (e.g., spin-coated CL) the etching step is necessary. Figure 2.5 demonstrates the confined and non-confined CS structures. It is inaccurate to assume that applying SCS on the test structures with non-confined CL yields reliable ρ_c results. To understand the differences between confined and non-confined CS structures, the concept of spreading resistance needs to be discussed.

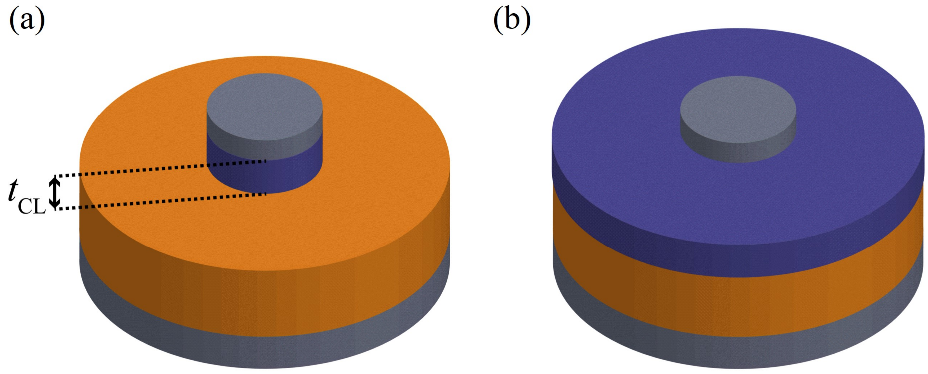

Figure 2.5. (a) Confined CL (purple) and (b) non-confined CL CS structures.

2.2.1 Spreading resistance

It is natural for current to spread inside the bulk once it enters from the layer with smaller dimensions, namely the contact stacks in the CS structures. If CL under the metal is not confined and has a comparable resistivity with the bulk, there is a current spreading happening inside both the CL and the bulk, affecting the measured resistance. In order to model this behavior and determine ρ_c using non-confined CS structures, one can use 3D FEM simulations, but it is rather a time-consuming task. Another alternative is to develop an analytical formulation that can model the spreading resistance of the multilayered structures with comparable resistivity values. This is done in our work [23], where we analyzed various spreading resistance models (adapted from various disciplines) of multilayered structures and analytically determined the resistance of the CS structures with non-confined CL. The calculated R is compared with numerically simulated values (using COMSOL Multiphysics [24] software) and the relative errors for each of the analyzed models are reported. We noted that the models providing the highest accuracy (< 0.1 % relative error) are computationally expensive and require expertise in using numerical software such as MATLAB. Therefore, we proposed an alternative formulation that is less computationally expensive than other alternatives and has a high degree of accuracy for the desired range of ρ_c (for solar cell application $\rho_c > 100$ mΩ.cm^2).

$$R_0 = \frac{\rho_\mathrm{m}}{\pi b^2} + \left[\frac{\pi b^2}{\rho_c + \rho_\mathrm{m} + \pi b^2 R_\mathrm{spr}} + \frac{2\pi kb}{R_\mathrm{CL}} \left(\frac{K_1(kb)I_1(ka) - I_1(kb)K_1(ka)}{K_0(kb)I_1(ka) + I_0(kb)K_1(ka)} \right) \right]^{-1} \qquad 2.16$$

where $k = [R_\mathrm{CL}/(\rho_\mathrm{rear} + \rho_c + \rho_\mathrm{b}\mathrm{h})]^{1/2}$, R_CL is the sheet resistance of CL, ρ_m is the contact resistivity of the electrode-CL interface, ρ_rear is the contact resistivity of the bottom electrode, a is the radius of the substrate, R_spr is the resistance given by the first term in Eq. 2.15, and I_0 and K_0 are the zeroth-order modified Bessel equations of the first and second kind, respectively, I_1 and K_1 are the first-order modified Bessel equations of the first and second kind, respectively.

To extract ρ_c using the approach in [23], which is named Extended Cox and Strack (ECS), one can fit the experimentally obtained data to the resistance formulation given in Eq. 2.16.

2.3 Four-Point Probe Method (4PP)

Alternative to TLM and SCS/ECS methods for extracting ρ_c, the four-point probe (4PP) method requires significantly fewer fabrication steps. This method was first used by Römer et al. [25] to determine ρ_c of poly-crystalline Si/mono-crystalline Si junctions with the presence of various interfacial Si oxides. For the sake of future discussion, the originally proposed 4PP method is referred to as the standard 4PP method (S4PP). Here, the test structures incorporating only two layers, a conductive layer (CL) and a substrate, are considered, although it is possible to extract ρ_c of structures with more than two layers. To extract ρ_c using S4PP following measurements should be made:

i. sheet resistance of CL, (R_{CL}),
ii. sheet resistance of the substrate, (R_{s}),
iii. sheet resistance of the test structure, (R_{stack}).

Note that all sheet resistance values are assumed to be measured using the 4PP station, although it is possible to measure R_{s} using the eddy-current method [26], [27]. Once the experimental data are obtained, namely R_{CL} and R_{s}, simulation tools are used to generate a R_{stack} versus ρ_c curve, and ρ_c is then correlated with experimentally measured R_{stack}. Figure 2.6 demonstrates test structures required for S4PP and an exemplary R_{stack} versus ρ_c curve.

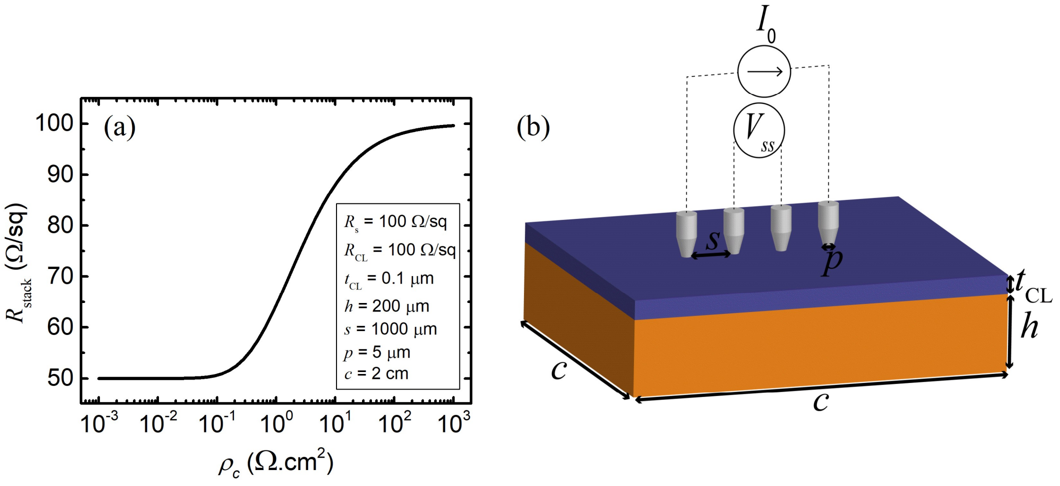

Figure 2.6. (a) An example of R_{stack} versus ρ_c of a 4PP test sample with the parameters specified in the inset. (b) Schematic of a test sample measured with 4PP station contacted from the CL side.

There are two main drawbacks of this method. The first one is the need for separate measurement of R_{CL}. To measure R_{CL}, the CL should be electrically isolated from the substrate on which it is deposited (e.g., glass, highly resistive Si) for accurate measurement of R_{CL}; this condition implies the use of an additional test sample which complicates the use of S4PP. Note that in some cases, the surface of the substrate for R_{CL} measurement and the surface of the substrate for R_{stack} measurement should be the same; otherwise, the electrical quality might differ due to possible differences in the deposited CL. The second drawback is the time-consuming generation of R_{stack} versus ρ_c curves using simulation tools. Since S4PP requires the simulations in 3D domain, this step of the S4PP method can take up to hours or days depending on the resolution of ρ_c (one simulation takes 15 to 30 min on the workstation used in this work). Regardless, S4PP is still attractive since it eliminates a metallization step for the cases when otherwise it would have been necessary, i.e., TLM or SCS/ECS.

To make the S4PP method more convenient to use, we [28] have analytically solved for R_{stack} of the structure in Figure 2.6b. Similar to Extended Cox and Strack method, the solution for R_{stack} employs the spreading resistance model to arrive at four equations to be solved (refer to the original publication for the formulations). With the analytical calculation of the R_{stack} versus ρ_c curve, which takes less than a minute, the S4PP method becomes much more time-efficient and more feasible to use. However, there is still the need for a separate sample for R_{CL} measurement, an extra expense, and a potential source of error (in the case of different electrical properties of the deposited CL).

In addition to the analytical formulation for R_{stack}, we also proposed an extended 4PP (E4PP) methodology. This method requires only one test sample and three following measurements to extract ρ_c:

i. R_{s}, measured before the deposition of the CL,

ii. $R_{\mathrm{stack,1}}$ measured from the CL side after the deposition of the CL,

iii. $R_{\mathrm{stack,2}}$ measured from the substrate side after the deposition of the CL.

Note that in this method, in addition to ρ_c, R_{CL} is also unknown. But this does not pose any limitation. Since $R_{\mathrm{stack,1}}$ and $R_{\mathrm{stack,2}}$ are both functions of R_{CL} and ρ_c, two equations with two unknowns are obtained:

$$\begin{aligned} f(R_{\mathrm{CL}}, R_{\mathrm{s}}, \rho_c, t_{\mathrm{CL}}, h) &= R_{\mathrm{stack,1}} \\ f(R_{\mathrm{s}}, R_{\mathrm{CL}}, \rho_c, h, t_{\mathrm{CL}}) &= R_{\mathrm{stack,2}} \end{aligned} \tag{2.17}$$

where f is the function calculating R_{stack} for given parameters, t_{CL} is the thickness of the CL. Solving this system of equations provides ρ_c and R_{CL}. Hence, with only three measurements and no need for extra samples, both ρ_c and R_{CSL} can be determined using the E4PP method.

2.4 Front Grid Optimization (FGO)

Besides the optimization of ρ_c of the interfaces present in the solar cell, its performance can be enhanced by a carefully designed front metal pattern. There is a trade-off between the series resistance (R_{series}) and the shadowing losses for any given front metal pattern. Shadowing losses arise due to the inability of the regions covered by the metal to generate the charge carriers; hence J_{sc} is decreased. R_{series}, on the other hand, is the product of a limited collection of the generated carriers across the surface of the solar cell. With the more significant metal coverage of the surface, R_{series} decreases, which in turn increases the FF, however at the same time, the J_{sc} drops due to the increased shadowing losses. Therefore, it is necessary to optimize the design of the metal pattern (front grid design) before proceeding to the metallization step in the solar cell fabrication.

Note that the front grids can take up any shapes and forms, making the available options infinite. However, the limitation arises from the feasibility of the fabrication of the grids. For example, Gupta et al. [29], [30] have done an extensive analysis of the optimization of front metallization patterns. However, their results include patterns that are not easily implementable using widely used metallization techniques (i.e., screen-printing). In this work, the optimization was focused on one type of grid design shown in Figure 2.7.

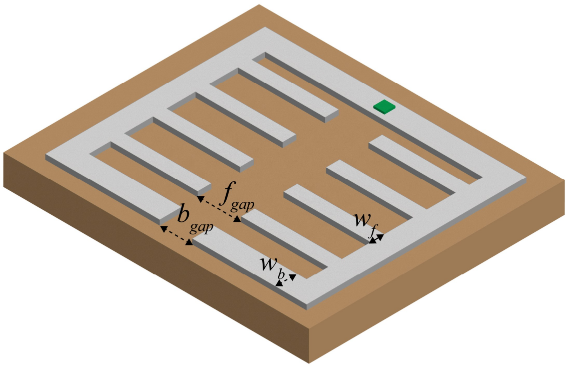

Figure 2.7 Front metal grid (grey) design on top of arbitrary TCO utilized in solar cells (light brown). The grid is contacted with a square electrode (green).

The following grid was optimized in terms of the number of the fingers (or the distance between them), their width (w_f)] and the width of the surrounding busbar (w_b). The need for a rigorous optimization analysis arose from the limitations dictated by the fabrication processes, namely, the thickness of the evaporated metal was limited only to 200 nm, and the minimum allowed w_f was 200 µm. Furthermore, b_{gap} and f_{gap} were fixed at 1 and 2 mm, respectively, to decrease the complexity of the optimization process. Therefore, with these limitations at hand, it was desired to obtain a front grid yielding minimum R_{series} without significant degradation in J_{sc}. R_{series} and shadowing losses for each combination were determined from the numerical simulations (methodology described in the next chapter), diode parameters were determined by fitting the experimentally obtained J-V characteristics of a heterojunction solar cell ($J_{\mathrm{sc}} = 36.83$ mA/cm^2, $J_0 = 55$ pA/cm^2, $n = 1.358$) using “Equivalent Circuit” online tool [31]. Finally, the fitted diode parameters together with R_{series} and shadowing losses were used to calculate the J-V characteristics using the diode equation (Eq. 1.1). Note that R_{series} is determined from the FEM simulations, and J_{sc} was scaled by the calculated shadowing fraction of the grid. The efficiencies of the generated J-V curves were determined and analyzed for the optimization of the given grid design.

CHAPTER 3

SIMULATIONS

Simulation tools are beneficial in testing various hypotheses developed in the process of any particular research. With a simulation study, one can design more efficient experiments, better interpret the experimental results, deeper understand the physical behaviors, verify the proposed hypotheses, etc. In this thesis, the simulation tools were used for two purposes:

i. Simulate the test structures used in TLM, CS, and 4PP methods to analyze the accuracy of the analytically proposed resistance formulations in [19], [23], [28].
ii. Determine the optimum grid design for the solar cells.

This chapter briefly discusses the FEM simulation tools. Then, the discussion is followed up by the description of the problem domains for TLM, CS/ECS, and S4PP/E4PP ρ_c extraction methods. Finally, the chapter is concluded by presenting the method for determining the optimum front grid design for the solar cells. Note that, unless stated otherwise, the simulation tool that was used is COMSOL Multiphysics' AC/DC module [24].

3.1 FEM simulation tool

The finite element method (FEM) is a widely used method for numerically solving partial differential equations. The capabilities of FEM are endless, and the limitations are only imposed by the user. The FEM solves the given problem by dividing a given domain into smaller and simpler parts, called finite elements. The division process is achieved by discretizing the given space resulting in the mesh of an object – a numerical domain for the solution. Each element of the mesh is assigned with a specific value according to the specified boundary conditions and notations inherent to FEM. After assigning the elements with their corresponding values, a system of algebraic equations with unknown variables is formed, which is then solved utilizing concepts from linear algebra. FEM does not provide an exact solution to the problem but rather finds an approximation. One key element in FEM is the density of the mesh (number of finite elements). While a domain with a very coarse mesh can lead to an inaccurate result, a domain with a very fine mesh can take up a lot of computation power and time.

Generally, to solve a particular problem with FEM, it is necessary to construct the aforementioned system of algebraic equations and then solve it. For these purposes, computational software such as MATLAB [32] is a good fit. With experience in FEM and the usage of MATLAB, one can successfully solve the given problem. However, FEM in itself is a rather complicated method involving lots of different approaches for meshing, assigning the values to the mesh elements making it challenging to use. To this end, there are commercially available software programs that incorporate well designed guided user interface (GUI) and provide the capabilities of solving given problems using FEM without the need for deep knowledge of the method itself. One such tool is COMSOL Multiphysics [24]. It is used in various fields such as mechanical engineering, chemical engineering, electrical engineering, optics, and many more. In the scope of this work, COMSOL was used to determine the total resistance of the structures mentioned in the previous chapter, namely:

- structures for TLM,
- structures for SCS and ECS,
- structures for S4PP and E4PP (for these structures, sheet resistance instead of total resistance was obtained).

Additionally, COMSOL was used to determine the optimum front grid metal design for the fabrication of the solar cells in terms of the series resistance (R_{series}) and shadowing fraction.

3.1.1 Meshing in COMSOL

It was mentioned that the accuracy of FEM results depends on the density of the mesh: the finer the mesh, the better the results (at the expense of computation time). COMSOL provides automatic algorithms for generating the mesh for given domains; however, it is also possible to specify the type of the shape and size of the elements in the mesh. In this work, the triangular mesh type used for surfaces (2D objects), and the swept mesh was used for 3D objects. Most of the time, it is necessary to build a custom mesh to reduce the computational load on the computer by making coarse elements in regions less relevant to the specified problem. The earlier mentioned system of equations in FEM is stored in RAM; hence it is expected that RAM of the computer is heavily utilized during the simulation of the domain meshed with many elements. A workstation with 192 GB of RAM, 20-core E5 central processing unit (CPU) at 3 GHz was used in this work.

To determine the optimum mesh density for a specific problem domain, structures for which R (or R_{series} for grid optimization) can be calculated analytically were simulated, and the mesh was refined until the relative error ($\delta_{rel.} = \frac{R_{sim.} - R_{theory}}{R_{sim.}} \times 100$) between simulated and analytically calculated results would be below 0.1 %. Note that the same definition of relative error was used when COMSOL results are compared with newly proposed analytical formulations.

3.2 TLM structures

For better understanding and more reliable extraction of ρ_c from the experimental TLM measurements, simulation of the TLM structures was performed. The simulation aimed to provide deeper insight into:

- effect of uncut edges (δ) on the extracted ρ_c and the applicability of analytical formulations proposed in [19].

As a first step in simulating TLM structures, mesh optimization was performed with the previously mentioned method. The domain for the mesh optimization step was implemented in such a way that all assumptions for TLM theoretical equations would be satisfied, that is:

- R_{sh} across the sample is uniform,
- metal thickness is large,
- h (thickness of the layer) is much smaller than d (finger separation),
- L (length of the fingers) is much larger than L_T,
- δ is 0.

With the optimized mesh, the structures for the analysis of the effects of δ on the measured resistance were implemented. Figure 3.1 demonstrates an exemplary structure implemented in COMSOL.

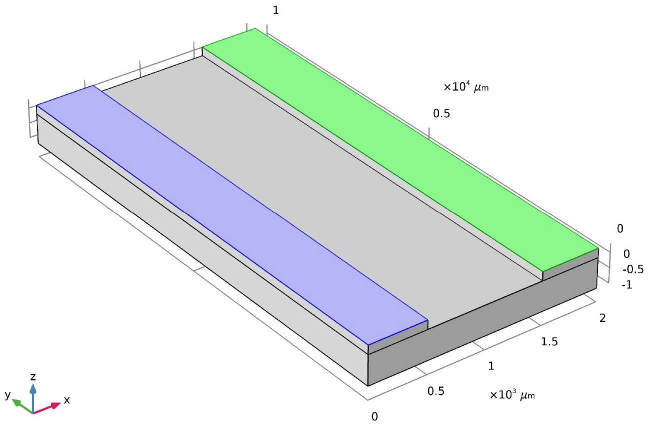

Figure 3.1. TLM structure in COMSOL (the dimensions are scaled for easier representation).

The voltage of 1 V is applied to the surface highlighted in blue, while the green highlighted surface is defined as ground. ρ_c is introduced with the help of the 'Contact Impedance' physics element. The table below summarizes the range of parameters used in the simulations for each of the aforementioned purposes.

Table 3.1. The parameter list for investigating the effects of the dimensions of TLM structures.

Effect of δ
$Z = 1$ cm
$L = 0.5$ mm
$h = 0.1$ μm
$d = 500$, 1000 μm
$\rho_c = 10^0, 10^1, 10^2, 10^3$ mΩ.cm^2
$R_s = 10^0, 10^1, 10^2, 10^3$ Ω/sq
$\delta =$ between 50 and 10^3 μm

3.3 CS structures

The purpose of simulating the CS structures was to verify the validity of the analytically determined spreading resistance models presented in [23]. Following similar steps as in the simulation of the TLM structures, mesh for CS structures was optimized by implementing the structure that complied with the assumptions for CS theoretical expression (2.15) and reducing $\delta_{rel.}$ between simulated and analytically calculated R's. Figure 3.2 demonstrates the CS structure without CL.

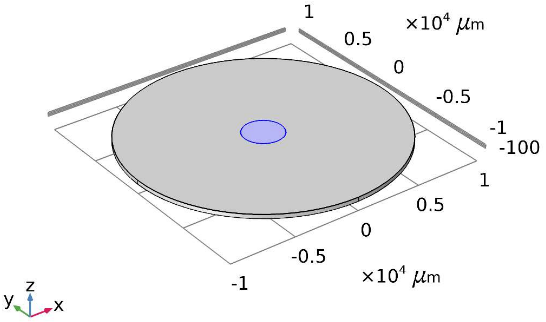

Figure 3.2. CS structure implemented in COMSOL. 1 V is applied to the blue region; the ground is the bottom surface of the structure (not highlighted).

The voltage of 1 V is applied to the top circular surface (blue region in Figure 3.2), and the ground is assumed to be the bottom surface. Following the mesh optimization step, CS structures with confined and non-confined CL, shown in Figure 2.5, were defined and simulated in the software. For simplicity of the analysis, ρ_c's of the metal-CL and substrate-metal interfaces were assumed to be 0 or 10 mΩ.cm^2, and only the CL-substrate interface had non-zero ρ_c. t_{CL} and t_{s} were assumed to be 0.1 and 200 µm, respectively. b, R_{CL} and ρ_c were varied between 10^1 and 10^3 µm, 10^2 and 10^4 Ω/sq, 10^0 and 10^3 mΩ.cm^2, respectively.

3.4 4PP structures

S4PP/E4PP methods have the potential to be very time-efficient methods for extracting ρ_c if the required FEM simulations would be replaced by an analytical formula that can be executed in under one second. For the development and derivation of an analytical formulation, it is necessary to have the reference results with which it should be compared; otherwise, it would be almost impossible to conclude whether the given formula provides accurate results. Therefore, in this work, 3D simulation of the 4PP structure, shown in Figure 2.6, was performed in

COMSOL to generate the reference values for the analysis of the analytical formulation reported in [28] for the calculation of R_{stack} of these structures.

The simulation domain was implemented according to the experimental measurement of sheet resistance by the 4PP station of a 2×2 or 10×10 cm^2 sample. (The working principle and other details, such as the geometry-dependent correction factors, of this measurement technique are described in the next chapter).

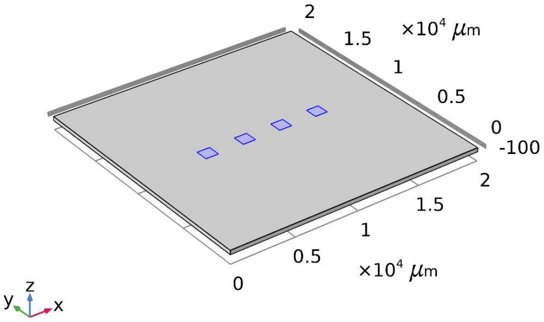

Figure 3.3. 4PP structure implemented in COMSOL. Blue regions are the probes.

Figure 3.3 demonstrates the implemented simulation domain in COMSOL. The probes are modeled as surfaces (four square areas in blue), the current of 1 mA is defined to enter from the leftmost probe and leave from the rightmost one. The voltage is measured by the inner two probes. To calculate the sheet resistance, the voltage difference between the inner probes is divided by the input current (1 mA) and then multiplied by the corresponding correction factor [33]. To optimize the mesh for the 4PP structure with two layers, R_{stack} of the structures with zero and infinite ρ_c was simulated. When ρ_c between the CL and the substrate is zero, measured R_{stack} is the parallel combination of R_{CL} and R_{s} ($R_{\text{stack}} = (\frac{1}{R_{\text{CL}}} + \frac{1}{R_{\text{s}}})^{-1}$), and for $\rho_c \to \infty$, R_{stack} is equal to the sheet resistance of the contacted layer. Hence, the expected results were compared with the simulated ones, and the mesh was refined accordingly. For the subsequent simulations, 4PP structures were contacted from the substrate and the CL sides, the substrate width was assumed to be 2 or 10 cm, ρ_c was varied between 10^{-3} to 10^{2} Ω.cm^2, R_{CL} from 10^0 to 10^3 Ω/sq, R_s from 10^0 to 10^3 Ω/sq and probe spacing from 10^1 to 10^3 μm.

3.5 Front Grid Optimization

Similar to the simulation of the test structures for ρ_c extraction methods, COMSOL was used to calculate R_{series} and shadowing losses of various grid designs to find the optimum design to be used in the fabrication of the solar cell. To reduce the complexity of the simulation domain, instead of simulating a fully operational solar cell, only its top part, i.e., TCO and metal grid, of the cell was considered. According to [34], lateral current inside a TCO linearly increases in the direction toward the electrode. To model the linear behavior of the current, a highly resistive layer (with known resistivity) between the TCO and the voltage terminal was introduced. To check the validity of this approach, and additionally to optimize the mesh, simulated results of the structure shown in Figure 3.4 were compared with the analytical formula given by [35]:

$$R_{series} = \frac{1}{3} R_{\mathrm{TCO}} L_{\mathrm{TCO}}{}^{2} \qquad 3.1$$

where R_{TCO} is the sheet resistance of the TCO, L_{TCO} is the length and width of the TCO.

R_{series} in COMSOL was calculated by subtracting the resistance of a highly resistive layer from the total resistance of the structure and multiplying it by the area of the TCO.

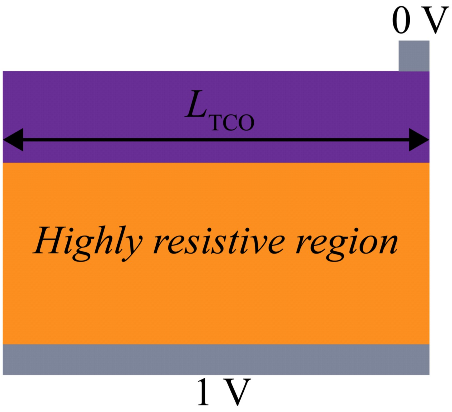

Figure 3.4. 2D view of the structure used to verify the proposed approach of estimating R_{series}.

For all optimization simulations, R_{TCO} was assumed to be 100 Ω/sq (most relevant for the fabricated solar cells), the thickness of the metal grid was defined 200 nm (metal's resistivity was assumed to be 1.6×10^{-8} Ω.m), size of the TCO was fixed at 1.2×1.2 cm^2. The electrode for the metal grid was defined at the bottom of the grid (region highlighted in green in Figure 2.7) with a 100×100 μm^2 area.

CHAPTER 4

EXPERIMENTS

Two previous chapters have discussed the non-experimental aspects of TLM, SCS/ECS, and S4PP/E4PP ρ_c extraction methods. However, to be able to state that the proposed modifications/extensions to those methods are valid, they should be validated on the experimental level. Therefore, in this chapter, the fabrication details of the test samples for TLM, CS/ECS, and S4PP/E4PP methods are described. Finally, methods for obtaining the resistance values, sheet resistance, and current-voltage (*I-V*) characteristics are described.

4.1 Fabrication of test samples for ρ_c extraction methods

All test samples for ρ_c extraction methods were fabricated using ~180 μm-thick 2×2 cm^2 double-side textured *n*-type c-Si wafers. In addition to the *n*-type wafers, *p*-type c-Si wafers were used to accurately determine R_{CL} for the S4PP method and ρ_c of the Ag/ITO interface. (*p*-type wafers ensured the rectifying behavior between the substrate and the CL, leading to the electrical isolation of the CL from the substrate.) Texturing of c-Si 156×156 mm^2 wafers was performed by immersing them into 75 °C H_2O:IPA:KOH (91.4 %: 4.5 %: 4.1 %) solution for 45 minutes. Then, the textured wafers were dipped into HF:HCl solution to remove the oxide on the surface and the residues of KOH [36]. Following the texturing process, the wafers were cleaved into 2×2 cm^2 samples using the IR wavelength laser. Prepared samples were divided into two groups: samples for CS and 4PP experiments. Figure 4.1 demonstrates the steps of texturing and cleaving procedures.

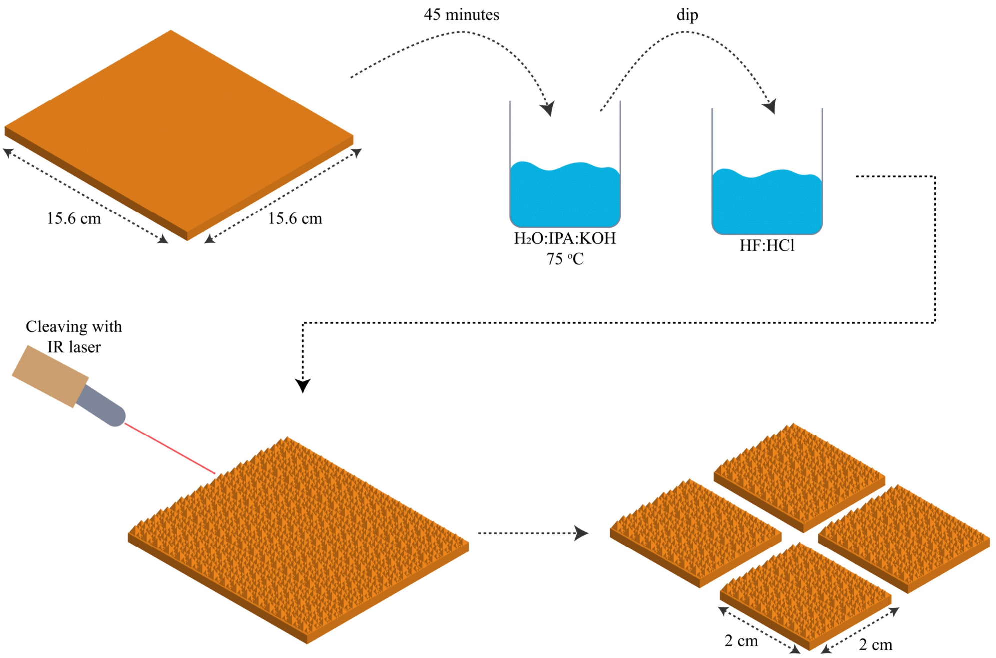

Figure 4.1. Illustration of texturing and cleaving steps of c-Si wafers.

To form the desired TLM (rectangular metal fingers with increasing distance) or CS patterns (circular metal contacts with increasing diameter), shadow masks using poly-Si were prepared using the aforementioned laser. For the TLM pattern, a mask containing 0.5×10 mm^2 openings with a distance increasing from 500 to 1000 μm (TLM mask) was prepared (Figure 4.2a). For the CS pattern, a CS mask with circular openings of 0.5, 0.75, and 1 mm radii (Figure 4.2b) was made.

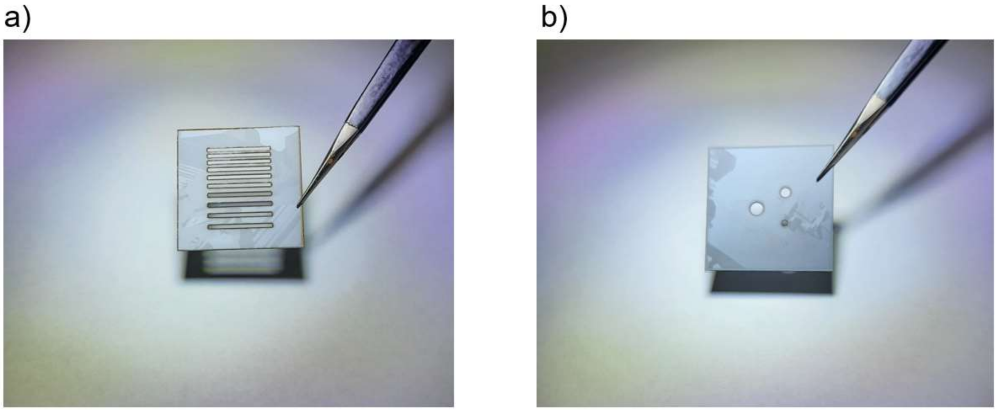

Figure 4.2. Polysilicon masks used for (a) TLM pattern, (b) CS pattern.

To control the range of ρ_c, amorphous Si (a-Si:H) stacks consisting of (*i*)a-Si:H (sheet resistance >10^{10} Ω/sq) and phosphorus-doped [(*n*)a-Si:H, >10^7 Ω/sq] a-Si:H were deposited under varying conditions (check next sections) using plasma-enhanced chemical vapor deposition (PECVD). Some samples with (*i*)a-Si:H/(*n*)a-Si:H were coated with ITO using sputtering. Lastly, evaporated Ag was used as a metal contact to ITO and evaporated LiF_x/Al to either (*i*)a-Si:H/(*n*)c-Si or (*n*)c-Si.

It should be noted that the extracted ρ_c from the textured surfaces is not corrected by the area of the pyramids to be represented as the ρ_c of the polished surface. In other words, if the same materials (assuming the same electrical qualities) were deposited on the polished surface, then the extracted ρ_c would be larger than the ρ_c extracted from the textured surface due to the smaller effective contacted area.

4.1.1 a-Si and ITO deposition

For deposition of the a-Si:H stacks in this work, Guner Cluster System (manufactured in 2009 by VakSis) has been used. The system is capable of depositing intrinsic (*i*), phosphorus-doped (*n*), and boron-doped (*p*) a-Si:H using capacitively coupled plasma technique in separate chambers. Moreover, there is a sputtering chamber with the controlled O_2 flow for depositing the ITO.

Figure 4.3. Guner Cluster System.

The table below demonstrates the deposition parameters of (*i*)a-Si:H, (*n*)a-Si:H, and ITO that were used in this work. Note that the thickness of the deposited material is mentioned as it is relevant for future discussion.

Table 4.1 Deposition parameters for (*i*)a-Si:H, (*n*)a-Si:H and ITO.

Material	*Thickness*	*Deposition parameters*
(*i*)a-Si:H[‡]	7 or 14 nm	Pressure: 1.2 Torr Temperature: 200 °C Power density: 48 mW/cm^2 SiH$_4$[a] flow rate: 40 sccm[*] H$_2$ flow rate: 120 sccm
(*n*)a-Si:H	13 nm	Pressure: 1 Torr Temperature: 200 °C Power density: 48 mW/cm^2 SiH$_4$ flow rate: 13 sccm PH$_3$[b] flow rate: 25 sccm Hydrogen flow rate: 125 sccm
ITO	75 or 210 nm	Pressure: 3×10^{-3} Torr Temperature: 200 °C Power: 400 W O$_2$: 0.6 % (0 %)[†]

[a] Silane gas; [b] Phosphine gas; [*] standard cubic centimeter per minute; [†] O_2 different partial pressure to achieve higher sheet resistance; [‡] Post treatment with H_2 plasma at 350 sccm H_2 flow and 58 mW/cm^2 power.

4.1.2 Ag and LiF$_x$/Al deposition

For the deposition of Ag and LiFx/Al stacks, Nanovak thermal evaporator (shown in Figure 4.4) was used. The chamber of the evaporator is capable of reaching the ultra-high vacuum (< 10^{-6} Torr) and has two heating sources. The deposition parameters and thickness of the deposited films are presented in Table 4.2.

Figure 4.4 Nanovak thermal evaporator located inside the glovebox.

Note that for Ag deposition, 99.99 % pure Ag pellets were used. Similarly, for LiF_x and Al, high purity sources (for LiF_x – 99.9 % pure pieces, for Al – 99.999 % pure wire) were used. LiF_x/Al evaporation was performed without breaking the vacuum in the evaporator chamber between LiF_x and Al depositions.

Table 4.2 Deposition parameters used in thermal evaporation of Ag and LiFx/Al.

Material	*Thickness*	*Deposition parameters*
Ag	300 nm	Pressure: < 10^{-6} Torr Deposition rate: 0.1 – 2 Å/s
LiF_x	~1 nm	Pressure: < 10^{-6} Torr Deposition rate: 0.1 Å/s
Al	~150 nm	Pressure: < 10^{-6} Torr Deposition rate: 0.1 – 20 Å/s

4.1.3 Test samples for CS experiments

Four types of samples were necessary to reliably extract ρ_c using CS methods. For these samples, ITO was used as CL. The first type of samples consisted of the structures with confined CL under the circular metal contacts (SCS sample). The second type had full area CL with circular metal contacts (ECS sample). The last two types were TLM samples. Figure 4.5 demonstrates the steps of fabrication of the test samples.

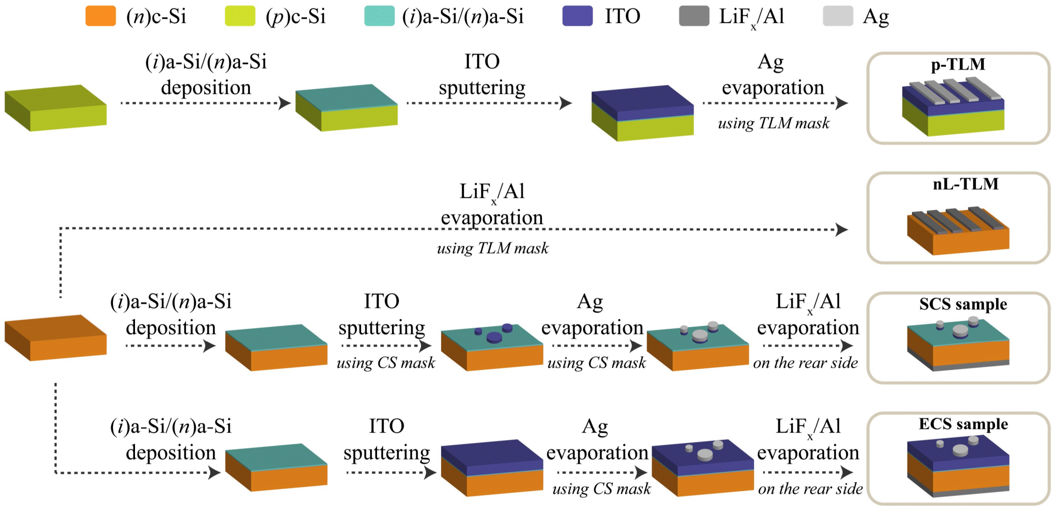

Figure 4.5. Fabrication of the test samples used in CS experiments. Note that the samples have textured surfaces (textured surfaces not shown in the schematic).

For the SCS and ECS samples, one side of (*n*)c-Si wafers was capped with (*i*)a-Si:H/(*n*)a-Si:H stack. The thickness of (*i*)a-Si:H was 7 and 14 nm to achieve ρ_c in two different ranges. Following the a-Si stack deposition, 75 nm of ITO was sputtered. Note that for the SCS samples, the CS mask was taped to the wafers prior to ITO deposition to form confined ITO regions. Following the ITO deposition, ~300 nm of Ag was thermally evaporated using CS shadow masks for both SCS (mask from the ITO deposition step was kept) and ECS samples. As a final step, the backside of the samples received thermally evaporated ~1 nm LiF$_x$/ ~150 nm Al stack.

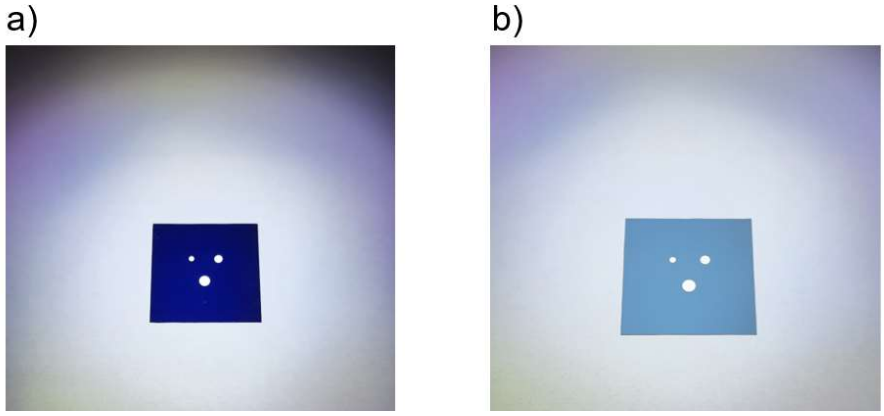

Figure 4.6. Circular metal contacts in test samples used in experiments for (a) Extended CS, (b) Standard CS.

Same stack of (*i*)a-Si:H/(*n*)a-Si:H/ITO/Ag with TLM mask was grown on (*p*)c-Si sample to prepare the TLM samples (p-TLM) for extracting ρ_c of Ag/ITO interface. And finally, to extract ρ_c of (*n*)c-Si/LiF$_x$/Al interface, the same stack was grown on (*n*)c-Si using TLM mask (nL-TLM).

4.1.4 Test samples for 4PP experiments

Figure 4.7 demonstrates the fabrication process of the samples used in 4PP experiments. The test samples for both S4PP and E4PP methods (S/E4PP samples) were fabricated on (*n*)c-Si with (*i*)a-Si:H/(*n*)a-Si:H/ITO and (*i*)a-Si:H/LiFx/Al stacks, both stacks acting as the CL. The thickness of (*i*)a-Si in (*i*)a-Si/(*n*)a-Si/ITO stack was 7 and 14 nm to achieve ρ_c in two different ranges. Moreover, the thickness of ITO was 210 and 75 nm to achieve sheet resistance of 20 and 80 Ω/sq, respectively. Note that no shadow mask was used for the fabrication of S/E4PP samples. Additionally, (*i*)a-Si:H/(*n*)a-Si:H/ITO stack (with aforementioned thicknesses) was deposited on (*p*)c-Si substrates to extract the sheet resistance of ITO (p-4PP samples). The thickness of (*i*)a-Si:H in (*i*)a-Si:H/LiF$_x$/Al stack was 7 nm, LiF$_x$ and Al were ~1 and ~150 nm thick. Note that due to the low sheet resistance of (*i*)a-Si:H/LiF$_x$/Al stack (< 0.38 Ω/sq), no additional sample on (*p*)c-Si was necessary for extracting the R_{CL}.

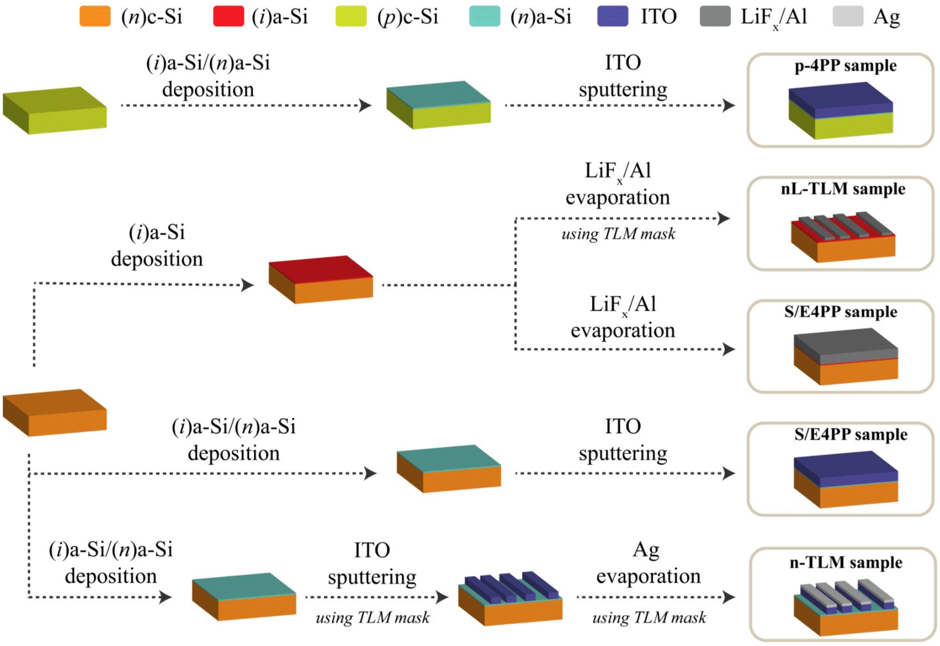

Figure 4.7 Fabrication of the test samples used in 4PP experiments. Note that the samples have textured surfaces (texturing not shown in the schematic).

In addition to S/E4PP and p-4PP test samples, samples containing TLM patterns (Figure 4.8) were fabricated using the same stacks as for the S/E4PP samples on (*n*)c-Si wafers (n-TLM).

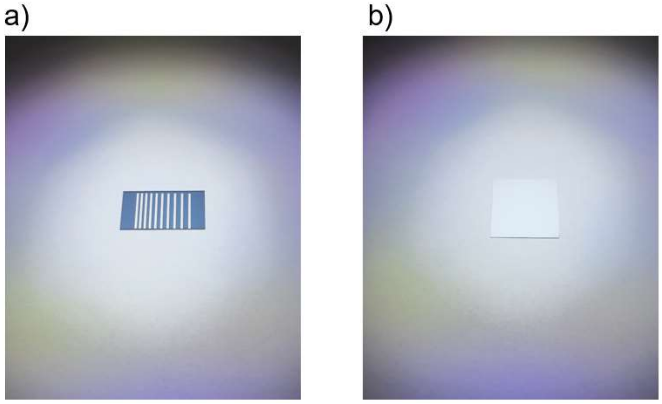

Figure 4.8. Exemplary (a) TLM test sample used in CS and 4PP experiments, (b) test sample for 4PP methods.

4.2 Electrical measurements

To obtain R values for TLM and SCS/ECS test samples, first I-V characteristics were obtained using a Keithley 2425 source meter (Figure 4.9a) and Kelvin probes in a four-wire configuration (Figure 4.9b). Note that TLM samples were contacted from the top using Kelvin probes, whereas SCS/ECS samples were contacted with Kelvin probes from the top and the measurement chuck (Figure 4.9c) from the bottom. The applied voltage varied from -0.2 to 0.2 V, and R values were obtained from the slope of the linear region in the I-V characteristics. To extract the ρ_c from the obtained R values, MATLAB's fitting tools were utilized together with the analytical formulations mentioned in Chapter 2.

To measure the sheet resistances of the S4PP/E4PP samples, Jandel RM3-AR probe station (Figure 4.9d) was used. The probe station had four collinear and equally separated probes with probe separation (s) = 635 μm and probe diameter (p) = 100 μm. Note that for the aforementioned probe station, it is very common to note and record the displayed sheet resistance value; however, in some cases, the output value of the device might not be correct due to the potential change of the correction factor, which is a function of the sample's dimension, s and p. In the following subsection, the aspect of applying the correction factors in 4PP measurements is discussed in detail.

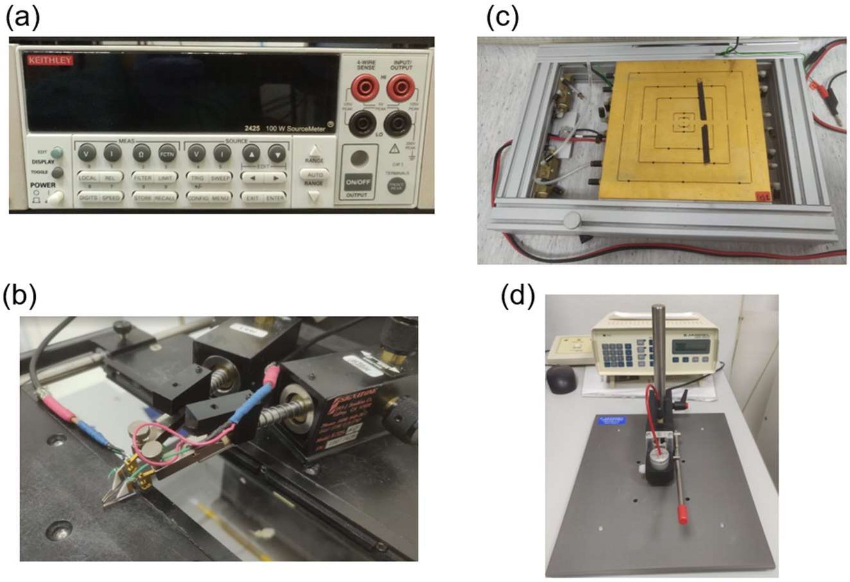

Figure 4.9. (a) Keithley 2425 source meter. (b) Kelvin probes used for measuring the *I-V* characteristics of the TLM samples. (c) Measurement chuck used for contacting CS samples from the backside. (d) Jandel RM3-AR four-point probe station.

4.2.1 Sheet resistance measurement with the 4PP station

In Jandel RM3-AR 4PP station, the sheet resistance is measured by means of supplying current (I_0) from the outer two probes and measuring the voltage difference between the two inner probes (V_{ss}), and applying the correction factor:

$$R_{4PP} = \frac{V_{ss}}{I_0} F_{cor} \tag{4.1}$$

where F_{cor} is the correction factor.

The device is capable of adjusting I_0 and displaying either measured V_{ss} or R_{4PP}. Note that by default, F_{cor} in this probe station is assumed to be 4.53, which is an analytically determined value assuming that [33]:

- a sample is much larger than the probe spacing ($c >> s$),
- probe spacing is much larger than the thickness of the sample ($s >> h$),
- the thickness of the sample is much larger than the diameter of the probes' tips ($h >> p$).

When these assumptions are not met, adjustments to the correction factor should be made accordingly. Various formulations for the correction factors can be found in [33], [37], which take into account the finite dimensions of the sample and the probes. In the scope of this work, F_{cor} was calculated using the formulation from [33], assuming the sample with 2×2 cm^2 area and specifications of the 4PP station mentioned earlier. Moreover, recorded sheet resistance was measured at 15 mV by accordingly adjusting I_0.

CHAPTER 5

RESULTS AND DISCUSSIONS

This chapter includes the simulation and experimental results obtained for the aforementioned ρ_c extraction methods. Additionally, the FGO results are demonstrated and discussed here as well. Note that all simulations, unless otherwise stated, performed in COMSOL had an optimized mesh for the corresponding domains.

5.1 Transfer Length Method

5.1.1 Simulation results

To analyze the effect of the current spreading inside the uncut edges (δ) of the TLM structures, the simulation domain in COMSOL was set up according to the specifications mentioned in Chapter 3.

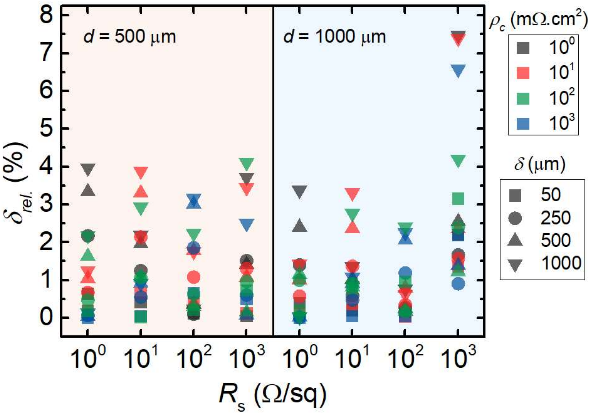

Figure 5.1. Relative error between Eq. 2.14 and COMSOL simulation for d = 500 and 1000 μm, $\rho_c = 10^0, 10^1, 10^2, 10^3$ Ω.cm^2; $R_s = 10^0, 10^1, 10^2, 10^3$ Ω/sq and δ = 50, 250, 500, 1000 μm.

Figure 5.1 demonstrates the relative error between resistance values between two fingers determined by Eq. 2.14 and COMSOL. It can be seen that for R_s (sheet resistance of the layer under the metal fingers) $\delta_{rel.}$ is smaller than 5 %. The error is increased up to ~7.5 % for larger finger spacing (d) and length of the uncut edge (δ) of the structures with $R_s = 10^3$ Ω/sq. The increase in the error for larger d and δ is expected since current spreading is becoming more pronounced as the sample becomes wider and fingers are placed further apart. The error analysis can be further expanded to analyze the corrected resistance taking into account non-zero, i.e., resistance given by Eq. 2.13.

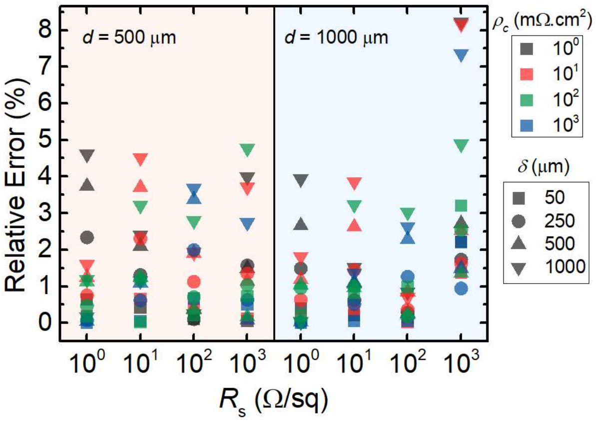

Figure 5.2. Relative error between theoretical resistance (calculated by Eq. 2.14 assuming $R_{//}$ is infinite) value of the TLM structure with $\delta = 0$ μm and corrected resistance given by Eq. 2.13.

As in Figure 5.1, similar trends are observed with the largest error of ~8.2 % observed for $R_s = 10^3$ Ω/sq and $\delta = 1000$ μm. Hence, it can be concluded that the proposed formulation has sufficient accuracy to be used to extract ρ_c from TLM samples with uncut edges.

5.1.2 Discussion

Generally, TLM method is prone to [38], [39] have many sources of error during the fabrication. The dimensions, separation, and thicknesses of the metal fingers might not be fabricated as desired. The mismatches in physical dimensions lead to erroneously extracted ρ_c. Therefore, one should pay careful attention during the fabrication of TLM test samples. To minimize this kind of error, it is common to measure the dimensions of the deposited fingers after the samples are fabricated.

It should also be noted that Eq. 2.13, which calculates the corrected resistance taking into account the uncut edges, is a modified version of the formulation proposed in [19]. In this work, it was found that using original expression of corrected resistance:

$$R' = 2R_{\mathrm{CE}} + \frac{2R_{//}(R_T - 2R_{\mathrm{CE}})}{R_{//} - 2(R_T - 2R_{\mathrm{CE}})} \qquad 5.1$$

yields relative errors above 50 %. It is expected that such large errors lead to more inaccurate results.

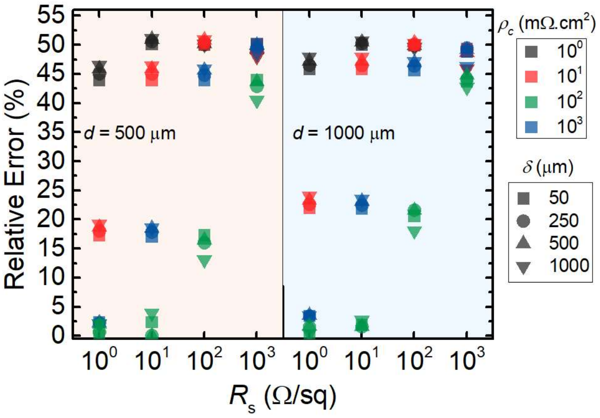

Figure 5.3. Relative error between theoretical resistance (calculated by Eq. 2.14 assuming $R_{//}$ is infinite) value of the TLM structure with $\delta = 0$ μm and corrected resistance given by Eq. 5.1.

5.2 Standard and Extended Cox and Strack methods

In this section, results from COMSOL simulations and experiments for SCS and ECS methods are presented. Additionally, the advantages and disadvantages of the general CS approach are discussed.

5.2.1 Simulation results

Comparing the numerical results with various spreading resistance models in Table 5.1, it can be seen that the "Exact" model [40] has the lowest relative error between analytical and simulation approaches ($\delta_{rel.}$) < 2 % compared to other models. However, implementing this model requires solving the Fredholm integral integration, which is time-consuming and challenging. To decrease the complexity of this model, simpler alternatives (listed in Table 5.1) have been developed. The simplicity of these alternatives, as expected, comes at the cost of accuracy.

Almost all models in Table 5.1 require complicated numerical procedures (e.g., nonlinear equation solving, indefinite integration, implementation of infinite summations), which makes them unattractive for wider use. As it was mentioned in Chapter 2, Turkay et al. [23] have proposed another spreading resistance model for non-confined CS structures, which can be implemented by a user with basic knowledge of the computing software (e.g., MATLAB). The proposed model has $\delta_{rel.} < 3$ % for $\rho_c > 100$ mΩ.cm^2, and the error increases with decreasing ρ_c and b. However, the region where $\delta_{rel.}$ reaches the highest 12 %, is for very small ρ_c and b values, which is irrelevant for solar cell applications.

Table 5.1. Comparison of spreading resistance models in terms of calculation requirements and accuracy.

Model	Duration (sec) of fitting ρ_c from a set of R_0[a]	$\lvert\delta_{rel.}\rvert$ (%)
Exact [40]	> 1000	< 2
Improved Variational [41]	25	< 5
Variational [42]	20	< 8
Schumann & Gardner [43]	1	< 13
Turkay [23]	0.5	< 12

[a] For three values of R_0 with varying top electrode diameter ($2b$). The root mean square error between the numerically calculated R_0 by SRMs, and the input R_0 values were minimized simultaneously for the three diameters, using the nonlinear least-squares method in Curve Fitting Toolbox of MATLAB [32].

5.2.2 Experimental results

As it was mentioned earlier, in SCS/ECS methods, the back contact should have an ohmic behavior. Figure 5.4 demonstrates exemplary *I-V* characteristics extracted from nL-TLM, ECS, and SCS test samples used in the experiments. It can be seen that in the range of -0.03 to 0.03 V, the lines are linear, indicating an ohmic behavior. Note that larger current passes through ECS samples (dash-dotted line) due to the significant spreading occurring inside the conductive layer. Moreover, from Figure 5.5b, it can be seen that ρ_c of (*n*)c-Si/LiF$_x$/Al interface is < 10 mΩ.cm2, which provides a more reliable extraction of ρ_c.

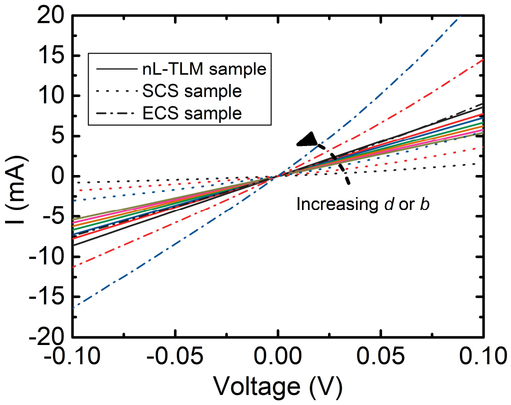

Figure 5.4. *I-V* characteristics of (*n*)c-Si/LiF$_x$/Al TLM sample (solid lines), SCS (dotted line) and ECS (dash-dotted line) samples with (*i*)a-Si:H/(*n*)a-Si:H/ITO/Ag stack.

Since the SCS method has been proven [44] to be reliable in extracting ρ_c from the structures with confined CL, it was used as a control method to verify the newly proposed ECS method. In addition, to fit performed to Eq. 2.16 (red triangles in Figure 5.5a), fitting experimental data was performed in COMSOL (orange triangles in Figure 5.5a) to compare the obtained results. The applicability of the ECS method can be confirmed by the results in Figure 5.5a. SCS and ECS methods yield similar ρ_c's, with SCS resulting in slightly larger ρ_c, which can be attributed to the ITO being deposited with a smaller area than designed due to the presence of the CS masks. Regardless, it can be concluded that the ECS method for the structures with non-confined CL and circular metal contacts is reliable in extracting ρ_c > 100 mΩ.cm^2. Note that reported ρ_c is the combination of ITO/(*n*)a-Si:H/(*i*)a-Si:H/(*n*)c-Si interface without the contribution of Ag/ITO and rear contact interfaces. Both ρ_c's of Ag/ITO and rear contact interfaces were determined using separate TLM samples prepared simultaneously with the ECS test samples. In Figure 5.5b it can be seen both Ag/ITO interface has ρ_c < 5 mΩ.cm^2.

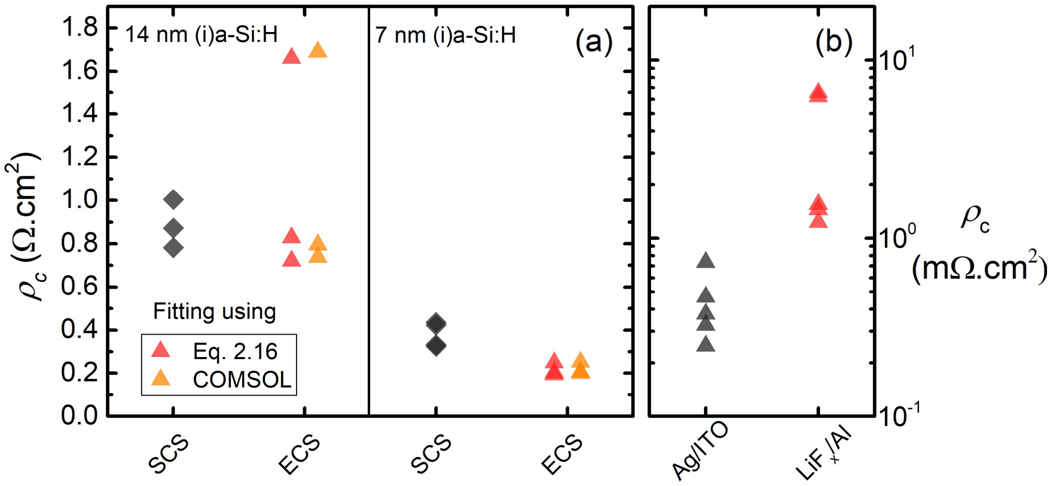

Figure 5.5. (a) ρ_c extracted using SCS and ECS methods using Eq. 2.16 and COMSOL. (b) ρ_c of Ag/ITO and LiF$_x$/Al measured from dedicated samples

5.2.3 Discussion

One of the advantages of the SCS method is the ability to extract lower ρ_c when compared with other methods. The metal contacts with a radius of 0.5 mm are easily contacted without the need for microprobes and microscope; therefore, for such a small radius, *R* is mainly dominated by ρ_c of the interface rather than the resistivity of the bulk. Contrary to the SCS method, the ECS method has worse accuracy due to the current spreading inside the CL, which affects the effective area of the contact (the area through which the current travels due to the presence of a CL). However, the advantage of the ECS method over the SCS method for the same CL of interest is the ease of fabricating the test samples, with ECS not requiring any time-consuming etching techniques.

Both CS methods, however, require an ohmic contact to the rear side of the test samples. This requirement significantly increases the test sample preparation time. Additionally, one needs to ensure that the rear side has ohmic behavior with low ρ_c

(for more reliable extraction of ρ_c of the desired interface), which might require a separate set of experiments optimizing the rear interface's ρ_c.

One of the main sources of error that can arise in applying SCS and ECS methods is related to the fabrication steps. In the course of preparing the test samples for these methods, it was noticed that sputtered ITO in SCS test samples was non-uniform (Figure 5.6), and the resulting circular shape was smaller than the expected size (note that the same behavior occurs for the deposited metal). Consequently, the extracted ρ_c of those samples was significantly overestimated. To eliminate this behavior, the poly-Si masks have undergone chemical treatment (immersion in HNO_3:HF (5:1) for 2 minutes) to reduce their thickness and clean the surface. This step mitigated the unwanted behavior and provided more reliable samples for extracting ρ_c. Overall, while analyzing the extracted results using SCS or ECS methods, in addition to looking for expected trends in the samples prepared under varying conditions, one has to be careful not to overlook other aspects of the fabrication sequence that might introduce the error and overshadow the expected change in the trends.

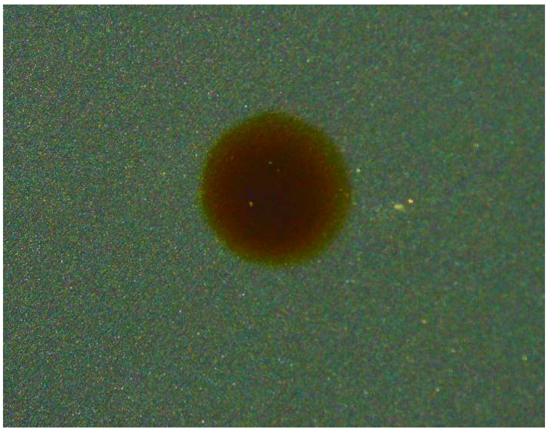

Figure 5.6. Non-uniform coating of ITO under the shadow mask.

5.3 Four-Point Probe Method

This section presents the simulation and experimental results for S4PP and E4PP methods. It is later followed by a discussion about the limitations, advantages, and possible improvements in the resolution of these methods.

5.3.1 Simulation results

Figure 5.7 shows the $\delta_{rel.}$ between the analytically and numerically (using COMSOL) obtained R_{stack} values.

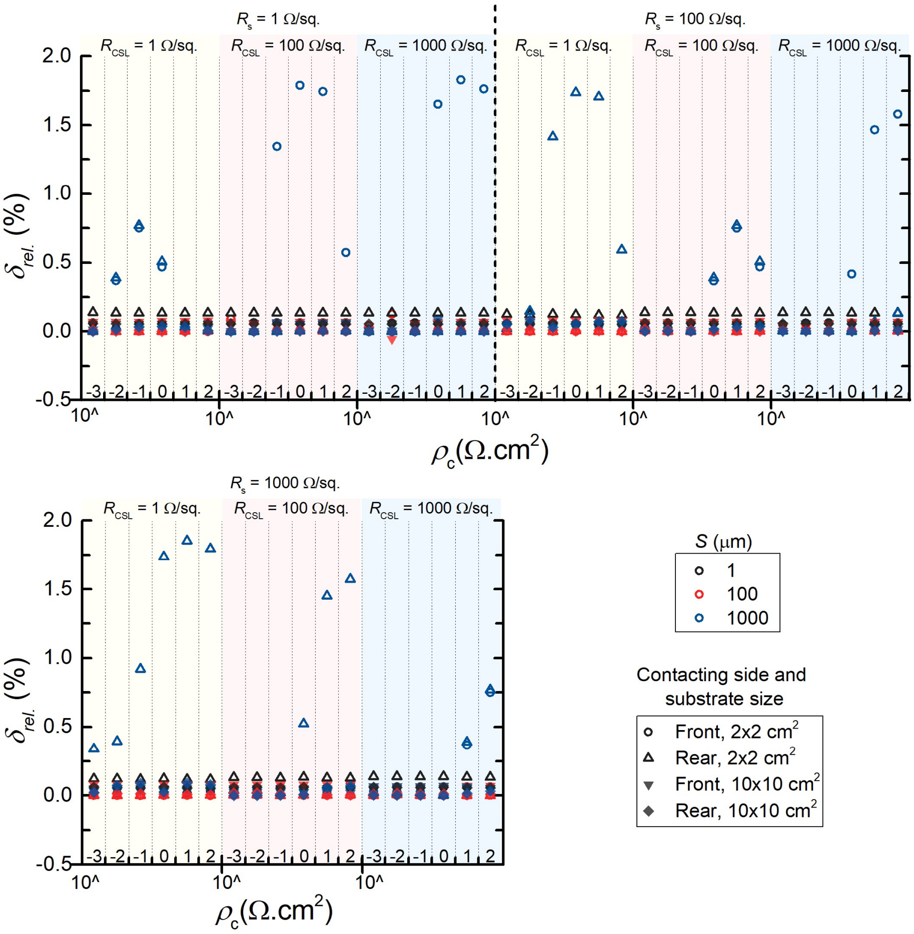

Figure 5.7. $\delta_{rel.}$ between the analytical model and FEM simulations. Front implies probes contacting the CL side; rear implies probes are touching the substrate [28]

It can be noted that for the samples with 10×10 cm^2 area (solid symbols), the agreement between analytical formulation and FEM results is excellent with $\delta_{rel.} <$ 0.1 % for all combinations of interest. For the 2×2 cm^2 samples, $\delta_{rel.}$ gets larger, however, still < 1.9 % for all configurations. The larger deviation is mainly observed with larger probe spacing and large ρ_c. The reason is the fact that the utilized spreading resistance model does not take into account the effect of the finite lateral dimensions of the sample (i.e., c), which becomes more effective on R_{stack} when ρ_c is large ($\rho_c > 1$ Ω.cm^2).

5.3.2 Experimental results

As it was mentioned before, ρ_c extracted using TLM structures was used to verify the validity and accuracy of the proposed S4PP and E4PP methods. Figure 5.8 demonstrates the *I-V* and resistance versus finger spacing results of one of the used TLM samples. ρ_c was extracted according to the methodology presented in Chapter 2.

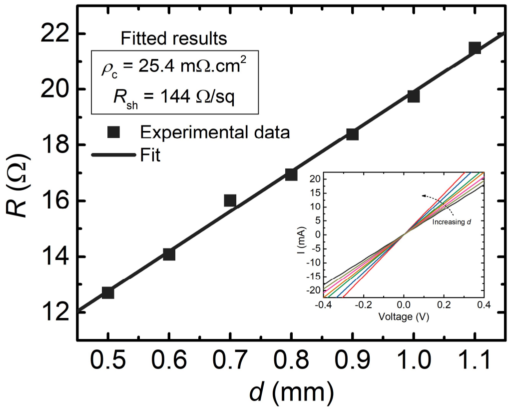

Figure 5.8. An exemplary *R* versus *d* data from a TLM sample (with 7 nm (*i*)a-Si:H/1.5 nm LiF$_x$/150 nm Al) used as a reference. The inset shows the *I-V* characteristics of each *d* in the sample.

Following the same steps, ρ_c from all the TLM samples for 4PP experiments was calculated and compared with ρ_c extracted using S/E4PP. There is a high degree of agreement between ρ_c extracted using the two methods, as shown in Figure 5.9. It should be noted that for the S4PP method, ρ_c can be extracted from the measurements made from either side of the sample since R_{CL} is known. ρ_c extracted from these measurements should yield similar results; however, it can be seen in Figure 5.9 that there is a difference between ρ_c extracted when the sample is contacted from ITO and Si sides. This deviation arises from the differences of extracted sheet resistance of ITO from the p-4PP sample and the actual sheet resistance deposited on (*n*)c-Si sample; and the higher sensitivity of the S4PP method on extracted results when the sample is contacted from the ITO side [28]. However, it can be seen that ρ_c extracted using S4PP contacted from Si side, E4PP and TLM agree closely with each other.

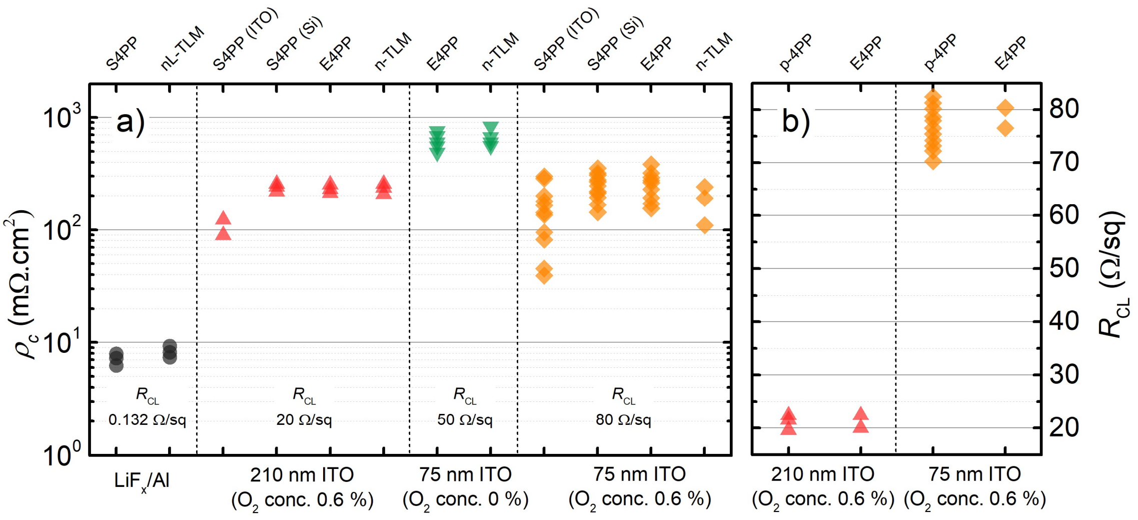

Figure 5.9. (a) Comparison of ρ_c extracted using E4PP, S4PP, and TLM methods. (b) RCL of ITO extracted using p-4PP samples and E4PP method [28].

Additionally, Figure 5.9b demonstrates the sheet resistance of ITO extracted using p-4PP samples and the E4PP method. From the high degree of agreement between these two methods, it can be concluded that the E4PP method is capable of reliably extracting the sheet resistance of ITO (hence of the CL).

5.3.3 Discussion

One of the main advantages of the 4PP methods is the simplicity of fabricating the test samples. As shown in Figure 4.7, the fabrication of the test samples for 4PP methods includes only one step. Moreover, there is no need for etching or shadow masking during the deposition of the CL, which eliminates the potential source of error arising from the difference between the designed and actual dimensions of the deposited patterns. Additionally, the measurement of the samples and ρ_c calculation takes significantly less time than any other method discussed in this thesis (provided that the methodology mentioned in [28] has been implemented in the computational software). The advantage of the E4PP method over the S4PP method, as mentioned earlier, is the ability of the E4PP method to extract both ρ_c and R_{CL} from a single sample, not requiring additional test samples for R_{CL} measurement as in the S4PP method.

While many aspects make 4PP methods attractive and superior to others, one cannot extract any information about the contact stack behavior, i.e., whether there is an ohmic or rectifying behavior. Up to now, ρ_c of interfaces with only ohmic behavior was determined, and there has not been any analysis done of interfaces with rectifying behaviors. The extraction of ρ_c of such interfaces can be a subject of another study.

The range of ρ_c extracted with S4PP, in the scope of this work, is between 2×10^{-3} and 5 Ω.cm^2, which is relevant to the development of silicon solar cells with heterocontacts. However, it is also possible to adapt the S4PP method to measure low ρ_c values by reducing the spacing between the probes and/or increasing the sheet resistance of the CL and the bulk. This follows from the sensitivity analysis that was performed in [28].

Another aspect that has not been studied in the scope of this work is the damage induced by the 4PP station to the deposited CL. This damage occurs due to the pressure applied by the probes on the sample. In this work, the thickness of the sputtered ITO was 75 and 210 nm. It is likely that ITO layers with these thicknesses have been slightly damaged while measuring R_{stack} with 4PP station. While no significant effect on the extracted R_{CL} and ρ_c was observed in the performed experiments, one should be aware that there is a possibility of a change in the electrical properties of the interface once the sample is probed for the sheet resistance measurement. However, the extent of how much (if at all) the quality of the interfaces CL itself can change is unknown and more research is required in this regard.

5.4 Front Grid Optimization

5.4.1 Simulation results

The validity of the approach to calculating the R_{series} of the solar cell without simulating the full operating device is depicted in Figure 5.10. R_{series} calculated by Eq. 3.1 and generated by COMSOL is plotted versus L_{TCO} for $R_{\text{TCO}} = 100\ \Omega/\text{sq}$ (thickness of the TCO is 100 nm). It can be seen that there is an excellent agreement between the analytical and numerical approaches. Hence, using the high resistive layer between the TCO and the bottom contact can successfully represent the solar cell operation under illumination.

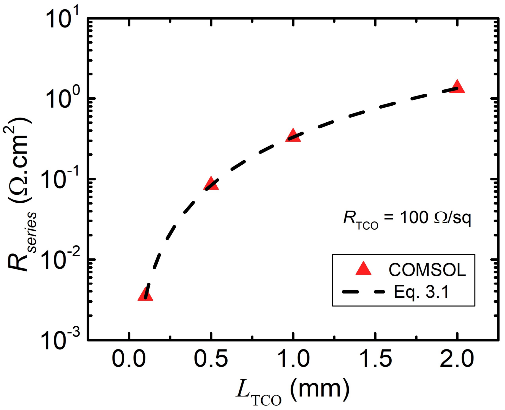

Figure 5.10. R_{series} versus L_{TCO} calculated using Eq. 3.1 (dashed line) and COMSOL (triangles).

Extending the simulation domain to 3D and implementing the grid design depicted in Figure 2.7, R_{series} was determined and used to calculate the potential efficiency of the solar cells with the proposed grid design.

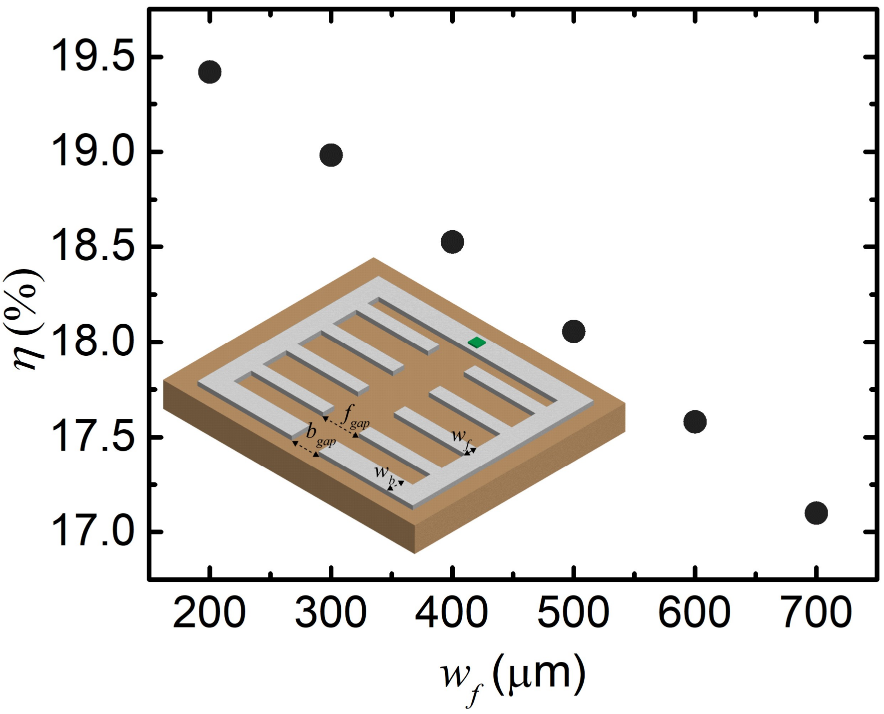

Figure 5.11. η versus w_f for the with 3 fingers, w_b = 2 mm, f_{gap} = 2 mm, b_{gap} = 1mm. The inset demonstrates the structure for simulations.

In Figure 5.11, the linear decrease of efficiency with increasing w_f can be observed. This relation implies that the resistive improvements with increasing w_f stay insignificant relative to the shadowing losses. Therefore, it can be concluded that choosing $w_f = 200$ µm, which is a limitation imposed by the fabrication steps, would yield the optimum value among other available w_f. Note that the linear trend between η and w_f is present regardless of the number of the fingers, w_b, f_{gap}, and b_{gap} since the minimum available w_f is 200 µm, at such high values, the shadowing losses are dominant over the R_{series} gains. To observe the resistive gains overcome the J_{sc} losses, w_f should be decreased to tens of µm.

Following the optimization of w_f, the effect of w_b on the performance of the solar cells was investigated. Note that w_b has no effect on the shadowing fraction of the grid and hence can be optimized only in terms of R_{series}. From Figure 5.12, it follows that making w_b as large as possible reduces R_{series} and consequently increases the efficiency. Due to the size limitation of the available wafers, $w_b = 2$ mm was chosen for the further optimization steps.

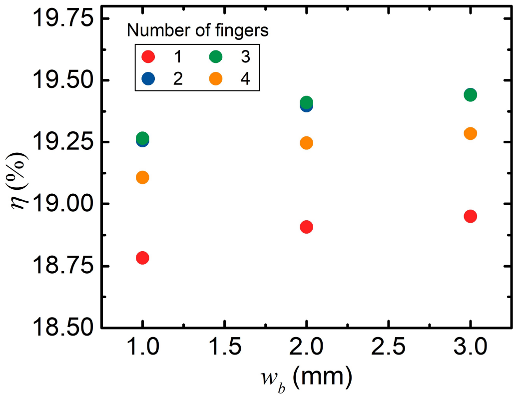

Figure 5.12. η versus w_b for different number of fingers with $w_f = 200$ µm, $f_{gap} = 2$ mm, $b_{gap} = 1$ mm.

With the fixed w_f and w_b, the number of the fingers has been changed from 0 to 4. Figure 5.13 demonstrates the change in the efficiency as the number is increased. Maximum efficiency of ~19.41 % is achieved for the grid design with 3 fingers. The reason for the existence of a maximum is the trade-off between the resistive gains and shadowing losses as the number of fingers is increased. With more fingers, the generated charge carriers have more potential paths to the terminal; however, the generation of the carriers itself decreases since a larger area of a solar cell is shadowed by the metal.

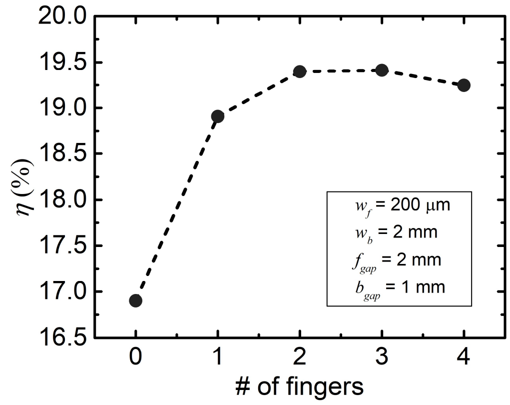

Figure 5.13. η versus number of fingers.

5.4.2 Discussion

As it was mentioned in Chapter 2, there are infinitely many possible designs for the front grid that can enable high-performing solar cells. Most of the time, however, fabrication processes impose limitations on the designs. Like in this work, the limitation for the grid was the maximum available metal thickness. Generally, the widely used screen-printing metallization technique is capable of fabricating grids almost seven times thicker (~20 μm) and much narrower fingers (~ 40 μm) [45], [46]. With these design limitations, however, another optimization analysis should be performed because the optimum parameters will most likely change. For example, if the grid design in Figure 2.7 were 20 μm thick, then the optimum number of fingers would most likely change to a smaller number due to the lower line resistance of the deposited metal. Overall, the optimum performance of the various grid types will be obtained at different geometrical properties determined by FGO, and the same optimized point should not be applied to other design specifications.

Moreover, in this work, FGO was performed only by considering R_{series} and losses in J_{sc} due to shadowing. However, there are solar cell structures in which the passivation quality (hence V_{oc}) may change depending on the grid design. For example, in solar cells with passivated emitter rear contact (PERC) [47], [48], the front grid undergoes firing (which allows contact to highly doped region). While firing allows interface with lower ρ_c, the passivation quality near and under the fired regions degrades, reducing the performance of the solar cells. Therefore, in PERC solar cells, an additional parameter (passivation) should be considered together with R_{series} and shadowing fraction while performing FGO. For such a purpose, the methodology utilized here is not sufficient because it assumes that the metal grid has no effects on the passivation quality of the solar cells. Therefore, additional simulation tools such as GRIDDLER [49] should be utilized where such effects can be taken into account.

CHAPTER 6

CONCLUSION

Due to the inability to directly measure the contact resistivity of an interface, various indirect methods have been developed. In this thesis, classic methods such as Transfer Length (TLM) and Cox and Strack (CS) methodologies have been discussed. Additionally, a recently proposed four-point probe method was described. Important modifications have been developed for standard Cox and Strack (extended Cox and Strack, ECS) and four-point probe (extended four-point probe, E4PP) methods, which allow more convenient fabrication and faster calculation of the contact resistivity. The development of the modified methods was performed in three steps. Firstly, an analytical formulation for determining the total resistance of the structure of interest was derived. Then, the accuracy of the formulations was cross-checked with finite element method simulations. Finally, new methodologies were verified by determining the contact resistivity of the fabricated test samples.

Finite element simulations were performed in COMSOL Multiphysics software. The relative error for the ECS method between analytical and FEM approaches below 3 % is reported. For E4PP, the relative error is below 1.9 %. These values are sufficiently low for determining contact resistivity of the interfaces relevant to the development of the solar cells. Test samples utilizing amorphous Si (intrinsic and phosphorous doped) and indium tin oxide stack, LiF_x/Al stack were fabricated to verify the accuracy of the E4PP and ECS methods. Good agreement between standard Cox and Strack and ECS, E4PP, and TLM methods has been obtained, indicating their validity.

Moreover, COMSOL and MATLAB were utilized to determine the optimum front grid metal design for heterojunction solar cells. With the limitations imposed by the fabrication techniques, a front grid with three fingers was found to be the optimum combination.

6.1 Outlook

Contact resistivity of the metal-semiconductor interfaces remains a crucial parameter in limiting the performance of any electronic device. The optimization of this parameter would be more efficient if simpler and faster methods of measuring contact resistivity were developed. Despite the methods described in this thesis being widely used, there is still room for further modifications in characterizing the contact resistivity of the metal-semiconductor interfaces. For example, all of the aforementioned methods require separate samples to determine the contact resistivity. However, the qualities of the investigated materials can be different in the operating device as opposed to in test samples for contact resistivity measurements. Therefore, methods that can determine contact resistivity non-destructively and can be directly performed on the fully operating devices are of great value. As an example in [50], a non-destructive, fast, and industry-feasible method for locating the regions with locally high series resistance is proposed. This method, however, does not provide the absolute values of series resistance but instead identifies the regions across the sample with higher series resistance. Therefore, there is still room for improvement for the method in [50]. Overall, the research and development of electronic devices will only benefit in terms of material and time consumption when more efficient and accurate methods of extracting contact resistivity are further explored.

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