AN ADAPTIVE CONVERTER FOR CONSTANT CURRENT STIMULATORS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MERT KOÇ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2021

Approval of the thesis:

AN ADAPTIVE CONVERTER FOR CONSTANT CURRENT STIMULATORS

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ABSTRACT

AN ADAPTIVE CONVERTER FOR CONSTANT CURRENT STIMULATORS

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September 2021, 82 pages

Functional electrical stimulation (FES) has been used to remedy neurological or physiological ailments for many years. Several methods for functional electrical stimulation exist, among which constant current stimulation is adopted by many devices thanks to its safety and charge control. One of the most successful among these devices is the cochlear implant. More than 120.000 people use them to improve the quality of their lives. In the last decade or so, the amount of research done to fully implant these cochlear implants has increased dramatically. To comply with the requirements of such a fully implanted device, rigorous specifications are necessary. One of the most important among these specifications is related to power consumption. Due to weight and volume restrictions the device must operate with ultra-low power. This, however, is quite difficult due to the necessity of high voltage compliance that is required for constant current stimulation. The high voltage must be generated with a converter circuit, which further degrades the efficiency of the system. To alleviate these issues an adaptive converter is designed in this thesis. The system tracks the voltages of an 8- channel stimulation electrode array. Accordingly,

with the utilization of a 3-stage charge pump, the necessary supply voltage for the stimulator ranging from 1.8 V to 5.5 V is generated. This way up to 35% power dissipation reduction is observed within the neural stimulator compared to when the converter is operating in its constant 5.5 V configuration, resulting in a much more efficient overall system.

Keywords: Functional Electrical Stimulation, Compliance Voltage, Charge Pump, Efficiency, Voltage Tracking

ÖZ

SABIT AKIM STIMÜLATÖRLER İÇİN UYARLANABILIR BIR DÖNÜŞTÜRÜCÜ

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Tez Yöneticisi: Prof. Dr. Haluk Külah

Eylül 2021, 82 sayfa

Fonksiyonel elektrik stimülasyonu (FES), nörolojik veya fizyolojik rahatsızlıkları gidermek için uzun yıllardır kullanılmaktadır. Fonksiyonel elektrik stimülasyonu için farklı metodlar mevcuttur, ki bunlar arasından güvenliği ve şarj kontrolü sayesinde sabit akım stimülasyon birçok cihaz tarafından benimsenmiştir. Bu cihazlar arasında en başarılı cihazlardan biri koklear implanttır. 120.000'den fazla kişi bu cihazları yaşam kalitelerini artırmak için kullanıyor. Son on yılda, bu koklear implantları tamamen implante etmek için yapılan araştırmaların miktarı önemli ölçüde artmıştır. Bu tür tamamen implante edilmiş bir cihazın gereksinimlerine uymak için, titiz spesifikasyonlar gereklidir. Bu özelliklerden en önemlilerinden biri güç tüketimi ile ilgilidir. Ağırlık ve hacim kısıtlamaları nedeniyle cihazın çok daha düşük güçle çalışması gerekir. Ancak bu, sabit akım uyarımı için gerekli olan yüksek voltaj uyumluluğunun gerekliliği nedeniyle oldukça zordur. Bu yüksek voltaj, sistemin verimliliğini daha da düşüren bir dönüştürücü devre ile üretilmelidir. Bu sorunları hafifletmek için bu tezde uyarlanabilir bir dönüştürücü tasarlanmıştır. Sistem, 8 kanallı bir stimülasyon elektrot dizisinin voltajlarını izler. Buna göre 3 kademeli şarj pompası kullanımı ile stimülatör için 1.8 V ile 5.5 V aralığında gerekli besleme gerilimi üretilir. Bu şekilde, dönüştürücü sabit 5.5 V konfigürasyonunda

çalıştığı zamana kıyasla nöral stimülatörde %35'e varan güç kaybı azalması gözlemlenir ve bu da çok daha verimli bir genel sistem sağlar.

Anahtar Kelimeler: Fonksiyonel Elektrik Stimülasyonu, Uyum Gerilimi, Şarj Pompası, Verim, Gerilim Takibi

To my father

ACKNOWLEDGMENTS

Firstly, I would like to express my sincerest gratitude to Prof. Dr. Haluk Külah for his supervision, guidance and support. I am forever greatful for being given the opportunity to be a part of an amazing group of people.

I would like to thank Assoc. Prof. Dr. Yeşim Serinağaoğlu Doğrusöz, Prof. Dr. Ali Muhtaroğlu, Assoc. Prof. Dr. Serdar Kocaman and Assoc. Prof. Dr. Dinçer Gökcen for sparing their valuable time to be a part of my thesis jury.

I would like thank Dr. Salar Chamanian, Dr. Hasan Uluşan and Dr. Aykan Batu for their guidance and experiences.

I would also like to thank BioMEMS Research Group members, Andaç, Yasemin, Akın, Berat, Berkay, Özlem, Abdurrahman, Anıl, Aziz, Zeynep and Mert.

This work has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant No:682756)

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ABBREVIATIONS

SC: Switched-Capacitor

SSL: Slow Switching Limit

FSL: Fast Switching Limit

PFM: Pulse Frequency Modulation

CHAPTER 1

INTRODUCTION

1.1 Motivation

Since the first fully electrical based stimulator was reported in the 1930s, neural and muscular stimulation has been utilized to treat neurological and physiological issues [1]. Thanks to further advances in technology, devices using stimulation such as cochlear implants [2], deep brain stimulators [3], and epiretinal stimulators [4] emerged to improve the quality of human lives. Cochlear implants, for example, are a successful group of stimulation devices and enabled hearing for more than 120.000 deaf people [5].

Several stimulation modes exist: voltage mode, charge mode and current mode [1]. Voltage mode, also called voltage-controlled stimulation (VCS), is the most efficient. However, poor control on the amount of charge delivered to varying electrode load makes it such that it is rarely used as it can lead to safety issues [1]. Charge mode, or switched-capacitor stimulation (SCS), enables accurate control on the amount of charge delivered and also achieves high efficiency. However, the large capacitors needed for this method make it unappealing for implantable or multi-channel systems. Current mode, or constant current stimulation (CCS), is the most popular method due to its ability to control the amount of charge delivered, safety, and wide load range. The drawback for this method, however, is its low efficiency [1].

As the name suggests, CCS method passes a constant current through the electrode to stimulate the target areas. A simple illustration for this method is shown below in Figure 1.1 [6]. Also shown in this figure is the generated biphasic current. Current is

passed from the common electrode in the cathodic phase and to the common electrode in the anodic phase. As the stimulators are generally implanted, the electrodes used for stimulation are small, which increases the impedance of the electrode-tissue interface [7]. Thus, taking into account the maximum possible load impedance and stimulation current, high voltage compliance is necessary [7]. This necessity is actually what causes the current mode stimulation to have lower efficiency. In fact, different stimulation sites will most definitely have different impedances due to human error during implantation of the electrodes. Additionally, subsequent stimulation pulses may have different magnitudes as is the case for amplitude modulated stimulators [8]. Thus, the highest possible voltage compliance that accomodates for the highest current and load will not always be necessary and cause decline in efficiency. For example, for a load of 8 kΩ and a stimulation current of 1 mA, the potential on the load will be 8 V. Thus, taking into account the voltage overhead needed for the current drivers, the minimum supply should be higher than 8 V, and is chosen to be 10 V for this instance. However, when the magnitude of the current drops to 200 μA, the potential across the load will be 1.6 V. In case the stimulator's supply is still 10 V, as was necessary for the previous case, the excess voltage overhead in the second scenario will be dissipated on the current drivers, which is unnecessary power loss.

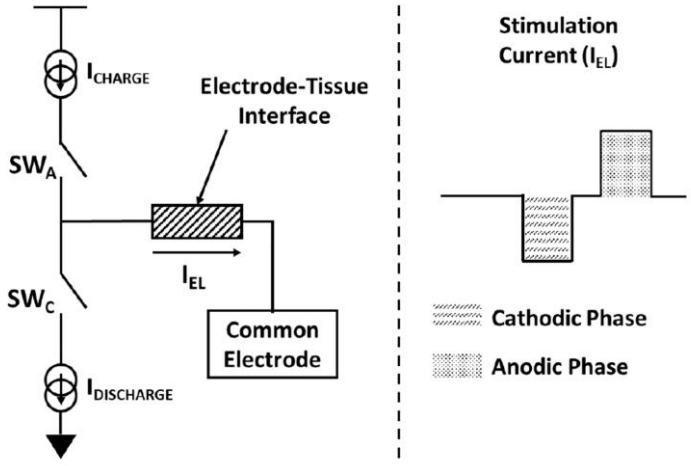


Figure 1.1. Simple illustration of CCS method [6]

Moreover, there are a number of examples that try to create ultra-low power stimulator devices [8], [36]. However, when the power budget of these systems are analyzed, it can be seen that the stimulator part is still the hungriest part. Thus, taking into consideration the inefficient nature of constant current stimulation and the fact that it consumes the most amount of power, extremely efficient implementations that create the necessary higher level voltages must be established.

The generation of these higher level voltages can be accomplished in different ways. Some utilize wireless power transfer [3], [9]-[11], while some utilize batteries to establish the necessary voltage levels [12]. However, efficiency is where these different implementations meet. This thesis aims to design a high voltage generator for a Fully Implantable Cochlear Implant (FICI) interface circuit that utilizes current mode stimulation in accordance with FLAMENCO project. Low efficiency problem of constant current stimulation is used as motivation and a method for adaptive voltage generation is implemented.

1.2 High Voltage Generator

The necessity of high voltage compliance brings the question of how this high voltage will be generated. There are examples that utilize wireless power transmission and create the necessary voltage level with some sort of rectification [9]. For FLAMENCO project, however, in addition to piezoelectric energy harvesting [33], wireless power transmission is intended to be used as a means of recharging the implantable battery that will be utilized [14]. As batteries have lower levels of voltages, a DC-DC converter is needed. Linear regulators can only perform step-down operation, which only leaves the option of switching power supplies. Depending on the type of active element, the switching power supply can be inductive [15]-[17], capacitive [13], [18]-[23] or mixed [24]-[26]. By utilizing off-chip components with high quality factors the inductive based converters can achieve high efficiency across a wide range of output voltages when used in moderate to high power (>100mW) applications [27-28], but, the sizes of these off-chip components

make them unsuitable for implanted devices. There are studies that focus on fully integrating the inductor-based converters [16-17], however, the necessity of costly additional fabrications steps, low quality factor and area overhead are important obstacles in this endeavor. Additionally, electromagnetic interference (EMI) concerns that arise considering that wireless power transmission and piezoelectric energy harvesting will take place within the system make the capacitive based converters more attractive for the application. Switched-capacitor converters are comprised of switches and capacitors only, both of which are easy to implement in CMOS technologies [29]. Moreover, thanks to scaling of the technology, integrated capacitors have high capacitance density [27].

The need for the stimulation system operating at minimum power consumption has already been emphasized. Accordingly, there are several capacitive based high voltage generators from the literature that concentrate on this issue. As shown in Figure 1.2, the system in [13] employs a 4-stage cross-coupled charge pump. The system utilizes a 10 kHz clock to create a 12.8 V output from 2.8 V input. Regulation of the output voltage with varying load is accomplished with an LDO that is connected between the input voltage and the input of the charge pump core as shown in Figure 1.2. This way, the input voltage of the charge pump is varied between 2.56 V to 2.64 V so that the output can be regulated at 12.8 V for a load range of 0 to 2 mA. The drawback of this system, however, is that because the clock frequency is quite low, the pumping capacitors are of greater value. In this case they are 1 μF as is the value of the output capacitor and they are implemented with external SMD capacitors. This, of course, is unwanted for scenarios where volume overhead is important. Similarly, [18] also utilizes multi-stage charge pumps that create ±9 V and -2.7 V output voltages with on-chip capacitors only, however, as the amount of capacitance is low and the maximum load current is high, the efficiency of all these charge pumps is in the range of 60%, which is quite low.

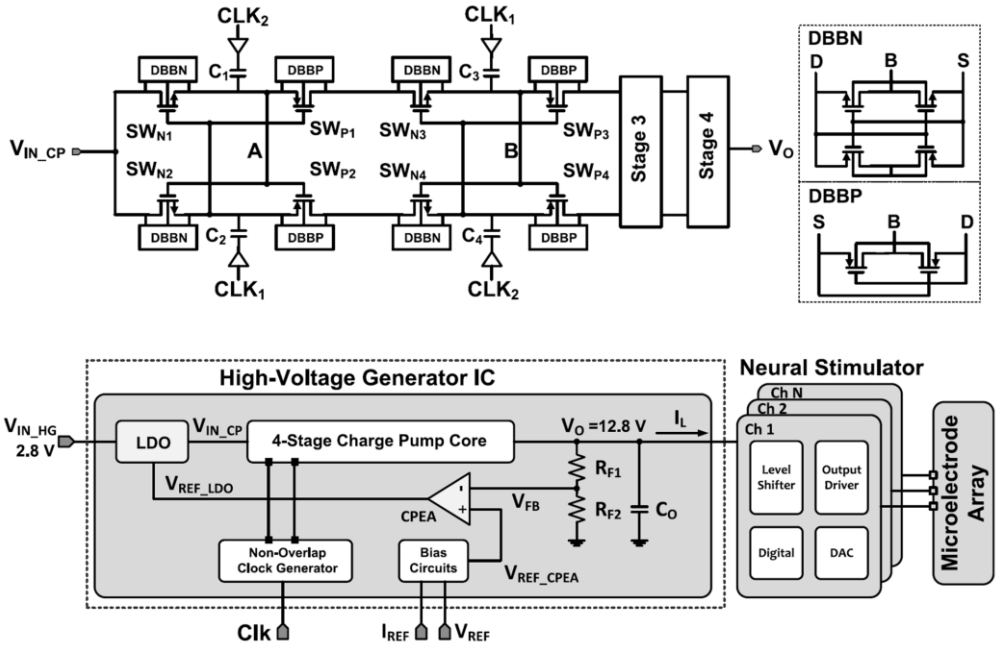


Figure 1.2. Charge pump and block diagram of the system in [13]

There are other similar examples that utilize multi-stage charge pumps to create a constant high voltage [12], [19]. However, research that focuses on another aspect of stimulators to improve the efficiency of these high voltage generators also exists. That aspect is the varying compliance voltage requirement of the stimulator. Figure 1.3 (a) presents the three-element model of the stimulation electrode neural tissue interface [30], where R_{leak} is ignored due to its greater value. Figure 1.3 (b), on the other hand, shows an example stimulation current that is passed through the electrodes and the resulting potential difference between them. According to the model, V_{MAX} can be calculated with equation (1.1).

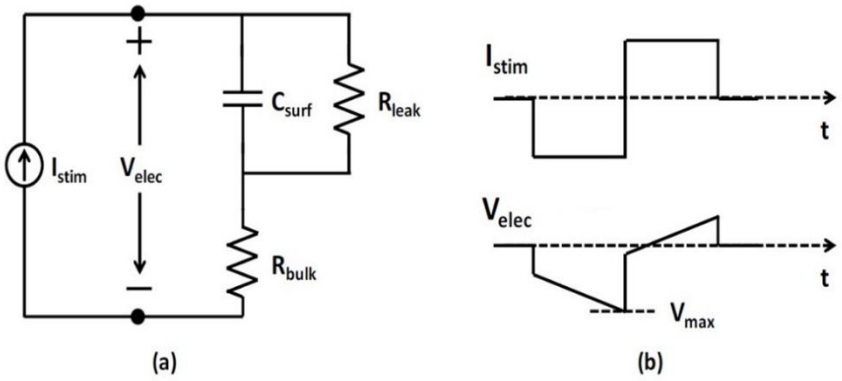


Figure 1.3. (a) Electrode impedance model (b) example stimulation current and resulting electrode potential difference

$$V_{MAX} = I_{STIM} * R_{bulk} + \frac{1}{C_{surf}} * \Delta t * I_{STIM} \quad (1.1)$$

Thus, V_{MAX} will change corresponding to the magnitude of the stimulation current and the impedance of the electrode-tissue interface as illustrated in Figure 1.4 (a). As V_{MAX} drops for lower and moderate current levels and/or electrode impedances, the required high supply voltage reduces as well. For a constant supply this causes unnecessary power loss as the excess voltage is dissipated on the output drivers that provide the stimulation current. If the supply were to be adapted according to the required voltage compliance as shown in Figure 1.4 (b), unnecessary power loss will not occur and the efficiency of the system will increase. The idea is similar to the DVFS feature that is utilized in processors to reduce power dissipation by altering the voltage and frequency [51], [52].

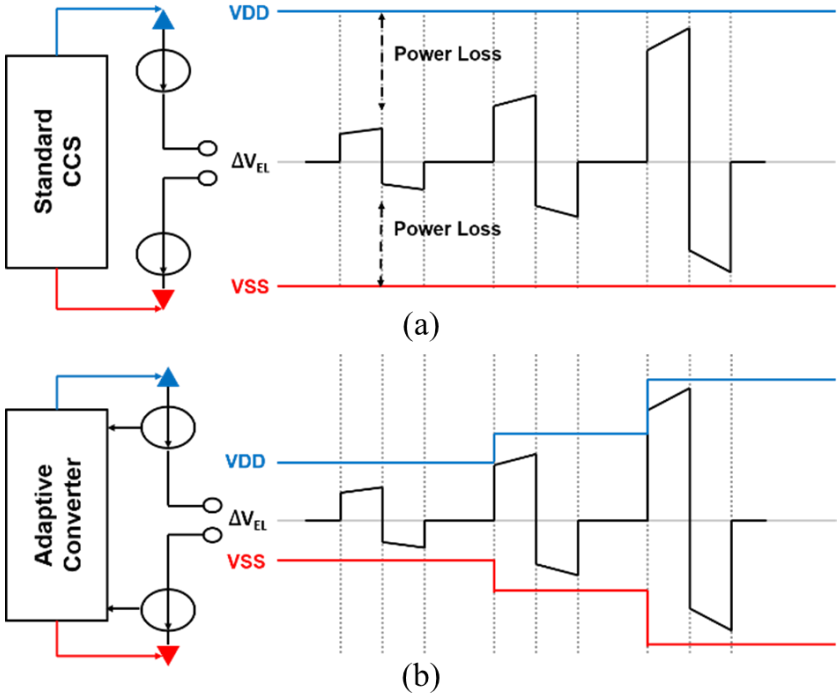


Figure 1.4. Example waveforms for constant current stimulator and (a) constant supply voltage (b) changing supply voltage

[20] works on adapting the supply voltage as explained above. The block diagram of the system is shown in Figure 1.5. Targeted stimulation current is 40 µA, V_{DD} is 3.3 V and the high voltage generator is a 4-stage cross-coupled charge pump making a high voltage of 16.5 V possible under no load conditions. The stimulation current is copied with Mn4 and Mn5 so that V_a becomes V_{DD} - I_{mirror} x R1. The other voltage V_b that V_a is compared to is $V_{DD}/2$. Thus, R1 is configured as 41.25 kΩ. According to the output of comparator C1, the charge pump starts/stops pumping and the supply is adapted by monitoring the stimulation current and keeping it around the targeted value. However, for multi-channel systems or in cases where the stimulation current must be changed, R1 must be changed as well, which is a disadvantage.

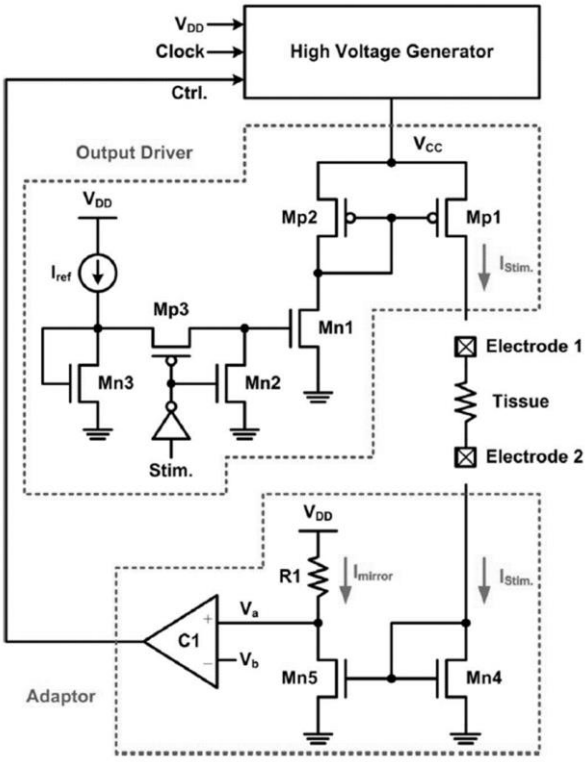


Figure 1.5. Block diagram of the system in [20]

In [31], the stimulation current is compared to a reference current and the supply is again adjusted accordingly. As shown in the system's block diagram in Figure 1.6, the current that is passed through the stimulation electrodes is sensed and compared to the reference current that is received from the FPGA. According to the output of the comparator, the supply excess/shortage monitor counts down/up the 3-bit counter inside the global VDD controller. Thus, the charge pump adjusts its output with 3-bit resolution. However, the usage of an external controller and the fact that the charge pump can only output discrete voltage levels can be considered as a drawback due to fast transients on the electrode voltages. Additionally, the average voltage level can be decreased by allowing the converter to take a continuous range of values.

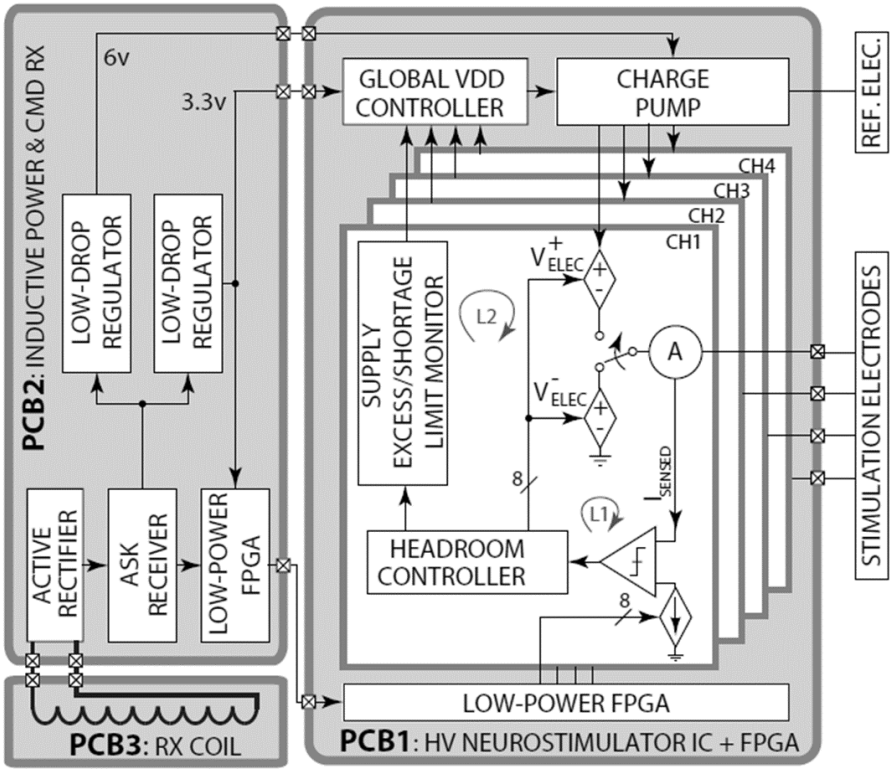


Figure 1.6. Block diagram of the system in [31]

There are also quite a few number of patents on adapting the supply according to the voltage compliance of the stimulator. Similar to the ones above, the method in [34] also operates by sensing the stimulation current and then creating a digital representation of the required supply to adjust the inductive converter. Figure 1.7, on the other hand, shows the schematic diagram for the method presented in [32]. The pair of current sources are utilized to sink and source current from the neural load. When in need of high voltage compliance, the electrodes are connected to a current source and sink with positive and negative supply, respectively. This way the total supply is configured to be 2V. In case of low voltage compliance, one of the electrodes is connected to ground and the other one is connected to the source in one phase and sink in the other so that the supply is V. Again, for this method the supply can take two values. Additionally, the method for determining the distinction for low and high voltage compliance is not described.

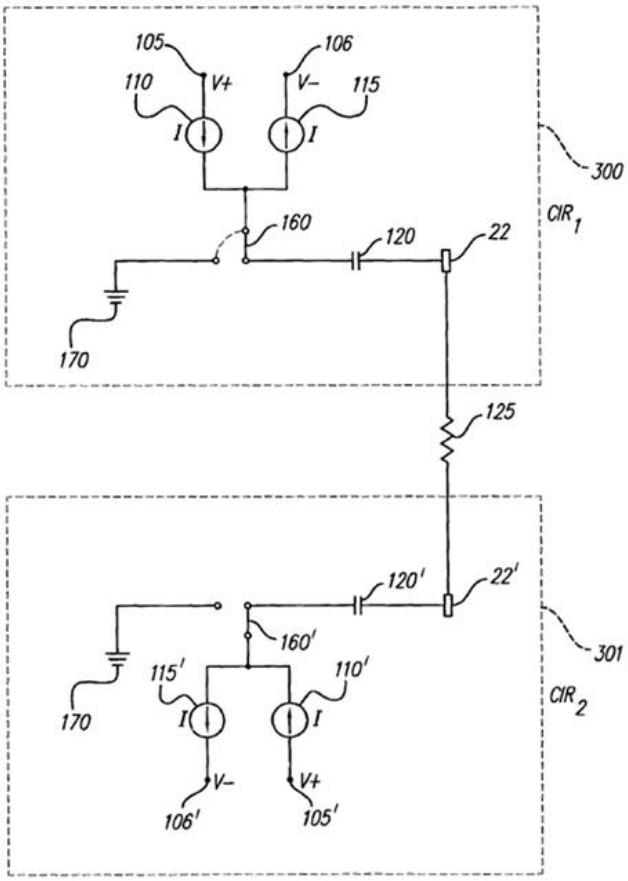


Figure 1.7. Schematic figure for the method presented in [32]

Meanwhile, the system in [49] utilizes complex algorithms to determine the optimum supply voltage for the stimulator. An example algorithm presented in the work is shown below in Figure 1.8. In order to carry out this flowchart complex circuitry is needed. Moreover, the system could work for multi-channel devices. However, in cases where amplitude modulation of the stimulation current is carried out quickly, in cochlear implants for instance, the system will not be feasible.

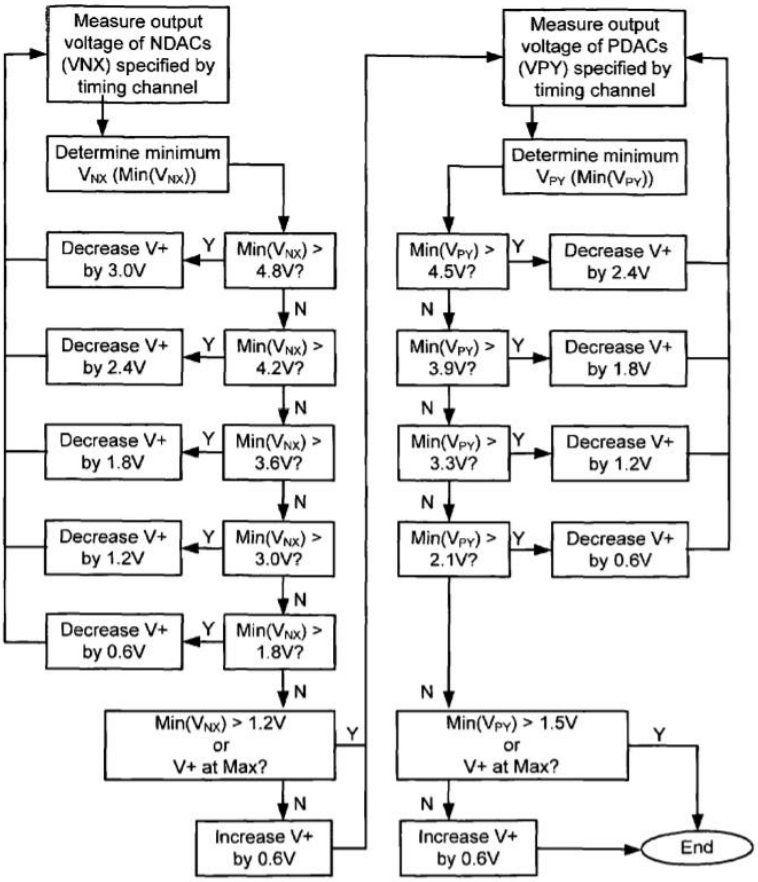


Figure 1.8. An example algorithm from the work in [49]

In contrast to the other implementations so far, the method in [1] adjusts the stimulation current instead of adapting the supply. As shown in Figure 1.9, if the high voltage monitoring block recognizes that the electrodes' potential difference is smaller than a predefined value, the following stimulation current's parameters are adjusted. Modification can be done to the shape, pulse width, amplitude etc. To accomplish this, however, complex circuitry is needed. Moreover, information from the previous stimulation period is used, which will not be feasible for multi-channel systems.

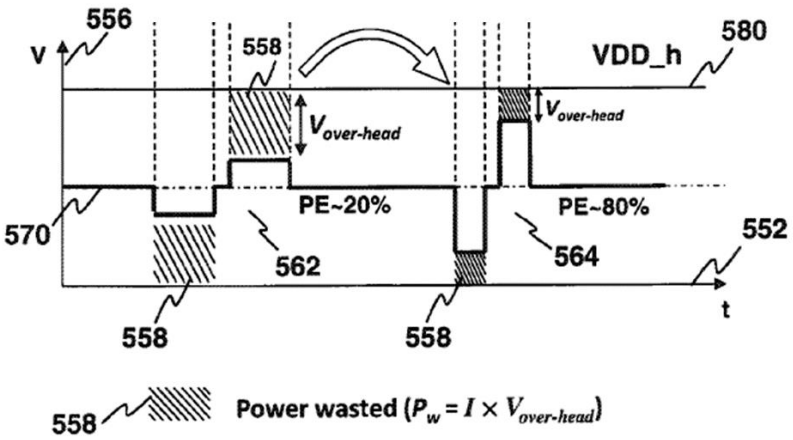


Figure 1.9. Example waveforms to modification performed on the stimulation current in [1]

As can be seen, there are studies that aim to make high voltage generators that are necessary for neural stimulators as efficient as possible. Modifying the supply voltage according to the necessary voltage compliance for the stimulators seems to be the most popular method. Altering the stimulation current seems to be another approach. However, they either use external components or controllers. Additionally, complex circuitry is required to operate the systems.

1.3 Objective of the Thesis

The main objective of this thesis is implementing a high voltage generator. The generator is to be used in a constant current stimulator that is a part of a fully implantable cochlear implant interface circuitry. A lower level DC voltage is to be utilized to cater to the high voltage needs of the stimulator. Both this work and the interface circuit are a part of FLAMENCO (A Fully Implantable MEMS-Based Autonomous Cochlear Implant) Project (www.flamenco.metu.edu.tr). Thus, the requirements of the system can be listed as follows:

1. The cochlear implant system is to be implanted within the human body. Thus, minimum intrusion is necessary in order not to disturb the person's biological

functions. Hence, volume is extremely limited. Therefore, number of bulky off-chip components must be no more than two.

2. Due to volume restrictions the energy source is limited. Being the most power hungry part of the implant, the stimulator necessates efficient operation of the high voltage generator. Thus, in accordance with where the systems mentioned above have evolved, the high voltage generator must adapt itself according to the compliance of the stimulator.

3. As the voltage of a battery is generally in the range of 3-4.2 V, and the required supply for the stimulator is determined to be up to 12 V, the converter must at least be able to quadruple its input voltage to achieve the required level.

4. Due to other sub-systems with inductive elements, such as wireless power-data transmission, the electromagnetic interference of the converter must be kept to a minimum.

1.4 Organization of the Thesis

Subsequent chapters of the thesis are as follows:

Chapter 2 starts by providing background information on switched capacitor converters. Subsequently, an adaptive converter system is detailed. The converter utilizes a 3-stage charge pump implemented in 180 nm HV process. With the utilization of a few external components, the adaptive converter system is tested with a constant current stimulator. The converter provides varying voltage levels depending on the required compliance and decreases the power dissipation of the stimulator compared to when the converter is operating in its constant voltage mode.

Chapter 3 presents an improved adaptive converter that solves the issues of its predecessor. Bulky external components are eliminated, enabling full integrate of the converter with the cochlear device. Moreover, the control loop of the previous version is improved. An 8-channel stimulator is implemented together with the

adaptive converter and experimental test results show that the adaptive converter fulfills its purpose and reduces the power dissipation of the stimulator.

Chapter 4 concludes the thesis with a brief summary of the achievements and describes possible future improvements that can be done to the adaptive converter.

CHAPTER 2

1ST GENERATION ADAPTIVE CONVERTER

2.1 Motivation

Devices utilizing constant current stimulation for improvement of human lives are being utilized in a lot of fields, be it for pain relievement, cochlear implants [2], deep brain stimulation [3], retinal stimulators [4] etc. To alleviate the low efficiency nature of current stimulation great effort is being spent. Focusing on the changing required voltage compliance seems to be the trend. The interface between the stimulation electrodes and neural tissue changes from person to person and even from time to time [35]. Moreover, for multi-channel systems where amplitude modulation is utilized [8], the magnitude of the constant stimulation current can vary as well. These circumstances cause the necessary voltage compliance for the stimulator to change. Different approaches can be found in the literature where some monitor the stimulation current and adjust the stimulator's supply voltage accordingly [20],[31]. Other concepts like manipulating the parameter of the stimulation current exist as well [1]. Each system has their advantages and drawbacks.

This chapter provides a brief discussion on switched capacitor circuits and presents an adaptive converter system that is utilized with a constant current stimulator. The converter utilizes a 3-stage charge pump with 540 pF on chip MIM capacitor to step the 3.3 V input up to 12 V. An Atmega2560 controller is used to digitally control the magnitude of the stimulation current with a 7-bit DAC. The controller is also used to configure the output of the charge pump to 3.3/6/9/12 V according to the required voltage compliance. An H-bridge was utilized to create the biphasic current pulse used for stimulation, enabling single supply operation [36,37].

Section 2 provides brief background information on switched capacitor circuits while Section 3 presents the charge pump used in this system. The adaptive converter system itself is detailed in Section 4 and the related experimental results are provided in Section 5. Finally, Section 6 summarizes the chapter.

2.2 Switched-Capacitor Converters Background

DC-DC converters can be divided into two categories: linear and switching. Linear converters are useful in scenarios where simplicity and minimum area consumption are important and the output is smaller than the input. Switching converters can be inductive, capacitive or hybrid. Both capacitive and inductive elements have not followed Moore's Law of scaling [27]. For instance, while other discrete components in devices were able to be integrated into an SOC, power management circuits could not be scaled as much [27]. Despite this, capacitive converters have been getting more attention due to their easier integration into CMOS technology compared to inductive converters and their advantages compared to linear regulators.

In case of linear converters, for which a representation is shown in Figure 2.1, the output cannot be greater than the input and the maximum efficiency that can be obtained for the ideal case can be calculated as the ratio of the output to the input.

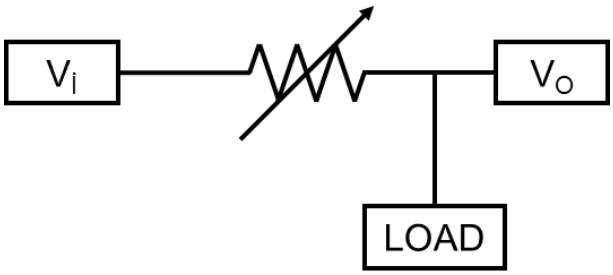


Figure 2.1. Representation of a linear regulator

The model of a SC converter is shown in Figure 2.2 [38-41]. R_O is the intrinsic output resistance of the converter, M_i is the conversion ratio and R is the load. As can be seen, it is similar to the representation of the linear regulator, the difference being

the transformer. This transformer, however, is what makes the switched capacitor converter more efficient as compared to linear regulators. The maximum attainable efficiency for the linear regulator was the ratio of the output to the input. With the inclusion of the conversion ratio, maximum attainable efficiency for the ideal SC converter becomes as shown in (2.1) [41].

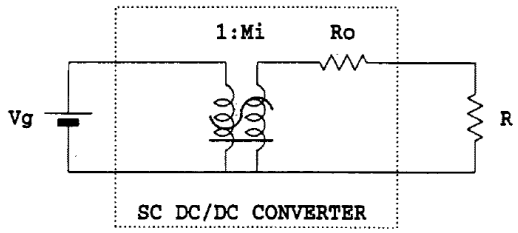


Figure 2.2. Model of switched-capacitor converter [41]

$$\eta_{MAX} = \frac{V_O}{V_G}\frac{1}{M_i} = \frac{1}{1+{R_O}/{R}} \tag{2.1}$$

Equation (2.1) shows the advantage of the SC converter as opposed to linear regulators: the incorporation of the conversion ratio boosts the efficiency. To illustrate, for a 0.4 V output and 1 V input, the LDO would achieve maximum 40% efficiency as the remainder of the power is dissipated on the resistor. This value increases to 80% for a switched capacitor with 1/2 conversion ratio as less power is dissipated on the output resistance of the SC converter while regulating the output.

As mentioned, R_O in Figure 2.2 is the intrinsic output resistance of the SC converter. This output resistance is composed of a slow switcing limit (SSL) and fast switching limit (FSL) component [38]. The SSL represents the operation range for the converter where the switching frequency is low enough so that charge on each capacitor reaches equilibrium during each phase. FSL, on the other hand, is the limit where the frequency is so high the currents between capacitors are constant and capacitor voltages are considered to be constant. The SSL models the loss resulting from charging and discharging process of the capacitors, i.e., ripple on the capacitors. FSL models the conductive losses that result from resistive elements such as switches. These limits are calculated as follows:

$$R_{SSL} = \sum \frac{a_{c,i}^2}{C_i \times f_{sw}} \tag{2.2}$$

$$R_{FSL} = 2\sum(R_i \times a_{r,i}^2) \tag{2.3}$$

where C_i is the capacitance of the i^{th} capacitor, f_{sw} is the switching frequency, R_i is the on-state resistance of switch i, $a_{r,i}$ and $a_{c,i}$ are charge multipliers for the i^{th} switch and capacitor, respectively [38]. These multipliers depend on the topology of the converter and thus change when the conversion ratio is altered. Moreover, the overall output resistance is obtained as:

$$R_O = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.4}$$

which means the output resistance can be manipulated by changing R_{SSL} or R_{FSL}. A graphical representation of the components and output resistance is also illustrated in Figure 2.3. f_z is the crossover frequency where R_{SSL} and R_{FSL} are equal. Figure 2.3 also illustrates the previous interpretations of SSL and FSL. For lower frequencies, the output resistance of the converter follows the SSL asymptote, increasing the output resistance. For higher frequencies, the output resistance follows the FSL asymptote. Thus, as it is apparent from (2.3) the output resistance does not change with f_{sw} in this region.

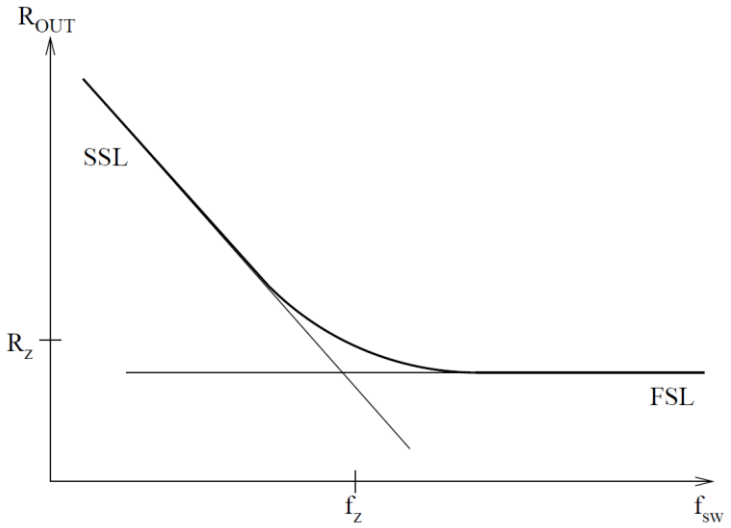


Figure 2.3. Graphical representation of the SC converter output resistance and its components

Furthermore, by inspection of equations (2.2), (2.3) and Figure 2.3 it can be deduced that in order to change these values, either C_i [23] or f_{sw} [45] must be changed for R_{SSL} and R_i [46] must be altered for R_{FSL}. In general, R_{SSL} is altered in order to perform regulation on the converters output, and between the modulation of capacitance and switching frequency, the latter is more popular. This brings to mind pulse frequency modulation (PFM), which means that the switching frequency will decrease for lower output voltages. Additionally, as in the case of the linear regulator, the efficiency will drop, per (2.1).

For scenarios where the output voltage must be altered, or when the output must stay constant for a range of input voltages the issue described above becomes a problem. However, altering the conversion ratio of the SC converter will alleviate this issue [40]. To illustrate, Figure 2.4 shows the efficiency values of a 2-stage and 3-stage converter for output voltages ranging from 8 V to 9 V, where the input is 3.3 V. As can be seen, the efficiency values for the 2-stage version are much greater than the 3-stage version.

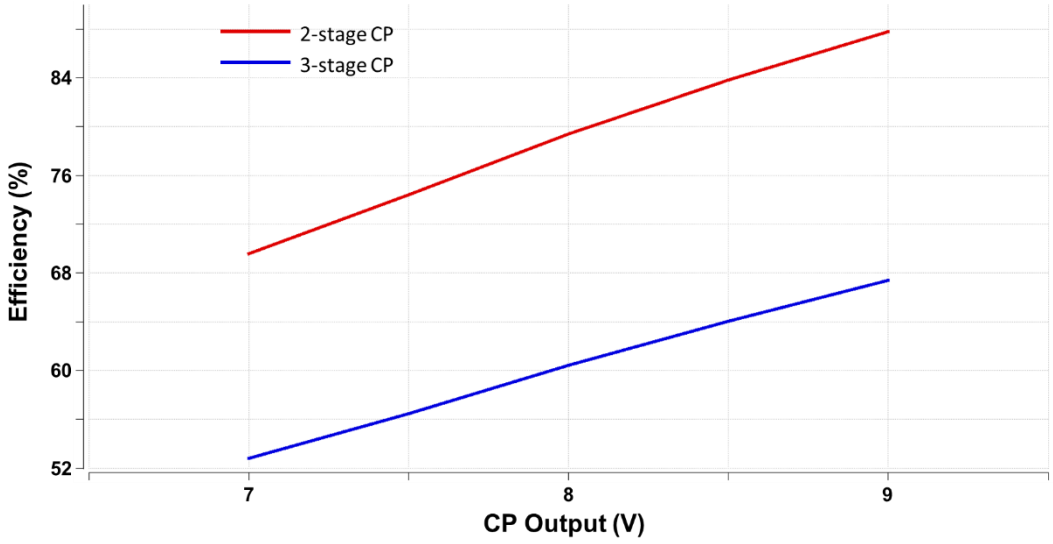


Figure 2.4. Efficiency values for simulated 2-stage and 3-stage charge pumps

In line with the background information given above, examples in the literature exist that work on adapting the system to keep the output constant for changing input voltages. In [40], the converter's topology, thus, its conversion ratio is altered as

shown in Figure 2.5 (a). Accordingly, the change in converter's effiency is illustrated in Figure 2.5 (b) for an input of 2 V. Thanks to the altering of the conversion ratio for different output levels, the converter is able to keep its efficiency as high as possible.

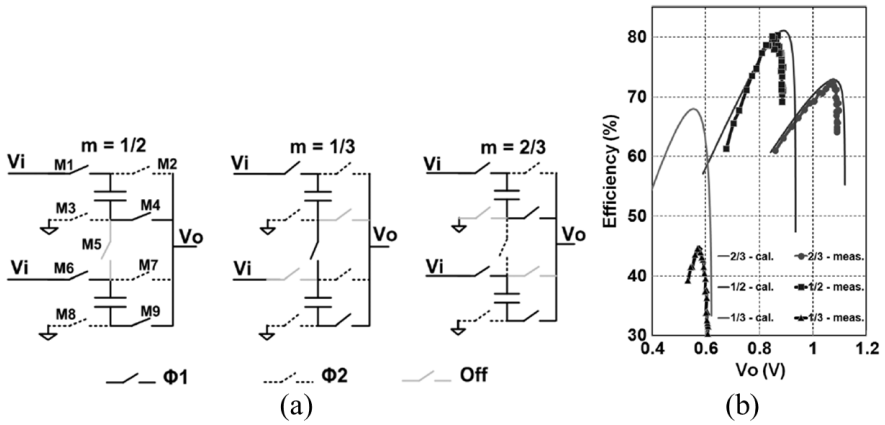


Figure 2.5. (a) Changing of converter topology in [40] (b) corresponding efficiency change

Similarly, [50] adapts the number of operational charge pump stages to generate a constant 1 V output independent from the output of the energy harvester it is connected to. In other words, the output of the system is kept constant for a varying range of output voltages coming from the harvester.

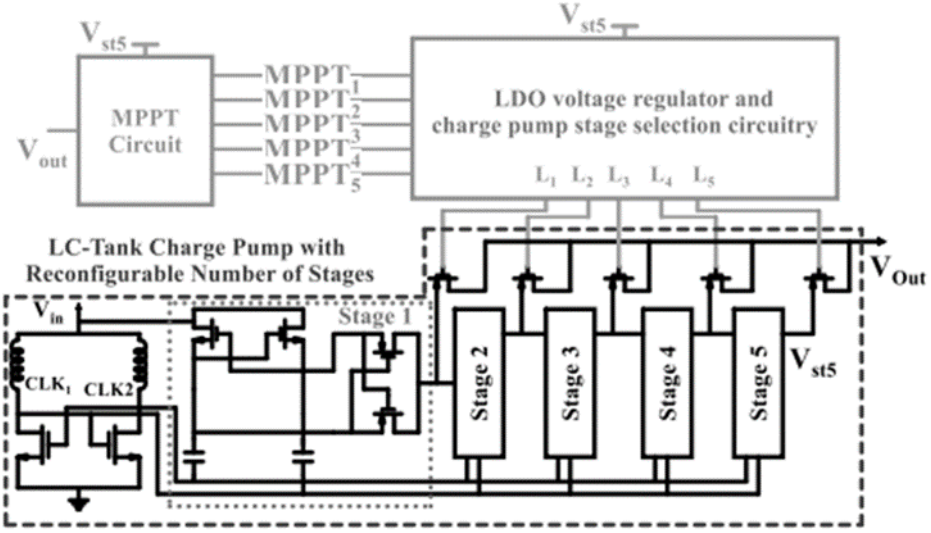


Figure 2.6. Charge pump structure in [50]

2.3 Step-Up Converter

The block diagram of the converter is presented in Figure 2.7. As can be seen, a 3-stage charge pump is utilized. The reason for this is that up to 12 V output is required from a 3.3 V input. A HV switch (M1-4) is connected at the output of each stage, which were optimized according to iterative simulation results. The reason for this was explained in the previous section; to alter the charge pump's conversion ratio. These switches are controlled with control bits Bit_2 and Bit_1. Depending on these control bits, V_{HIGH} is connected to a different node with the utilization of said switches and conventional level shifters. This way the conversion ratio of the converter is altered. Corresponding output voltages, operational number of stages and the value for the control bits are shown in Table 2.1.

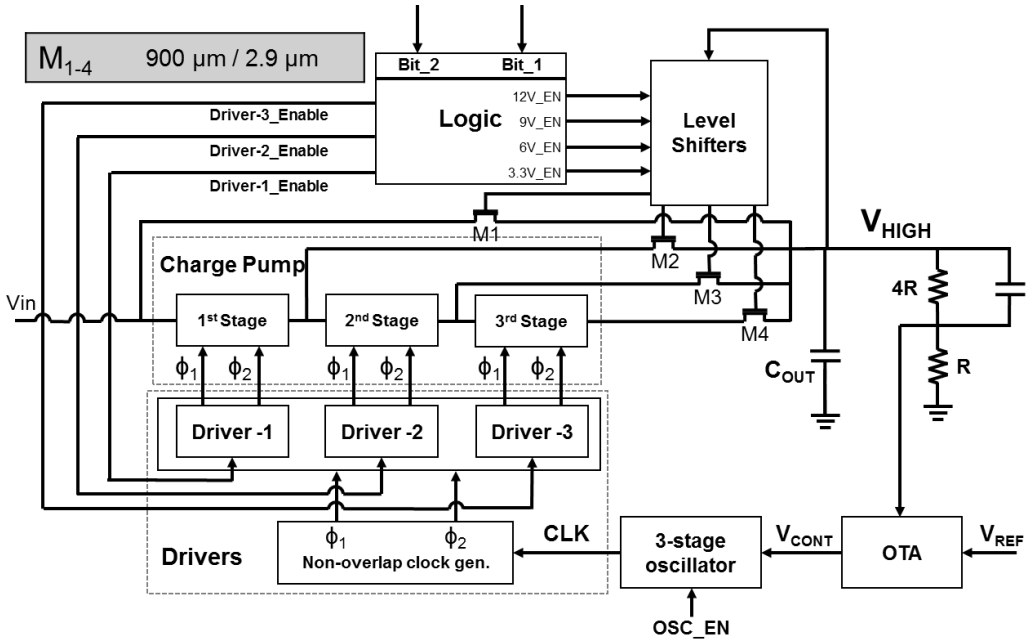
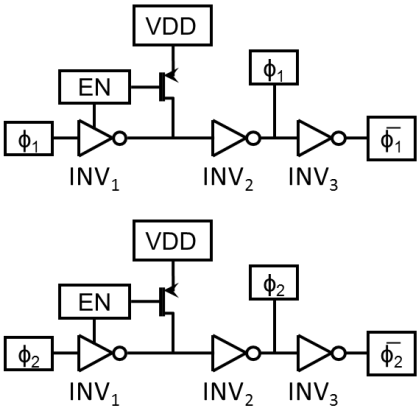


Figure 2.7. Block diagram of the converter

Table 2.1 Control bit values and corresponding output voltages

Bit_2	Bit_1	# Stage Operating	Output
0	0	0	3.3 V
0	1	1	6 V
1	0	2	9 V
1	1	3	12 V

Also governed by the control bits are the drivers for each individual charge pump stage, where they are turned off if the corresponding charge pump stage is not operating. The schematic of the drivers is shown in Figure 2.8. The logic used to control the drivers and switches M1-4 is presented in Figure 2.9.



	PMOS / L – NMOS / L
INV_1	10 µm / 0.3 µm – 5 µm / 0.35 µm
INV_2	20 µm / 0.3 µm – 10 µm / 0.35 µm
INV_3	30 µm / 0.3 µm – 15 µm / 0.35 µm

Figure 2.8. Schematic diagram of the drivers

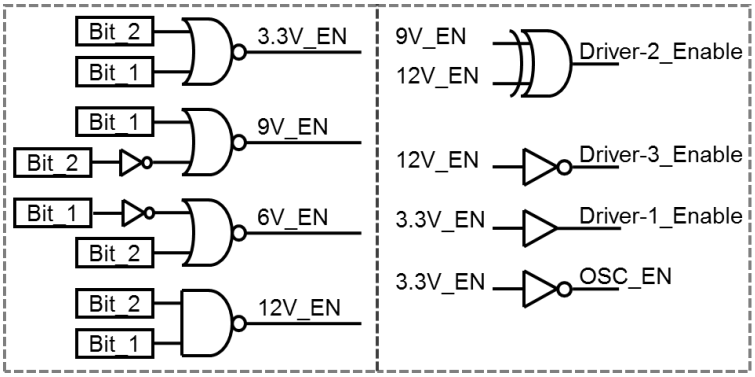


Figure 2.9. Simple logic used to control switched M1-4 and drivers

To overcome short circuit losses, non-overlapping clock phases are utilized [40], [42], which are named as ϕ_1 and ϕ_2 in Figure 2.8. Figure 2.10 depicts the non-overlapping clock generator where the transmission gate and MOSFET capacitor act as an RC circuit to introduce delay. The phases themselves are presented in Figure 2.11.

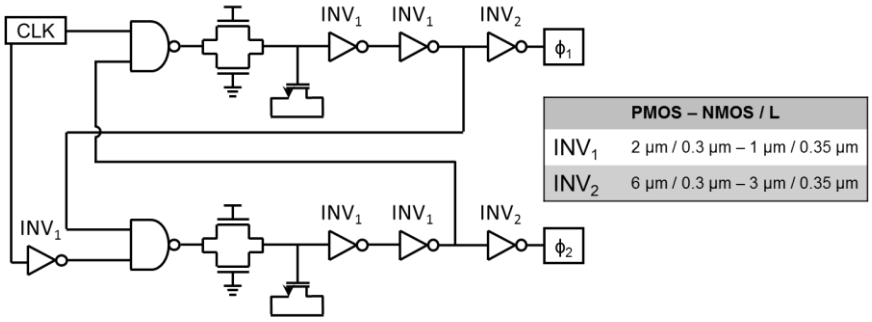


Figure 2.10. Schematic diagram of the non-overlapping clock generator

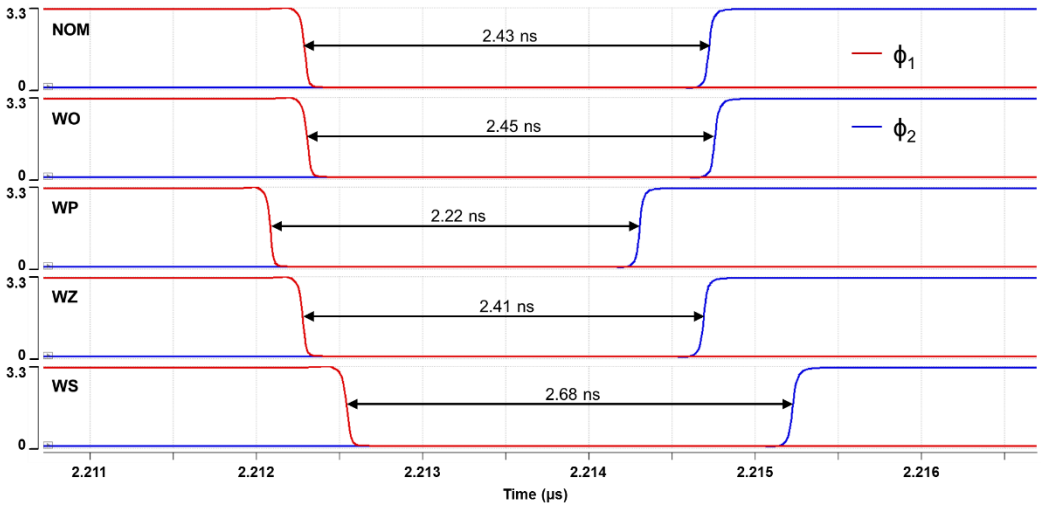


Figure 2.11. Dead-time variation with different corners for non-overlapping phases

One stage of the charge pump is presented below in Figure 2.12. It is the charge pump presented in [43] without the charge reusing method that was implemented in that design as well. The operating principle can be explained as follows. When ϕ_1 is HIGH, node B_i is charge to V_{i-1}. When ϕ_1 becomes low, the bottom plate of C_2 gets boosted to VDD and node B_i increases to VDD+V_{i-1}. Capacitor C_1 operates in the

same way as C_2, but in the opposite phase. Then, the output of one stage can be calculated as in (2.5).

$$V_i = V_{i-1} + VDD \tag{2.5}$$

Thus, from the equation above, a 3-stage charge pump will quadruple the input voltage at no load condition. As the input of the system is 3.3 V and the required supply for the stimulator is maximum 12 V, a 3-stage version is utilized. The values for C_1 and C_2 are 90 pF per stage. Sizing of the switches were performed by performing iterative simulations with the drivers and the fall and rise time of the clock signals according to these sizes.

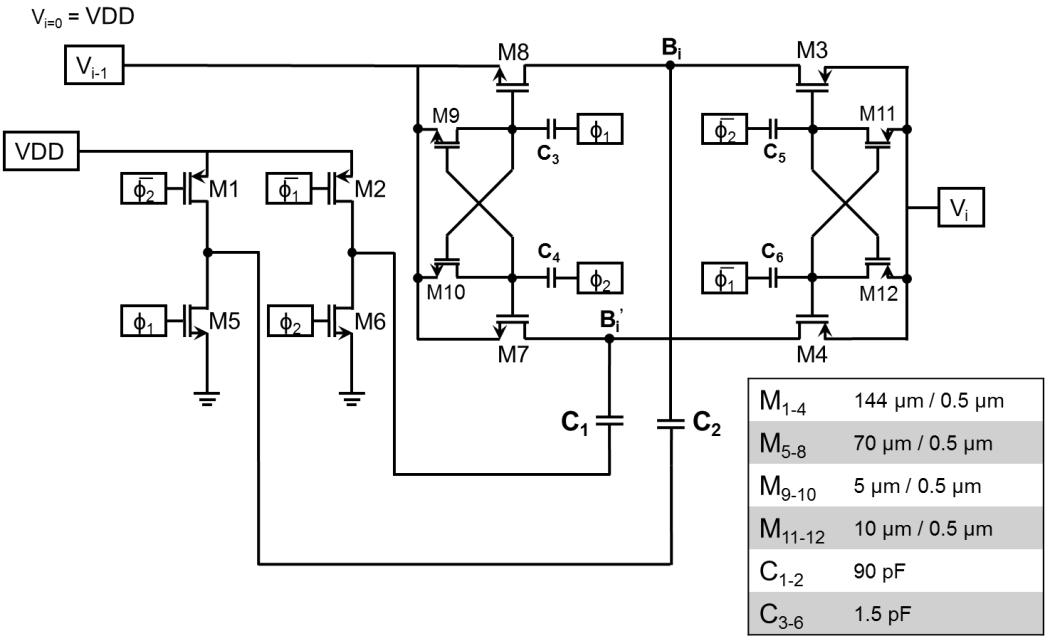


Figure 2.12. Schematic diagram of 1-stage charge pump

To regulate the output of the converter, pulse frequency modulation, which can be considered as "fine" regulation, is utilized. A resistive divider as shown in Figure 2.7 is utilized where R is 150 kΩ. Filtering capacitor used is 300 pF. Moreover, as Table 2.1 showed, the control bits change the number of operational charge pump stages, and thus, the conversion ratio of the converter. This can be considered as "coarse" regulation. Depending on the desired output, Bit_1 and Bit_2 take different values.

In addition the these control bits, the correct reference voltage V_{REF} must be provided to the converter as well. To illustrate, in case the output of the converter must be configured to 9 V, two of the stages must be operating as approximately three times the input voltage is desired. Furthermore, for PFM the correct V_{REF} must be provided. As the ratio of the resistive divider at the output of the converter 1/5, the referecen voltage should be 1.8 V. To conclude, by manipulating Bit_1, Bit_2 and V_{REF}, the output can be configured to 3.3/6/9/12 V.

2.4 Adaptive Converter System

The converter presented in the previous section is to be used to provide an adaptive supply to a constant current neural stimulator. To do this, some signals must be provided to the converter. As mentioned, these are Bit_1, Bit_2 and V_{REF}. For this, the system shown in Figure 2.13 is implemented [44]. The system can be explained as follows. To create the biphasic stimulation current, an H-bridge is utilized. Its schematic can be seen in Figure 2.14 [8]. Control signals P_A and P_C are manipulated so that the stimulation current is steered from one electrode to the other and vice versa.

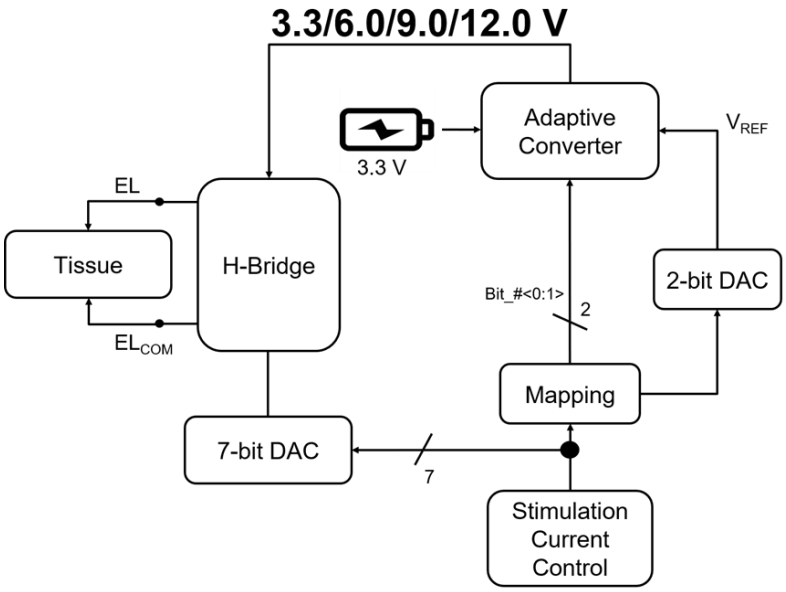


Figure 2.13. Adaptive converter system block diagram

Also presented in Figure 2.14 is a 7-bit DAC. V_G in this figure is kept constant at 3.3 V and D_i is utilized to alter the magnitude of the stimulation current. This 7-bit control signal is provided by an Atmega2560 controller. The controller also creates Bit_1 and Bit_2 by mapping the 7-bits transmitted to the DAC to 2-bits with a lookup table. In order to do this, the load information is entered into the code written onto the controller.

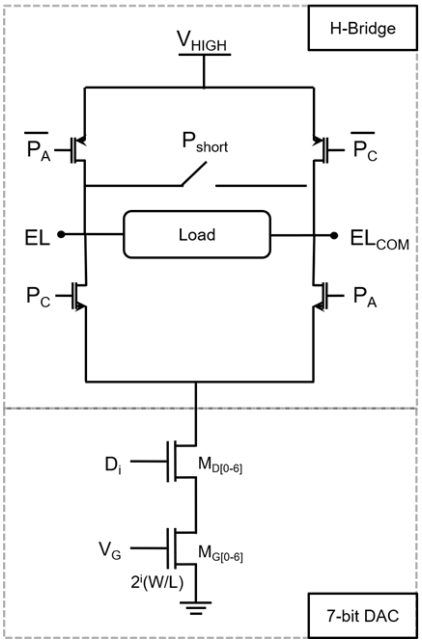


Figure 2.14. Schematic diagram of H-bridge and 7-bit DAC

The 2-bits that are used as Bit_1 and Bit_2 are also fed to an off-chip 2-bit DAC. This is done to generate V_{REF}. Thus, when Bit_1 and Bit_2 change according to the necessary voltage compliance, the reference voltage changes as well, enabling proper regulation of the converter's output. The 2-bit DAC is a simple resistive DAC and an inverting amplifier at the end providing the necessary offset for the correct reference voltage (Figure 2.15). After generation of the reference voltage and control bits, the output of the charge pump is regulated properly and provided to the H-bridge.

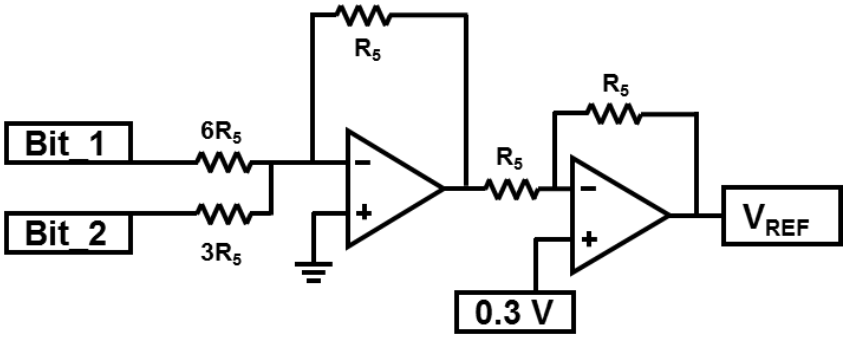


Figure 2.15. 2-bit DAC structure

2.5 Experimental Results

The adaptive converter system is designed and implemented in 180 nm HV X-FAB process. Figure 2.16 depicts the micrograph of the converter and Figure 2.18 shows the designed PCB to test the adaptive converter system. The entire die is 3.1 mm x 3.1 mm (9.61 mm^2) whereas the active area of the converter is approximately 1.02 mm^2 as shown in the figure. Majority of the active area is occupied by the on-chip 540 pF MIM capacitors.

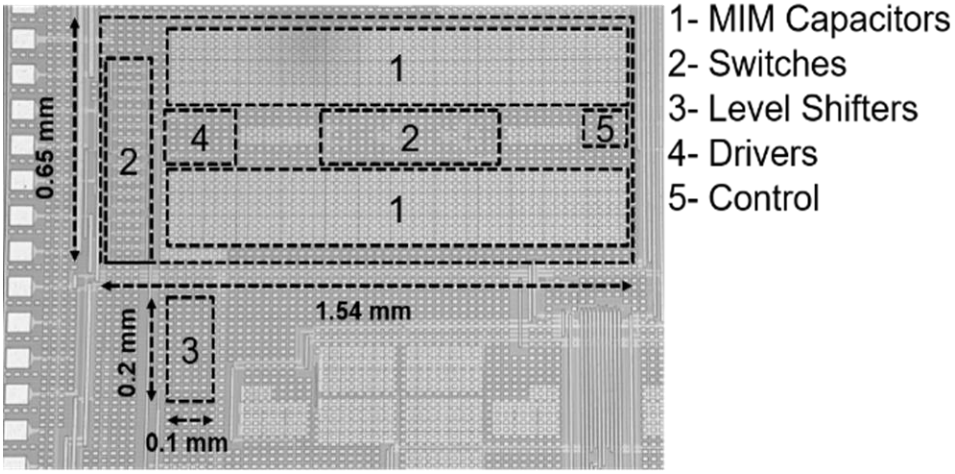


Figure 2.16. Die micrograph of the converter

First, the converter was tested to obtain its power efficiency values for different output voltages. Figure 2.17 shows the efficiency values for a range of loads. The input voltage is set to 3.3 V.

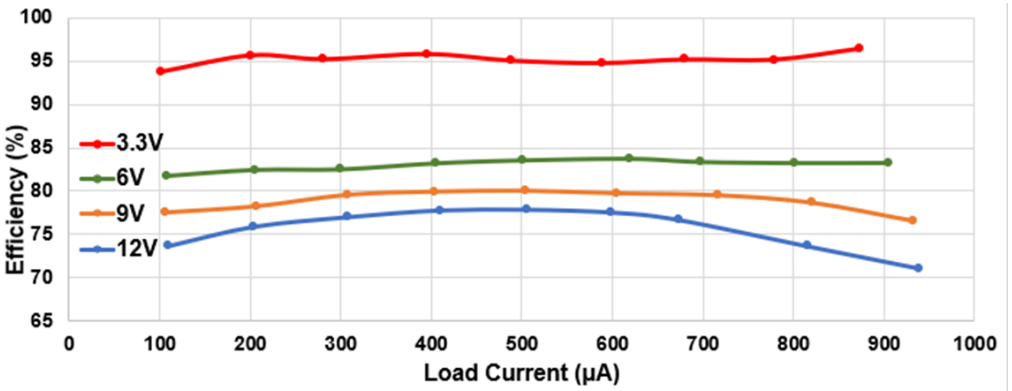


Figure 2.17. Power efficiency values of the converter for different outputs

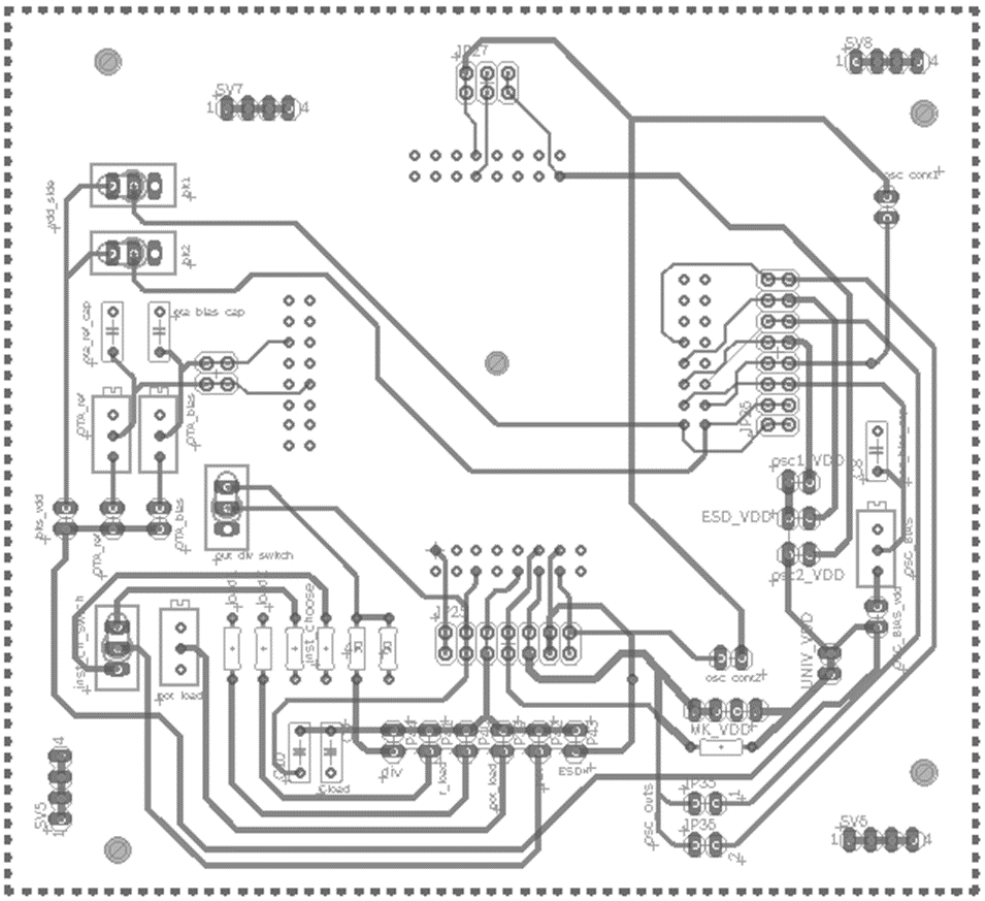


Figure 2.18. PCB designed to test adaptive converter

Subsequently, tests were performed on the converter together with the H-bridge and 7-bit DAC presented in [8]. The bits of the 7-bit DAC were altered with a controller. By manipulating these control bits, the magnitude of the stimulation current was changed. As explained before, the same controller mapped the 7-bit data to 2-bits for the converter to use. It also provided the same bits to the 2-bit DAC for the generation of the reference voltage (Figure 2.13). An example illustration is shown in Figure 2.19 for a better explanation.

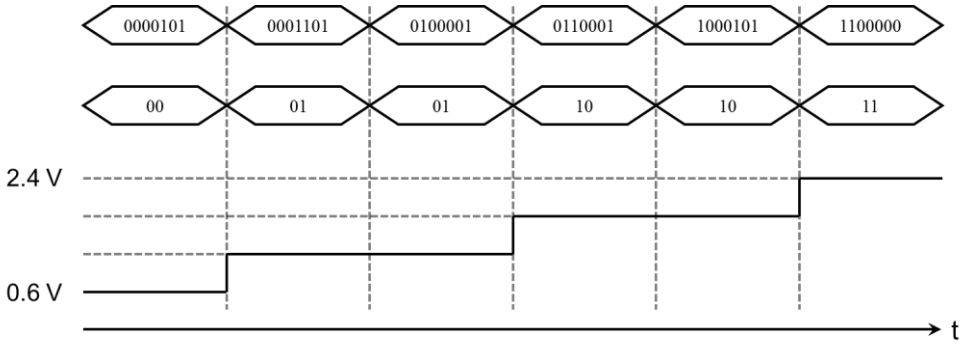


Figure 2.19. Illustration for the generation of the reference voltage

The first load that was used to test the adaptive converter system was an artificial series R-C load, as is the model of the neuraon-tissue interface. Values for the loads were 9.76 kΩ and 33 nF and they were connected between the electrodes as illustrated in Figure 2.20.

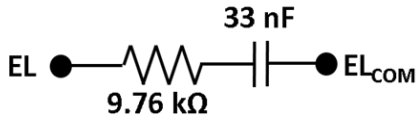


Figure 2.20. Illustration of connected artificial load between the electrodes

Five stimulation current magnitudes were configured within the code on the controller and passed through the load in a loop. The resulting waveforms are presented in Figure 2.21 (a). As can be seen, the converter's output is configured from 3.3 V at around 0.5 ms to 12 V in the subsequent stimulation period. This is because the stimulation current is increased from 100 µA to 800 µA. Thus, the

required voltage compliance increases as well. Another aspect that can be observed from the figure is that the converter's output is pulled to 12 V before the subsequent stimulation period. This is to ensure there's enough voltage compliance in the subsequent stimulation period.

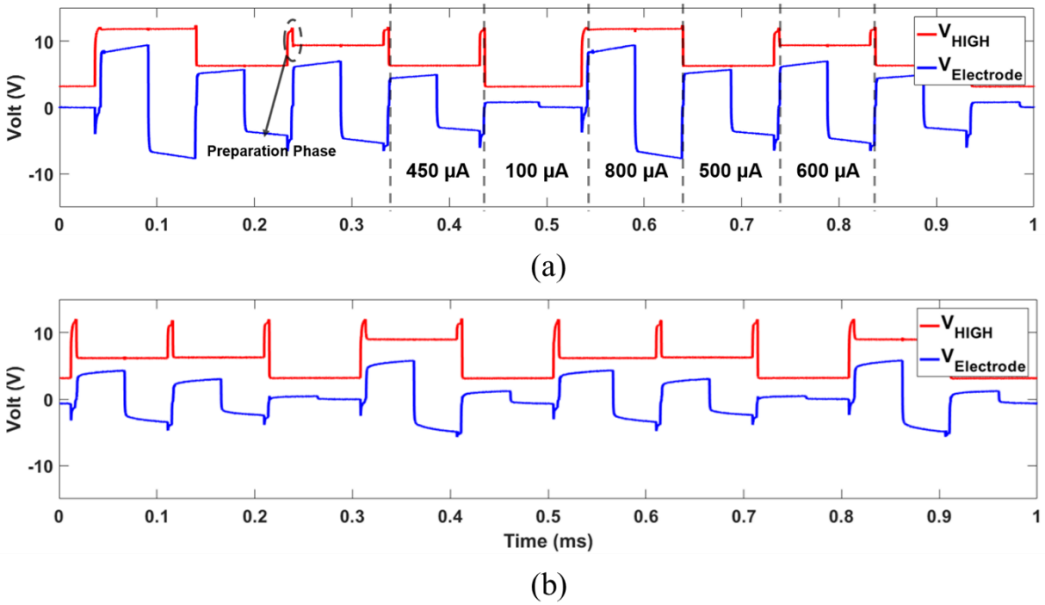


Figure 2.21. Electrode voltages and adaptive converter output for (a) artificial load (b) in-vitro

Secondly, in-vitro test was performed on the system. It was tested with a single channel platinum stimulation electrode in a saline mixture. The impedance of the electrode was determined to be 7 kΩ and 65 nF upon measurement with Agilent E4980A LCR meter in Cs-Rs configuration. The resulting waveforms confirming the operation of the system are presented in Figure 2.21 (b).

By taking into account the measurements in Figure 2.17, Figure 2.22 is created, which shows the power dissipation values of the converter in adaptive voltage configuration and constant 12 V configuration for a range of loads. The calculations were made according to the load shown in the figure and do not include the power dissipation of the controller and off-chip DAC. It also depicts the percentage of reduction in power dissipation.

The reduction in power dissipation is 4.1 mW for 500 µA stimulation current, which corresponds to a 53% decrease. This ratio increases to around 79% for 200 µA as the charge pump is not operational for that current magnitude.

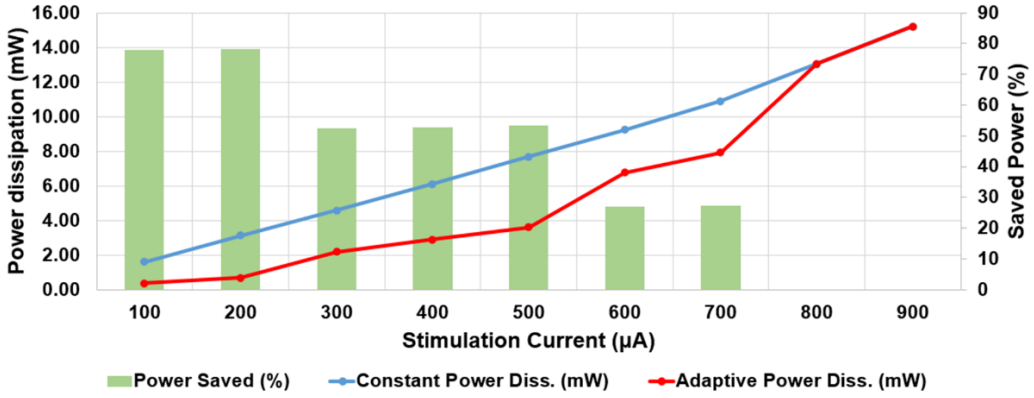


Figure 2.22. Power dissipation for constant and adaptive output configuration

2.6 Summary of the Chapter

In this chapter, an adaptive converter system is presented. The converter was implemented in 180 nm HV X-FAB process. A total of 540 pF on-chip MIM flying capacitors were integrated on-chip to minimize the number of external components. An Atmega2560 controller was utilized to create the 7-bit control signal to adjust the magnitude of the stimulation current. In addition, these 7-bits were mapped to 2-bits to control the number of operational charge pump stages and generate a reference voltage for coarse and fine regulation of the converter's output. This enabled the converter to provide 3.3/6/9/12 V outputs for a range of load currents. Up to 79% reduction in power dissipation was observed when the converter is operating in adaptive mode as opposed to constant supply mode.

Despite the achievements mentioned above, there are several issues with this system. Firstly, there are a lot of external components. The 2-bit DAC is off-chip, and the controller, which governs the whole system, is not integrated. Implanting this system will not be possible due to obvious reasons. Moreover, the control loop is not closed. Load information must be entered into the code in order for it to configure the

converter. Furthermore, the CP's output can only take discrete values. Enabling the converter to take continues values so that it follows the electrodes' potential difference will improve power dissipation reduction. Finally, the converter should be able to operate with a multi-channel stimulator. These problems must be overcome in the next generation of the adaptive converter.

CHAPTER 3

2ND GENERATION ADAPTIVE CONVERTER

3.1 Motivation

The previous chapter presented a system that was implemented to drive a neural stimulator with varying supply voltages. However, three main drawbacks that must be overcome exist in that system. First one is external components. As mentioned, a controller together with an off-chip DAC was used to control the charge pump. As the system must operate within a cochlear implant and volume occupation is limited, using such external components is not acceptable. The second limitation of the system is related to the control mechanism of the charge pump. The controller determines the number of operational stages in the charge pump and provides the reference voltage necessary for pulse frequency modulation. It also controls the magnitude of the stimulation current. In order for the controller to decide on the neural stimulator's supply voltage, the neural load information is needed. This information is entered manually while testing. In other words, the control mechanism's loop is not closed. Thus, the integration of a control system automating this process is necessary. Moreover, the converter's output can only take discrete values. Making it possible so that it can take a range of values will improve efficiency. Finally, the system work with a single channel. However, for cochlear implants multi-channel stimulators are utilized, thus, the converter should be able to operate with these systems.

In this chapter, an improved version of the adaptive converter is presented. In this version, external components are eliminated, and the loop is closed so that the integrated system can automatically decide on the necessary supply voltage for the neural stimulator. To do this, the stimulation electrodes' potential difference is tracked. By taking a portion of this potential difference, giving it an offset and

providing it to the charge pump regulation scheme, a voltage that follows the electrode voltages is obtained.

The circuit is implemented in 180 nm CMOS technology. A 3-stage charge pump is again utilized to step up the input voltage. However, due to timing reasons the process was changed. As a result of limitations of transistor terminal voltages in the new process, the input is dropped to 1.8 V from 3.3 V. Thus, maximum supply is reduced to 5.5 V. Tests were performed on the adaptive converter system while operating in constant 5.5 V supply mode as well as electrode voltage tracking mode. Power dissipation reduction of up to 35% was observed for tracking mode compared to its constant voltage operating mode.

Section 2 of this chapter presents the step-up converter that utilizes a 3-stage charge pump. Section 3 goes into detail about the voltage tracking circuitry and how the electrode voltages are scaled and provided to the converter as reference voltage. Section 4 presents the experimental results of the adaptive converter system and Section 5 summarizes the chapter.

3.2 Step-Up Converter

The heart of the converter is the same 3-stage charge pump structure in the previous version. A 3-stage structure is again adapted due to the supply voltage requirement of up to 5.5 V from 1.8 V input voltage. This time, however, the flying capacitor amount is 176 pF per stage due to area restrictions. Additionally, as the input voltage is reduced to 1.8 V, transistors with maximum 2 V terminal differences are utilized. The block diagram of the charge pump side of the system is shown below in Figure 3.1.

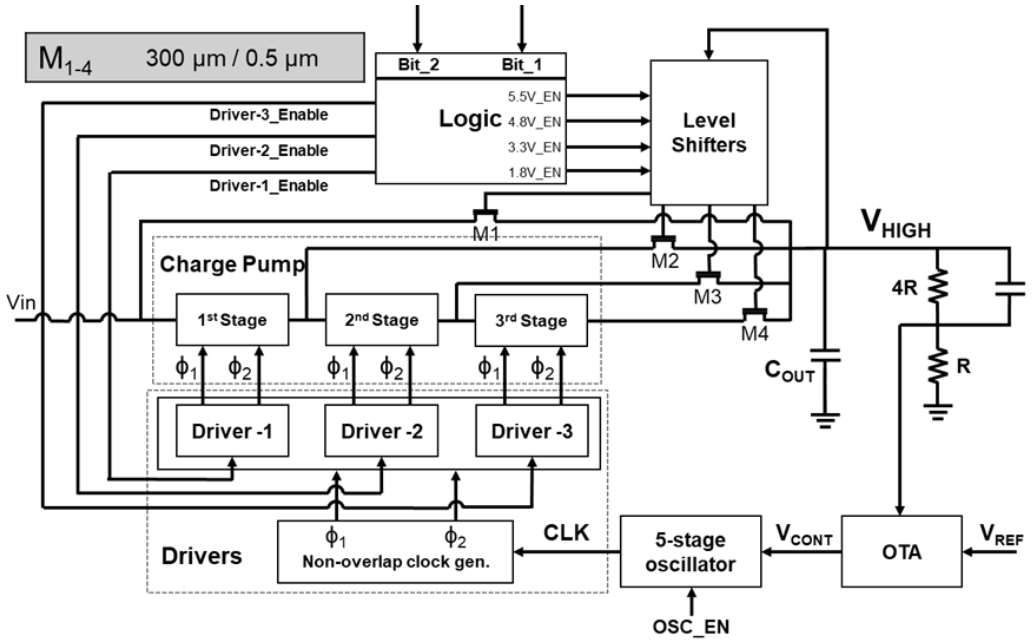


Figure 3.1. Block diagram of the charge pump side of the system

The structure is similar to the previous version with small changes inside the sub-blocks. The current starved voltage-controlled oscillator (VCO) was changed to a 5-stage version and its schematic can be seen in Figure 3.2.

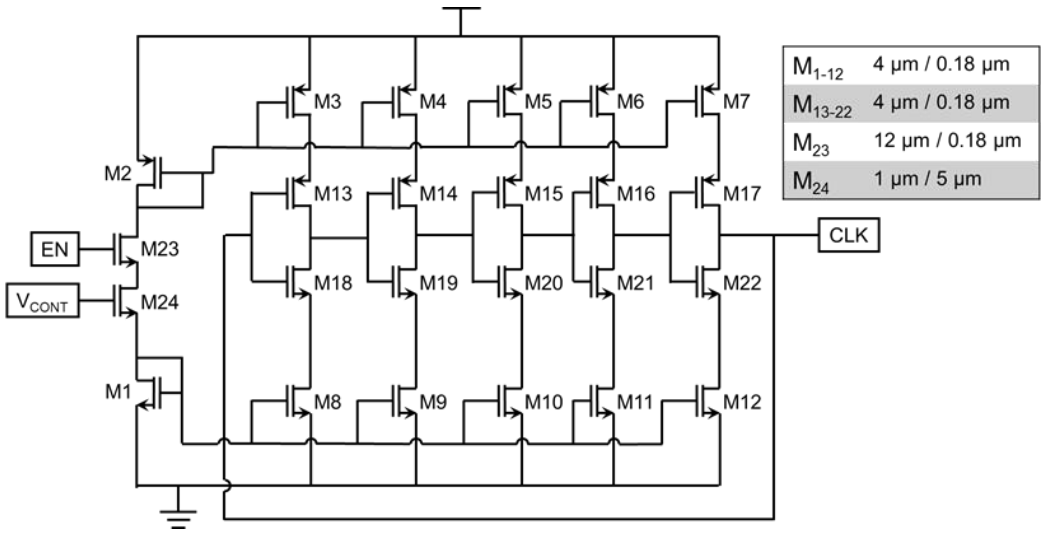
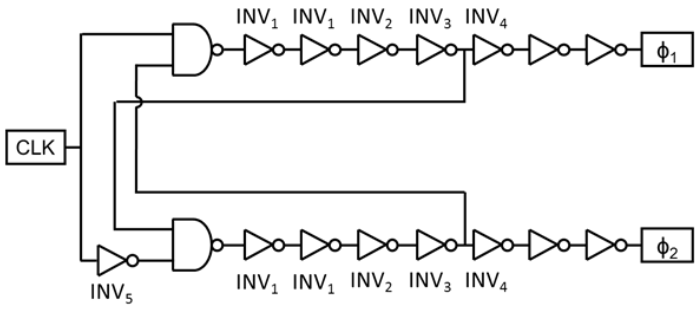


Figure 3.2. Schematic diagram of the 5-stage current starved VCO

Non-overlapping clock generator is also tweaked compared to its previous version. As can be seen in Figure 3.3, the transistors used as capacitive loads are eliminated

and the delay is adjusted with the inverters. INV_1's length is different compared to the other inverters to adjust the deadtime between the phases. This approach was chosen as opposed to increasing the number of inverters to keep power dissipation low. Corner simulations showing the variation in dead-time are provided in Figure 3.4.



	PMOS – NMOS / L
INV_1	1 µm – 0.5 µm / 1.5 µm
INV_2	1 µm – 0.5 µm / 0.18 µm
INV_3	2 µm – 1 µm / 0.18 µm
INV_4	4 µm – 2 µm / 0.18 µm
INV_5	0.5 µm – 0.25 µm / 0.18 µm

Figure 3.3. Schematic of the non-overlapping clock generator

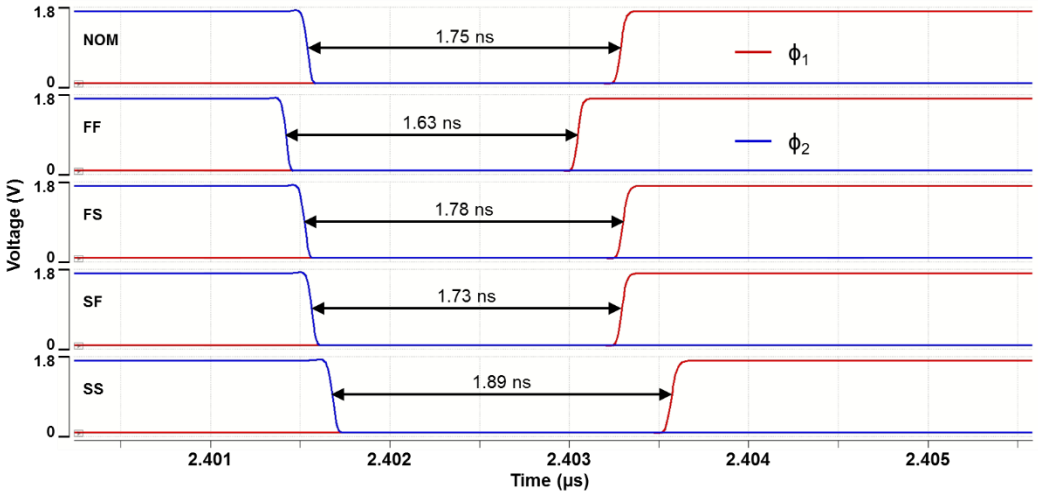
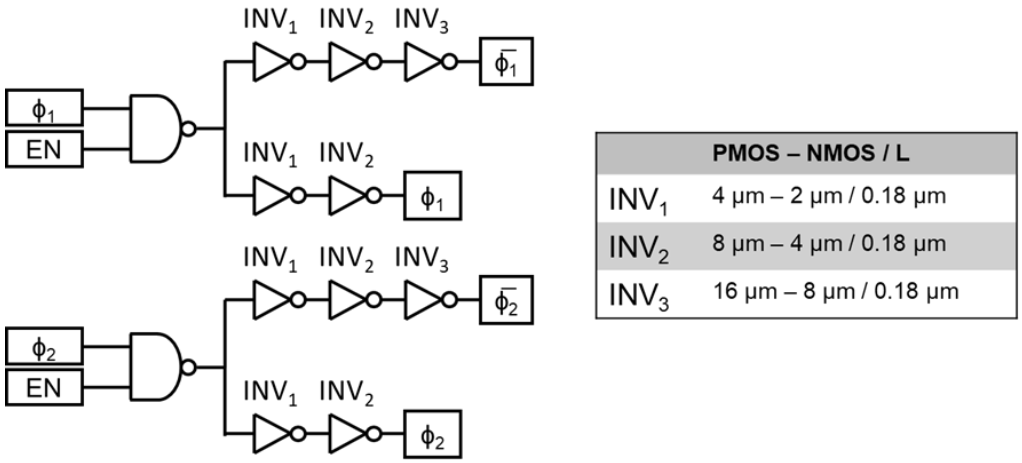


Figure 3.4. Dead-time variation with different corners for non-overlapping phases

The two phases generated by the non-overlapping clock generator are transmitted to the drivers, whose structure can be seen in Figure 3.5. The drivers are configured such that the gates of PMOS transistors are pulled to HIGH and to LOW for NMOS when they are disabled. This way the discharge paths of the capacitors are disabled and only leakage currents act.



	PMOS – NMOS / L
INV_1	4 µm – 2 µm / 0.18 µm
INV_2	8 µm – 4 µm / 0.18 µm
INV_3	16 µm – 8 µm / 0.18 µm

Figure 3.5. Schematic diagram of clock drivers

One stage of the charge pump is shown below in Figure 3.6. The operation of one-stage is the same as in the previous charge pump. As shown in the table next to the schematic, flying capacitors C_1 and C_2 are 88 pF each, making the total capacitance per stage 176 pF. C_3 to C_6 are again boosting capacitors and operate as explained in the previous version of the system. The part of this charge pump that was not present in the previous version is the NOR gate and the NMOS switch. Operation for these added components can be explained as follows. As was shown in Figure 3.4, non-overlapping clock is used to overcome short circuit losses. During the dead-time, both ϕ_1 and ϕ_2 are low. Thus, by utilizing a NOR gate the bottom plates of the flying capacitors are shorted during this time interval. This way, some of the charge that is present when one of the flying capacitors' bottom plate is charged to VDD can be transferred to the other capacitor's bottom plate when that one is charging up [43]. Doing this reduces the charges lost to charging the bottom plates of the flying capacitors and improves the efficiency of the charge pump.

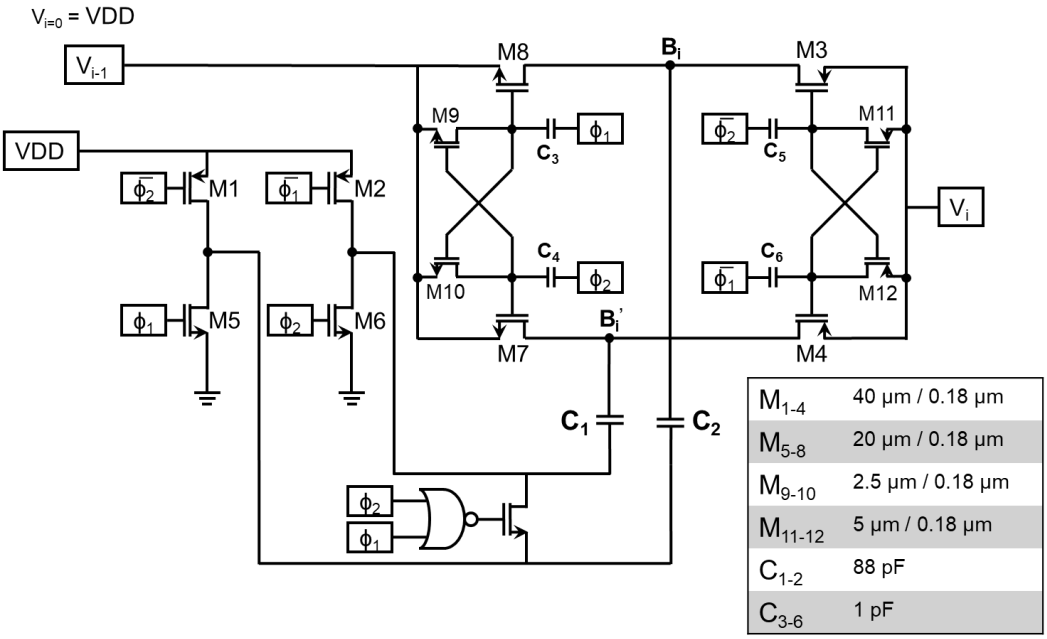


Figure 3.6. 1-stage charge pump schematic diagram

The small logic circuitry used to control the switches M1-4 in Figure 3.1 is depicted below in Figure 3.7, which is similar to the previous version. Also shown in this figure is the logic that enables and disables the drivers for the individual stages and the 5-stage oscillator for when the charge pump is not operating. According to this logic, the number of operational charge pump stages corresponding to Bit_2 and Bit_1 is shown in Table 3.1. The corresponding output voltages are also shown in this table.

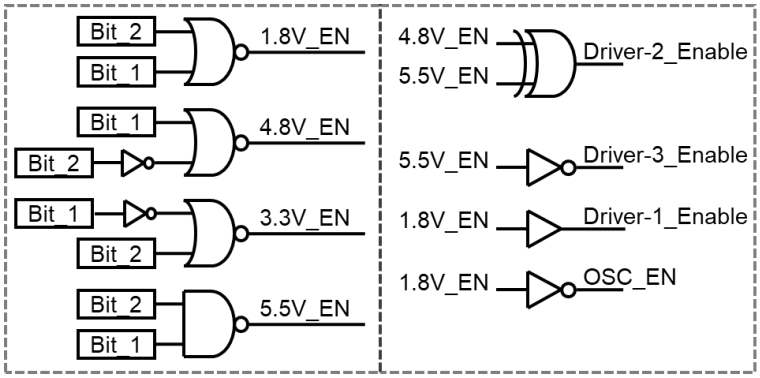


Figure 3.7. Simple logic used to control switched M1-4 and drivers

Table 3.1 Charge pump operating conditions according to control bits

Bit_2	Bit_1	# Stage Operating	Output Range
0	0	0	1.8 V
0	1	1	1.8 V – 3.3 V
1	0	2	3.3 V – 4.8 V
1	1	3	4.8 V – 5.5 V

The control signals created in Figure 3.7 are low level so level shifters are needed. Conventional level shifters that are being supplied by the charge pump are utilized. Simulation results for all corners confirming its operation for 5.5 V and 1.8 V supply voltage is shown in Figure 3.8.

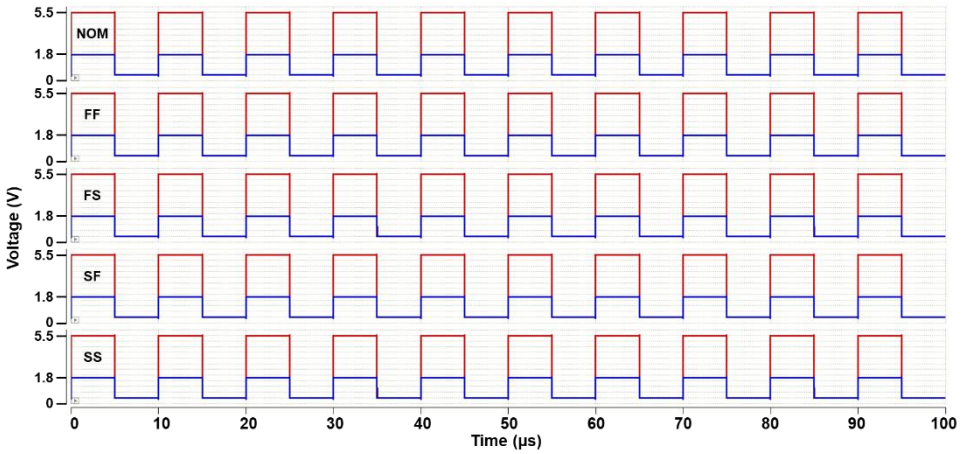


Figure 3.8. Level shifters operation for switches M1-4 for 1.8 V and 5.5 V supply

The reason for changing the number of operating charge pump stages was explained in the previous section. This method was regarded as the course regulation of the output. For fine regulation of the output for this system, PFM regulation is again used. The OTA used for this is shown in Figure 3.9.

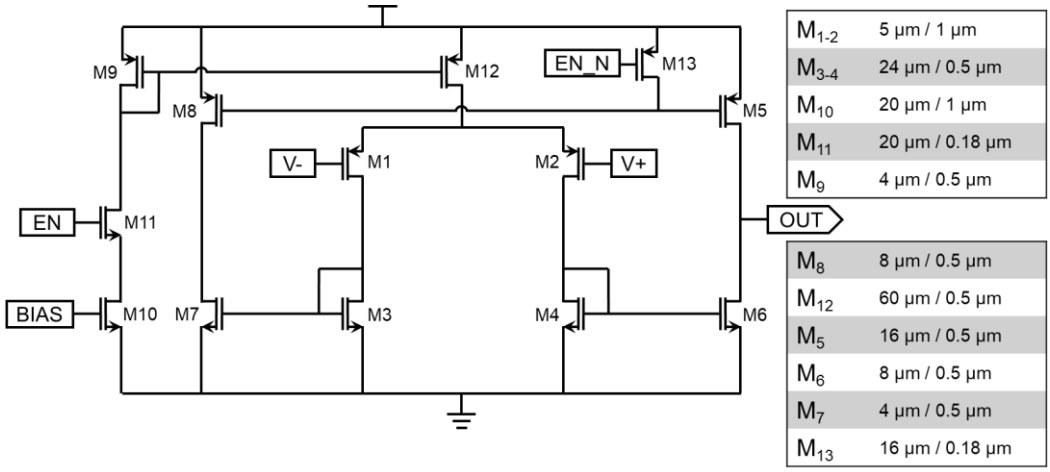


Figure 3.9. OTA used in PFM

Also related to PFM regulation of the charge pump output are the voltage divider and filter capacitor, which were shown in Figure 3.1. The filtering capacitor used was 2.2 nF. R value of the resistive divider is 200 kΩ. The capacitor connected in the divider network is to provide a feedforward path and make the regulation more fast and stable. Its value is 2 pF. Thus, the OTA again compares the divided output and V_{REF} so that the desired charge pump output can be obtained. An example transient simulation results is shown below in Figure 3.10. As can be seen, the charge pump's output is regulated according to the reference voltage. Although the reference voltage below is manually provided to the charge pump to observe the regulation, the control mechanism that governs the number of operating charge pump stages does this according to the reference and is automated. Moreover, one can locate the locations where a charge pump stage start operating as there is a small spike present as shown in the figure.

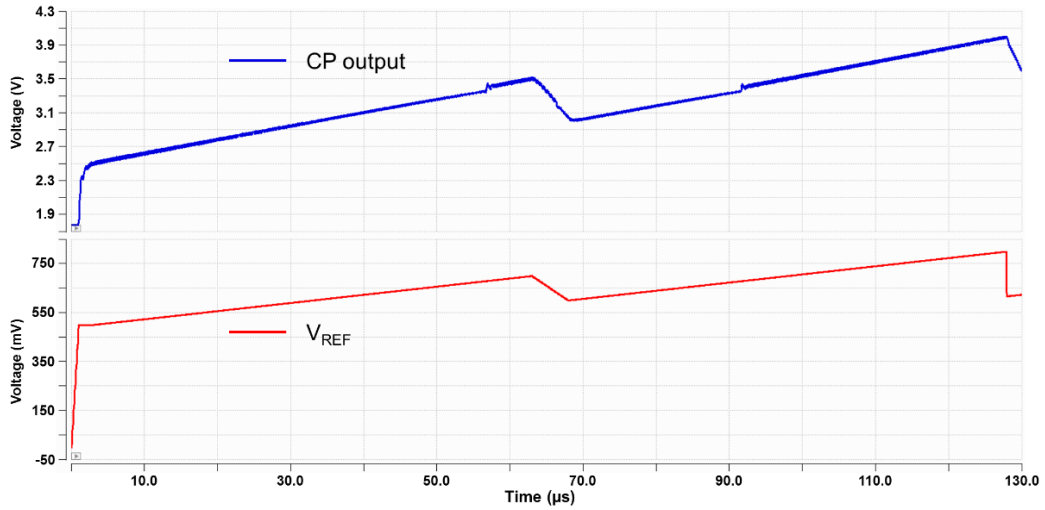


Figure 3.10. Transient simulation showing the regulation of the converter

In the previous system control bits Bit_1 and Bit_2, the control mechanism for operational charge pump stages, as well as the reference voltage were provided by external components and the elimination of these components was necessary. The subsequent section will detail the voltage tracking circuitry that undertakes both these tasks.

3.3 Voltage Tracking Circuitry

With the help of the external components, the previous system's output can be configured to discrete voltages. In this improved version of the adaptive converter the supply voltage fed to the neural stimulator can take a range of values. Moreover, the external components are eliminated and an integrated system automatically configures the output of the step-up converter. To do this, the voltage tracking circuitry shown in Figure 3.11 is utilized.

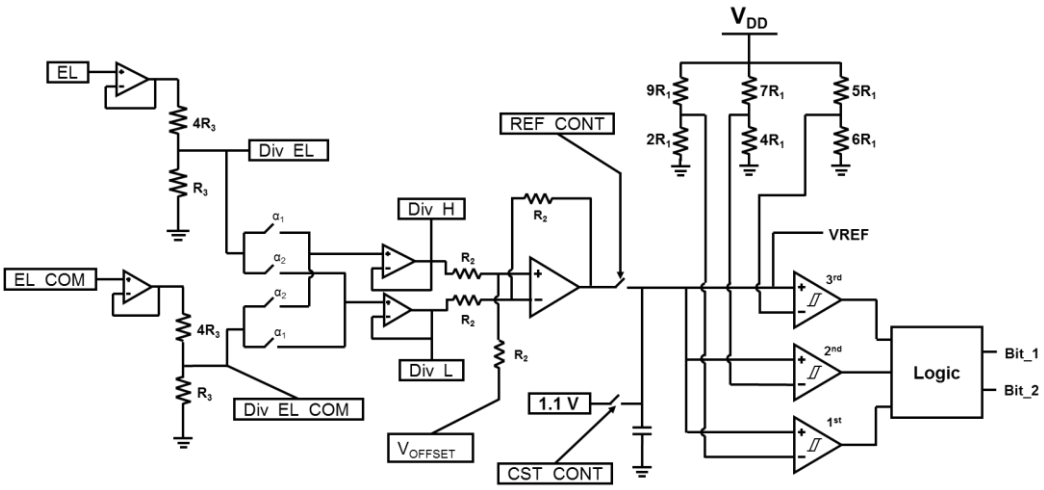


Figure 3.11. Block diagram of the voltage tracking circuitry

The following sub-sections will detail the operation of the sub-blocks, however, it is advantageous to summarize the operation of the overall tracking circuitry. The fundamental idea of the system is to take a ratio of the electrodes' potential difference, give it an offset and provide it to the step-up converter as reference. This is done as follows. The inputs of the circuit are EL and EL_COM. EL_COM represents the common electrode of the neural stimulator. EL, on the other hand represents the active electrode amongst 8 that are present, namely, EL-1, EL-2, EL-3, etc. [8, 36]. First, these nodes are buffered to isolate them from the resistive divider that comes next. Div_EL and Div_EL_COM denote the divided EL and EL_COM voltages. These divided electrode voltages are then passed through a switch array, for which the reason will be explained later, and fed through another set of buffers. Afterwards, subtraction is performed on the divided electrode voltages with a difference amplifier. The resulting waveform will then be the scaled down electrode potential difference and can be used as reference for PFM regulation. It is also used by a flash ADC to determine the number of operational charge pump stages by creating the control bits Bit_1 and Bit_2.

3.3.1 Switch Matrix and High Voltage Buffers

As a ratio of the electrodes' potential difference is needed, a division operates must be performed. In this system, resistive dividers are utilized. These dividers cannot be directly connected to the electrode nodes, these nodes must first be isolated. Therefore, the buffer shown in Figure 3.12 is utilized [47]. The circuit utilizes feedback to operate as a buffer. NMOS input pair are chosen because nodes EL and EL_COM take values close to supply voltage. DC sweep simulation results of the buffer with a load of 125 kΩ for all corners are shown in Figure 3.13.

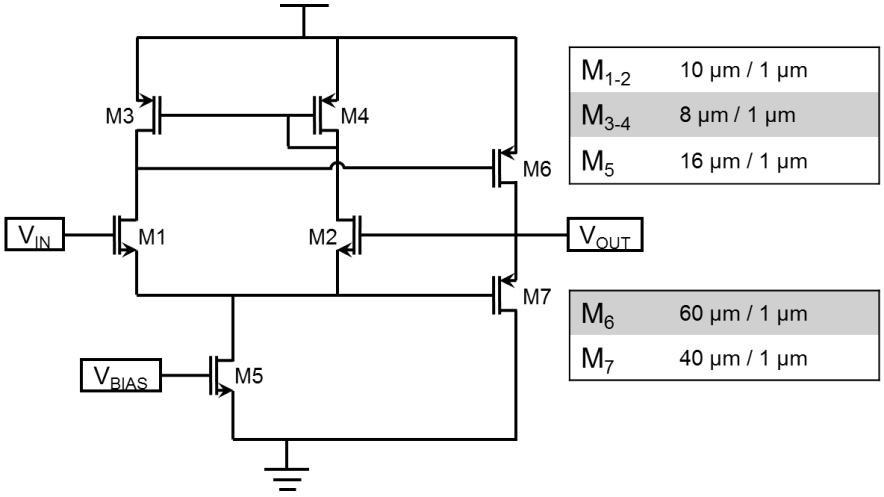


Figure 3.12. Schematic diagram of the HV buffer utilized to isolate the electrodes

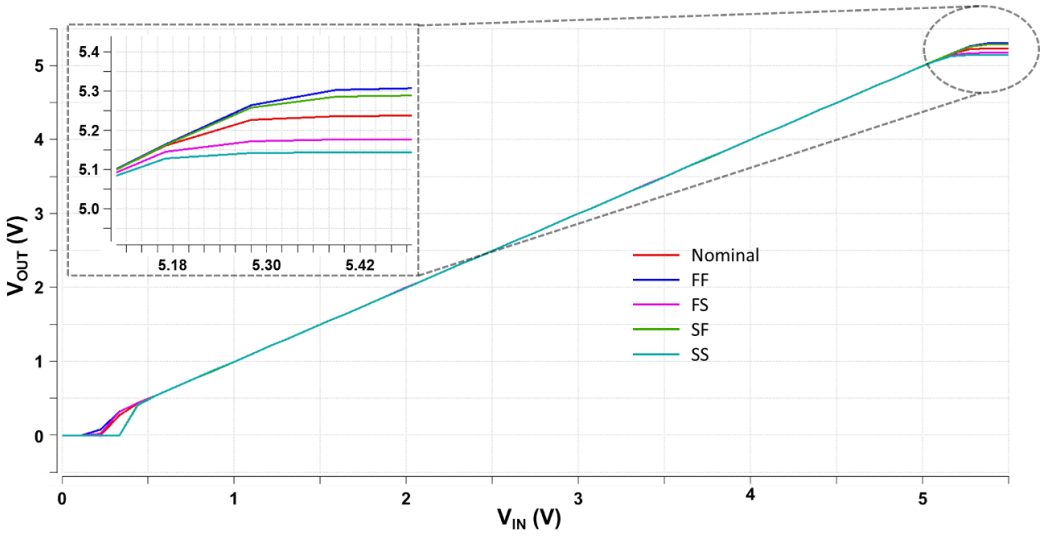


Figure 3.13. DC sweep simulation results of the HV buffer for all corners

For node EL_COM one buffer is sufficient. However, for nodes EL-1 to EL-8 additional circuitry is needed. In order to utilize only one buffer with these 8 electrodes, the switch matrix shown in Figure 3.14 is used. The control signals P and N are generated from the shift register control circuit, which will be explained later.

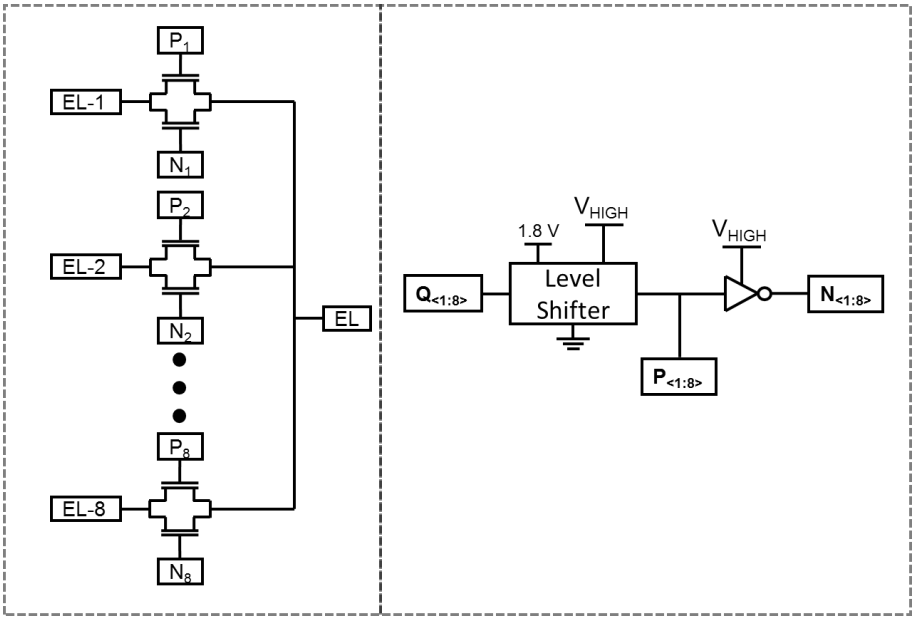


Figure 3.14. Switch matrix utilized to use one buffer with EL-1 to EL-8

3.3.2 Magnitude Arrangement and Low Voltage Buffers

Waveforms of the electrode voltages and stimulation current were presented in the previous section and are reiterated below in Figure 3.15. The individual voltage waveforms for the electrodes are also presented in this figure.

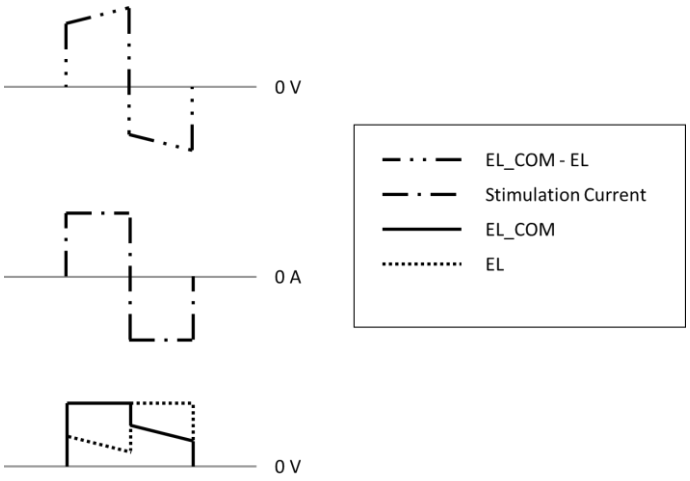


Figure 3.15. Example waveforms to stimulation current and electrode voltages

As can be seen, during one phase EL_COM voltage is greater and vice versa in the other phase. This necessitates the magnitude arrangement of electrode voltages before subtraction operation. To do this, the simple transmission gates shown in Figure 3.16 are utilized. Div_H represents the greater of the two while Div_L is the lower one. CLK_H, as will be seen later, is the clock that is used to change the electrode that is active. Here it is utilized to signal the circuit that the second phase of the biphasic pulse has started. This was illustrated in Figure 3.15. Consequently, their scaled versions Div_EL and Div_EL_COM also change magnitudes. Thus, as these divided voltages will be used to perform subtraction operation, their magnitudes must be sorted.

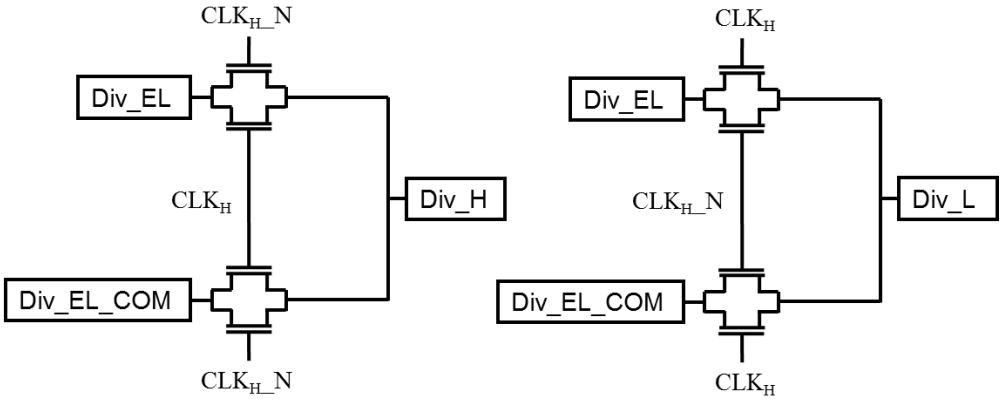


Figure 3.16. Circuitry to arrange magnitudes of electrodes

After their magnitudes are sorted they are fed to the low voltage buffers. The structure for these buffers is similar to the high voltage buffers but here they are PMOS input because the divided voltage is low. This is because their magnitudes can be 1.1 V maximum as the supply voltage is 5.5 V and the scaling ratio is one fifth. The schematic of the buffer is shown in Figure 3.17 [47]. DC sweep simulation results are presented in Figure 3.18. As can be seen the buffer operates properly from 1.1 V down to around 30 mV, which is enough for the circuit to operate properly.

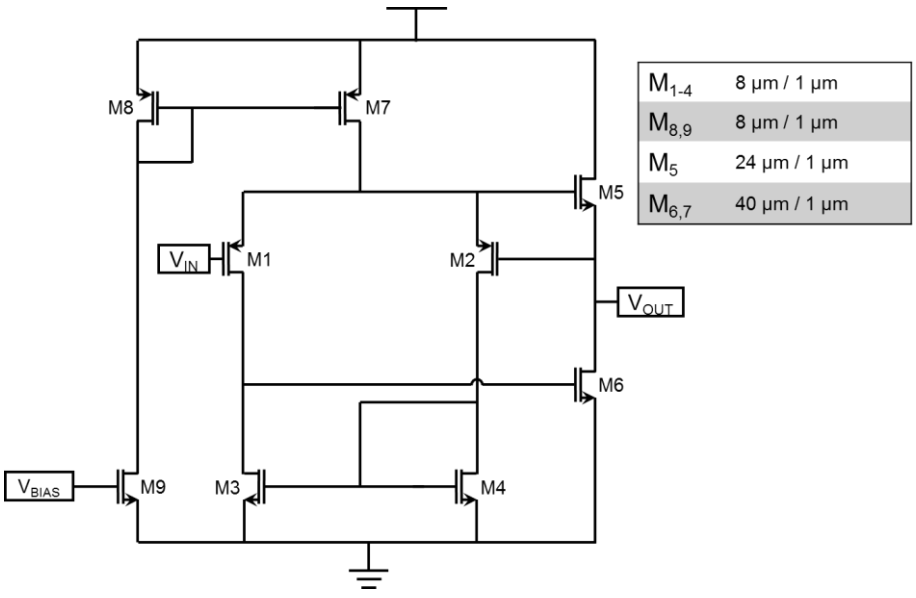


Figure 3.17. Schematic diagram of the used LV buffer

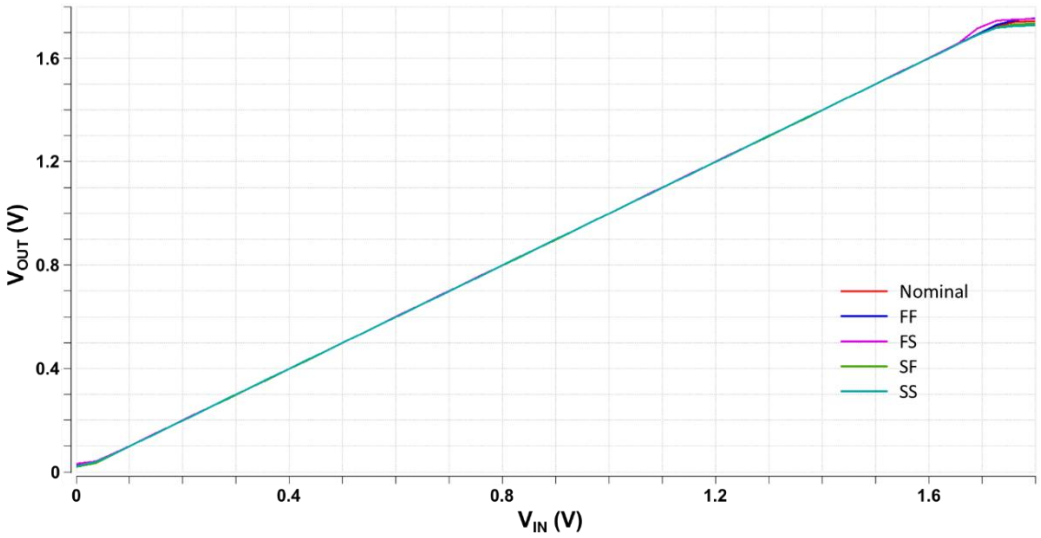


Figure 3.18. DC sweep simulation results of the LV buffer for all corners

3.3.3 Difference Amplifier and Reference Voltage Generator

Up to now the electrode voltages are divided and their magnitudes are sorted. Now, subtraction operation can be performed on these voltages. A difference amplifier structure is utilized for this purpose as shown in Figure 3.11. The amplifier used is a folded cascode with a common drain output. The schematic is presented in Figure 3.19. Low voltage cascodes are utilized to improve the swing at the output of the current summing transistors [48]. Moreover, folded-cascode structure was adopted for the same reason. As shown in an example simulation result in Figure 3.20 the amplifier performs subtraction on the input waveforms and with an offset.

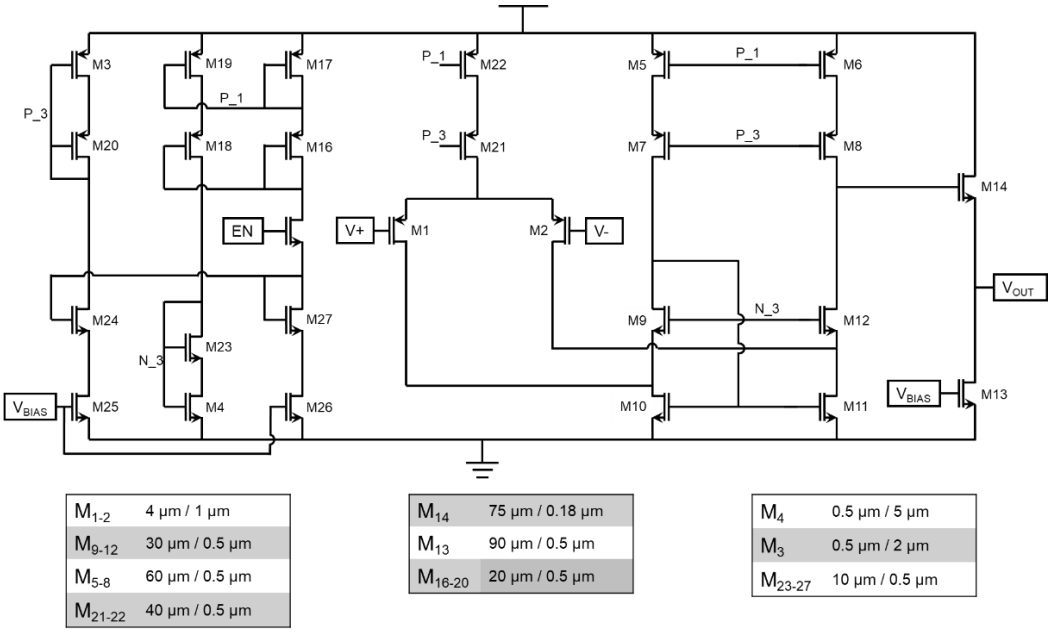


Figure 3.19. Folded cascode utilized as difference amplifier

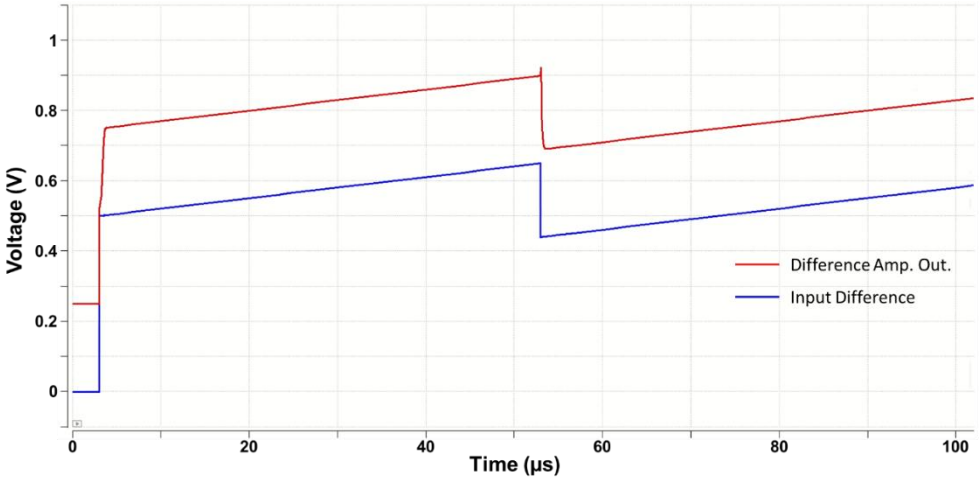


Figure 3.20. Difference amplifier input and output with offset

However, an important issue and difference to note from Figure 3.15 as opposed to the waveforms provided in Figure 3.20 is that nodes EL and EL_COM cross each other during phase change. Moreover, as the difference amplifier is performing subtraction, the resulting waveform will reach zero in this same time interval. Because the output of the difference amplifier is to be used as a reference voltage, this will prompt the charge pump to operate in 1.8 V output mode, which means the

necessary compliance voltage cannot be supplied to the neural stimulator and stimulation current will go down as a result. To overcome this issue the structure shown in Figure 3.21 is utilized. The difference amplifier continues to subtract the divided electrode voltages, however, at times of phase changes control signal REF_CONT creates a 3 µs pulse that opens the switch connecting the output of the amplifier to the capacitor. This way the reference voltage held on the capacitor at the time of phase change is used as reference voltage for 3 µs. Afterwards the output of the amplifier is connected to the capacitor again and continued to be used as reference.

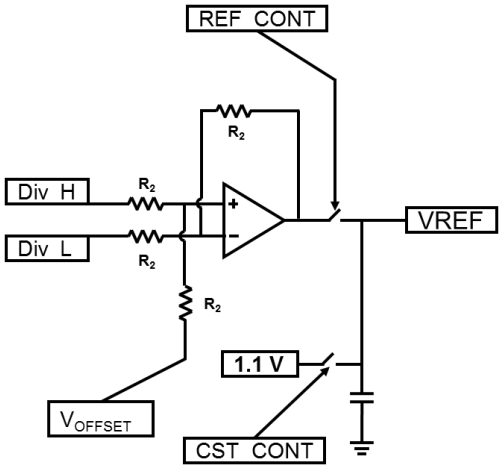


Figure 3.21. Circuit used to perform subtraction operation

The other control signal CST_CONT shown in the same figure is used for another purpose. The system does not extract information about the stimulation current magnitude or the neural load. In other words, when one stimulation period ends, the system does not know whether the subsequent period will need higher or lower supply voltage. In the case of a higher supply voltage requirement, the current source within the neural stimulator will not have the required voltage compliance and the correct stimulation current will not be created. Thus, to ensure every stimulation period has the necessary voltage compliance, the charge pump's output is reset at the end of each one. The duration of the stimulation is set to be 128 µs. An additional counter is used to count to 123 with 1 µs clock period to generate CST_CONT and give the charge pump 5 µs to pull its output to 5.5 V, hence the 1.1 V reference

voltage. The reason for maximum 5.5 V supply voltage is due to the terminal voltage limitations of the high voltage transistors used in the stimulator. Circuits used to generate the control signals REF_CONT and CST_CONT are illustrated below in Figure 3.22 and Figure 3.23, respectively. The signal depicted as CLK is a 1 MHz clock and is provided externally. The circuits can be explained as follows. For Figure 3.22, there's two of the same structure. For the one above, the D-flipflop's output is pulled to HIGH so that the 3-bit counter can start counting. As it is counting, its bits are compared to the given digital 3-bit value. During this period A is HIGH. When the output of the comparator becomes low when the two values are equal, D-flipflop is reset and A goes to LOW. The same operation is valid for the structure below, but this time it operates at the negative edge of D<0> while the one above operates at the positive edge. This way, in both phase changes these pulses are generated.

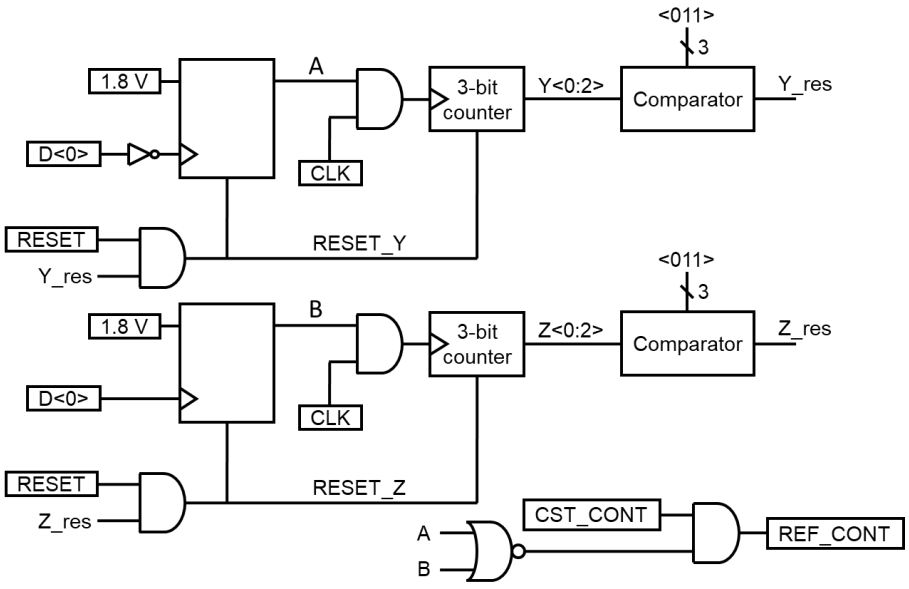


Figure 3.22. Circuitry used to generate REF_CONT

Finally, for the combinational logic at the bottom, REF_CONT goes to LOW when either of A or B is HIGH, turning off the switch connecting REF_CONT to VREF. CST_CONT can also be seen at the input of the AND gate so that the switch connecting REF_CONT to VREF is not ON when the one connecting CST_CONT is ON.

For Figure 3.23, a similar structure is employed. This time, the counter is 7-bit and the value that it is being compared to is different. At the negative edge of D<0>, which is when a stimulation period starts, the counter starts. When it reaches the predefined value, which is 5 µs before the stimulation period ends, HALT signal resets the flipflop and CST_CONT goes to low, severing VREF from the output of the difference amplifier and connecting it to 1.1 V.

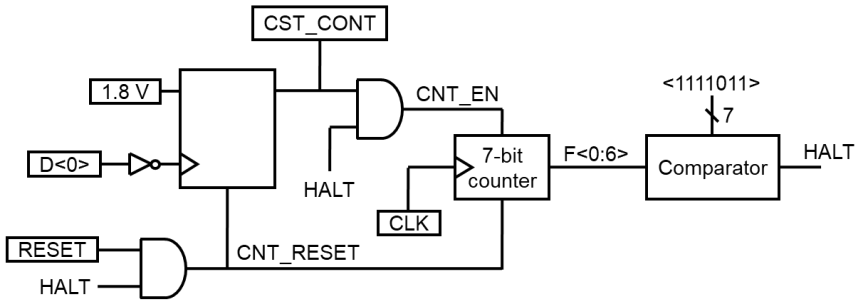


Figure 3.23. Circuitry used to generate CST_CONT

The signal D<0> is again a control signal from the shift register. The resulting reference voltage when CST_CONT control signal is added to the structure is shown in Figure 3.24. This voltage will be used in the PFM regulation of the charge pump as well as in the flash ADC to determine the number of operational charge pump stages, which is detailed next.

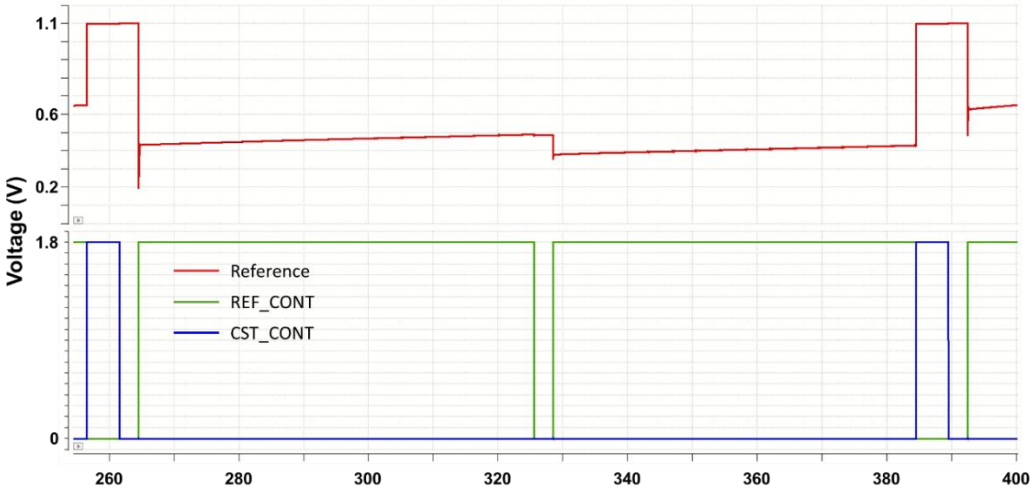


Figure 3.24. CST_CONT, REF_CONT and obtained reference voltage for the charge pump

3.3.4 Flash ADC and Control Signals

The output of the difference amplifier in the previous subsection was regarded as the reference voltage to be used for PFM. It was also mentioned that a 3-stage charge pump is used in the system. Moreover, the background information about switched-capacitor converters explained that in order to keep the efficiency high, the conversion ratio of the charge pump should be manipulated. Thus, the number of operational charge pump stages needs to be altered. Bit_2 and Bit_1 are utilized for this purpose. Previous system used an external controller and the entered load information to create the control signals. In the improved version a flash ADC is used to generate these signals as shown in Figure 3.25. The schematic of the hysteresis comparator used in Figure 3.25 is shown in Figure 3.26.

Resistive dividers are used to generate the voltages for the hysteresis comparator to compare the reference voltage to and they are connected to the input voltage of the charge pump. This way these voltages can move up and down with the supply voltage and the charge pump can keep operating with better efficiencies. The reason for this can be explained as follows. It was demonstrated that switched-capacitor converters have discrete conversion ratios and they operate the most efficiency when they are regulated to voltages that are closest to these discrete conversion ratios. Thus, while the charge pump may be operating the most efficient with two stages for 7 V output with 3.3 V input, only one stage is sufficient when the input is recharged to 4 V. Looking at issue from the opposite view is also enlightening. While the converter can provide 7 V output with only one stage for 4 V battery voltage, two stages are needed when the battery discharges to 3.3 V.

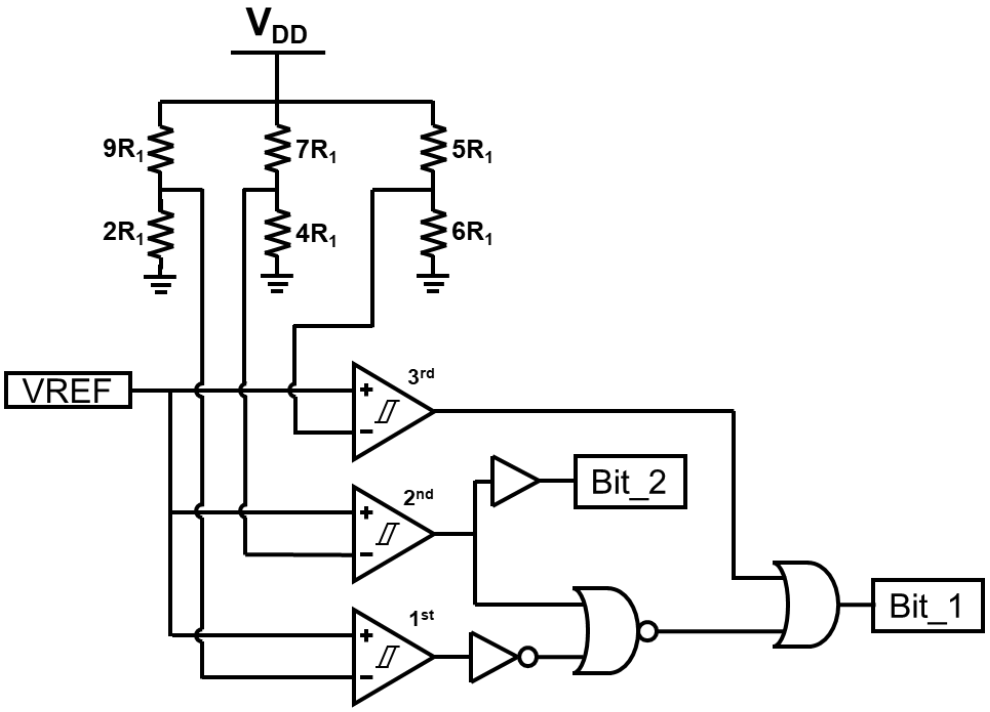


Figure 3.25. Flash ADC and creation of Bit_1 and Bit_2

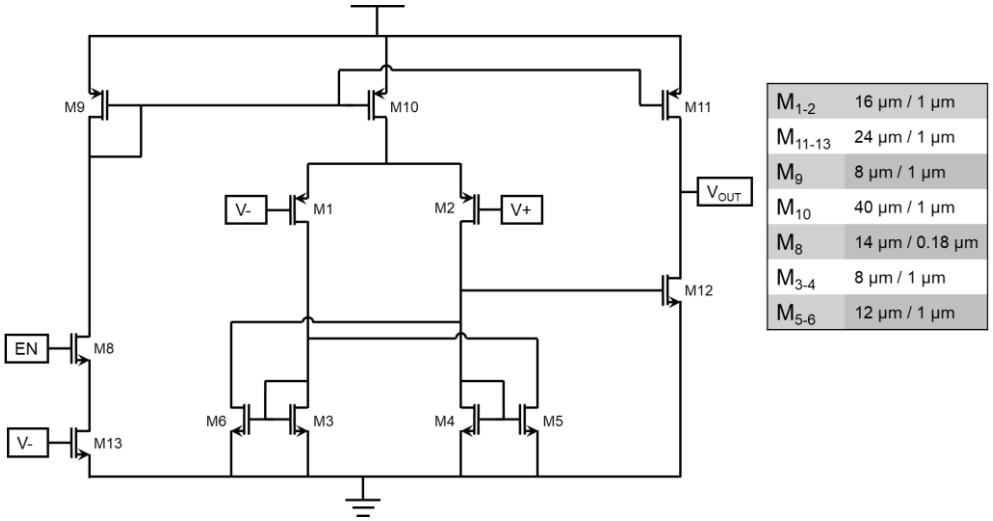


Figure 3.26. Hysteresis comparator used in the flash ADC

Hysteresis comparators were utilized to overcome issue with glitches. Figure 3.27 shows the DC sweep simulation of the comparator for all corners. They all give the same hysteresis window, which is why it seems there is only one waveform.

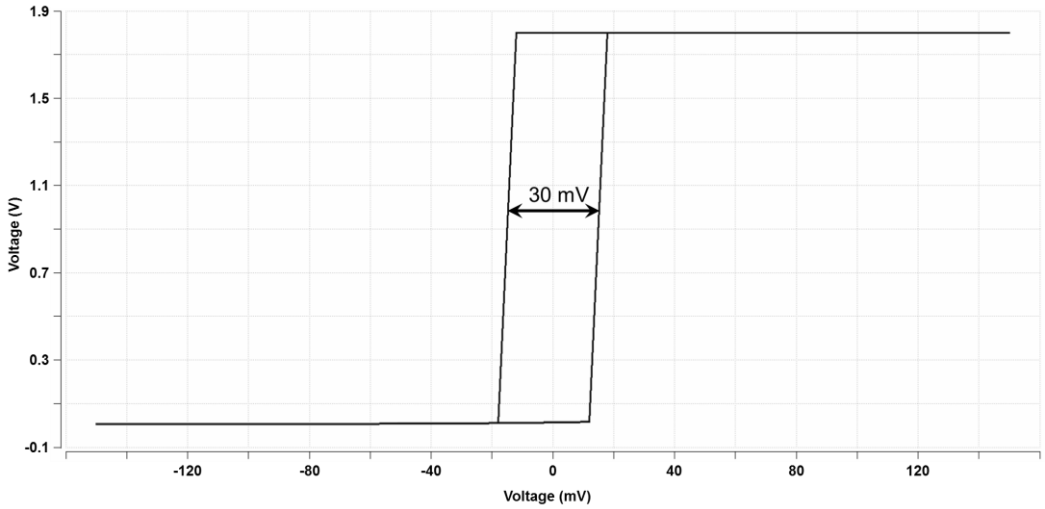


Figure 3.27. DC sweep simulation result of the hysteresis comparator for all corners

3.3.5 H-Bridge and Control Circuitry

The adaptive converter is designed to supply a neural stimulator with the proper compliance voltage. The stimulator is part of an interface circuit for a fully implantable cochlear implant and in this work the neural stimulator of a previous work is used [6]. To create the biphasic current pulse used for neural stimulation the H-bridge shown below in Figure 3.28 is utilized. Control signals D<0:8> and C<0:8> are utilized to direct the current created by V_{STIM} to form a biphasic current pulse.

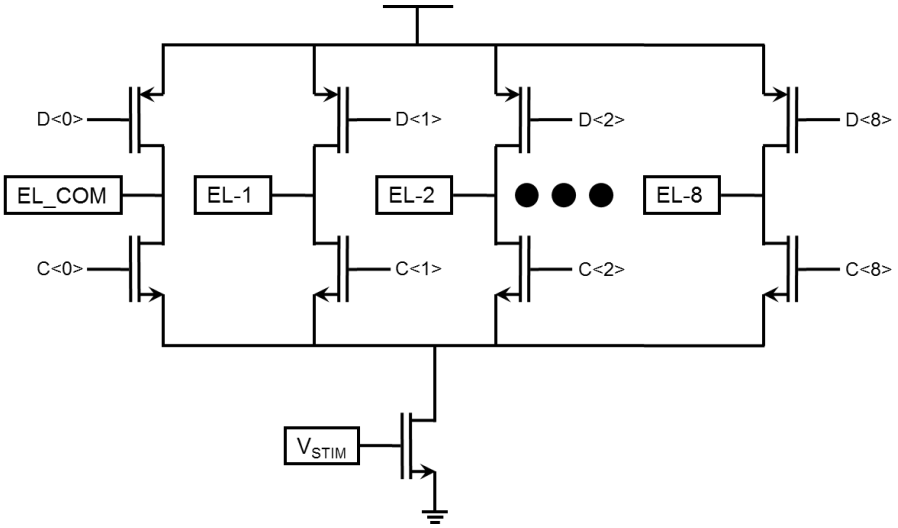


Figure 3.28. Schematic diagram of H-bridge used for biphasic pulse

As was shown in Figure 3.22 and Figure 3.23, D<0> was also utilized to generate additional control signals. Its positive and negative edges were used to do this. The generation of D<0:8> and C<0:8>, on the other hand, was done with the shift register shown in Figure 3.29 and additional combinational circuitry. CLK_H and CLK_L shown in this figure are obtained from the 1 MHz CLK signal that was previously shown in Figure 3.22 and Figure 3.23 as well. CLK_H's period is 128 µs, while CLK_L's is 1024 µs. The shift register starts operating with the positive edge of CLK_L and the pulse generator creates a HIGH pulse. This pulls Q of SR latch to HIGH as well and after a delayed CLK_H arrives at the clock input of the D-FF, Q<1> becomes HIGH. To overcome Q<1> becoming HIGH in the next state as well the SR latch's output is reset when Q<1> is HIGH. This way, with the subsequent positive edge of CLK_H, Q<2> becomes HIGH and Q<1> goes to LOW. Thus, the HIGH bit is shifted withing the register. Simulation result showing this is provided in Figure 3.30.

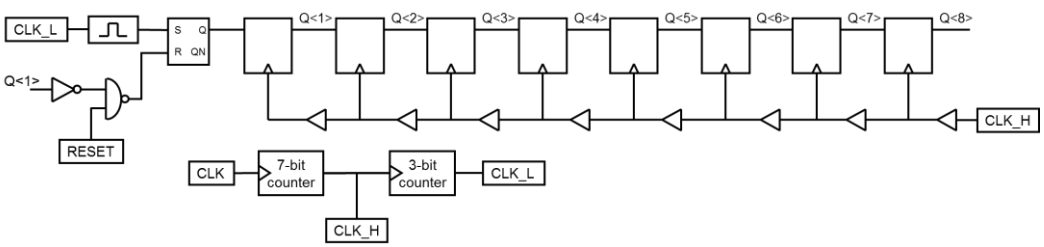


Figure 3.29. Shift register used to generate the control bits

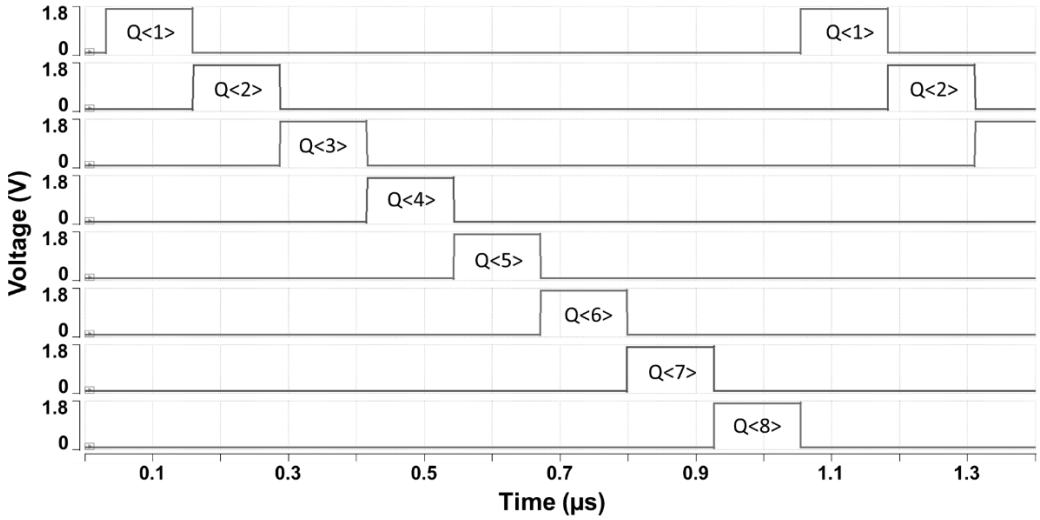


Figure 3.30. Simulation result showing operation of shift register

The bits of the shift register Q<1:8> were also used in the circuit illustrated in Figure 3.14. These are the signals that control the switch matrix connecting EL-1 to EL-8 and the HV buffer. In other words, as Q<1:8> denotes which electrode is active, it is also used to connect that electrode to the buffer. Simulation result showing an example potential difference for a sequence of 8 stimulation electrodes is shown in Figure 3.31.

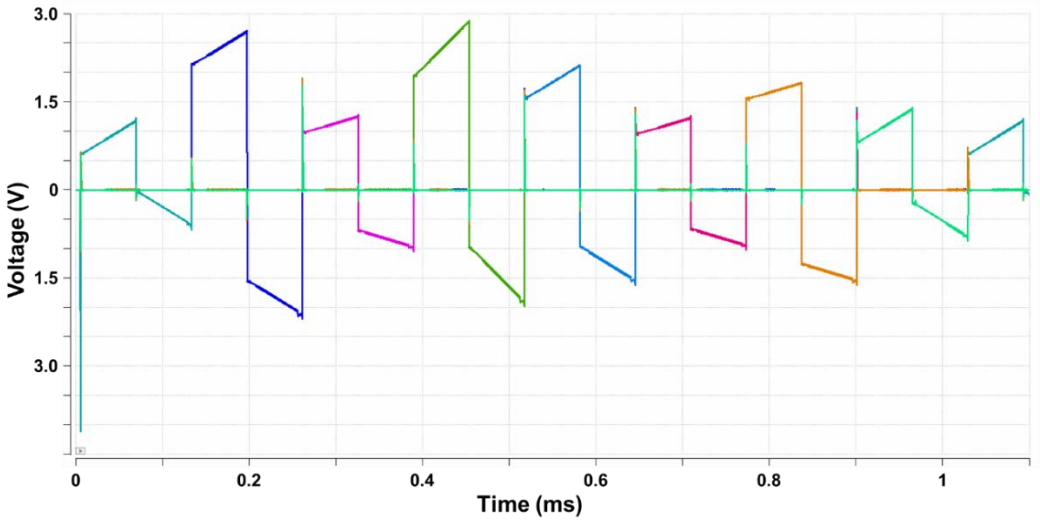
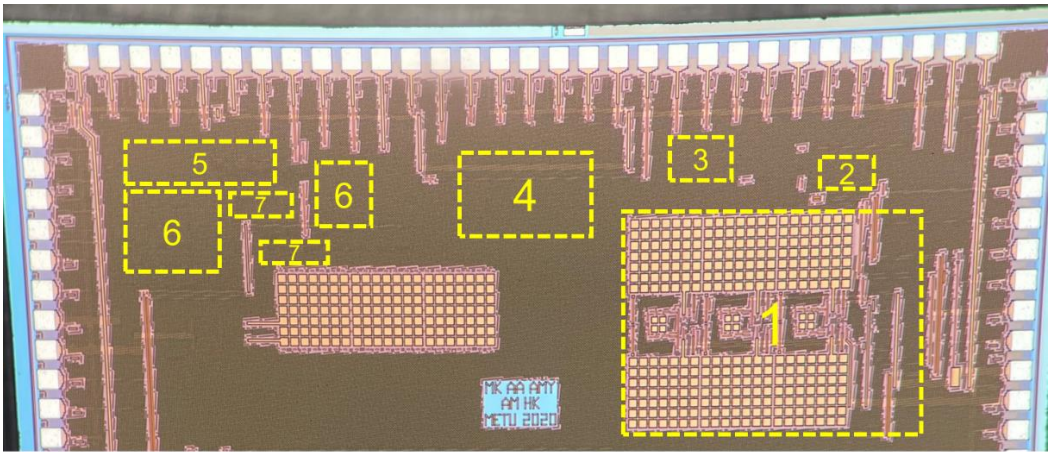


Figure 3.31. Example waveforms for a sequence of 8 stimulation electrodes

3.4 Experimental Results

The adaptive converter system was implemented in TSMC 180 nm High Voltage BCD process. Figure Figure 3.32 shows the micrograph of the design.



1- 3-stage CP
2- PFM Control
3- Difference Amp.
4- Buffers
5- H-Bridge
6- Level-Shifters
7- Control

Figure 3.32. Micrograph of the design

A PCB is designed for test purposes (Figure 3.33). An 8-channel system was used to test the system (Figure 3.28). The three-element electrical model of the electrode-tissue interface (Figure 1.3 (a)) was taken in mind and a series R-C load was connected between the electrodes. The input of the system was set to 1.8 V.

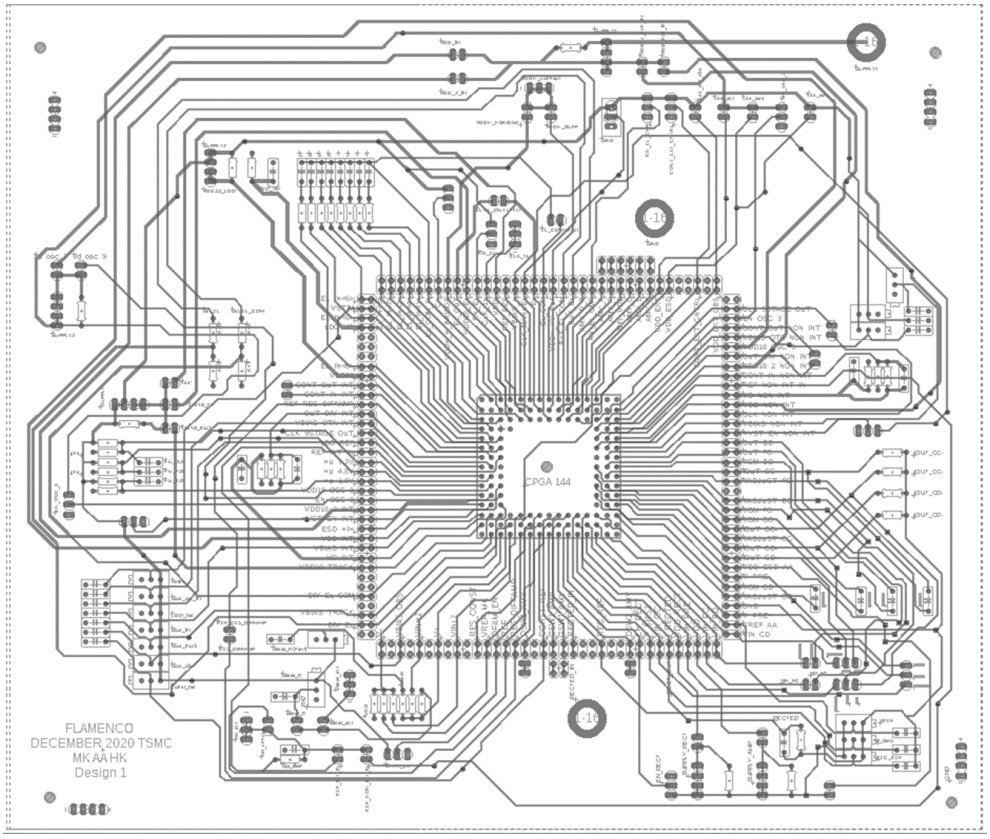


Figure 3.33. Adaptive converter test PCB

The following sub-sections will provide waveforms from sub-blocks where the charge pump is operating in both constant 5.5 V output and adaptive mode.

3.4.1 Step-Up Converter

Firstly, power measurements were performed on the step-up converter to assess its performance. Figure 3.34 shows the power efficiency values of the converter for different load resistances and output voltage levels. Similar to the efficiency graph shown previously in Figure 2.5 (b), the waveforms exhibit valleys and peaks. This is a results of changing the conversion ratio of the converter according to the required output voltage. Maximum efficiency was observed for 3 V output and 6.86 kΩ load, which was 79%.

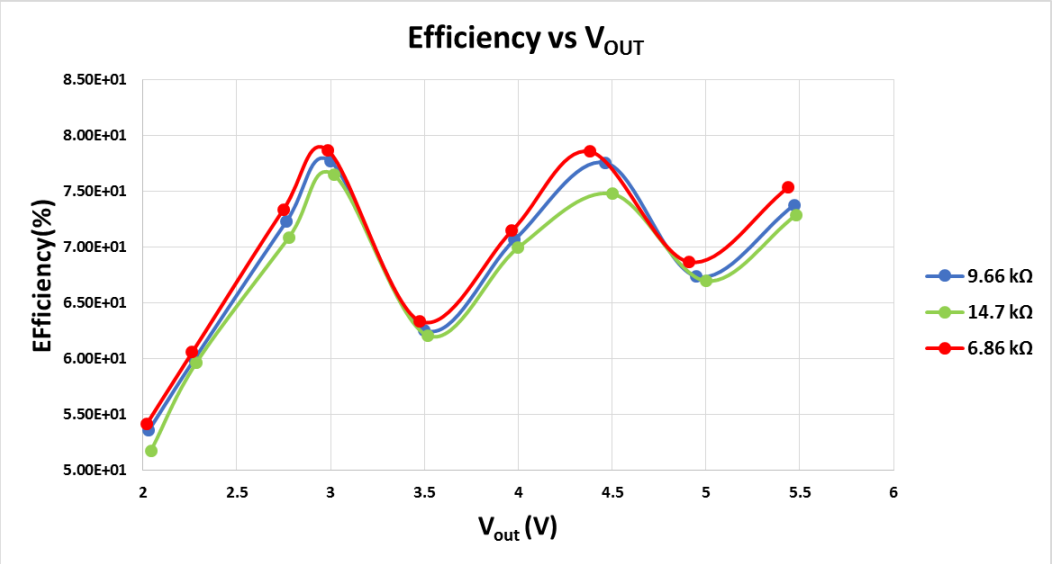


Figure 3.34. Efficiency of the step-up converter vs V_{OUT} and varying loads

3.4.2 HV Buffers

HV buffers were utilized to isolate the electrodes. Figure 3.35 and Figure 3.36 show the waveforms for these buffers. Figure 3.35 shows the waveforms for the buffer that is connected to EL - #, while Figure 3.36 shows the one that is connected to EL_{COM}. In both cases, (a) depicts the waveforms when the supply, which is the output of the CP, is kept constant at 5.5 V. (b), on the other hand, is the case where the CP is operating in its adaptive mode.

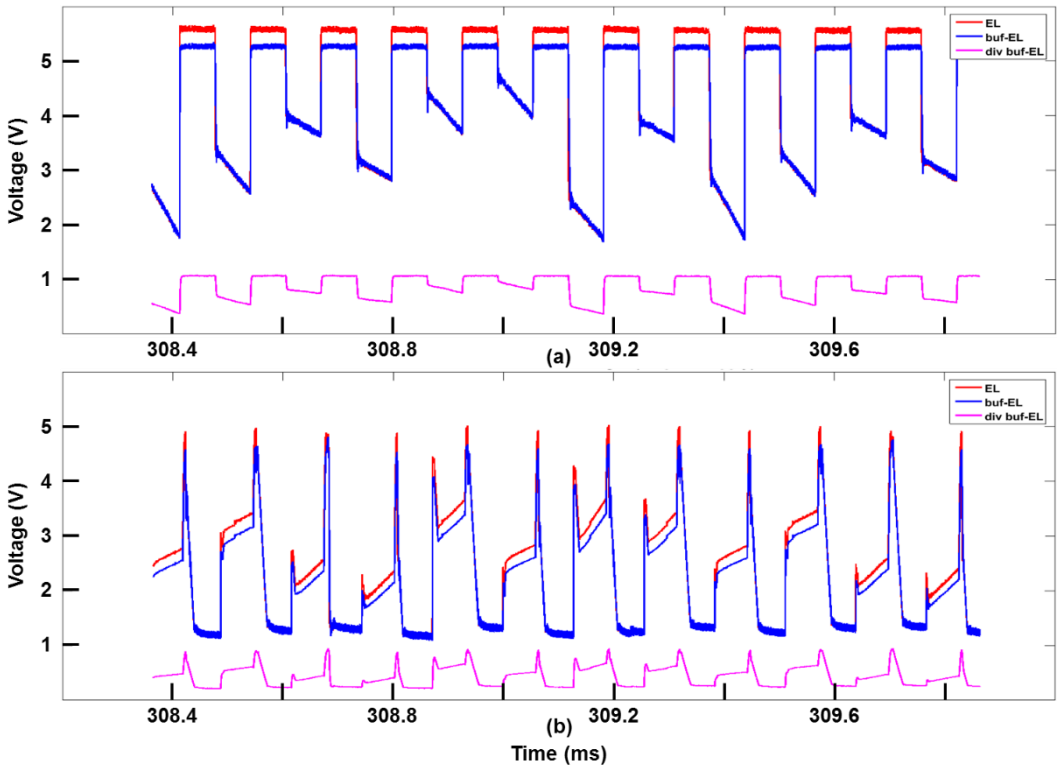


Figure 3.35. Input and output waveforms for HV buffers (EL - #) and after resistive division for (a) constant 5.5 V supply (b) adaptive supply

As can be seen the buffer is operating properly. The instances where the buffered output cannot exactly reach the electrode voltage is due to the fact that lower resistance is used for the divider at the output of the divider (30 kΩ for R_3 in Figure 3.11) than anticipated due to parasitics. However, this is easily fixed with the offset that is provided in the difference amplifier. Also shown in these figures is the output of the resistive divider, which will be transmitted to the next stage of the tracking circuitry. These are reiterated in Figure 3.37 where the scaled versions of EL - # (div buf-EL) and EL_{COM} (div buf-EL_{COM}) can be seen.

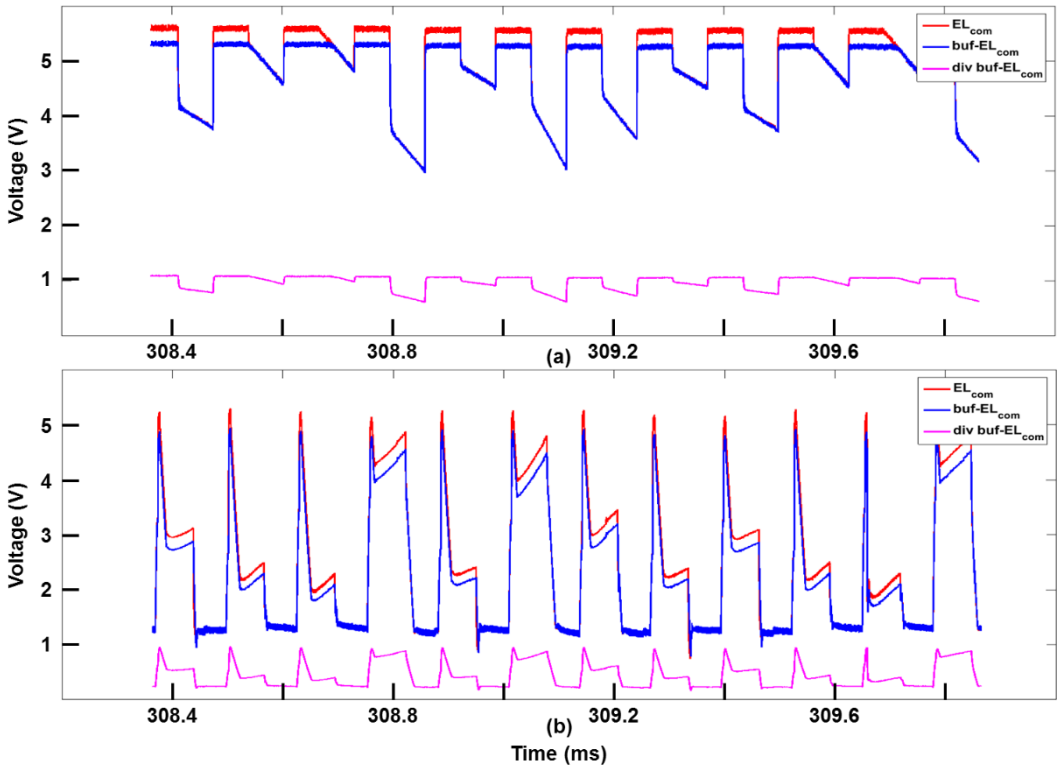


Figure 3.36. Input and output waveforms for HV buffers (EL_{COM}) and after resistive division for (a) constant 5.5 V supply (b) adaptive supply

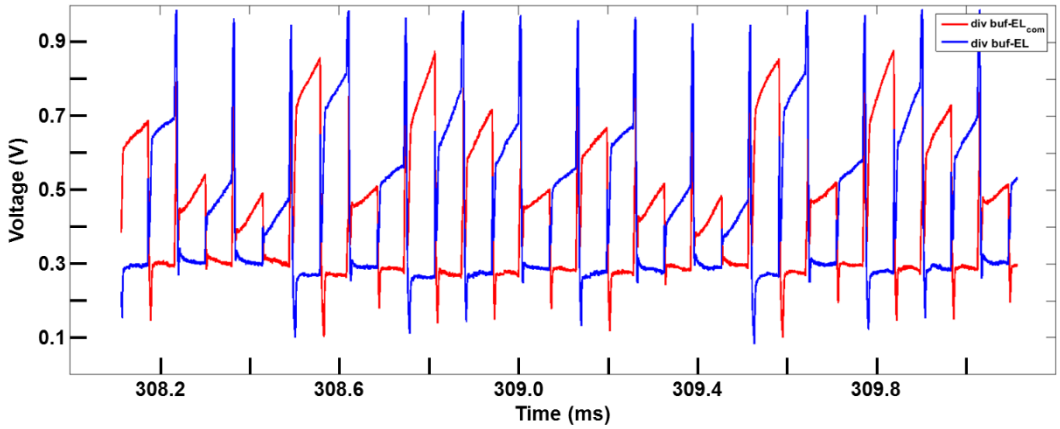


Figure 3.37. Scaled electrode voltages

3.4.3 Magnitude Sorting and Reference Generation

Subsequent to generation of the scaled electrode voltages, they are sorted so that proper subtraction operation can be performed. Figure 3.37 showed the scaled electrode voltages, while Figure 3.38 shows them after sorting. VinH represents the greater voltage, thus, VinL is to be subtracted from VinH.

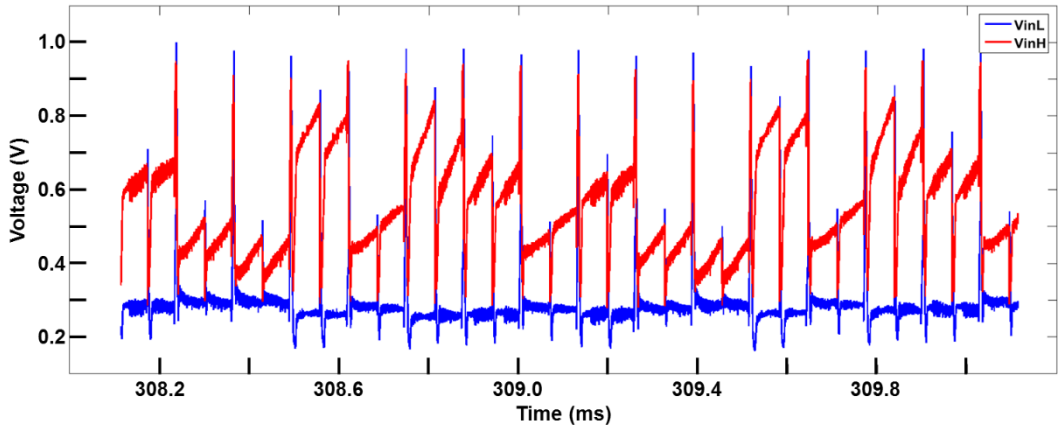


Figure 3.38. Sorted scaled electrode voltages

Hence, Figure 3.39 shows the difference between VinH and VinL calculated in MATLAB from individually obtained waveforms as well as the generated reference voltage. To put it another way, VinH-VinL is the input of the difference amplifier and the reference voltage is the output.

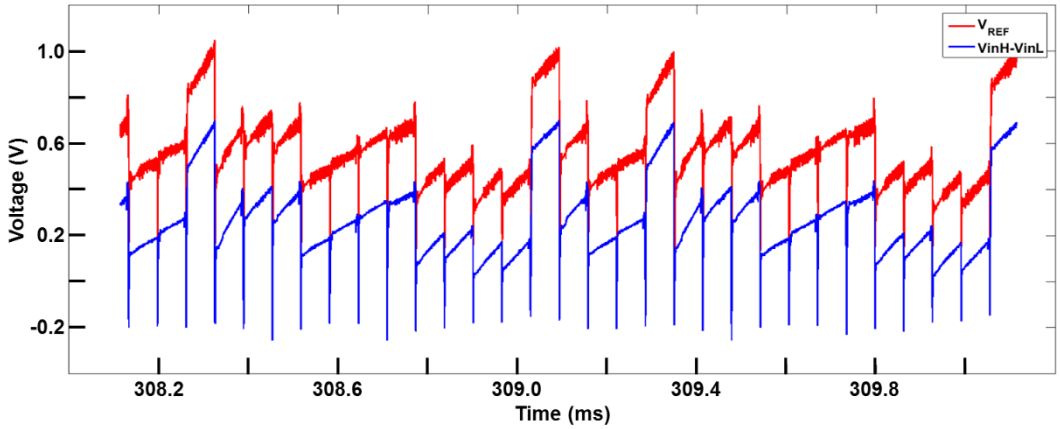


Figure 3.39. Input and output of difference amplifier

As can be seen, the difference amplifier operates as it should and the difference of the of the signals at the input are obtained. Moreover, the required offset is added to the reference voltage and it can be provided to the converter to perform regulation.

3.4.4 Overall System

The previous subsections provided the waveforms of the internal nodes of the design. This subsection provides the electrode voltage and the converter's output, confirming the operation of the design. Moreover, power measurements of several scenarios are provided showing that the system is achieving its goal.

To prove that the concept works, the system is tested with two different sets of artificial loads. Table 3.2 shows the first set of loads connected to the electrodes. These loads were tested with four different current magnitudes.

Table 3.2 Artificial load values for the electrodes, set-1

EL - #	**R (kΩ)**	**C (nF)**
EL - 1	1.98	33
EL - 2	7.05	33
EL - 3	3.13	68
EL - 4	6.36	20
EL - 5	5.12	33
EL - 6	3.13	68
EL - 7	5.12	68
EL - 8	2.65	33

Figure 3.40 through Figure 3.43 show the waveforms for the electrode voltages and the charge pump outputs for cases where the stimulation current's magnitude is 450, 300, 230 and 140 μA, respectively. Waveforms in (a) show the converter operating in constant mode and the ones in (b) illustrate the converter switched to its adaptive

mode. As can be seen, the converter can follow the electrode voltages when it is switched to adaptive mode.

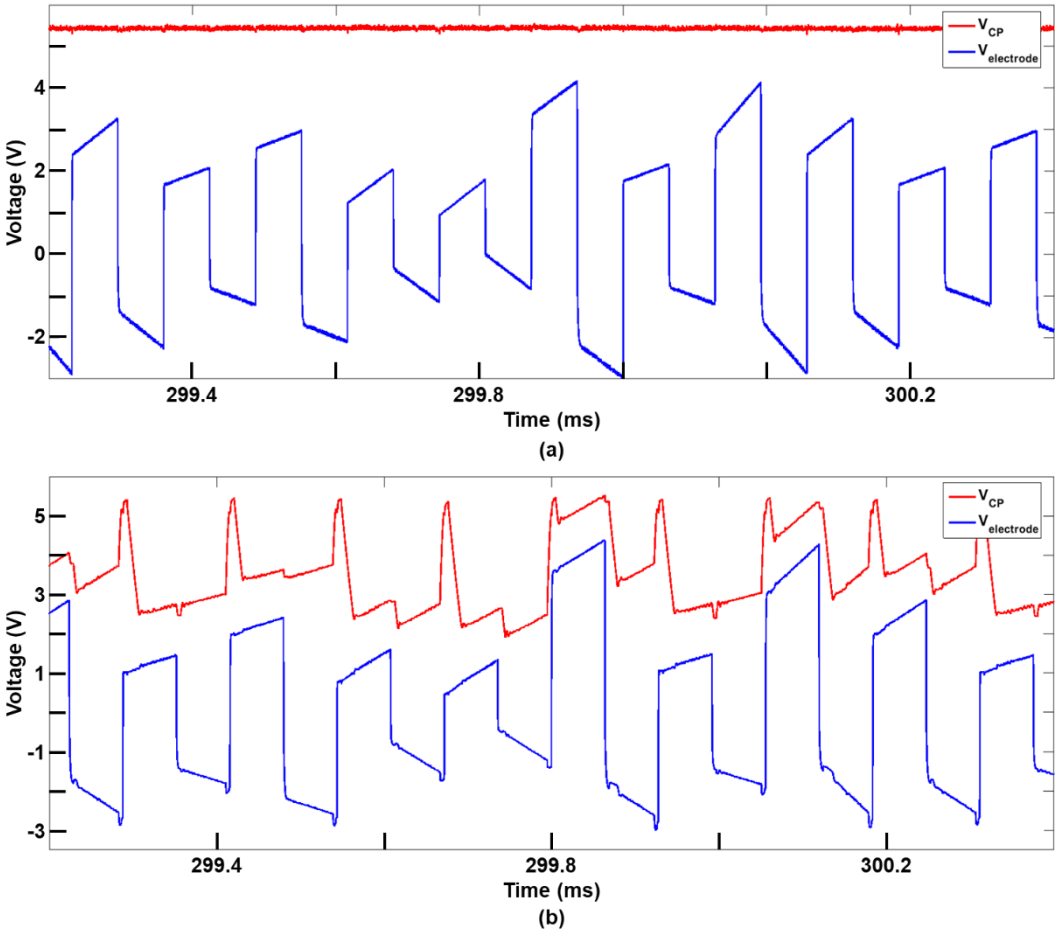


Figure 3.40. Electrode voltages and CP output for 450 µA and loads in Table 3.2 (a) constant mode (b) adaptive mode

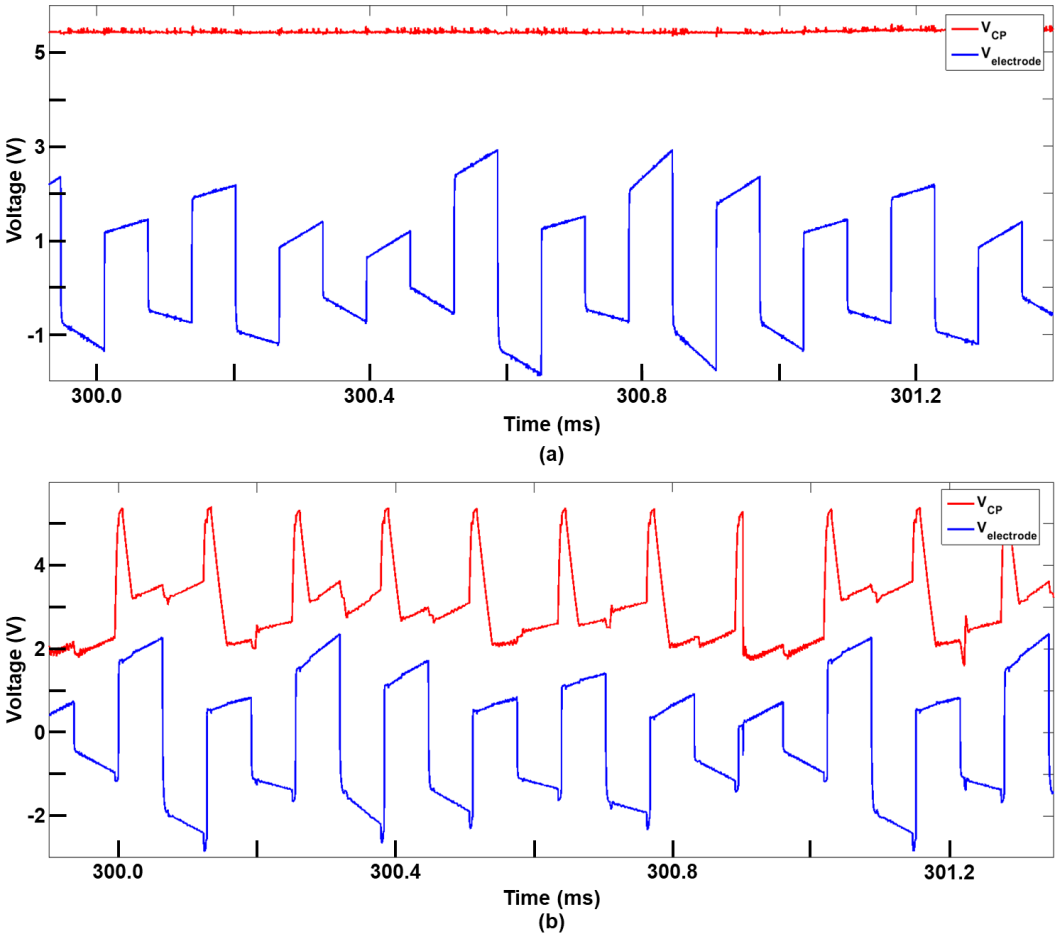


Figure 3.41. Electrode voltages and CP output for 300 µA and loads in Table 3.2 (a) constant mode (b) adaptive mode

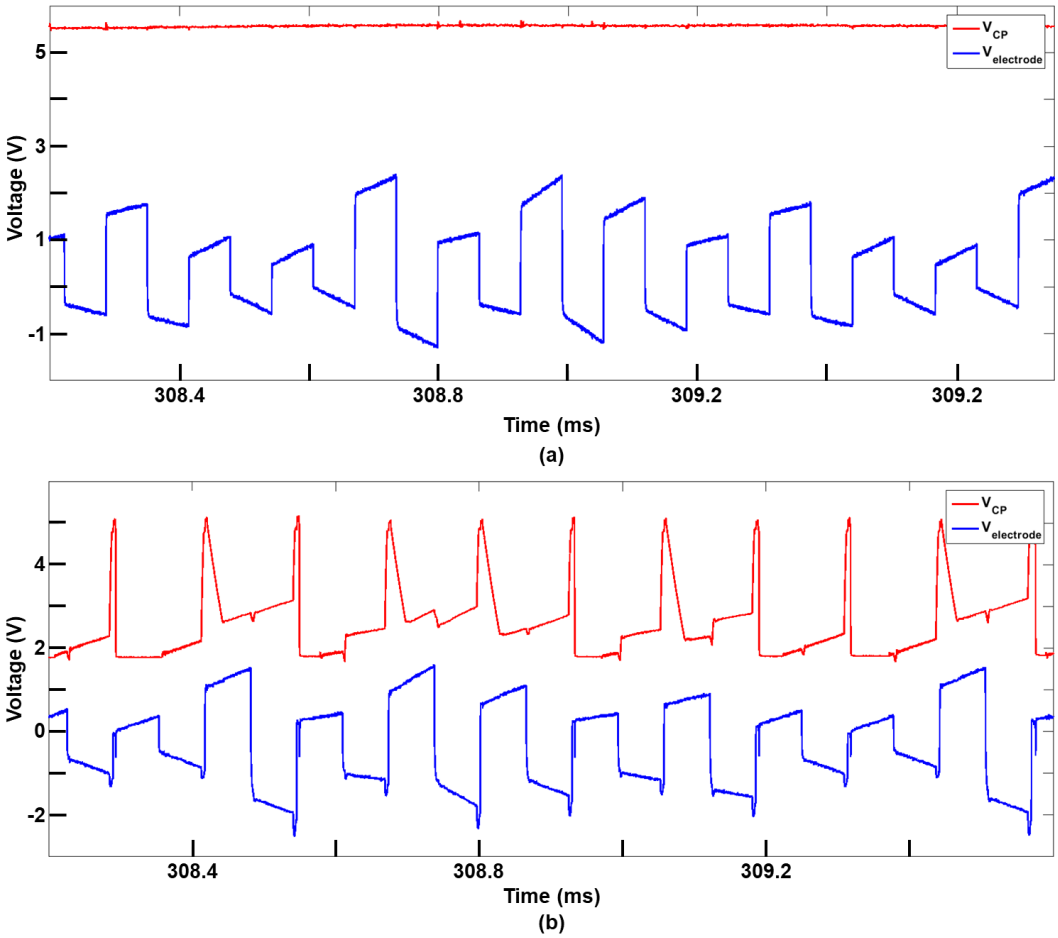


Figure 3.42. Electrode voltages and CP output for 230 µA and loads in Table 3.2 (a) constant mode (b) adaptive mode

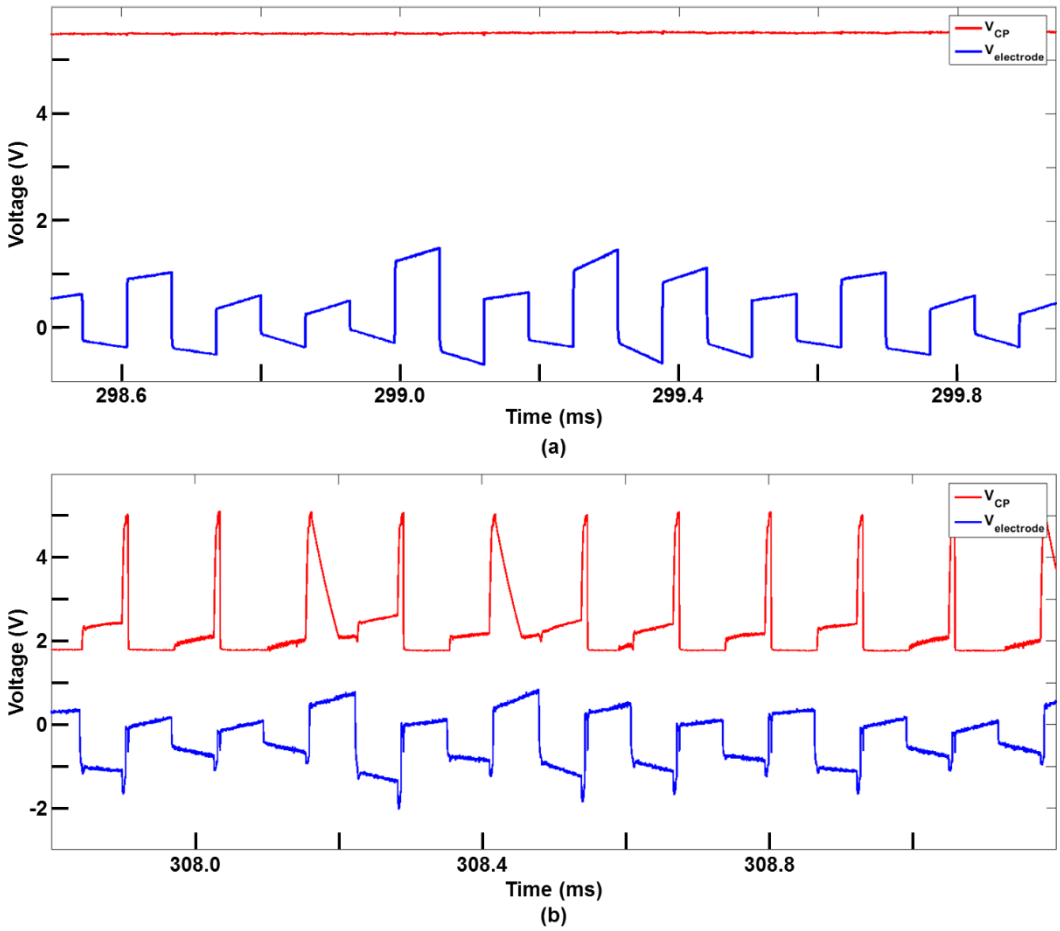


Figure 3.43. Electrode voltages and CP output for 140 µA stimulation current and loads in Table 3.2

Moreover, the system is tested with another set of artificial loads to verift that it can operate with different loads as well. The values for the second set are given in Table 3.3. The waveforms for this set is provided in Figure 3.44. As shown, the converter is operating with changing load values as well.

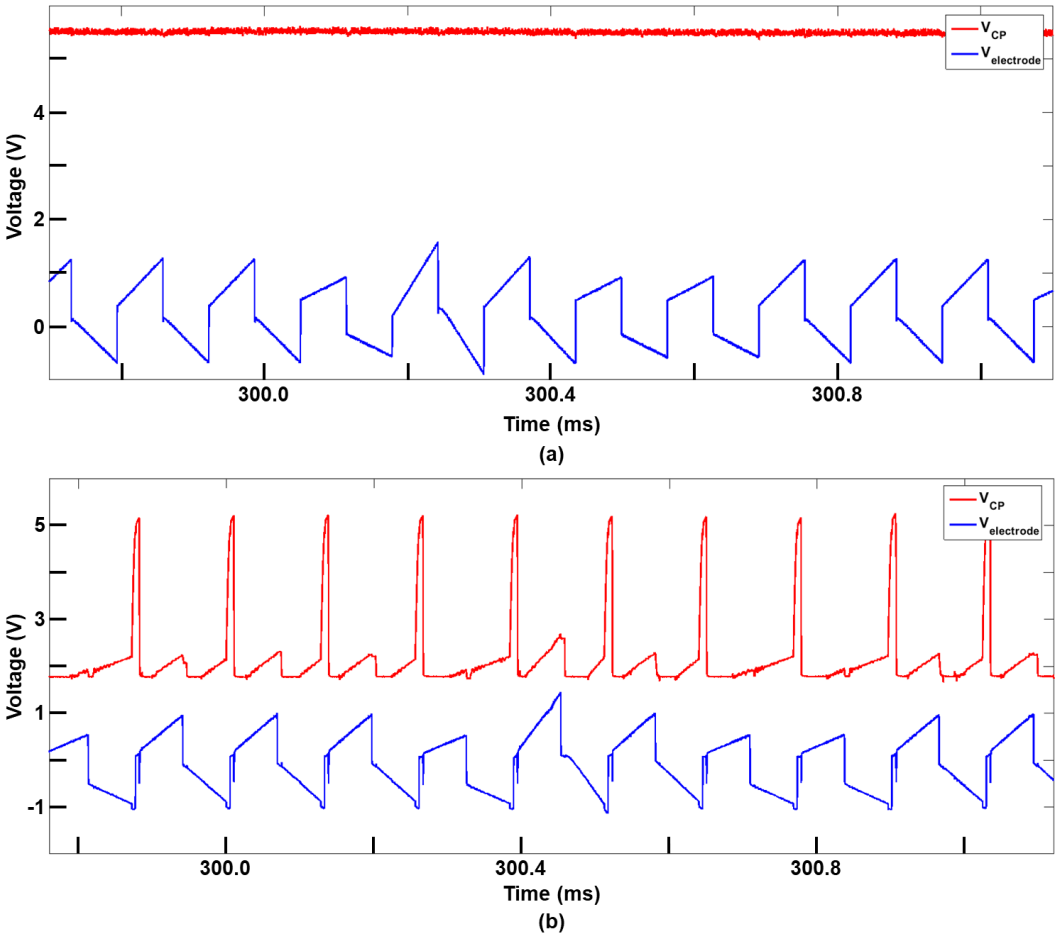


Figure 3.44. Electrode voltages and CP output for 470 µA and loads in Table 3.3 (a) constant mode (b) adaptive mode

One can note from the waveforms above that the electrode voltages have notches when the CP's output rises or falls quickly. These can be attributed to the parasitic capacitances at nodes EL-# and EL_COM. These parasitic capacitances result from the oscilloscope probes, which are 11 pF. When the supply voltage of the H-bridge is changed quickly, the voltages of these nodes must transition accordingly. Thus, the parasitics at these nodes will have charge or discharge currents. According to KCL, this affects the stimulation current passing through the load during the transition period. As the parasitic capacitances of the probes are much larger than these nodes normally would have been, the resulting waveforms have more dramatic artifacts. Moreover, these artifacts are observable when the output of the converter

is connected to the input supply directly, which is 1.8 V. As a results, the transition is quicker compared to the other waveforms provided, increasing the charge/discharge currents of the parasitics. Slowing this transition similar to the other waveforms will also decrease the notches present in the waveforms. Furthermore, adding a charge balance method [36] will improve the system and ensure that the charges delivered in both phases are equal. The fact that the converter provides a continuous range of output levels as opposed to discrete levels is an advantage in this regard. Changing the output of the converter to different discrete values during stimulation will no doubt increase the number of these artifacts.

Table 3.3 Artificial load values for the electrodes, set-2

EL - #	**R (kΩ)**	**C (nF)**
EL - 1	1.05	33
EL - 2	1.05	33
EL - 3	1.05	68
EL - 4	1.05	20
EL - 5	1.05	33
EL - 6	1.05	68
EL - 7	1.05	68
EL - 8	1.05	33

The main purpose of the system was to decrease power consumption. Therefore, power measurements were performed on scenarios for the waveforms provided above to see if this was the case. Table 3.4 presents the power dissipation results for the converter where it is operating in its constant and adaptive mode for the same load and stimulation current magnitudes. In its constant mode, the converter is supplying the H-bridge that is stimulating the load values given above with constant 5.5 V supply voltage. Accordingly, a 1.1 V reference is provided to regulate the output at this level for varying load currents. For the adaptive mode, however, the voltage tracking circuit is operating so that it can create the reference voltage

necessary for the converter to adapt its output according to the potential difference between the electrodes, as was shown in the figures above. The results below show that there is indeed some reduction in power dissipation when the converter is operating in its adaptive mode compared to its constant 5.5 V output configuration.

Table 3.4 Power dissipation comparison for constant and adaptive mode

	Constant (5.5 V)	**Adaptive**		
I_{STIM} (μA)	**Power Dissipation (mW)**		**Reduction (%)**	**Load set**
450	3.46	2.79	19.36	Set-1
300	2.35	1.86	20.85	Set-1
230	1.79	1.35	24.58	Set-1
140	1.13	1.04	7.96	Set-1
470	3.63	2.33	35.81	Set-2

The table shows that the reduction in power dissipation decreases for lower level stimulation currents compared to its constant operation mode. However, if the magnitude becomes too low, the reduction in power dissipation decreases as well. This can be attributed to the power dissipation of the auxillary circuits, such as the buffers and the difference amplifier. Moreover, it was mentioned that the resistive divider at the output of the HV buffers had lower resistance than anticipated due to parasitics. Thus, its contribution to increase the power dissipation of the auxillary circuits was greater than anticipated as well.

Moreover, as mentioned, the first set shows shows that the system does indeed reduce power dissipation. However, the second load set shows that smaller loads are where the greatest power saving occurs. A 35.81% reduction in power dissipation for 470 μA stimulation current demonstrates this. As the load is smaller, lower voltage compliance is needed, and because the stimulation current is not that low, the power dissipation reduction is greater compared to the first scenarios. Set-2 also

shows that the power saving of the converter depends on the neural load it is supplying.

3.5 Summary of the Chapter

In this chapter, an adaptive converter system that provides 1.8 V to 5.5 V supply voltage from a 1.8 V supply is presented. The system uses HV buffers to isolate the electrodes and scale their voltage to on fifth of their values with resistive dividers. Subsequently, these scaled electrode voltage are sorted depending on the phase of the biphasic current pulse. This way, correct subtraction is performed and a scaled down version of the electrodes' potential difference is obtained with an offset. This scaled voltage is then used to perform PFM regulation and determine the number of operational charge pump stages in the charge pump, which, incidentally has three stages due to the necessary voltage range.

The design is implemented in 180 nm TSMC process and experimental tests are performed to verify the method to decrease power consumption. Tests show that the converter is able to provide the stimulator with a supply ranging from 1.8 V to 5.5 V. The reduction in stimulation current for a specific set of artificial loads shows an increasing reduction in power dissipation. Lower neural tissue loads show a more profound reduction in power dissipation which reaches more than 35%.

In the previous work, a 3-stage charge pump was designed and tested in a system that would enable the converter's operation in adaptive mode. However, several drawback existed in that system. Firstly, external components, like Atmega2560, were utilized. Power consumption for these elements were not accounted for. Additionally, the sheer size of these elements inhibit the integration of these components in devices which perform stimulation due to size and weight restrictions. Moreover, the loop of the control mechanism was not closed and load information was entered manually. The new implementation fixes both of these issues and presents a solution that can easily be integrated on-chip. In addition, the ability to be

able to operate in multi-channel systems makes this version much more desirable compared to its predecessor. Despite these improvements, as it is true with every work, there are some aspects of the design that can be improved or elements that can be added. These will be detailed in the subsequent section.

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

In this thesis, an adaptive converter that tracks the potential difference of stimulation electrodes is designed and implemented. The reason for this adaptive nature is to alleviate the issue of low efficiency that is inherent in constant current stimulators. This way, the energy source that is already scarce will last longer. Thus, resulting in fewer recharge cycles for a certain period of time, prolonging the lifetime of the said energy source.

Accomplishments can be listed as follows:

1. The literature was reviewed to understand switching converters. Designs based on switched-capacitor converters were examined and their properties, analysis was investigated. Converters specific to constant current stimulation were examined to assess the state of the art and figure out what aspects need improvements in this regard.

2. An adaptive converter system to reduce power dissipation in constant current stimulators was introduced. At its heart, the system utilizes a 3-stage charge pump. This charge pump was configured so that it could provide different levels of output voltages from 3.3 V input, namely, 3.3/6/9/12 V. This was done with two ways of regulation. The first one is PFM, where the switching frequency of the converter is adjusted with an error amplifier by comparing a ratio of its output with a reference voltage. This was considered as fine regulation. The second one, coarse regulation, was accomplished by changing the number of operational charge pump stages within the converter. This way, the conversion ratio of the converter was altered and maximum efficiency was obtained for all output levels. The charge pump was tested

with an H-bridge in the form of a stimulator. The stimulators current magnitude was altered with a controller. The same controller also determined the number of charge pump stages that must be operating according to this current. Furthermore, the controller made use of an off-chip DAC to provide the converter with the required reference voltage. In other words, the Atmega2560 governed the whole operation. In-vitro tests and tests performed with artificial loads showed power dissipation reduction of up to 80% for lower stimulation current magnitudes compared to the converter's constant 12 V operation mode.

3. Second generation adaptive converter was implemented that fixed the issue of the first one. Circuits undertaking the roles of the controller and off-chip DAC were integrated, eliminating external components. The control loop, which was not closed in the first design, was closed and the determination of the required voltage compliance was automated. Lastly, the control mechanism and charge pump were configured so that the converter's output could take a range of values instead of several discrete voltage levels. Fine and coarse regulation of its predecessor were reintroduced with the new charge pump, the control signals necessary being supplied by the voltage tracking circuitry. Comprised of buffers, difference amplifier, digital circuitry, the tracking circuitry took a ratio of electrodes' voltages and performed subtraction operation on them. This way the reference voltage necessary for PFM regulation was obtained. With the utilization of a flash ADC, the number of operational charge pump stages was also determined. Tests of the adaptive converter system with an 8-channel stimulator and 1.8 V input showed that the converter can configure its output according to the electrode voltage. Up to 35% reduction in power dissipation was observed for low load impedances compared to its constant 5.5 V operation mode. This reduction in the power dissipation of the most power hungry part of the cochlear implant interface circuit will result in longer time intervals between battery recharges, which will positively impact both the implant and the user.

4.2 Future Work

Experimental results show that the adaptive converter does indeed reduce power dissipation. However, there are some additions that can be done to further increase the performance and obtain a more robust design:

1. In-vivo tests of the adaptive converter integrated with the fully implantable cochlear implant interface circuit can be performed to verify the operation of the whole system within its intended operation environment.

2. It was explained that the converter pulls its output to it maximum value before the subsequent stimulation periods starts. The magnitude of the stimulation current is not extracted from the interface circuit. Moreover, there is no current sensing or impedance detecting circuitry that will provide this information either. Thus, to ensure the subsequent stimulation periods has enough voltage compliance, the converter's output is reset before every period. Naturally, recharging the filter capacitor at the output consumes power. To overcome this issue, a circuit can be added that extracts the information of the subsequent stimulation current from the interface circuit. This way, the converter can decide not to reset its output if the magnitude of the next stimulation current is below a threshold. Additionally, the extracted information about the stimulation current magnitude can also be used to pull the output of the converter to intermediate output levels and not the maximum level. Both scenarios improve the reduction in power dissipation.

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