WIRELESS DATA TRANSMISSION FOR MEDICAL IMPLANTS WITH FULLY DIGITAL NON-COHERENT DETECTION

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ABSTRACT

WIRELESS DATA TRANSMISSION FOR MEDICAL IMPLANTS WITH FULLY DIGITAL NON-COHERENT DETECTION

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Number of people awaiting therapeutic devices and implants increase with the increase in population. Cochlear implants are one of these implants which aid patients with sensorineural hearing loss. Conventional cochlear implants consist of two distinct parts inside and outside of the ear. Communication in between these parts is conducted wirelessly. In fully implantable cochlear implants, there is no operational outside block. Hence, in order to interact with all the blocks, wireless data transfer should be used in an extensive manner. In this thesis, a bidirectional wireless data transfer system for fully implantable cochlear implants utilizing inductive coupling with Binary Phase Shift Keying is designed. In addition to system being designed to be primarily used for patient fitting application, magnet-free system can also transfer data and carrier with BERs of $3x10^{-3}$ in worst coupling conditions, bidirectionally. The patient fitting processor has less than 1 bit error for each fitting cycle. With fully digital non-coherent detection, implanted structure consumes 47.1 μW power without power amplifiers.

Keywords: Binary Phase Shift Keying, Implantable Medical Devices, Wireless Data Transfer, Digital Demodulation

ÖZ

TIBBİ İMPLANTLAR İÇİN TAMAMEN DİJİTAL TUTARLI OLMAYAN TESPİTLİ KABLOSUZ VERİ AKTARIMI

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Artan nüfusla birlikte tedavi edici cihaz ve implant bekleyenlerin sayısı da artmaktadır. Koklear implantlar, sensörinöral işitme kaybı olan hastalara yardımcı olan implantlardan biridir. Geleneksel koklear implantlar, kulağın içinde ve dışında iki ayrı parçadan oluşur. Bu parçalar arasındaki iletişim kablosuz olarak gerçekleştirilir. Tamamen implante edilebilir koklear implantlarda, operasyonel bir dış blok yoktur, bu nedenle tüm bloklarla etkileşime girebilmek için kablosuz veri aktarımının kapsamlı bir şekilde kullanılması gerekir. Bu tezde, Binary Phase Shift Keying ile endüktif kuplaj kullanan tamamen implante edilebilir koklear implantlar için çift yönlü bir kablosuz veri aktarım sistemi tasarlanmıştır. Mıknatıssız sistem, öncelikli olarak hastaya uyarlama uygulaması için kullanılmak üzere tasarlanmış olmasının yanı sıra, en kötü kuplaj koşullarında $3x10^{-3}$ BER ile veri ve taşıyıcıyı çift yönlü olarak aktarabilir. Hasta uyarlama işlemcisinde her bir yerleştirme döngüsü için 1 bitten daha az hata bulunmaktadır. Tam dijital tutarsız algılama ile implante edilmiş yapı, güç amplifikatörleri olmadan 47,1 µW güç tüketir.

Anahtar Kelimeler: İkili Faz Kaydırmalı Anahtarlama, İmplante Edilebilir Tıbbi Cihazlar, Kablosuz Veri Aktarımı, Dijital Demodülasyon

To My Beloved Family

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ABBREVIATIONS

WDT: Wireless Data Transfer

T_X: Transmitter Coil / Transmitter

R_X: Receiver Coil / Receiver

BPSK: Binary Phase Shift Keying

DPSK: Differential Phase Shift Keying

BER: Bit-Error-Rate

CHAPTER 1

INTRODUCTION

1.1 Motivation

According to the estimates of World Health Organization, by 2050, 2.5 billion people will have hearing loss to some degree and almost 10% of the entire world population will suffer from hearing disabilities [1]. As the number of patients awaiting for therapeutic devices to enhance their quality of life increases, the need for more efficient and robust medical implants increase as well.

In medical implants, there are various sub-units that are responsible for proper operation of the implant. These sub-units interact with the area they are implanted on not only by intervening the operation of the tissues but also by monitoring them. Moreover, operation of the implant's sub-units are needed to be monitored. Adding to all of the needs given, interacting with or controlling the implanted devices after surgery "directly" – with wire control – is not a feasible approach, due to possible complications [2]–[4].

Cochlear implants (CI) - as an example to implants or neuroprosthesis - are implants used to stimulate the neurons that are connected to the central nervous system, providing the patients with sensorineural hearing loss a sense of sound. First ideas leading to invention of cochlear implants (CI) have started with stimulating neurons that are responsible for hearing externally in late 1950s and early 1960s [5], [6]. The design and manufacturing of the cochlear implants with multi-channel structure goes back to 1980s [7], [8]. These cochlear implants are considered as convential cochlear implants.

In a convential CI, sound waves are captured with an external microphone, that is replaced just outside of the ear. Captured sound signal is processed with a signal processor and divided into frequency bands. This division is necessary since different regions of the cochlea are responsible for different frequencies of sound while converting sound waves into electrical signals [9]. Capturing sound signals and processing them are performed outside of the ear. Neurons inside the ear are stimulated using the processed information. This is done by cochlear electrodes and stimulator block. These electrodes and stimulator blocks are implanted inside the ear. Therefore, there is a necessity for data transmission in conventional cochlear implants in between the outside and inside blocks. A modern conventional CI system is shown in Figure 1.1. As it can be seen, there are two distinct parts that are not connected to one another directly with electrical wire connection.

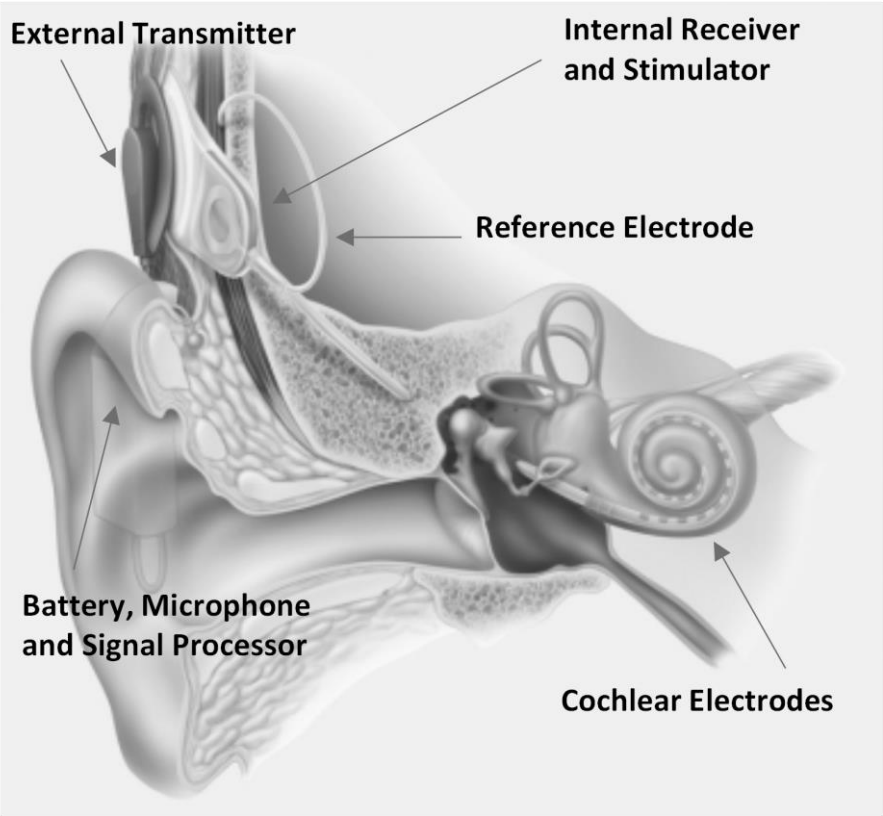


Figure 1.1. Modern conventional cochlear implant system [10]

In addition to conventional cochlear implants with an out-of-ear operational block, there are also fully implantable cochlear implants [11]–[15]. In these implants, the capture and processing of the audio signal are performed inside the ear. Thus, the transducer that converts sound into electrical signals and the circuits that process these signals are implanted in the ear during surgery. This means that fully implantable cochlear implants do not require wireless data transfer as in conventional cochlear implants. However, the need for wireless data transmission still arises due to the need to interfere and monitor the transducer and processing circuits.

A major reason for these interventions is patient fitting. Patient fitting is a procedure performed to increase the patient's comfort level with the implant after surgery. In patient fitting, implant work settings are readjusted by patient feedback. Thus, the best operation condition for the patient is made. Wireless data transmission can also be used to monitor the operating ranges of the sound processor and the operations of the stimulators as well as patient fitting. This way, performance parameters of the implanted electronics can be checked regularly.

Wireless data transfer in CIs are generally performed using an inductive RF Link [16]. In order to have minimum loss of energy during the transmission, magnets are used. Magnets reduce mismatches, and help alignment of the coils that are used for RF Link. However, using magnets causes implants becoming magnetic resonance imaging (MRI) incompatible, especially with large magnetic flux densities [17]. One of the most important motivations for fully implantable cochlear implants is to reduce patient discomfort from the implant. In an inductive design with magnets, the requirement to remove the magnet in case of MRI is an uncomfortable practice for the patient. In addition, the magnet may cause complications on the skin where it is placed [18]. For these reasons, using magnets in fully implantable cochlear implants is not a suitable option.

The main goal of this thesis is to design a system that will provide bidirectional wireless data transmission for fully implantable cochlear implants. The system

should be able recover the data input given by the transmitter with minimum error. System is primarily used for patient fitting application, therefore, there should be an interface circuit to extract fitting information from the transmitted data. Design should be MRI compatible, meaning that magnets must not be used for alignment in between the coils/inductors if an inductive link is the choice of linking method. Accordingly, receiver should be able to work under varying transmission conditions.

1.2 Wireless Data Transfer Techniques

Wireless data transfer (WDT), or any signal transferring/carrying operation in general, requires a medium that the signal of concern to be transferred. For WDT applications, there are many possible mediums and methods that can be selected. During data transmission operation, power transmission occurs in parallel which affects the medium and its surrounding. For implants, one of the main concerns and priorities is not to harm the body in non-reversible ways. Moreover, patient should not feel any discomfort when implant operates. Another concern is the compatibility of the transmission system for the application.

In commercial cochlear implants, inductive links are used mostly. For near field applications, capacitive links, infrared transmission, and visible light wave transmissions can also be used as transferring techniques. In this section, near field transmission techniques are explained.

1.2.1 Inductive Coupling

Biot-Savart Law [19] forms the foundation of inductive coupling (Figure 1.2) and wireless data/power transmission with electromagnetic induction (Eq (1.1)).

$$\vec{B} = -\frac{\mu_0}{4\pi}\oint_l \frac{I\overrightarrow{dl} \times \overrightarrow{\epsilon_r}}{r^2} \qquad Eq(1.1)$$

Here $\vec{B}$ is the magnetic flux density vector, I is the current passing through an inductor/coil. Vector $\overrightarrow{dl}$ defines the current passing coil's directional property and $\overrightarrow{\epsilon_r}$ is the unit vector of the distance factor r. If the current passing is alternating, a time varying magnetic flux is created, which carry information about the frequency and magnitude of the current, related to the point of observation. When there is another coil present, magnetic flux affects the secondary coil according to its properties. Flux on the second coil can be represent as in Eq (1.2).

$$\Phi_{21} = \int_s \vec{B}_{21} \cdot d\overrightarrow{S_2} \qquad Eq(1.2)$$

Magnetic flux density $\vec{B}_{21}$ is the flux density generated by the primary coil and $\overrightarrow{S_2}$ is the surface of the secondary coil. If this flux varies in time, then according to Faraday's law of induction [20] an induced voltage is created on secondary coil.

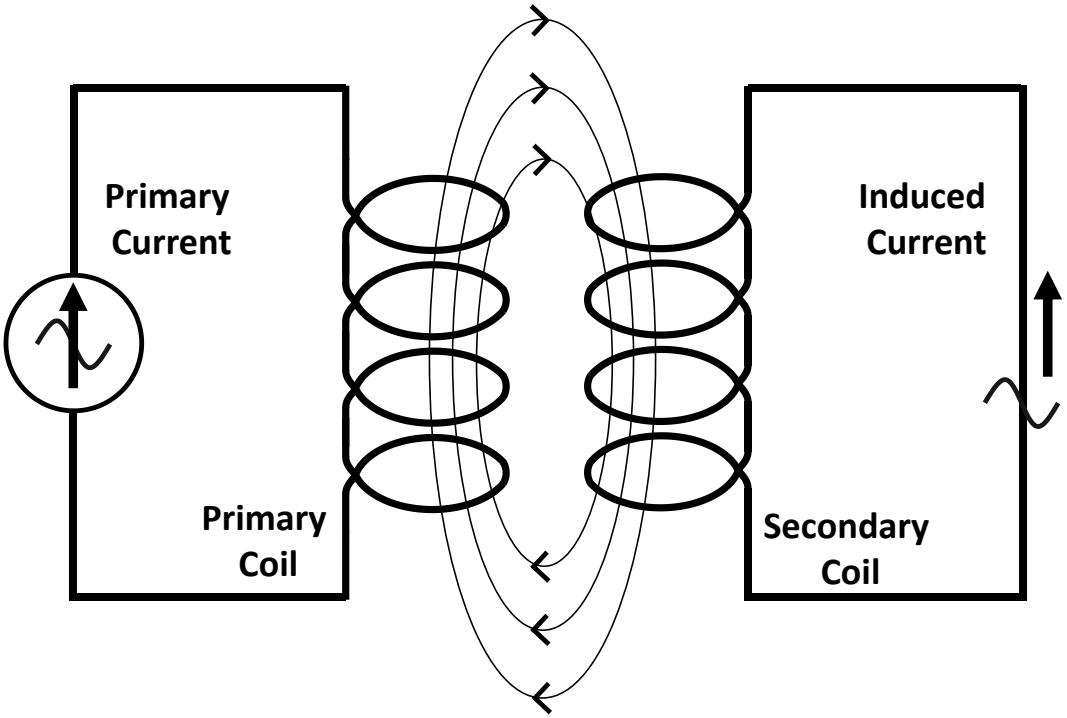


Figure 1.2. Inductive coupling system

With the induced voltage and current on the secondary coil, amplitude, and frequency properties of the primary current can be transferred to the secondary

side. This near field transmission can be used in numerous applications such as medical implants [21]–[23], mobile phones [24] and payment systems [25]. When used for medical implants, there are many factors involved in design process, such as implant area limitations, required link strength and signal power level. The power transferred is related to the mutual inductance [26] between the coils, which can be further explained with coupling coefficient concept [27].

1.2.2 Capacitive Coupling

In inductive coupling, magnetic flux generated on the secondary coil by the primary coil is utilized. In capacitive coupling, electric field created in between the parallel plates are exploited. These plates, or transmitter and receiver electrodes, form a capacitor. The in-between medium, skin in our case, is the dielectric. The time-varying and oscillating input signal creates an oscillating electric field, causing electrostatic induction on the receiver plate. Capacitive coupling systems can be employed in two styles, bipolar (transverse) and unipolar (longitudinal). Bipolar coupling is shown in Figure 1.3. In unipolar case, bottom plates are used as passive plates and they do not interact with each other.

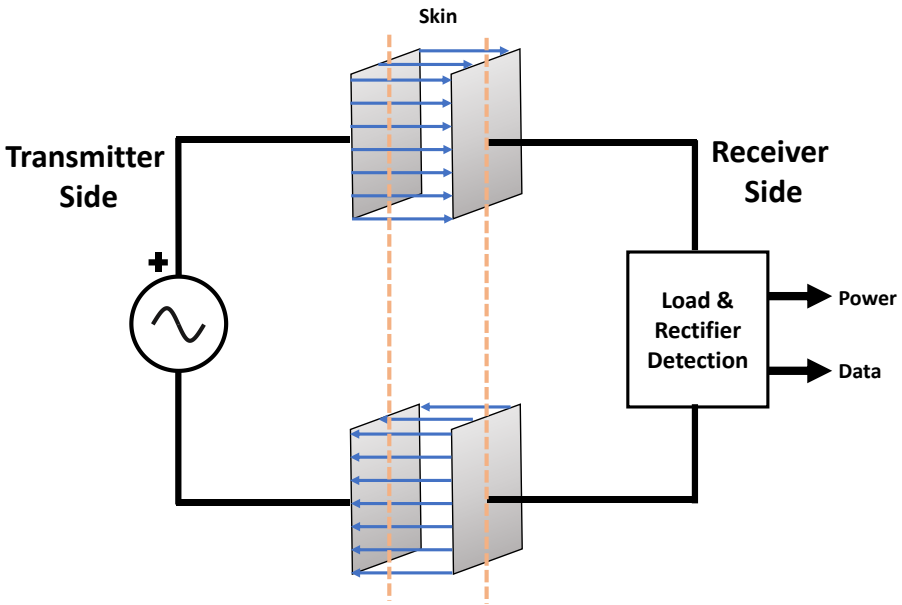


Figure 1.3. Bipolar capacitive coupling [28]

Capacitive power/signal transmission is useful for low power applications since to transmit significant power, very high voltage levels are required on the electrodes [28]. For biomedical applications, high voltages can be hazardous [29], [30]. Compared to magnetic fields, electric fields tend to interact more with the tissues it is exposed to and may cause formation of toxics ions. One of the advantages it brings on table compared to inductive coupling is that capacitive coupling interferes less with the surrounding electronics. Therefore, it has some uses in medical implants [28].

1.2.3 Infrared Transmission

Infrared transmission is the transmission of data over infrared (IR) light. IR covers the range of wavelengths from 700 nm to 1000 nm. It is used for short-range communication. For IR transmission, light emitting diodes (LEDs) are used. Generally, wavelengths near 810 nm are used even though human skin transmission is higher at 1000 nm, as the efficiency of conversion is better at 800 nm [31].

Figure 1.4 shows the diagram of an infrared power/signal transmission system [32]. Near-infrared signal generated by a laser diode is transferred to a photodiode array that is implanted under the skin. The array generates current which carry power and information about the sent signal. With such a system, an on-off keying (OOK) scheme can be used to transfer data. This brings disadvantages for infrared transmission. The robustness of infrared devices is greatly affected by the presence of other light sources in the environment. Moreover, error rates tend to increase as distance in between the transmitter and receiver increases since light density decreases [33]. Combining this with amplitude change proneness of OOK, effects of distance change become quite significant. Therefore, infrared transmission is not a suitable choice for a fully implantable cochlear implant with varying coupling conditions.

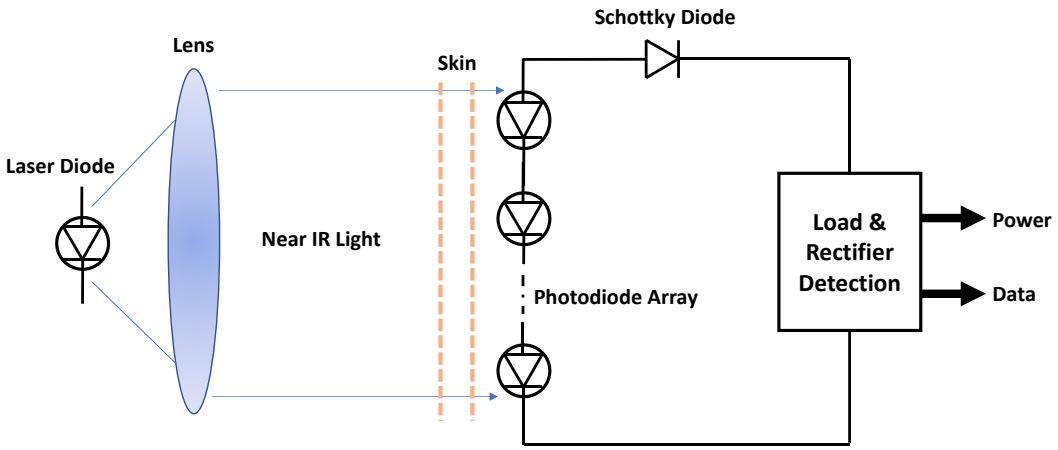


Figure 1.4. Diagram of an IR transmission system [32]

1.2.4 Far-field Transmission

Far-field transmission methods define transmission with longer ranges than the near-field transmission. So, they are used when the transmitter and receiver are not close to each other. Far-field transmission is used for ranges up to multiple kilometers in space applications, military, and telecommunication.

For far-field transmission, laser and microwaves are used. Transmission via microwaves utilizes antennas, whereas lasers include photovoltaic cells. Both of these transmission methods may have hazardous effects on human body [34], [35].

1.3 Data Modulation Methods

In wireless data transfer, besides the medium and coupling, data modulation method is another factor. Modulation is the process of modifying the frequency, phase, or amplitude of a periodic signal. The purpose of modulation is to make the information to be transferred ready for transfer through these modifications. Basically, data is converted into a signal that can be transferred easily between the receiver and transmitter via modulation.

Modulation methods can be investigated under 4 categories (Figure 1.5). Analog modulation involves modulation of analog waveforms, such as raw sound. In pulse modulation, information can be transmitted with pulse amplitude or duration variations. Amplitude variation is prone to environmental factors and generally feasible for analog waveforms, and duration variation requires large bandwidth for low error rates just like spread spectrum. Therefore, these modulation schemes are not explained in detail. Digital modulation schemes on the other hand are used for transmission of digital information such as binary bits. These schemes can be inspected under two categories, single and multi-carrier modulation. For their simplicity and application requirements, single carrier modulation methods are the focus of this section.

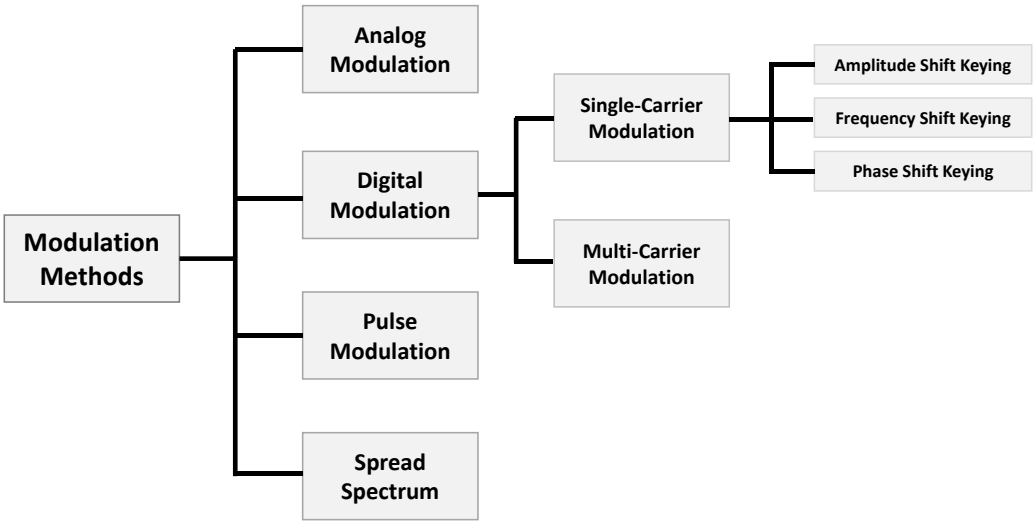


Figure 1.5. Modulation Methods [50]

1.3.1 Amplitude Shift Keying

Amplitude Shift Keying (ASK) is a digital modulation technique that digital data is represented as changes in the amplitude of a carrier signal. Each data symbol is represented by a fixed amplitude in the keying method. Symbols can include more

than one bit. Each symbol occupies a fixed time interval. The carrier signal also has a fixed frequency and phase.

Circuitry required for ASK is generally quite simple. Demodulation can be performed coherently and non-coherently. Demodulation method affects error possibility as well. ASK is sensitive to noise caused by the medium since amplitude changes are directly related to the nature of the process. In inductive coupling systems, if mutual inductances and hence coupling coefficients and conditions can be kept near constant, this noise proneness can be minimized. ASK can also be utilized with optical systems, such as infrared transmission and far-field laser transmission.

In its simplest form, a symbol would represent a single bit, either binary 1 or 0. Binary 1, then, would be modulated with the presence of the carrier and binary 0 with absence of the carrier signal. ASK modulation can be performed with a single switch, if a symbol only represent a single bit, which is a special case and called on-off keying (OOK).

A data transfer system circuit design for ASK [36] is shown on Figure 1.6. In this system, there is also a power transfer operation ongoing and as frequency and phase of the carrier can be changed, the transmitted signal is manipulated with changing loads seen at the coil. This is called Load Shift Keying (LSK). The received modulated waveform is compared with a reference voltage and data is recovered. A BER of 10^{-4} is achieved with this system, however, for power and data transfer, different carrier frequencies are used. Using different frequencies for power and data transfer applications increases the bandwidth and decreases spectral efficiency. Also, system is designed only for forward telemetry, since coils are optimized to operate at different carrier frequencies.

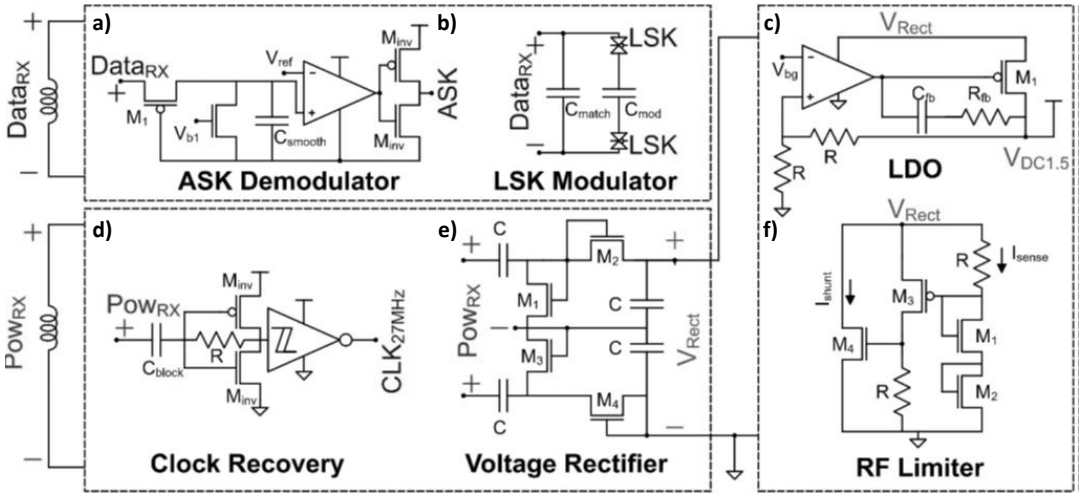


Figure 1.6. (a) ASK demodulator, (b) LSK modulator, (c) LDO regulator, (d) clock recovery, (e) voltage rectifier, (f) RF limiter circuit topologies [36]

LSK is generally used widely in forward telemetry WDT systems where power transfer is also performed with multiple carriers [37], [38].

In [39], 10 MHz carrier frequency is used. The design does not consider coupling condition variation. Detection is made coherently; clock information is extracted from the modulated waveform with an amplifier. For data recovery (Figure 1.7), a class AB stage op-amp is utilized. If voltage difference in between the input ports of the op-amp is large, then one of the input crossing branches is cut-off. Using the latch structure, amplitude change in ASK is locked and saved. Finally, Schmitt trigger detects the amplitude change point as a low duration pulse. With this structure, a BER level of 10^{-3} is acquired.

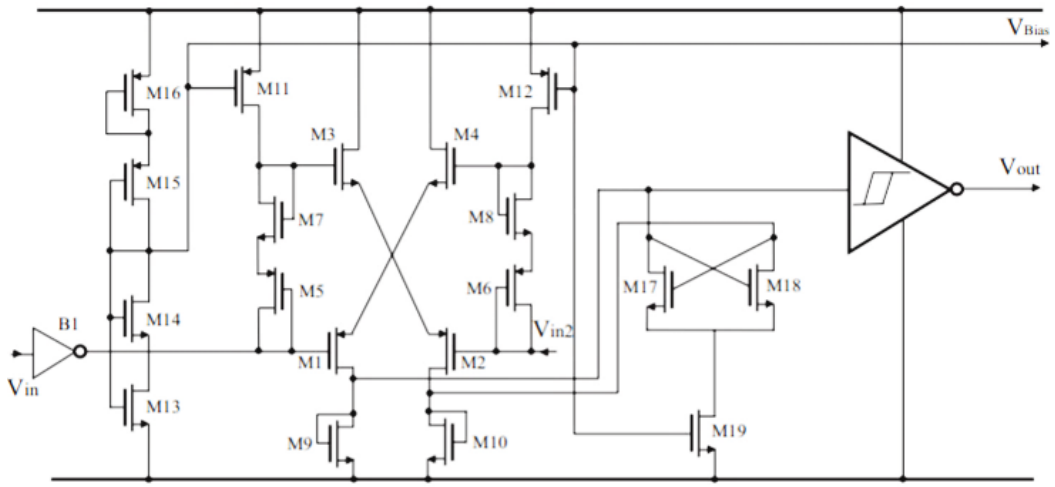


Figure 1.7. Schematics of the ASK demodulator [39]

In LSK schemes, power and data transfer carrier frequencies are seperated from each other by large intervals. The modulation nature of the LSK is quite similar to a system with varying coupling conditions with amplitude change, however this brings an added BER under low coupling conditions. In ASK detection on the other hand, amplitude levels of the received data are compared. As this comparison is optimized around a fixed coupling condition, under varying conditions, performance deteriorates.

1.3.2 Frequency Shift Keying

Frequency Shift Keying (FSK) is a modulation scheme where digital data is transferred with frequency changes of the carrier. In this method, each symbol is represented by a frequency, with the simplest form of binary 0 and 1 being symbols. This form of FSK is called Binary Frequency Shift Keying (BFSK).

Phases of the carriers used in FSK are not necessarily the same, meaning that there might be abrupt changes in phase during symbol changes. These abrupt changes are reflected on to modulated waveform with voltage level changes. Abrupt changes on the waveform consumes bandwidth, meaning that changes in phases of the carriers

cause inefficient usage of the bandwidth. Continuous-phase Frequency Shift Keying (CP-FSK) resolves this issue which utilizes a single oscillator with frequency change when switching symbol.

An FSK receiver design is shown in Figure 1.8 [40]. In this receiver, split-channel BFSK system is designed at 900 MHz band with 0.88 mW power consumption. This multi-mode structure consists of two modes- data and wake up. Modulated waveform, after an analog front-end consisting of low-noise input amplifier stage and mixers multiplying with base carriers, is distributed into different channels with a frequency-to-energy demodulator. The output waveform is then processed in digital domain with a closed loop, using an external microcontroller unit to increase sensitivity. With the split-channel approach, as tones are placed with a distance in between, bit error rate is improved as well. However, with this approach, available bandwidth must be large and therefore, for a limited bandwidth application, error rates would be bound to increase.

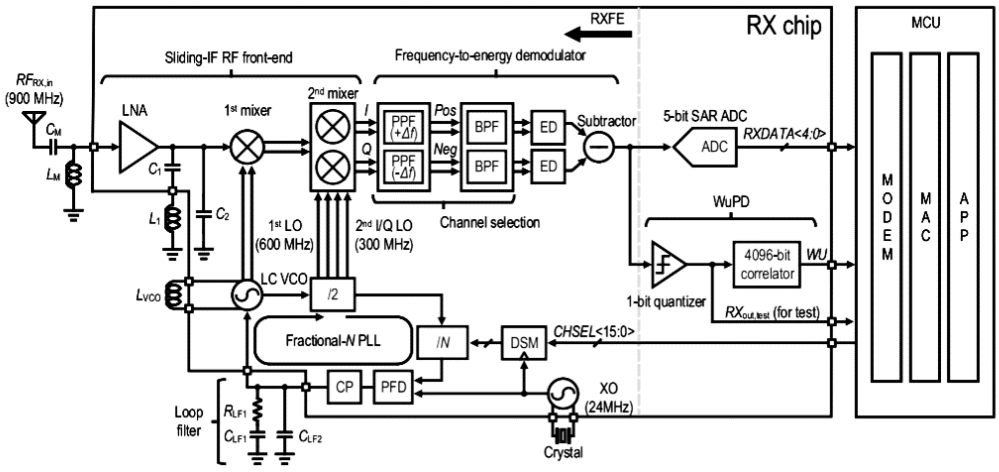


Figure 1.8. Block diagram of FSK receiver [40]

For the demodulation of FSK, both coherent and non-coherent designs can be made. Coherent detection of FSK includes internal sample clock, with the carrier frequency (Figure 1.9). This means that, in the receiver side there should be a clock generator circuit. On the hand, in non-coherent designs, clock information is extracted from received signal. In [41], using a sample clock, incoming waveform is converted into parallel data using shift registers. With square waves with periods of integer multiples of the period of sample clock, converted parallel data is multiplied. By setting the minimum voltage level of this multiplication operation, frequencies in between the two carrier frequencies are extracted. This way, anomalies in the parallel sequence are detected. With this approach, BER of $3x10^{-3}$ is achieved for average Signal-to-Noise (SNR) levels, corresponding to typical coupling conditions. System consumes 1.44 mW power with 0.015 mm^2 area.

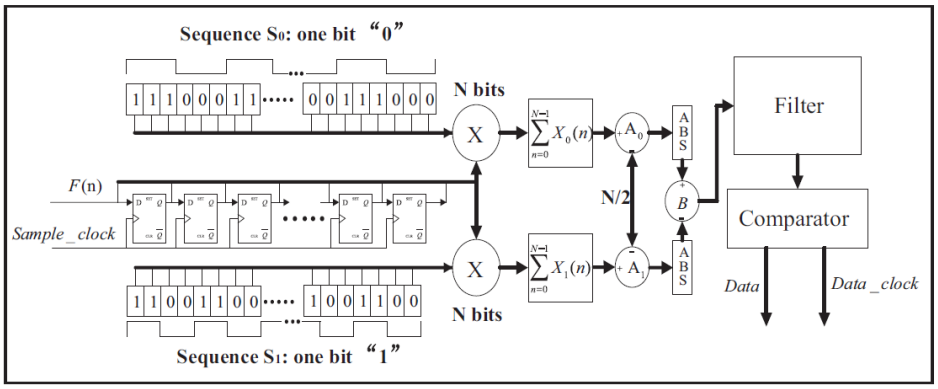


Figure 1.9. Coherent demodulation of FSK [41]

For non-coherent detection, envelope detectors or frequency to amplitude conversion and amplitude detectors are used. Envelope detectors are optimized for different carrier frequencies and high-quality factor band-pass filters are necessary for non-coherent detection to achieve low error rates. Using non-linear blocks, frequency deviation can be converted into amplitude variation, making demodulation of FSK into demodulation of ASK hence converting problem into an amplitude detection. In [42], detection is performed by using a non-linear amplifier. Amplifier is designed to have its low pass cut-off frequency near the carrier frequency; therefore, frequency changes are converted into amplitude

variations. Non-coherent detection of FSK in [42] is shown in Figure 1.10. Center carrier frequency is selected is 0.85 kHz. System consumes 1.1 mW power.

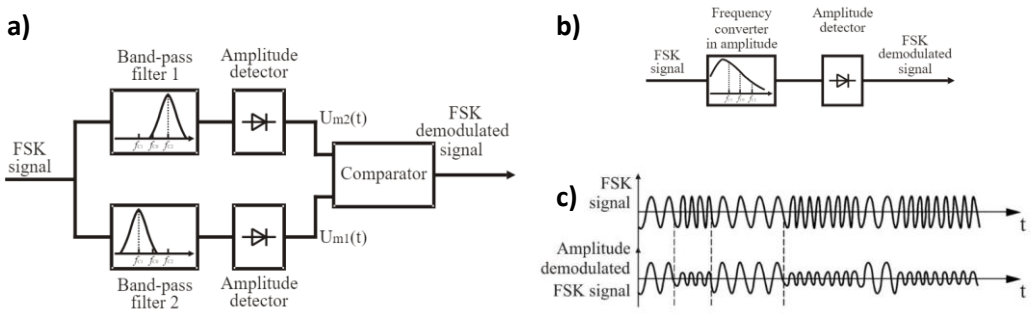


Figure 1.10. a) Non-coherent detection of FSK using Band-Pass Filters, b) FSK demodulation with frequency-to-amplitude conversion, c) amplitude demodulated FSK signal [42]

1.3.3 Phase Shift Keying

The last single carrier digital modulation scheme is the Phase Shift Keying (PSK). In PSK, digital data is conveyed by changing the phase of a carrier signal, with constant frequency and amplitude. Number of bits fitted into a symbol varies in between different sub-schemes of PSK. Each symbol is represented by a phase. Binary Phase Shift Keying (BPSK) is the sub-scheme of PSK in which each symbol represents a single bit and there is a phase difference of 180° in between accompanying waves. As in the Frequency Shift Keying, voltage discontinuity is a possible issue, if symbol duration is not an integer multiple of the carrier period. These discontinuities cause inefficient usage of the bandwidth.

PSK detection can also be conducted both coherently and non-coherently. In coherent detection, demodulator compares the phase of the transmitted signal with the phase of an internal reference signal. In such a system, variable delays in between the transmitter and receiver play an important role. For coherent detection of PSK, original carrier waveform, without phase changes, must be detected. Since there might be more than 2 phases in the modulated waveform, deciding the

primary phase is a complicated problem. A special case of BPSK, Differential Phase Shift Keying (DPSK) allows non-coherent demodulation, since in DPSK, detection is made by differentiating the symbols carrier phases. With a relatively easier protocol, DPSK becomes a simpler scheme, if data transfer speed is not a priority.

A design with BPSK demodulation utilizing On-Off Keying [43] is illustrated in Figure 1.11(a), in this design, using a baseband pulse generator, a pulse train is generated. Using this pulse train, outputs of a voltage-controlled oscillator is manipulated and BPSK waveform is created. Design also includes a leakage cancelling output stage; however, this stage decreases power efficiency. 11.8 mW power consumption is observed, with more than it being consumed by the leakage cancellation block. Chip occupies, 1.37 mm^2 area. Design waveforms of the system are given in Figure 1.11(b).

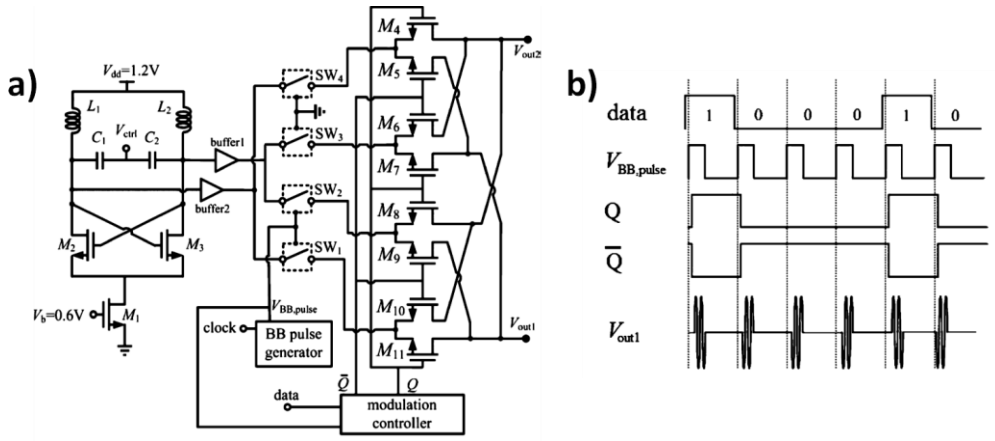


Figure 1.11. a) BPSK Modulator with OOK basis [43], b) signal waveforms

In Figure 1.12(a), coherent demodulation of BPSK is shown [44]. As mentioned, phase comparison is necessary for the detection. Costas Loops (Figure 1.12(b)) are used for this operation. After recovering the carrier, by coherent multiplication raw data is obtained. This raw data includes timing properties and phase overlaps. With timing recovery using two reference frames covering an entire period of the carrier, at first clock then data is recovered.

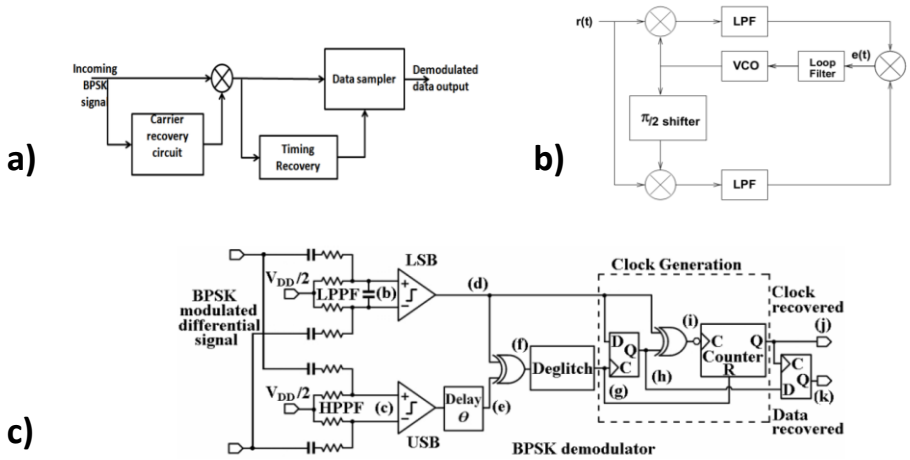


Figure 1.12. a) Coherent detection diagram of BPSK [44], b) Costas Loop [45], c) non-coherent detection overall diagram of BPSK [45]

On the other hand, in non-coherent detection, carrier waveform is not needed to be reshaped, demodulation is performed by logic design or analog measures. In [45], input waveform is filtered using low pass and high pass filters to extract lower and upper side band of the signal. Using comparators and OR gate, digitized lower and upper side band information are digitized. With logic design given in Figure 1.12(b), data and clock are recovered. This demodulator structure has BER of 10^{-3} on circuit level, overall BER is not given. The chip occupies 0.04 mm^2 core area and consumes 82 μW.

1.4 Objective of the Thesis

The main objective of this thesis is to design and implement a bidirectional wireless data transfer system for fully implantable cochlear implants. The system should be able to recover transmitted data with less than 1-bit errors for each fitting and data transfer cycle of 8 pockets consisting of 32 bits each. Combining less than 1-bit error for each cycle with parity bit check, error probability in each cycle can be minimized.

Patient fitting information should be extracted from the transmitter serial data with an interface circuit. The wireless data transfer system utilizes inductive coupling. This work is a part of FLAMENCO (A Fully Implantable MEMS-Based Autonomous Cochlear Implant) Project (www.flamenco.metu.edu.tr) which is a fully implantable and autonomous CI, utilizing piezoelectric cantilevers as transducers with an interface circuit, mimicking hair cell operation [46]. The design criteria for the wireless data transfer application are listed below:

1. Wireless data transfer system should operate bidirectionally, meaning that data and carrier waveforms of the transmitter side should be extracted at the receiver side as the same data and carrier waveforms.
2. Wireless data transfer system should transfer binary data, to carry encoded information about the implanted electronics operations such as current consumptions of the channels, battery power level with back telemetry alongside with forward telemetry patient fitting.
3. For one patient fitting cycle, error rate should be less than 1 bit. Therefore, Bit-Error-Rate of the system should be less than 3.9×10^{-3} for all coupling conditions since the implanted system has 8 channels and each data pocket consists of 32 bits.
4. The implantation area under the skin is 5 mm^2 at maximum[47]. Consequently, receiver coil and modulator-demodulator complex should not occupy more than 5 mm^2.
5. According to ITU regulations for household applications, center frequency of the carrier waveforms must be 13.56 MHz with the maximum bandwidth of 14 kHz with real frequencies. Hence, data rate should be less than 20 kbps for the modulated signal.

1.5 Organization of the Thesis

The rest of the thesis covers five chapters. Chapter contents are as follows:

Chapter 2 explains the wireless link with inductive coupling and gives detailed information about coupling coefficient range selected for the design. A skin phantom is prepared and coupling levels are tested. Moreover, shift keying off-chip designs used for selection of the keying method are given. Experimental results acquired with off-chip modulation-demodulation setup on Printed Circuit Board (PCB) are given.

Chapter 3 presents the semi-coherent Binary Phase Shift Keying (BPSK) based Wireless Data Transfer (WDT) system. Modulator utilizes the fact that differential phase modulation is an extension of Amplitude Shift Keying with data and inverse of the data are modulated separately with one carrier. Implemented demodulator is a semi-coherent, Locked Loop free circuit which operate at 13.56 MHz with a voltage-controlled oscillator. Coupling range reflection of the work and patient fitting application simulation example of the system is given. Moreover, Experimental result are presented in the chapter.

Chapter 4 describes the improved version of the WDT system, with double carriers and amplitude continuity. 180° phase shifted carrier signal is generated with current manipulation using the initial carrier signal and switching of the carriers are used for modulation. Demodulator block is oscillator free, non-coherent and fully digital. With further improved version, delay blocks are eliminated and delay correction is applied. Circuit implementations, schematics, simulation, and experimental results are given with comparisons.

Chapter 5 concludes the thesis with the summary of the designed system and future improvement that can be studied are given.

CHAPTER 2

WIRELESS LINK AND DATA KEYING METHOD SELECTION

2.1 Motivation

The most common wireless linking method in cochlear implants are inductive links [48]. The fully implatable cochlear implant (FICI) in concern is charged with wireless power transfer using an inductive link [49]. Combining the already present inductive link in the system and the advantages against other linkage methods given in the previous chapter, the wireless data transfer system utilizes an inductive link. An inductive link can be easily created with coils. The energy that is transferred from a transmitter coil to a receiver coil depends on many parameters. These parameters include coil sizes, distance between the coils, and the misaligment of the axes of the coils.

Generally, after surgery, changes in these parameters are negligible as the coil sizes are predefined, and coils merely move both inside the body and in the external parts. The assumption of coils staying at the same distance and with the same alignment during operation depend on magnets being present inbetween the coils. To achieve magnetic resonance imaging (MRI) compatibility, magnets are removed in the design, hence the voltage/power coupling in between the tranmistter and receiver coils change both during data transfer operation and also in between different data transfer sessions. This means that the designed system should be able to operate for varying coil distance and alignment. Both of these artifacts result in inconsistent coupling conditions and they can be simplified with a coupling coefficent term. The approach is to find out the coupling coefficient ranges that wireless data transfer (WDT) system has to deal with.

With an inductive link, a wide choice of keying methods can be used [50]. The selection of the keying method depends on the application. As mentioned in the previous chapter, Amplitude Shift Keying (ASK) offers simple modulation and demodulation operation, but is largely affected by noise [51]. Frequency Shift Keying (FSK) is a more robust [52], [53] data keying method, however, the bandwidth limitations of the application mean that the carrier frequencies should be quite close to each other meaning that high-quality factor filters are needed, increasing power consumption and complexity [54]. Phase Shift Keying, on the other hand, depends on proper detection of the initial carrier, is affected by phase delays and require locked loop circuits for demodulation operation [55].

Since FICI system already includes a wireless power transfer using an inductive link, no further studies regarding the coil design is made, however, the ranges that the wireless data transfer system has to operate is defined using the previously designed and fabricated coils.

Using Applied Wave Research (AWR) Sofware, keying scenarios for alternating coupling conditions and performances of these data keying methods are observed under simulation. Then, in order to verify the simulation results, a printed circuit board (PCB) with discrete integrated circuit (IC) components is designed and tests are performed with the selected coils, under misalignments. Operation coupling coefficient range selection, PCB design and keying operation verifications in simulation and test results are provided in this chapter of the thesis.

2.2 Coil Operation

Coils are passive, two terminal, inductive electrical components that store energy with magnetic field when an electrical current passes through. The inductance L with the unit of henry (H), is described as the ratio of the voltage difference in between the terminals to the rate of change of the current passing through, which characterizes a coil/inductor.

Since the energy storing nature of coils arise from the magnetic field that they create, when there are multiple coils nearby, shared magnetic field has some effects on the coils. This phenomenon forms the basis of a transformer. The wireless data transfer and power transfer operations with inductive link utilize the shared magnetic field created by one of the coils – *transmitter coil (T_X)*. The coil that is induced with the magnetic field created by the transmitter coil is the – *receiver coil (R_X)*. The amount of energy transferred from the transmitter to the receiver is related to the mutual inductance (M). Mutual inductance is calculated by Eq. 2.1, where L_1 and L_2 are the inductances of the coils and K is the coupling coefficient. Magnitude of K is less than or equal to 1.

$$Mutual\ Inductance\ (M) = K\sqrt{L_1 L_2} \qquad Eq.(2.1)$$

Coupling coefficient (K) is the main concern of the coil design. K is affected by the size of the coils, distance in between them and the alignment of the coils with respect to each other. The distance "d" and alignment angle "θ" are shown in Figure 2.1 . Given results are according to these definitions.

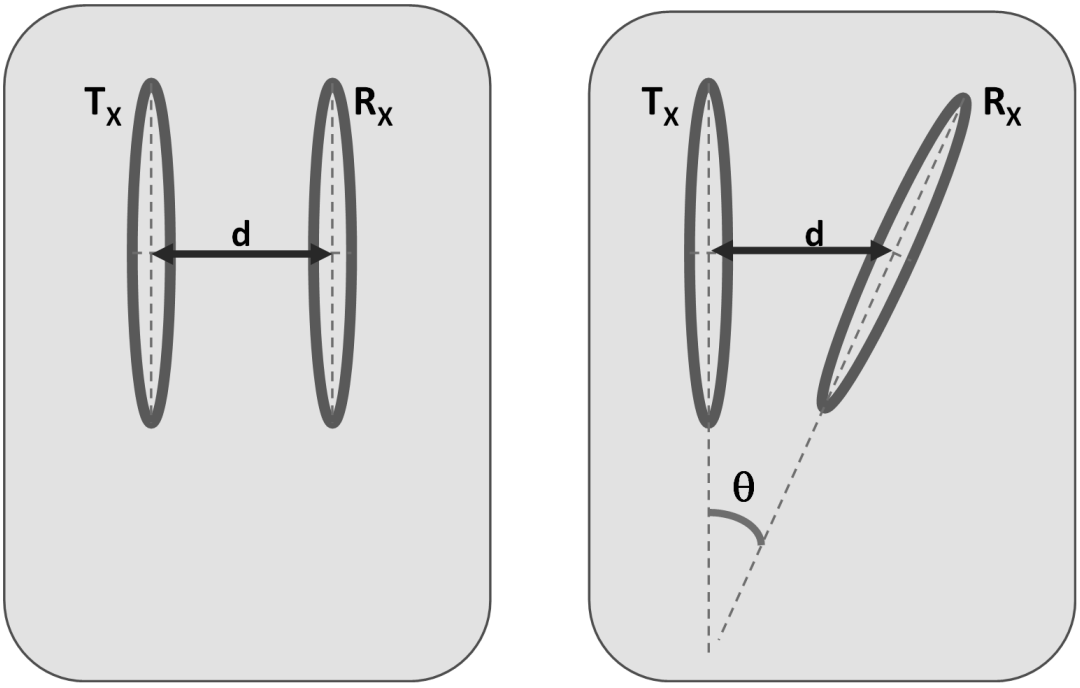


Figure 2.1. Distance, d of the coils and alignment parameter, θ definitions

2.2.1 Coil Parameters

Normally in coil design and selection, an optimization process within the design and application boundaries is required. However, for our application, the coils are already optimized according to the power transfer operation [56]. Thus, the parameters and simulation/test result used for the wireless power transmission system are given in this section.

The simulations were performed with ANSYS EM Simulation tool. Initial simulations are performed on air medium, with the assumption that the electromagnetic permeability of the skin-tissue complex is almost the same as the air permeability [57]. This assumption accepts that there is no blood component which includes iron. In the simulations, 20 different coil structures are simulated which are given in Figure 2.2. The 20 coils presented are manufactured, 2 coils are selected as transmitter and receiver coils, with the parameters shown in Table 2.1

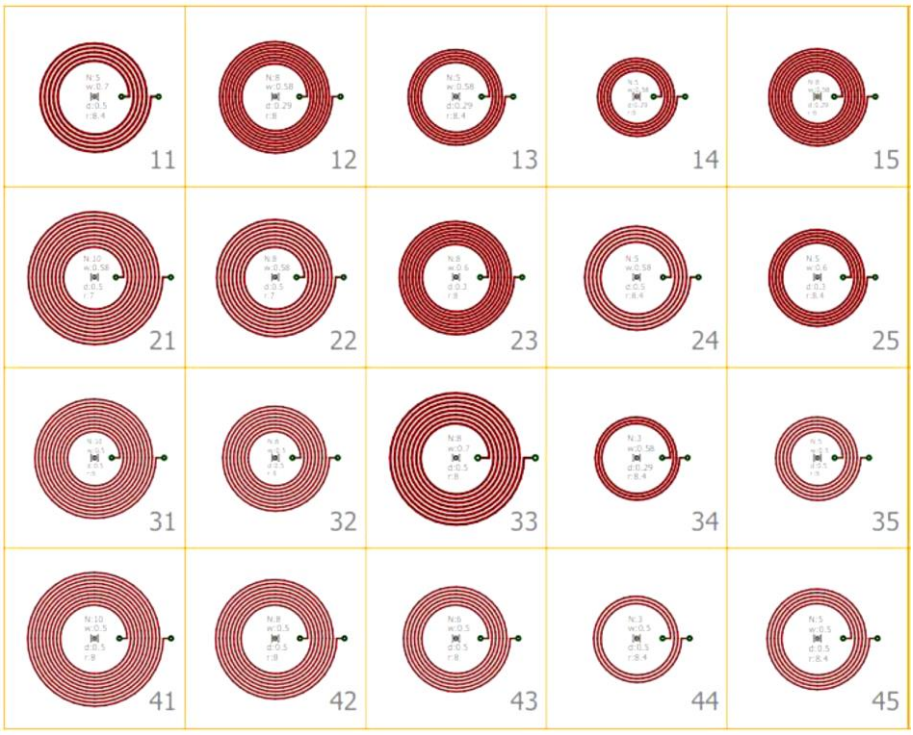


Figure 2.2. Manufactured coils for receiver and transmitter coil selection [58].

Coils are optimized to work at 13.56 MHz frequency, since this carrier frequency with 14 kHz interval band is selected for near field mobile applications according to ITU Radio Regulations.

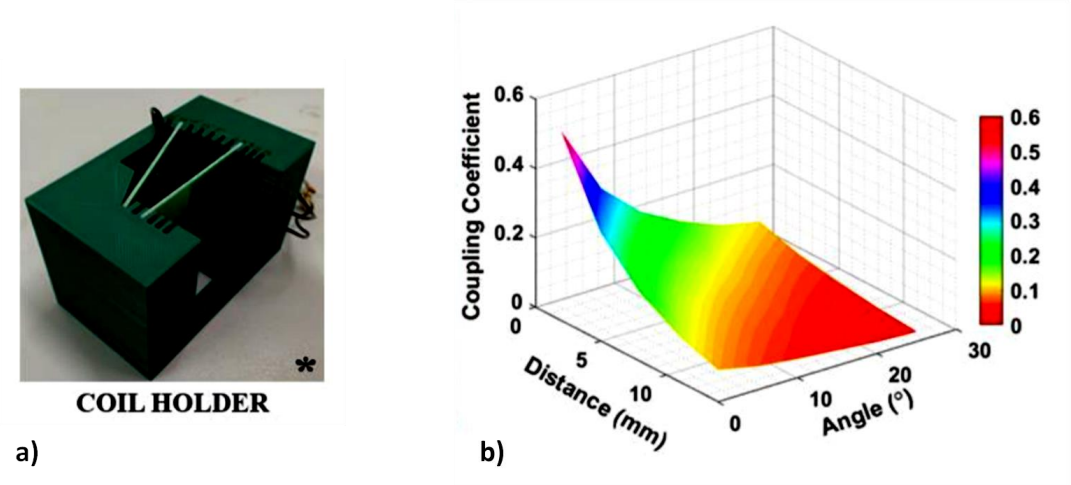
Table 2.1. Parameters of the Selected T_X and R_X Coils [58].

Properties	***T_X***	***R_X***	***M(Mutual)***
Inductance	1101 nH	345 nH	189 nH
Inner Radius	8.00 mm	8.40 mm	-
Turn Number	6	3	-
Wire Radius	0.25 mm	0.25 mm	-

2.2.2 Coupling Coefficient Range Selection

In order to decide the coupling coefficient range that the wireless data transfer system has to operate, the distance (d) and alignment (θ) parameters are swept with the manufactured coils. Air is the medium of transmission in the tests as well. However, further inspection of the effect of the medium is made with a skin phantom, which will be explained in the latter sections of the thesis.

The coil displacement (d) is swept from 2 mm to 14 mm. Normally, skin thickness that the receiver coil is placed is 5 mm in average [59]. Since there are no magnets used, the distance in between the coils would be larger than the average value, hence 10 mm is selected as the maximum distance for the coupling coefficient range selection. For the alignment effect on the coupling coefficient, the alignment angle (θ) is swept from 0º to 30º. The results are shown in Figure 2.3. As expected, increase in distance and alignment angle decreases the coupling coefficient in between the receiver and transmitter coils.



*Coil Holder is designed by M.Berat Yüksel, METU BioMEMS Research Group.

Figure 2.3. (a) Coil holder for tests with 2 mm to 14 mm distance and 0º to 30º misalignment angle variation, (b) Coupling coefficient test results for the swept variables [58].

Under the best coupling condition with 5mm distance and 0º angle in between the coil, coupling coefficient is around 0.30 and under the worst condition with 10 mm distance and 30º alignment angle, coupling coefficient is around 0.05. The test results with the manufactured coils suggest that with distance in between the coils (d) changing from 5 mm to 10 mm and the alignment angle (θ) changing in between 0º to 30º, the coupling coefficient varies in range of 0.30 to 0.05. This means that the wireless data transfer should be able to handle coupling coefficients in this given range.

2.2.3 Coupling Verification

Coil tests and coupling level selections are performed with air in between the coils, however in a real-life application, besides air, skin will be present. In order to test the performance of the coils and deviation from the air medium, a skin phantom is prepared and coupling levels for different voltage levels are tested.

Before modeling the skin, organic and inorganic contents in the skin should be investigated. Skin consists of three different layers, epidermis, dermis and hypodermis [60].

To model these layers, following structures are used [60].

- Top layer: Epidermis, involving proteins and lipid – 0.11 mm
- Middle layer: Dermis, muscle and blood cells – 2.41 mm
- Bottom layer: Subcutaneous Tissue and hypodermis – 0.62 mm

Fat and muscle are chosen to be the most dominating structures in these layers and are modeled with the chemicals given in Table 2.2.

Table 2.2 Fat and muscle phantom ingredients [61].

	fat	*muscle*
Kerosene (ml)	330.0	50.0
Oil (ml)	330.0	50.0
p-tol acid (gr)	170.0	800.0
n-propanol (ml)	8.5	40.0
Water (ml)	160.0	750.0
Gelatin (gr)	30.0	135.0
Formaldehyde (ml)	2.0	8.0
Surfactant (ml)	140.0	10.0

The prepared shin phantom and transmitter and receiver voltages with perfect alignment and 7 mm distance in between the coils are show in Figure 2.4.

a)

b)

Transmitter Voltage,pp (V)	Receiver Voltage,pp (V)	Coupling Coefficient
0.95	0.17	0.178
1.86	0.32	0.172
2.76	0.48	0.174
3.68	0.64	0.174
4.59	0.80	0.174
5.50	0.96	0.174
6.39	1.12	0.175
7.30	1.3	0.178
8.30	1.46	0.176
9.20	1.60	0.174

Figure 2.4. (a) Skin phantom (b) coupling coefficients for different T_x and R_x voltage levels.

Results using a skin phantom does not vary when compared to the air case. This means that the range we selected is a valid range for real-life application. Linear behaviour of the T_x and R_x voltage levels is also seen with this setup, simplfying circuit design of modulator and demodulator pair.

2.3 Data Keying Method Selection

The data keying/modulation methods can be summed up into 3 categories Amplitude Shift Keying (ASK), Frequency Shift Keying (PSK) and Phase Shift Keying (PSK). Quadrature Amplitude Modulation (QAM) can also be classified as a separate family of digital keying method, however, as it carrier the properties of both ASK and PSK, it is not inspected separately. These modulation schemes, with their subsections, can be inspected and compared under a variety of conditions and parameters. These include transmission performances, spectral properties such as spectral efficiency, robustness under interference, and compexity.

Selected data keying method should be able perform with single carrier frequency of 13.56 MHz and 14 kHz bandwidth, alongside with inductive coupling with no magnets to be available for our application. In order to select the modulation methods that are available for our application, tests with discrete integrated circuits (IC) printed circuit board (PCB) setup are performed. The test setup created is able to generate modulated signals using ASK with On/Off Keying (OOK) and with varying non-zero amplitudes, FSK with two carrier frequencies – or in other words with a carrier frequency with bandwidth at max and finally, PSK with two distinct phases Binary Phase Shift Keying (BPSK) or more specifically Differential Phase Shift Keying (DPSK) which is a technique of BPSK.

2.3.1 Amplitude Shift Keying Design

Amplitude Shift Keying (ASK) has many subforms. The simplest form is On-Off Keying (OOK). In OOK, the data is transferred by the presence or absence of the carrier wave signal. Generally, presence of the carrier for a specific period represents a binary one and the absence of it represents binary zero, however, it can also be vice versa. ASK operation equation with a single carrier is shown in Eq 2.2, the carrier *c(t)* may be a fixed frequency signal but also may change as well. *D(t)* is the data that is wanted to be transferred. With two different out of phase carriers used with amplitude modulation, the data encoding method becomes Quadrature Amplitude Modulation (QAM).

QAM utilizes that "the two out of phase carriers – with the same frequency" are orthogonal, meaning that their inner product/integral over one period is zero (Eq 2.3 & Eq 2.4).

$$ASK\ Modulated\ Signal(m(t)) = D(t) * c(t) \qquad Eq(2.2)$$

$$\langle c_1 c_1 \rangle_w = \int_T c_1(t) c_2(t)\, dt \qquad Eq(2.3)$$

$$\langle c_1 c_1 \rangle_w = 0 \qquad Eq(2.4)$$

Our aim is to verify that with the coupling coefficient range of our concern, ASK (Figure 2.5) can be used as the data encoding and decoding method. To test this, a modulator and demodulator are needed. ASK modulation – with OOK – can be achieved with a single switch (Figure 2.6(a)), assuming that the switch can operate at frequencies of the carrier signal. If wanted to extend the modulation operation to QAM, additional circuitry is needed. The aim is to see ASK viability, so QAM modulation and demodulation are not performed.

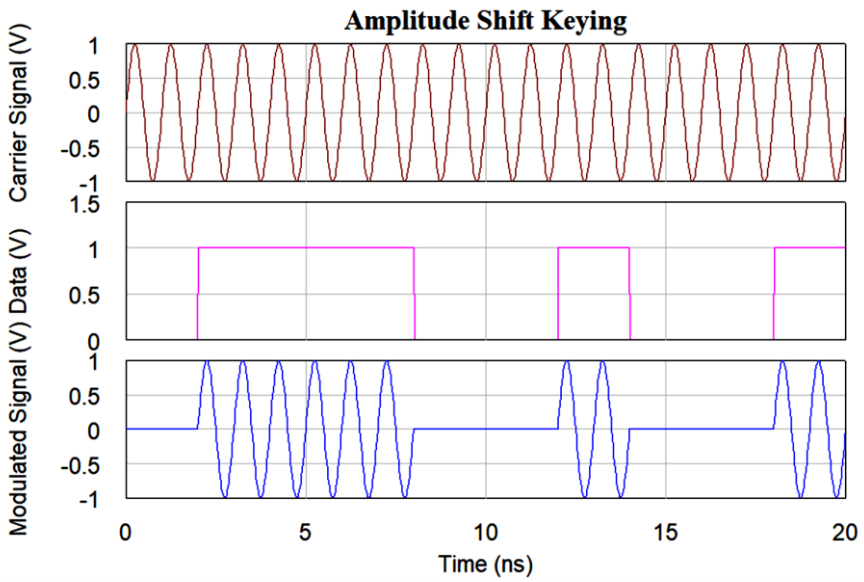


Figure 2.5. Carrier (c(t)), Data (D(t)) and ASK (m(t)) waveforms

To demodulate ASK signal, received signal is rectified and passed through an envelope detector. Output waveform is then buffered/digitized to recover the sent data (Figure 2.6(b)). Detecting the sent data at the receiver end is not enough to verify data transfer operation. Detected signal is only the waveform of the incoming data but the data clock – or the bit duration – is also needed to be transferred and detected. If an additional encryption protocol is decided to be used, a periodic signal can be generated at the receiver end. However, with this approach, when the sent data bit change points overlap with the receiver clock transition points, glitches may occur.

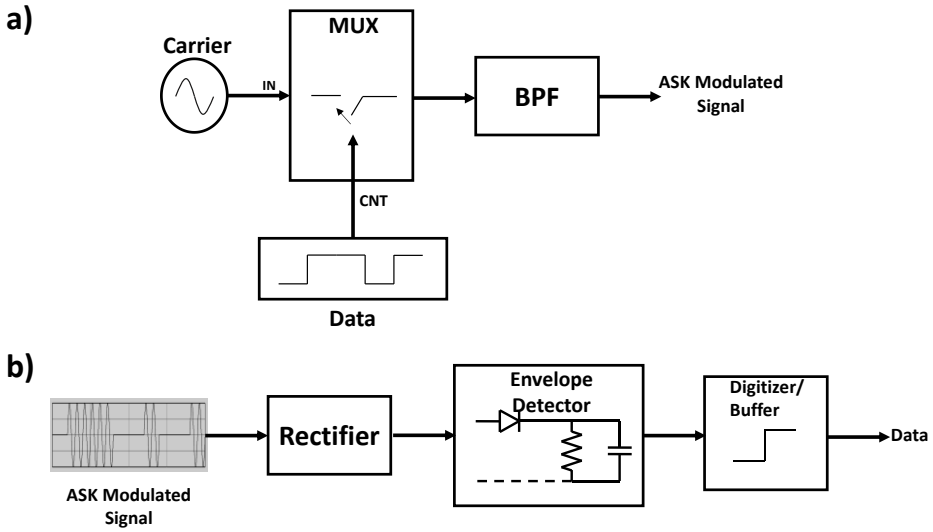


Figure 2.6. a) ASK modulation overall diagram, b) ASK demodulation overall diagram

2.3.2 Frequency Shift Keying Design

Frequency Modulation – Frequency Shift Keying – technique simply involves two frequencies for binary data transmission (Figure 2.7). Two frequencies are seperated by frequency Δf which is small compared to the central frequency f_c. Bandwidth is directly related to the frequency seperation since the entire range is considered to be used by the modulation scheme. The frequency spacing Δf is generally specified with the modulation index d with the relation given in Eq 2.5. T in the equation is the bit duration of the modulated data or inverse of the data rate.

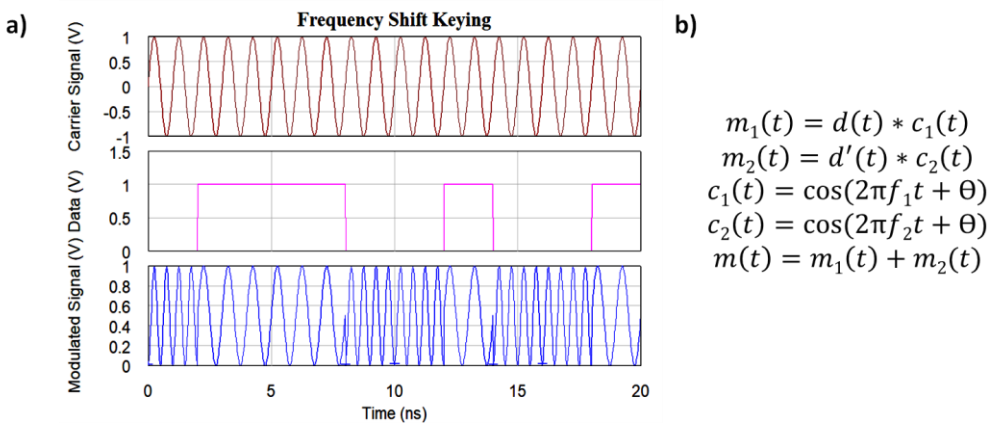


Figure 2.7. a) Carrier (c(t)), Data (D(t)) and FSK (m(t)) waveforms, b) FSK equations

FSK can be detected coherently or non-coherently, just as any other shift modulation schemes. For non-coherent detection, two band-pass filters with each encoding carrier frequencies being the center frequencies of the filters, can be used (Figure 2.8). Detection can also be performed by using a single band-pass filter with one of the carrier frequencies. If this method is used, demodulation can be reduced to amplitude shift keying demodulation.

$$d = \Delta f T \qquad Eq(2.5)$$

Just as any other analog demodulation method, envelope detectors are also included into the design. One problem with the two band-pass filter non-coherent detection is the overlapping issue. Frequency spacing of the two selected frequencies must be greater than the data rate, meaning that d index should be greater than 1. If this is not the case, detection error and noise-like behaviour caused by the band-pass filters cause excess Bit-Error-Rate (BER) at the demodulator.

Another method to detect FSK is to use discriminators. A discriminator converts frequency variations into amplitude variations. By using a frequency discriminator, the frequency separation is at first converted into a phase difference with a linearly inverse relationship by utilizing delay. Then, with the help of a phase detector, the FSK signal turns into an amplitude modulated signal. The advantage coming from this approach is that the frequency separation constraint of "d being greater than 1" is no longer necessary. Hence, higher data rates can be achieved if discriminator approach is used at the demodulator for non-coherent detection methods. However, with frequency separation becoming smaller, robustness is significantly affected, especially at the modulator end. In the tests, non-coherent detection is used for its simplicity and robustness.

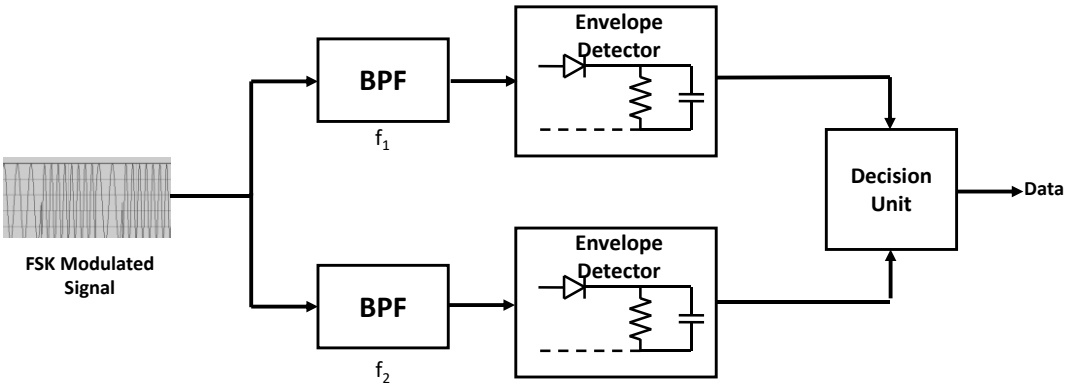


Figure 2.8. Non-coherent FSK demodulation diagram

Besides the standart FSK modulation, there are also other sub-schemes. Continuous phase frequency shift keying (CP-FSK) is one of these methods. In regular FSK, phases of the two carriers are not necessarily the same at bit transition points. This causes hasty phase changes. These abrupt changes result in decrease in spectral efficiency. In CP-FSK, phases are adjusted so that there are no abrupt changes in the modulated waveform, this is done by arranging the frequencies of the carriers in a way that a bit duration can overlap with it for every single bit transferred. The CP-FSK system can be seen in Figure 2.9. Detection of CP-FSK is performed coherently. As the bandwidth can now be used more efficiently, the band-pass filters can operate more loosely. Compared to non-coherent detection of FSK, with CP-FSK, seperation contraint d can be smaller, to levels of 0.7 [62]. For maximum spectral efficiency, CP-FSK modulation is used.

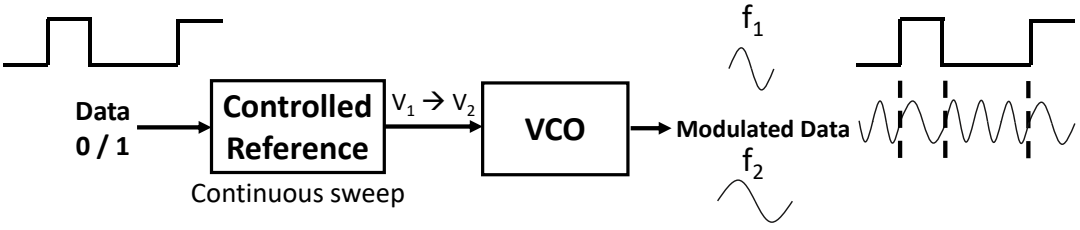


Figure 2.9. CP-FSK modulation overall diagram

2.3.3 Phase Shift Keying Design

Digital phase modulation – Phase Shift Keying (PSK) – encodes data by using phase changes for different symbols. With the fact that each channel has delays [63], since phase shifting corresponds to time delays, phase shift keying generally requires coherent detection. The type of PSK in which each symbol carries a single bit information is called Binary Phase Shift Keying (BPSK).

In coherent BPSK, carriers are seperated from each other by 180° phase shift. Detection is performed by using a reference carrier waveform, that is derived from the incoming signal waveform. This operation requires a loop oscillator algorithm. Another BPSK form is the Differentially Encoded Phase Shift Keying or DE-PSK. In DE-PSK main difference is the denotation of the incoming carrier signal. Instead of encoding each symbol with a different phase, in DE-PSK change in phase means a change in the symbol, meaning that phase only changes at times when symbol changes. Then the signal returns to the original phase.

Modulated Differential Phase Shift Keying (DPSK) and DE-PSK are the same. The difference is the demodulation algorithm. Rather than extracting the exact carrier waveform as a reference, previous bit sequence encoding is used for data recovery. Modulated waveforms of BPSK and DE-PSK/DPSK are shown in Figure 2.10.

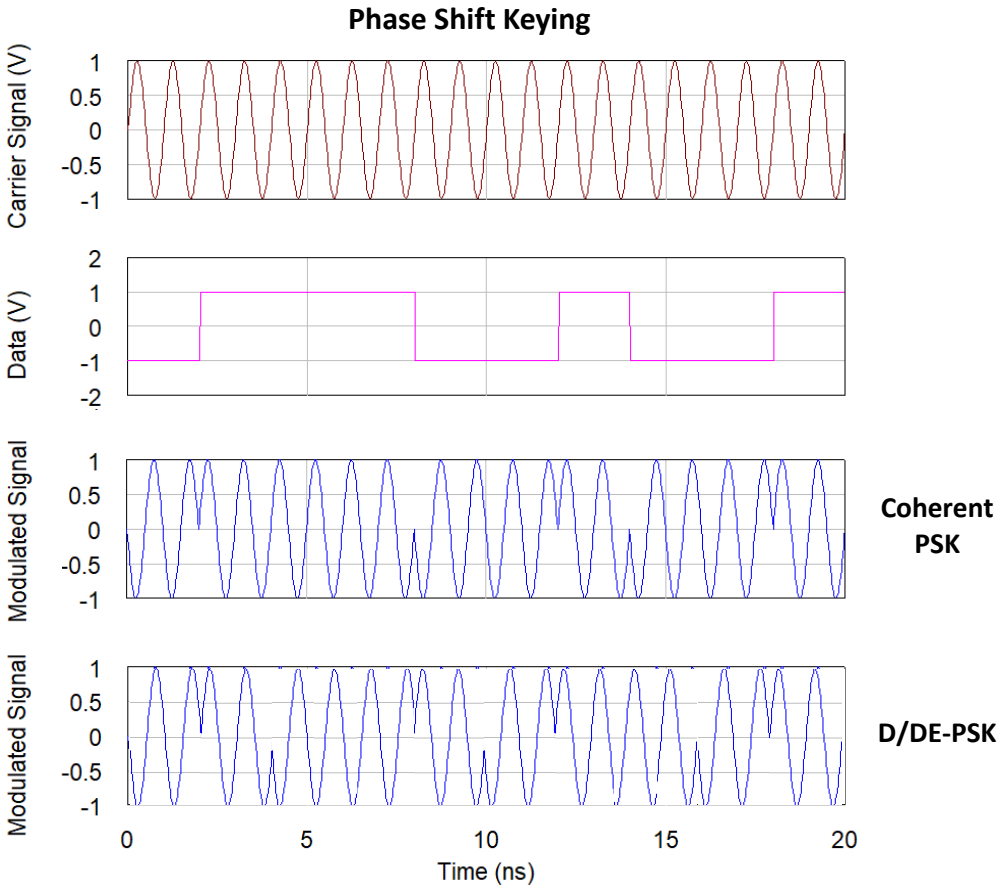


Figure 2.10. BPSK modulated signal waveforms with carrier and data inputs

As it can be seen, modulated waveforms of coherent BPSK and D/DE-PSK are different. In D/DE-PSK, change of data input is modulated with the phase shifted carrier, instead of assigning phases to different symbols.

For modulation of coherent BPSK, the system that is shown in Figure 2.11 can be used. It should be noted that the mixer is a non-linear element used to mix the carrier signal with the level converted analog input. Same system can also be used for other BPSK forms if the digital input is manipulated accordingly. In the scheme tests, an analog mixer is used with upconverting property. Mixer performs the operations given in Figure 2.11, offset correction of the data, upsampling to improve bandwidth with rect filter and finally mixing processed data with the carrier.

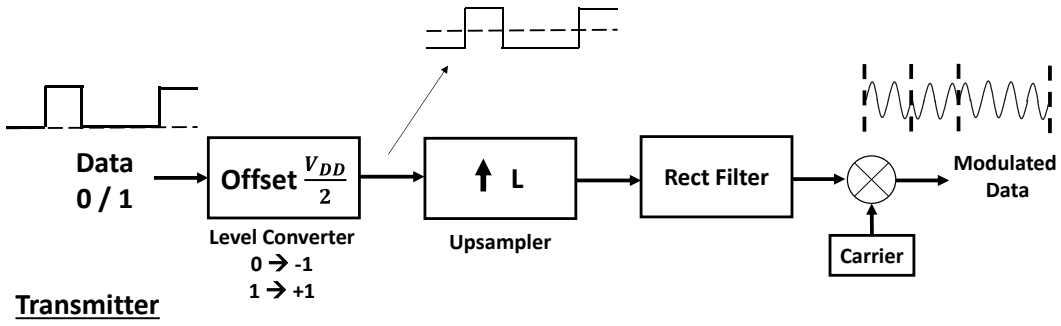


Figure 2.11. BPSK modulation diagram

For the detection of BPSK, coherent and non-coherent mechanisms can be used. In Figure 2.12, coherent detection of BPSK is shown. Input waveform is mixed with the reference waveform which has the same phase with the received signal's original carrier. Output waveform, which include second harmonics of the original carrier, is than integrated over a period, leaving the squared terms. Then, output of the mixer is digitized and mixed with itself again at sampled instances, with rates at least the double of the original data rate. Finally, with a decision unit, sent data is extracted. Coherent multiplication is used for BPSK detection.

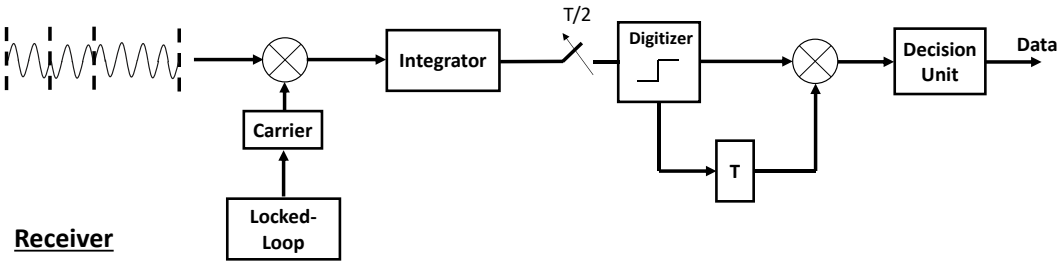


Figure 2.12. BPSK demodulation diagram

2.4 Data Modulation Scheme Test Setup

Two general foundations of wireless data transmission are transmission method and data modulation technique. Data transmission method is selected to be an inductive link, considering the study limitations and compatibility issues. For choosing data modulation scheme, there are 3 possible candidates: Amplitude Shift Keying, Frequency Shift Keying and Phase Shift Keying. Considering that data transmission speed is not a design consideration, robustness and operation with limited bandwidth - single carrier and magnet free inductive coupling are the most cruical aspects during modulation scheme selection.

With MRI compatibility concern bringing alignment and varying coupling conditions, selected modulation method should provide operation for the required alignment and coil distance range. For this specific problem, in order to choose the proper modulation scheme, at first, using Applied Wave Research (AWR) Sofware, simulations are performed. These simulations include basic modulator and demodulator circuitries as explained in the previous section. The sole purpose of these simulations are to provide information about the characteristics of these modulation schemes.

Following the simulations, A Printed Circuit Board (PCB) is designed to test the modulation schemes under varying coupling conditions with the inductive link. Test results are compared and result are tabulated for ASK, FSK and PSK schemes. For this operation discrete analog mixer ICs are used. Specifications of the analog mixers are given in Table 2.3

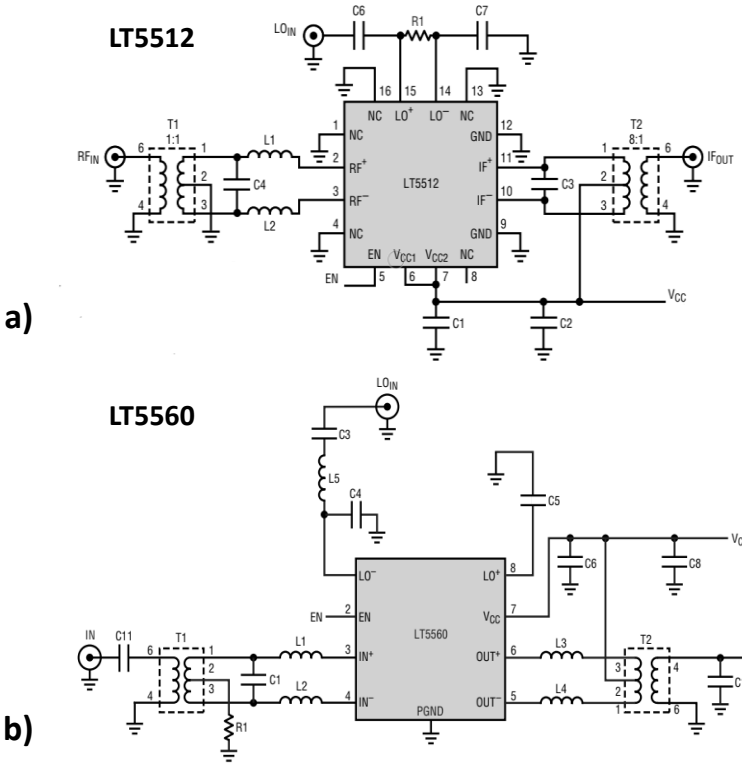
Table 2.3 Analog Mixers Specifications [64].

	LT5526	***LT5512***	***LTC5562***	***LT5560***
Bandwidth	0.1 MHz-2 GHz	1 kHz-3 GHz	0-7 GHz	10 kHz-4 GHz
LO to RF leakage	-65 dBm	-63 dBm	-55 dBm	-52 dBm
RF to LO isolation	69 dB	61 dB	42 dB	52 dB
LO to IF leakage	-56 dBm	-35 dBm	-45 dBm	-47 dBm
Noise figure	12.7 dB	11 dB	13.9 dB	10.5 dB
Input 3rd Order Intercept	15.2 dBm	20.4 dBm	19 dBm	10.1 dBm
2RF-2LO Output Spurious Product	-75 dBc	-66 dBc	-62 dBc	-68 dBc
P1dB	5 dBm	10.5 dBm	7 dBm	-0.8 dBm

For the demodulation operation, LT5512 is widely used in Wireless Medical Telemetry Systems with its lowest minimum available frequency of 1 kHz. Having low noise figure (NF) and high 3rd order intercept point, it is the best candidate for downconverting applications. The high LO port to IF port leakage does not cause any problems since the LO component in the IF port can be filtered.

For the modulation operation, LO-IF leakage should be small, so harmonics of the carrier frequency are not observed at the output. This leakage generates DC offset at the output, too. These effects also can be filtered using a low pass filter as well. IF-LO leakage causes harmonics of the data input which corrupts the data so it should be small. LT5560 is the better choice among the components except the P1dB point. However, this is not an important issue since the mixer can be used with a low input carrier signal with a power amplifier.

According to these criterias, structures for modulation and demodulation in Figure 2.13 are realized.



Component	Value
L1	47nH
L2	47nH
C1	0.01uF
C2	1uF
C3	1.8pF
C4	10-100pF
C6	0.01uF
C7	0.01uF
R1	50-150 Ohm

Component	Value
L1	180nH
L2	180nH
L5	100nH
C1	100-300pF
C3	1000pF
C4	8.2pF
C5	1000pF

Figure 2.13. a) LT5512 configuration, b) LT5560 configuration

Using these mixer configurations a PCB is designed and manufactured (Figure 2.14). In this section, simulation results of ASK-OOK, FSK-BinaryFSK and PSK-BinaryPSK are given in terms of spectral efficiency and bit-error rate (BER) under the same and constant coupling conditions. Then, test performances of these schemes with varying alignment and distance situtations are illustrated.

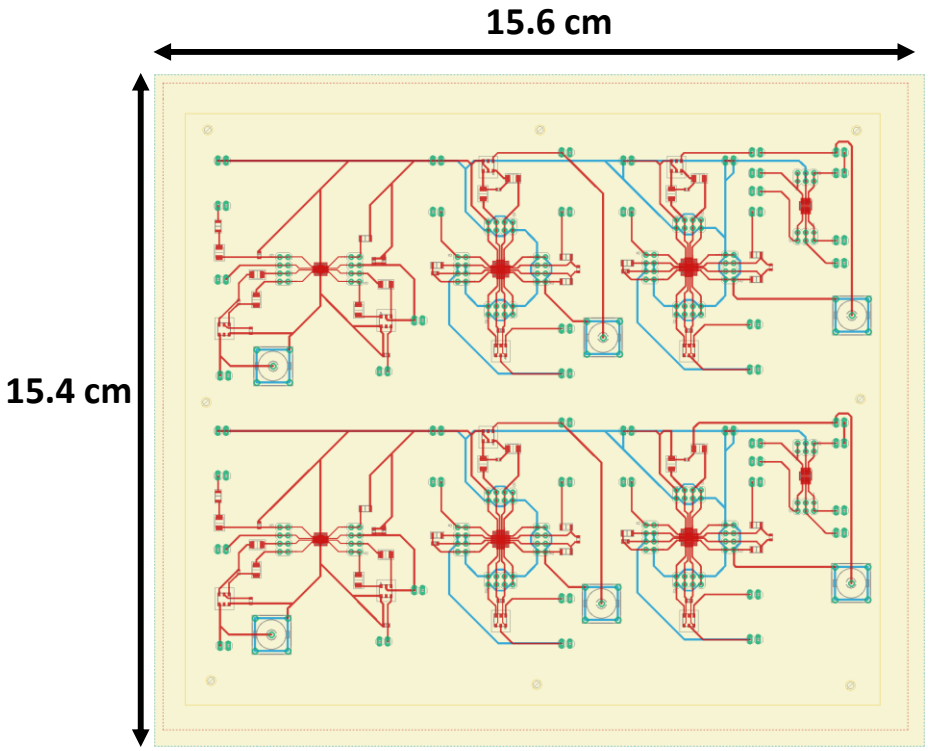


Figure 2.14. PCB layout of test mixers

PCB design is done using AutoCad Eagle Software.

2.4.1 Simulation Results

In order to test different schemes waveforms were as follows:

1- For ASK, LT5512 is used as the modulator with data input being upconverted with the carrier. Received signal at the receiver side is downconverted with the carrier to extract data using LT5560.
2- For FSK, two LT512s are used for modulation of the data and inverse of the data separately with upconverting using two carriers, then summed BFSK signal is transferred. Received waveform is downconverted using two LT5560s, with both of the carriers.
3- For PSK, a similar approach to FSK modulation is used. Each phases with 180° shift are used to modulate and its complement with 1 bit symbols,

upconverting using LT5512s, for the demodulation, modulated waveform is downconverted with the 1 symbol duration delayed version of the modulated data, for coherent detection using a single LT5560.

For all transferring schemes, bit error rates (Figure 2.15) and spectral efficiencies (Table 2.4) are calculated according to the simulations. BER is calculated by dividing the number of falsely detected bits to the number of the overall bits transferred. For each method, SNR is adjusted by adding white gaussian noise to the transfer medium.

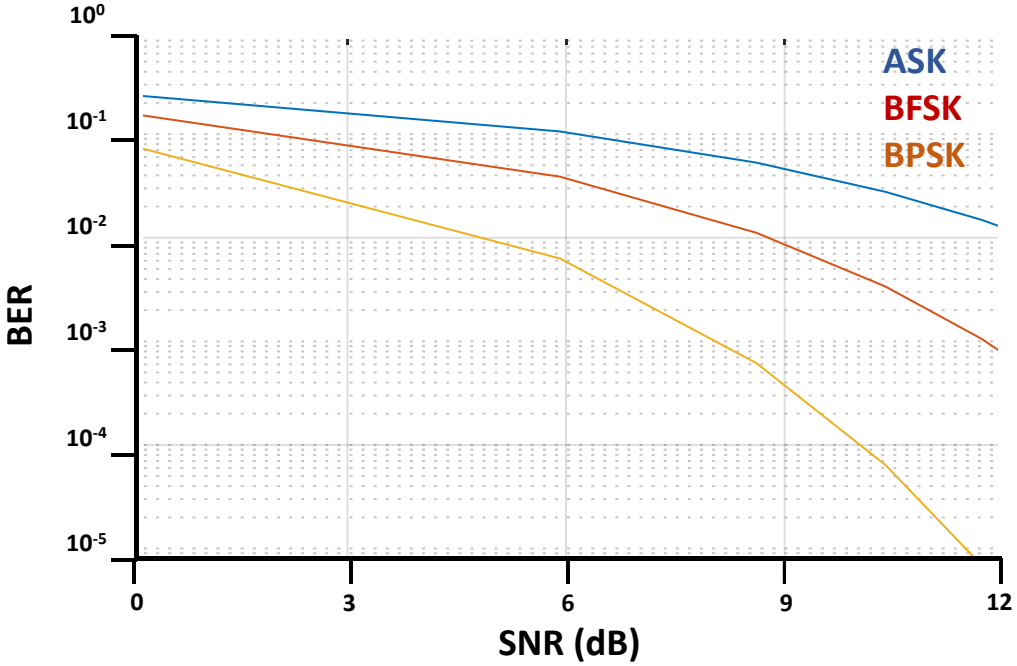


Figure 2.15. BER vs SNR characteristics of ASK, BFSK and BPSK

BPSK among other schemes shows the best performance under additive medium noise. For Spectral Efficiency, normally, assuming that all bandwidth is available for all of the schemes, metric of bits per second per Hz is used. However, abrupt phase changes in non CP-FSK FSK schemes and BPSK, edges of the bandwidth cannot be utilized as efficiently. Moreover, filter performances affect efficiency of the data transfer system. To find out spectral efficiency, SNR and data rate are

swept. In the frequency spectrum, highest data rate that bandwidth is still limited to initial bandwidth is found. In Table 2.4, comparison of spectral efficiencies of ASK, BFSK, BPSK are shown.

Table 2.4 Spectral efficiencies and corresponding coupling coefficients

Modulation Scheme	*Bit/Sec/Hz*	*Minimum Coupling Coefficient*
ASK	0.5	0.12
BFSK	1.0	0.09
BPSK	1.0	0.06

BPSK, can operate at lower coupling coefficients with the same spectral efficiency of BFSK. Since both methods are coherent, detection related variations are minimized. ASK has a lower base Bit/Sec/Hz value with larger minumum coupling coefficient.

2.4.2 Test Results

In simulations, detection performances are only investigated under spectral efficiency. Coupling conditions variations, on the other hand, can be considered as additional noise. For varying coupling conditions, BERs of the modulation schemes are inspected. Test setup can be seen in Figure 2.16.

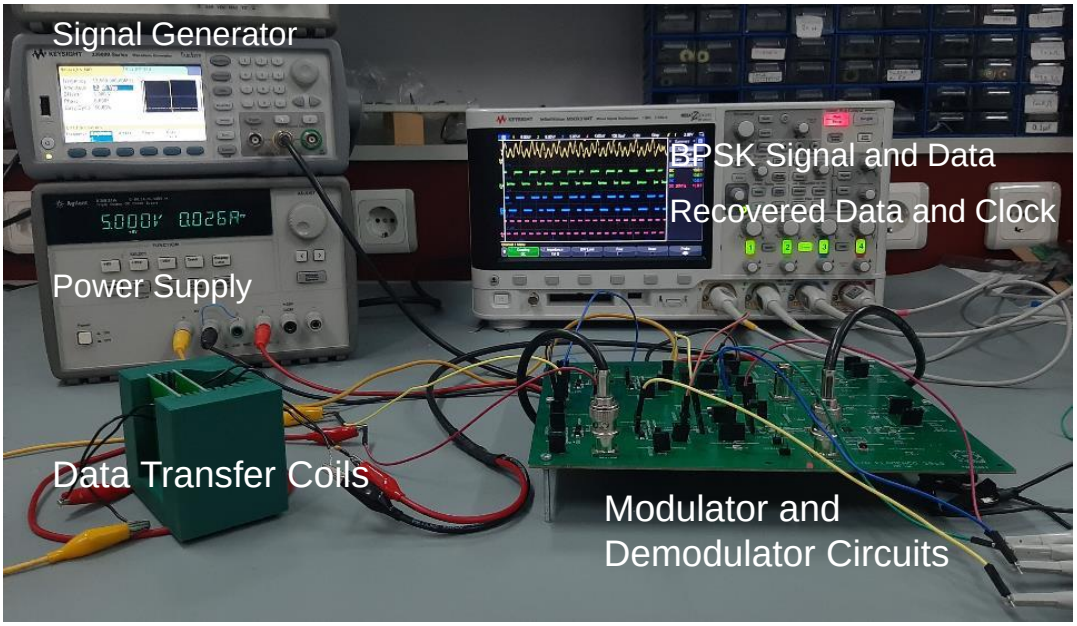


Figure 2.16. Coupling and detection test setup

BERs of ASK, BFSK and BPSK are shown for varying coupling conditions in Figure 2.17. It can be seen that ASK cannot operate at coupling conditions lower than 0.16. This is due to the fact that the coupling variations directly change the amplitude of the received signal, meaning that worse coupling conditions decrease SNR directly. For FSK, performance is better than ASK, however narrow bandwidth of the system in transmitter side burdens the demodulator performance. Filters used for non-coherent detection need to have large quality factors, increasing power consumption and complexity significantly. In PSK, noise affects both phases equally, meaning that the received waveform has the same amplitude and frequencies regardless the coupling coefficient. Therefore, PSK can be reduced to the BER-SNR relation directly and it is affected by the changes of coupling conditions minimally.

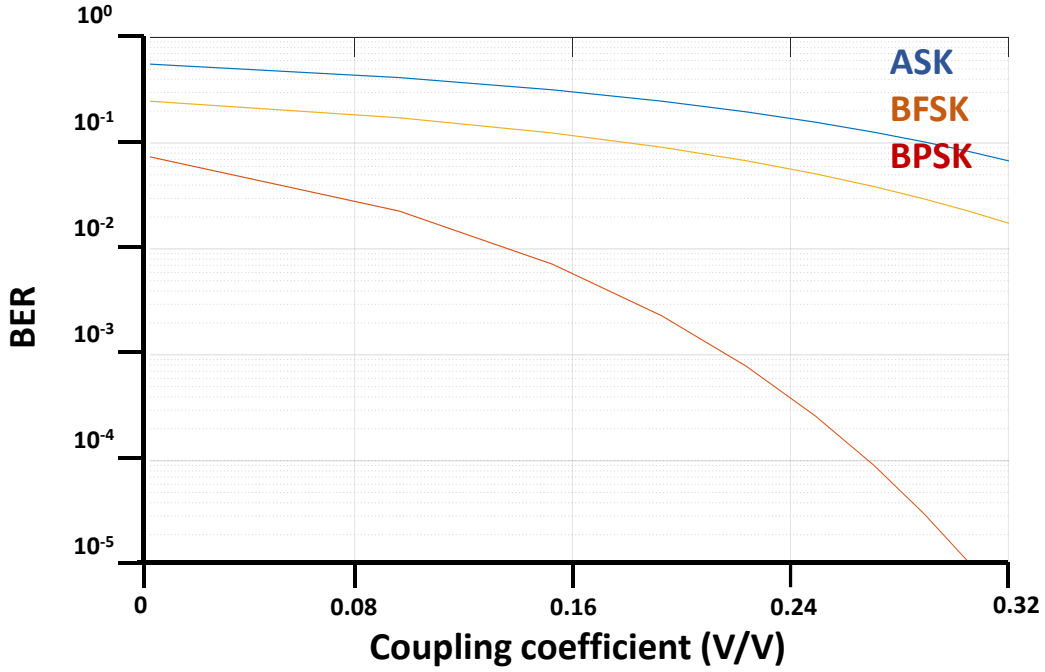


Figure 2.17. BER vs coupling coefficient for ASK, BFSK and BPSK

2.4.3 Discussion

In order to choose the best possible modulation scheme, simulations and tests are performed. First, a PCB consisting of analog mixers, used as downconverters and upconverters is designed. Then modulation schemes, ASK, BFSK and BPSK are simulated under varying Signal-to-Noise (SNR) conditions. It is seen that BPSK is the more robust option compared to other two under simulations. Then, to further investigate performances of the schemes, ASK, BFSK and BPSK transferring data rates are increased and the point of performance degradation is compared. For choosing the minumum coupling condition that the scheme can work, BER is chosen as 0.25 since symbols are 1 bit size. It is found at that BPSK can work at lower coupling condition with higher transmission rate.

Finally, PCB is tested under varying coupling condition to investigate BER variation with condition. ASK is not able to perform reliably under 0.16 coupling coefficient. BFSK performs better than ASK, however, to further increase its

performance, high quality factor filters and presicely controlled oscillators are necessary. Since the tests are performed under same conditions for BFSK and BPSK cases, or given conditions, BFSK is far from BPSK performance-wise. With its reliability and noise insensitivity BPSK is the best choise among these three modulation schemes. BFSK with wide bandwidth application is not considered since for the application concerned, single carrier bandwidth and narrow bandwidth is necessary. Overall, for the data transmission system, BPSK is chosen as the modulation scheme.

CHAPTER 3

SEMI COHERENT BINARY PHASE SHIFT KEYING SYSTEM

3.1 Motivation

In wireless data transmission systems, modulation and demodulation circuits vary in between coherent and non-coherent detection. Coherent detection systems are robust, affected less by delay distortion and circuit noise. On the other hand, detection circuits for coherent detection are complex and generally require multiple oscillators, which increase power consuption and occupy large area. In Binary Phase Shift Keying (BPSK) and Differential Phase Shift Keying (DPSK), tolerance of the system in additional phase shift is needed to be addressed at both modulator and demodulator ends.

For BPSK modulators, many approaches can be chosen. By its nature, BPSK and DPSK are quite similar to Amplitude Shift Keying (ASK). The difference is that data is encoded twice with On-Off Keying, with data input being the 1's complent for the second carrier. Second carrier has the same frequency with the first one but there is a phase shift in between the carriers. For our case, this phase shift is 180°. Two distinct ASK waveforms then can be summed up and BPSK or DPSK modulated signal is obtained.

BPSK demodulation can be performed by coherent and non-coherent measures. Coherent detection requires creation of the original carrier waveform with its frequency and phase matched with the sent carrier waveform. Locked-Loop circuits are necessary for this matching operation. However, these circuits consume large amounts of power, compared to the overall receiver side power consumption [65].

In this chapter, design and implementation of the BPSK wireless data transfer system with its modulator and demodulator blocks are presented. Modulator is used to encode the data in BPSK form with 13.56 MHz carrier frequency. Data rate is 10 kbps, however it can be increased if desired. Modulator utilizes the fact that DPSK is an addition of ASK with two branches. 180° shift in phase is achieved by differentiation of the ASK modulated waveforms. Demodulator operation is semi-coherent. There is a voltage controlled oscillator at the receiver end. Oscillator is relaxation type and produces 13.56 MHz square wave signal. Demodulator detects the points phase changes by utilizing the 13.56 MHz signal as the clock and checking the received BPSK signal at phase change points.

Section 2 of this chapter explains the modulation operation. Modulator circuit is explained and BPSK modulation is shown. In Section 3, demodulation circuit is presented. Patient fitting operation with data conversion from the bit stream into a meaningful parallel output is shown in Section 4. In Section 5, experimental results are shown. Finally, in Section 6, possible improvements are shown and performance is discussed.

3.2 BPSK Modulator

The first step in any wireless data transmission (WDT) system is to manipulate the data signal so that it can be transferred easily. In our defined problem, WDT system has to perfom under different coupling conditions as the alignment and distance between the coils in the inductive link are not constant since there is no magnet present, making the system magnetic resonance imaging compatible. Coupling performance will be discussed in the latter sections since it can be dealt with or observed with other perspectives, from receiver end for instance.

Data transfer systems and modulation schemes require a carrier for data transfer operation, or more correctly to bury the data into an easily transferable signal. In the design, carrier generation is not mentioned as a separate block. It is assumed to

be always available for use. The general block diagram of the modulator is shown in Figure 3.1. Same carrier voltage is used for both of the phases. By using common gate amplifiers, data is amplitude modulated for both data input and inverse of the data input. The output waveforms for each modulation operation have the same phase. Difference of these two signals would result in 180° phase shift for data and its complement.

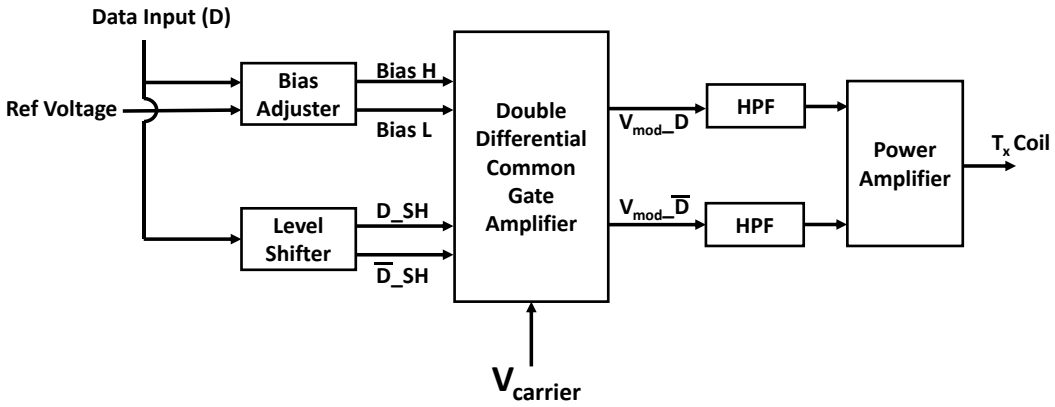


Figure 3.1. BPSK modulator overall diagram

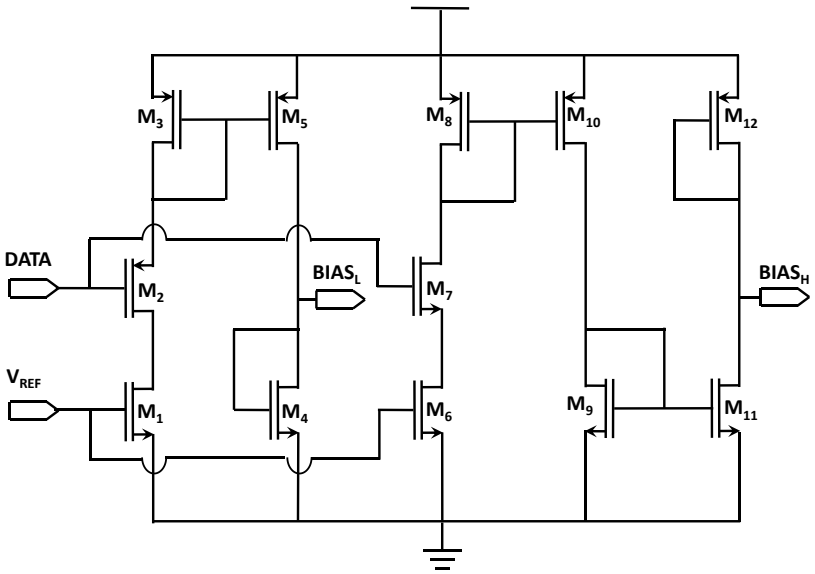
High Pass Filters (HPF) are used to get rid of the DC offset voltage, making the DC offset 0 V. Minimum voltage available in the design is 0 V, meaning that without on chip inductors, transmitter coil would set the branches of the amplifier the same as DC voltagewise and disrupt operation. Using HPF allows separation of the amplifier branches from receiver coils' and power amplifiers' loading effects. HPFs are passive RC filters with large resistances so that power consumption becomes low.

Design does not include an on-chip power amplifier since coil is driven with differential input with 0 V DC offset. Operation with power amplifier will also be explained in latter chapters of the thesis. Ideally, in a shift keying data transfer system, for the best spectral efficiency, modulation index should be as small as possible whilst allowing demodulation within an acceptable bit-error-rate (BER) level. To achieve small modulation index, transitions at data change points should

be smooth. With two different ASK modulation, achieving the ideal spectral efficiency is an issue. The advantage of such a system is its simplicity and low power consumption.

3.2.1 Bias Adjuster

The first block of the modulator is the bias adjuster. Basically, bias adjuster block generates two signals for the common gate amplifiers that create the two amplitude modulated signals forming BPSK when differentiated. Two signals, $BIAS_H$ and $BIAS_L$ are modulated or analog multiplexed versions of the input reference voltages themselves. DATA inputs are rail-to-rail, hence bias adjuster keeps leakage currents small on amplifier blocks. Morever, since the data rate is 10 kbps, transistor sizes do not have to be large in the bias adjuster circuit. In view of these items, the bias adjuster circuit is designed as given in Figure 3.2.



M_1	2 µm/1 µm
M_2	3 µm/1 µm
M_3	3 µm/1 µm
M_4	3 µm/1 µm
M_5	6 µm/1 µm
M_6	2 µm/1 µm
M_7	2 µm/1 µm
M_8	3 µm/1 µm
M_9	3 µm/1 µm
M_{10}	6 µm/1 µm
M_{11}	3 µm/1 µm
M_{12}	6 µm/1 µm

Figure 3.2. Bias adjuster circuit

When DATA is high, M_2 is off. Then no current passes through M_3 transistor and M_5 transistor. $BIAS_L$ becomes 0 V. For the DATA low case, current passing through M_1 transistor is copied to M_4 transistor branch with 2/1 ratio. For M_6 transistor branch, operation is in reverse. M_7 is on when DATA is high, current passing through transistor M_6 is copied to M_9 transistor branch with 2/1 ratio and then copied once more to $BIAS_H$ branch. The aim with this is to bias the amplifier circuit with PMOS using $BIAS_H$ connection. When DATA is low, M_7 is off and $BIAS_H$ becomes 0 V.

With this bias adjustment, two different bias voltages acquired that complement each other. Since at once only one of the current mirror structure is open, total power consumption does not change comparing with a single bias circuit. Also, one advantage is that the bias voltages can be controlled easily by manipulating data signal voltage levels if needed.

Figure 3.3 illustrates the waveforms of the bias voltages created with this bias circuit. The input reference voltage is modulated with DATA input and two bias voltages that are complements of each other are acquired. The circuit can keep up with 10-14 kbps data rate which covers the entire spectrum, however speed can be increased.

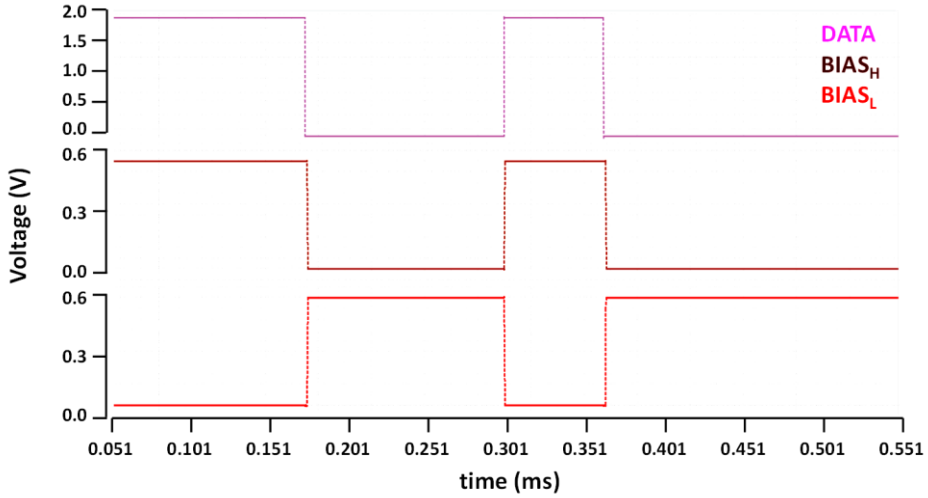


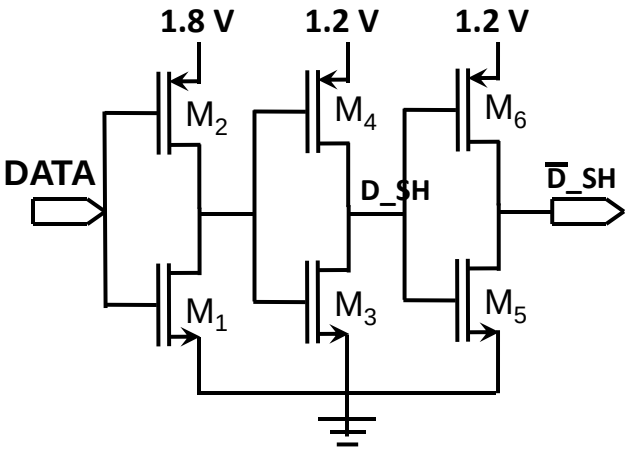
Figure 3.3. Bias adjuster waveforms

3.2.2 Level Shifter

Level shifters are blocks that translate a digital signal from one logic level to another. This way, different voltage level requirements can be satisfied within the design. In our design there are 2 uses of the level shifter. First one is the translation of voltage levels. The design is made with 2V transistors and the supply voltage is 1.8 V. Hence for outside control of the data inputs, if the control device has voltage levels different then 1.8 V, level shifter is necessary. This level shifter is independent from the modulator design and always available on the chip.

The second use of the level shifter is directly related to the modulator. With bias adjuster, modulated bias voltages are created, however, in order to not have remaining charges in the modulator when one of the branches keying the data is not operating, the common gate amplifier needs to be discharged. This is done by introducing data waveform's inverse to each branch respectively to their perspective of the data input. When this is done, the branch that is not keying becomes a simple inverter with output voltage 0. This will be further explained in the amplifier section.

Level shifter can give output as the same data sequence of the input and also as inverse of it. The level shifter circuit is given in Figure 3.4, and Figure 3.5 shows the waveforms.



M_1	0.55 µm/0.18 µm
M_2	0.3 µm/0.18 µm
M_3	1 µm/0.18 µm
M_4	1.5 µm/0.18 µm
M_5	1 µm/0.18 µm
M_6	1.5 µm/0.18 µm

Figure 3.4. Level shifter circuit

An additional input inverter is added as a buffer to design. Transistor sizes are not minimum to be able to drive the inputs of the main modulator block.

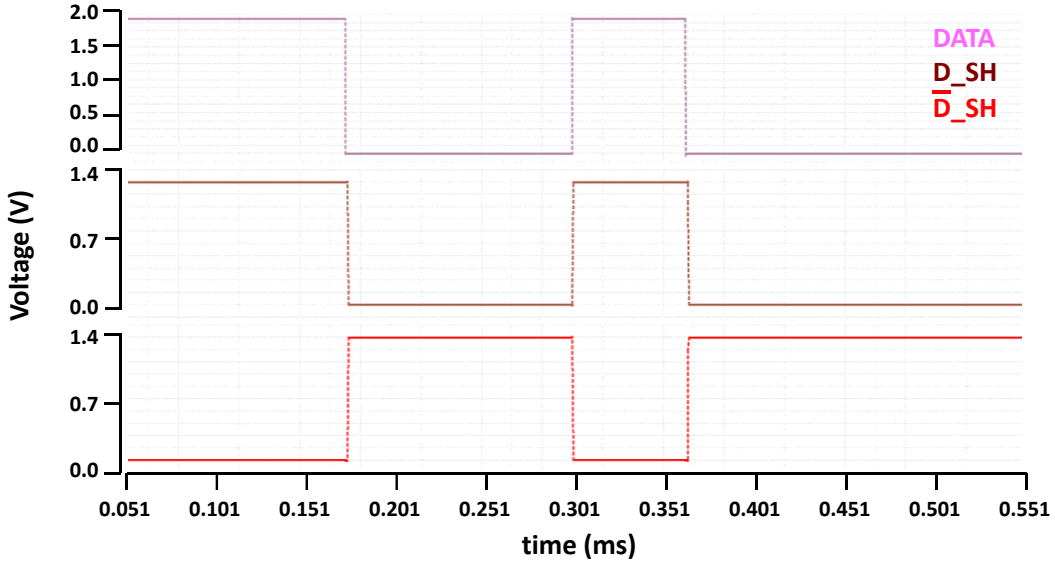
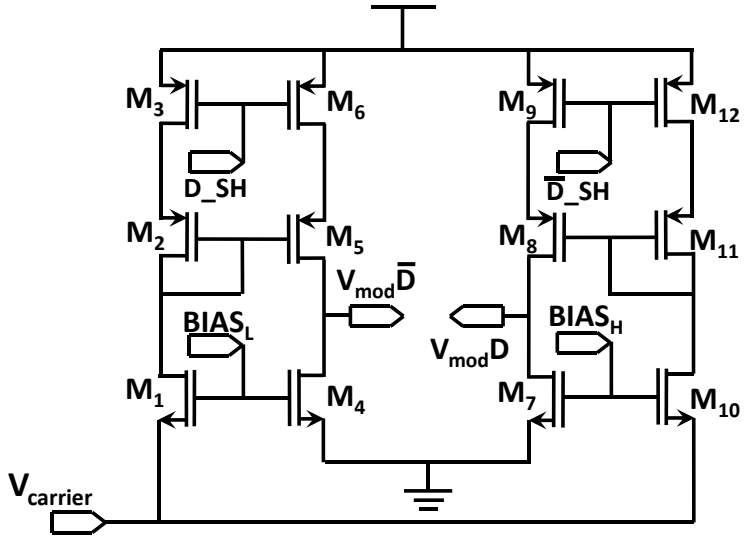


Figure 3.5. Waveforms of the level shifter circuit

3.2.3 Common Gate Amplifier

The main block where the modulation happens is the amplifier block. What we expect from this amplifier block is operation at 13.56 MHz with stable performance. The data rate is 10 kbps in general, hence 13.56 MHz is the highest switching speed for this block. Carrier signal is generated outside of the modulator block. Gain of the amplifier is not crucial since the output can be processed with a power amplifier before driving the transmitter coil if needed. For carrier input of the amplifier, switching speed is an issue since the carrier has 13.56 MHz frequency. Therefore, input impedance of the amplifier should be small and resistive. With this considered, a common gate structure is chosen. Since we are modulating data and inverse of the data separately, we need two amplifiers. The circuit of the amplifier block is shown in Figure 3.6. Branches are kept symmetrical. Transistor sizes are adjusted so that input impedance of the amplifier is small.



M_1	20 µm/1 µm
M_2	10 µm/1 µm
M_3	6 µm/1 µm
M_4	20 µm/1 µm
M_5	10 µm/1 µm
M_6	6 µm/1 µm
M_7	20 µm/1 µm
M_8	10 µm/1 µm
M_9	6 µm/1 µm
M_{10}	20 µm/1 µm
M_{11}	10 µm/1 µm
M_{12}	6 µm/1 µm

Figure 3.6. Common gate amplifier, main modulator block

In the circuit, M_1 and M_{10} transistors are the input transistor for the carrier signal. M_4 and M_7 transistors are kept same in size and they create a reference point for the carrier signal to compare. Carrier signal has 0 V DC offset. Gates of M_1 and M_4 transistors are biased with $BIAS_L$ which is the modulated version of the bias voltage with the inverse of data input. When DATA is low, $BIAS_L$ is high and M_1 and M_4 are on. M_3 and M_6 are also on since DATA is low and D_SH is low in that case. Amplified carrier signal is passed to the $V_{mod}\overline{D}$ node.

On the other amplifier branch, when DATA is low, $BIAS_H$ is low and M_7 and M_{10} are off. With $\overline{D}$_SH being high, M_9 and M_{12} transistors are also off. Then no current passes through the transistors an $V_{mod}D$ node becomes High-Z being isolated from the circuit. With DATA becoming high, $BIAS_L$ becomes low and D_SH is high, meaning that, this time $V_{mod}\overline{D}$ is High-Z. With $BIAS_H$ becoming high, M_7 and M_{10} are on. $\overline{D}$_SH is related to inverse of DATA hence it is low and carrier signal is passed to $V_{mod}D$ node.

The common mode structures are used as switches with this structure, rather than being amplifiers. Therefore, high speed operation is achieved. In Figure 3.7, output waveforms are shown.

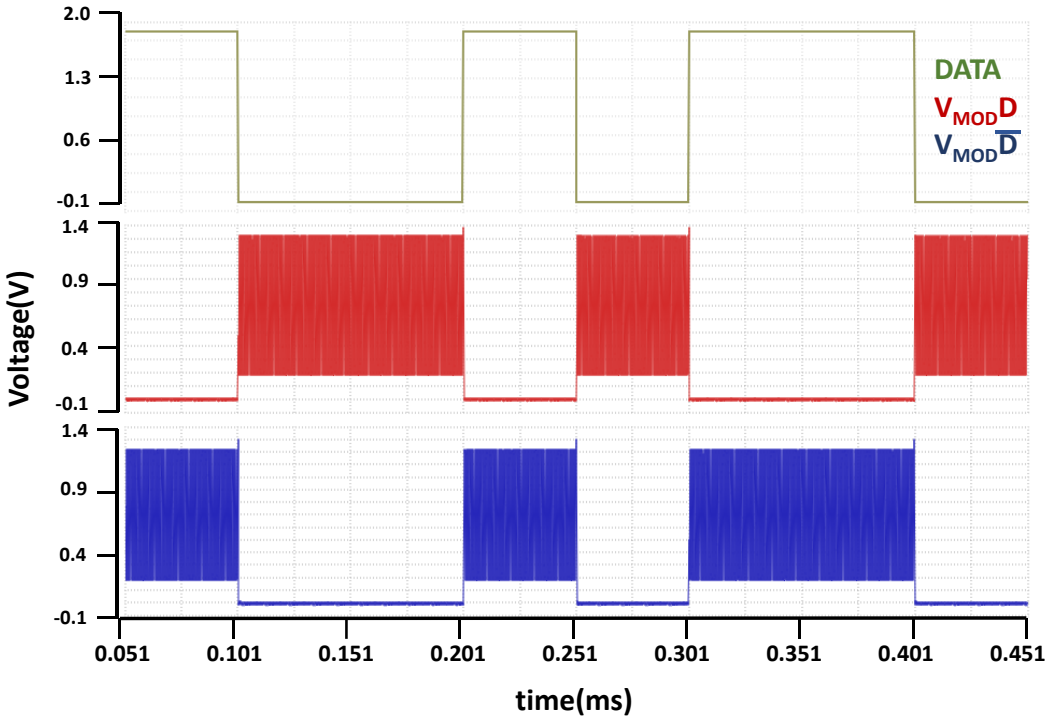


Figure 3.7. Amplitude modulated amplifier outputs

3.2.4 High Pass Filters

Output waveforms of the modulated signals have non-zero DC offset voltages. However, when carrier signal is not observed at the output node, these output voltages are 0 V. In order to get Binary Phase Shift Keying modulated signal, these two signals need to be differentiated. Since for data and data inverse cases, DC offsets are not the same in the modulated waveforms, output of the difference operation would be different than expected with distorted maximum and minimum values. This effect is shown in Figure 3.8.

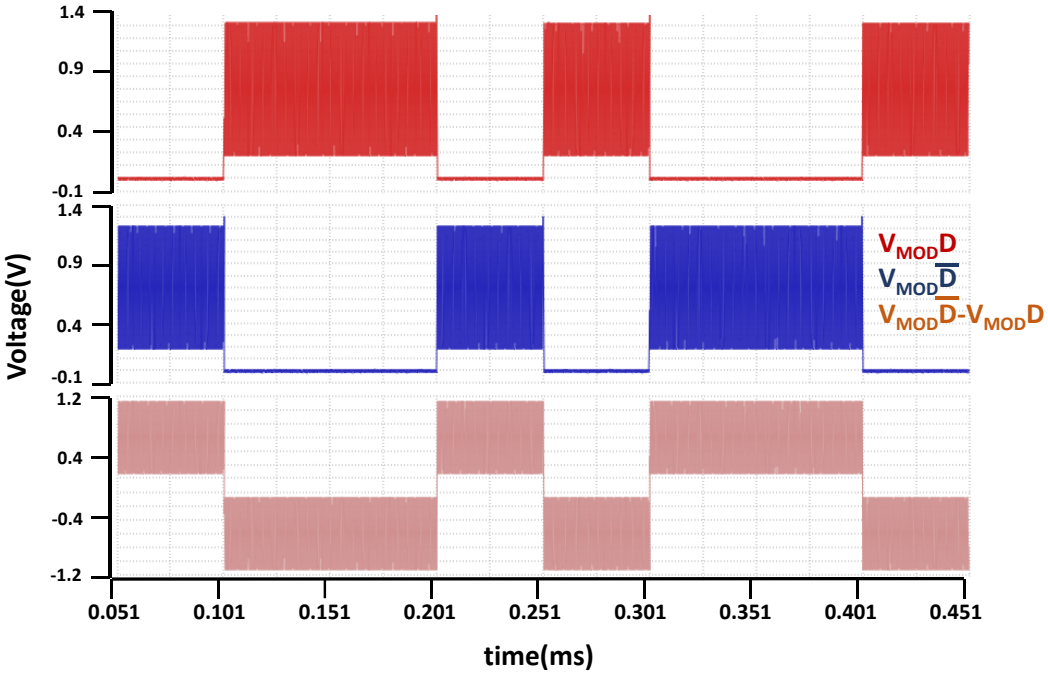


Figure 3.8. Difference and distortion of modulated waveforms

In order to filter out the non-zero DC offset of the ampitude modulated waveforms, high pass filters are used. High pass filters in the system are passive RC filters. Passive filters are chosen since accuracy and compactness are not issues for the filter design. Moreover, with passive filters, whenever needed, external low pass filter can be added to convert the filter into a bandpass filter, and it is easily tunable with external components to adjust the cut-off frequency if another carrier frequency is wanted to be used. The filter structures are shown in Figure 3.9. There are 1st and 2nd order filters shown, on chip design includes 1st order structure, if needed 2nd order filter is added with external components. Equations governing the filter behaviour for 1st and 2nd order structures are given in Eq 3.1. and Eq 3.2.

$$f_c = {}^{1}/_{2\pi RC} \qquad Eq(3.1)$$

$$f_c = {}^{1}/_{2\pi\sqrt{R_1C_1R_2C_2}} \qquad Eq(3.2)$$

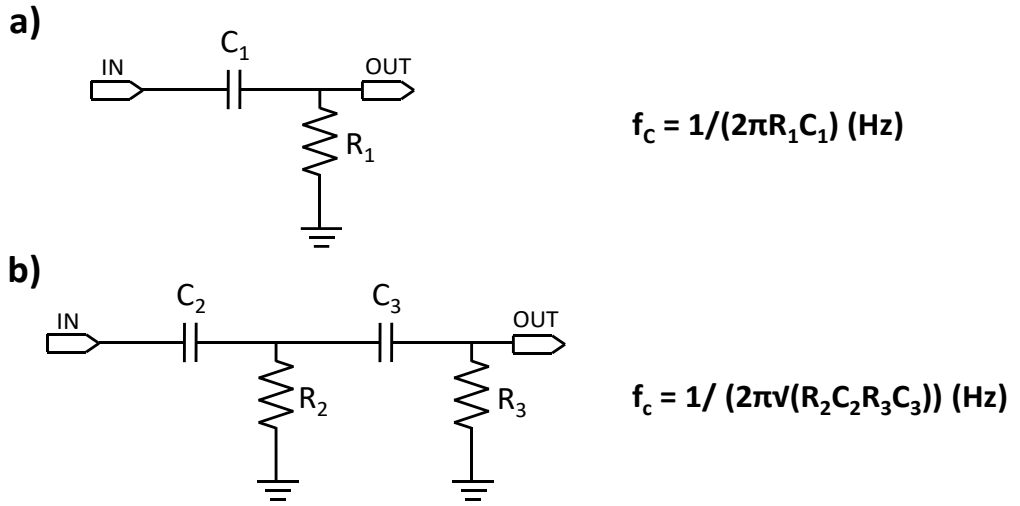


Figure 3.9. Passive high pass filters and cut-off frequencies (a) first order (b) second order

For the 1st order passive high pass filter, a polysilicon resistance of 120 kΩ is used. Filters consume 6 µA current together, since only one is active at the same time. Corresponding MIM capacitor value for the cut-off frequency of 13 MHz is 100 fF. Filter responses, phase response and magnitude response are given in Figure 3.10.

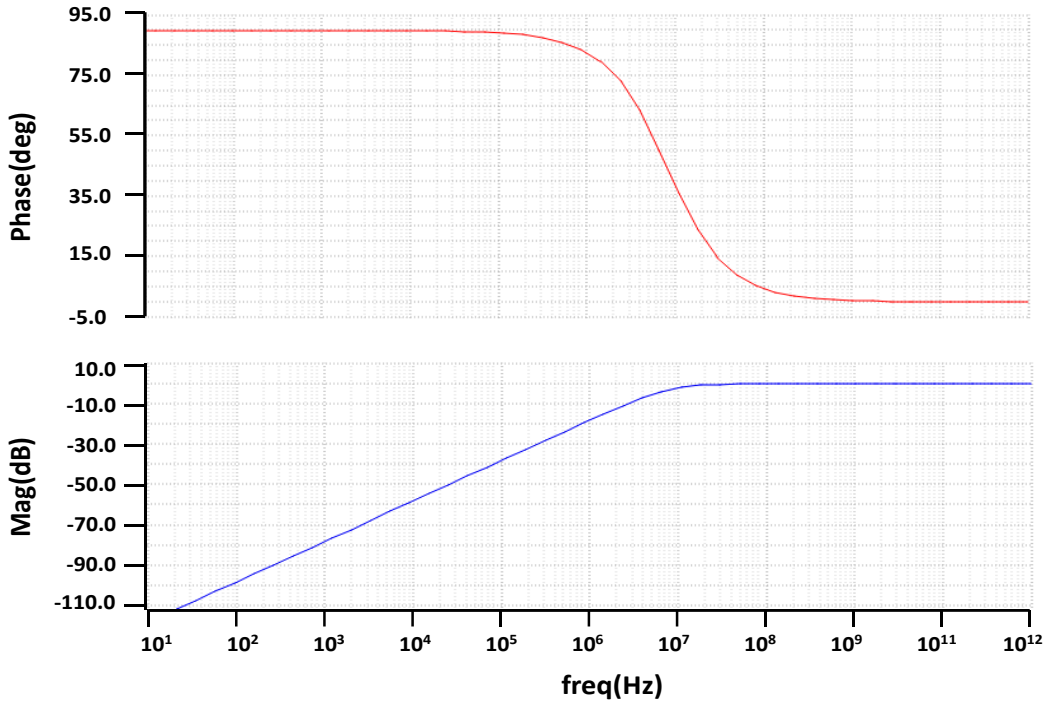


Figure 3.10. AC magnitude and phase responses of the high pass filter

3.2.5 Simulation Results

The modulator circuit proposed is designed in 180 nm high voltage TSMC(Taiwan Semiconductor Manifacturing Company) process on the EDA software CADENCE and simulations performed with SPECTRE simulation tool.

Modulator block creates the modulated waveforms in two distinct branches and then combines them on the coil. Output waveform does not have any DC offset and hence branches affect operation of each other minimally. Coupling coefficients are calculated with both sides, but generally, for the lowest coupling coefficient that the system has to operate, with 0.05 will be used for the minumum input voltage level for the demodulator operation.

In the simulations, data rate is chosen as 10 kbps, and carrier frequency is 13.56 MHz. Modulator can perform with other carriers but for this modulator design, carrier frequencies are kept the same as the semi-coherent demodulator is designed to work with 13.56 MHz carrier frequency and modulation at other frequencies are not feasible. Results given are conducted with coils connected to the outputs. In Figure 3.11, outputs for data input amplitude modulation and filter outputs are given. Data inverse amplitude modulation and filter ouputs are given in Figure 3.12.

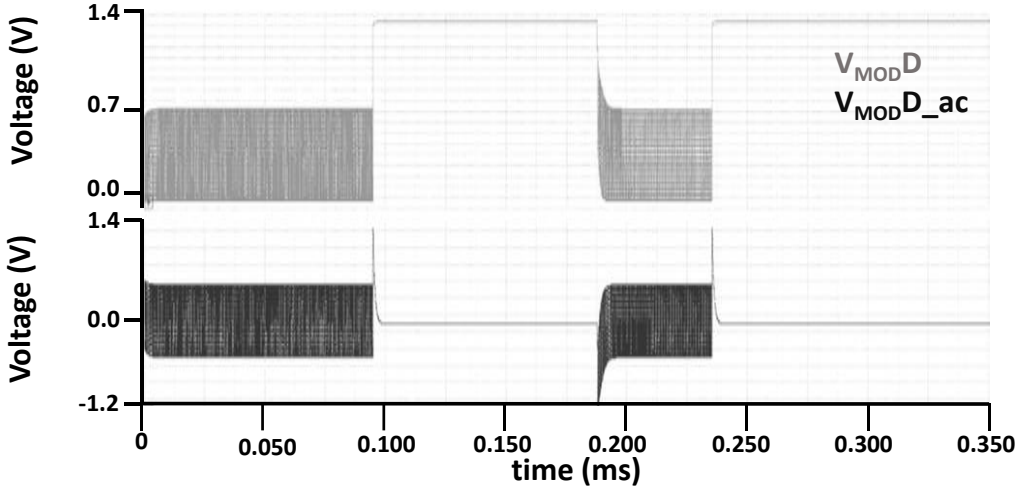


Figure 3.11. Data amplifier modulator and filter outputs

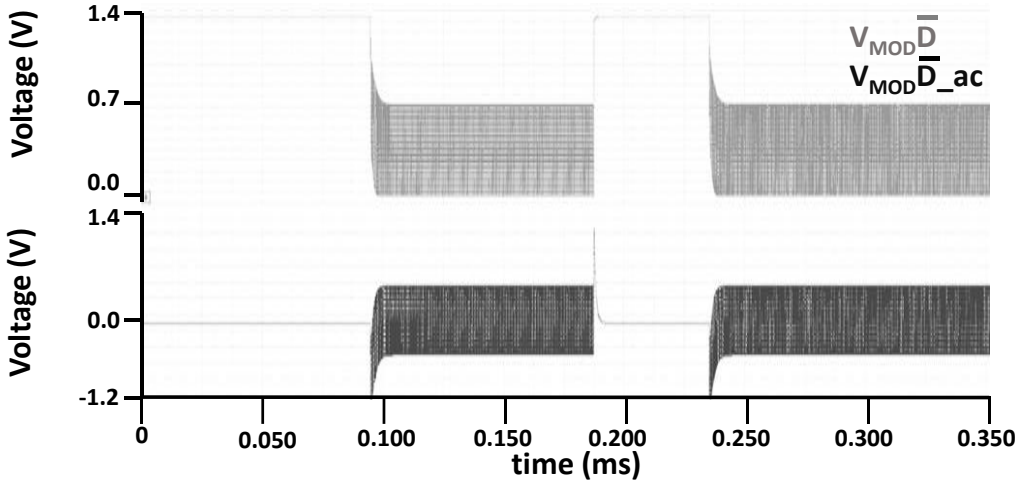


Figure 3.12. Data inverse amplifier modulator and filter outputs

The BPSK modulated signal overall is the subtraction of the filter outputs. The modulated waveform is given in Figure 3.13.

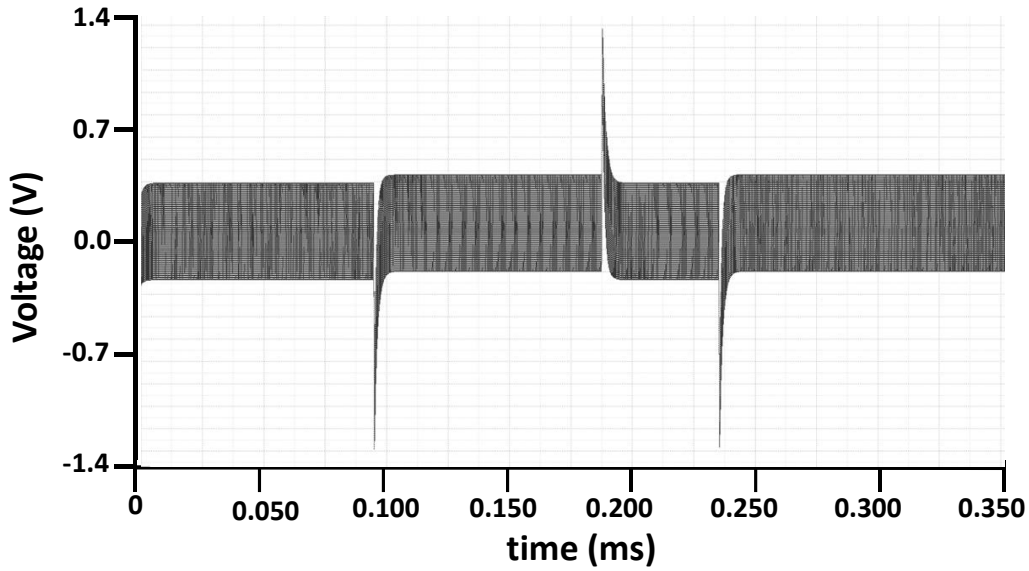


Figure 3.13. BPSK modulated waveform

The parameters defining the modulator performance are given in Table 3.1.

Table 3.1 BPSK modulator parameters.

Parameter	*Value*
Vcarrier-ac	200 mV,pp
Data Rate	10 kbps
Gain	19 dB
Supply Voltage	1.8 V
Power Consumption	224.5 uW
Max Phase Delay	28.2 degrees, 5.77 ns
Carrier Suppression	80 dB
CM Gain	-80 dB
Carrier to Data Leakage	-43 dB

3.3 BPSK Demodulator

The modulated BPSK waveform has to be converted back to data output and clock information is required for timing and reading of the extracted data. In non-coherent detection, Differential Phase Shift Keying Systems are used. These detection methods detect data by checking the modulated waweform for two symbol durations, meaning that to detect data, information at that instant and information of the previous symbol is necessary.

Modulated waveforms in DPSK are different than BPSK as explained before. Therefore if BPSK modulated waveform is given as an input to the DPSK non-coherent demodulator, data will be detected falsely. Because of this, an additional decision unit is required to convert the detected data into the original data signal.

In DPSK detection circuits, detection is perform with analog signals. The incoming signal is processed with a filter and integrator followed by an analog mixer with the

second input signal as a signal that has the same frequency with the original carrier. Phase of the mixer carrier is not important as there will be differences for the DPSK carrier phase shifted signal at all times. Then, resultant signal is shifted by a symbol duration and once more multiplied with itself. Utilizing the orthogonality of waveforms with 180° phase shift, data is recovered. If two consecutives symbols are the same, multiplication operation gives high output, otherwise it gives low output.

In this demodulator design shown in Figure 3.14, these operations are performed digitally and with different order. First the incoming signal is digitized using a common gate amplifier with digital buffers. Then by using this signal with a relaxation oscillator as the start-up, carrier is regenerated. This carrier's frequency is adjusted to the half of the original carrier frequency and initially digitized BPSK modulated waveform is read by this carrier. This allows detecting the points where the phase changes in the original signal. Finally, by uzing a T-Flip Flop, original data is recovered. In this section, operation of the blocks in the demodulator and simulation results are presented.

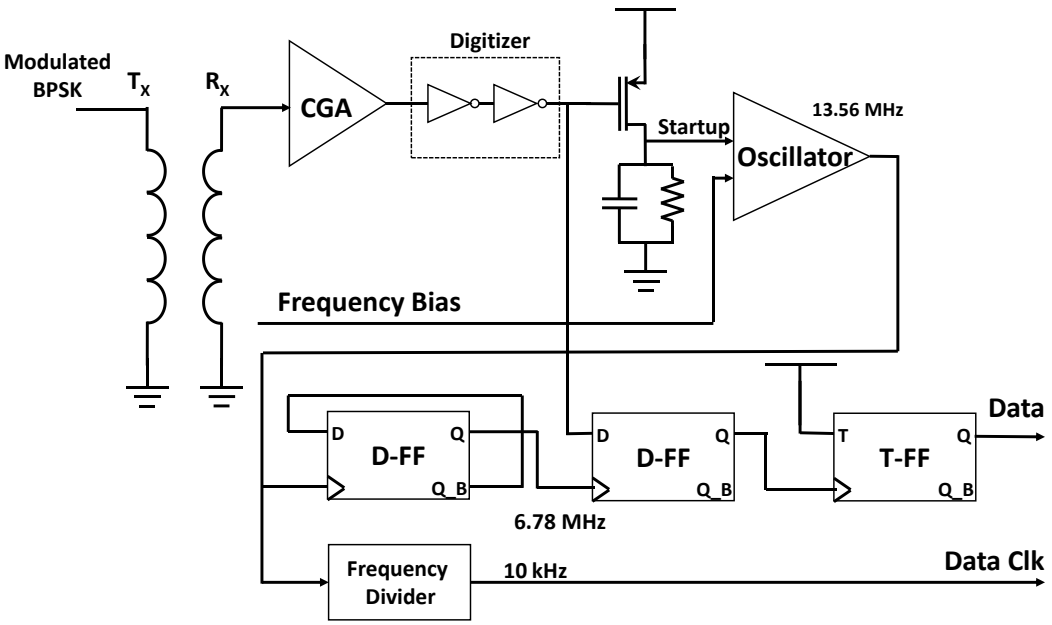
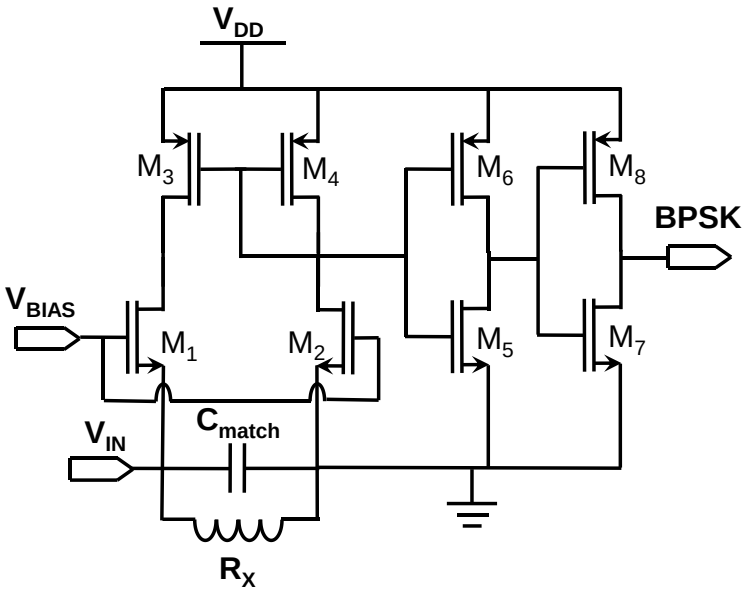


Figure 3.14. BPSK semi-coherent demodulator overall diagram.

3.3.1 Common Gate Input Stage and Digitizer

The received signal at the receiver coil has varying amplitude for different coupling levels. Demodulator operates with digital inputs, hence input signal must be amplified and converted to digital domain. Similar to the modulator case, a common gate amplifier is used for high frequency operation capabilities. During amplification, in order to be able to convert the input waveform to output linearly, output DC voltage level of the amplifier is set to $V_{DD}/2$. Transistor sizes and reference voltage level are set accordingly. Amplifier output is then digitized using a digital buffer with increasing current driving capability. Schematics of the amplifier and digital buffer and shown in Figure 3.15.



M_1	10 µm/1 µm
M_2	10 µm/1 µm
M_3	15 µm/1 µm
M_4	15 µm/1 µm
M_5	6 µm/1 µm
M_6	9 µm/1 µm
M_7	10 µm/1 µm
M_8	15 µm/1 µm

Figure 3.15. 1-Bit Digitizer with delay buffer

The DC voltage at the amplifier output affects the duty cycle of the digitized output. For detection purposes, in the coupling range we have chosen, duty cycle different than 50% does not disturb the operation, however coupling variation does. Digitizer output waveforms for different coupling levels are shown in Figure 3.16.

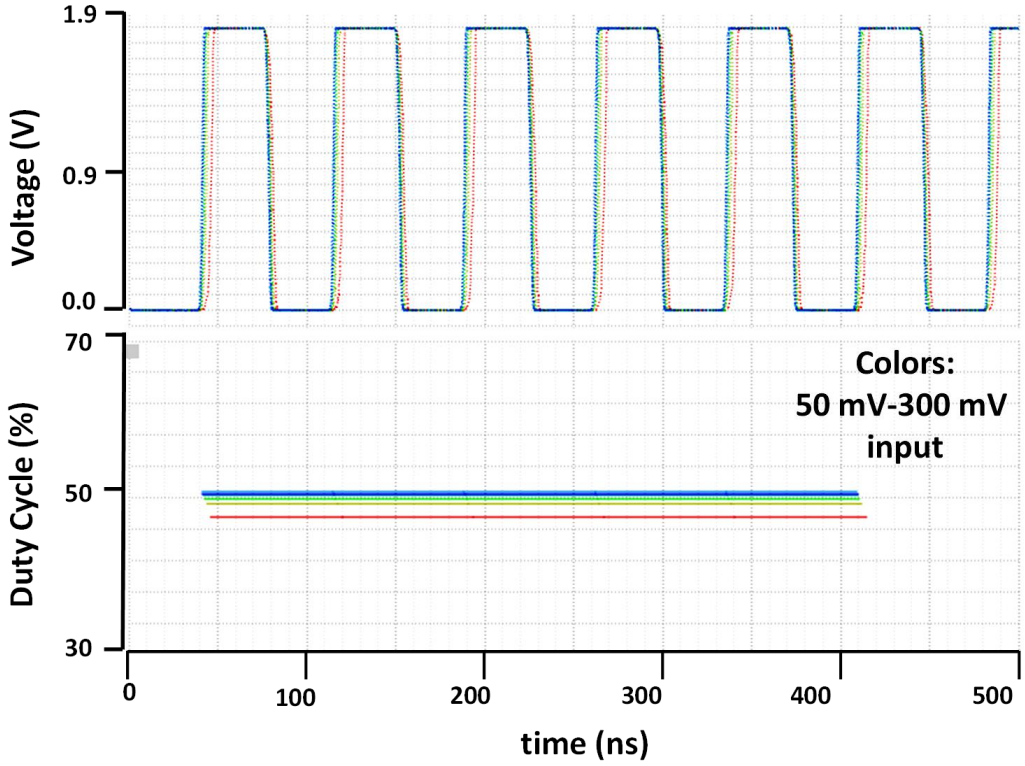


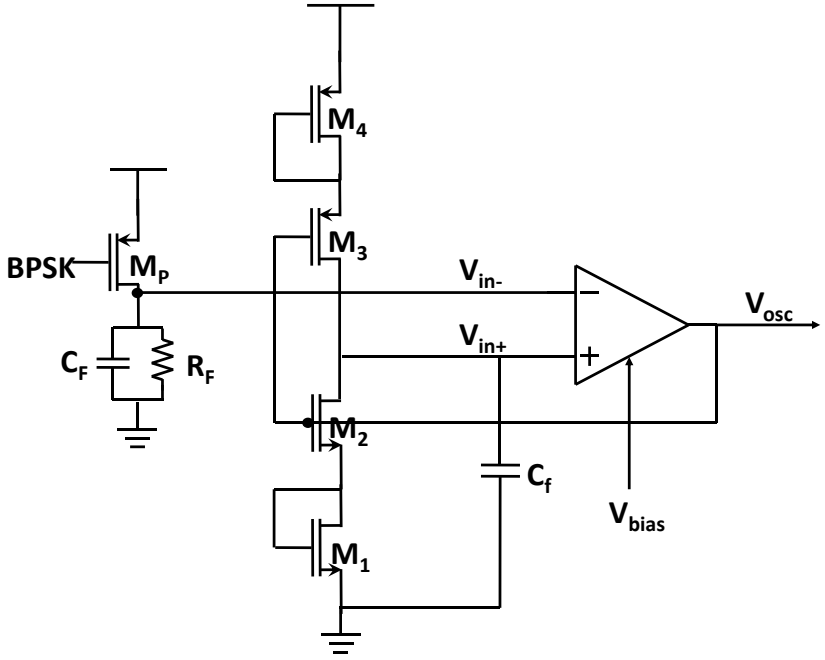
Figure 3.16. Digitized waveforms for varying coupling conditions with input 50 mV to 300 mV and their duty cycles

It is seen that for different coupling levels (input voltage levels), digitizer output duty cycles are nearly the same around 50%, which means that digitizer is not affected by coupling level changes, in the range we are interested in.

3.3.2 Relaxation Oscillator

In order to use a clock reference for detection of the digitized signal, clock generation is necessary, created clock should have a delay that is less than half period of the carrier period to detect without glitches. Moreover, jitter of the oscillator should be less than half period of the original carrier, too. There are a number of different architectures for oscillator design. Relaxation type oscillator is chosen for its wide controlling possibilities. Frequency and duty cycle of the oscillator can be controlled from outside with bias adjustments easily, also, using

external capacitors, frequency of the clock can be further manipulated. Relaxation oscillator is shown in Figure 3.17.



M_1	1 µm/2.6 µm
M_2	1 µm/1 µm
M_3	2.4 µm/1 µm
M_4	2.4 µm/1 µm
M_5	0.7 µm/20 µm
C_F	10.8 pF
R_F	1.25 MΩ
C_f	Variable

Figure 3.17. Relaxation oscillator schematics

M_1 and M_4 transistors are used to adjust the voltage level on the V_{in+} input of the comparator and also charging and discharging currents. Transistors M_2 and M_3 behave as an inverter, which's input is driven by the comparator output. Capacitor decides the charging and discharging time, directly affecting the oscillating frequency. V_{in-} input of the comparator is given from outside, deciding the duty cycle of oscillating output.

With V_{osc} voltage is at V_{DD}, comparator V_{in+} input voltage decreases according to the current passing on the capacitor to discharge it and also to the capacitance. When V_{in+} input becomes smaller than V_{in-} input voltage, V_{osc} becomes 0 V. This time capacitor starts charging until the point V_{in+} input becomes larger than V_{in-} input voltage. Then V_{osc} voltage becomes V_{DD} again and oscillation continues with the same mechanism.

Input V_{in-} is driven by the digitized BPSK modulated waveform, by converting it into a DC signal using a passive 1st order low pass filter. This way oscillator always starts under same conditions, meaning that delays are always the same for different usages. Waveforms of the relaxation oscillator is shown in Figure 3.18.

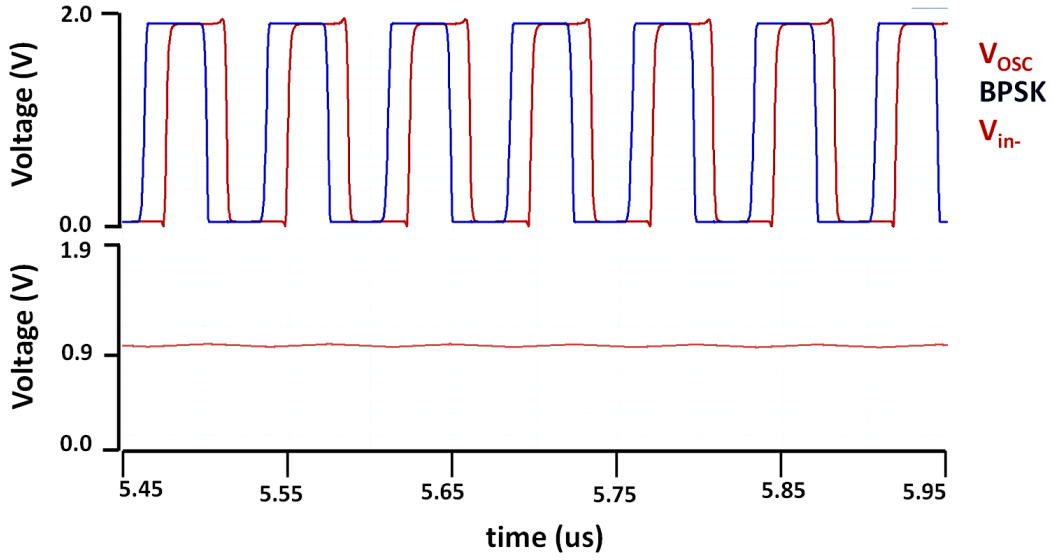


Figure 3.18. Relaxation oscillator waveforms and low pass filter output

As mentioned, initial delay and phase jitter are the two most important parameters of the relaxation oscillator. Jitter and delay time ranges are shown in Table 3.2, which satisfy the requirement of being less than a half period 36.87 ns with 11.6 mW power.

Table 3.2 Phase jitter, initial phase, and total max / min delays of the oscillated waveform

Type of Travel	*Max*	*Average*	*Min*
Phase Jitter	2.2° / 0.45 ns	2° / 0.4 ns	1.9° / 0.38 ns
Initial Phase	+12.6 ns	+12.3 ns	+11.9 ns
Total	13.05 ns		11.52 ns

3.3.3 Data Recovery

After getting the raw clock to detect the data transferred, data recovery becomes a trivial operation. The digitized BPSK modulated waveform is detected using the raw clock generated with a D-Flip Flop. Since initial delay of the clock is a non-zero value that is also smaller than half period of the BPSK carrier, detection can be performed. D-Flip Flop schematics are given in Figure 3.19. Detection of the data using D-Flip Flop can be seen in Figure 3.20.

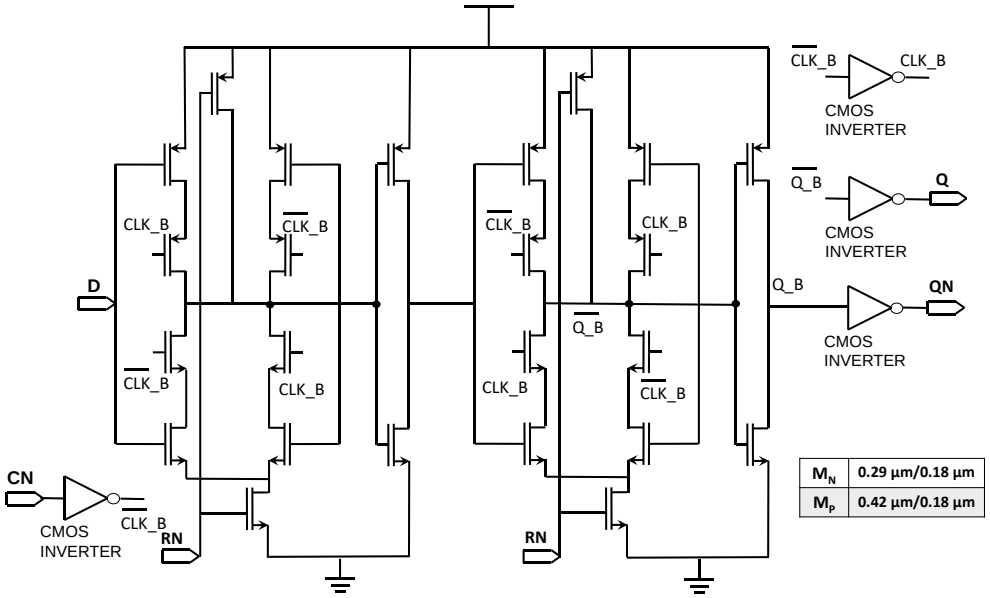


Figure 3.19. Master-slave D-Flip Flop schematics

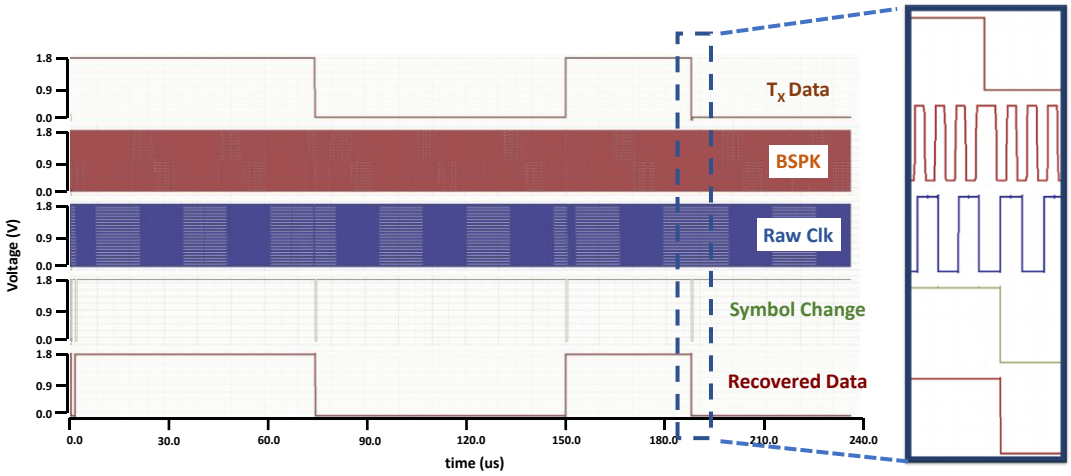


Figure 3.20. Data recovery using D-Flip Flop

3.3.4 Clock Recovery

Clock recovery concept here is not a generic clock recovery process and will not be mentioned in detail. Basically, in order to process the data transferred with correct timing, data rate should also be extracted at the receiver end. For this purpose, a frequency divider is used to convert the raw clock generated by the relaxation oscillator.

3.3.5 Simulation Results

The semi-coherent demodulator circuit proposed is designed in 180 nm high voltage TSMC(Taiwan Semiconductor Manifacturing Company) process on the EDA software CADENCE and simulations performed with SPECTRE simulation tool.

Data and clock/carrier information is expected to be extracted from the modulated waveform using the demodulator. Besides operational success, demodulator should be able work at coupling coefficients in the range of 0.05-0.30.

To test this, modulated waveforms are given as an input to the demodulator with varying amplitudes representing different coupling levels. The idea is that in a linear range, demodulator should be able recover data minimal error rate while the modulator can sustain these voltage levels so that coupling range can be considered valid for application. For 0.05 coupling coefficient, 50 mV amplitude is used. According to this, 0.30 coupling coefficient corresponds to 300 mV amplitude input level. Digitizer and overall and current consumptions for this range are shown in Figure 3.21.

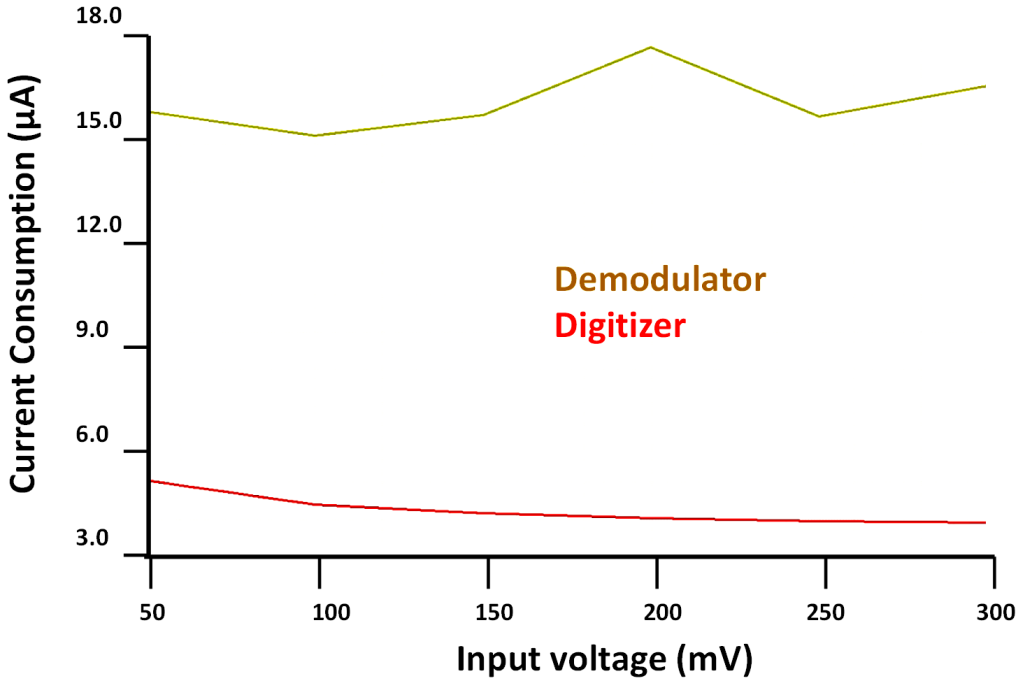


Figure 3.21. Current consumptions of the digitizer and the demodulator

For raw clock generation, phase jitter and initial delay amount are needed to be seen. Phase jitter must be less than 90° for proper detection. Also initial delay must be less than 36.87 ns. For varying couplings, these values are given in Table 3.3.

Table 3.3 Max phase jitter and initial delay minimum and maximum values for coupling coefficient values

Coupling Coefficient (for 1 V T_X)	*Phase Jitter Max magnitude*	*Initial delay Min / Max value (ns)*
0.05	2.22°	12.11 / 12.60
0.10	2.16°	12.04 / 12.46
0.15	2.04°	11.98 / 12.24
0.20	1.96°	11.90 / 12.05
0.25	2.08°	12.01 / 12.33
0.30	2.15°	12.07 / 12.42

For the data recovery operation, long data sequences are used to find error rates, as first symbol is destined to be lost, for all coupling levels, there is a non-zero error rate. Jitter variations affect BER directly, combined with the in built BER of BPSK, BER and coupling relation is given in Figure 3.22.

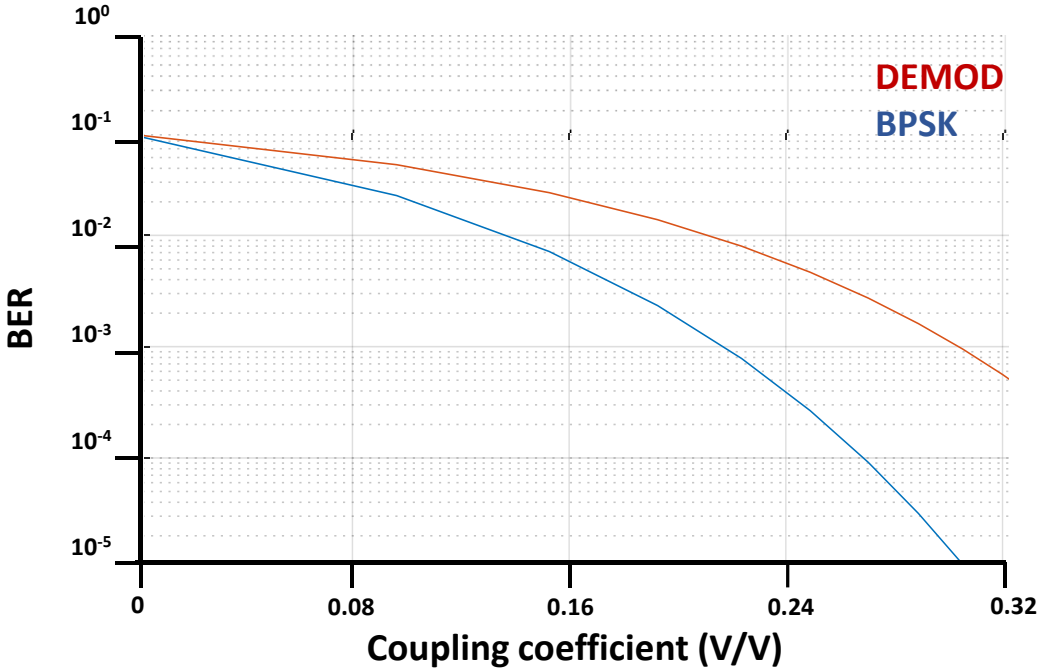


Figure 3.22. Demodulator and coherent BPSK BER vs coupling coefficients

3.4 Patient Fitting

One of the main applications of the wireless data transfer system for the cochlear implant is the patient fitting operation. Patient fitting operation is used to adjust the stimulation current levels for each channel after surgery to increase the comfort level of the patient with the implant. In Figure 3.23, stimulation current generator used in FLAMENCO project is shown. Basically, it is a current generator with an in-built Digital-to-Analog Converter (DAC). For each channel, 7-bit adjustment information is needed to be extracted from the transferred data. This operation is presented to show the operation of data and clock recovery with an example.

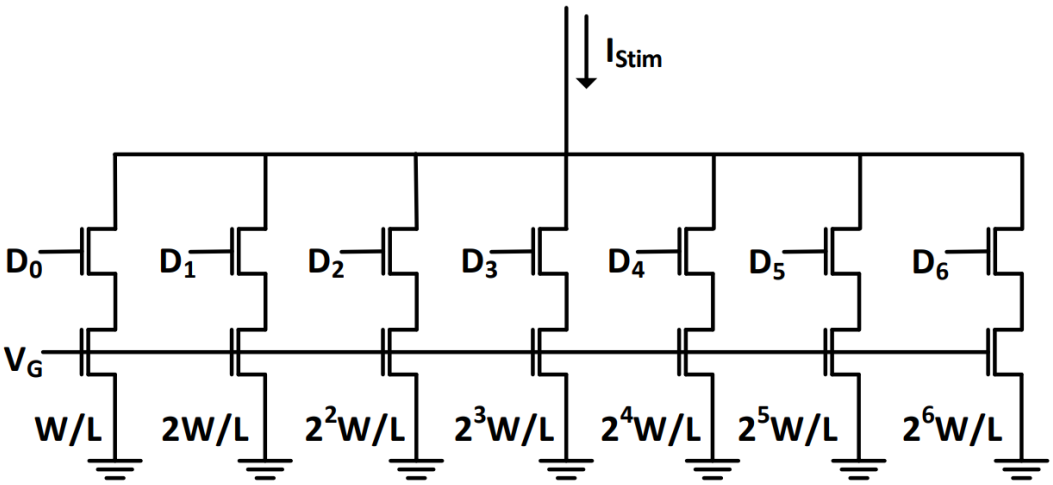


Figure 3.23. Stimulation current generator schematic for patient fitting [66].

At first, from the serial data, channel information in extracted. This channel information is a 3-bit sequence. Data that is wanted to be placed inside that channel with the current generator is also extracted. Then with a distributer consisting of demultiplexers, bits are distributed to the relevant spots. Finally using SR latches, placed bits are preserved until a new stream of 7-bit 8 channel information is wanted to be placed. The overall diagram of the fitting system is shown in Figure 3.24.

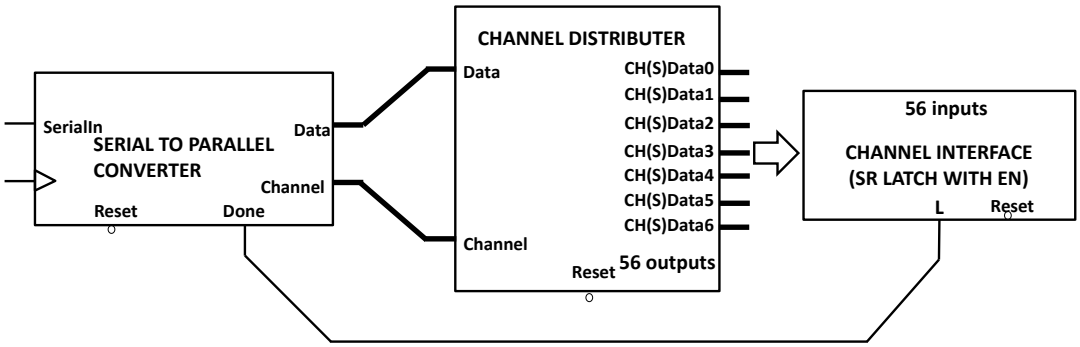


Figure 3.24. Patient fitting processor overall diagram

First block is the serial to parallel converter block (Figure 3.25). This block does not only convert the serial data stream into parallel bits but also extracts 10 bit information of channel information and channel data.

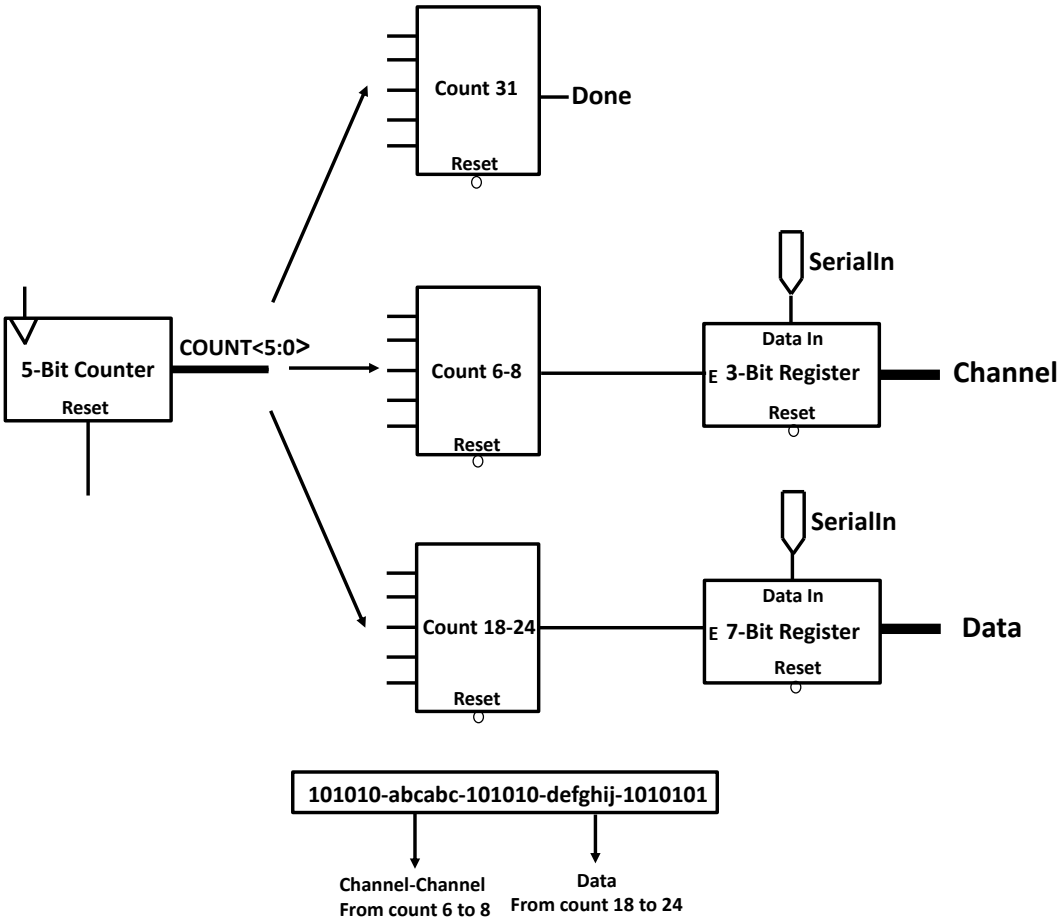


Figure 3.25. Recovered serial data input to parallel data extractor diagram

Each pocket, which are responsible for a single channel adjustment has 32 bits. Using 3 counters, pocket end, channel information and channel data spots are detected. When they are detected, bits related to those spots are written into registers. Registers are designed using the same D-Flip Flop designed in the demodulator.

Then, by using 7 1-to-8 demultiplexers (Figure 3.26), channel information and channel data are placed into their relevant 56 spots are stored in SR latch arrays.

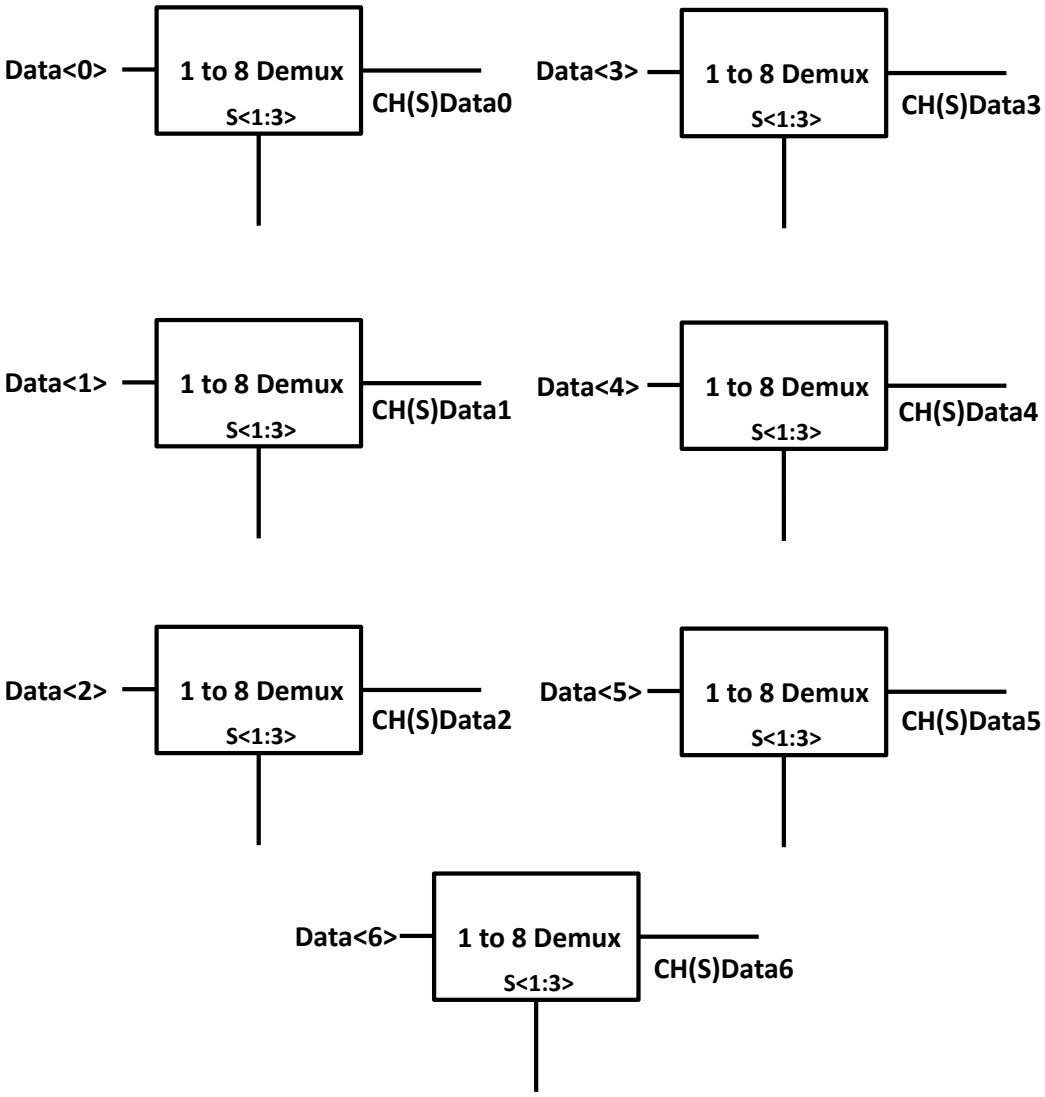


Figure 3.26. Data placer block with demultiplexer (1 to 8)

General operation of the fitting data processor is shown in Figure 3.27. There are 2 pockets transferred in the stream, first pocket is set to be placed on channel 5, with data sequence 0011111, second pocket is set to placed on channel 1, with data sequence 0010001. It can be seen that fitting information is successfully placed into the channels and also previous channel information are kept after operation.

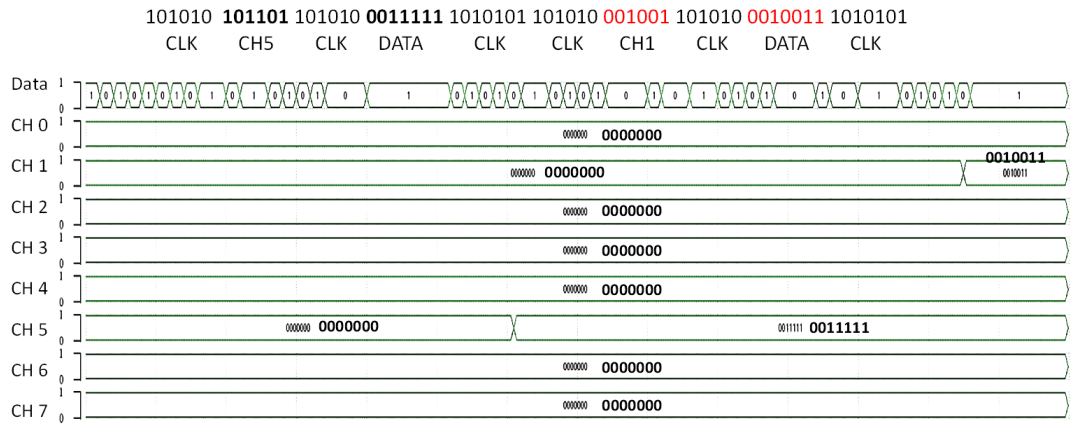


Figure 3.27. Channel adjusting patient fitting simulation results

3.5 Experimental Results

The wireless data transfer system circuit is designed and implemented in 180 nm high voltage TSMC process. Simulation were performed with extracted layout with all possible parasitic effects. In Figure 3.28, fabricated chip micrograph can be seen.

To perform the test, a Printed Circuit Board (PCB) is designed (Figure 3.29). AC signals are isolated and kept short in the design.

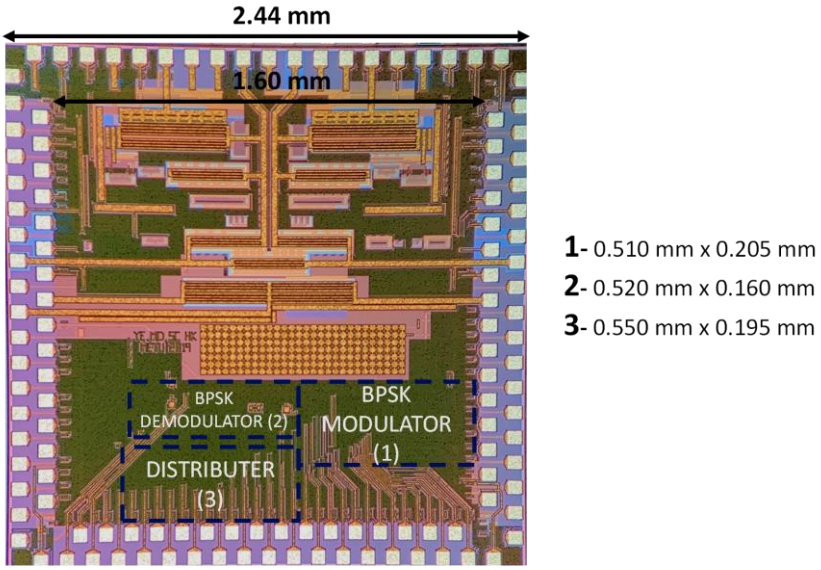


Figure 3.28. Fabricated chip micrograph with 180 nm TSMC process

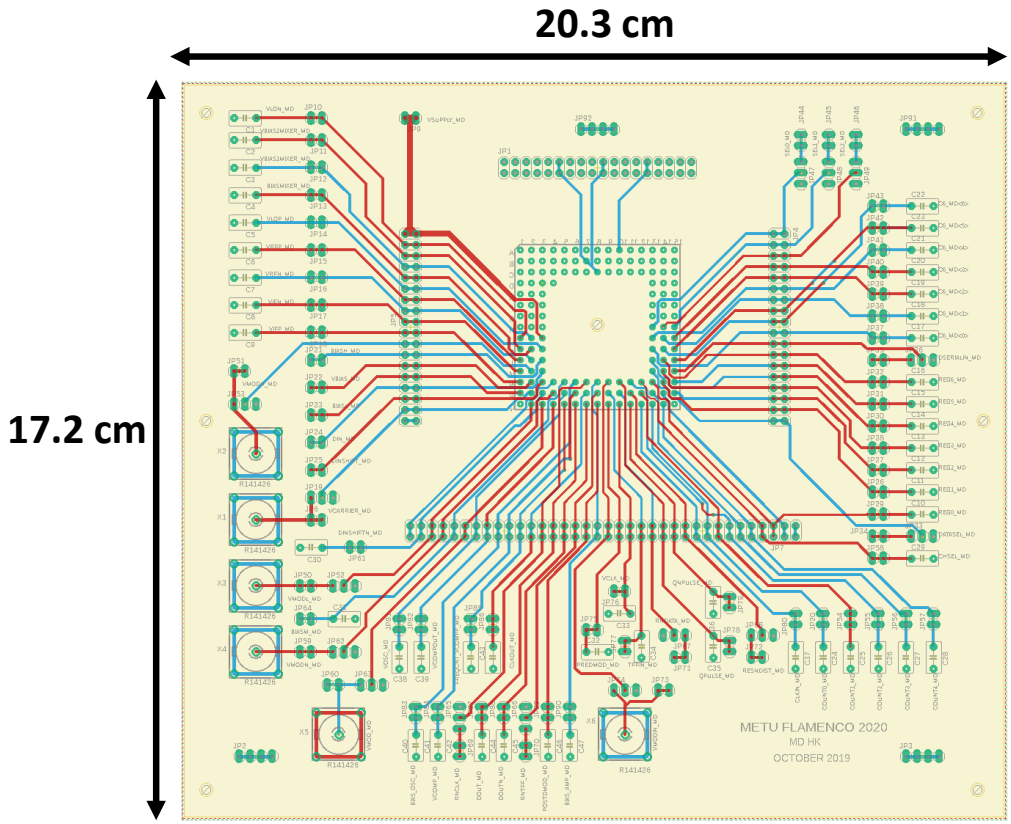


Figure 3.29. Designed printed circuit board experimental results

First block of concern is the BPSK modulator block. Modulator block was designed to operate at 13.56 MHz frequency. In the simulations, there was a phase delay of 5.77 ns during symbol changes. This value is satisfactory for BPSK modulation since phase changes under 45° can be detected with a BPSK demodulator and 5.77 ns corresponds to phase delay of 28.2°.

Modulated BPSK waveform test results are given in Figure 3.30. First observation is that the amplitudes of the modulated waveforms are smaller than the simulation results. This is due to the transistor sizing at the output stage of the modulator. With reduced gain, effective coupling coefficient ranges are changed and scaled with a parameter 6/5, meaning that at coupling coefficient 0.05, demodulator should be able work with 40 mV amplitude corresponding to 0.04 coupling coefficient at previous case.

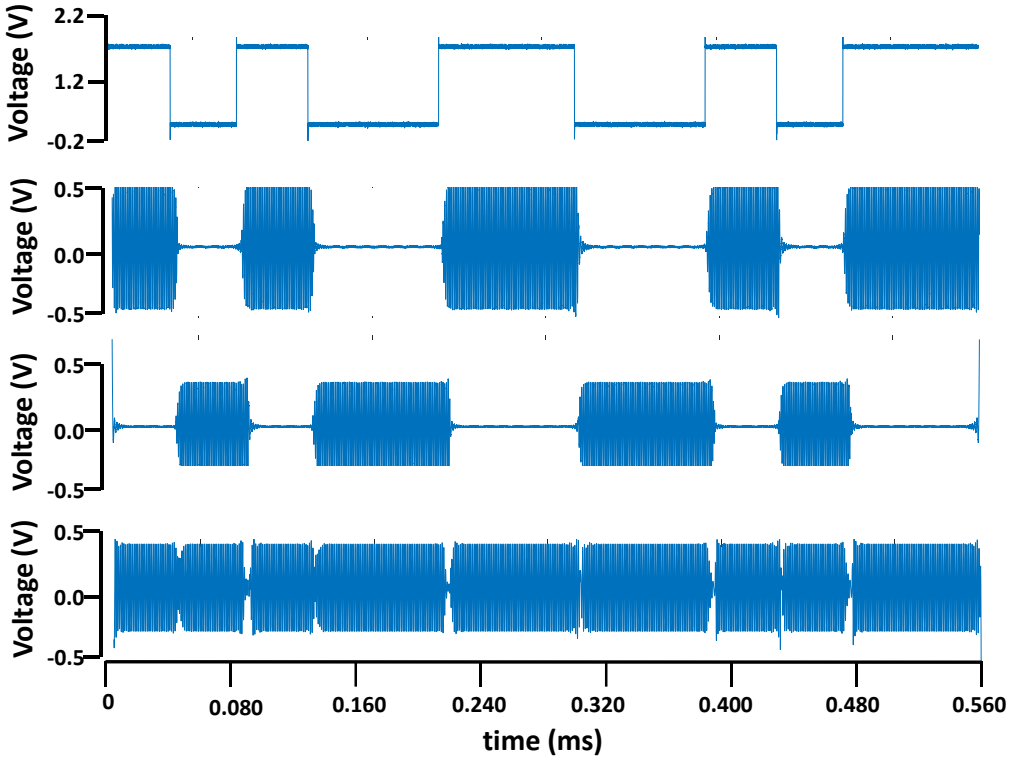


Figure 3.30. Modulator waveforms (a) data input (b) data amplitude modulated filtered waveform (c) inverse amplitude modulated filtered waveform (d) BPSK modulated output

Another observation is that the delays in between symbols vary in between different intervals. In bit value 0 to bit value 1 transition, delays are larger than the other case. Data input to carrier input leakages are higher than simulation results as switch sizes are small. Still this symbol change delay is less than 45°, with 31.7° - 6.49 ns. On average symbol delay is 6.14 ns with 1-to-0 delay being 5.80 ns, in compliance with the simulation results. For demodulator tests, two methods are used, at first the expected modulator output is given as the input to the demodulator to verify operation. Then, modulator and demodulator pair are used together. Data recovery and extraction for fitting application test results are given in Figure 3.31.

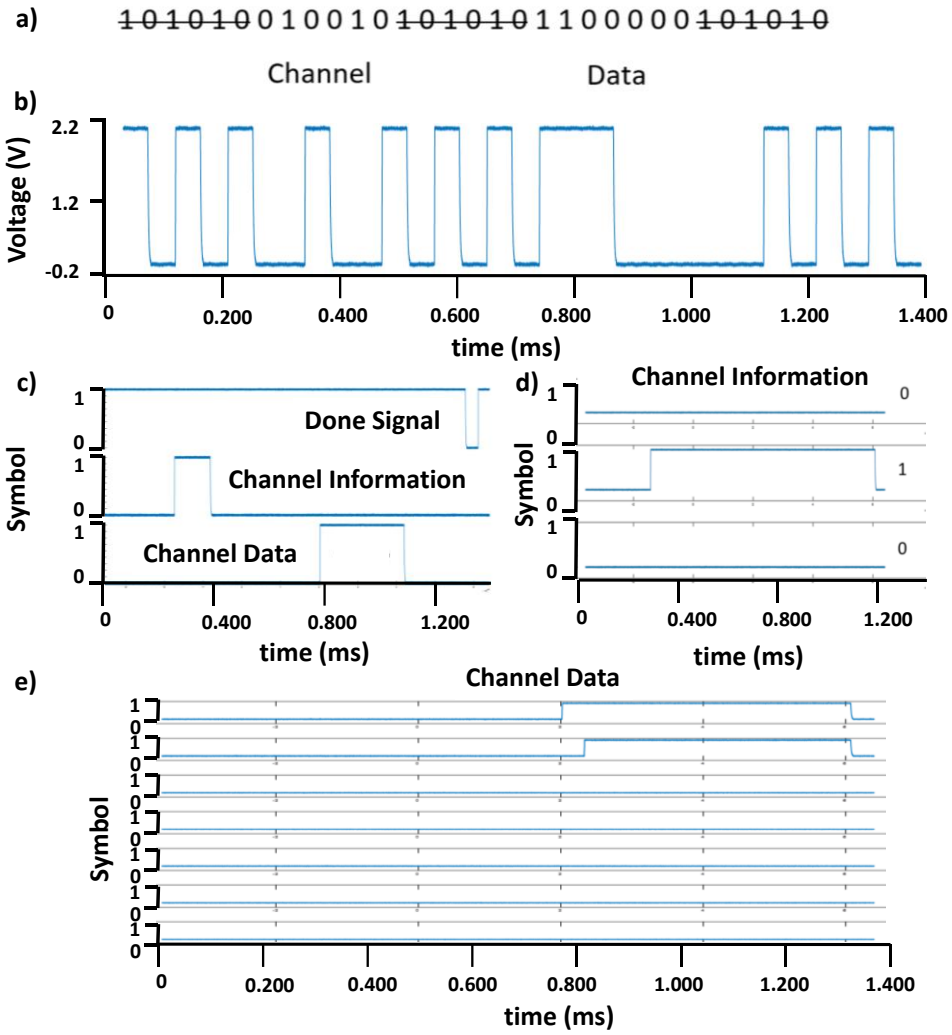


Figure 3.31. (a) Transmitted data (b) recovered data (c) recovered data to channel information converter output (d) channel information extraction (e) channel data extraction

Performance parameters for the WDT system are given in Table 3.4.

Merit of digitizer efficiency is calculated as in Eq (3.3).

$$Dig.\ Efficiency = \frac{Max\ coupling\ digitizer\ consumption}{Coupling\ digitizer\ consumption} \times 100 \quad Eq(3.3)$$

Moreover, overall efficiency metric is calculated by normalizing BERs with overall power consumption and T_X power.

Table 3.4 Performance table for the WDT system.

Coupling Coeff. (1 V T_x)	*BER*	*Overall Power Consumption*	*Digitizer Efficiency (%)*	*Overall Efficiency (%)*
0.05	2.8×10^{-2}	26.82 µW	77.6	0.40
0.10	1.0×10^{-2}	25.65 µW	88.9	1.15
0.15	7.1×10^{-3}	26.64 µW	94.0	1.57
0.20	1.2×10^{-3}	29.70 µW	96.8	8.33
0.25	3.0×10^{-4}	26.55 µW	98.7	37.30
0.30	1.0×10^{-5}	28.46 µW	100.0	100.00

3.6 Discussion

In this chapter, a wireless data transfer system consisting of a BPSK modulator, a semi-coherent BPSK demodulator and a patient fitting processor are presented. Circuits are designed and implemented in 180 nm TSMC process. The problem addressed into was to design a wireless data transmission system that can operate with coupling coefficient as low as 0.05 and up to 0.30.

For this purpose, a BPSK modulator was designed and fabricated. The modulator utilized amplitude modulation for data and its inverse. It was expected that with this approach, bandwidth efficiency would be lower than the generic coherent BPSK case since abrupt voltage changes occur at symbol changing points. The phase delay of symbols were 28.2° in simulation results and 31.7° in the experimental results. While being satisfactory for detection of the BPSK, these results reflect as lower effective coupling coefficient at the receiver side and therefore should be improved in the next design to achive lower BER. To do this, each phases should be isolated from one other and digital switches should also be bigger in size in the improved design.

Demodulator was a semi-coherent BPSK demodulator. Semi-coherency comes from the idea that the oscillator block in the demodulator starts its operation when there is a signal present at the receiver side so that delays are the same at all times. To do this, range of comparison voltage on the relaxation oscillator was limited using additional stack transistors. As targeted, demodulator block was able to operate with voltages as low as 50 mV input level, corresponding to 0.05 coupling coefficient with 1 V transmitter voltage amplitude. BER for this input level is measured as 2.8×10^{-2}, being close to in-built BER of BPSK. In order to not disturb operation at larger couplings and to have the same digitalized BPSK waveforms, a digitizer with large gain and constant $V_{DD}/2$ output DC offset voltage was used. The demodulator design with this approach still includes an oscillator block, which has random jitter at all times. The delay amount of the raw clock signal limits the bandwidth constantly and this delay is necessary for detection. Therefore, such a design always increases BER of the tranmission and hence a fully digital, oscillator free, non-coherent design could achieve better BERs.

At last, recovered data and clock have been used for a patient fitting application into 8 channels with 7-bit control setup. From the data pockets, necessary 10 bit information for channel information and channel data were extracted and placed into the spots in a current stimulator setup. Overall, BER for lower coupling coefficient levels can be further improved with a less delay dependent and non-coherent design.

CHAPTER 4

NON-COHERENT BPSK WIRELESS DATA TRANSFER SYSTEM

4.1 Motivation

Semi-coherent BPSK data transfer system offers many advantages compared to coherent demodulation systems. In coherent systems, adding to the complexity of the system, control resolution of the voltage controlled oscillator has to be high, combined with the constantly operating phase and delay detection and adjustment mechanisms in the locked loop circuits cause large power consumptions.

The modulator with two branch amplitude modulation offers simplicity and high output power, however, non-continuous phase shifting operation and differential driving of the coil causes unefficient bandwidth usage. This is mainly caused by the delays during bit changes, delay changes not only affect spectral efficiency by consuming available bandwidth, but they also decide the minimum coupling coefficent value that demodulator can operate.

In this chapter, an improved modulator and demodulator complex is presented. The demodulator circuit is a novel, fully digital and non-coherent BPSK demodulation circuit, that occupies minimal area. Added to 13.56 MHz carrier frequency operation, demodulator can also operate with 6.78 MHz carrier frequency, which allows another bandwidth that is reserved for medical applications to be available for use. In the modulator, instead of using the same carrier signals for data and inverse of the data, ac-wise inverse of the carrier signal is generated with an additional block. Then data and its inverse are modulated using two carriers and instead of subtraction, addition operation is performed. Therefore, delays are minimized on the modulated waveform.

Section 2 of this chapter explains the revised modulator and demodulator circuitries, with simulation results. In section 3, experimental results are presented with previous design comparison. Lastly, in Section 4, modulator and demodulator pair is discussed.

4.2 Non-Coherent Data Transfer Circuit

Non-coherent detection methods for BPSK utilizes 180° phase shift and orthogonality during detection. This detection is, however, performed in analog domain with mixers, which consume large power, and "to limit bandwidth" in analog domain, decrease power efficiency with filters. In this section, a modulator and demodulator pair with fully digital non-coherent operation is explained, mimicking Differential Phase Shift Keying detection, exploiting digital Exclusive-OR (XOR) gates as digital mixers.

4.2.1 Modulator

The first version of the modulator that has been explained in the previous chapter there were delays up to 6.49 ns in between the data high and data low encoded carriers. Adjusting biasing voltage, without voltage regulators caused varying delays in between, which lowers demodulator performance, resulting in faults at low coupling coefficients under 0.15. To eliminate these defects, switching operation is conducted using a constant bias and delay adjusted digital inverters and buffers in the second design. These buffers and inverters have equal propagation delays, combined with the phase shifted carrier creation, result in less delays and current spikes during data/phase change. General structure of using two amplitude modulated waveforms remains the same in the design.

4.2.1.1 Inverse Carrier Generator

The first sub-block of the modulator is the inverse current/voltage generator. This block subtracts the main carrier AC current from a base DC bias current. This creates an AC signal with 180 degrees phase shift. Generating an inverse carrier signal brings an advantage that instead of creating the BPSK modulated data with subtraction of two amplitude modulated waveforms with the same carrier, addition of these modulated waveforms can be utilized, meaning that driving the transmitter coil becomes option without using real inductors. The generator block is shown in Figure 4.1.

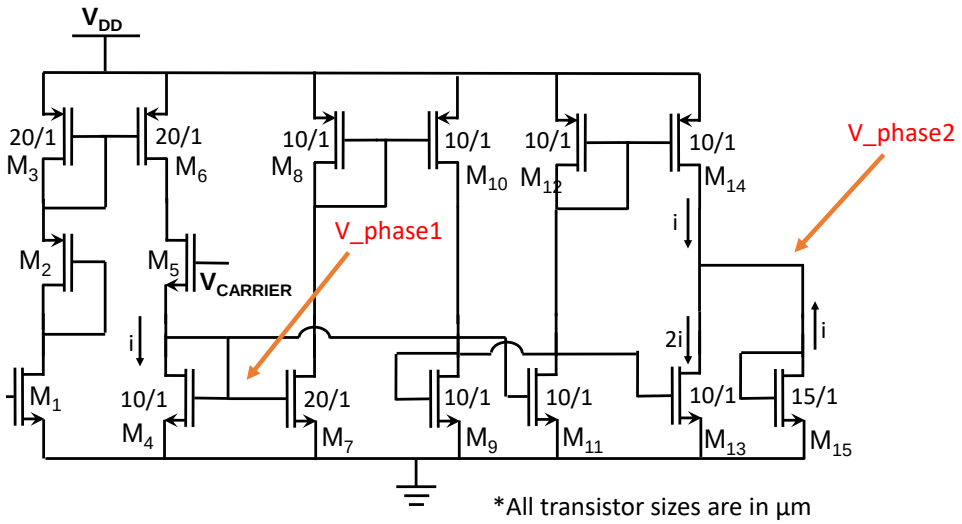


Figure 4.1. Inverse carrier generator block

Transistor M_1 creates a constant current with the bias voltage, which is copied to M_6. Assuming that transistors M_5 and M_6 are at saturation, a constant DC current flows through these transistors. Since gate of the transistor M_5 is connected to the carrier signal, an AC signal is generated at the source of it, with constant DC current passing through. Therefore, Vbias, current i and carrier signal is copied to transistor M_4. This current is than copied to transistor M_7 with 1:2 ratio. Finally, copied current is subtracted from the initially generated AC current, resulting in a signal waveform of inverse of the carrier signal. Generated currents are shown in Figure 4.2. Transistors M_5 and M_6 are also confirmed to be at saturation.

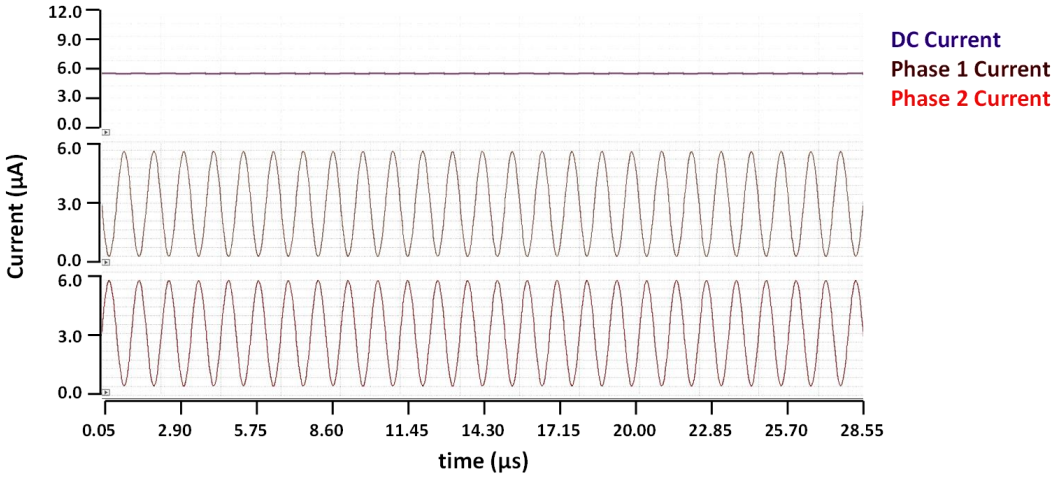


Figure 4.2. Waveforms of the Negative current generator block.

4.2.1.2 Phase Modulator

Phase modulator block is basically, two common source amplifiers with switch controls, that modulate data and inverse of it. In Figure 4.3, phase modulator is depicted with a block diagram.

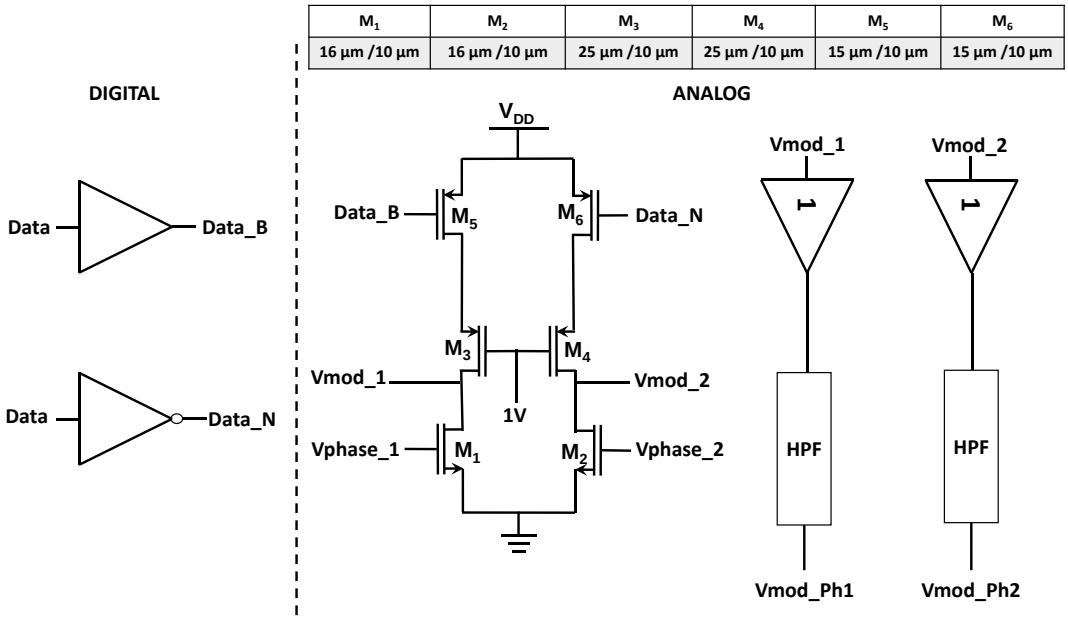


Figure 4.3. Phase modulator block diagram with amplifier circuit

The digital control voltages Data_B and Data_N are buffered and inverted versions of the data input. In order to have equal propagation delays, additional capacitances are added. Control voltage waveforms are shown in Figure 4.4. Main modulator block is connected to the coils with analog voltage buffers and high pass filters. Buffer block schematic is shown in Figure 4.5.

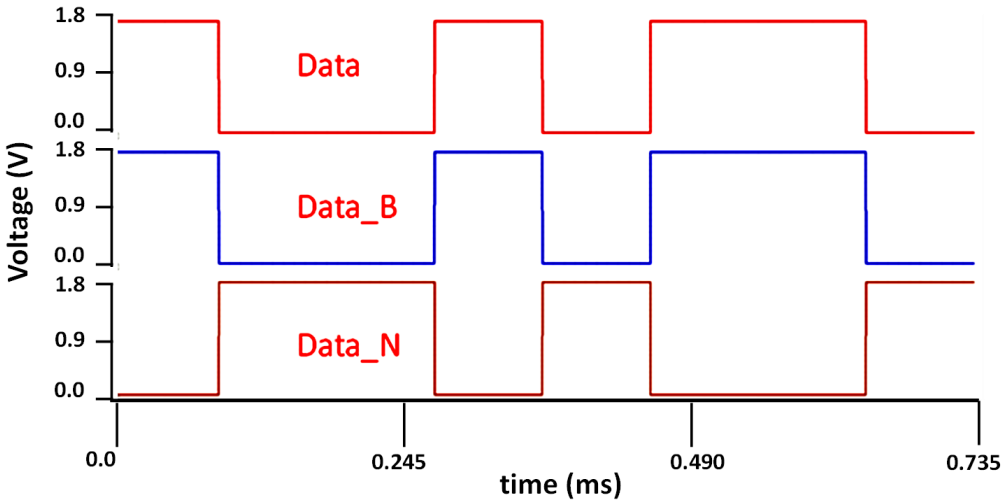
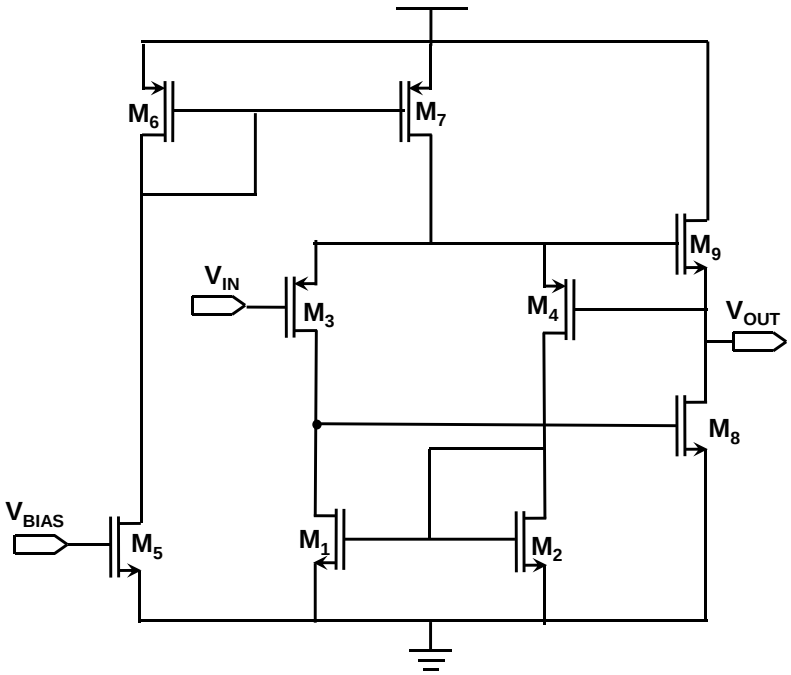


Figure 4.4. Data, buffered and inverted control voltage waveforms



M_1	8 µm/1 µm
M_2	8 µm/1 µm
M_3	8 µm/1 µm
M_4	8 µm/1 µm
M_5	8 µm/1 µm
M_6	8 µm/1 µm
M_7	40 µm/1 µm
M_8	40 µm/1 µm
M_9	24 µm/1 µm

Figure 4.5. Voltage buffer schematics

Main advantage of this modulator design is the symmetrical operation and lower phase delays. Since coils are not directly connected to the high pass filters which are driven by the modulator block, loading effects are minimal. This also reduces power consumption of the modulator. However, in order to drive the transmitter coil, additional power amplifying structure becomes necessary. High pass filters are the same high pass filters used in the previous BPSK modulator design and 1st order passive filters are used.

4.2.1.3 Simulation Results

The improved modulator circuit proposed is designed in 180 nm high voltage TSMC (Taiwan Semiconductor Manufacturing Company) process on the EDA software CADENCE and simulations performed with SPECTRE simulation tool.

The aims are to get lower delays in between symbol changes and consistent delays, because large delays and inconsistency reflect to the receiver side as additional noises and therefore increase BER for poor coupling coefficients. In Figure 4.6, the output waveforms of the modulator are given. A closer look at near symbol change is given in Figure 4.7. It is seen that symbol change delays are consistent for all transitions and delays are as small as 2.05 ns. This means that demodulator's effective input coupling ranges become larger than it is with the previous modulator.

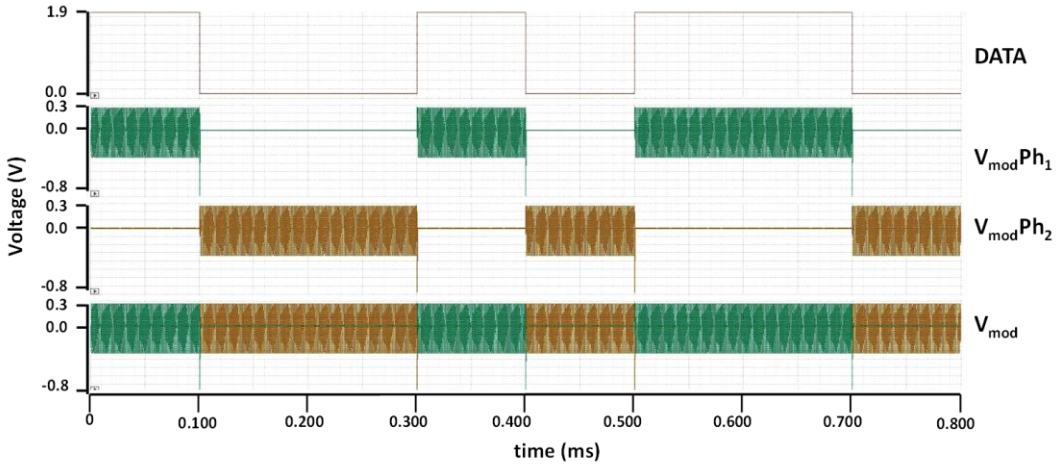


Figure 4.6. Demodulator output waveforms, separate phases, and overall modulated signal

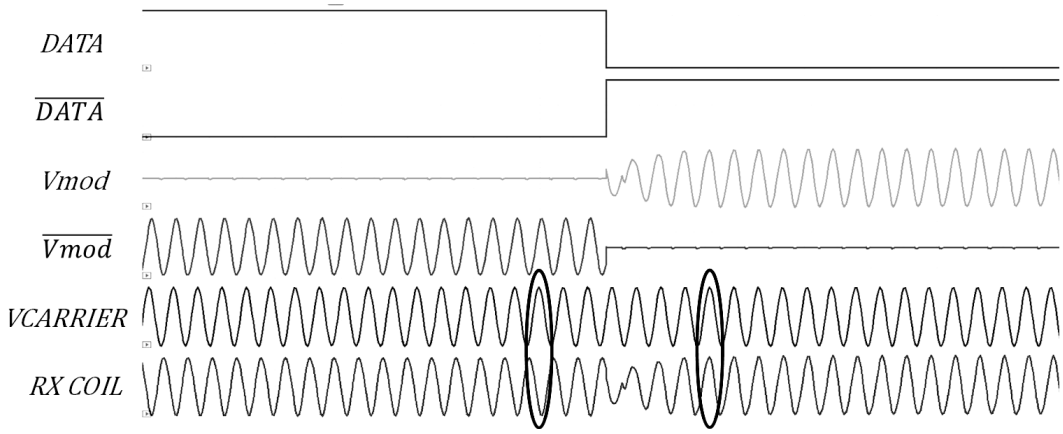


Figure 4.7. Modulator block waveforms with symbol transition close look-up

The specifications of the modulator block are given in Table 4.1 . Compared to the first version, gain is smaller, this means that input voltage level of the demodulator will be smaller for same coupling coefficient values. This is dealt by using an external amplifier for transmission. Power consumption of the second version is significantly lower; however, this is because second version of the modulator do not drive the coils on its own.

The most significant difference is the phase delay, with second modulator having one third of the first modulator. For poor coupling conditions, this means an improvement in BER by a factor of 2 with diminishing returns for increasing coupling coefficient.

Carrier leakage onto data input is also reduced in this design by changing switch sizes and digital control mechanisms. Same also applies for the carrier suppression at the output modulated waveform for each branch. With larger suppression, harmonic distortion at the output is reduced.

Table 4.1 Modulator v1 and v2 comparison

Parameter	*Modulator v1*	*Modulator v2*
$V_{carrier}$ Amplitude	200 mV	100 mV
Data Rate	10 kbps	20 kbps
Gain	19 dB	14.44 dB
Supply Voltage	1.8 V	1.8 V
Power Consumption	224.5 uW	21.6 uW, 50% duty cycle 21.8 uW, 100% duty cycle 21.4 uW, 0% duty cycle
Max Phase Delay	28.2 degrees, 6.02 ns	9.9-10.1 degrees, 2.05 ns
Carrier Suppression	80 dB	87.1 dB
CM Gain	-80 dB	-
Carrier to Data Leakage	-43 dB	-60.2 to -59.3 dB

4.2.2 Digitally Delay Mixed Non-Coherent Demodulator

In Figure 4.8, the block representation of the demodulator is given. As the first stage, the incoming carrier signal is amplified with an amplifier in common gate configuration so that the data can be recognized even at low coupling coefficients. Secondly, the amplified carrier signal is digitized with a digital buffer, allowing digital operation.

At the second stage, the digitized BPSK signal is delayed with a duration of half of a bit period. The delayed and the original digitized signals are digitally mixed with an Exclusive-OR (XOR) gate.

At the final stage, the digitized BPSK signal is reevaluated with the mixed pre-clock signal and the data is recovered. Finally, the clock of the carrier signal is recovered again with digital mixing of the recovered data and the digital BPSK signals.

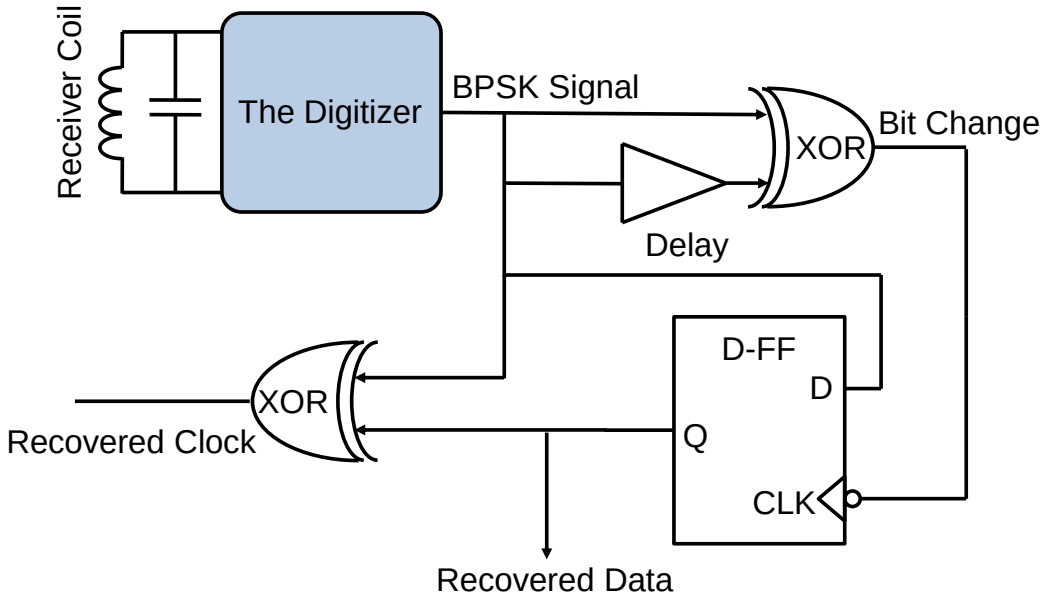
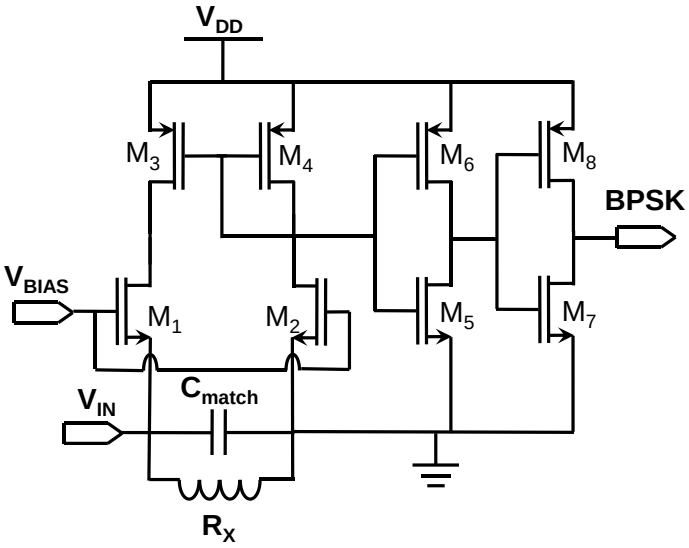


Figure 4.8. Fully digital non coherent demodulator v1

4.2.2.1 1-Bit Digitizer

Similar to the semi-coherent demodulator, incoming waveform is digitized at first. The structure of the digitizer block is the same, however transistor sizing at the digital buffer are changed. In Figure 4.9, schematics can be seen.



M_1	10 µm/1 µm
M_2	10 µm/1 µm
M_3	15 µm/1 µm
M_4	15 µm/1 µm
M_5	6 µm/1 µm
M_6	10 µm/1 µm
M_7	10 µm/1 µm
M_8	16 µm/1 µm

Figure 4.9. 1-Bit Digitizer Block

For different coupling conditions, digitized waveforms are illustrated in Figure 4.10. It can be seen that the DC offset at the output is fixed to $V_{DD}/2$ and digiziter successfully digitizes the received signal even at coupling as low as 0.04.

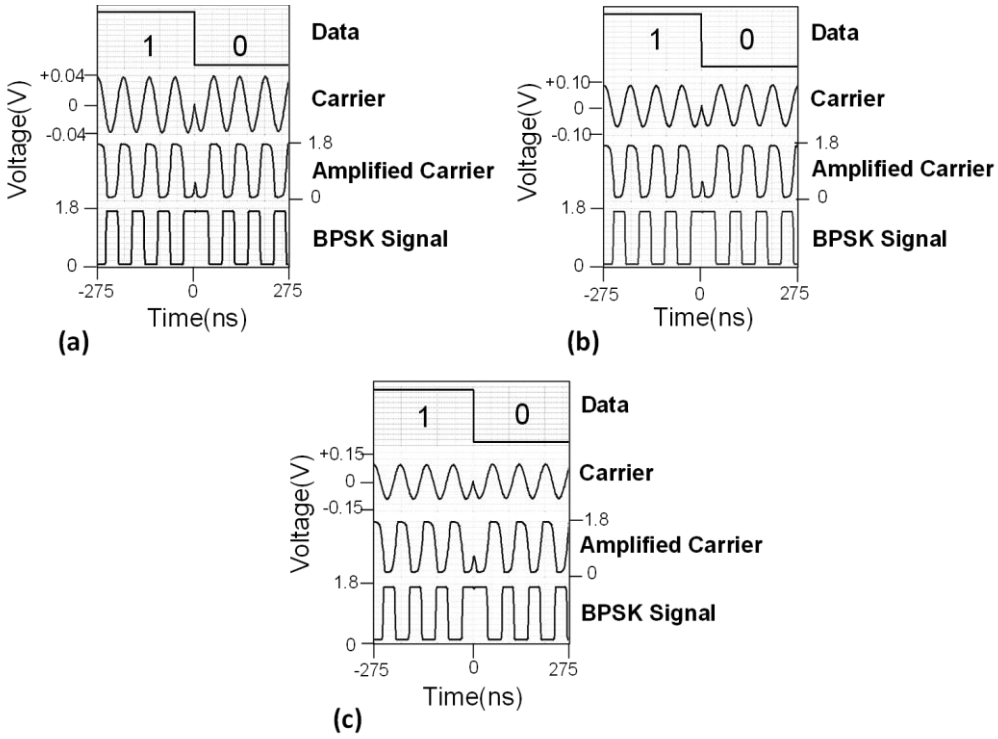


Figure 4.10. Digitized waveforms for (a) k=0.04 (b) k=0.10 (c) k=0.14

4.2.2.2 Delay Buffer and Digital Mixing Circuit

In BPSK, the magnitude and the frequency of the carrier signal remains constant and 0 and 1 bits are encoded with different phases. These two subcarriers whose phases are separated from each other with 180° separation are orthogonal. This means that if the incoming carrier signal is multiplied with itself after a transferred bit duration of time delay, unless the bit value that is transferred changes the output of this multiplication will be nonzero when integrated over one period.

The mixing of two signals can be utilized digitally as well, instead of using mixers. The XOR gate operates very similar to the operation of an analog mixer as illustrated in Figure 4.11. This digital mixing property of the XOR gate is used to detect the phase changes in the digital BPSK signal.

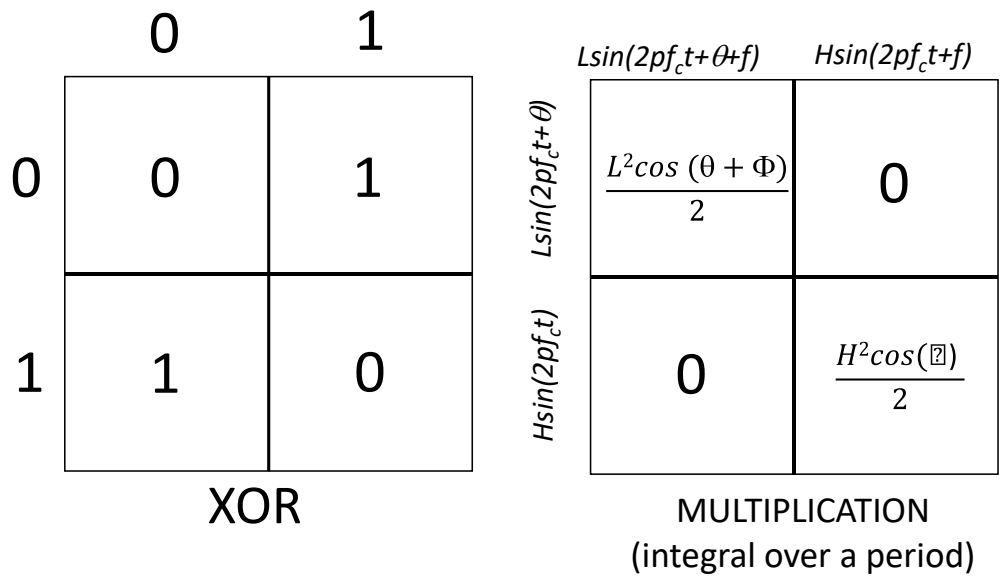


Figure 4.11. XOR operation analogy with analog multiplication

In Eq (4.1) *c* is the carrier signal with frequency f_c before the modulation operation. The signal *d* (Eq(4.2) is the BPSK modulated carrier signal with two complementary data sequences *H* symbolizing high bits and *L* symbolizing low bits.

$$c(t) = sin(2\pi f_c t) \qquad Eq(4.1)$$

$$d(t) = Hsin(2\pi f_c t) + L\,sin(2\pi f_c t + \theta) \qquad Eq(4.2)$$

Once the signal arrives at the receiver side there are some delays caused by transfer path but this delay affects both phases, therefore it may be omitted during calculations. Analog mixing operation is multiplication of the two signals. In non-coherent detection, this is done mixing signal with itself with the delayed version of the signal. Angle Φ corresponds to this delay in Eq(4.3).

$$m(t) = (Hsin(2\pi f_c t) + L\,sin(2\pi f_c t + \theta)) *$$

$$(Hsin(2\pi f_c t + \Phi) + L\,sin(2\pi f_c t + \theta + \Phi) \qquad Eq(4.3)$$

$$sin(x)\,si\,n(y) = 0.5(cos(x + y) - cos(x - y)) \qquad Eq(4.4)$$

Hence

$$m(t) = 0.5(H^2(\cos(4\pi f_c t + \Phi) + \cos(\Phi)) +$$

$$L^2(\cos(4\pi f_c t + \theta + \Phi) + \cos(\theta + \Phi)) \qquad Eq(4.5)$$

Since H and L are complements of each other.

Integrating Eq(4.5) over a period of time leaves the equation with only two terms. If two consecutive bits are different, as θ corresponds to 180°, m(t) becomes zero. For other cases it is nonzero. This operation corresponds to XOR operation when conducted digitally (Figure 4.12). It should also be noted that to smooth the XOR output and clear glitches caused by delay inconsistency, a small capacitor (200 fF) is added to the XOR output. Hence noncoherent demodulation of the BPSK can be conducted with same approach as in the analog case with digital design as well.

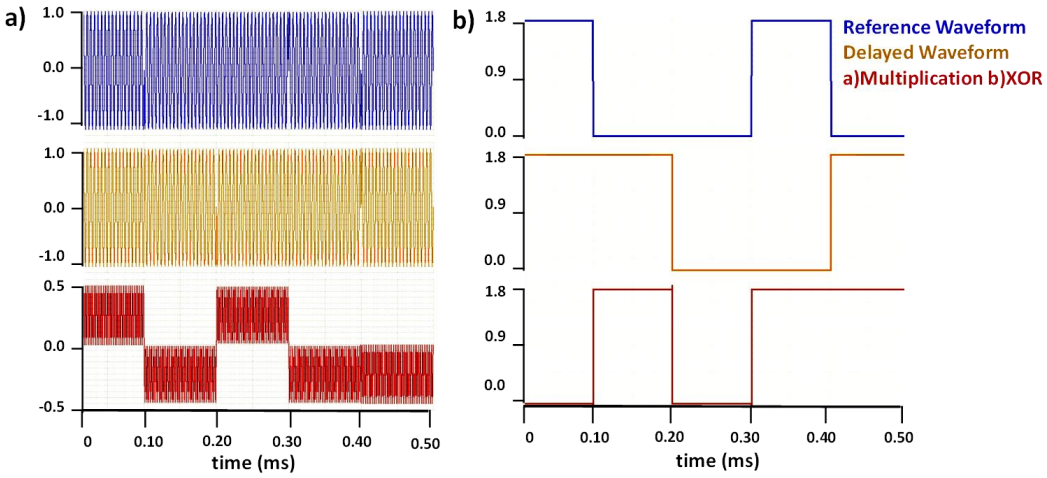


Figure 4.12. (a) multiplication and (b) XOR waveforms

For digital delays, an inverter array is used (Figure 4.13), each inverter adds a delay of 1.5 ns. With 50 inverters, 75 ns delay is achieved corresponding to 1 bit duration/ carrier period.

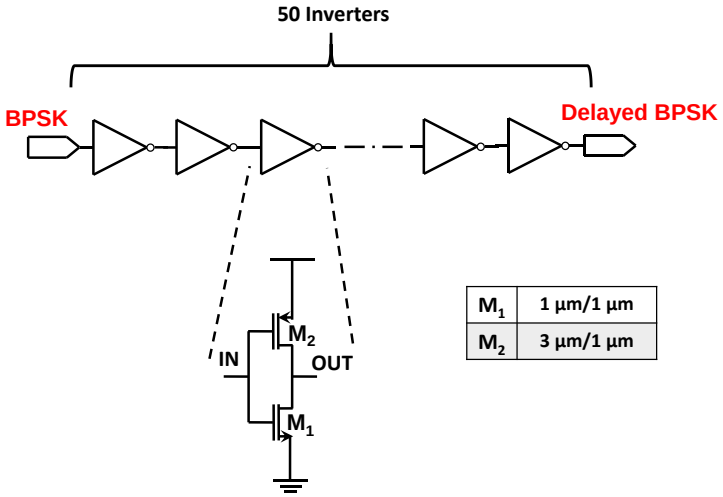


Figure 4.13. Delay inverter array circuit

4.2.2.3 Data Recovery

Once decided whether the two consecutive bits are the same or not, it is not necessary to check the BPSK at each period. When the digitally mixed signal transitions from high to low, it means that there happens a change in the received

data so in order to recover the data, the digitally mixed signal is used as the clock signal whilst reading the digital BPSK at the high to low transition points with a D Flip-Flop. D-Flip-Flop is the same master-slave configurated type used in semi-coherent demodulator and works with negative edge triggering (Figure 3.19).

4.2.2.4 Clock Recovery

Similar to the pseudo clock generation before in digital mixing, to recover the clock, recovered data and the BPSK signals are mixed with an XOR gate.

When the data transmitted remains the same, the BPSK acts as the clock signal itself. This means that the BPSK is accepted as the clock when data remains the same. At the point the data bit changes, this time BPSK signal remains the same as before either high or low. During low to high transition, it remains high. As both the data and the BPSK signals are high, the generated clock signal transitions from high to low. During high to low transition, the BPSK signal remains low. Hence the clock changes from high to low again, preserving the periodicity of the clock signal, converting BPSK to the original carrier.

4.2.2.5 Simulation Results

The demodulator circuit proposed is designed in 180 nm high voltage TSMC (Taiwan Semiconductor Manifacturing Company) process on the EDA software CADENCE and simulations performed with SPECTRE simulation tool.

The extracted simulation results for the typical NMOS, typical PMOS (TT) cases are illustrated in Figure 4.17. The carrier signal frequency is chosen as 13.56 MHz. The max bit rate is 13.56 Mbps, meaning that data-rate-to-carrier-frequency (DRCF) ratio is 100%. The demodulator consumes 32.3 μW power in average for coupling variations with 1.8 V supply. Larger power consumption is caused by the inverter array consuming more than half of the overall power consumption.

Inverter array simulation results are shown in Figure 4.14.

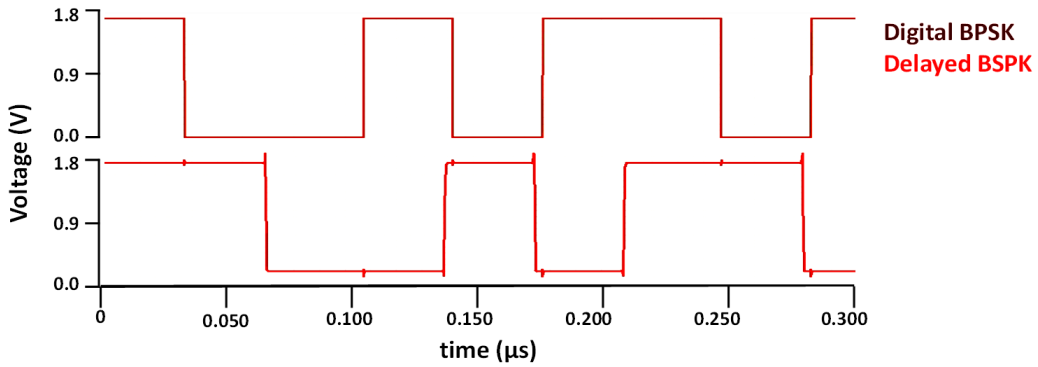


Figure 4.14. Digital and delayed BPSK simulation results

Digital mixing operation is conducted by using an XOR gate by mixing the BPSK waveform with its shifted version. Waveforms given in Figure 4.15 are acquired. In these waveforms it can be seen that whenever symbol changes digitally mixed signal gives a low output detecting the change.

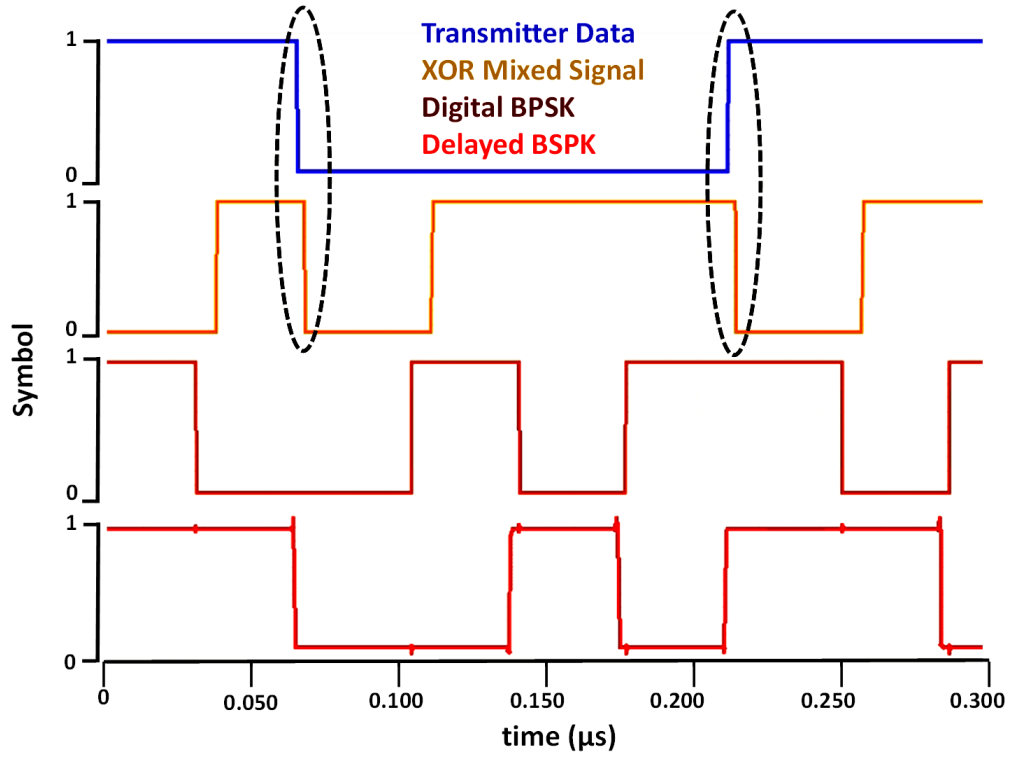


Figure 4.15. Digital mixing operation results

As explained in the digital mixing operation, XOR gate gives a low voltage output when symbol changes. For data recovery, this is utilized by using a negative edge triggered D-Flip Flop. With recovered data, clock is recovered as well, as shown in Figure 4.16.

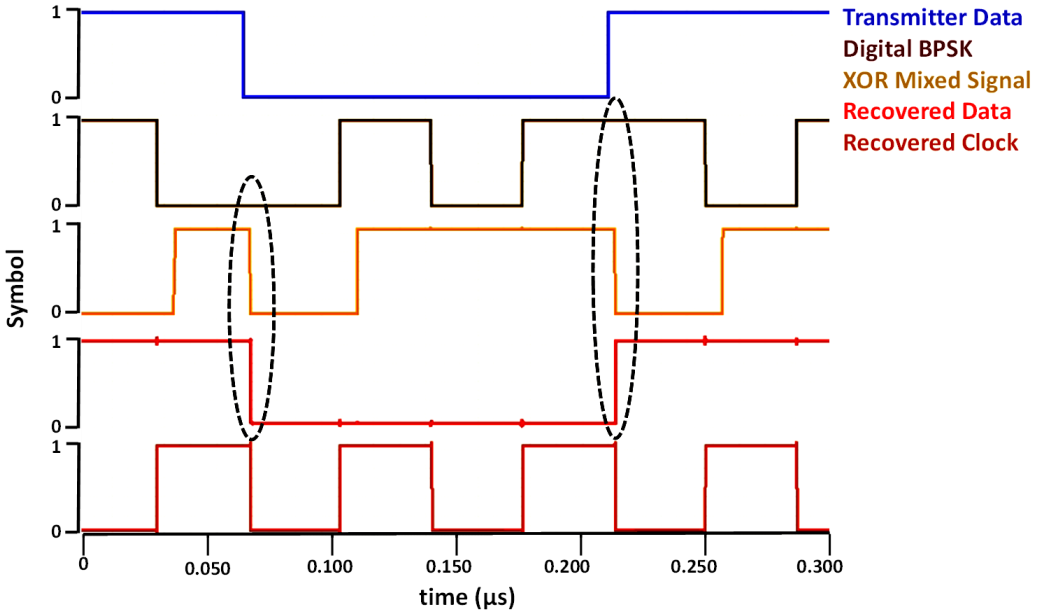


Figure 4.16. Data and clock recovery using digitally mixed signal

As a summary, for the data sequence, overall simulation results are illustrated in Figure 4.17. With the digital mixing concept, main advantage of the demodulator is that it can utilize the entire bandwidth with lower BER. However, while used with the BPSK modulator, data-rate-to-carrier-frequency ratio drops to 50% since a full period of the carrier is needed for modulated signal settling.

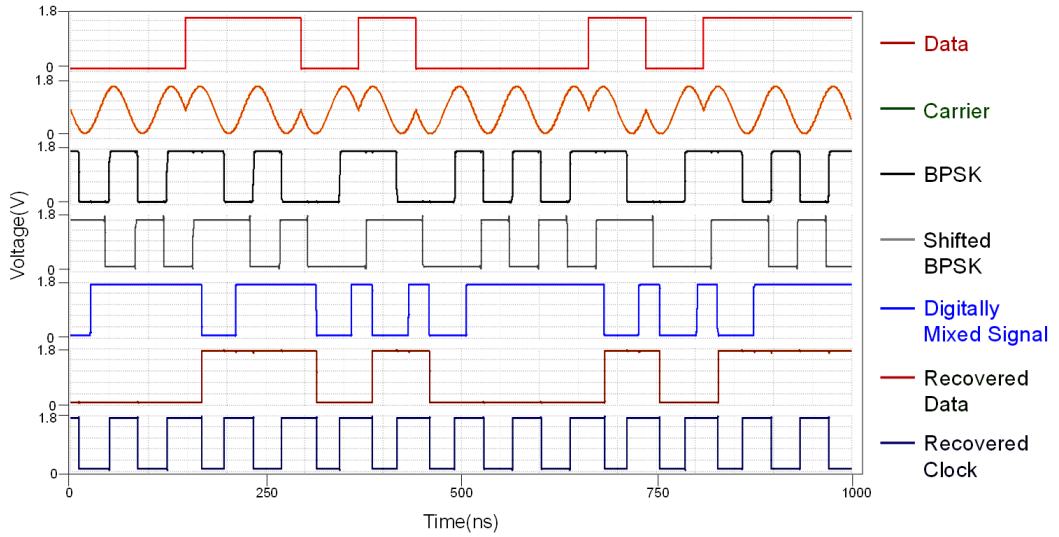


Figure 4.17. Overall simulation results of the demodulator v1

4.2.3 Fully Digital Instantaneous Non-Coherent Demodulator

As an extension to the delay mixed demodulator, a fully digital delay free non-coherent demodulator is designed. The need for such a design had arisen from the fact that created digital delay might cause glitches under process variation and long time use since it is capacitance dependent.

Recovered clock, using the delay mixed demodulator, has distorted duty-cycles caused by varying delay amounts. If a system were to be designed with stable and robust delay mechanisms, entire focus of non-coherent detection becomes obsolete and it becomes more feasible to design a coherent detection system with locked-loop logic.

The fully digital intanstaneous non-coherent demodulator utilizes capacitor charging and discharging with anomaly detection by making discharging operation faster than charging operation and hence creating a temporary off-set spike voltage. In Figure 4.18, overall diagram of the demodulator can be seen.

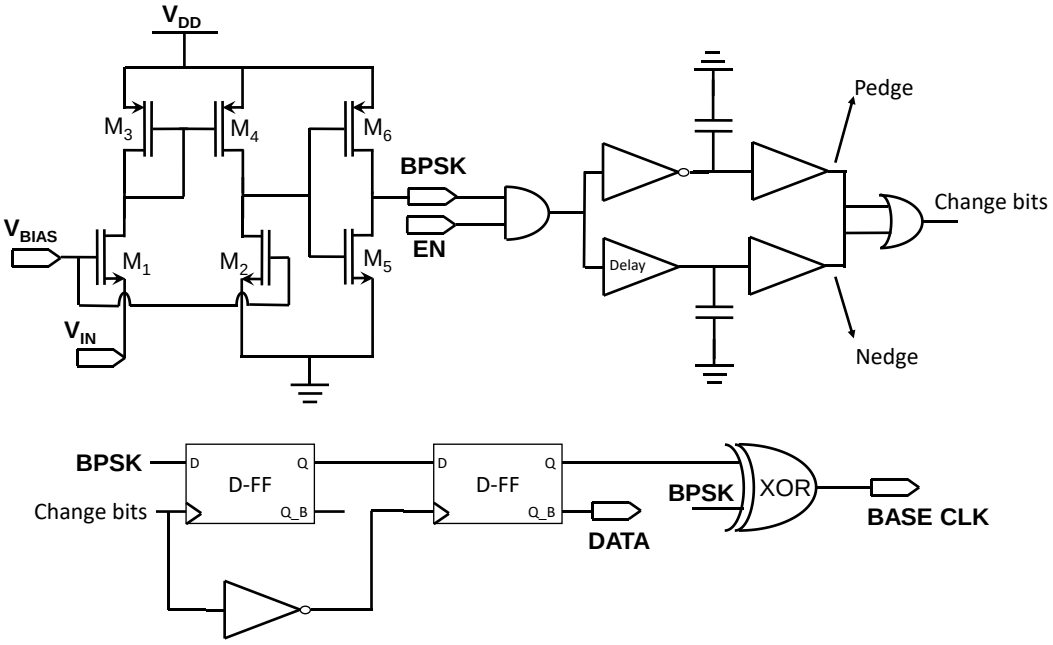


Figure 4.18. Overall diagram of the improved non-coherent demodulator

Demodulator uses the same digitizer block with the delay mixed demodulator. After digitization operation, digitized BPSK and its inverse are used to charge and discharge two distinct capacitors. As discharging currents are larger than charging currents, no excess charge remains on the capacitors. By using a CMOS inverter, points where the voltages of the capacitors are larger than a threshold voltage are detected. When capacitor discharges, output of the inverter returns to its original state, therefore two edges, positive and negative for each symbol change are created.

This change bits information is used as a clock signal to read the BPSK signal with master-slave configuration. This master-slave configuration allows detection at either one of the edges, therefore clears the delays caused by the circuitry after digitization of the incoming modulated waveform.

In order to recover clock, same approach with delay mixed modulator is used. For different symbols, digitized BPSK signal has to be inverted, corresponding to 180° phase shift in digital domain. So, an XOR gate is used for clock recovery.

4.2.3.1 Simulation Results

As with other designs, fully digital delay free demodulator circuit proposed is designed in 180 nm high voltage TSMC(Taiwan Semiconductor Manifacturing Company) process on the EDA software CADENCE and simulations performed with SPECTRE simulation tool.

At first, operation of the demodulator is verified. The digitized BPSK modulated waveform and its inverse are used to charge and discharge two capacitors as explained. In Figure 4.19, this operation is shown. Since discharge currents are twice of the charging currents, capacitors discharge to its original state after charging for a whole period, in half period duration.

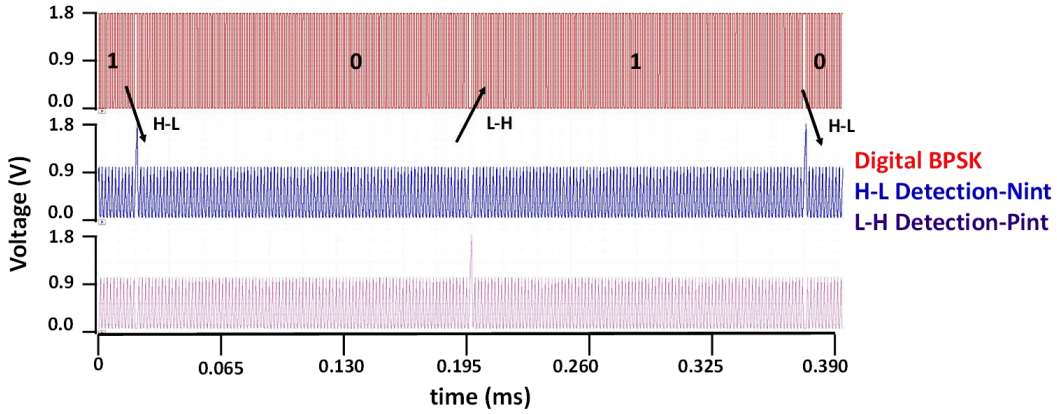


Figure 4.19. Digitized BPSK signal waveform and charging and discharging at symbol changes

Secondly, the voltages on the capacitors are converted to digital control signals using digital buffers (Figure 4.20). This way, for symbol changes from symbol 0 to 1 and 1 to 0, detections are performed.

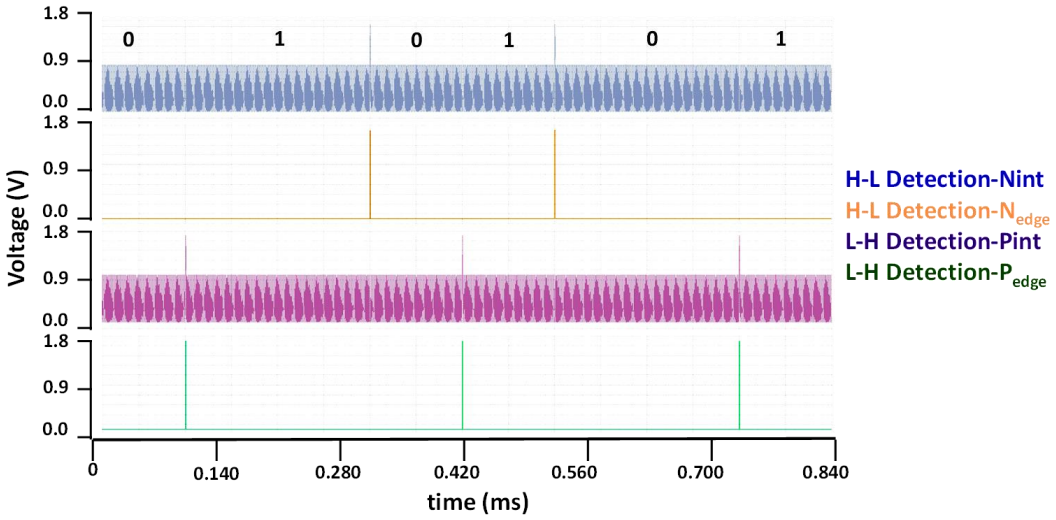


Figure 4.20. Digital control voltages for symbol changes with capacitor voltages

Using these control signals with master-slave configuration with two master-slave D-Flip Flops, data is recovered (Figure 4.21). This master-slave configuration allows faster detection, clearing delays caused by the circuitry until that point.

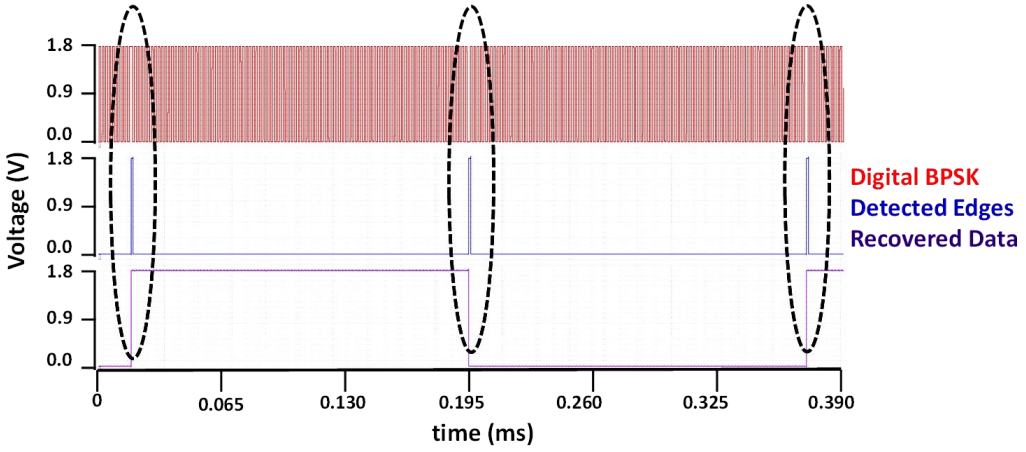


Figure 4.21. Data recovery using control spike voltages, projected onto symbol change points on the digital BPSK waveform

For clock recovery, XOR operation is used. At the points symbol changes, digitized BPSK waveform is inverted, XOR process corresponds to this operation. To have duty cycles closer to 50% in this demodulator, delays are minimized with the master-slave configuration (Figure 4.18) was used. With this configuration,

maximum duty cycle is observed as 53.4% while the minumum was, 47.6%. Recovered clock is shown in Figure 4.22.

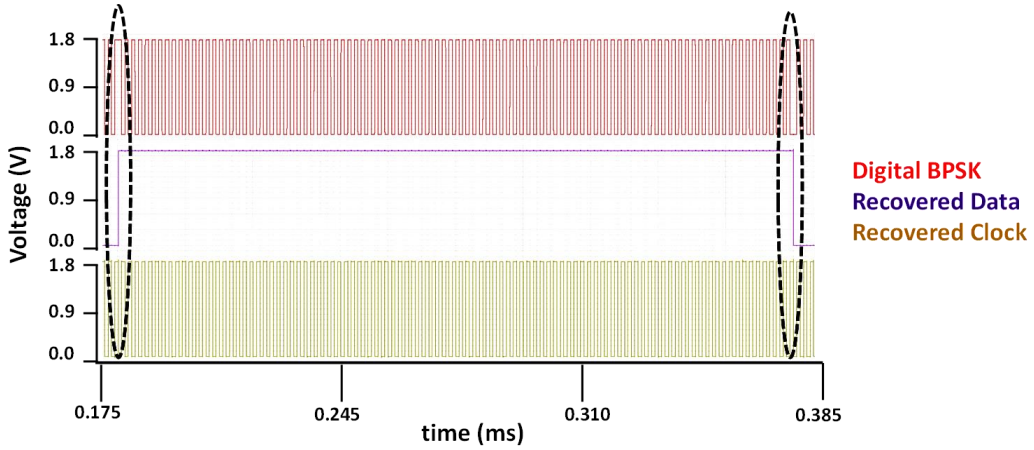


Figure 4.22. Recovered clock with recovered data and digital BPSK waveforms

BER performance is inspected in experimental results.

4.3 Experimental Results

The wireless data transfer system circuit is designed and implemented in 180 nm high voltage TSMC process. Simulation were performed with extracted layout with all possible parasitic effects. In

Figure 4.23, fabricated chip micrograph is shown. In this layout conditions, block were placed separately, areas given are not core areas.

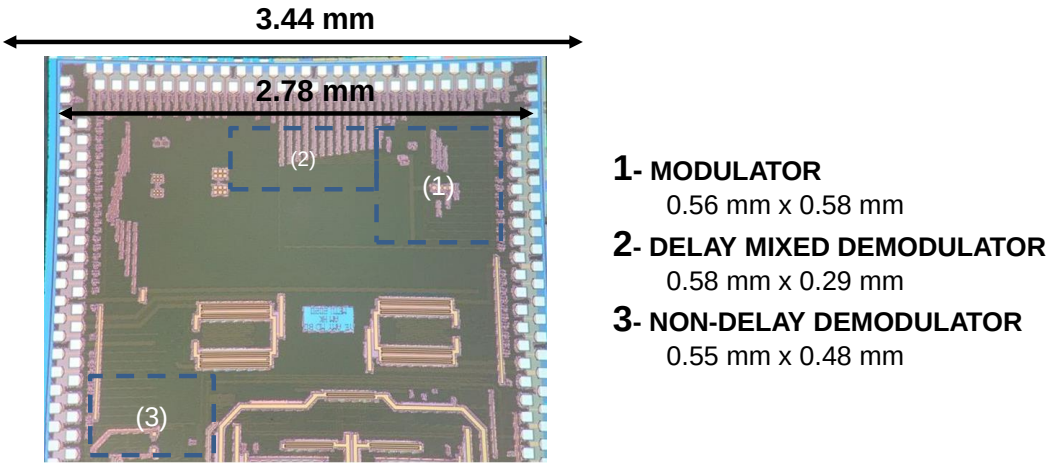


Figure 4.23. Fabricated chip micrograph

In order to test the chip, a Printed Circuit Board (PCB) is designed (Figure 4.24). AC signals are separated with ground isolation, however, due to bottom and top level cross-talk caused by large number of pins on the chip, experimental results vary from simulation results for the modulator. This situation also reflects on the demodulator performance with increased noise and current consumption levels. For the tests, fully digital instantaneous non-coherent demodulator is used.

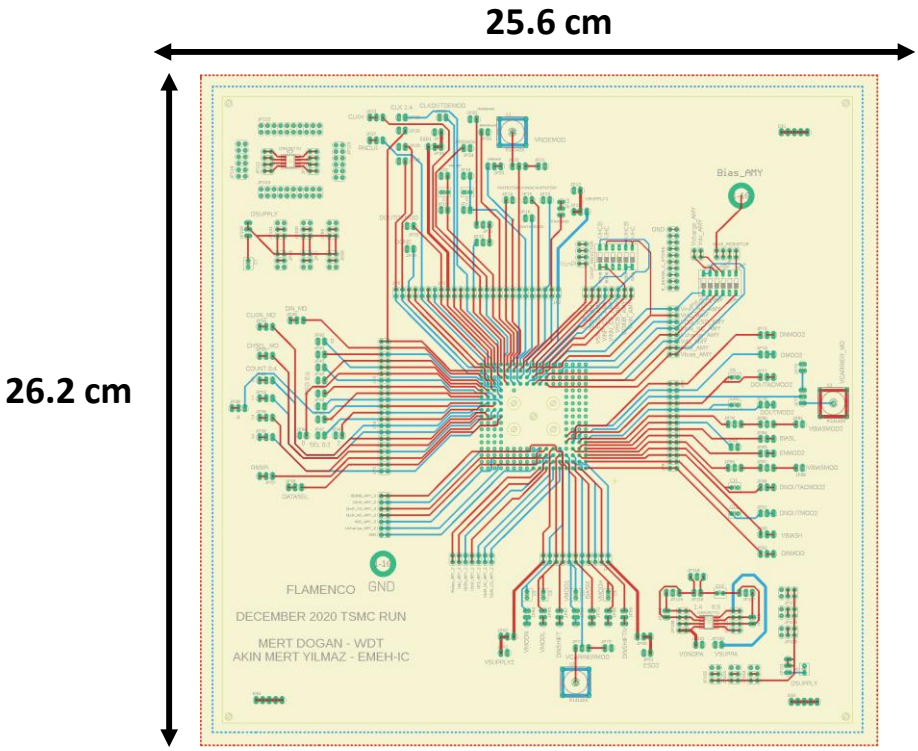


Figure 4.24. Non-Coherent WDT system circuit test PCB layout

As mentioned in modulator description, to drive the coils, an external amplifier was needed. AD 600/602 [67] variable gain amplifier is used for this operation. Instead of using amplifier's differential input pins as the inputs, gain control inputs are used as signal inputs. This is done to reduce the loading effects on the modulator. Differential input voltage level is set to 300 mV and gain amount is adjusted diffentially using modulator outputs. The setup is shown in Figure 4.25. To drive the coils, differential setup with two amplifiers is used. Using two resistors of 100 Ω have increased the stability of the amplifiers and isolated amplifier outputs. Coil is driven with floating configuration, DC offset level is not important on the transmitter coil as it is cleared at the receiver side. For modulator operation, receiver coil voltage is observed.

Symbol transition from 1 to 0 is shown in Figure 4.26, whereas transition from 0 to 1 is shown in Figure 4.27.

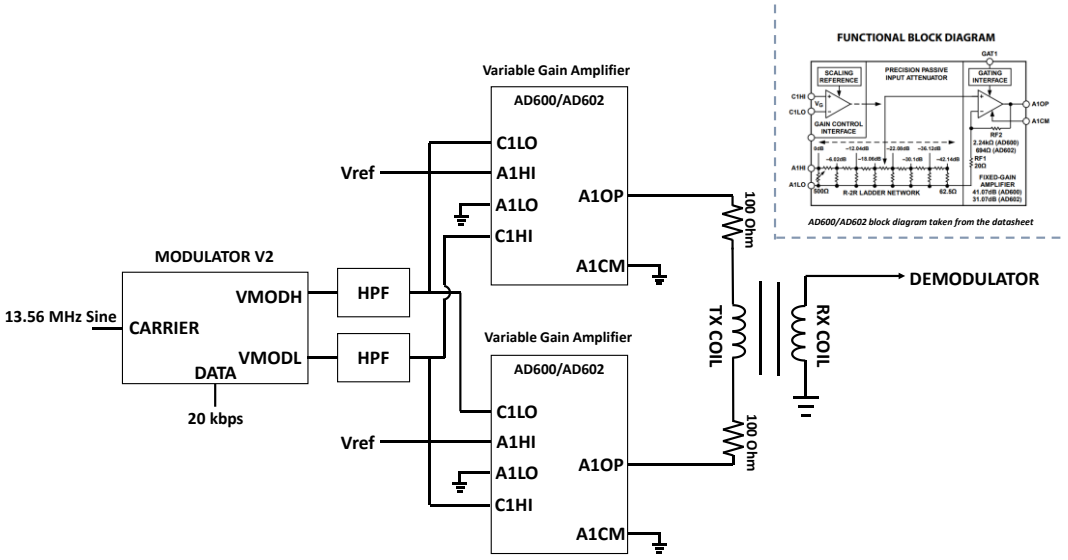


Figure 4.25. Modulator and external amplifier configuration with coil connections

The first period of the carrier at the transition point is lost during transmission, however, phase difference performance of the original carrier and the 180° shifted carrier are better than the simulation results with no significant phase changes. For 0 to 1 transition, two periods of the carrier signal are lost. This means that, entire bandwidth until 13.56 MHz cannot be utilized with this modulator design. However, delays and settling times do not vary for different coupling coefficients, meaning that BERs are improved at the modulator end. A PCB design with better isolation and less crosstalk would have improved the carrier loss problem increasing available bandwidth for use.

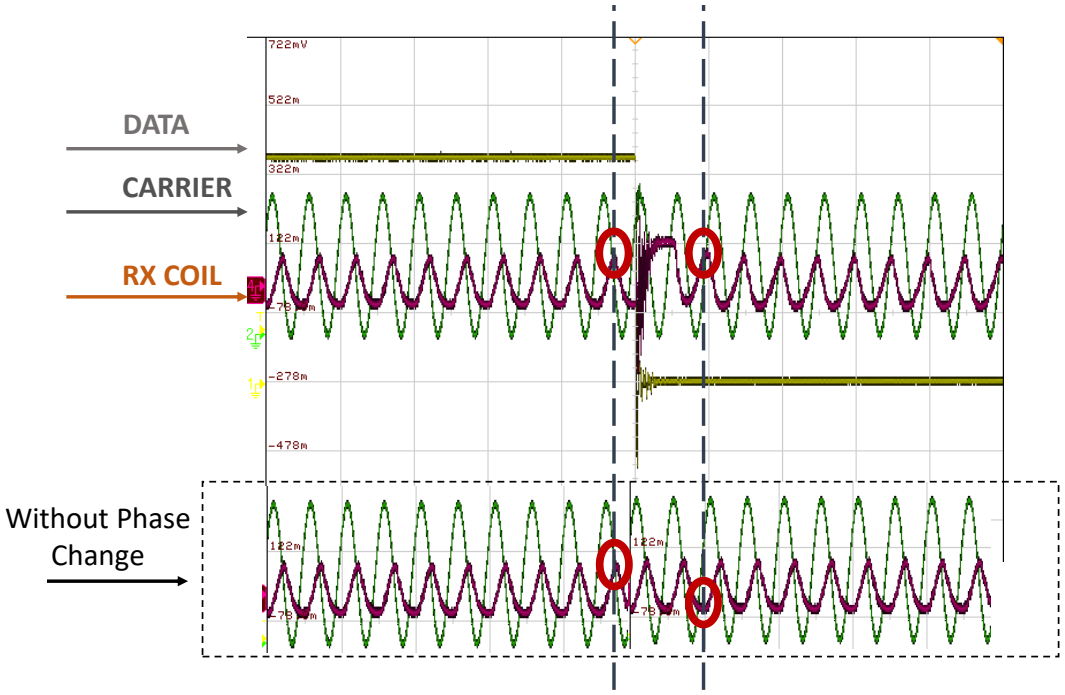


Figure 4.26. Symbol 1 to 0 transition modulated waveform received at the receiver coil with no modulation comparison

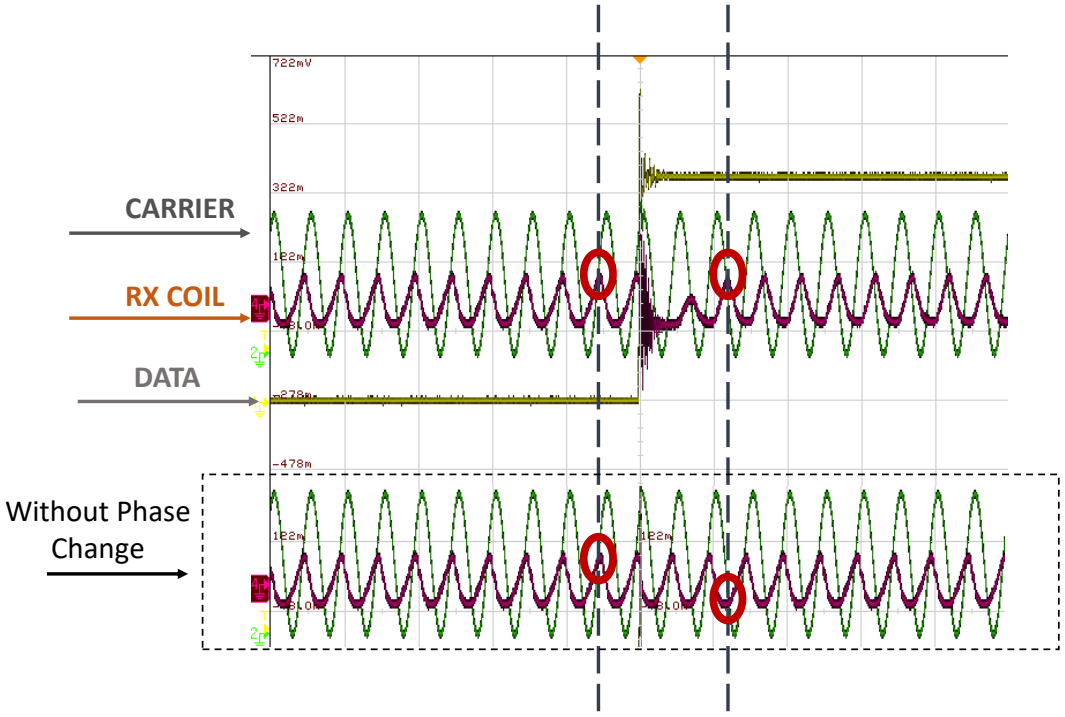


Figure 4.27. Symbol 0 to 1 transition modulated waveform received at the receiver coil with no modulation comparison

Remainder of the experimental results deal with the demodulator tests. As mentioned before, PCB leakages affect demodulator performances. For symbol value 0, voltage of the capacitor for 1 to 0 detection drops below 0 V. Similarly, for symbol 1, voltage of the capacitor for 0 to 1 detection drops below 0 V (Figure 4.28). This does not affect demodulator operation, however increases current consumption by 3 to 4 µA depending on the data duty cycle.

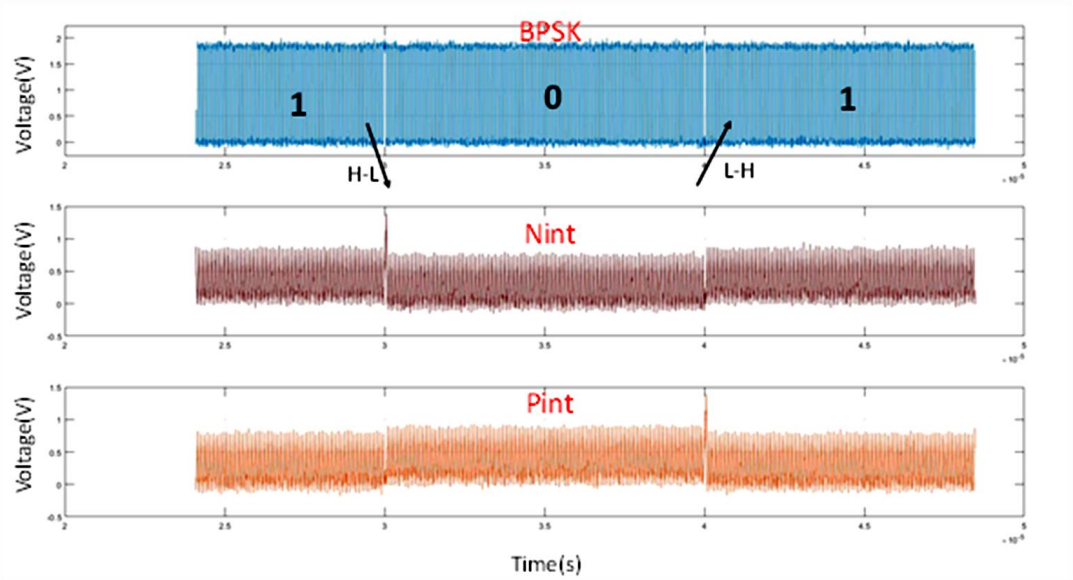


Figure 4.28. Experimental results of the symbol detection capacitance voltages

As the last step, control signal waveforms that define symbol change can be seen in Figure 4.29 alongside with recovered data. The claim with this modulator and demodulator structure was to obtain better BERs and overall WDT efficiency. In Figure 4.30, BERs for coupling coefficients are given. Input voltage levels of the demodulator are set as the same with the semi-coherent demodulator, 0.05 coupling coefficient corresponding to 50 mV and 0.30 coupling coefficient corresponding to 300 mV amplitudes.

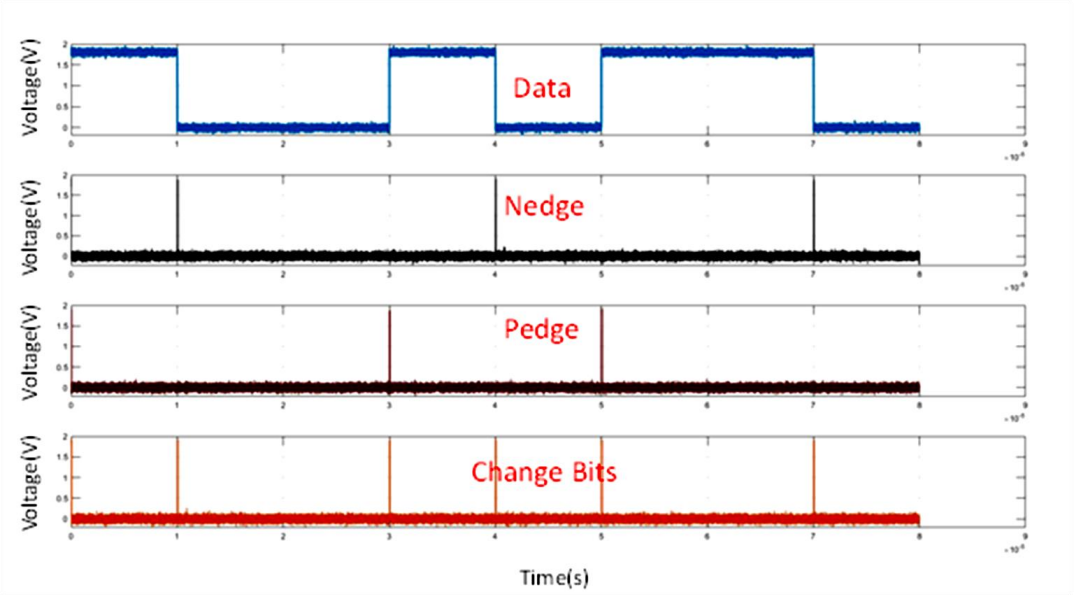


Figure 4.29. Control signals and recovered data waveform

As a summary, performance specifications of the non-coherent WDT system are presented in Table 4.2. It can be seen that all parameters improved compared to previous design.

Table 4.2 Performance table for the WDT system demodulator.

Coupling Coeff. (1 V T_x)	*BER*	*Overall Power Consumption*	*Digitizer Efficiency (%)*	*Overall Efficiency (%)*
0.05	3.0×10^{-3}	24.21 µW	81.6	4.42
0.10	1.2×10^{-3}	24.12 µW	90.9	13.16
0.15	8.5×10^{-4}	23.98 µW	96.6	17.42
0.20	2.4×10^{-4}	24.01 µW	97.8	28.46
0.25	6.3×10^{-5}	24.16 µW	98.9	49.71
0.30	2.8×10^{-6}	24.12 µW	100.0	100.00

For the designed demodulator, BERs for lower coupling are improved compared to the in-built BPSK BER.

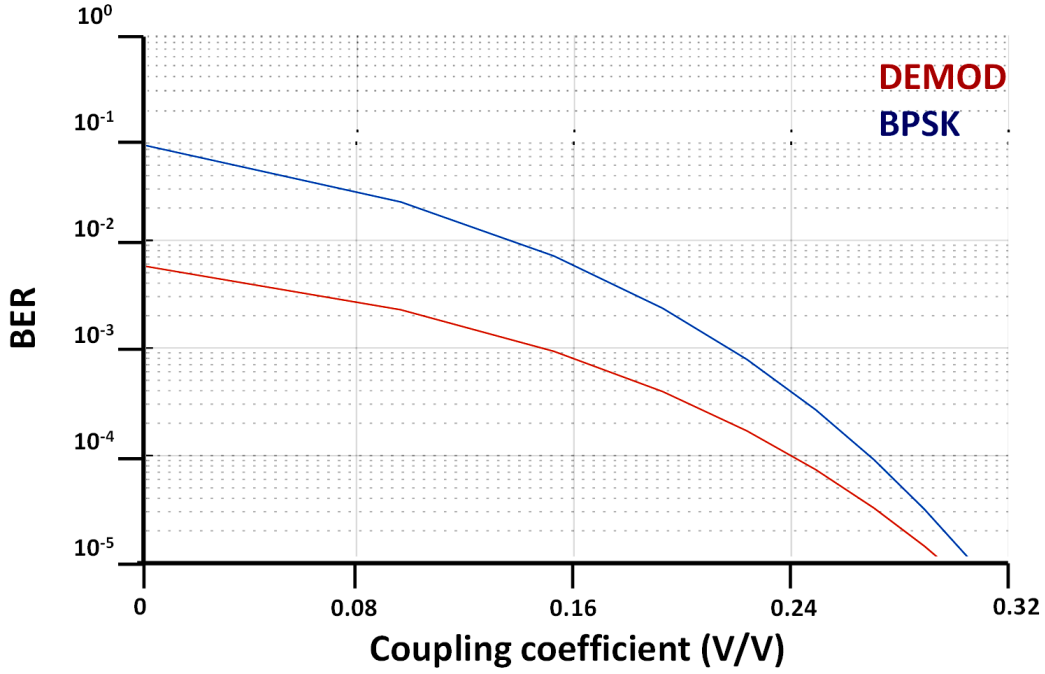


Figure 4.30. BERs for the proposed demodulator and BPSK

4.3.1 Discussion

In this chapter, a fully digital non-coherent wireless data transfer system is presented. The system is composed of a BPSK modulator, which is an improved version of the previous design and two non-coherent demodulators. Circuits are designed with 180 nm TSMC techonology and manufactured.

Modulator utilized two carriers, with 180° phase shift in between, acquired by a current subtraction circuitry with bias manipulation. In this version, amplitude modulated waveforms were created using common source amplifiers different than the first modulator with common gate amplifiers. This resulted in a decrease in gain dropping from 19.1 dB to 14.44 dB. Moreover, voltage buffers were placed in between the high-pass filters and amplifier outputs, isolating coil and amplifiers. Combining these two factors, an external amplifier was used to drive the transmitter coil. For this AD 600/602 variable ampfliers were utilized. Phase delays in between the two modulated phases dropped significantly to a range that could

not be distinguished after these actions. Moreover, without modulator driving the coils, power consumption dropped significantly, to 23.1 μW.

For the demodulator side, a fully digital, delay and oscillator free structure was designed. In this design, detection was performed directly by detecting phase changes in digital domain. By discharging detection capacitor two times faster than charging at phase change points, digital control signals were acquired. Current consumption of the demodulator was measured as 13.32 μA, 3 μA of it was caused by the test PCB leakages, producing below 0 V capacitor voltages. As a future work, this needs to be addressed. When compared with the semi-coherent design, BER was improved by a factor of at least 10 for the lowest coupling coefficients, to the limit of BPSK BER limitations.

As an overall improvement, transistor sizes should be optimized before implantation, as there is no overall control block designed in the system, loading effects and conditions are unknown and digital pins are not tested for different loading conditions. Overall control block should also include back-telemetry control signal as well.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, a wireless data transfer system with magnet free inductive coupling has been designed and implemented. These designs include modulator and demodulator blocks with different architectures, semi-coherent and non-coherent detection with improved bit-error-rate. The aim of this system is to provide communication with the medical implants after surgery. Target implants are magnet free, hence wireless data transfer system should be able to work under varying inductive coupling conditions. Tests and measurements are performed with the designed circuits in the system, and results are observed.

Following accomplishments are achieved with this thesis:

1. Literature reviews are made and wireless data transfer techniques are examined in detail. Data modulation methods are inspected, drawbacks and advantages of these methods are compared with previous studies.
2. Inductive coupling is used for data transmission. For magnet free operation, inductive coupling strength ranges are decided for a realistic application. These ranges are tested using a skin phantom. Data modulation methods are simulated and their spectral efficiency and robustness are observed. Moreover, these methods are tested with mixer components under varying conditions.
3. A Wireless Data Transfer System circuitry is designed, which utilizes Binary Phase Shift Keying, as it has been chosen as the most feasible modulation method. System included a modulator-demodulator pair and a patient fitting processor. Designed demodulator operates digitally and semi-coherently with an oscillator of which output waveform depends on the DC

level of the digitized modulated waveform. Digitized waveforms for different coupling coefficients are adjusted in a way that all of them have the same DC offset and duty cycle. Design is implemented in 180 nm high voltage TSMC process. Modulator carrier phase delays are measured as 31.7°, less than 45° which is the minumum phase different that can be detected in BPSK. For the lowest coupling coefficient targeted, system has a BER of 2.8 x 10^{-2}. Operation of the modulator-demodulator pair is verified using a patient fitting processor. With the BPSK system altogether, for 8 channels, 7 bit channel data are transferred and placed succesfully.

4. Another improved version of the BPSK system is designed for wireless data transfer operation. In this design, modulator block used two carriers with 180° phase shift. Secondary carrier is generated by current subtraction, therefore it always has 180° phase shift. Transmitter coil is driven by using an external amplifier of which control signals are modulator outputs. Two different but related non-coherent demodulator designs are made. First design utilized digital mixing operation with XOR gates. Digitized waveform is mixed with a shifted version of itself digitally and symbol changes are detected. Second demodulator detected phase changes directly by charging and discharging detection capacitors with different currents. A delay correction master-slave configuration is used before clock generation to reduce duty-cycle variations of the clock, which was an issue in the previous designs. The improved system is also designed and implented with 180 nm high voltage TSMC technology. Compared to previous design modulator performance is increased by reducing phase delays to 9.95°. This delay is not observed in the tests. Demodulator performances, combined with the improvements on the modulator block, have improved significantly. For 0.05 coupling coefficient, BER is measured as 3.01 x 10^{-3}, which is more than 10 times. Duty cycle of the recovered clocked varied in between 53.4% and 47.6%, which is improvement compared to other digital designs. Overall system consumes 47.1 μW, without external amplifiers.

5.2 Future Work

Future improvements regarding the Wireless Data Transfer System can be given as follows:

1. The designed system is targeted to be used in medical implants. Implanted system will have both demodulator and modulator circuits together. In this setup, a control block is necessary for autonomous back-telemetry operation. This mode should be added to the overall control block of the implant. As a future work, control block must include mode selection for forward and back telemetry.
2. As a digital design, test chips suffered from a large number of controlling and monitoring pins and therefore buffers are overlooked at some points of design. For digital pins, buffers with increase in transistor sizes should be added to the output stages before implemantation. During the tests, this issue is overcome by using external buffers and integrated circuits such as programmable silicon on-chips with differential active probes.
3. For fully-autonomous operation, an oscillator and voltage reference circuit design is necessary for carrier generation and biasing. In the design, carrier and references signals are assumed to be available at all times.
4. In vivo tests should be performed with animal subjects to validate data transfer operation. This might be available using patient fitting system and observing stimulation levels according to adjustments.
5. The system should be tested with the wireless power transfer system design since coils are shared for wireless transmission applications. A secondary sense coil should be designed if any interference is observed.

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