INVESTIGATION OF PARALLEL-CONNECTED GAN E-HEMT VSI-BASED SERVO DRIVES

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submitted by **HÜSEYIN YÜRÜK** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Engineering**

Assoc. Prof. Dr. Ozan Keysan
Supervisor, **Electrical and Electronics Engineering, METU**

Examining Committee Members:

Assist. Prof. Dr. Emine Bostancı
Electrical and Electronics Engineering, METU

Assoc. Prof. Dr. Ozan Keysan
Electrical and Electronics Engineering, METU

Assist. Prof. Dr. Erhan Demirok
Electrical and Electronics Engineering, Dokuz Eylül University

Prof. Dr. Işık Çadırcı
Electrical and Electronics Engineering, Hacettepe University

Prof. Dr. Muammer Ermiş
Electrical and Electronics Engineering, METU

Date: 19.01.2022

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Hüseyin Yürük

Signature :

ABSTRACT

INVESTIGATION OF PARALLEL-CONNECTED GAN E-HEMT VSI-BASED SERVO DRIVES

Yürük, Hüseyin
Ph.D., Department of Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Ozan Keysan

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Nonlinearities in voltage source inverters (VSIs) are thought to be the primary cause of output voltage distortions which cause low-order harmonics in the output current. These nonlinearities also considerably degrades control performance and system stability for low-speed applications with low-inductance motors, particularly when the system operates in the low-torque area. The impact of the nonlinearities on the phase current and current control of a silicon (Si) metal-oxide-semiconductor field-effect transistor (MOSFET) based VSI are examined in this thesis using a coreless permanent magnet synchronous motor (PMSM). To address this issue, a gallium nitride (GaN) enhancement-mode high electron mobility transistor (E-HEMT) based VSI is proposed. Based on the results, a GaN E-HEMT VSI-based servo drive is being developed to replace its Si MOSFET VSI-based counterpart. It is about half the size of the previous one, allowing for the use of two servo drives in parallel rather than one for redundancy. The use of parallel-connected servo drives offers the benefit of increased torque capacity, reliability, redundancy, and modularity. Smaller variances in the system clocks of the separate microcontrollers, asynchronous pulse width modulation (PWM) carrier signals, and hardware differences, on the other hand, might cause non-identical output voltages of the parallel modules, resulting in circulating currents. These circulating currents limit parallel operation, increase power consumption, induce imbalanced power distribution, and degrade control performance. A fault-tolerant parallel-connected GaN E-HEMT VSI based servo drive scheme is proposed to reduce the circulating currents and to eliminate the need for extra inductors at the output and separate DC supplies at the input of the inverters. Various experimental tests are conducted with up to six parallel-connected servo drives and a PMSM for validation.

Keywords: nonlinearity in VSIs, dead time, coreless PMSMs, GaN E-HEMT VSI-based servo drive, parallel-connected VSIs

ÖZ

PARALEL BAĞLI GAN E-HEMT VSI TABANLI SERVO SÜRÜCÜLERİN İNCELENMESİ

Yürük, Hüseyin
Doktora, Elektrik ve Elektronik Mühendisliği Bölümü
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Çıkış akımında düşük dereceli harmoniklere neden olan çıkış gerilimi bozulmalarının birincil nedeninin gerilim kaynağı eviricilerindeki (VSIler) doğrusal olmayan yapılar olduğu düşünülmektedir. Bu doğrusal olmama durumları ayrıca, özellikle sistem düşük torklu alanda çalıştığında, düşük endüktanslı motorlara sahip düşük hızlı uygulamalar için kontrol performansını ve sistem kararlılığını önemli ölçüde düşürür. Doğrusal olmayan yapıların, bir silikon (Si) metal-oksit-yarı iletken alan etkili transistör (MOSFET) tabanlı VSInin faz akımı ve akım kontrolü üzerindeki etkisi, bu tezde çekirdeksiz bir sabit mıknatıslı senkron motor (PMSM) kullanılarak incelenmiştir. Bu sorunu ele almak için, bir galyum nitrid (GaN) geliştirme modlu yüksek elektron hareketli transistör (E-HEMT) tabanlı VSI önerilmiştir. Sonuçlara dayanarak, Si MOSFET VSI tabanlı yerine muadili GaN E-HEMT VSI tabanlı bir servo sürücü geliştirilmiştir. Bir öncekinin yaklaşık yarısı büyüklüğündedir ve yedeklilik için bir servo sürücü yerine paralel olarak iki servo sürücünün kullanılmasına izin verir. Paralel bağlı servo sürücülerin kullanımı, artan tork kapasitesi, güvenilirlik, yedeklilik ve modülerlik avantajı sunar. Ayrı mikrodenetleyicilerin sistem saatlerindeki küçük farklılıklar, asenkron darbe genişlik modülasyonu (PWM) taşıyıcı sinyalleri ve donanım farklılıkları ise paralel modüllerin özdeş olmayan çıkış gerilimlerine neden olabilir ve bu da dolaşan akımlara neden olabilir. Bu dolaşan akımlar paralel çalışmayı sınırlar, güç tüketimini arttırır, dengesiz güç dağılımına neden olur ve kontrol performansını düşürür. Hataya toleranslı paralel bağlı GaN E-HEMT VSI tabanlı bir servo sürücü şeması, dolaşan akımları azaltmak ve invertörlerin çıkışında ekstra indüktör ve girişinde ayrı DC besleme ihtiyacını ortadan kaldırmak için önerilmiştir. Doğrulama için altı adede kadar paralel bağlı servo sürücü ve bir PMSM kullanılarak çeşitli deneysel testler gerçekleştirilmiştir.

Anahtar Kelimeler: VSI'lerde doğrusal olmayan yapılar, ölü zaman, çekirdeksiz PMSM'ler, GaN E-HEMT VSI tabanlı servo sürücü, paralel bağlı VSI'ler

To My Family

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TABLE OF CONTENTS

ABSTRACT v

ÖZ vii

ACKNOWLEDGMENTS x

TABLE OF CONTENTS xi

LIST OF TABLES xvi

LIST OF FIGURES xviii

LIST OF ABBREVIATIONS xxv

LIST OF SYMBOLS xxvii

CHAPTERS

1 INTRODUCTION 1

  1.1 Motivation and Scope of the Thesis 1

  1.2 The Outline of the Thesis 6

2 NONLINEARITIES FOR SI MOSFET AND GAN E-HEMT BASED VSIS 11

  2.1 Introduction 11

  2.2 Nonlinearity Analysis of SI MOSFET-Based VSI 14

  2.3 Experimental Study on SI MOSFET-Based VSI 20

    2.3.1 Observation of Current Harmonics as a Result of Nonlinear Effects 20

2.3.2 Relationships Between Switching Frequency and Nonlinearities 23

2.3.3 The Calculation of the Compensation Function 30

2.3.4 Experimental Results of the Compensation of the Nonlinearity 32

2.4 Experimental Work with GaN E-HEMT Based VSI 33

2.4.1 Nonlinearities in GaN E-HEMT Based VSI: Effects of Switching Frequency and Dead Time 33

2.4.2 Nonlinearities in GaN E-HEMT Based VSI: Phase Current Harmonic Distortions 37

2.4.3 Current Control Bandwidth Measurements of the GaN E-HEMT Based VSI 39

2.5 Power Loss and Cost Comparison 40

2.6 Chapter Summary 46

3 GAN E-HEMT VSI-BASED SERVO DRIVE DESIGN 49

3.1 Introduction 49

3.2 Wide Bandgap Semiconductor: Gallium Nitride E-HEMT 49

3.2.1 History 49

3.2.2 GaN HEMT Structure 50

3.2.2.1 Cascode GaN HEMT 50

3.2.2.2 True Normally off GaN HEMT 51

3.2.3 Material Properties 52

3.2.4 Third Quadrant Operation 54

3.2.5 Current Collapse Effect 55

3.2.6 Short Circuit Behavior 56

3.2.7 High dv/dt and Switching Frequency 57

3.2.8 Importance of Layout Design 57

3.3 GaN E-HEMT VSI-Based Servo Drive Design 58

3.3.1 The Inverter Card of the GaN E-HEMT VSI-based Servo Drive 60

3.3.2 The DSP Card of the GaN E-HEMT VSI-based Servo Drive . 64

3.3.3 The Interface Card of the GaN E-HEMT VSI-based Servo Drive 65

3.3.4 The GaN E-HEMT VSI-based Servo Drive 65

3.3.5 Load Tests of the GaN E-HEMT VSI-based Servo Drive . . . 66

3.3.5.1 Efficiency Determination of the GaN E-HEMT VSI-based Servo Drive 66

3.3.5.2 Thermal Analysis of the GaN E-HEMTs of the Servo Drive 72

3.3.6 Conducted Emission Tests of the GaN E-HEMT VSI-based Servo Drive 75

3.4 Conclusion 77

4 PARALLEL CONNECTED GAN E-HEMT VSI-BASED SERVO DRIVES FOR PMSMS 81

4.1 Introduction 81

4.2 Circulation Current Due to Asynchronous Carrier Signals 83

4.2.1 Region (I) 86

4.2.2 Region (II) 88

4.2.3 Region (III) 88

4.2.4 Region (IV) 90

4.2.5 Simulation Results 92

4.3 Experimental Work 94

4.3.1 Effect of Clock Inconsistencies Between Individual Microcontrollers 96

4.3.2 Comparison with Simulation Results 97

4.3.3 Block Schema of the Parallel Operation 99

4.3.4 Dynamic Performances of the Parallel Operation 100

4.3.4.1 Startup Condition 100

4.3.4.2 Step Torque Disturbance 101

4.3.4.3 Chirp Torque Disturbance 101

4.3.4.4 Step Speed Reference 102

4.3.5 Faulty Conditions of the Slaves 103

4.3.5.1 Turning Off the Slave-#3 During Operation 103

4.3.5.2 Opening the Output of Phase A of the Slave-#2 During Operation 104

4.3.6 Efficiency Comparison: Parallel vs. Single Operation 105

4.3.7 Current Ripple Comparison 110

4.4 Chapter Summary 110

5 CONCLUSIONS 113

5.1 A Short Synopsis of the Thesis 113

5.2 Literature Contributions 116

5.3 Prospects for the Future 118

REFERENCES 121

APPENDICES

A PUBLICATIONS ARISING FROM THE THESIS 135

CURRICULUM VITAE 137

LIST OF TABLES

TABLES

Table 2.1 PMSM Parameters 21

Table 2.2 Phase Current Harmonic Distortions [%] at 10 Hz and 40 Hz Electrical Reference Speed at No Load 23

Table 2.3 Phase Current Harmonic Distortions [%] at 10 Hz and 40 Hz Electrical Reference Speed at No Load with GaN E-HEMT based VSI 38

Table 2.4 Parameters used in loss calculations 44

Table 2.5 Power Losses of the Leg A at some of the operating points 46

Table 3.1 test caption 54

Table 3.2 Features of GaN E-HEMT VSI based Servo Drive 60

Table 3.3 Available GaN E-HEMTs 62

Table 3.4 PMSM and Experimental Setup Parameters 68

Table 3.5 Servo Drive Parameters 69

Table 3.6 Experimentally Efficiency Calculation Procedure 70

Table 3.7 Analytically Efficiency Calculation Procedure 71

Table 3.8 Common Parameters for Thermal Experiment Tests 75

Table 3.9 Thermal Experiment Tests Parameters 75

Table 3.10 Thermal Tests, T_C of GaN E-HEMTs of the Servo Drive 77

Table 4.1 Simulation Circuit Parameters 93

Table 4.2 Motor Drive and PMSM Parameters 95

Table 4.3 Parameters of Experimental Setup for Efficiency Comparison of Parallel vs. Single Operation 108

Table 4.4 Efficiency Calculation of the Single Operation 108

Table 4.5 Efficiency Calculation of the Parallel Operation 109

Table 5.1 Experimental Parameters of the Studies in the Literature 118

LIST OF FIGURES

FIGURES

Figure 1.1 The block diagram of the nonlinearity problem. 4

Figure 1.2 test caption 5

Figure 1.3 The simplified block diagram of two servo drives connected in parallel. 6

Figure 1.4 test caption 7

Figure 1.5 test caption 8

Figure 2.1 Si MOSFET-based VSI PMSM drive block schema 15

Figure 2.2 Gate signals and leg A output voltages of the SI MOSFET-based VSI 15

Figure 2.3 Voltage errors in the legs as a result of VSI nonlinearities. 18

Figure 2.4 Voltage errors in α-β reference frame as a result of VSI nonlinearities. 19

Figure 2.5 Voltage errors in d-q reference frame as a result of VSI nonlinearities. 19

Figure 2.6 Experimental setup with Si MOSFET-based VSI. 21

Figure 2.7 Phase current i_a, d-q reference frame current i_d and i_q and their frequency spectrums in open-loop control. 22

Figure 2.8 i_d current and u_d voltage, Si MOSFET-based VSI at $f_{sw} = 10$ kHz to 100 kHz. 24

Figure 2.9 u_d voltage versus i_d current, Si MOSFET-based VSI at $f_{sw} = 10$ kHz to 100 kHz. 25

Figure 2.10 Closed-loop time domain response of i_{dref} and measured i_d current, at $f_{sw} = 100$ kHz, Si MOSFET-based VSI. (a) without any offset (b) offset at linear region (c) offset at nonlinear region 26

Figure 2.11 Frequency response of i_{dref} and measured i_d current, at $f_{sw} = 100$ kHz, at nonlinear and linear regions, Si MOSFET-based VSI. . . . 27

Figure 2.12 u_d voltage versus i_d current, with varying motor shaft speed and $f_{sw} = 100$ kHz, Si MOSFET-based VSI. 27

Figure 2.13 Variation of the apparent resistance value along the nonlinear region at $f_{sw} = 100$ kHz. 29

Figure 2.14 Current control open-loop at linear and nonlinear regions at $f_{sw} = 100$ kHz. 29

Figure 2.15 The effect of the nonlinear region on the position control loop at $f_{sw} = 100$ kHz. 30

Figure 2.16 The sections of the i_d current and u_d voltage graph at $f_{sw} = 20$ kHz. 31

Figure 2.17 u_d voltage versus i_d current graph with fitted curves at $f_{sw} = 20$ kHz. 31

Figure 2.18 The 100 Hz i_d reference and the measured i_d values with and without the nonlinearity compensation, Si MOSFET-based VSI. 32

Figure 2.19 Chirp signal from 10 Hz to 250 Hz i_d reference and measured i_d in time domain, Si MOSFET-based VSI. (a) without compensation (b) with compensation 33

Figure 2.20 Chirp signal from 10 Hz to 250 Hz i_d reference and measured i_d with and without compensation in frequency domain, bode diagram, Si MOSFET-based VSI. 34

Figure 2.21 Experimental setup for GaN E-HEMT based VSI. 35

Figure 2.22 u_d and i_d with time, GaN E-HEMT based VSI at $f_{sw} = 10\ kHz$ to 100 kHz, t_{dead} 20 ns and 100 ns. 36

Figure 2.23 u_d voltage versus i_d current, at $f_{sw} = 10\ kHz$ to 100 kHz, $t_{dead} = 20\ ns$ and 100 ns, GaN E-HEMT based VSI and Si MOSFET-based VSI at $f_{sw} = 100\ kHz$ and $t_{dead} = 1 \mu s$. 37

Figure 2.24 Chirp signal from 10 Hz to 250 Hz i_d reference and measured i_d, at $f_{sw} = 100\ kHz$ in time domain, GaN E-HEMT based VSI. (a) with 20 ns dead time (b) with 100 ns dead time 38

Figure 2.25 Frequency response of the i_{dref} and measured i_d current, at $f_{sw} = 100\ kHz$, with 20 ns and 100 ns dead time, GaN E-HEMT based VSI and Si MOSFET-based VSI at nonlinear region. 39

Figure 2.26 The open-loop frequency response characteristics of the i_d current control loop at $f_{sw} = 100\ kHz$, GaN E-HEMT based VSI. (a) gain and phase (b) gain zoomed at zero-crossing dB 41

Figure 2.27 The open-loop frequency response characteristics of the i_q current control loop at $f_{sw} = 100\ kHz$, GaN E-HEMT based VSI. (a) gain and phase (b) gain zoomed at zero crossing dB 42

Figure 2.28 Conduction power losses of the leg A for Si MOSFET and GaN E-HEMT. 44

Figure 2.29 Switching power losses of the leg A for Si MOSFET and GaN E-HEMT. 45

Figure 2.30 Total power losses of the leg A for Si MOSFET and GaN E-HEMT. 45

Figure 3.1 Cascode GaN HEMT, low voltage Si MOSFET in series with depletion mode GaN HEMT (D-HEMT) 51

Figure 3.2 The true normally OFF GaN HEMT by p-GaN gate method (a) zero or negative gate bias to turn-off (b) positive gate bias to turn-on . . 53

Figure 3.3 Material Properties of Si, SiC and GaN 54

Figure 3.4 Dimensions of the servo drives:(a) The Si MOSFET VSI-based servo drive (b) The GaN E-HEMT VSI-based servo drive 59

Figure 3.5 The basic functions of the cards of the GaN E-HEMT VSI-based servo drive and the signals between them. 61

Figure 3.6 The block diagram of the inverter card and the signals between the inverter and DSP cards of the GaN E-HEMT VSI-based servo drive. 63

Figure 3.7 The inverter card of the GaN E-HEMT VSI-based servo drive (a) top side (b) bottom side 64

Figure 3.8 The DSP card of the GaN E-HEMT VSI-based servo drive . . . 65

Figure 3.9 The interface card of the GaN E-HEMT VSI-based Servo Drive . 66

Figure 3.10 Inside view of the GaN E-HEMT VSI-based servo drive (a) Front view (b) Back view 67

Figure 3.11 The block schema of the FOC to control the PMSM 68

Figure 3.12 The block diagram of the test setup for efficiency evaluation of the GaN E-HEMT VSI-based servo drive. 68

Figure 3.13 mycaption 70

Figure 3.14 The loss distributions of the parts of the GaN E-HEMT VSI-based servo drive at $24V$. 72

Figure 3.15 The efficiency estimation of the GaN E-HEMT VSI-based servo drive at $48V$. The blue line is the efficiency based on the experimental results, and the orange line is the efficiency based on the analytical calculations. 73

Figure 3.16 The loss distributions of the parts of the GaN E-HEMT VSI-based servo drive at $48V$. 73

Figure 3.17 The simplified equivalent thermal circuit to calculate the junction temperature of the GaN E-HEMTs. 74

Figure 3.18 Thermal images at steady state of the GaN E-HEMTs of the servo drive (a) test-#1 (b) test-#2 (c) test-#3 (d) test-#4 76

Figure 3.19 The equivalent EMI filter circuit of the power input of the GaN E-HEMT VSI-based servo drive 78

Figure 3.20 The conducted emission test setup for the GaN E-HEMT VSI-based servo drive 78

Figure 3.21 CE102 test results of the GaN E-HEMT VSI-based servo drive (a) power lead (b) return 79

Figure 3.22 CE101 test results of the GaN E-HEMT VSI-based servo drive (a) power lead (b) return 80

Figure 4.1 Circuit diagram of the parallel-connected inverters and PMSM. . 84

Figure 4.2 The phase angle difference between carrier signals of the parallel-connected inverters is 90°. 85

Figure 4.3 (a) The circulation current path when the phase angle difference between carrier signals is 90°, region (I) (b) Equivalent circuit of the circulation current path. 87

Figure 4.4 (a) The circulation current path when the phase angle difference between carrier signals is 90°, region (II) (b) Equivalent circuit of the circulation current path. 89

Figure 4.5 (a) The circulation current path when the phase angle difference between carrier signals is $90°$, region (III) (b) Equivalent circuit of the circulation current path. 90

Figure 4.6 (a) The circulation current path when the phase angle difference between carrier signals is $90°$, region (IV) (b) Equivalent circuit of the circulation current path. 91

Figure 4.7 Simulation results when the phase angle difference between carrier signals is $90°$ and the switching frequency is 200 kHz at steady-state. 92

Figure 4.8 Simulation results during startup with $90°$ phase angle difference between carrier signals and the switching frequency is 200 kHz. 94

Figure 4.9 Experimental setup with four parallel-connected GaN E-HEMT VSI-based servo drives. 95

Figure 4.10 V_{a1} and V_{a2} waveforms (a) without synchronization (b) with synchronization where $t_0 = 0$ and $t_f = 200000\ \mu s$. 96

Figure 4.11 Experimental results when the phase angle difference between carrier signals is $90°$ and the switching frequency is 200 kHz at steady-state. 98

Figure 4.12 Experimental results during startup with $90°$ phase angle difference between carrier signals and the switching frequency is 200 kHz. . 98

Figure 4.13 Experimental results when the phase angle difference between carrier signals is $90°$ and the switching frequency is 400 kHz at steady-state. 99

Figure 4.14 The overall block schema of the parallel operation of servo drives. 100

Figure 4.15 Speed of the PMSM and phase A currents of servo drives and PMSM at startup. 101

Figure 4.16 Speed of the PMSM and phase A currents of servo drives and PMSM with step torque disturbance. 102

Figure 4.17 Speed of the PMSM and i_q currents of servo drives with chirp torque disturbance ($0.1Hz$ to $1.0Hz$ at full load). 103

Figure 4.18 Speed of the PMSM and phase A currents of servo drives and PMSM with step speed reference variation. 104

Figure 4.19 Speed of the PMSM and phase A currents of servo drives and PMSM, slave-#3 goes to faulty and back to a healthy condition by manually during operation. 105

Figure 4.20 Experimental setup with six parallel-connected GaN E-HEMT VSI-based servo drives. 106

Figure 4.21 Speed of the PMSM, phase A currents of servo drives and PMSM, and phase currents of the slave-#2, phase A of the slave-#2 is open-circuited by a relay during operation. 107

Figure 4.22 The block diagram of the test setup for efficiency comparison of the parallel and single operation. 107

Figure 4.23 The results of the efficiency calculations of the single operation and parallel operation. 109

Figure 4.24 Phase A currents of test and load motor (a) at higher torque (b) at lower torque (c) at lower torque in the switching time domain. 111

LIST OF ABBREVIATIONS

2DEG	Two-dimensional Electron Gas
AC	Alternating Current
ADALINE	Adaptive Linear Neuron
AlGaN	Aluminium Gallium Nitride
AWG	American Wire Gauge
CAN	Controller Area Network
CI	Coupled Inductor
CMI	Common Mode Inductor
CMMD	Common Mode
DC	Direct Current
DCL	Direct Current Leakage
DSP	Digital signal Processor
D-HEMT	Depletion-Mode High Electron Mobility Transistor
eCAP	Enhanced Capture
E-HEMT	Enhancement-Mode High Electron Mobility Transistor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
FOC	Field Oriented Control
FOM	Figure of Merit
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
HB	Half-Bridge
HFCC	High-Frequency Circulating Current

IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
JTAG	Joint Test Action Group
LiDAR	Light Detection and Ranging
LMS	Least Mean Square
MISFET	Metal-Insulator-Semiconductor Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
RF	Radio Frequency
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
TVS	Transient Voltage Suppression
USB	Universal Serial Bus
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
ZSCC	Zero-Sequence Circulating Current
ZSV	Zero-Sequence Voltage

LIST OF SYMBOLS

θ	Rotor Angle
C	Capacitance
i, I	Current
f	Frequency
L	Inductance
Q	Charge
P	Power
R	Resistance
u, V	Voltage
ω	Angular Speed

Subscripts

α	Alpha Reference Frame
β	Beta Reference Frame
a	Leg A Output of the Inverter
b	Leg B Output of the Inverter
c	Leg C Output of the Inverter
d	Quadrature D-axis Reference Frame
ds	Drain to Source
e	Electrical
g	Gate
gd	Gate to Drain
gs	Gate to Source
q	Quadrature Q-axis Reference Frame

sd	Source to Drain
sw	Switching

Superscripts

$*$	Reference

CHAPTER 1

INTRODUCTION

1.1 Motivation and Scope of the Thesis

Permanent magnet synchronous motors (PMSMs) with a coreless structure that is wound on itself rather than on iron, offer benefits such as zero cogging, linear torque characteristics, and low inertia. These features make them a good candidate for applications such as gimbals, aerospace, robotics, unmanned systems, optic stabilizers, etc. where high-precision position control is required [1]. On the other hand, these motors have low inductance and low electrical time constant, which require a high switching frequency to reduce current ripple [2] and to obtain a high current control bandwidth.

For a specific target tracking radar application, due to target maneuvers and the beamwidth of the antenna, the system requirements are specified as a 0.02° tracking error for $5\ Hz$ and 5° sinusoidal position reference. The following equations can be used to calculate the required bandwidth (f_{bw_pos}) of the position controller of the servo drive which feeds a PMSM coupled to an antenna.

$$\begin{aligned}
\theta &= A\sin(wt) \\
\dot{\theta} &= -Aw\cos(wt) \\
\ddot{\theta} &= -Aw^2\sin(wt) \\
\tau &= J\ddot{\theta} \\
k_p &= \tau\Delta\theta \\
f_{bw\_pos} &= \frac{1}{2\pi}\sqrt{\frac{k_p}{J}}
\end{aligned} \tag{1.1}$$

where $A = 5\pi/180\ rad$, $w = 2\pi 5\ rad/s$, the inertia of the antenna $J = 0.005\ kgm^2$.

From these equations, the required torque $\tau = 0.43\ Nm$, the required position controller gain $k_p = 1233.7\ Nm/rad$ and the required position controller bandwidth $f_{bw\_pos} = 79.06\ Hz$ are calculated. To be on the safe side, the target position controller bandwidth is taken as $100\ Hz$. As a general rule of thumb, for a cascade control scheme, the bandwidth of the inner loops should be about ten times higher than the outer loop. So, following this rule of thumb, the required speed and current controller bandwidth are approximately $1\ kHz$ and $10\ kHz$, respectively. In the same manner, the target switching frequency of the servo drive is set to $100\ kHz$ during the thesis.

Two types of inverters, voltage source inverters (VSIs) and current source inverters (CSIs), are considered for the servo drive. VSIs have DC-link capacitors to achieve a constant voltage at the outputs. On the other hand, CSIs have DC-link inductors to deliver a constant current to the loads. The power switches of the VSIs should have bidirectional current conduction capability and block forward voltage [3]. Hence, commercial power switches such as Si MOSFETs and GaN E-HEMTs are suitable for VSIs. The current conduction of the power switches in CSIs is unidirectional, but the power switches should block reverse polarity voltage as well. Thyristors meet the v-i requirements of CSIs, but they are mainly used for medium-high voltage and power applications [4]. The power switches stated above should be used either back to back connected, which introduces complexity to the gate driver, or in series with a diode. In both cases, CSIs need six additional power switches, which increases the conduction losses and also the size of the inverter. The DC-link inductor of the CSIs helps to limit the current when the motor phases are short-circuited, but it negatively affects the dynamic response of the system [5]. With the help of output filter capacitors, CSIs have nearly sinusoidal voltages at the outputs. This is an advantage for the EMI problem and also reduces over-voltage problems on the terminals of the motor compared with the VSI case [6]. However, since the servo drive is supplied from a low voltage battery, typically $24V$, in the target tracking radar application, there will not be such a voltage at the terminals of the motor to cause the insulation to wear off, even in the case of VSI. Based on the comparisons above, in the thesis, VSI is preferred for the servo drive due to its lower size and higher dynamic response, and it is more appropriate for low-voltage and low-power applications.

In the application, the target switching frequency of the servo drive was set to 100 kHz. But, as the switching frequency increases, the effects of the time-related terms in the nonlinearity in VSIs also increase. The key causes of output voltage distortions in VSIs are nonlinearities such as

- dead time,
- switching time,
- delay time,
- voltage drops on the power switches,
- parasitic capacitances.

Low-order harmonics in the output current are caused by these distortions, which raise core losses and cause torque ripples [7–10]. Due to the nonlinearities in VSI, control efficiency and system stability degrade significantly in low-speed applications with low-inductance motors, particularly when the system operates in the low-torque region. In Fig. 1.1, the problem is also depicted as a block diagram.

Fig. 1.2a shows an IGBT-based VSI driving a PMSM and the impact of the dead time, which is one of the nonlinearity factors of the VSIs, on the phase current and the quadrature currents is shown in Fig. 1.2b ([11]). The dead time is compensated by a least-mean-square algorithm ([11]) and the compensation results are given in Fig. 1.2c.

The effects of these nonlinearities on the phase current and current control of the Si MOSFET-based VSI are studied in this work using a coreless PMSM. The influence of the nonlinearities on the current control bandwidth is investigated. This effect should be considered before tuning linear controllers to achieve high-bandwidth current control in zero-crossing regions. In this thesis, a GaN E-HEMT-based VSI is suggested as a solution to this issue. Following that, advancements in the current control mechanism are illustrated by analyzing experimental findings obtained with GaN E-HEMT and Si MOSFET-based VSIs. It is shown that GaN E-HEMT-based VSI is a better option for applications requiring high bandwidth control.

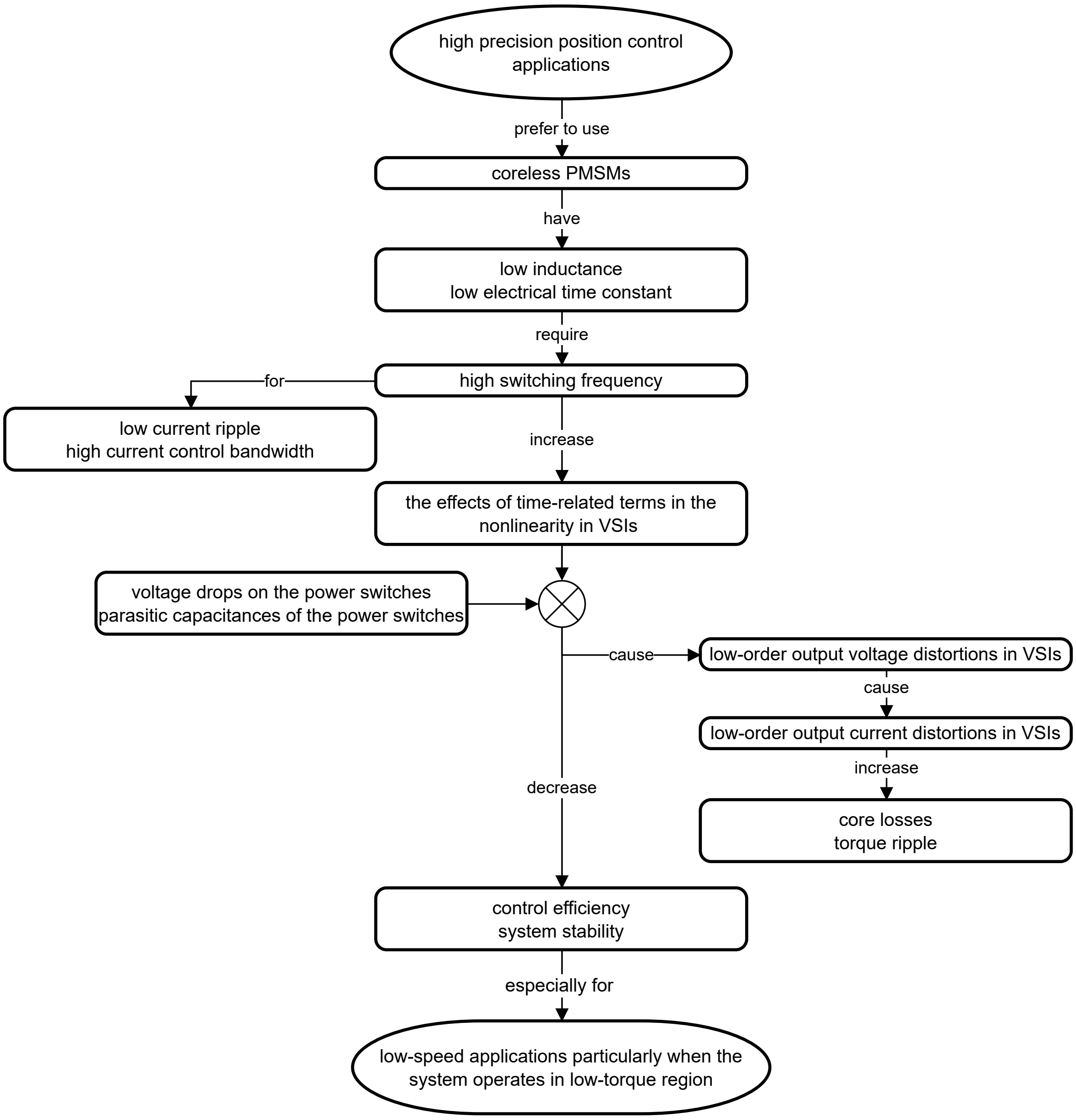
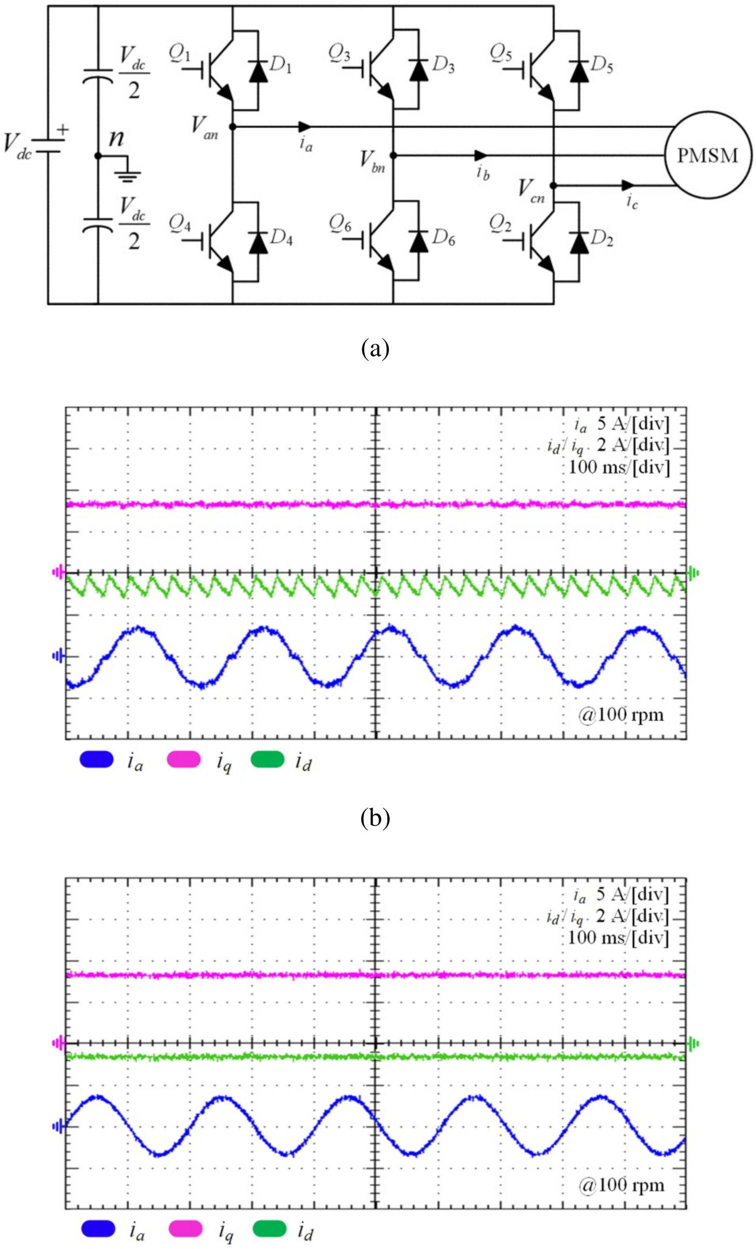

high precision position control applications
prefer to use
coreless PMSMs
have
low inductance
low electrical time constant
require
high switching frequency
for
low current ripple
high current control bandwidth
increase
the effects of time-related terms in the nonlinearity in VSIs
voltage drops on the power switches
parasitic capacitances of the power switches
cause
low-order output voltage distortions in VSIs
cause
low-order output current distortions in VSIs
increase
core losses
torque ripple
decrease
control efficiency
system stability
especially for
low-speed applications particularly when the system operates in low-torque region

Figure 1.1: The block diagram of the nonlinearity problem.

Considering the results of this work, a GaN E-HEMT VSI-based servo drive is designed to replace its Si MOSFET VSI-based counterpart. The size of the designed servo drive is about half of the previous one. This and the fast switching capability of the GaN E-HEMT makes it possible to use two parallel servo drives instead of one to increase redundancy, as shown in Fig. 1.3.

Using parallel-connected servo drives has many benefits [12], including increased torque (hence power output) capacity, reliability, redundancy, and modularity. Smaller variations in the system clocks of the individual microcontrollers, asynchronous PWM carrier signals, and hardware differences, on the other hand, will cause the output



(a)

(b)

(c)

Figure 1.2: (a) IGBT-based VSI to drive a PMSM. (b) Phase A current (i_a) and quadrature axis currents (i_d, i_q) without dead time compensation (c) with dead time compensation (Figures are taken from: [11])

voltages of the parallel modules to be non-identical, resulting in circulating currents between inverters [13], [14]. These circulating currents restrict parallel operation, add extra power dissipation, disrupt power transfer, and reduce control efficiency [15–17].

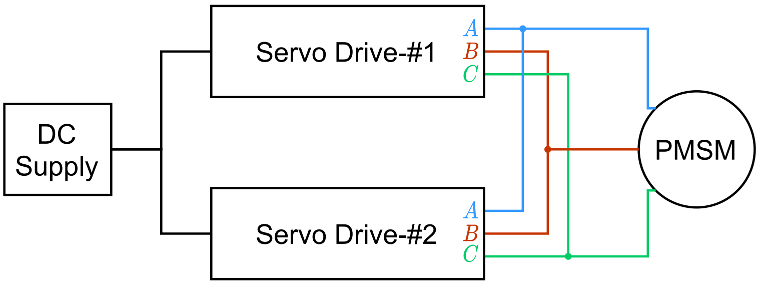


Figure 1.3: The simplified block diagram of two servo drives connected in parallel.

To better visualize, the structure of the two parallel-connected inverters is shown in Fig. 1.4 ([18]). Fig. 1.5a ([18]) depicts the circulating current between inverters caused by asynchronous PWM carriers. The circulating current is decreased using a high-frequency voltage compensation technique, as seen in Fig. 1.5b ([18]).

Separated DC supplies, extra inductors at the outputs, PWM techniques, changed control approaches, and other strategies have been suggested in the literature to minimize circulating currents. In this study, a fault-tolerant parallel-connected GaN E-HEMT VSI-based servo drive system, which removes the requirement for extra inductors and separate DC supplies while allowing the use of a conventional PI current control and a standard SVPWM method is presented. By synchronizing the carrier signals, the circulating current generated by the phase mismatch between carrier signals of the parallel-connected inverters is removed. By increasing the switching frequency without adding extra inductors to the output of the inverters, the circulating current caused by inherent hardware variations is reduced. Up to six servo drives are connected in parallel and tested under various situations using a $24V$ PMSM to investigate the performance of the proposed approach. The results demonstrate that parallel operation not only enhances the system's torque capacity but also its modularity, flexibility, reliability, and redundancy.

1.2 The Outline of the Thesis

Chapter 2 presents the background information on the nonlinear components in the Si MOSFET-based VSI-fed PMSM drive. Next, the effect of changing the switching frequency on nonlinearities is investigated using an i_d current controller. The impact

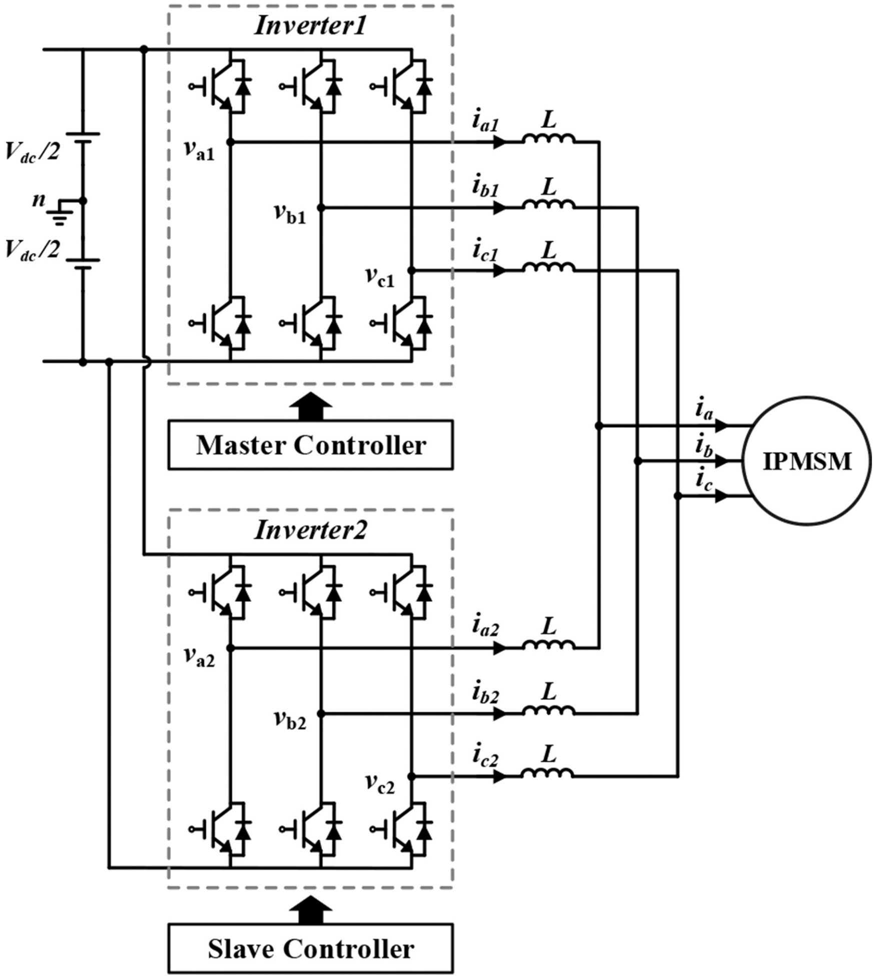
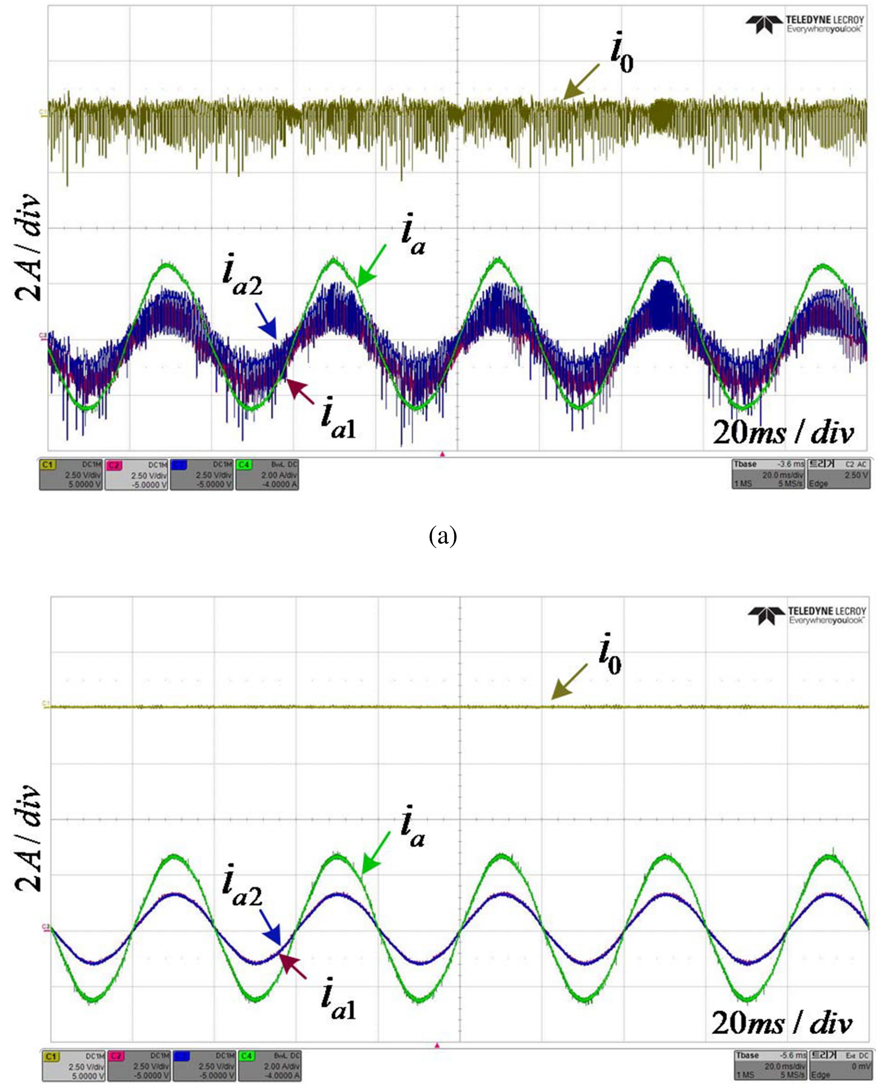

Inverter1
$V_{dc}/2$
n
$V_{dc}/2$
v_{a1}
v_{b1}
v_{c1}
i_{a1}
L
i_{b1}
L
i_{c1}
L
Master Controller
i_a
i_b
i_c
IPMSM
Inverter2
v_{a2}
v_{b2}
v_{c2}
i_{a2}
L
i_{b2}
L
i_{c2}
L
Slave Controller

Figure 1.4: The structure of the two parallel-connected inverters (Figure is taken from: [18]).

of the change in apparent resistance along the nonlinear region on the stability of cascaded control loops is studied. The WBG GaN E-HEMT based VSI is used to analyze the influence of switching frequency and dead time on nonlinearity. For the GaN E-HEMT based VSI-fed PMSM drive with various dead time values, the bandwidth measurements of the i_d and i_q control loops are provided. Finally, the power losses and costs of GaN E-HEMTs and Si MOSFETs are determined and compared with an application.

In Chapter 3, first, a basic overview of GaN E-HEMTs is provided. The significance of the layout as well as the problems of high dV/dt and high switching frequency are highlighted. Then, some details on a three-phase, two-level GaN E-HEMT VSI-based



(a)

(b)

Figure 1.5: Phase A currents (i_{a1}, i_{a2}) of each inverter and the high-frequency circulating current (i_0) (a) without compensation (b) with compensation (Figures are taken from: [18])

servo drive design are provided. The servo drive's card compositions and functionalities are discussed, and finally, the servo drive's load and emission tests are demonstrated.

In Chapter 4, the circulating current path produced by asynchronous carrier signals is examined case by case, and the circulating current simulation outputs are discussed. Following that, the problem of clock differences across separate microcontrollers is shown, and a solution is provided. The suggested parallel servo drive system's functioning is explained, and finally, the results of dynamic performances under various situations are demonstrated.

In Chapter 5, the conclusion and recommendations for future work are provided.

CHAPTER 2

NONLINEARITIES FOR SI MOSFET AND GAN E-HEMT BASED VSIS

2.1 Introduction

In industrial applications, PWM VSIs are commonly used to drive PMSMs. The nonlinearites in VSI create low-order output voltage distortions. The effect of these distortions on the output voltage depends on the switching frequency, modulation index, and output frequency. These voltage distortions cause low-order harmonic components in the inverter's output current and distort the current waveform, particularly in the current zero-crossing regions.This reduces power efficiency and increases torque ripple [7–10]. The nonlinearities in VSI have also an impact on the control efficiency of low-speed applications, especially when the system is operating in the low-torque zone. For gimbal applications, for example, when disturbances such as g-force are not present, low torque with a speed approaching zero is required during the tracking of a distant object. A high-performance PMSM VSI-fed drive can be accomplished by utilizing high current bandwidth regulation and the minimization of VSI nonlinearity effects.

In the literature, various nonlinearity compensation methods for PWM VSIs are discussed, with an emphasis on dead time compensation. Compensation techniques can be classified as either hardware-based which needs additional circuits or software-based.

A voltage measurement circuit is designed in [19] to calculate the real pole voltage by using the time measurement module (eCAP) of the DSP. From this information, the average output voltage is calculated for every switching cycle, and it is compared to the reference voltage. The difference is applied in the next loop to compensate for the effect of dead time. In [20], the phase voltages are scaled using hardware and given to the controller as an input to calculate the actual duty cycles. The difference between the actual and desired duty cycle is calculated and utilized as an input to the dead time distortion shaping algorithm, which compensates for both the dead time effect and the parasitic capacitance effect. A diode-conduction detector is designed in [21] to identify the polarity of the phase current by measuring the diode voltage and comparing it to a reference. When the phase current is flowing out of the leg, only the top switch is utilized, and the current is freewheeling from the diode of the bottom switch. It is vice versa when the phase current is flowing in. The dead time issue is eliminated since the technique does not require dead time to function. An FPGA is used in [22]. During the zero voltage states, the phase currents of the inverter are oversampled and the phase current slopes are calculated by using the linear least mean squares regression. With these inputs, the FPGA predicts the phase currents of the next switching cycle. A look-up table that is constructed off-line holds needed compensation times according to predicted currents, and the duty cycles of switches are updated to compensate for the dead time effect.

Software-based methods can be categorized by

- monitoring sixth harmonics and multiples in quadrature axis currents,
- using a wide bandwidth current controller,
- compensating for average voltage error in each switching period.

Because dead time generates sixth harmonics and multiples in quadrature axis currents in the d-q frame, a revised repetitive controller, which is preferred for rejecting periodic signals, is used in [23]. The current loop's closed-loop gain is increased at those frequencies. The controller is modified by changing the periodicity as a function of the PMSM's angular speed and it is added in cascade to the PI current controller. The quadrature d-q frame real voltages are computed using the PMSM model and measured phase currents in [24]. The reference d-q frame voltages are then calculated using reference quadrature currents while assuming no dead time. The difference is then added to the reference voltages to remove the dead time effect. An adaptive single-frequency noise canceller filter is designed by using the least mean square (LMS) algorithm to reduce the sixth harmonic of the quadrature currents in the d-q frame for FOC and V/f control in [11] and [25], respectively. The cyclical disturbances in the d-q reference frame are compensated by the iterative learning strategy in [26]. The learning patterns are constructed off-line for a specific operating output frequency and stored in the memory to be used later for that operating frequency. By using a look-up table that shows a relation between the rotor angle and distorted voltage in the d-q reference frame, the disturbance voltages are estimated in the d-q reference frame by an adaptive linear neuron-based (ADALINE) algorithm [27]. In [28], based on the harmonic analysis and the Extended Kalman filter algorithm, the magnitude of the voltage error is estimated by using the model of the PMSM in the quadrature axis d-q frame. The polarity detection is based on estimated quadrature currents during the zero crossing regions.

The performance of wide-bandwidth current controllers with an experiment is examined in [29] to reject disturbances induced by inverter nonlinearities. Complex PI, symmetrical optimum, and pole placement current controllers are designed for a PMSM and the symmetrical optimum current controller provides the best results among them.

In [30], a graphical approach is utilized to compensate for average voltage errors in each switching period. Voltage drops, turn-on and off times of the power switches, and dead time parameters of the inverter are measured offline and used in the voltage compensation algorithm. To find the direction of the phase currents during zero-crossing regions, a current observer is designed by using a discrete model of a PMSM. The reference voltages are updated for each switching period according to the voltage compensation method.

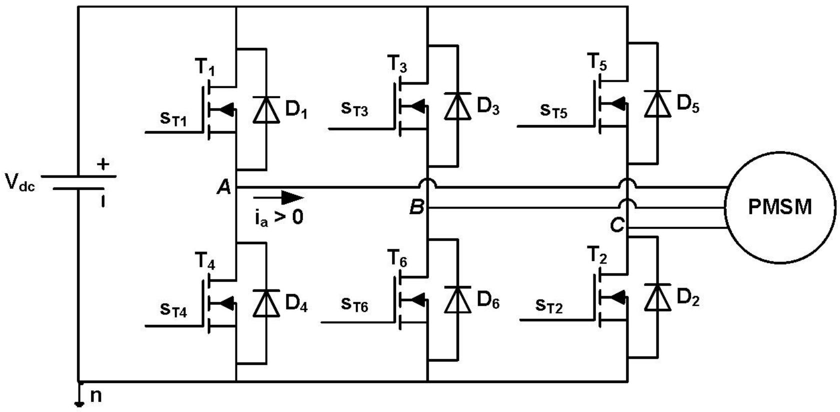
The purpose of this chapter is to examine the effects of nonlinearities in the zero-crossing regions of the d axis quadrature current of Si MOSFET and GaN E-HEMT VSI-based servo drives. In the d-axis, an offline compensation function for Si MOSFET VSI-based servo drive is designed to reduce nonlinearities. But it is difficult to obtain a valid compensation function for each input voltage, for all motor speeds, and for all environmental conditions. However, by using the GaN E-HEMT VSI-based servo drive, the nonlinearities in the zero-crossing regions of the d axis quadrature current are reduced without any compensation method. How nonlinearities influence current control bandwidth is also demonstrated in the chapter.

2.2 Nonlinearity Analysis of SI MOSFET-Based VSI

In this part, the nonlinearities in a Si MOSFET-based VSI are analyzed by comparing ideal and actual phase output voltages. The voltage errors on the phases are transformed first to the α-β frame by the Clarke transform, then to the d-q frame by the Park transform. Then Fourier analysis is performed to analyze harmonics of the phase output voltage distortions caused by nonlinearities in the VSI.

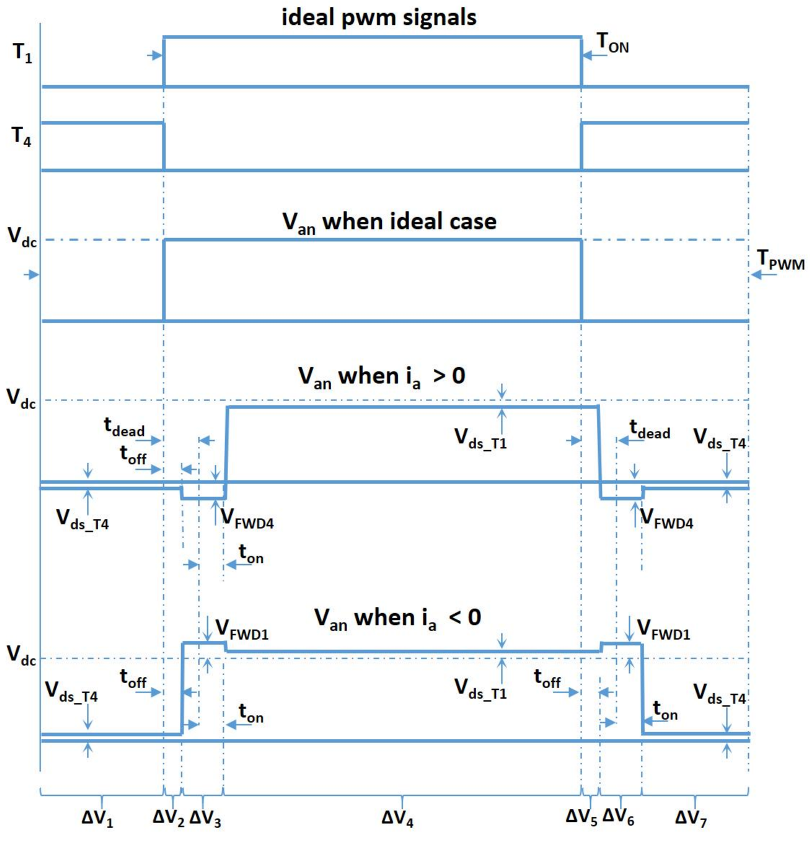
In an ideal case, a switch is assumed to have a zero switching time and a zero voltage drop while in conduction. Fig. 2.1 depicts a standard Si MOSFET-based VSI-fed PMSM. The top row of Fig.2.2 shows the gate signals of the leg A, T_1, and T_4 Si MOSFETs, and the second row of the figure shows the ideal midpoint voltage, V_{an}. However, voltage drops occur on power switches when they are in conduction and they have finite turn-on and off times. Their gate drives also have turn-on and turn-off propagation delay times. To prevent the cross-conduction of the leg of the VSI, a dead time is inserted into the corresponding PWM signals of the upper and lower switches. The third and fourth rows of Fig.2.2 show these situations.
Where;
$\mathrm{t}_{\mathrm{dead}}$: the dead time
t_{on} : turn on delay + rise time of the gate drive/Si MOSFET
$\mathrm{t}_{\mathrm{off}}$: turn off delay + fall time of the gate drive/Si MOSFET
V_{ds}: drain to source voltage of the Si MOSFET
$\mathrm{V}_{\mathrm{FWD}}$: voltage of the free wheeling diode
T_{on} : ON time of the upper Si MOSFET
$\mathrm{T}_{\mathrm{PWM}}$: time period of the PWM

The forms of the falling and rising edges of the leg voltage are affected by the dead-time interval [31]. Furthermore, because of the output capacitance of the power device, the rise and fall periods of the leg voltage will vary depending on the phase



T1
T3
T5
ST1
D1
ST3
D3
ST5
D5
Vdc
+
A
ia > 0
B
C
PMSM
T4
T6
T2
ST4
D4
ST6
D6
ST2
D2
n

Figure 2.1: Si MOSFET-based VSI PMSM drive block schema



ideal pwm signals
T1
TON
T4
Vdc
Van when ideal case
TPWM
Vdc
Van when ia > 0
tdead
toff
Vds_T1
tdead
Vds_T4
Vds_T4
VFWD4
VFWD4
ton
Van when ia < 0
VFWD1
VFWD1
Vdc
Vds_T4
toff
Vds_T1
toff
Vds_T4
ton
ton
ΔV1
ΔV2
ΔV3
ΔV4
ΔV5
ΔV6
ΔV7

Figure 2.2: Gate signals and leg A output voltages of the SI MOSFET-based VSI

current direction and magnitude [32]. For the sake of convenience, the leg voltage transition is considered instantaneous in this study. All transistors in VSI are supposed to have identical properties, and all inverter legs are considered to be symmetrical. This allows the inverter to be analyzed for just one leg. The phase current is also assumed to not alter the sign during the study time.

During the dead time interval, the current flows through the freewheeling diode D_4 when the phase current is greater than zero and through the freewheeling diode D_1 when the phase current is less than zero. Because the output voltage is affected by the direction of the current, an uncontrollable zone is introduced.

The total voltage difference ΔV_{an} between the ideal V_{an} and the actual V_{an} can be determined as follows:
when $i_a > 0$:

$$\begin{aligned}
\Delta V_1 + \Delta V_7 &= -(T_{PWM} - T_{on} - t_{dead} - t_{on})(V_{ds}) \\
\Delta V_2 &= -(t_{off})(V_{dc} + V_{ds}) \\
\Delta V_3 &= -(t_{dead} - t_{off} + t_{on})(V_{FWD} + V_{dc}) \\
\Delta V_4 &= -(T_{on} - t_{dead} - t_{on})(V_{ds}) \\
\Delta V_5 &= (t_{off})(V_{dc} - V_{ds}) \\
\Delta V_6 &= -(t_{dead} - t_{off} + t_{on})(V_{FWD}) \\
\Delta V_{i_a>0} &= \Delta V_1 + \Delta V_2 + \Delta V_3 + \Delta V_4 + \Delta V_5 + \Delta V_6 + \Delta V_7
\end{aligned} \tag{2.1}$$

where ΔV_1 to ΔV_7 are depicted in Fig. 2.2.

$$\begin{aligned}
\Delta V_{i_a>0} = V_{ds}(-T_{PWM} + 2t_{dead} + 2t_{on} - 2t_{off}) \\
+ V_{dc}(-t_{dead} - t_{on} + t_{off}) \\
+ V_{FWD}(-2t_{dead} - 2t_{on} + 2t_{off})
\end{aligned} \tag{2.2}$$

The following formula can be used to measure the voltage error ΔV over a period:

$$\Delta V = \frac{\Delta V_{i_a>0}}{T_{PWM}} \tag{2.3}$$

when $i_a < 0$:

$$\begin{aligned}
\Delta V_1 + \Delta V_7 &= (T_{PWM} - T_{on} - t_{dead} - t_{on})(V_{ds}) \\
\Delta V_2 &= -(t_{off})(V_{dc} - V_{ds}) \\
\Delta V_3 &= (t_{dead} - t_{off} + t_{on})(V_{FWD}) \\
\Delta V_4 &= (T_{on} - t_{dead} - t_{on})(V_{ds}) \\
\Delta V_5 &= (t_{off})(V_{dc} + V_{ds}) \\
\Delta V_6 &= (t_{dead} - t_{off} + t_{on})(V_{FWD} + V_{dc}) \\
\Delta V_{i_a<0} &= \Delta V_1 + \Delta V_2 + \Delta V_3 + \Delta V_4 + \Delta V_5 \\
&\quad + \Delta V_6 + \Delta V_7
\end{aligned} \tag{2.4}$$

$$\Delta V_{i_a<0} = -(\Delta V_{i_a>0}) \tag{2.5}$$

After calculating the volt-second area differences $\Delta V_{i_a>0}$ when $i_a > 0$ and $\Delta V_{i_a<0}$ when $i_a < 0$, the overall voltage error ΔV_{an} can be expressed as follows:

$$sign(i_a) = \begin{cases} -1, & \text{if } i_a < 0 \\ 1, & \text{if } i_a > 0 \end{cases} \tag{2.6}$$

$$\Delta V_{an} = sign(i_a)\Delta V \tag{2.7}$$

where ΔV is defined in equation (2.3).

Assuming the PMSM is Y-connected, the overall voltage errors of the legs can be stated as follows [11]. The associated voltage errors are illustrated in Fig. 2.3 to better visualize them by using ideal phase currents where I_p is the peak phase current value.

$$\begin{bmatrix} \Delta V_{an} \\ \Delta V_{bn} \\ \Delta V_{cn} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} sign(i_a)\Delta V \\ sign(i_b)\Delta V \\ sign(i_c)\Delta V \end{bmatrix} \tag{2.8}$$

Through the use of transforms by Clarke and Fourier [33], phase voltage errors in the α-β reference frame can be given as follows and it is illustrated in Fig. 2.4:

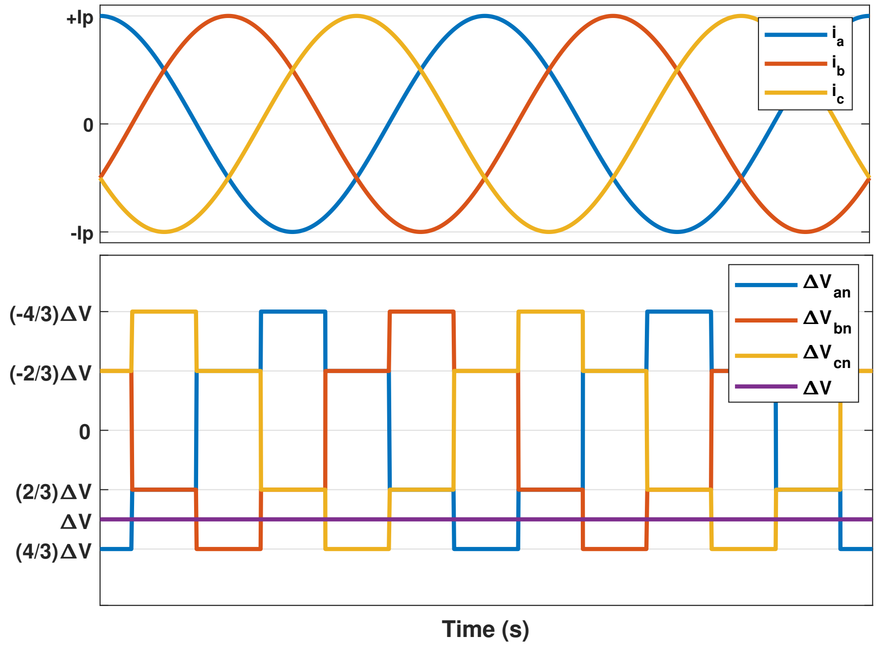


Figure 2.3: Voltage errors in the legs as a result of VSI nonlinearities.

$$\begin{bmatrix} \Delta u_\alpha \\ \Delta u_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ 0 & \frac{2}{\sqrt{3}} & \frac{-2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \Delta V_{an} \\ \Delta V_{bn} \\ \Delta V_{cn} \end{bmatrix} = \frac{4}{\pi}\Delta V \begin{bmatrix} \sin \dot{\theta}_e t + \sum\limits_{k=6n-1}^{\infty} \frac{\sin k\dot{\theta}_e t}{k} + \sum\limits_{k=6n+1}^{\infty} \frac{\sin k\dot{\theta}_e t}{k} \\ -\cos \dot{\theta}_e t + \sum\limits_{k=6n-1}^{\infty} \frac{\cos k\dot{\theta}_e t}{k} - \sum\limits_{k=6n+1}^{\infty} \frac{\cos k\dot{\theta}_e t}{k} \end{bmatrix} \tag{2.9}$$

where $n = 1, 2, 3...$ and $\dot{\theta}_e$ is the electrical angular speed.

The following are the synchronous rotating d–q frame voltage errors after implementing the Park transform and are depicted in Fig. 2.5.

$$\begin{bmatrix} \Delta u_d \\ \Delta u_q \end{bmatrix} = \begin{bmatrix} \cos \theta_e & \sin \theta_e \\ -\sin \theta_e & \cos \theta_e \end{bmatrix} \begin{bmatrix} \Delta u_\alpha \\ \Delta u_\beta \end{bmatrix} = \frac{4}{\pi}\Delta V \begin{bmatrix} \frac{12}{35} \sin 6\dot{\theta}_e t + \frac{24}{143} \sin 12\dot{\theta}_e t + ... \\ -1 + \frac{2}{35} \cos 6\dot{\theta}_e t - \frac{2}{143} \cos 12\dot{\theta}_e t + ... \end{bmatrix} \tag{2.10}$$

The current distortion in the d–q reference frame can then be determined as:

$$\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} = \frac{4}{\pi}\Delta V \begin{bmatrix} \frac{12}{35Z_6} \sin(6\dot{\theta}_e t - \phi_6) + ... \\ \frac{-1}{R_s} + \frac{2}{35Z_6} \cos(6\dot{\theta}_e t - \phi_6) + ... \end{bmatrix} \tag{2.11}$$

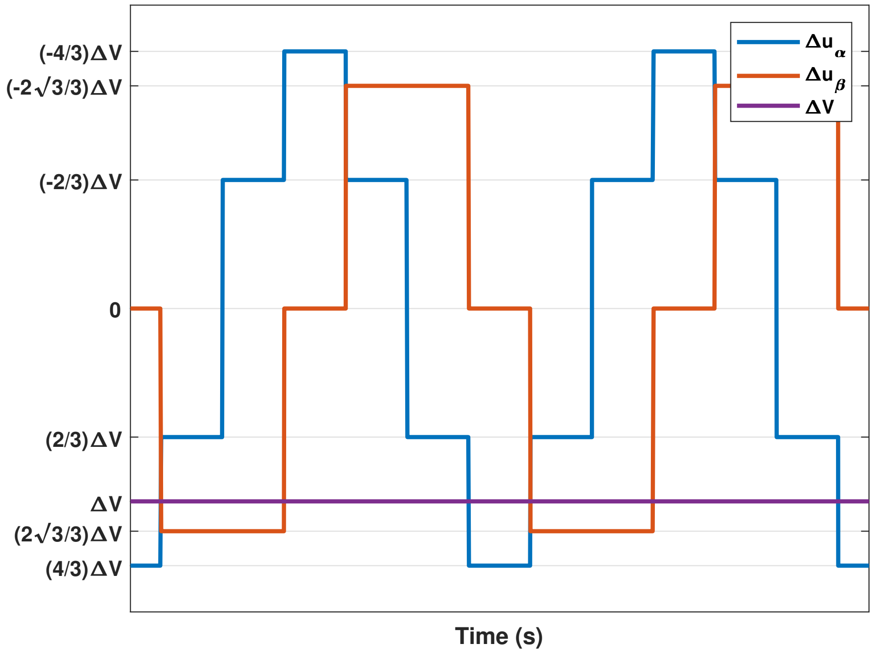


Figure 2.4: Voltage errors in α-β reference frame as a result of VSI nonlinearities.

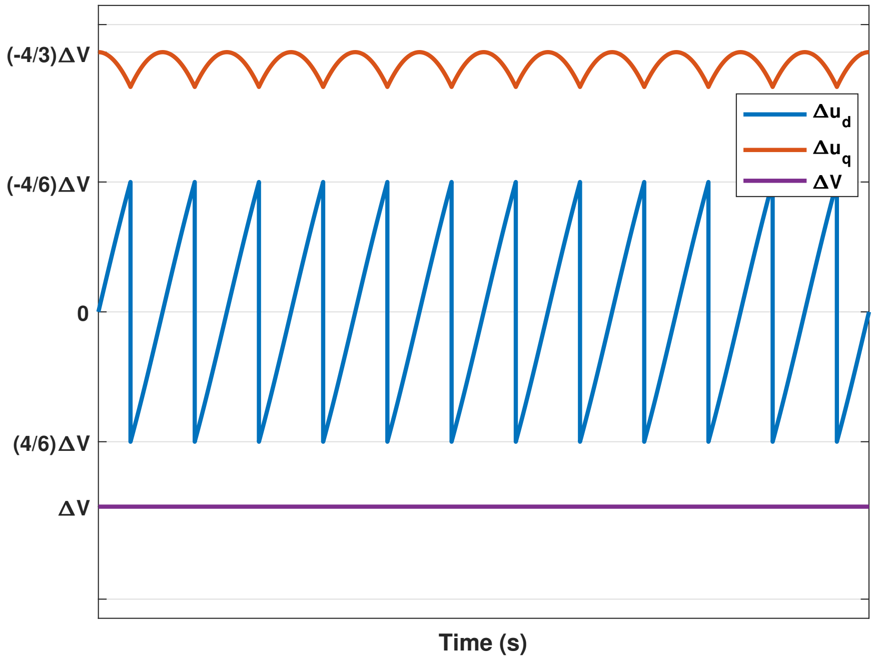


Figure 2.5: Voltage errors in d-q reference frame as a result of VSI nonlinearities.

L_s denotes stator inductance, R_s denotes stator resistance, $m = 6, 12, 18....$ Z_m and

ϕ_m are given as:

$$Z_m = \sqrt{R_s^2 + (m\dot{\theta}_e L_s)^2}$$
$$\phi_m = \tan^{-1} \frac{m\dot{\theta}_e L_s}{R_s}$$

The output voltage disturbances introduced by nonlinearities contribute 5^{th} and 7^{th} harmonics to the phase current as well as to the α-β reference frame currents in the stationary reference frame, as shown by Equations (2.9) to (2.11). By applying the Park transform, it is obtained that the phase voltage distortions also introduce the 6^{th} harmonic and its multiples of the fundamental output frequency on the d and q currents. This condition creates ripples in the phase currents as well as the d–q currents. The resulting torque pulsations limit the performance of the controller.

2.3 Experimental Study on SI MOSFET-Based VSI

In this part, nonlinearities in VSI are investigated experimentally by using a Si MOSFET-based VSI.

The Si MOSFET-based 3-phase, 2-level VSI-based servo motor drive is used to control a coreless type low inductance PMSM. The servo motor drive is comprised of TrenchFET Si MOSFETs (SUM90N10), a 3-phase gate driver (IRS2336), and a floating-point microcontroller (F28335). By considering the dynamic electrical time parameters of the gate driver and Si MOSFETs in the VSI, dead time is set to 1 μs during the experiments.

Table 2.1 lists the motor parameters, and Fig. 2.6 depicts the experimental setup.

2.3.1 Observation of Current Harmonics as a Result of Nonlinear Effects

To observe the harmonics in the phase current and the d-q reference frame currents that are caused by the nonlinearities of the VSI, the motor is driven at a speed of 5 Hz mechanical speed. To get rid of the audible noise, the recommended switching frequency (f_{sw}) is given as a minimum of 20 kHz [34]. Therefore, the switching

Table 2.1: PMSM Parameters

Parameters	**Value**
Rated voltage	24 V
Rated torque	63.3 mNm
Rated speed	16700 rpm
Rated current	5.45 A
Torque constant	12.8 mNm/A
Inductance (l-l)	29.5 μH
Resistance (l-l)	0.248 Ω
Number of pole pairs	2
Rated power	100 W

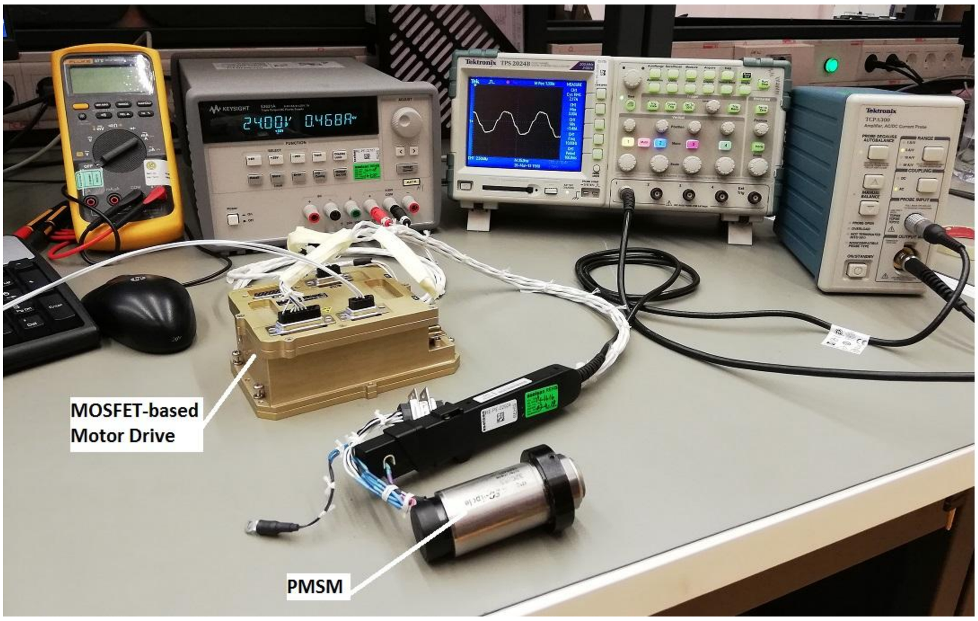


Figure 2.6: Experimental setup with Si MOSFET-based VSI.

frequency of the VSI is set to 20 kHz, which is also sufficient to observe these harmonics.

As seen in Fig. 2.7, nonlinear effects primarily generate 5^{th} and 7^{th} harmonics in phase currents, as well as 6^{th} and its multiple harmonics in d-q reference frame currents.

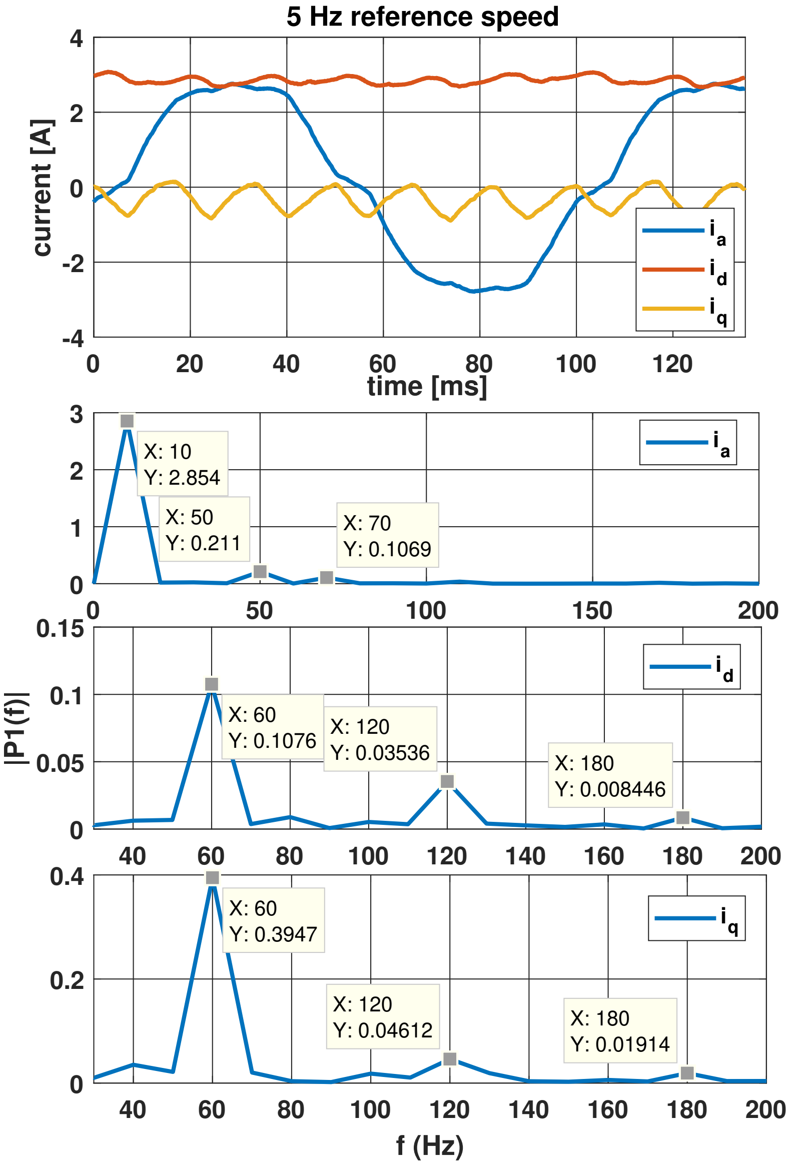


Figure 2.7: Phase current i_a, d-q reference frame current i_d and i_q and their frequency spectrums in open-loop control.

Phase currents are measured using a power analyzer to see how the fundamental output frequency f_o value affects phase current distortion. The phase voltage error ΔV occurs $\frac{h}{2}$ times during the half-cycle of output voltage, where $h = \frac{f_{sw}}{f_o}$ and the difference can be calculated as $A_{diff} = h\Delta V$. Therefore, as f_o is increased, the distortion of the phase voltage decreases, which in turn reduces the distortion of the phase current. Table II shows the percentages of harmonic distortion values of the measured phase currents when the PMSM is operating at $5\ Hz$ and $20\ Hz$ mechanical speeds, that is, 10 Hz and 40 Hz electrical speeds, respectively.

Table 2.2: Phase Current Harmonic Distortions [%] at 10 Hz and 40 Hz Electrical Reference Speed at No Load

Current Harmonics	**@10 Hz**	**@40 Hz**
5^{th}	7.42	4.67
7^{th}	3.75	2.06
11^{th}	1.27	0.17
13^{th}	0.04	0.70
17^{th}	0.57	1.02
19^{th}	0.21	0.60
THD_I	8.52	5.43

2.3.2 Relationships Between Switching Frequency and Nonlinearities

In this part, by using the u_d-i_d graph, the effect of the switching frequency on the nonlinearity is investigated. This part also demonstrates how the current controller bandwidth changes according to the operating region in the u_d-i_d graph.

The d-q reference frame voltage equations of the PMSM are indicated in (2.12). where;

$\mathrm{u_d}$: d axis voltage

$\mathrm{u_q}$: q axis voltage

$\mathrm{L_d}$: d axis inductance

$\mathrm{L_q}$: q axis inductance

λ_f : the permanent magnet flux linkage

ρ : the derivative operator

Note that, for surface mount cylindrical rotor PMSM, L_d and L_q are identical and denoted as L_s.

$$\begin{bmatrix} u_q \\ u_d \end{bmatrix} = \begin{bmatrix} R_s + L_q\rho & \dot{\theta}_e L_d \\ -\dot{\theta}_e L_q & R_s + L_d\rho \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} \dot{\theta}_e\lambda_f \\ 0 \end{bmatrix} \tag{2.12}$$

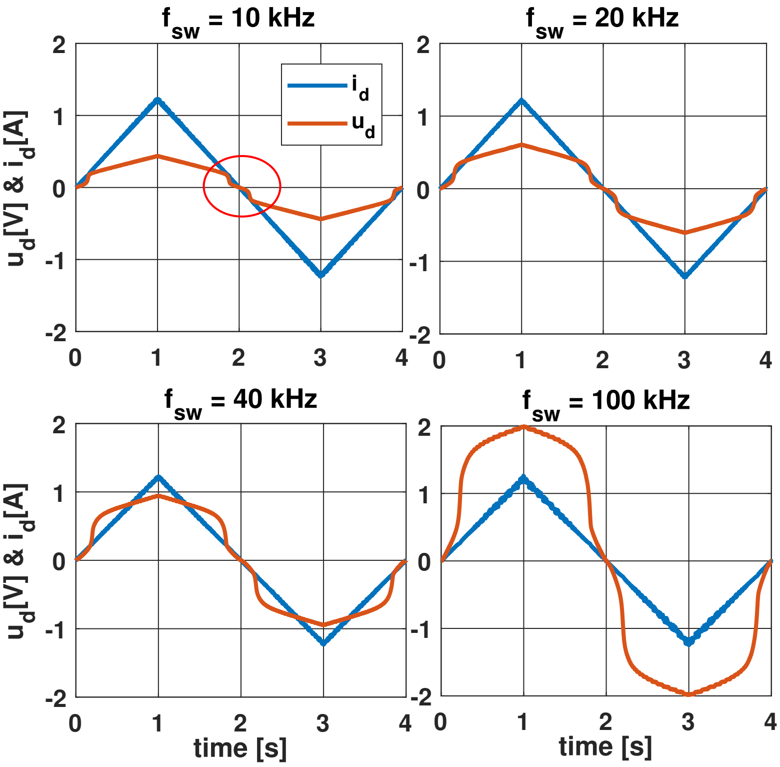


Figure 2.8: i_d current and u_d voltage, Si MOSFET-based VSI at $f_{sw} = 10\ kHz$ to $100\ kHz$.

The standard PI current control approach is used to investigate the influence of switching frequency on nonlinearity. To reach zero speed, the i_q current reference is set to 0 to minimize the influence of the back electromotive force (emf) voltage ($\dot{\theta}_e \lambda_f$) part. Furthermore, to mitigate the influence of the inductance L_s on the output, the i_d current reference is varied slowly enough that the $L_d \rho i_d$ term is close to zero.

In the ideal scenario, the necessary u_d voltage equals $R_s i_d$ for a given i_d current. However, this equation is not linear because of the nonlinearity of the system, which degrades the performance and reliability of the control system. Nonlinearity is particularly evident in zero-crossing regions of the i_d current and is exacerbated by increasing the switching frequency, as depicted in Fig. 2.8 and Fig. 2.9. It should be noted that the experimental findings presented in the figures indicate the combined effect from the microcontroller's PWM outputs to the microcontroller's current readings, which includes parasitic output capacitance, turn on/off time, delay time, dead time, voltage drops on different modules, and so on.

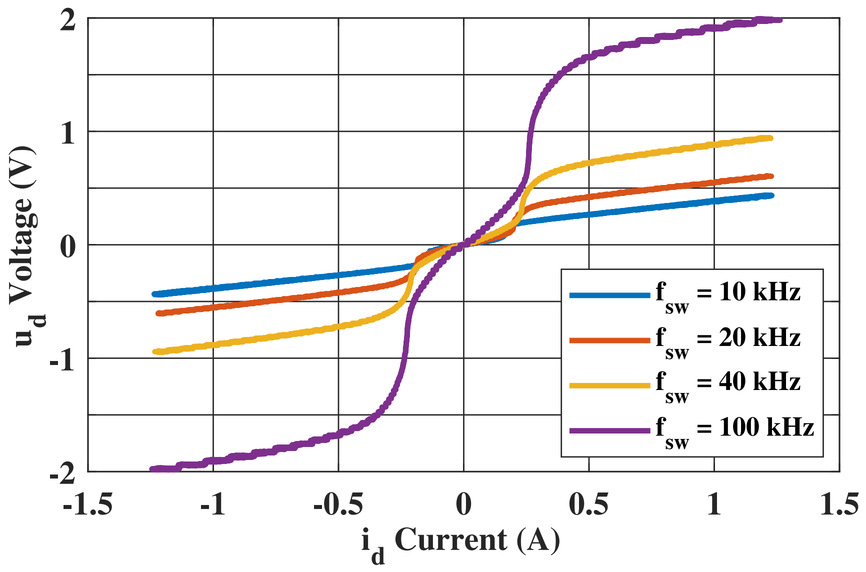


Figure 2.9: u_d voltage versus i_d current, Si MOSFET-based VSI at $f_{sw} = 10\ kHz$ to $100\ kHz$.

To evaluate the influence of nonlinearity, a chirp signal ranging from $10\ Hz$ to $250\ Hz$ is used as the i_d reference at $f_{sw} = 100\ kHz$. While the current controller's bandwidth is built to be about $1\ kHz$, as presented in Fig. 2.10a, it cannot follow the reference signal at frequencies greater than $30\ Hz$. Then, on the i_d reference chirp signal, an offset current is applied such that u_d versus i_d acts as a linear system in this region (Fig. 2.10b). In this linear region, the i_d current can follow the reference. Following that, an offset current is applied to the i_d reference chirp signal, causing the device to enter the nonlinear region (Fig. 2.10c). As can be seen, the reference signal cannot be followed in this region. It can be concluded that the controller bandwidth changes according to the operating region in the u_d-i_d graph. The bode diagram illustrates this issue as well, which can be seen in Fig. 2.11.

The same experimental setup and procedures are performed with varying speeds when f_{sw} is set to $100\ kHz$ to investigate the influence of speed on the nonlinearity in the u_d-i_d graph. As shown in Fig. 2.12, as the speed increases, the distortion of the curves reduces at the zero crossing area of the u_d-i_d graph, and the u_d-i_d curve begins to behave as a piece-wise linear line. This is to be predicted because current harmonic distortions reduce as speed increases, as seen in Table 2.2. The DC offset (i.e. $-\dot{\theta}_e L_q i_q$) in (2.12) is subtracted from the u_d voltage to get the curves to cross the

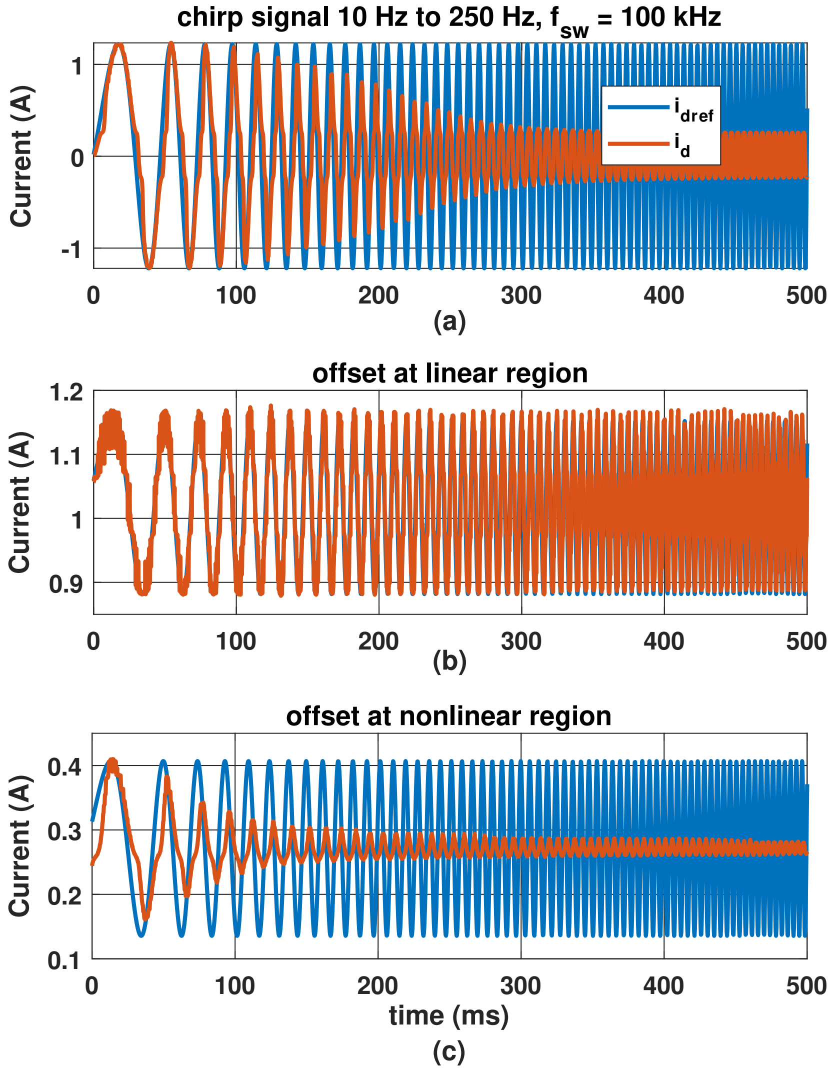


Figure 2.10: Closed-loop time domain response of i_{dref} and measured i_d current, at $f_{sw} = 100\ kHz$, Si MOSFET-based VSI. (a) without any offset (b) offset at linear region (c) offset at nonlinear region

origin of Fig. 2.12.

According to industry experience, when $L_q = L_d$, current controllers in motor control applications are better tuned by using the d axis, since tuning in the q axis can result in problems due to back-emf effects acting as disturbance factors. The motor shaft may be locked or rotated by a second motor at constant speed in order to tune the current controllers in the q axis. However, because the used motor has identical d and q axis parameters, tuning the controller in the q axis yields identical controller parameters. Since the controller parameters are obtained by where the tuning occurs

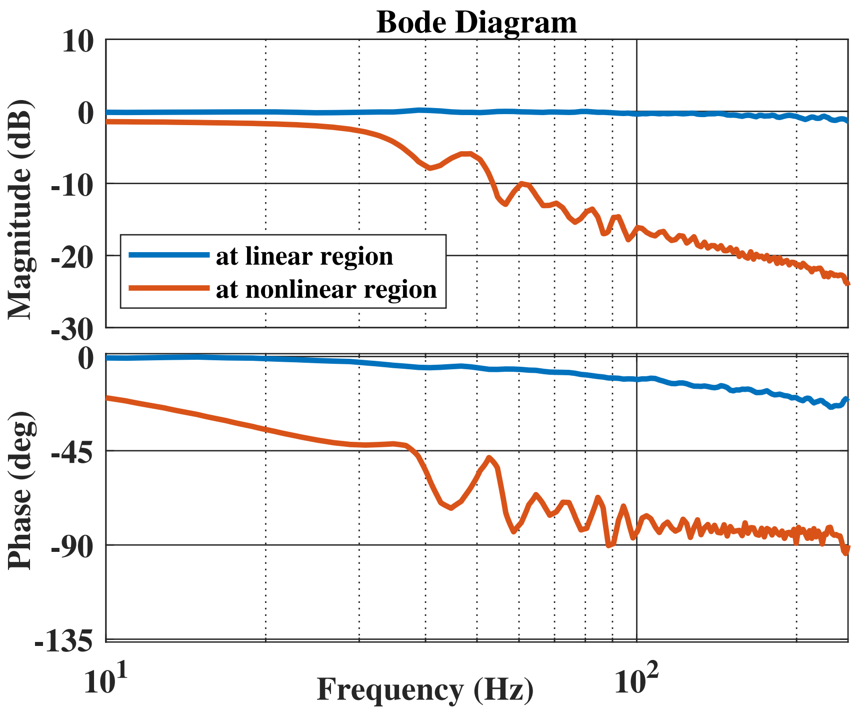


Figure 2.11: Frequency response of i_{dref} and measured i_d current, at $f_{sw} = 100\ kHz$, at nonlinear and linear regions, Si MOSFET-based VSI.

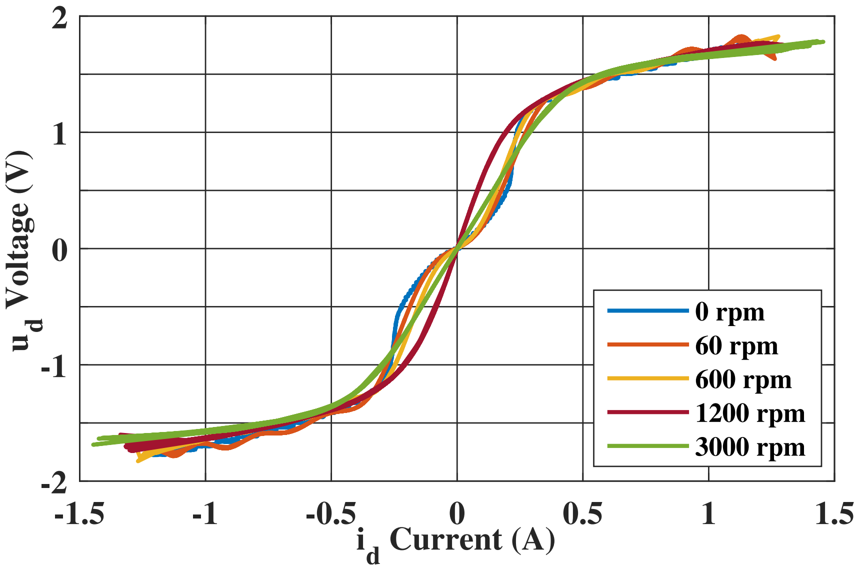


Figure 2.12: u_d voltage versus i_d current, with varying motor shaft speed and $f_{sw} = 100\ kHz$, Si MOSFET-based VSI.

in a particular region in the u_d-i_d graph seen in Fig. 2.10, these parameters have the potential to destabilize the system in the other regions of the same graph. As an example, when the tuning is performed in the linear region, the system may become unstable when the operation point moves to the nonlinear region. This will be further investigated below:

To achieve a smooth integrator-like open-loop response when using a traditional PI controller in a current controller, the general rule of thumb is to position the controller's zero close to the pole of the R-L circuit. Given the plant as an R-L circuit, the transfer function from u_d voltage to i_d current can be expressed as in (2.13). The current controller parameters can then be selected by (2.14) and (2.15), where f_{bw} is the target bandwidth, which is set to 1 kHz.

$$\frac{i_d}{u_d} = \frac{1}{L(s + \frac{R}{L})} \tag{2.13}$$

$$K_p = 2\pi f_{bw} L \tag{2.14}$$

$$K_i = K_p \frac{R}{L} \tag{2.15}$$

However, as discussed above and shown in Fig. 2.9, the apparent resistance, that is the resistance seen by the controller, obtained from the u_d-i_d curve changes along the nonlinear region. The local slope of the u_d-i_d curve is used to estimate the changing apparent resistance value. For $f_{sw} = 100\ kHz$, the difference in u_d voltage for every 0.25A change in i_d is recorded, and the apparent resistance (Δu_d / Δi_d) is determined and shown in Fig. 2.13. As shown in Fig. 2.13, the apparent resistance value increases more than tenfold as the system enters the nonlinear region. To demonstrate the impact of the nonlinear region on system performance, a current controller is calculated using (2.14) and (2.15). Then, the open-loop bode diagram of the controller and plant model is calculated. Then, for comparison, a ten-fold resistor value is used in the plant model. The change in the open-loop bode diagram is compared in Fig. 2.14. The bandwidth of the current control in the nonlinear region is decreased as the apparent resistance value increases. When a 100 Hz bandwidth position controller is tuned, assuming a 1 kHz bandwidth current control loop, the device may become

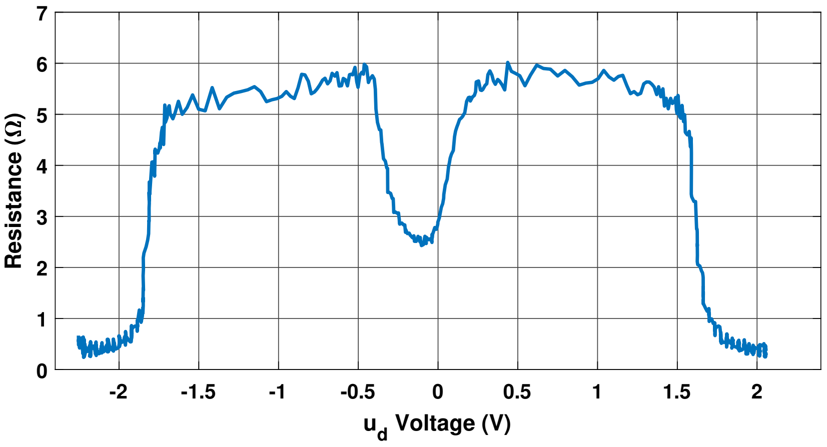


Figure 2.13: Variation of the apparent resistance value along the nonlinear region at $f_{sw} = 100\ kHz$.

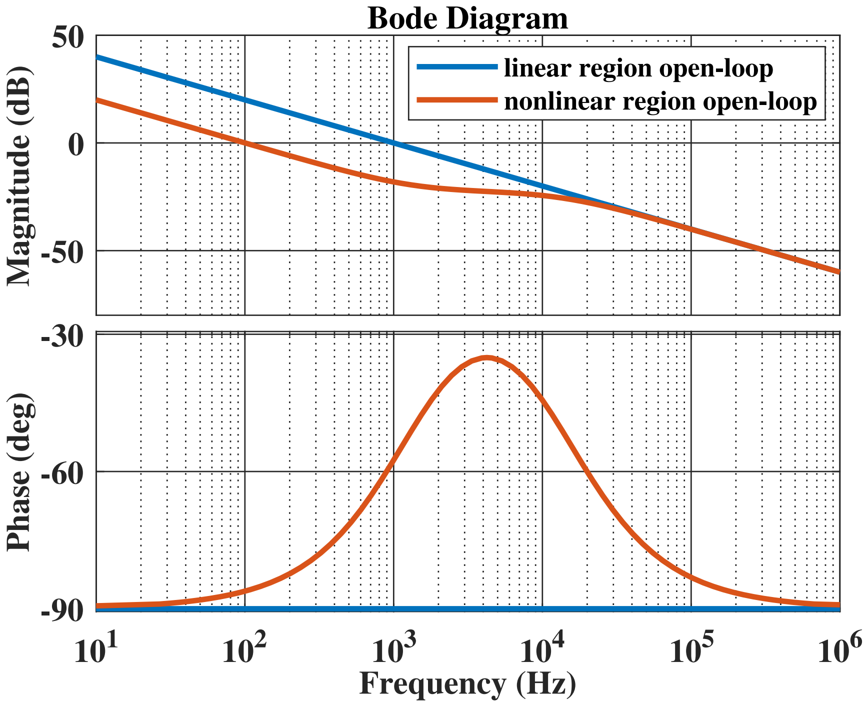


Figure 2.14: Current control open-loop at linear and nonlinear regions at $f_{sw} = 100$ kHz.

unstable since the bandwidth of the current controller in the nonlinear region is reduced. Fig. 2.15 depicts this phenomenon, in which the position closed-loop system becomes unstable in the nonlinear region of the current control.

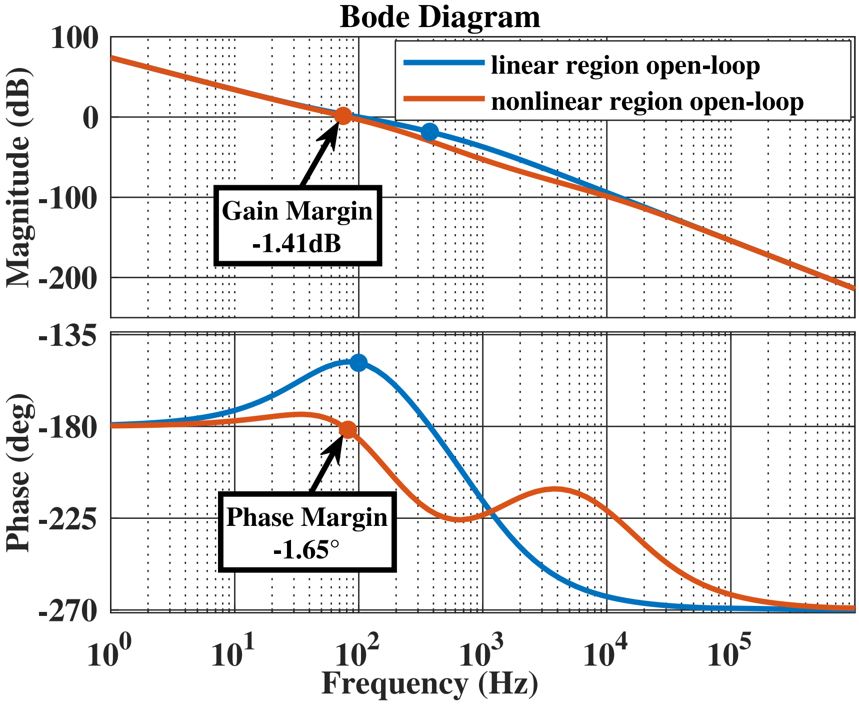


Figure 2.15: The effect of the nonlinear region on the position control loop at $f_{sw} = 100\ kHz$.

2.3.3 The Calculation of the Compensation Function

As stated in the previous section, nonlinearities in the zero-crossing regions will cause the device to become unstable. A compensation function ($f(i_d)$) can be used to reduce such nonlinearities. The i_d and u_d values obtained at a switching frequency of 20 kHz are used in this part. The u_d versus i_d graph is divided into sections, and curve fitting is used on each section to determine the function of $f(i_d)$. Fig. 2.16 depicts these divided sections. As can be seen from the figure, especially at the zero-crossing regions of the i_d current where the effects of nonlinearity arise, the number of sections had to be increased to better fit the curves at these regions. Note that each section is shown as a separate number. To calculate the compensation function, eight parts are used in total. Then, using polynomial functions of up to order five, curve fitting is performed on each of these parts. The results of the curve fitting of each part are shown in Fig. 2.17, and they are demonstrated on the original measurements to better visualize them. It should be noted that the number of sections, the degree of the fitted polynomials, the data logging sampling frequency, and the input voltage all have

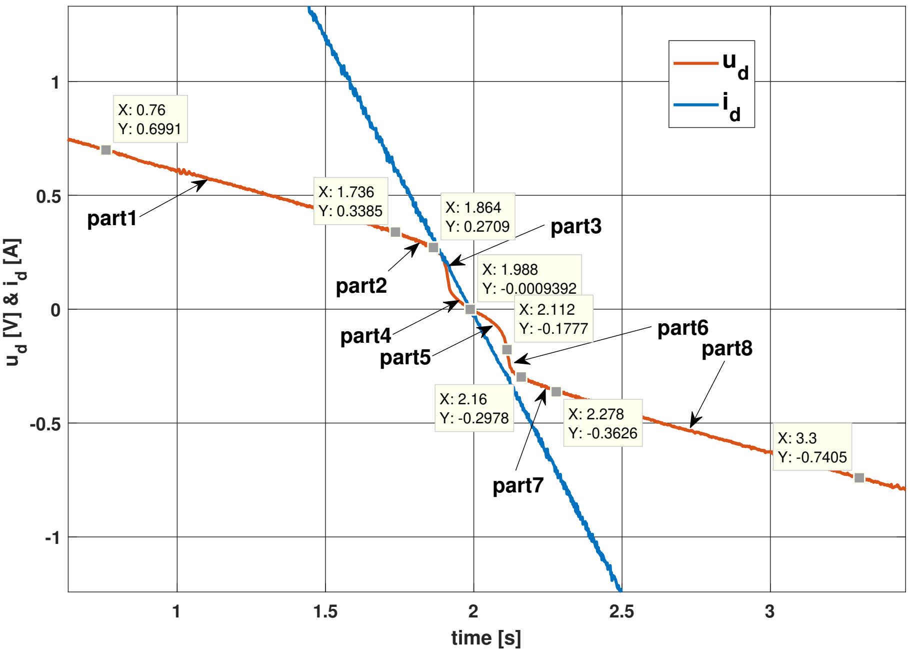


Figure 2.16: The sections of the i_d current and u_d voltage graph at $f_{sw} = 20\ kHz$.

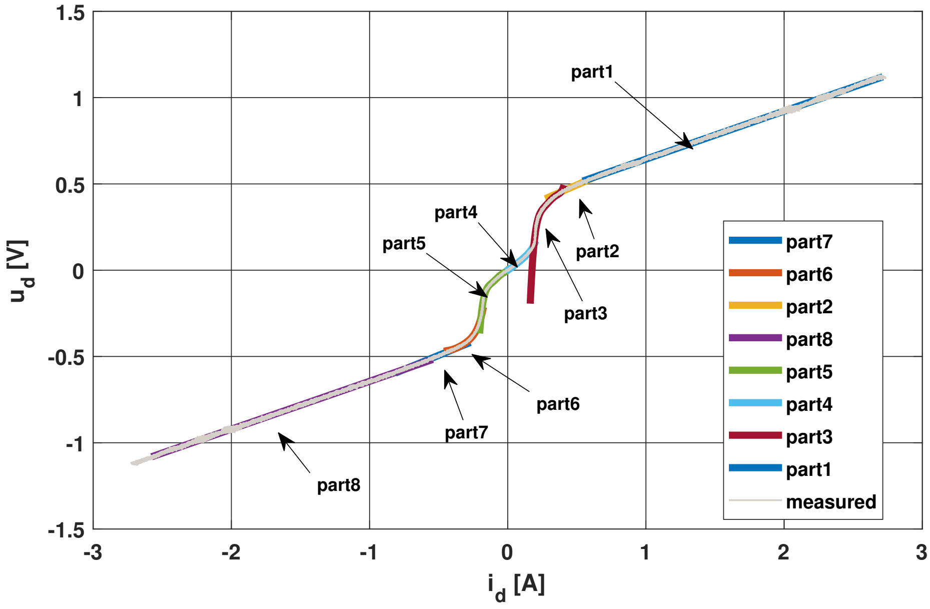


Figure 2.17: u_d voltage versus i_d current graph with fitted curves at $f_{sw} = 20\ kHz$.

an impact on the results and should be taken into consideration when producing the compensation function of $f(i_d)$.

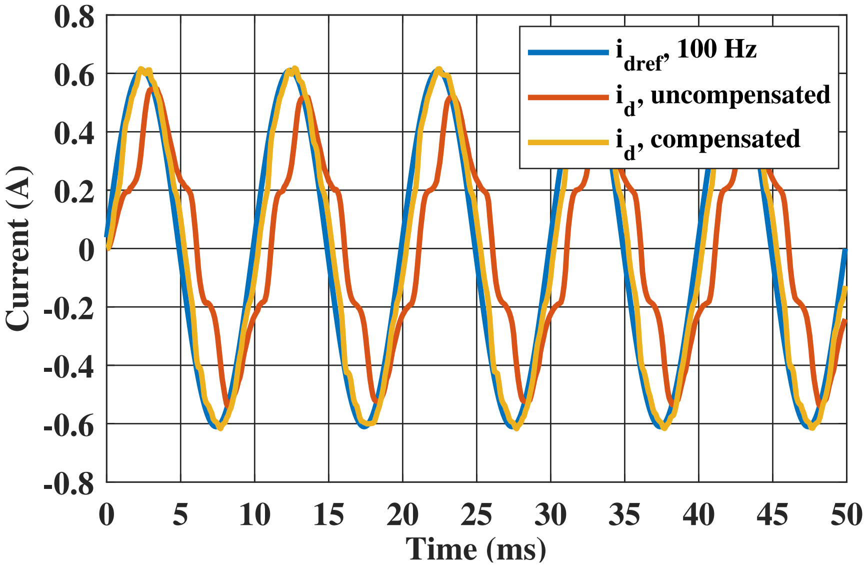


Figure 2.18: The 100 Hz i_d reference and the measured i_d values with and without the nonlinearity compensation, Si MOSFET-based VSI.

2.3.4 Experimental Results of the Compensation of the Nonlinearity

The compensation function $f(i_d)$ is validated experimentally in this section. The results are analyzed both in the time and frequency domains.

A 100 Hz sinusoidal i_d reference signal is applied without and with compensation of nonlinearity by using the function $f(i_d)$. The results are shown in Fig. 2.18. As can be seen from the figure, the effect of nonlinearity on current controller bandwidth is reduced by using the compensation function.

As an i_d reference signal, a chirp signal with a frequency range of 10 Hz to 250 Hz is used, both with and without compensation of the nonlinearity, which is shown in Fig. 2.19. The increase in the bandwidth of the current controller is also presented by using the bode diagram, and it is depicted in Fig. 2.20.

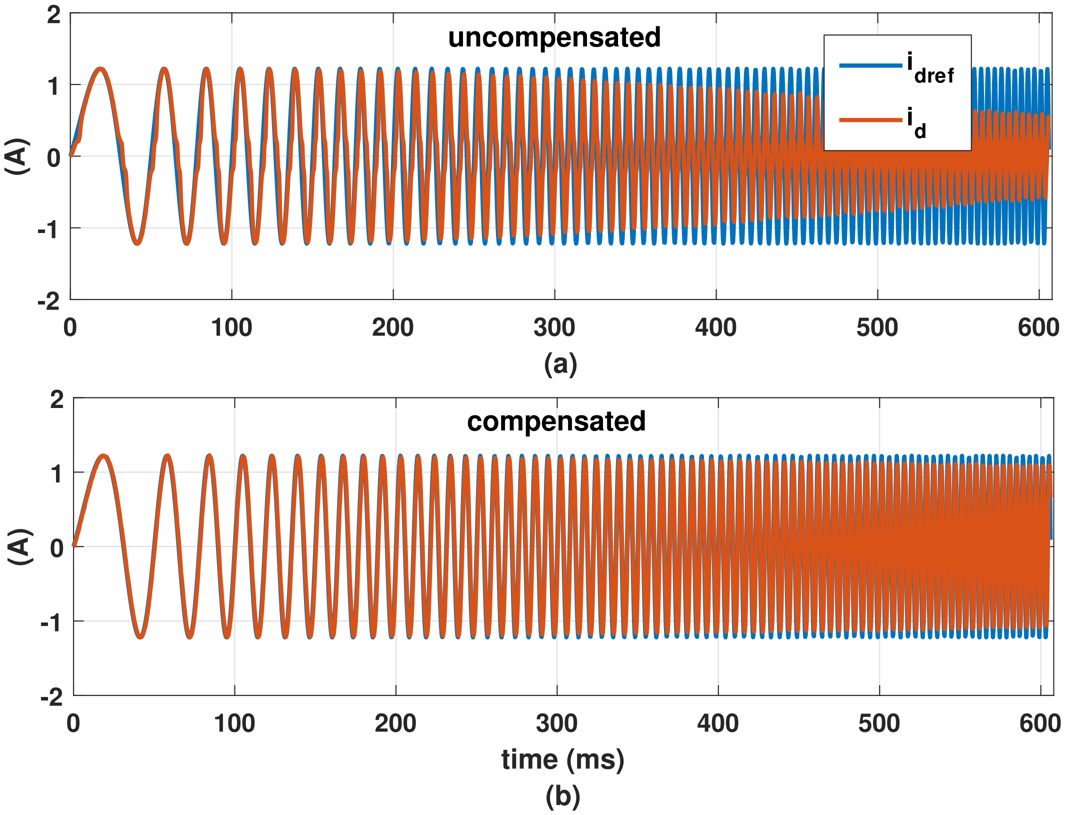


Figure 2.19: Chirp signal from 10 Hz to 250 Hz i_d reference and measured i_d in time domain, Si MOSFET-based VSI. (a) without compensation (b) with compensation

2.4 Experimental Work with GaN E-HEMT Based VSI

2.4.1 Nonlinearities in GaN E-HEMT Based VSI: Effects of Switching Frequency and Dead Time

In this part, the effect of the switching frequency and the dead time on the nonlinearity are demonstrated by using the u_d-i_d graph. A GaN E-HEMT based VSI is utilized during the experiments.

The most dominant terms in the nonlinearity are dead time, Si MOSFET/gate driver rise/fall time, and Si MOSFET/gate driver turn-on/off delay time. The effect of these time parameters increases as the switching frequency increases. A dead time of 1 μs, for instance, refers to 1% of the period when f_{sw} is 10 kHz, but 10% when f_{sw} is 100 kHz. Different techniques are used to reduce these nonlinearities in the literature,

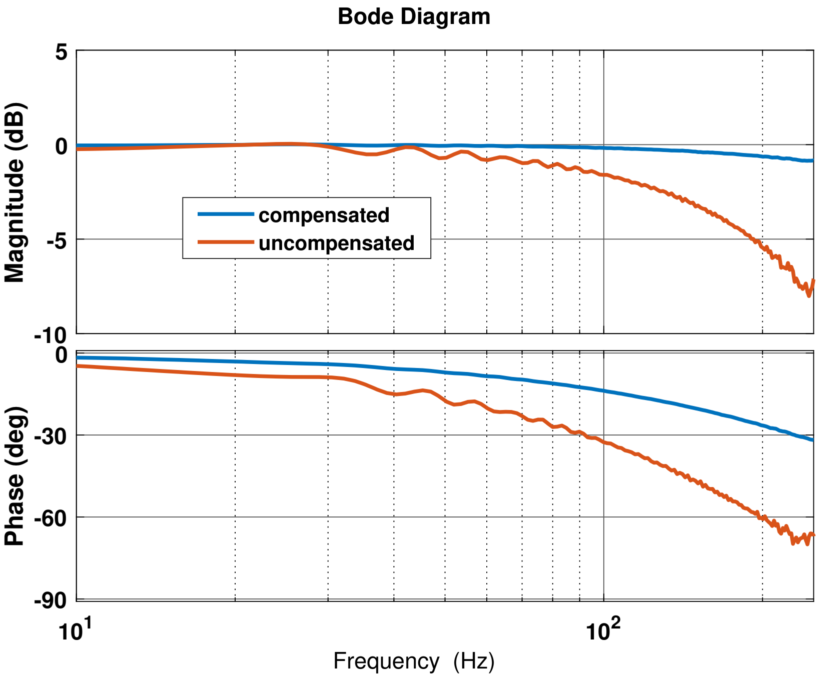


Figure 2.20: Chirp signal from $10\ Hz$ to $250\ Hz$ i_d reference and measured i_d with and without compensation in frequency domain, bode diagram, Si MOSFET-based VSI.

such as [19], [23], [29], [30], where details are given in Chapter 2.1. Aside from these, the compensation function $f(i_d)$ can also be used to reduce nonlinearities. However, for each input voltage, for all motor speeds, and all environmental conditions, it is still hard to obtain a valid $f(i_d)$. Thus, in place of the Si MOSFET-based VSI motor drive, a GaN E-HEMT-based VSI motor drive can decrease the impact of time parameters on nonlinearity without having to deal with complicated calculations.

The switching frequency must be high enough to build a high current control bandwidth VSI [35], but as the switching frequency increases, the nonlinearities in the system also increase accordingly, as described in the previous sections. GaN E-HEMT VSI fed motor drives are considered as an alternative to Si MOSFET-based VSI motor drives to balance this condition by having the fast switching capability of the GaN E-HEMT, which allows much shorter dead time. A 3-phase, 2-level GaN E-HEMT-based inverter (BOOSTXL-3PHGANINV) and a floating-point type microcontroller (C2000 F28379D) are used in the experiment. Each phase of the inverter is com-

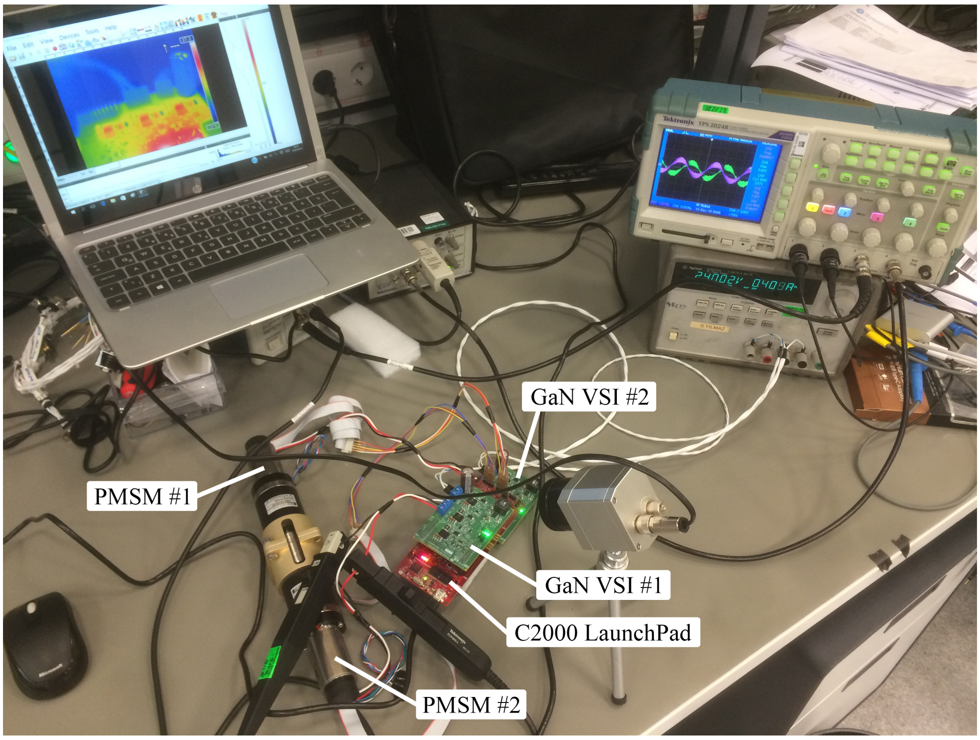


Figure 2.21: Experimental setup for GaN E-HEMT based VSI.

posed of two GaN E-HEMTs in a half-bridge configuration with an integrated gate drive (LMG5200). Although LMG5200 allows even lower, the dead time is set to 20 ns to be on the safe side while using these evaluation boards. Fig. 2.21 depicts the experimental setup.

The same PMSM that was presented in Section 2.3 is used to investigate the influence of switching frequency on nonlinearity. To test the GaN E-HEMT based VSI, the same test method as defined in Section 2.3.2 is used. The maximum switching frequency of the GaN E-HEMT based VSI is held at 100 kHz for comparative analysis. 20 ns of dead time refers to 0.02% of the switching period when f_{sw} is 10 kHz and 0.2% when f_{sw} is 100 kHz. As shown in Fig. 2.22, it is not so straightforward to observe nonlinearities in zero-crossing regions with a dead time of 20 ns compared with the Si MOSFET-based VSI case (Fig. 2.8). Since the dead time and also the turn-ON/OFF times of the GaN E-HEMT and integrated gate driver (LMG5200) are too small, the corresponding nonlinearities do not need any further compensation.

To show the effect of the dead time on the nonlinearity, the same test is applied to the

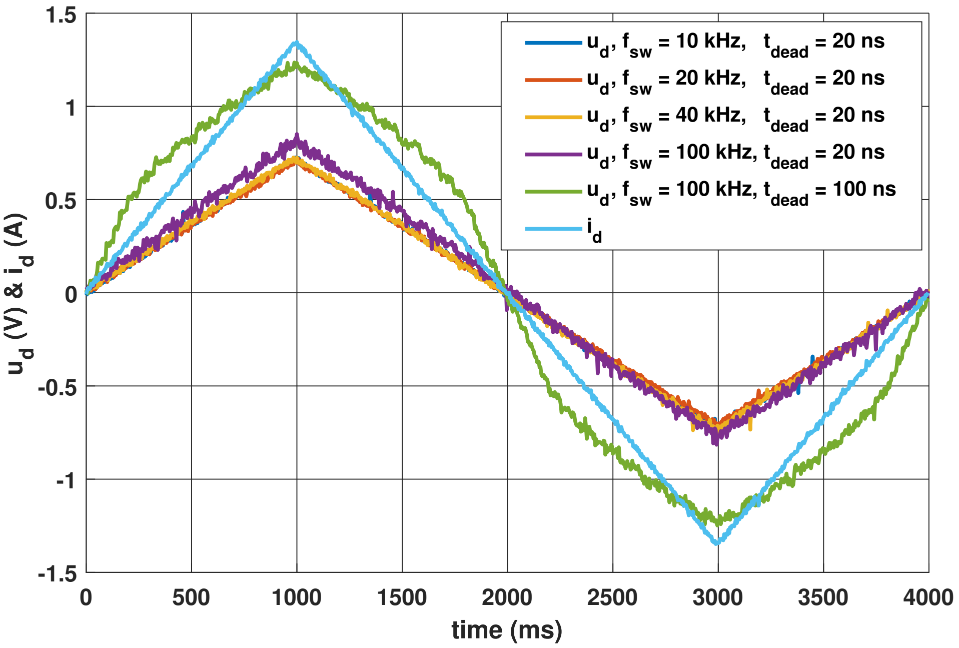


Figure 2.22: u_d and i_d with time, GaN E-HEMT based VSI at $f_{sw} = 10\ kHz$ to 100 kHz, t_{dead} 20 ns and 100 ns.

GaN E-HEMT based inverter, but this time the dead time is intentionally increased to 100 ns. As can be seen with the green line in Fig. 2.22, as the dead time duration increases, the distortion of the voltage around the zero-crossing region of the i_d current becomes more notable.

The u_d versus i_d graph is shown in Fig. 2.23. To have a better understanding of the difference between the zero crossing regions of the id current in GaN E-HEMT and Si MOSFET based VSIs, the u_d-i_d curve at $f_{sw} = 100\ kHz$ of the Si MOSFET based VSI (Fig. 2.9) is added to Fig. 2.23.

In order to compare the Si MOSFET-based VSI (see Fig. 2.11), the same chirp signal (starting at 10 Hz and ending at 250 Hz) is used as an i_d reference (see Fig. 2.10) with a switching frequency of 100 kHz. The current controller bandwidth is adjusted to 1 kHz by using equations (2.13) to (2.15) and the dead time is 20 ns. As shown in Fig. 2.24a, the current controller can follow the i_d reference signal nearly over the entire frequency range. To demonstrate the effect of the dead time, the test is repeated with 100 ns dead time and it is shown in Fig. 2.25b. The bode diagram of the Si MOSFET at the nonlinear region (Fig. 2.11) is also adapted to the figure for

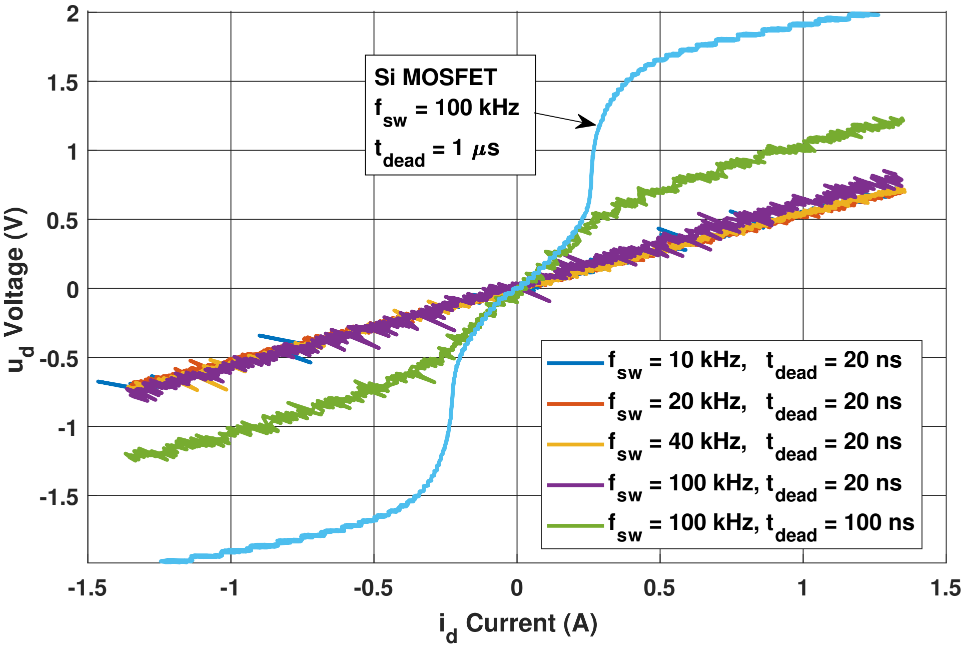


Figure 2.23: u_d voltage versus i_d current, at $f_{sw} = 10\ kHz$ to $100\ kHz$, $t_{dead} = 20$ ns and $100\ ns$, GaN E-HEMT based VSI and Si MOSFET-based VSI at $f_{sw} = 100$ kHz and $t_{dead} = 1\mu s$.

comparison.

2.4.2 Nonlinearities in GaN E-HEMT Based VSI: Phase Current Harmonic Distortions

The harmonics in the phase current caused by the VSI's nonlinearities are observed in this section using the GaN E-HEMT based VSI.

The same coreless PMSM and the same test procedure in Section 2.3.1 are followed to measure phase current harmonic distortions.

The PMSM is driven in open-loop with electrical speeds of $10\ Hz$ and $40\ Hz$ with the same switching frequency, which is $20\ kHz$. In Table 2.3, the percentages of harmonic distortion values of the phase currents, which are taken from the power analyzer, are listed.

As can be seen from the table compared with Table 2.2, the phase current harmonic

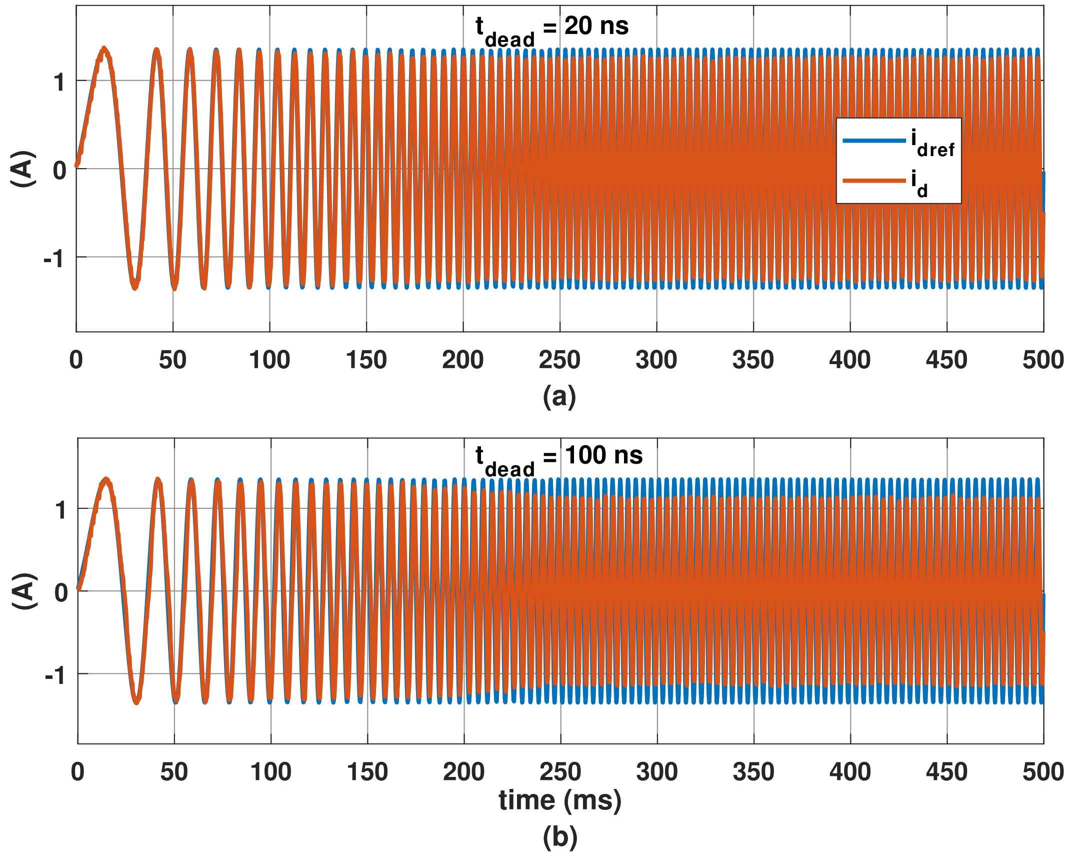


Figure 2.24: Chirp signal from $10\ Hz$ to $250\ Hz$ i_d reference and measured i_d, at $f_{sw} = 100\ kHz$ in time domain, GaN E-HEMT based VSI. (a) with $20\ ns$ dead time (b) with $100\ ns$ dead time

Table 2.3: Phase Current Harmonic Distortions [%] at 10 Hz and 40 Hz Electrical Reference Speed at No Load with GaN E-HEMT based VSI

Current Harmonics	**@10 Hz**	**@40 Hz**
5^{th}	0.31	0.39
7^{th}	0.2	0.19
11^{th}	0.05	0.08
13^{th}	0.07	0.03
17^{th}	0.03	0.05
19^{th}	0.01	0.07
THD_I	0.84	0.53

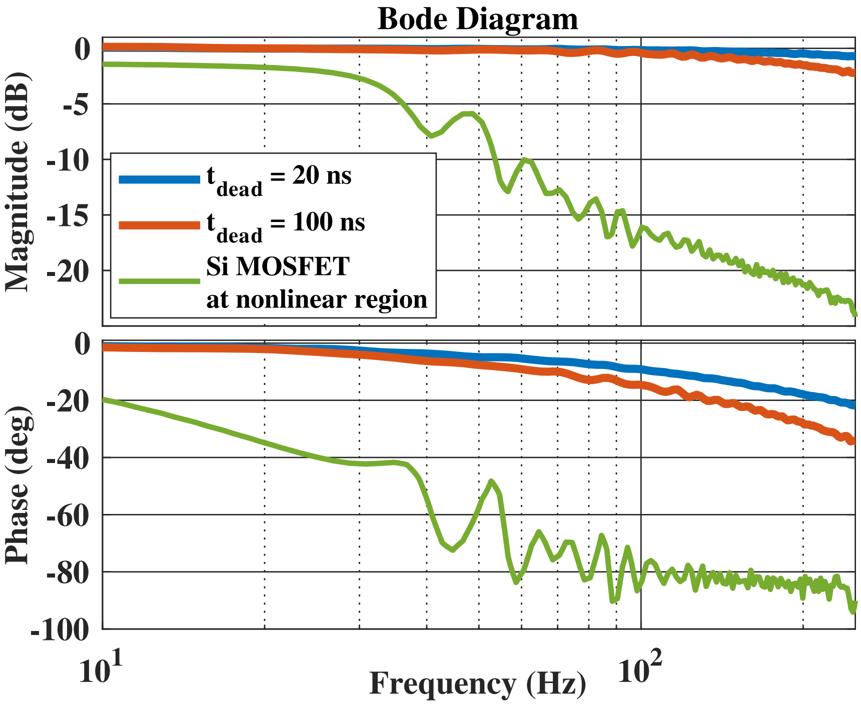


Figure 2.25: Frequency response of the i_{dref} and measured i_d current, at $f_{sw} = 100$ kHz, with 20 ns and 100 ns dead time, GaN E-HEMT based VSI and Si MOSFET-based VSI at nonlinear region.

distortions are significantly reduced. The main reason is that the GaN E-HEMT based VSI has a much shorter, 20 ns, dead time. Lower dead time means less nonlinearity in VSI, resulting in reduced distortion of phase current harmonics.

2.4.3 Current Control Bandwidth Measurements of the GaN E-HEMT Based VSI

The experimental setup shown in Fig. 2.21 is used to show how the dead time affects the bandwidth of the i_q and i_d current controllers. In this configuration, PMSM-#1 serves as the driver motor, maintaining constant shaft velocity, while PMSM-#2 serves as the load motor. The load motor is used to analyze the control loop's frequency response [36]. To examine the impact of the dead time, measurements are repeated with dead times of 20 ns, 100 ns, and 200 ns. The current control bandwidth of the i_d and i_q loops is adjusted to be 1.66 kHz. The closed-loop system is run with the configured controller, and the data needed for estimating the open-loop characteristics is collected. Fig. 2.26 and Fig. 2.27 show the measured open-loop properties of the i_d and i_q current control loops.

As can be seen from the Fig. 2.26b, the dead-time affects the bandwidth of the i_d current controller. The bandwidth is reduced by approximately 36% when the dead time is adjusted to $200\ ns$. Since the FOC method is applied when running the PMSM, i_{dref} is set to zero. This results in an i_d current operating around zero, where the nonlinearity effects are more dominant. This is not the case for i_q current controller. Since i_q current is around $2.3A$, which corresponds to the linear region, the effect of the dead time could not be observed easily during the frequency analysis test (as presented in Fig. 2.27) compared to the i_d current controller case.

2.5 Power Loss and Cost Comparison

The conduction and switching power losses of the Si MOSFET (SUM90N10) and GaN E-HEMT (LMG5200) are compared in this section. Assuming a balanced PMSM, the power losses in one of the inverter legs are investigated. Assume that the output phase current leg A (Fig. 2.1) is presented as in (2.16).

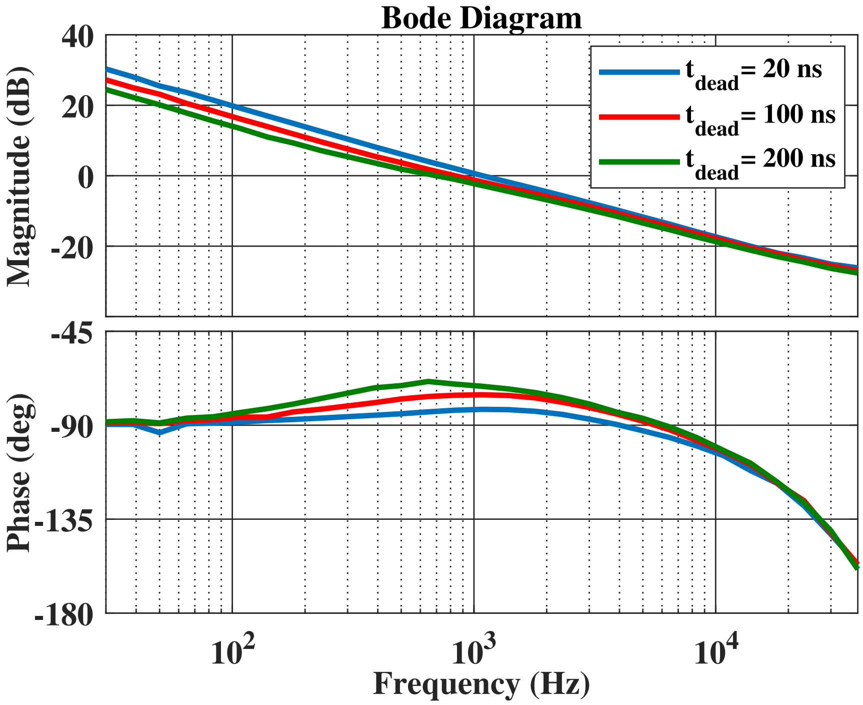
$$i_a(t) = \sqrt{2} I_{a_{rms}} \sin(\dot{\theta}_e t) \tag{2.16}$$

For both transistors, the conduction power losses of the leg A can be determined as in (2.17), where $R_{ds_{on}}$ is the drain-to-source resistance during conducting.

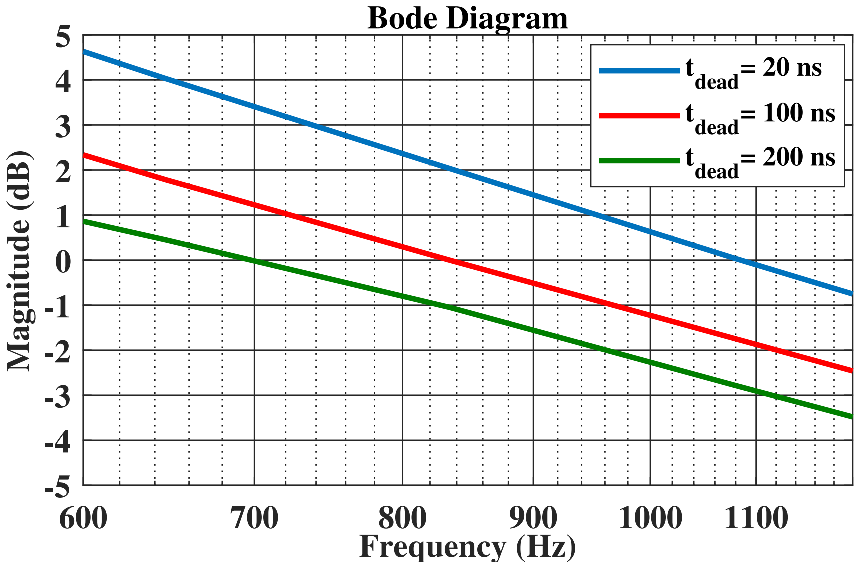
$$P_c = R_{ds_{on}} I_{a_{rms}}^2 \tag{2.17}$$

According to the reverse current conduction properties of the transistors, the current passes through the body diode of the Si MOSFET and the 3^{rd} quadrant of the GaN E-HEMT during the dead time. So during the dead time, conduction power losses of the leg A can be determined as in (2.18)

$$P_{c_{dead}} = I_{a_{avg}} u_{sd} (2t_{dead}) f_{sw} \tag{2.18}$$

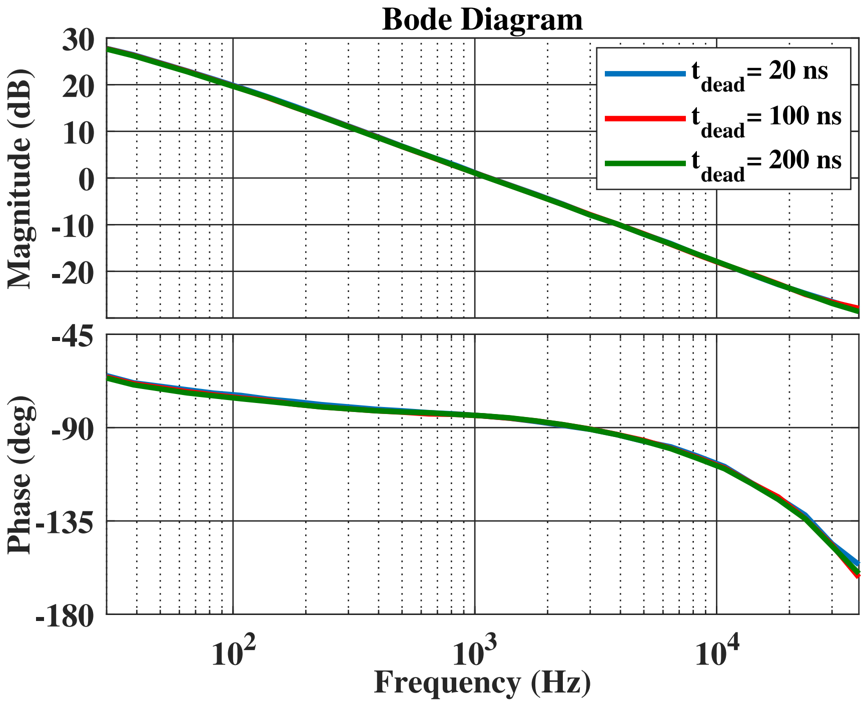


(a)

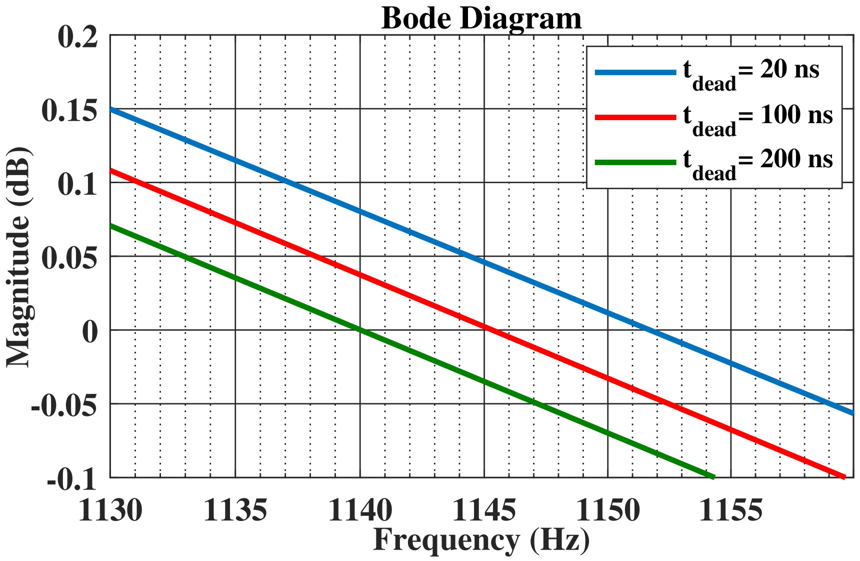


(b)

Figure 2.26: The open-loop frequency response characteristics of the i_d current control loop at $f_{sw} = 100\ kHz$, GaN E-HEMT based VSI. (a) gain and phase (b) gain zoomed at zero-crossing dB



(a)



(b)

Figure 2.27: The open-loop frequency response characteristics of the i_q current control loop at $f_{sw} = 100\ kHz$, GaN E-HEMT based VSI. (a) gain and phase (b) gain zoomed at zero crossing dB

where;

u_{sd} : source-to-drain voltage

$I_{a_{avg}}$: average phase current $= \sqrt{2}I_{a_{rms}}/\pi$

The switching power losses of leg the A for Si MOSFET and its body diode are given in (2.19) and (2.20).

$$P_{sw_{simos}} = (V_{dc}I_{a_{avg}}(t_r + t_f) + (2Q_{rr}V_{dc}))f_{sw} \tag{2.19}$$

$$P_{sw_{simosbd}} = Q_{rr}V_{dc}f_{sw} \tag{2.20}$$

where;

V_{dc} : DC bus voltage $(24V)$,

t_r : rise time of the transistor

t_f : fall time of the transistor

Q_{rr} : reverse recovery charge (typ. $91nC$)

The switching power losses of the leg A for GaN E-HEMT are given in (2.21). It should be noted that the GaN E-HEMT has no recovery loss.

$$P_{sw_{gan}} = V_{dc}I_{a_{avg}}(t_r + t_f)f_{sw} \tag{2.21}$$

For both transistors, the switching power loss of the output capacitance of leg A can be determined as in (2.22), where Q_{oss} is the transistors' output charge.

$$P_{oss} = 2Q_{oss}V_{dc}f_{sw} \tag{2.22}$$

The total switching, conduction, and overall power losses of the leg A for the Si MOSFET and GaN E-HEMT are shown in Fig.2.28, 2.29, and 2.30, respectively, with various phase currents and switching frequencies using the parameters given in Table 2.4.

As the switching frequency increases, the conduction losses during the dead time of the Si MOSFET become more dominant, as seen in Fig. 2.28. The switching losses

Table 2.4: Parameters used in loss calculations

Parameters	**Si MOSFET**	**GaN E-HEMT**
$R_{ds_{on}}$	$6.7\ m\Omega$	$15.0\ m\Omega$
t_{dead}	$1.0\ \mu s$	$0.02\ \mu s$
$t_r + t_f$	$26.0\ ns$	$0.96\ ns$
Q_{oss}	$35.3\ nC$	$21.0\ nC$

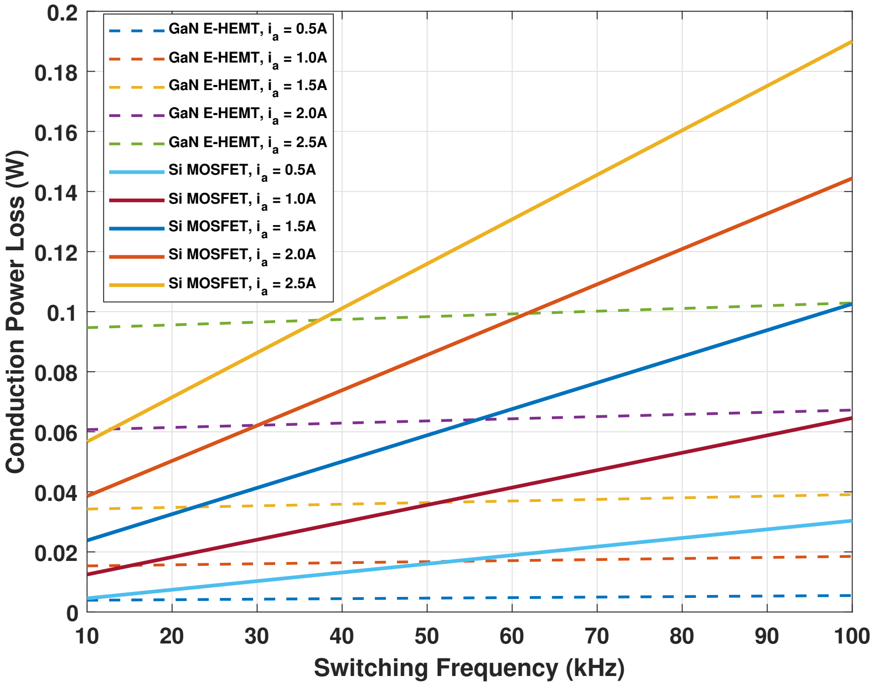


Figure 2.28: Conduction power losses of the leg A for Si MOSFET and GaN E-HEMT.

of the GaN E-HEMT are much lower than those of the Si MOSFET, particularly as the switching frequency increases (see Fig. 2.29). This is due to the GaN E-HEMT's fast switching capability, low output charge, and lack of reverse recovery charge. For comparison, the total power losses (P_{loss}) of the leg A at some of the operating points are listed in Table 2.5.

The cost of the three LMG5200s ($29.06\$$) is about 60% higher than the Si MOSFET equivalents (six SUM90N10 and single gate driver pack IRS2336, $18.14\$$). In the application, the cost of Si MOSFET power components over the total cost of the inverter

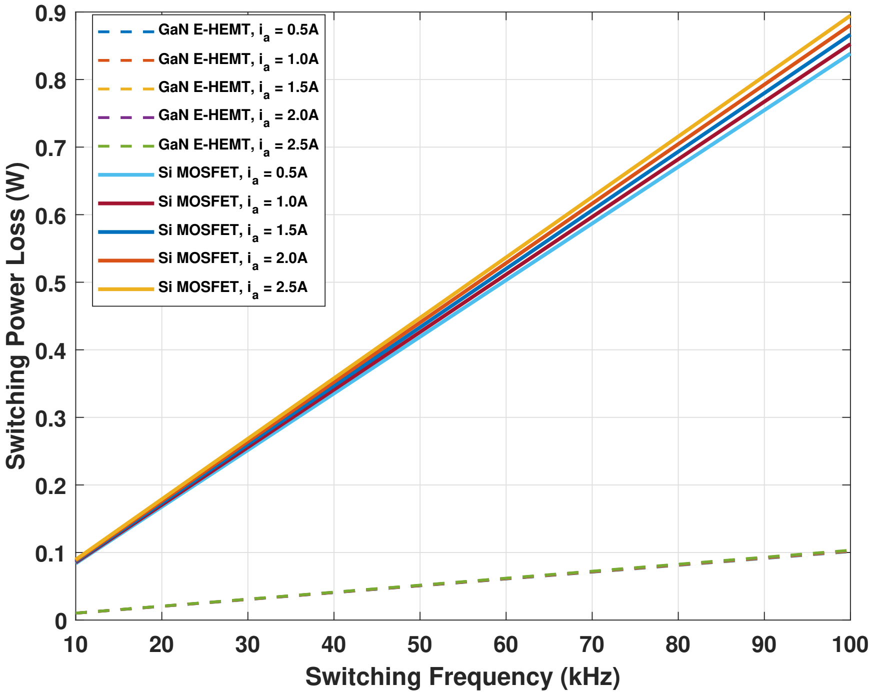


Figure 2.29: Switching power losses of the leg A for Si MOSFET and GaN E-HEMT.

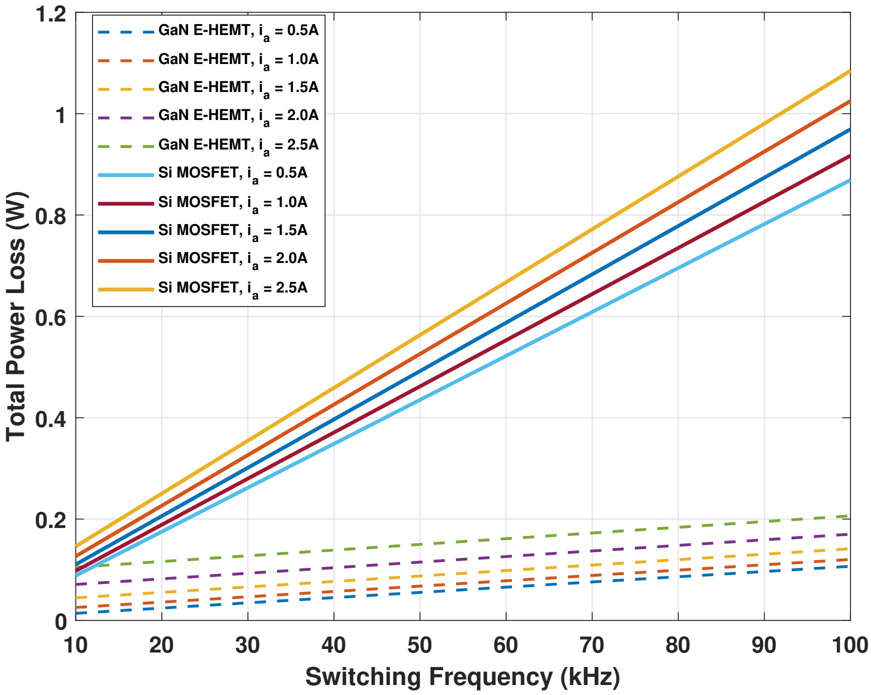


Figure 2.30: Total power losses of the leg A for Si MOSFET and GaN E-HEMT.

card and over the servo motor drive is approximately 10.73% and 2.71%, respectively. As a result, the GaN E-HEMT solution increases the inverter card cost only by 6.46%

Table 2.5: Power Losses of the Leg A at some of the operating points

	Si MOSFET	**GaN E-HEMT**
P_{loss}(20kHz,0.5A) (W)	0.1751	0.0244
P_{loss}(20kHz,2.5A) (W)	0.2504	0.1163
P_{loss}(100kHz,0.5A) (W)	0.8689	0.1068
P_{loss}(100kHz,2.5A) (W)	1.0846	0.2063

and the servo motor drive cost by 1.63%. Although the GaN E-HEMT based inverter is more expensive, it can be acceptable for high-performance applications.

2.6 Chapter Summary

In this chapter, the effect of nonlinearities on phase current and current controller is investigated using a coreless type, a low inductance PMSM, and a Si MOSFET-based VSI fed motor drive. The effects of increasing the switching frequency on nonlinearities are examined. Furthermore, the current controller's response is shown to change between nonlinear and linear regions. To linearize the u_d-i_d relationship, a mapping function of $f(i_d)$ is derived, and the applicability of this approach is tested experimentally. However, obtaining such a function in all operational conditions is impractical. To address the aforementioned issues, a GaN E-HEMT-based VSI-fed PMSM drive is suggested. The same experiments are performed on the GaN E-HEMT-based VSI, and the findings are compared to the Si MOSFET-based design. It is demonstrated that the performance of a VSI-based on GaN E-HEMT is preferable for high-bandwidth control applications. With frequency analysis and by loading the PMSM, the impact of dead time on the bandwidth of the current controller of the GaN E-HEMT based VSI is also examined. Finally, the conduction and switching power losses of the Si MOSFET (SUM90N10) and GaN E-HEMT (LMG5200) are compared, and the costs of the alternative solutions are given.

The dead time of the VSI should be adjusted to the minimum allowable value by considering the gate driver and power switch time parameters with a safety factor. In this chapter, it is shown that as the dead time value decreases, nonlinearities in VSI, THDs of output phase current, and 3^{rd} conduction losses also decrease. On the other hand, to achieve a high current controller bandwidth, the switching frequency should be increased. As the switching frequency increases, the nonlinearity in VSI rises due to the increase in the ratio of dead time over the switching period. However, if the i_q current is operating in the linear region even when the dead time increases, the bandwidth of the i_q controller does not change so much. This is also demonstrated in Section 2.4.3, where the dead time is intentionally increased to $200\ ns$ compared to the default value of $20\ ns$. This is because, during the bandwidth test, the i_q current is still operating in the linear region. Therefore, the operating torque region of the system should also be taken into consideration, besides the required current control bandwidth, switching losses, current ripples, etc., when deciding the value of the switching frequency of the VSI.

CHAPTER 3

GAN E-HEMT VSI-BASED SERVO DRIVE DESIGN

3.1 Introduction

In this chapter, first, basic information about GaN E-HEMTs, such as their structures, material properties, 3^{rd} quadrant operations, etc., is provided. Then, an overview of the designed GaN E-HEMT VSI based servo drive is given, which includes efficiency, thermal and conduction emissions tests of the servo drive.

Wide-bandgap (WBG) devices like GaN E-HEMT and silicon carbide (SiC) MOSFET are becoming increasingly common in applications for power electronics. WBG devices have shorter turn-ON/OFF time periods, almost zero reverse recovery loss, better thermal capability, and lower conduction losses than traditional Si MOSFETs and IGBTs [37], [38]. Because of these properties, the switching frequency may be increased, resulting in considerable weight and size reduction [1, 39, 40]. Wireless power transfer systems, plasma generators, LiDAR, RF power supply, and RF envelope tracking converters are just a few of the present and upcoming applications where GaN HEMTs provide remarkable performance rise [37, 41].

3.2 Wide Bandgap Semiconductor: Gallium Nitride E-HEMT

3.2.1 History

In 2006, AlGaN/GaN HEMTs were produced and put into mass production [42]. They were used in high frequency (GHz) radio frequency (RF) applications such as digitally modulated base station applications. They are normally ON, which means they are depletion-mode devices, and a negative gate voltage is needed to switch them off. However, depletion-mode devices are not preferable in most power electronic applications because a negative voltage should be applied to the gate of the transistor at the startup of the operation. EPC introduced the first commercially available normally OFF, which means enhancement-mode, GaN transistors in 2009. The power GaN market has doubled ($46M) in 2020 compared to 2019 and is expected to exceed $1B by 2026 [43].

3.2.2 GaN HEMT Structure

For GaN-based devices, there are two methods for achieving normally OFF (enhancement-mode) operation [44]:

1. Utilizing a cascode structure that integrates a low-voltage Si MOSFET and a high-voltage normally ON GaN device in a package.
2. Utilizing a true, normally-OFF GaN power device on a single chip.

3.2.2.1 Cascode GaN HEMT

Gate control in cascade configuration is analogous to Si MOSFET since the gate of the package is bonded directly to the gate of the low voltage Si MOSFET, as seen in Fig. 3.1. Due to the lack of direct control over the gate of the GaN depletion-mode HEMT (D-HEMT), slew rate control is challenging. The slew rate tuning is essential to minimize ringing voltage and EMI while remaining in the safe operating area. Added package contacts inside the cascode system cause increased parasitic inductance, which can cause excessive ringing and reduce the frequency of operation [45]. A stack-die type package is proposed to reduce parasitic inductance in [46]. The junction capacitors of the two devices are critical and should be well-matched, particularly during the turn-off transition, since the voltage distribution between the GaN D-HEMT and Si MOSFET during the turn-off transition is heavily influenced by the junction capacitor charge [47]. In certain cases, the Si MOSFET can undergo an avalanche, resulting in increased switching loss and reliability issues. These cascode-

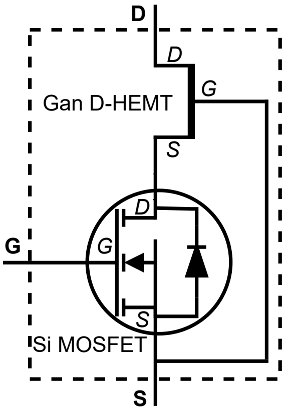


Figure 3.1: Cascode GaN HEMT, low voltage Si MOSFET in series with depletion mode GaN HEMT (D-HEMT)

type hybrid solutions are more efficient when the GaN transistor is high voltage and the MOSFET is low voltage (about $30V$). As a result, hybrid systems are feasible at voltages greater than $200V$ [48].

3.2.2.2 True Normally off GaN HEMT

The p-GaN gate FET and metal-insulator-semiconductor FET (MISFET) are defined in [44] as two successful methods for achieving true, normally-OFF GaN HEMT devices (GaN E-HEMT).

The general configuration of GaN power devices is primarily classified into two categories: lateral and vertical conduction devices. Vertical conduction GaN devices have several benefits [40,49], including:

- The potential to achieve high breakdown voltage and current levels while not increasing chip size.
- Thermal control is simpler than the lateral device.
- The high electric field region is located inside the substance and apart from the surface, which decreases the current collapse effect.

While vertical GaN devices have many advantages, native GaN substrates are commonly needed, and GaN wafers are not of adequate quality. As a result, the production and commercialization of vertical GaN power transistors is constrained by the availability of low-cost substrates [50]. Because of the good results of epitaxial growth of GaN/AlGaN thin layers above a conventional Si substrate, a lateral GaN power transistor for $600V$ and lower voltage applications has been commercially launched [51].

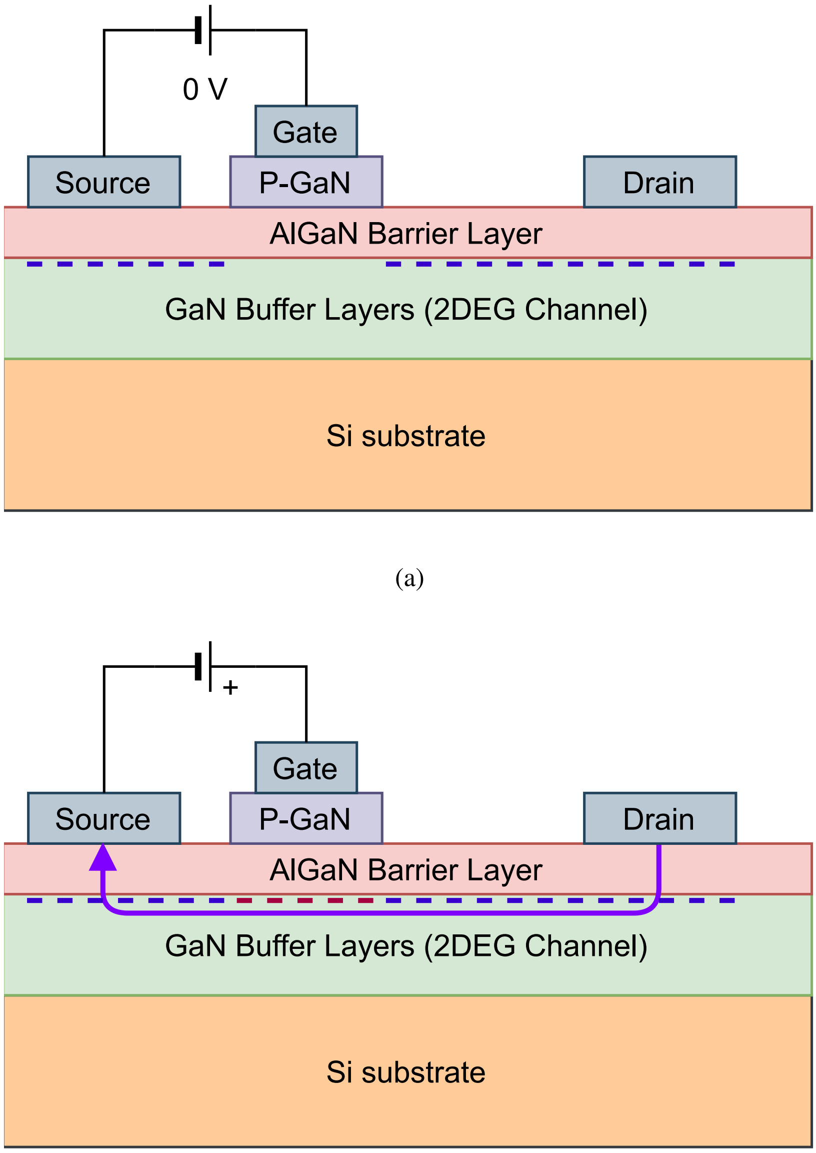
Fig. 3.2 depicts a simplified and unscaled lateral p-GaN gate, normally-off GaN HEMT structure [52]. As a starting material, the Si substrate is shown in Fig. 3.2. Among the SiC, sapphire, and Si, the best lattice match with GaN is SiC, and it has better thermal conductivity. However, when the GaN power device's growth material is SiC, the cost is much higher. Although sapphire and Si have similar lattice matches, sapphire thermal conduction is poor and the relative cost is higher. As a substrate, SiC is widely used for devices that need very high power densities, such as RF applications. Therefore, silicon is the preferred device for commercial applications where cost is important, such as power conversion applications, class D audio amplifiers, etc. [40, 48, 53].

At $0V$ or negative gate bias, the p-GaN gate depletes the two-dimensional electron gas (2DEG) underneath, which is shown in Fig. 3.2a. The 2DEG channel is activated by a positive gate bias as depicted in Fig. 3.2b.

3.2.3 Material Properties

High polarization effects create a 2DEG channel in AlGaN/GaN heterostructures, which provide high charge density and mobility. Therefore, the 2DEG channel is ideal for high electron mobility transistors (HEMT) [54]. Table 3.1 ([48], [55]) shows some of the material properties of GaN. For comparison, the material properties of Si and SiC are also added. To better visualize, the graph form of the table is also given in Fig. 3.3. The temperature dependence of these properties is investigated in [56].

The energy needed to jump an electron from the valence band to the conduction band is referred to as the bandgap. The larger the bandgap, the larger the critical electric field required to produce an avalanche breakdown, that means high current flow in the structure. As a result of the higher critical electric field, for the same breakdown


0 V
Gate
Source
P-GaN
Drain
AlGaN Barrier Layer
GaN Buffer Layers (2DEG Channel)
Si substrate
+
Gate
Source
P-GaN
Drain
AlGaN Barrier Layer
GaN Buffer Layers (2DEG Channel)
Si substrate

(a)

(b)

Figure 3.2: The true normally OFF GaN HEMT by p-GaN gate method (a) zero or negative gate bias to turn-off (b) positive gate bias to turn-on

voltage, thinner drift regions can be configured, leading to lower ON resistance. Since conductivity is proportional to electron mobility, high electron mobility decreases ON resistance even further. Higher saturation velocity and lower ON resistance enable a smaller die size to be used to achieve a specified current capacity, resulting in lower input and output capacitances. The lower capacitance allows for more rapid transient

Table 3.1: Material Properties of Si, SiC and GaN ([48], [55])

Properties	**Si**	**4H-SiC**	**GaN**
Energy Gap (eV)	1.12	3.26	3.39
Critical Electric Field (MV/cm)	0.23	2.2	3.3
Electron Saturation Velocity $(10^7\ cm/s)$	1.0	2.2	2.5
Electron Mobility $(10^3\ cm^2/V.s)$	1.4	0.95	1.5
Thermal Conductivity $(W/cm.K)$	1.5	3.8	1.3

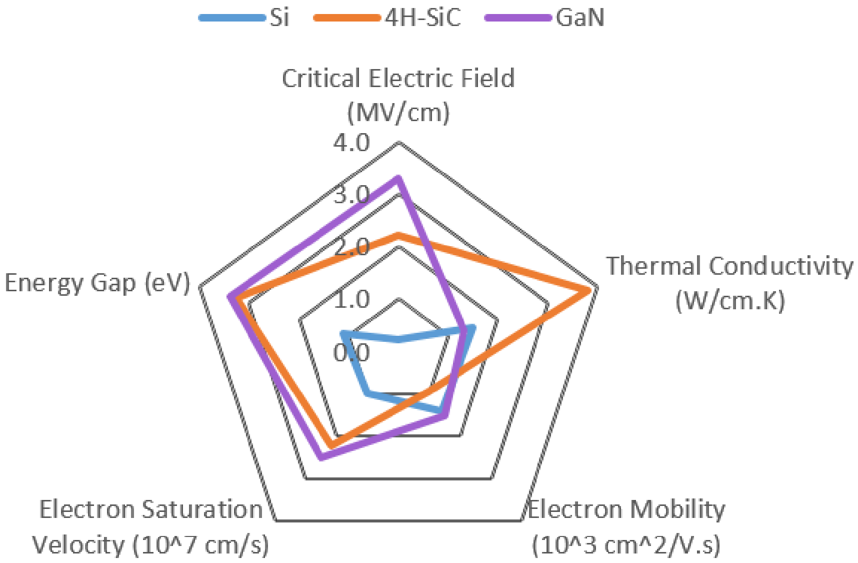


Figure 3.3: Material Properties of Si, SiC and GaN

switching. Overall, WBG semiconductor material characteristics result in a power transistor with lower ON resistance and switching losses than a Si power transistor with similar voltage and current capability. Despite SiC's outstanding performance in high-temperature applications, GaN's material properties are preferable in high-efficiency, high-frequency converters [57].

3.2.4 Third Quadrant Operation

GaN E-HEMT devices, like Si MOSFETs, are voltage-controlled devices that are controlled by the charging and discharging of their input capacitances C_{ISS}. GaN

E-HEMT devices, on the other hand, have much lower gate charges (Q_g) and gate biases (V_{gs}), typically $5 - 6V$, resulting in faster switching and lower drive loss. Another distinction between GaN E-HEMT devices and Si MOSFETs is the absence of a $p - n$ junction within the lateral structure, resulting in the absence of an intrinsic body diode and the absence of a reverse recovery charge (Q_{RR}), which means no reverse recovery loss. The 2DEG channel of the lateral GaN E-HEMT can conduct in the 3^{rd} quadrant without needing an anti-parallel diode, allowing for effective high-frequency operation in hard-switched topologies. One drawback of not including an intrinsic body diode is that the reverse voltage drop (V_{sd}), which is given in (3.1), is comparatively higher during the dead time. The 2DEG channel is turned on when the gate to drain voltage (V_{gd}) is above the threshold voltage ($V_{gd,th}$), which is roughly the same as the gate to source threshold voltage ($V_{gs,th}$). $R_{sd,rev}$ is the drain to source resistance during reverse conduction and is usually greater than the drain to source ON resistance ($R_{ds,on}$) [57]. V_{sd} becomes higher if the device is turned off with a negative gate bias, which increases the dead time conduction losses. These losses can be minimized by shortening the dead time or by using an adaptive dead time solution [58]. It is worth noting that avalanche breakdown does not occur in lateral GaN HEMT devices since they do not have a $p - n$ junction for voltage blocking. However, when subjected to sufficient overvoltage, they undergo disastrous dielectric failure, which is destructive and irreversible. As a result, GaN devices are normally rated at much lower voltages than their actual breakdown voltages [57, 59].

$$V_{sd} = V_{gd,th} - V_{gs} + I_d R_{sd,rev} \tag{3.1}$$

3.2.5 Current Collapse Effect

When a lateral GaN E-HEMT device is turned off, the drain to source voltage creates an electric field parallel to the conductive channel that exists in the epitaxial layer. This field can cause charges to become trapped on the surface or in the defects of the epitaxial layer. These trapped charges weaken the 2DEG and increase the drain to source ON resistance ($R_{ds,on}$). This effect causes a dynamic $R_{ds,on}$ for each switching cycle. The $R_{ds,on}$ value is proportional to the magnitude of the blocking voltage in the OFF state and also the duration of the OFF state [57, 60]. While most of the leading GaN device manufacturers have greatly reduced the current collapse issue, it is important to be mindful that the phenomenon still exists, as it can have an impact on modeling and loss analysis [61].

3.2.6 Short Circuit Behavior

The short circuit behavior, that is, hard switching fault, and degradation of a $650V/60A$ GaN E-HEMT under different test conditions are presented in [62]. The short-circuit behavior of the device at different gate drive voltages and temperatures ($25°C$ and $125°C$) has been investigated. At DC bus voltages ranging from $50V$ to $400V$, the device is subjected to a single pulse, $10\mu s$ us short-circuit tests. When the DC bus voltage is less than $300V$ and the gate voltage is $6V$, the devices under test pass all $10\mu s$ short-circuit tests. It is observed that at $10\mu s$, the gate to source current rises approximately 100 times higher than its nominal value because of the excessively high temperature of the main channel and gate structure. This rise causes a voltage drop on the external gate resistor, resulting in a voltage drop on the gate to source terminals of the device. When the DC bus voltage is equivalent to or greater than $350V$, device failures occur within $700ns$ at both $25°C$ and $125°C$. The same experiments are performed with $4V$ and $5V$ gate voltages, and it is reported that devices under test can withstand up to $400V$. It has also been stated in [62] that GaN E-HEMTs suffer from parameter changes in the main channel and gate structure that reduce the conductivity of the device after short-circuit tests. In [63], the short circuit behavior of $600-650V$ GaN cascodes, p-GaN HEMTs, and MISHEMTs devices is investigated. The experimental results showed that none of the analyzed devices could survive a short-circuit test at $400V$ DC bus voltage for $10\mu s$. Similar findings are published in [64] for $650V$ GaN E-HEMTs manufactured by GaN Systems Inc. Under a $400V$ DC bus voltage, nearly all of the measured devices failed in a very short period. In [62], it is advised to drive the device with a lower gate voltage under high DC bus voltages. In [63], it is proposed that gate current tracking by using a smart gate driver may be a useful state predictor for short circuit prevention in GaN E-HEMTs. According to [62] and [63], the response time of the protection circuit should be less than $300ns$ to turn the device off safely.

3.2.7 High dv/dt and Switching Frequency

Because of the inverter's PWM operation, the drive and motor terminal potentials change between the positive and negative sides of the DC bus. This situation pushes common mode currents to the ground of the system via parasitic capacitances and causes common mode EMI emission. When the frequency range from $150kHz$ to $30MHz$ is considered, the impact of high dV/dt on the inverter common mode voltage spectrum is relatively minimal; however, the effect of switching frequency is more important [65]. Severe over-voltages may arise at the motor terminals, and the magnitude of these voltages is directly related to the cable length and the rising time of the PWM pulses, and they may cause degradation of motor insulation [66]. High dV/dt and common-mode voltage can also produce bearing currents and grounding currents through stray capacitors inside a motor. In [67] and [68], these currents are investigated with suggested solutions.

3.2.8 Importance of Layout Design

The effect of parasitic inductances of device packages and PCB traces is increased by fast switching transients (di/dt) of GaN E-HEMT [57]. In [69], the influence of parasitic inductance of PCB layout on the efficiency and the overshoot voltage of the device is analyzed. According to the paper, a proper layout design can minimize high-frequency loop inductance by 40%, voltage overshoot by 35%, and total power loss by 10% when compared to a typical PCB design. Various approaches are used to evaluate the power loop inductance of the PCB layout. The PCB stray inductance for a particular loop form is computed analytically in [70], without the need for finite element analysis (FEA) or physical experiments.

The significance of gate loop inductance can be summarized as follows:

- It has the potential to affect switching performance by lowering the effective gate driver speed [71].
- It forms a resonant tank when combined with the gate capacitance of the device, which can cause an overvoltage at the gate terminal, and may exceed maximum

permissible gate-source voltage of the device, which is typically $6V$ [71, 72].

- In the half-bridge structure, the rapid dv/dt causes displacement current flow through the Miller capacitance (C_{gd}) of the power device. During the positive dv/dt of the drain to source voltage (V_{ds}) of the upper power device, the displacement current might cause the device to turn on. This is due to the low threshold gate to source voltage ($V_{gs,th}$), which is typically $1.4V$ but can be as low as $0.7V$, and this results in a shoot-through. During the negative dv/dt V_{ds} of the power device, a negative gate to source voltage (V_{gs}) can be generated that may exceed the negative limit of V_{gs}, which is typically $-10V$, and this decrease the reliability of the power device [73].

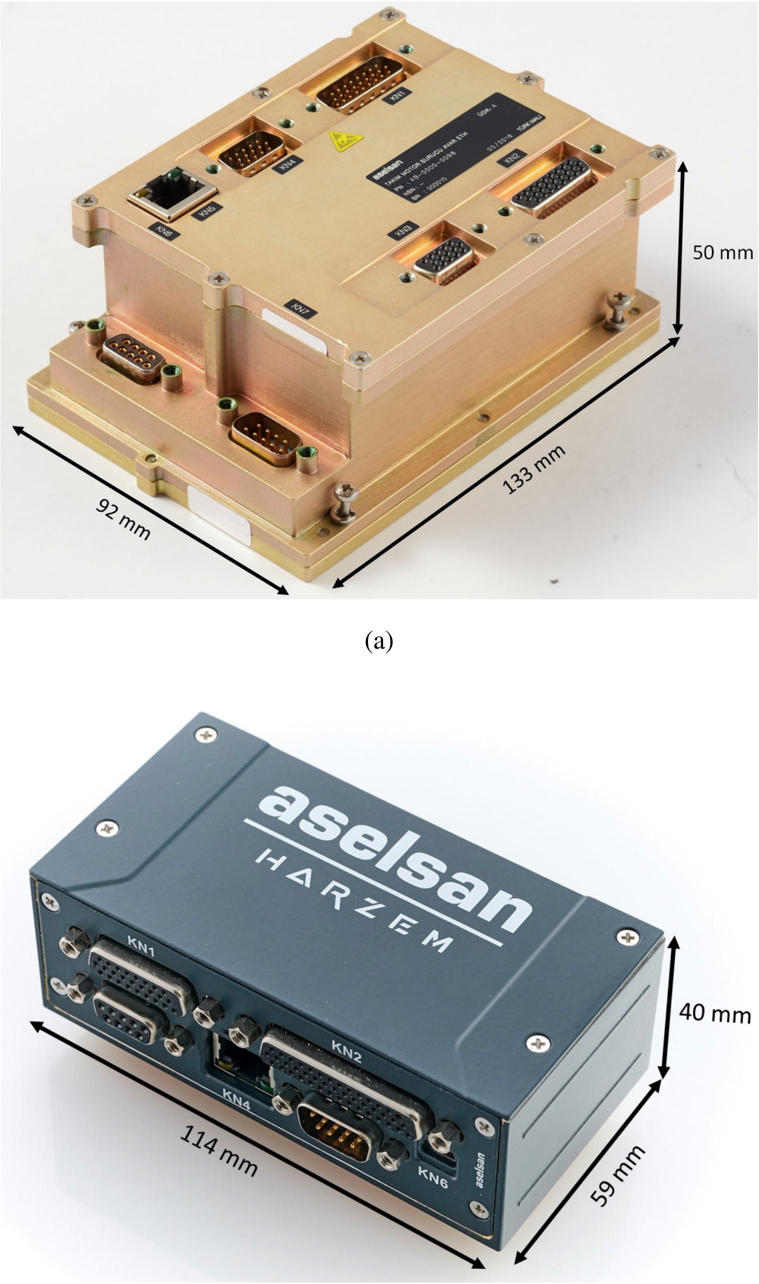
During the turn-off state of the power device, the impedance of the gate drive is so crucial that the gate should be kept down with a minimum of impedance [74].

Lateral GaN on Si transistor structure allows the simple integration of several power devices such that they can be electrically insulated from each other. A half-bridge combined with a gate driver in a single package enables customers to create smaller, more efficient, and more reliable solutions while eliminating problems such as gate overshoot and undershoot through optimum layout design [41, 75–77].

3.3 GaN E-HEMT VSI-Based Servo Drive Design

Chapter 2 concludes that, for high-bandwidth applications, the switching frequency should be increased. But as the switching frequency increases, the effects of the time-related terms in the nonlinearity in VSIs also increase. Since the GaN E-HEMT has a fast switching capability with a much shorter dead time, GaN E-HEMT based VSI fed PMSM is preferred in high-bandwidth applications.

A GaN E-HEMT VSI-based three-phase, two-level servo drive is developed as shown in Fig. 3.4b to replace its Si MOSFET VSI-based equivalent shown in Fig. 3.4a. The size of the designed servo drive is about 44% of the previous one, and the weight of the GaN E-HEMT VSI-based servo drive is $0.311\ kg$, whereas the Si MOSFET VSI-based servo drive is $0.612\ kg$. Table 3.2 lists the features of the GaN E-HEMT


50 mm
133 mm
92 mm
KN1
KN2
KN3
KN4
KN5
KN6
KN7
KN8
aselsan
HARZEM
KN1
KN2
KN4
KN6
40 mm
114 mm
59 mm

(a)

(b)

Figure 3.4: Dimensions of the servo drives:(a) The Si MOSFET VSI-based servo drive (b) The GaN E-HEMT VSI-based servo drive

VSI-based servo drive.

The GaN E-HEMT VSI-based servo drive is made up of three cards: an inverter card, a DSP card, and an interface card. The basic functions of the cards and the signals

Table 3.2: Features of GaN E-HEMT VSI based Servo Drive

Parameters	Value
Nominal operating voltage	$24V$
Maximum operating voltage	$48V$
Operating temperature range	$-40°C$ to $65°C$
Storage temperature range	$-40°C$ to $85°C$
Peak continuous output phase current	$10A$
Dimensions (length, width, height)	$114mm$ x $59mm$ x $40mm$
Weight	$0.311kg$
Electromagnetic compatibility	MIL-STD-461F
Environmental conditions compatibility	MIL-STD-810G

between them are given in Fig. 3.5.

3.3.1 The Inverter Card of the GaN E-HEMT VSI-based Servo Drive

Some of the available GaN E-HEMTs in the industry are given in Table 3.3 with the basic parameters. In the table, the figure of merit (FOM) is calculated by multiplying the gate charge (Q_g) with the drain to source ON resistance (R_{ds}). So a lower FOM means better performance. According to the concerns discussed in subsection 3.2.8, a half-bridge (HB) combined with a gate driver in a single package enables the design of smaller, more efficient, and more reliable solutions while eliminating problems such as gate overshoot and undershoot through optimum layout design. For this reason, although LMG5200 has a higher FOM compared to other GaN E-HEMTs in the table, it is utilized for one of the legs in the inverter card. It should be noted that EPC2152 was introduced in March 2020, and it was not available during the design of the inverter card and is still in engineering status.

The following functionalities are included with the inverter card:

- Power input EMI filters and protection circuits such as a TVS for high voltage, a fuse for a short circuit, and a reverse input connection,

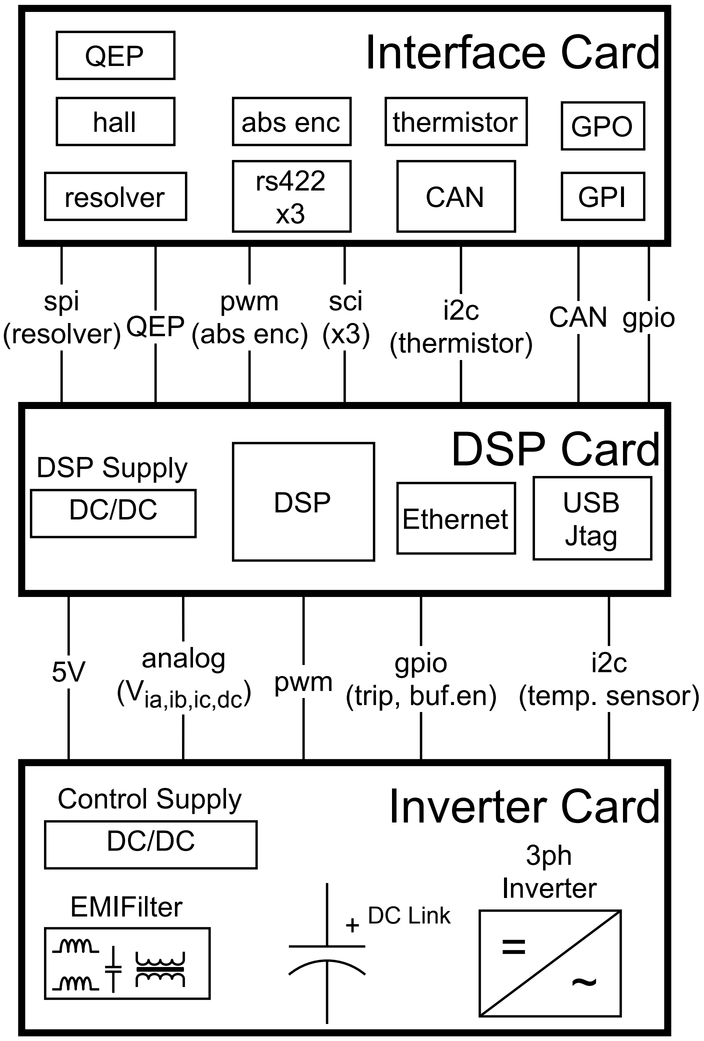
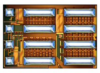
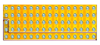
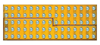
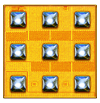
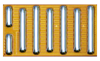
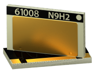

Interface Card
QEP
hall
abs enc
thermistor
GPO
resolver
rs422 x3
CAN
GPI
spi (resolver)
QEP
pwm (abs enc)
sci (x3)
i2c (thermistor)
CAN
gpio
DSP Card
DSP Supply
DC/DC
DSP
Ethernet
USB Jtag
5V
analog ($V_{ia,ib,ic,dc}$)
pwm
gpio (trip, buf.en)
i2c (temp. sensor)
Inverter Card
Control Supply
DC/DC
EMIFilter
+ DC Link
3ph Inverter
=
~

Figure 3.5: The basic functions of the cards of the GaN E-HEMT VSI-based servo drive and the signals between them.

- Phase current sensing with a shunt resistor,
- DC link voltage monitoring,
- Overcurrent protection for phases,
- PCB temperature monitoring,
- Power switch for the motor brake.

The block diagram of the basic functions of the inverter card and the signals between the inverter and the DSP card are given in Fig. 3.6.

Table 3.3: Available GaN E-HEMTs

Part No	Type	V_{ds} (V)	I_d (A)	R_{ds} $(m\Omega)$	Q_g (nC)	Q_{oss} (nC)	FOM $(m\Omega * nC)$	Dimensions (mm x mm)
LMG5200 ([78])	HB+Drv.	80	10	15	3.8	21	57	8.0 x 6.0
EPC2152 ([79])	HB+Drv.	80	15	8.5	NA	NA	NA	3.9 x 2.6 
EPC2105 ([80])	HB	80	10	10	2.7	11	27	6.05 x 2.3 
EPC2103 ([81])	HB	80	30	4	6.5	30	26	6.05 x 2.3 
EPC2214 ([82])	Single	80	10	15	1.8	8	27	1.35 x 1.35 
EPC2065 ([83])	Single	80	60	2.7	9.4	33	25.4	3.5 x 1.95 
GS61008T ([84])	Single	100	65	7	8	20	56	7.0 x 4.0 

Because the servo drive is supplied by a DC source, no current ripple is expected to be injected into the DC-link capacitor. The DC source provides the load's average current. The DC-link capacitor, on the other hand, supplies high-frequency current harmonics generated by PWM operation. The magnitude of the high-frequency current harmonics is determined by the type of PWM, modulation index, the load current, and load angle. These harmonics can be calculated as in (3.2) for continuous PWMs such as SPWM and SVPWM [85].

$$K_{dc} = \frac{{I_{hrms}}^2}{{I_{1rms}}^2} = \frac{2\sqrt{3}}{\pi^2} M_i + \left(\frac{8\sqrt{3}}{\pi^2} - \frac{18}{\pi^2} M_i \right) M_i \cos^2 \varphi \tag{3.2}$$

where;

K_{dc} : DC link current ripple factor

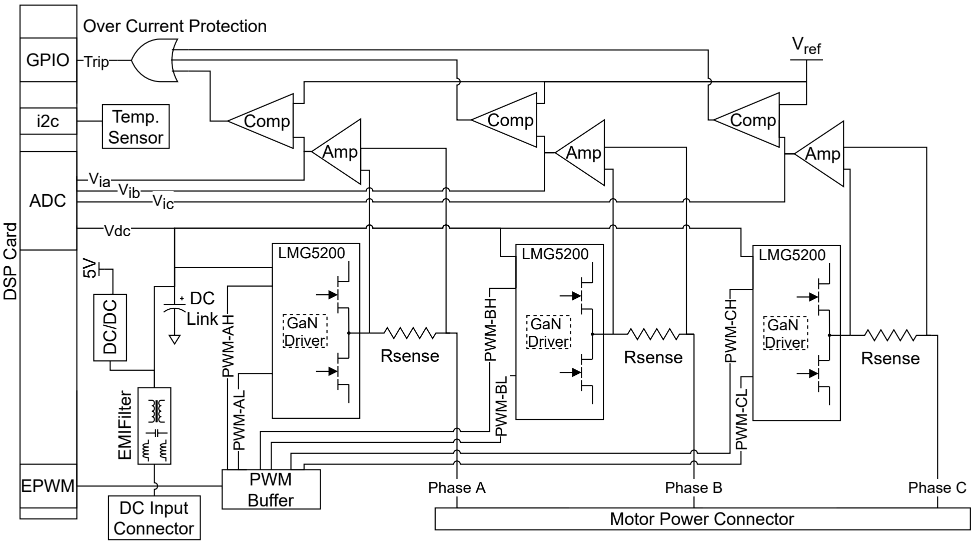
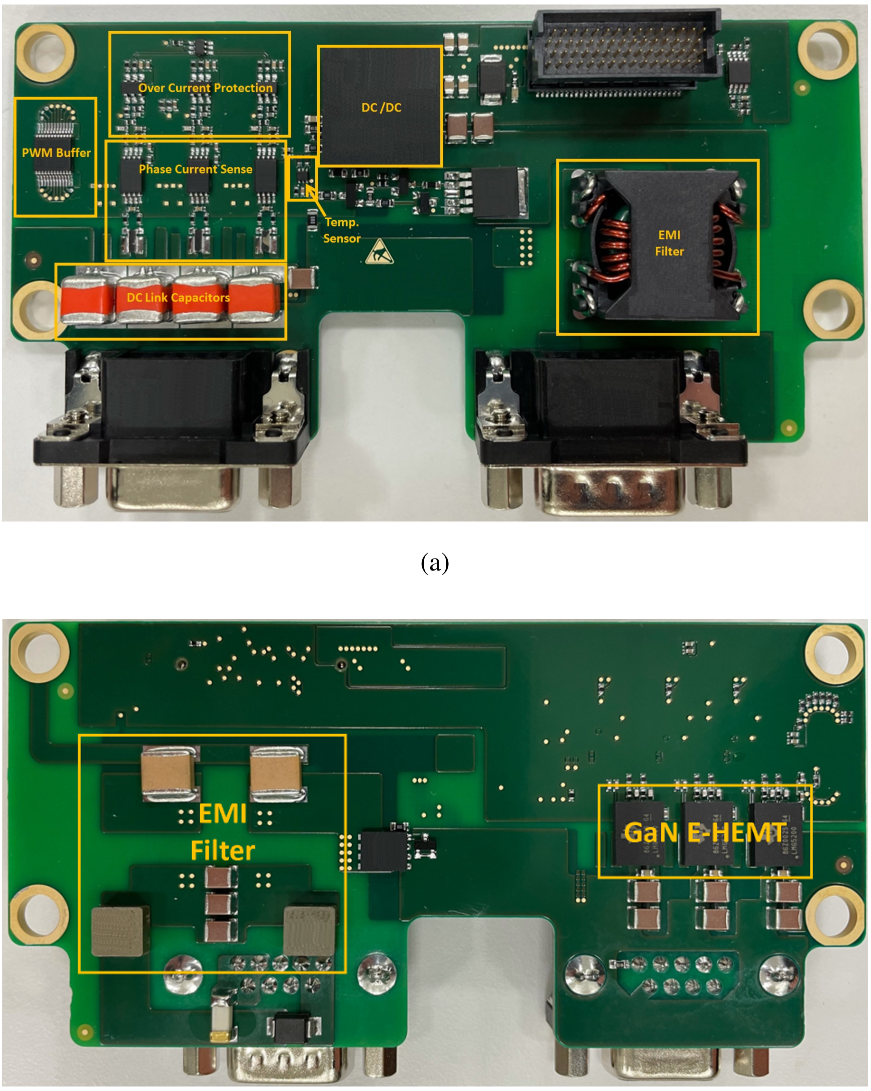

DSP Card
GPIO
i2c
ADC
EPWM
Over Current Protection
Trip
Temp. Sensor
V_ref
Comp
Comp
Comp
Amp
Amp
Amp
Via
Vib
Vic
Vdc
5V
DC/DC
DC Link
LMG5200
LMG5200
LMG5200
GaN Driver
GaN Driver
GaN Driver
Rsense
Rsense
Rsense
PWM-AH
PWM-AL
PWM-BH
PWM-BL
PWM-CH
PWM-CL
EMIFilter
PWM Buffer
DC Input Connector
Phase A
Phase B
Phase C
Motor Power Connector

Figure 3.6: The block diagram of the inverter card and the signals between the inverter and DSP cards of the GaN E-HEMT VSI-based servo drive.

$\mathrm{I_{hrms}}$: High-frequency current harmonics (rms)
$\mathrm{I_{1rms}}$: Fundamental load current (rms)
$\mathrm{M_i}$: Modulation index
$\cos\varphi$: Load power factor

The maximum K_{dc} value, which is about 0.42, occurs when M_i is about 0.48 and the load power factor ($\cos\varphi$) is 1. According to equation (3.2), the rms value of the high-frequency harmonic current will be about $4.6A$ at full load, which is 7 A_{rms} for LMG5200. Four $50V$, $47uF$ solid tantalum capacitors each allows 1.1 A_{rms} ripple current at 100 kHz [86] are used in parallel to distribute power loss due to harmonic current ripples and they are supported with ceramic capacitors as well. The solid tantalum type capacitor is preferred due to its stable ESR, capacitance, and DC leakage (DCL) characteristics over changing temperature, voltage, and time. It also lacks shelf-life limitations, wear-out mechanisms, and end-of-life degradation [87].

The details of the EMI filter part of the inverter card will be given in Section 3.3.6. Fig. 3.7a and Fig. 3.7b depict the top and bottom sides of the inverter card, respectively.


Over Current Protection
DC /DC
PWM Buffer
Phase Current Sense
Temp. Sensor
DC Link Capacitors
EMI Filter
EMI Filter
GaN E-HEMT

(a)

(b)

Figure 3.7: The inverter card of the GaN E-HEMT VSI-based servo drive (a) top side (b) bottom side

3.3.2 The DSP Card of the GaN E-HEMT VSI-based Servo Drive

The DSP card shown in Fig. 3.8 has a dual-core microcontroller (F28379D), an isolated USB-JTAG emulator, and a fully compliant 10/100/1000Base-T network ethernet controller.

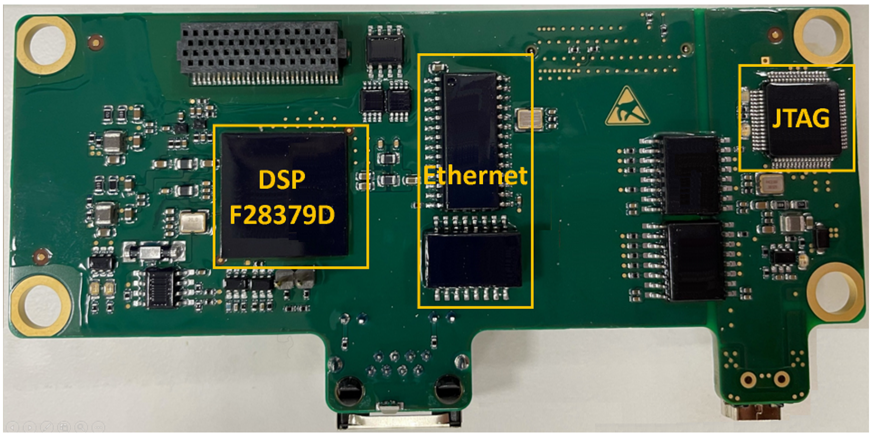


Figure 3.8: The DSP card of the GaN E-HEMT VSI-based servo drive

3.3.3 The Interface Card of the GaN E-HEMT VSI-based Servo Drive

The interface card includes the following features, and Fig. 3.9 shows the interface card:

- Motor feedback interfaces such as resolver, hall, incremental encoder,
- Three serial configuration interfaces,
- CAN interface with ISO 11898 standard,
- Synchronous serial interface for an absolute encoder,
- Four general-purpose isolated outputs,
- Six general-purpose inputs.

3.3.4 The GaN E-HEMT VSI-based Servo Drive

Fig. 3.10 depicts the composition of the GaN E-HEMT VSI-based servo drive from the three cards stated above.

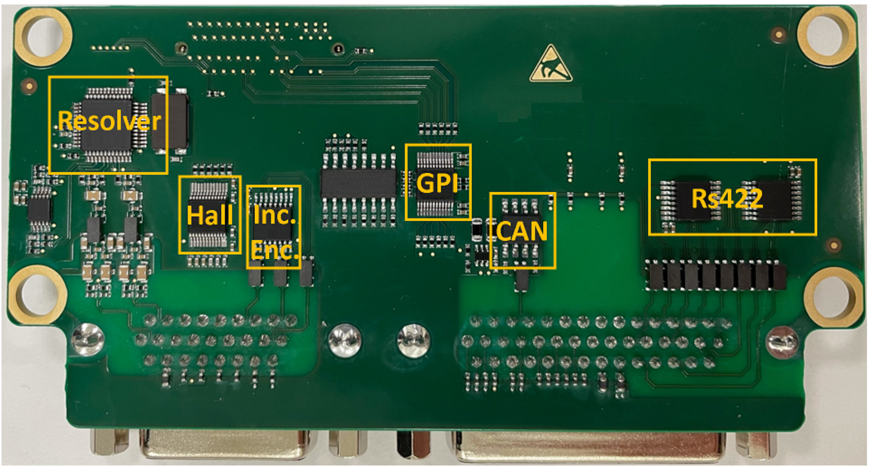


Figure 3.9: The interface card of the GaN E-HEMT VSI-based Servo Drive

3.3.5 Load Tests of the GaN E-HEMT VSI-based Servo Drive

3.3.5.1 Efficiency Determination of the GaN E-HEMT VSI-based Servo Drive

The efficiency of the GaN E-HEMT VSI-based servo drive is evaluated by feeding a PMSM at $24\ V$ and $48\ V$ supply voltages. To control the PMSM, the field-oriented control (FOC) method is used with the space vector PWM (SVPWM). The block schema of the FOC is given in Fig. 3.11.

The desired load torque is applied via a torque loader. The block diagram of the test setup is shown in Fig. 3.12, where the parts included in loss calculations are demonstrated.

Where;

$\mathrm{V_{dc}}$: DC supply voltage

$\mathrm{I_{dc}}$: DC supply current

$\mathrm{R_{dc\_cable}}$: Cable resistance of the DC power supply

$\mathrm{L_{s}}$: Serial inductor for EMI filtering

$\mathrm{N_{mos}}$: N channel MOSFET for reverse voltage protection

$\mathrm{R_{sense}}$: Resistor for the output phase current measurement

$\mathrm{R_{m\_cable}}$: Cable resistance of motor power connection

$\mathrm{I_{o\_rms}}$: Phase output RMS current

τ_{L} : Load torque

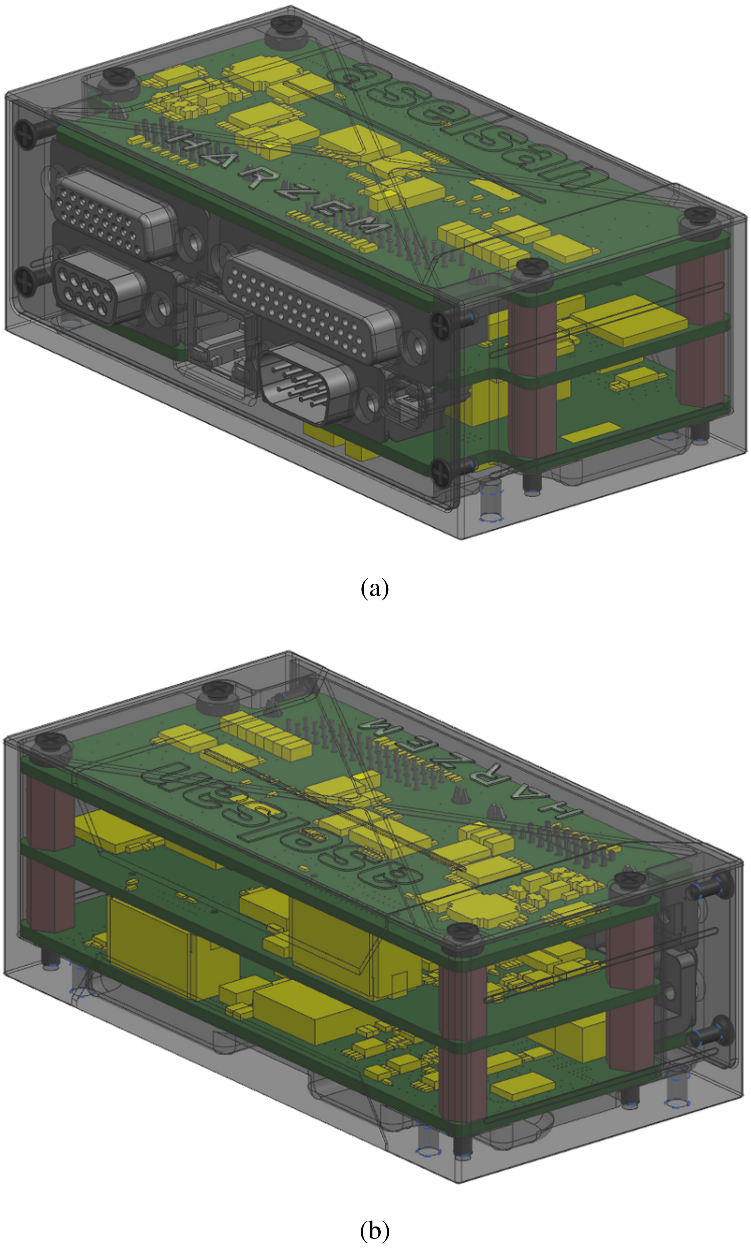

HARZEM
aselsan
(a)
HARZEM
aselsan
(b)

Figure 3.10: Inside view of the GaN E-HEMT VSI-based servo drive (a) Front view (b) Back view

ω_{L} : Load angular speed (rad/s)

n_{L} : Load speed (rpm)

The parameters of the PMSM and the experimental setup are given in Table 3.4.

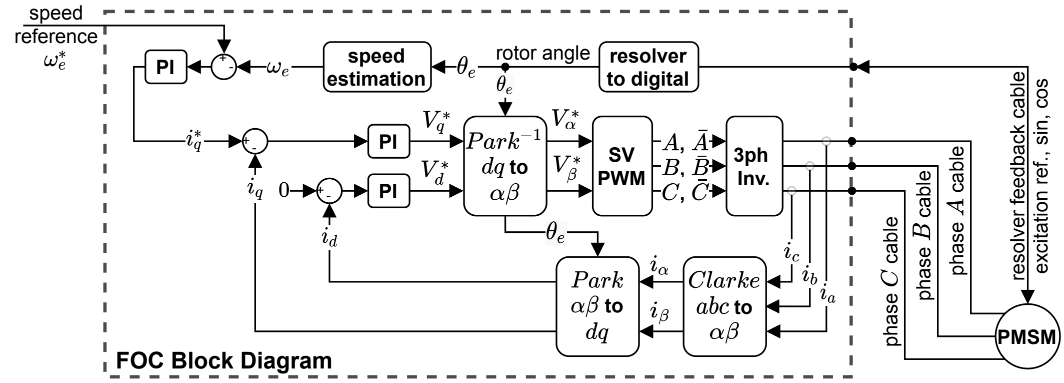

speed reference ω_e^*
PI
ω_e
speed estimation
θ_e
rotor angle
resolver to digital
θ_e
i_q^*
PI
V_q^*
V_d^*
i_q
0
PI
i_d
$Park^{-1}$ dq to $\alpha\beta$
V_α^*
V_β^*
SV PWM
$A, \bar{A}$
$B, \bar{B}$
$C, \bar{C}$
3ph Inv.
θ_e
i_c
i_b
i_a
i_α
i_β
$Park$ $\alpha\beta$ to dq
$Clarke$ abc to $\alpha\beta$
FOC Block Diagram
phase C cable
phase B cable
phase A cable
resolver feedback cable
excitation ref., sin, cos
PMSM

Figure 3.11: The block schema of the FOC to control the PMSM

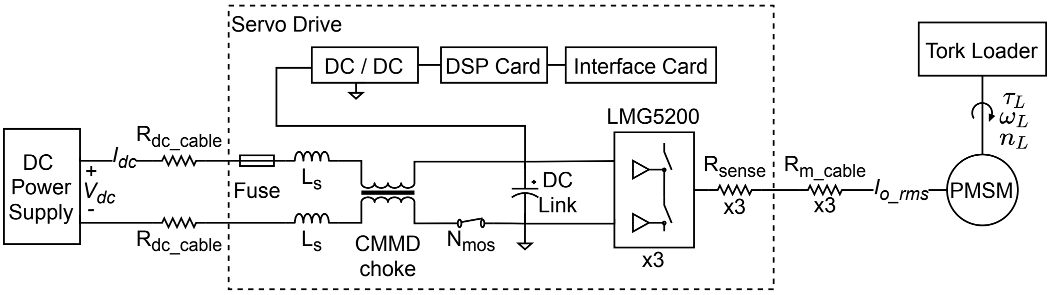

Servo Drive
DC / DC
DSP Card
Interface Card
Tork Loader
τ_L
ω_L
n_L
DC Power Supply
R_{dc_cable}
I_{dc}
+
V_{dc}
-
Fuse
L_s
L_s
CMMD choke
N_{mos}
DC Link
LMG5200
x3
R_{sense}
x3
R_{m_cable}
x3
I_{o_rms}
PMSM

Figure 3.12: The block diagram of the test setup for efficiency evaluation of the GaN E-HEMT VSI-based servo drive.

Table 3.4: PMSM and Experimental Setup Parameters

Parameters	Value	Parameters	Value
PMSM torque constant, K_t	0.91 Nm/A_{rms}	DC supply cable length, l_1	1.5 m
PMSM BEMF constant	58.8 V_{rms}/K_{rpm}	Motor power cable (AWG20) length, l_2	2 m
PMSM line-to-line inductance	4.4 mH	Motor power cable (AWG16) length, l_3	0.25 m
PMSM line-to-line resistance, R_m	0.57 Ω	AWG20 cable resistance per meter, k_{AWG20}	33.29 $m\Omega$
PMSM static friction, T_f	0.3 Nm	AWG16 cable resistance per meter, k_{AWG16}	13.17 $m\Omega$
PMSM viscous damping, K_{dv}	0.04 Nm/K_{rpm}	DC supply cable resistance, R_{dc_cable}	16.65 $m\Omega$
PMSM number of pole-pairs	5	Motor cable resistance, R_{m_cable}	36.59 $m\Omega$
PMSM rated power	2.91 kW	Measured DC supply cable resistance, $R_{dc\_cable\_meas}$	14.95 $m\Omega$
		Measured motor cable resistance, $R_{m\_cable\_meas}$	33.68 $m\Omega$

The resistance of the DC supply cable is calculated in (3.3) where three AWG20 cables are paralleled for both the positive and negative sides.

$$R_{dc\_cable} = (l_1 * k_{AWG20})/3 \tag{3.3}$$

Table 3.5: Servo Drive Parameters

Parameters	Value	Parameters	Value
Switching frequency, f_{sw}	100 kHz	Dead time, t_{dead}	20 nS
Current consumption of integrated circuits @24V, I_{ICs24V}	131.91 mA	DC link capacitor ESR, R_{dc_link}	240 $m\Omega$
Current consumption of integrated circuits @48V, I_{ICs48V}	88.27 mA	DC link ripple current factor, K_{dc}	0.42
L_s serial inductor ESR, R_{Ls}	12.7 $m\Omega$	R_{sense} current sense resistor	5 $m\Omega$
Fuse resistance, R_{FUSE}	4.9 $m\Omega$	LMG5200 slew rate (rise time + fall time), k_{trf}	25 V/ns
Common mode (CMMD) choke ESR, R_{CMMD}	3.75 $m\Omega$	LMG5200 drain to source resistance, $R_{ds\_LMG5200}$	15 $m\Omega$
N_{mos} drain to source resistance, $R_{ds\_N_{mos}}$	3.4 $m\Omega$	LMG5200 output charge, Q_{oss}	21 nC
		LMG5200 source to drain voltage, u_{sd}	2.75 V

The resistance of the motor phase cable is calculated in (3.4), where two AWG20 cables are paralleled and in series with an AWG16 cable for each phase.

$$R_{m\_cable} = (l_2 * k_{AWG20})/2 + (l_3 * k_{AWG16}) \tag{3.4}$$

The parameters of the GaN E-HEMT VSI-based servo drive are given in Table 3.5.

It is assumed that the output phase currents are sinusoidal and that the PMSM is balanced.
The calculations to find the servo drive efficiency experimentally are given step by step in Table 3.6.

Table 3.7 shows the step-by-step procedures for calculating the servo drive efficiency analytically.

The efficiency estimation of the servo drive is given in Fig. 3.13 at $24V$ DC supply voltage, where the blue line shows the efficiency based on the experimental results according to Table 3.6, and the orange line shows the efficiency based on the analytical calculations according to Table 3.7. The loss distributions of the parts of the servo drive are depicted in Fig. 3.14, which is calculated analytically as expressed in Table 3.7. It should be noted that the power loss of ICs is dominant at low power outputs. The typical current consumption values of the ICs are utilized to estimate ICs loss; variations in these typical values have a direct impact on the results. This situation explains the discrepancy between experimental and analytical estimates of servo drive efficiency at low power outputs. On the other hand, the typical values of

Table 3.6: Experimentally Efficiency Calculation Procedure

Parameters	Equation
Power at load	$P_L = \tau_L \omega_L$ (3.5)
PMSM copper loss (measurement)	$P_{m\_cu\_meas} = 3(I_{o\_rms\_meas})^2(R_m/2)$ (3.6)
PMSM friction loss	$P_{m\_f} = (T_f \omega_L) + ((K_{dv}(60\omega_L/2\pi)/1000)\omega_L)$ (3.7)
Motor cable loss (measurement)	$P_{m\_cable\_meas} = 3(I_{o\_rms\_meas})^2 R_{m\_cable\_meas}$ (3.8)
Servo drive output power (measurement)	$P_{out\_meas} = P_L + P_{m\_cu\_meas} + P_{m\_f} + P_{m\_cable\_meas}$ (3.9)
DC power cable loss (measurement)	$P_{dc\_cable\_meas} = 2(I_{dc\_meas})^2 R_{dc\_cable\_meas}$ (3.10)
DC supply output power (measurement)	$P_{dc\_supply\_out\_meas} = V_{dc} I_{dc\_meas}$ (3.11)
Servo drive input power (measurement)	$P_{in\_meas} = P_{dc\_supply\_out\_meas} - P_{dc\_cable\_meas}$ (3.12)
Servo drive efficiency (measurement)	$\eta_{meas} = P_{out\_meas}/P_{in\_meas}$ (3.13)

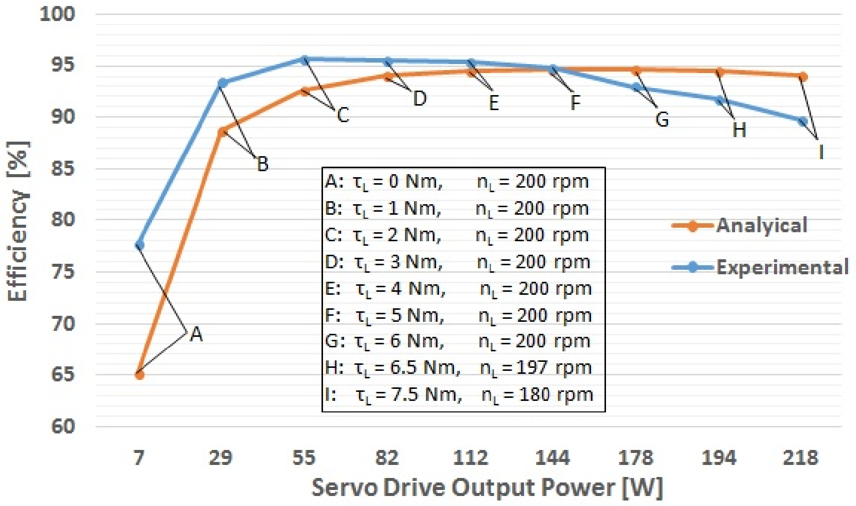


Figure 3.13: The efficiency estimation of the GaN E-HEMT VSI-based servo drive at 24V. The blue line is the efficiency based on the experimental results, and the orange line is the efficiency based on the analytical calculations.

the power device's conduction resistors are used, resulting in a higher analytic efficiency estimation for high power outputs. However, when the junction temperature of the power devices increases, conduction losses also increase.

The efficiency estimation and the loss distributions of the parts of the servo drive at

Table 3.7: Analytically Efficiency Calculation Procedure

Parameters	Equation
Output RMS phase current	$I_{o\_rms} = (\tau_L + T_f + (K_{dv}(60\omega_L/2\pi)/1000))/(K_t)$ (3.14)
PMSM copper loss	$P_{m\_cu} = 3(I_{o\_rms})^2(R_m/2)$ (3.15)
Motor cable loss	$P_{m\_cable} = 3(I_{o\_rms})^2 R_{m\_cable}$ (3.16)
Servo drive output power	$P_{out} = P_L + P_{m\_cu} + P_{m\_f} + P_{m\_cable}$ (3.17)
Current sense resistor loss	$P_{R_{sense}} = 3(I_{o\_rms})^2 R_{sense}$ (3.18)
LMG5200 3^{rd} quadrant conduction loss	$P_{GaN\_3^{rd}} = 3(I_{o\_rms}\sqrt{2}/\pi)u_{sd}(2t_{dead})f_{sw}$ (3.19)
LMG5200 conduction loss	$P_{GaN\_cond} = 3(I_{o\_rms})^2 R_{ds\_LMG5200}$ (3.20)
LMG5200 switching loss	$P_{GaN\_sw} = 3(V_{dc}(I_{o\_rms}\sqrt{2}/\pi)(V_{dc}/k_{trf}) + 2Q_{oss}V_{dc})f_{sw}$ (3.21)
DC link capacitor harmonic loss	$P_{DC\_link} = K_{dc}(I_{o\_rms})^2(R_{dc\_link}/4)$ (3.22)
Power loss of integrated circuits (ICs)	$P_{ICs\_Vdc} = V_{dc}I_{ICsVdc}$ (3.23)
Servo drive input current	$I_{dc} = (P_{out} + P_{R_{sense}} + P_{GaN\_3^{rd}} + P_{GaN\_cond} + P_{GaN\_sw}$ $+ P_{DC\_link} + P_{ICs\_Vdc})/V_{dc}$ (3.24)
N_{mos} conduction loss	$P_{N_{mos}\_cond} = (I_{dc})^2 R_{ds\_N_{mos}}$ (3.25)
CMMD choke loss	$P_{CMMD} = (I_{dc})^2 R_{CMMD}$ (3.26)
L_s serial inductor loss	$P_{L_s} = 2(I_{dc})^2 R_{L_s}$ (3.27)
Fuse loss	$P_{FUSE} = (I_{dc})^2 R_{FUSE}$ (3.28)
Servo drive input power	$P_{in} = P_{out} + P_{R_{sense}} + P_{GaN\_3^{rd}} + P_{GaN\_cond} + P_{GaN\_sw} + P_{DC\_link}$ $+ P_{ICs\_Vdc} + P_{N_{mos}\_cond} + P_{CMMD} + P_{L_s} + P_{FUSE}$ (3.29)
Servo drive efficiency	$\eta = P_{out}/P_{in}$ (3.30)

$48V$ DC supply voltage are given in Fig. 3.15 and Fig. 3.16, respectively. The blue line shows the efficiency based on the experimental results according to Table 3.6, and the orange line shows the efficiency based on the analytical calculations according to Table 3.7. As can be seen from the figures, the conduction losses become dominant as the output power increases. When the supply voltage is increased to $48V$, the

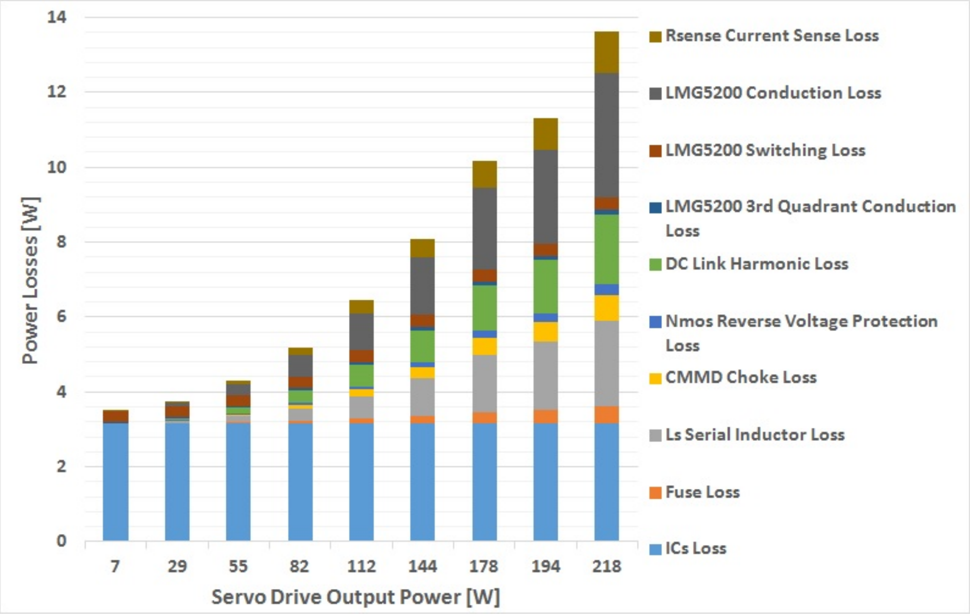


Figure 3.14: The loss distributions of the parts of the GaN E-HEMT VSI-based servo drive at $24V$.

conduction current value is decreased for the same power. For this reason, lower conduction losses at high power output result in higher efficiency at $48V$ DC supply voltage. This result also shows the switching loss of the GaN E-HEMT (LMG5200) is still not dominant, although the working voltage has been doubled.

The power density of the GaN E-HEMT VSI-based servo drive is calculated to be around $1.4\ W/cm^3$.

3.3.5.2 Thermal Analysis of the GaN E-HEMTs of the Servo Drive

A thermal investigation has been performed on the servo drive's GaN E-HEMTs (LMG5200). As an $R-L$ load, a PMSM with a brake is used. Four tests were conducted to achieve this goal. The supplied voltage, switching frequency, and output phase current have all been altered.
An infrared camera is used to monitor the case temperatures (T_C) of the GaN E-HEMTs, and a snapshot of the measurement is captured at a thermal steady state. The formulas (3.19), (3.20), and (3.21) in Table 3.7 are used to compute the case

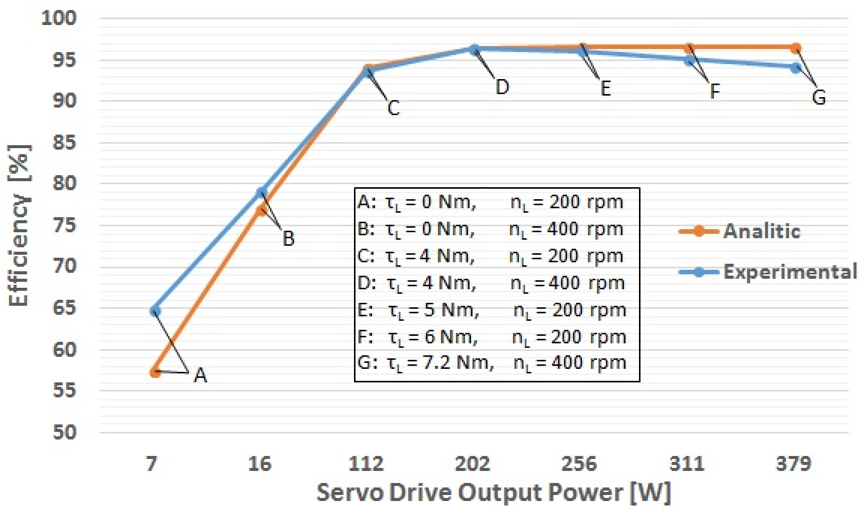


Figure 3.15: The efficiency estimation of the GaN E-HEMT VSI-based servo drive at $48V$. The blue line is the efficiency based on the experimental results, and the orange line is the efficiency based on the analytical calculations.

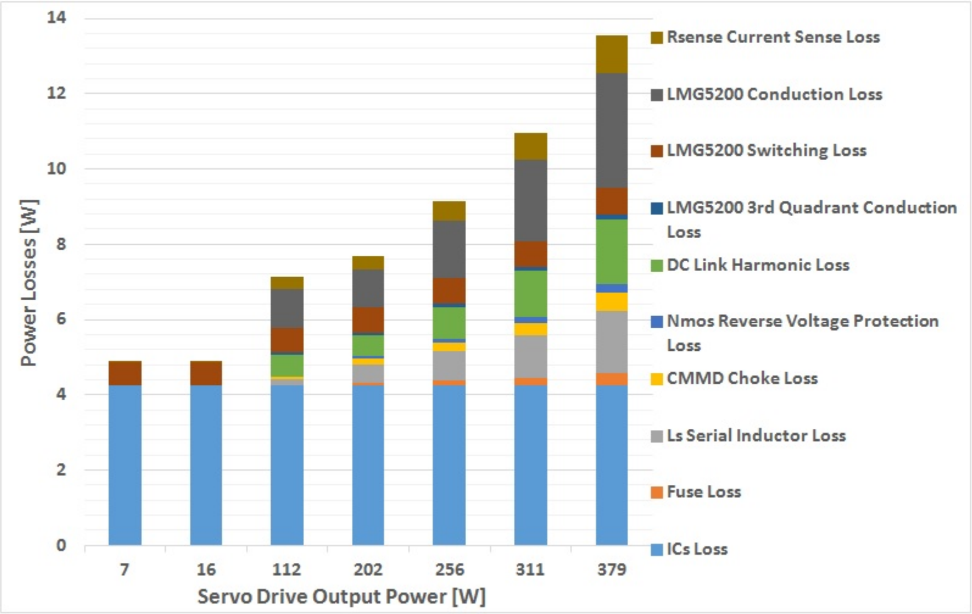


Figure 3.16: The loss distributions of the parts of the GaN E-HEMT VSI-based servo drive at $48V$.

temperatures of the GaN E-HEMTs.

$$\begin{aligned} P_{GaN\_total} &= P_{GaN\_3^{rd}} + P_{GaN\_cond} + P_{GaN\_sw} + P_{GaN\_gate\_drv} \\ T_C &= T_A + R_{CA} P_{GaN\_total} \end{aligned} \tag{3.31}$$

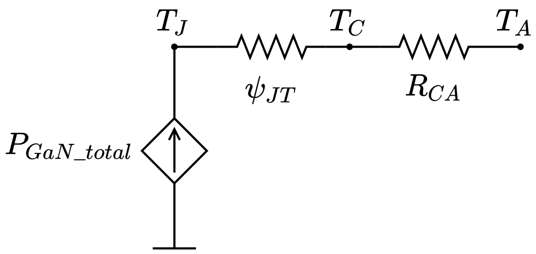


Figure 3.17: The simplified equivalent thermal circuit to calculate the junction temperature of the GaN E-HEMTs.

where T_A is the ambient temperature, and R_{CA} is the case-to-ambient thermal resistance. The loss of the gate driver ($P_{GaN\_gate\_drv}$) of the GaN E-HEMT is also included in the calculation and is taken from the datasheet. The thermal resistance R_{CA} of the GaN E-HEMTs is determined by experimental tests. The thermal resistance R_{CA} of GaN E-HEMTs varies depending on the PCB layout, such as copper area, position of the component, number of vias etc. The junction temperature of the GaN E-HEMTs can be calculated using the following equation based on the case temperature T_C, where ψ_{JT} is the junction-to-top characterization parameter of the GaN E-HEMT [88]. The simplified equivalent thermal circuit is given in Fig. 3.17.

$$T_J = T_C + \psi_{JT} P_{GaN\_total} \tag{3.32}$$

The common parameters for all thermal tests are given in Table 3.8, and Table 3.9 lists the other parameters utilized in these tests. The 3^{rd} quadrant conduction and the switching losses of the GaN E-HEMTs are also included in the table because they do not differ from phase to phase.

The thermal images of the tests are given in Fig. 3.18. The expected case temperatures T_C of the GaN E-HEMTs and the comparisons of them with measurements are given in Table 3.10. The drain to source resistance of GaN E-HEMTs is determined by considering the temperature of the device. It is worth noting that, even though the switching frequency is doubled in test-#3 while the supply voltage and phase output current remain constant compared with test-#1, the case temperatures of the GaN E-HEMTs only rise by about $3°C$. As shown in the table, the estimation errors for the

Table 3.8: Common Parameters for Thermal Experiment Tests

Parameters	Value	Parameters	Value
Load resistance	$0.48\ \Omega$	Phase A LMG5200 R_{CA}	$83.26\ [°C/W]$
Load inductance	$2.5\ mH$	Phase B LMG5200 R_{CA}	$85.56\ [°C/W]$
dead time, t_{dead}	$10\ ns$	Phase C LMG5200 R_{CA}	$77.69\ [°C/W]$
Sinusoidal I_{out} frequency	$6\ Hz$	LMG5200 output charge, Q_{oss}	$21\ nC$
		LMG5200 slew rate (rise time + fall time), k_{trf}	$25\ V/ns$

Table 3.9: Thermal Experiment Tests Parameters

Parameters	Test-#1	Test-#2	Test-#3	Test-#4
Supply Voltage, V_{dc}	$24\ V$	$24\ V$	$24\ V$	$48\ V$
Sinusoidal (rms) output current, I_{out_rms}	$4.87\ A_{rms}$	$6.83\ A_{rms}$	$4.87\ A_{rms}$	$4.96\ A_{rms}$
Switching frequency, f_{sw}	$100\ kHz$	$100\ kHz$	$200\ kHz$	$200\ kHz$
Ambient temperature, T_A	$25\ °C$	$24.5\ °C$	$24.5\ °C$	$24\ °C$
Gate drive loss,$P_{GaN\_gate\_drv}$	$6\ mW$	$6\ mW$	$11\ mW$	$11\ mW$
Source to drain voltage,u_{sd}	$2.14\ V$	$2.24\ V$	$2.14\ V$	$2.14\ V$
3^{rd} quadrant conduction loss, $P_{GaN\_3^{rd}}$	$9\ mW$	$14\ mW$	$20\ mW$	$20\ mW$
Switching loss, P_{GaN_sw}	$106\ mW$	$108\ mW$	$212\ mW$	$444\ mW$

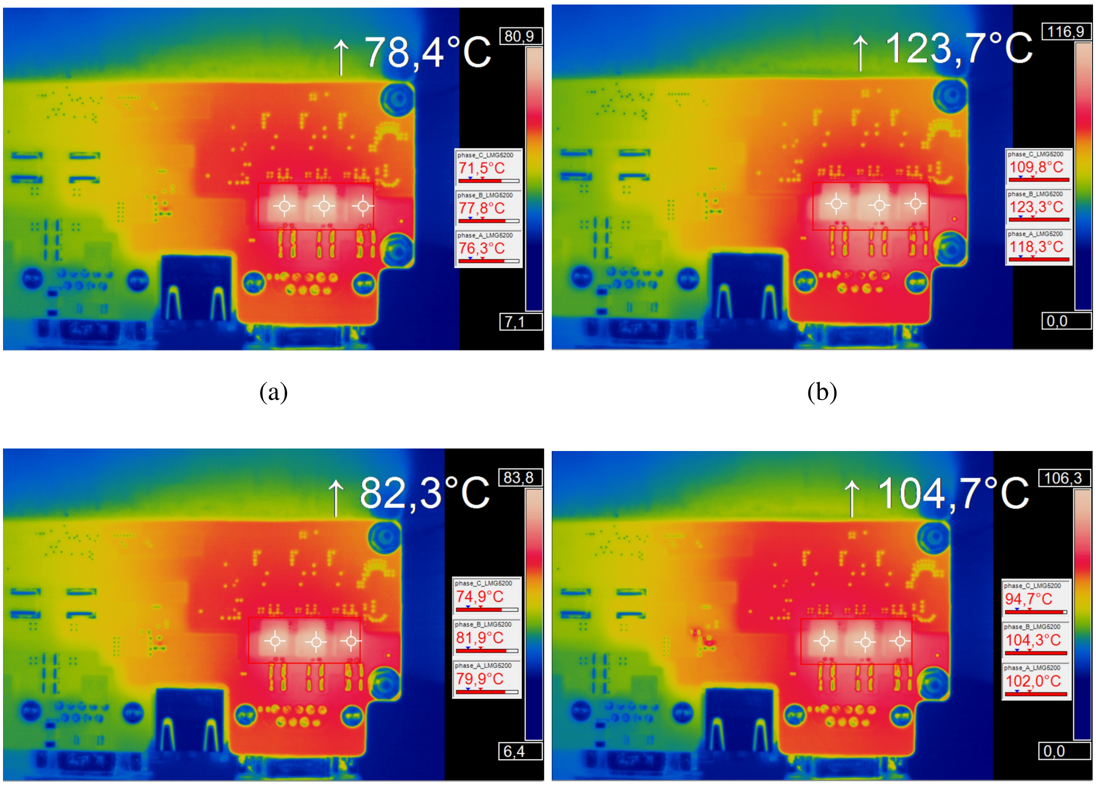
case temperatures of the GaN E-HEMTs remain below 6%.

3.3.6 Conducted Emission Tests of the GaN E-HEMT VSI-based Servo Drive

Conducted emission tests, CE101 and CE102, are performed on the GaN E-HEMT VSI-based servo drive to ensure that electromagnetic emissions from the servo drive do not exceed the defined criteria for power input leads, including returns, as specified by MIL-STD-461F.

According to Fig. 3.19, the common mode and differential mode cut-off frequencies can be computed using the following equations (3.33) and (3.34).

$$f_{cm} = \frac{1}{2\pi\sqrt{(L_{cm} + L_{dm}/2)(2C_y)}} \tag{3.33}$$


↑ 78,4°C
80,9
phase_C_LMG5200
71,5°C
phase_B_LMG5200
77,8°C
phase_A_LMG5200
76,3°C
7,1
↑ 123,7°C
116,9
phase_C_LMG5200
109,8°C
phase_B_LMG5200
123,3°C
phase_A_LMG5200
118,3°C
0,0
↑ 82,3°C
83,8
phase_C_LMG5200
74,9°C
phase_B_LMG5200
81,9°C
phase_A_LMG5200
79,9°C
6,4
↑ 104,7°C
106,3
phase_C_LMG5200
94,7°C
phase_B_LMG5200
104,3°C
phase_A_LMG5200
102,0°C
0,0

(a) (b)

(c) (d)

Figure 3.18: Thermal images at steady state of the GaN E-HEMTs of the servo drive (a) test-#1 (b) test-#2 (c) test-#3 (d) test-#4

$$f_{dm} = \frac{1}{2\pi\sqrt{(2L_{dm} + L_{cm,leakage})(C_x + C_y/2)}} \tag{3.34}$$

The servo drive has a common mode cut-off frequency of about 16.3 kHz and a differential mode cut-off frequency of about 19.1 kHz.

The conducted emission test setup is depicted in Fig. 3.20. The CE102 and CE101 test results for the power lead and returns are shown in Fig. 3.21 and Fig. 3.21, respectively. During the measurements, the servo drive's phase current is around 7 A_{rms}, the switching frequency is 100 kHz, and the PMSM speed is 3600 rpm. Table 2.1 lists the parameters of the PMSMs. As can be seen from the figures, electromagnetic emissions from the servo drive do not exceed the predefined limits.

Table 3.10: Thermal Tests, T_C of GaN E-HEMTs of the Servo Drive

Tests	Parameters (LMG5200)	Phase A	Phase B	Phase C
Test-#1	Drain to source resistance R_{ds}	$18.8\ m\Omega$	$19.3\ m\Omega$	$18.4\ m\Omega$
	Conduction loss, P_{GaN_cond}	$446\ mW$	$458\ mW$	$436\ mW$
	Total loss, P_{GaN_total}	$567\ mW$	$579\ mW$	$557\ mW$
	Estimated case temperature,T_{C_est}	$72.2\ °C$	$74.5\ °C$	$68.3\ °C$
	Measured case temperature,T_{C_meas}	$76.3\ °C$	$77.8\ °C$	$71.5\ °C$
	Estimation error	$-5.7\ \%$	$-4.4\ \%$	$-4.7\ \%$
Test-#2	Drain to source resistance R_{ds}	$23\ m\Omega$	$23.4\ m\Omega$	$22\ m\Omega$
	Conduction loss, P_{GaN_cond}	$1073\ mW$	$1092\ mW$	$1026\ mW$
	Total loss, P_{GaN_total}	$1201\ mW$	$1220\ mW$	$1154\ mW$
	Estimated case temperature,T_{C_est}	$124.5\ °C$	$128.8\ °C$	$114.1\ °C$
	Measured case temperature,T_{C_meas}	$118.3\ °C$	$123.3\ °C$	$109.8\ °C$
	Estimation error	$5\ \%$	$4.3\ \%$	$3.8\ \%$
Test-#3	Drain to source resistance R_{ds}	$19.3\ m\Omega$	$19.3\ m\Omega$	$18.8\ m\Omega$
	Conduction loss, P_{GaN_cond}	$458\ mW$	$458\ mW$	$446\ mW$
	Total loss, P_{GaN_total}	$701\ mW$	$701\ mW$	$689\ mW$
	Estimated case temperature,T_{C_est}	$82.8\ °C$	$84.9\ °C$	$78\ °C$
	Measured case temperature,T_{C_meas}	$79.9\ °C$	$81.9\ °C$	$74.9\ °C$
	Estimation error	$3.5\ \%$	$3.5\ \%$	$3.9\ \%$
Test-#4	Drain to source resistance R_{ds}	$21.6\ m\Omega$	$21.6\ m\Omega$	$20.5\ m\Omega$
	Conduction loss, P_{GaN_cond}	$531\ mW$	$531\ mW$	$504\ mW$
	Total loss, P_{GaN_total}	$1006\ mW$	$1006\ mW$	$979\ mW$
	Estimated case temperature,T_{C_est}	$107.8\ °C$	$110.1\ °C$	$100.1\ °C$
	Measured case temperature,T_{C_meas}	$102\ °C$	$104.3\ °C$	$94.7\ °C$
	Estimation error	$5.4\ \%$	$5.3\ \%$	$5.4\ \%$

3.4 Conclusion

In this chapter, first a basic overview of GaN E-HEMTs is provided, such as the history of GaN transistors, the structures of GaN HEMTs, material properties, 3^{rd} quadrant operations, current collapse effects, short circuit behaviors, etc.

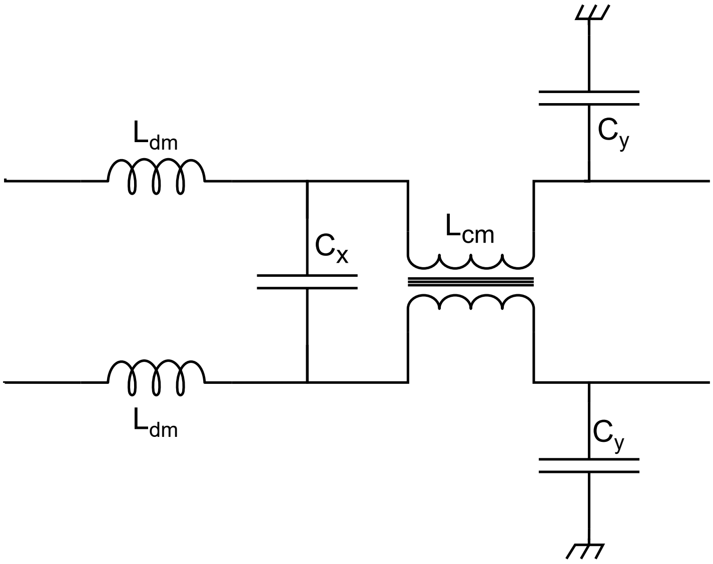

L_{dm}
C_y
C_x
L_{cm}
L_{dm}
C_y

Figure 3.19: The equivalent EMI filter circuit of the power input of the GaN E-HEMT VSI-based servo drive

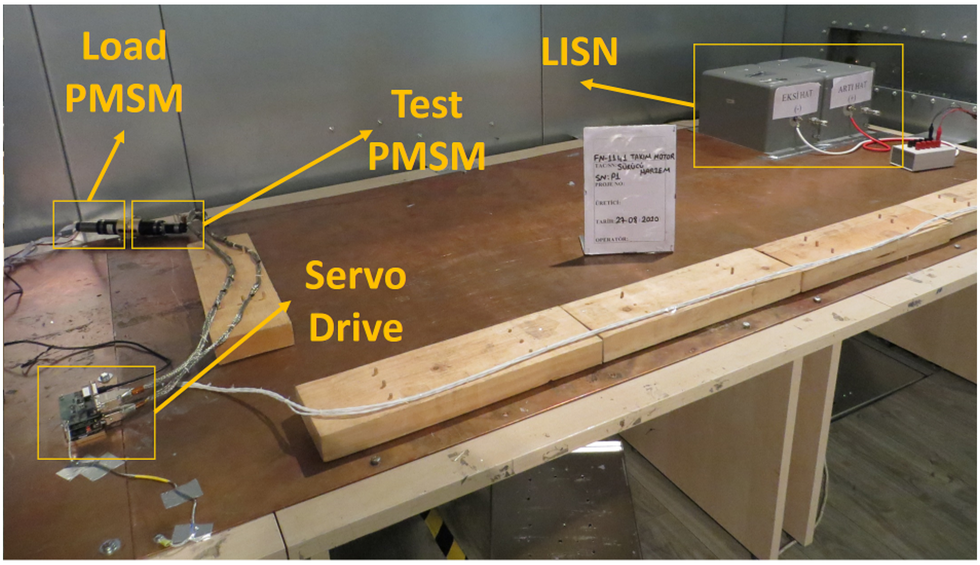
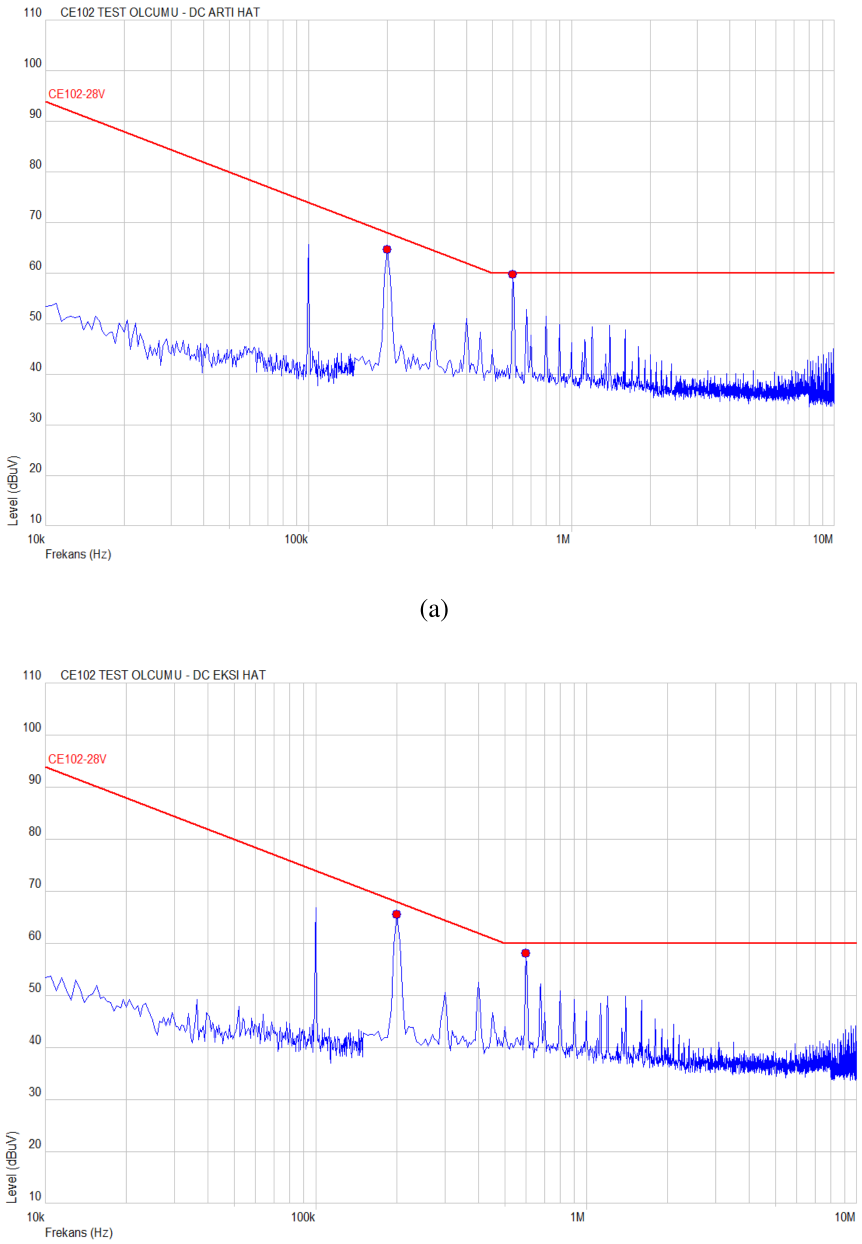

Load
PMSM
LISN
Test
PMSM
Servo
Drive

Figure 3.20: The conducted emission test setup for the GaN E-HEMT VSI-based servo drive

Then, some details on a three-phase, two-level GaN E-HEMT VSI-based servo drive design are given. The servo drive's card compositions and their functionalities are discussed. The benchmarking results of the available GaN E-HEMTs for the servo



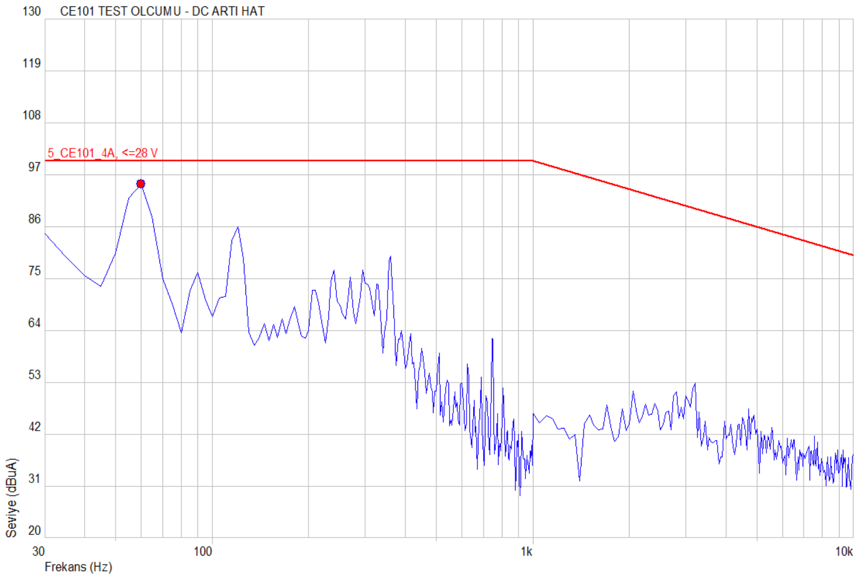
(a)

(b)

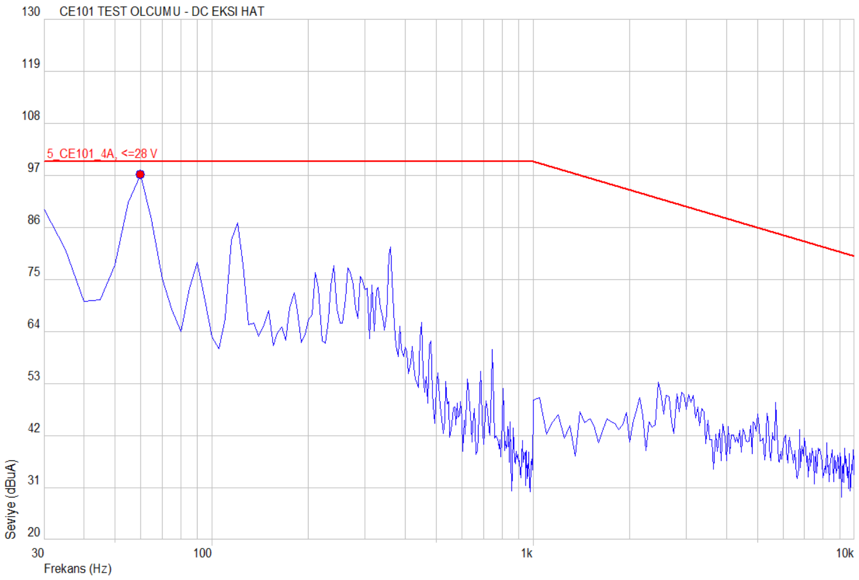
Figure 3.21: CE102 test results of the GaN E-HEMT VSI-based servo drive (a) power lead (b) return

drive and the details of the DC-link capacitor sizing are provided.

Next, the efficiency estimations of the GaN E-HEMT VSI-based servo drive at $24V$ and $48V$ are evaluated both experimentally and analytically. Power loss distributions of the components of the servo drive are also provided. The case temperatures of the



(a)



(b)

Figure 3.22: CE101 test results of the GaN E-HEMT VSI-based servo drive (a) power lead (b) return

GaN E-HEMTs are estimated analytically and validated experimentally.

Finally, the results of the conducted emission tests are shown at the end of the chapter.

CHAPTER 4

PARALLEL CONNECTED GAN E-HEMT VSI-BASED SERVO DRIVES FOR PMSMS

4.1 Introduction

Paralleling inverters increases power output while also allowing for a more flexible, scalable, and reliable system with redundancy [12]. However, the difference in switching time, hardware variations, and dead time differences lead to the circulation current between voltage source inverters, which are wired together both at the DC input and AC output sides [13], [14]. The circulation current between parallel drives causes a distortion of output current, uneven load sharing, lower efficiency, and lower parallel operating power [15–17]. In the literature, the circulating current is suppressed in different ways. Either using a separate DC supply for every inverter input [89] or inserting insulating transformers into every inverter output [90] would eliminate the current path. Adding coupled inductors (CIs) and common-mode inductors (CMIs) to the current path increases its impedance, which helps to minimize circulating current [91–99].

The circulating current includes both low- and high-frequency elements. The low-frequency part occurs near the output fundamental frequency and is caused mainly by the inverters' differing average zero-sequence voltages. On the other hand, asynchronous carrier signals between parallel-connected inverters at switching frequency are primarily responsible for the high frequency circulating current [100–102]. Asynchronous carrier signals may be caused by differences in microcontroller system clocks or deliberately produced by the controller for interleaving operation.

To decrease the low-frequency circulating current, various modulation methods are used in the literature. The selective harmonic elimination PWM approach is used in [103] to eliminate zero-sequence circulating current (ZSCC) by removing zero-sequence harmonics. In [104], the open-loop dual modulator compensation approach is utilized to minimize ZSCC induced by discrepant zero-sequence modulation waveforms of the space vector PWM (SVPWM). The method can independently control the three-phase fundamental voltages and the zero-sequence voltage such that the zero-sequence voltage of the slave inverters are synchronized with the master one. In [105], a zero vector feed-forward control technique with a proportional-integral (PI) controller is used to increase the bandwidth of the zero-axis current loop to minimize ZSCC, which is caused by the phase difference of the zero-sequence voltages. This is extended to more than two inverters in [106]. Deadbeat control is proposed in [107] to eliminate ZSCC by changing the duty ratios of SVPWM zero vectors. In [108], an improved common-mode injection PWM method is utilized to minimize ZSCC. Instead of adding common mode injection signals to the modulating signals individually as in the SVPWM method, the average of the common-mode injection signals of the inverters is added to both of the inverters. In the multicarrier PWM procedure, instead of using the SVPWM's zero vectors, opposite active vectors are used to synthesize the required output voltage, resulting in a lower ZSCC [109]. ZSCC is reduced in [110] by minimizing the difference in zero-sequence voltages (ZSV) between inverters by modifying the ZSV vectors of SVPWM.

In order to reduce the high-frequency circulating current (HFCC), the period of the carrier signal is modified to synchronize it with the master module in [111]. In [112], each inverter produces a square wave containing the frequency and phase information of its carrier signal, which is then compared to the synchronization signal to match carrier signals and suppress HFCC. The virtual oscillator control-based synchronization method is used in [113] to minimize HFCC without communicating signals. This approach generates the carrier wave with a virtual oscillator and synchronizes it with the electrical connection between paralleled inverters. To suppress HFCC, a closed-loop carrier phase adjustment control is utilized in [100] to align the carrier phase difference between the two inverters. In [18], a high-frequency voltage correction is performed on the slave module using the zero-sequence current to decrease HFCC caused by asynchronous carrier signals. In [114], the variable switching frequency

PWM approach is used to suppress HFCC by preventing carrier misalignment. The carrier of each slave inverter is synchronized by the master module via a synchronization signal.

In this chapter, a fault-tolerant parallel-connected GaN E-HEMT VSI-based servo drive system is presented, which removes the requirement for extra inductors at the output and separate DC supplies at the input of inverters while simultaneously allowing the use of a conventional PI current control and a standard SVPWM method. By synchronizing the carrier signals, the circulating current generated by the phase mismatch between the carrier signals of the parallel-connected inverters is removed. By increasing the switching frequency without installing extra inductors at the inverters' output, the circulating current produced by inherent hardware variations is minimized. The GaN E-HEMT wide-bandgap device is utilized for this purpose. The GaN E-HEMT device's properties, such as its short turn on/off time, zero reverse recovery loss, good thermal capability, low conduction, and switching losses, allow for higher switching frequencies. Up to six parallel-connected GaN E-HEMT VSI-based servo drives are used to demonstrate the benefits of parallel operation for the PMSM, and various dynamic tests (startup, step torque disturbance, chirp torque disturbance, step speed reference, and servo drive faulty conditions) are used to demonstrate system performance [115].

4.2 Circulation Current Due to Asynchronous Carrier Signals

In this section, the circulating current caused by the phase difference of the PWM carrier signals of the parallel-connected inverters is analyzed case by case.

Fig. 4.1 depicts a simplified schematic diagram of parallel-connected inverters. The principle of circulating current induced by phase-shifted carrier signals is shown using two modules. Both inverters are powered by the same DC source, and their outputs are connected directly without the use of additional inductors.

Where x stands for the number of the inverter;
$\mathrm{L}_{\mathrm{xa,xb,xc}}$: cable inductances of the output of the inverters
$\mathrm{R}_{\mathrm{xa,xb,xc}}$: cable resistances of the output of the inverters

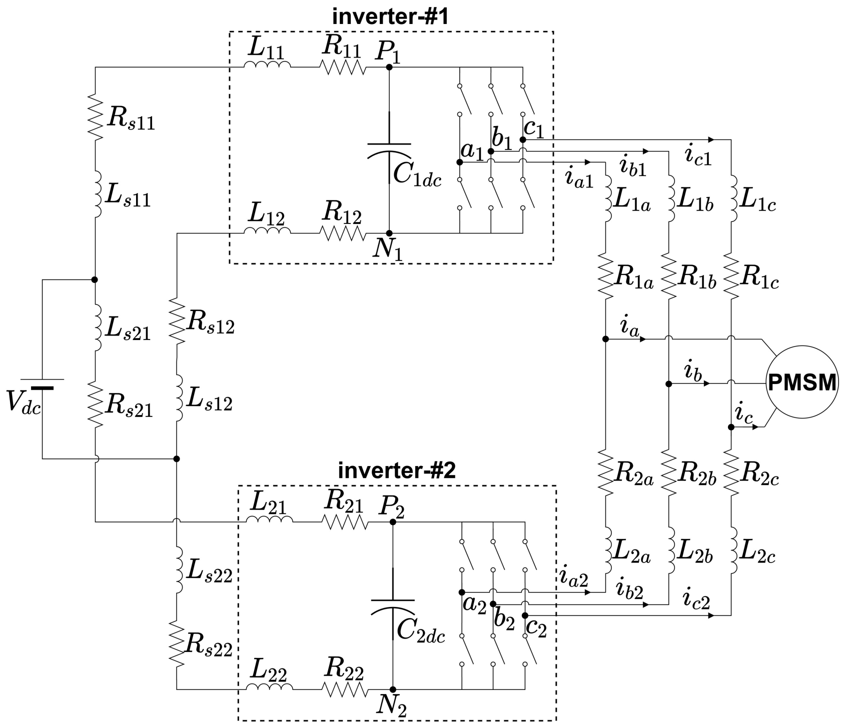

inverter-#1
L_{11}
R_{11}
P_1
R_{s11}
L_{s11}
C_{1dc}
a_1
b_1
c_1
i_{a1}
i_{b1}
i_{c1}
L_{1a}
L_{1b}
L_{1c}
L_{12}
R_{12}
N_1
R_{1a}
R_{1b}
R_{1c}
L_{s21}
R_{s12}
i_a
i_b
PMSM
V_{dc}
R_{s21}
L_{s12}
i_c
inverter-#2
R_{2a}
R_{2b}
R_{2c}
L_{21}
R_{21}
P_2
L_{s22}
L_{2a}
L_{2b}
L_{2c}
i_{a2}
i_{b2}
i_{c2}
a_2
b_2
c_2
C_{2dc}
R_{s22}
L_{22}
R_{22}
N_2

Figure 4.1: Circuit diagram of the parallel-connected inverters and PMSM.

$\mathrm{L_{sx1}}$: cable inductances of the positive distributed point of the DC power supply to the inverters

$\mathrm{R_{sx1}}$: cable resistances of the positive distributed point of the DC power supply to the inverters

$\mathrm{L_{sx2}}$: cable inductances of the negative distributed point of the DC power supply to the inverters

$\mathrm{R_{sx2}}$: cable resistances of the negative distributed point of the DC power supply to the inverters

$\mathrm{L_{x1}}$: inductances of the positive side of the inverters

$\mathrm{R_{x1}}$: resistances of the positive side of the inverters

$\mathrm{L_{x2}}$: inductances of the negative side of the inverters

$\mathrm{R_{x2}}$: resistances of the negative side of the inverters

Assume that the phase difference angle between the carrier signals is set to 90°. It can be concluded that no torque will be transferred to the motor when the speed reference is set to zero and there exists no disturbance. This leads to $i_a = i_b = i_c = 0$. In

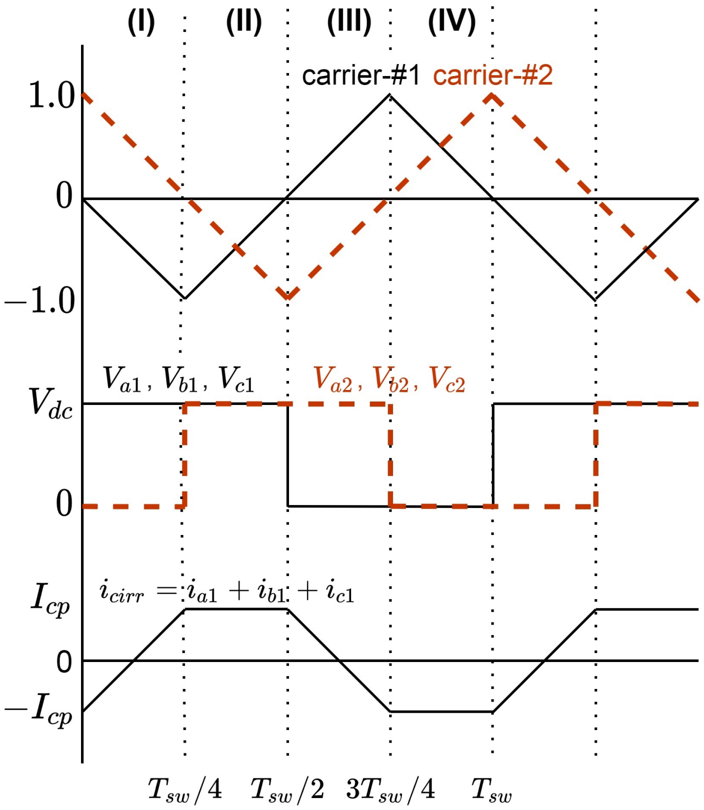


Figure 4.2: The phase angle difference between carrier signals of the parallel-connected inverters is $90°$.

this case, the duty cycle of each inverter output is 50%. Fig. 4.2 depicts the carrier signals, inverter output voltages, and circulating current waveforms in this situation.

Where;

V_{a1} : the midpoint of the leg A of the inverter-#1

V_{b1} : the midpoint of the leg B of the inverter-#1

V_{c1} : the midpoint of the leg C of the inverter-#1

V_{a2} : the midpoint of the leg A of the inverter-#2

V_{b2} : the midpoint of the leg B of the inverter-#2

V_{c2} : the midpoint of the leg C of the inverter-#2

I_{cp} : the peak value of the circulating current (i_{cirr})

4.2.1 Region (I)

The switches on the top side of inverter-#1 and the switches on the bottom side of inverter-#2 are all turned on during region (I) of Fig. 4.2. The circulation current direction for this case is shown in Fig. 4.3a.

It is worth noting that the circulating current branches in two directions from node N_2 as positive and negative lines. Then, at node P_1, they merge once again.
Let's define:
$\mathrm{R_p}$: the equivalent resistance of the positive line
$\mathrm{L_p}$: the equivalent inductance of the positive line
$\mathrm{R_n}$: the equivalent resistance of the negative line
$\mathrm{L_n}$: the equivalent inductance of the negative line

$$\begin{aligned} R_p &= R_{21} + R_{s21} + R_{s11} + R_{11} \\ L_p &= L_{21} + L_{s21} + L_{s11} + L_{11} \end{aligned} \tag{4.1}$$

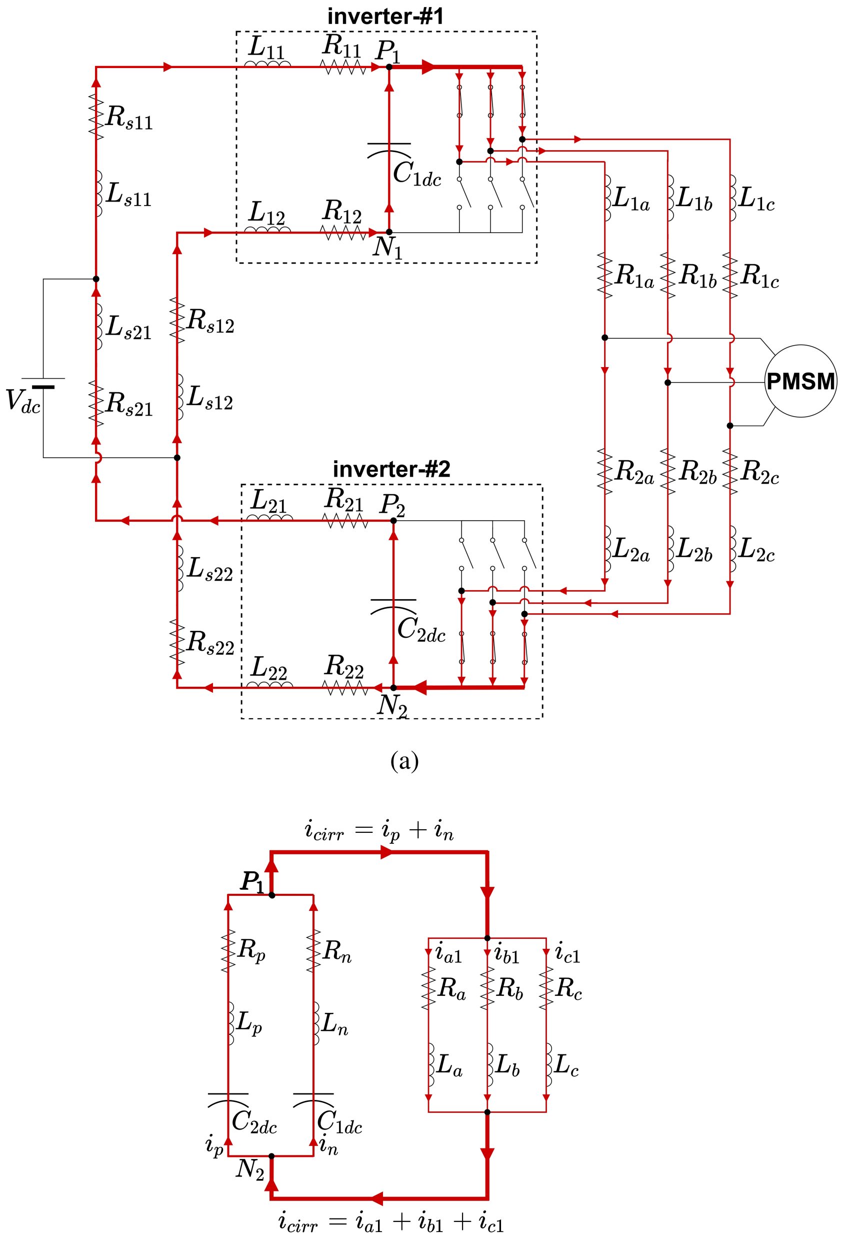
$$\begin{aligned} R_n &= R_{22} + R_{s22} + R_{s12} + R_{12} \\ L_n &= L_{22} + L_{s22} + L_{s12} + L_{12} \end{aligned} \tag{4.2}$$

Let R_a and L_a be defined as the equivalent resistance and inductance of the nodes between a_1 and a_2 respectively. These nodes are the phase A outputs of the inverters. The same descriptions are also made for the B and C phases.

$$\begin{aligned} R_a &= R_{1a} + R_{2a} \\ L_a &= L_{1a} + L_{2a} \end{aligned} \tag{4.3}$$

$$\begin{aligned} R_b &= R_{1b} + R_{2b} \\ L_b &= L_{1b} + L_{2b} \end{aligned} \tag{4.4}$$

$$\begin{aligned} R_c &= R_{1c} + R_{2c} \\ L_c &= L_{1c} + L_{2c} \end{aligned} \tag{4.5}$$


inverter-#1
L_{11}
R_{11}
P_1
R_{s11}
L_{s11}
C_{1dc}
L_{12}
R_{12}
N_1
L_{1a}
L_{1b}
L_{1c}
R_{1a}
R_{1b}
R_{1c}
L_{s21}
R_{s12}
V_{dc}
R_{s21}
L_{s12}
PMSM
inverter-#2
R_{2a}
R_{2b}
R_{2c}
L_{21}
R_{21}
P_2
L_{s22}
L_{2a}
L_{2b}
L_{2c}
C_{2dc}
R_{s22}
L_{22}
R_{22}
N_2
$i_{cirr} = i_p + i_n$
P_1
R_p
R_n
L_p
L_n
i_{a1}
i_{b1}
i_{c1}
R_a
R_b
R_c
L_a
L_b
L_c
C_{2dc}
C_{1dc}
i_p
i_n
N_2
$i_{cirr} = i_{a1} + i_{b1} + i_{c1}$

(a)

(b)

Figure 4.3: (a) The circulation current path when the phase angle difference between carrier signals is $90°$, region (I) (b) Equivalent circuit of the circulation current path.

Fig. 4.3b depicts the simpler equivalent circuit of Fig. 4.3a. Assume that the voltage on the DC-link capacitors C_{2dc} and C_{1dc} is equal to the supply voltage, V_{dc}. Let's simplify the equation by stating,

$$\begin{aligned} R_p = R_n &= R_{in} \\ L_p = L_n &= L_{in} \\ R_a = R_b = R_c &= R_{out} \\ L_a = L_b = L_c &= L_{out} \end{aligned} \tag{4.6}$$

The differential equation for the circulating current path is as follows:

$$V_{dc} = \frac{R_{in}}{2} i_{cirr} + \frac{L_{in}}{2} \frac{di_{cirr}}{dt} + \frac{R_{out}}{3} i_{cirr} + \frac{L_{out}}{3} \frac{di_{cirr}}{dt} \tag{4.7}$$

To further simplify the equation, the voltage drops on the resistors are ignored, and the circulating current can be written as follows:

$$\Delta i_{cirr} = \frac{V_{dc} \Delta T}{L_{eq}} \tag{4.8}$$

where:

ΔT : the phase difference of the carrier signals, $\Delta T = T_{sw}/4$ for 90°

T_{sw} : the switching period

The path's equivalent inductance, L_{eq}, can be determined as:

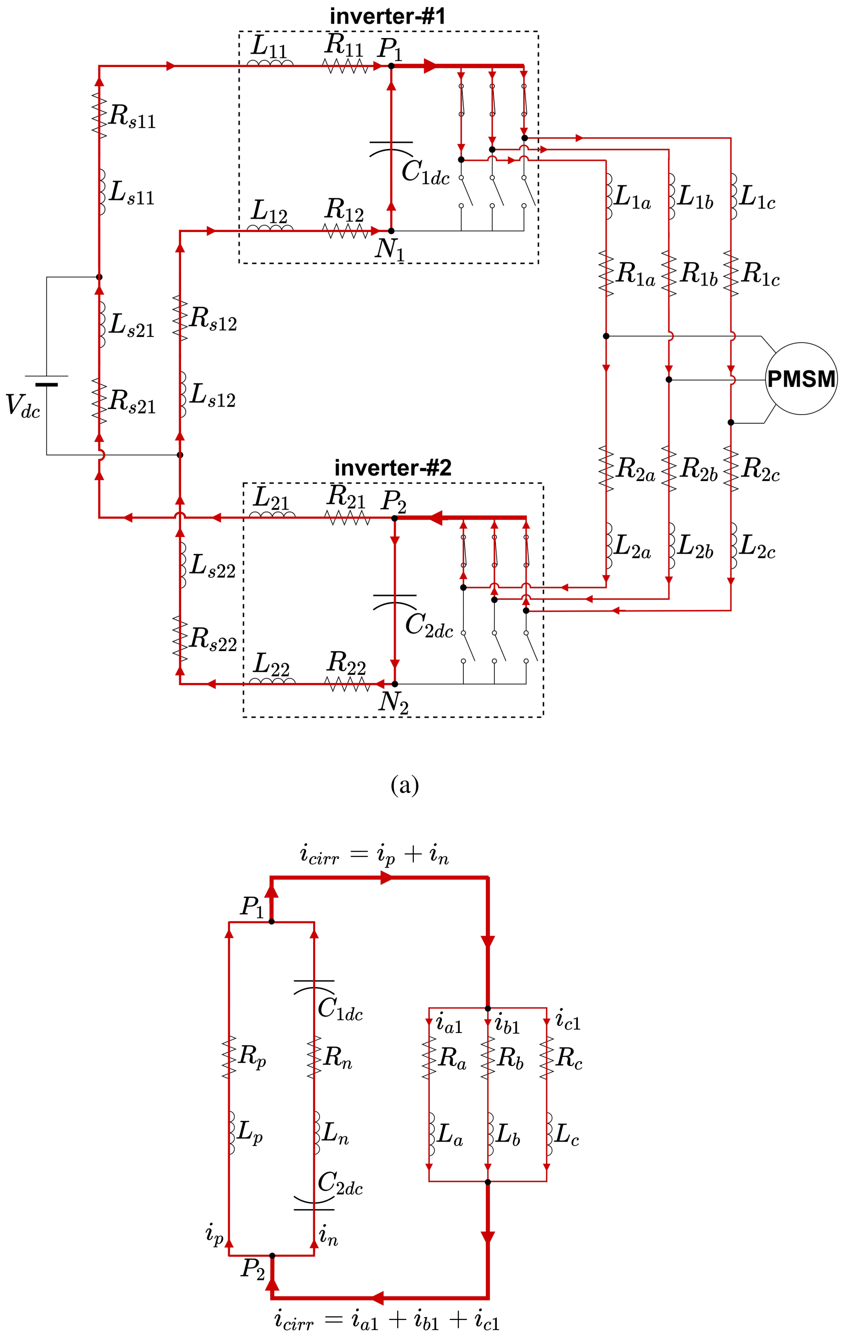
$$L_{eq} = \frac{L_{in}}{2} + \frac{L_{out}}{3} \tag{4.9}$$

4.2.2 Region (II)

The top-side switches of both inverters are turned on during region (II) of Fig. 4.2. Fig. 4.4a and Fig. 4.4b indicate the circulation current paths and equivalent circuits, respectively. Notice that because capacitor voltages cancel each other in this region (II), it can also be concluded that the circulating current remains constant.

4.2.3 Region (III)

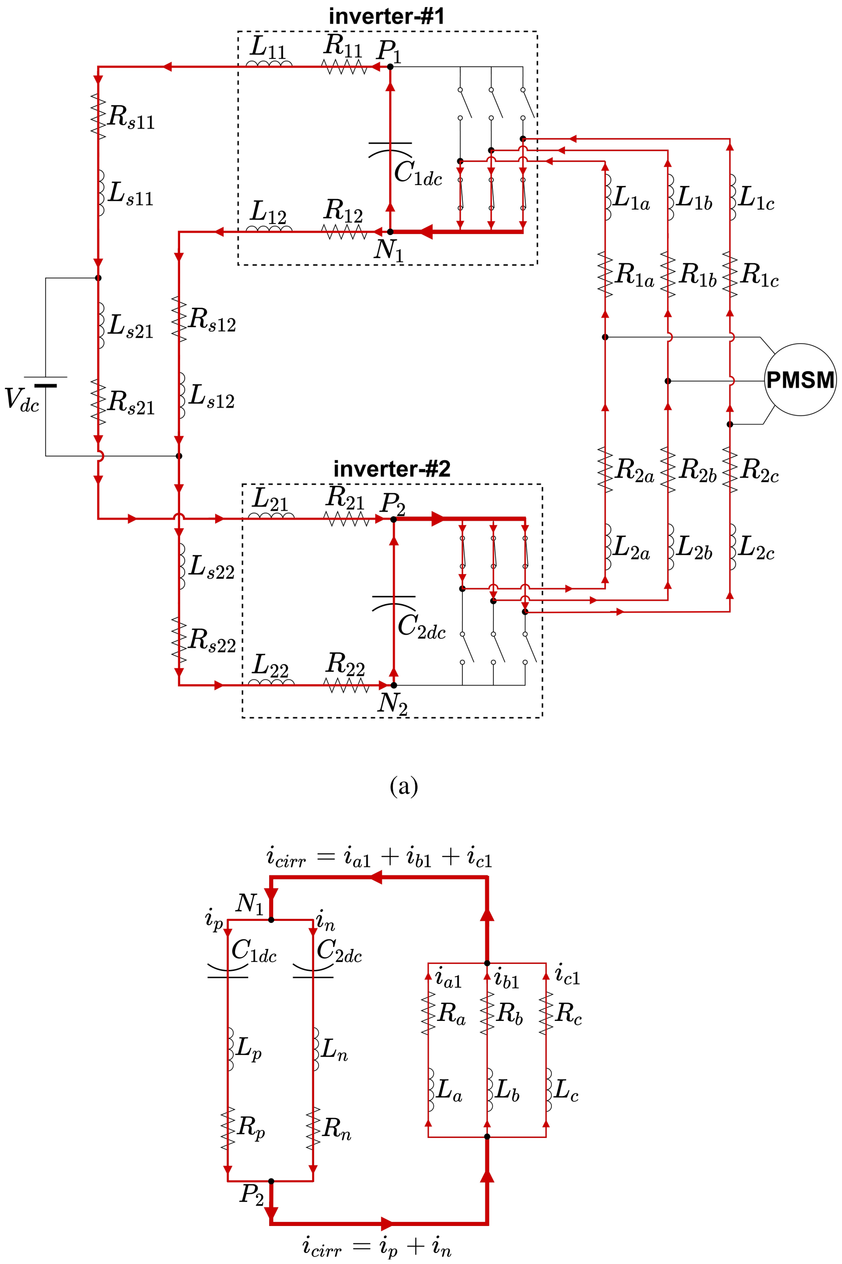
The switching states of the inverters are exchanged during region (III) of Fig. 4.2, and the top side switches inverter-#2 are now turned on. Fig. 4.5a and Fig. 4.5b depict the circulation current path and equivalent circuit, respectively. The same (4.8) equation applies to this region as well.


inverter-#1
L_{11}
R_{11}
P_1
R_{s11}
L_{s11}
C_{1dc}
L_{12}
R_{12}
N_1
L_{1a}
L_{1b}
L_{1c}
R_{1a}
R_{1b}
R_{1c}
L_{s21}
R_{s12}
V_{dc}
R_{s21}
L_{s12}
PMSM
inverter-#2
L_{21}
R_{21}
P_2
R_{2a}
R_{2b}
R_{2c}
L_{s22}
L_{2a}
L_{2b}
L_{2c}
C_{2dc}
R_{s22}
L_{22}
R_{22}
N_2
$i_{cirr} = i_p + i_n$
P_1
C_{1dc}
i_{a1}
i_{b1}
i_{c1}
R_p
R_n
R_a
R_b
R_c
L_p
L_n
L_a
L_b
L_c
C_{2dc}
i_p
i_n
P_2
$i_{cirr} = i_{a1} + i_{b1} + i_{c1}$

(a)

(b)

Figure 4.4: (a) The circulation current path when the phase angle difference between carrier signals is 90°, region (II) (b) Equivalent circuit of the circulation current path.


inverter-#1
L_{11}
R_{11}
P_1
C_{1dc}
L_{12}
R_{12}
N_1
R_{s11}
L_{s11}
L_{s21}
R_{s21}
R_{s12}
L_{s12}
V_{dc}
L_{1a}
L_{1b}
L_{1c}
R_{1a}
R_{1b}
R_{1c}
PMSM
R_{2a}
R_{2b}
R_{2c}
L_{2a}
L_{2b}
L_{2c}
inverter-#2
L_{21}
R_{21}
P_2
L_{s22}
R_{s22}
C_{2dc}
L_{22}
R_{22}
N_2
$i_{cirr} = i_{a1} + i_{b1} + i_{c1}$
N_1
i_p
i_n
C_{1dc}
C_{2dc}
L_p
L_n
R_p
R_n
P_2
i_{a1}
i_{b1}
i_{c1}
R_a
R_b
R_c
L_a
L_b
L_c
$i_{cirr} = i_p + i_n$

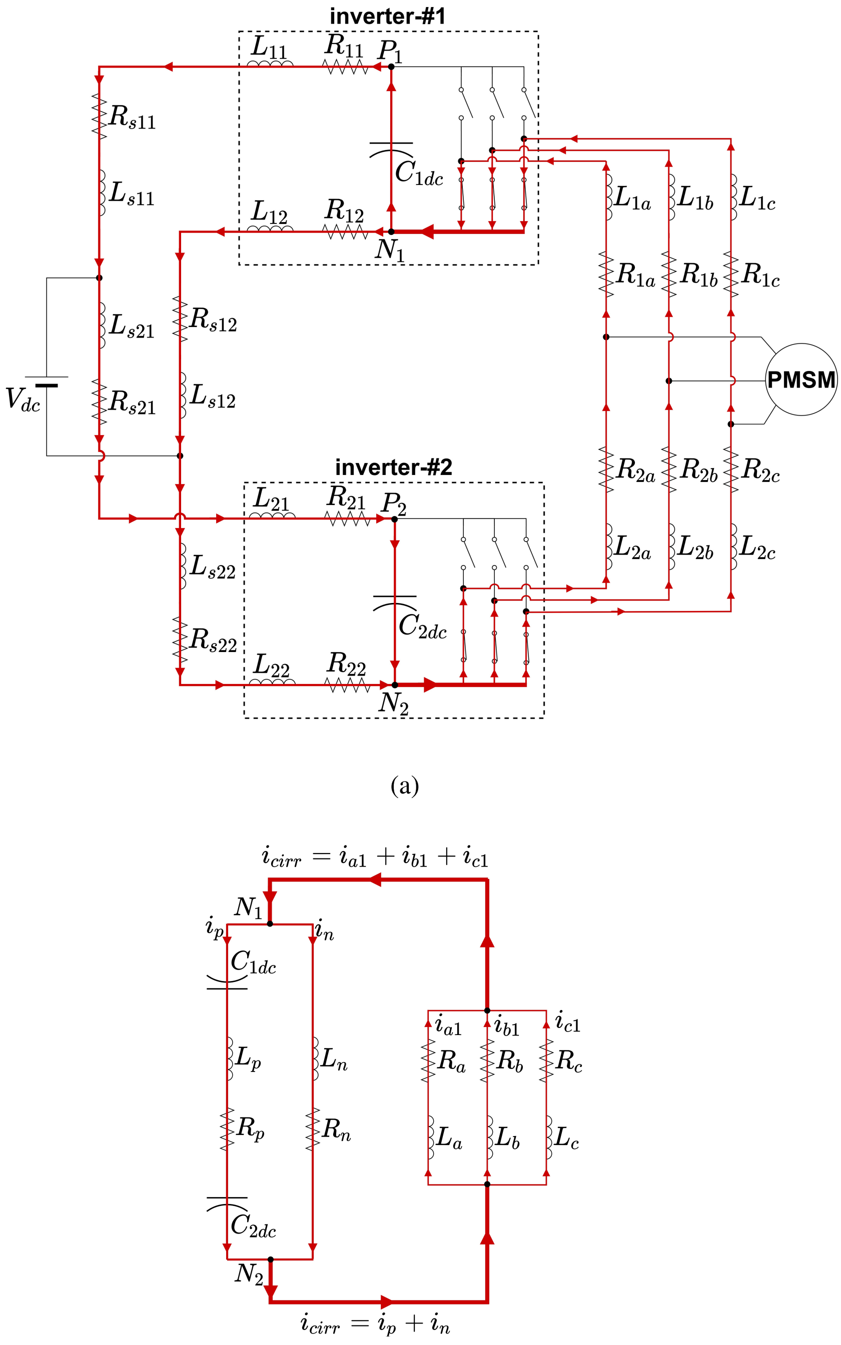
(a)

(b)

Figure 4.5: (a) The circulation current path when the phase angle difference between carrier signals is $90°$, region (III) (b) Equivalent circuit of the circulation current path.

4.2.4 Region (IV)

Finally, in Fig. 4.6a and Fig. 4.6b, during region (IV) of Fig. 4.2, the circulation current path and equivalent circuit can be seen. In both inverters, the bottom switches


inverter-#1
L_{11}
R_{11}
P_1
R_{s11}
L_{s11}
C_{1dc}
L_{12}
R_{12}
N_1
L_{1a}
L_{1b}
L_{1c}
R_{1a}
R_{1b}
R_{1c}
L_{s21}
R_{s12}
V_{dc}
R_{s21}
L_{s12}
PMSM
inverter-#2
L_{21}
R_{21}
P_2
R_{2a}
R_{2b}
R_{2c}
L_{s22}
L_{2a}
L_{2b}
L_{2c}
C_{2dc}
R_{s22}
L_{22}
R_{22}
N_2
$i_{cirr} = i_{a1} + i_{b1} + i_{c1}$
N_1
i_p
i_n
C_{1dc}
i_{a1}
i_{b1}
i_{c1}
R_a
R_b
R_c
L_p
L_n
R_p
R_n
L_a
L_b
L_c
C_{2dc}
N_2
$i_{cirr} = i_p + i_n$

(a)

(b)

Figure 4.6: (a) The circulation current path when the phase angle difference between carrier signals is 90°, region (IV) (b) Equivalent circuit of the circulation current path.

are ON. As in region (II), the capacitor voltages cancel each other and the circulating current is expected to be kept constant.

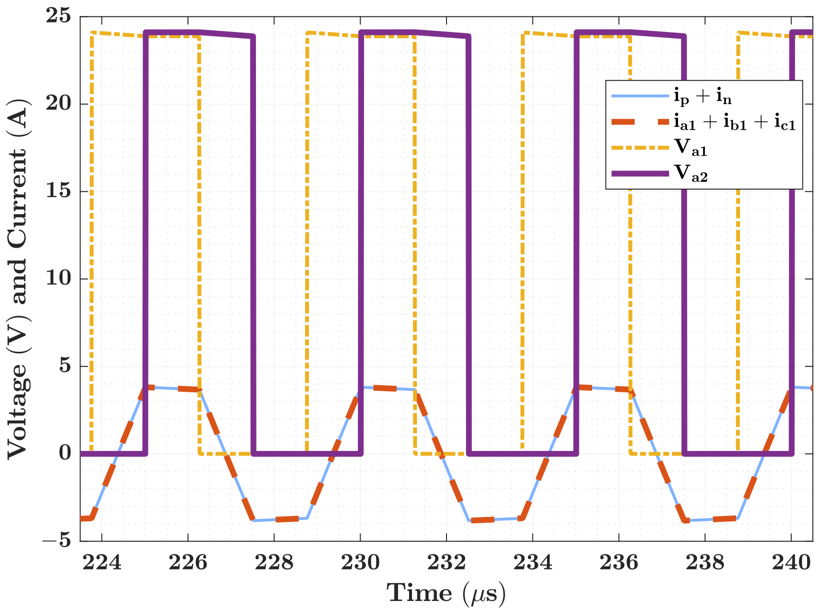


Figure 4.7: Simulation results when the phase angle difference between carrier signals is $90°$ and the switching frequency is $200\ kHz$ at steady-state.

When the phase angle of the carrier signal is increased to the highest value of $180°$, only two regions will be available: (I) and (III). The equation (4.8) holds for both parts, and since $\Delta T = T_{sw}/2$, the peak to peak value of the circulating current would be twice that of the $90°$ case.

4.2.5 Simulation Results

The simulation waveforms that are produced by using Ansoft Simplorer can be seen in Fig. 4.7 when the phase angle difference between carrier signals is $90°$ ($\Delta T = T_{sw}/4$) at steady state.

The circulating current along positive and negative lines are defined by the symbols i_p and i_n, respectively. Simulation and the circuit parameters that are taken from the experimental setup are given in Table 4.1.

By using (4.9) and (4.8), the equivalent inductance (L_{eq}) is calculated as $4\ \mu H$, and the peak to peak circulation current (i_{cirr}) is $7.5A$. The peak to peak circulating current would be $15A$ if the phase angle difference between the carrier signals of the parallel-connected inverters in Fig. 4.1 was increased to $180°$ ($\Delta T = T_{sw}/2$), which

Table 4.1: Simulation Circuit Parameters

Parameters	**Value**
f_{sw}	$200\ kHz$
T_{sw}	$5\ \mu s$
V_{dc}	$24\ V$
R_{in}	$94\ m\Omega$
L_{in}	$6.4\ \mu H$
R_{out}	$159\ m\Omega$
L_{out}	$2.4\ \mu H$

is the worst case. The circulating current can be re-written for this condition as the following equation where f_{sw} is the switching frequency and $f_{sw} = 1/T_{sw}$.

$$\Delta i_{cirr} = \frac{V_{dc}}{2 f_{sw} L_{eq}} \tag{4.10}$$

It is worth noting that if the switching frequency were reduced to $20\ kHz$ while maintaining the same L_{eq}, (4.10), the circulating current would be $150A$. The equivalent inductance should be increased by ten times in order to obtain the same circulating current value. The findings demonstrate that even though the phase difference is the worst case, increasing the switching frequency without inserting additional inductors limits the circulating currents.

The simulation waveforms at startup are shown in Fig. 4.8. The elapsed time to reach the steady state depends on the time constant of the equivalent circuit of the circulating current path. The equivalent resistance (R_{eq}) of the circulating path can be determined by the following equation:

$$R_{eq} = \frac{R_{in}}{2} + \frac{R_{out}}{3} \tag{4.11}$$

By using the values given in Table 4.1, R_{eq} is equal to $100\ m\Omega$. The time constant

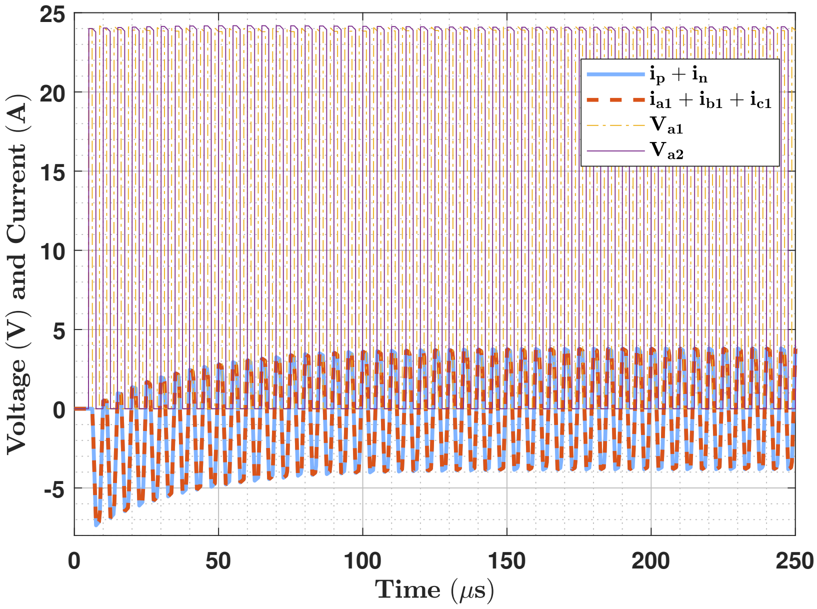


Figure 4.8: Simulation results during startup with $90°$ phase angle difference between carrier signals and the switching frequency is $200\ kHz$.

can be calculated as:

$$\tau_{eq} = \frac{L_{eq}}{R_{eq}} \tag{4.12}$$

and it is equal to $40\ \mu s$. At startup, the circulating peak current value can be Δi_{cirr}, before the steady-state condition is reached. This peak current value should be allowed by the inverter without entering the overcurrent protection. Note that at steady state this value drops to $\Delta i_{cirr}/2$.

4.3 Experimental Work

An experimental setup, shown in Fig. 4.9, is being prepared to verify the previous section's analyses and simulation results, as well as to demonstrate the performance of the PMSM's parallel operation.

A three-phase, two-level GaN E-HEMT VSI-bases servo drive is designed for this purpose; details are given in Chapter Chapter 3.3. Up to six parallel-connected servo drives are being used. All servo modules are powered by the same DC supply, and the servo drive outputs are tied directly to each other. Table 4.2 contains the servo drive and PMSM parameters.

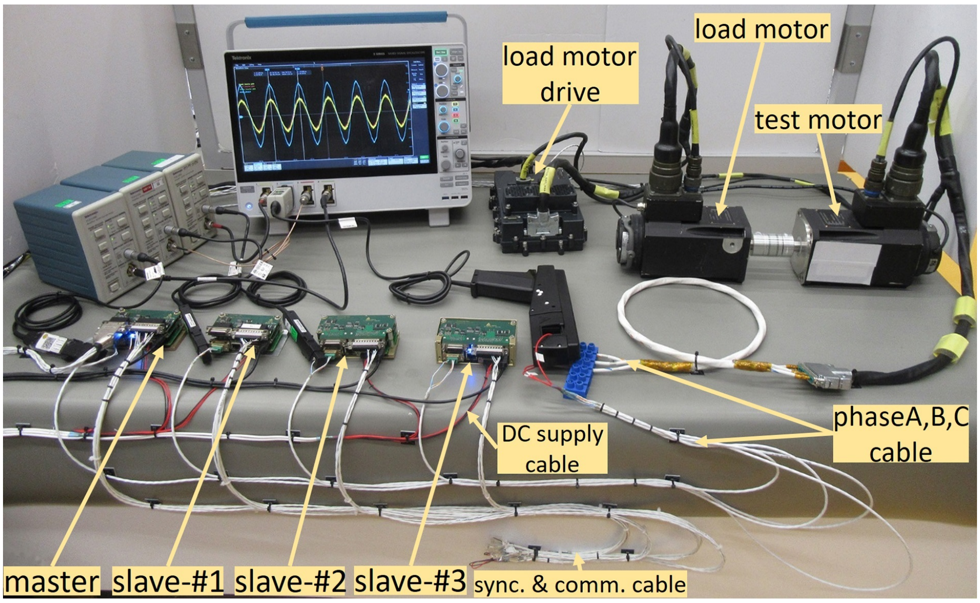
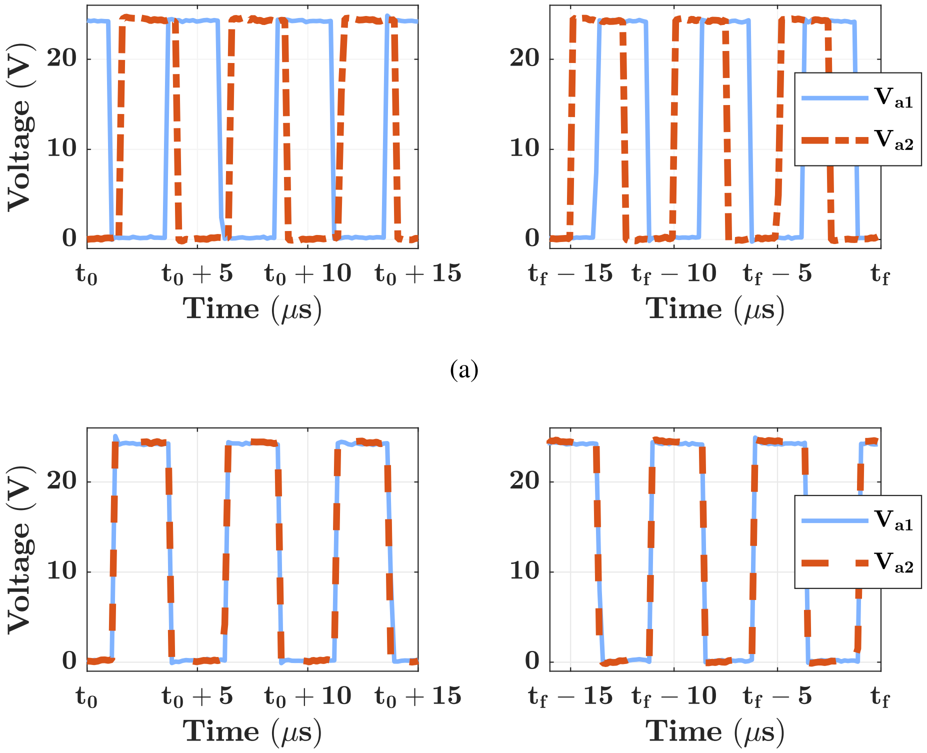

load motor
load motor drive
test motor
DC supply cable
phaseA,B,C cable
master
slave-#1
slave-#2
slave-#3
sync. & comm. cable

Figure 4.9: Experimental setup with four parallel-connected GaN E-HEMT VSI-based servo drives.

Table 4.2: Motor Drive and PMSM Parameters

Parameters	**Value**
DC link voltage	24 V
Switching frequency	200 kHz
Dead time	10 ns
Output phase current limit	7.07 $Arms$
PMSM nominal voltage	24 V
PMSM nominal torque	3.9 Nm
PMSM nominal current	61.9 $Arms$
PMSM phase inductance	12 μH
PMSM phase resistance	4.13 $m\Omega$
PMSM number of pole pairs	6
PMSM rated power	1430W



(a)

(b)

Figure 4.10: V_{a1} and V_{a2} waveforms (a) without synchronization (b) with synchronization where $t_0 = 0$ and $t_f = 200000\ \mu s$.

4.3.1 Effect of Clock Inconsistencies Between Individual Microcontrollers

In this part, two parallel servo drives with master and slave arrangements are used to illustrate the issue of clock inconsistencies of the individual microcontrollers. For both inverters, the duty cycle is adjusted to 50%. The output voltages for Phase A are obtained without any connection with the inverters, and the measurements are presented in Fig. 4.10a.

The measurement lasts $200\ ms$, and it can be observed that even if the switching frequencies are set to the identical value, the difference in the phase angles of the carrier signals drifts over time. The parallel operation would not perform as expected due to variations in the phase angle of the carrier signals unless the carrier signals are aligned. When only one microcontroller is used, the number of parallel-connected inverters is constrained by the microcontroller's peripheral capability. A microcontroller for each servo drive is an alternative approach that increases the system's modularity and flexibility. Without using any additional circuitry, the carrier signals are synchronized using the microcontroller's time-base synchronization (EPWMxSYNCI) input. The same measurement was done with this synchronization signal, and the results can be seen in Fig. 4.10b. It is worth noting that when using the synchronization signal, not only the time dependency of the carrier phase angle is overcome, but also the phase angle of the carrier signals is removed.

Although the carrier phase discrepancy between inverters can ideally be removed, high frequency circulating currents can still occur due to instantaneous variations in output voltages induced by unavoidable hardware differences in gate driver turn on and off delays, PWM buffer delays, phase current measuring errors, and so on. The amplitude of the high-frequency circulating current can be reduced by increasing the switching frequency [110] without the need of any additional inductors at the inverters' outputs. The GaN E-HEMT VSI-based servo drive is chosen for this reason due to its numerous advantages, which are primarily discussed in the previous work [116].

4.3.2 Comparison with Simulation Results

In this part, the simulation results in Section 4.2.5 are compared with the experimental results.

The master and slave-#1 servo drives are used, and a $90°$ phase angle difference between PWM carriers is introduced manually to verify theoretical analysis and simulation performance. The inverter's DC supply input is used to determine the sum of positive and negative line currents that is $i_p + i_n$. As shown in Fig. 4.11 and Fig. 4.12, comparable waveforms and values are achieved to the findings seen in Fig. 4.7 and Fig. 4.8 without exceeding the servo drives' current limit which is about $10A$ phase output current.

In a further experiment, the validity of (4.8) was demonstrated by increasing the switching frequency to $400\ kHz$ and comparing it to $200\ kHz$ (Fig. 4.11). As shown in Fig. 4.13, the amplitude of the circulation current is decreased by half as the

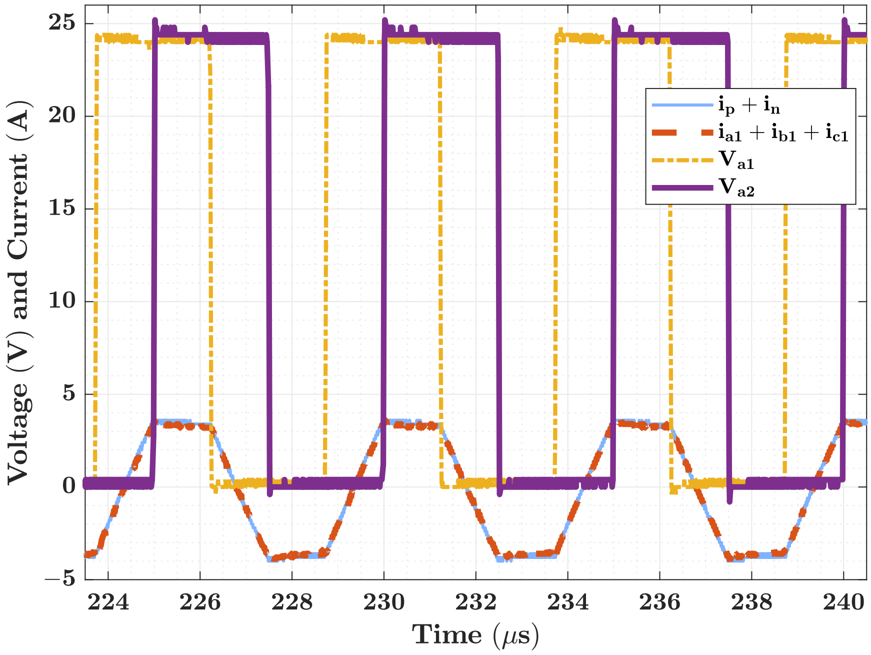


Figure 4.11: Experimental results when the phase angle difference between carrier signals is 90° and the switching frequency is 200 kHz at steady-state.

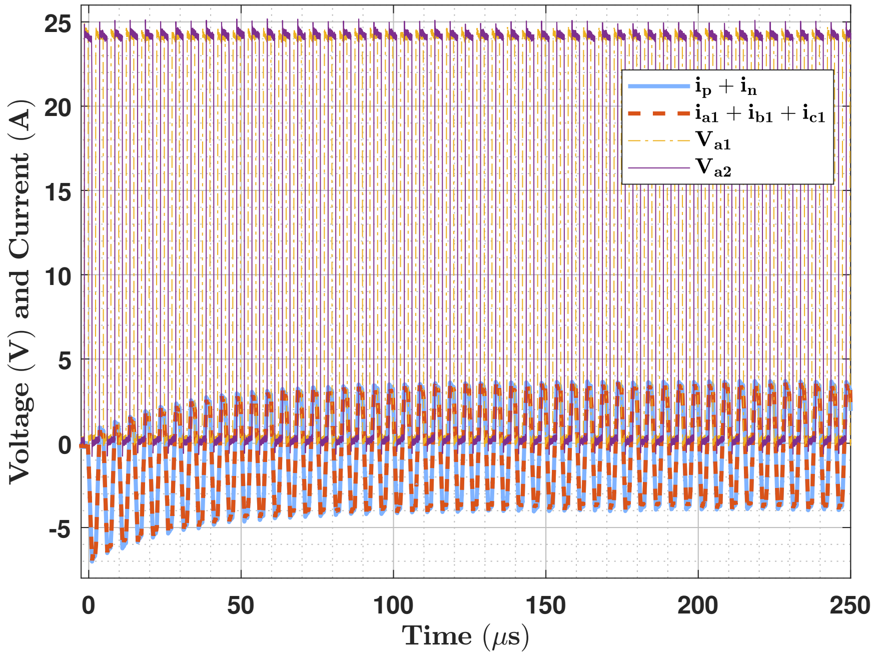


Figure 4.12: Experimental results during startup with 90° phase angle difference between carrier signals and the switching frequency is 200 kHz.

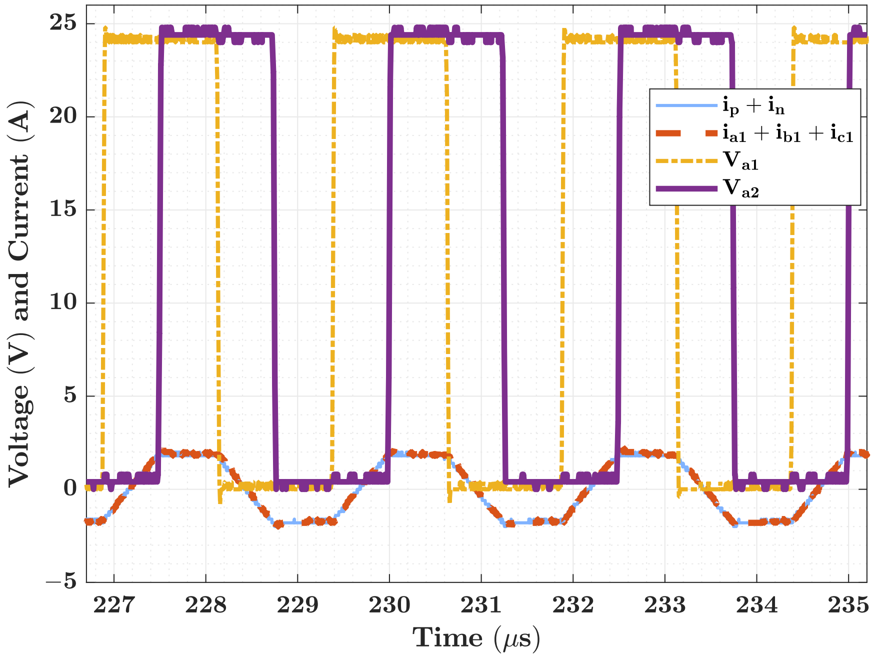


Figure 4.13: Experimental results when the phase angle difference between carrier signals is $90°$ and the switching frequency is $400\ kHz$ at steady-state.

switching frequency is doubled.

4.3.3 Block Schema of the Parallel Operation

Fig. 4.14 shows the overall block schema of the parallel operation. To control the PMSM, the field-oriented control approach with SVPWM is used. The master module reads the rotor angle through the resolver interface and transfers it to the slave modules. The speed loop is also closed by the master module. The PI speed controller output, which is quadrature axis reference (i_q^*) is divided by the overall number of servo drives in the process, which is $n+1$, where n is the number of slave modules. The master module sends this i_q^* value along with the rotor angle (θ_e) to the slaves via the same message structure. The number of inverters is limited by the bus capability of the synchronization and communication (i_q^* and θ_e) lines. The servo drives all measure their output currents and use the same PI current controller parameters. The master module produces a synchronization signal at the switching frequency and sends this signal to the slaves.

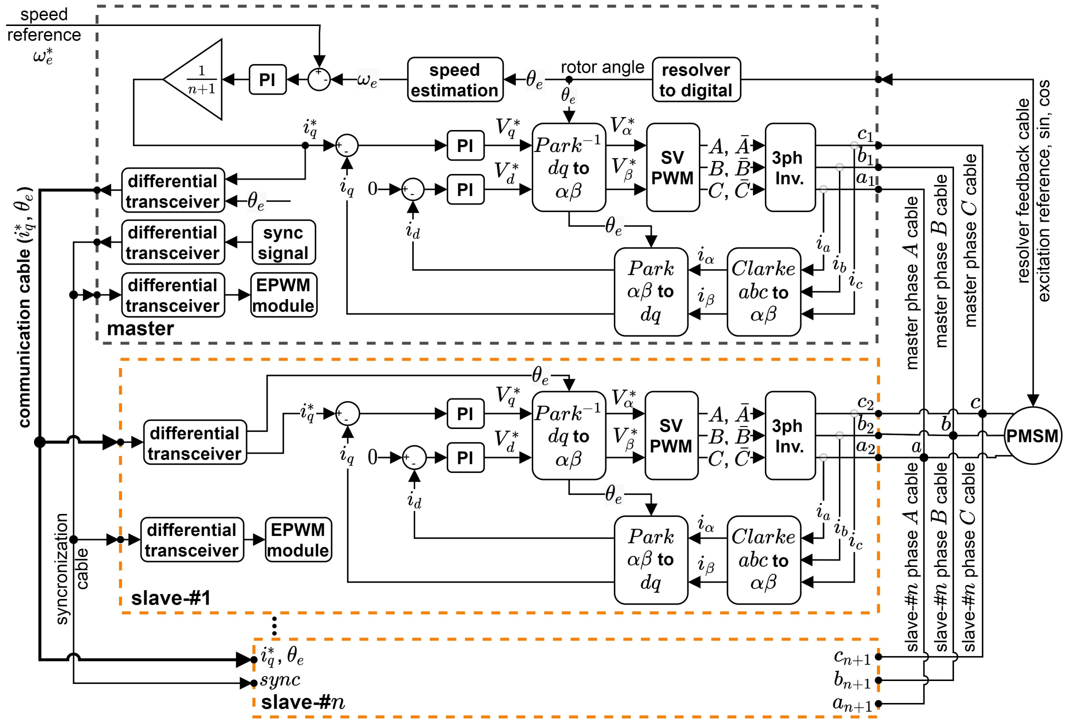

speed reference ω_e^*
$\frac{1}{n+1}$
PI
ω_e
speed estimation
θ_e
rotor angle
resolver to digital
i_q^*
V_q^*
V_α^*
$Park^{-1}$ dq to $\alpha\beta$
SV PWM
A, $\bar{A}$
B, $\bar{B}$
C, $\bar{C}$
3ph Inv.
c_1
b_1
a_1
i_q
0
V_d^*
V_β^*
i_d
$Park$ $\alpha\beta$ to dq
$Clarke$ abc to $\alpha\beta$
i_α
i_β
i_a
i_b
i_c
differential transceiver
sync signal
EPWM module
master
communication cable (i_q^*, θ_e)
master phase A cable
master phase B cable
master phase C cable
resolver feedback cable excitation reference, sin, cos
c_2
b_2
a_2
a
b
c
PMSM
syncronization cable
slave-#1
slave-#n phase A cable
slave-#n phase B cable
slave-#n phase C cable
i_q^*, θ_e
$sync$
slave-#n
c_{n+1}
b_{n+1}
a_{n+1}

Figure 4.14: The overall block schema of the parallel operation of servo drives.

4.3.4 Dynamic Performances of the Parallel Operation

The parallel operation of servo drives feeding the PMSM is examined under startup, step torque disturbance, chirp torque disturbance, and step speed command conditions. In addition, the scenarios of one of the slaves leaving and re-entering and one of the phase outputs of a slave being open-circuited while the motor is running are also tested.

4.3.4.1 Startup Condition

To show the startup performance of the parallel-connected system, the mechanical speed reference is changed from 0 to 600 rpm, which is 60 Hz in electrical speed. Fig. 4.15 shows the measured phase A currents of the servo drives and the summation of these currents, which is the phase A current of the motor. As shown in the figure, the phase current of the motor is shared fairly well among the servo drives during startup.

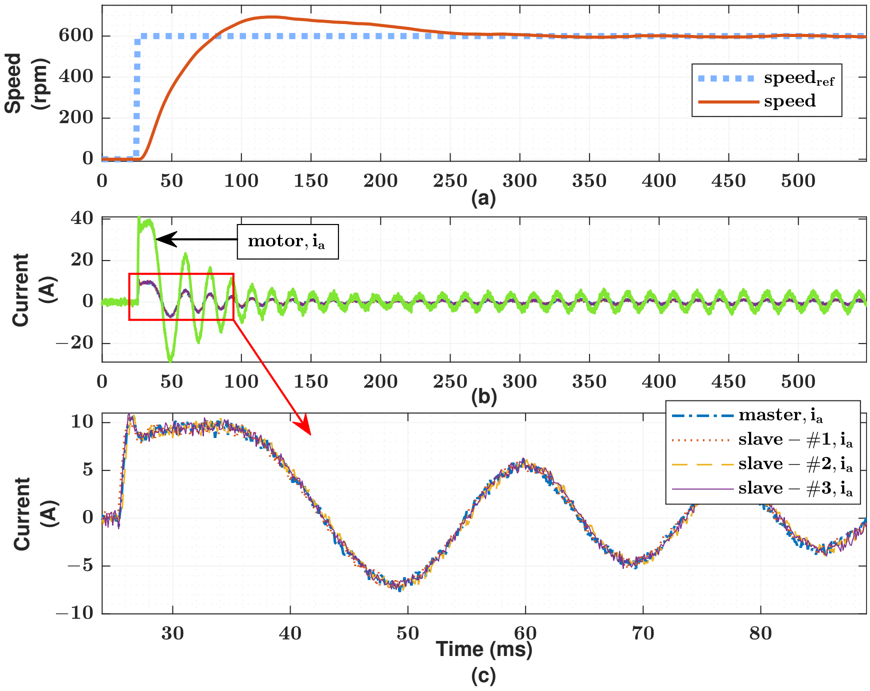


Figure 4.15: Speed of the PMSM and phase A currents of servo drives and PMSM at startup.

4.3.4.2 Step Torque Disturbance

Fig. 4.16 shows the step torque disturbance of the load motor. The torque varies between the half and full-rated torque capacities of the parallel operation. The phase current of the motor is divided evenly between the servo drives in step torque disturbances, as shown in Fig. 4.16f and Fig. 4.16g.

4.3.4.3 Chirp Torque Disturbance

Fig. 4.17 depicts another load type, the chirp torque disturbance, which is produced by the load motor. At the full rated torque capacity of the parallel operated system, the applied torque frequency changes from $0.1Hz$ to $1.0Hz$. Fig. 4.17b shows the quadrature axis current reference, i_{qref} (i_q^*), generated by the master servo module as well as the quadrature axis currents of all servo drives. As seen in Fig. 4.17b, the quadrature axis current of the motor is divided evenly among the servo drives.

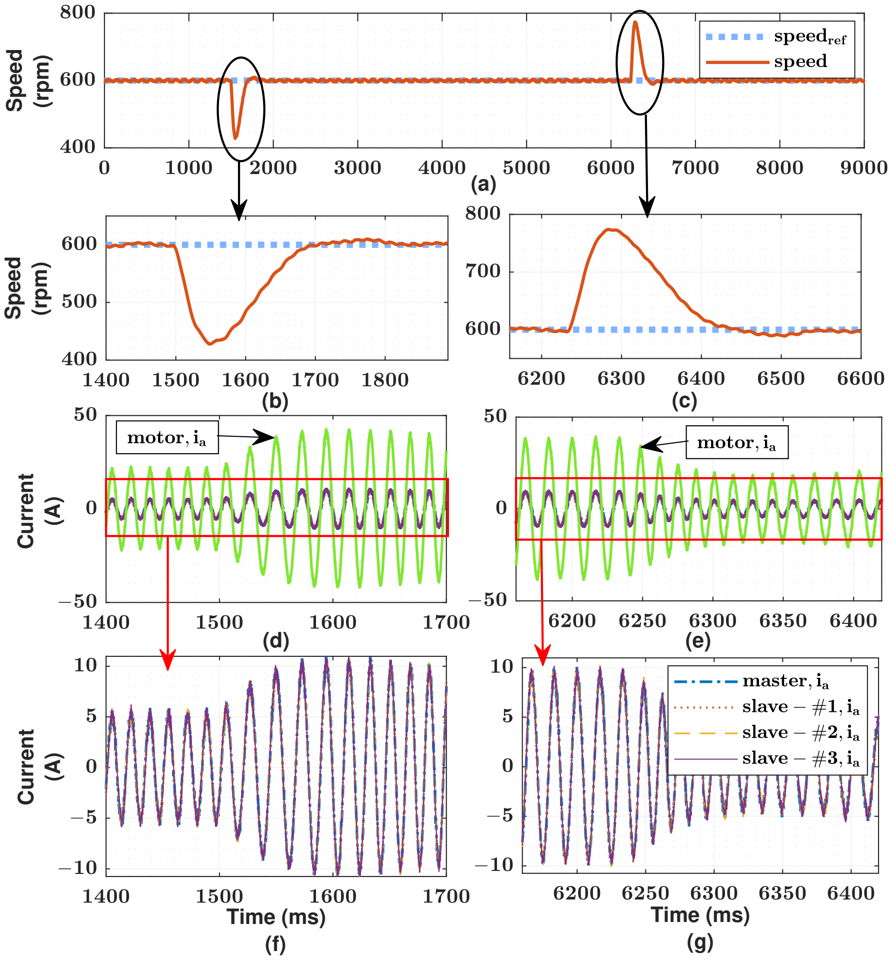


Figure 4.16: Speed of the PMSM and phase A currents of servo drives and PMSM with step torque disturbance.

4.3.4.4 Step Speed Reference

To examine the output of the parallel operating system under step speed references, the mechanical speed reference is changed between 600 rpm and 1200 rpm, as seen in Fig. 4.18.

As can be seen from the figures, Fig. 4.15b, Fig. 4.16d, Fig. 4.16e, Fig. 4.18d, and Fig. 4.18e, under startup, step torque disturbance, and step speed references, the phase current of the PMSM is the summation of the phase currents of the servo drives. As a result, the system's torque capacity increases linearly with the number of servo drives, and the PMSM phase current is quite evenly distributed among all servo drives.

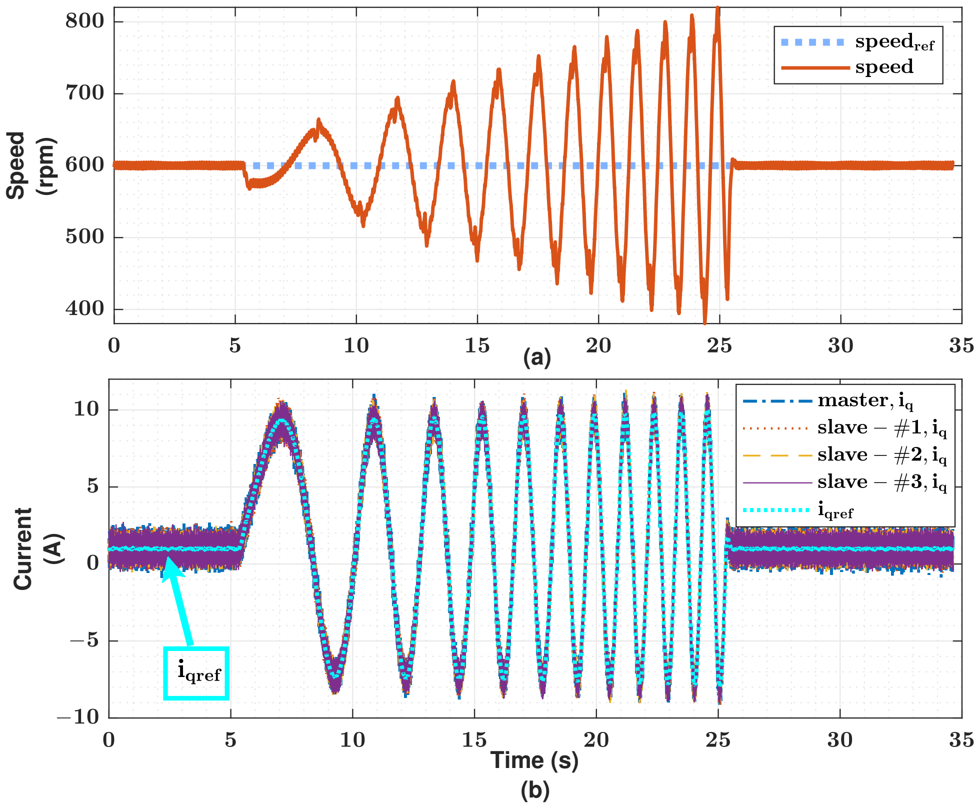


Figure 4.17: Speed of the PMSM and i_q currents of servo drives with chirp torque disturbance ($0.1Hz$ to $1.0Hz$ at full load).

4.3.5 Faulty Conditions of the Slaves

4.3.5.1 Turning Off the Slave-#3 During Operation

As seen in Fig. 4.19d and Fig. 4.19f, the slave-#3 servo drive is disabled by deliberately lowering the software current limit when the PMSM is running. An overcurrent fault condition has occurred and the PWM signals of the microcontroller of the slave-#3 servo drive are driven to high impedance. The fault is removed by setting the current limit back to the previous value, which allows the servo drive to resume functioning. This can be seen in Fig. 4.19e and Fig. 4.19g. The load torque is divided by the rest of the servo drives when the slave-#3 stops functioning and the PMSM still operates. Moreover, the servo drive can be re-commissioned into the system without interrupting the operation. This property would improve system reliability and add redundancy.

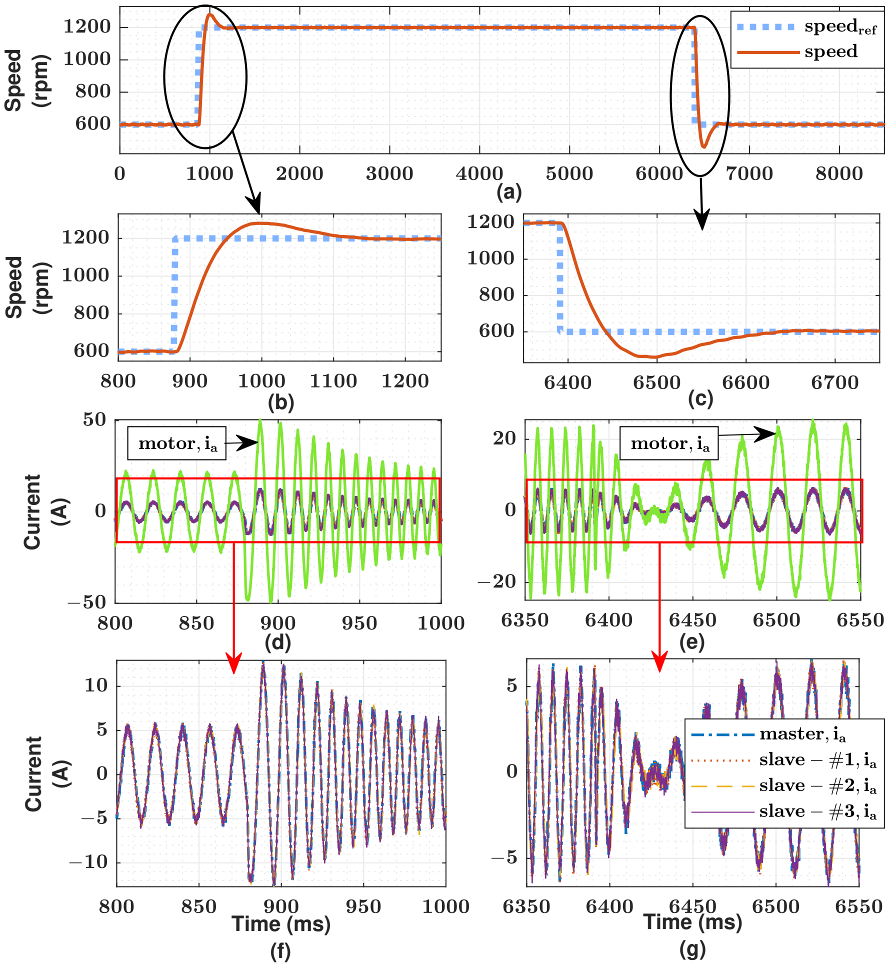


Figure 4.18: Speed of the PMSM and phase A currents of servo drives and PMSM with step speed reference variation.

4.3.5.2 Opening the Output of Phase A of the Slave-#2 During Operation

Assume that the system requirements have changed and that an additional servo drive is needed to produce the required torque. To demonstrate the modularity and flexibility of the proposed approach, two extra servo drives are added to the system, as shown in Fig. 4.20, one of which is redundant to enhance system reliability. The phase A output of the slave-#2 is open-circuited by a relay while it is operating. The current limit of one of the phase currents of the slave-#2 is exceeded, as can be seen in Fig. 4.21d, and the servo drive enters the trip zone. As can be seen in Fig. 4.21b and 4.21c, the load torque is well shared by the remaining five servo drives, and the operation continues without interruption.

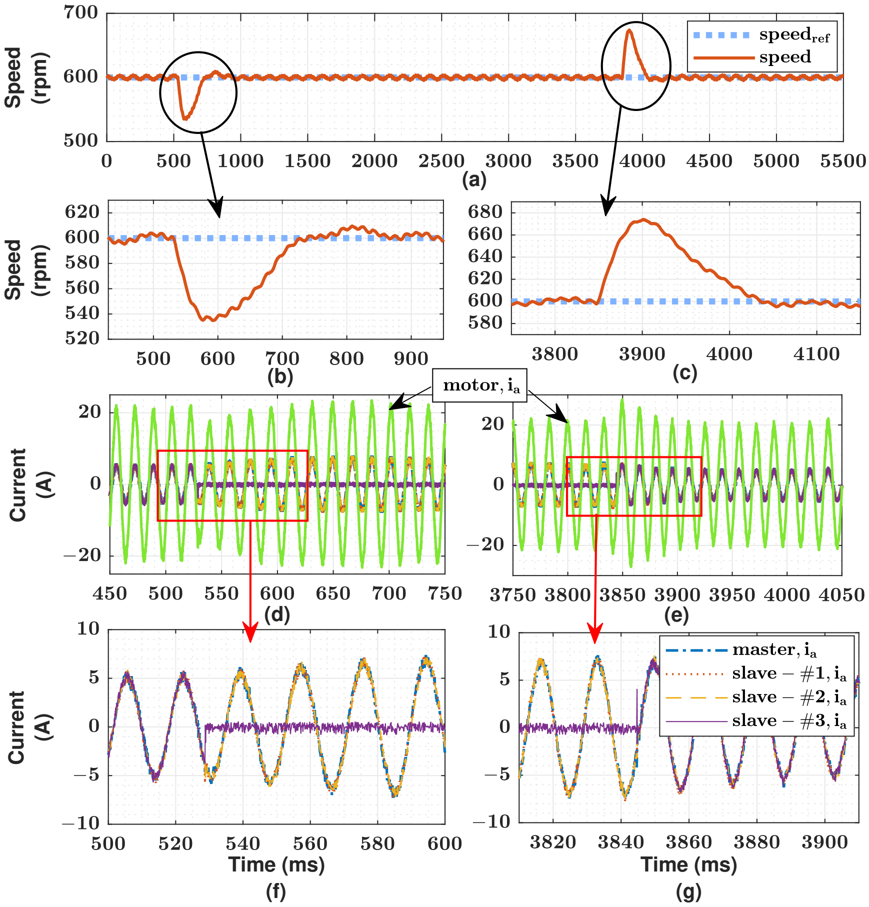


Figure 4.19: Speed of the PMSM and phase A currents of servo drives and PMSM, slave-#3 goes to faulty and back to a healthy condition by manually during operation.

4.3.6 Efficiency Comparison: Parallel vs. Single Operation

In this part, the efficiencies of the single and parallel operations are compared.

The same experimental setup shown in Fig. 4.9 is utilized to examine the efficiency of parallel and single operations. Only the master module feeds the PMSM during the single operation. For parallel operation, the master and slave-#1 are connected in parallel. The block diagram of the test setup used for efficiency comparison of the parallel and single operations is given in Fig. 4.22.

Where,
I_s : DC supply current
I_{s1} : DC supply current of the master

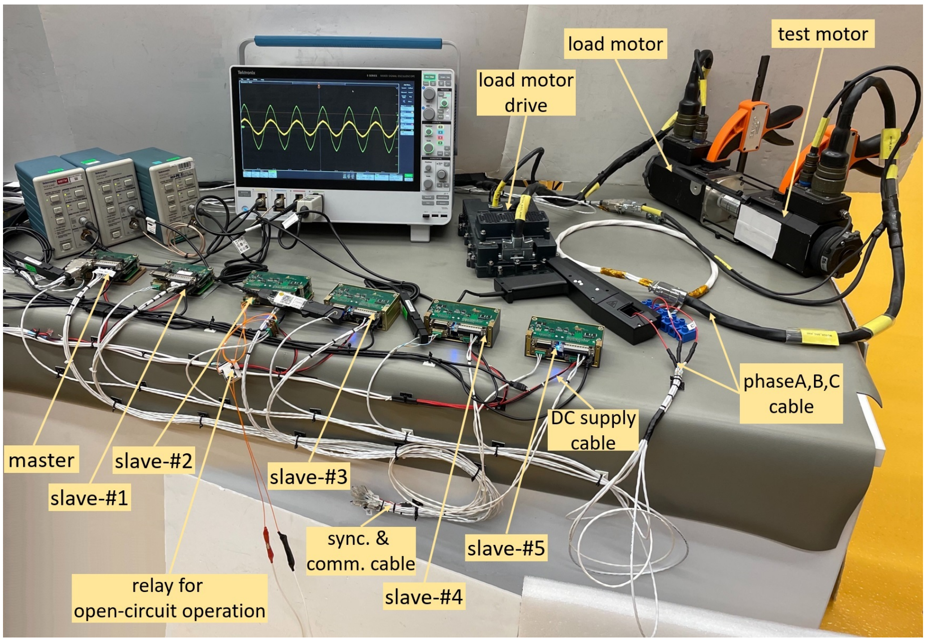

load motor
test motor
load motor drive
phaseA,B,C cable
DC supply cable
master
slave-#2
slave-#1
slave-#3
sync. & comm. cable
slave-#5
relay for open-circuit operation
slave-#4

Figure 4.20: Experimental setup with six parallel-connected GaN E-HEMT VSI-based servo drives.

I_{s2} : DC supply current of slave-#1
I_{m} : Motor phase current
I_{m1} : Motor phase output current of the master
I_{m2} : Motor phase output current of slave-#1
τ_{L} : Load torque
ω_{L} : Load angular speed (rad/s)
n_{L} : Load speed (rpm)

The parameters of the experimental setup are given in Table 4.3.

During the single operation, slave-#1 is disconnected. Hence, $I_{s2} = 0$ and $I_{m2} = 0$, which results in $I_s = I_{s1}$ and $I_m = I_{m1}$.

The calculations used to find the efficiency of the single operation and parallel operation experimentally are given in Table 4.4 and Table 4.5, respectively.

The results of the efficiency calculations of the single and parallel operations are presented in Fig. 4.23. At low load power outputs, ICs losses are dominant among the

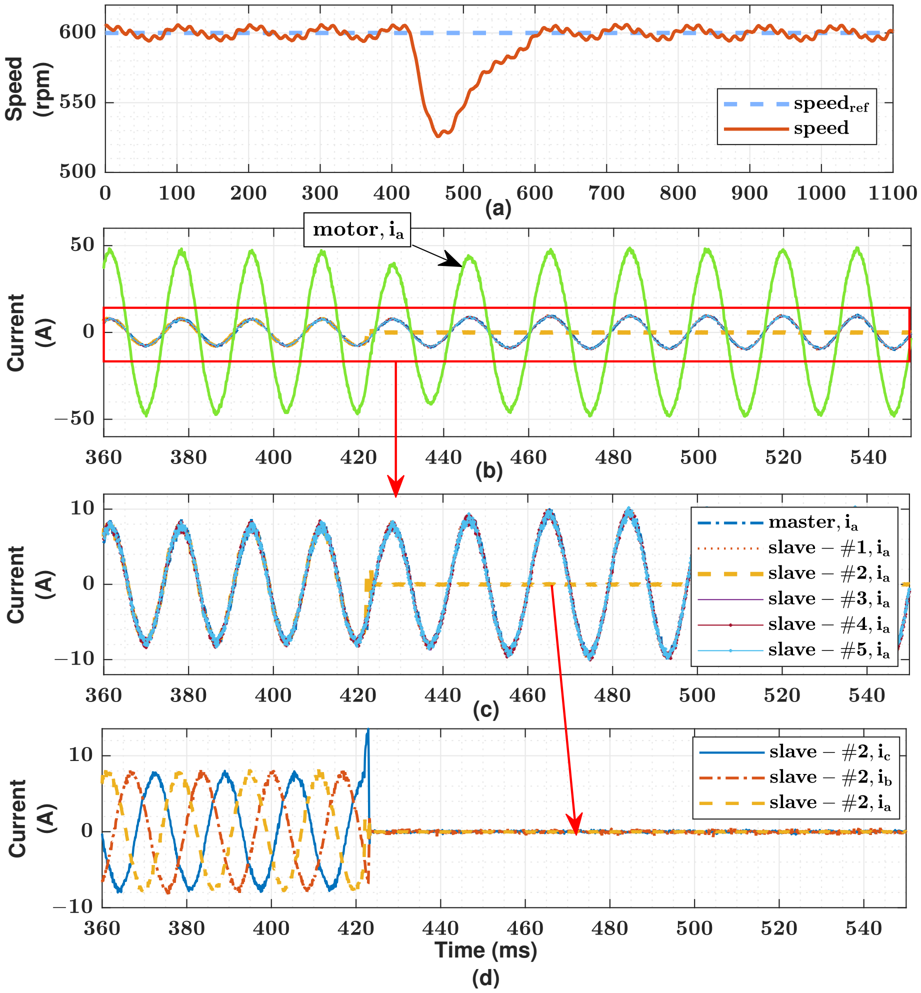


Figure 4.21: Speed of the PMSM, phase A currents of servo drives and PMSM, and phase currents of the slave-#2, phase A of the slave-#2 is open-circuited by a relay during operation.

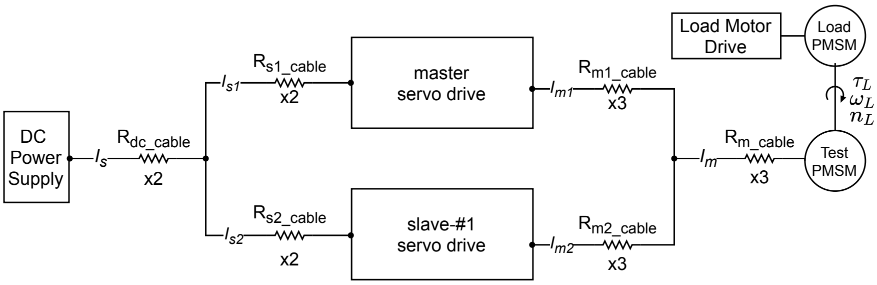

DC Power Supply
I_s
R$_{dc\_cable}$
x2
I_{s1}
R$_{s1\_cable}$
x2
I_{s2}
R$_{s2\_cable}$
x2
master servo drive
slave-#1 servo drive
I_{m1}
R$_{m1\_cable}$
x3
I_{m2}
R$_{m2\_cable}$
x3
I_m
R$_{m\_cable}$
x3
Load Motor Drive
Load PMSM
Test PMSM
τ_L
ω_L
n_L

Figure 4.22: The block diagram of the test setup for efficiency comparison of the parallel and single operation.

Table 4.3: Parameters of Experimental Setup for Efficiency Comparison of Parallel vs. Single Operation

Parameters	**Value**
DC link voltage	$24\ V$
Switching frequency	$200\ kHz$
Dead time	$10\ ns$
PMSM phase resistance, R_m	$4.13\ m\Omega$
PMSM torque constant, k_t	$0.067\ Nm/Arms$
Phase cable resistance, R_{m_cable}	$5.3\ m\Omega$
Phase cable resistance at the master output, R_{m1_cable}	$85\ m\Omega$
Phase cable resistance at slave-#1 output, R_{m2_cable}	$85\ m\Omega$
DC supply cable resistance, R_{dc_cable}	$20\ m\Omega$
DC supply cable resistance at the master input, R_{s1_cable}	$7\ m\Omega$
DC supply cable resistance at slave-#1 input, R_{s2_cable}	$7\ m\Omega$

Table 4.4: Efficiency Calculation of the Single Operation

Parameters	Equation
Load Torque	$\tau_L = k_t I_m \quad (4.13)$
Load Power	$P_L = \tau_L \omega_L \quad (4.14)$
Power output of the single operation	$P_{o1} = P_L + 3I_m^2(R_m + R_{m\_cable} + R_{m1\_cable}) \quad (4.15)$
Power input of the single operation	$P_{in1} = V_{dc}I_s - 2I_s^2(R_{dc\_cable} + R_{s1\_cable}) \quad (4.16)$
Efficiency of the single operation	$\eta_{meas} = P_{o1}/P_{in1} \quad (4.17)$

components of the servo drive, as can be seen also from Fig. 3.14. In parallel operation, these ICs losses are doubled, which results in lower efficiency compared with single operation. As the load power increases, conduction losses become dominant. Since the conduction current is shared among the servo drives in parallel operation, the efficiency of the parallel operation increases as the load power increases.

Table 4.5: Efficiency Calculation of the Parallel Operation

Parameters	Equation
Power output of the parallel operation	$P_o = P_L + 3I_m^2(R_m + R_{m\_cable}) + 3I_{m1}^2 R_{m1\_cable} + 3I_{m2}^2 R_{m2\_cable}$ (4.18)
Power input of the parallel operation	$P_{in} = V_{dc}I_s - (2I_s^2 R_{dc\_cable} + 2I_{s1}^2 R_{s1\_cable} + 2I_{s2}^2 R_{s2\_cable})$ (4.19)
Efficiency of the parallel operation	$\eta = P_o/P_{in}$ (4.20)

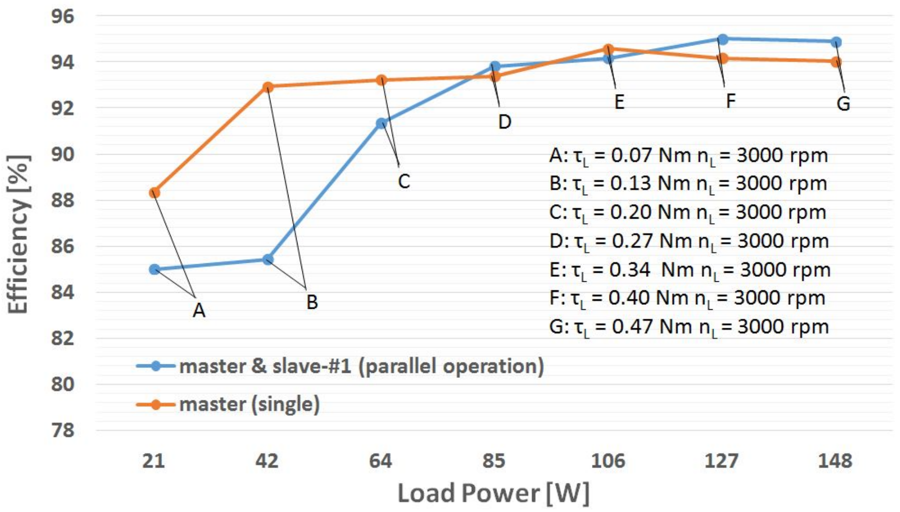


Figure 4.23: The results of the efficiency calculations of the single operation and parallel operation.

In parallel operation, the slave servo module may be disabled to reduce losses while the system operates at low load output power. If the load power increases to a level that can be decided by the phase current of the master module, the servo module can be recommissioned to the system again. To realize this scenario, the application should be able to tolerate the time delay caused by the recommissioning of the slave servo module.

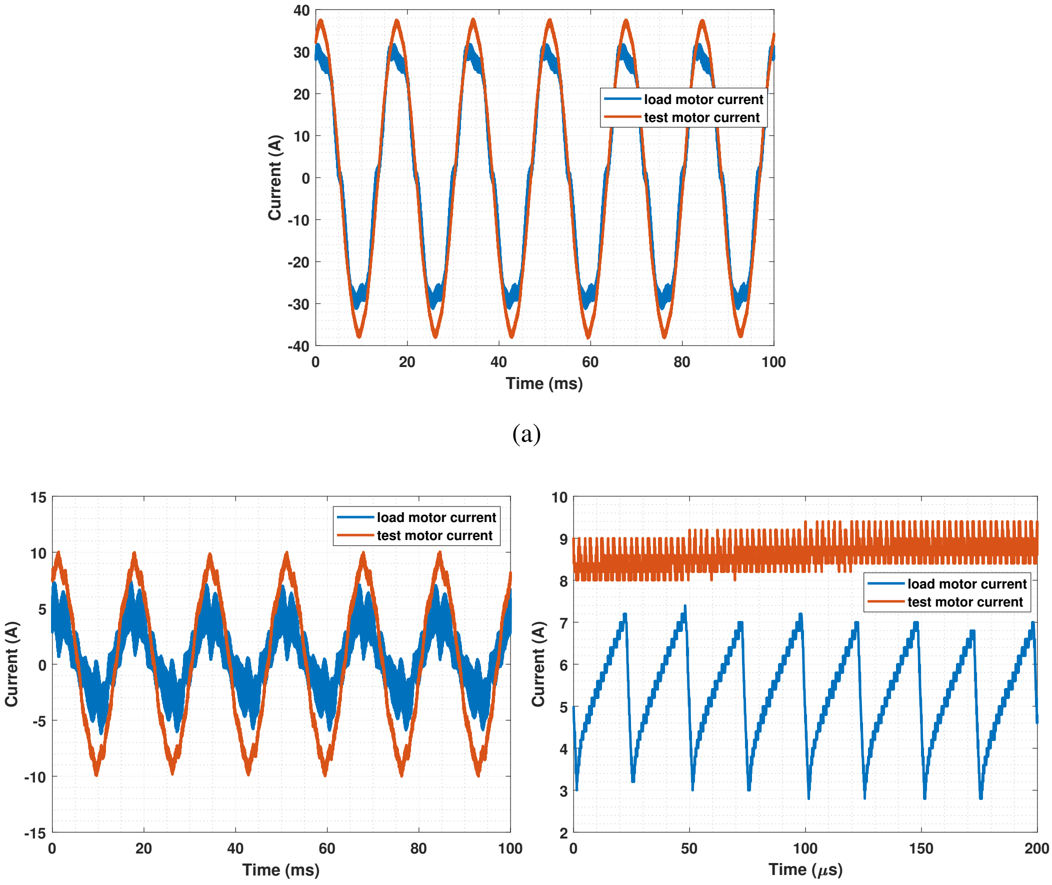
4.3.7 Current Ripple Comparison

In this part, the phase current ripples of the test motor, which is driven by the parallel-connected GaN E-HEMT VSI-based servo drives, are compared with the load motor, which is driven by a Si MOSFET VSI-based servo drive.

To produce torque disturbances, a load motor of the same type as the test motor is used. This motor is driven by a Si MOSFET VSI-based servo drive, which is called the load motor drive, as shown in Fig. 4.9. Each half-bridge of the Si MOSFET VSI is composed of two Si MOSFETs (IRFP4468) and their gate driver (FAN7391). The switching frequency of the servo drive is $20\ kHz$, and by considering the gate driver and Si MOSFET time parameters, the dead time is set to $1.33\ \mu s$. Fig. 4.24a depicts the phase A currents of the test and load motors. The test motor is driven by four parallel-connected GaN E-HEMT VSI-based servo drives, as shown in Fig. 4.9. The current ripple increases as the switching frequency decreases. To make it easier to see, the load torque is reduced, and the results are depicted in Fig. 4.24b and Fig. 4.24c. It is worth noting that the motors used in the experiment have a phase inductance of just $12\ \mu H$, as indicated in Table 4.2. As can be seen in the figures, the current ripple is decreased as the switching frequency is increased by using the high switching capability of the GaN E-HEMT.

4.4 Chapter Summary

In this chapter, the circulating current generated by the carrier phase difference of parallel-connected inverters is investigated in detail. The problem of continuous carrier phase angle drift caused by clock discrepancies across microcontrollers in each servo drive is demonstrated experimentally. The synchronization of the carrier signals eliminates the carrier phase angle variation between inverters. By increasing the switching frequency, the circulating current produced by inherent hardware variations is minimized. GaN E-HEMT-based servo drives are utilized for this purpose, with no additional extra inductors. The performance of the parallel operating servo drives that feed a PMSM is then evaluated under a variety of conditions. These dynamic performance tests demonstrate that the PMSM currents are distributed evenly among the



(a)

(b) (c)

Figure 4.24: Phase A currents of test and load motor (a) at higher torque (b) at lower torque (c) at lower torque in the switching time domain.

servo drivers. The consequences of faulty servo drive conditions on the system are also studied in the chapter. Furthermore, the efficiency comparison of single-versus-parallel operations is examined. Finally, the current ripples of the test motor with the load motor are compared.

CHAPTER 5

CONCLUSIONS

5.1 A Short Synopsis of the Thesis

For a specific target tracking radar application, due to the system requirements, the target switching frequency of the servo drive is taken as $100\ kHz$ throughout the thesis to get the desired position control bandwidth. In this study, VSI is preferred instead of CSI for the servo drive due to its lower size and higher dynamic response. It is also suitable for low-power and low-voltage applications like the target tracking radar application.

The effects of nonlinearities in VSI on the phase current and current controller are explored in this work by utilizing a coreless low inductance PMSM and a Si MOSFET-based VSI-fed motor drive. The effects of increasing switching frequency on nonlinearities are demonstrated. Furthermore, it is shown that the response of the current controller is different for nonlinear and linear regions of the d and q axes. A compensating strategy is proposed by developing a mapping function of $f(i_d)$ to linearize the u_d-i_d relation, and the applicability of this technique is tested experimentally. However, obtaining such a function for all operational conditions is impractical.

To address the aforementioned issues, a GaN E-HEMT-based VSI-fed PMSM drive is presented. The same experiments are carried out on the GaN E-HEMT-based VSI, and the results are compared to the Si MOSFET-based case where the switching frequency of the servo drives is $100\ kHz$. By considering the electrical time parameters of the gate driver and the power switch, the dead time of the GaN E-HEMT VSI based servo drive is set to $20\ ns$, and $1\ \mu s$ for the Si MOSFET VSI based servo drive. It is demonstrated that the performance of a GaN E-HEMT-based VSI is preferable for high-bandwidth control applications. This is mostly owing to the low gate charge, low output capacitance, and near-zero reverse recovery current, all of which resulted in a substantially shorter dead time. The influence of dead time on the bandwidth of the current controller of the GaN E-HEMT-based VSI is also investigated while the PMSM is under load. The i_d current is around zero due to the FOC method being used with a zero i_d current reference. Since this value is in the nonlinear region of the u_d-i_d curve, the bandwidth of the i_d current controller is reduced by about 36% when the dead time is intentionally increased to $200\ ns$. However, the i_q current controller is not affected so much by this dead time increase during the test. Because the value of the i_q is about $2.3A$ to supply the load torque and this value is in the linear region.

The dead time of the VSI should be kept to the minimum value by taking the gate driver and power switch time parameters into account, along with a safety factor. It is demonstrated that as the dead time value decreases, nonlinearities in VSI, THDs of output phase current, and 3rd conduction losses also decrease. To achieve a high current controller bandwidth, the switching frequency should be increased. As the switching frequency increases, the nonlinearity in VSI also increases. This is mainly because of the increasing ratio of dead time over the switching period. As stated above, dead time influence on the current controllers depends on the operating regions of the quadrature currents. Hence, the operating torque region of the system should also be taken into consideration, besides the required current control bandwidth, switching losses, current ripples, etc., when deciding the value of the switching frequency of the VSI.

Based on the findings on nonlinearities in VSI research, a GaN E-HEMT VSI-based servo drive is designed to replace its Si MOSFET VSI-based counterpart. Details on a three-phase, two-level GaN E-HEMT VSI-based servo drive design, as well as load and conducted emission tests, are provided. The size of the proposed servo drive is about 44% of the previous one, allowing for the use of two parallel servo drives instead of one to provide redundancy.

There are several advantages to using parallel-connected servo drives, including improved torque capacity (and hence power output), reliability, redundancy, and modularity. Minor differences in the system clocks of the individual microcontrollers, asynchronous PWM carrier signals, and hardware variances, on the other hand, will lead to non-identical output voltages of the parallel modules, causing circulating currents across inverters. The circulating current induced by the carrier phase difference of parallel-connected inverters is investigated case by case, with results validated through simulation and experimentally. The problem of carrier phase angle drift induced by clock differences across separate microcontrollers in each servo drive is illustrated experimentally.

The synchronization of the carrier signals eliminates the carrier phase angle mismatch between inverters. By increasing the switching frequency, the amplitude of the circulating current produced by inherent hardware variances is minimized. For this reason, GaN E-HEMT-based servo drives are used, with no extra inductors at the servo drives' outputs. The performance of the four parallel-connected servo drives, with an output current limit of 4 x 7 A_{rms}, that drive a 24 V PMSM, which has a nominal current of 61.9 A_{rms}, is examined under a variety of scenarios, such as at

- startup, 0 rpm to 600 rpm, that is 0 Hz to 60 Hz in electrical speed, at no load,
- step torque disturbance, half rated 4 x 3.5 A_{rms} to full rated 4 x 7 A_{rms} output phase current, at 60 Hz electrical speed,
- chirp torque disturbance, the applied torque frequency is changed from 0.1 Hz to 1.0 Hz,
- step speed reference, 600 rpm to 1200 rpm, that is 60 Hz to 120 Hz in electrical speed, at half rated torque.

These dynamic performance tests demonstrate that the PMSM currents are distributed evenly across the servo drivers. The torque capacity of the system increases linearly with the number of servo drivers.

The impacts of servo drive failure on the system are also examined. While the system is running at 60 Hz electrical speed at half rated torque, that is, each servo drive has 3.5 A_{rms} phase output current, one of the slaves is deactivated and then manually reactivated. It is shown that the system continues to run without any interruption. The load torque is distributed across the remaining servo drivers such that the phase output currents of the remaining servo drives are increased to $4.7\ A_{rms}$.

To demonstrate the modularity and flexibility of the proposed approach, two additional servo drives are installed on the parallel-connected servo drive system, so total output current limit of the system increases to 6 x $7\ A_{rms}$ per phase. One of the slaves is utilized for redundancy. Another fault condition is studied at $60\ Hz$ electrical speed, while each servo drive has around $5.83\ A_{rms}$ of output phase current. The output of one phase of the slave is open-circuited during the operation. The load torque is shared among the remaining five servo drivers in this case as well, such that the output phase currents of the remaining servo drives increase to $7\ A_{rms}$. These characteristics will increase the system's reliability and redundancy in the event of servo drive failures, which will be critical for applications that demand high reliability.

Finally, the efficiencies of the single and parallel operations are compared. In the single operation, only the master servo module is utilized, and it is loaded up to approximately 150 W. For the parallel operation, the master and a slave servo drive are connected in parallel, and are also tested under the same load power. At low load powers, the efficiency of the parallel operation remains below that of the single operation due to ICs losses being dominant. But as the load power increases, the efficiency of the parallel operation also increases. Because the conduction currents are shared among the servo drives and this results in lower conduction losses in parallel operation.

5.2 Literature Contributions

One conference paper and two journal papers are published as part of this thesis, as indicated in Appendix A.

The following are the primary contributions of the thesis:

This study will help researchers compare nonlinearities in GaN E-HEMT and Si MOSFET-based VSIs. The work originated after facing difficulties in tuning current controllers in the zero-crossing regions during the sequential control loop tuning. Upon researching the difficulties, it was found that the problem stems from the nonlinearity in the zero-crossing region of u_q vs i_q and u_d vs i_d curves, which is mainly dependent on the dead time in addition to the other effects. Not only the nonlinearities in VSIs are investigated and the findings are reported, but also how this nonlinearity affects the current control bandwidth is demonstrated. It is pointed out that nonlinearity effects should be considered when the controller tuning is done at the zero crossing regions of the d and q axes.

As the switching frequency increases, the dead time effect on nonlinearity also increases. However, it is demonstrated that the effect of dead time on current controller bandwidth depends on the system's operating point in the d and q axes. For this reason, the operating torque region of the system should also be taken into consideration when deciding the value of the switching frequency of the VSI.

The effect of dead time on the phase current harmonic distortions is also presented in this work. It is demonstrated that the lower dead time means lower nonlinearities in VSI, lower THDs of output phase current, and lower 3^{rd} conduction losses. Hence, it should be kept as minimal as possible.

The circulating current caused by the phase difference of PWM carrier signals in parallel-connected inverters is explored analytically case by case, and the results are validated by simulation and experiment. The issue of carrier phase angle drift induced by clock differences between various microcontrollers in each servo drive is highlighted. A fault-tolerant parallel-connected GaN E-HEMT VSI-based servo drive scheme is proposed and verified by various tests, which removes the requirement for extra output inductors and separate DC supplies at the input while allowing the use of a conventional PI current control and SVPWM method. Although the synchronization of the carrier signals eliminates the circulation current caused by phase carrier difference and clock discrepancy, the study emphasizes that the circulation current caused by inevitable hardware variations can be decreased with the benefit of the GaN E-HEMT's high switching capability.

Experimental parameters are given in Table 5.1 to compare the proposed scheme with other studies in the literature where the main focus is to reduce the high-frequency circulating currents caused by asynchronous carriers. As shown in the table, by utilizing the GaN E-HEMT's high-frequency switching capabilities, up to six inverters,

Table 5.1: Experimental Parameters of the Studies in the Literature

Parameters	W. Jiang et al. [111]	Z. Xueguang et al. [100]	S.-W. Kang et al. [18]	J. Hu et al. [113]	This study
DC-link voltage	670 V	400 V	311 V	30 V	24 V
# of parallel inverters	2	2	2	3	6
Switching frequency	6 kHz	5 kHz	5 kHz	1 kHz	200 kHz
Output inductor for each inverter	4 mH	6 mH	2.5 mH	3 mH	not required
Communication for carrier synchronization	no	no	no	no	yes
Other Communication	i_d^*, i_q^*	no	i_q^*	no	i_q^*, θ_e

which results in a total output current limit of 6 x 7 A_{rms} per phase, can be connected in parallel without the use of any extra inductors at the phase outputs of each inverter.

Note that although the circulating current generated by the phase mismatch of the carrier signals and clock discrepancies of the microcontrollers of the parallel-connected inverters is removed by synchronizing the carrier signals, high frequency circulating currents can still occur. This is due to instantaneous variations in the output voltages of the parallel-connected inverters induced by unavoidable hardware differences. By increasing the switching frequency, the amount of the circulating current produced by inherent hardware variations is minimized without the need for extra inductors at the phase outputs of the inverters. The number of inverters can be increased further; the only constraint is the bus capabilities of the synchronization and communication lines.

5.3 Prospects for the Future

There are certain concerns that can be considered future research within the context of this thesis such as:

- In Chapter 4, faulty conditions are demonstrated, such as one of the slaves being disabled during the operation and then enabled again, and one of the output phases of a slave being open-circuited. These analyses can be expanded further for future work. For instance, as explained in the chapter, the master module provides the synchronization signal and sends the quadrature axis current reference (i_q^*) and the rotor angle (θ_e) to the slave modules. How can a slave take control if the master module has problems generating the synchronization signal and/or producing the rotor angle?

- Although the synchronization of the carrier signals eliminates the carrier phase angle variation between the parallel-connected inverters, high frequency circulating currents can still occur due to instantaneous variations in the output voltages of the inverters induced by unavoidable hardware differences. In this study, GaN E-HEMT-based servo drives are utilized to reduce these circulating currents by increasing the switching frequency. The importance of the high switching capability of a power device can be emphasized by constructing a similar test setup but instead of GaN E-HEMT, Si MOSFET-based VSI servo drives may be used without any additional inductors at the output. Will the circulating current be under desired values?

- In Chapter2, a compensating strategy is proposed by developing a mapping function of $f(i_d)$ to linearize the u_d-i_d relation. The u_d versus i_d graph is divided into sections and curve fitting is used on each section to determine the function of $f(i_d)$. This is used at the output of a classical PI current controller. Instead of this method, maybe a different current controller can be used, such as a controller that has different tune parameters with respect to the magnitude of the i_d current. Can a fuzzy control be suitable for this purpose?

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APPENDIX A

PUBLICATIONS ARISING FROM THE THESIS

This thesis has resulted in the following publications:

Ref. #	Title	Published at
[117]	High Bandwidth Current Control via Nonlinear Compensation and GaN-based VSI	CPE-POWERENG 2019, Sonderborg, Denmark
[116]	Comparison of the Effects of Nonlinearities for Si MOSFET and GaN E-HEMT Based VSIs	IEEE Transactions on Industrial Electronics, 2021
[115]	Parallel connected GaN E-HEMT VSI-based servo drives for PMSMs	IET Electric Power Applications, 2021

CURRICULUM VITAE

PERSONAL INFORMATION

Surname, Name : Yürük, Hüseyin

EDUCATION

Degree	Institution	Year of Graduation
MS	METU Electrical and Electronics Engineering	2008
BS	Hacettepe Electrical and Electronics Engineering	2005
High School	Sülayman Demirel Fen Lisesi, Isparta	2000

WORK EXPERIENCE

Year	Place	Enrollment
2005-Present	Aselsan	Analog Design Engineer

FOREIGN LANGUAGES

Advanced English, Elementary German

PUBLICATIONS

1. I. Ulusoy and H. Yuruk, "New method for the fusion of complementary information from infrared and visual images for object detection", IET Image Processing, vol. 5, no. 1, pp. 36–48, 2011.
2. H. Yürük, O. Keysan, and B. Ulutas, "High Bandwidth Current Control via Nonlinear Compensation and GaN-based VSI", IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), pp. 1–7, 2019.

3. H. Yuruk, O. Keysan, and B. Ulutas, "Comparison of the Effects of Nonlinearities for Si MOSFET and GaN E-HEMT Based VSIs", IEEE Transactions on Industrial Electronics, vol. 68, no. 7, pp. 5606–5615, 2021.
4. H. Yuruk and O. Keysan, “Parallel connected GaN E-HEMT VSI-based servo drives for PMSMs", IET Electric Power Applications, vol. n/a, no. n/a, 2021.

HOBBIES

Snooker, Air Crash Investigation Documentaries