MODELING OF GAN POWER TRANSISTOR PACKAGE FOR DESIGN OF BROADBAND HIGH-POWER AMPLIFIER

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ÖZLEM BAŞTÜZEL ÇAKMAK

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ABSTRACT

MODELING OF GAN POWER TRANSISTOR PACKAGE FOR DESIGN OF BROADBAND HIGH-POWER AMPLIFIER

Baştüzel Çakmak, Özlem
Master of Science, Electrical and Electronic Engineering
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Radio frequency (RF) power amplifiers (PAs) are the most crucial part for the development of high performance front-end RF and microwave systems. Power transistor is the key component of a power amplifier, which should be accurately modeled to provide good correlation between simulation and measurement results. Bare die transistor needs to be packaged, before attaching on printed circuit boards (PCBs) to provide protection, easy fabrication and prevent mechanical issues. In recent years, Gallium Nitride (GaN) High Electron Mobility (HEMT) transistors are popular because of high output power, high reliability and high frequency operation capabilities. This thesis reports modeling of an air cavity ceramic package for bare GaN HEMT die transistor to design 0.5-3 GHz broadband PA with 50 W output power and 40 % drain efficiency. For package modeling, two approaches are utilized which are lumped element model based on analytical equations and a numerical model based on full-wave electromagnetic (EM) simulations by Advance Design System (ADS) software. The package and designed PA are fabricated and measured for performance validation. The results show a very good agreement with the simulations, indicating the validity of the modeling methodology.

Keywords: Bare Die Transistor, Air Cavity Ceramic Package, PA, Modeling, GaN HEMT

ÖZ

GENİŞ BANTLI GÜÇ YÜKSELTEÇ TASARIMI İÇİN YÜKSEK GÜÇLÜ GAN TRANSİSTÖR PAKETİNİN MODELLENMESİ

Baştüzel Çakmak, Özlem
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Şubat 2022, 118 sayfa

RF güç yükselteçler, yüksek performanslı aktif RF ve mikrodalga sistemlerinin geliştirilmesinde en önemli parçalardır. Yüksek güçlü amfi tasarımında ölçüm ve simülasyon tutarlılığı açısından, doğru modellenmiş güç transistör kullanmak kritiktir. Çip transistörler, koruma, üretim kolaylığı ve mekanik güç gerekliliği sebepleriyle, baskı devre kartı tasarımlarında paketlenerek kullanılmalıdır. Son yıllarda, yüksek çıkış gücü, yüksek güvenilirlik ve yüksek frekanslarda çalışabilme yetenekleri sayesinde Gallium Nitride (GaN) High Electron Mobility (HEMT) transistörler oldukça popülerdir. Bu tezde, 0.5-3 GHz geniş bandında 50 W çıkış gücü ve 40 % verimlilik sağlayabilen yüksek güçlü amfi tasarımında kullanmak üzere paketlenmiş GaN HEMT çip transistör modellenmiştir. Paket modellemede, ADS kullanılarak simüle edilen 3 boyutlu model ve analitik denklemlere dayanan yığın eleman modeli olmak üzere iki yaklaşım kullanılmıştır. Paket ve tasarlanan amfinin üretimi ve ölçümleri tamamlanmıştır. Simülasyon sonuçları ile modellerin tutarlılığı karşılaştırılmıştır.

Keywords: Çip Transistör, Hava Boşluklu Seramik Paket, Yüksek Güçlü Amfi, Modelleme, GaN HEMT

To my Family…

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CHAPTER 1

INTRODUCTION

1.1 Background

1.1.1 RF Power Amplifiers

RF PA is a critical component of transmitters which amplify the power of signal being transmitted [1]. PAs operate in nonlinear large signal operation region, which results in distortion of the signal reducing the efficiency of transmission. Furthermore, efficiency should be high to prevent power dissipation. To maximize efficiency, harmonic terminations may be presented to the output of the transistor [1]. Also, because of the need for high-speed wireless transmitters, the bandwidth of PAs should be enhanced. To design a broadband PA, design architectures should be modified which is very challenging.

RF PAs have following characteristics as given below [2];

- RF response with a limited band
- Direct current (DC) to RF conversion efficiency of less than 100 %
- RF coupled response with no DC
- Nonlinearity which results in mixing products from numerous signals
- Phase difference between the input and output
- Higher gain at low temperatures, in other words, temperature dependent gain
- Power dependent amplitude

It is possible to divide the history of PAs in three eras [3]. First one is the era of waveguides and microwave vacuum tubes that extend over 10 GHz in terms of practical devices. The second era of PAs is a longtime period which is through 1960s

until the end of the 1980s [3]. Major new developments such as reduction in size, which is achieved by using integrated circuits, are achieved in this term. During this era, many of the military systems are developed by using chip components, which are attached to the ceramic substrates. Today, this technology is known as Microwave Integrated Circuit Technology (MIC), which is still an integral part of microwave components in the high frequency band [3]. The third era of PA technology is wireless communications which can be characterized by low cost and high-volume complex systems. More functional chips and high frequency packaging advances are observed. Broadband techniques are placed aside, because all military systems are inherently broadband.

The first one of the two of leading field effect transistors (FETs) is lightly doped metal-oxide semiconductor (LDMOS), which is a low-cost transistor used below 3 GHz applications [1]. The second one is the GaN HEMT, whose operating frequency reaches up to mm-waves because of its high electron mobility feature. Drain voltages of both technologies are very large up to 60 V, which provides high output power levels [1]. For GaN devices, drain voltage up to 90 V is also possible [1].

GaN HEMT structure is given in Figure 1.1, which shows source to drain cross-section of a single finger of die transistor.

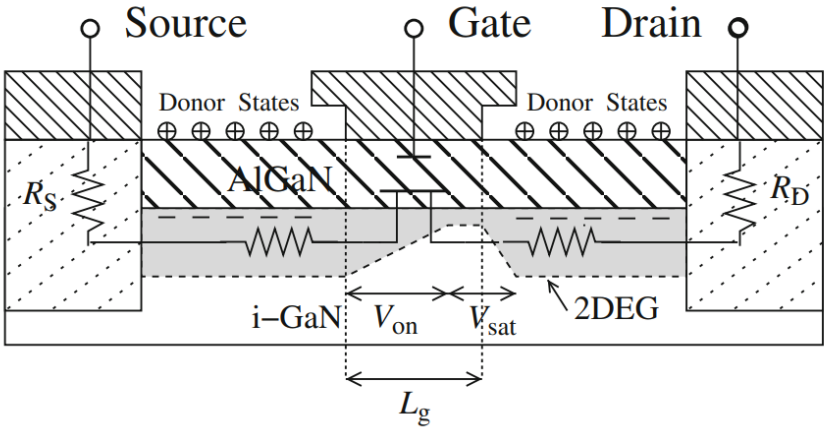


Figure 1.1: Cross-section of GaN HEMT [1]

Source and drain electrodes are placed at the top of the Aluminium Gallium Nitride (AlGaN) layer, which creates an ohmic contact with 2-Dimensional Electron Gas (2DEG). AlGaN layer presents wide bandgap which acts as an insulator for field effect transistor. Short circuit is created between source and drain electrodes until 2DEG pool of electrons is depleted and GaN crystal blocks the current flow. In order to deplete 2DEG pool of electrons, the gate electrode is placed on the AlGaN layer. By applying a negative voltage to the gate electrode relative to the drain and source, device can be turned off. This is why the device is named as depletion mode transistor. Thus, a negative voltage must be applied to the gate of the transistor in order to prevent short circuit [4]. Because the channel is undoped, electrons in 2DEG region present high mobility which is the reason that FET is calling as HEMT.

1.1.2 RF Packages

RF packages are commonly used for telecommunication and military applications [4]. In general, transistors are placed in low-cost plastic packages for commercial applications. However, for military applications, custom packages are designed in order to obtain higher performance and reliability [4]. With respect to modeling methods, operating frequency band and cost, RF packaging technologies are quickly growing up.

Selecting an appropriate package and assembly technique has an important effect on performance, reliability and cost of a transistor. Effects of assembly techniques and package parasitic should be minimized during packaging process in order to prevent performance degradation of transistor. Also, package complexity should be considered to minimize the cost.

Most commonly used packaging method is first level package assembly which means transistor is placed in individual package as seen in Figure 1.2 [4]. First level package assembly includes die bonding and wire bonding. The most critical challenge in first level package assembly is to prevent effect of assembly on performance of RF component. The most important parameters that should be taken

into consideration are bond wire dimension, lead dimension, grounding effect of leads and thermal effect of package materials to keep temperature of transistor in the safe zone.

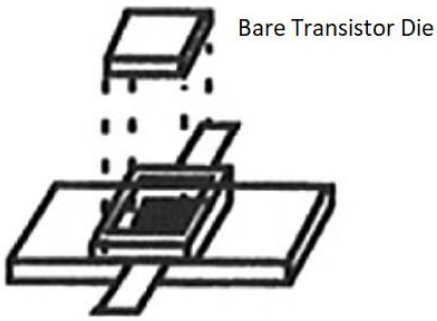


Figure 1.2: First Level Package Assembly [4]

Specifications of the packaging depend on application. For example, in communication applications below 18 GHz and low power operations, Gallium Arsenide (GaAs) technology transistors are housed in plastic packages to decrease the cost. However, for high power, high frequency and high performance requirements, ceramic packages with metal base are required because of low thermal resistance, high power capability and better reliability [4].

1.1.2.1 Types of RF Packages

RF packages can be classified according to their material, which are determined with respect to operating frequency, thermal reliability, cost, dissipated power and etc. The basic package types are ceramic and plastic packages.

1.1.2.1.1 Ceramic Packages

Ceramic packages comprise of a ceramic material as a base material under the leads, in order to provide high isolation and lower loss [4]. Bare die transistor is placed in an air cavity with a ceramic or metal lid on the top. Die is generally soldered on the metal base to provide heat transfer from the package. For high power applications,

metal base which is named as flange is directly attached to the heat sink. Depending on the environmental requirements, packages can be hermetic or non-hermetic. The ceramic packages can be surface mounted on PCB or soldered on modules. Different examples of air-cavity ceramic packages are shown in Figure 1.3 [4].

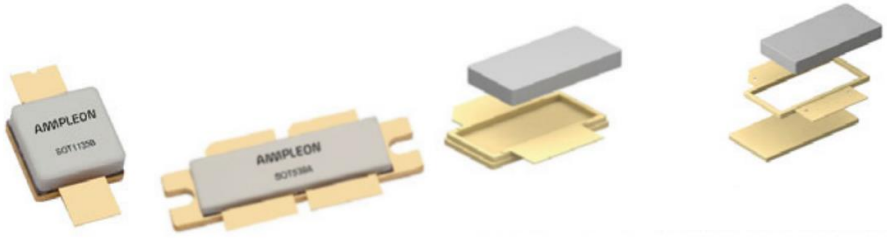


Figure 1.3: Air-cavity Ceramic Package Examples [4]

1.1.2.1.2 Plastic Packages

Plastic packages are generally covered with plastic molding compound, no lid is involved and there is no air cavity [4]. The molding compound has an impact on the operating frequency of the transistor at high frequencies. Because of material properties of plastic, isolation between the leads of the plastic packages is lower. Also, plastic packages are non-hermetic. Although plastic packages have lower isolation and operating frequency, they are more suitable for high volume manufacturing because of their low cost.

The lead frame is the supporting structure for die attach in the plastic packages. The lead frame is sealed from a thin metal. Die is attached on the lead frame with electrically conductive epoxy. Examples of plastic packages are given in Figure 1.4 [4].

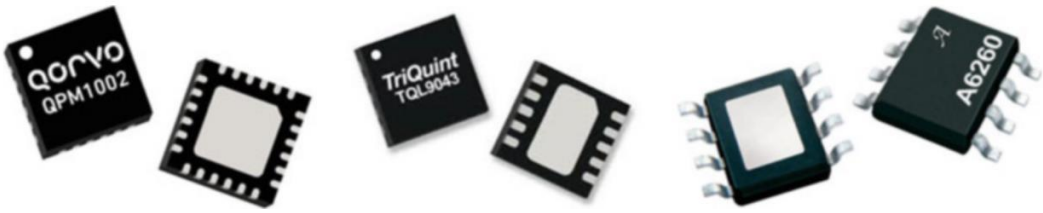


Figure 1.4: Plastic Package Examples [4]

1.1.2.2 Materials for RF Packages

Types of materials used in the RF packages are given in this part.

1.1.2.2.1 Ceramics

Substrate materials of ceramic packages are generally alumina (Al_2O_3), aluminum nitride (AlN), beryllium oxide (BeO), glass (SiO), glass alumina (LTCC) or silicon carbide (SiC) [4]. Al_2O_3 is the most popular substrate material between them. High melting point and chemical stability are the most important features of ceramic materials. Furthermore, electrical, thermal and mechanical properties of ceramic materials are perfectly combined.

1.1.2.2.2 Metals

The most popular lead material of ceramic packages is kovar [4]. Kovar has good thermal expansion coefficient (CTE) match with ceramics. In contrast to all good specifications, kovar has poor thermal conductivity. Thus, kovar is used at package leads in high power applications and as a flange in low power applications. The preferred flange material for high power applications is generally CuW or CMC (Cu-Mo-Cu) because of good thermal conductivity [4].

1.2 Aim and Importance of the Study

High power transistors should be packaged in order to keep junction temperature low and steady and improve heat sinking capability [4]. Furthermore, thermal consideration prevents performance degradation of transistor and provides high reliability and durability. High power transistor packages require thermal interface materials, heat spreaders and bonding materials. The source of the bare die transistor is directly attached to the ground with back-vias, in order to provide low thermal resistivity [1].

Moreover, high power transistors should be packaged to protect bare die transistor from environmental conditions, make circuit fabrication easier and provide mechanical strength in PCB applications.

Contrary to all these functional advantages of transistor packages, package parasitic degrade the performance of bare die transistors [1]. Because of parasitic of package, operating frequency of transistor decreases. Also, gain and output power degradation are observed. Therefore, dimension and materials of packages should be determined to decrease parasitic effects as much as possible. However, there are some difficulties. High power bare die transistor size is the first factor to determine package size, because the bond wire shape should be identical all around the die to provide equal current distribution. The other and the most important limiting factor is the manufacturing capabilities. Distance between bond wires, dimension of bond wire, material mismatches and cost, should be considered during the package design. In this work, specifications of all components of the package are determined to decrease parasitic effects without disturbing manufacturing tolerances.

One of the most critical point in this work is the accurate modeling of the package. Since the parasitic degrade the performance of transistor, it should be determined accurately to estimate the performance of packaged transistor correctly. In order to validate a PA design, packaged transistor model should be accurate to obtain a good agreement between simulation and test results. Because it is not straightforward to measure the response of a package, a modeling approach should be utilized to obtain the behavior of the package. In addition, because response of package is not provided by any manufacturer, the only way is modeling of the package.

Furthermore, because procurement of high-power packaged transistor is not easy, there is a need to model and manufacture package and embed the die transistor in it to use in high PA design.

In this work, two different approaches are presented. The first one is the lumped element model which replaces the package parts such as bond wires, gate and drain leads by their lumped element representations, whose values are obtained by

analytical equations. The importance of suggested lumped element model of the package is that there is no need to use a 3-D EM simulation tool. Also, it is possible to create model easier, quicker and cheaper than the simulation tools. The second approach is the 3-D EM model of the package which is created by using ADS EM simulation software.

The last critical part of this work is the design of a broadband high PA, by using the package model with the nonlinear bare die transistor model. The designed PA is manufactured, tested and results are compared with simulations. Suggested lumped element and EM models of the package are verified.

The main contributions of this work can be summarized as below;

- Two modeling methodologies are developed for accurate model of power transistor package.
- The first in-house power transistor package is manufactured, by utilizing the developed modeling methodologies.
- The manufactured package is used in the design of a 0.5-3 GHz broadband 50 W high PA.
- The designed power amplifier is manufactured and tested.
- The validity of the lumped element and full-wave EM package models are verified by comparing simulations and measurement results.
- As a future work, a package model is suggested. This model is designed to eliminate package parasitic and increase operation frequency of PA design.

1.3 Brief Review on Literature

For package modeling, almost always, full-wave EM simulation methodologies are used [5]. Although the most reliable way to obtain response of the package is 3-D EM simulation, it is a complex and long-time process. Also, high computing power and memory are needed. Furthermore, there is a need of EM simulation software which is expensive. To provide numerical robustness and increase convergence speed, a distributed model is provided [6]. By using S-parameter matrix which is

obtained by using EM simulation software, lumped element values are estimated at 2 GHz [6]. However, the accuracy of this extraction method is not enough to estimate the resonant frequency of package at high frequencies. Thus, the lumped element model methodology is suggested in this work, which is based on generation of the equivalent circuit and calculation of lumped element values of each part of the package analytically. Suggested methodology is more accurate and eliminates the need of 3-D EM simulation software.

1.4 Outline and Description of the Thesis

This work comprises of three parts, modeling of the GaN power transistor package with two different approaches, design of a broadband high PA and suggestion of a packaging strategy for performance improvement.

In Chapter 2, package geometry and structure of packaged transistor are described and effects of package parasitic are mentioned. Generation of first modeling method which is lumped element model is described step by step. Analytical formulations of lumped element values of package are determined and completed model of package is obtained. As a second approach, 3-D EM model of the package which is obtained by using ADS is presented. 3-D EM simulation process is started by generating 3-D lay-out of package which comprises of creating bond wire profile, defining stack-up, assigning ports and simulation, respectively. Modeling strategy and simulation results are examined. As a last, 2 different modeling approaches are compared and discussed shortly. Nonlinear model of the transistor which is provided by the manufacturer and the package model in this work are combined. Packaged transistor model is obtained in order to be used in the PA design in Chapter 3. At the end of the chapter, thermal characterization of the packaged transistor is performed and a thermal model is created.

In Chapter 3, PA design fundamentals and design procedure are described step by step. In order to test the modeled and fabricated package performance, broadband, high PA is designed. All simulations are performed with the packaged transistor

models of Chapter 2. Broadband high PA with embedded produced packaged transistor is measured and simulation results are compared at the end of the chapter.

In chapter 4, a new package is suggested as future work. First, electrical model of package is created by using simulation software. Then, thermal model of package is created. At the end of the chapter, contributions of the suggested package are described and compared with air cavity ceramic package.

CHAPTER 2

AIR CAVITY CERAMIC PACKAGE MODELING

2.1 Geometry and Structure of Packaged Transistor

High power transistors are generally placed in air cavity ceramic package [1]. An air cavity ceramic package includes a metal flange, a dielectric window frame, gate and drain leads and a lid as seen in Figure 2.1.

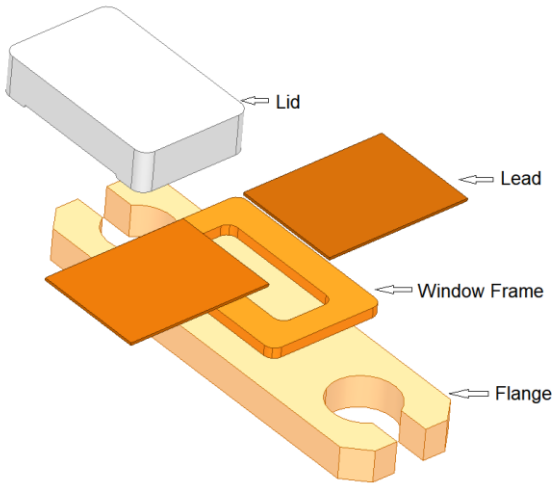


Figure 2.1: Package Structure

Metal flange material is chosen as S-CMC (Cu:Mo:Cu:Mo:Cu) because of good thermal specifications [1]. This material provides low thermal resistance and good CTE match with the active device. Standard metal flange dimension is preferred in order to decrease manufacturing cost. For mounting purpose, there are two holes in the flange, which behaves as a heat sink for the power transistor. A dielectric window frame is mounted on the flange which is chosen as Al_2O_3, because of high temperature stability and low CTE specifications [4]. Leads are mounted onto the

dielectric window frame which provides connection between gate and drain pads of the die and the PCB through bond wires, as seen in Figure 2.2 [1]. Material of leads are chosen as kovar, because of good CTE match with Al_2O_3 [4]. The bare die transistor is attached to the flange by using eutectic soldering. There are three gold 1-mil-diameter bond wires connected at each gate and drain pad of the bare die transistor. The distance between the bond wires is kept constant while considering manufacturing limits. The lid which is manufactured with epoxy on it is glued on the top of the package.

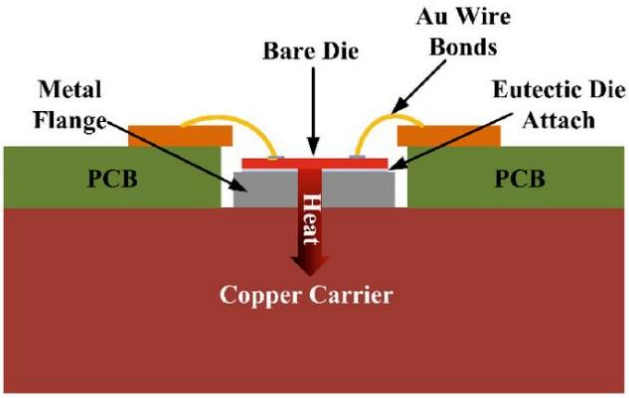


Figure 2.2: PCB Connection of Packaged Transistor Die [1]

Source of the bare die transistor is directly connected to the flange with back vias, in order to provide good mechanical contact with low thermal resistivity. To reduce the thermal resistance and provide strong physical contact between flange and heat sink carrier, generally, a gap filler material is inserted between them [1].

2.1.1 Transistor

In this work, GaN HEMT bare die transistor is chosen as an active device. GaN technology has prominent properties which are large bandgap, high breakdown voltage, high electron velocity and high thermal conductivity [7]. Thanks to high breakdown voltage capability, high drain voltage can be applied to the drain of the transistor and higher output power level can be obtained. Because of high electron

velocity feature, high frequencies can be reached. By means of high thermal conductivity, high temperature can be tolerated [7].

Bare die transistor consists of power unit cells which include gate, drain and source pads as seen in Figure 2.3 [8]. Source pads are grounded with back vias, thus transistor is used as common source transistor model. Gate DC biasing and RF feeding is done through gate pads. Drain DC biasing circuitry and RF output matching network are connected to drain pads as seen in Figure 2.4.

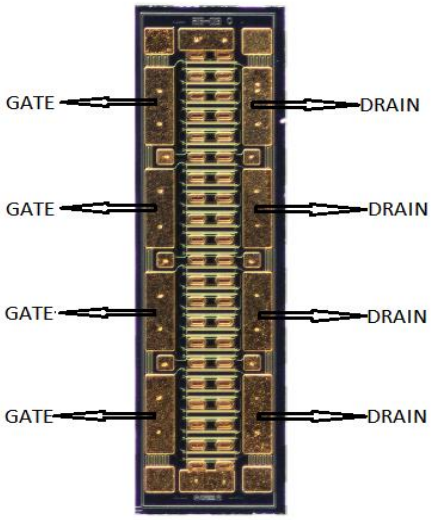


Figure 2.3: GaN on SiC HEMT Bare Die [8]

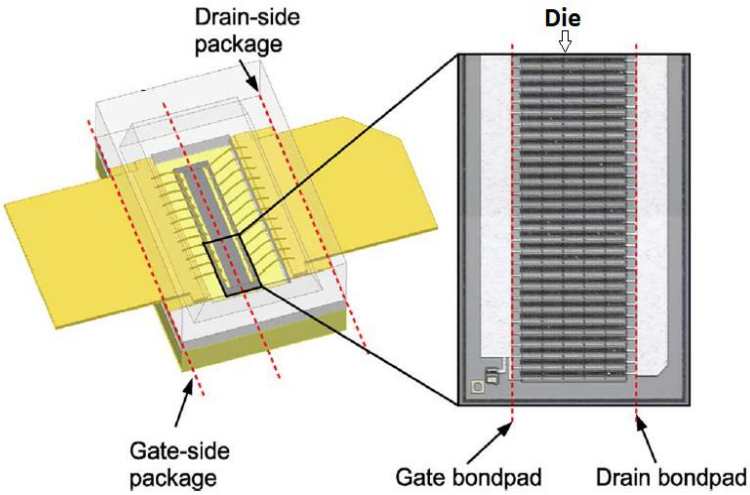


Figure 2.4: Illustration of Packaged Transistor [9]

The basic GaN HEMT structure which includes gate, source and drain electrodes is shown in Figure 2.5 [10].

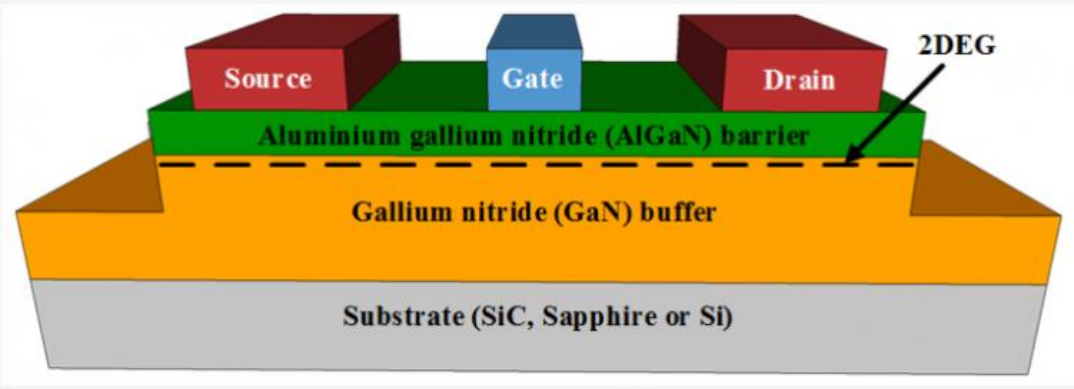


Figure 2.5: GaN HEMT Structure [10]

2.1.2 Package Parasitic

Power transistor package has important functions such as protecting bare die transistor from environmental conditions, making circuit fabrication easier, improving heat sinking capability and providing mechanical strength [11]. Besides all these functionalities, package affects the electrical performance of transistor [11].

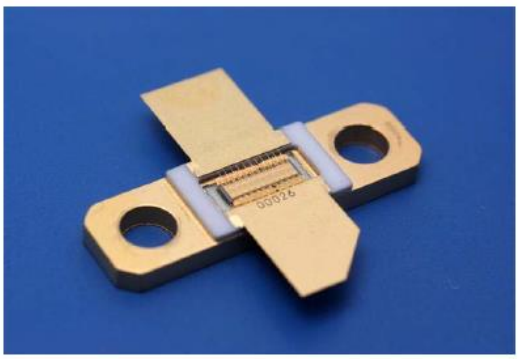


Figure 2.6: Packaged GaN HEMT Transistor without Lid [11]

Packaged transistor has generally degraded performance with respect to bare die transistor as shown in Figure 2.7 which illustrates large signal performance of both chip on wafer and chip in case. Same degradation is valid for small signal performance of the transistor as shown in Figure 2.8 [12]. At high frequencies, small signal gain degradation is obvious. Because of package resonance, usable frequency range reduces [12].

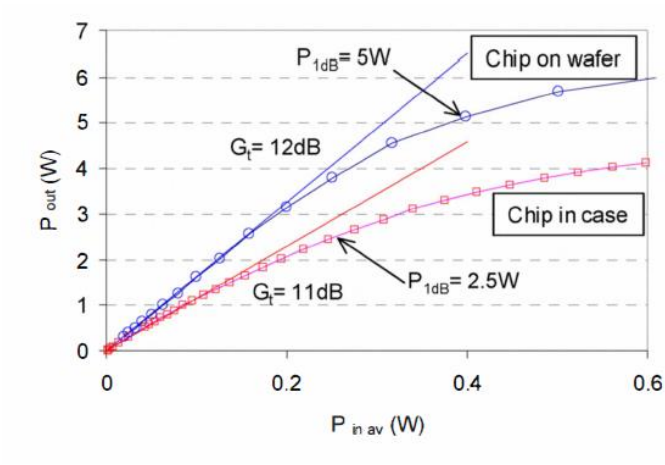


Figure 2.7: Comparison of Output Power Characteristics of Bare Die Transistor and Packaged Transistor [12]

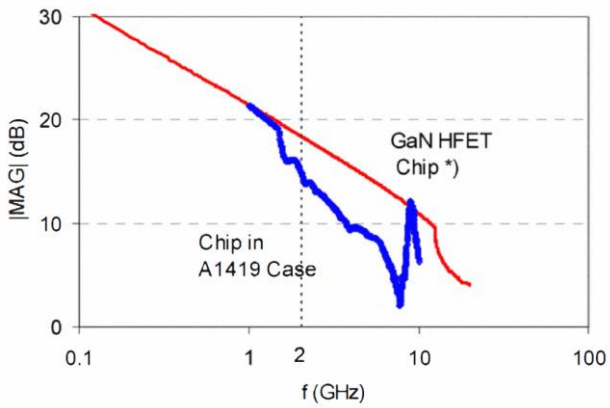


Figure 2.8: Comparison of Small Signal Gain Graph of Bare Die Transistor and Packaged Transistor [12]

Package effects are mainly due to bond wire inductances, mutual coupling between bond wires, lead capacitances and coupling between the input and the output of the package [12]. The inductance and capacitance provided by the package result in resonances, which are critical for high frequency applications [12]. Resonance occurs due to large physical dimensions of the package. For wideband transistors, resonance is critical [12]. At the input of the transistor, lead capacitance and inductance of bond wires create a resonance. The simple equivalent circuit of input of the packaged device is depicted in Figure 2.9 [12]. These effects should be carefully modeled in order to predict electrical performance of the packaged transistor accurately [6].

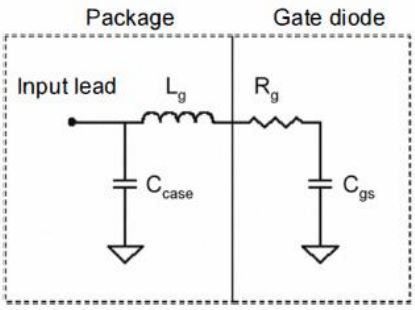


Figure 2.9: Equivalent Circuit of Input of the Packaged Transistor [12]

In this work, two different modeling approaches are discussed and compared. The first approach is the equivalent lumped element model based on analytical calculations of package parasitic. The second approach is based on 3-D EM simulation model.

2.2 Lumped Element Model of Package

Lumped element model is the simplest way to predict the impact of package on electrical behaviour of the die transistor [5]. Bond wire inductances, mutual coupling between parallel bond wires and lead capacitances can be calculated analytically. Lumped element models can be used to increase simulation speed and increase numerical convergence even at higher frequencies with some extentions [5]. Even though, calculating the coupling between gate and drain side bond wires is not

possible with lumped element modeling method, it can be ignored in this work because of low operating frequency range.

The development of the analytical model consists of multiple steps. First, a single bond wire is modeled. Then, the mutual inductances between the neighboring bond wires are included. Finally, the leads are modeled and lumped element values are calculated. The final analytical model is compared with 3-D EM simulation model.

2.2.1 Single Bond Wire Model

Bond wires are represented as a self inductance and series resistance as shown in Figure 2.10 [13]. Capacitance of the landing pad of the bond wire should be added to the model.

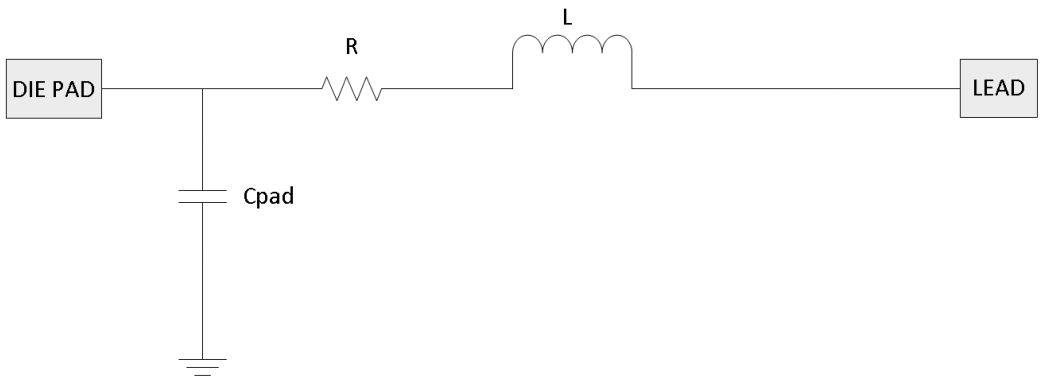


Figure 2.10: Bond wire Equivalent Lumped Element Model

For a bond wire with length l and radius r parallel to a ground plane, self inductance calculation can be written as Equation (2.1) where h is the distance between ground plane and the conductor [13] .

$$L = \frac{\mu_0 \mu_r}{2\pi} \ln\left(\frac{2h}{r}\right) l \tag{2.1}$$

The relative permeability μ_r can be taken as 1 for a nonmagnetic substrate and μ_0 is the permeability in a vacuum ($4\pi \times 10^{-7}$ H/m).

The inductance of bond wire depends on its profile, which is shaped by dividing it in 5 smaller pieces to obtain producible and real-like bond wire as shown in Figure 2.11. Contributions of all parts of the bond wire can be calculated separately and summed to obtain the total inductance. The inductances of all 5 pieces of the bond wire profile can be calculated by using Equation (2.2), where α is angle between ground plane and piece of bond wire as seen in Figure 2.11 .

$$L_i = \frac{\mu_0}{2\pi} \int_0^{l_i \sec(\alpha_i)} \ln\left[\frac{2(l\, sin(\alpha_i) + h_i)}{r}\right] dl \qquad where\ i = 1,2,3,4,5 \tag{2.2}$$

Calculated inductance values by using Equation (2.2) are given in Table 2.1, together with the associated geometrical parameters.

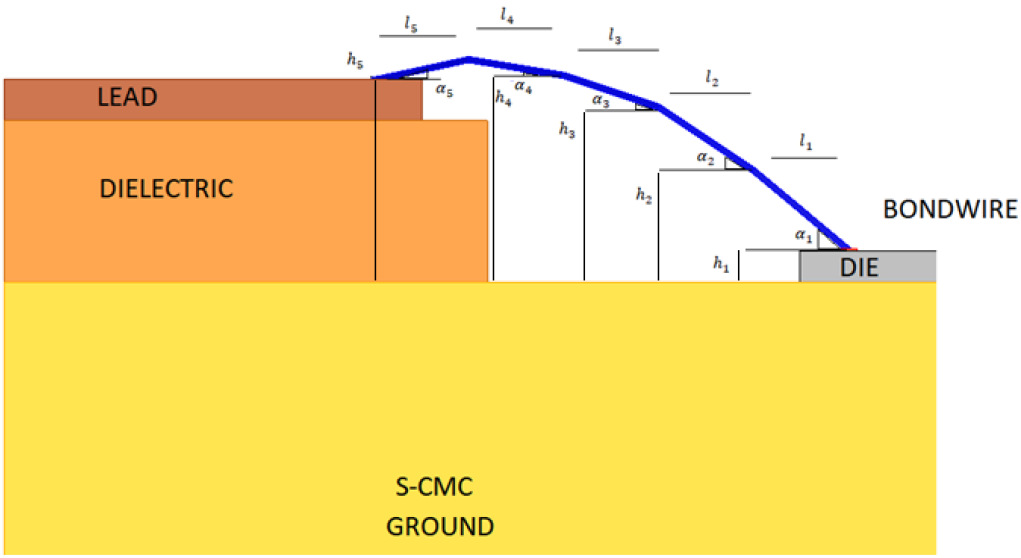


Figure 2.11: Bond Wire Profile

Table 2.1: Geometrical Parameters for Bond Wire Profile

Height	(µm)	Length	(µm)	Angle	(°)	Inductance	(nH)
h_1	100	l_1	300	α_1	39.80	L_1	0.275
h_2	350	l_2	300	α_2	33.69	L_2	0.307
h_3	550	l_3	300	α_3	18.43	L_3	0.288
h_4	650	l_4	300	α_4	9.46	L_4	0.284
h_5	640	l_5	300	α_5	12.24	L_5	0.287

Although the length of the bond wire is short, skin effect at high frequencies increases resistance which can not be ignored. DC series resistance of bond wire can be calculated by using Equation (2.3) [14], where l is the total length, r is the radius of bond wire, σ is the conductivity of the material and t is the thickness of the ground. Because skin effect decreases the conductivity of bond wire by limiting current to the outer conductor surface, resistance calculation should include skin effect. AC resistance of a cylindrical conductor where δ is skin depth is given in Equation (2.4) [14].

$$R_{dc} = \frac{l}{\pi\sigma r^2 t}(\pi r^2 + t) \tag{2.3}$$

$$R_{ac} = -\frac{l}{\pi\delta\sigma(\delta - 2r)}(2\pi r - \pi\delta + 2) \text{ for } \delta < t \; and \; \delta < r \tag{2.4}$$

Total length of the bond wire l can be calculated as given in Equation (2.5) .

$$l = \frac{l_1}{\cos(\alpha_1)} + \frac{l_2}{\cos(\alpha_2)} + \frac{l_3}{\cos(\alpha_3)} + \frac{l_4}{\cos(\alpha_4)} + \frac{l_5}{\cos(\alpha_5)} \tag{2.5}$$

Skin depth formula is given in Equation (2.6) [14].

$$\delta = \sqrt{\frac{1}{\pi \sigma f \mu_r \mu_0}} \tag{2.6}$$

Table 2.2: Properties of Bond Wire

Conductivity of Gold (σ)	Radius of Bond wire (r)	Total Length of Bond wire (l)	Diameter of Bond wire (d)
$4.10\times10^{7}\left(\frac{S}{m}\right)$	12.5 (µm)	~1700 (µm)	25 (µm)

For the bond wire properties given in Table 2.2, skin depth and frequency dependent resistance (R_{ac}) values are given in Figure 2.12 and Figure 2.13.

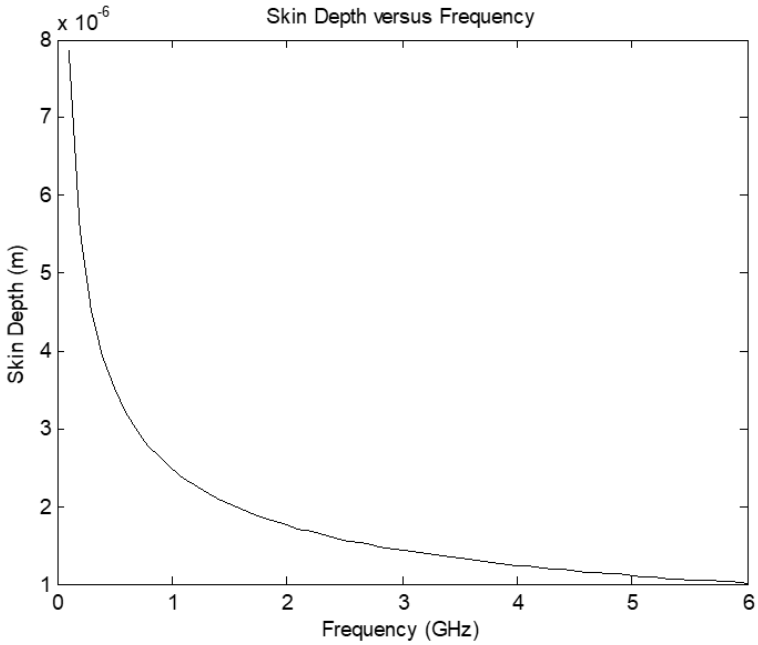


Figure 2.12: Skin Depth versus Frequency Graph of Bond Wire

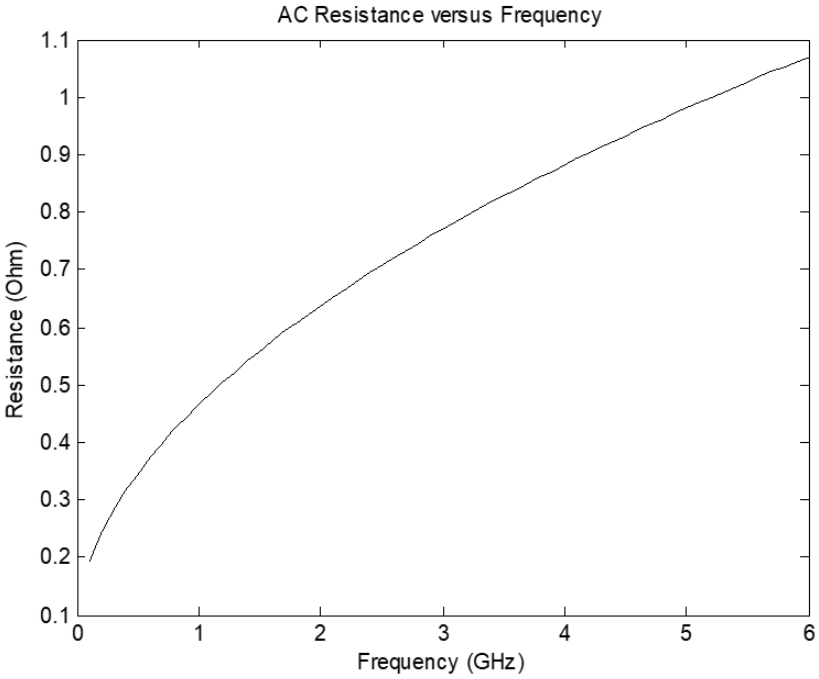


Figure 2.13: AC Resistance versus Frequency Graph of Bond Wire

Capacitance of the landing pad of the bond wire with the area A on chip can be calculated as given in Equation (2.7) and fringing effect can be ignored [15].

$$C_{pad} = \frac{\varepsilon_0 \varepsilon_r A}{h} \tag{2.7}$$

Capacitive effect on lead side can be neglected because of small area and high distance to ground plane.

Calculated lumped element values of a single bond wire are given in Table 2.3 below.

Table 2.3: Analytically Calculated Lumped Element Values of Single Bond Wire

Inductance (L)	Pad Capacitance (C_{pad})	Resistance (R)
1.44 nH	0.63 fF	R_{ac} =Frequency Dependent (Figure 2.13) $R_{dc} = 84.5\ m\Omega$

In order to decrease the bond wire inductance, the bond wire profile should be short as much as possible, allowed by manufacturing. Inductances of two different length bond wire profiles are compared in Figure 2.14 . Short one is 1700 µm which is used in this work whereas the long one is 2000 µm. Inductances of the short and long ones are calculated as 1.44 nH and 1.74 nH, respectively.

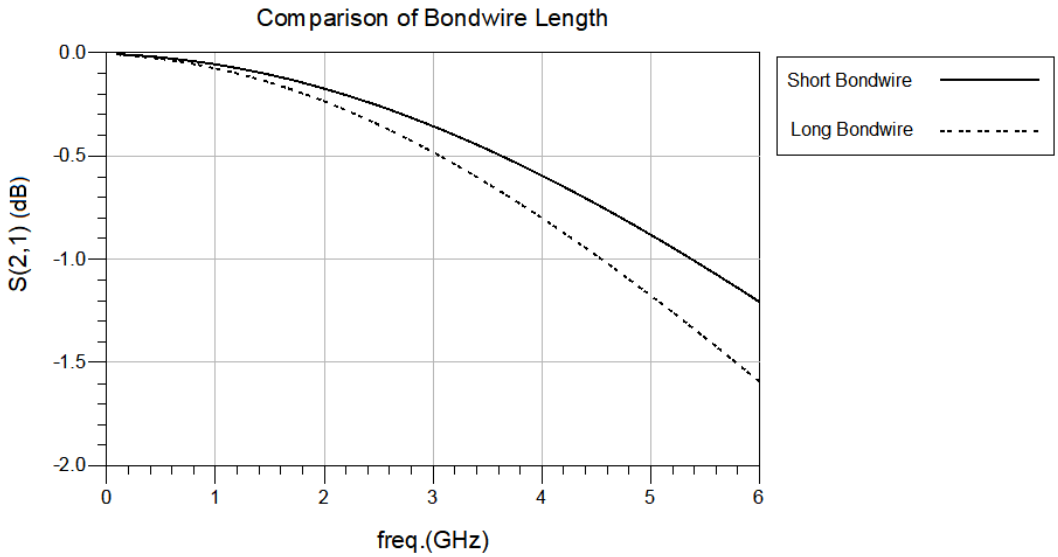


Figure 2.14: Comparison of Bond wire Length

Total inductance of bond wires can be decreased by increasing the number of bond wires which are connected parallel. However, this is not an ultimate solution to the resonance problem as there is not a linear relation between total inductance and the total number of parallel bond wires as seen in Figure 2.15 [15].

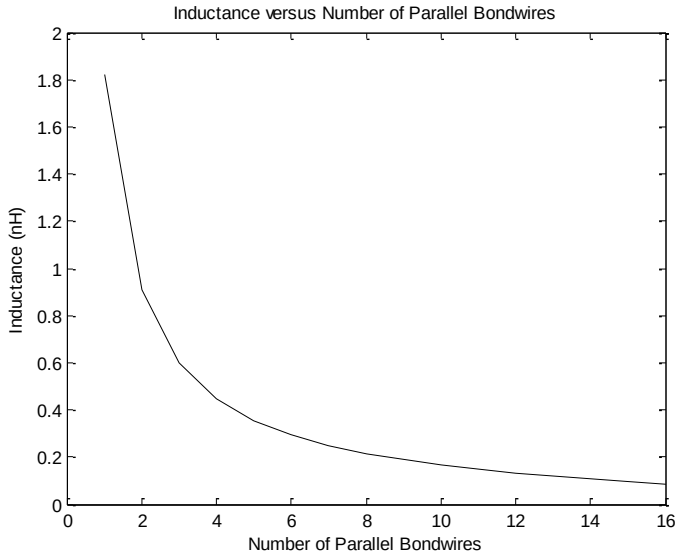


Figure 2.15: Inductance versus Number of Parallel Bond Wires

2.2.2 Mutual Inductance

3 parallel bond wires are connected parallel at each gate and drain pads with respect to manufacturing limits. 3 parallel bond wires equivalent model can be represented as Figure 2.16 below.

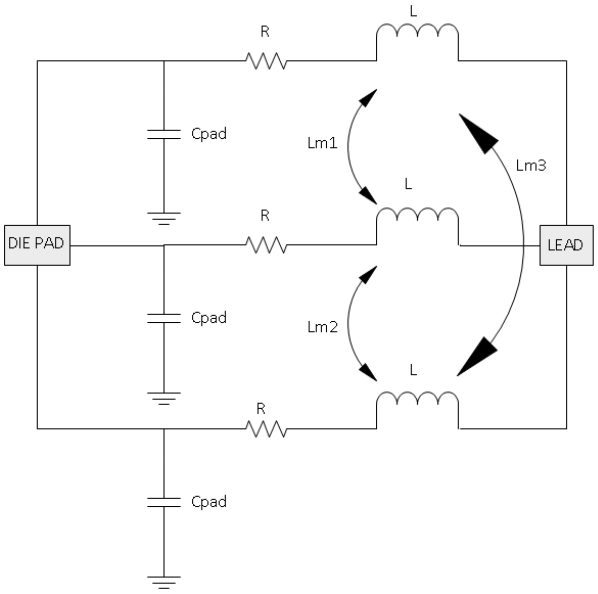


Figure 2.16: Lumped Element Model of 3 Parallel Bond Wires

Mutual inductance for bond wire pair parallel to ground can be defined as given in Equation (2.8) where d is distance between two bond wires and h is the distance between the ground plane and bond wires [15].

$$L_m = \frac{\mu_r \mu_0}{4\pi} \ln\left(1 + \left(\frac{2h}{d}\right)^2\right) l \tag{2.8}$$

Mutual inductance calculation of first piece of bond wire is given in Equation (2.9)

.

$$L_{im} = \frac{\mu_0}{4\pi} \int_0^{l_i \sec(\alpha_i)} \ln\left[1 + \left(\frac{2(l\, sin(\alpha_i) + h_i)}{d}\right)^2\right] dl \;\; where\; i = 1,2,3,4,5 \tag{2.9}$$

Total L_{m1} and L_{m2} are calculated as 0.663 nH and L_{m3} is calculated as 0.446 nH.

Comparison of 3-parallel bond wires with and without mutual inductances is shown in Figure 2.17. Clearly, the mutual inductance has a significant impact on the overall performance and should be included in the calculations to obtain an accurate model.

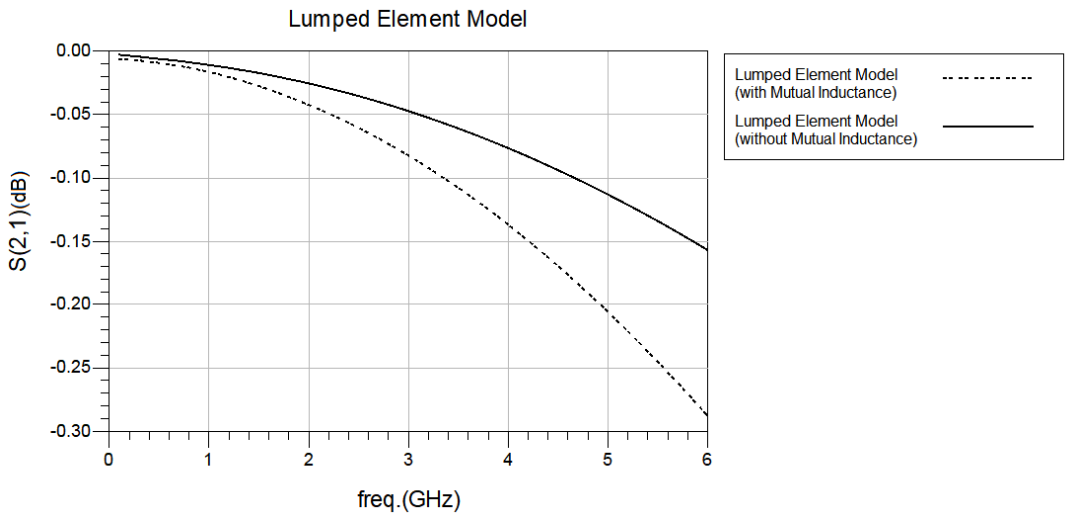


Figure 2.17: 3 Parallel Bond Wires with and without Mutual Inductance Model

Because there are 4 gate pads on the gate side and each gate pad includes 3 bond wires, mutual inductance between neighbor bond wires should be calculated and added to the model for a better model accuracy. Hence, 66 mutual inductance values are calculated and added to the model.

2.2.3 Lead Model

Gate and drain leads provide connection between PCB and the bare die transistor through bond wires. Capacitance of the package is formed by the lead metals. By decreasing value of lead metal capacitance, resonant frequency can be increased. Reduction of lead capacitance and bond wire inductance creates the same impact in shifting resonant frequency. However, lead metal width should be as large as possible in order to connect parallel bond wires throughout bare die transistor gate and drain pads, without disturbing shapes of them. Similarly shaped bond wires provide same current and power distribution between them which is critical for transistor performance. Also, it should be as narrow as possible to prevent lower resonant frequency of package. In this work, lead metal width is chosen in order to fit in all equally shaped bond wires and prevent decreasing resonant frequency without disturbing manufacturing limits and increasing cost.

Lead can be expressed as microstrip capacitance, inductance and resistance as shown in Figure 2.18.

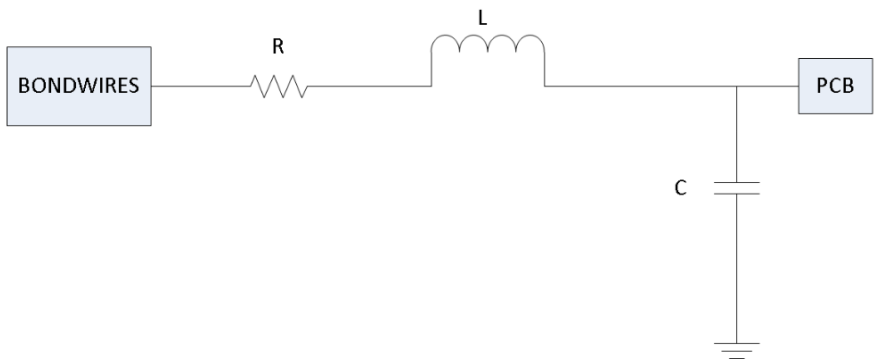


Figure 2.18: Lead Equivalent Model

Capacitance and inductance calculations are given in Equations (2.10) and (2.11) where w is width of lead, h is distance between ground plane and lead, l is length of lead and c is speed of light in a vacuum [14].

$$C_{lead} = \frac{\varepsilon_r l \left[\frac{w}{h} + 1.393 + 0.667 \ln\left(\frac{w}{h} + 1.444\right)\right]}{120\pi c} \text{for } \frac{w}{h} > 1 \tag{2.10}$$

$$L_{lead} = \frac{120\pi l}{c\left[\frac{w}{h} + 1.393 + 0.667 \ln\left(\frac{w}{h} + 1.444\right)\right]} \text{for } \frac{w}{h} > 1 \tag{2.11}$$

DC resistance of microstrip conductor is calculated as in Equation (2.12) where t is thickness of lead and g is thickness of the ground plane [14].

$$R_{dc} = \frac{l}{\sigma w t} + \frac{l}{\sigma g} \tag{2.12}$$

AC resistance of microstrip conductor is calculated as in Equation (2.13) where $2\delta < w$, $2\delta < t$ and $\delta < g$ [14].

$$R_{ac} = \frac{l}{\delta \sigma_0 \sigma_r (2t - 4\delta + 2w)} + \frac{l}{\sigma_0 \sigma_r \delta} \tag{2.13}$$

By using Equation (2.10)-(2.13), lead capacitance, inductance and resistances are calculated as in Table 2.4. Skin depth and frequency dependent resistance (R_{ac}) values are given in Figure 2.19 and Figure 2.20, respectively.

Table 2.4: Analytically Calculated Lumped Element Values of Single Bond Wire

Inductance (L_{lead})	Capacitance (C_{lead})	Resistance (R)
0.116 nH	1.5 pF	R_{ac} = Figure 2.20 $R_{dc} = 1.1\ m\Omega$

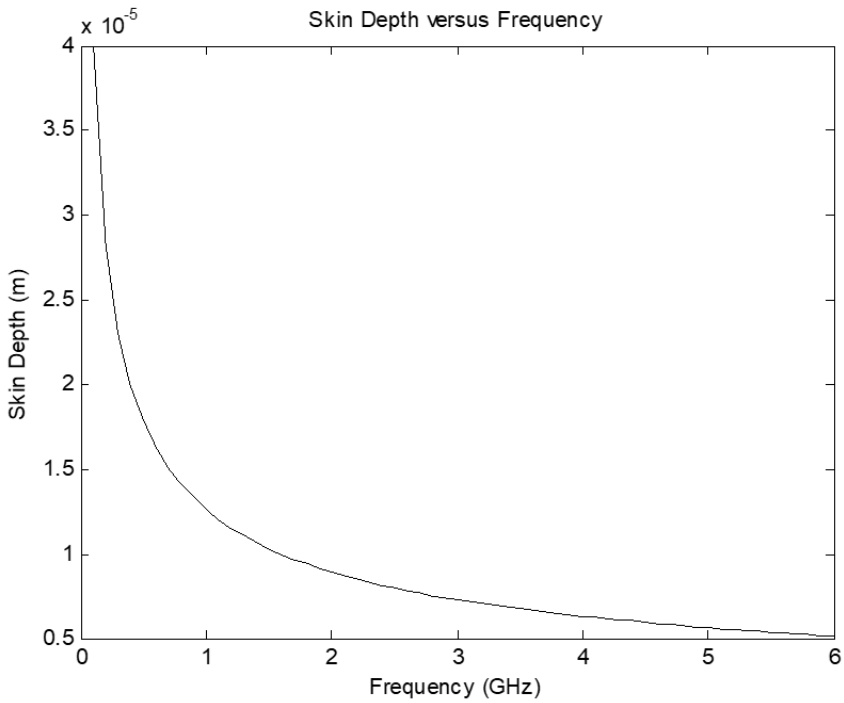


Figure 2.19: Skin depth versus Frequency Graph of Lead

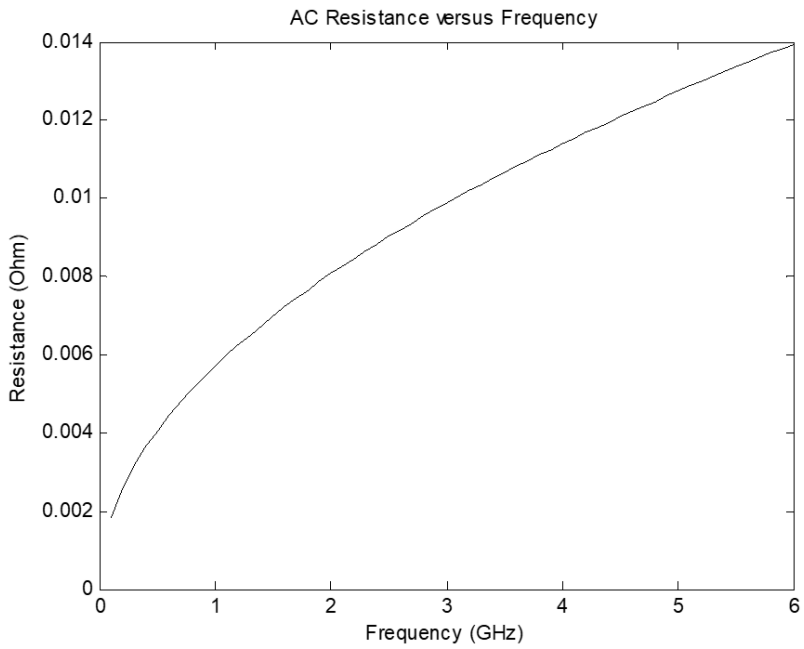


Figure 2.20: AC Resistance versus Frequency Graph of Lead

2.2.4 Complete Model

By combining the calculated lumped element model of bond wires including mutual inductances and lead capacitances, gate and drain side of the package can be modeled as given in Figure 2.21.

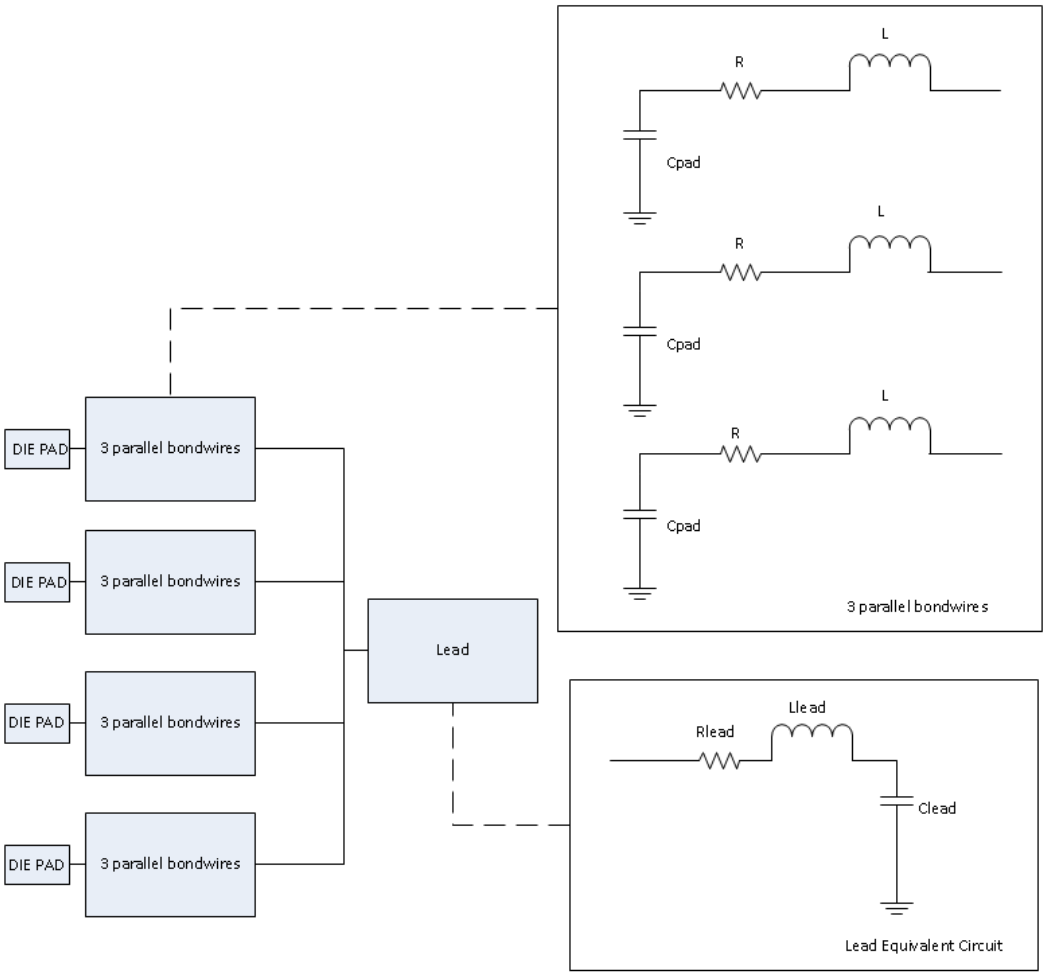


Figure 2.21: Completed Lumped Element Model of Gate or Drain Side of Package

2.3 3-D Simulation Model of Package

Final model of the packaged transistor consists of two main parts which are the nonlinear model of the bare die transistor and model of package. The package model cannot be determined by measurement because it is not possible to probe where the bond wires mounted on the chip [5]. Finite Element Method (FEM) is one of the commonly used technique to analyze and characterize geometrically complex 3-D structures such as bond wires and dielectric substrates [5]. 3-D EM simulations are performed by using ADS software in this work.

2.3.1 Modeling Strategy

2.3.1.1 Material Property Modeling Methodology

2.3.1.1.1 Dielectric Loss Models

Dielectric model is extremely important for the overall accuracy of the simulations. The permittivity is a complex number, whose real part (ε') determines the propagation speed within the dielectric and the imaginary part (ε'') represents the dielectric losses given in Equation (2.14) [16]. A commonly used term to indicate the dielectric losses is the loss tangent, which is also called as the dissipation factor ($\tan\theta$) given in Equation (2.15) [16].

$$\varepsilon = \varepsilon' - j(\varepsilon'') \tag{2.14}$$

$$\tan\theta = \frac{\varepsilon''}{\varepsilon'} \tag{2.15}$$

The real and imaginary parts of the complex permittivity are related to each other via Kramers-Kronig relations and this should be properly modeled, particularly for broadband simulations. Otherwise, obtained S-parameters may violate causality. In this study, Svensson/Djordjevic model has been adopted, which satisfies the causality requirement [17]. Frequency dependent permittivity formula of Svensson/Djordjevic Model which is used by ADS is given in Equation (2.16) [17].

$$\varepsilon(\mathrm{f}) = \varepsilon_\infty + a.\ln\left(\frac{f_H + jf}{f_L + jf}\right) \tag{2.16}$$

f_H and f_L are low and high frequencies for $\tan\theta$ calculation respectively. ε_∞ is permittivity value for infinite frequency and a is a constant factor [17].

Although, Svensson/Djordjevic Model is used as the main dielectric loss modeling approach, frequency independent permittivity model gives very similar results in the

frequency domain chosen, because loss tangent ($\tan\theta$) values of the dielectric materials of the package are very low. Difference between permittivity values at low and high frequency of operation of transistor is lower than 0.01%.

2.3.1.1.2 Impact of Temperature

ADS EM simulator has the capability to define temperature dependent properties of materials. Temperature dependent resistivity and conductivity can be defined for conductors, through Equations (2.17) and (2.18) [17] where T_{nom} is the nominal temperature, T_{C1} is linear temperature coefficient and T_{C2} is quadratic temperature coefficient.

$$R(T) = R(T_{nom}) \times (1 + T_{\mathrm{C1}} \times (T - T_{nom}) + T_{\mathrm{C2}} \times (T - T_{nom})^2) \qquad (2.17)$$

$$Cond(T) = \frac{Cond(T_{nom})}{(1+T_{\mathrm{C1}}\times(T-T_{nom})+T_{\mathrm{C2}}\times(T-T_{nom})^2)} \qquad (2.18)$$

The simulation temperature (T) is defined in the EM simulator setup. Because linear temperature coefficient value of lead and bond wire materials are low and temperature difference between T (approximately 55.5°C as shown in Figure 2.35) and T_{nom} (25°C) is small, a significant temperature dependence was not observed in the simulations.

2.3.1.1.3 Impact of Surface Roughness

Conductors on dielectrics do not have perfectly smooth surface [17]. Copper surface roughness increases conductor loss and slows the phase velocity of signals. Losses due to copper surface roughness depends on frequency and increases with increasing frequency. Loss becomes significant when skin depth is comparable or lower than surface roughness. Typical surface roughness values are in the range of 0.5-6 µm.

Skin depth of copper at 1 GHz is around 2 µm. Thus, surface roughness is significant for multi-gigahertz signal components [18].

Three models are available in ADS EM simulator which are the Hammerstead, the Hemispherical model and the Huray models. Roughness data which is provided by manufacturer is enough to calculate the surface roughness but for more accuracy, other parameters should be obtained by scanning electron microscope (SEM) [17]. The simulator determines the parameter values even if they are not described by using the roughness data. The Hammerstad model is not accurate at high frequencies. The hemispherical model is more accurate than the Hammerstad model, but it still losses accuracy at high frequencies. The Huray model provides good accuracy for frequencies over 50 GHz [17].

Since the operating frequencies of the transistor are quite low and surface roughness of conductor materials are quiet low with respect to skin depth, the impact of surface roughness on conductor loss is negligible.

2.3.1.2 3-D EM Modeling Methodology

Because only the passive part of the package is needed to be analyzed, active part which is the bare die transistor should be removed without affecting the electromagnetic behaviour [6]. Thus, bare die transistor is replaced by a GaN dielectric block. On the top of this dielectric block, metal areas are placed which represent the gate and drain pads of bare die transistor. Internal ports are placed at the end of bond wires on metals. For each bond wire, one internal port is defined. Because die transistor is removed and there is no connection between gate and drain pads on GaN dielectric block, there is no transmission between external ports. Thus, resonant frequency of package can be obtained by performing small signal analysis.

External ports are placed at the edge of the gate and drain leads of the package. As a result of full-wave EM simulation, a multi-port S-parameter matrix is obtained. By inserting the nonlinear model of the bare die transistor to the internal ports on GaN dielectric block, model of packaged transistor is obtained.

2.3.2 Layout

Another integral part of the modeling process is the layout generation which is composed of defining the bond wire profile and stack-up.

2.3.2.1 Bond Wire Profile

EBOND shape component is a bond wire profile generation tool used in ADS. By using parameter window shown in Figure 2.22 below, all the values which determine the shape of a bond wire can be specified.

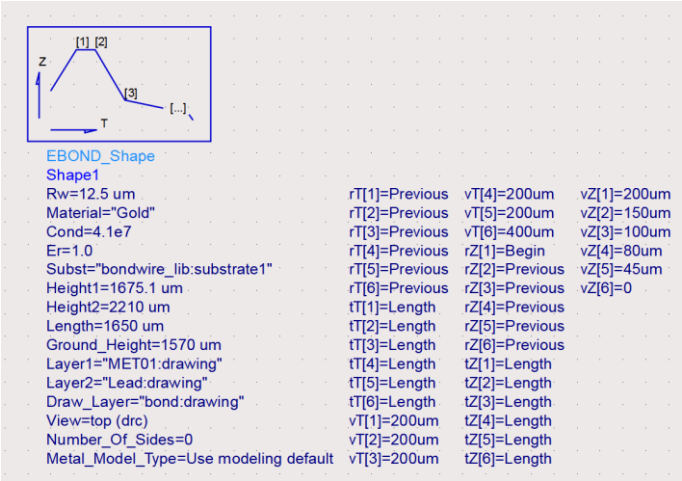


Figure 2.22: EBOND Shape Component

Standard EBOND shape parameters such as radius, material, height, length etc. can be defined within this window. Substrate is selected as initialization for the height settings for circuit simulation. Shape of the bond wire is created as seen in Figure 2.23 by introducing length and height of pieces.

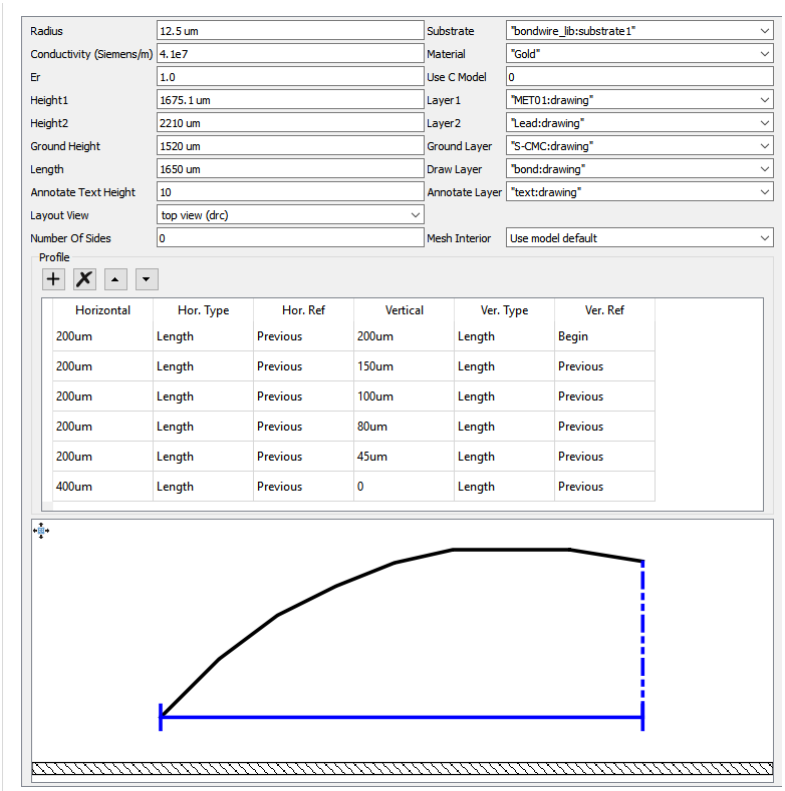
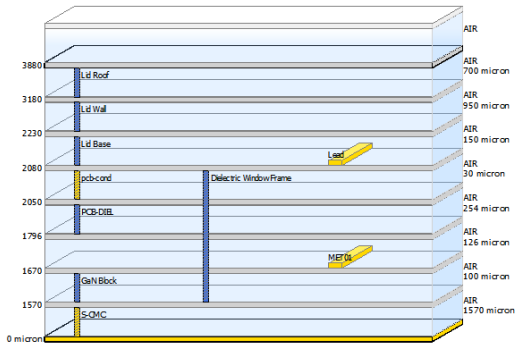


Figure 2.23: EBOND Shape Parameter Window

2.3.2.2 Defining Stack-up

A well defined stack-up is required in order to simulate a design. Stack-up definition consists of various layers of metal, dielectric material and ground planes. Also, position of layers of physical design in the substrate and specifications of material characteristics are included. Stack-up is created as a first step of 3-D EM simulation as seen in Figure 2.24.



Substrate Layer Stackup

	Type	Name	Material	Thickness
	Dielectric		AIR	
	Dielectric		AIR	700 um
	Dielectric		AIR	950 um
	Dielectric		AIR	150 um
4	Conductor Layer	Lead (52)	LEAD	130 um
	Dielectric		AIR	30 um
	Dielectric		AIR	254 um
	Dielectric		AIR	126 um
7	Conductor Layer	MET01 (51)	CHIP	5.1 um
	Dielectric		AIR	100 um
	Dielectric		AIR	1570 um
	Cover		PERFECT_CONDU...	0 mm

Figure 2.24: Stack-up of Package

2.3.2.3 Assigning Ports

3-D layout is created as shown in Figure 2.25. Ports are necessary in order to inject energy into circuit to analyze the circuit behavior [6].

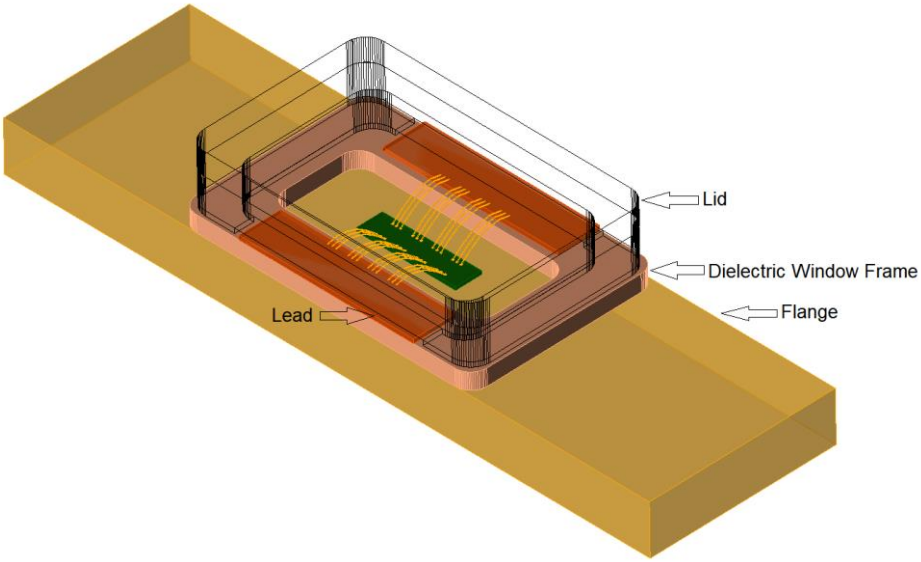


Figure 2.25: Lay-out of 3-D Package

Lay-out pins are used to define ports in ADS which are point pin, area pin and edge pin [19]. Point pin can be used inside a metal which defines cylinder port. Area pin is used inside a metal which defines cylinder port too. Edge pin can be used at the edge of a metal which defines sheet port or waveguide port as seen in Figure 2.26 [19].

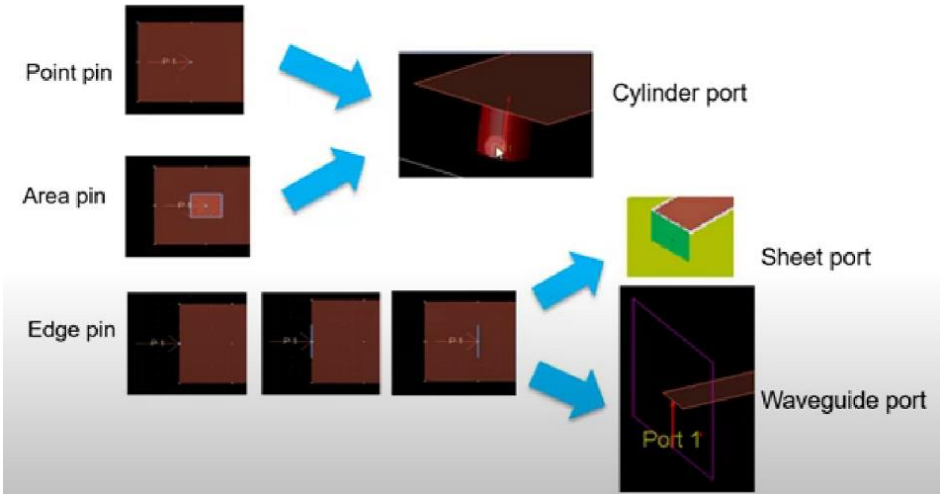


Figure 2.26: Pin and Port Relation for EM Simulations in ADS [19]

Edge pins are assigned at the edge of gate and drain leads. Feed type of external ports is chosen as TML which is defined as 'Waveguide Port' and can be applied to surface of bounding box. TML calibration assumes the structure is fed through a transmission line [19]. TML calibration removes the parasitic effects and fringe capacitance at the edge of the metal. Modal TML port solver is used to excite structure by using TML port. The modal S-parameters obtained may not be stable at low frequencies, although being more accurate at high frequencies [19]. Generalized S-parameters with reference impedance that is frequency dependent characteristic impedance for each modes can be described as modal S-parameters, which are useful to analyze transitions between microstrip lines with different impedances. External ports can be seen in Figure 2.27.

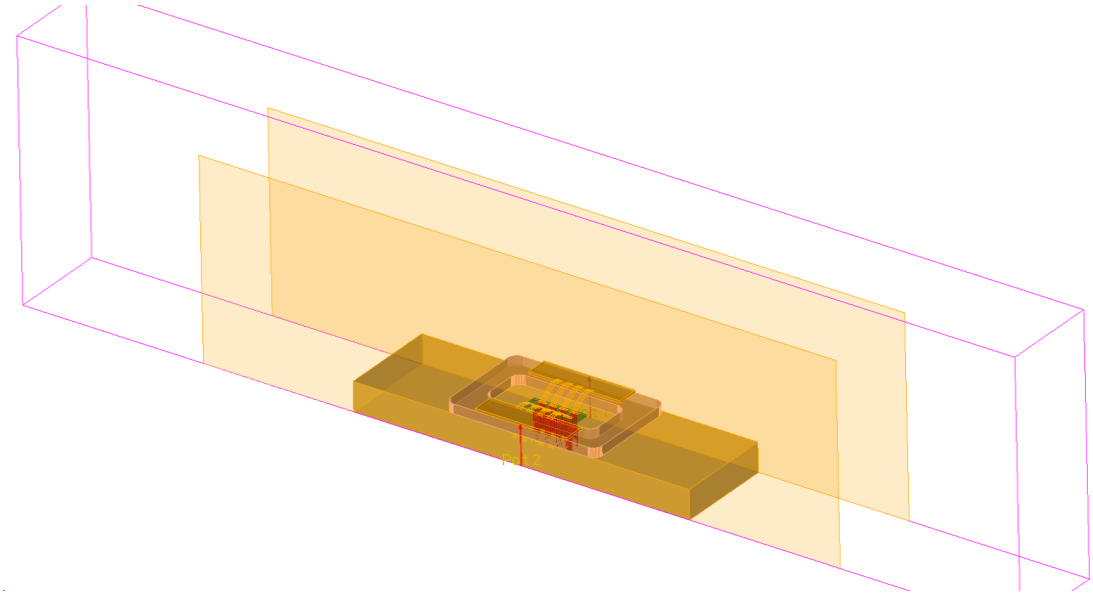


Figure 2.27: External Ports

Point pins are assigned at the end point of each bond wire which can be defined as 'Cylinder Port' which use cylindrical set of current filaments as shown in Figure 2.28. Direct port is used when circuit includes transmission lines that connect to a device such as a transistor. [19]. Because direct port is partially calibrated, it removes self and mutual inductance between ports.

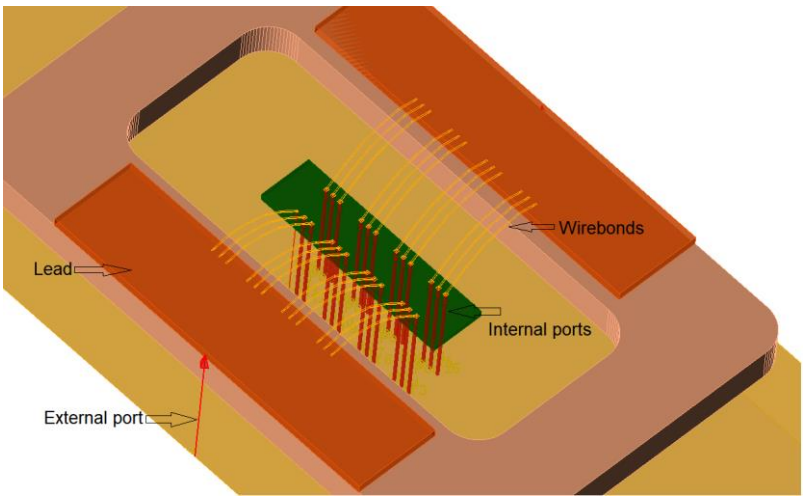


Figure 2.28: Internal Ports

To analyze the sturucture accurately, modal excitations, modal impedances and propagation should be solved correctly [20]. If port width is chosen too narrow, fields can couple to side walls and incorrect modal solution is obtained. Also, if port length is chosen too short, fields can couple to the top wall. Thus, size of waveguide port can be adjusted by using the guideline in Figure 2.29 [20]. If width of the microstrip trace, w, is more than the dielectric height, h, the width of the port should be chosen as 10 w. The height of the port can be chosen between 6 h and 10 h. In this work, the width of the port is chosen as 10 w and the height of the port is chosen as 8 h.

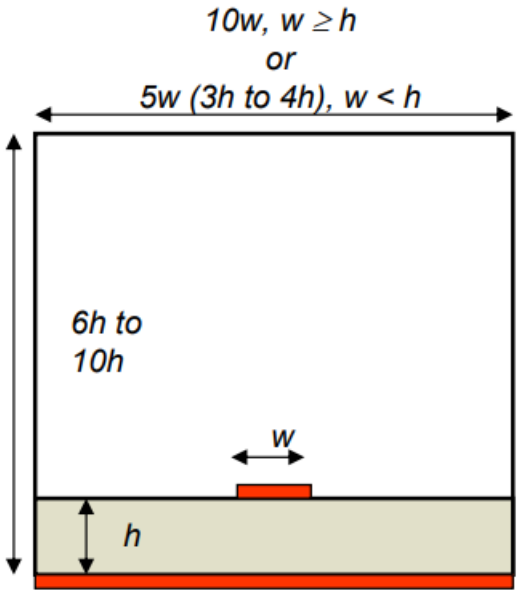


Figure 2.29: Waveguide Port Dimension Guideline [20]

Because FEM ports are physical models and physically meshed, they have self-inductance [21]. Also, there is mutual inductance between uncalibrated ports. Feed type determines calibration of ports. The FEM feed types used in ADS and which effect is calibrated out is described in Table 2.5 [21].

Table 2.5: Feed Type versus Calibration used in ADS [21]

Feed Type	Removes Self-Inductance	Removes Mutual Inductances
Auto, TML, TML (zero length), Direct	Yes	Yes
SMD	Yes	Not with other SMD or Delta Gap ports
Delta Gap	No	Not with other SMD or Delta Gap ports

2.3.3 Simulation

Finite element method (FEM) simulation technique is used in order to calculate 3-D EM field inside an arbitrarily shaped passive 3-D structure [19]. FEM divides the full space of problem into smaller regions which are called as tetrahedras and by using local function field in each tetrahedras is represented [19]. To increase accuracy of simulation results, FEM mesh settings should be made carefully. There is a trade-off between mesh size and computer memory and process time. To produce appropriate mesh structure, the iterative process is used. Mesh is refined in critical regions automatically in this process. It generates a solution and refines the mesh with respect to delta error and creates better solution until S-parameters converge to the desired limit. Also, maximum number of adaptive passes should be determined, which is the number of refinement passes reached before the delta error criterium is met and refinement process ends. Refinement frequency should be determined to specify the frequency where mesh will be generated. The refinement frequency is chosen as 12 GHz, because current distribution should be investigated at the highest simulation frequency to prevent missing spatial variations in reality [19]. After defining mesh settings, solver settings should be defined. Iterative process is chosen, because memory requirements and computing time is lower than the direct solver which guarantee convergence. However, by chosing maximum number of iterations sufficiently, convergence of solutions can be improved.

In this work, simulation frequency range for FEM simulation is set up to 12 GHz. Although operating frequency band of packaged transistor is DC to 4 GHz, to include 2nd and 3rd harmonic behaviour, simulation frequency bandwidth is chosen over wideband.

Resonant frequency of simulated package is around 6.39 GHz as seen in Figure 2.30 below. This means that above approximately 4 GHz, package decreases performance of transistor dramatically.

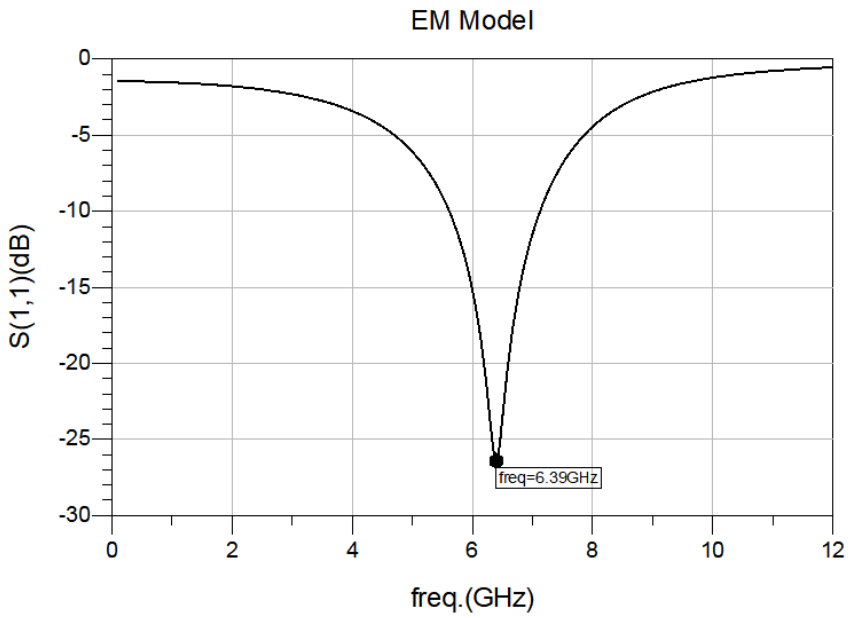


Figure 2.30: Resonance of the Input Circuit of Package in S_{11}

2.4 Comparison of Models

Comparison of calculated lumped element model of single bond wire and EM analysis of it are shown below in Figure 2.31. Thus, there is no significant difference between models of single bond wires.

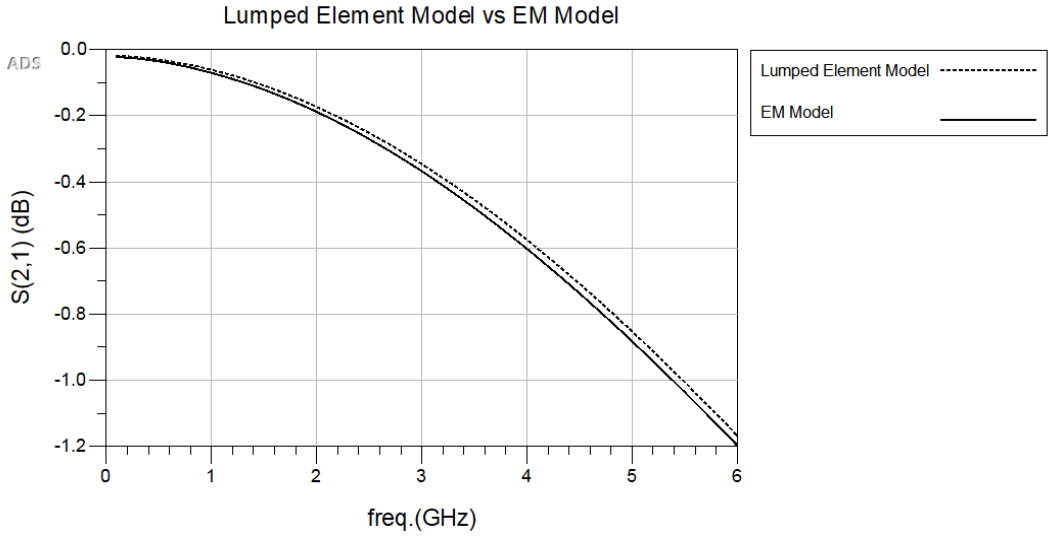


Figure 2.31: EM Model versus Lumped Element Model S_{21} Graph of Single Bond wire Model

Also, comparison of calculated lumped element model of 3 parallel bond wires and EM analysis of them is shown below in Figure 2.32. Thus, there is no significant difference between models of three parallel bond wires.

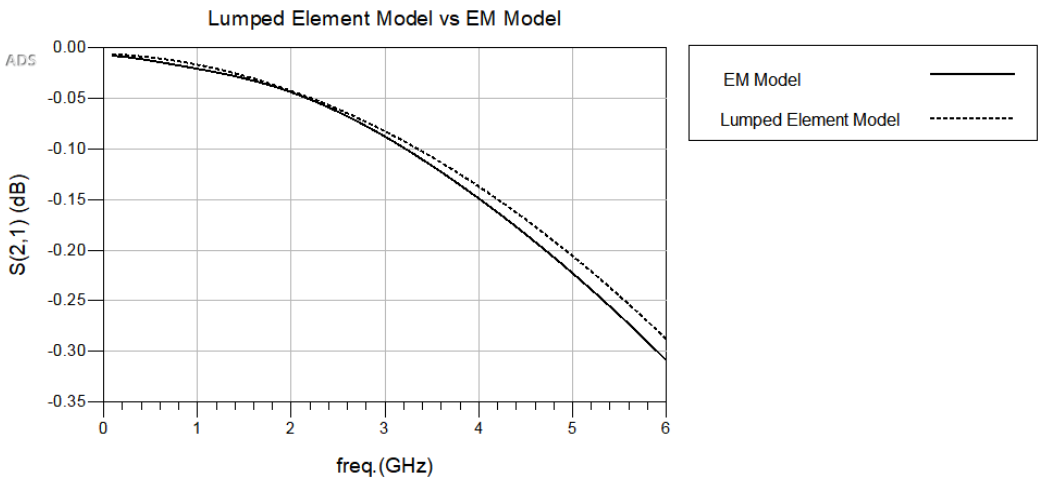


Figure 2.32: EM Model versus Lumped Element Model S_{21} Graph of Three Parallel Bond wire with Mutual Inductance Between Bond wires

Resonant frequencies of the EM and lumped element models of the package are around 6.39 GHz and 6.48 GHz, respectively as seen in Figure 2.33.

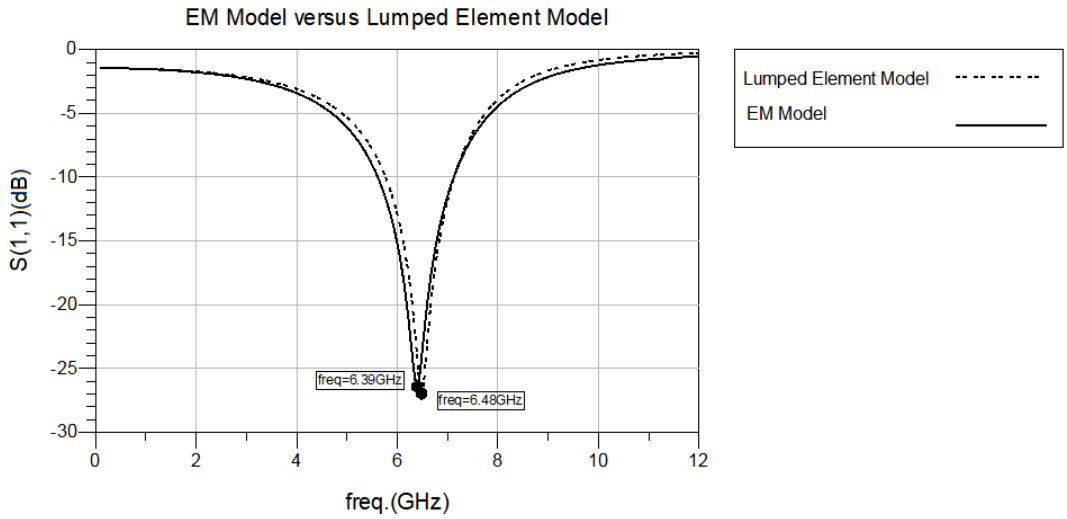


Figure 2.33: EM Model versus Completed Lumped Element Model of Package S_{11} Graph

This comparison shows that both EM model and lumped element model can be used accurately for this package. EM model is generally more accurate than lumped element model because geometrically complex structures can be characterized in electromagnetic environment and all effects can be added to the calculations with FEM analysis. The parasitic effect between gate and drain bond wires, coupling between the input and the output of the package or other effects between materials can not be predicted by using analytical calculations. If the frequency band of operation of transistor is higher, these parasitic effects get more important. In this work, the operating frequency of the transistor is quite low, thus lumped element model can predict accurate results.

The other important difference between the lumped element and the EM model is the need for sophisticated simulation software. If lumped element model is chosen, basic equations can be derived from the bond wire geometry and analytical

calculations are sufficient to create a model. On the other hand, to create an EM model, more complex and long time process is needed. Creating wirebond profile, defining substrate and assigning ports should be performed carefully to solve the problem accurately. Because the structure is complex, simulation takes long time as well.

2.5 Thermal Characterization of Air Cavity Ceramic Package

In addition to the electrical performance, thermal resistance of packages is another important design parameter. Thermal resistance is an ability of package to transfer the heat, which is generated by the transistor die, to the ambient. In order to obtain high performance air cavity ceramic package transistor, heat transfer should be through cold plate which is attached to the base of the package. Junction temperature refers to the temperature of chip transistor and case temperature refers to the temperature of the outside surface of the package which is at the center of the S-CMC block. In order to calculate the thermal resistance, Equation (2.19) [22] can be used where L is width (m), k is thermal conductivity $\left(\frac{W}{m.K}\right)$ and A is area (m^2) of the surface to which the heat will be transfered.

$$R = \frac{L}{kA} \tag{2.19}$$

In order to calculate temperature difference between cold plate and case, Equation (2.20) [22] can be used where Q is dissipated power (W), R is thermal resistivity $\left(\frac{°\mathrm{C}}{\mathrm{W}}\right)$ and ΔT is temperature difference (°C).

$$\Delta T = QR \tag{2.20}$$

2.5.1 Thermal Model Description

A die transistor is soldered to the top of the S-CMC block. S-CMC block is attached to the Al Module with screws. Module base temperature remains stable at 30 °C. Thermal model stack-up is prepared as seen in Figure 2.34. Thermal properties of materials and their dimensions are referred in Table 2.6.

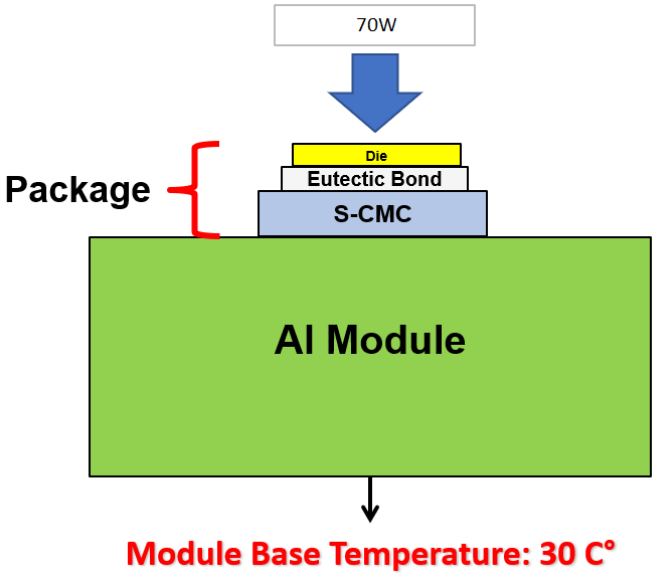


Figure 2.34: Air Cavity Ceramic Package Thermal Stack-Up

Table 2.6: Material Properties of Package

Layer	Material	Dimension (m^2)	Thickness (m)	Thermal Conductivity $\left(\frac{W}{m.K}\right)$
Al Module	Aluminum	1.04×10^{-3}	5.00×10^{-3}	180.00
S-CMC	Composite	8.58×10^{-5}	1.57×10^{-3}	301.80

2.5.2 Calculation and Simulation Comparison

In order to perform thermal analysis, large signal test result of the amplifier which is designed by using the air cavity ceramic package model is needed. Large signal test

result of designed PA is shown in Table A. Maximum dissipated power which is spread as heat to the ambient is 70 W.

Thermal resistances of layers which should be verified by simulation are calculated in Table 2.7.

Table 2.7: Thermal Resistance of Layers

Layer	Dimension (m^2)	Thickness (m)	Resistance $\left(\frac{°C}{W}\right)$	Temperature (°C)
Al Modul	1.04×10^{-3}	5.00×10^{-3}	2.67×10^{-2}	31.87
S-CMC	8.58×10^{-5}	1.57×10^{-3}	0.6×10^{-1}	36.07

To create thermal model of the air cavity ceramic package and simulate thermal characteristics of it, HFSS-ICEPACK program is used.

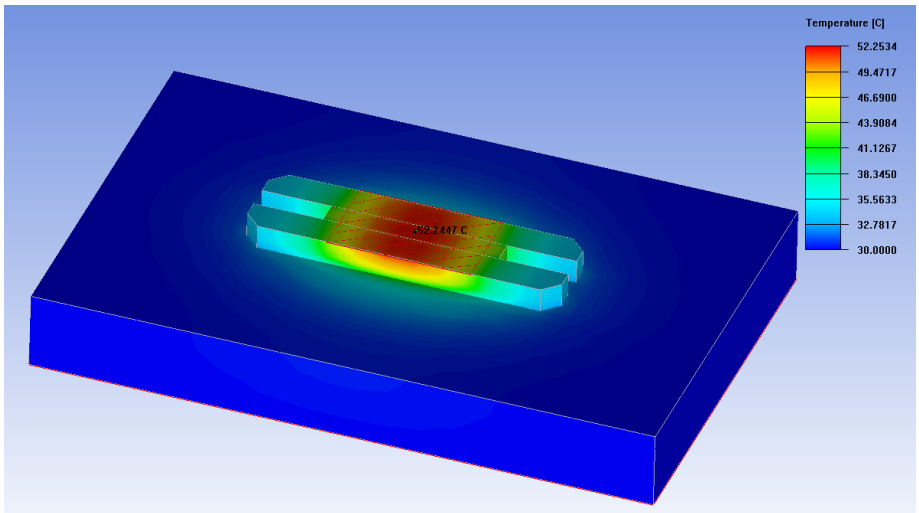


Figure 2.35: Simulation Result of Package

As seen in Figure 2.35, case temperature is calculated by the software as 52.25 °C which is not close to the calculated temperature of 36.07 °C as given in Table 2.7. Because the area of the die transistor is far smaller than the area of S-CMC flange, heat spread through the flange is nonuniform. Thus, it can be said that equations are

not accurate enough for the calculation of case temperature, because the effective area of materials, where heat is spread should be used in the equations instead of the physical area of the case. However, calculation of the effective area is not possible without simulations. Using the simulation results, the effective area of S-CMC is estimated as seen in Table 2.8 below to match the results of simulation and calculation. The estimated effective area of the case can be used to calculate the temperature of another packaged transistor with same die transistor and flange dimensions, without a need for a numerical simulation.

Table 2.8: Thermal Resistance of Layers

Layer	Dimension (m^2)	Thickness (m)	Resistance $\left(\frac{°C}{W}\right)$	Temperature (°C)
Al Modul	1.04×10^{-3}	5.00×10^{-3}	2.67×10^{-2}	31.87
S-CMC	1.72×10^{-5}	1.57×10^{-3}	3.02×10^{-1}	53.00

Die transistor can safely operate with a maximum junction temperature of 225°C. Junction to case thermal resistance for die only is 1.66 $\frac{°C}{W}$ [8]. Junction temperature of die transistor can be calculated with Equation (2.21) [22] where T_j is junction temperature, T_c is case temperature, R is junction to case thermal resistance of die and P_d is dissipated power of amplifier.

$$T_j = T_c + (R \times P_d) \tag{2.21}$$

$$T_j = 168.45\ °C$$

Junction temperature is calculated as ~170 °C, which is under maximum safety junction temperature 225°C.

CHAPTER 3

POWER AMPLIFIER DESIGN

3.1 Power Amplifier Fundamentals

Desired amplifier design has high linearity and high efficiency over wideband. However, all of these specifications are hard to be obtained in a single design. There is a trade-off between gain and bandwidth, frequency of operation and output power, linearity and efficiency. Most important characteristics that should be considered when designing an amplifier are bandwidth, gain, input and output reflection, output power and drain efficiency which are discussed in this chapter.

3.1.1 Bandwidth

In general, bandwidth of an amplifier is defined as the frequency range across which the circuit matches the requirements. Broadband amplifier design cannot be obtained easily because of limitations. High power GaN transistors require large periphery devices, hence lower real impedance and larger reactive input and output impedance levels are observed. Especially, large reactive part of impedance limits wide frequency band matching [2].

Equivalent circuits of the input and output impedances of a transistor are shown in Figure 3.1 [2].

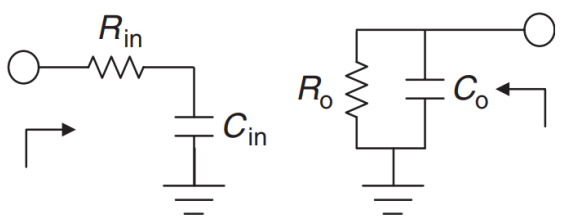


Figure 3.1: Equivalent Circuit of a Transistor [2]

Input and output bandwidths of transistor are given in Equations (3.1) and (3.2) where f_0 is center frequency, R_{in} is input resistance, C_{in} is input capacitance, R_o is output resistance and C_o is output capacitance of the transistor [2]. These equations show that bandwidth of transistor is limited by the input impedance.

$$\frac{\Delta f_{in}}{f_0} = 2\pi f_0 R_{in} C_{in} \tag{3.1}$$

$$\frac{\Delta f_{out}}{f_0} = \frac{1}{2\pi f_0 R_o C_o} \tag{3.2}$$

Furthermore, bandwidth equations show that series resistance addition can increase the bandwidth. However, transistor gain reduces in this case. Hence the bandwidth of an amplifier is inversely proportional to its gain. From another point of view, it can be said that better matching results in narrower frequency band.

3.1.2 Power Gain

The power gain of an amplifier can be defined as the ratio between output and input powers.

A commonly used gain definition for power amplifiers is the transducer gain (G_T), which can be expressed as in Equation (3.3), where P_L is power delivered to the load and P_S is power available at the source [2].

$$G_T = \frac{P_L}{P_S} \tag{3.3}$$

3.1.3 Input and Output Return Loss

The input and output return loss values are used to describe how well input and output impedance matchings are performed which are shown in Figure 3.2 below [23].

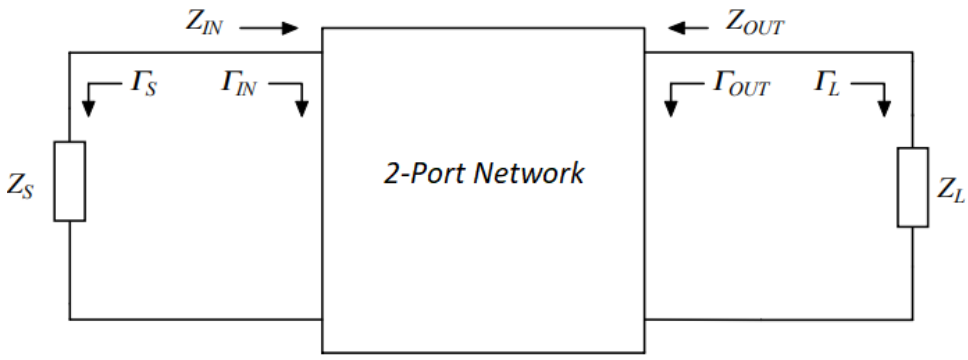


Figure 3.2: 2-Port Network [23]

Input and reflection coefficient can be described as given in Equations (3.4) and (3.5), respectively [23].

$$\Gamma_{IN} = \frac{Z_{IN} - Z_S^*}{Z_{IN} + Z_S} \tag{3.4}$$

$$\Gamma_{OUT} = \frac{Z_{OUT} - Z_L^*}{Z_{OUT} + Z_L} \tag{3.5}$$

When the output and input of an amplifier is not perfectly matched, a mismatch loss is observed. This is called as return loss (RL), which is the ratio between input power P_{in} and reflected power P_R as given in Equation (3.6) [2].

$$RL = -10\log\left(\frac{P_R}{P_{in}}\right) = -10\log\left(|\Gamma|^2\right) \tag{3.6}$$

Mismatch of output matching circuit causes output power degradation. Calculated worst case output power degradation with respect to output reflection coefficient is shown in Figure 3.3 [23].

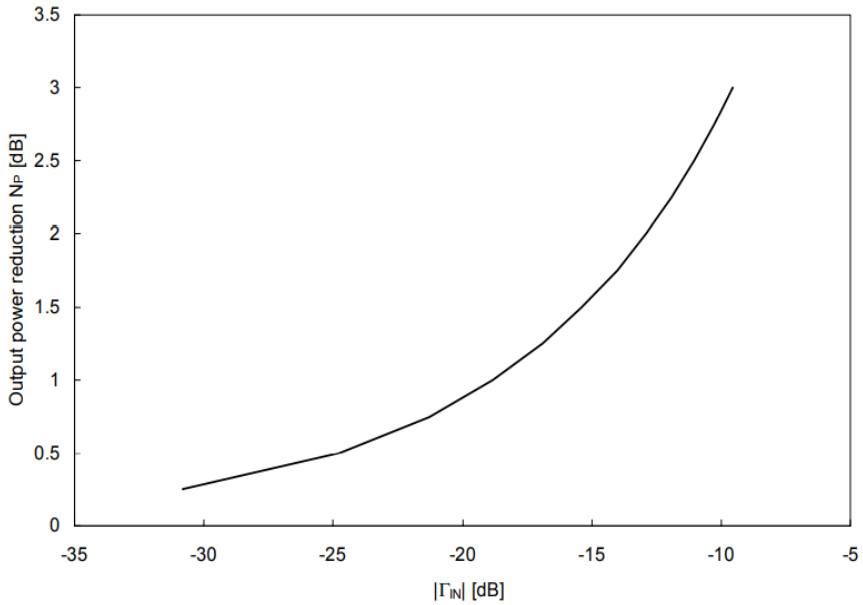


Figure 3.3: Output Power Degradation with respect to Output Reflection Coefficient [23]

3.1.4 Output Power

Power delivered to the load from the power amplifier can be defined as the output power which is a function of the input power. When the amplifier is compressed by 1 dB, output power can be defined as P_{1dB}. Saturated output power can be defined as the maximum output power which cannot increase while input power increases. Generally, this output power is obtained at where the amplifier gain is compressed by 3-5 dB [2]. Gain versus output power of an amplifier is shown in Figure 3.4.

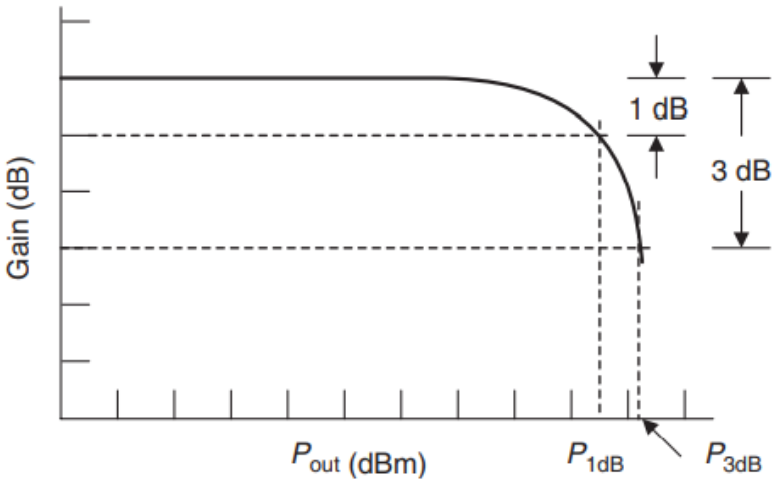


Figure 3.4: Gain versus Output Power Graph of a Power Amplifier [2]

3.1.5 Efficiency

Power amplifiers consume DC power and generates RF output power. Power amplifiers are designed to provide best efficiency in order to prevent power dissipation which is converted to heat. Drain efficiency is defined as in Equation (3.7) where P_{out} is output power and P_{DC} is DC power applied to the transistor [1].

Another commonly used performance parameter for PAs is the power added efficiency (PAE), which is defined as in Equation (3.8) where P_{out} is output power, P_{in} is input power and P_{DC} is DC power applied to the transistor [1].

$$Eff. = \frac{P_{out}}{P_{DC}} \tag{3.7}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{3.8}$$

3.2 Design Procedure

Design methodology of a power amplifier is based on the selection of an appropriate set of transistor, substrate material, topology and design method. The performance goals, targeted in this work are given in Table 3.1. A broadband amplifier design is targeted in this work, in order to compare simulation and measurement results over a wide frequency band. Because of microstrip losses of the matching circuits, the mismatch over bandwidth, the need for stability resistances and the trade-off between broadband operation and gain of amplifier, the target gain and output power values are chosen below the maximum values listed on datasheet of the bare die transistor. Small signal gain and output power targets are selected as minimum 15 dB and 50 W, although the maximum values provided in the datasheet are 19 dB and 75 W, respectively. Moreover, because of the wideband operation of the amplifier, the return loss target is chosen as maximum 5 dB over the entire bandwidth. When the bare die transistor is in saturation, typical efficiency value is given as 60 % in the datasheet. Drain efficiency target is chosen as minimum 40 %, because of the wideband operation target. Furthermore, an equivalent product is taken as a reference to determine the target specifications. Drain efficiency of the equivalent product which is biased near the Class-A point is measured higher than 50 %, even exceeding 60 % at some frequencies [24].

Table 3.1: Power Amplifier Specifications

PARAMETERS	SPECIFICATIONS
Frequency Band	0.5-3 GHz
Output Power	> 50 Watt
Small Signal Gain	> 15 dB
Input Return Loss	< -5 dB
Output Return Loss	< -5 dB
Drain Efficiency	> 40 %

3.2.1 Transistor Selection

First step of the amplifier design is the selection of an appropriate transistor with respect to the system requirements such as frequency of operation, output power level, small signal and large signal gain and efficiency. There are several transistor technologies such as InP, LDMOS, GaAs, SiGe, GaN/Si and GaN/SiC. Most recent and popular technology is GaN on SiC. This technology provides high efficiency and high output power due to large bandgap, high breakdown voltage, high electron velocity, high mobility and high sheet charge density properties [10]. Because of high breakdown voltage of the GaN technology, high drain voltage can be applied to the transistor, and hence, a high output power level can be obtained. Also, high operation temperature and low thermal resistance properties provide long term reliability of the transistor. GaN on SiC devices have large input and output impedance levels, which provide less effort to match to 50 Ω, smaller size matching circuitry and wideband design [10].

In this work, design targets are output power of 50 W, 40 % efficiency with 15 dB small signal gain in 0.5-3 GHz operation frequency band as mentioned at Table 3.1. The discrete GaN transistor, modeled in Chapter 2, is used for this goal.

3.2.2 Substrate Material Selection

Second step of the power amplifier design is the selection of an appropriate PCB material. Each material has tradeoffs between the quality of specifications and cost. However, relatively higher operating frequency of the amplifier design requires a high performance PCB material [25]. Thus, system requirements, which are frequency of operation, output power level, size of the design, loss requirements, environmental conditions and cost should be considered. Also, some of important PCB material specifications such as power handling capability, stability over environmental conditions, EM loss, thermal properties, producibility and cost should be considered too [25].

Relative permittivity (D_k) is one of the basic specifications of a PCB material [26]. Value of D_k affects the size of the amplifier design, because higher value of D_k results in shorter guided wavelength which results in shorter physical length of transmission lines. Also, how it is affected by environmental conditions such as temperature and humidity is important, because these environmental effects can change the relative permittivity with respect to nominal value at room temperature. Stable D_k over operating bandwidth prevents phase distortion and provide consistent transmission line impedance. Amplifier design requires impedance matching to the characteristic impedance over operating frequencies in order to maximize power transmission. Uniformity of D_k across dimensions of PCB material is required for transmission line impedance control. Furthermore, it is important that D_k value is stable with changing temperature, which is determined by the thermal coefficient parameter. It represents the amount of change in dielectric constant in parts per million (ppm) for one degree change in temperature.

Dissipation factor (D_f) or loss tangent is the other basic specification of a PCB material. D_f should be low to be appropriate for high power applications. Dissipation factor is a measure of dissipated signal energy through the PCB material. In order to minimize loss in output power and gain, D_f should be as low as possible. Also, low loss materials have less D_k vs. frequency slope. Figure 3.5 shows D_k and D_f versus frequency graph.

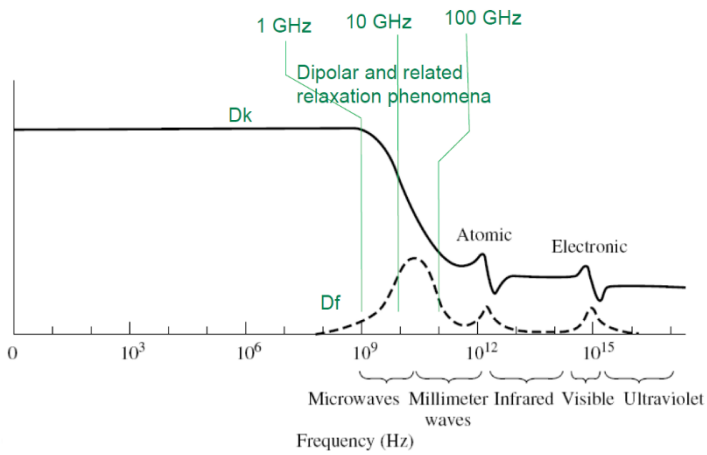


Figure 3.5: D_k and D_f versus Frequency Graph [27]

Because of the high operating temperature of the power amplifier, coefficient of thermal expansion (CTE) of PCB material should be considered too. CTE value should be as low as possible in order to result minimal physical change in the PCB material with temperature change.

Thermal conductivity is the other important specification that should be considered for power amplifier design. In order to assure long term reliability of the amplifier, heat should be transferred away from the transistor. Higher value of thermal conductivity assures better power handling capability.

PCB conductors are not perfectly smooth surfaces which is quantified by conductor surface roughness. Electrical impact of the conductor roughness increases with frequency.

3.2.2.1 Chosen Substrate

When all trade offs and performance requirements are considered, 0.254 mm thickness Rogers 6035 substrate with ½ oz copper is chosen for this study. This material provides high thermal conductivity, improved dielectric heat dissipation which enables lower temperatures for high power applications, low loss tangent and good high frequency performance. Also, D_f and D_k are thermally stable as desired [28]. Material specifications can be seen in Table 3.2. Furthermore, heat flow versus temperature rise graph is shown below in Figure 3.6 which indicates how better Rogers6035 substrate material is than the others, in terms of thermal conductivity.

Table 3.2: RO6035 Material Properties [28]

Parameter	Value	
Dielectric Constant	3.6	
Loss Tangent ($\tan\theta$)	0.0013	
Thermal Conductivity $\left(\frac{W}{m.K}\right)$	1.44	
Coefficient of Thermal Expansion $\left(\frac{\text{ppm}}{°\text{C}}\right)$	X	19
	Y	19
	Z	39
Thickness	10 mil	

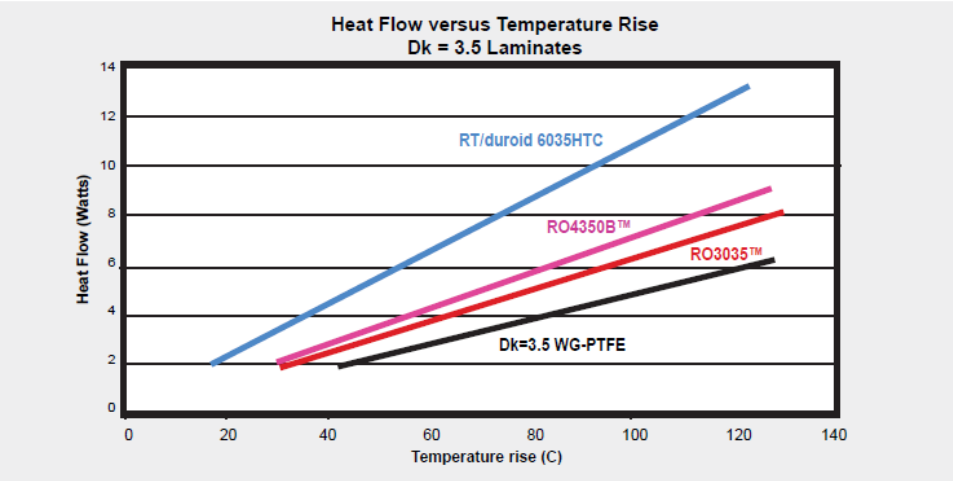


Figure 3.6: Heat Flow versus Temperature Rise Graph [28]

3.2.2.2 Substrate Characterization

Dielectric constant values are provided in the datasheet, however they are average values over frequency and dependent on fabrication process. Because transmission line impedance is very important in amplifier design process, precise values of dielectric constant at operating frequencies should be known. There are different test

methods for material characterization. In this work, microstrip differential phase length method is used, which is the method Rogers Corporation also uses. This method is based on the measurements of S parameters, especially S_{21} phase.

Two different-length transmission line should be designed on the PCB with typically 3:1 length ratio [27]. Circuits should be identical and designed on the same panel. 50 Ω characteristic impedance should be chosen [27].

The microstrip phase angle formula is given in Equation (3.9) [27] where Φ is phase angle, L is the length, f is the frequency and ε_{eff} is the effective dielectric constant.

$$\Phi = 2\pi f \frac{\sqrt{\varepsilon_{eff}}}{c} L \tag{3.9}$$

$\Delta\Phi$ is the difference of phase angle for two different-length transmission lines where ΔL is the difference of transmission line lengths and c is the speed of light in free space as given in Equation (3.10) [27].

$$\Delta\Phi = 2\pi f \frac{\sqrt{\varepsilon_{eff}}}{c} \Delta L \tag{3.10}$$

Rearranged formula in order to find ε_{eff} is given in Equation (3.11) [27].

$$\varepsilon_{eff} = \left(\frac{\Delta\Phi c}{2\pi f c \Delta L}\right)^2 \tag{3.11}$$

Two different length 50 Ω microstrip lines are designed by using ADS. Two lines are designed with 100 mm length difference to provide calculation simplicity. S-parameter simulation results are compared with measured results, as shown in Table 3.3.

Table 3.3: Comparison of Simulated and Measured Phase Differences

Frequency (GHz)	Simulated phase difference (°)	Measured phase difference (°)
0.5	101.12	99.74
1.0	202.54	199.08
1.5	302.69	298.38
2.0	403.42	397.58
2.5	504.14	496.59
3.0	604.93	595.75

There is a 1.5% deviation between simulated and measured phase differences. With respect to obtained data, calculated ε_{eff} and D_k values are given in Table 3.4. Thus, D_k=3.65 is used for design within frequency band 0.5-3 GHz.

Table 3.4: Calculated ε_{eff} and D_k Values versus Frequency wrt Measured Phase Difference Data

Frequency (GHz)	ε_{eff}	D_k
0.5	2.76	3.68
1.0	2.74	3.66
1.5	2.74	3.65
2.0	2.73	3.65
2.5	2.73	3.64
3.0	2.73	3.64

3.2.3 Class of Amplifier

RF power amplifiers are classified as Class A, B, AB, C, D, E and F according to DC bias points and conduction angle of current [29]. Class of operation is chosen with respect to system requirements such as linearity, gain, efficiency and output

power level. There is a trade-off between linearity, efficiency and output power level. With decreasing conduction angle, efficiency increases but linearity decreases.

Class AB amplifier is a combination of Class A and Class B whose conduction angle is between 180° and 360° with bias conditions are chosen between Class A and B operations. This class operation has higher efficiency than Class A and higher linearity than Class B. Comparison of operation classes are given in Table 3.5 [29].

Table 3.5: Classes of Amplifiers and Characteristics [29]

Class	Gain	Efficiency (%)	Linearity	Conduction Angle (◦)	Power Handling
A	High	Under 50	Best	360	Low
B	Medium	Under 78.5	Better	180	High
AB	High	50-78.5	Good	180 < n < 360	Medium-high

Class AB is chosen in this work in order to obtain moderate gain, efficiency and linearity. Class AB amplifier is operated at quiescent drain current of 0.1 to 0.2 I_{dss} as shown in Figure 3.7 [29].

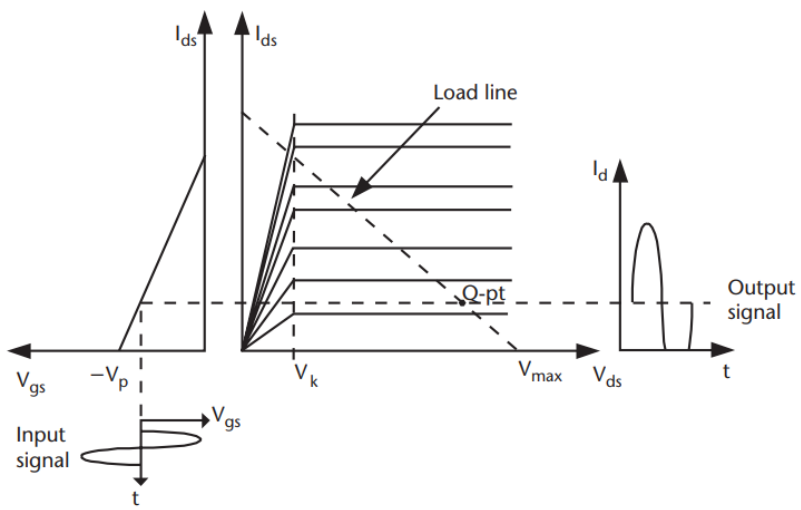


Figure 3.7: Class AB Operation Waveform [29]

3.2.4 Design Methodology

Design methodology is composed of DC I-V characteristics analysis, bias circuit design, stability analysis, input matching, load pull and output matching steps.

3.2.4.1 DC I-V Characteristics Analysis

The quiescent point is one of the most important parameter of PA design procedure. Bias point determines class of amplifier which affects the specifications of amplifier such as efficieny and linearity. Hence, making load line analysis is important. In this way, a design should be started with I-V graph analysis of the transistor.

Obtained I-V graph is shown in Figure 3.8. Marker m_1 shows I_{dss} current (near to peak current) and m_2 shows cut-off point. m_3 is around 0.1-0.2 I_{dss} which describes class AB point [29].

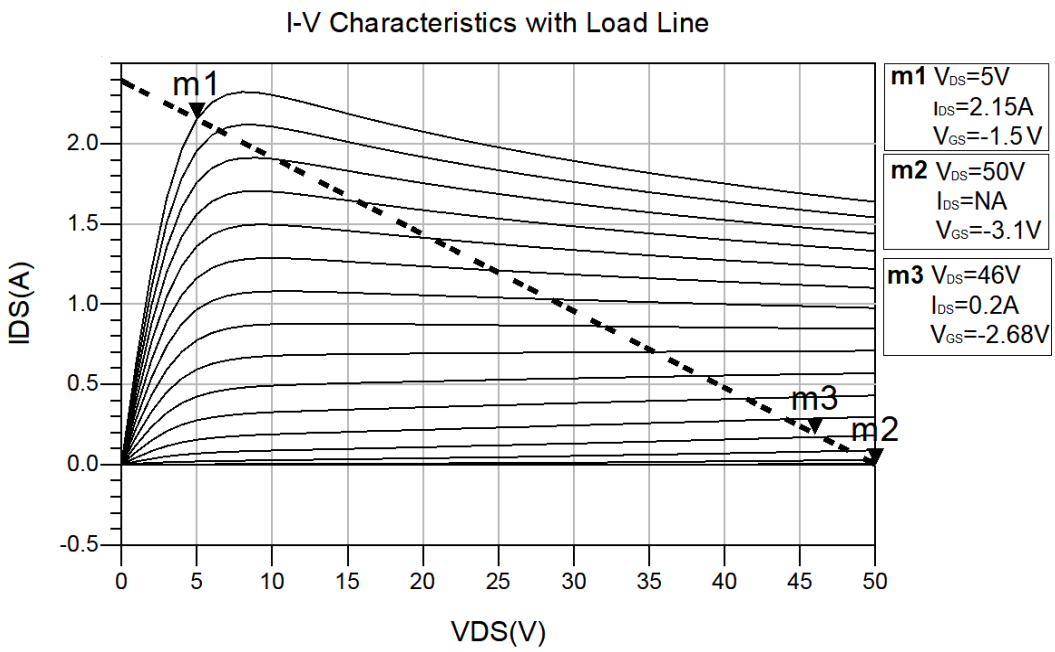


Figure 3.8: DC I-V Characteristics with Load Line

I_{dss} is between 1.9 A - 2.2 A, as seen in Figure 3.8, around marker m_1. m_3 shows quiscent point which should be chosen to provide 0.1-0.2 I_{dss}. Thus, bias current should be between 190 mA - 220 mA. The quiscent point is chosen as V_{GS}=-2.68 V and I_{DS}=200 mA at V_{DS}=50 V where class of amplifier is deep Class AB which is the point closer to Class B.

3.2.4.2 Bias Circuit Design

Bias network should be designed in order to make sure that appropriate bias reaches to device and also there is no leak of RF power. Bias network topology is based on the frequency of operation. In DC bias circuitry, RF choke or high impedance λ/4 (quarter wavelength) line can be used depending on the frequency of operation [30]. If the frequency of operation is low, RF choke can be used. However if high frequencies are reached, the inductance value of the RF choke starts to change with frequency. At self resonant frequency (f_{SR}), which can be reached at relatively lower frequency levels, the inductor looks like an open circuit. In this way, at high frequencies high impedance line is preferred [30].

Resistors are used in the gate bias circuitry to improve stability and also to provide isolation between transistor gate and power supply. Bias circuit includes not only quarter wavelength line but also resistors, which provide stability, and bypass capacitors. These components add extra length to the quarter wavelength line. Therefore, the bias line should be adjusted with extra components and their footprints.

In this work, microstrip line design is preferred to achieve bias conditions because of relatively easier design and unrequired component assembly.

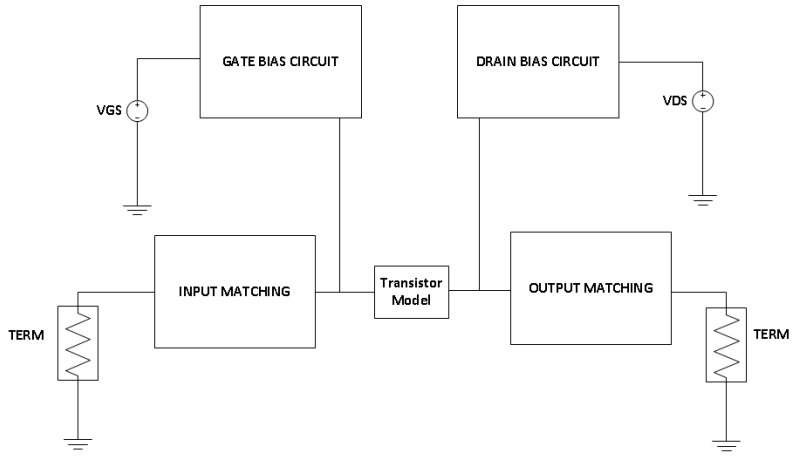


Figure 3.9: Block Diagram of Power Amplifier Design

Coupling capacitors are used in drain bias circuitry as shunt capacitive elements [30]. Appropriate values of bypass capacitors should be chosen in order to decouple RF signals from drain bias voltage (V_{DD}) supply line to ground over wide bandwidth. Proper selection of bypass capacitor provides very low impedance to ground. Theoretically, ideal impedance is zero ohms, however, actual non-ideal capacitors show some impedance because of its reactance and parasitics. Some of frequency dependent capacitor parameters such as series resonant frequency (f_{SR}) and equivalent series resistance (ESR) should be analyzed. ESR is the summation of all losses of capacitor. f_{SR} is the resonant frequency at which net reactance of capacitor is zero and the impedance is equal to ESR [30].

A capacitor which has an f_{SR} value close to the desired bypass frequency should be chosen in order to establish a low impedance path with minimum net reactance, which makes it ideal for bypass applications.

Drain bias circuitry is shown below in Figure 3.10. High impedance quarter wavelength line is designed over bandwidth with minimum loss as seen in Figure 3.11.

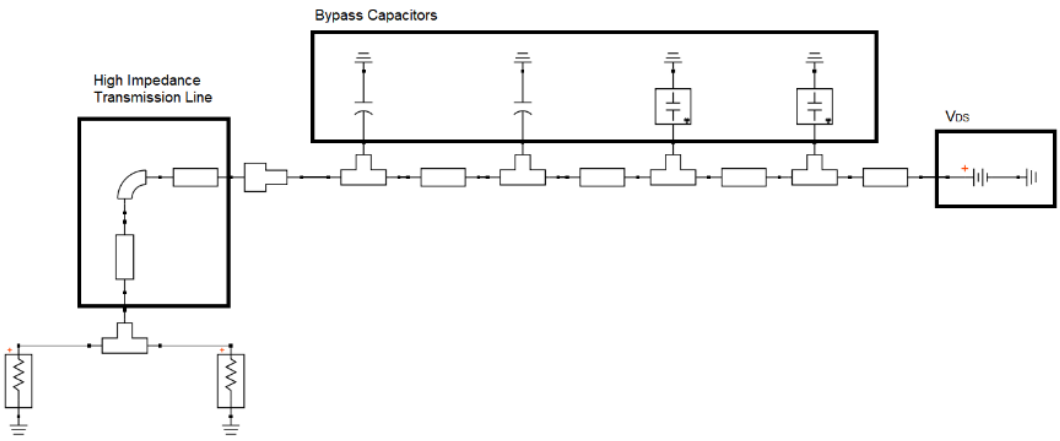


Figure 3.10: Drain Bias Circuit

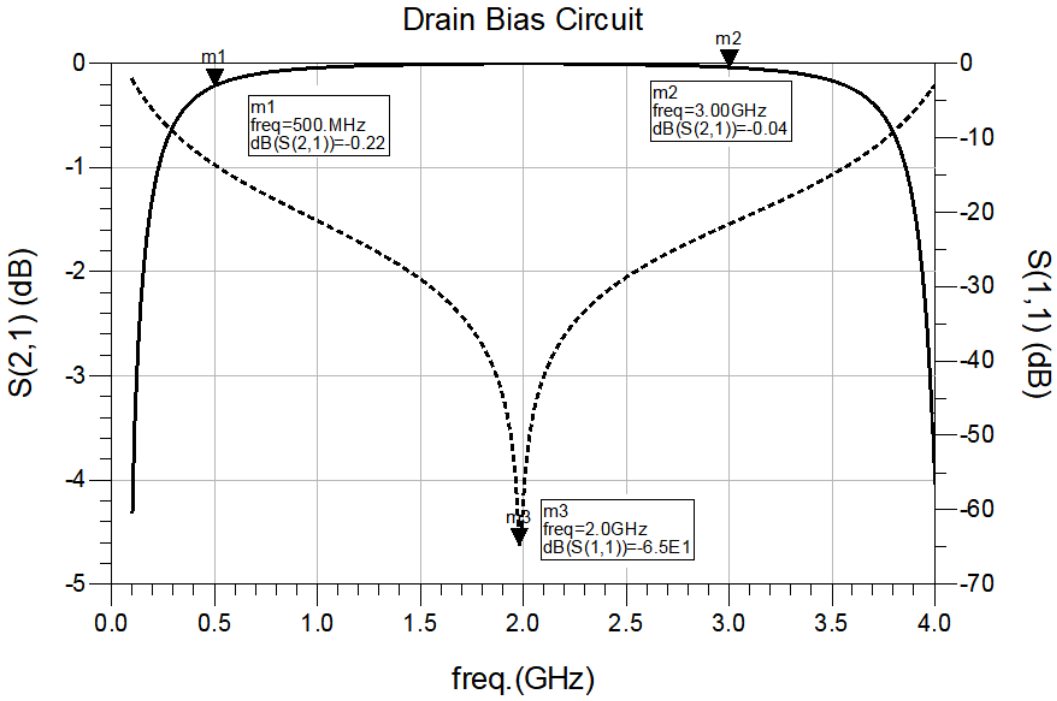


Figure 3.11: Drain Bias Circuit S_{21} and S_{11} Graph

A resistance is used in the gate bias circuitry in order to improve stability. Also, bypass capacitors are used in order to eliminate small voltage spikes of DC power

supply and reduce noise. High impedance quarter wavelength line is designed over the bandwidth with minimum loss, as seen in Figure 3.13.

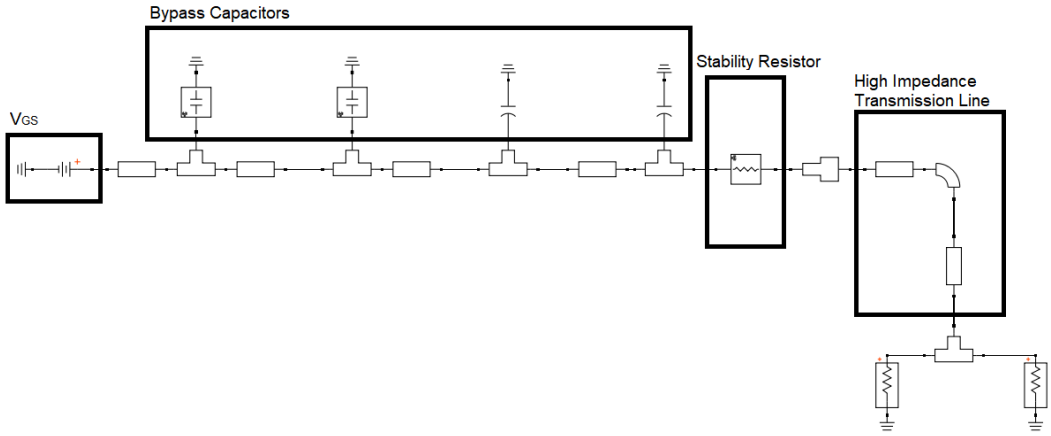


Figure 3.12: Gate Bias Circuit

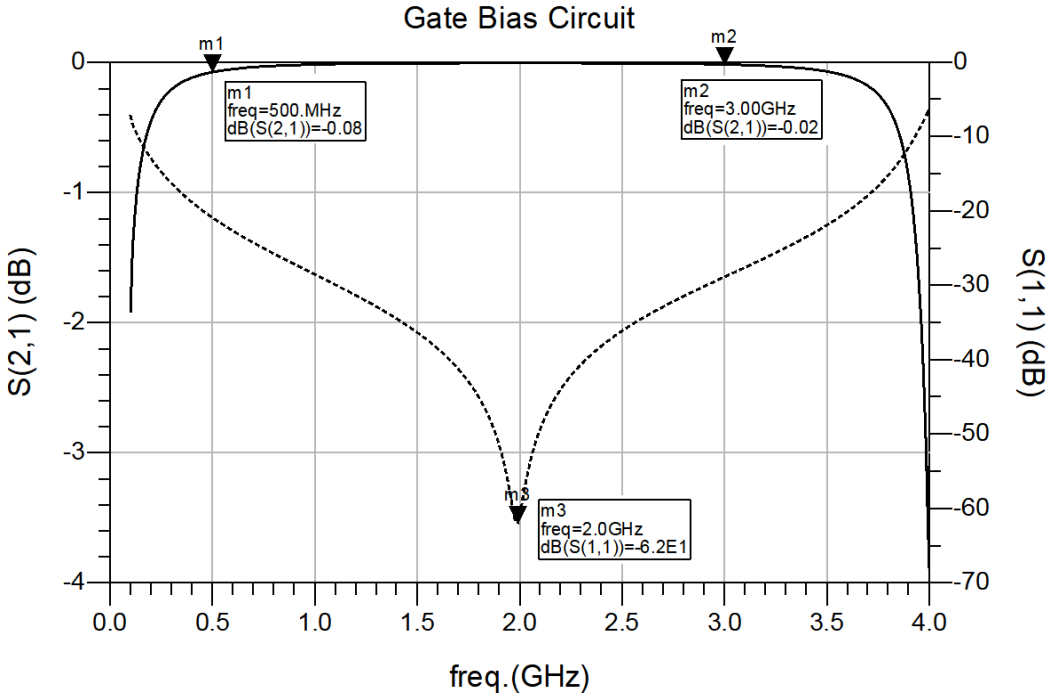


Figure 3.13: Gate Bias Circuit S_{21} and S_{11} Graph

3.2.4.3 Stability Analysis

After selecting DC bias point of the transistor, small signal stability analysis should be performed. Stability is a very important requirement, because if stability conditions are not satisfied, power amplifier oscillates [2]. Furthermore, transistors have a tendency to be unstable at low frequencies, because gain of transistor is extremely high at that frequencies due to the internal structure of field effect transistor (FET).

The stability of an amplifier can be determined by the S-parameters and input and output matching networks.

Unconditional stability is the most desirable scenario which indicates that PA is stable not only within operational frequency band, but also in the entire frequency spectrum [2]. In order to guarantee unconditional stability there are two necessary conditions that should be satisfied. For a two port network $K > 1$ and $|\Delta| < 1$ where K and Δ are in Equations (3.12) and (3.13) [2].

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{3.12}$$

$$K = \frac{(1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2)}{2(S_{21}S_{12})} \tag{3.13}$$

With increasing ‘K’ value , more stable power amplifier can be obtained. But there is a tradeoff between the value of K and gain of the amplifier because ‘K’ increases with resistive components [2].

Stability is improved by adding resistance in the gate bias circuitry as shown in Figure 3.12. Stability resistance in the gate bias decreases the excessive gain at low frequencies.

Resistor and short stub integration as seen in Figure 3.15 provides better S_{11} and stability. When resistor value is high enough, S_{11} and stability at low frequencies

gets better. If resistor value is low enough, S_{11} and stability at high frequencies gets better.

RC circuitry improves stability while capacitor introduces higher impedance at low frequencies and resistance causes loss for RF path . Resistor should be chosen in order to have enough power handling capacity to prevent burn out during large signal operation.

Mu prime (μ') is the geometrically derived stability factor for the source side of the amplifier. This measurement gives the value of distance from the center of the Smith Chart to the nearest unstable source stability circuit. This stability factor is given in Equation (3.14) [19] where Δ is the determinant of the S-parameter matrix.

$$\mu' = \frac{(1 - |S_{22}|^2)}{|S_{11} - conj(S_{22})\Delta| + |S_{21}S_{12}|} \tag{3.14}$$

To have $\mu' > 1$ is the only necessary and sufficient condition for uncondinional stability of a two port network. μ' plot of the design over all operating frequencies can be seen in Figure 3.14.

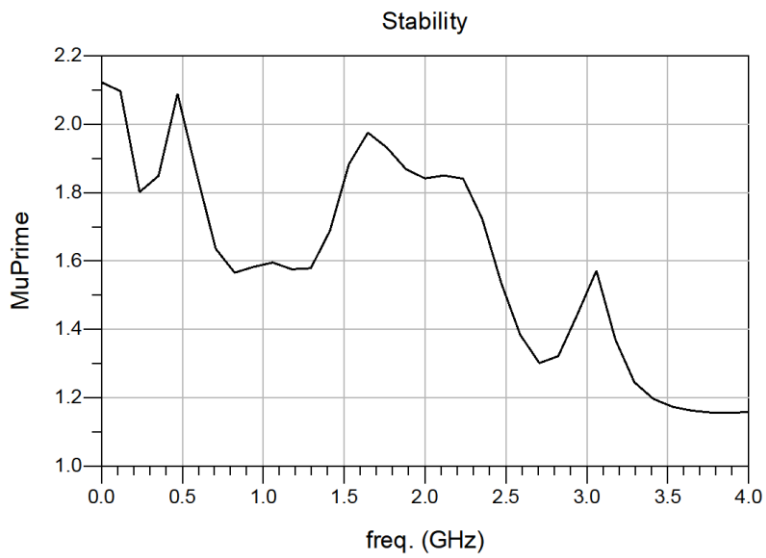


Figure 3.14: μ' Graph of the Design

3.2.4.4 Input Matching

Input matching network is one of the most important subcircuit of the amplifier design. To provide maximum power transfer to the transistor, input matching network should be carefully designed. Input matching network design is more complicated than output matching network design because input impedance of transistor has low real and high reactive parts. Because of that, input matching network determines bandwidth of the amplifier. In other words, high reactive part limits broadband matching [2].

Also, since FET device has excessive gain at low frequencies, there is too much gain difference between high and low frequencies of a broadband amplifier design [2]. For this reason, parallel RC network is used for stability by introducing high attenuation at low frequencies.

The input of the transistor shows low impedances as shown below in Figure 3.16. Because of low impedances, there is a need of resistive component in order to match almost a purely imaginary impedance to 50 Ω. Thus, RC stability network is used as a part of input matching network.

DC block capacitor is used to isolate RF source from gate bias voltage (V_{GS}). It is selected to show very low impedance at operating frequency band. In other words equivalent series resistance (ESR) values should be as low as possible over the bandwidth. Also, quality factor (Q) of the DC block capacitor should be high in order to have low insertion loss. Power handling capacity of DC block capacitor should be taken into consideration, too. DC block capacitor should be mounted after the bias circuitry.

Resistor and short stub integration as seen in Figure 3.15 is used in order to obtain better S_{11} and stability.

Bias circuitry, RC stability network, DC block capacitor and resistor with short stub are parts of the matching network.

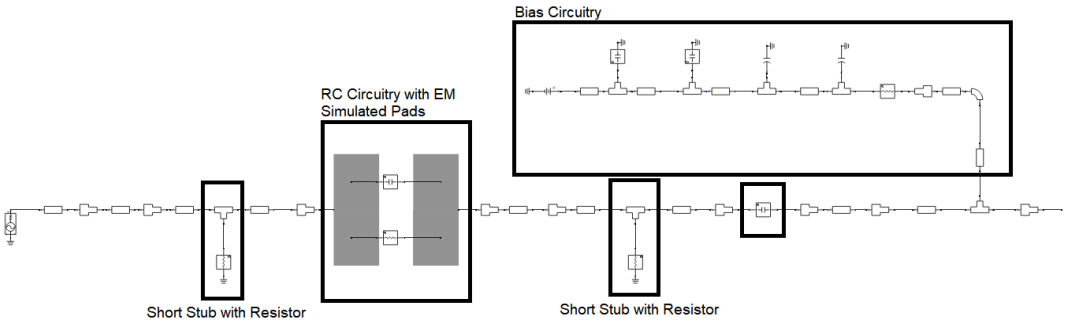


Figure 3.15: Input Matching Circuitry

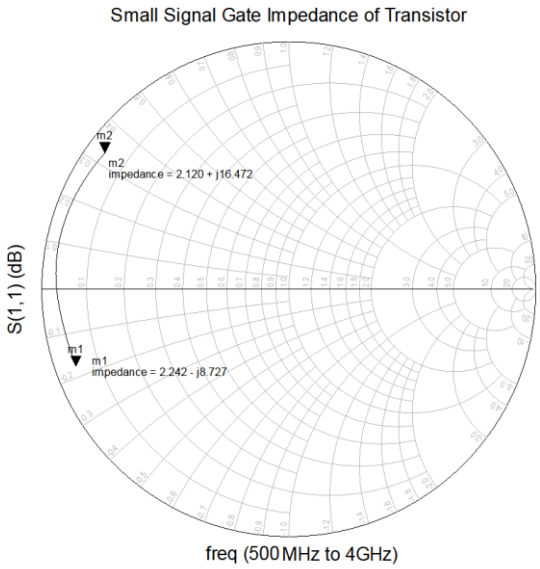


Figure 3.16: Gate Impedances of Transistor Over 0.5-3 GHz Bandwidth

After designing the input matching network in schematic, EM simulation should be performed in order to analyze parasitic coupling between components especially at high frequencies. Input matching network EM simulation is performed by using ADS EM simulation tool. EM simulation setup should be prepared carefully to obtain good agreement between simulation and measurement results of the PA.

Full 3-D solvers, such as HFSS or ADS FEM tools, are capable of simulating complex 3-D structures. These tools require long procesor time and at least 64 GB

memory [31]. For PCBs which are planar, planar solvers can be used to lower the computation time and memory requirements. The main advantage of planar solvers is the computation speed which increase at least 10 times compared to 3-D solvers [31]. Also, the computation time does not exponentially increase with size of structure contrary to 3-D solvers [31].

MoM simulation method is referred to as a 3-D planar solver whose main practical advantage is that it mesh only the metal interconnects in the structure [32]. MoM solver uses planar mesh which is much simpler than 3-D mesh of FEM solver. MoM mesh consists of rectangles, quadral shaped cells and triangles which are created on metal interconnects. To be able to use a 3-D planar solver, the simulated structures should be planar and fit inside the layered stack-up or planar objects which are extruded along z-plane [32]. As a result, PCB lay-outs can typically be solved by using MoM solver as seen in Figure 3.17 [32]. Because MoM solver uses reduced number of mesh cells, fewer unknowns and more efficient simulation is obtained compared to an FEM solver. The other benefit of MoM solver is that for all port excitations on structure, only one matrix should be solved which decreases computation time and memory [32]. Therefore, for planar structures, ADS MoM solver is a more efficient simulation method which is generally recommended for analysis of PCB interconnects, planar antennas and etc. [32]. On the other hand, for 3-D complex structures such as connectors, waveguides, packages and etc. FEM solver is more appropriate. That is why MoM 2.5-D planar solver is preferred, for the PA simulations, over the 3-D FEM solver, which was used for package modeling.

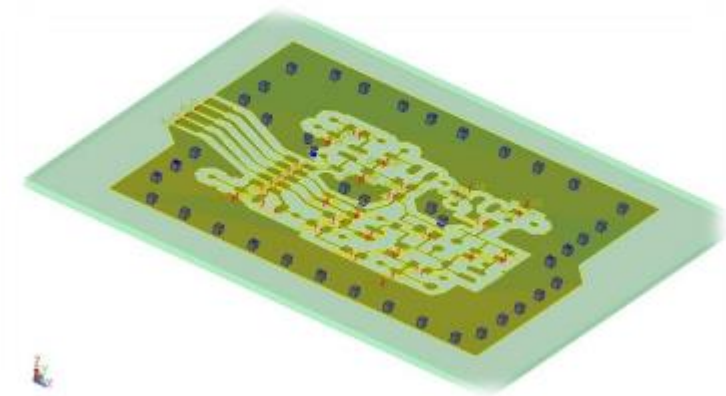


Figure 3.17: An Example of PCB Lay-out on MoM Solver [32]

Momentum simulator defines a voltage source between + and – terminals of port where distance between terminals should be smaller than $\frac{1}{10}$ of wavelength at highest operation frequency [32]. Pins are connected to the input and output of the layout and to the pads of the components. Feed type of ports on component pads are chosen as surface mount device (SMD) which is a differential port with two edge pins on a gap in the layout and removes self inductance and capacitance to ground [19]. Feed type of input which is connected to the transistor is chosen as TML which has an edge pin and is used for electrically long transmission lines. Feed type of output and bias are chosen as TML (zero length) which has an edge pin and is used for electrically short transmission lines. Both TML and TML (zero length) calibration types remove port feed parasitics [19].

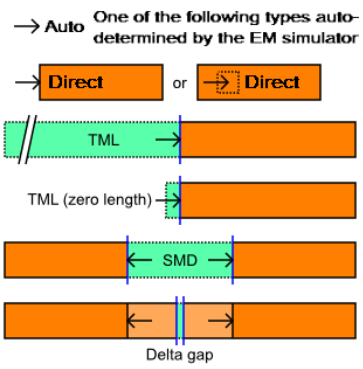
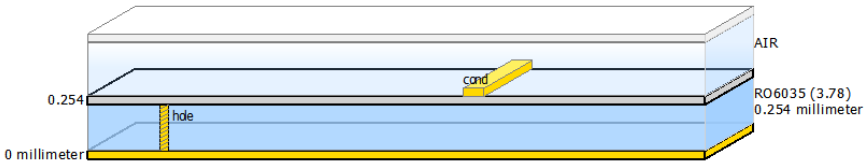


Figure 3.18: Port Feed Types [17]

Method of Moments (MoM) simulator, which is a 2.5-D planar EM simulation tool is chosen. MoM simulator is used for general planar circuits, such as microstrip, stripline, coplanar waveguide etc. [19].

Simulation frequency plan is chosen up to 12 GHz to include harmonics. For MoM simulation, planar mesh elements are used, which are generated only on flat metal surfaces. After the simulation is performed, EM model is created as seen in Figure 3.20, in order to combine discerete components along with the layout.



Substrate Layer Stackup

	Type	Name	Material	Thickness
	Dielectric		AIR	
1	Conductor Layer	cond (1)	Copper	30 um
	Dielectric		RO6035	0.254 mm
	Cover		PERFECT_CONDU...	0 um

Figure 3.19:Proper Substrate Definition

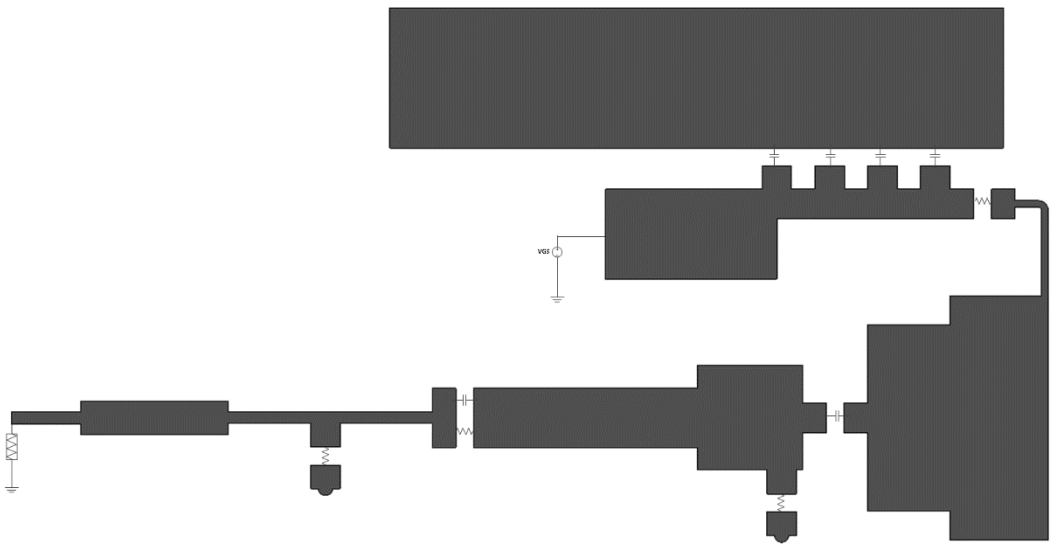


Figure 3.20: Input Matching Network Lay-out

EM simulation results are compared below in Figure 3.21 and Figure 3.22. Because output matching circuit is not performed yet, load tuner is used on the output side of amplifier. Solid line shows transistor with EM model of package and dotted line shows transistor with lumped element model of package on the amplifier design.

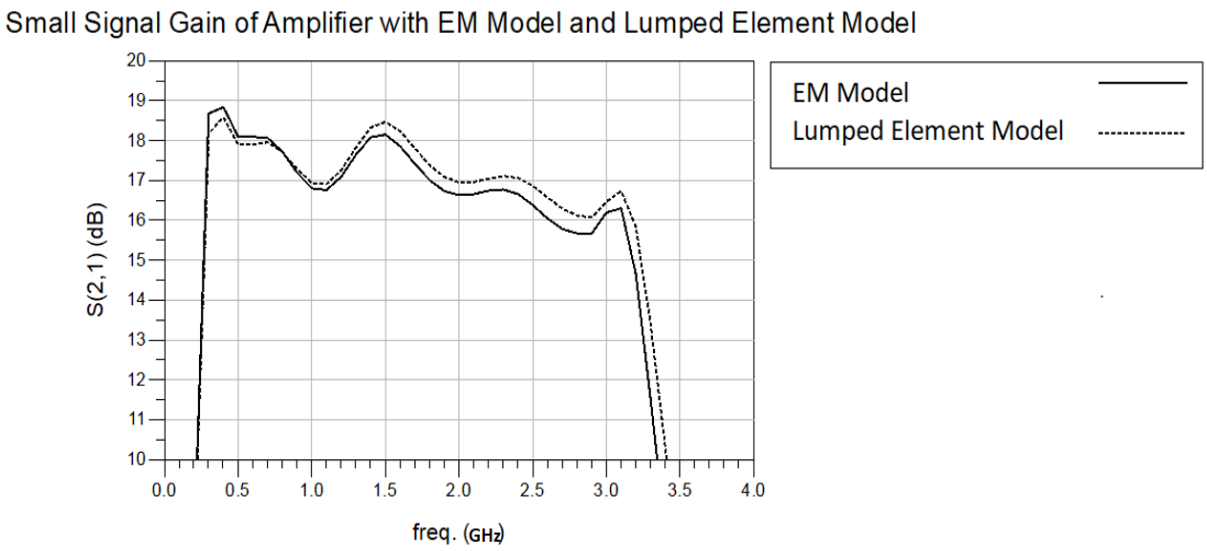


Figure 3.21: S_{21} Graph with Input Prematch and Load Tuner

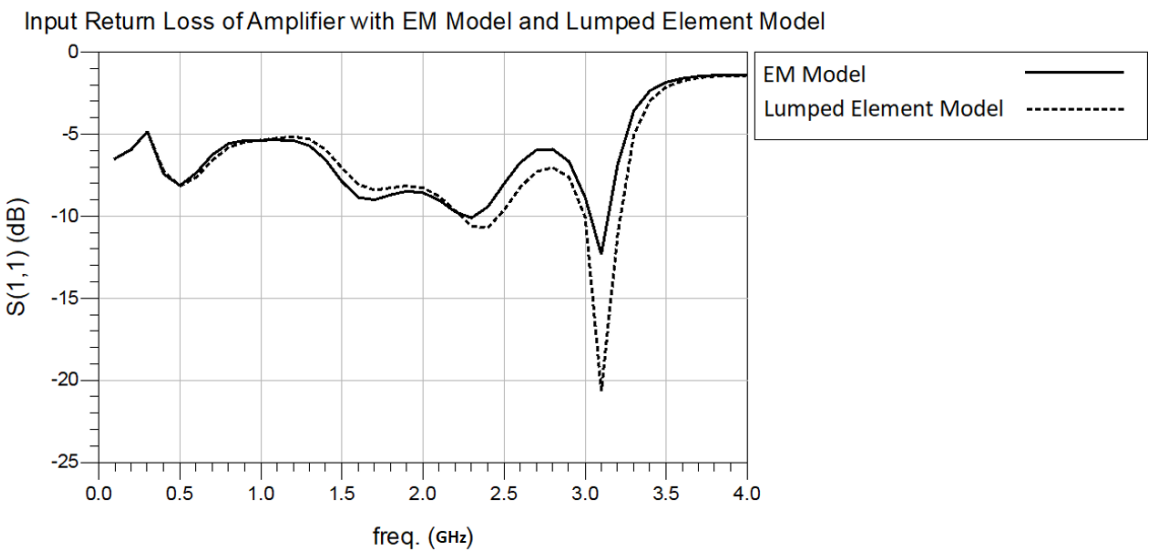


Figure 3.22: S_{11} Graph of Amplifier with Input Prematch

3.2.4.5 Load Pull

Load pull is an analysis which is used to find optimum impedance at the output of the transistor in order to obtain target output power and efficiency [35]. Load pull analysis includes input matching circuitry in order to stabilize transistor and make sure that small signal gain is as desired across the bandwidth. There is an ideal DC feed and DC block elements provided by ADS tool on the output of the transistor as shown in Figure 3.23. Furthermore, load pull instrument is showed in Figure 3.23.

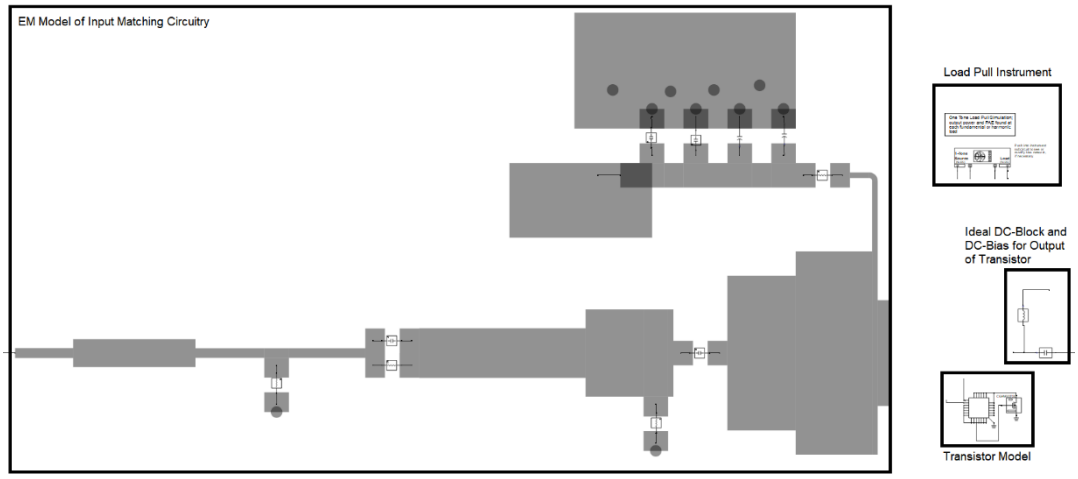


Figure 3.23: Load Pull Analysis Schematic

Since the goal of this work is to maximize the output power with sufficient efficiency, the impedance values given in Table 3.6 were chosen accordingly.

Table 3.6: Desired Load Matching Impedances with respect to Load Pull Data

Frequency (GHz)	Desired Load Matching Circuitry Impedance (Ω)	Output Power (Watt)	Drain Efficiency (%)
0.5	16.43+5.43j	83.17	72
1.0	10.07+9.39j	75.16	60
1.5	10.34+4.32j	81.65	64
2.0	10.34+4.36j	66.22	52
2.5	10.27+4.36j	72.77	56
3.0	5.31-0.84j	67.29	52

3.2.4.6 Output Matching

Impedance, seen by the transistor output determines the performance of an amplifier such as output power and efficiency [26]. Thus, output matching network design is one of the most critical part of the amplifier design. The output matching network should present optimum load impedance to the transistor output. This matching also should provide smallest matching loss and include DC bias supply circuit with DC decoupling capacitors.

Drain bias network, matching components and DC block capacitor are parts of the output matching network. Low loss matching components should be used in order to prevent power loss. Distributed components such as transmission lines and stubs should be used because, lumped components such as capacitors, resistors and inductors can not be used at microwave frequencies because of their physical sizes.

Also, since the frequency bandwidth is wide and includes 2nd and 3rd harmonics, in order to prevent undesirable notch in output power and efficiency of amplifier, output matching circuitry should be designed carefully. To observe the impact of

harmonics, load tuner is used and appropriate impedance values are determined to prevent notch in the frequency bandwidth.

Designed output matching circuitry with the ADS tool can be seen in Figure 3.25. Real and imaginary parts of the load matching circuitry impedance with respect to frequency is as seen in Figure 3.26. Table 3.7 and Figure 3.24 shows that, desired and obtained impedance values are close to each other.

Table 3.7: Load Matching Circuit Impedance Comparison Graph

Frequency (GHz)	Desired Load Matching Circuitry Impedance (Ω)	Obtained Load Matching Circuitry Impedance (Ω)
0.5	16.43+5.43j	10.77+11.09j
1.0	10.07+9.39j	11.48+3.73j
1.5	10.34+4.32j	12.89+2.43j
2.0	10.34+4.36j	11.70+2.17j
2.5	10.2+4.36j	12.50+1.97j
3.0	5.31-0.84j	8.41+3.59j

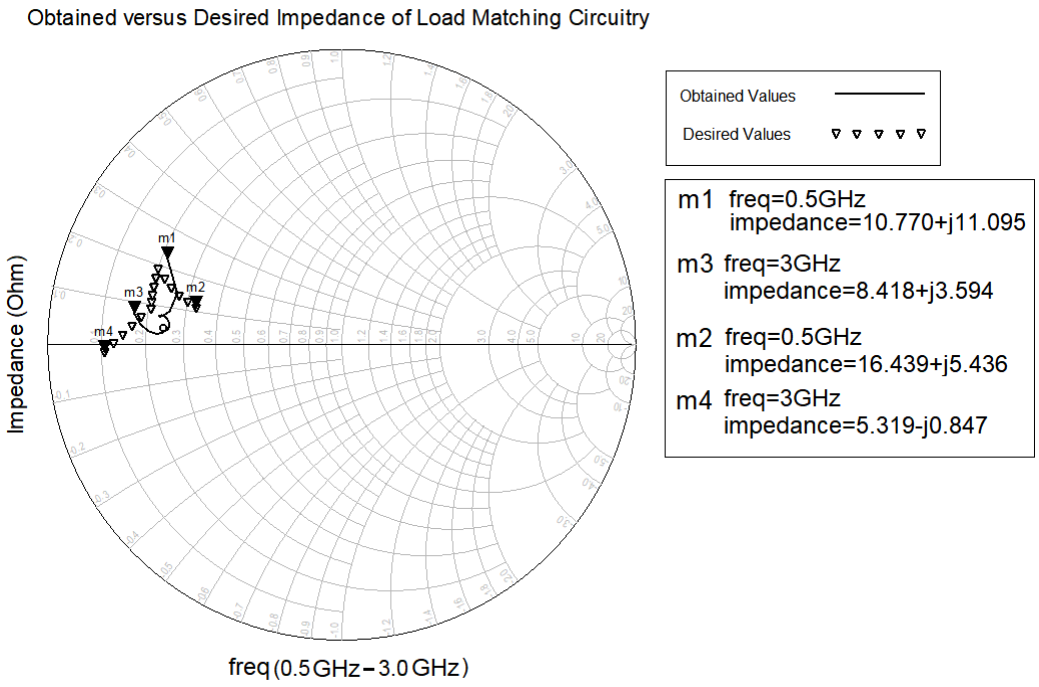


Figure 3.24: Obtained and Desired Output Matching Impedance Values on Smith Chart

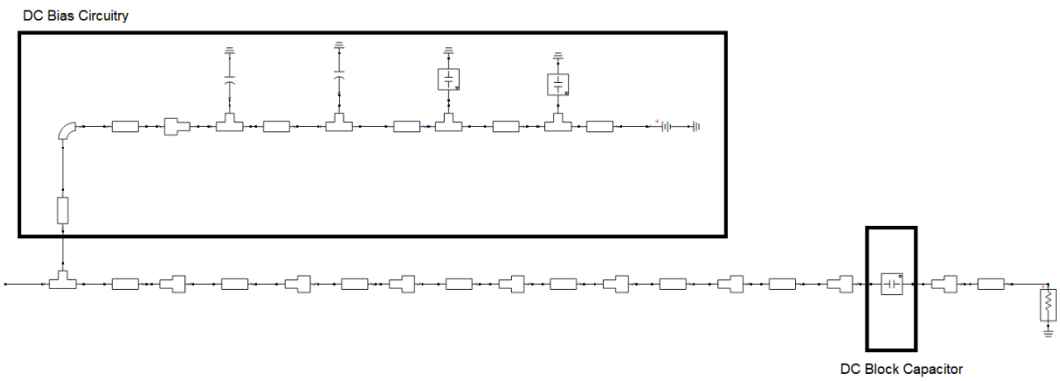


Figure 3.25: Output Matching Circuitry

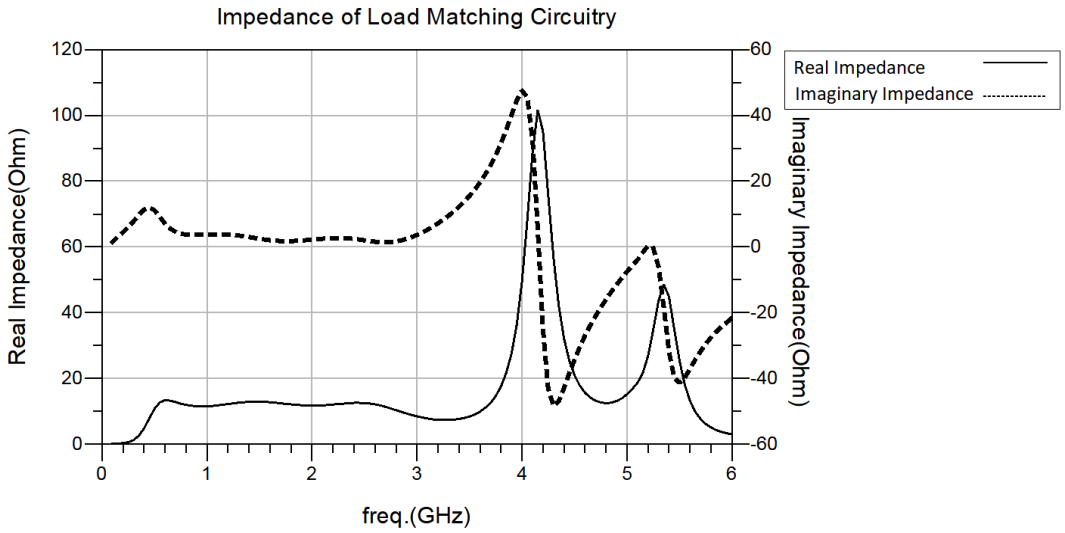


Figure 3.26: Load Matching Circuitry Impedance

After designing the output matching network, electromagnetic simulation should be performed with the same process applied to input matching network. Output matching network simulation is performed by using ADS Momentum EM. Pins are connected to input and output of layout and also pads of the components. Feed type of ports on component pads are chosen as SMD.

Feed type of input which is connected to the transistor is chosen as TML. Feed type of output and bias are chosen as TML (zero length).

Proper substrate definition is made as seen in Figure 3.19 which is the same as the input matching network EM simulation. Simulation frequency band and conductor meshing properties are defined. After simulation is done, EM model is created as seen in Figure 3.27 in order to combine discrete components along with the layout.

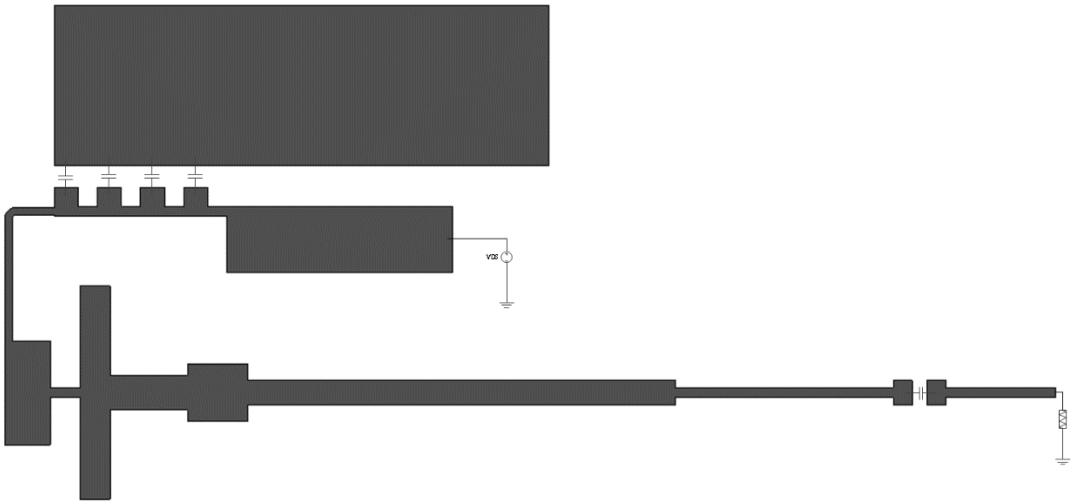


Figure 3.27:Output Matching Network Lay-out

EM simulation small signal results of the overal amplifier design are given in Figure 3.28 - Figure 3.31. Both EM model and Lumped element models are used in the simulations and compared. S_{21}, S_{11} and S_{22} responses agree well within the band of interest.

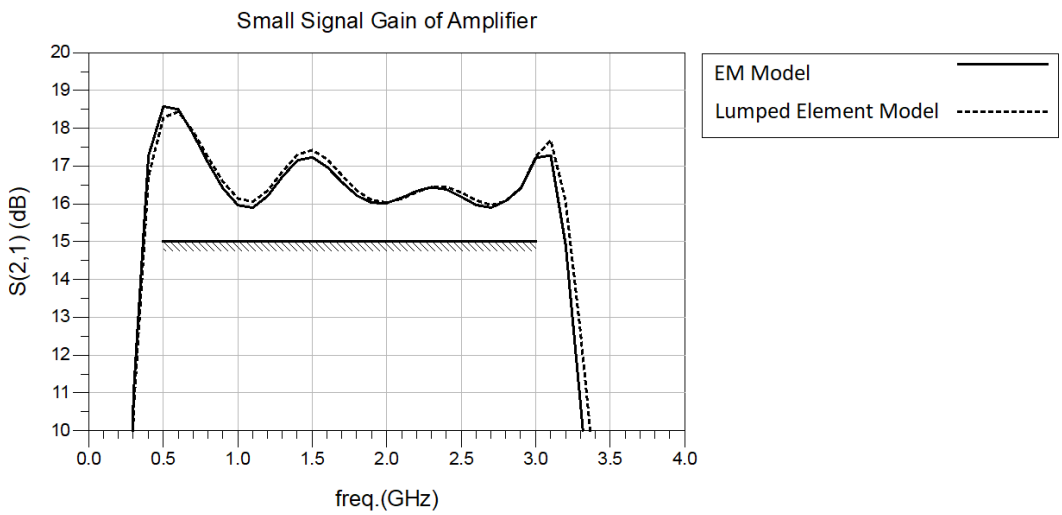


Figure 3.28: S_{21} Graph of Overal Amplifier

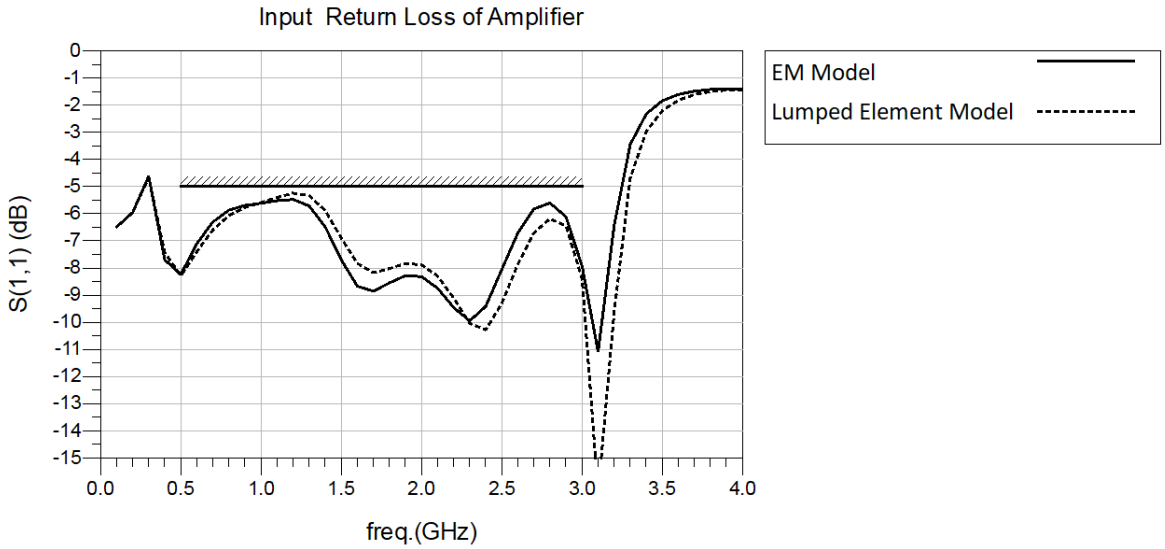


Figure 3.29: S_{11} Graph of Overal Amplifier

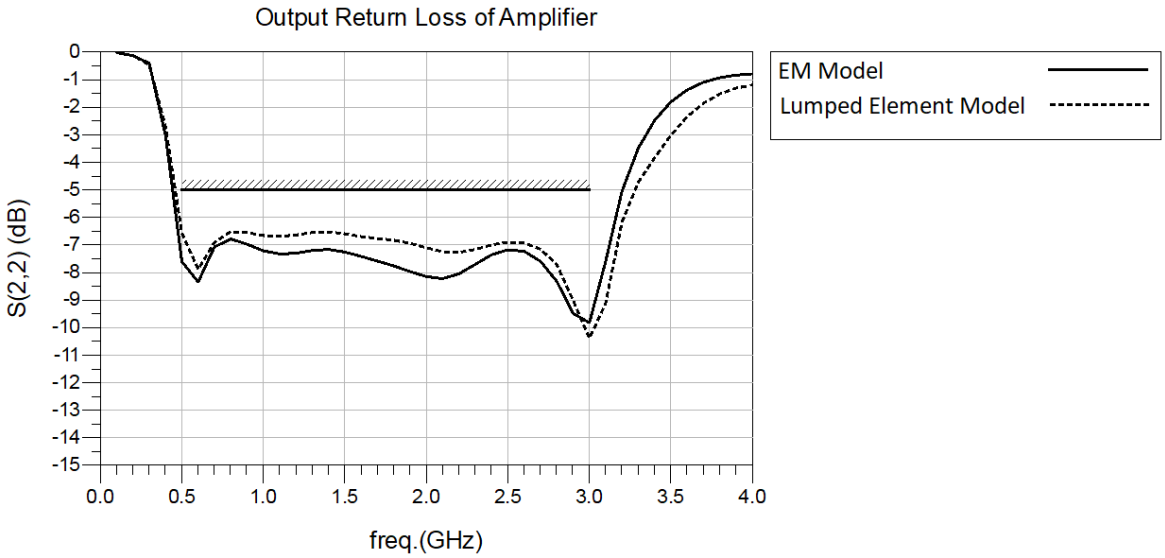


Figure 3.30: S_{22} Graph of Overal Amplifier

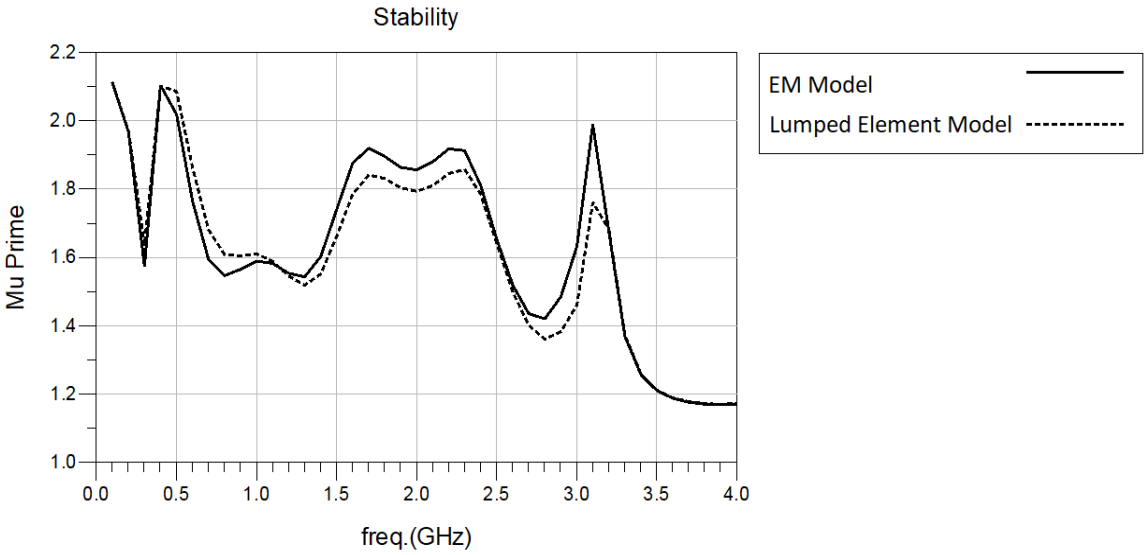


Figure 3.31: μ' Graph of Overal Amplifier

EM simulation large signal results of the overal amplifier design are given in Figure 3.32 and Figure 3.33. Both EM model and Lumped element models are used in the simulations and compared. Output power and drain efficiency responses obtained by two different models are very close to each other.

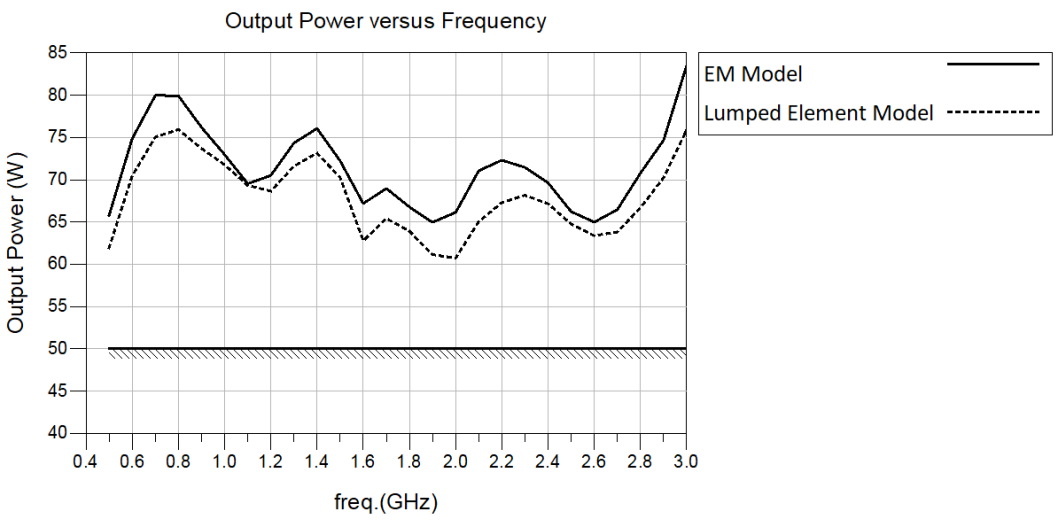


Figure 3.32: Output Power Graph of Amplifier

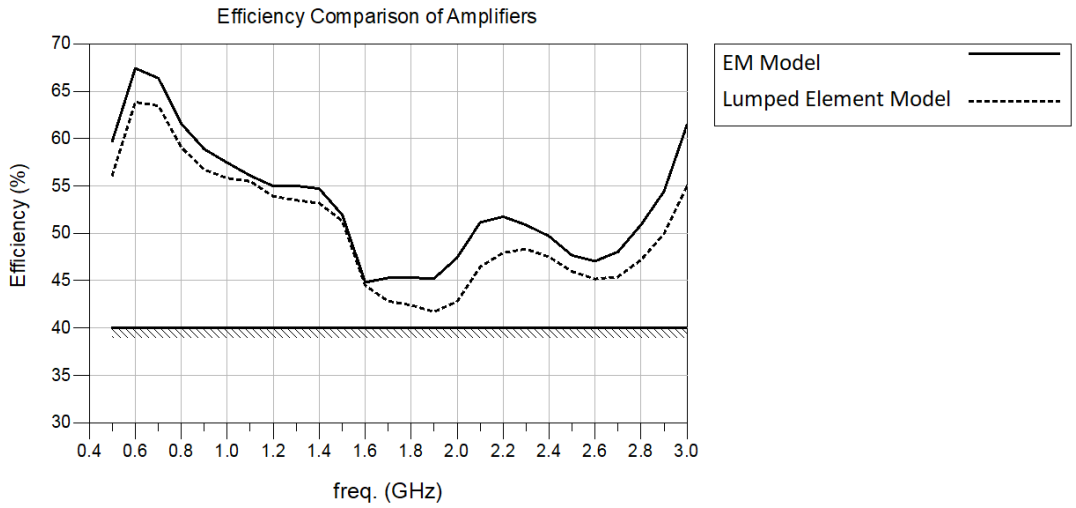


Figure 3.33: Efficiency Graph of Amplifier

3.3 Measurement

Measurement part includes a discussion on the description of the assessment of the measurement setup and measurement results.

3.3.1 Measurement Setup

Two different measurement setups are prepared to measure the small signal S-parameters and large signal output power and drain efficiency. Because stability of base temperature of the transistor is extremely important to get good correlation between simulation and measurement results, base temperature of the module is stabilized to 30 °C by using refrigeration. To improve measurement accuracy, by using temperature sensor, case temperature of the packaged transistor is checked after large signal test for each frequency step. To cool down the transistor and stabilize the base temperature of module to 30 °C, a waiting time is inserted between each frequency step of the large signal test. Furthermore, to obtain accurate measurement results, nonlinear model of the die transistor provided by manufacturer

should be reliable. Nonlinear model of the die transistor is direcly obtained from the measurements by manufacturer.

Electronic calibration tool (E-Cal) is used to calibrate the Network Analyzer which uses SOLT (short-open-load-thru) calibration technique. Accuracy of the calibration is tested before Small Signal Test of the amplifier.

The equipment used in the measurement setup is given in Table 3.8. Test setups are illustrated below in Figure 3.34 and Figure 3.35 as block diagrams. In addition, device under test (DUT) and a picture of the amplifier and attenuator combination is given in Figure 3.36 and Figure 3.37, respectively.

Table 3.8: Equipment List

Small Signal	Large Signal
Network Analyzer	Signal Generator
Electronic Calibration Device	Signal Analyzer
DC Supply	DC Supply
Attenuator	Predriver Amplifier
	Attenuator

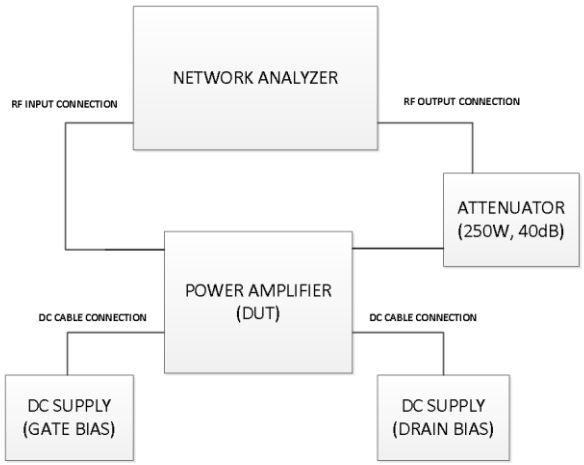


Figure 3.34: Small Signal S-parameter Measurement Setup

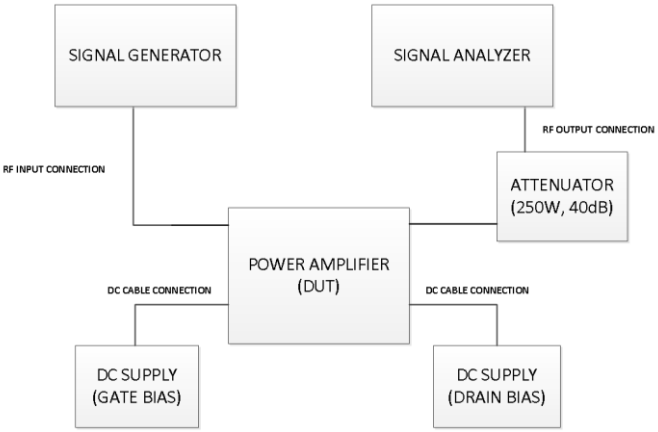


Figure 3.35:Large Signal Measurement Setup

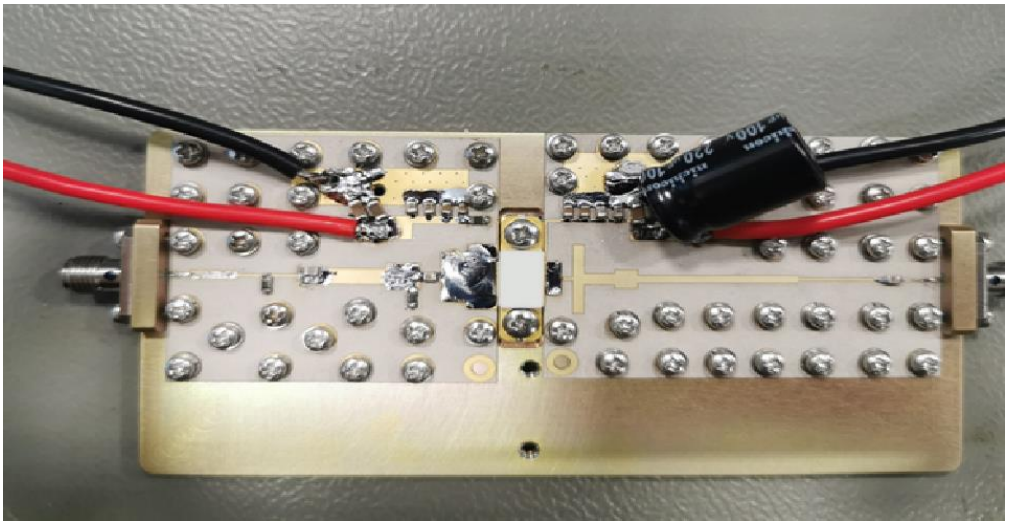


Figure 3.36: Power Amplifier (DUT)

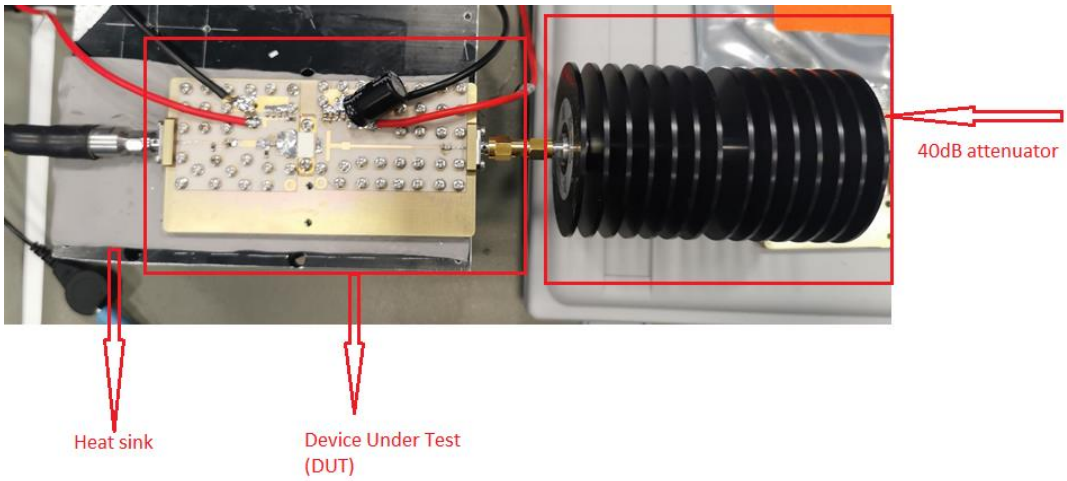


Figure 3.37:DUT, Heat Sink and 40 dB Attenuator

3.3.2 Measurement Results

Simulated and measured S-parameters are very close to each other as seen in Figure 3.38 - Figure 3.40. EM and lumped element models also agree well. Small signal gain target of amplifier which is above 15 dB is reached as seen in Figure 3.38. Moreover, input and output return loss target which is maximum 5 dB is reached as seen in Figure 3.39 and Figure 3.40.

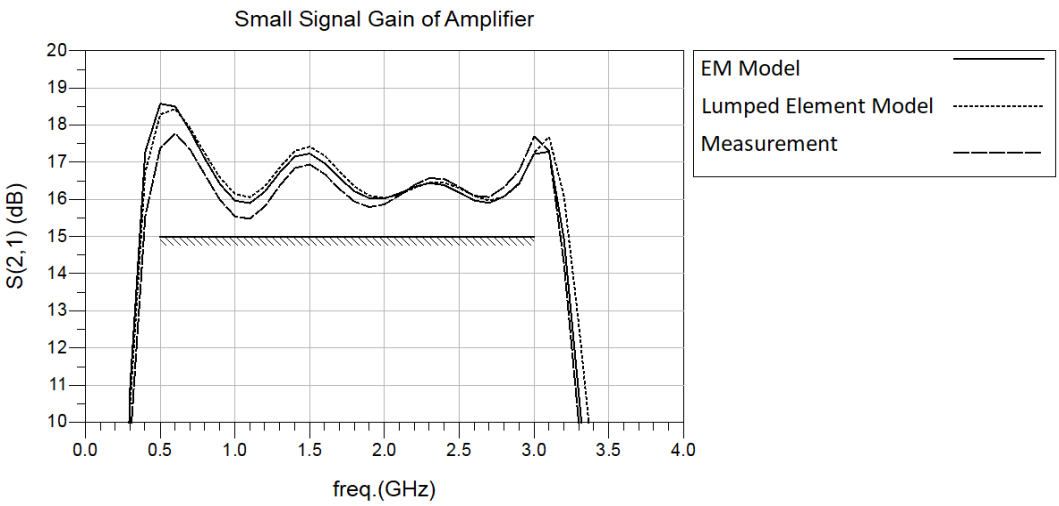


Figure 3.38: S_{21} Graph

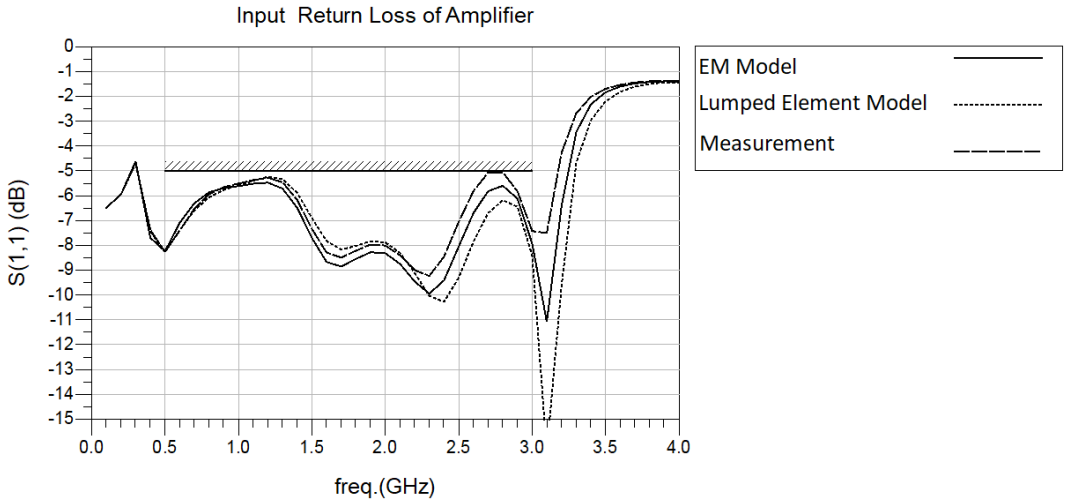


Figure 3.39: S_{11} Graph

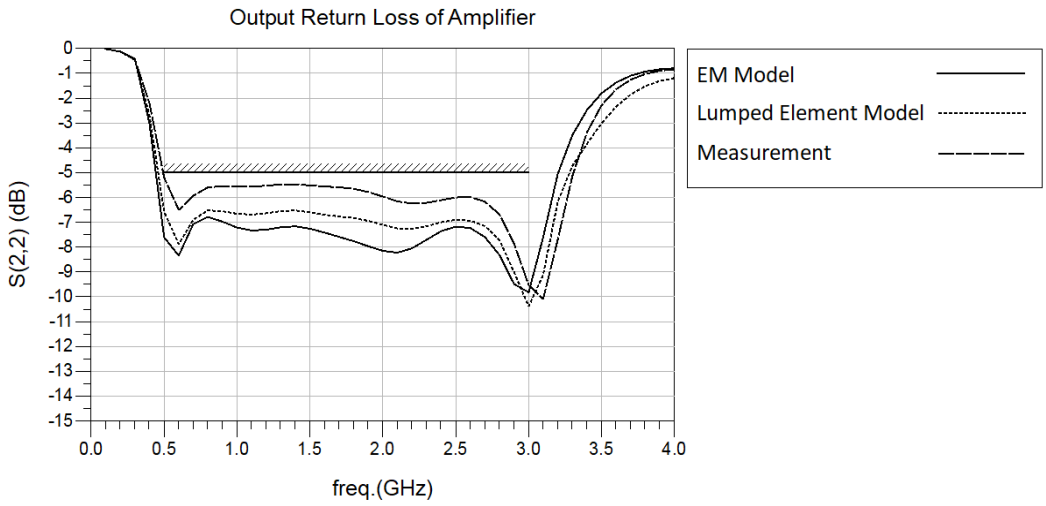


Figure 3.40: S_{22} Graph

Simulated and measured output power and drain efficiency graphs are given in Figure 3.41 and Figure 3.42. Measured output power of the amplifier is slightly lower than simulations, however the general response with respect to frequency is very similar. Measured efficiency of amplifier correlates well with simulations but as seen in Figure 3.42, especially between 1-2 GHz, efficiency is lower than that of overall band. Thus, in this range, transistor heat up and output power decreases. Because the model of bare die transistor is supplied at room temperature, difference between

model and measurement gets higher at that region as seen in Figure 3.41. Because the scale is in watts, difference seems high but in dB scale it is approximately 0.3 dB which is acceptable.

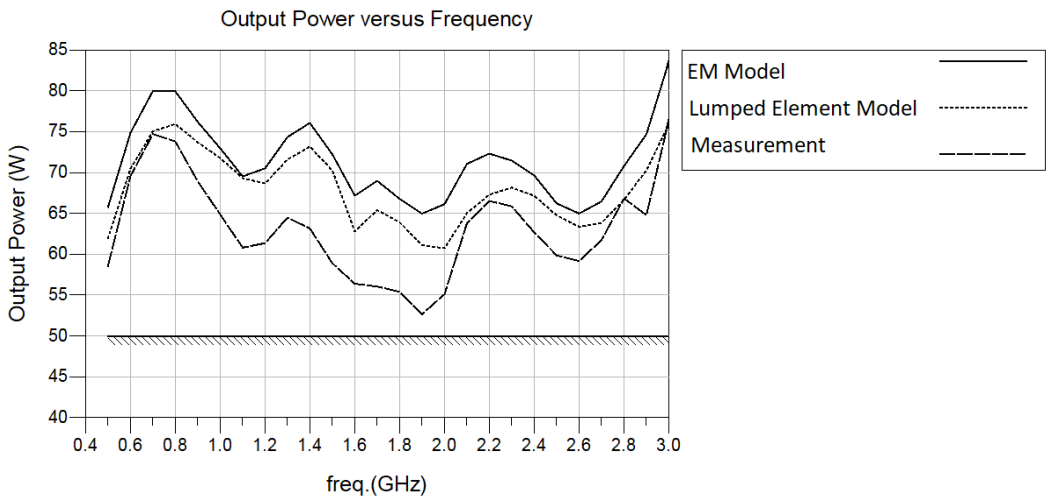


Figure 3.41: Output Power versus Frequency

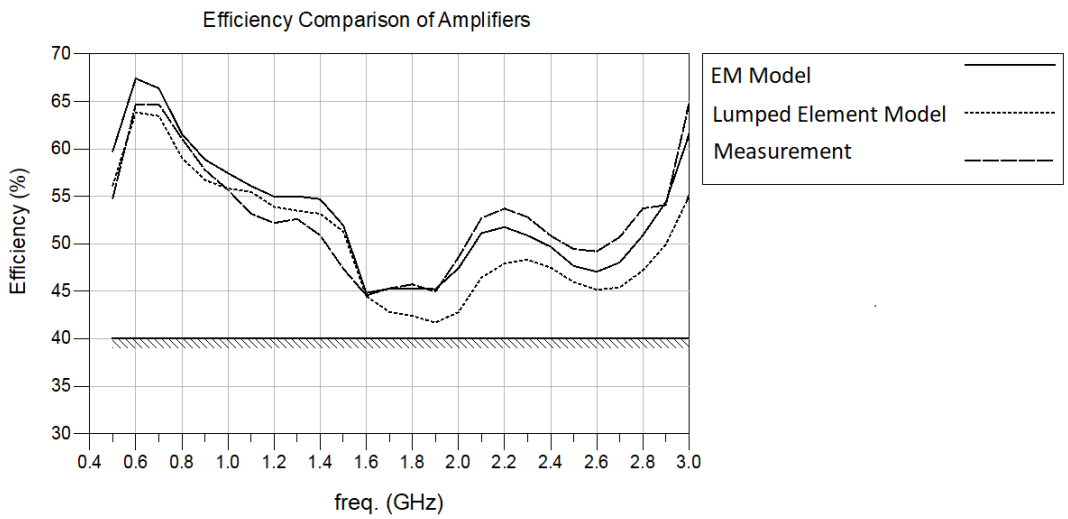


Figure 3.42: Efficiency versus Frequency

Obtained and targeted amplifier specifications are given in Table 3.9 below.

Table 3.9: Obtained and Desired Amplifier Specifications

Parameters	Targeted Specifications	Obtained Specifications
Frequency Band (GHz)	0.5-3	0.5-3
Output Power (Watts)	> 50	> 52
Small Signal Gain (dB)	> 15	> 15.4
Input Return Loss (dB)	< -5	< -5
Output Return Loss (dB)	< -5	< -5
Drain Efficiency (%)	> 40	> 44

CHAPTER 4

FLIP CHIP PACKAGE MODELING

4.1 Flip Chip Package Modeling

In flip chip technology, in contrast to wire bonding, the active side of the die is at the bottom and the electrical connection between the die and substrate or PCB is maintained by controlled collapse chip connection (C4) bumps [35]. The main advantage of this technology is the elimination of bond wires which significantly reduces unwanted parasitic inductance at the RF input and output, particularly at high frequencies. Without generating unwanted gain loss, GaN transistor die can be attached to the PCB by using flip chip technology [35]. Contrary to air cavity ceramic package, bare die transistor which is used in flip chip technology does not have back-vias which helps heat spread through source of transistor to ground. Thus, because of absence of back-vias, bumps should be designed in order to radiate heat efficiently. One of the most important disadvantage of the flip chip technology is the heat removal in this way [35]. Thus, flip chip technology is preferred for low power applications. Heat removal can be improved by enlarging the contact area of the bumps or inserting a metal connection between the bottom of the GaN bare die transistor and the ground of the module [35].

A simplified schematic drawing of the flip chip packaging is given in Figure 4.1 [36].

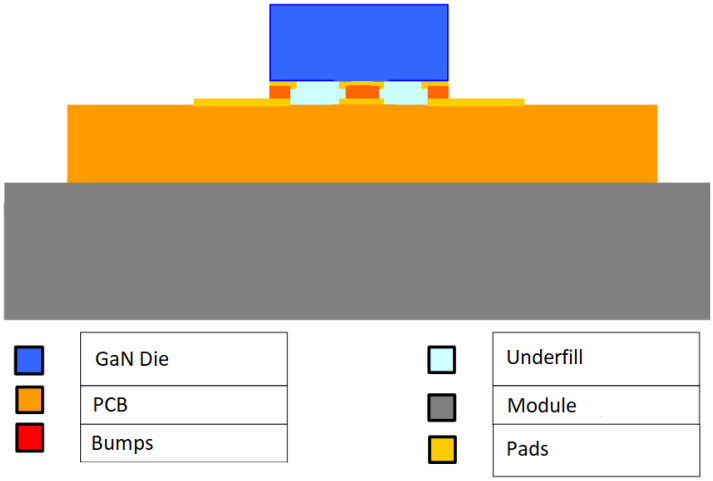


Figure 4.1: General Flip Chip Topology [36]

Two different bump technologies are used for flip chip technology [37]. First one is bonding by thermocompression and the second one is soldering in reflow oven. To determine bump material, CTE mismatch, manufacturability and cost should be taken into consideration. Bump geometry should be chosen to prevent reflections at the interconnect [37]. Especially bump diameter has an important effect on reflections contrary to bump height [37]. Thus, high frequency performance of transistor depends on the interconnect size.

High power transistors are generally housed in air cavity ceramic packages. However, because of large dimensions of this package, package parasitic results in degrading the performance of the transistor. Small signal gain and output power of transistors decrease at high frequencies. Operating maximum frequency decreases because of large inductance of long bond wires, mutual inductance between neighboring bond wires and large dimensions of the leads of air cavity ceramic package. To minimize package parasitics and easing the amplifier design for wideband applications, the flip chip package is suggested in this chapter based on full-wave simulations. Contrary to the work done so far, a high-power transistor is used and a mechanical model is suggested to provide heat transfer. Bottom of the GaN bare die transistor is attached to the ground of the module for this purpose.

4.2 Electrical Modeling

In this part of the thesis, flip chip package model is analyzed and compared with the air cavity ceramic package model. Instead of using a substrate, the die is directly attached to the PCB.

4.2.1 Geometry and Structure of Package Transistor

The flip chip package includes S-CMC heat sink, bumps and epoxy filling material between bare die transistor and the PCB as seen in Figure 4.2. To minimize the inductance of the bond wires and the capacitance of the leads, the connection between the PCB and the transistor is maintained by C4 bumps. The S-CMC the heat sink is used to spread heat at the bottom of the bare die transistor. The bare die transistor is attached to the heat sink with eutectic soldering same as the air cavity package design. Gate and drain pads of the bare die transistor are attached to the PCB metals with bumps whose material is copper due to high electrical. In order to provide electrical isolation between the bumps and and prevent thermal stress, epoxy underfill is used.

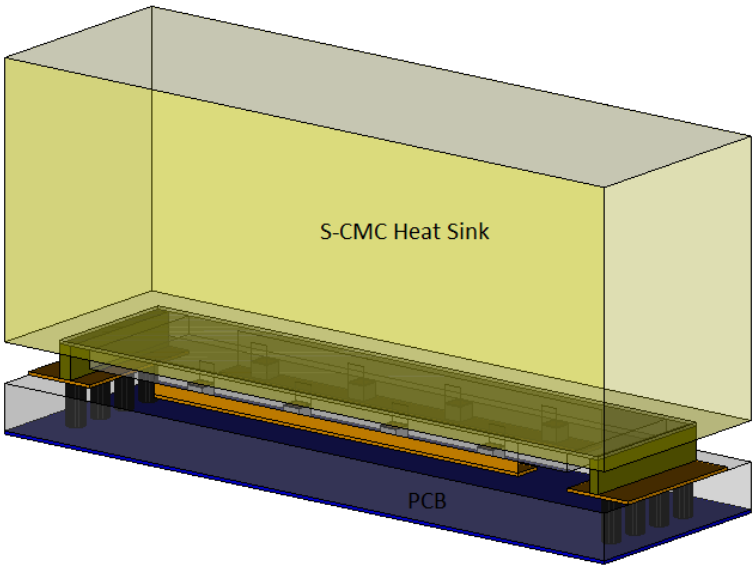


Figure 4.2: 3-D Model of Flip Chip Package

Source of the bare die transistor is directly connected to the S-CMC heat sink with back vias, to provide low thermal resistivity. Also, ground connection between the PCB ground and the ground of the bare die transistor is achieved by a metal wall between them.

4.2.2 3-D EM Modeling Methodology

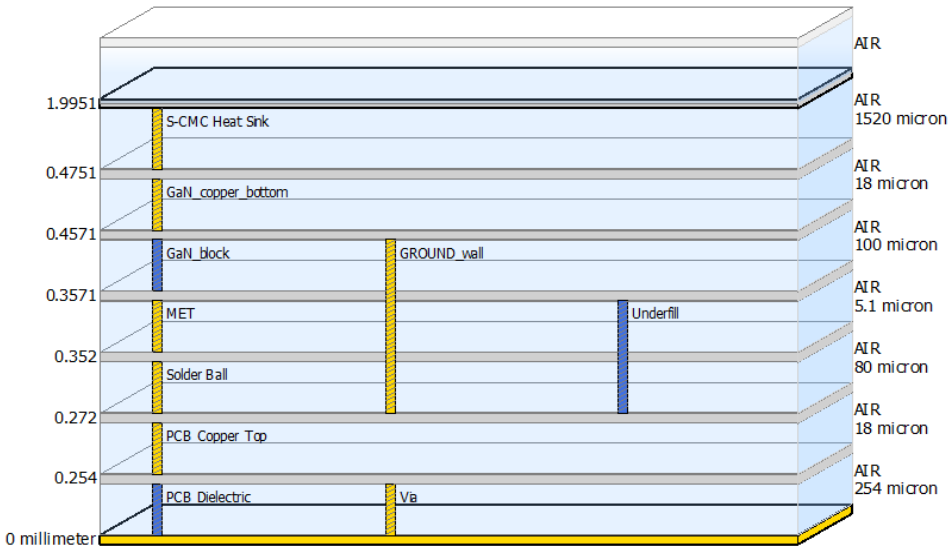
To model the flip chip package, 3-D FEM simulator of ADS is used in this work. The bare die transistor is replaced by GaN dielectric block to prevent disturbing electromagnetic behavior. On top of the GaN dielectric block, metal areas are replaced with gate and drain pads of the bare die transistor. Internal ports are placed at the edges of the metal areas. Bumps are placed at the bottom of metal areas to connect with PCB metals. External ports are placed at the edge of the flip chip package. As a result of FEM simulations, an S-parameter matrix is obtained and the bare die transistor is embedded into it. Thus, the flip chip packaged transistor model is obtained.

4.2.2.1 Lay-out

Modeling process starts with lay-out generation, which is composed of defining the stack-up and assigning ports.

4.2.2.1.1 Defining Stack-up

Stack-up definition, which consists of metal layers, dielectric materials and ground planes of package as seen in Figure 4.3, is an important part of lay-out design process.



Substrate Layer Stackup

	Type	Name	Material	Thickness
	Dielectric		AIR	
	Dielectric		AIR	1520 um
	Dielectric		AIR	18 um
	Dielectric		AIR	100 um
	Dielectric		AIR	5.1 um
	Dielectric		AIR	80 um
	Dielectric		AIR	18 um
	Dielectric		AIR	254 um
	Cover		PERFECT_CONDU...	0 um

Figure 4.3: Defined Stack-up of Flip Chip Package

4.2.2.1.2 Assigning Ports

Second process of the lay-out creation is assigning internal and external ports. Internal ports are assigned at the end of each metal areas. External ports are assigned at the gate and drain edges of the flip chip package, as seen in Figure 4.4.

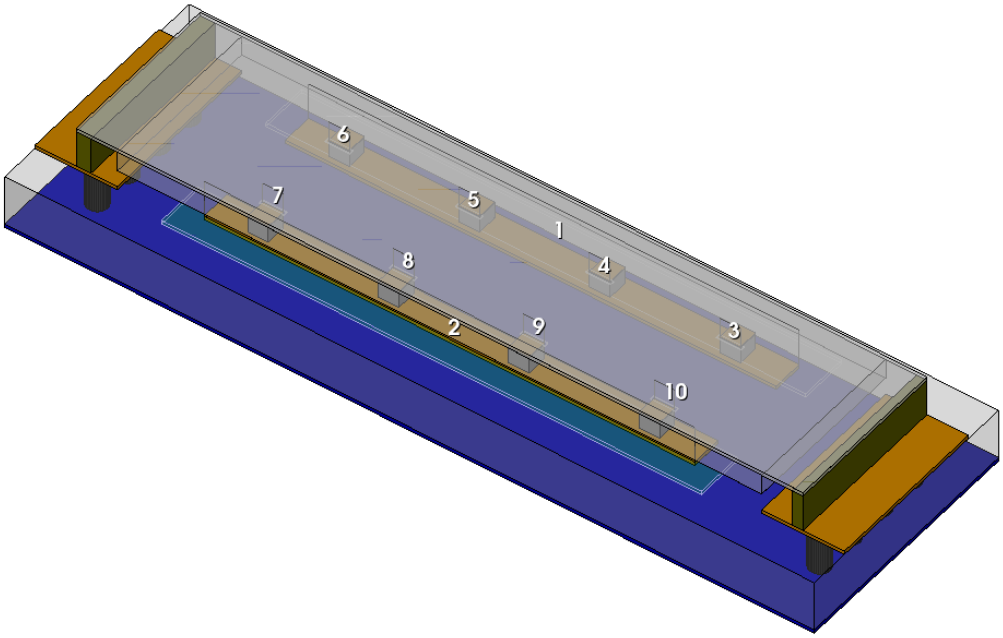


Figure 4.4: Assigned Ports

4.2.2.2 Simulation

Simulation frequency range is chosen up to 20 GHz, in order to include 2nd and 3rd harmonic behaviour of the package. Mesh frequency is chosen as 20 GHz. Resonant frequency of the flip chip package is obtained at 14.10 GHz, as shown in Figure 4.5. Resonant frequency of the air cavity ceramic package is approximately 6.4 GHz. As expected, resonant frequency of the flip chip package occurs at a higher frequency. This means that flip chip package can be used until approximately 10 GHz wihout affecting performance of bare die transistor.

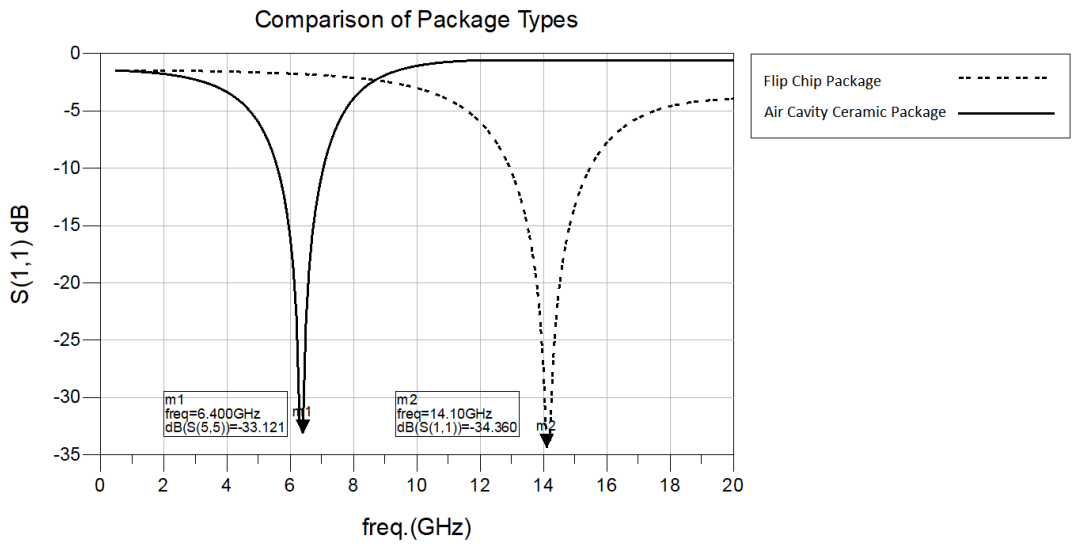


Figure 4.5: Comparison of Resonant Frequencies of Packages Types

4.2.3 Comparison of Package Models

Comparison of input impedances of the air cavity ceramic package and the flip chip package are given in Table 4.1.

Table 4.1: Input Impedance Comparison of Package Types

Frequency (GHz)	Input Impedance of the Flip Chip Package (Ω)	Input Impedance of the Air Cavity Ceramic Package (Ω)
0.5	2.01-9.38j	2.24-8.72j
4.0	0.71-0.25j	2.12+16.47j
6.0	0.52+1.15j	268.90+115.92j

Package parasitics are more effective at high frequency levels as seen in Figure 4.6.

Thus, high frequency amplifier design is not possible by using the air cavity ceramic package.

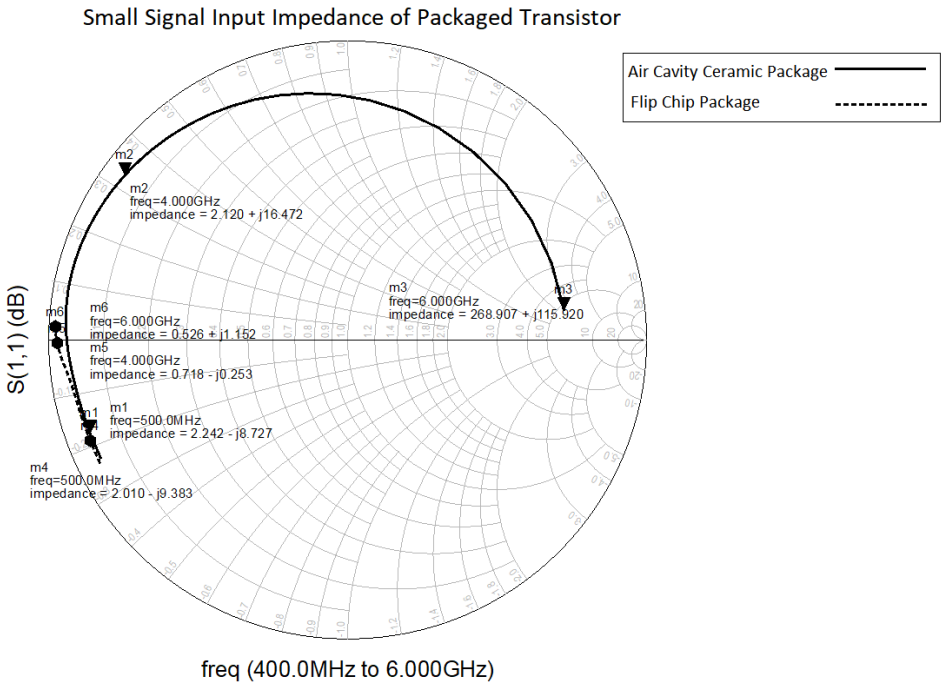


Figure 4.6: Comparison of Input Impedances of Package Types

Small signal gain and output power of the packaged transistors with perfect matched input and output circuitries at 4 GHz are compared in Figure 4.7 and Figure 4.8, respectively. Although input and output of the air cavity packaged transistor are perfectly matched to 50 Ω, the small signal gain of it is maximum 14.3 dB which is 3.7 dB lower than the flip chip packaged transistor. Also, the output power of the air cavity packaged transistor is about 46.5 W at 4 GHz, which is 46 W lower than that of the flip chip packaged transistor.

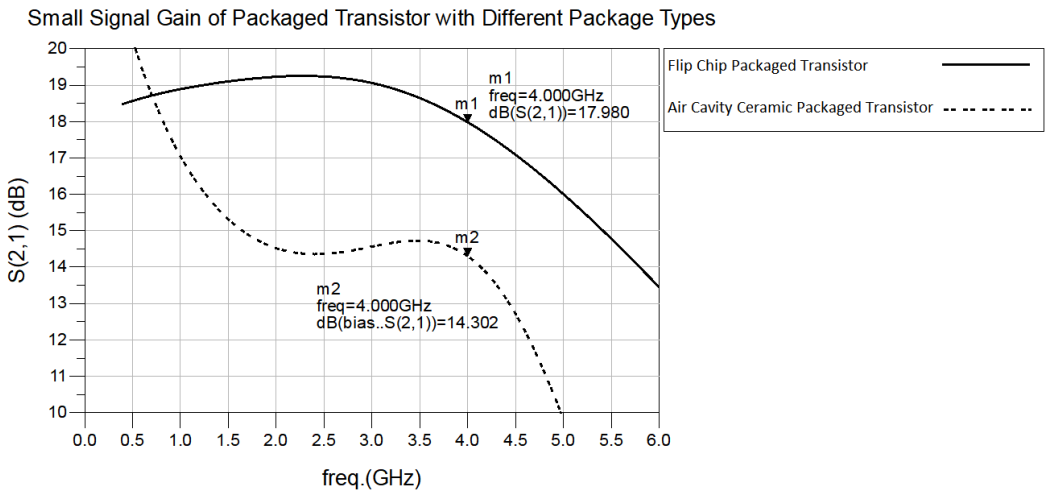


Figure 4.7: Comparison of Small Signal Gain of Packaged Transistors at 4 GHz

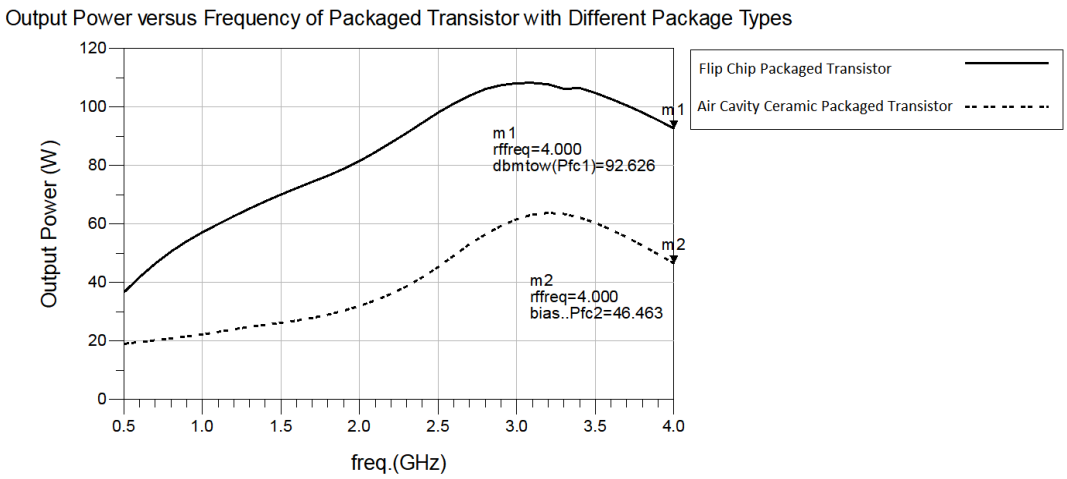


Figure 4.8: Comparison of Output Power of Packaged Transistors at 4 GHz

Small signal gain and output power of the packaged transistors with perfect matched input and output circuitries at 6 GHz are compared in Figure 4.9 and Figure 4.10, respectively. Although the input and output of the air cavity packaged transistor are perfectly matched to 50 Ω, small signal gain of it is maximum 9.85 dB which is 7.35 dB lower than the flip chip packaged transistor. Also, output power of the air cavity packaged transistor is about 24.7 W at 6 GHz which is 50.4 W lower than that of the flip chip packaged transistor.

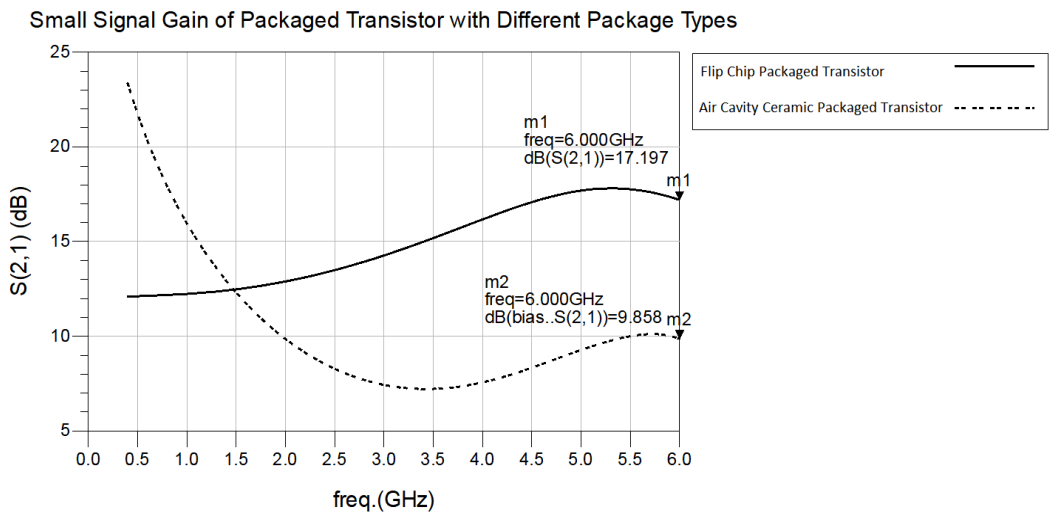


Figure 4.9: Comparison of Output Power of Packaged Transistors at 6 GHz

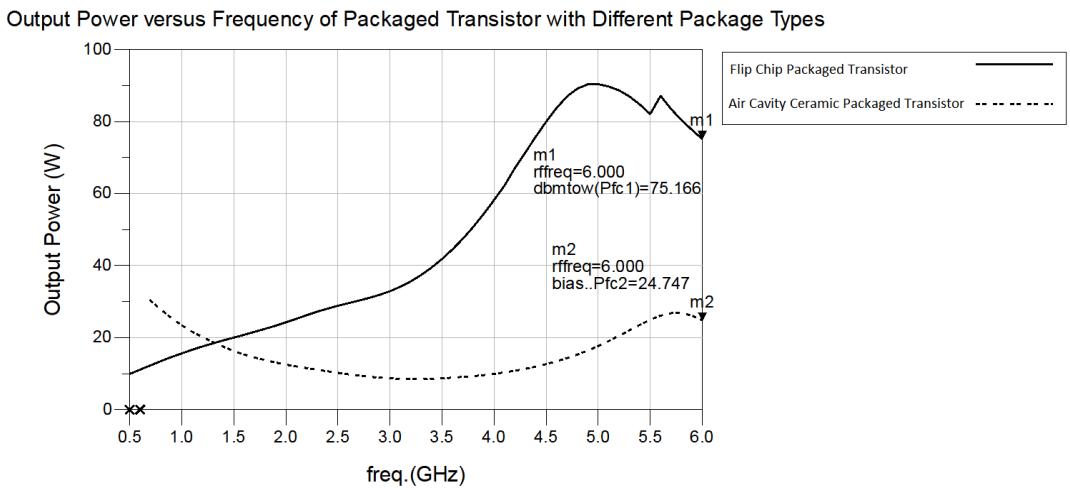


Figure 4.10: Comparison of Small Signal Gain of Packaged Transistors at 6 GHz

4.3 Thermal Modeling

In order to obtain high performance flip chip package transistor, heat transfer should be passed through cold plate, which is attached to the top of the package. In order to calculate the thermal resistance, Equation (2.19) [22] can be used where L is the

width (m), k is the thermal conductivity $\left(\frac{W}{m.K}\right)$ and A is the area (m^2) of the surface to which the heat will be transfered. In order to calculate the temperature difference between the cold plate and the case, Equation (2.20) [20] can be used where Q is the dissipated power (W), R is the thermal resistivity $\left(\frac{°C}{W}\right)$ and ΔT is the temperature difference (°C).

4.3.1 Thermal Model Description

The bare die transistor is attached with C4 bumps to the top of the S-CMC block, which is used as a heat sink. S-CMC block is attached to the Al Module with screws. Temperature of top of Al module remains stable at 30 °C. Thermal model stack-up is prepared as seen in Figure 4.11. Thermal properties of materials and their dimensions are listed in Table 4.2.

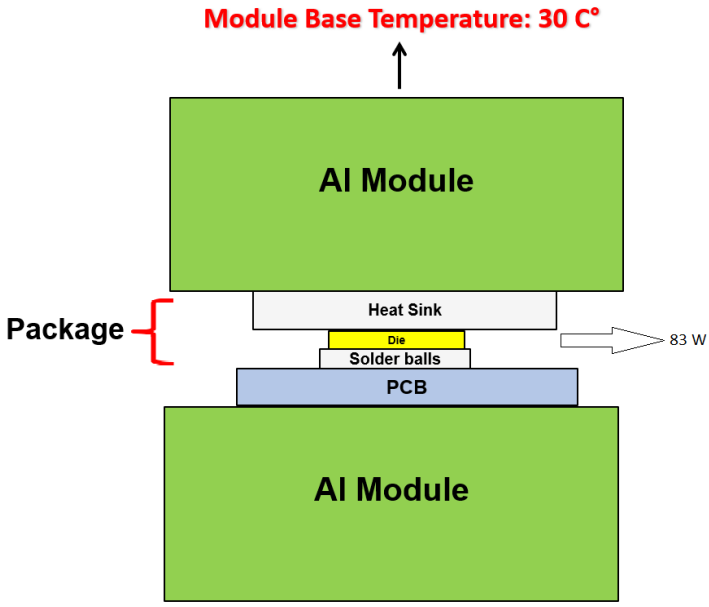


Figure 4.11 : Flip Chip Package Thermal Stack-Up

Table 4.2: Material Properties of Flip Chip Package

Layer	Material	Dimension (m^2)	Thickness (m)	Thermal Conductivity $\left(\frac{W}{m.K}\right)$
Al Module	Aluminum	1.04×10^{-3}	5.00×10^{-3}	180.00
S-CMC	Composite	1.72×10^{-5}	1.57×10^{-3}	301.80
Bumps	Cu	NA	NA	394

4.3.2 Calculation and Simulation Comparison

Large signal test results of the designed amplifier using flip chip package transistor is shown in Table C. Maximum dissipated power which is spread as heat to the ambient is 83 W.

Thermal resistances of layers are calculated in Table 4.3.

Table 4.3: Thermal Resistance of Layers

Layer	Dimension (m^2)	Thickness (m)	Resistance $\left(\frac{°C}{W}\right)$	Temperature (°C)
Al Modul	1.04×10^{-3}	5.00×10^{-3}	2.67×10^{-2}	32.90
S-CMC	1.72×10^{-5}	1.57×10^{-3}	2.92×10^{-1}	57.96

To create thermal model of the air cavity ceramic package and simulate thermal characteristics of it, HFSS-ICEPACK program is used in order to compare calculation and simulation results. Because all heat transfer is performed through source back-vias of the bare die transistor, there is no help of bumps and bottom Al module to heat transfer. Thus, all heat transfer is performed through the S-CMC heat sink and the top Al Module.

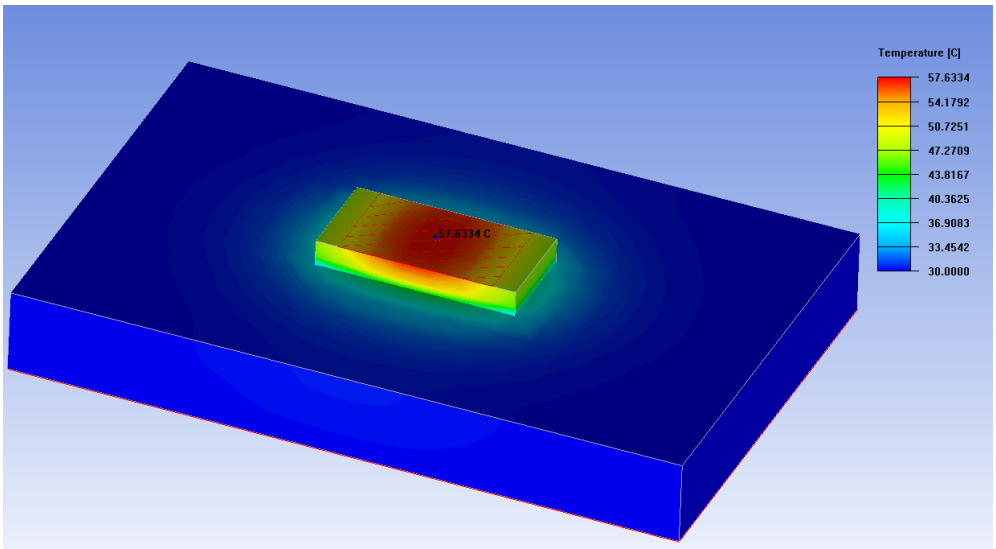


Figure 4.12: Simulation Result of Package

As seen in Figure 4.12, S-CMC heat sink temperature is calculated by program as 57.63 °C, which is close to the analytical calculation of it 57.96 °C in Table 4.3.

The bare die transistor can safely operate with a maximum junction temperature of 225°C [8]. It is known that to assess the overall thermal performance of the flip chip package, the junction temperature should be calculated. Junction to case thermal resistance for the die only is 1.66 $\frac{°C}{W}$ [8]. Junction temperature of the die transistor can be calculated with Equation (2.21) [22] where T_j is the junction temperature, T_c is the case temperature, R is the junction to case thermal resistance of die and P_d is dissipated power of an amplifier.

$$T_j = T_c + (R \times P_d) \tag{4.1}$$

$$T_j = 195.41°C$$

Junction temperature is calculated as ~196 °C, which is critically close to maximum safety junction temperature 225°C. Thus, base temperature of module can be decreased.

4.4 Amplifier Design and Comparison with Air Cavity Package

0.5-4 GHz broadband high-power amplifier design is targeted to observe the impact of package types on the operating frequency of the packaged transistor. Following specifications are aimed however it is known that because the frequency band widen specifications can be lower than that of amplifier with air cavity ceramic package transistor. Same design procedure is followed with the amplifier design in Chapter 3. Lay-out of the amplifier is obtained as seen in Figure 4.13. The amplifier design with the air cavity packaged transistor and the design with the flip chip package design have same dimensions.

Table 4.4: Power Amplifier Specifications

PARAMETERS	SPECIFICATIONS
Frequency Band	0.5-4 GHz
Output Power	> 50 Watt
Small Signal Gain	> 15 dB
Input Return Loss	< -5 dB
Output Return Loss	< -5 dB
Drain Efficiency	> 40 %

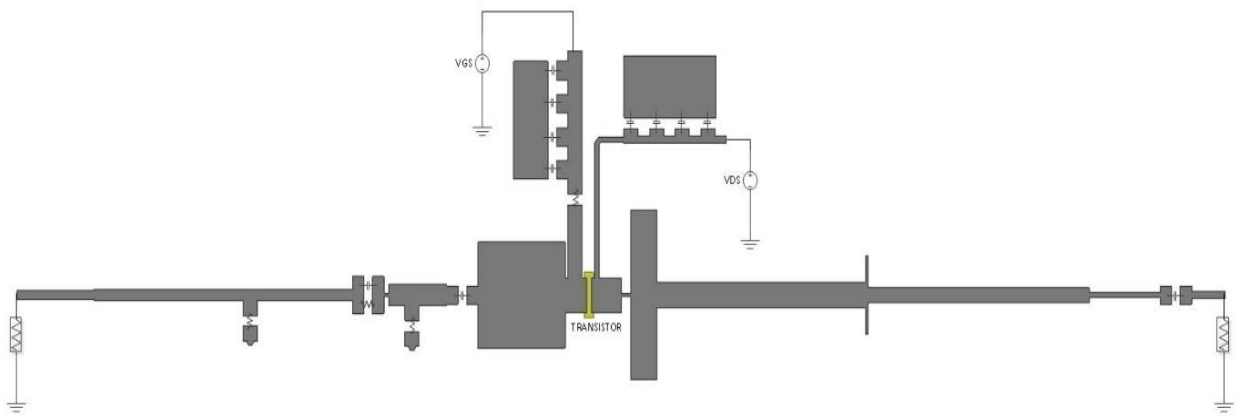


Figure 4.13 : EM Simulated Lay-out of Designed Amplifier with Flip Chip Packaged Transistor

Small signal comparison of the designed amplifiers with different transistor packages are given in Figure 4.14. As seen, the targeted frequency band with the targeted small signal gain is reached by using flip chip packaged transistor. Furthermore, the input and output return loss goals of the amplifier with the flip chip package are achieved, as shown in Figure 4.15 and Figure 4.16.

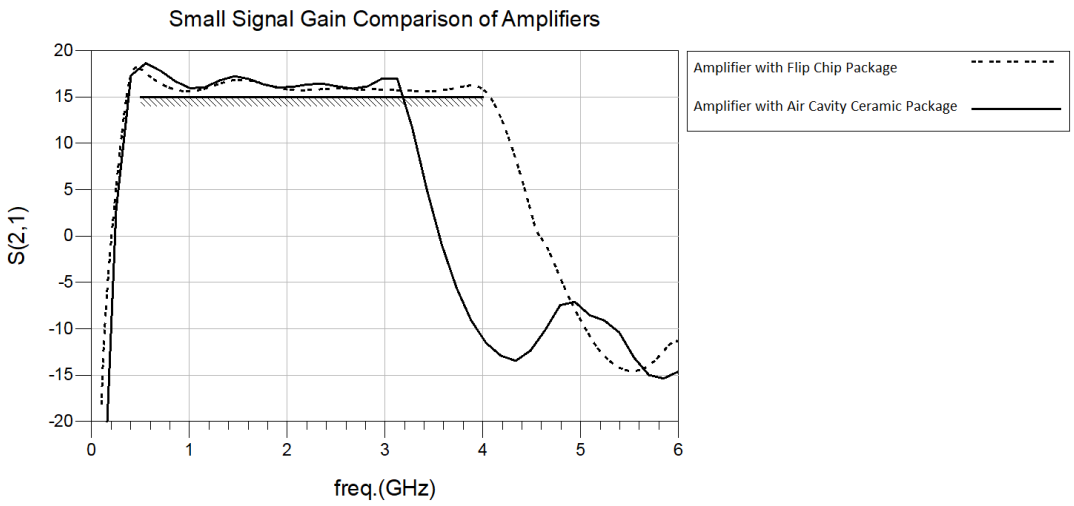


Figure 4.14:Small Signal Gain Comparison of Amplifiers with Different Packaged Transistor

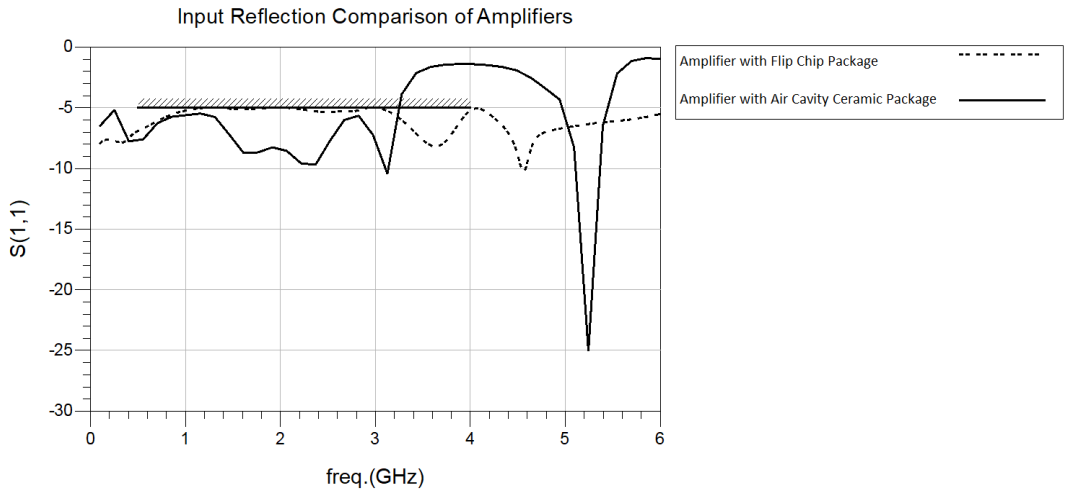


Figure 4.15: Input Return Loss Comparison of Amplifiers with Different Packaged Transistor

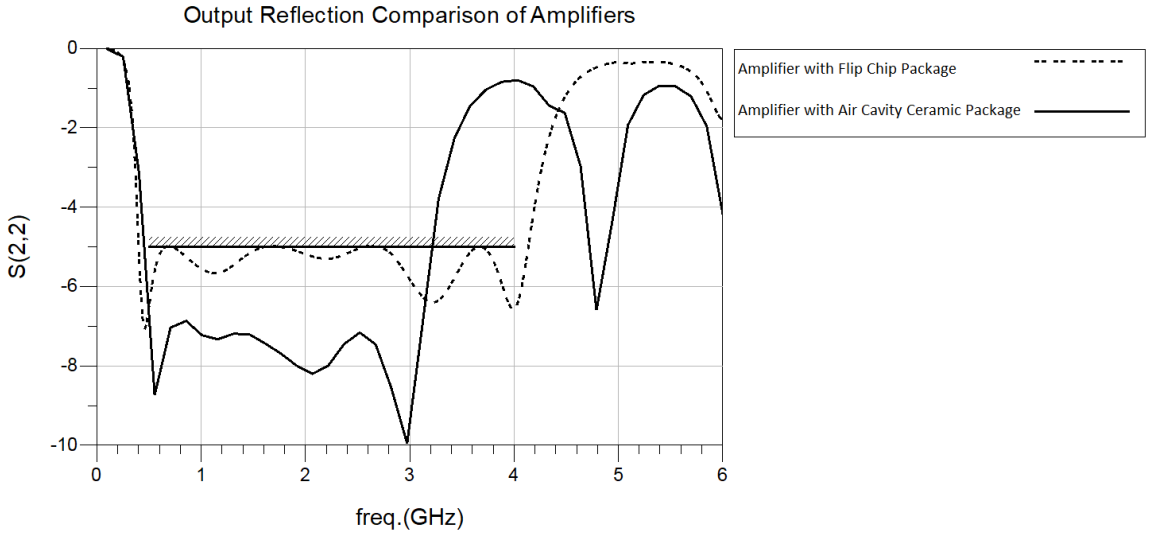


Figure 4.16: Output Return Loss Comparison of Amplifiers with Different Packaged Transistor

Output power and efficiency comparison of the power amplifiers with different package types are given in Figure 4.17 and Figure 4.18. More than 50 W of output power target is achieved with the flip chip packaged transistor. Also, 40 % of efficiency target is reached except for some frequencies.

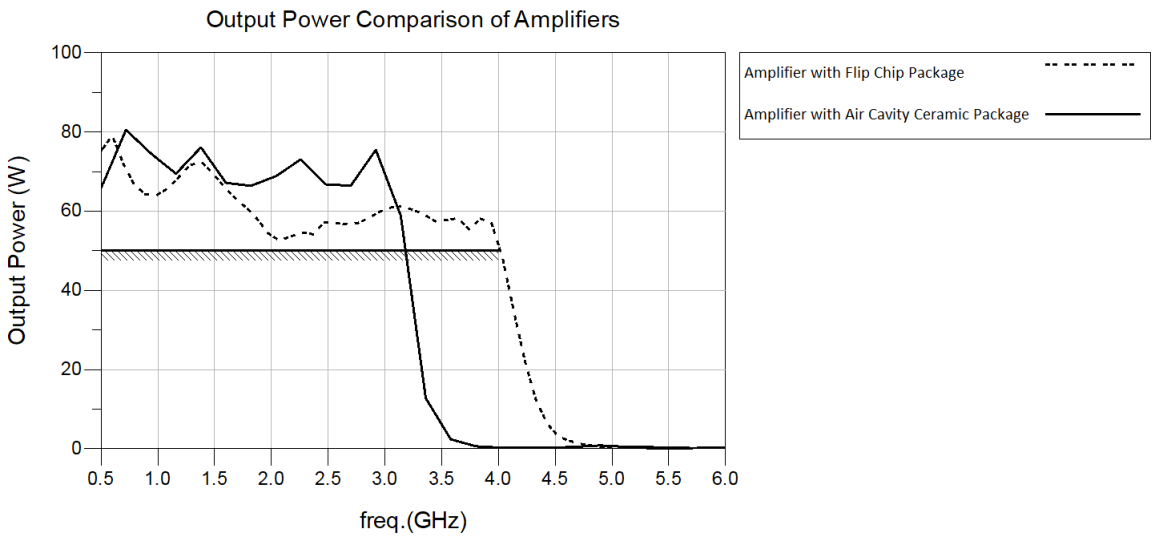


Figure 4.17: Output Power Comparison of Amplifiers with Different Packaged Transistor

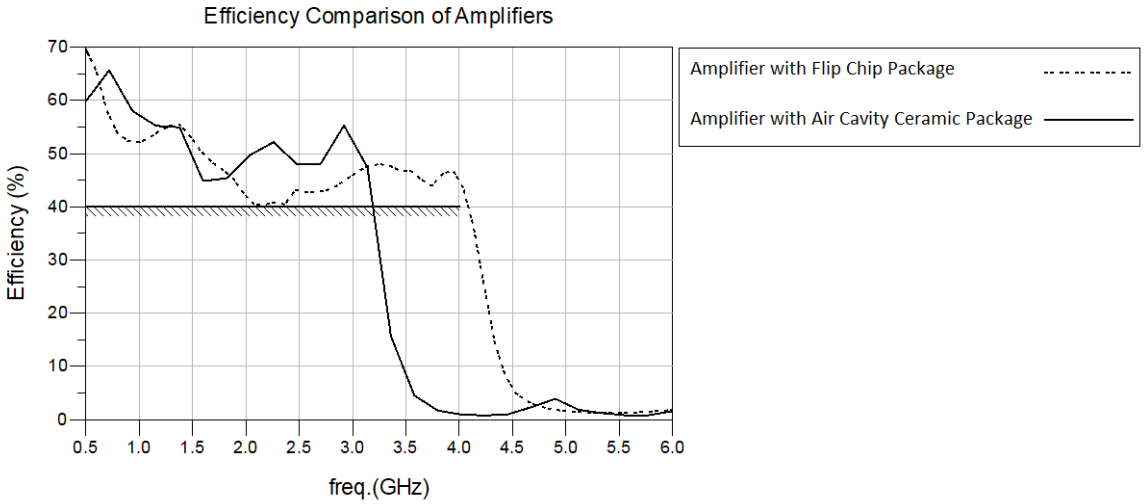


Figure 4.18: Efficiency Comparison of Amplifiers with Different Packaged Transistor

CHAPTER 5

CONCLUSION

In this work, an air cavity ceramic package is partially designed, modeled, manufactured and embedded in a broadband high-power amplifier design. The designed amplifier is tested and the modeling results are verified by measurements. The work is started by designing the package according to the bare die transistor specifications and manufacturing tolerances. In order to use packaged transistor in an amplifier design, there is a need for modeling. To model the designed air cavity ceramic package, two different modeling methods are suggested. The first one is the lumped element model which is based on analytical equations. By using analytical equations, lumped element values for the bond wire inductance and pad capacitance are calculated and a complete lumped element model of the package is obtained. At first, the inductance of a single bond wire is obtained. Secondly, the mutual inductances between all neighboring bond wire are calculated with the derived equation. Capacitive effect of landing pads is calculated and added to the complete model. At last, lumped element equivalent model of the leads of the package is obtained and all values are calculated. At the end of the modeling process, equivalent circuits of all parts of the package are combined and complete model is obtained. The second modeling method is based on 3-D FEM simulations by using ADS tool. To create this model, there is a need of high-performance simulation tool which takes some time to simulate whole complex structure. The first step of this modeling method is creating the bond wire profile. Secondly, a stack-up and 3-D layout of the package are created. After port assignment, simulation steps are defined. As a result of 3-D FEM simulation, small signal parameters are obtained.

After creating two different models, nonlinear bare die transistor model which is supplied by the manufacturer is embedded in the models and packaged transistor models are obtained. The second modeling method is safer because it is a well-known and a more used method among transistor manufacturers. Thus, to check the reliability of the first modeling method, the results of the two modeling methodologies are compared. The comparisons show that there is a very good agreement between the analytical and full-wave models. Furthermore, the designed package is fabricated and utilized in a PA design. Since the packaged transistor is a nonlinear device, there is a need to design an amplifier to test the packaged transistor. For this purpose, a broadband high-power amplifier is designed in the 0.5-3 GHz frequency range. Broadband design is preferred to observe the response of the packaged transistor over a wide frequency range. PA design process starts with the selection of specifications according to the bare die transistor features. Then, substrate material is chosen and characterized. Class of amplifier is selected and bias point analysis is performed for the chosen class. Bias circuit and matching circuit design and stability analysis are performed step by step. At last, designed amplifier is fabricated and tested. Thus, verification of the suggested models is done and comparison between simulations and measurements are reported. Furthermore, the thermal model of the designed package is created and thermal analysis is performed by using the dissipated power of the designed amplifier. Lastly, as a future work, a new package model is suggested to minimize parasitic effects of large dimension RF packages. Electrical and thermal models of the package are created with the ADS software. Then, an amplifier with extended frequency band (0.5-4 GHz) is designed and compared with the amplifier which is designed with air cavity ceramic packaged transistor.

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APPENDICES

A. Test Results of Amplifier Design with Air Cavity Ceramic Package Transistor

Table A: Large Signal Test Results of Amplifier Design (with Packaged Transistor Sample-1)

Freq. (GHz)	PA Output Power (dBm)	PA Output Power (W)	PA Efficiency (%)	PA V_{DD} (V)	PA I_{DD} (A)	50V DC Supply (W)	PA Loss (W)
0.5	47.67	58.47	54.73	50.00	2.13	106.85	48.37
0.6	48.42	69.50	64.65	50.00	2.15	107.50	37.99
0.7	48.73	74.64	64.65	50.00	2.30	115.45	40.80
0.8	48.68	73.79	61.11	50.00	2.41	120.75	46.95
0.9	48.38	68.86	57.74	50.00	2.38	119.25	50.38
1.0	48.12	64.87	55.68	50.00	2.33	116.50	51.62
1.1	47.84	60.81	53.18	50.00	2.28	114.35	53.53
1.2	47.87	61.23	52.09	50.00	2.35	117.55	56.31
1.3	48.09	64.41	52.56	50.00	2.45	122.55	58.13
1.4	48.00	63.09	50.84	50.00	2.48	124.10	61.00
1.5	47.70	58.88	47.37	50.00	2.48	124.30	65.41
1.6	47.51	56.36	44.55	50.00	2.53	126.50	70.13
1.7	47.48	55.97	45.25	50.00	2.47	123.70	67.72
1.8	47.43	55.33	45.67	50.00	2.42	121.15	65.81
1.9	47.21	52.60	44.90	50.00	2.34	117.15	64.54
2.0	47.41	55.10	48.57	50.00	2.26	113.45	58.34
2.1	48.04	63.67	52.62	50.00	2.42	121.00	57.32
2.2	48.22	66.37	53.61	50.00	2.47	123.80	57.42
2.3	48.18	65.76	52.76	50.00	2.49	124.65	58.88
2.4	47.97	62.66	50.86	50.00	2.46	123.20	60.53

2.5	47.77	59.84	49.43	50.00	2.42	121.05	61.20
2.6	47.72	59.15	49.19	50.00	2.40	120.25	61.09
2.7	47.90	61.65	50.66	50.00	2.43	121.70	60.04
2.8	48.24	66.68	53.62	50.00	2.48	124.35	57.66
2.9	48.11	64.71	54.01	50.00	2.39	119.80	55.08
3.0	48.83	76.38	65.64	50.00	2.36	118.15	41.76

Table B: Large Signal Test Results of Amplifier Design (with Packaged Transistor Sample-2)

Freq. (GHz)	PA Output Power (dBm)	PA Output Power (W)	PA Efficiency (%)	PA V_{DD} (V)	PA I_{DD} (A)	50V DC Supply (W)	PA Loss (W)
0.5	47.53	56.62	54.73	50.00	2.15	107.50	50.87
0.6	48.45	69.98	64.65	50.00	2.15	107.50	37.51
0.7	48.68	73.79	64.65	50.00	2.32	116.00	42.20
0.8	48.68	73.79	61.11	50.00	2.42	121.00	47.20
0.9	48.42	69.50	57.74	50.00	2.40	120.00	50.49
1.0	48.00	63.09	55.68	50.00	2.28	114.00	50.90
1.1	47.78	59.98	53.18	50.00	2.28	114.00	54.02
1.2	47.92	61.94	52.09	50.00	2.36	118.00	56.05
1.3	47.95	62.37	52.56	50.00	2.46	123.00	60.62
1.4	48.05	63.82	50.84	50.00	2.47	123.75	59.92
1.5	47.65	58.21	47.37	50.00	2.47	123.90	65.68
1.6	47.45	55.59	44.55	50.00	2.50	125.00	69.40
1.7	47.52	56.49	45.25	50.00	2.45	122.50	66.00
1.8	47.35	54.32	45.67	50.00	2.45	122.50	68.17
1.9	47.15	51.88	44.90	50.00	2.35	117.50	65.61

2.0	47.38	54.70	48.57	50.00	2.27	113.50	58.79
2.1	48.10	64.56	52.62	50.00	2.38	119.00	54.43
2.2	48.20	66.06	53.61	50.00	2.48	124.25	58.18
2.3	48.22	66.37	52.76	50.00	2.52	126.00	59.62
2.4	47.89	61.51	50.86	50.00	2.45	122.50	60.98
2.5	47.65	58.21	49.43	50.00	2.40	120.00	61.78
2.6	47.82	60.53	49.19	50.00	2.42	121.00	60.46
2.7	47.85	60.95	50.66	50.00	2.45	122.50	61.54
2.8	48.20	66.07	53.62	50.00	2.52	126.00	59.93
2.9	48.15	65.31	54.01	50.00	2.38	119.00	53.68
3.0	48.75	74.98	65.64	50.00	2.37	118.50	43.51

B. Simulation Results of Amplifier Design with Flip Chip Package Transistor

Table C: Large Signal Simulation Results of Amplifier Design with Flip Chip Package Model

Freq. (GHz)	PA Output Power (dBm)	PA Output Power (W)	PA Efficiency (%)	PA Loss (W)
0.5	48.76	75.19	68.62	34.38
0.6	48.98	79.12	64.61	43.32
0.7	48.57	72.01	57.13	54.02
0.8	48.23	66.58	52.92	59.22
0.9	48.07	64.25	51.36	60.83
1.0	48.06	64.06	51.11	61.27
1.1	48.18	65.76	51.82	61.13
1.2	48.36	68.69	53.23	60.34
1.3	48.55	71.64	54.16	60.61
1.4	48.59	72.42	54.41	60.68

1.5	48.42	69.59	52.15	63.85
1.6	48.21	66.32	49.42	67.86
1.7	48.02	63.40	47.46	70.17
1.8	48.84	60.93	46.05	71.38
1.9	48.63	58.03	44.50	72.36
2.0	47.35	54.40	41.72	75.98
2.1	47.20	52.57	39.51	80.48
2.2	47.29	53.60	39.35	82.60
2.3	47.37	54.61	39.85	82.40
2.4	47.34	54.20	39.43	83.22
2.5	47.56	57.13	42.15	78.40
2.6	47.55	56.93	41.78	79.32
2.7	47.54	56.78	41.76	79.17
2.8	47.55	56.95	42.12	78.25
2.9	47.65	58.27	42.98	77.31
3.0	47.77	59.89	44.33	75.21
3.1	47.84	60.93	45.66	72.50
3.2	47.86	61.16	46.67	69.87
3.3	47.80	60.32	46.97	68.09
3.4	47.71	59.1	46.74	67.34
3.5	47.58	57.38	45.73	68.08
3.6	47.61	57.75	45.75	68.47
3.7	47.65	58.22	44.149	73.65
3.8	47.43	55.36	42.91	73.63
3.9	47.64	58.11	45.07	70.82
4.0	47.57	57.16	45.94	67.24