Al-Ge EUTECTIC BONDING FOR WAFER-LEVEL VACUUM PACKAGING OF MEMS DEVICES

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ABSTRACT

AL-GE EUTECTIC BONDING FOR WAFER-LEVEL VACUUM PACKAGING OF MEMS DEVICES

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Packaging is one of the most critical processes regarding the commercialization of MEMS devices. Wafer-level packaging is both yield and cost-efficient compared to die-level packaging. Various MEMS-based devices require vacuum encapsulation, such as microbolometers and resonators.

Among other bonding methods and alloy systems used for wafer-level packaging, the Al-Ge system is advantageous since it can bond wafers by coating all the metallic layers on a single wafer. This eliminates the need for additional process steps on the device wafer. On the other hand, the limitation of the system is that the eutectic melting point (425 °C) is close to the CMOS process temperature limit (450 °C), which restricts the use of Al-Ge in critical CMOS-based applications. In this regard, the applicability of Al-Ge eutectic alloys for vacuum encapsulation of microbolometers through wafer-level packaging has been studied in this thesis study.

Throughout this study, the suitability of thermally evaporated and co-sputtered Al-Ge alloys has been examined in detail. Bonding performance after both methods appeared poorly. Results of annealing experiments indicated that the poor performance is due to sluggish diffusion between Al and Ge. Al-Ge layer stack has

been coated on a single wafer using thermal evaporation and sputtering. The microstructural evolution of the layer stack has been examined in detail after annealing and bonding experiments to devise an optimum bonding procedure with the minimum eutectic bonding temperature. A eutectic bonding procedure with a solid-state bonding step at 400 °C has been compared with a traditional eutectic bonding procedure, the former of which has performed better. The vacuum level inside the packages has been characterized using cap deflection test. Vacuum packaging has been achieved using both thermal evaporation and sputtering. In pursuing the lowest possible eutectic bonding temperatures, a successful vacuum sealing with 27 MPa average shear strength was performed at 435 °C, and 51 MPa average shear strength was obtained at 440 °C.

Keywords: Wafer-Level Packaging, Al-Ge alloy, Eutectic Bonding, MEMS Packaging, Vacuum Packaging

ÖZ

MEMS AYGITLARININ AL-GE ÖTEKTİK BAĞLAMA YÖNTEMİ İLE DİSK SEVİYESİNDE VAKUM PAKETLENMESİ

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Ağustos 2022, 85 sayfa

Paketleme, MEMS tabanlı aygıtların ticarileştirilebilmesi için önemli bir konudur. Disk seviyesi paketleme yöntemleri, aygıt seviyesi yöntemlere kıyasla hem düşük maliyetli hem de yüksek verimlidir. Mikrobolometreler ve rezonatörler gibi çok sayıda MEMS aygıtının çalışabilmesi için vakum ortamında paketlenmesi gerekmektedir.

Al-Ge alaşımının diğer yöntem ve alaşımlara kıyasla en önemli avantajı, bağlayıcı katman gerektirmediği için iki metalin tek disk üzerine üst üste kaplanarak disk bağlama işleminin yapılabilmesidir. Bu sayede aygıtların bulunduğu disklere herhangi bir üretim adımı eklenmeden disk seviyesinde paketleme işlemi yapılabilmektedir. Fakat ötektik erime noktasının (425 °C) CMOS disklerin sıcaklık limitine (450 °C) yakın olması Al-Ge alaşımının CMOS disk içeren uygulamalarda kullanımını kısıtlamaktadır. Bu bağlamda, Al-Ge alaşımının mikrobolometrelerin disk seviyesinde paketleme işlemine uygunluğu değerlendirilmiştir.

Bu çalışmada termal buharlaştırma ve eş zamanlı saçtırma yöntemleri kullanılarak kaplanmış Al-Ge alaşımları ile disk bağlama deneyleri yapılmıştır. Yapılan disk

bağlama deneyleri sonucunda iki yöntemle elde edilen kaplamalarla da başarılı bir şekilde vakum paketleme işlemi gerçekleştirilememişti. Bu metallere yapılan ısıl işlem deneylerinin sonucunda düşük performanslarının kaplama yöntemlerinden kaynaklı yavaş difüzyon mekanizmasına bağlı olduğu belirlenmiştir.

Hem termal buharlaştırma hem de saçtırma yöntemleri ile Al ve Ge'nin tek diske üst üste kaplanmıştır. Mümkün olan en düşük bağlama sıcaklığına sahip disk bağlama prosedürünü geliştirebilmek için, disk bağlama ve ısıl işlem deneylerinin ardından katman yığınının iç yapısal gelişimi detaylı bir şekilde incelenmiştir. Ötektik bağlama adımından önce 400 °C katı halde bağlama adımı içeren bir disk bağlama prosedürü, tek adımda ötektik bağlama prosedürü ile karşılaştırılmış ve ilk yöntem daha iyi sonuç vermiştir. Hücrelerin içerisindeki vakum seviyesinin karakterizasyonu kapak bükülme testi ile yapılmıştır. Hem termal buharlaştırma hem de saçtırma yöntemi ile elde edilmiş örnekler ile vakum paketleme işlemi başarılı bir şekilde gerçekleştirilmiştir. Saçtırma yöntemi ile kaplanmış metallerde bağlama sıcaklığı 435 °C'ye düşürülmüş ve ortalama kesme dayancı yaklaşık 27 MPa olarak belirlenmiştir. 440 °C bağlanmış örneklerde ortalama kesme dayancı 51 MPa seviyesine yükselmiştir.

Anahtar Kelimeler: Disk seviyesi paketleme, Al-Ge alaşımı, Ötektik Bağlama, MEMS Paketleme, Vakum Paketleme

To everyone who asks, “It’s for the weather forecast, right?” when I say metallurgy

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CHAPTER 1

INTRODUCTION

1.1 Overview

Micro-Electro-Mechanical Systems (MEMS) are devices fabricated using microfabrication techniques such as thin film deposition, lithography, and etching. A wide range of MEMS-based sensors is used in industry and consumer products[1].

There is a variety of MEMS-based sensors used in daily life. Some examples are motion sensors such as resonant accelerometers and gyroscopes. These sensors are used in smartphones and vehicles for various needs. Figure 1.1 compares the MEMS market value in 2017 and the forecast values for 2023[2].

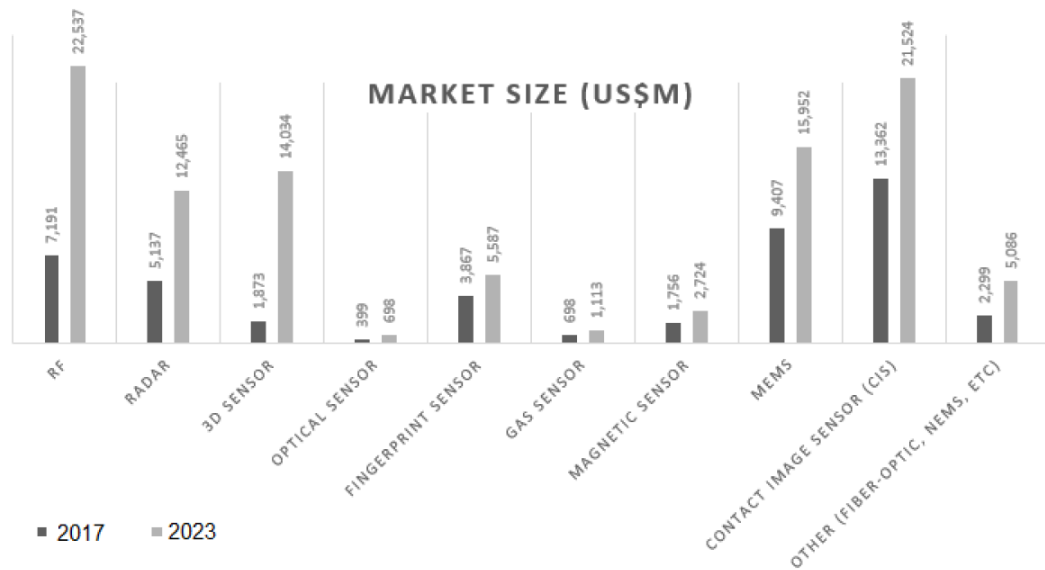


Figure 1.1 Comparison of MEMS market values between 2017 and 2023 forecast

1.1.1 Thesis Overview

The main objective of the thesis is to develop an Al-Ge eutectic bonding procedure at the lowest possible to enable its use for wafer-level packaging of CMOS-based MEMS devices. Al-Ge alloys coated on wafers using co-sputtering and thermal evaporation followed by arc melting are characterized based on their thermal properties, microstructures, and mechanical properties after wafer bonding. The results are compared with samples obtained by coating Ge over Al using thermal evaporation and sputtering.

The organization of the thesis is as follows:

Chapter 1 starts with information about MEMS devices that require vacuum packaging and addresses issues related to vacuum packaging. The main packaging approaches and wafer bonding methods used for wafer-level packaging are explained.

Chapter 2 contains literature review data about Al-Ge alloy properties and their use for various bonding applications, especially for wafer-level packaging.

Chapter 3 describes the experimental procedure. The fabrication and characterization methods used throughout the study are explained in detail. Two different bonding procedures are given, with each step being explained.

Chapter 4 is where the results of the experiments are presented, and the outcomes are discussed. Microstructures, shear strengths, and vacuum packaging performances are mainly compared for co-sputtered and thermally evaporated alloys, and Al/Ge layers stacks obtained using thermal evaporation and sputtering.

Chapter 5 concludes the overall findings of the experiments. Future recommendations for the potential further progress of the study are discussed.

1.2 MEMS Packaging

Packaging is the encapsulation of MEMS devices under proper conditions. It is one of the most critical aspects of the commercialization of products. The increasing demand for MEMS devices entails cost-efficient manufacturing methods. Developing efficient packaging methods is essential since the majority of the production cost in most cases is related to packaging [3]–[5].

The package of a sensor has several significant functions. First, most MEMS devices cannot function under atmospheric conditions because of issues related to their basic working principles. They require particular environments like an inert gas atmosphere or vacuum. Sensors are encapsulated inside the packages under necessary atmospheres. The package is required to provide an interface between the sensor and the outside environment. Finally, the package protects the sensor from environmental effects such as impact, humidity, or dust.

Many MEMS devices require vacuum sealing, for which there are two main reasons. Some resonant sensors, such as gyroscopes or accelerometers, vibrate at high frequencies. They detect motion through the change in capacitance between vibrating plates. Air molecules around the devices damp the vibration and motion of the structures. Hence, such devices are packaged in a vacuum to enhance their responsivity. Microbolometer is another MEMS-based sensor that requires vacuum packaging. They are used for the detection of infrared radiation (IR). The working principle is based on the fact that the active material heats up upon interaction with IR. The active material (VO_x) has a low-temperature coefficient of resistivity (TCR). The data output is received as a change in resistivity. Since IR detection is based on temperature change, thermal isolation of the device is an important issue. It has a bridge-like structure to be thermally isolated from the substrate. The device shall be sealed in a vacuum so the heat loss to the air molecules around the sensor can also be prevented[6]. Figure 1.2 represents a microbolometer and the heat loss mechanism for the gas molecules inside the package.

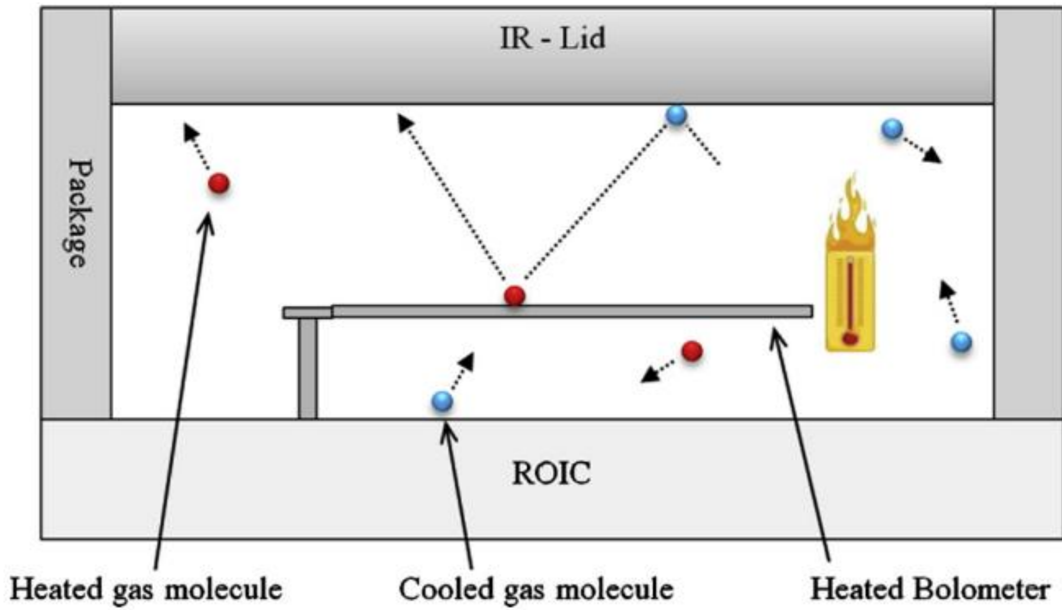


Figure 1.2 Schematic representation of a microbolometer and its heat loss mechanism[7]

The noise equivalent temperature difference (NETD) and image quality changing with the pressure inside the package have been shown in Figure 1.3 by Voronel and Schaefer from Palomar technologies.

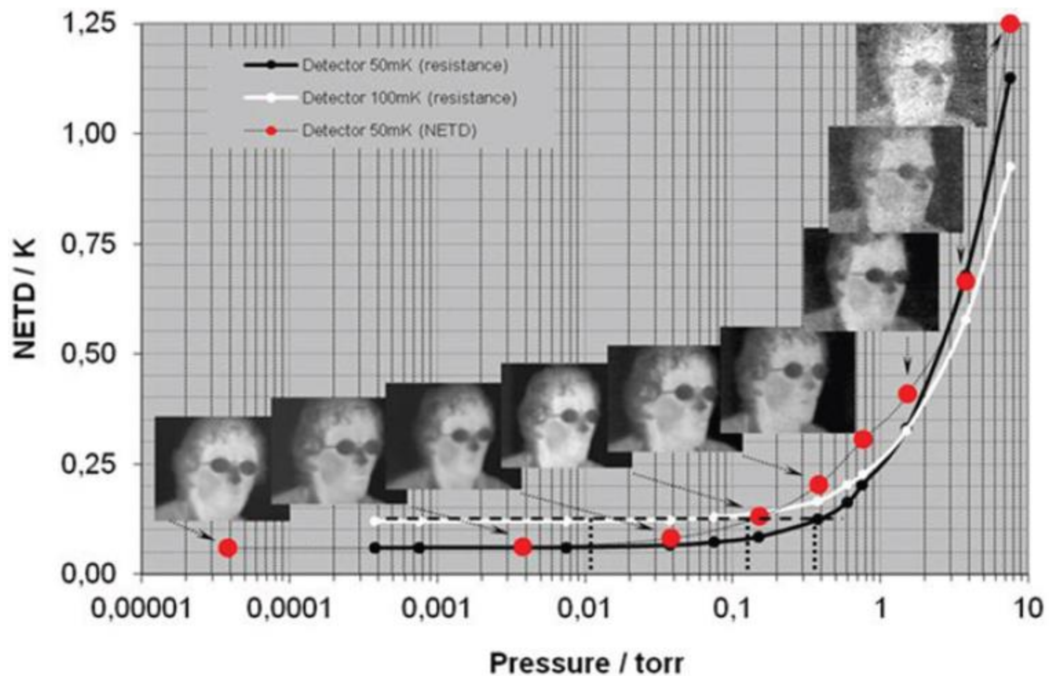


Figure 1.3 NETD and image quality at different pressure levels

1.2.1 Issues Related to Vacuum Packaging

Every MEMS device has different packaging requirements depending on its working principle and design constraints. Packaging constraints for a microbolometer are based on mechanical strength, vacuum level, hermeticity, thermal budget, IR permeability, and getter activation.

The minimum mechanical strength required for an electronic package dictated by MIL-STD-883 is 6 MPa in shear. This limit is for the device to be protected from environmental effects such as impacts and to survive the mechanical effects that occur during dicing[8]. It is measured by loading the package in shear with a suitable setup[9].

The pressure inside the package for the microbolometer shall be 10 mTorr or below for adequate performance. The vacuum level can be measured using pressure-sensitive features inside the package, such as Pirani gauges or a cap deflection method. Impermeability of the package is determined using He leakage test, for which the limitations are also specified by MIL-STD-883 depending on the inner volume of the package[10], [11].

Getter films are used in vacuum packages to enhance or maintain the vacuum level. Gas molecules absorbed into the device or the package walls may diffuse into the package over time. Figure 1.4 shows the increase in pressure in a vacuum cavity over time as a function of volume due to outgassing.

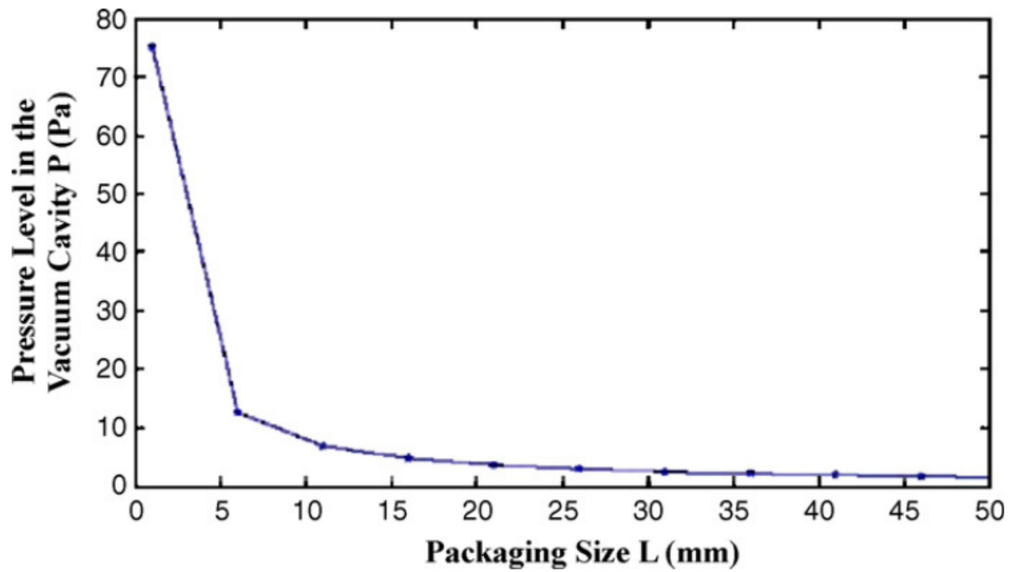


Figure 1.4 Relationship between the package size and pressure caused by desorption[12]

Getters are used to reduce the number of gas molecules within the package. They are made of reactive metals such as Ti, Zr, or V[13]. They naturally have a passive oxide layer on the surface. This passive layer is annihilated by different mechanisms, as shown in Figure 1.5, through heat application, and the film reacts with residual gas molecules inside the package. Depending on the application, the getter film can be activated before, during, or after packaging. For a Ti getter film, a minimum temperature of 400℃ is required for 15 minutes to activate the getter film.

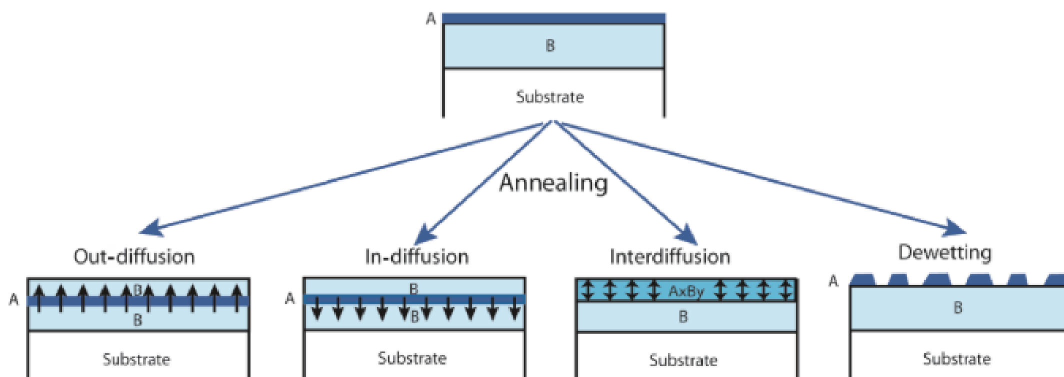


Figure 1.5 Activation mechanisms for getter films[13]

CMOS wafers are reading circuits designed for specific requirements. They are used to manufacture a wide range of MEMS devices, and CMOS compatibility of the

packaging method is an important issue. The most significant limitation caused by CMOS wafers is the thermal budget. Temperatures above 450 °C damage the structures built into the wafer. Hence, the temperature profile shall remain below this temperature during packaging [14], [15].

Finally, the package shall be transparent to wavelengths of 8-12 µm, which is the detection spectrum of microbolometers. The most widely used IR windows are Si and Ge. It should be noted that proper applications of antireflection (AR) coatings are also required for the windows to be functional [16].

1.2.2 Packaging Methods

There are two main approaches to MEMS packaging. The first method is device(die) level packaging. The wafer is diced into single devices. Afterward, the devices are placed inside ceramic or metallic packages and encapsulated in a vacuum. The second method is wafer-level packaging, for which all the devices on one wafer are encapsulated once before dicing. Figure 1.6 is a schematic representation of the device and wafer-level packaging, respectively. Wafer-level packaging is more advantageous than device-level packaging in several aspects. First of all, it is more cost and time-saving to package devices on the wafer l-vel. Mass production using device-level methods leads to high labor and material costs[17].

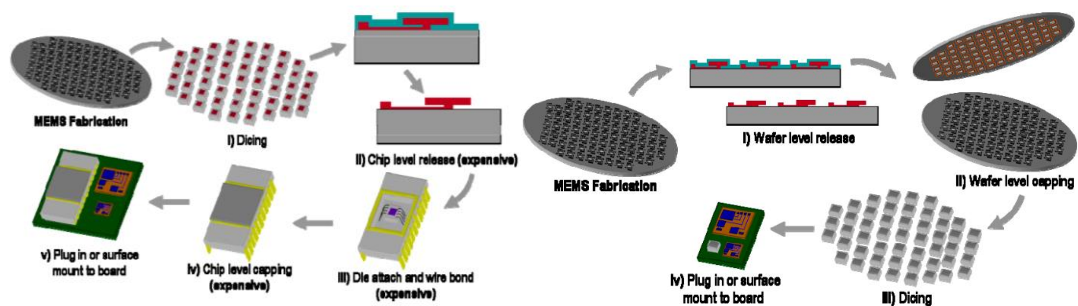


Figure 1.6 Schematic representation of device(left) and wafer(right) level packaging methods

Finally, when the devices are diced before packaging for die-level encapsulation, some of the dies may be damaged or contaminated due to mechanical stresses or particles caused by the dicing saw. The package mechanically protects the devices during dicing, producing a higher production yield.

1.2.3 Wafer-Level Packaging Methods

Thin Film Packaging

A thin film packaging procedure starts with a sacrificial layer around the device. A thin film is coated over the sacrificial layer. There are holes etched on this film through which the sacrificial layer is etched, and a cavity is formed. Afterward, a second film is coated over the thin film to seal the etching holes. Figure 1.7 is a schematic representation of thin film packaging. Another thin film packaging approach is transferred thin film packaging. The thin film is coated on a carrier wafer over a sacrificial layer and bonded to the device wafer. Afterward, the carrier wafer is removed by etching the sacrificial layer. Figure 1.8 is a schematic process flow for this method.

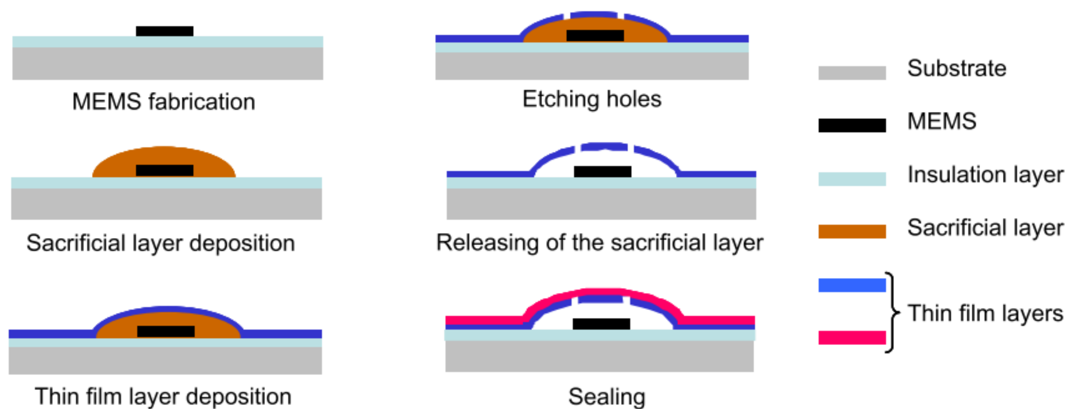


Figure 1.7 Schematic process flow for thin film packaging[18]

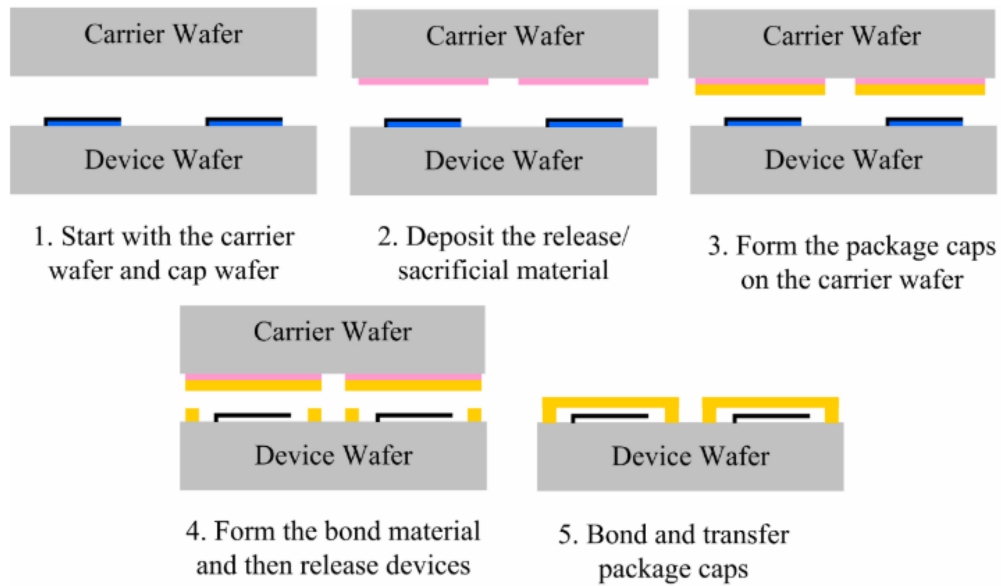


Figure 1.8 Schematic process flow for transferred thin film packaging [17]

Wafer Bonding

Wafer bonding involves the use of a second wafer called the cap wafer. It has cavities formed using chemical or plasma etching. The devices are encapsulated in these cavities using different methods. Figure 1.9 is a generic process for wafer-level packaging using wafer bonding.

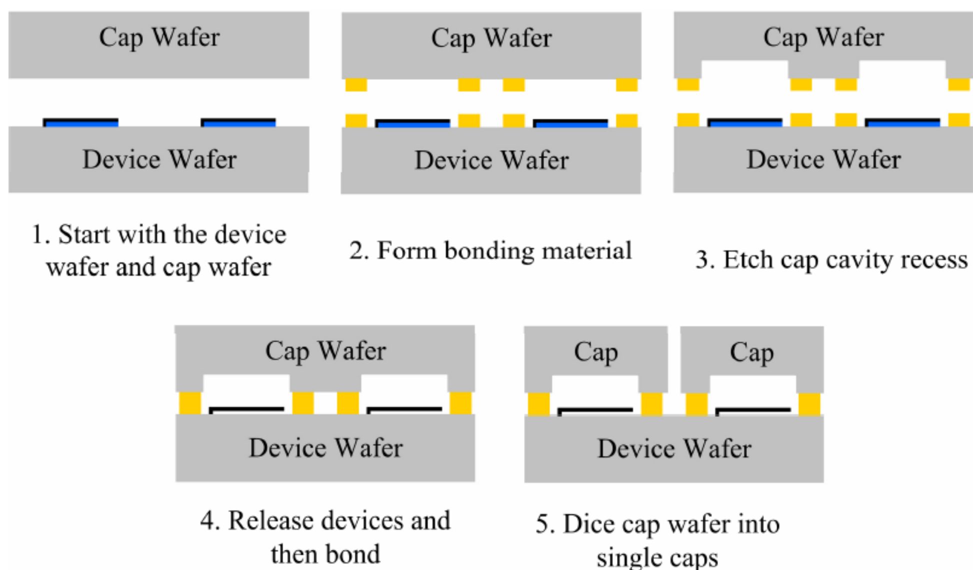


Figure 1.9 Generic process flow for wafer bonding [17]

Fusion Bonding

Fusion bonding is used for bonding wafers directly, without the use of any bonding material. Wafers are heated up to around 1000°C under compression after chemical surface activation. It is possible to decrease the bonding temperature by chemical or plasma activation. It results in reliable bonds with high hermeticity and high-temperature resistance. The most significant limitation of this method is that the bonding surfaces should have extremely low surface roughness for a hermetic bonding procedure [4].

A Si_3N_4/Si_3N_4 direct bonding procedure at 300 °C has been reported by Lo et al. It involves an HF treatment followed by nitrogen plasma activation before bonding[19].

Anodic Bonding

Anodic bonding is another direct bonding method. It is used to bond Na-containing glass wafers to Si wafers. Silicon-glass wafer stack is heated to a temperature between 200-500 ºC, and a high voltage (400-2000V) is applied. Na ions inside the glass migrate away from the silicon wafer, and Si atoms of the wafer form strong covalent bonds with the oxygen ions left behind. Figure 1.10 is the schematic representation of anodic bonding. Anodic bonding also requires highly smooth surfaces since it does not involve filler material. Also, the effect of the high voltage on the device to be packaged shall be considered.

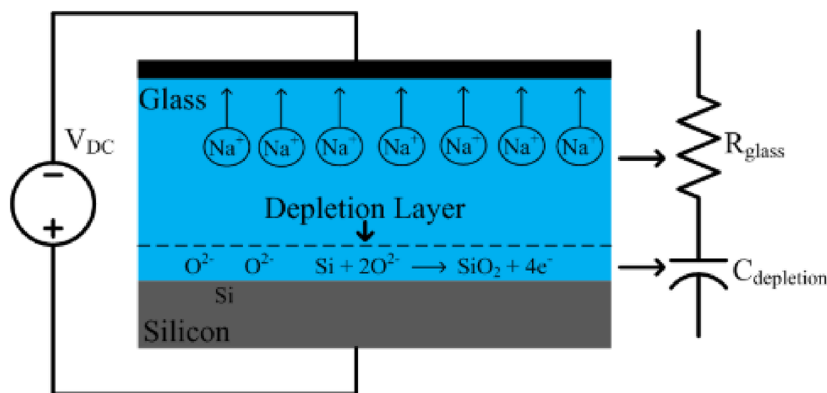


Figure 1.10 Schematic representation of anodic bonding[20]

Glass Frit

Glass frit is a paste mixture that involves binders. Bonding temperatures vary around 450 °C. It transforms into a glass form through heat and bonds the wafers. The frit softens before transforming into a glass. Hence, it is adequate for covering topography. It also results in a strong bond resistant to high temperatures. Finally, being an insulator, glass does not lead to short circuits in the case of lateral electrical feed-throughs. There are two main limitations to the use of glass frit. Firstly, the glass frit contains Pb to keep its melting temperature low, which brings up environmental constraints. Secondly, the minimum feature size possible with current glass frit printing methods cannot be smaller than 100 μm [21].

Thermocompression

Thermocompression involves joining two layers of the same metal at high temperatures under compression. The temperature is high enough for the metals to soften, but it is lower than their melting temperature. Au, Al, and Cu are the most common metals for thermocompression bonding. Bonding temperatures vary according to the used metal, generally around 400°C. It is possible to form hermetic joints using thermocompression. However, it is possible to cover topography using thermocompression. However, it requires high forces since the bonds occur at a solid state [22], [23].

Eutectic & TLP Bonding

Figure 1.11 is a schematic binary eutectic phase diagram. The eutectic composition of a binary alloy usually has the lowest melting point on its phase diagram. The main principle of eutectic bonding is to heat a layer stack of the two components above the eutectic temperature under compression. The two metals diffuse into each other in a solid state. Eventually, the eutectic composition is reached, and a liquid alloy is formed, acting as solder to bond the wafers. Table 1.1 shows the most common alloy systems used for eutectic bonding.

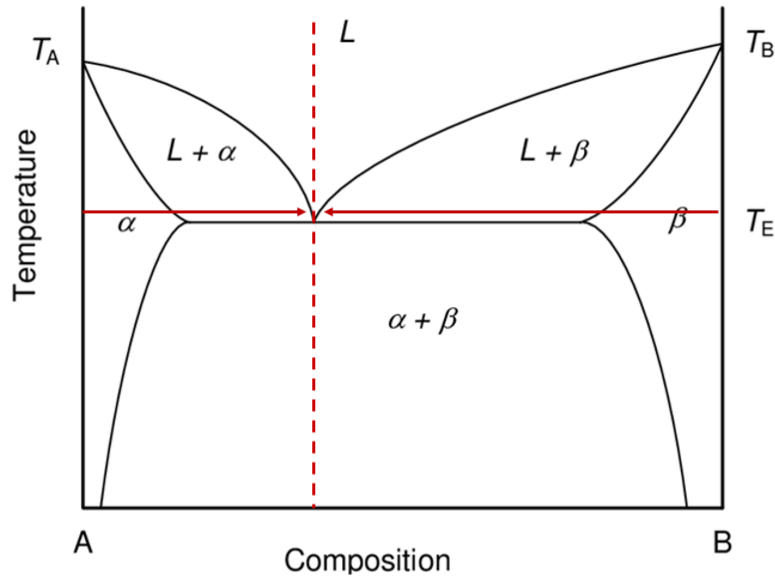


Figure 1.11 A Schematic binary eutectic phase diagram [24]

Table 1.1 Common alloys used in eutectic bonding [25]

Alloy	Eutectic Temperature (°C)
Au-Sn	280
Au-Si	363
Al-Ge	423

The thicknesses of the metallic layers are adjusted to reach the eutectic composition upon mixing. Although the liquid formation is advantageous for covering topography on the surface, some of the liquid metal is squeezed out of the bonding area due to the applied force. An excessive squeeze-out shall be prevented since it may compromise the devices.

TLP (Transient Liquid Phase) or SLID (Solid-Liquid Interdiffusion) bonding is applied for alloy systems that can form intermetallic compounds (IMC). It is based on the same principle as eutectic bonding. However, the target composition is different. After a liquid phase, diffusion continues in the solid state, and IMCs are

formed. The melting temperature of the final composition is higher than the bonding temperature, which is the most significant advantage of TLP bonding. Figure 1.12 is the Au-Sn phase diagram with its target composition[26].

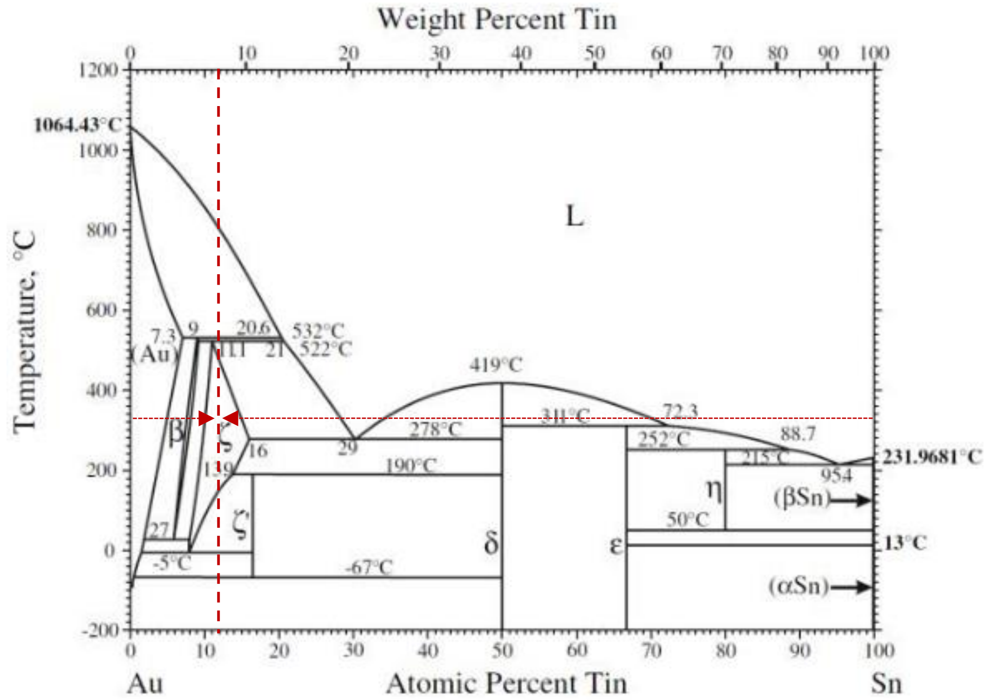


Figure 1.12 Au-Sn Phase diagram[27]

There are several issues related to TLP bonding. First of all, most intermetallic compounds are brittle, which might cause problems related to mechanical properties. Second, solid-state phase transformation may result in Kirkendall voids in the structure and affect the bond integrity [28]. Thirdly, a sufficient amount of liquid formation is of the essence for vacuum sealing. Transient formation of liquid phases shall be considered for an adequate vacuum packaging process. There is a minimum thickness value for the metal to melt, so a sufficient amount of liquid can occur before IMC formation. The value is named critical interlayer thickness [29]. It is calculated based on the equation.

$$h_c = 2h_\delta C_\delta \left(\frac{\rho_{alloy}}{\rho_M}\right)^2 \quad 1.1$$

Table 1.2 shows the alloy systems used for TLP bonding with their bonding and melting temperatures [27], [30].

Table 1.2 TLP alloy systems with bonding and melting temperatures

Alloy	**Bonding Temperature (°C)**	**Melting Temperature (°C)**
Au-Sn	>278 °C	<500 °C
Au-In	>156 °C	~500 °C
Cu-Sn	>232 °C	< 400 °C
Ni-Sn	>232 °C	<900 °C

CHAPTER 2

LITERATURE REVIEW

The Al-Ge phase diagram is shown in Figure 2.1. It has a eutectic melting. Its eutectic composition is at 51.6 wt% (28.8 at%) Ge. The microstructures of the eutectic, hypo-eutectic, and hyper-eutectic alloys are shown in Figure 2.2. Composition shifts from 51.6 wt% Ge in applications due to continuous cooling conditions. At 51.6% composition, Al nucleates and grows as the primary phase. The probability of Ge nucleating as a primary phase occurs at undercooling levels greater than 80 K [31]. Microstructure after differential scanning calorimetry has shown that the microstructure closest to the eutectic point has been obtained at 53 wt% Ge[32]. Although experimental results indicate metastable rhombohedral and monoclinic phase formations, they occur due to significant undercooling at highly hypo-eutectic compositions[33], [34].

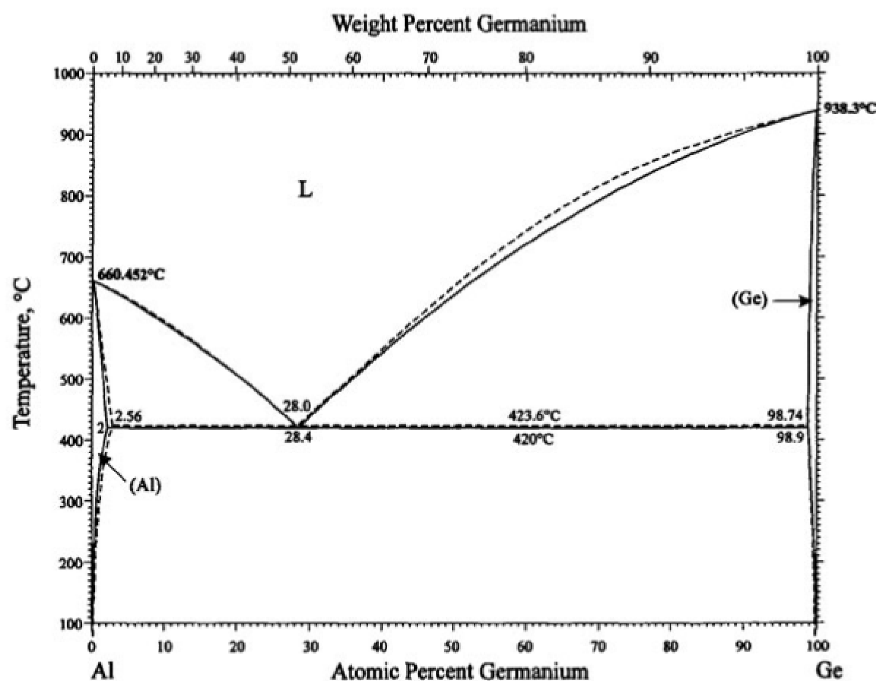


Figure 2.1 Al-Ge phase diagram[21]

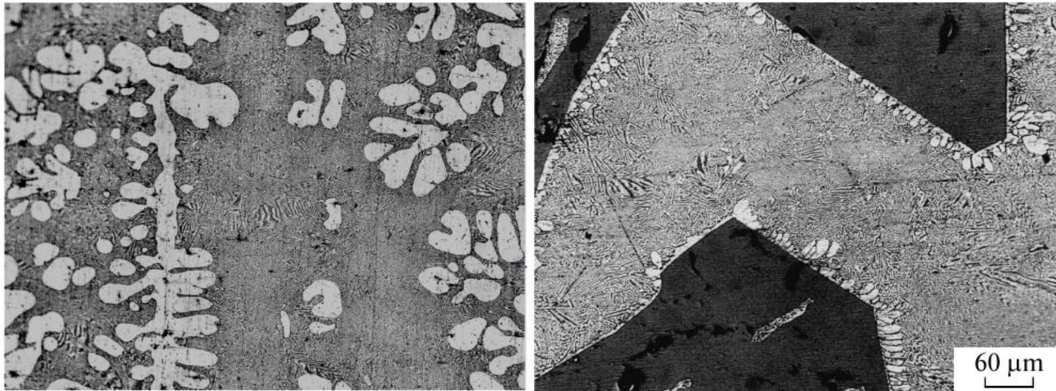


Figure 2.2 Microstructure of the Al-Ge alloys with pro-eutectic Al(left) and Ge(right) phases[32]

The study of Derkachenko et al. on directionally crystallized Al-Ge alloy indicates that the tensile strength of the alloy increases with increasing Ge content up to the eutectic composition, where it is 200 MPa. At compositions higher than the eutectic point, the tensile strength decreases since brittle fracture occurs in the hypereutectic region [35]. However, according to the work of Quintana et al. on thermally evaporated Al-Ge layer stack, the presence of pro-eutectic Al increases the strength of the alloy[36].

The most significant advantage of Al-Ge alloy for wafer bonding is that both metals are widely used for CMOS fabrication, which averts compatibility issues. Al is a standard bond pad material, while Ge is used to fabricate Si-Ge. It is also used for transistors built into the CMOS wafer [37]–[39]. On the other hand, the main limitation of the alloy is that the eutectic melting point is close to the process temperature limit of CMOS wafers. Heterogeneous integration of a CMOS wafer and a Si photonic wafer at 450 °C has been reported by Quack et al. The bond strength has been evaluated based on fracture toughness (G_{1c}) of the joint, which was calculated as 8 J/m^2[40]. Aluminum adheres on passive surfaces such as SiO_2, Si_3N_4, or TiN with no adhesion layer requirement [41], [42]. Lumineau et al. have compared the behavior of Al-Ge alloy on SiO_2 and TiN substrates by coating Ge over Al and annealing. The alloy wets both surfaces with a better contact angle on

TiN. It was also indicated that better wetting increases the likelihood of squeeze-out, and a minimum possible bonding force shall be applied to prevent it [43].

The thickness ratio required for the desired composition is calculated as follows [23],

$$\frac{t_{Ge}}{t_{Al}} = \frac{wt\%_{Ge} \times \rho_{Al}}{wt\%_{Al} \times \rho_{Ge}} \qquad (1)$$

Because of the effective thickness of the deposited layers, the actual thickness ratio differs from the theoretical value. There is consensus in the literature that 0.59 is the optimum thickness ratio for Al-Ge eutectic bonding with different values of total layer thickness [44]–[46].

The most common layer stack design is formed by depositing Ge over Al, schematically shown in Figure 2.3. This design is because the oxide layer on the top surface affects bond quality and Al_2O_3 is much more tenacious compared to GeO_2 and suboxides of Ge. GeO_2 is reported to be soluble in DI water. 30 seconds of dilute HF bath (2%) followed by DI water rinse is reported to remove GeO_2 and other suboxides on the surface [47]–[49].

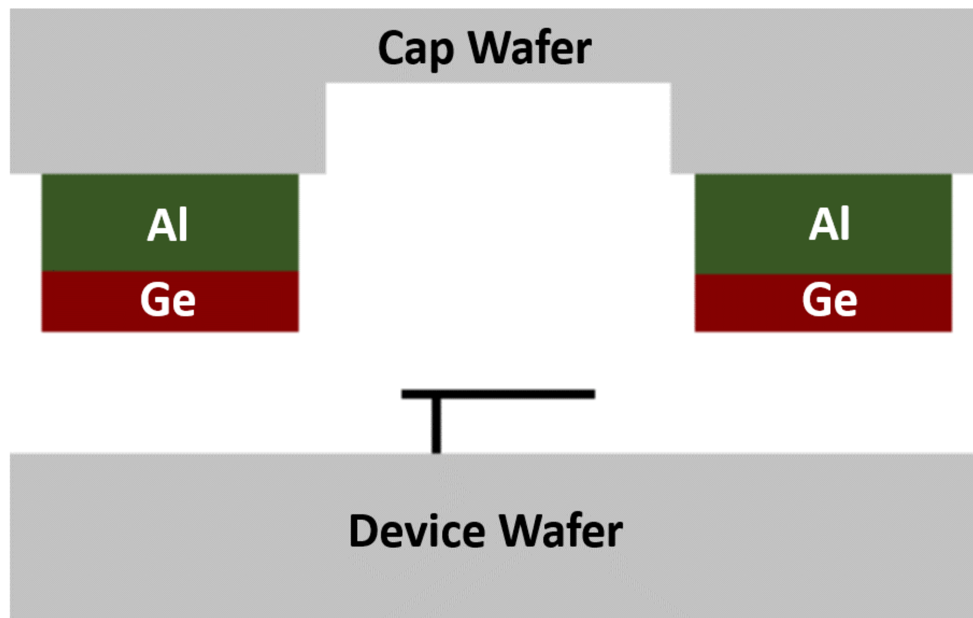


Figure 2.3 Layer stack design for Al-Ge eutectic bonding

Formic acid treatment is also effective for GeO_2 removal. [50]. Oxide layers on both Al or Ge surface can be removed by inverse sputtering or plasma etching [47], [51].

Crnogorac et al. performed eutectic bonding with the same stack design at 435°C with 0.2 MPa bonding pressure and diluted HF treatment before bonding. They sputtered 59 nm thick Ge layer on 100nm Al. Figure 2.4 is the microstructure revealed after grinding and etching away the top wafer. They measured the fracture toughness of the bonded sample to asses the bond strength, which appeared to be 51 J/m^2 [44].

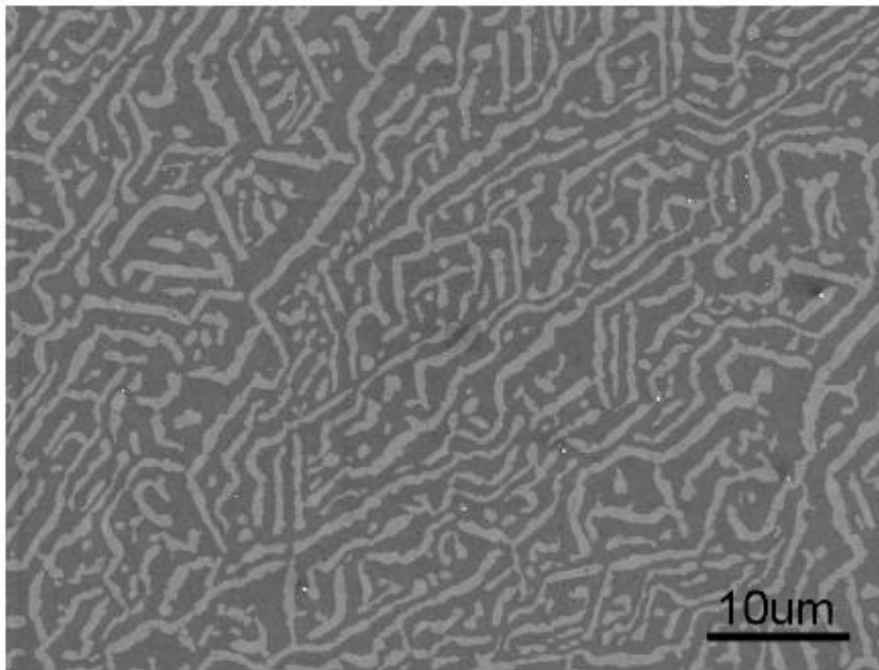


Figure 2.4 SEM image of the Al-Ge alloy after bonding

Huang et al. performed wafer bonding at 430 °C with approximately 15 MPa bond pressure and obtained a shear strength of 18 MPa [45].

Another approach is to coat the layers with the same thickness ratio in sequential order, so the increased number of interfaces and shorter diffusion distances can reduce the required bonding time. This method was used by Chidambaram et al. They coated a layer stack of 0.75 µm Al/0.43 µm Ge/0.25 µm Al/0.16 µm Ge and performed hermetic sealing at 475°C that after diluting HF treatment and solid state

diffusion bonding at 400°C. The average bond strength after bonding at 475°C was 45 MPa [48].

Another layer stack design is to coat Al and Ge on separate wafers. Chidambaram and Wickramanayaka studied Al-Ge diffusion bonding at different temperatures. They use formic acid to clean the Ge surface in the bond chamber, while they use inverse sputtering for Al before bonding. They tried diffusion bonding at 300, 350, and 450 °C temperatures. Figure 2.5 shows cross-section SEM images of bonded samples after bonding at 350°C and 450 °C. Although the eutectic bonded sample had the highest shear strength, they report that liquid formation is not essential for hermetic sealing. They also examined the effect of thermal aging on the samples, which improved the strength of diffusion bonded samples but did not affect the eutectic bonded ones. The average shear strength was approximately 37 MPa after bonding at 450 °C while 25 MPa at the lower temperatures. [50].

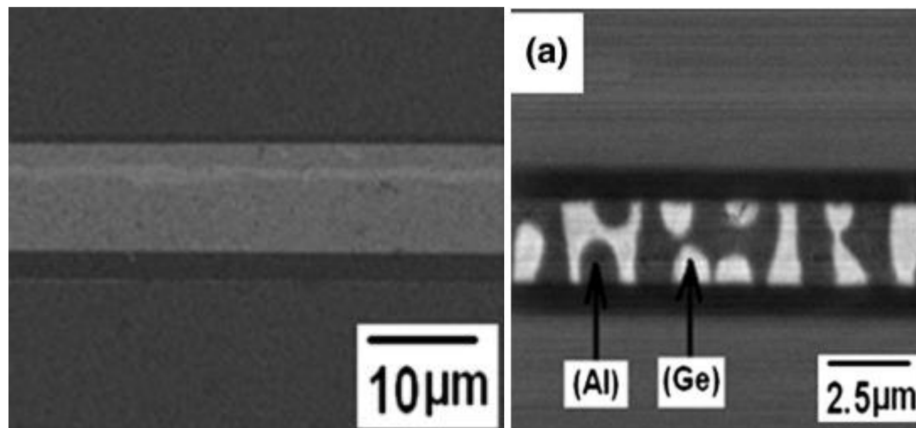


Figure 2.5 Cross-section SEM images of bonded samples after bonding at 350°C(left) and 450 °C(right)

In some cases where Al and Ge are coated on separate wafers, an additional layer of Al is coated under Ge to increase the number of interfaces [50], or for cushioning to cover topography. Xu et al. used the latter for vacuum packaging of Pirani gauges at 430 °C. The bonding procedure involved 15 minutes of solid-state bonding at 400 °C with a low bonding pressure followed by 30 minutes of eutectic bonding at 430 °C with a relatively higher bond pressure. Related temperature versus time curve is shown in Figure 2.6 [38].

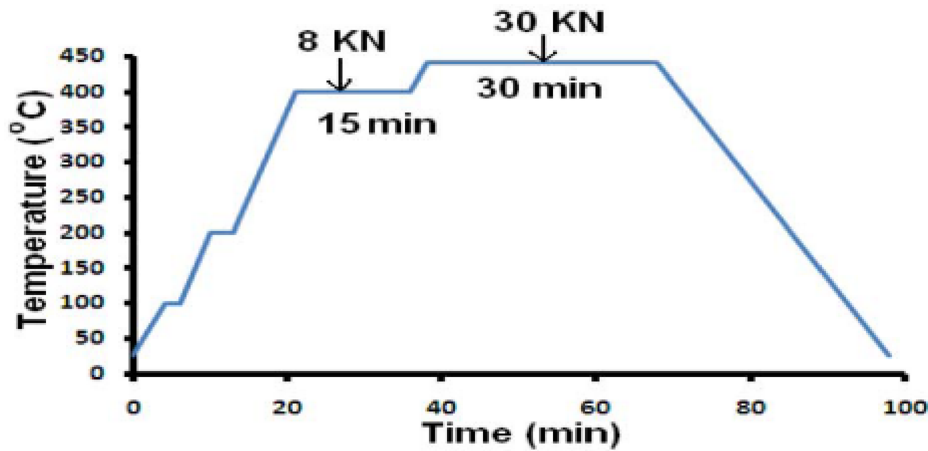


Figure 2.6 Temperature vs. time curve for wafer low temperature Al-Ge eutectic wafer bonding process

Chua et al. have performed eutectic bonding by coating Al and Ge layers on separate wafers and removing the oxide layers before bonding.[52]. Baum et al. performed eutectic bonding at 450°C after using 0.32% HF for the GeO_2 layer and a mixture of 60%H_3PO_3 and 30%HNO_3 for the Al_2O_3. They have conducted wafer bonding experiments with patterns having varying strip lengths to measure the fracture toughness (G_{Ic}). The G_{Ic} results ranged between 25 J/m^2 and 34 J/m^2 [34]. Another method to remove the oxide layers when Al and Ge are coated on separate wafers is to apply bonding pressures in the range of 6-9 MPa and crush the oxide layer during bonding. It is argued that it is nearly impossible to perform bonding before the oxide layers regenerate. Results of experiments with different bonding temperatures, bonding pressures, and time. It has been reported that lower temperatures and higher bonding pressures result in higher bond strengths. Eutectic bonding was performed at 430°C with 9 MPa bonding pressure. The effect of temperature has been explained by the higher viscosity of the liquid at lower temperatures [45]. An inertial sensor packaged using Al-Ge eutectic bonding with Al and Ge on separate wafers has been reported by Wu-et al. Ge is coated over poly-Si with no adhesion layer. The average shear strength has been reported as 55 MPa. However, the bonding temperature was not specified. [53]. However, Gao et al. used Ti under Ge to enhance the adhesion. They also designed network-like structures to reduce side leakage. The designs are shown in Figure 2.7 [49].

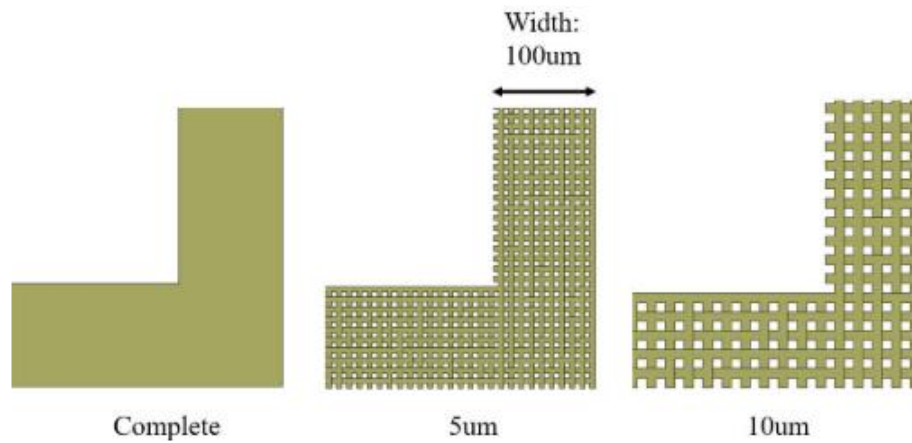


Figure 2.7 Network-like bond ring design to prevent side leakage

There are Al-based high aspect ratio and microfluidic structures successfully bonded by using co-deposited Al-Ge alloy. 1.5 MPa bonding pressure has been used at 510 °C. Both structures displayed a highly ductile fracture mode, which is related to the excess Al provided by the structure. Figure 2.8 shows the fracture surface after the tensile test. The tensile strength was 50 MPa after bonding at 400 °C, and it varied between 80 and 156 MPa after bonding at 450 °C [54], [55]. Examples of Al-Ge eutectic bonding applications are summarized in Table 2.1.

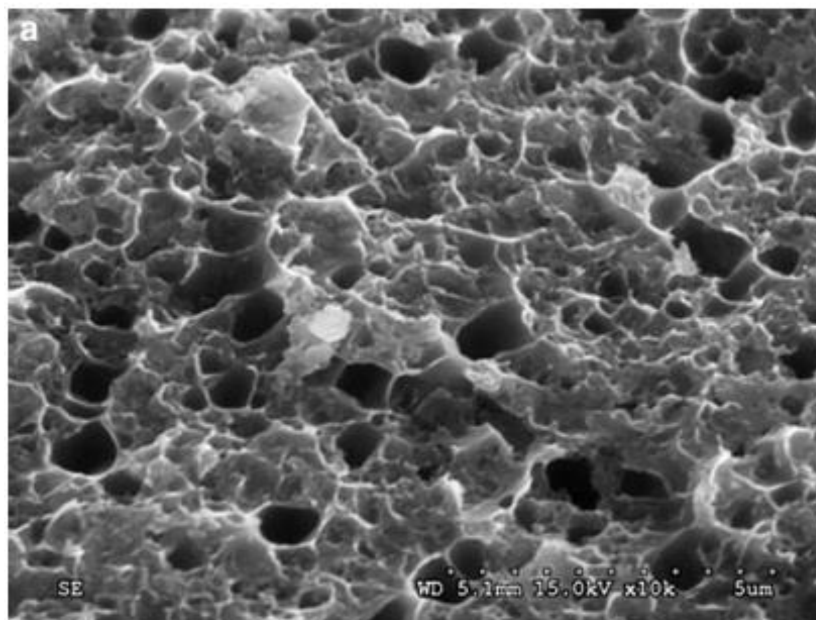


Figure 2.8 Fracture surface of the bond area after tensile load [54]

Table 2.1 Summary of Al-Ge eutectic bonding studies in the literature

	Bonding Approach	**Bonding Temperature (°C)**	**Bond Pressure (MPa)**	**Oxide Removal**	**Shear Strength (MPa)**	**Tensile Strength (MPa)**	**G_{Ic} (J/m^2)**
[34]	Metallization on both wafers	450	NS**	0.32% HF 60% H_3PO_3+30% HNO_3	-	-	25-34
[40]	Al/Ge Layer Stack	450	NS	NS**	-	-	8
[44]	Al/Ge Layer Stack	435	0.2	Dilute HF (2%)	-	-	51
[45]	Al/Ge Layer Stack	430	15	None***	18	-	-
[50]	Metallization on both wafers	450	11	Formic Acid (GeO2) Inverse Sputtering (Al_2O_3)	37	-	-
[50]	Metallization on both wafers	350	35	Formic Acid (GeO_2) Inverse Sputtering (Al_2O_3)	25	-	-

	Bonding Approach	Bonding Temperature (°C)	Bond Pressure (MPa)	Oxide Removal	Shear Strength	Tensile Strength	G_{Ic} (J/m^2)
[52]	Metallization on both wafers	Not Specified	-	Inverse Sputtering	-	-	-
[53]	-	--	-	-	55	-	-
[54]*	Co-sputtered Al-Ge	510	-	NS**	-	50	-
[55]*	Co-sputtered Al-Ge	450	-	NS**	-	80-156	-

***:** Substrates are Al-based structures

****:** Not specified

*****:** Oxide layer is crushed during bonding due to the high bonding force

CHAPTER 3

EXPERIMENTAL PROCEDURE

The experimental procedure is conducted with optical glass and single-side polished Si wafers. Experiments are applied on blank wafers to optimize the parameters for CMOS compatibility. After microfabrication and wafer bonding, the samples are characterized for their structural and mechanical properties.

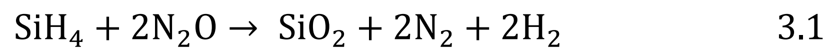
3.1 Fabrication Methods

Arc Melting

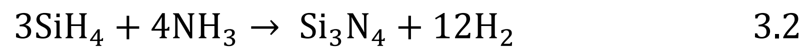
Arc melting is used to produce alloys with desired compositions for microstructural characterization and bulk alloys for thermal evaporation. Components weighed for the desired composition are placed on a water-cooled copper plate in a vacuum chamber. Afterward, the metals melt and mix into each other as a result of an arc between the metals and an electrode. Every sample has been melted three times and turned over for microstructural homogeneity. Figure 3.1 is a photograph of the system. Samples of 0.3 and 1 g of samples are prepared for microstructure and thermal evaporation, respectively.

Deposition of passivation layers

Passivation layers prevent diffusion and provide electrical insulation for devices formed for the subject experiments. Another function of these layers is to protect the wafer's polished surface when the wafer's backside is to be processed. Passivation layers used for the experiments are SiO_2 or Si_3N_4 with 50-200 nm thicknesses deposited using plasma enhanced chemical vapor deposition (PECVD). Figure 3.2 is the photo of the STS PECVD system. Depositions occur based on the following reactions.



$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2 \qquad 3.1$$



$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \qquad 3.2$$

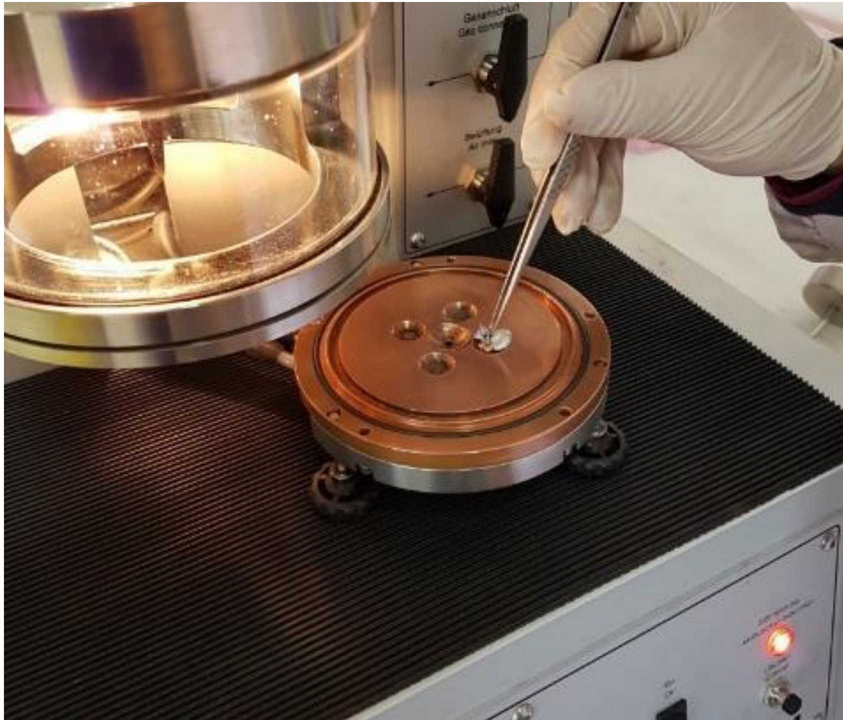


Figure 3.1 Edmund Buhler arc melter

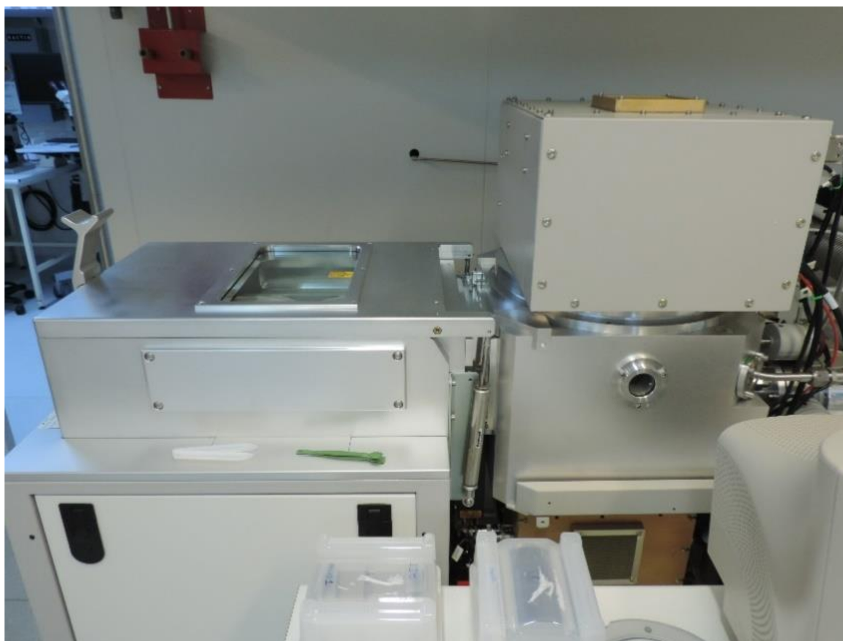


Figure 3.2 STS PECVD system

Metal Deposition

Metallic layers are deposited using thermal evaporation and sputtering. Varian 3119 system is used for thermal evaporation of the alloy manufactured by arc melting and separate deposition of Al and Ge layers. AJA sputtering system is used to sputter pure Al and Ge layers and co-sputtering these layers. Photos of the two systems are shown in Figure 3.3. Figure 3.4 shows a wafer being co-sputtered.

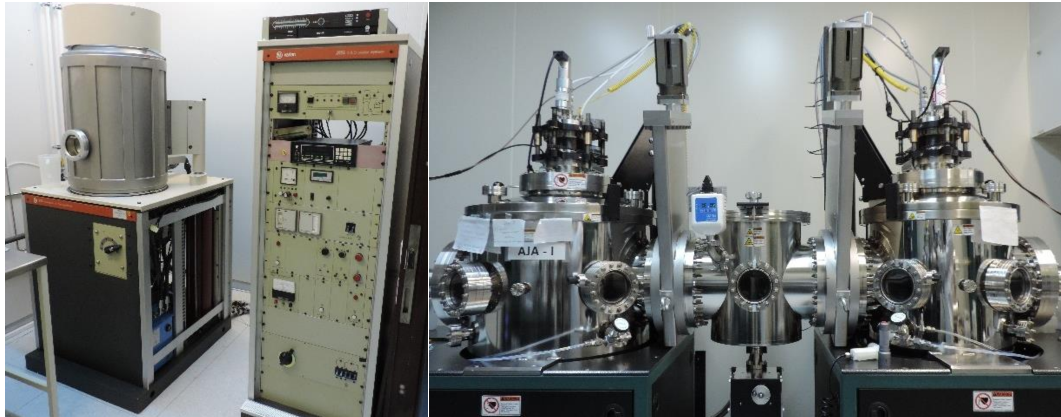


Figure 3.3 Varian thermal evaporation(left) and AJA sputtering systems(right)

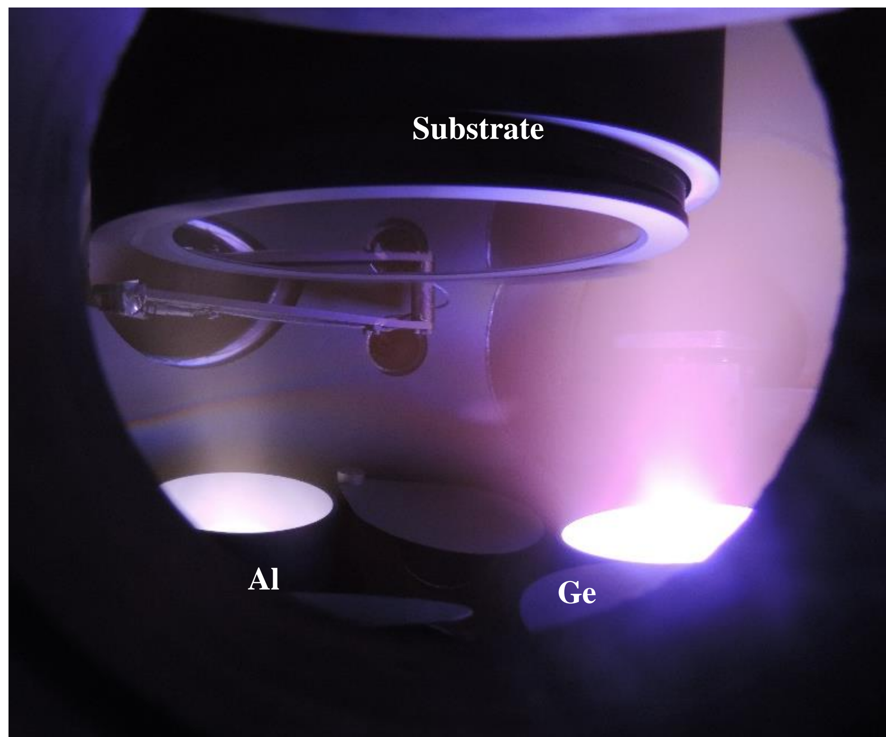


Figure 3.4 A wafer being co-sputtered

Cavity Formation

Deep reactive ion etching (DRIE) is a dry plasma etching system used to etch structures with high aspect ratios. The wafers are etched with SF_6 gas in a cyclic manner. A protective layer is deposited using C_4F_8 gas to prevent lateral etching. Figure 3.5-a is a schematic representation of DRIE steps [56]. Figure 3.5-b is the photo of the STS Pegasus DRIE system used for the experiments. The system is used for etching cavities and back-side alignment marks.

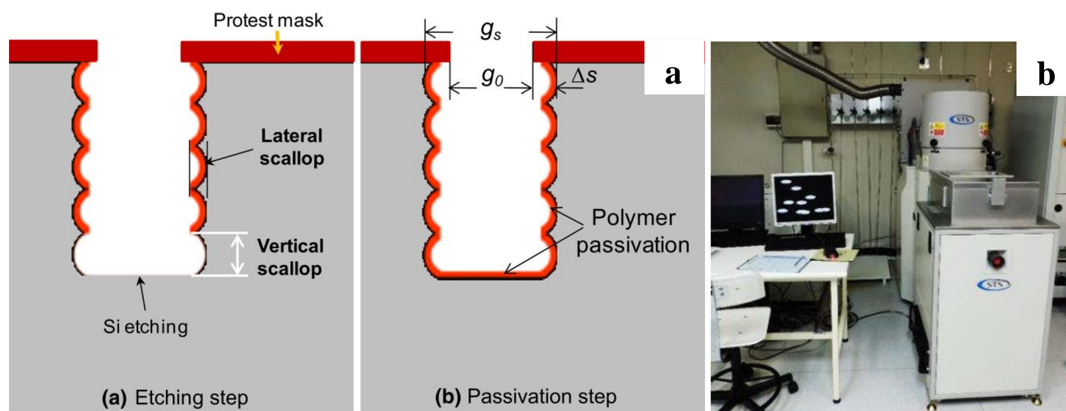


Figure 3.5 a) Schematic representation of etching and passivation steps during DRIE, b) a photo of the STS Pegasus DRIE system.

Lithography

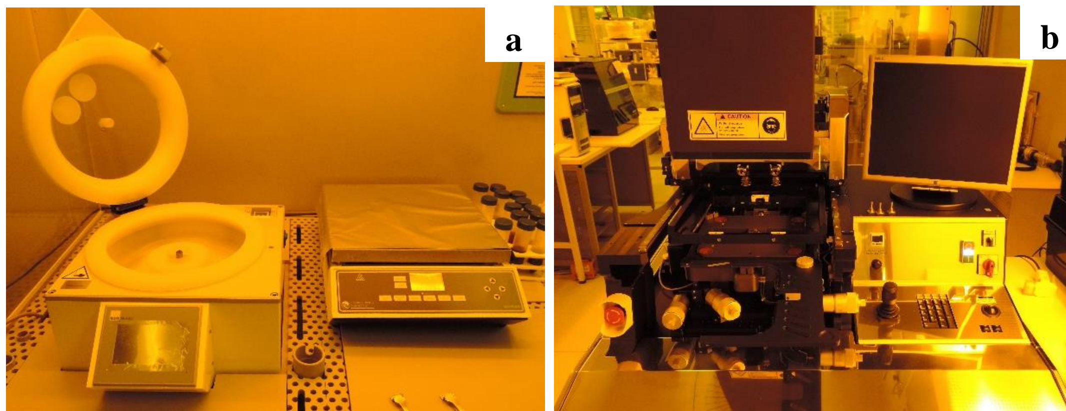


Figure 3.6 a) SUSS MicroTec spinner(left) and Torrey Pines hot plate(right), b) EVG 6200 contact aligner

UV lithography is used to obtain the desired patterns of the metallic layers over the wafers. Wafers are dehydrated by annealing at 110 °C for 10 minutes. Photoresists

(PR) are coated using a SUSS MicroTec spinner and soft baked on a Torrey Pines hot plate, photos of which are shown in Figure 3.6. Afterward, PR-coated wafers are exposed to UV with masks of desired patterns on an EVG 6200 contact mask aligner (Figure 3.6-b) The system is also used for bond alignment when necessary.

Post-exposure baking may be necessary depending on the PR, after which the wafers are developed. Hard baking may be used if the wafer is etched using wet or deep reactive ion etching (DRIE) for cavities or back-side alignment marks. After development, metallic layers are coated, and PR is removed by acetone lift-off. If the lithography is done for DRIE, PR is removed using PRS-2000 PR stripping solution with prior O_2 plasma treatment. Negative PRs are used for lift-off patterning metallic rings, while positive PRs are used for cavity etching processes. Hard baking is required for the lithography of PRs used in HF DRIE and BHF treatments.

Surface Treatment

Surface treatments are applied to the metallic surfaces to remove the oxide layers on top of metals. The effects of two surface treatments have been examined. The first method is inverse sputtering, during which the surface of the wafer is cleaned with Ar plasma for 60 seconds. The applied power was 300W with 3.5 sccm Ar flow into the chamber. Figure 3.7 is a photo of the BesTec sputtering system used for the process.

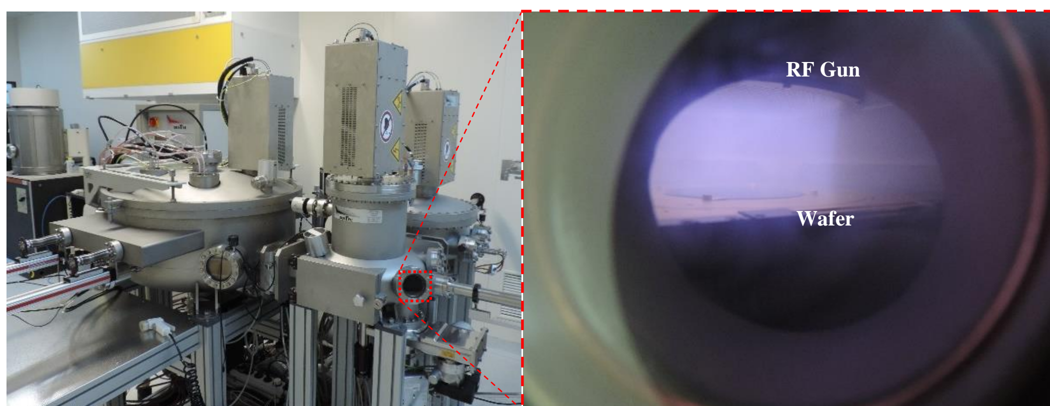
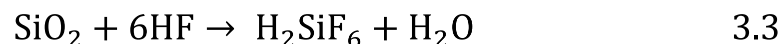


Figure 3.7 BesTec Sputtering System used for inverse sputtering

The second surface treatment is dilute HF treatment. The wafers with the Al/Ge layer stack are dipped in a 2% HF solution for 30 seconds. Afterward, they are rinsed in DI water and dried using an N_2 gun. When wet treatments are applied on wafers with cavities, the samples are dried using spin rinse drying (SRD), which is a method that the wafers are spun under an N_2 atmosphere. The Avenger Ultra-Pure 8 SRD system is used for the experiments, a photo shown in Figure 3.8.

Figure 3.8 Avenger Ultra-Pure 8 SRD system

Buffered hydrofluoric acid (BHF) is another wet treatment used during the experiments. It is a mixture of ammonium fluoride (NH_4F), hydrofluoric acid (HF), and water. It is used the remove the oxide passivation layer before cavity etching in DRIE. SiO_2 layer is etched by HF based on the following reaction.



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + H_2O \quad 3.3$$

Wafer Bonding

Wafers are bonded by applying heat and pressure in a vacuum chamber. Wafers are aligned using an EVG 6200 contact aligner. They are kept separated by thin

spacers(flags) between the wafers so that the cavities can be vacuumed effectively and process gasses can reach the bonding surfaces facing each other. The most common process gas is forming gas (95% N_2, 5% H_2). Flags are pulled at the desired stage of the process, and force is applied. Figure 3.9 is a photo of the EVG 520 IS wafer bonder used for the experiments.

Figure 3.9 EVG 520 IS wafer bonder.

Two different wafer bonding processes have been applied. The first one, referred to as Process I, is a simple eutectic bonding process in which the wafers are held at 450 °C with 3 MPa bonding pressure. The temperature and pressure profiles of the bonding process are shown in Figure 3.10. The wafers are annealed at 200 °C in a vacuum, so the gas molecules diffused into the wafers can be outgassed. Afterward, the chamber is purged with forming gas, and the temperature is increased to 350 °C and held for 15 minutes. Then, the chamber is evacuated, the temperature is increased to 450 °C, and the bonding force is applied. After 30 minutes, the temperature is lowered to room temperature while the bonding force is removed at 200 °C.

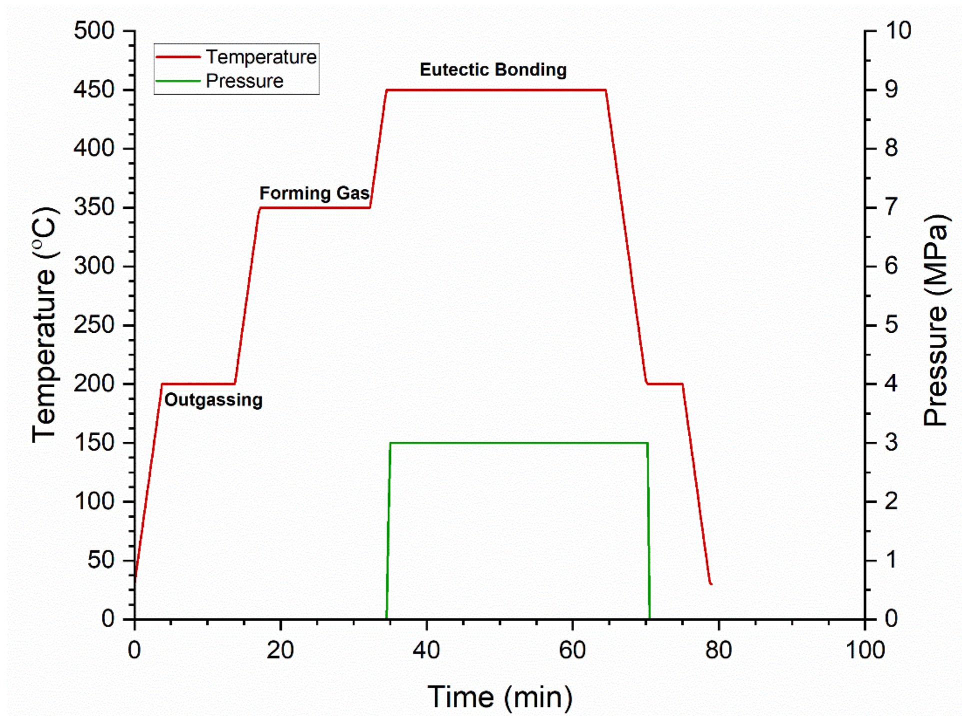


Figure 3.10 Temperature and pressure profile of the plain eutectic bonding procedure (Process I)

For the second bonding process (Process II), a solid-state bonding step with a higher bonding pressure is added. The wafers are bonded with 5 MPa bonding force at 400 °C, followed by eutectic bonding at 450 °C with 1.5 MPa bonding pressure. Temperature and pressure profiles are shown in Figure 3.11. For the second process, pressure at 400 °C is higher for bond integrity while lowering it to 450 °C to minimize squeeze-out.

The temperature and pressure of the eutectic bonding stage of Process II have later been lowered to minimize the heat input and squeeze-out.

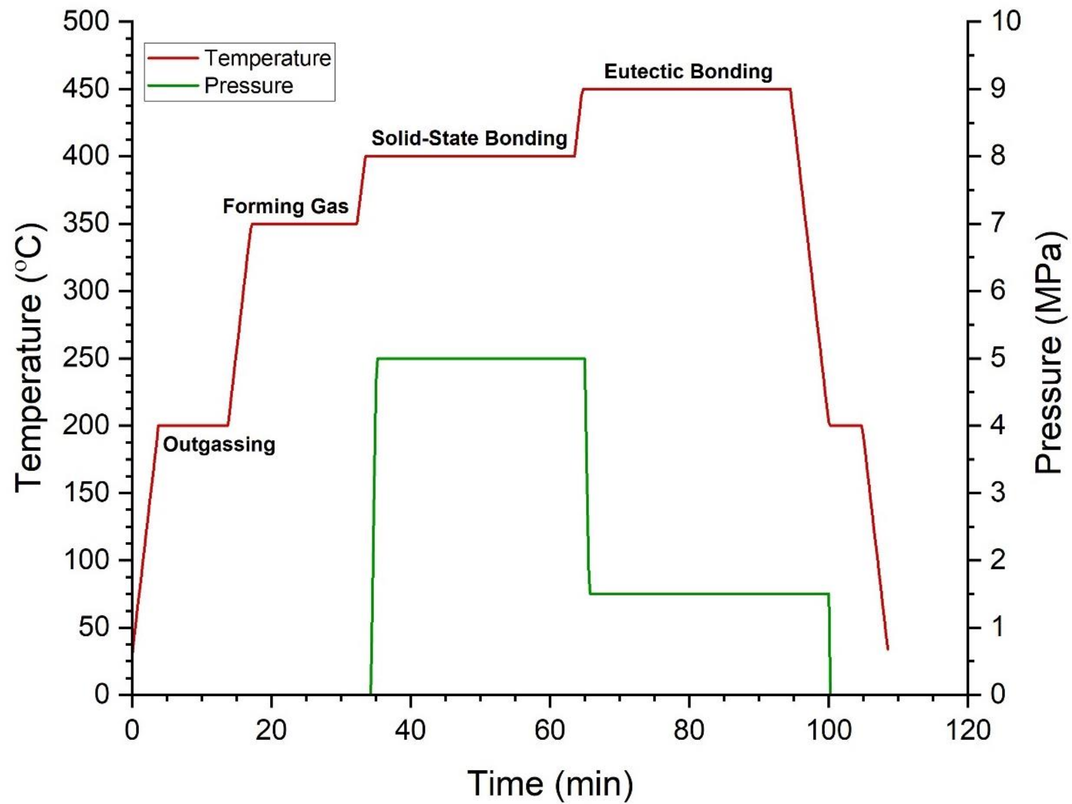


Figure 3.11 Temperature and pressure profile of the bonding procedure with solid-state bonding step (Process II)

Dicing

Dicing is used to separate the devices after wafer-level packaging. After wafer bonding, the wafers are diced for different characterization methods. The samples are mounted on an adhesive polymer film before dicing so that every piece will remain stationary during dicing. Afterward, the polymer film is exposed to UV to weaken the adhesion with the samples, and the dies are separated. Photos of the DAD 3350 dicing system and a bonded wafer pair after dicing are shown in Figure 3.12.

Figure 3.12 DAD 3350 dicing system(left) and a diced wafer pair(right)

3.2 Characterization Methods

The microstructures of alloys and thin films have been examined using optical microscopy (OM) and SEM. EDS module of the SEM and the XPS system at METU Central Laboratory is used for elemental analysis.

Veeco Dektak 8 profilometer is used to measure the thickness of the coated films while it is supported with SEM images when there are two coatings one over another. The profilometer is also used to deflection of the caps after vacuum packaging. Thicknesses of the passivation layers are measured using Filmetrics F40 thin film analyzer. Photos of the systems are shown in Figure 3.13.

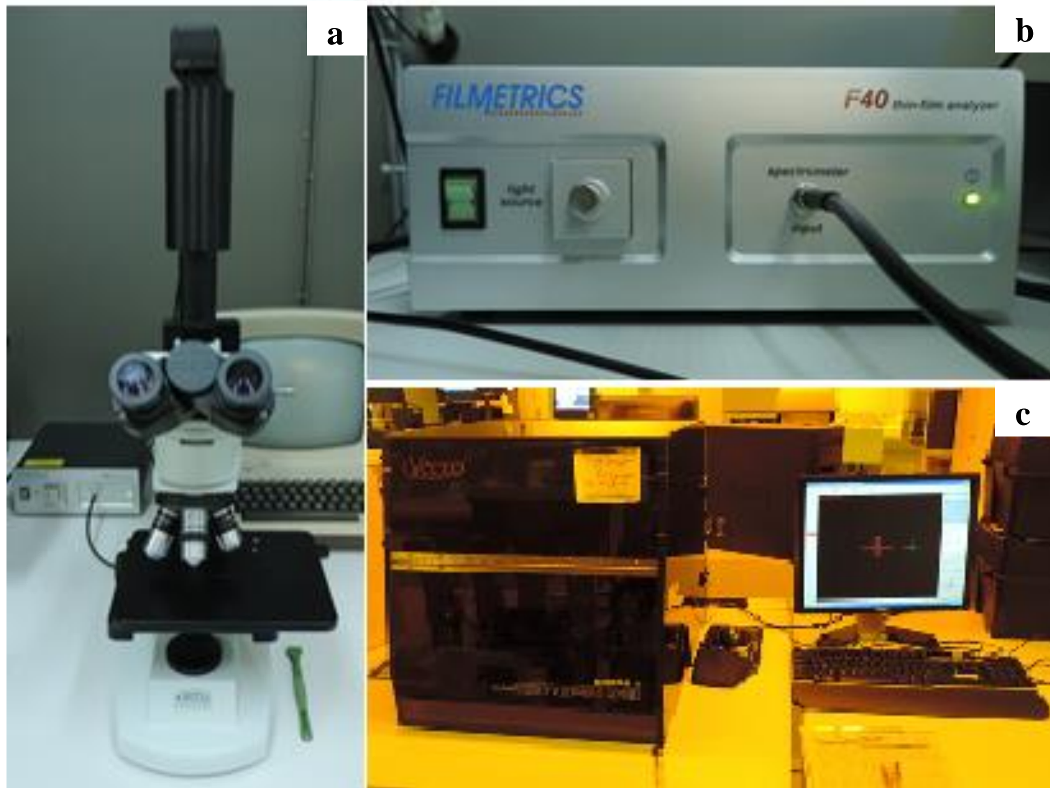


Figure 3.13 a,b) Filmetrics thin film analyzer, c) Veeco Dektak 8 Profilometer.

The differential scanning calorimetry (DSC) system of the METU Central Laboratory is used for the thermal characterization of bulk alloys and deposited films.

Scanning Acoustic Microscopy

Scanning acoustic microscopy (SAM) is a characterization method that provides imaging through acoustic waves. Sound waves generated by a 200 MHz transducer are reflected from every interface they collide, resulting in a peak on time versus intensity diagram as shown in Figure 3.14(b). Figure 3.14(c) is an image example formed using this signal data. Samples are placed in DI water since acoustic waves are conducted more efficiently in a liquid medium. Bonded wafers are examined in a PVA TepLA 301 HD SAM. Figure 3.14(a) is a photograph of the system.

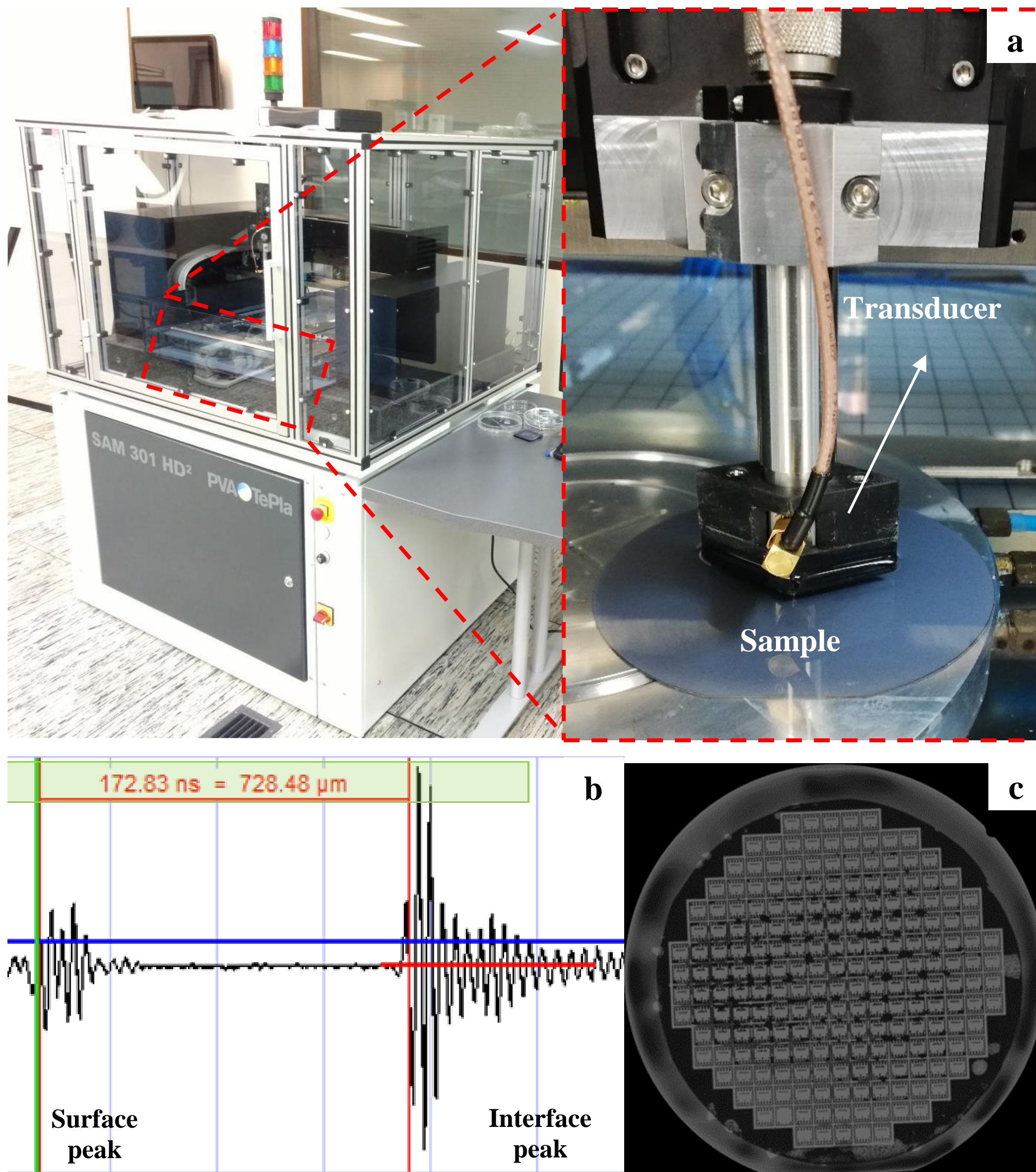


Figure 3.14 PVA TePlA 301 HD SAM(a), surface and interface peaks, and the SAM image

Shear Test

The mechanical strength of the bonded wafers is measured using DAGE Nordson 4000 Bond Tester. The setup of the system is given in Figure 3.15. Bonded wafers are loaded in shear after the height of a loading chisel is adjusted according to their thicknesses.

Figure 3.15 Shear testing system

He Leak Test

He leak test is used for the qualification of hermetic seals. The samples are bombarded by He under a certain pressure for a time specified by MIL-STD-883. Afterward, the samples are placed in a He spectrometer with a vacuum chamber to quantify the He atoms leaking out of the samples. Table 3.1 contains the pressure, minimum exposure time, and maximum He leak values for hermeticity, depending on the inner volume of the package. The setup for He bombardment and MS 40 CE VIC Leak Detector are as shown in Figure 3.16 and Figure 3.17, respectively.

Table 3.1 He leak test conditions according to package sizes.

Volume of package (V) in cm^3	Bomb condition			R_1 Reject limit (atm cc/s He)
	Psia ±2	Minimum exposure time hours (t_1)	Maximum dwell hours (t_2)	
<0.05	75	2	1	5×10^{-8}
≥ 0.05 - <0.5	75	4	1	5×10^{-8}
≥ 0.5 - <1.0	45	2	1	1×10^{-7}
≥ 1.0 - <10.0	45	5	1	5×10^{-8}
≥ 10.0 - <20.0	45	10	1	5×10^{-8}

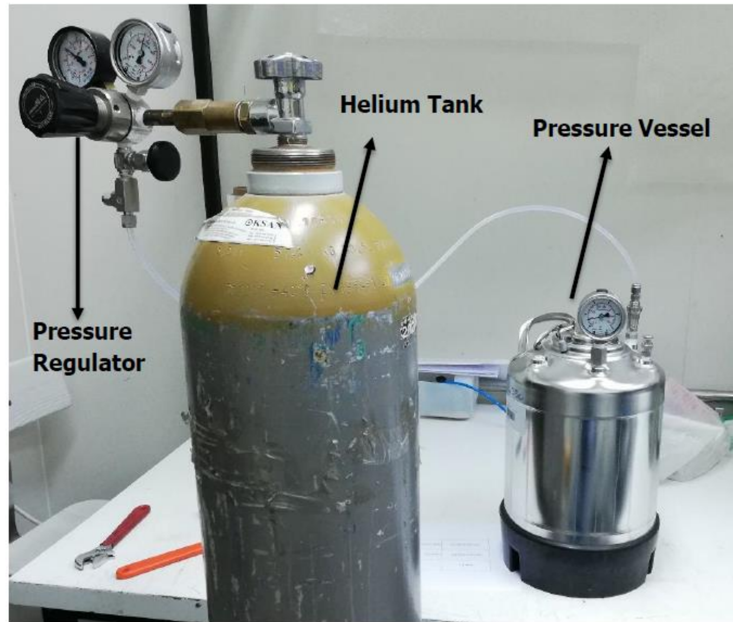


Figure 3.16 The He bombardment setup

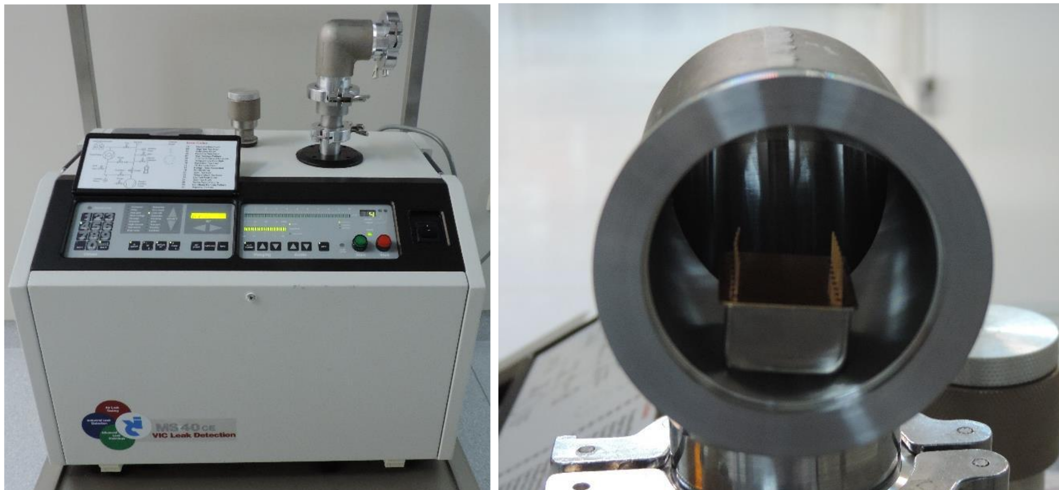


Figure 3.17 The He spectrometer and a sample in the vacuum chamber

Cap Deflection Test

Cap deflection is a practical method to measure the pressure inside a cavity sealed in a vacuum. The cap wafer is etched until it is approximately 100 µm thick so that it can act as a membrane that can deflect due to the pressure difference between the cavity and the atmosphere. The mechanism of the cap deflection is schematically shown in Figure 3.18.

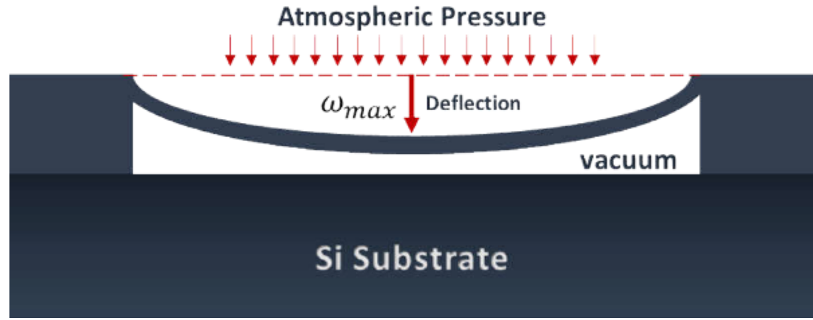


Figure 3.18 Schematic representation of cap deflection

the pressure difference based on deflection is calculated by the following equation,

$$\Delta P_{total} = \frac{32Eh^3(l^4+w^4)}{5(1-\vartheta^2)l^4w^4} \tag{2.1}$$

Where h is the thickness of the diaphragm, ϑ is the Poisson's ratio, and l is the distance between the two ends of the diaphragm.

Deflection values for different membrane thicknesses and pressure levels are calculated using COMSOL Multiphysics Simulation Software and given in Figure 3.19.

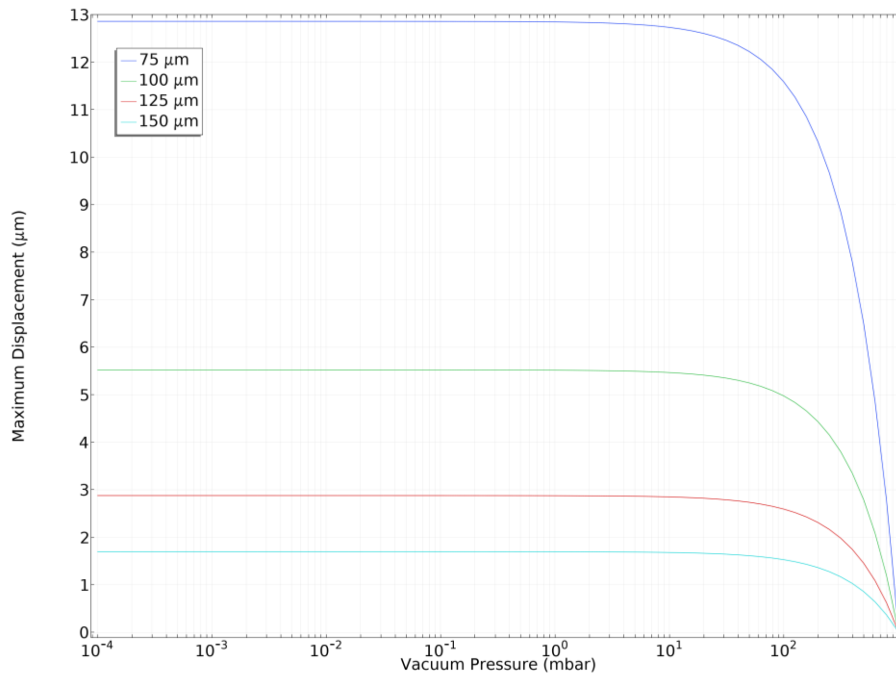


Figure 3.19 Cap deflection values for different membrane thicknesses and pressure levels

CHAPTER 3

RESULTS & DISCUSSION

4.1 Alloy Deposition

4.1.1 Microstructure of the alloy after arc melting

The samples have been melted three times by arc melting and flipped between every time for chemical homogeneity. Figure 4.1 is the SEM image of the cross-section of the alloy with 51.6 wt% Ge. There is a significant amount of pro-eutectic Al due to continuous cooling.

Figure 4.1 SEM image of the alloy with 51.6 wt% Ge

Several compositions with a higher amount of Ge have been tried for the following samples (53, 54, and 56.5 wt% Ge). Figure 4.2 is the SEM image of the sample with 56.5 wt% Ge. It has the microstructure closest to 100% eutectic morphology with only a trace amount of pro-eutectic Ge. The pro-eutectic phase disappeared when 1g samples were fabricated for thermal evaporation.

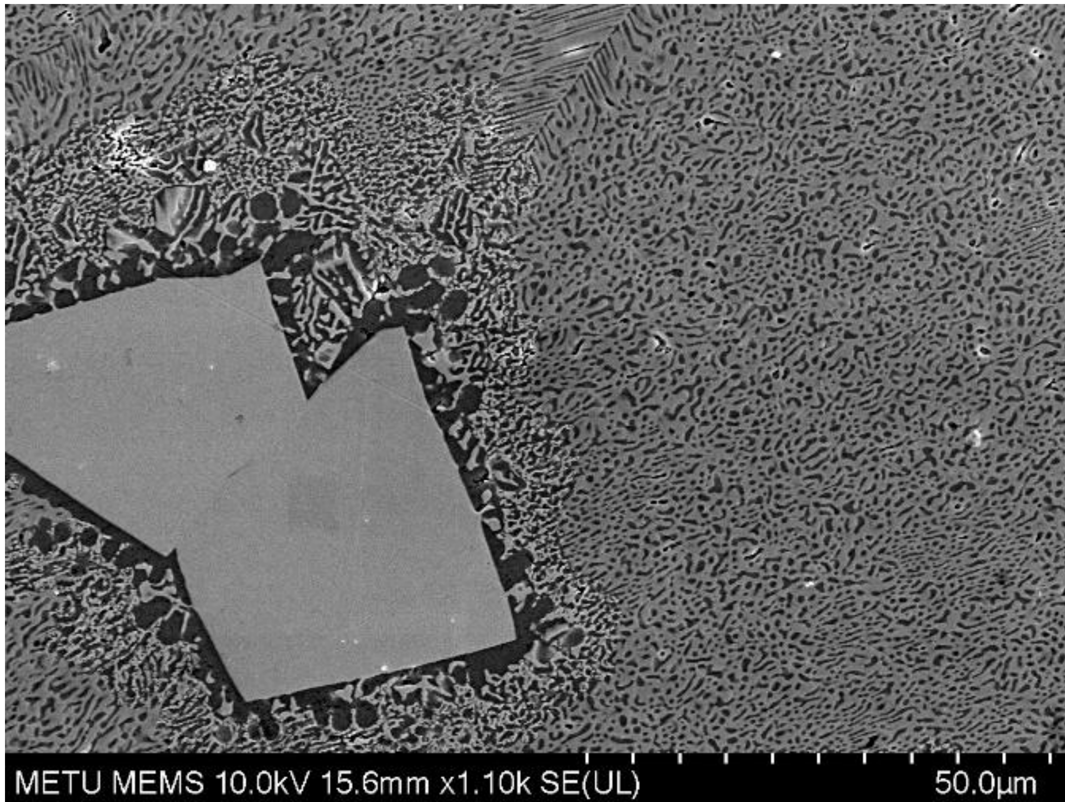


Figure 4.2 SEM image of the alloy with 56.5 wt% Ge

The DSC result of the alloy is shown in Figure 4.3. Melting appears to begin at 425 °C, while solidification starts at 413 °C. There is a second peak very close to the melting peak, which means that the composition is slightly off the eutectic point.

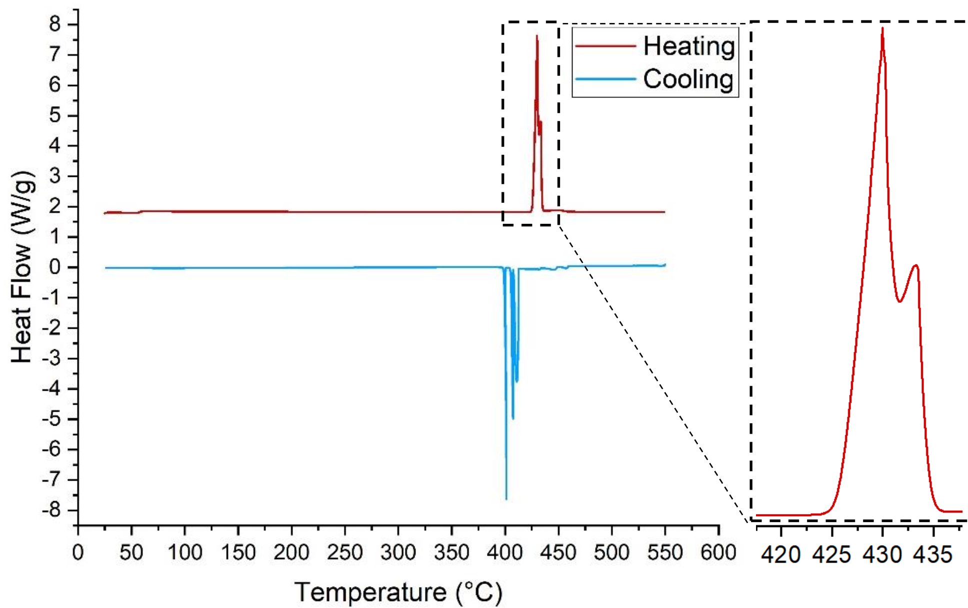


Figure 4.3 DSC curve of the alloy with 56.5 wt% Ge

4.1.2 Thermal Evaporation and Annealing

The initial thermal evaporation experiment was conducted with an alloy of 1g. The surface of the substrate is coated with a SiO_2 layer to prevent Si diffusion into the alloy. The deposition rate is kept in the range of 4-5 Å/s. Using 1g Al-Ge alloy resulted in a 450 nm thick layer. Figure 4.4 is the SEM image and the EDS map of the cross-section of the alloy. Al and Ge have segregated during thermal evaporation due to different melting points and vapor pressures. Figure 4.5 shows the composition profiles of Al and Ge through the thickness of the layer. The film was annealed for 1 hour at 450 °C and 25 °C above the eutectic melting temperature. SEM image of the film after annealing is shown in Figure 4.6. It indicates that diffusion between Al and Ge has not been completed. The film has been at 550 °C to observe the final microstructure. Figure 4.7 shows microstructure after 20 hours, which is the time required for the film to homogenize.

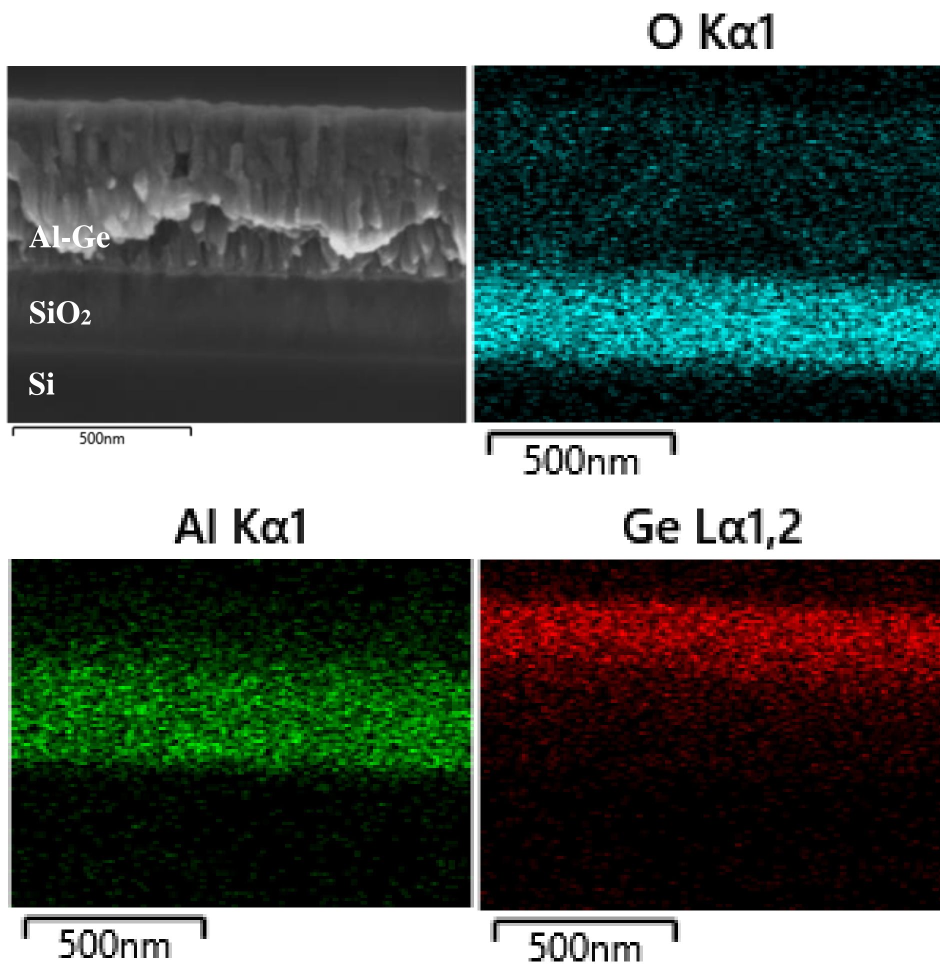


Figure 4.4 SEM image and EDS map of the cross-section of the deposited alloy

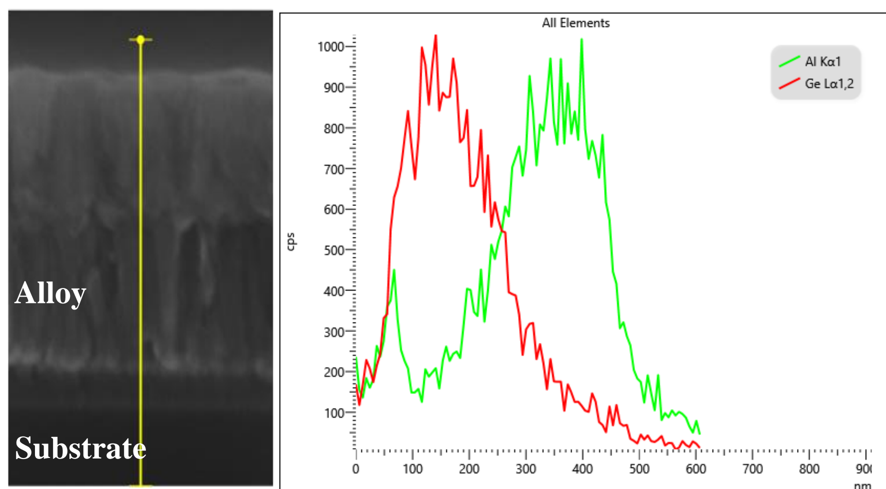


Figure 4.5 EDS line profile of Al and Ge

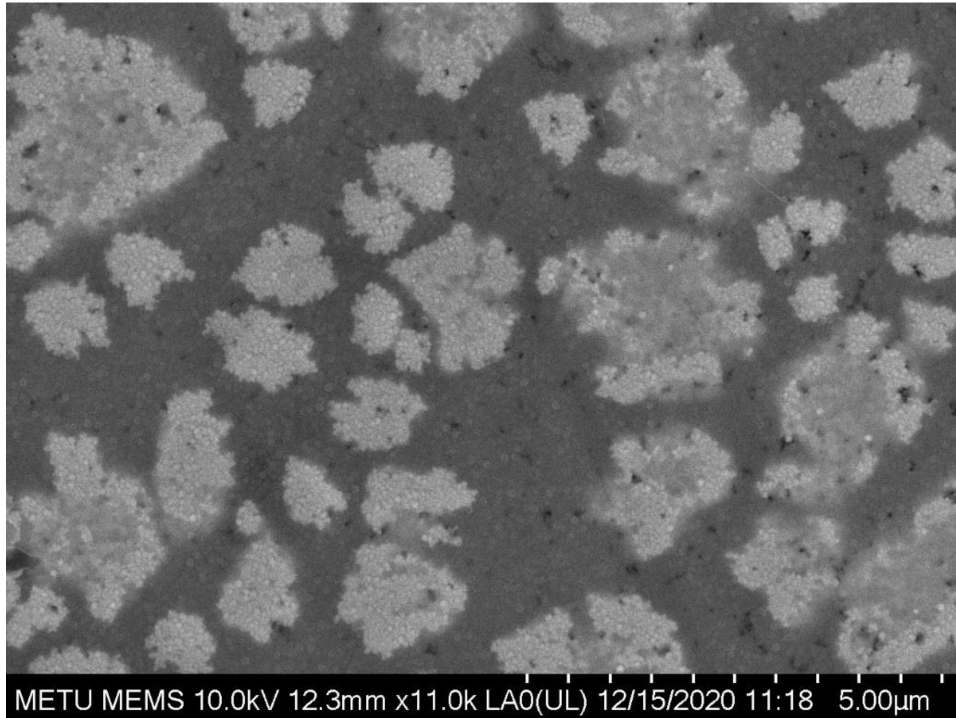


Figure 4.6 SEM image of the film after 1h of annealing at 450°C

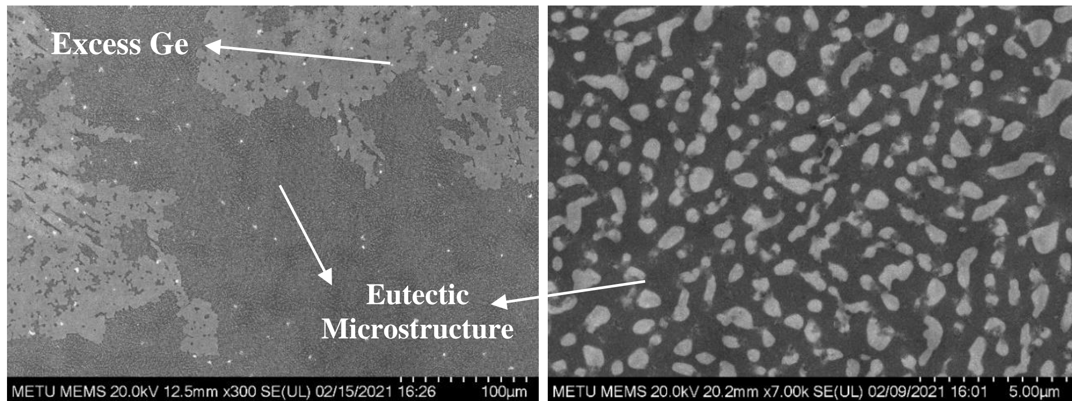


Figure 4.7 SEM image of the film after 20h of annealing at 550°C

For the second thermal evaporation experiment, the current passing through the boat has been increased to reduce the composition gradient along the cross-section. The deposition rate rose to the range of 10-12 Å/s as a result of the increase in current. Composition profiles of Al and Ge through the cross-section are shown in Figure 4.8. Although it displays the same profile, composition gradients are significantly smaller than the layer with a slower deposition rate. Figure 4.9 is the SEM image of

the film after annealing. The time required for a homogeneous microstructure decreased from 20 hours to 5 hours. An increase in current resulted in more heat input into the alloy inside the boat, causing the Ge to evaporate faster. As a result, the compositions of the Al and Ge within each other have increased. Due to the annealed samples resulting in excess Ge, the thermal evaporation experiment has been repeated with 51.6 % Ge. There was no apparent eutectic phase formation after extended annealing, which indicates that it is difficult to control the composition during thermal evaporation of the alloy.

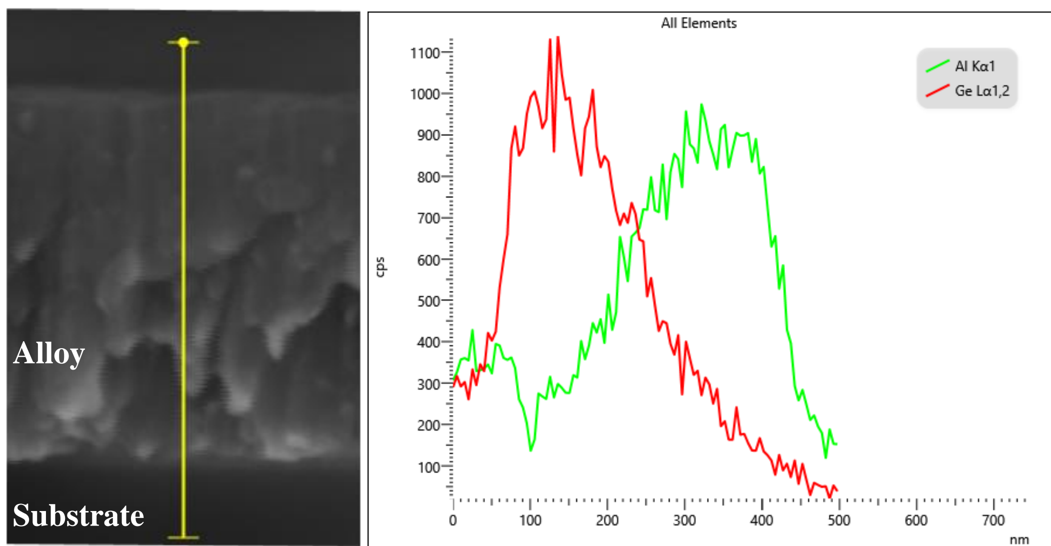


Figure 4.8 Composition profiles of Al and Ge through the cross-section

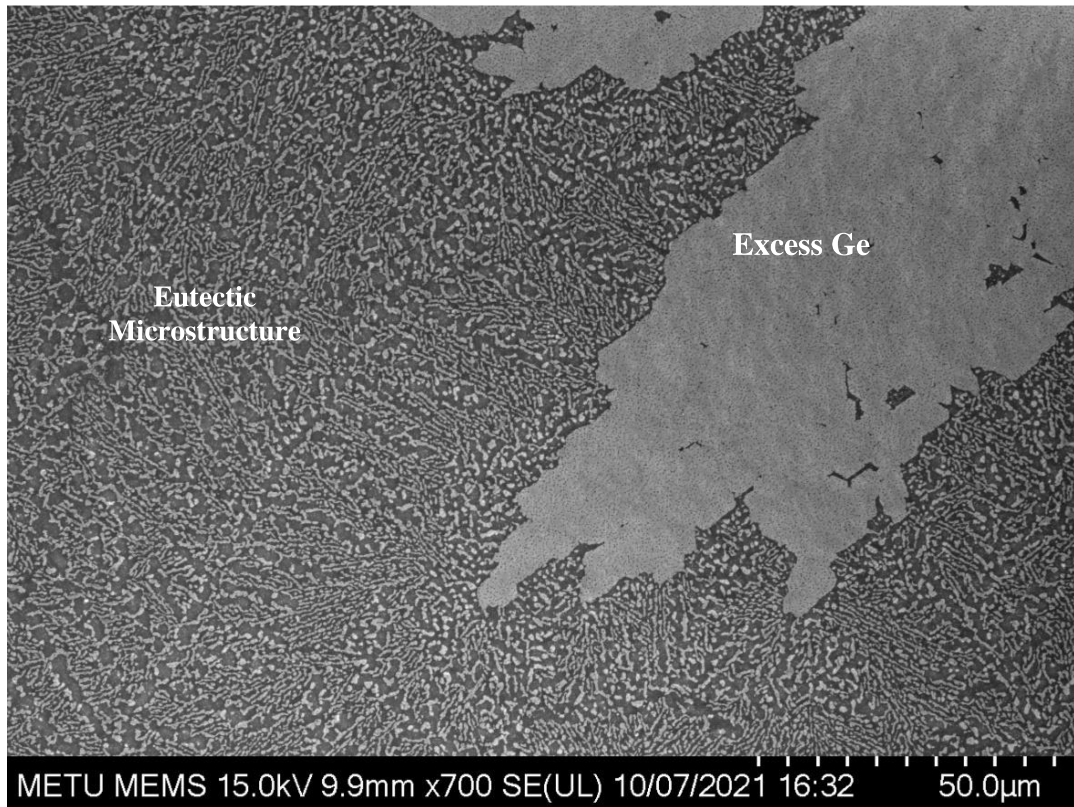


Figure 4.9 SEM image of the film with a high deposition rate after 5 hours of annealing at 550°C

Figure 4.10 is the DSC curve of the as-coated film. The curve shows a small melting peak at 427 °C while solidification starts at 396 °C. The intensity of the peaks is small for two main reasons. First, the sample is a 400 nm thick layer over a 500 µm thick Si wafer. The greater mass of Si dilutes the melting effect on the DSC detector. The slight increase in the peak intensity during the second heating indicates that the sample has only partially melted since the interdiffusion between Al and Ge layers is not complete. The analysis has been repeated with an annealed sample, and the peak intensity increased further due to the increased amount of liquid, as shown in Figure 4.11. Also, the solidification peak has been shifted to the same point as the melting peaks.

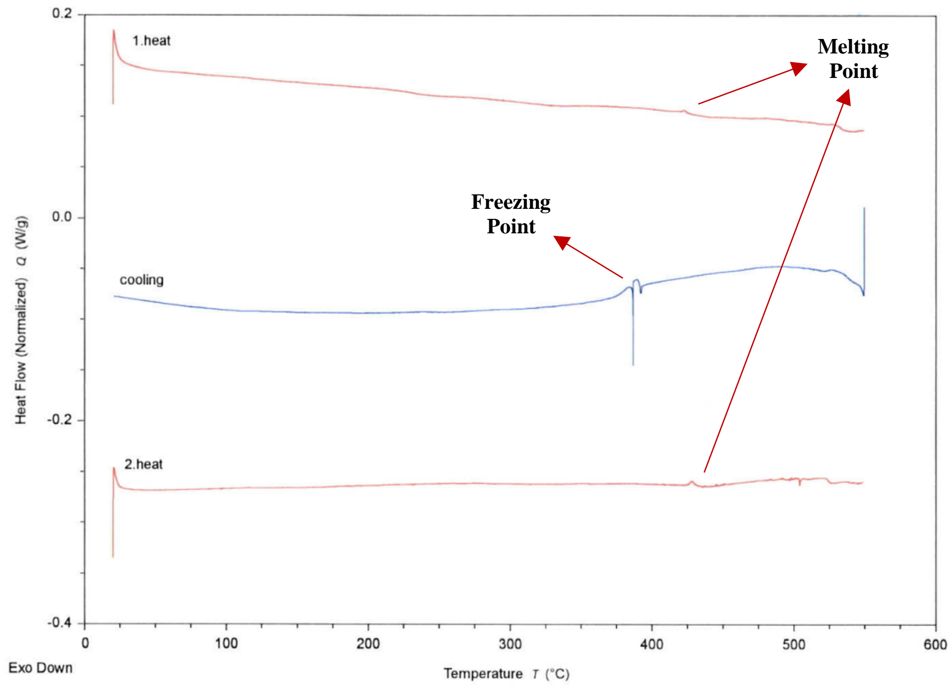


Figure 4.10 DSC curve of the as-coated film

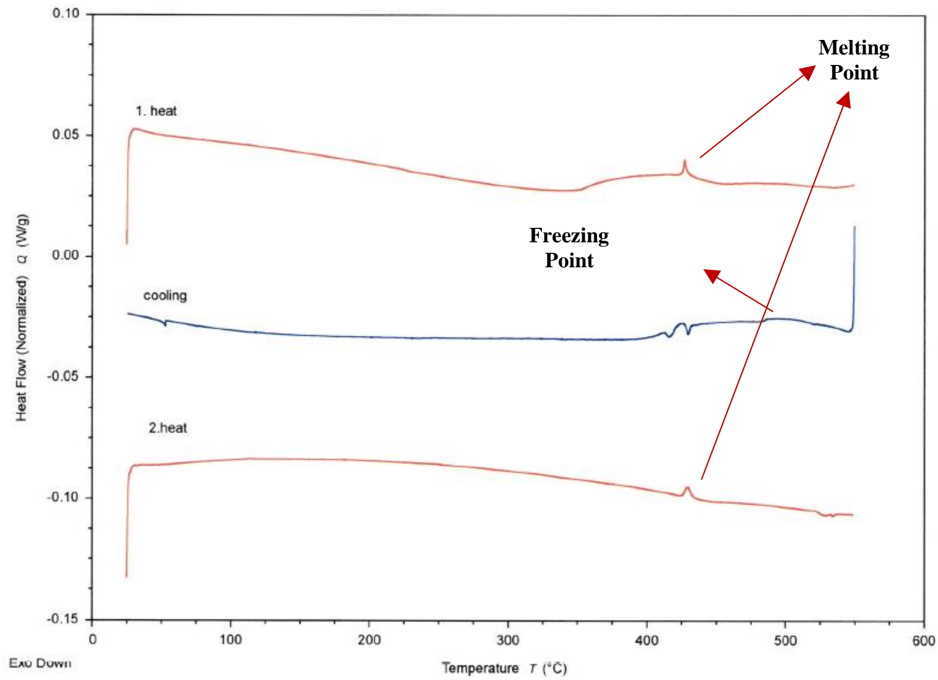


Figure 4.11 DSC curve of the annealed film

4.1.3 Wafer Bonding

The first three experiments were conducted after thermal evaporation with a 4-5 Å/s deposition rate. Process I has been used for the initial bonding experiment. Figure 4.12 is the SAM image of the bonded wafers. The position of the white circular area on the image corresponds to the region where the vacuum chuck holds the sample in place. It appears white since the wafer is separated due to the vacuum force exerted by the chuck, which means the wafers have weak bond strength. The strength could not be determined since the wafers separated during dicing.

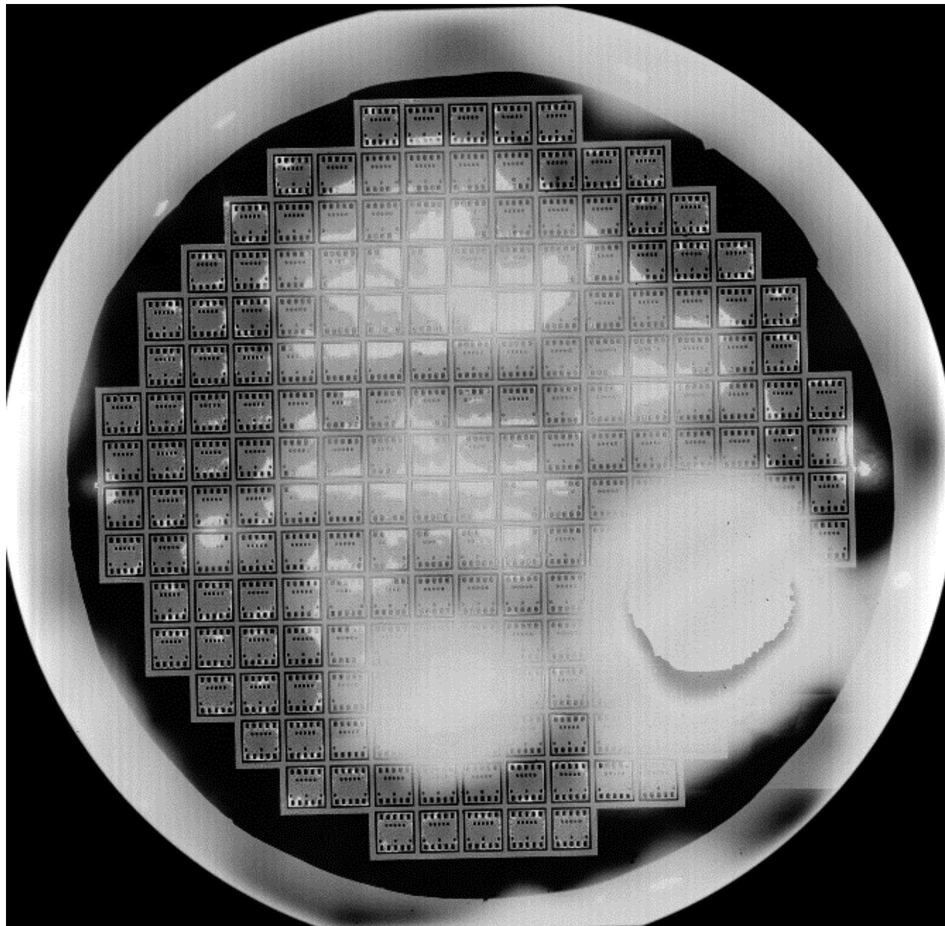


Figure 4.12 SAM image of the bonded wafers after the initial wafer bonding experiment

The interface of the separated wafers has been examined. Optical microscope images of both SiO_2 and Si_3N_4 surfaces are shown in Figure 4.13. The liquid squeezed out of the bond rings adheres well on both surfaces as the bisection has occurred at the passivation layers instead of the interface at some points. However, there is no adhesion on the actual bond area. Also, the amount of liquid squeezed out of the bond areas indicates there was not enough time for diffusion.

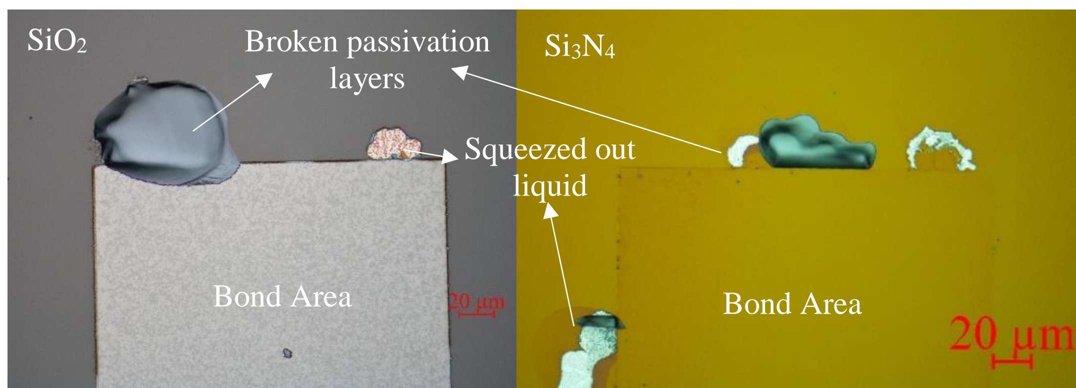


Figure 4.13 SiO_2 and Si_3N_4 surface of the bond interface

Figure 4.14 is the optical microscope image of the bisected interface. The amount of squeeze-out has increased significantly compared to the first bonding experiment.

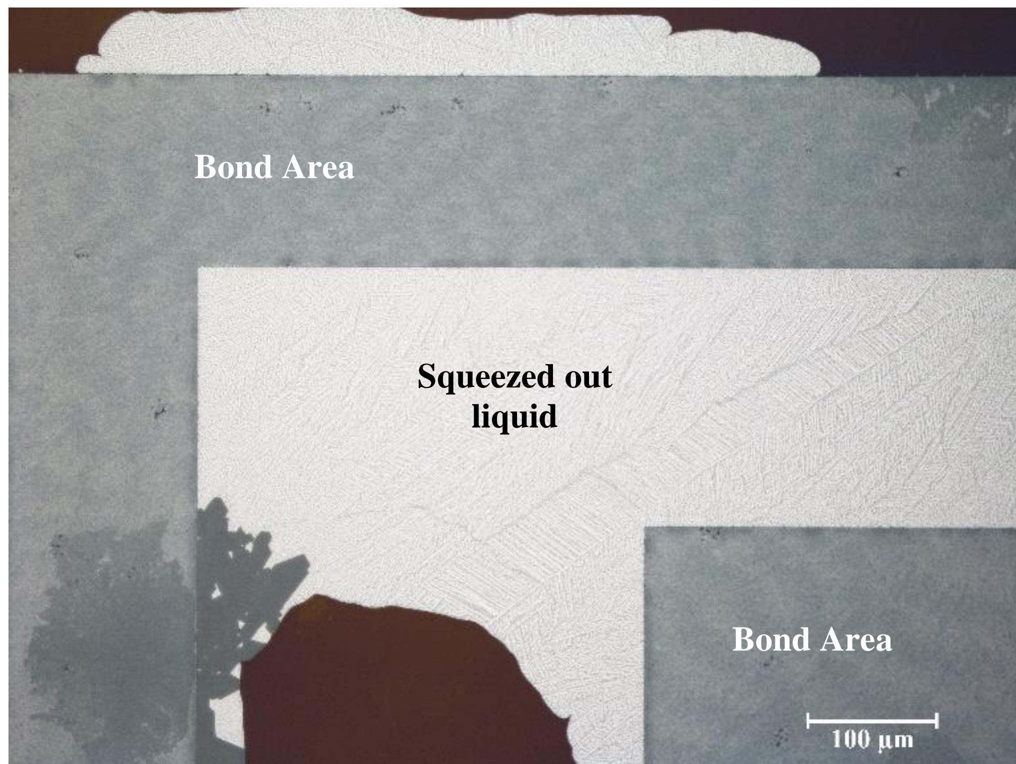


Figure 4.14 Optical image of the bonding interface

The same bonding process was used for the second wafer bonding experiment. However, the wafer with the metallic layer has been annealed at 550 °C for 20 hours before bonding to ensure a homogeneous microstructure.

Figure 4.15 is the SAM image of the bonded wafers. Although the wafers seem to be in integrity, the DI water from the SAM leaked in most of the dies, which means there is no hermeticity.

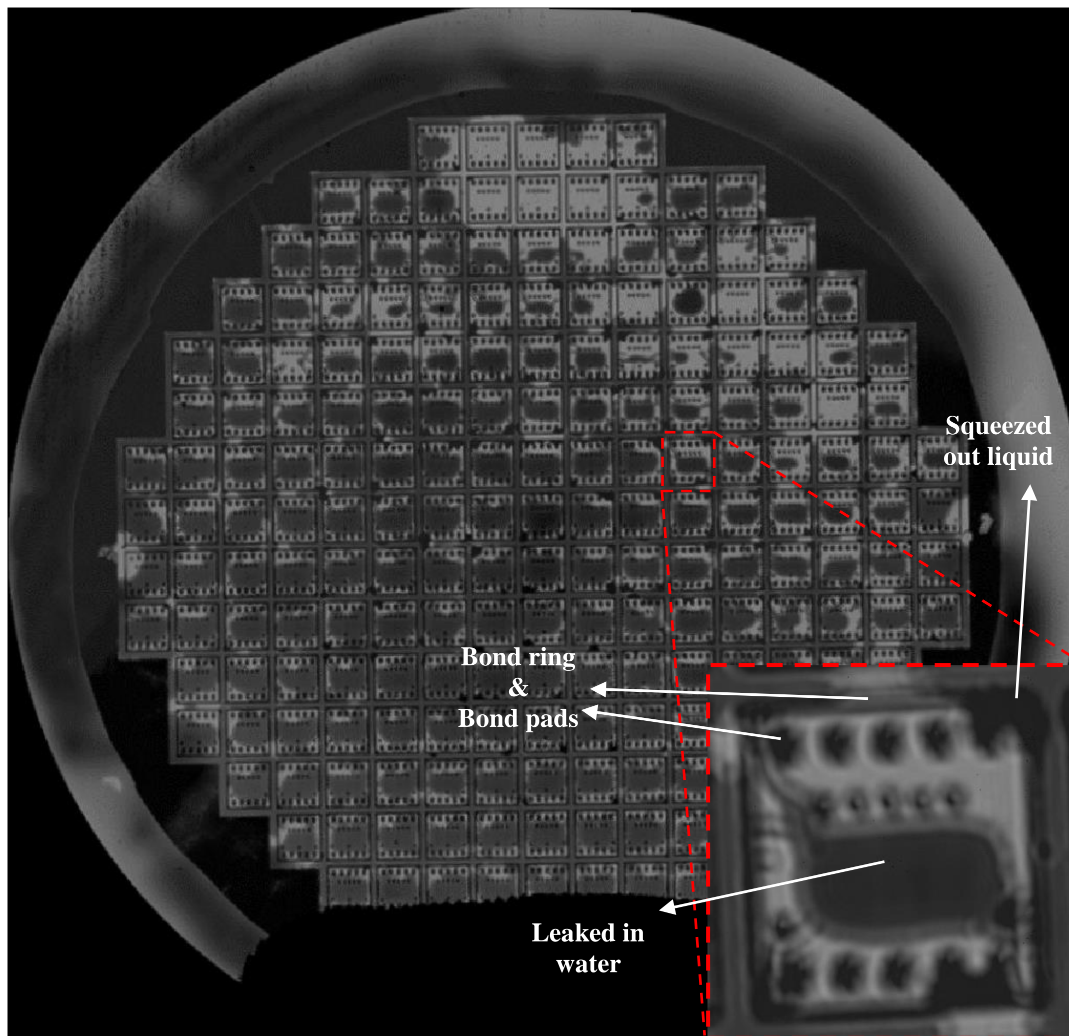


Figure 4.15 SAM image of the bonded wafers after wafer bonding with pre-annealing

Process II has been used for the next wafer bonding experiment. Also, the surface of the wafer with the metallic coating has been cleaned using inverse sputtering. Figure 4.16 is the SAM image of the wafers after bonding. SAM image shows a problem at the outer dies, which got separated during dicing. However, the remaining dies displayed higher strength. The weaker strength on the outer dies is related to the wafer bonding system. There is considerably less squeeze-out on the outer dies, which indicates that the force applied by the wafer bonding system is not uniform over the surface of the wafer.

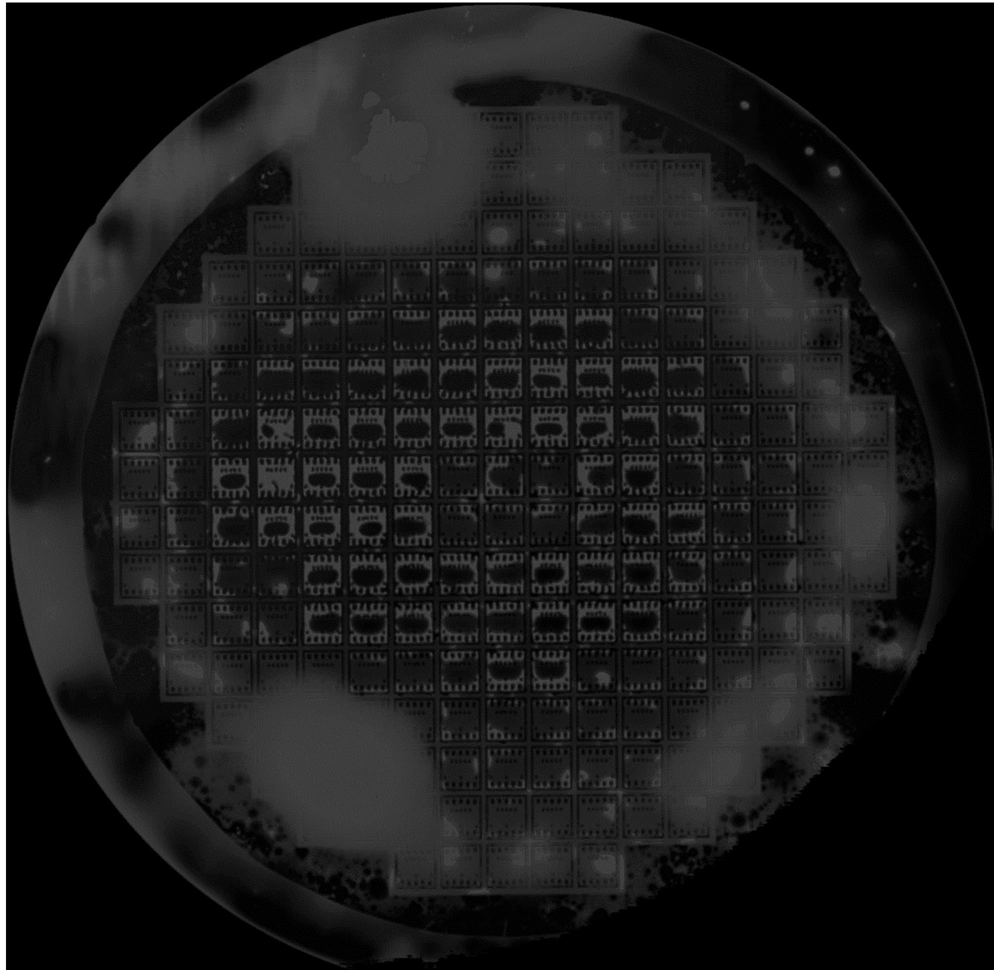


Figure 4.16 SAM image after wafer bonding with solid state bonding step

Shear test results of the pre-annealed and solid-state bonded wafer pairs are shown in Figure 4.17. The average shear strength of the pre-annealed sample appeared to be 16±4 MPa which increased to 24±5 MPa for the solid-state bonded wafers.

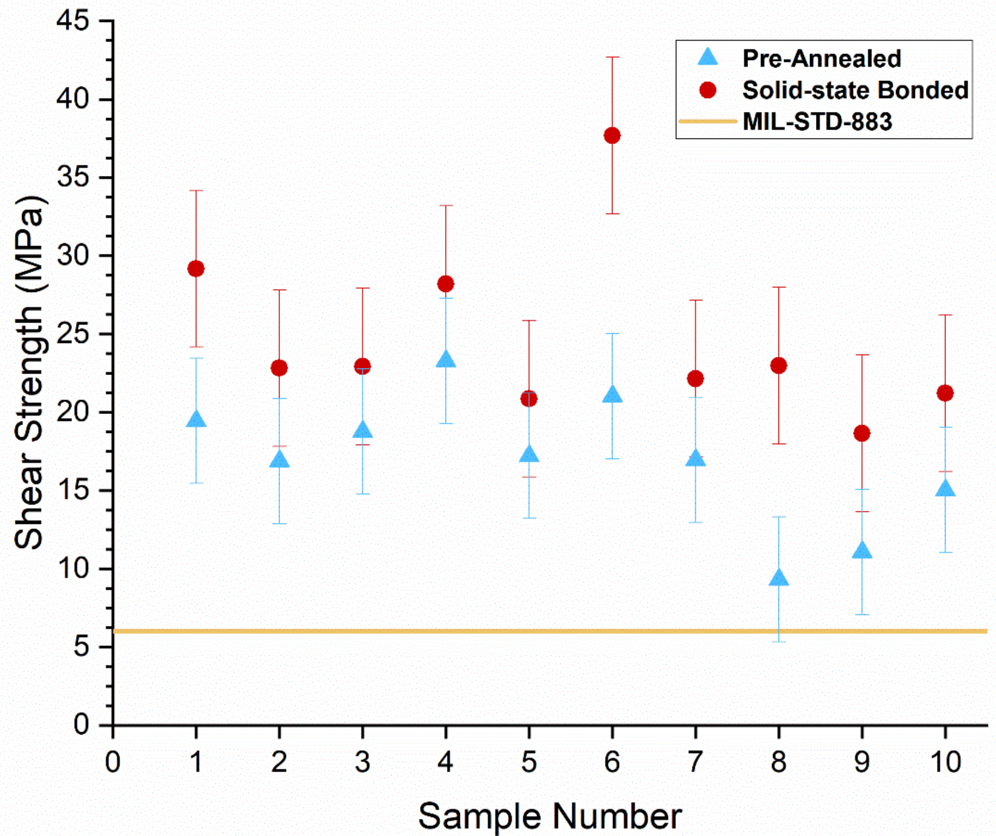


Figure 4.17 Shear strength results of the bonded samples

4.2 Co-Sputtering

4.2.1 Deposition and Annealing

Al and Ge have been co-sputtered on the substrate using the same parameters for each metal. Figure 4.18 is the SEM image of the cross-section. The deposited film appeared to be highly porous. EDS line and map profiles of the cross-section of the film are shown in Figure 4.19 and Figure 4.20, respectively. Both results have shown that the composition is uniform along the cross-section.

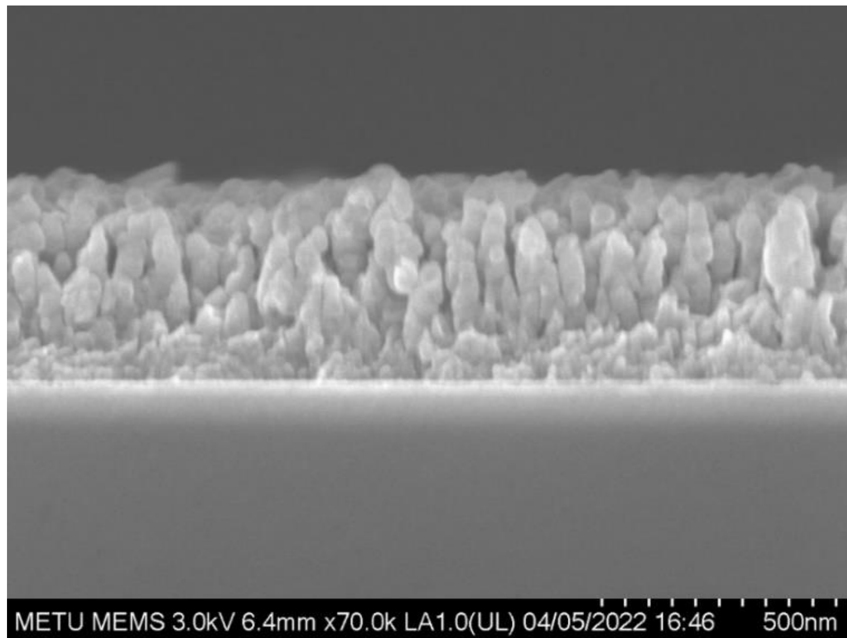


Figure 4.18 SEM image of the cross-section of the co-sputtered film

Annealing at 450 °C for 1 hour resulted in the microstructure shown in Figure 4.21. There is no eutectic morphology appearing after annealing. This results from sluggish diffusion between the metallic species caused by porosity. The deposition pressure has been reduced from 3 mTorr to 0.3 mTorr to minimize porosity. Thickness increased due to the longer mean free path, but the film was still porous.

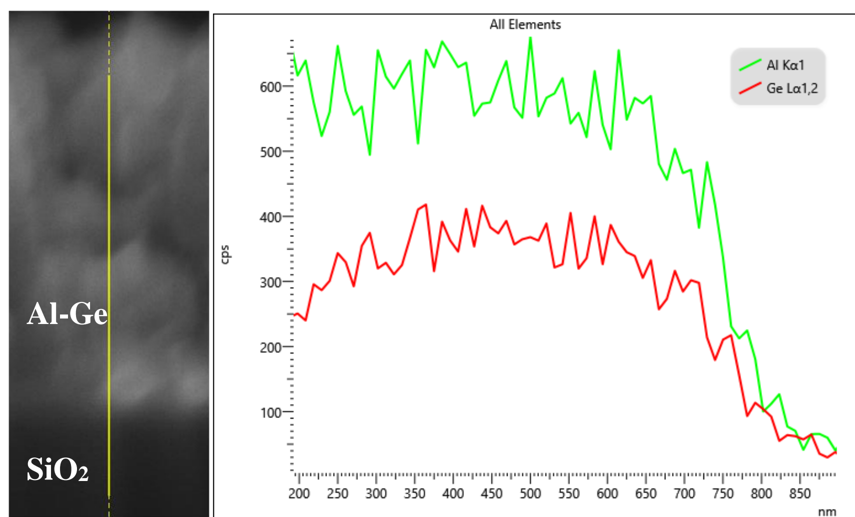


Figure 4.19 EDS line profile of the co-sputtered alloy

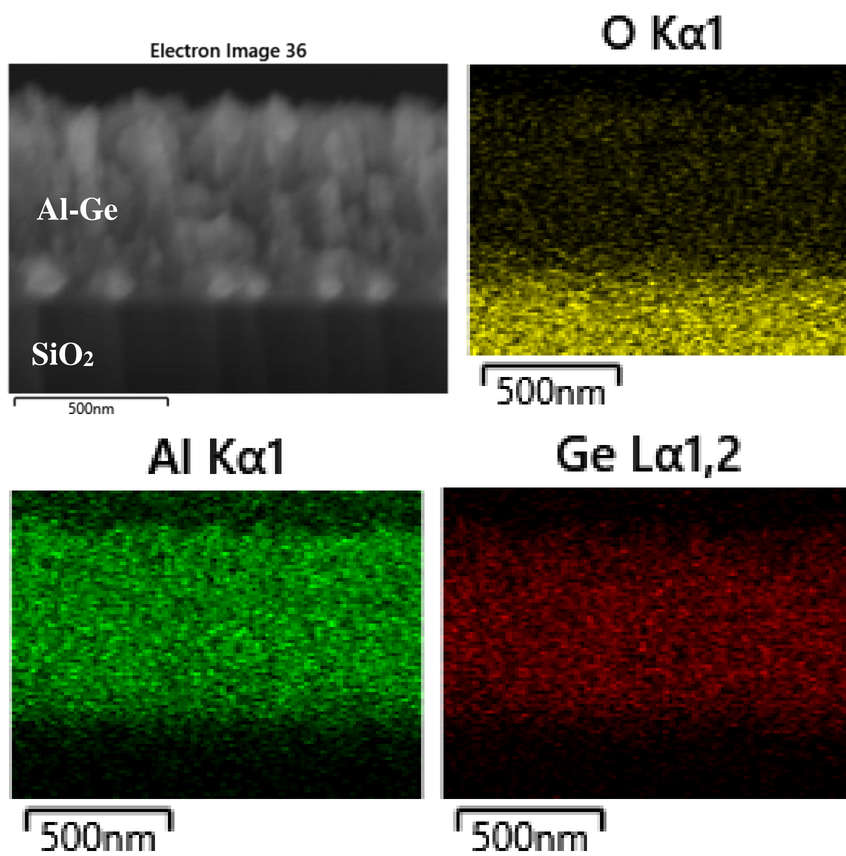


Figure 4.20 SEM image and EDS map of the co-sputtered film

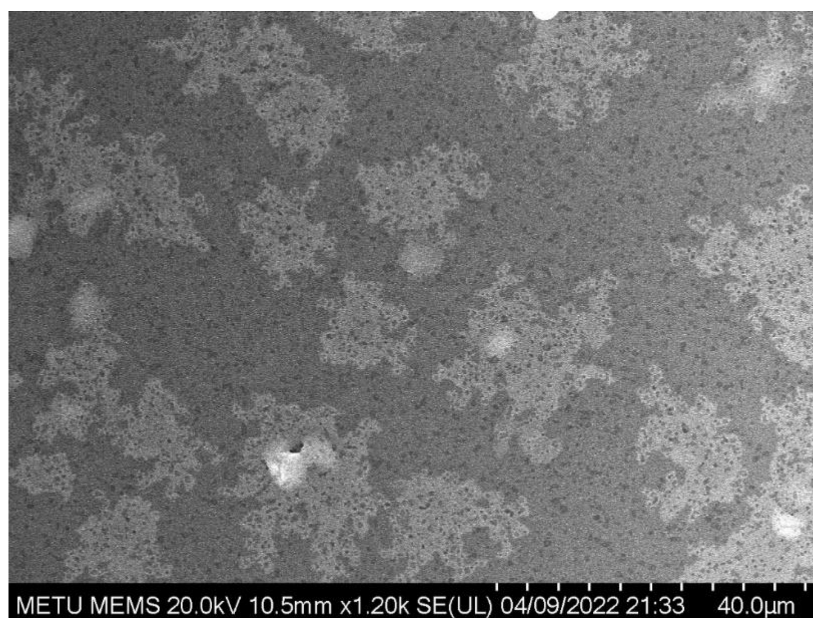


Figure 4.21 SEM image of the co-sputtered film after annealing at 450 °C for 1 hour

Figure 4.22-a is the SEM image of the film. Porosity seems to have increased sharply after 200 nm thickness. Hence, the following sample has been coated with a 200nm thick layer (Figure 4.22-b) and annealed. SEM image of the film after annealing is shown in Figure 4.23. Although there was further diffusion between the metallic species, there was no eutectic phase formation.

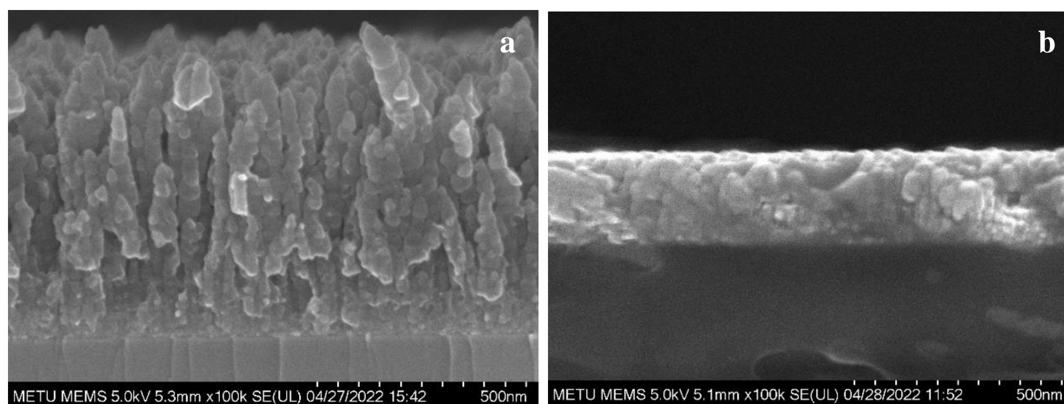


Figure 4.22 SEM images of the films after sputtering at 0.3 mTorr pressure

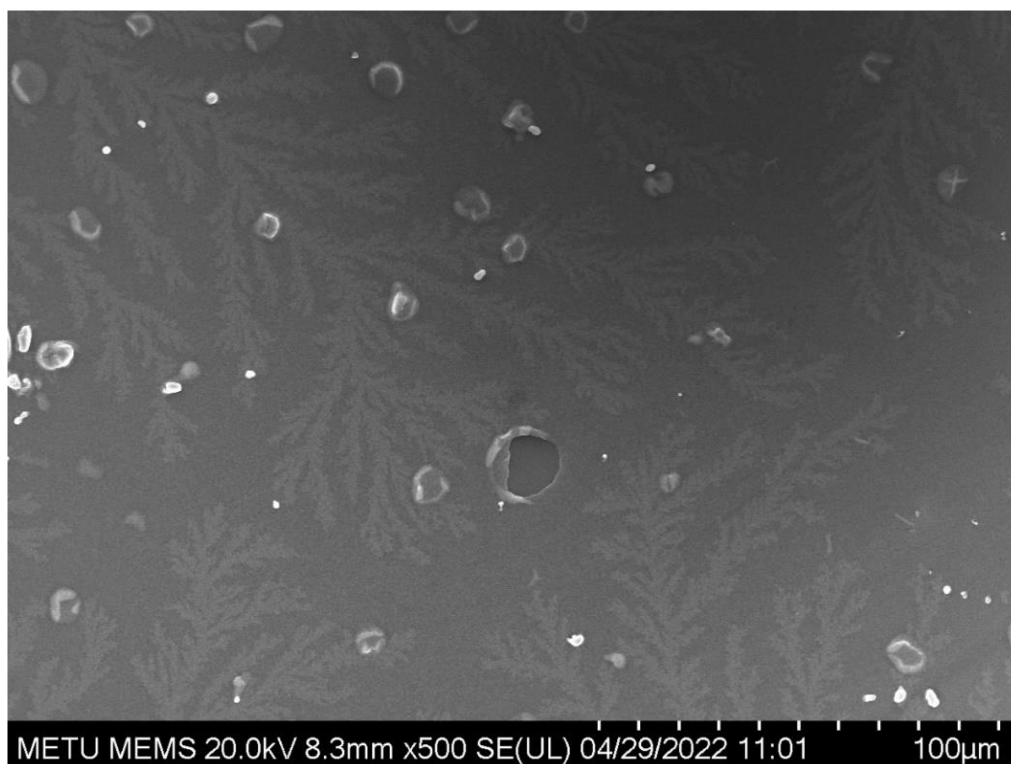


Figure 4.23 SEM image of the film after annealing for 1h at 450°C

The porosity of the deposited film decreased after coating at 30 mTorr pressure while the deposition rate dropped dramatically. Figure 4.24-a is the SEM image of the deposited film. Annealing at 450 °C for 1h resulted in a similar microstructure. Hence, the temperature has increased to 500 °C, resulting in only a trace amount of eutectic phase formation. Figure 4.24-b is the SEM image after annealing at 500 °C.

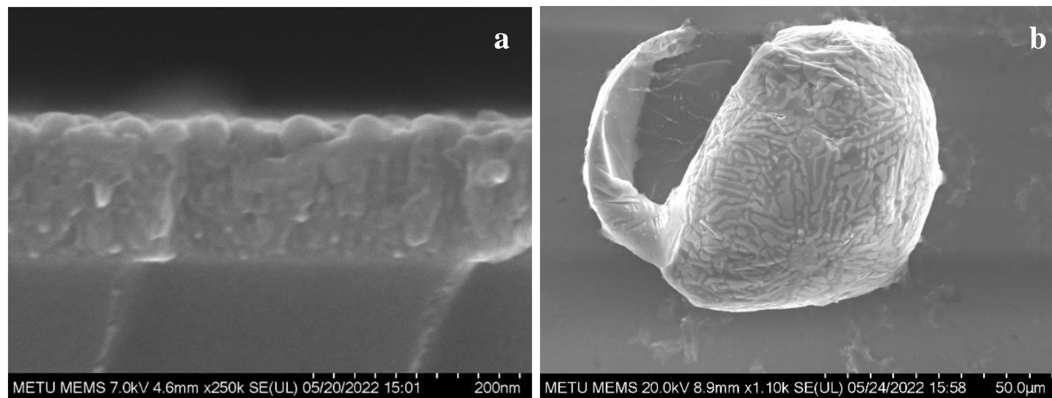


Figure 4.24 Cross-section of the as-deposited film(a) and microstructure of the annealed film after co-deposition at 30 mTorr pressure

4.2.2 Wafer Bonding

Co-deposition for wafer bonding has been performed at 30 mTorr pressure, from which the best results have been obtained. The wafer with the co-sputtered bond rings has been bonded to a glass wafer using Process II at 450 °C. OM images of the bond rings through the glass wafer are shown in Figure 4.25. There was no liquid formation detected. There is no SAM image of the bonded wafers since they separated easily after bonding.

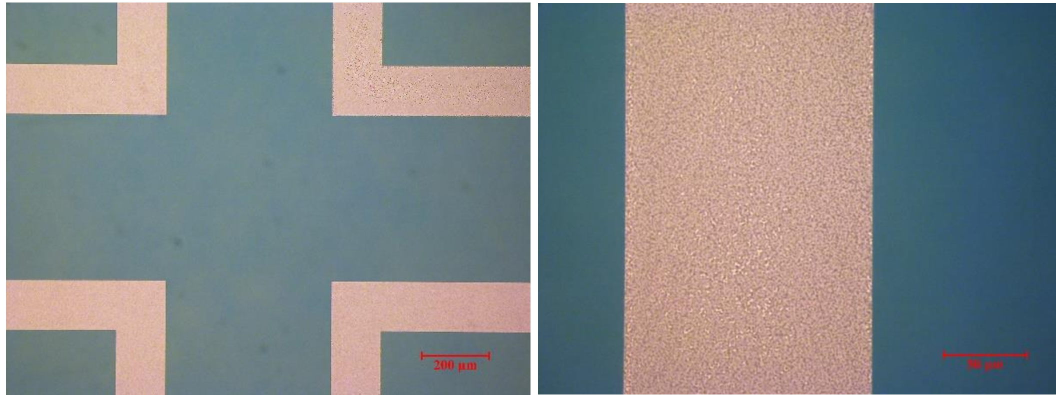


Figure 4.25 OM images of the bond rings through the glass wafer after bonding

4.3 Layer by Layer Deposition

4.3.1 Deposition and Annealing

The initial experiment for layer-by-layer deposition was conducted using magnetron sputtering. A 300 nm thick Al layer has been coated using a DC source with 300 W power, while 175 nm Ge has been coated using an RF source with 150 W power. Figure 4.26 is the SEM image of the cross-section of the deposited layers. The layers stack has been annealed at 450 °C for 1h hour under an N_2 atmosphere. Figure 4.27-a is the SEM image of the film after annealing. Although the eutectic morphology has occurred, there is some excess Ge in the microstructure. A Layer stack with a 0.45 thickness ratio has also been annealed to observe the morphology of pro-eutectic Al, the microstructure of which is given in Figure 4.27-b.

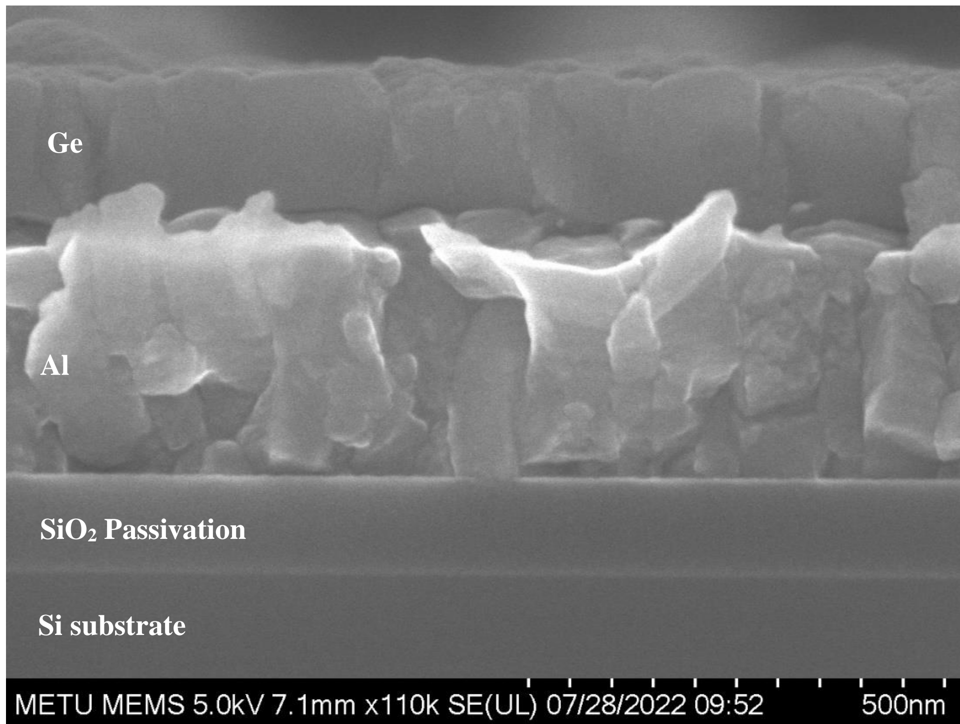


Figure 4.26 Cross-section of the Al/Ge layers deposited by sputtering

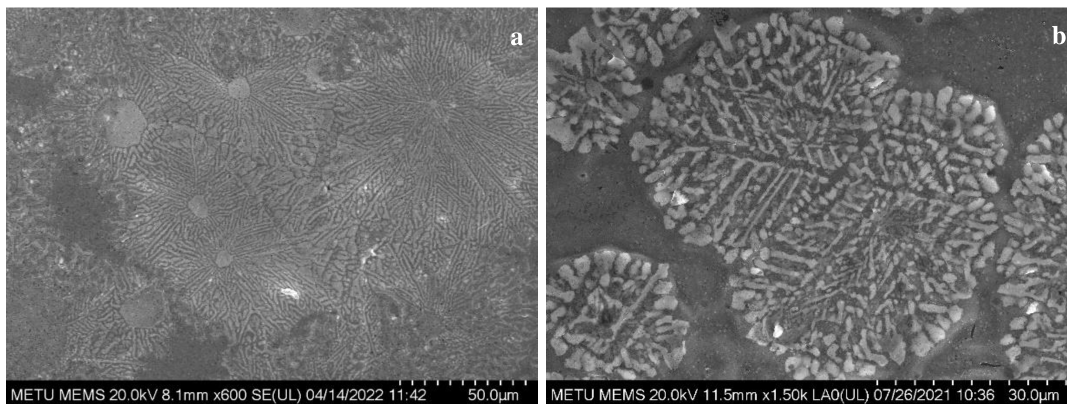


Figure 4.27 SEM image of the Al/Ge layer stack after annealing at 450 for 1 hour

The experiment has been repeated using thermal evaporation instead of sputtering. 300nm Al/175nm Ge layers stack has been coated on a Si wafer with a SiO_2 passivation layer using thermal evaporation. The layer stack has been annealed at 450 C for 1 hour under an N_2 environment, after which the alloy has displayed a eutectic phase with different morphology, as shown in Figure 4.28.

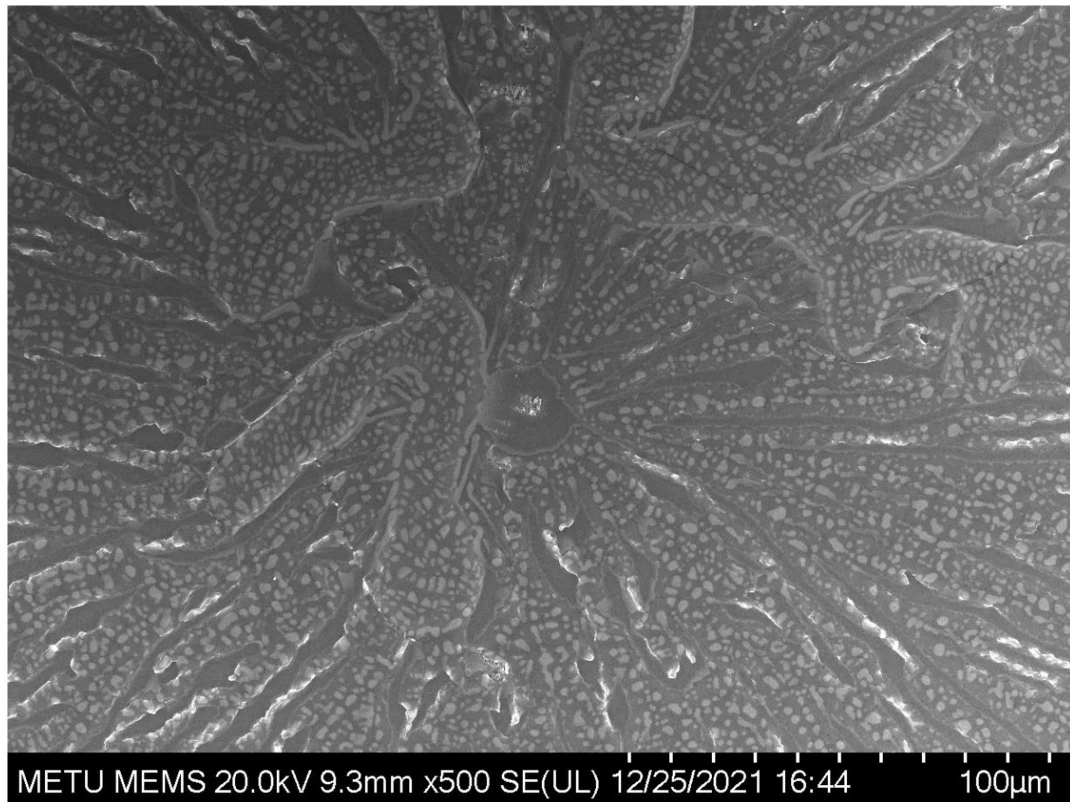


Figure 4.28 SEM image of the layer stack after annealing at 450 °C for 1 hour

4.3.2 Wafer Bonding

4.3.2.1 Bonding after thermal evaporation

The first wafer bonding experiment with a thermally evaporated layer stack was conducted using Process II with no prior surface treatment since it resulted in higher strength during previous experiments. Figure 4.29 is the SAM image after wafer bonding. The water inside the tank of the SAM has leaked into most of the dies.

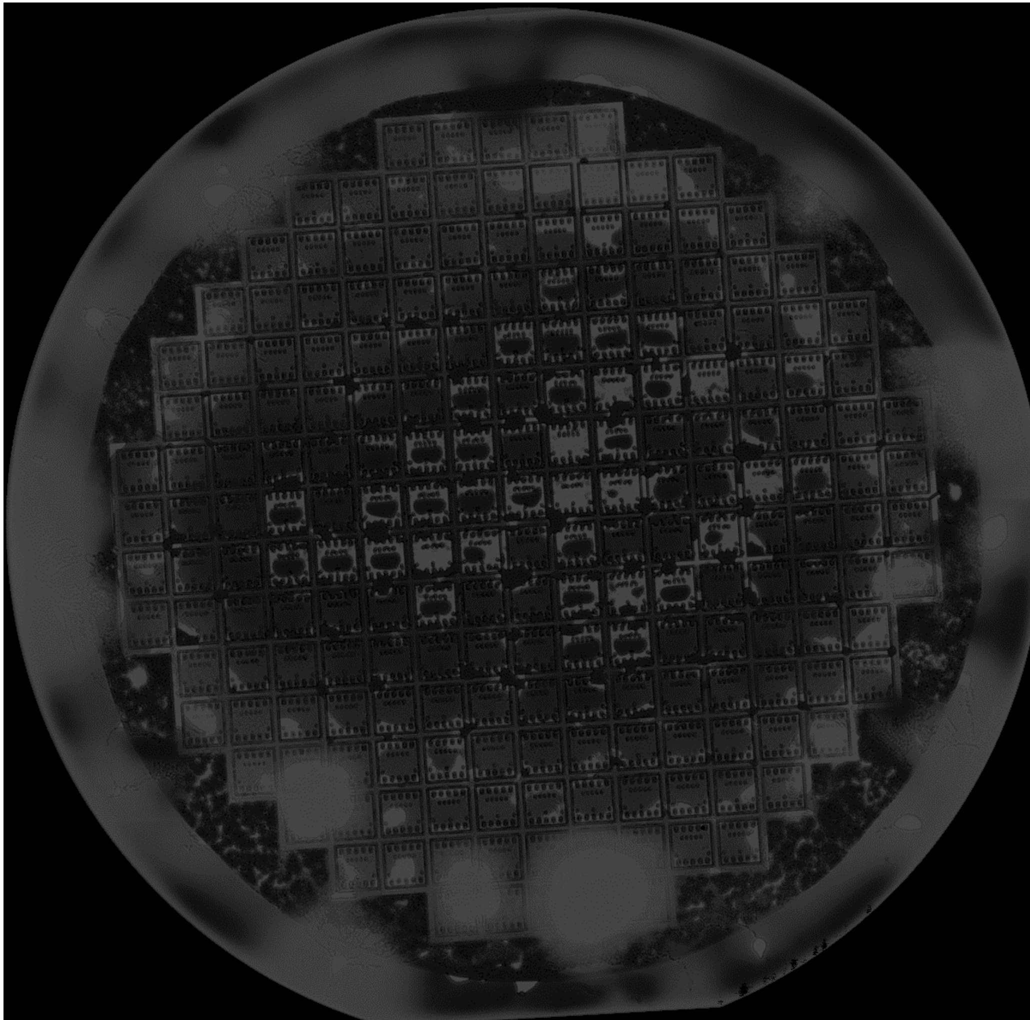


Figure 4.29 SAM image of the wafers after the first wafer bonding experiment

Inverse sputtering was applied to the wafer with the layer stack before wafer bonding for the second experiment. Figure 4.30 is the SAM image of the wafers after bonding. Although the outer dies are problematic, the water has not leaked into most of the dies. The majority of the problematic dies are in the two outermost lines of the wafer. Figure 4.31 a and b are the OM images of inner and outer dies, respectively. They seem to have the same dendritic microstructure. Hence, the problem is related to adhesion rather than the alloy's inherent properties, which indicates that inverse sputtering is not homogeneous throughout the surface since the distance between the DC source and the wafer is too short.

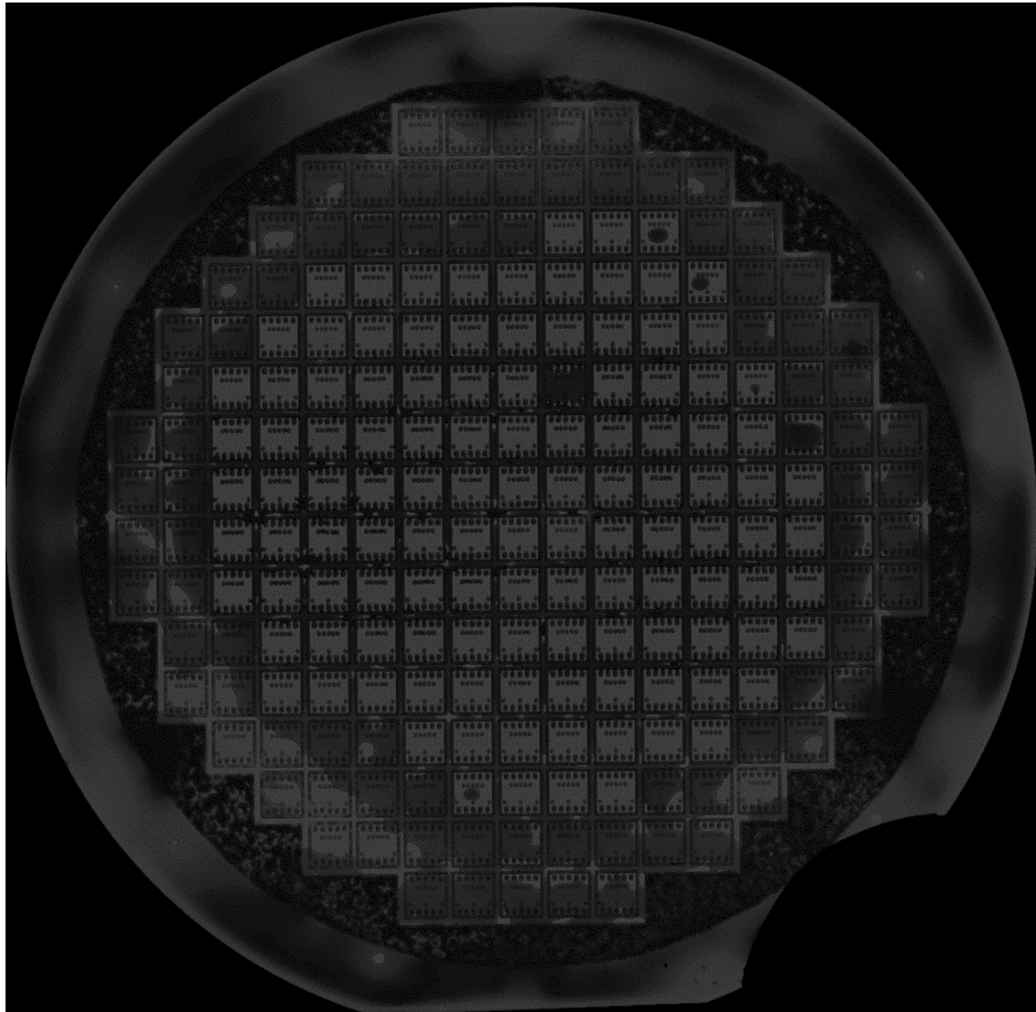


Figure 4.30 SAM image of the wafers after bonding with prior inverse sputtering

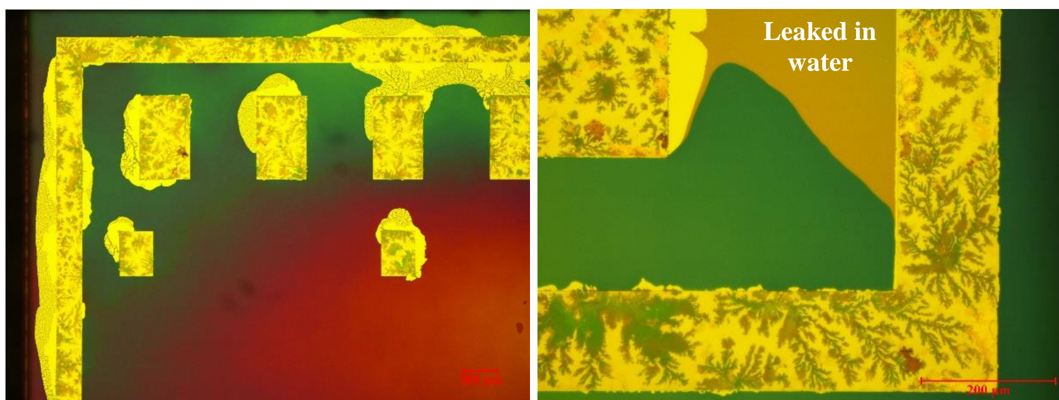


Figure 4.31 OM images of inner(a) and outer(b) dies

After the SAM examination, the wafer was diced for the shear test. The results are shown in Figure 4.32. The average shear strength of the dies appeared to be 52±10 MPa.

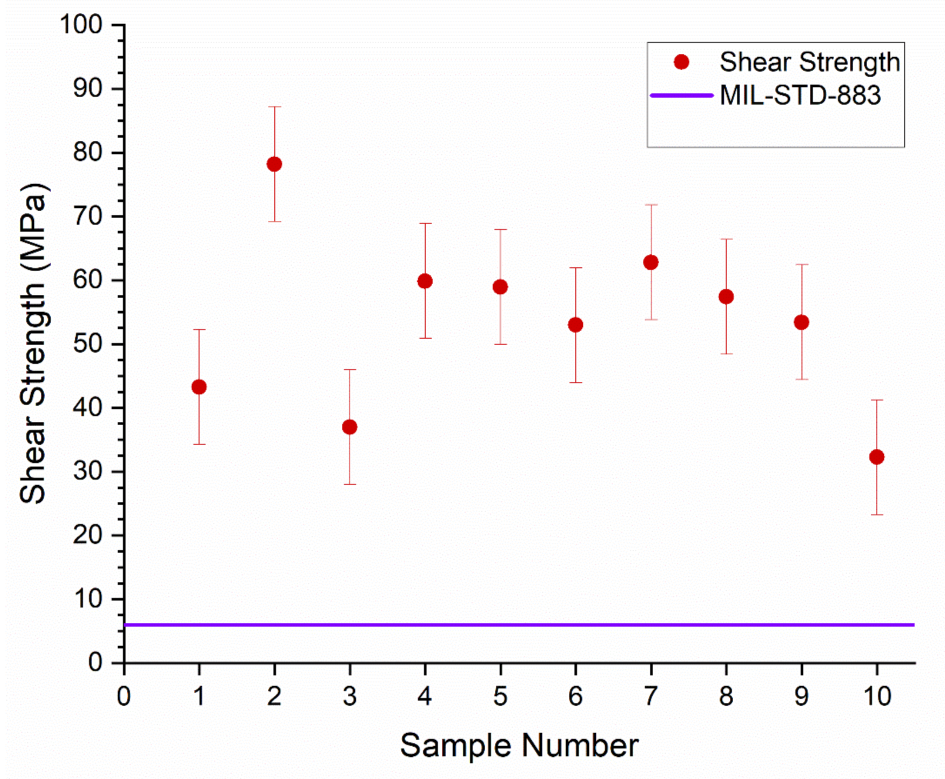


Figure 4.32 Shear test results after bonding wafer bonding with prior reverse sputtering

Figure 4.33 is the optical microscope image of a Si_3N_4 surface after the shear test. There are areas where the nitride surface has broken instead of the alloy or the interface. Also, Al of the squeezed-out liquid has remained on the surface while Ge remained on the other side.

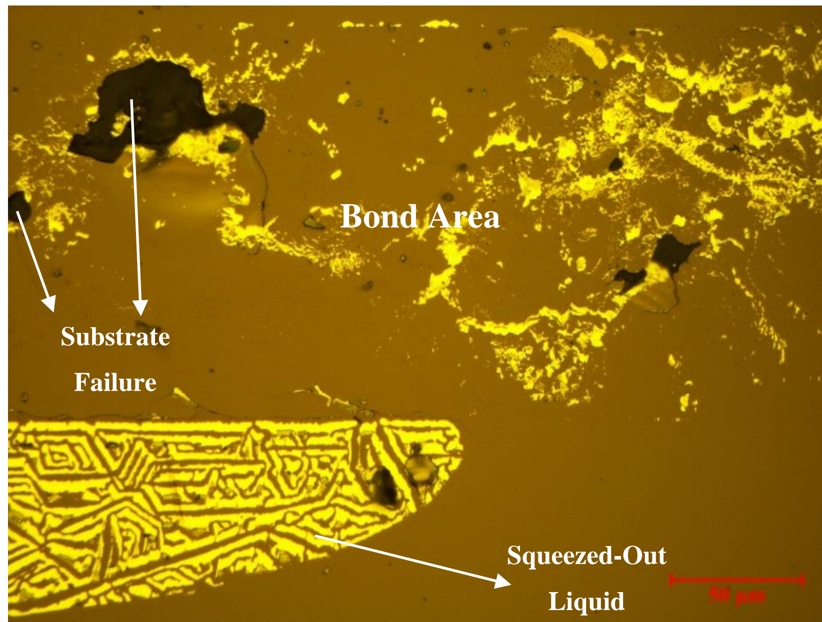


Figure 4.33 OM image of a Si_3N_4 surface after the shear test

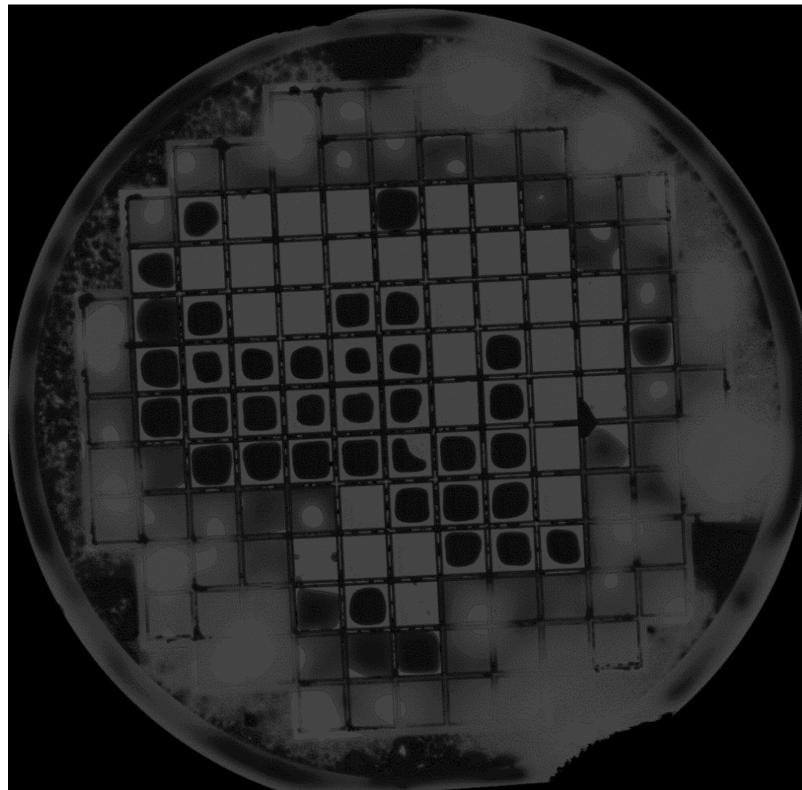


Figure 4.34 SAM image of the wafer after wafer bonding with Process I after reverse sputtering

For the next experiment, Process I was used with prior inverse sputtering. Figure 4.34 is the SAM image after bonding. Water leakage behavior is similar to that of the previous experiment.

Figure 4.35 is an OM image of a small portion of the bonding area around the center of the wafer. There is a significant increase in the amount of squeeze-out while dendrites are visible on the bond area, meaning liquid formation throughout the cross-section. There is a considerable amount of pro-eutectic Al in the squeezed-out liquid. However, the thickness ratio is maintained since Al provides ductility, and its amount will decrease when lower eutectic bonding temperatures are targeted.

Figure 4.35 OM image of the bonding area through the glass wafer

Figure 4.36 is the OM image of an outer die through the glass wafer. Although the same dendritic microstructure is discerned on the whole bonding area, there is a partial change in color since inverse sputtering is ineffective and the alloy does not adhere entirely to the glass wafer.

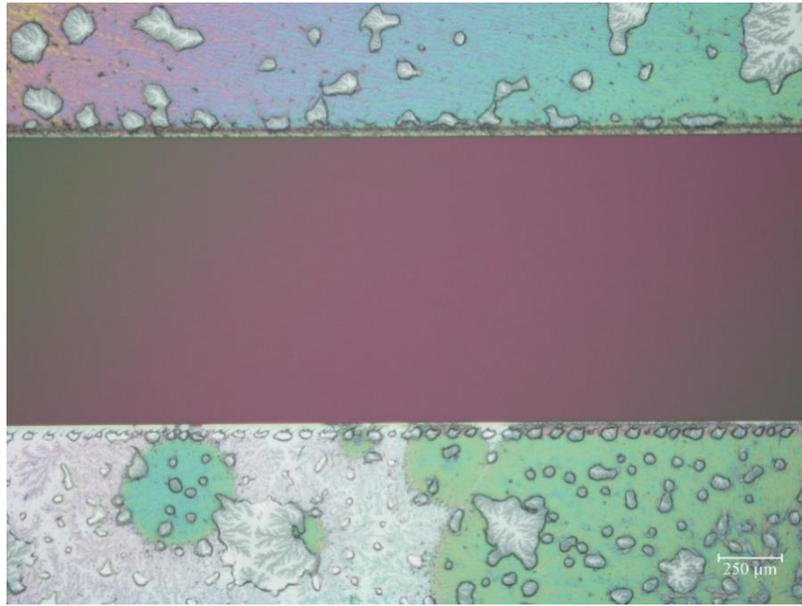


Figure 4.36 OM image of an outer die through the glass wafer

Figure 4.37 is a photo of the bonded wafers. Although there is no cavity on any of the wafers, the dies maintaining vacuum after bonding can be discerned due to the deflection of the glass on those dies.

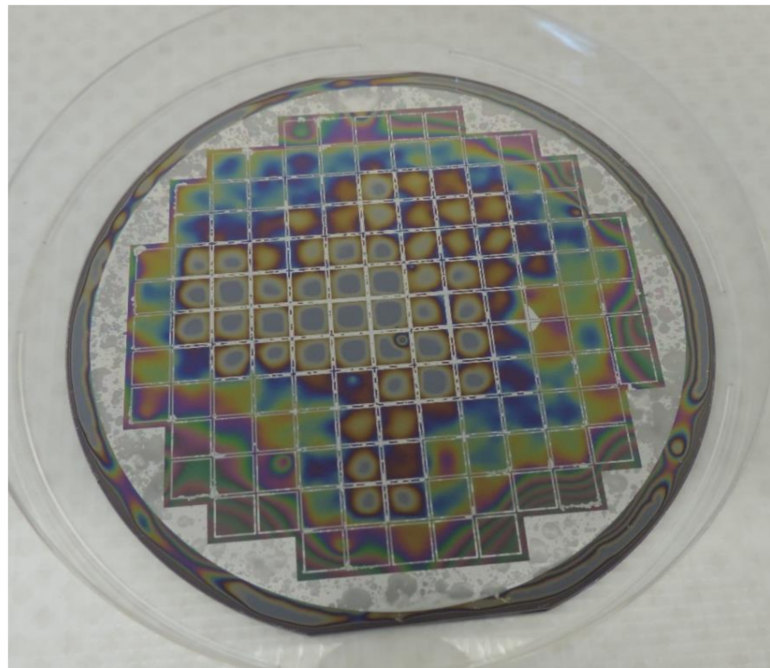


Figure 4.37 A photo of the wafers after bonding with Process I

Although the number of dies that do not leak water appears to be the same after both Processes I and Process II, the first experiment with cavities was conducted using Process II since there is significantly less squeeze-out.

Figures 4.38 a and b are OM images of the dies and the alignment marks after the cavities are etched. The alignment mark marked as "I" in the figure is used for the alignment during lithography for the cavities. It has been deformed since it was exposed to BHF and DRIE plasma. The second alignment mark is protected by the PR during these processes to be used for bond alignment. The depth of the cavities has been measured as 120 µm. Figures 4.39 a and b are photos of the wafer with cavities before and after bonding.

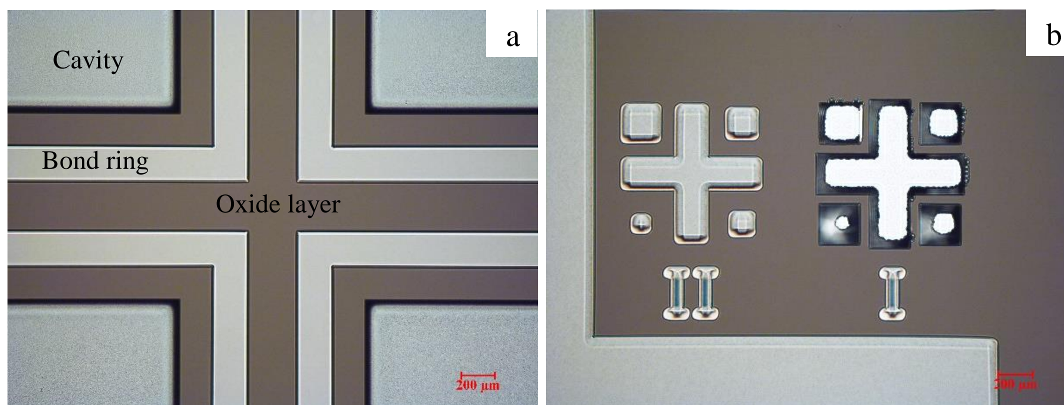


Figure 4.38 OM images of the dies (a) and the alignment marks (b) after cavity etching

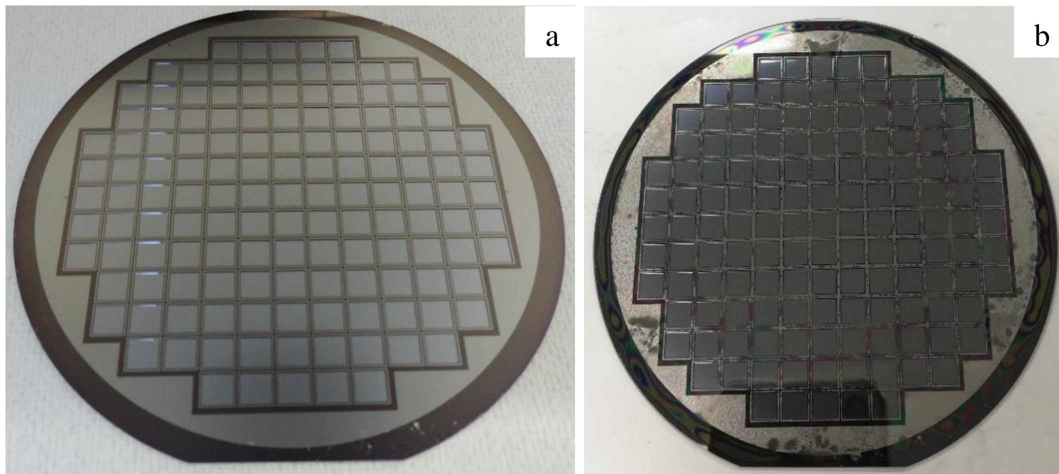


Figure 4.39 Photos of the wafer with cavities before(a) and after(b) bonding with Process II

Figure 4.40-a is a SAM image of the bonded wafers, while Figure 4.40-b is a SAM image of the same sample after it is kept in the water tank for 24 hours. The water leaked into the outer cavities in the earlier samples. Unlike the sample bonded using Process I, there is no squeeze-out into the dies. Figure 4.41 is a photo of the wafer after 48 hours in the water tank of the SAM. The outer dies that have leaked water are easily discernable. He leak test has been performed on the samples. However, the test results have been omitted since the He spectrometer's sensitivity was insufficient to detect leakage from packages of the subject size.

The experiment has been repeated with approximately 400 μm deep cavities for cap deflection measurements. 3.4 μm deflection has been measured on dies near the center of the wafer. The thickness of the membrane has been measured as 120 μm after the wafers are bisected.

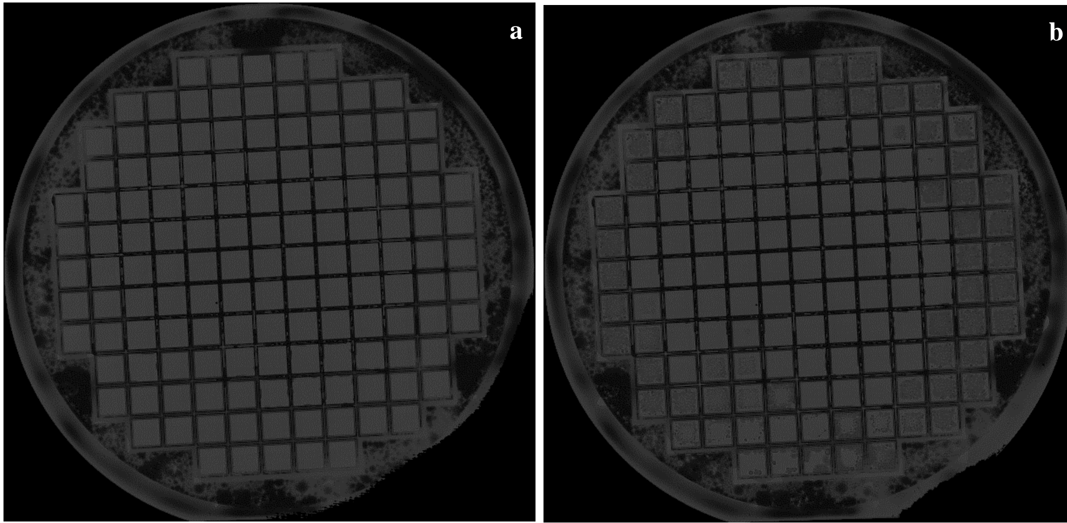


Figure 4.40 SAM of the wafer with cavities right after bonding(a) and after 24 hours in the water tank(b)

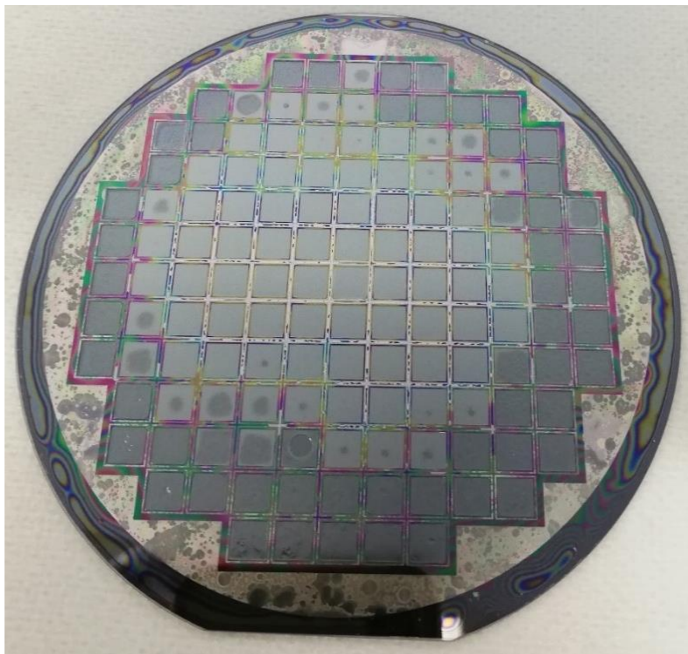


Figure 4.41 Photo of the bonded wafers after 48 hours in the water tank

4.3.2.2 Bonding after sputtering

The first wafer bonding experiment with sputtered layers was conducted using Process II. Figure 4.42-a is the SAM image of the bonded wafers after 24 hours in the water tank. There was no leakage into the outer bond ring. Hence, the dies have been examined using SAM after dicing. Figure 4.42–b is an image of an outer die that leaked water, while Figure 4.42-c is an image of a die with no leakage.

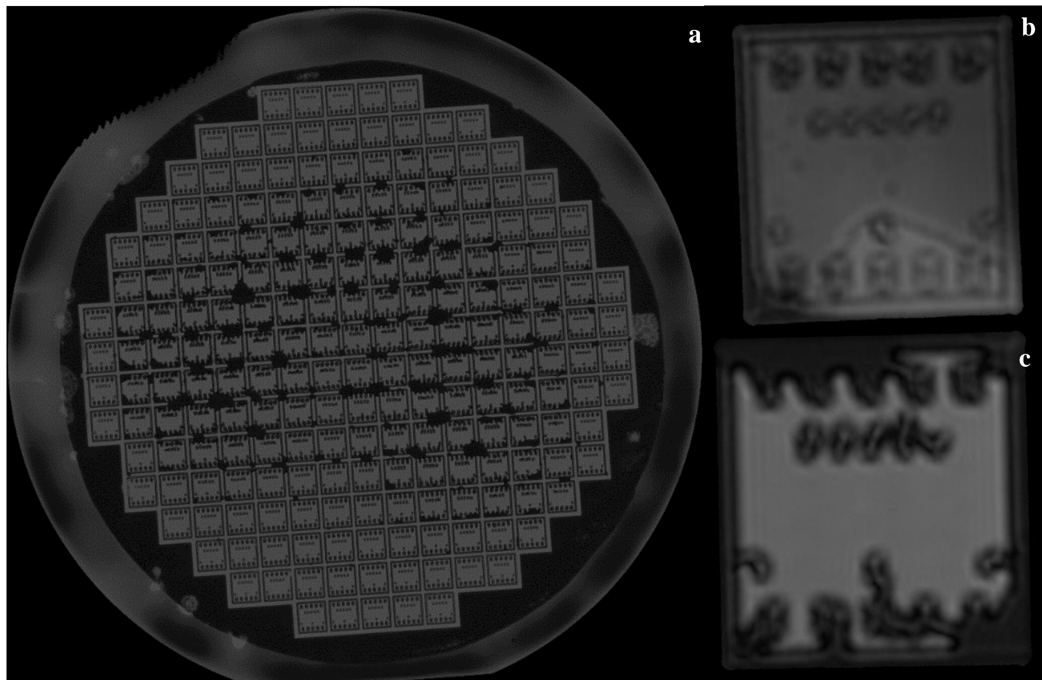


Figure 4.42 SAM image of the bonded wafers

OM images of the bonded wafers through the glass wafer are given in Figure 4.43. Unlike the results of the bond rings coated using thermal evaporation, the bond rings have the same eutectic morphology as the squeezed-out liquid.

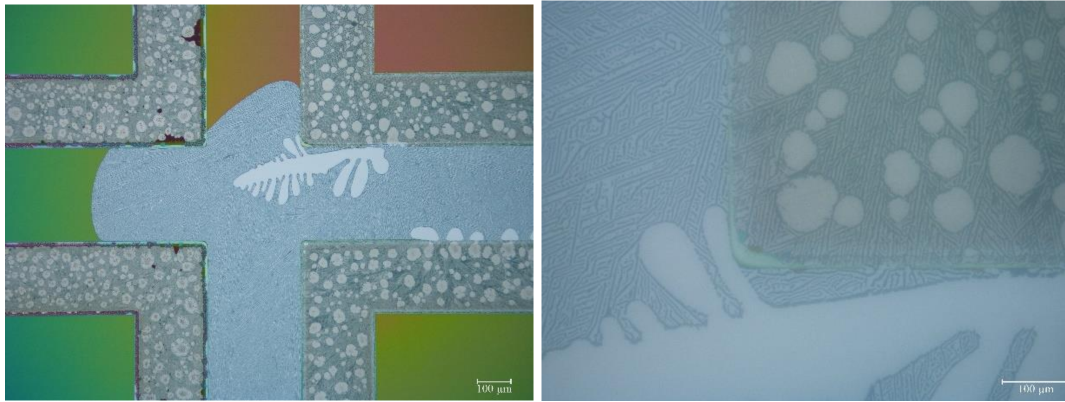


Figure 4.43 OM images of the bonded wafers through the glass wafer

Shear strength and microstructure results being promising, the experiment has been repeated with eutectic bonding temperatures of 440, 435, and 430 °C. Figure 4.44 is the SAM image of the wafers after bonding at 440 °C. A little water leaked into the dicing streets, but no water leakage into the dies has been observed.

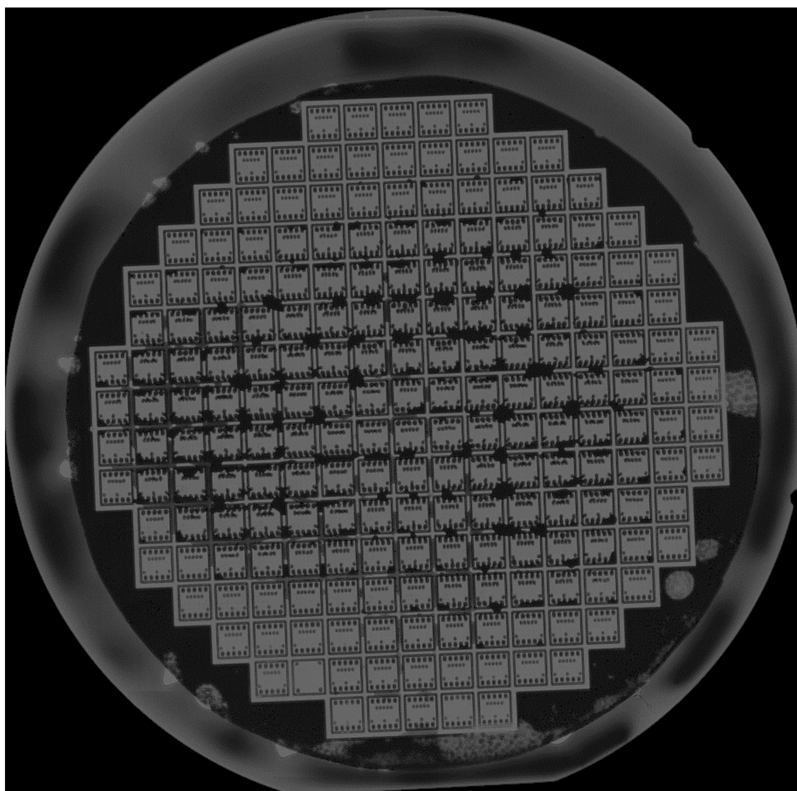


Figure 4.44 SAM image of the bonded wafers after bonding at 440°C

Figure 4.45 is an OM image of the bond rings after through the glass wafer after bonding. Although it is close to the eutectic structure of the squeezed-out liquid, it does not have the same morphology as it has after bonding at 450 °C.

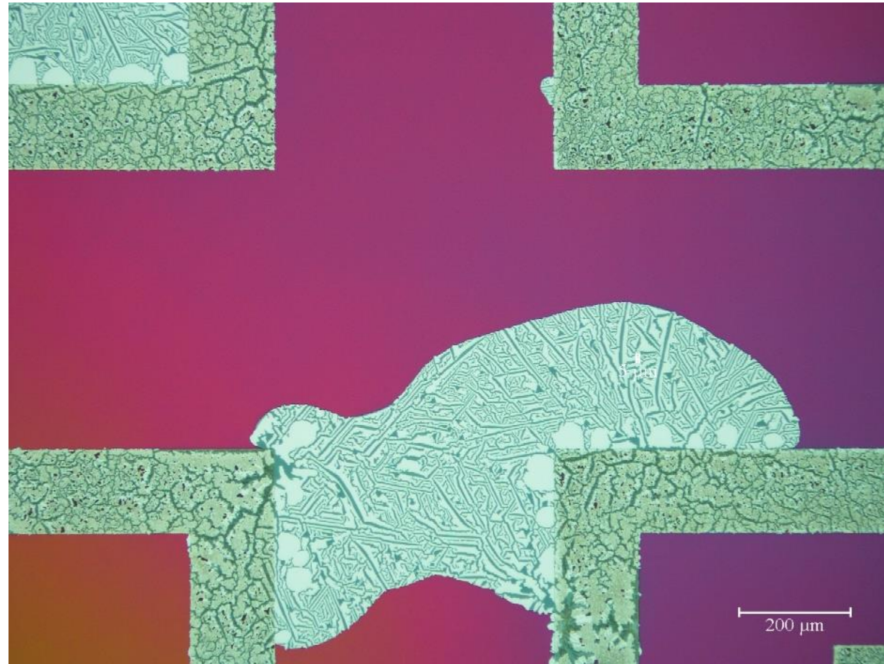


Figure 4.45 OM image of the wafers through the glass wafer after bonding at 440°C

OM images of the bond areas after bonding at 435 °C and 430 °C are given in Figure 4.46 and Figure 4.47, respectively.

The amount of liquid squeezed out of the bond decreased significantly at 430 °C. The microstructure of the bond on the bond area is similar to those shown in Figure 4.6 and Figure 4.21, which are products of insufficient interdiffusion between Al and Ge. Although vacuum sealing has been observed based on cap deflection, it could not be maintained since the dies have been bisected during dicing because of their low bond strength.

Figure 4.46 OM image of the wafers through the glass wafer after bonding at 435°C

Figure 4.47 OM image of the wafers through the glass wafer after bonding at 430°C

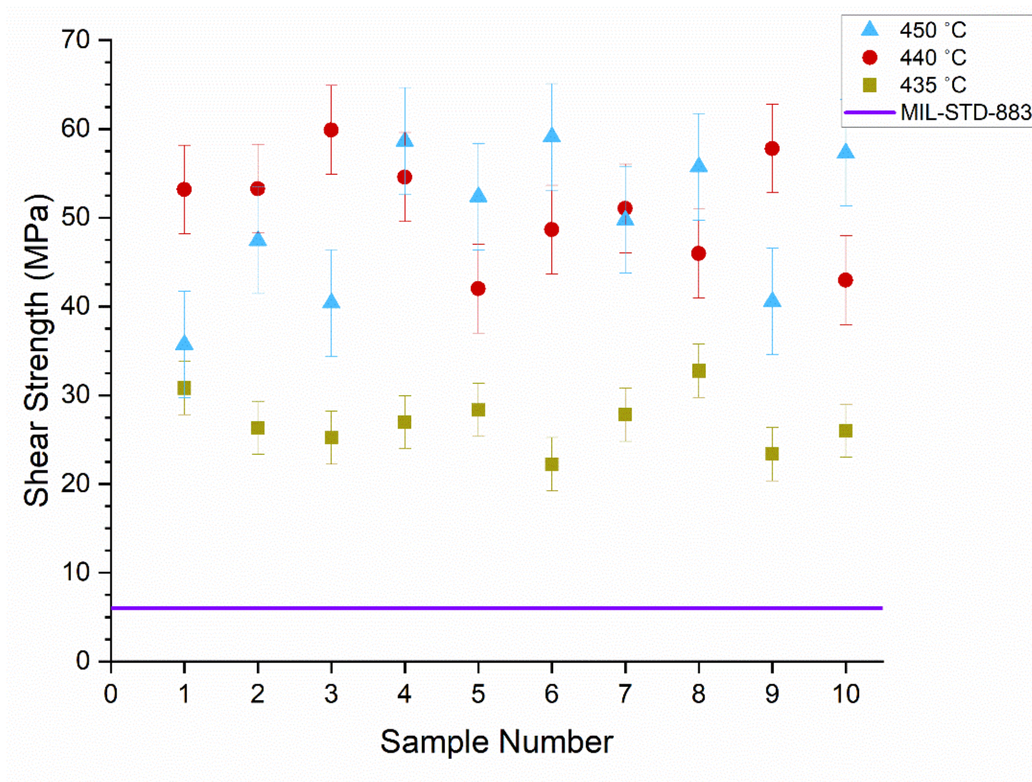


Figure 4.48 Shear strength of the dies after bonding at 450, 440 and 435°C

Shear strength results of the dies after bonding at both 450, 440, and 435 °C are given in Figure 4.48. The average shear strength after bonding at 450 °C is 49±6 MPa, while it is 51±5 MPa after bonding at 450 °C. The average strength has decreased to 27±3 MPa after bonding at 435 °C. The shear strength of the samples bonded at 430 °C could not be measured since they had been broken during dicing. The bonding experiment at the lower temperatures has been repeated for the cap deflection test with 125 μm membrane thickness. Approximately 10.5 mm deflection has been measured, which remained after dicing. According to the data in Figure 3.19, the deflection shall not exceed 4 μm. It appeared as 10.5 μm since membrane thickness after DRIE was not uniform, and it was around 80 μm near the edge of the membrane. Cross-section SEM images of the membrane near the edge and in the mid-area are given in Figures-a and b, respectively.

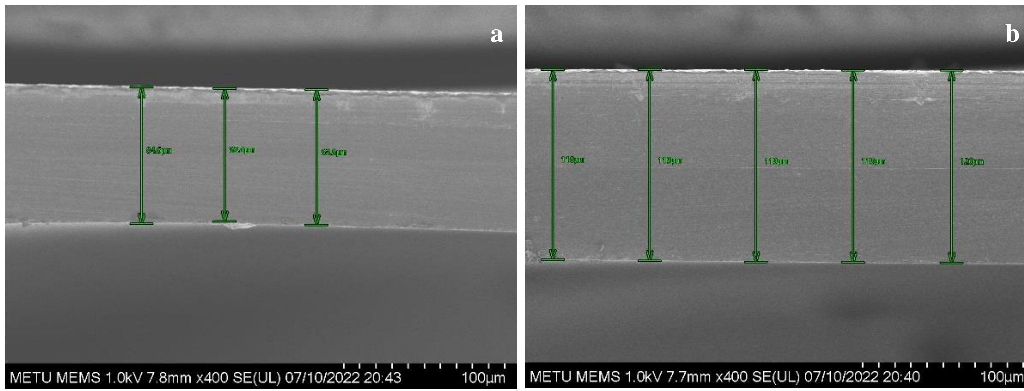


Figure 4.49 Cross-section SEM images of the membrane near the edge(a) and in the mid-area(b) of the die

CONCLUSION & FUTURE RECOMMENDATIONS

The Al-Ge eutectic alloy system has been investigated for wafer-level vacuum packaging of CMOS-based devices. The electronic packaging using Al-Ge in this system has several advantages. First of all, both Al and Ge are CMOS-compatible materials. Secondly, wafer bonding can be performed by coating the Al/Ge layer stack on only one wafer since the alloy adheres on passive surfaces without needing an adhesion layer. Hence, vacuum packaging can be performed with no additional process step on the device wafer. The main disadvantage of the system is that the eutectic melting temperature is close to the CMOS process temperature limit. So, obtaining a sufficient amount of liquid at the minimum bonding temperature is essential.

Initial experiments were based on reducing the time required for diffusion to form the eutectic composition. The eutectic alloy was fabricated using arc melting, which was later coated on the cap wafers using thermal evaporation. Al and Ge segregated during thermal evaporation due to different vapor pressures of the components. The samples have been annealed to observe the final microstructure after bonding. The eutectic morphology appeared only after extended heat treatment, which means the diffusion between Al and Ge is sluggish. Also, it seemed to be challenging to maintain the composition during coating. Although the samples obtained using this method have an average strength of 24 MPa, the vacuum level inside the packages could not be maintained. Co-sputtering has been tried to get a bonding material already in the eutectic composition. Coated films have appeared to be highly porous, resulting in even more sluggish diffusion than that after thermal evaporation. The wafer bonding experiment conducted using the co-sputtered film had no integrity, causing the wafers to be bisected easily after bonding.

The layer-by-layer deposition has been tried using both thermal evaporation and sputtering. A 175 nm thick Ge has been deposited over a 300 nm thick Al layer. Vacuum sealing at 450 °C has been achieved using thermal evaporation and sputtering. The results being more promising, the bonding temperature has been reduced to 435 °C with the sputtered layer stack. Although there was no significant difference between the samples bonded at 450 °C and 440 °C, the average shear strength decreased to 27 MPa at 435 °C. Although vacuum sealing has been achieved at 430 °C, the vacuum inside the dies has been due to the low bond strength.

As a continuation of this study, the adhesion performance of the material on other passive surfaces, such as SiO_2, Al_2O_3, or TiN can be investigated. The sluggish diffusion of the co-sputtered film is related to its porous structure. Changing the deposition pressure affected the porosity only slightly. The performance of the co-sputtered film may be re-investigated after reducing the porosity by heating the substrate during deposition.

Undercooling behavior of liquids may be evaluated to further reduce the heat input into the devices. The wafers can be bonded at the melting point or even at lower temperatures if the liquid formation is initiated by heating the samples to higher temperatures for a short time.

After shear tests, the microstructures and optical images indicate that squeezed-out liquids adhere to the passive surface better than the surfaces in the designated areas since they are not exposed to atmospheric conditions before bonding. New bond ring designs can be devised so the actual sealing areas are initially empty and filled by the squeezed-out liquid.

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