A WAFER LEVEL VACUUM PACKAGING TECHNOLOGY FOR MEMS BASED LONG-WAVE INFRARED SENSORS

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ABSTRACT

A WAFER LEVEL VACUUM PACKAGING TECHNOLOGY FOR MEMS BASED LONG-WAVE INFRARED SENSORS

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This thesis proposes a new approach to obtain a wafer level vacuum packaging that satisfies the requirements of the thermal sensors at low cost and with high performance. The moth-eye structures are formed on both side of a polished flat silicon wafer without any cavity to allow the transmission of the infrared radiation in long wave infrared region (LWIR). Then, this wafer is bonded to another spacer wafer using Au-In Trans-liquid phase (TLP) approach that allows bonding at low temperature (around 200℃); the advantage of the TLP approach is that it can handle very high temperatures (such as 500℃) after the bonding is complete. This allows the use of glass frit bonding of the cap wafer stack to the sensor wafer using high temperature bonding approaches such as glass frit at around 430℃, which can activate the getter perfectly. The spacer wafer is etched using deep RIE approach to form the cavity opening of the cap wafer stack, where the getter layer is deposited using a shadow mask.

This packaging approach is verified (i) by fabricating the grating structures on a double sided polished wafer and demonstrating their measured infrared transmission performance as about 85%, (ii) optimizing and verifying the TLP bonding performance of the window cap wafer and the spacer wafer, (iii) optimizing the

cavity opening step without damaging the moth-eye structures, (iv) optimization of glass frit deposition and glass frit bonding for 8" size wafers, (v) developing a vacuum sensor wafer with Pirani vacuum gauges for bonding quality measurements (vi) bonding the cap wafer stack to various silicon wafers and measuring bonding quality including the vacuum level of the hermetically sealed cavity regions.

The bonding quality of the wafer level packaging approach is measured with three different approaches: He-leak tests, cap deflection, and pirani vacuum gauges. The bonds formed with the offered method were tested hermetic via He-leak tests performed according to MIL-STD 883. For the polished wafer usage case, the average shear strength obtained with the offered wafer level bonding method is 23.38 MPa and He-leak values as low as $0.1\text{x}10^{-9}\ atm.cc/sec$ were obtained. For the grinded wafer usage case, the average shear strength obtained with the offered wafer level bonding method is 18.72 MPa and He-leak values as around $1\text{x}10^{-8}\ atm.cc/sec$ were obtained. Best package pressure is measured around 3-4 Torr if getter is not used whereas in the case of getter usage best pressures ranging from 1 mTorr to 500 mTorr are measured.

Keywords: MEMS, Wafer Level Vacuum Packaging, Hermetic Encapsulation, TLP Bonding, Glass Frit Bonding, Thermal Infrared Detectors

ÖZ

MEMS TABANLI UZUN DALGABOYLU KIZILÖTESİ ALGILAYICILAR İÇİN PUL SEVİYESİNDE VAKUM PAKETLEME TEKNOLOJİSİ

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Bu tez, termal sensörlerin gereksinimlerini düşük maliyetle ve yüksek performansla karşılayan pul seviyesinde vakumlu paketleme elde etmek için yeni bir yaklaşım önermektedir. Güve gözü yapıları, kızıl ötesi radyasyonun uzun dalgaboyunda iletilmesine olanak sağlamak için herhangi bir boşluk olmaksızın silisyum bir alttaşın her iki tarafında oluşturulmuştur. Daha sonra, bu alttaş, düşük sıcaklıkta (yaklaşık 200 ℃) bağlanmaya izin veren Au-In geçici sıvı faz (TLP) yaklaşımı kullanılarak başka bir ara parça alttaşına yapıştırılır; TLP yaklaşımının avantajı, yapıştırma tamamlandıktan sonra çok yüksek sıcaklıkları (500℃ gibi) kaldırabilmesidir. Bu method, yaklaşık 430°C'de hem alıcıyı mükemmel şekilde aktive edebilen hem de cam hamuru bağlama yaklaşımları kullanarak önerilen kapak yığınının sensör puluna bağlanmasının kullanılmasına izin verir. Ara parça olarak kullanılan alttaş, alıcı katmanın bir gölge maskesi kullanılarak biriktirildiği kapak yığınının boşluk açıklığını oluşturmak için Derin reaktif iyon aşındırma (DRIE) yaklaşımı kullanılarak elde edilir.

Bu paketleme yaklaşımı, (i) ızgara yapılarının çift taraflı pürüzsüz bir alttaş üzerinde üretilmesi ve ölçülen kızılötesi iletim performansının yaklaşık %85 olarak

gösterilmesiyle, (ii) IR pencere alttaşı ve ara levha alttaşının TLP bağlama performansının optimize edilmesi ve doğrulanmasıyla, (iii) güve gözü yapılarına zarar vermeden kavite açma adımının optimize edilmesi, (iv) 8” boyutlu diskler için cam hamurunun serigrafi yöntemi ile oluşturulması ve cam hamuru bağlama yönteminin optimizasyonu, (v) yapıştırma kalitesi için Pirani vakum göstergeli bir vakum sensörlü pul geliştirme ve karakterizasyonuna yönelik ölçümler (vi) kapak yığınının çeşitli silisyum disklere yapıştırılması ve hermetik olarak kapatılmış boşluk/kavite bölgelerinin vakum seviyesi dahil olmak üzere bağlanma kalitesinin ölçülmesi ile doğrulanır. Disk seviyesi paketleme yaklaşımının yapıştırma kalitesi üç farklı yaklaşımla karakterize edilmiştir: He-sızıntı/kaçak testleri, kapak pulunun ince bir diyafram haline getirilip çökmenin analiz edilmesi ve pirani vakum ölçerler. Önerilen yöntemle oluşturulan bağlar, MIL-STD 883'e göre yapılan He-kaçak testleri ile hermetik olarak test edilmiştir. Pürüzsüz pul kullanım durumu için, önerilen disk seviye yapıştırma yöntemi ile elde edilen ortalama kesme dayancına sahip bağlar 23.38 MPa elde edilmiştir ve oluşturulan bağların helyum sızdırmazlık değerleri $0.1x10^{-9}$ atm.cc/sn’den daha düşük ölçülmüştür. Öğütülmüş/inceltilmiş disklerin yüzeyi daha pürüzlüdür ve bu disklerin kullanım durumu için, önerilen disk seviye yapıştırma yöntemi ile elde edilen ortalama kesme dayancına sahip bağlar 18.72 MPa elde edilmiştir ve oluşturulan bağların helyum sızdırmazlık değerleri $1x10^{-8}$ atm.cc/sn’den mertebelerinde ölçülmüştür. Paket basıncı, getter kullanılmadığında en iyi 3-4 Torr civarında ölçülürken, getter kullanım durumunda en iyi 1 mTorr ile 500 mTorr arasında değişen basınçlar ölçülmüştür.

Anahtar Kelimeler: MEMS, Disk Seviyesi Paketleme, Hermetik Paketleme, TLP Bağlama, Cam Hamuru Yapıştırma, Termal Kızılötesi Dedektörler

To My Love Murat

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ABBREVIATIONS

METU: Middle East Technical University

MEMS: Micro Electro Mechanical Systems

WLP: Wafer Level Packaging

IC: Integrated Circuit

SOG: Silicon-on-Glass

AR: Anti-Reflective

ARC: Anti-Reflective Coating

TLP: Transient Liquid Phase

IMC: Intermetallic Compounds

NEGs: Non-evaporatable Getters

CMOS: Complementary Metal Oxide Semiconductor

IR: Infrared

FE: Finite Element

SSP: Single Side Polished

ROIC: Readout Integrated Circuit

DSP: Double Side Polished

LWIR: Long Wave Infrared

SW: Subwavelength

SWARG: Subwavelength antireflective gratings

CZ: Czochralski

FZ: Float Zone

RR: Right Reading

WR: Wrong Reading

T: Top

B: Bottom

USM: Under-Seal Metallization

UV: Ultra-Violet

OM: Optic Microscope

SEM: Scanning Electron Microscope

EDS: Energy-Dispersive X-ray Spectroscopy

SAM: Scanning Acoustic Microscope System

DIW: Deionized Water

LIST OF SYMBOLS

SYMBOLS

Na: Sodium

O_2: Oxygen

SiO_2: Silicon dioxide

GaAs: Gallium Arsenide

BCB: Benzo cyclobutene

PI: Polyimide

Au: Gold

Al: Aluminum

Cu: Copper

Si: Silicon

Sn: Tin

In: Indium

Ge: Germanium

Ni: Nickel

Ag: Silver

SiN: Silicon Nitride

Ti: Titanium

CO: Carbon Monoxide

C_xH_y: Hydrocarbon

CHAPTER 1

INTRODUCTION

MEMS refers to Micro-Electro-Mechanical Systems, which offers the advantages of lower cost, better compatibility with high-volume batch fabrication compared to the conventional electro-mechanical systems, while requiring smaller space and providing higher reliability. Although some MEMS components must have a direct physical contact with the outer world such as gas flow sensors and pressure sensors; nearly all of the MEMS devices must be isolated from the atmosphere for correct operation purposes, ranging from the inertial sensors (gyroscopes and accelerometers), resonators, to infrared detectors [1]–[3]. This isolation is necessary mainly for two reasons: (i) forming an operation environment for accurate response and (ii) keeping these tiny components safe from the adverse effects of various factors. Needless to say, the isolation of the MEMS devices from the ambient is simply achieved by encapsulating them in convenient packages; so, MEMS packaging is a crucial and major interrupting block for the commercial success of MEMS devices.

The most costly and problematic part of the MEMS technology is the packaging because the package must fulfill the several requirements ranging from IC package compatibility and depending on the type of the device sensor any other additional functionalities. Although MEMS packaging is application specific, the MEMS industry is trying to find generic and cost-effective solutions for the packaging of the device sensors. For the correct operation, MEMS devices need special environment such as vacuum, inert atmosphere, or controlled gas atmosphere. One type of such MEMS devices with specific packaging need is MEMS based thermal detectors for infrared sensing or imaging, such as microbolometers and thermopiles.

MEMS-based thermal detectors have a suspended and thermally isolated body region that absorbs electromagnetic radiation that increases the temperature of the body region, where this temperature increase is measured with various temperature sensing elements, such as resistors, thermocouples, or diodes. The performance of these devices directly depends on the thermal isolation of the suspended body, where the biggest portion of thermal conductance comes from the vacuum level of the environment. Achieving the vacuum packaging on wafer level is a must for reducing the cost of the vacuum packaging. A big challenge in wafer level vacuum packaging is the need for this package to allow the transmission of the infrared radiation. The selection of the packaging material as silicon is a very straight forward and compatible approach, but the silicon wafers reflect the infrared radiation, reducing the transmission to about 50% in the 8-12μm wavelength range. The use of anti-reflective coatings on both sides of the polished silicon cap wafers is a good option, increasing the transmission to over 90%; however, coating AR layers on both sides of the silicon wafers are not straight forward, especially as one side of the wafers need to have a cavity to get the vacuum regions on the sensors. The use of moth-eye structures on the silicon surface has been used in the literature and industry for a while and is becoming widespread. But, creating these structures in the cavity is also a big challenge. There is also a need to put a getter material in the cavity, which should be activated at high temperature to provide a high vacuum level. The wafer bonding approach and bonding temperature are also other critical issue at wafer level vacuum packaging of the thermal sensors.

This thesis presents a versatile, high performance 8” size wafer level vacuum packaging (WLVP) solution to reduce the cost of vacuum packaging necessary for MEMS-based long-wave infrared thermal detectors. The organization of the introduction chapter is as following; in Section 1.1 MEMS packaging requirements are briefly described. Section 1.2 introduces the WLP approaches and the worldwide works from the literature in terms of solder, TLP, and glass frit bonding methods. Finally, Section 1.3 summarizes the objectives of this research and the organization of this thesis.

1.1 MEMS Packaging Requirements

The main requirements during the packaging or encapsulation of MEMS devices could be categorized as mechanical protection, hermetic encapsulation, and lead transfer. Although MEMS packaging is design specific, the vacuum level requirements of some common MEMS devices can be seen in Table 1.1.

Table 1.1 Some common MEMS devices and their vacuum requirements [4].

Sensor type	*Working pressure (mbar)*
Accelerometer	≈300-700
Absolute pressure sensor	≈1-10
Resonator	10^{-4}-0.1
Gyroscope	10^{-4}-0.1
RF switch	10^{-4}-0.1
Microbolometer	$\leq 10^{-4}$
Optical MEMS	Moisture free
Digital micro-mirror and light processing MEMS	Moisture free

This section describes the main requirements of MEMS packaging in terms of mechanical protection, hermetic encapsulation, and lead transfer, respectively.

Mechanical Protection: All MEMS packages must fulfill the major requirements such as mechanical rigidity and stability throughout the lifetime. MEMS structures consist of fragile and damageable parts, so they must be mechanically protected from outer world damages such as mechanical shocks, vibrations, contaminations, and other physical damages during the operation and storage [5]. Besides, the thermal expansion coefficient of the package's material has to be selected close to the thermal expansion coefficient of the device's material in order to obtain the MEMS package with low stress. Last, but not least, the dimensions of the package are taken into consideration for device compatibility, easy handling, testing, and storage.

Hermetic Encapsulation: Environmental effects causes some problems such as degradation and erosion of materials and this shorten the lifetime; so, protection of the MEMS devices is the most significant function of the package. In an ideal case, the MEMS package should keep the device safe from all the undesired environmental hazards, which can be mechanical, electrical, optical, thermal, or chemical. As mentioned in Table 1.1, working environments are sensor and its usage area specific; therefore, the MEMS package must be designed sensor and its usage area compatible.

Lead Transfer: The package is the only communication bridge between the device and the outer world so electrical signal transfer is the major issue that must be concerned. In conventional packages, the electrical connection is provided with package pins; whereas in wafer level packaging, lateral and vertical feedthroughs are the two main approaches which are used for the electrical connection issues. In these two main branches conductivity is taken into consideration. If the sealing material has enough thickness (for step height coverage purposes of laterally transferred sensor lead) and is not conductive such as in the case of glass frit; a cap wafer can directly be bonded for hermetic sealing of the device. However, if the sealing material is conductive (vertical feedthroughs case), an additional passivation layer is required. Needless the say, integrating additional passivation layer not only increasing the process steps and complexity but also the cost [2]. In vertical feedthroughs, a thinner sealing material can be preferred because of the fact that the leads do not cause a step-height under the sealing region as in the case of lateral feedthroughs [6]. Obviously, the complexity and number of the process steps both for the device and the cap wafers increases in the vertical feedthroughs approach. Also, it is really difficult to obtain the sealing and the lead transfer in the same step which is important for thickness control of the sealing material and their regions, sensor leads, and vertical feedthroughs. Therefore, any problem or mismatch between some of the previously mentioned parameters may cause failures.

1.2 MEMS Packaging Methods

There are two main approaches for the MEMS packaging: die level and wafer level packaging. Figure 1.1 shows the die level packaging method, which relies on the packaging of the individual dies after the sensor wafer is directly diced following its fabrication steps. The diced sensors are released and mounted on the package for the electrical circuit integration issues. After the die placement, each sensor is individually packaged; this method unfortunately not only increases labor and time but only reduces the process yield and reliability. Figure 1.2 shows the general approach in wafer level packaging. Sealing the MEMS devices at the wafer-level is much better compared with die level packaging, as this method has several advantages such as reducing the packaging costs, labor, time; and increasing the yield and reliability [2]. The packaging at wafer level has many advantages, but achieving this becomes more challenging when the wafer size increases, especially for 8" wafer sizes. There are two main approaches for wafer level packaging: packaging by thin-film encapsulation and packaging by using cap wafer bonding. These two approaches are explained further in detail in the next section.

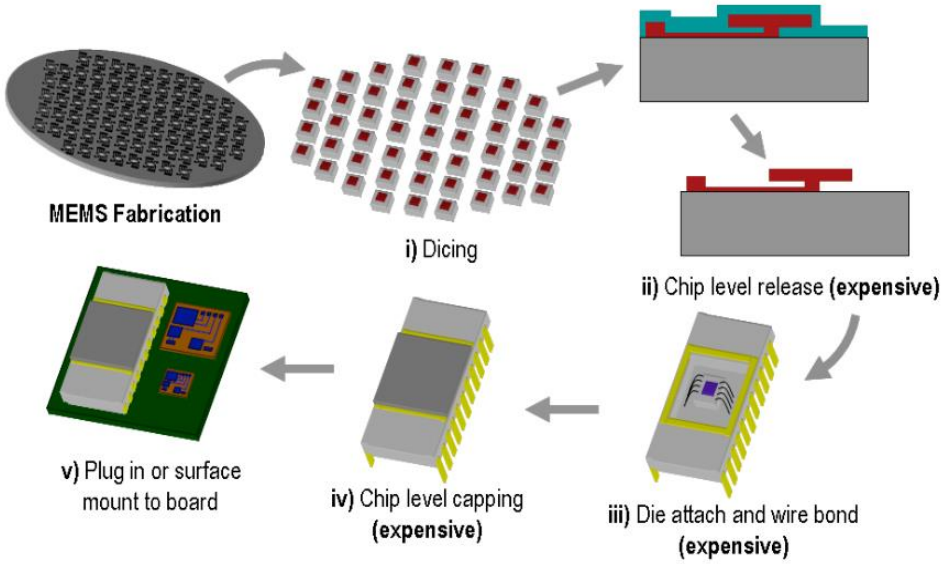


Figure 1.1. A schematic showing the typical packaging steps in a MEMS chip level packaging process [7].

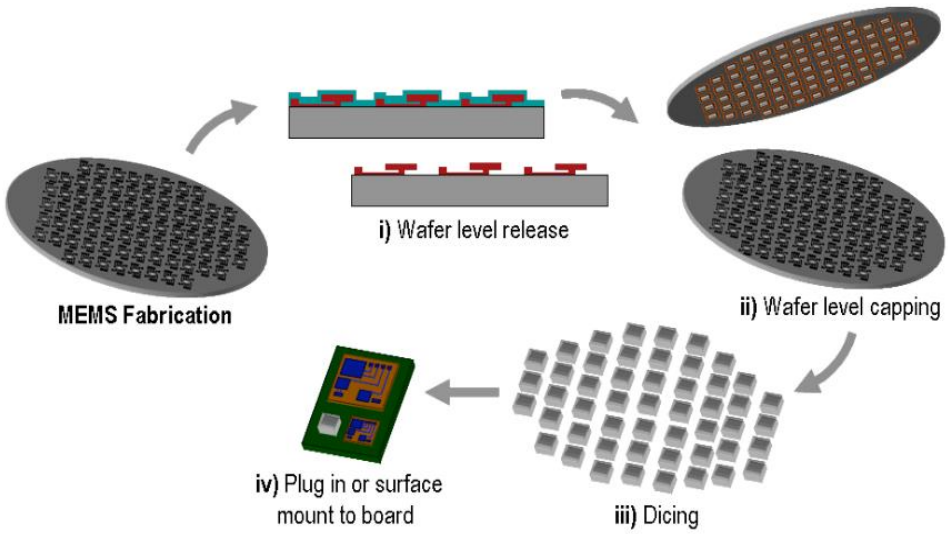


Figure 1.2. Typical packaging steps in a MEMS WLP process [7].

1.2.1 Packaging by Thin Film Deposition

Figure 1.3 shows the thin film packaging method, which is based on deposition of packaging material on a sacrificial layer that is etched later, where the cavity sealing is achieved with another thin film layer. This technique offers several advantages. The first is the reduced and minimized package size because of the lack of the bond rings. The second advantage is that there is no need for extra process equipment's such as wafer bonders for the packaging approach which reduces cost significantly.

The major drawback of this approach is to obtain a good vacuum level: (i) the very small cavity cannot tolerate even very small outgassing, (ii) putting a getter layer inside this small cavity and activating it are not easy. Achieving a hermetic sealing is also a challenge with thin film materials, as can be seen by the results of the studies that have used various materials, including various types of metals, semiconductors and insulators used for those purposes such as nickel, poly silicon, amorphous and single crystal silicon, silicon dioxide and polymers [8]–[13]. Some of these layers require very high temperature for deposition, degrading the sensor performance, while other layers might not provide enough mechanical support, requiring additional mechanical protection for increasing the robustness of the cap layer [2].

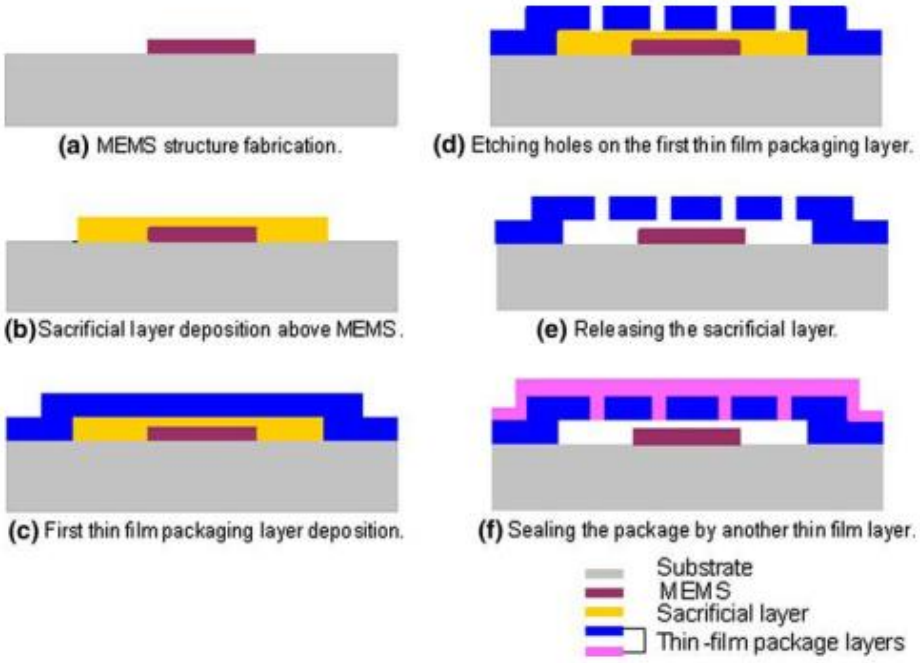


Figure 1.3. Conceptual process flow for wafer level packaging by thin film deposition method [8].

1.2.2 Packaging by Wafer Bonding

The second approach of wafer level packaging is to use a separate cap wafer instead of thin film layers for hermetic sealing. The concept is simply bonding the produced MEMS sensor wafer to the convenient capping wafer by an additional wafer bonding process step. There are several wafer level hermetic bonding methods in the literature such as anodic, eutectic, glass frit, and low temperature fusion bonding depending on the MEMS packaging requirements previously discussed; and Table 1.2 summarizes and compares wafer level vacuum encapsulation approaches to show the pros and cons according to each other. After showing the quick summary in Table 1.2, the following sections describes the commonly used wafer level packaging techniques and their requirements in detail.

Table 1.2 Summary of the MEMS Packaging Methods.

Bond Parameters	**Thin Film**	**Anodic**	**Plasma Activated Fusion**	**Polymer Adhesive**	**Metal Thermo Comp.**	**Solder/ Eutectic**	**Glass Frit**
Temperature (°C)	250-1080°C	250-450°C	200-400°C	below 250°C		Au-In~200°C Au-Sn~300°C Au-Si:380-400°C	430-450°C
Strength	High	High	High	High	High	High	High
Special Requirement	*	Bond Voltage	Special Cleaning	*	*	*	*
Outgassing	*	O_2	H_2, H_2O	permeable for gases	Noble gases	Noble gases	CO, CxHy
Line Width	*	>20µm	>20µm	*	>60µm	>60µm	>250µm
Step Heights Coverage	Up to 3µm	30nm	0	Up to 3µm	*	Up to 1 µm	Up to 2µm
Vacuum with Getter	*	High	Activation Problem	*	Medium	Au-In: Medium Au-Sn: Medium Au-Si: High	High
Vacuum without Getter	Med.	Med.	Not Known	*	Medium	Medium	Med.
Leak Rate	Very Low	Low	Very Low	Very High	Low	Low	Low

1.2.2.1 Anodic Bonding

The anodic bonding is the most common way for bonding glass and Si wafers to each other and has been used in many research studies as well as many commercial products. Figure 1.4 shows a representation of the anodic bonding method, where Si

and Na doped glass wafers are put into contact with Si wafer, heated and a potential is applied between them. This phenomenon causes Na^+ atoms become mobile and leave O_2 atoms alone at the bonding interface; then these O_2 atoms interacts with the Si atoms and form a strong SiO_2 bond [14].

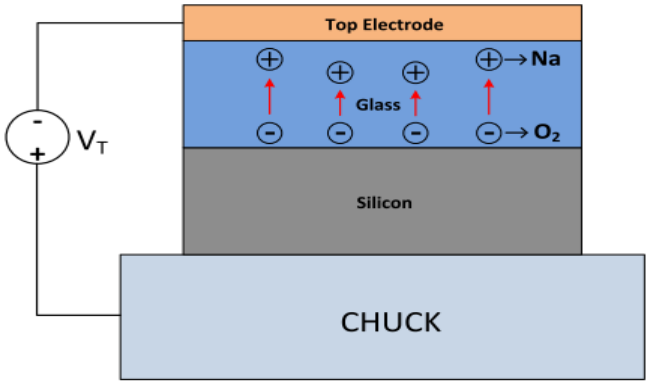


Figure 1.4. A schema representing the anodic bonding approach [15].

In anodic bonding the critical bonding parameters which must be taken into consideration are temperature, applied voltage, time and force. Bonder's chuck heated up to temperatures between 250-450°C and applied voltage values are in the range of 400-2000V depending on the application [14], [16], [17] .

This technique allows highly reliable, uniform and high strength hermetic seals even at lower process temperatures compared to other techniques. This approach is convenient for some sensors, such as gyroscopes, pressure sensors, and resonant devices and has been used at METU for fabrication of a number of devices, such as the fabrication of resonance-based MEMS temperature sensors by the application of SOG (silicon-on-glass) process in 4" size wafers in the study of [18].

Although this approach is very useful for the fabrication of MEMS structures, its use in the wafer level packaging is not convenient: (i) placement of feedthroughs is not easy, (ii) O_2 releasing during the process may cause to lower the vacuum level even there is a getter layer [19], (iii) a number of precautions need to be taken to prevent the possible damaging of the devices during the bonding due to the high voltage.

1.2.2.2 Direct/Fusion Bonding and Plasma Activated Direct/Fusion Bonding

The direct/fusion bonding is used for the bonding of two polished and chemically active wafer surfaces, where a wide range of materials can be bonded, including Si-Si, Si-SiO_2, Si-Si_3N_4, Si-GaAs, and Si-sapphire (Al_2O_3). Wafer surfaces are activated chemically before the actual bonding; then wafers are brought into contact to initiate the bonding with Van der Waals forces. Unfortunately, the strength of this bond is not sufficient and has to be improved by an annealing process. Therefore, wafers are annealed at high temperature in order to construct a strong covalent bonding between the wafers [20]. This technique requires a temperature range of 600-1200°C. The need for this high temperature annealing process limits the direct use of fusion bonding technique for the WLP of MEMS components. Another drawback of the technique is that it can only be applied to the devices with vertical feedthrough because of the lack of the surface topography tolerances.

The plasma activated version of the method is developed for achieving bonding at low temperatures [21], [22]. Similarly, the surface of the wafers is chemically activated in a high vacuum before the bonding. Needless to say, the high vacuum environment prevents the re-oxidation of surface atoms, and the bonding occurs even at room temperature if the wafers are immediately brought into contact. The bond strength can be improved by applying a low temperature annealing process (200°C-400°C) [21]. When compared with standard fusion bonding, this technique has an advantage in terms of the bonding at lower process temperatures with similar bonding strength as in the case of conventional fusion bonding. However, it is still applicable to the device with vertical feedthroughs.

1.2.2.3 Polymer Adhesive Bonding

The polymer adhesive bonding utilize organic compounds to form bonding structure; BCB and PI are sample organic compounds which can be used as a material in this bonding technique. The main advantages of this technique can be listed as:

- relatively low (usually below 250 °C) bonding temperature;
- can applied different wafer materials;
- tolerable to surface topography and particles;
- various polymer adhesive materials compatibility;
- cost friendly process [23].

One of the most significant drawbacks of this method is that organic compound has permeability for gases; therefore, hermetic sealing and vacuum environment is not satisfied with polymer adhesive bonding.

1.2.2.4 Metal Thermo-Compression Bonding

Another bonding approach is metal thermo-compression. In order to form bonding, metal deposited wafers are brought together; force and heat parameters are applied to provide solid-state diffusion between the metals [24]. Frequently preferred metals can be listed as gold (Au), Aluminum (Al), and Copper (Cu) in this bonding type. Although vacuum packages can be obtained using metal thermo-compression method; it is not handling the surface topography.

1.2.2.5 Solder/Eutectic Bonding

The working principle of eutectic bonding is based on the alloy formation due to diffusion of two materials at their eutectic temperature. The selected metals are deposited on the bonding interface or ring at a desired composition stack with barrier layers and forced to obtain physical contact. Due to the interdiffusion phenomena, the surface layer liquidifies when heating them above their eutectic point. As a

second step the surface layer is cooled, then mixture solidifies and a strong bond is obtained accordingly [15]. The most commonly used eutectic systems used for the wafer level vacuum packaging of MEMS devices are Au-Sn, Au-Si, Au-Ge, Al-Ge, and Au-In, and Table 1.3 provides their bonding temperatures. This bonding technique not only enables reliable and high yield vacuum seals at lower process temperatures in the range of 200-400°C, but also provides a perfect sealing capability on the step height caused by laterally transferred sensor leads. On the other hand, there is additional insulating layer requirement which increases process steps and complexity.

Table 1.3 Some most common metallic systems which provide eutectic reaction.

Metallic Alloys	Eutectic Point
Au: Sn	300 ℃
Au: Si	380 ℃
Au: Ge	380 ℃
Al: Ge	440 ℃
Au: In	510 ℃

The transient liquid phase (TLP) bonding or Solid-Liquid Inter-Diffusion bonding (SLID) is known as combination of diffusion bonding and brazing. The SLID and TLP bonding processes share many similarities. Usually the term SLID bonding is used when new phases are formed within the bond, but both terms are used interchangeably [25]. The advantage of TLP bonding is the melting temperature of bonding area ($T_{re\text{-}melting}$) is higher than bonding temperature ($T_{bonding}$) after bonding. The IMCs are generally the phases with high strength and high melting point; so, it is possible to obtain bonds with high melting temperature [26]. However, it can be a challenging bonding process because very high heating rates are required to reach to melting temperature of the transient layer. Therefore, this method can be also equipment limited.

There are many different material systems that enable TLP bonding and some of them are given in Table 1.4. Also, the sample phase diagram of the TLP system is given in Figure 1.5.

Table 1.4 Comparison of various TLP bonding systems, data from [27].

Material	Temperature (°C) bonding	re-melt(IMC)	Relative market price*	Relative conductivity* Thermal	Electrical	Note
Cu-Sn	280	415 (Cu_6Sn_5) 676 (Cu_3Sn)	Cu: 0.5 Sn: 0.8	Cu: 4.4	Cu: 4.1	Complex phase
Ni-Sn	300	800 (Ni_3Sn_3)	Ni: 1 Sn: 0.8	Ni: 1	Ni: 1	Conventional pack-aging materials for high temp. device
Au-Sn	250	419 (AuSn)	Au: 2600 Sn: 0.8	Au: 3.5	Au: 3.1	Free from oxidation
Ag-Sn	250	480 (Ag_3Sn)	Ag: 63 Sn: 0.8	Ag: 4.7	Ag: 4.4	-
Ag-In*	200	495	Ag: 63 In: 37.5	Ag: 4.7	Ag: 4.7	-
Au-In	175	880	Au: 2600 In: 37.5	Au: 3.1	Au: 3.1	Most expensive

* Relative values are normailized to Ni.

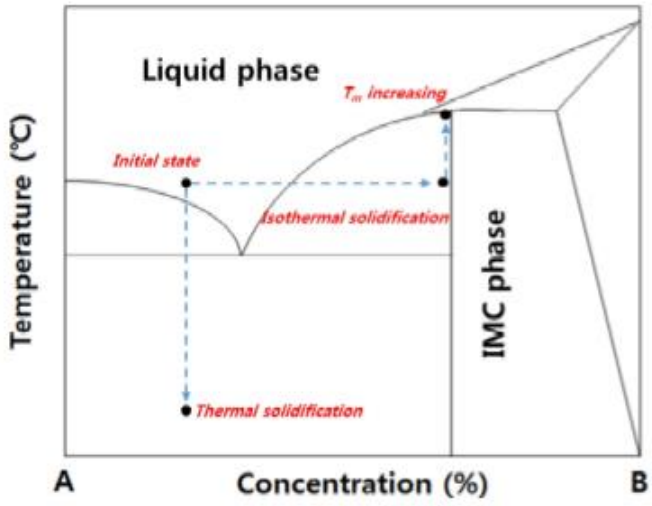


Figure 1.5. The sample phase diagram of the TLP system [28].

There are some challenges for performing TLP bonding techniques in practice and major ones be listed as following,

- TLP bonding methods depends on the diffusion process of the metals. Therefore, higher than 5 μm thick electro plated metal layers are needed in the processes; so metal deposition methods such as evaporation and sputtering can be challenging for process development and especially in 8" wafers nonuniformity can be observed.

- There is high possibility of oxidation of metals which can results failure in the bonding.
- The getter activation temperatures for conventional getter materials are above 400 ℃; so, this can be problematic for low temperature bonding; so, getter material selection or developing may be another concern.

1.2.2.6 Glass Frit Bonding

This bonding also referred to as glass soldering or seal glass bonding. It is one of the most reliable and high yield wafer level vacuum packaging approaches applied to a wide range of sensors. There is no need to integrate additional passivation layer for preventing leakage currents at process temperatures up to 125°C because glass frit is a dielectric material [29]. The glass frit bonding, principle is like that under the desired bonding pressure wafers are heated up to the process temperature around 430°C for a few minutes [29]. There is a trade of between shortness of the bonding time. For instance, bonding time shortening causes the glass frit to spread insufficiently whereas a longer bonding time causes the glass frit to be overflown subsequently leaving voids [30]. In [31], the principle of glass frit bonding is illustrated in a good manner (Figure 1.6) which consists of three main steps: screen-printing of the glass paste, thermal conditioning and thermo-compressive wafer bonding.

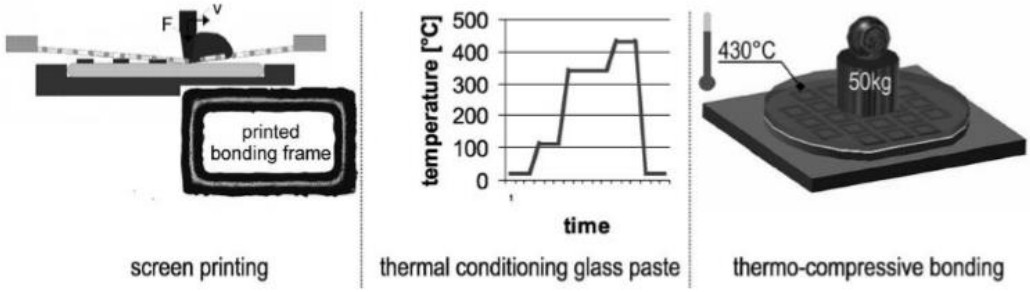


Figure 1.6. The principle process flow of glass frit bonding phenomena [31].

This bonding approach has the high capability of providing planarization over step heights up to about 2 μm which is an essential property for the hermeticity; and it is commercially significant bonding process, which can be applied for many different substrate materials ranging from Si, SiO, SiN, to Al, Ti and glass. A layer thickness of 5 μm or greater is required to allow a good reflow of the glass during bonding (Figure 1.7.). Typically, in the used glass frit materials in literature, with particle sizes up to 15 μm, the mesh width is 45 μm at a wire thickness of about 35 μm and a film thickness of about 10 μm.

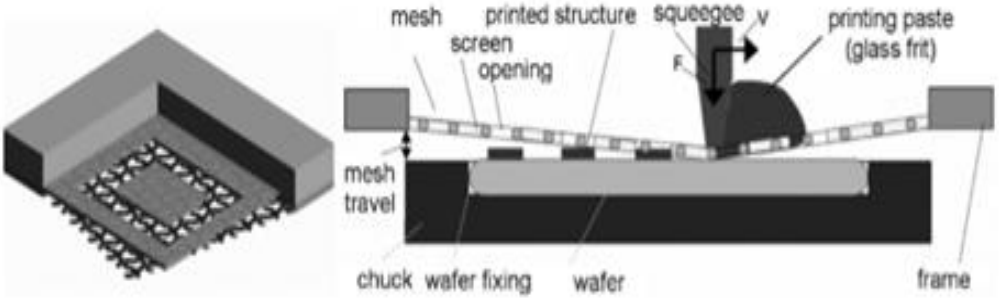
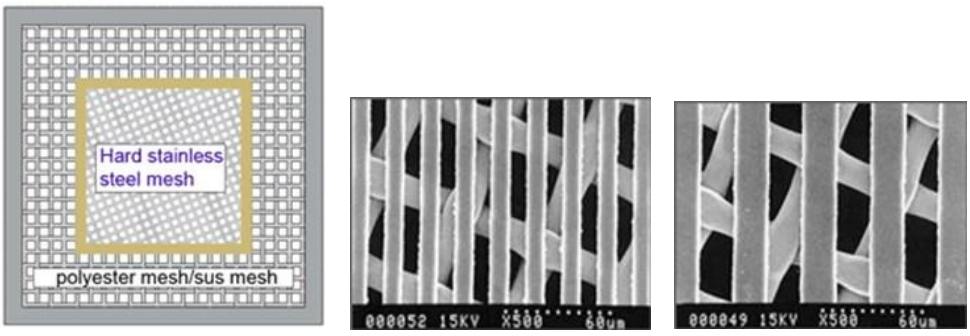
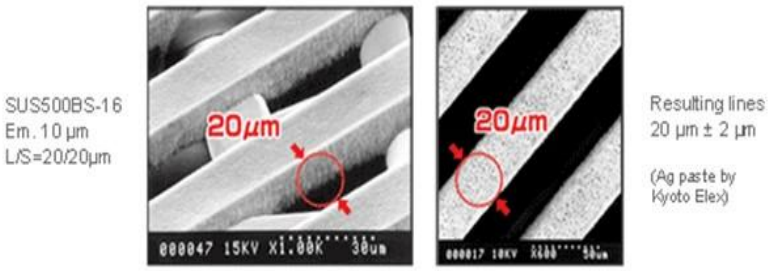


Figure 1.7. The principle of screen printing and technical names of the tools used for glass frit bonding [32].

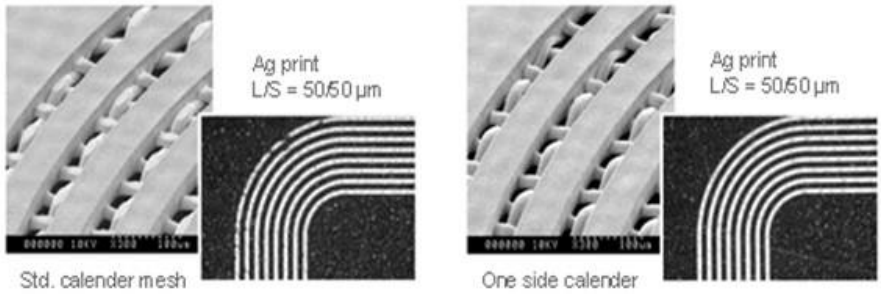
The most frequently used screen-printer models are Samsung, MPM, Speedline MPM, Ekra, and DEK. Briefly, there are various mask types (Figure 1.8.) ranging from trampoline mask (for fine pattern printing); black screen mask (for better adhesion of the emulsion and very smooth aperture walls for the best possible paste flow) to one side calender mask (good for the final result of the curved pattern prints; best choice for RFID and touch panel applications.); and 3D screen mask (for enhancing the thick screen-printing process). The mesh materials can be polyester, stainless steel and Tungsten [33]. Polymer meshes are mainly used with the structures of width in the range 150– 300 μm at a wet thickness of about 45μm can be realized with glass frit pastes. Needless to say, structure size, mesh travel, squeegee speed and force, as well as paste properties such as viscosity and particle size have a strong influence on the structure definition and placement accuracy.



(a)



(b)



(c)

(d)

Figure 1.8. Representative image showing various screen-printing mask types: (a) trampoline mask, (b) black screen mask, (c) one side calender mask, (d) 3-D screen mask [33].

1.2.2.7 Getter Integration

Getter integration, usually as a thin film, is a necessary step in the package cavity to form a reliable vacuum environment. The most commonly used getter materials are titanium, tantalum, zirconium, and yttrium. The getter material interacts with the gas molecules in the cavity and acts as chemical vacuum pump when heated, which is necessary for the activation. The getter materials must satisfy chemical activation concerns [19]. The activation temperature is required to be over 350°C for good vacuum levels, however, this high temperature not only should be compatible with the wafer bonding technique but also should not damage the sensor devices.

There are various types of getters in the literature. Non-evaporable getters (NEGs) were first investigated for micro-packaging in the 1990s. Typically, NEGs consist of sintered metal particles which are packaged or adhered onto one of the inside surfaces of a vacuum chamber or vacuum cavity. There are two main drawbacks for applications of NEGs for micro-packaging: 1) the need for assembling or depositing sintered metal particle into the micro-cavity and 2) these sintered metal particles can shift inside of the package, interfering with the operation of the MEMS device. An alternative to using NEGs is to sputter or evaporate a thin metal film such as Ti which acts as the gettering material. As opposed to sintered metal particles, thin metal films can be easily deposited and photo-lithographically patterned. As a result, no special configurations are needed to physically separate the getter from the device. Such a thin film can be photo- lithographically formed inside of the micro-cavity for wafer level packaging. Last but not least, the getter materials must enhance some requirements ranging from chemical and mechanical stability to low gas emission, and easy activation.

1.2.3 Previous Studies for Wafer Level Packaging

Wafer level packaging by using wafer bonding has been widely used in the MEMS area since 1990's. This section provides literature review examples of significant

packaging studies based on the use of various wafer bonding techniques of MEMS devices since 2000's specialized for glass frit and eutectic/solder bonding in the literature.

In 2000, Song et. al. reported a study on the wafer level sealing of MEMS gyroscopes [34]. In their study the wafer level packaging was performed using glass frit bonding at 450°C and they do not use getters. The vacuum inside the packages were checked with the integrated gyroscopes and found as 1.5 Torr. There is no long-term data on the package vacuum for this study. Sparks et. al. published another work in 2001 in which MEMS resonators were packaged at wafer level using the solder bonding. The pressure inside the packages was around 1.5 Torr and stably can be monitored even after 42 days [35]. E. Mottin et. al. from LETI LIR, France, published the other study; in which the vacuum sealing was done using Au- Sn solder bonding with Non-evaporable getters (NEG) and the vacuum inside the packages were checked with the integrated MEMS bolometers and found as 1 Torr; at the same year [36]. T. Schimert et. al. from Raytheon Electronics System published their study in 2003 [37] in which, MEMS bolometers were capped at wafer level by using the Au- Sn solder bonding; the pressure inside the packages was around 4 mTorr and monitored to be stable even after 950 days.

In 2004, M. Ebert et. al. presented the study related with determination of residual stress by finite element analysis, and advanced characterization of glass frit bonding and performance increment methods [38]. In the work, they investigate how the residual stress which is caused by different coefficients of thermal expansion of the glass frit layer and the silicon wafer that includes chips; effect the bonding quality. In the study, three-dimensional Finite Element (FE) model of a typical chip structure was developed which consists of a silicon device wafer, the glass frit layer and a silicon cap wafer with a cavity; and at the end of the study, it is reported that after bonding about 100 MPa stress occurred in the plane of seal glass caused by cooling.

In 2005, Sparks et. al. presented the wafer level packaging study by glass frit bonding around 400°C [39]. They showed that in the reflowed glass frit sealing process; the

glass can hermetically cover relatively small steps and particles which is the most significant advantages over the anodic, eutectic and fusion bonding approaches which they do not provides. After the packaging, packages were subjected to a series of bake tests (95 °C) storage conditions for chips with and without getters in order to estimate the package performance throughout the life time which is more than three years (3000 – 26520 h) as well as the package robustness and they detected under 790 micro-Torr high vacuum levels inside the packages by using the integrated resonators which have laterally transferred sensor leads as can be seen in Figure 1.9; so with the proper design and process, this approach can produce a reliable vacuum seal with metal feedthroughs.

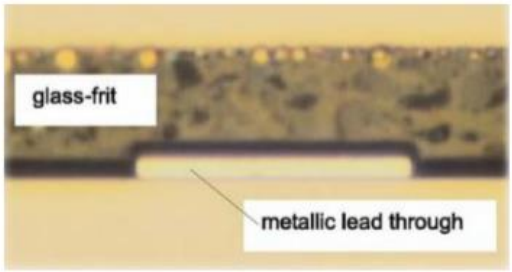


Figure 1.9. Glass frit bonded on the laterally transferred sensor leads [39].

In 2006, Knetchel et. al. introduced many characterization techniques for their glass frit bonded wafers ranging from mechanical stresses (cap wafers shows bow values up to 450µm), pull tests (around 20 MPa) to rapid thermal shocks (190°C air to 25°C water); and the electrical characterization of the glass frit has yielded ε_r = 4,6 and a good isolation behavior up to 150°C. To conclude, the characterization of the bonded wafers and the glass frit in their study has shown that this bonding technique provides a lot of advantages in the practical use [31]. In the same year, a paper related with the mechanical properties of the glass frit bonded packages is published by C. Dresbach et. al [40]. In their paper, the glass layer after bonding is about 10 µm thick and the width of the printed lines is about 200 µm. They calculated the stress situation in a micro package by a 3D thermomechanical FE Analysis. Furthermore, in their study, the residual stress in the glass layer and the linear thermal expansion

coefficient were determined by a crack width measurement in an environmental SEM; and the characterization results obtained in their work are as the following: They reported the fracture toughness of the used specimen to 0.57 MPa√m; the residual stress to 126 MPa and the linear thermal expansion coefficient to $5.6e^{-6}$ K^{-1}. These parameters are significant for the prediction of a lifetime (15-20 years for automotive industry). They also reported the tensile stresses of about 100 MPa can occur in plain and normal to the glass layer.

The studies showed that large bond rings and high temperature limitations could be reduced with the use of metal-based alloys; so in the year of 2007, W. C. Welch et. al. offered a wafer level vacuum packaging approach in which Pirani gauges are encapsulated by using Ni-Sn TLP bonding at 300°C with Ti getters. They reported a package vacuum inside the cap of 200 mTorr and stability for 20 days. Figure 1.10 represents the cross-section of the wafer pairs in [41].

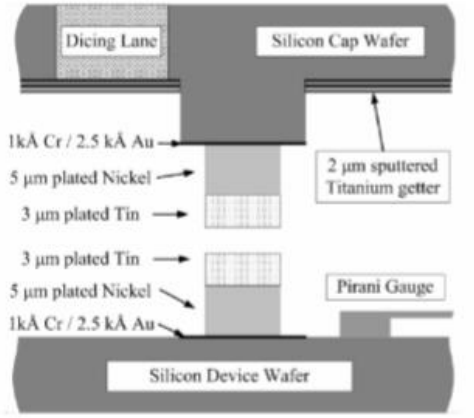


Figure 1.10. Cross section of the cap and device wafer pairs before Ni-Sn TLP bonding in the study of [41].

In the same year, Yoon-Chul et al. [42] introduced Au-In TLP bonding by applying two different bonding conditions (first type bonding parameters: T:210°C P:0.04MPa, time: 10 minutes and second type bonding parameters: T:180°C, P:0.02MPa, time: 30 minutes) to the 4" size wafers (in first type configuration glass-glass and in second type configuration glass-silicon) with the material stacks shown in Table 1.5. They reported that at the end of sufficient wafer level bonding sliced

dies are selected from different locations of the wafer and the shear strength values for type-1 samples were 40 MPa whereas for type-2 samples they were 20 MPa.

Table 1.5 Material stacks used for Au-In TLP bonding by Yoon-Chul et al. [42].

	Type-1	Type-2
Cap wafer	Glass (4 inches)	Glass (4 inches)
Metallization	Ti/Ni/Au/In/Au 500/2000/500/25000/ 500 (Å)	Ti/Ni/Au/In/Au 500/2000/500/25000/500 (Å)
Bottom wafer	Glass	Si
Metallization	Ti/Ni/Au 500/1000/20000(Å)	Cr/Au 400/20000 (Å)

Welch et. al. reported a low temperature (200℃ for 1 hour) Au-In TLP packaging study for encapsulation of MEMS Pirani vacuum gauges with lateral feedthroughs in 2008 [43]. The advantage of Au-In TLP is that although the sealing of the packages was done at 200℃, the re-melting temperatures of the packages were higher than 200℃ up to 500℃. In their approach, after packaging process was done successfully the getters inside the packages were activated at the temperature value of 400℃ for 40 minutes without degrading the hermeticity. They reported the measured package pressures after bonding were variation between 200mTorr to 5Torr; and the leak rate was as low as $1x10^{-16}$atm.cc/sec. Figure 1.11 represents the SEM image of the Au-In TLP bonded packages in [43].

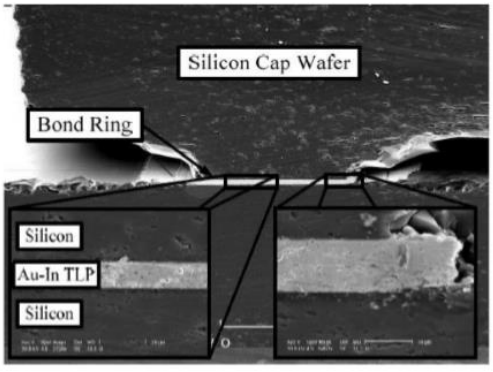


Figure 1.11. The cross-sectional SEM image of the bond region after the packages hermetically capped by using Au-In TLP bonding in [43].

Similarly, in 2008, Mitchell fabricated vacuum packages with Au-Si eutectic bonding method and reported reliability and yield results of them [7]. In the scope of the study, he monitored the performance of the packages by using Pirani vacuum gauges and reported that the pressure remained stable as 25mTorr over 4 years using Nanogetters^{TM}.

In 2010, another WLP process is reported by A. Yu et. al. [44]. In their work, the vacuum sealing of micromachined resonators are achieved without using getters and applying Au-Sn eutectic bonding at relatively low temperature, which is 280°C; and a vacuum level of the package 200 mTorr for 7 days stability is reported.

In 2011, R. M. Haque et. al. reported a new packaging approach in which the electrical leads of the sensors were vertically transferred with highly doped silicon patterns embedded in a glass substrate. The fabrication of these vertical silicon patterns is based on the glass reflow process [45]. This approach provides the fabrication of such vertical feedthroughs simpler than the ones in the literature up to 2011. The main drawback of the packaging approach in [45] is the conductance of vertical silicon feedthrough patterns. It is not good way to transfer RF signals with such highly doped silicon feedthroughs.

In 2012, MEMS resonators are packaged (Figure 1.12) by using the glass frit bonding approach at 430°C was reported by G. Wu et. al.[46]. In their work the electrical signal transfer is done with Al lateral feedthroughs on the cap wafer by forming an Al-Au eutectic bonding. In the packaged resonators inside the sealed micro packages monitored and reported as 1 mbar.

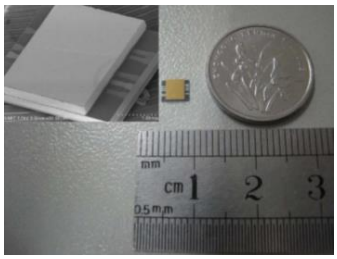


Figure 1.12. Optic microscope and SEM images of the glass frit packaged resonator chips after dicing in [46].

In 2013, H. Xu et. al. reported another work for wafer level MEMS encapsulation using the Au-Sn and Cu-Sn SLID bonding. In their bonding approach the bonding temperature varied between 300°C and 350°C [47]. They used resonators for measuring the package pressure inside the sealed micro packages and reported the pressure less than 0.1 Pa. Figure 1.13 presents bonding ring structure and related process flow details.

It is obvious that functionality and reliability of a bonding seal is the most significant issue that must be taken into consideration, so qualified test methods are required for evaluating the quality of them in terms of the strength of the bonding interfaces. In [48], Naumann et. al. adapted the micro-chevron-test for glass frit bonded samples and also, they discussed arising challenges. In addition, acoustic inspection with high resolution is not only used for estimating the effective bond strength but also used for sample pre-selection and defect localization in their study.

In 2014, V. Chidambaram et al. performed alternative Au-In bonding by using Au- In materials systems with/without gold protective layer on the In metal layer and Ti/Ni/Pt adhesion layers between Au and In; and they implemented the approach not only in 8" size wafer level bonding but also chip-level bonding with 16x16mm^2 dies [49]. Unfortunately, in the wafer-level bonding case the heating rate was 45°C/min; whereas for chip scale bonding, they were able to apply a higher heating rate, which was 100°C/min. They reported the best barrier/adhesion layer material as Ni with the thickness of 20 nm. The bond interface for without the barrier case, had a structure with voids as shown in Figure 1.14 and finally the He-leak test results for the hermicity purposes of Au-In TLP bonded samples are summarized in Table 1.6.

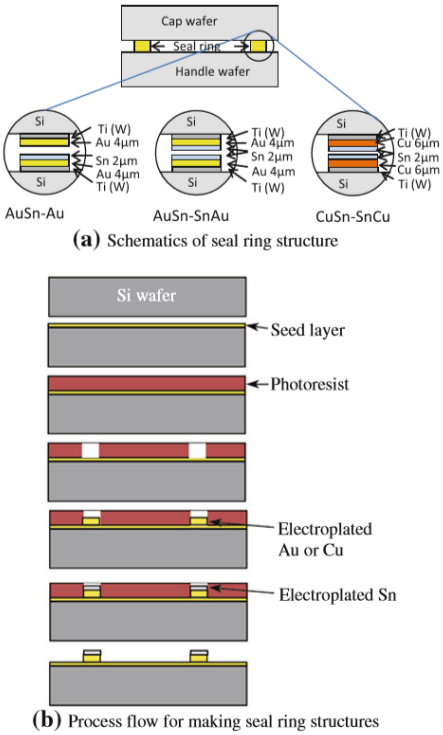


Figure 1.13. Schematics of the bond ring and its process flow in [47].

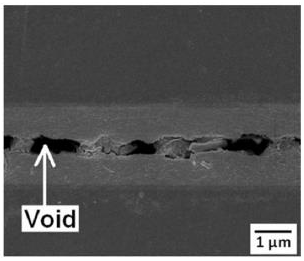


Figure 1.14. The cross-section of the Au-In TLP bond interface when adhesion layer is not used in [49].

Table 1.6 Tabulated form of the He-Leak test results of the Au-In TLP bonded samples comparing with and without barriers/adhesions in [49].

	Without diffusion barriers		With diffusion barriers		
S. no.	Without Au protective coverage layer (atm cc/s)	With Au protective coverage layer (atm cc/s)	Ti (atm cc/s)	Pt (atm cc/s)	Ni (atm cc/s)
1.	0.2×10^{-5}	0.1×10^{-7}	0.2×10^{-7}	$4.8x\ 10^{-7}$	0.5×10^{-7}
2.	1.3×10^{-5}	0.2×10^{-8}	1.3×10^{-6}	$0.2x\ 10^{-8}$	0.3×10^{-8}
3.	0.8×10^{-6}	0.5×10^{-8}	1.0×10^{-5}	$2.5x\ 10^{-7}$	0.3×10^{-8}
4.	0.4×10^{-7}	2.2×10^{-6}	1.0×10^{-5}	$1.6x\ 10^{-7}$	0.6×10^{-8}
5.	0.2×10^{-6}	0.7×10^{-8}	0.2×10^{-7}	3.2×10^{-7}	5.5×10^{-7}

In 2015, L. Deillon et. al. showed a work on the WLP using the SLID bonding in the Au-In system at 200°C for 15 minutes [25]. Inside the sealed micro packages, the package pressure is measured 1.8 bar. Also, they reported that during the hermeticity tests 17% of the packages were sealed hermetically. Figure 1.15 presents seal ring structure and related process flow.

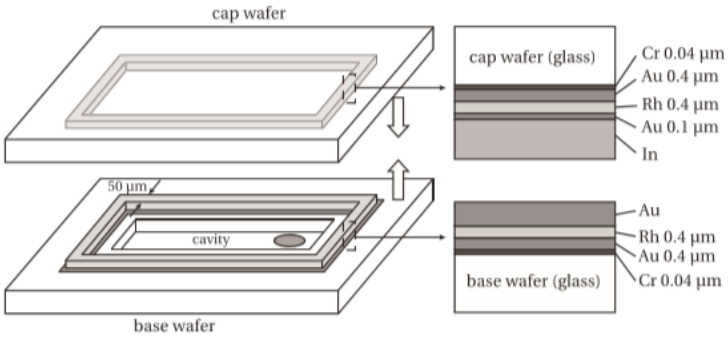


Figure 1.15. Schematic representation of a bond ring and the metallization layers deposited on the device and cap wafers in [25].

In 2016, L. Yifang et. al. offered two-step silicon wet etching method for the control of the width and height of the glass frit bonding layer in terms of to eliminate the squeezed-out problems (Figure 1.16) for improving bonding strength and reliability in WLP MEMS processes [50]. They reported the bonding strength increases from 10.2 to 19.1 MPa as compared with a conventional thermal annealing process in air; and hermetic sealing leakage tests of 5×10^{-8} atm ccs^{-1}.

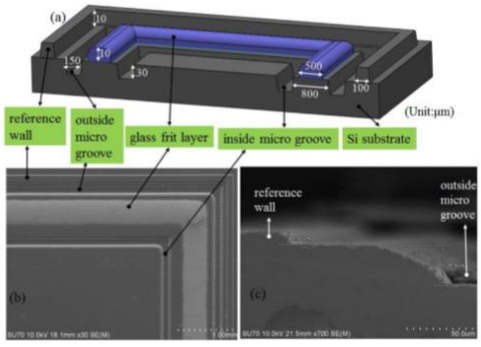


Figure 1.16. (a) The schematic diagram showing the screen-printed substrate; (b) top view of a SEM image of the fabricated cap wafer; (c) cross-section of the height reference wall and the outside micro groove in [50].

In 2018, A. Rautiainen et. al. published a work on the wafer level MEMS encapsulation using the AuSn/Pt SLID bonding at 320℃ with 3 MPa bonding pressure for 6" size wafers [51]. In this work, thin film Nanogetters^{TM} is used and getter activation starts at 352 ℃. Figure 1.17 shows the seal ring structure and related process flow.

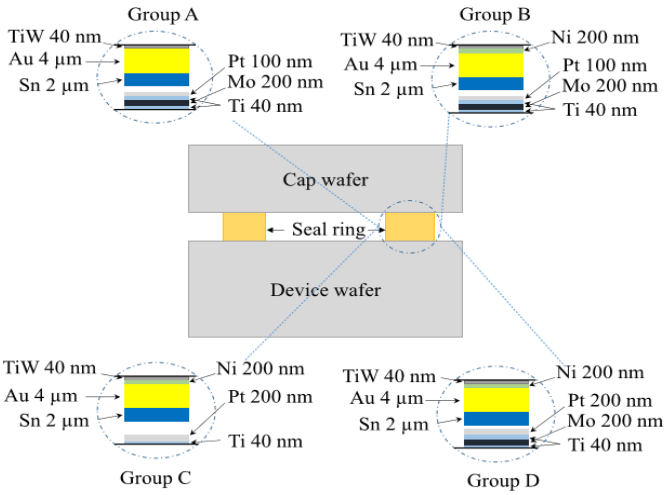


Figure 1.17. Schematic presentation of the bond structures in [51].

In 2020, Temel investigated Al-Ge, Au-In, and Au-Sn alloys in terms of chemical, structural, thermal properties, and capabilities for forming a reliable and device compatible bonding structures [19].

Overall, in the literature there are well established WLP approaches. The step coverage of metal-based alloys is not good because they are limited to few microns when compared with glass frit material. Also, thickness increment results with high stress in metal-based alloys so, the widely used hermetic packaging method is the glass frit bonding. Glass frit has some drawbacks including high bonding temperatures and large bonding rings. However, for getter activation also high temperature is a necessity. To conclude, WLVP of MEMS is application specific and Table 1.7 comparatively shows the summary of wafer level packaging works in the literature from 2000's to today.

Table 1.7 Tabulated form of the state-of-the-art wafer level vacuum packaging approaches since 2000's.

Author /Year	**WLP**	**Sensor**	**Lead Trans.**	**Max. Temp. (℃)**	**Pressure**	**Getter**	**Long Term (Days)**
Song et. al. /2000 [34]	Glass Frit	Gyroscope	Lateral	450	150mTorr	-	-
D. Sparks et. al./2001 [35]	Solder	Resonator	Lateral	-	1.5 Torr	-	42
E. Mottin et. al./2001 [36]	Solder	Bolometer	Lateral	-	1 Torr	NEG	-
T. Schimert et. al./2003 [37]	Solder	Bolometer	Lateral	-	4 mTorr	-	950
D. Sparks et. al./2005 [39]	Glass Frit	Resonator	Lateral	-	850 µTorr	Thin Film	-
Welch et. al./2007 [41]	TLP	Pirani Gauge	Lateral	300	200 mTorr	Thin Film	20
Welch et. al./2008 [43]	TLP	Pirani Gauge	Lateral	400	200 mTorr	Thin Film	180
Mitchell /2008 [7]	Eutectic	Pirani Gauge	Lateral	390	1-16 mTorr	Thin Film	1000
A. Yu et. al. /2010 [44]	Eutectic	Resonator	Lateral		200 mTorr	-	10
R. M. Haque et. al. /2011 [45]	Eutectic	Resonator	Vertical	400	-	Thin Film	-
Wu et. al. /2012 [46]	Glass Frit	Resonator	Lateral	430	1mbar	-	-
Xu et. al./2013 [47]	SLID	Resonator	Lateral	350	<0.1 Pa	-	-
Deillon et. al./2015 [25]	SLID	-	-	200	1.8 bar	-	-
Rautiainen et. al./2018 [51]	SLID	-	-	352	3.3 MPa	Thin Film	-
Temel/2020 [19]	TLP	-	-	440	-	-	-

1.3 Motivation, Research Objectives and Outline of the Thesis

Wafer level vacuum packaging (WLVP) compatible with CMOS processed wafers is most demanding issue, especially for MEMS based infrared detectors. Most common MEMS packaging approaches either use anodic bonding or metals such as gold that are not compatible with CMOS front end processing [52]. Therefore, there is a need for a robust, CMOS compatible bonding process that not only provides a hermetic seal and protection of the MEMS package but also provides electrical interconnections across the bond interface including low cost and small size abilities. Although for wafer level packaging there are various types ranging from anodic, glass-frit and direct to metal diffusion, adhesive and eutectic; in the scope of this thesis study Au-In TLP bonding and glass frit bonding selected and specialized for uncooled infrared bolometers.

The aim of this thesis is developing a multi-purpose, high performance, and low-cost 8” size wafer level vacuum packaging (WLVP) solution for MEMS-based long- wave infrared thermal detectors specialized for the technology development of uncooled resistive type IR MEMS bolometers processed in METU MEMS Center.

Uncooled infrared bolometer arrays have become the promising technology for the infrared imaging systems for various applications. Some of the IR imaging applications are thermography, nigh vision (military, commercial and automotive), mine detection, reconnaissance, surveillance, firefighting, medical imaging or high temperature detection, predictive maintenance and industrial process control. Bolometers are thermal infrared sensors, which absorbs electromagnetic radiation, and due to that absorption temperature increases accordingly; and it is a function of the radiant energy striking the bolometer and is measured with various ways such as thermoelectric, pyroelectric, resistive or other temperature sensing principles [53].

Uncooled IR bolometers need vacuum environment for the operation; it is known that these sensors accurately work with vacuum levels < 0.01 mbar. There are some design considerations for the packaging of bolometer arrays which can be listed as

accurate and reliable hermetic seal; integration of cap wafer with good infrared transmission; and high yield low-cost packaging [53]. For uncooled infrared micro bolometers many efforts have been made to improve the productivity and reduce the cost in the vacuum packaging issue. In the literature there are various packaging methods are reported up to day, ranging from wafer-level packaging [54]–[57], collective packaging [58], chip scale packaging [59], batch packaging [60], [61], and pixel-level packaging [62], [63] technologies.

In the thesis, the moth-eye structures are formed on both side of a polished flat silicon wafer without any cavity for the transmission improvements of the Si wafer in long wave infrared region (LWIR). The moth-eye structures are used for eliminating the AR coating usage, because AR coating usage has several disadvantages ranging from complex technology requirements to high cost and in a long-time degradation in coating quality. After patterning moth-eye structures, this wafer is bonded to another spacer wafer using low temperature Au-In TLP bonding approach. The TLP bonding has some advantages, and they can be listed as low bonding temperature, high remelting temperatures, under seal metallization (USM) layers do not contact with liquid phase, and surface treatment is not necessary for Au-In material system. After the TLP bonding, the spacer wafer is etched using DRIE for the cavity openings and inserting the moth-eye structures inside. Also, with the help of a shadow mask getter layer is deposited for obtaining high vacuum inside the cavity package. After the cap wafer preparation as a final bonding glass frit approach is selected for encapsulating the IR sensors. The glass frit bonding happens at around 430°C; this is good for perfect getter activation without any effort. Last but not least, some advantages of the glass frit can be listed as easy processing (there is no additional effort requirement like photolithography), strong bond strength, can handle larger surface topography, good hermeticity and high process yield. The bonding quality of the offered cap wafer technology is measured with three different approaches: He-leak tests, cap deflection, and Pirani vacuum gauges.

The organization of this thesis and the contents of the following chapters can be summarized as following: Chapter 2 provides information about the design, and process flow steps of offered cap wafer technology and sensor wafer.

Chapter 3 gives the fabrication results obtained during the optimizations of the offered 8” size wafer level hermetic encapsulation method which synergistically combined Au-In TLP bonding and glass frit bonding approaches. Also, device wafer fabrication is also mentioned in Chapter 3.

Chapter 4 begins with the cap wafer monitoring methods used for the hermeticity evaluation of the wafer level encapsulation processes. All the test results of the fabricated MEMS vacuum sensors in both atmospheric and vacuum level environmental conditions and characterization of them before and after wafer level packaging results are presented and discussed in Chapter 4.

Finally, Chapter 5 summarizes the concluding points and the possible future works.

CHAPTER 2

OFFERED CAP WAFER TECHNOLOGY APPROACH

This chapter introduces the new 8” size wafer-level fabrication and hermetic encapsulation process approach for uncooled infrared MEMS bolometers. Reliable wafer-level vacuum packages for infrared MEMS devices are formed by synergistically integrating Au-In TLP bonding and glass frit bonding process steps.

The cap wafer material, also called window in the literature, is made in single-crystal Si wafers with low oxygen concentration to obtain good IR transmission over the long wavelength range which is 8-12μm. Instead of standard AR coating deposited on both sides of the wafer, anti-reflective grove type gratings are processed based on the know-how developed at METU since 2012. The back side of the cap wafer, also called the window areas, is etched in DRIE to obtain a cavity for the sensors and Ferro glass paste is screen-printed after obtaining successful Au-In TLP bonding and grinding them. The process sequence for the WLP has advantages of building of additional thin-film getter structures into each die with the help of the shadow mask. Needless to say, the SSP Si CMOS probe wafer or sensor/device wafer prepared compatible with the designed cap wafer. After completing the fabrication of the cap and device wafers separately; they aligned and attached to each other and sealing take place in vacuum by applying glass-frit bonding. After sealing, the chips are removed by standard wafer dicing in order to release the wire bonding pads. Figure 2.1 shows a detailed cross section of the offered 8” size wafer level hermetic encapsulation method.

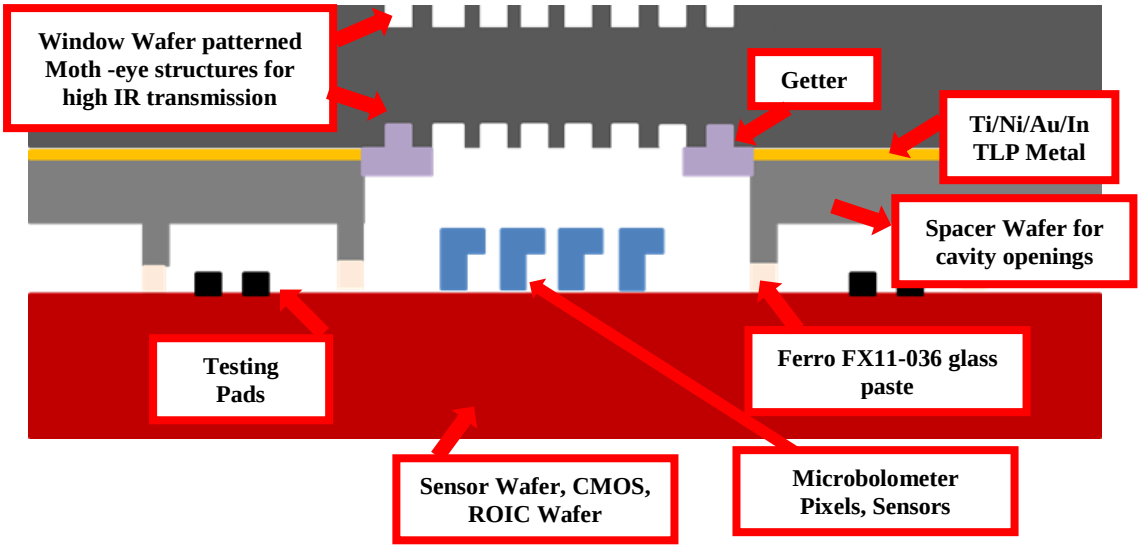


Figure 2.1. The cross-section of 8" size wafer level hermetic encapsulation method specialized for uncooled infrared MEMS bolometers.

2.1 Cap Wafer Process Flow

The planned scenario's schematic for the offered cap wafer technology is detailed in Figure 2.2.

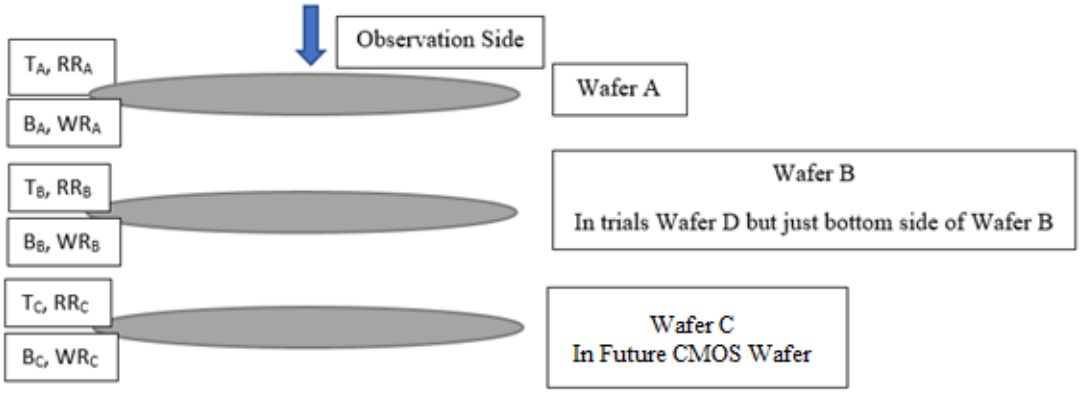


Figure 2.2. The schematic representation of the offered cap wafer stack's planned scenario.

After showing the schematics it can be better to explain the meanings of the wafers before presenting the offered process flow steps and other abbreviations' meanings could be found in the "LIST OF ABBREVIATIONS" part of the thesis.

Wafer A: Window cap wafer for high IR transmission in LWIR, 725 μm thick DSP wafer including grating structures in both sides and metallization in bottom side for Au-In TLP bonding.

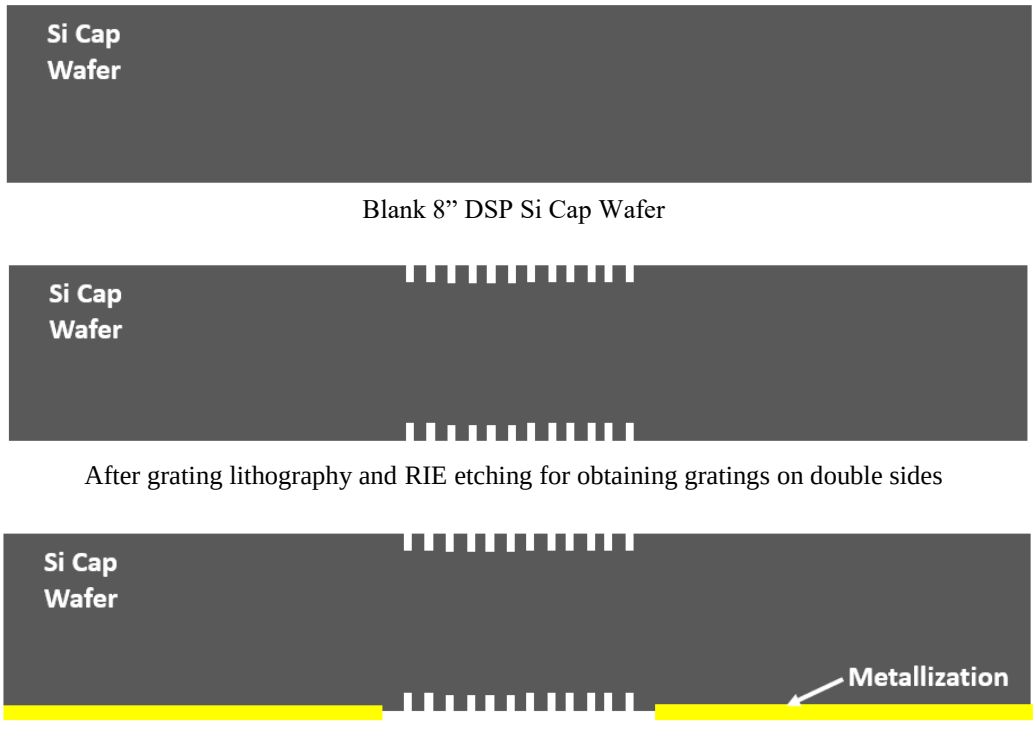
Wafer B: Spacer wafer, 725 μm thick SSP wafer or 400 μm DSP wafer (to eliminate the grinding step) both of them including metallization in top side for Au-In TLP bonding and cavity opening mask to obtain 150-200 μm cavity to integrate grating structures inside, screen printing for glass frit pasting alignment mark and shadow mask for getter deposition alignment mark in bottom side.

Wafer C: CMOS Probe wafer; by processing Wafer C, CMOS Wafer's top side is going to be simulated; and it is planned to observe as if the real wafer existed, and glass frit bonding has been tried for the optimization. Also, to monitor the vacuum level inside the cap some preliminary work was done; vacuum sensors are produced and characterized in die level and some new designs also drawn. As a final step it is decided to integrate those vacuum sensors to Wafer C.

Wafer D: Cap Cavity Probe Wafer. By processing Wafer D, Au-In TLP bonded stack of Wafer A and Wafer B cap wafers' bottom side is going to be simulated for observing both screen printing mask alignment is successful during glass pasting and shadow mask alignment is successful before Ti getter deposition. In screen printing step Ferro FX11-036 model glass paste is used and all the screen-printing steps are performed in METU GÜNAM Center. Also, for getter deposition purposes after optimized solution found in 6" size compatible shadow mask, 8" shadow layout is drawn, produced, and optimized to integrate proposed packaging design.

2.1.1 Proposed Packaging Design and Process Flow for Au-In TLP Bonding

In this sub-section, Figure 2.1 is going to be detailed step by step up to Au-In TLP bonding. Figure 2.3 presents Wafer A (Si Cap Wafer) process flow including grating structures in the double sides of the wafer for transmission improvements in the proposed packaging design. Notice that both for protection and etch stop purposes at the end of the grating's lithography passivation SiO_2/Si_3N_4 is coated. Similarly, Figure 2.4 shows Wafer B (Spacer Wafer) process flow which is used for cap cavity formation for inserting subwavelength antireflection grating structures inside the cavity for transmission improvements. After preparing Wafer A and Wafer B separately; finally, Figure 2.5 shows the low temperature Au-In TLP bonded Wafer A+B stack which is ready to cap cavity formation step.

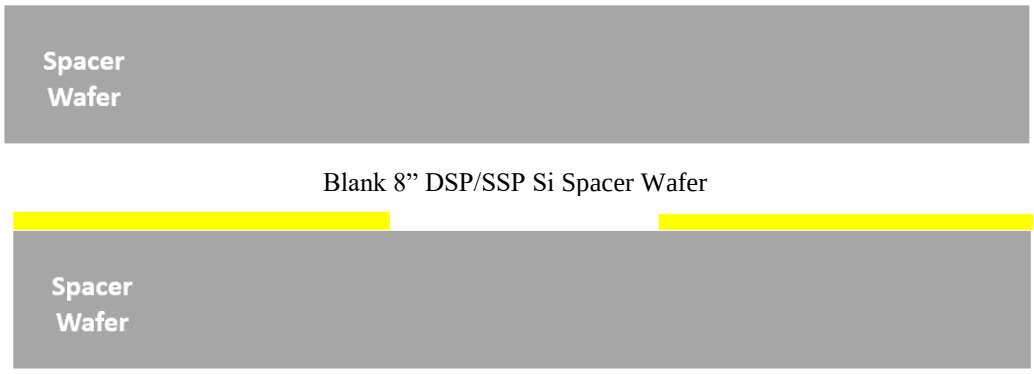


Blank 8" DSP Si Cap Wafer

After grating lithography and RIE etching for obtaining gratings on double sides

After metallization lithography, metal deposition, and lift-off

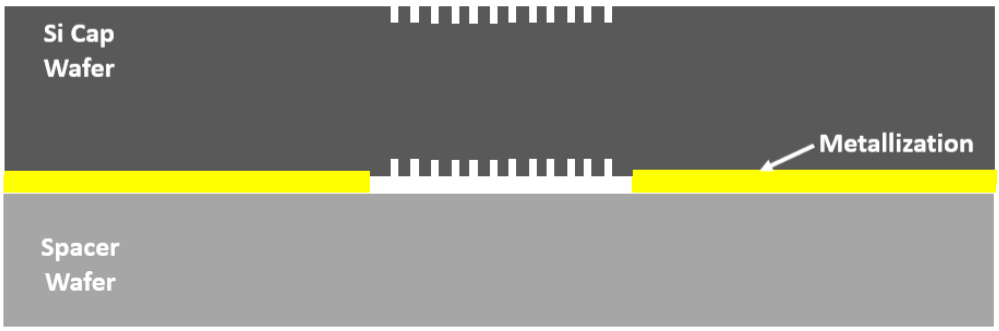
Figure 2.3. Wafer A process flow steps including groove type moth-eye structures in double sides.



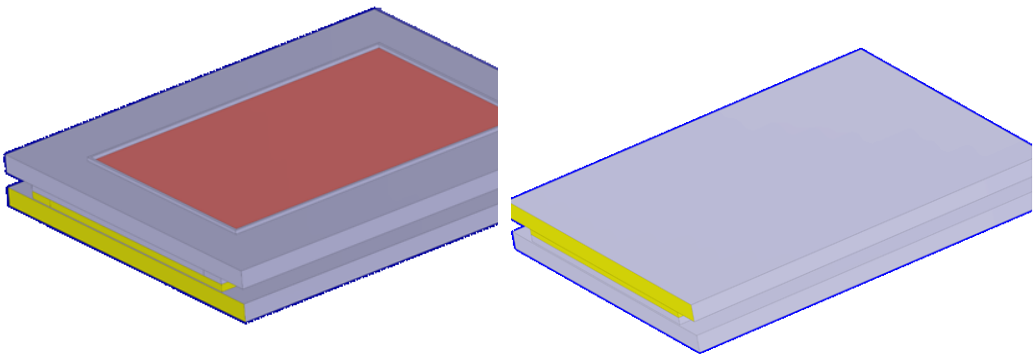
Blank 8” DSP/SSP Si Spacer Wafer

After metallization lithography, metal deposition, and lift-off

Figure 2.4. Wafer B process flow steps which would be used for cavity openings.



After Au-In TLP Bonding



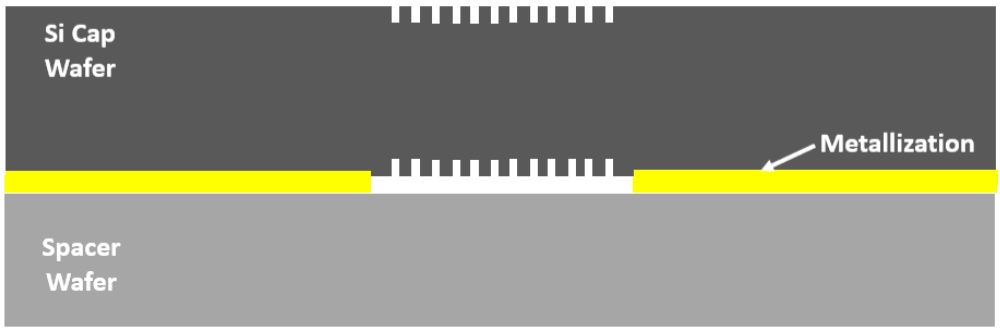
Front Side of the Au-In TLP Bonded Wafer A+B Stack

Back Side of the Au-In TLP Bonded Wafer A+B Stack

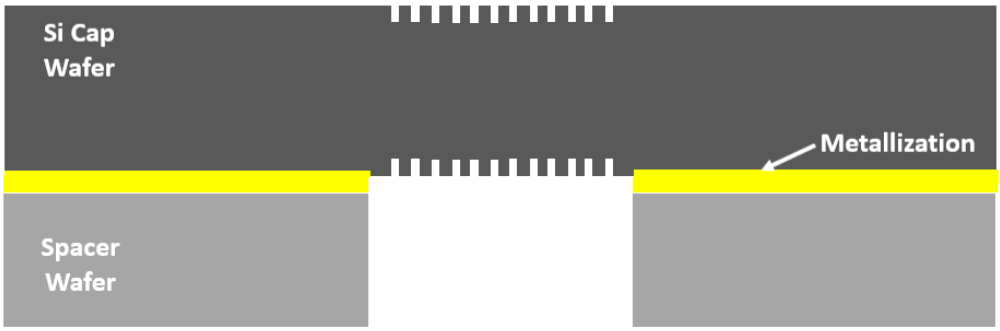
Figure 2.5. The low temperature Au-In TLP bonded Wafer A+B stack cross-section and 3D representation.

2.1.2 Process Flow for Cavity Openings

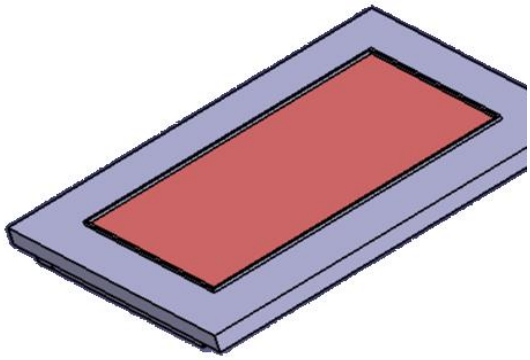
At the end of the Au-In TLP bonding performance of the window cap wafer and the spacer wafer; the spacer wafer is etched using deep RIE approach to form the cavity opening of the cap wafer stack, where the getter layer is going to be deposited using a shadow mask. Figure 2.6 shows the process steps details, and the 3D visualization.



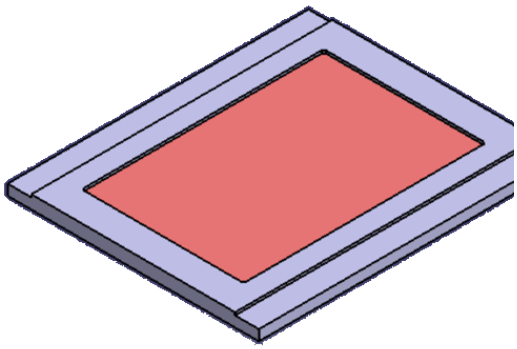
Au-In TLP bonded Cap Wafer stack ready for cavity lithography



Cavity openings with DRIE & Passivation oxide removal



Front Side of the Au-In TLP Bonded Wafer A+B Stack



Back Side of the Au-In TLP Bonded Wafer A+B Stack After Cavity Opening

Figure 2.6. The proposed Cavity Process Flow Steps and 3D representation.

2.1.3 Proposed Packaging Design and Screen-Printing the Paste for Glass Frit Bonding and Getter Deposition

After cap cavity formation, the next step is screen-printing the cap wafer for glass frit bonding purposes and finally getter material deposition with shadow mask for obtaining high vacuum schematic representation could be found in Figure 2.7.

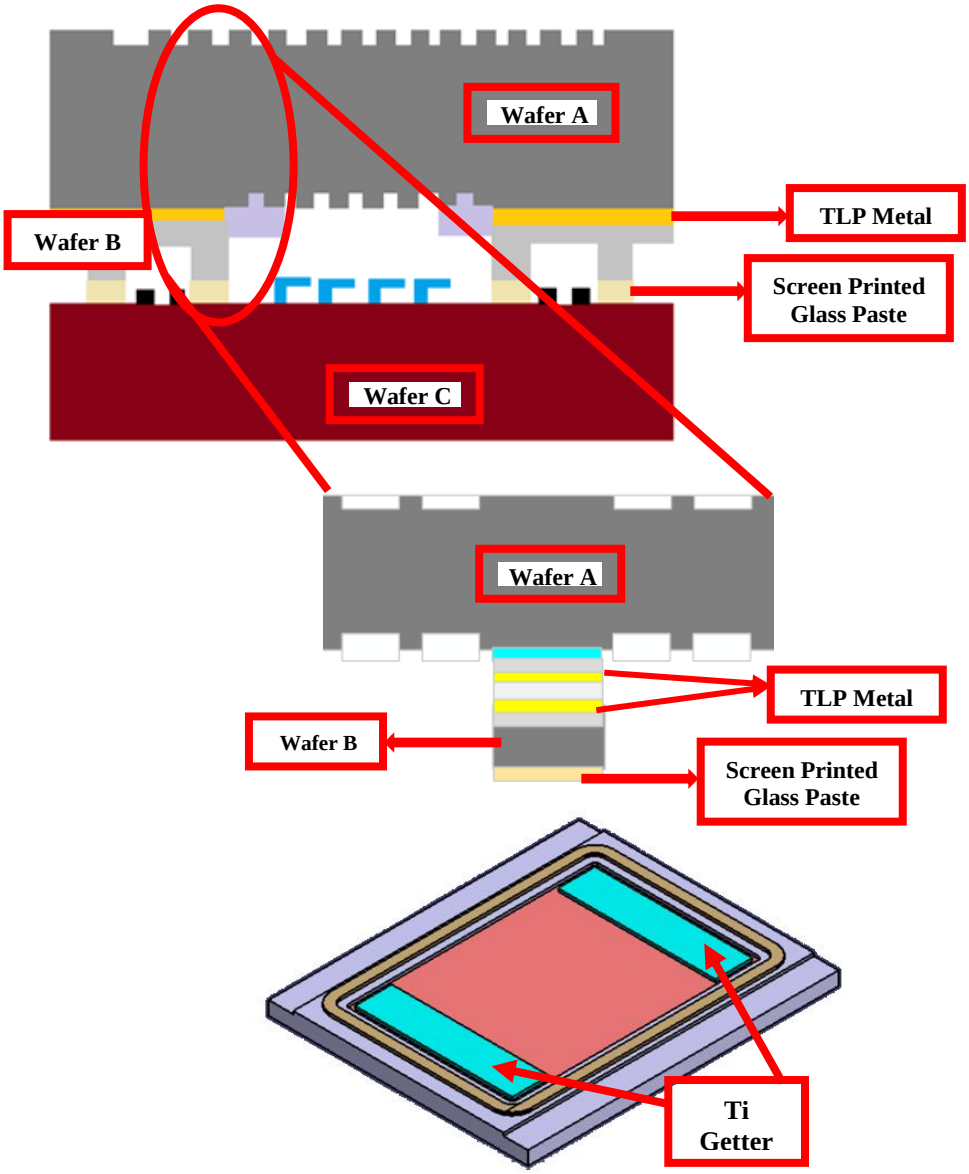


Figure 2.7. The schematic representation of screen-printed glass pastes on the proposed cap wafer.

2.2 Sensor Wafer Process Flow

SSP Si CMOS probe wafer or sensor/device wafer is prepared compatible with the designed cap wafer. After searching the literature, it is decided to adapt resistive type Pirani gauges as in the study of [64] and variation are designed and fabricated in the scope of this study by using again METU MEMS Center clean room facilities. It is decided to integrate Pirani vacuum sensors to Silicon test wafers (Wafer C) for wafer level packaging purposes. Geometrical design properties can be seen in Figure 2.8 and process flow steps are shown in Table 2.1 for fabrication of Wafer C.

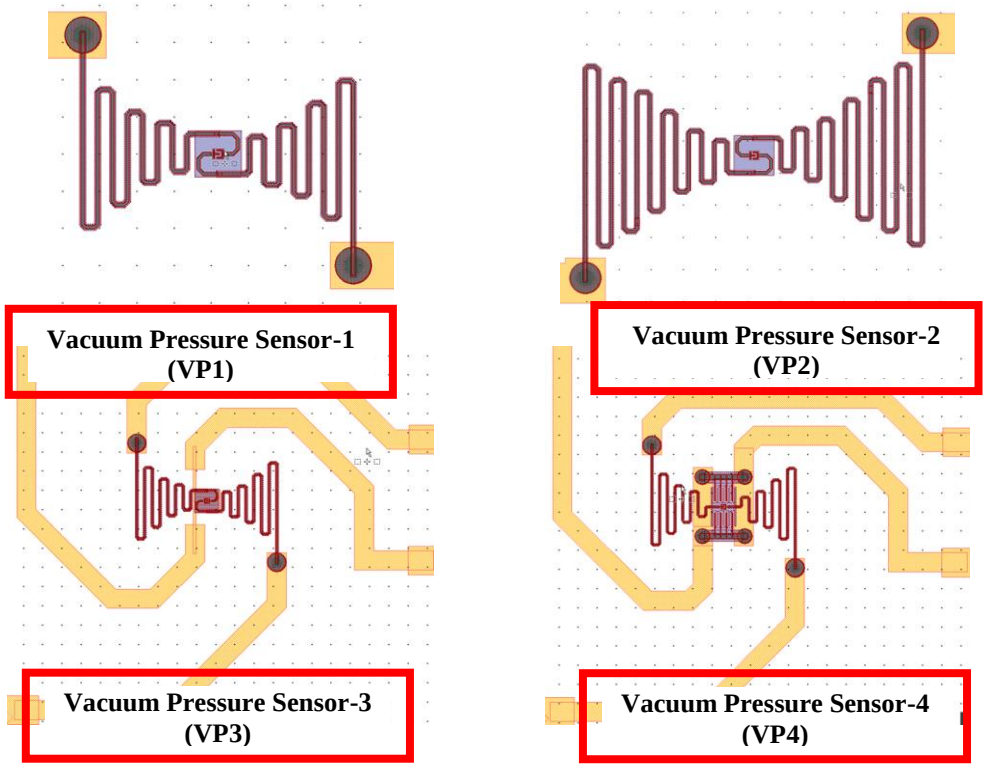
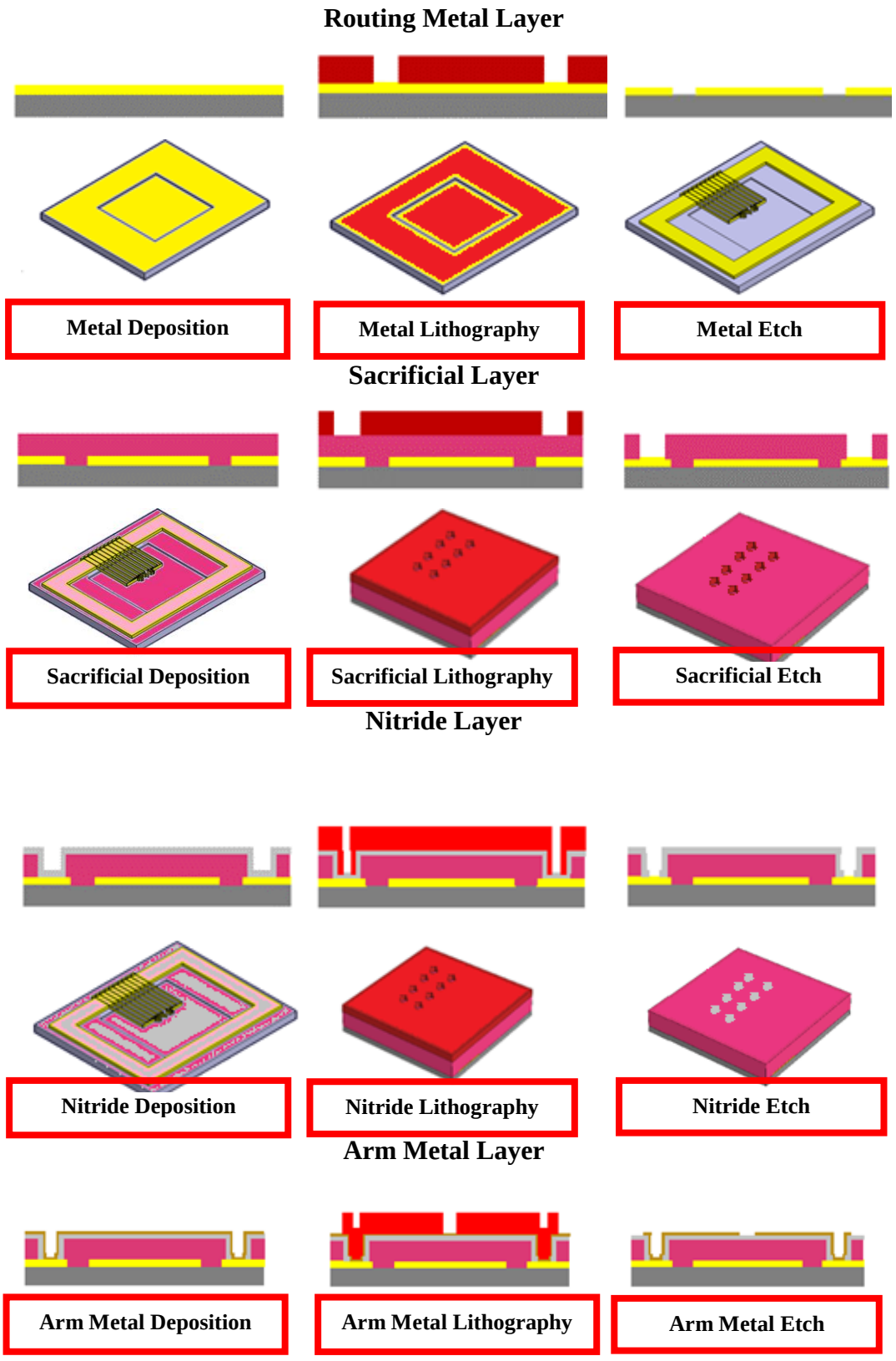
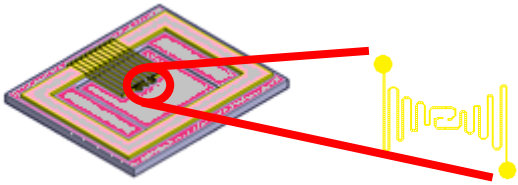


Figure 2.8. The images showing layout details of four different vacuum pressure sensors designed and produced in METU MEMS Center.

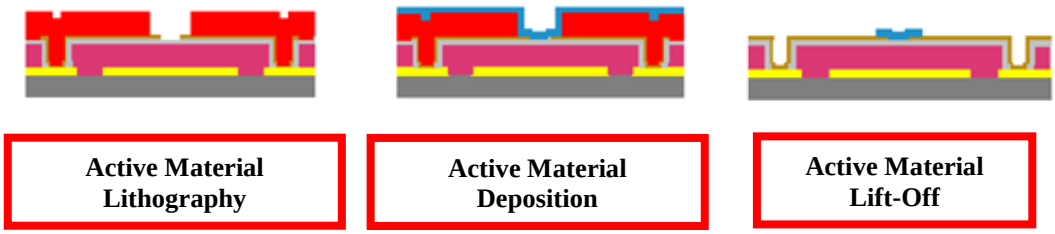
The major difference between vacuum pressure sensor 1 and 2 is the arm lengths; in VP1 arm length is 190 µm whereas in VP2 the arm length is 440 µm and other design geometries are the same. VP3 and VP4 have the arm lengths of 218 µm.

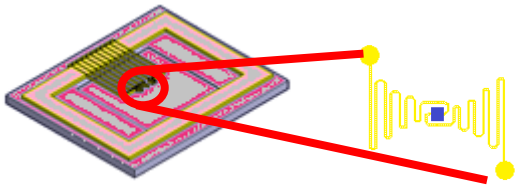
Table 2.1 Wafer C Process Flow Steps



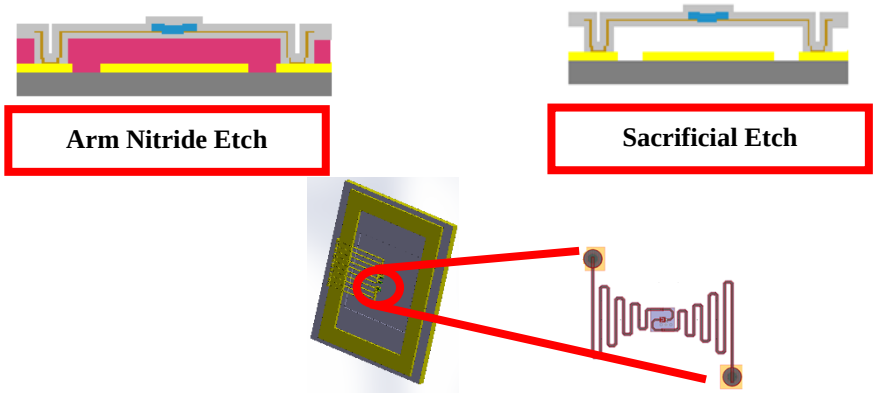


Active Material Layer





Arm Body Nitride/Structural Layer Deposition, Litography and Etch & Sacrificial Layer Removal



After completing the fabrication of the cap and device wafers separately; they aligned and attached to each other and sealing take place in vacuum by applying Glass-Frit bonding. After sealing, the chips are removed by standard wafer dicing in order to release the wire bonding pads.

CHAPTER 3

FABRICATION & OPTIMIZATION STUDIES

This chapter introduces the new 8” size wafer-level fabrication and hermetic encapsulation process approach for one version of uncooled infrared MEMS bolometers processed in METU MEMS Center. Au-In TLP bonding and glass frit bonding was integrated synergistically to form reliable wafer-level vacuum packages for MEMS devices and experimental steps detailed one by one.

The organization of the chapter is done as follows: First of all, Section 3.1 explains wafer level packaging using Au-In TLP bonding results ranging from AR Gratings optimization for transmission increasement to Au-In material systems microfabrication for TLP bonding and the characterization and inspection outputs such as optic microscope, scanning electron microscope and surface acoustic microscope, mechanical shear stress analyzes, reliability and repeatability test results. Secondly, after the successful Au-In TLP bonding, in our center for the first time grinding of the 8” size bonded wafer stacks are tried for decreasing the stacks total thickness, and bonded wafer stack thinning process worked properly with Strasbaugh Grinder Machine; and alternative 400µm thin wafer usage for eliminating grinding steps detailed as a first part; then, cap cavity formation step details for inserting subwavelength antireflection grating structures inside the cavity for transmission improvements are presented in Section 3.2 and Section 3.3. Next, Section 3.4 provides the details of Ferro FX11- 036 model glass frit screen- printing optimization, frit firing trials and glass- frit bonding results and the characterization and inspection steps ranging from optic microscope, scanning electron microscope and surface acoustic microscope analyzes to mechanical shear stress analyzes and reliability and repeatability test results. Then, Section 3.5 summarizes the production

of shadow mask for getter integration and performed experimental works. After explaining the cap wafer fabrication and optimization steps; sensor wafer fabrication steps detailed in Section 3.6. Finally, in Section 3.7 wafer level hermetic encapsulation of sensor wafer with offered cap wafer technology is detailed.

3.1 Wafer Level Packaging Using Au-In TLP Bonding

In this study, 8” wafer level Au-In TLP hermetic encapsulation technique have been selected as a first branch for offered cap wafer design and its details given below subtitles one by one.

3.1.1 Anti-Reflection Gratings Instead of ARC for Transmission Increments of the Cap Wafer

A double side polished (DSP) Si based cap wafer typically transmits around 50% within the LWIR (8–12 μm) wavelength range, and transmissivity can be increased above 85% with AR coating of stacked layers on both sides of the cap wafer [65], [66]. Unfortunately, AR stack layers usage is not only expensive but also complex technology for achieving a high transmission performance and they requires high temperatures causing delamination and performance degradation issues especially for WLVP applications [67], [68]. For that purpose, recently for one version of uncooled infrared MEMS bolometers used and developed in METU in 6” wafer size is sent to another country for AR coating steps, so this is not only time consuming but also costly and decreases the yield of the sensors. Alternatively, sub wavelength antireflective gratings (SWARGs) have been proposed since 1986 for increasing the transmission, which is achieved by patterning and micromachining on the surface the cap wafer pillar-like/moth-eye or groove-like/inverse moth-eye structures [67]–[69].

Moth-eye structures alternative to AR coating has been developed by METU imaging sensor group since 2012[1], and IR transmission better than %72 had been demonstrated on the moth-eye structures fabricated on one side of the double-side polished (DSP) Si wafers in 2012, suggesting IR transmission better than %92 if the moth-eye structures were fabricated on the two sides of double-side polished Si wafers, a performance very close to the transmission of AR coated Si wafers. As a follow up to these experimental studies, numerical modeling and simulations were performed at METU for pillar and groove type gratings with various topological configurations changing in various period sizes, various heights/depths, and various pillar/groove width-to-period ratios, and these results were experimentally verified and published [70].

Single-side polished (SSP) 8-inch size Si wafers are used for transmission improvement experiments during the process development steps (Figure 3.1) considering the previous studies at METU. After the optimization in SSP dummy wafers, the gratings are applied both side of the real process cap wafer by using double side polished (DSP) 8-inch size cap wafers with convenient die size design, which is compatible with the uncooled infrared MEMS bolometers produced at 8" wafer size; and reticle production (Figure 3.2). All the process is performed in 8" size which will increase the yield and number of sensors.

[1] The internal reports of METU imaging sensors group submitted by Dr. Mahmud Yusuf TANRIKULU to Prof. Dr. Tayfun AKIN.

The performed recipe details in METU MEMS cleanroom are listed below.

- Get one 8” Si wafer.
- Measure 8” wafer’s transmission before starting lithography processes. Notice that all infrared measurements are performed with the reflection/transmission (R/T) module of J.A.Woollam IR Ellipsometer, and during the measurements following settings are set: a resolution of 8 cm^{-1}, a bandwidth of 0.04 μm, and scans/spectrum of 50.
- De-hydration baking at 110℃ in N_2 environment.
- Spin coating of photoresist (PR).
- Soft-bake on hotplate.
- Clean wafers back side.
- UV expose in ASML PAS5500-200 Stepper System.
- Development (etching of UV exposed PR in development solution) in SUSS ACS 200 Automatic Coater and Developer.
- Optical microscope and SEM investigation.
- RIE 2 silicon etching process.
- PR strip with PRS 2000 for 30 minutes (Figure 3.2).
- Measure 8” wafer’s transmission after lithography processes in WVASE-IR program with the R/T module of J.A.Woollam IR Ellipsometer.

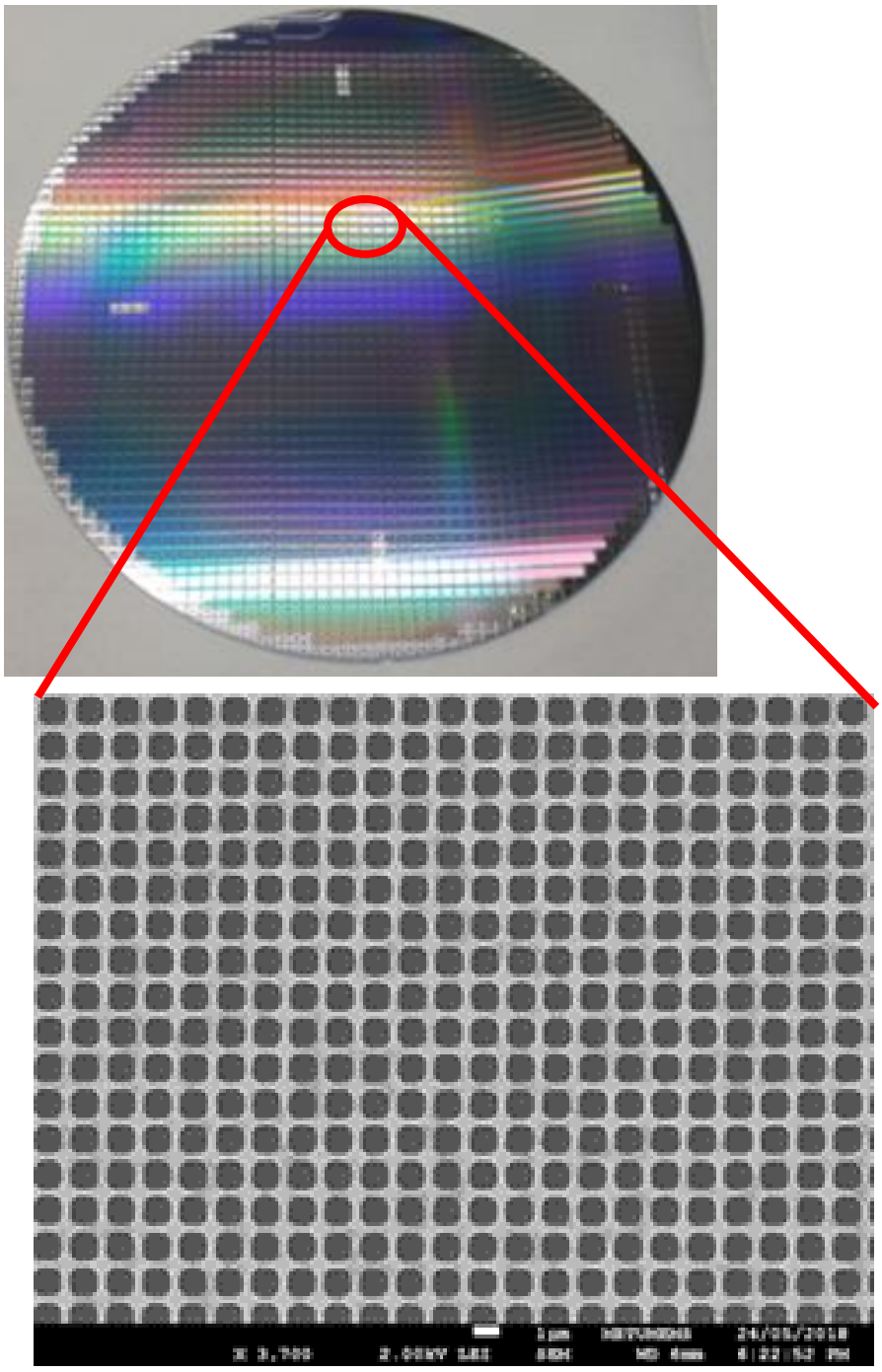
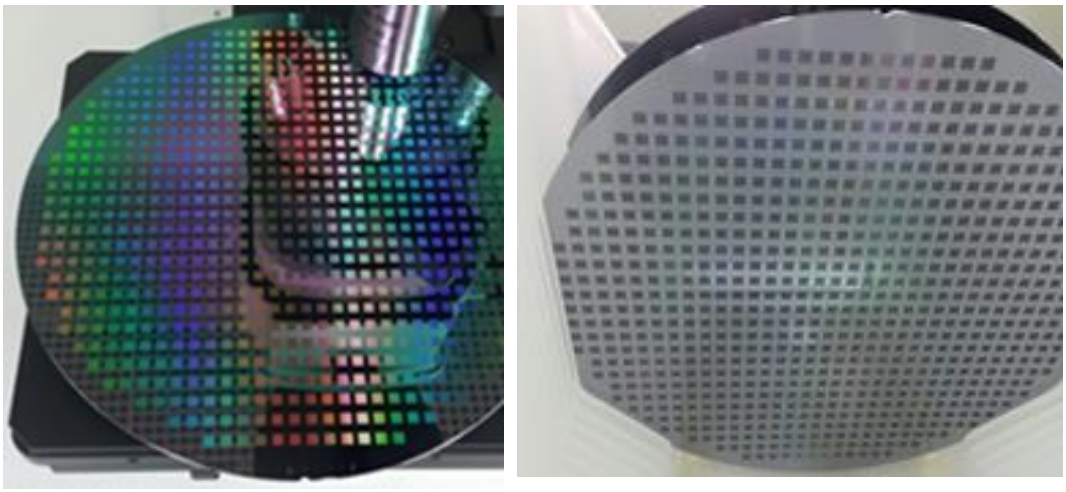
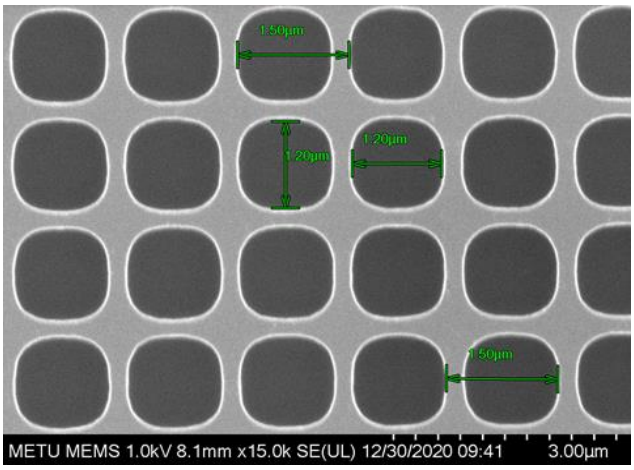


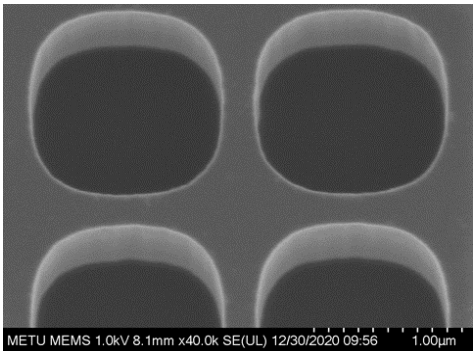
Figure 3.1. The processed 8” size dummy SSP Si Cap wafer and closure SEM investigations of it to show square grooves are obtained.

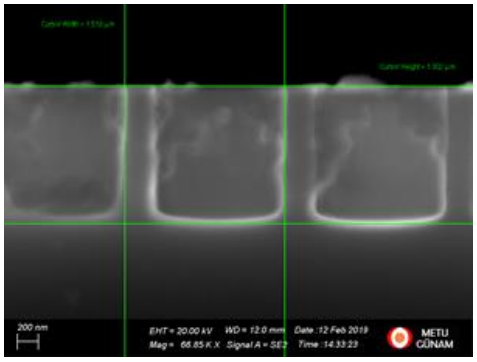


(a) (b)



(c)





(d) (e)

Figure 3.2. After the optimization, (a-b) the gratings are applied both side of the real process cap wafer by using 8” size DSP Si cap wafer with convenient die size design (772 dies); and (c-e) SEM investigations for determining x-y (1.2µm) and z (1.3µm) dimensions of the grooves.

The comparison of a SSP and a DSP mono-crystalline Si based cap wafers transmission within the LWIR (8– 12 µm) wavelength range could be seen in Figure 3.3. As can be seen, DSP Si wafer transmits around 50-55% whereas SSP wafer transmits around 40-45%.

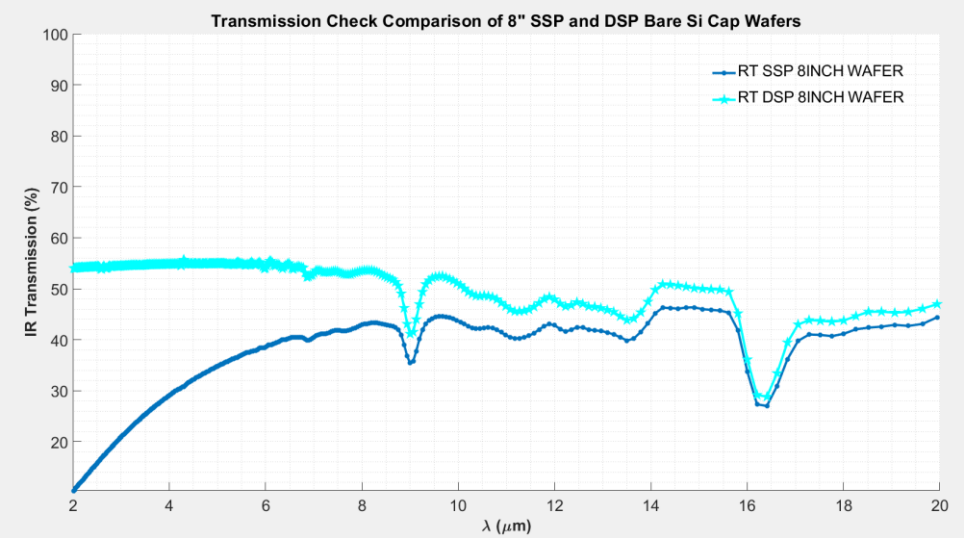


Figure 3.3. The comparison of a SSP and a DSP mono-crystalline Si based cap wafers transmission within the 2–20 µm wavelength range before processing them.

After the optimization, the AR gratings are applied first of all the SSP mono- crystalline silicon (Si) based 8" size three different cap wafers to observe how the square grooves improve the transmission within the LWIR (8–12 µm) wavelength range (Figure 3.4). As it can be seen for, bare silicon at 8-12 µm wavelength range transmission is 45% and for the processed wafers at 8-12 µm wavelength range transmission is around 60% so there is enhancement after process.

After checking single side polished wafer's transmission increment, the next step is the adaptation of AR gratings to double sides of the mono-crystalline silicon (Si) based cap wafers and observe how double side patterned AR grating structures effect the transmission. The performed process steps are exactly same to the double sides of the wafer. Transmission repeatability tests plot could be found in Figure 3.5. As it can be seen for 8-12 µm wavelength transmission is 85% so there is enhancement after process.

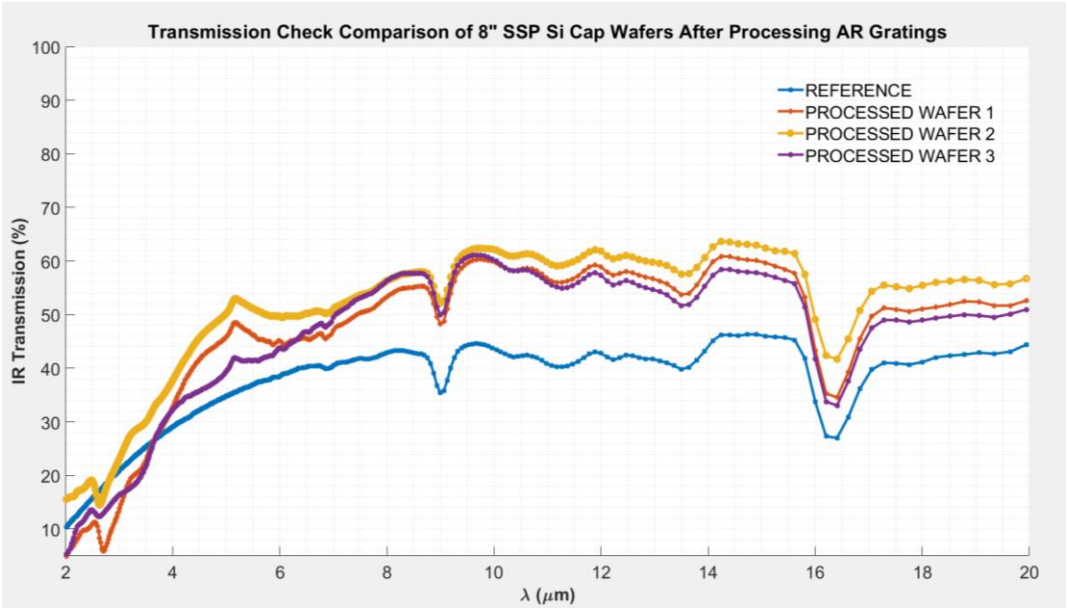


Figure 3.4. Repeatability test comparison for blank SSP 8” Si wafer’s transmission versus wavelength plot and processed 8” Si Cap wafers transmission measurements from 3 different sample wafers. As it can be seen for, bare Si at 8-12 μm wavelength range transmission is 45% and for the processed wafers at 8-12 μm wavelength range transmission is around 60% so there is enhancement after process.

Overall comparison for single side patterned and double side patterned case comparison could be found in Figure 3.6. Last but not least, in those trials 8” DSP wafers from Wafer Pro company have been used because they are relatively cheap and produced by CZ (Czochralski) type process; but if the one needs to eliminate the transmission decrement in 9 μm; 8” DSP wafers from Si-Mat company which is produced by float zone method can be used. In the scope of the study also 8” DSP wafers are ordered from Si-Mat company and their IR transmission are measured with the reflection/transmission (R/T) module of J.A.Woollam IR Ellipsometer, with the following settings: a resolution of 8 cm^{-1}, a bandwidth of 0.04 μm, and scans/spectrum of 50. The related plot of blank 8” DSP Si wafer’s transmission versus wavelength comparison could be seen in Figure 3.7.

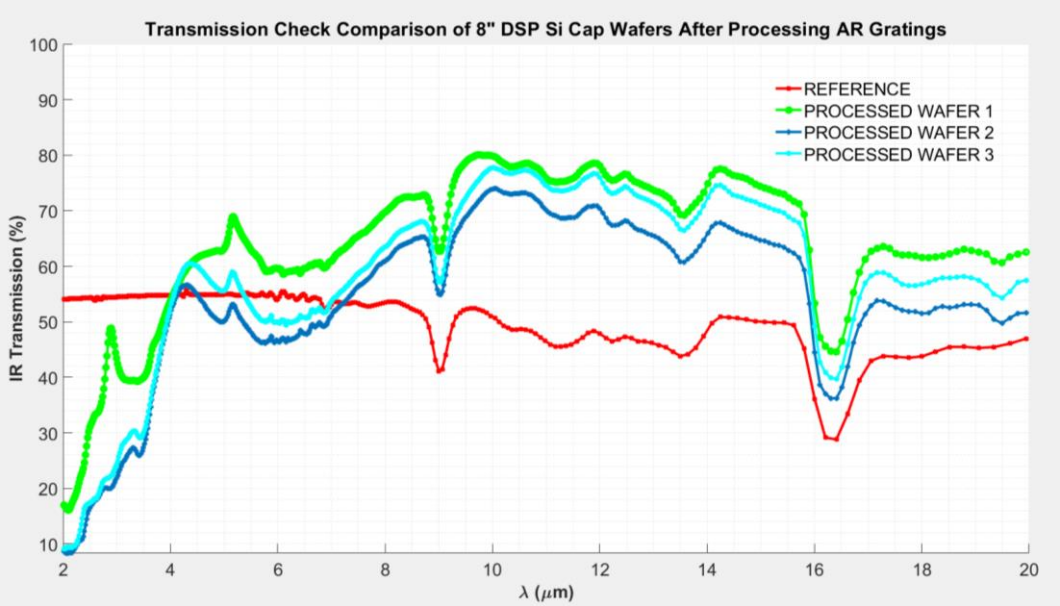


Figure 3.5. Repeatability test comparison for blank DSP 8" Si wafer's transmission versus wavelength plot and double side processed 8" Si Cap wafers transmission measurements from 3 different sample wafers. As it can be seen for, bare Si at 8- 12 μm wavelength range transmission is 50% and for the processed wafers at 8- 12 μm wavelength range transmission is around 80-85% so there is enhancement after process.

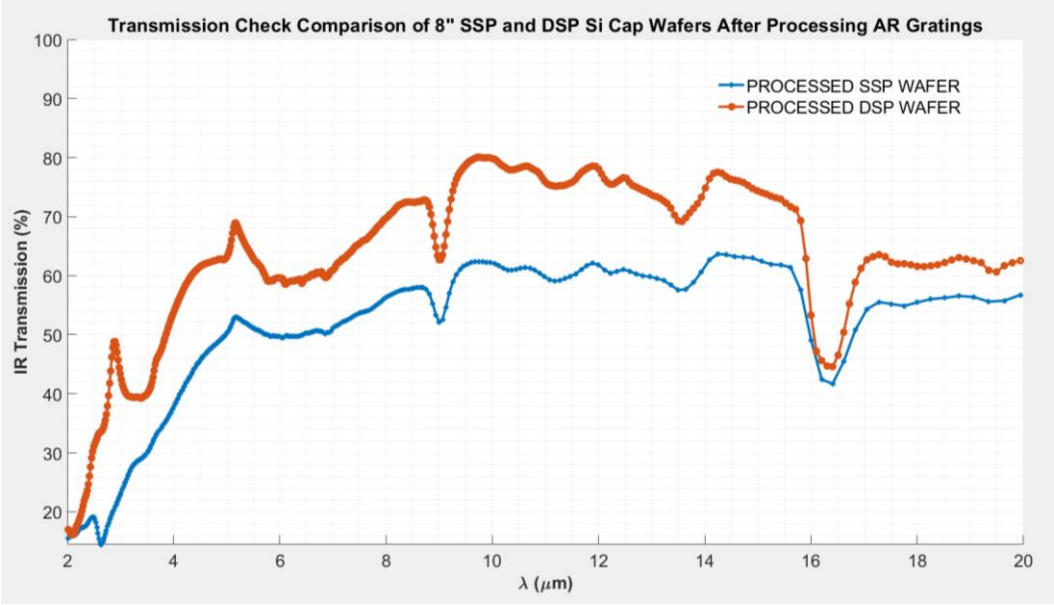


Figure 3.6. Repeatability test comparison check for 8" Si SSP and DSP wafers transmission versus wavelength plot transmission measurements after full grating processes on single side for SSP; and both sides for DSP.

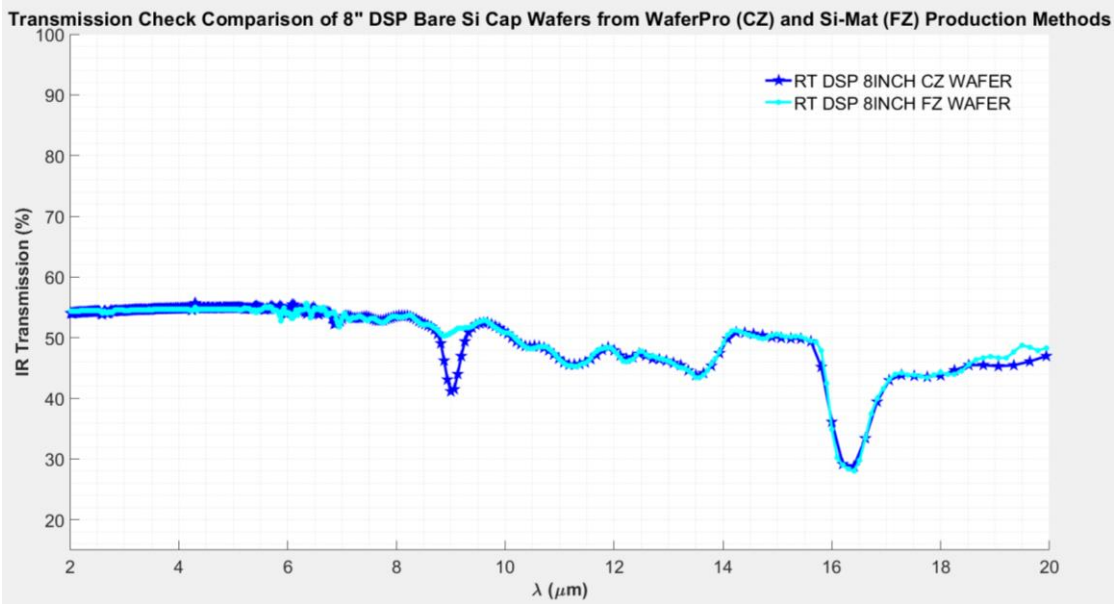
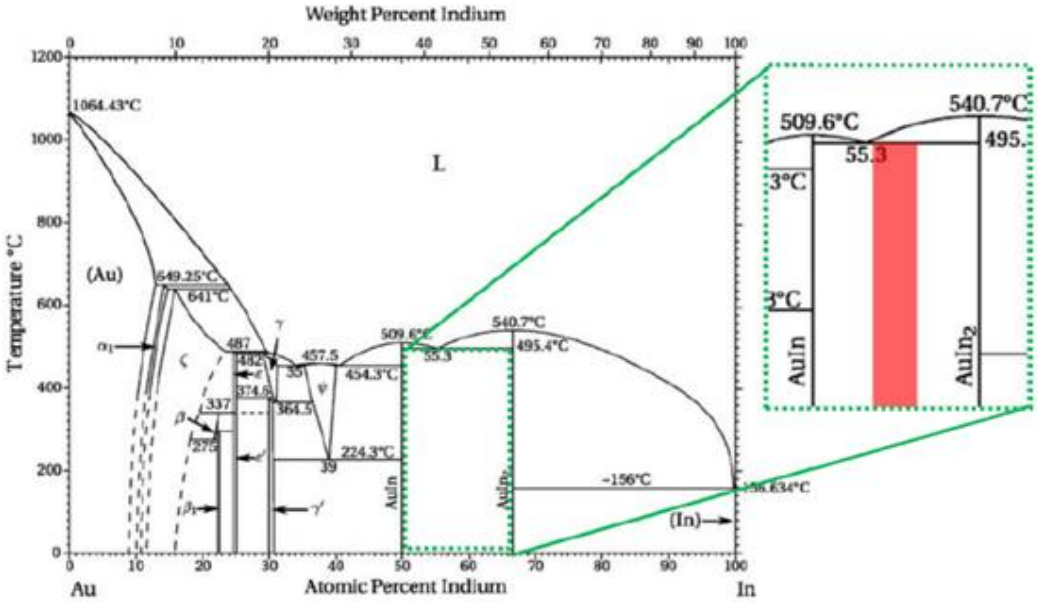


Figure 3.7. Transmission comparison for blank 8" DSP Si wafer's transmission versus wavelength plot of Si-Mat (FZ method) and WaferPro (CZ method) wafers. As it can be seen in Si-Mat wafer the transmission decrement in 9μm is not observed.

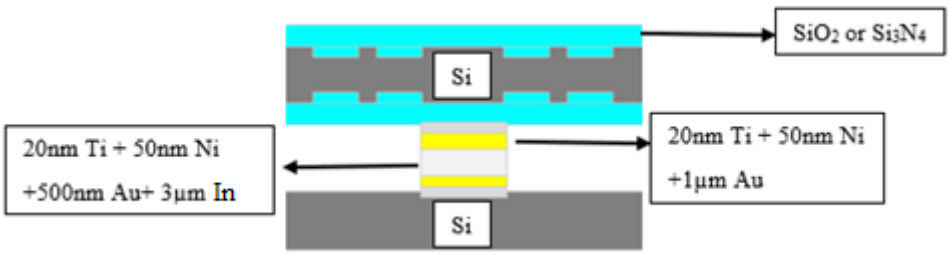
3.1.2 The Studied Au-In Material Systems and Microfabrication for TLP Bonding

The advantage of TLP bonding is the melting temperature of bonding area ($T_{re\text{-}melting}$) is higher than bonding temperature ($T_{bonding}$) after bonding. The Au-In material system phase diagram is shown in Figure 3.8. As can be seen in the Figure 3.8, Au- In material system has a complicated phase diagram including many intermetallic phase formations and among the others the region between AuIn and $AuIn_2$ intermetallic is significantly convenient for TLP bonding applications. In this region, the re-melting temperature is 495°C for a wide range of compositions; so it can be concluded that the minor variations in composition change do not affect the re-melting temperature of the final bond. Although in wafer level packaging using glass-frit bonding part of the thesis details is explained, it would be better to mention why Au-In TLP bonding is selected as a first branch of the study. The first reason is

the bonding temperature is low (200℃) and the second reason is the re-melting temperature is high (495℃); so in the second branch of the proposed packaging design which is glass-frit bonding of Wafer C with Wafer A+B stack bonding temperature of 430℃ will be applied and luckily it is below 495℃. Third reason is that the under-seal metallization (USM) layers do not contact with the liquid phase and finally surface treatment is not necessary for Au-In material system. As in the study of [19] the USM layers for the adhesion/wetting and barrier functions 20nm Ti and 50nm Ni is applied and Au-In bond material configuration is specialized 1µm Au for Wafer A and 500nm Au and 3µm In for Wafer B.



(a)



(b)

Figure 3.8. (a) Au-In phase diagram[19] and (b) the offered Au-In bond material configuration.

As it is known for the new wafer-level fabrication and hermetic encapsulation process approach for one version of uncooled infrared MEMS bolometers; 8-inch size wafers are used during the development of all process experiments. Needless to say, the grating formation for transmission improvement and bond ring formation for Au-In TLP bonding have been processed/fabricated by using the MEMS fabrication techniques.

Now the used microfabrication techniques are going to be detailed. The first step is UV lithography which is necessary for pattern generation on the wafer. After PR spin coating to Wafer A and Wafer B cases, UV expose step of grating lithography (for Wafer A top and bottom side) and bond ring metallization lithography (for Wafer A bottom and Wafer B top side) have been performed by using ASML PAS 5500/200 Stepper System (Figure 3.9).

Wafer Handling System of Stepper

Front View and User Control Interface

Figure 3.9. The pictures of ASML PAS 5500/200 Stepper UV Lithography System used in METU MEMS Center.

The second step is reactive ion etching process of patterned Si wafers for grating structures formation (for Wafer A top and bottom side) in RIE-II Systems (Reactive Ion Etching System) used in METU MEMS Center (Figure 3.10) and for protection purposes during the bottom side processes, SiO_2/Si_3N_4 coating (for Wafer A top side) and for etch stop purposes SiO_2/Si_3N_4 coating (for Wafer A bottom side) in PECVD- II Systems (Plasma Enhanced Chemical Vapor Deposition System) used in METU MEMS Center (Figure 3.11)

Overall View and User Control Interface

Wafer Handling System of RIE-II

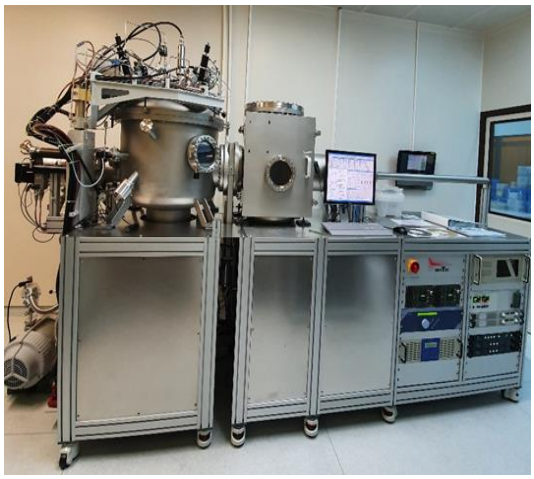
Figure 3.10. The pictures of RIE-II System used in METU MEMS Center.

Overall View and User Control Interface

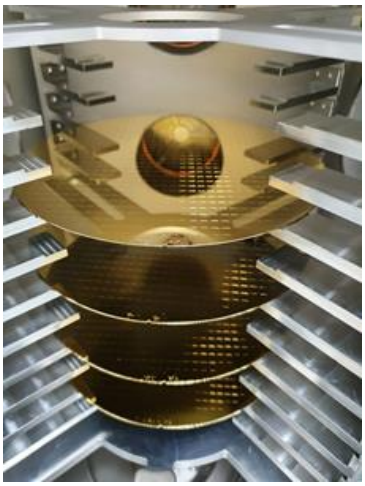
Wafer Handling System of RIE-II

Figure 3.11. The pictures of PECVD- II System used in METU MEMS Center.

The third step is metal deposition to Wafer A and Wafer B after bond ring metallization lithography was performed. For Wafer A and Wafer B, Ti/Ni/Au metal deposition steps are performed in BESTEC-II Sputtering Systems (Figure 3.12) and In metal deposition step for Wafer B is performed in Nanovak NVTH-500 Thermal Evaporation System (Figure 3.13).

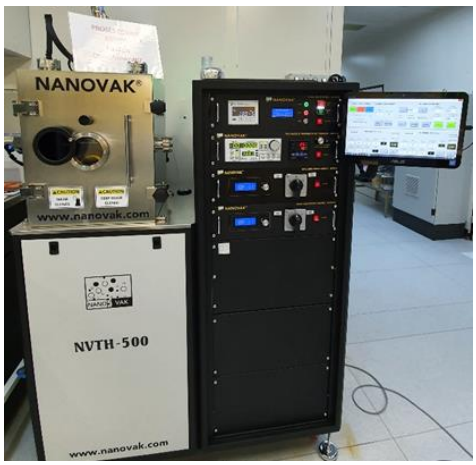


Overall View and User Control Interface

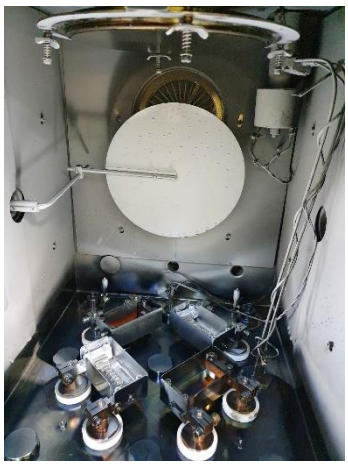


Wafer Handling System of BESTEC-II

Figure 3.12. The pictures of RIE-II System used in METU MEMS Center.



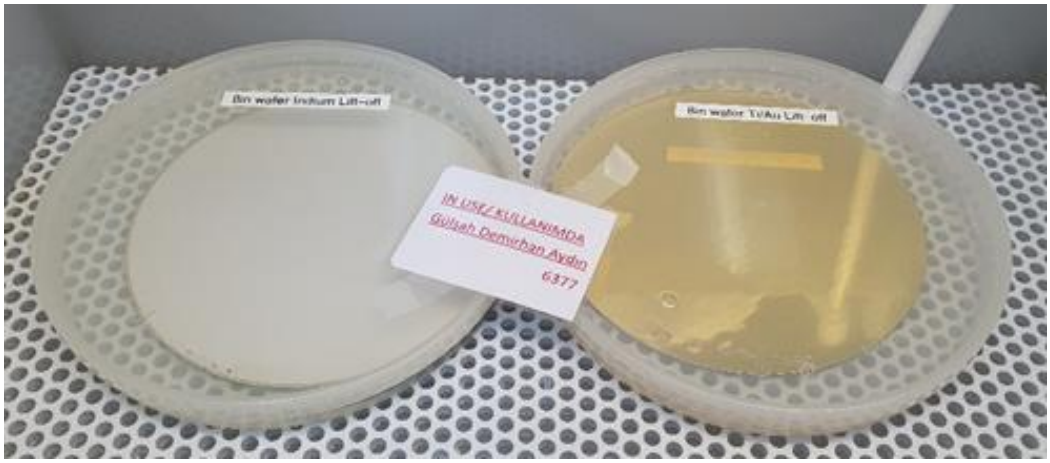
Overall View and User Control Interface



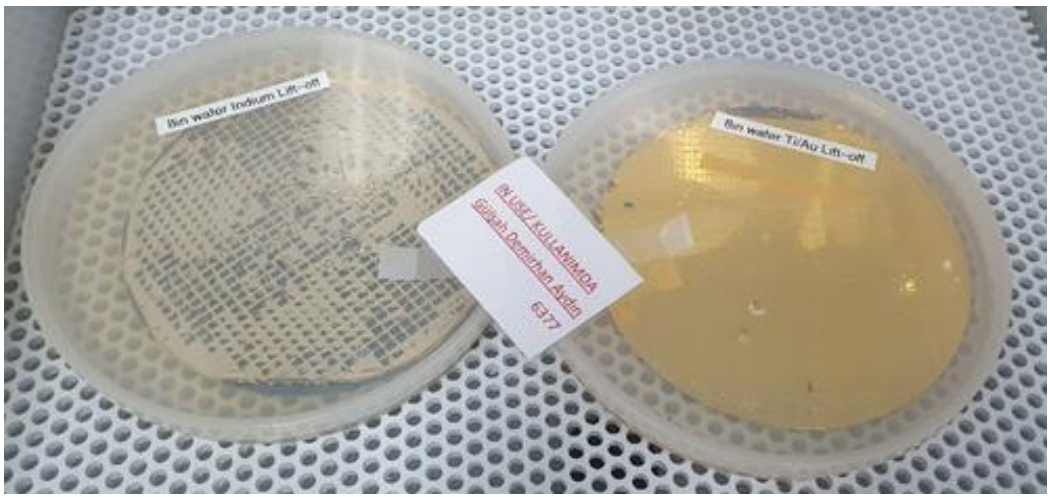
Wafer Handling System of NVTH-500

Figure 3.13. The picture of Nanovak NVTH-500 Thermal Evaporation System used in METU MEMS Center.

After the metal deposition, the fourth step is metal patterning with the lift-off method in which the metal on PR was stripped in acetone (Figure 3.14) whereas the metal layers in the PR openings is leaving on the wafers. The process steps for the lift-off can be listed as: soaking wafers in acetone for at least 6 hours, spraying with syringe, ultrasonic cleaning with buzzer, 1 min in acetone + 1min IPA cleaning and drying the wafers.



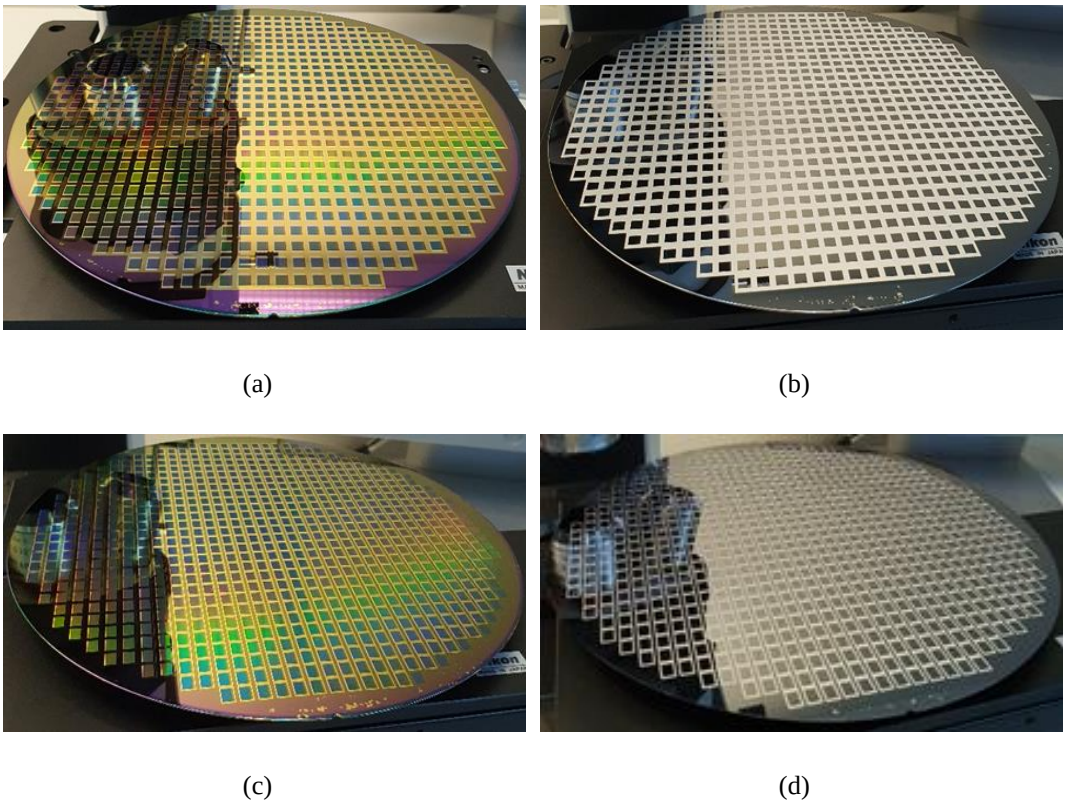
(a)



(b)

Figure 3.14. The pictures of Au coated Wafer A and In coated Wafer B (a) while soaking wafers in acetone for at least 6 hours and (b) at the end of the 6 hours wafers are ready for ultrasonic cleaning.

At the end of lift-off process, wafers are ready for Au-In TLP bonding (Figure 3.15).



(a) (b)

(c) (d)

Figure 3.15. The pictures showing wafers after lift-off process: (a) Wafer A full metal case (c) Wafer A bond ring case and (b) Wafer B full metal case (d) Wafer B bond ring case. Notice that wafers are ready for Au-In TLP bonding process.

The fifth step is Au-In TLP bonding but before the Au-In TLP bonding process bonding force calculation is necessary for performing correct bonding force. The calculation of bonding force is based on the design parameters and proposed cap wafer process mask set is designed using the L-Edit design software. In proposed design there are two cases for bond metal area calculation as shown in Figure 3.18 one is full metal case which is called Bond Met 1 case and second is bond ring case which is called Bond Met 2. One die area of the cap wafer suitable with Wafer C is calculated according to dimensions as shown in Equation 3.1:

$$Die\ Area = 5.41mm * 6.48mm = 35.06mm^2 \qquad (3.1)$$

Bond metal area for one die for bond met 1 case is calculated via L-Edit design software as 21.5144mm^2. There are totally 772 dies so total area could be calculated as in Equation 3.2:

$$Total\ Area = 772 * 21.5144mm^2 = 16609.12mm^2$$

$$3MPa = \frac{Bonding\ Force}{Total\ Area} = \frac{Bonding\ Force}{16609.12mm^2}$$

$$Bonding\ Force\ Bond\ Met\ 1 = F = 49827.35\ Newton\ \cong 49.83\ kN \qquad (3.2)$$

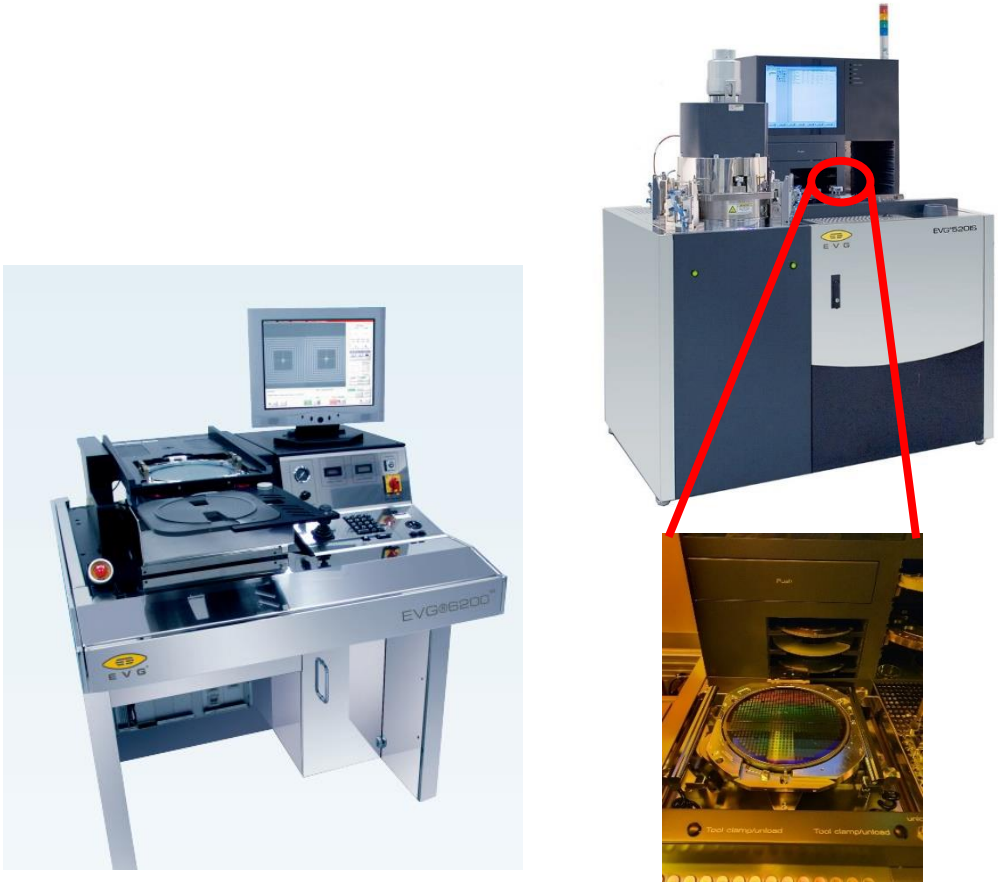
Similarly, bond metal area for one die for bond met 2 case is calculated via L-Edit design software as 9.288mm^2. There are totally 772 dies so total area could be calculated as in Equation 3.3:

$$Total\ Area = 772 * 9.288mm^2 = 7170.336mm^2$$

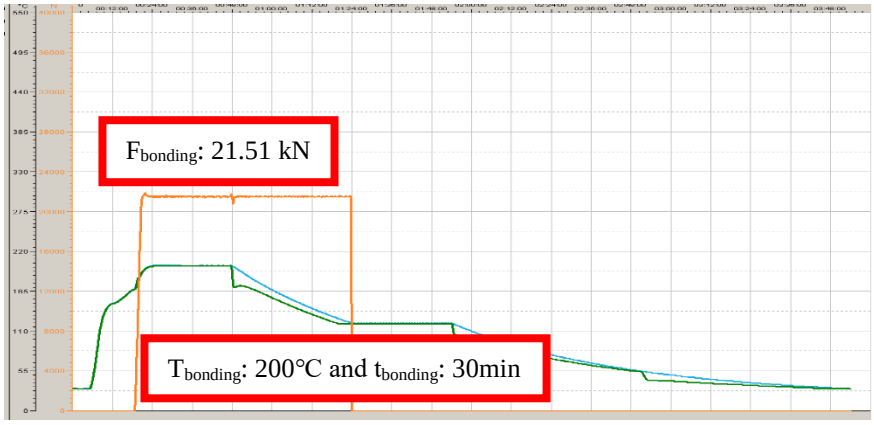
$$3MPa = \frac{Bonding\ Force}{Total\ Area} = \frac{Bonding\ Force}{7170.336mm^2}$$

$$Bonding\ Force\ Bond\ Met\ 2 = F = 21511.01\ Newton\ \cong 21.51\ kN \qquad (3.3)$$

After the bonding force calculation, the prepared Wafer A and Wafer B type wafers were aligned with each other using the EVG 6200 Bond Alignment System and aligned Wafer A+B stack were placed into the bond chamber and bonding recipe was started with the optimized force, temperature, ramp rate and process environment parameters. Notice that initially bonding process started at room temperature and first heating is applied in atmosphere by applying forming gas (5% H_2 and 95% N_2). The performed TLP bonding recipe is "AuIn_TLP_200C_0835AB_M2M2_version2" and bonding conditions are as the following: Applied Force=21510N, Ramp Rate=12000N/min and Bonding Temperature=200ºC. EVG 6200 Bond Alignment and EVG 520IS Wafer Bonder Systems used in METU MEMS Center also sample bonding profile could be seen in Figure 3.16.



(a) (b)



(c)

Figure 3.16. The pictures of (a) EVG 6200 Bond Alignment; (b) EVG 520IS Wafer Bonder Systems used in METU MEMS Center; and (c) example TLP bonding profile.

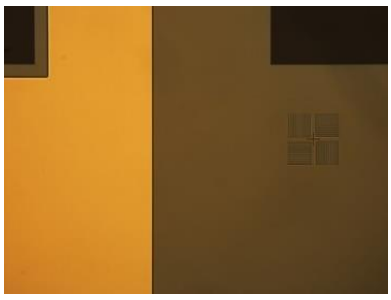
3.1.3 Characterization and Experimental Analysis Results for Au-In TLP Bonded Wafers

After performing successful lift-off process the metal layers have been characterized in terms of structural, chemical, and thermal properties. Similarly, after performing Au-In TLP bonding, the bonded wafer stack has been analyzed for characterization purposes. Under this heading structural and morphological investigation, elemental analysis, thermal analysis, and mechanical characterization details given below subtitles one by one. Notice that this characterization and experimental analysis is necessary for continuing the process in terms of cap cavity formation and glass frit bonding steps.

3.1.3.1 Optic Microscope Inspections

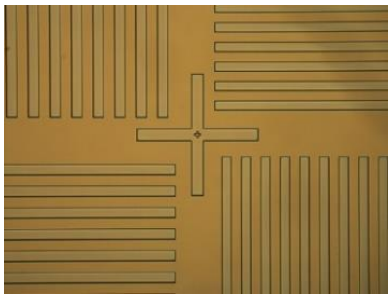
Optic Microscope (OM) investigations are necessary for structural and morphological characterizations. Figure 3.17 shows the Optical Microscope investigations for W_A after lift- off process completed wafers and similarly Figure 3.18 shows the optic microscope details for W_B.

(a)

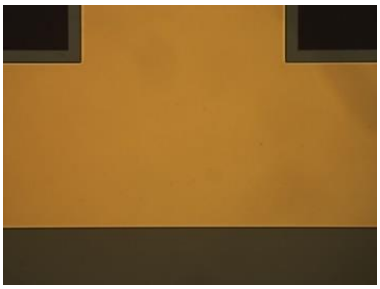


(b)

(c)

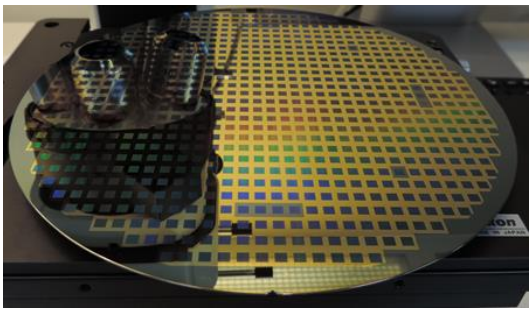


(d)



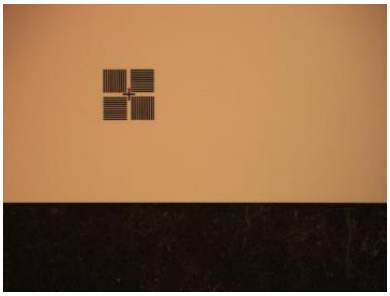
(e)

(f)



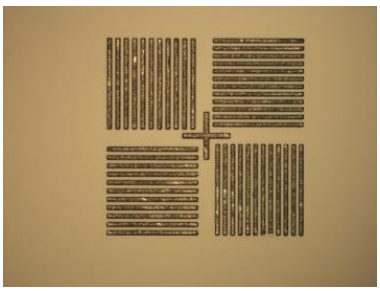
(g)

Figure 3.17. The Optical Microscope investigations for W_A after lift- off process completed wafers are cleaned and dried. (a-f) Closure view of the dies and alignment marks; (g)Wafer level image.



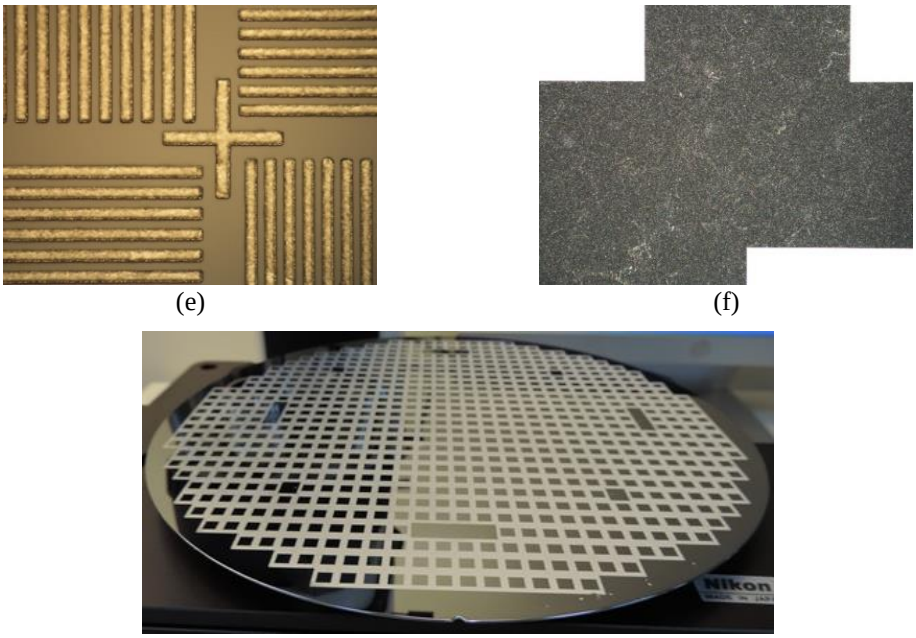
(a)

(b)



(c)

(d)



(e) (f)

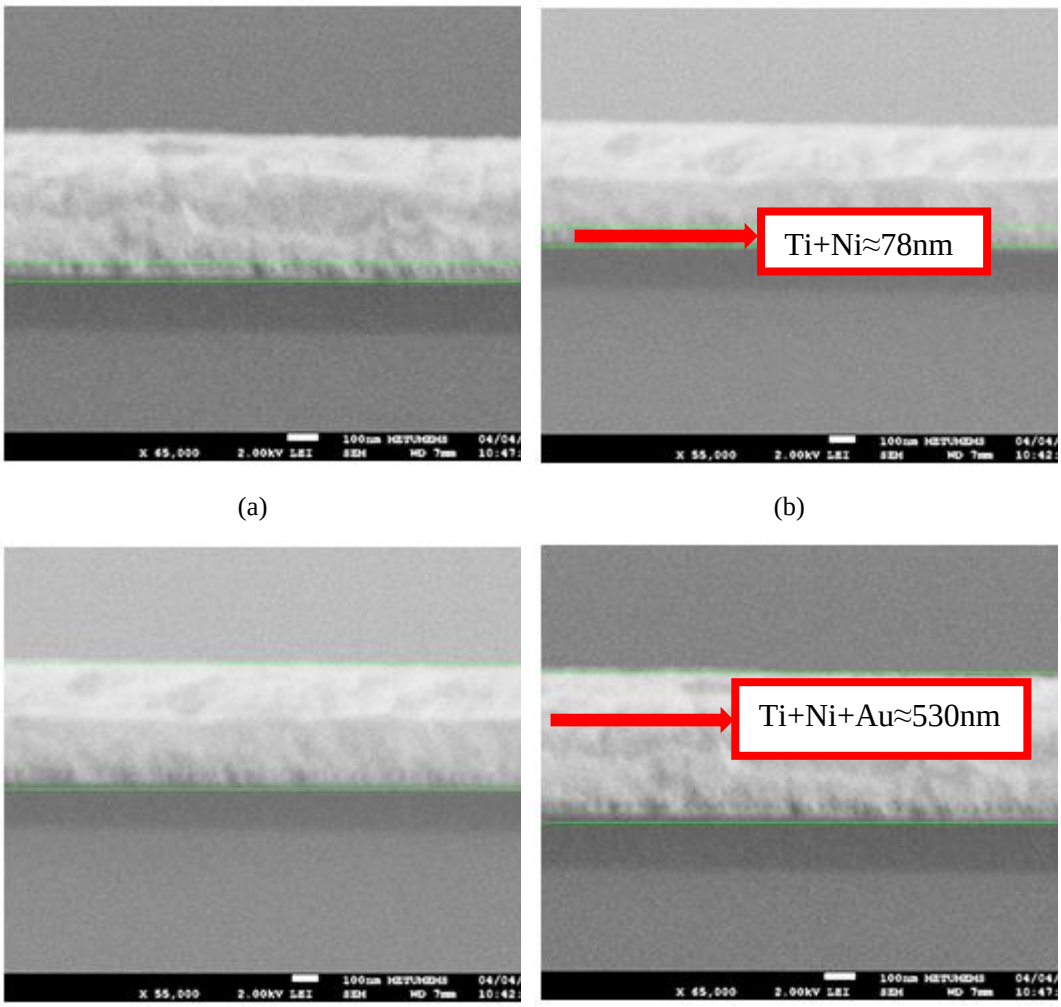
(g)

Figure 3.18. The Optical Microscope investigations for W_B after lift- off process completed wafers are cleaned and dried. (a-f) Closure view of the dies and alignment marks; (g)Wafer level image.

After optic microscope analyses it is verified that lift-off applied wafers are structurally and morphologically ready for Au-In TLP bonding.

3.1.3.2 SEM, EDS and Profilometer Inspections

To be ready for Au-In TLP bonding, in metal deposition part thickness optimization is required so structural and morphological characterizations and inspections of thin films are measured with Hitachi Regulus 8230 scanning electron microscopes (SEM). Also, for the verification of those thicknesses Veeco NT1000 Optical Surface Profiler (OSP) and Veeco Dektak8 Stylus Profilometer is used. The optimized metal thicknesses for sample representation for Wafer B up to In coating can be seen in Figure 3.19.



(a) (b)

(c) (d)

Figure 3.19. The SEM analysis for W_B pieces just after Ti/Ni/Au coating in BESTEC-2 systems. (a)-(b) The titanium and nickel thickness are approximately 78nm; (c) – (d) The titanium, nickel and gold thickness are approximately 530nm.

After SEM analyzes for the verification of those thicknesses Veeco Dektak8 Stylus Profilometer is also used and for Wafer A case metal thickness from the center is measured as 1.1 µm; similarly, for Wafer B case metal thickness from the center is measured as 3.6 µm.

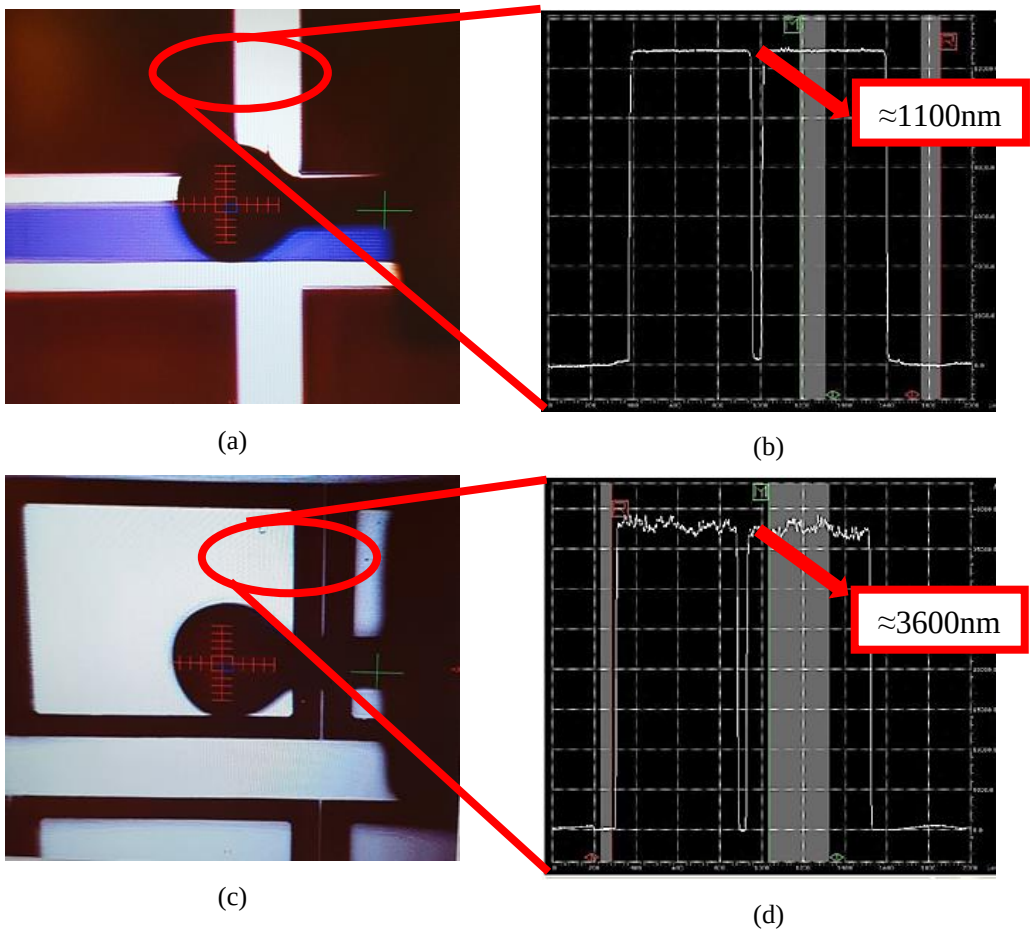
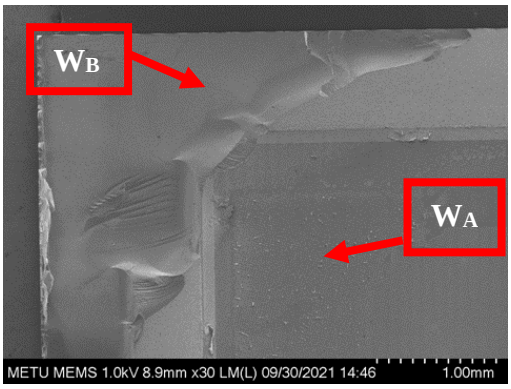
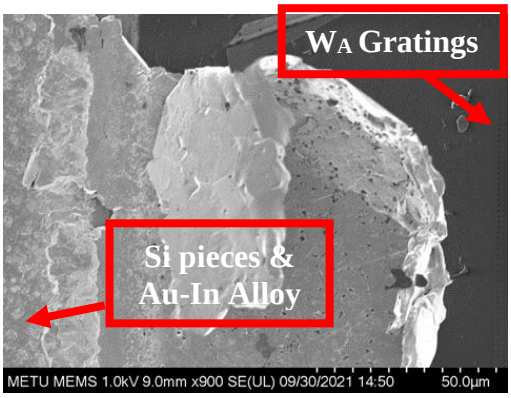


Figure 3.20. The metal thickness analysis in Veeco Dektak8 Stylus Profilometer. (a)-(b) The W_A Dektak camera view and profilometer analysis results as can be seen the titanium, nickel and gold thickness are approximately 1100nm; (c)-(d) The W_B Dektak camera view and profilometer analysis results as can be seen the titanium, nickel, gold and indium thickness are approximately 3600nm.

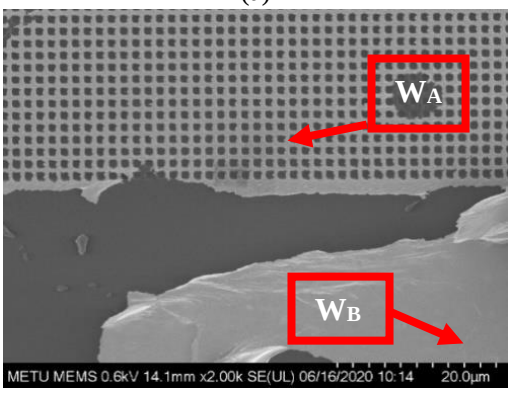
After being sure metal layers are characterized as wanted thicknesses, elemental analysis of the thin films has been performed with energy-dispersive X-ray spectroscopy (EDS) after dicing Au-In TLP bonded stack and applying destructive shear tests. Notice that although destructive shear test details will be given in the sub heading of "3.1.3.4 Destructive Shear Tests" SEM images of the analyzed broken dies could be seen in Figure 3.21.


WB
WA
METU MEMS 1.0kV 8.9mm x30 LM(L) 09/30/2021 14:46 1.00mm

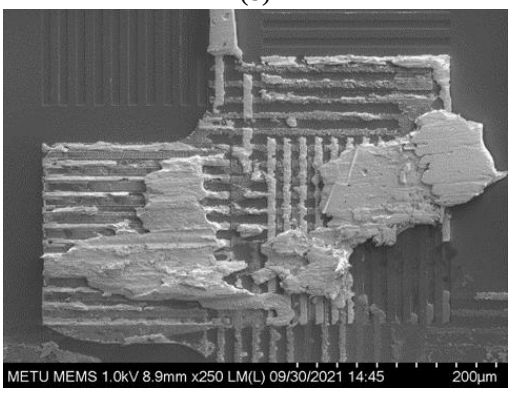
(a)


WA Gratings
Si pieces &
Au-In Alloy
METU MEMS 1.0kV 9.0mm x900 SE(UL) 09/30/2021 14:50 50.0µm

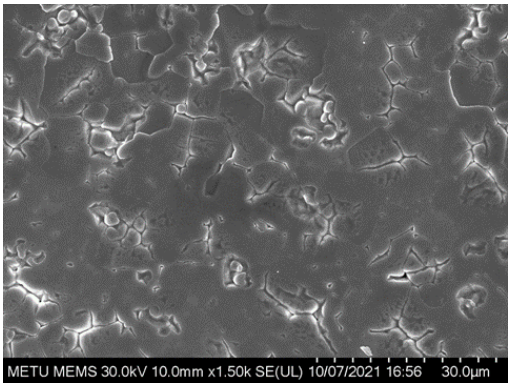
(b)


WA
WB
METU MEMS 0.6kV 14.1mm x2.00k SE(UL) 06/16/2020 10:14 20.0µm

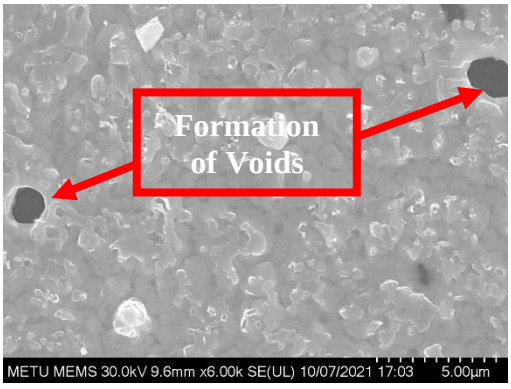
(c)


METU MEMS 1.0kV 8.9mm x250 LM(L) 09/30/2021 14:45 200µm

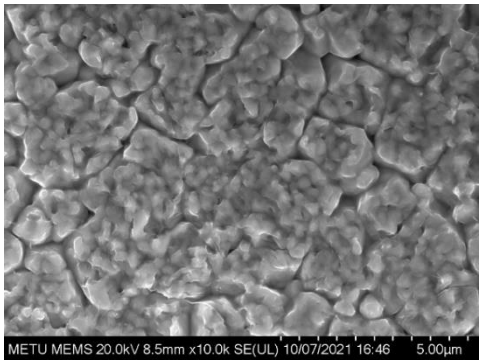
(d)


METU MEMS 30.0kV 10.0mm x1.50k SE(UL) 10/07/2021 16:56 30.0µm

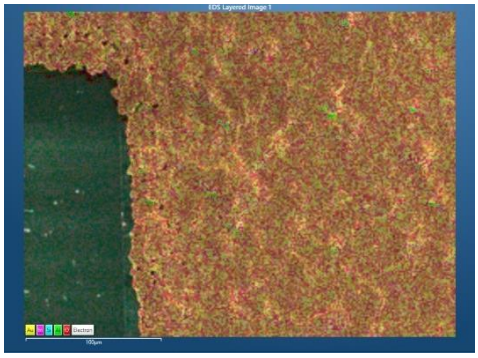
(e)


Formation
of Voids
METU MEMS 30.0kV 9.6mm x6.00k SE(UL) 10/07/2021 17:03 5.00µm

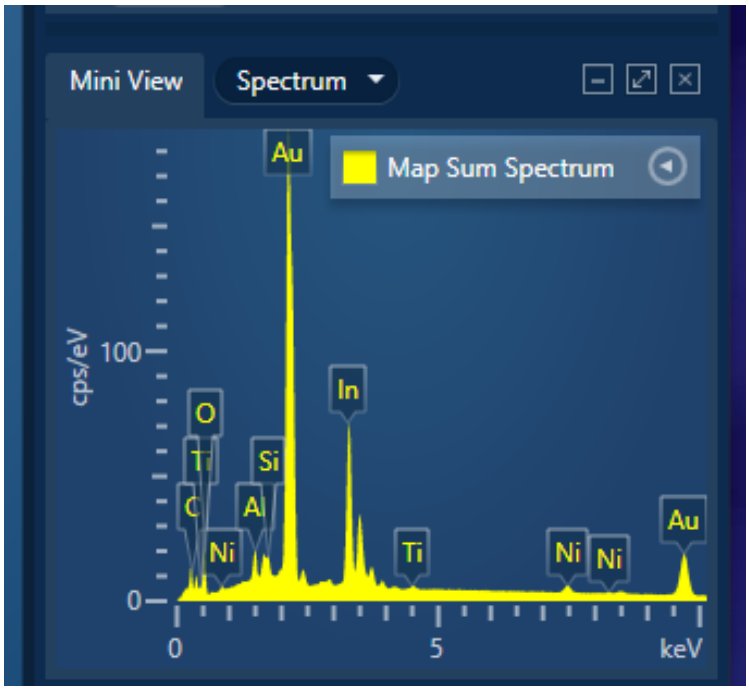
(f)


METU MEMS 20.0kV 8.5mm x10.0k SE(UL) 10/07/2021 16:46 5.00µm

(g)



(h)



(i)

Figure 3.21. The images of the Au-In TLP bonded stack diced and shear test applied case: (a-g) the SEM analyze results from the broken pieces; (h) – (i) EDS analyze results from the broken pieces' Au-In alloy part it seems bonding quality is good and all the elements (Si-Ti-Ni-Au-In-O_2) are seen in the EDS analysis results.

After investigating the cross-sectional view in detail in Figure 3.22, the side views could be found in the Figure 3.21. As can be seen, the bonding quality is satisfied because the bonded stack is not easily separated from each other, and Wafer A pieces is on Wafer B or vice versa (Figure 3.21 a-d). Besides, the SEM analyze results from the Wafer B indium side diced and shear test applied broken pieces it seems bonding quality is good, and due to volume shrinkage void formations are observed (Figure 3.21 f). As can be seen in EDS analysis (Figure 3.21 g-i) all the elements (Si-Ti-Ni-Au-In-O_2) are seen. To conclude, after SEM and EDS analyses it is verified that Au- In TLP bonded wafers are structurally and morphologically ready for SAM inspections.

3.1.3.3 SAM Inspections

After the Au-In TLP bonding experiments, the bonded 8” size wafer stacks are tested with PVA TePLA SAM 301 HD^2 scanning acoustic microscope system (SAM)’s C- SAM imaging mode. The surface acoustic microscopy enables non-destructive investigation of the bond interface utilizing scanning of the sample by acoustic waves inside the deionized water (DIW) as can be seen in Figure 3.22. The C- SAM working principle is like that; it takes an image from inside the device using sound waves and detects whether it is a cavity/space or a different material or defect/crack etc. according to the reflection, scattering, or absorption. The minimum resolution with 200 MHz transducers is approximately 10-20 µm.

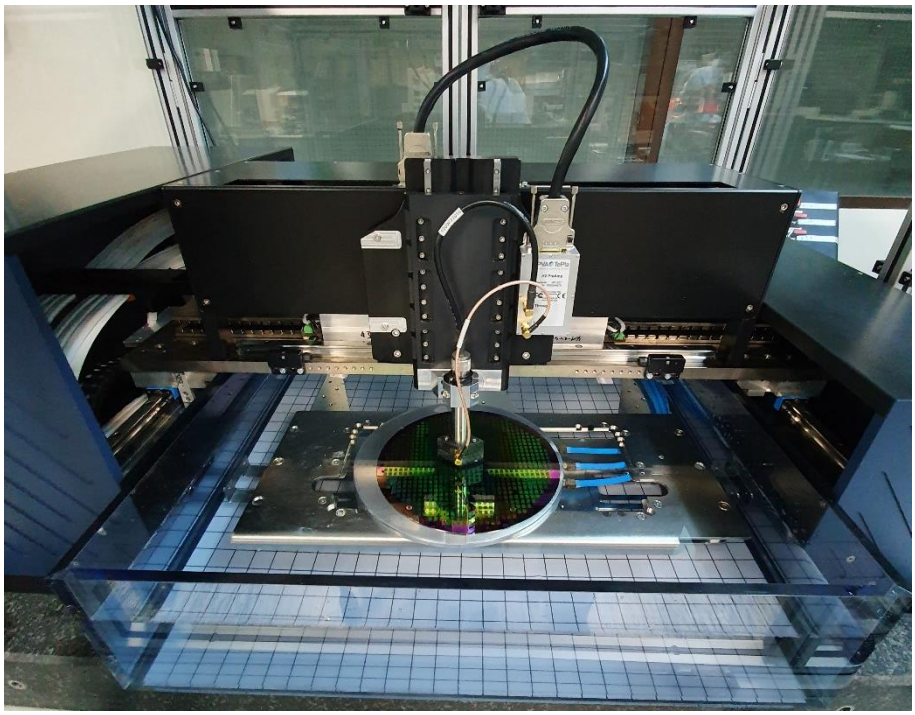


Figure 3.22. The PVA TePLA SAM 301 HD^2 scanning acoustic microscope setup and the Au-In TLP bonded Wafer A+B stack on it.

The bonding pressure is the most important parameter to obtain a strong and reliable bond formation. SAM characterization is necessary for the determination of the bonding force because some metals squeezed out to the dies and this situation is

unwanted case for decreasing the transmissivity of the packaged sensors. The bonding force should not only satisfy the optimum material contact while providing a minimum amount of liquid loss caused by the squeeze-out but also strong enough mechanically for hermeticity and leakage protection. In the scope of the thesis, in first Au-In bonding trials applied bonding force was 21.51 kN but after SAM inspections to eliminate the In squeeze out to the dies force is 15% decreased and new bonding force is 18.3 kN and to find the optimum bonding force experiments continued and in 15.5 kN Au-In TLP bonding force is optimized and uniformity is satisfactory as can be seen in Figure 3.23.

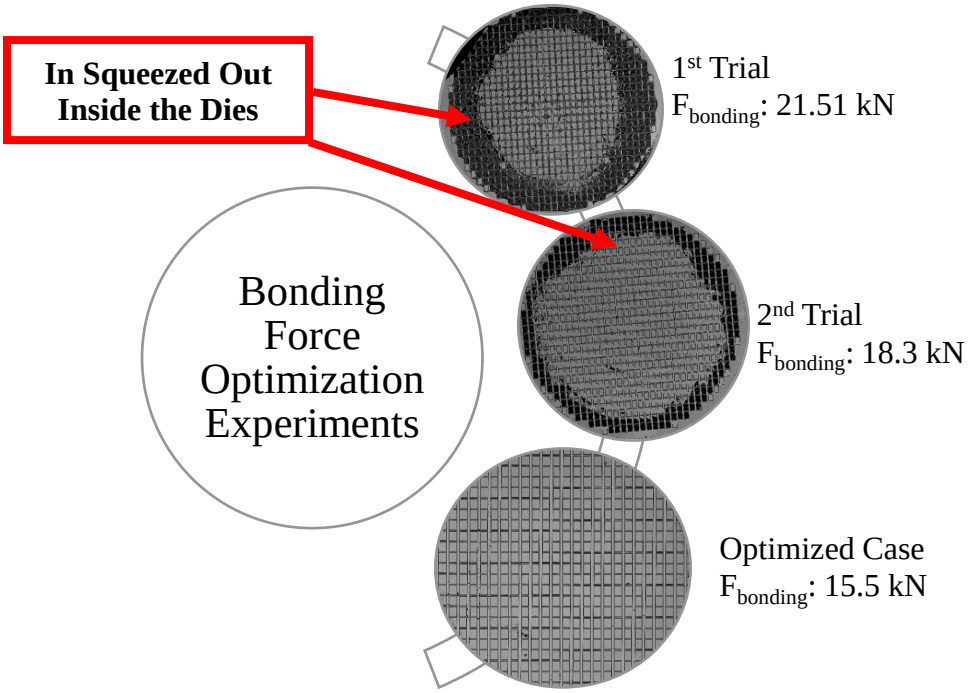


Figure 3.23. The surface acoustic microscope analysis results for offered wafer level packaging method. Notice that in the first trial outer dark circular side means In squeezed out into the dies and it is optimized and uniformity is satisfactory in the final case.

Figure 3.24 shows the optimized case SAM image of the Au-In TLP bonded Wafer A+B stack. In the Figure 3.24, the dark colors refer to continuous penetration of ultrasound waves. The bond-ring regions are in dark gray color, which refers to

continuous material structure in the bond-ring region. The leaked water in the streets between dies can be seen in the image as a light gray color and finally the other light side means gratings and unbonded parts.

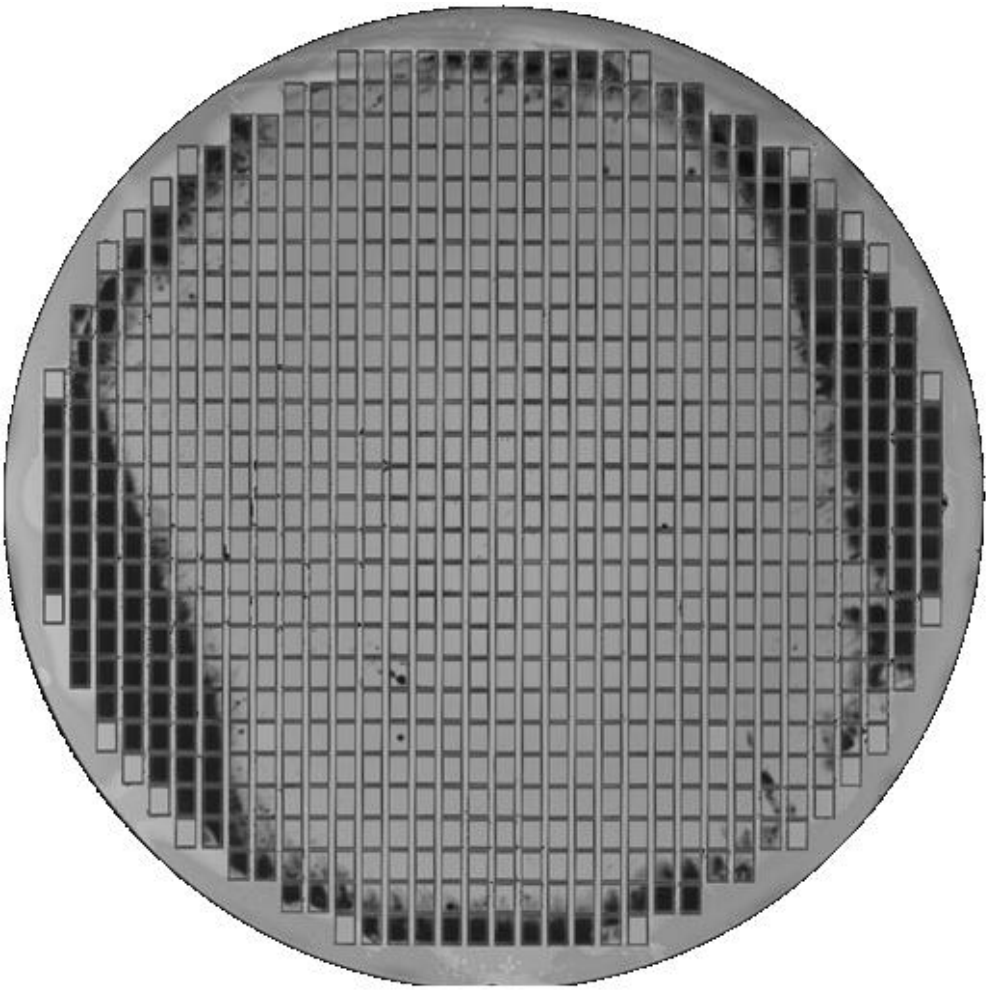


Figure 3.24. The surface acoustic microscope results for wafer level optimized case as can be seen all sides are uniform and there is no In squeezed out problem.

The SAM image has showed some defected regions which may have resulted during the microfabrication process or handling. There are some squeezed-out In metals around the bond rings and outer circular part of the 8” wafer refers to the liquid metal that had been obtained during the bonding process.

3.1.3.4 Destructive Shear Tests

After the structural inspection steps for mechanical inspection the prepared wafers are diced in DISCO, DAD3350 Automatic Dicing Saw machine. After dicing the wafer stack for analyzing Au/In TLP bonding quality of the dies DAGE Nordson 4000 Bond Tester is used as illustrated in Figure 3.25. Shear tests are one of the destructive testing methods for measuring the ability to resist creep under a constant load, applied parallel to the surface of the substrate. The main purpose of this destructive method is to compare the performance of an adhesive in a joint and to determine its mechanical response. According to military standard MIL-STD 883 [71] the minimum shear strength value is 6 MPa for the microelectronic packages. The shear strength of the bonds was tested in the following conditions: die level; using 20 µm/sec travel speed; and using the maximum load 1000 N.

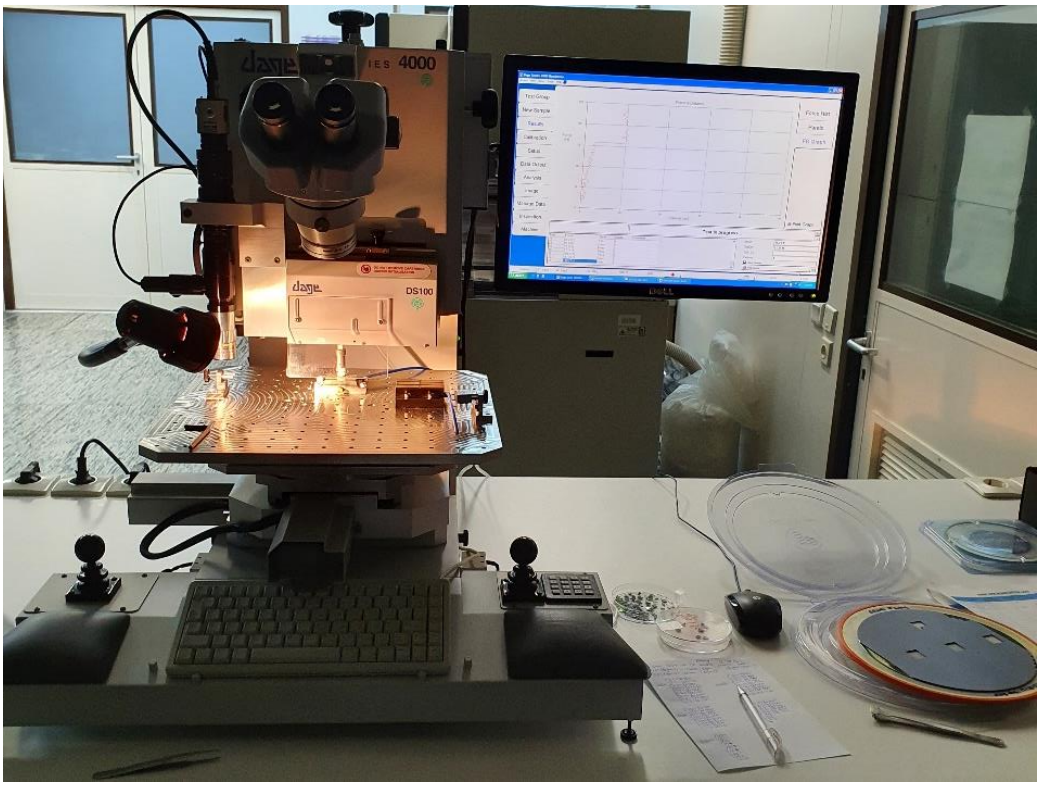


Figure 3.25. The DAGE Nordson 4000 Bond Tester setup and the Au-In TLP bonded and diced Wafer A+B dies on it.

Under the destructive shear tests heading not only the reliability of the dies after nearly one year but also after annealing experiments are analyzed and tested regions from the wafers could be seen in Figure 3.26.

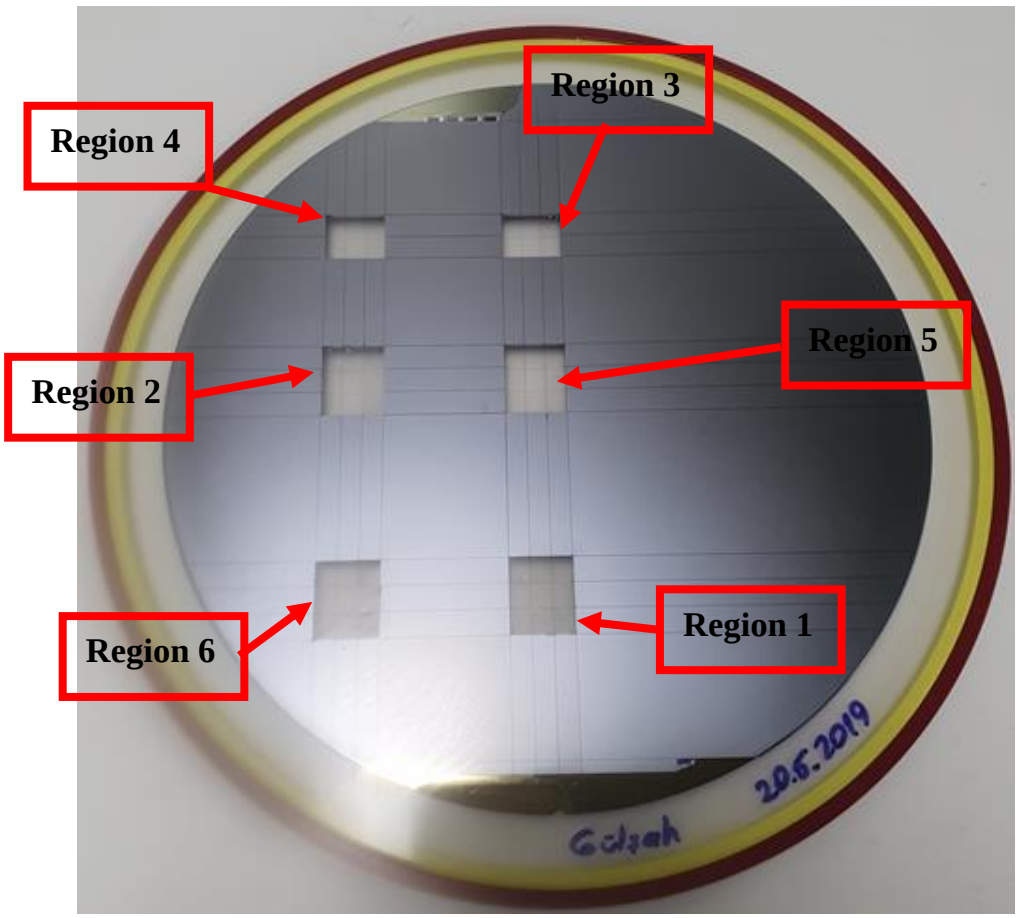


Figure 3.26. The image showing one of the diced wafers and shear test applied regions to analyze Au/In TLP bonding quality after a year and annealing experiments.

3.1.3.4.1 Room Temperature Destructive Shear Tests for Reliability and Repeatability Check After a Year:

For the mechanical characterization purposes three different bonded stacks are analyzed with the same bonding parameters and all results are similar so just one of them is integrated to thesis. Approximately one year later reliability and repeatability

results are obtained as the following shown in Figure 3.27. Notice that from die name s1.3 to s3.6 (including Regions 1, 2, and 3) results are obtained at 21.05.2019 and from die name s4.2 to s6.9 (including Regions 4, 5, and 6) results are obtained at 21.04.2020. In test date of 21.05.2019 average shear strength is measured as 32.10±5.29 MPa for approximately 21.52 mm^2 single die area. Similarly, approximately a year later, in test date of 21.04.2020 average shear strength is measured as 29.61±2.31 MPa for approximately 21.52 mm^2 single die area.

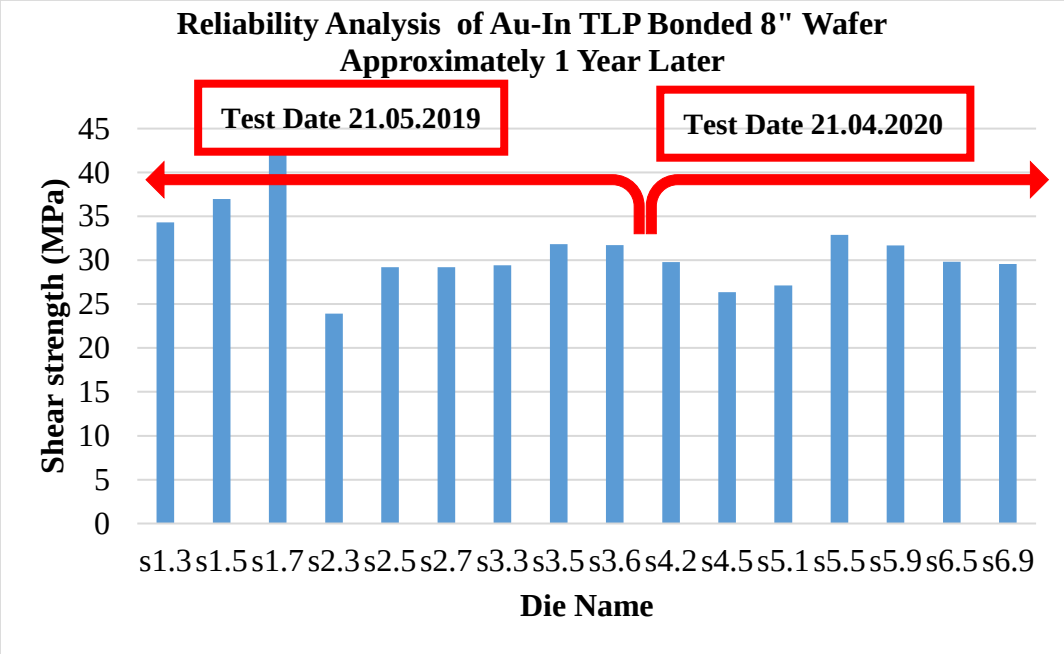


Figure 3.27. The reliability analysis approximately one year later. Notice that from s1.3 to s3.6 results are obtained at 21.05.2019 and from s4.2 to s6.9 results are obtained at 21.04.2020. Notice that for a single die, bonded area is calculated as 21.52 mm^2.

As can be seen from the Figure 3.27 shear test results, Au-In TLP bonding is one of the strongest bonding type and shear test results seem good for a single die bonding area of 21.52 mm^2 even after a year later. During the tests, some dies are failed, or weak results are obtained due to the lack of poor bonding caused by voids or dust and it is possible to conclude that after a year TLP bonding remains strong; so, this

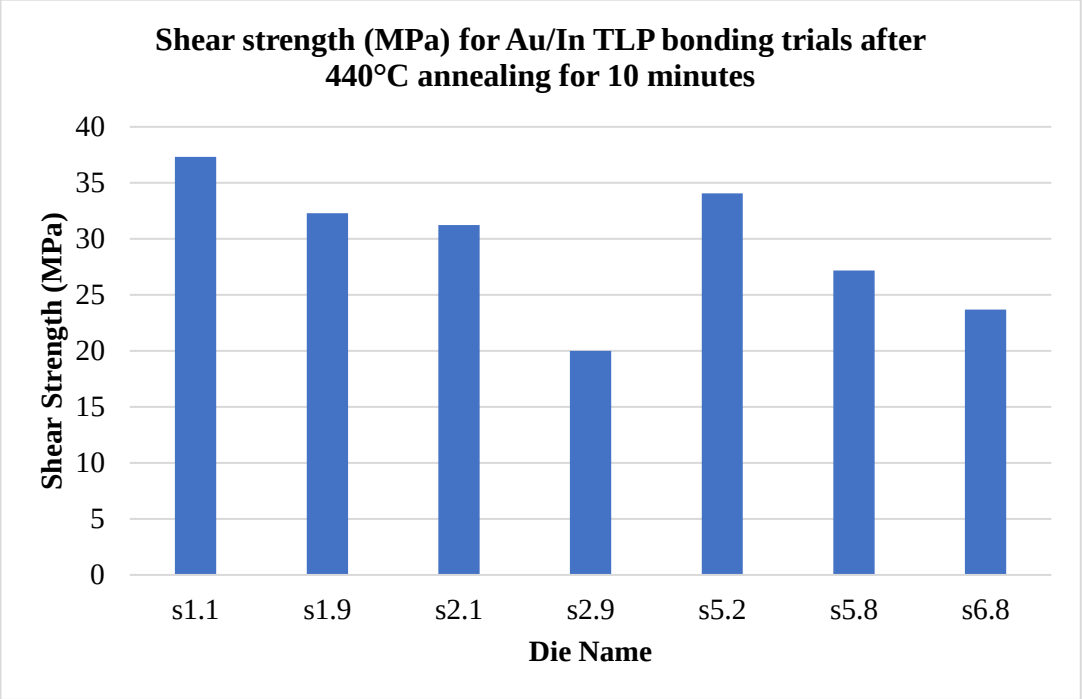
bonding type can be concluded reliable and repeatable. Overall, Table 3.1 summarizes all the results.

Table 3.1 The tabulated form of the shear test results for reliability and repeatability characterization performed at DAGE Nordson 4000 Bond Tester available in METU MEMS Center.

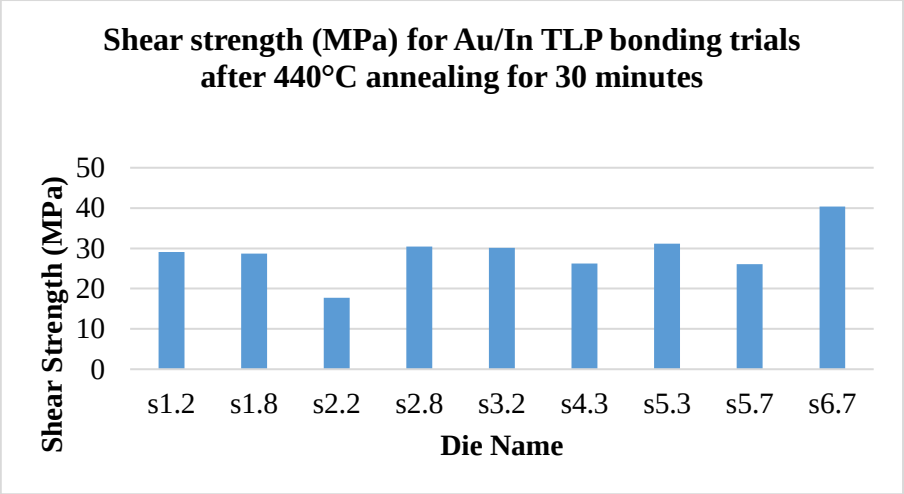
Test Date	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)	Annealing Situation
190521	**s1.3**	738.30	34.32	Not annealed tested just after bonding. SAM analyzes and dicing
	s1.5	795.43	36.97	
	s1.7	910.21	42.31	
	s2.3	514.79	23.93	
	s2.5	628.16	29.20	
	s2.7	628.02	29.19	
	s3.3	632.84	29.41	
	s3.5	684.73	31.83	
	s3.6	682.31	31.71	
200421	**s4.2**	640.55	29.77	Not annealed tested nearly 1 year later to understand reliability of the packaging
	s4.5	567.22	26.36	
	s4.6	Fail	Fail	
	s5.1	583.57	27.12	
	s5.5	707.54	32.89	
	s5.9	681.70	31.69	
	s6.5	641.68	29.83	
	s6.9	636.20	29.57	

3.1.3.4.2 Destructive 21.04.2020 Shear Test Results for same Au-In TLP Bonded Dummy Wafer After 440°C Annealing for 10, 30 and 60 minutes:

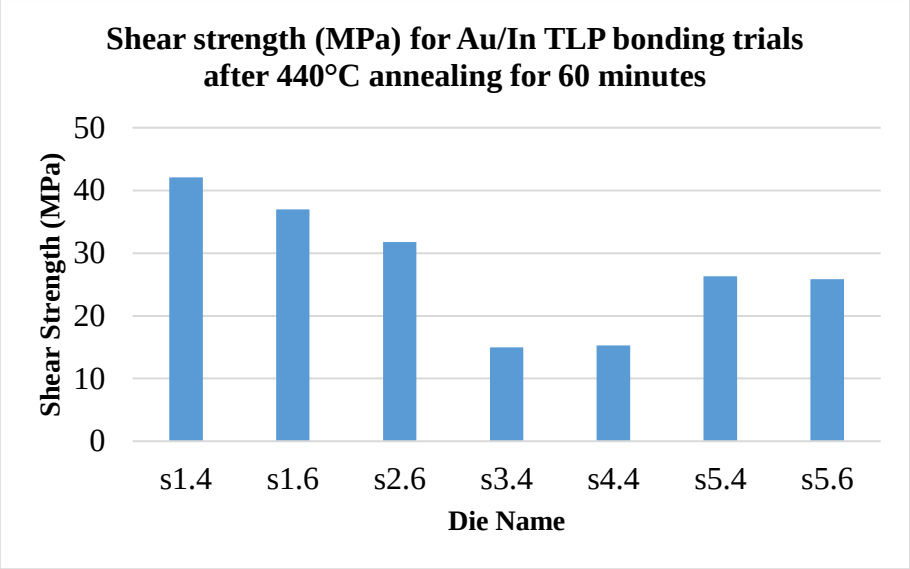
In this subsection again for the mechanical characterization and checking the reliability of the packages approximately one year later diced dies are annealed for checking the thermal cycling (RT to 250℃) for 5 cycles, high temperature storage (300℃ for a day), and high temperature annealing to check robustness during both getter activation and glass frit bonding. For annealing experiments, three different test groups are decided which are annealing at 440°C for 10 minutes, 440°C for 30 minutes and 440°C for 60 minutes. After annealing experiments, the destructive shear tests are applied, and their results are shared (Figure 3.28). Notice that the annealing steps was performed for 440°C because the second branch of the proposed study is screen-printing glass paste to the cavity opened cap wafer for glass frit bonding of vacuum sensors or bolometer designs; and glass frit bonding and getter activation is going to be performed at the temperature of 440°C.



(a)



(b)



(c)

Figure 3.28. The applied shear tests to analyze Au/In TLP bonding quality after nearly one year later and after annealing at 440°C annealing for: (a) 10 minutes, (b) 30 minutes, (c) 60 minutes. Notice that for a single die, bonded area is calculated as 21.52 mm^2.

All annealing experiments performed, and shear tests applied to them in test date of 21.04.2020. The average shear strength is measured as 26.41±10.14 MPa for approximately 21.52 mm^2 single die area after 10 minutes annealing at 440°C. After 30 minutes annealing, the average shear strength is measured as 28.90±5.91 MPa. Finally, for 60 minutes annealing case, the average shear strength is measured as

27.61±10.25 MPa. For comparison purposes before and after annealing shear test results are plotted in a same graph in Figure 3.29. Notice that obtained shear strength results are the average ones in each region.

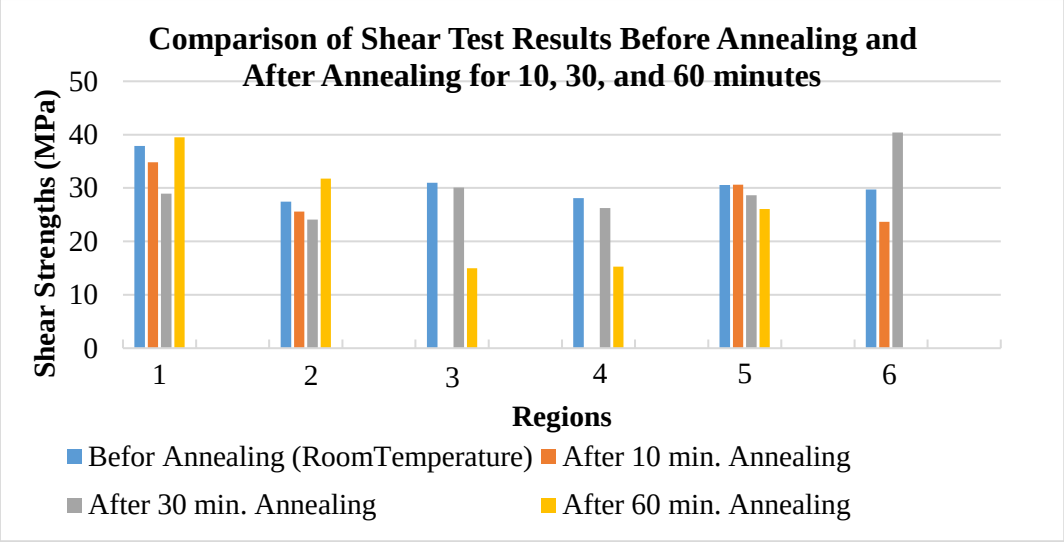


Figure 3.29. The comparison of shear test results of 6 regions in terms of before-after annealing for 10, 30, and 60 minutes. Notice that blue color for before annealing, orange color for annealing at 430°C for 10 minutes, gray color for annealing at 440°C for 30 minutes and yellow color for annealing at 430°C for 60 minutes.

As can be seen from the Figure 3.29 shear test results, even after one year later and thermal annealing, Au-In TLP bonding is one of the strongest bonding type and shear test results seem good for a single die bonding area of 21.52 mm^2. Besides, in all regions, MIL-STD 883 which is the microelectronic packages minimum shear strength must have a minimum of 6 MPa criteria is satisfied. During the tests, some dies are failed, or weak results are obtained due to the lack of poor bonding caused by voids or dust and it is possible to conclude that after a year TLP bonding remains strong; so, this bonding type can be concluded reliable and repeatable and satisfactory as a first branch of the cap wafer study. Overall, Table 3.2 summarizes all the results.

Table 3.2 The tabulated form of the shear test results after annealing for mechanical characterization.

Test Date	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)	Annealing Situation
200421	**s1.1**	802.68	37.31	Annealed at 440°C for 10 minutes
	s1.9	694.48	32.28	
	s2.1	671.82	31.23	
	s2.9	430.13	19.99	
	s3.1	Fail	Fail	
	s4.1	119.00	5.53/Fail	
	s5.2	732.57	34.05	
	s5.8	584.75	27.18	
	s6.8	509.77	23.69	
200421	**s1.2**	626.69	29.13	Annealed at 440°C for 30 minutes
	s1.8	618.14	28.73	
	s2.2	382.04	17.76	
	s2.8	654.81	30.44	
	s3.2	647.57	30.10	
	s4.3	565.11	26.27	
	s5.3	671.09	31.19	
	s5.7	561.55	26.10	
	s6.7	869.04	40.39	
200421	**s1.4**	905.26	42.08	Annealed at 440°C for 60 minutes
	s1.6	795.68	36.98	
	s2.6	683.60	31.77	
	s3.4	322.58	14.99	
	s4.4	329.05	15.29	
	s5.4	565.96	26.31	
	s5.6	556.12	25.85	
	s6.6	Fail	Fail	

To conclude, as can be seen from Tables 3.1 and 3.2, totally 44 dies are shear tested and 4 of them are failed due to the lack of poor bonding caused by voids or dust.

3.2 Thinning the Au-In TLP Bonded Stack or Alternative Thin Wafer Usage for Offered Cap Wafer's Cap Cavity Formation

As it was remembered, in the scope of proposed cap wafer design, after obtaining good bonding and being sure Au-In TLP bonding configuration is a correct choice with characterization and experimental analysis; for cavity opening purposes, the next step is thinning the bonded stack at first grinder then after applying cavity lithography steps etching the wafer in DRIE or using 400µm DSP Wafer (to eliminate the grinding step); so in the following subsections the two cases details are going to be shared.

3.2.1 7AF Strasbaugh Grinder Trials for Thinning Au-In TLP Bonded Wafer Stack:

For thinning the 8" size bonded wafers stack also called wafer back grinding, the removal amount is typically a few hundred microns (in wafer thickness). In the proposed cap wafer design, Wafer A+B stack is going to be grinded from 1450µm to 875µm. That is to say, Wafer B side is going to be grinded from 725µm to 150µm thickness (Figure 3.30).

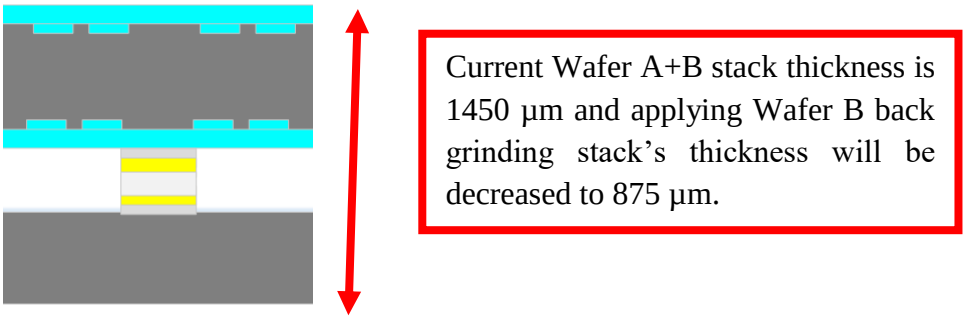


Figure 3.30. The schematic diagram showing the Wafer A+B stacks situation and after back grinding expected thickness.

When literature searched, usually, back grinding is carried out in two major steps which are coarse grinding and fine grinding, respectively. Additionally, Chemical Mechanical Polishing or CMP is also applied in some studies as a final step. Coarse grinding removes silicon faster using coarse grinding wheel with larger diamond abrasives. Unfortunately, the damage induced by coarse grinding is too much and must be removed by a fine grinding step. In fine grinding silicon removal rate is much slower and used diamond particle size is much smaller. Also, fine grinding is used to remove a small amount of silicon (for example, from 10 to 30 μm) [72], [73]. In the offered cap wafer, only coarse and fine grindings are applied to Wafer A+B stacks and for the remaining process steps; which are cavity lithography, DRIE cavity etch, oxide removal, screen printing and getter activation steps; before glass frit bonding that value is acceptable.

In METU MEMS Center, till the proposed cap wafer trials never 8” size chuck installed, and processes done before, so with the help of new superuser and technical personnel 8” size compatible chuck changed as the Work Chuck. Then, several processes with 8” Single Wafer Processes are done. After dummy wafers thinning achieved successfully as a next step Au-In TLP Bonded Wafer A+B Stacks are thinned, and written recipes worked properly (Figure 3.31 and Figure 3.32). During the grinding process the stacks’ thicknesses are thinned from 1450μm to 875μm successfully in written 3 step recipe which are: 1) from 1450μm to 1240μm at 650rpm with 2.0μm/s speed; 2) from 1240μm to 1025μm at 640rpm with 2.0μm/s speed; and 3) from 1025μm to 875μm at 650rpm with 3.0μm/s speed.

Before continuing the 8” size compatible cap wafers’ cavity opening lithography steps one of the grinded Wafer A+B stacks’ front and back side is illustrated in Figure 3.33.

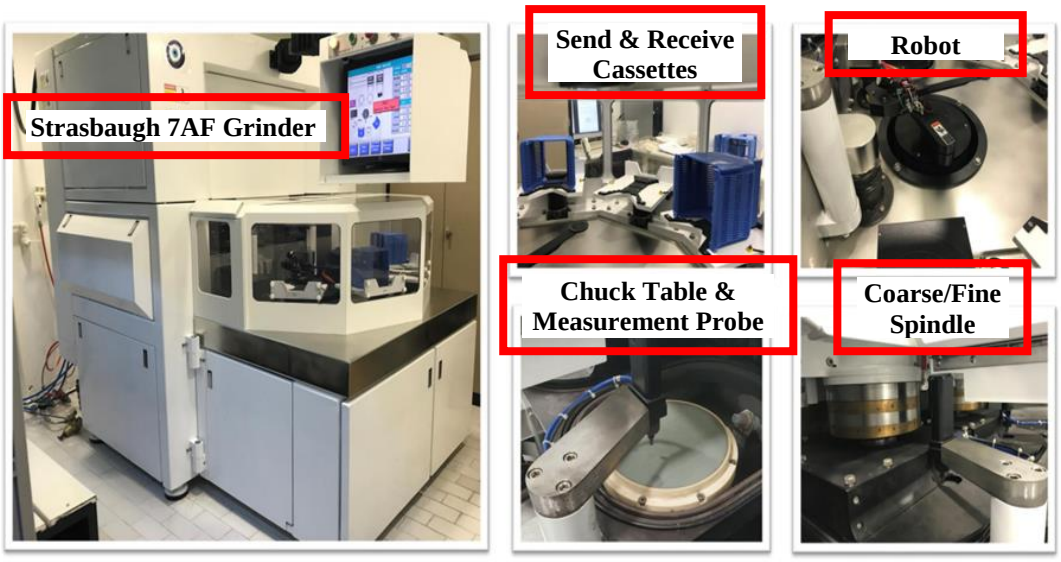


Figure 3.31. 7AF Strasbaugh Grinder System available in METU MEMS Center.

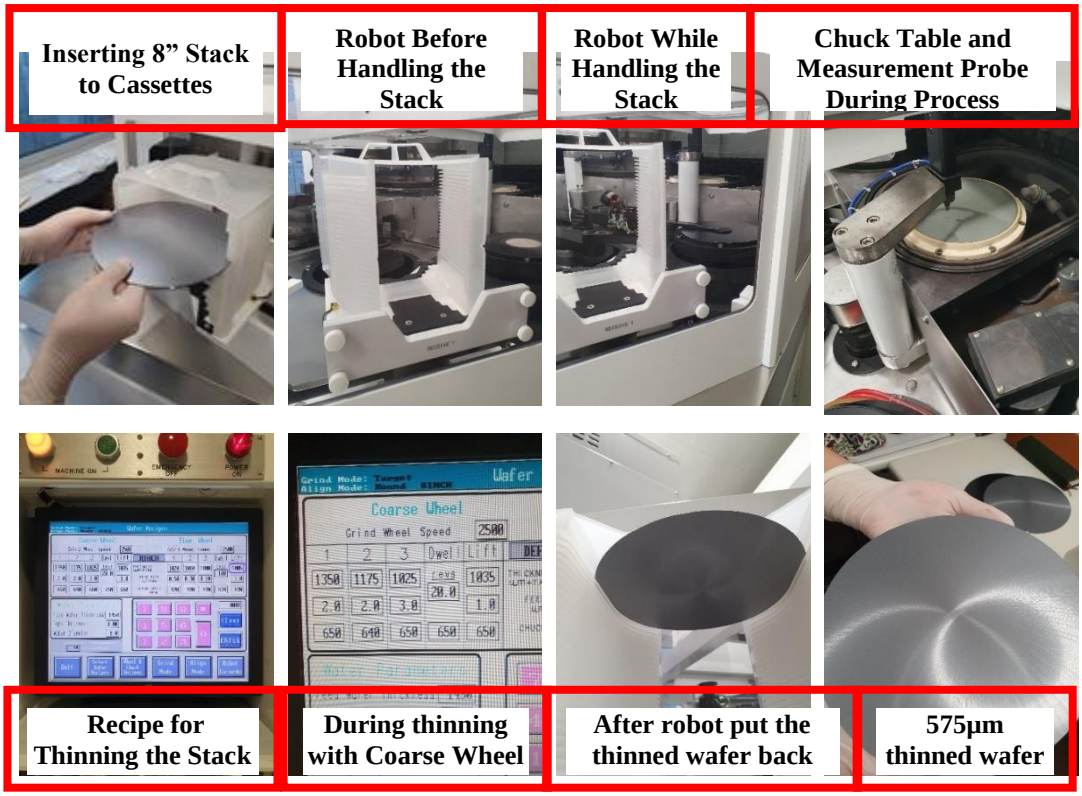


Figure 3.32. 7AF Strasbaugh Grinder System Images and Applied Recipe while thinning my 8” Au-In TLP Bonded Wafer Stack from1450µm to 825µm successfully.

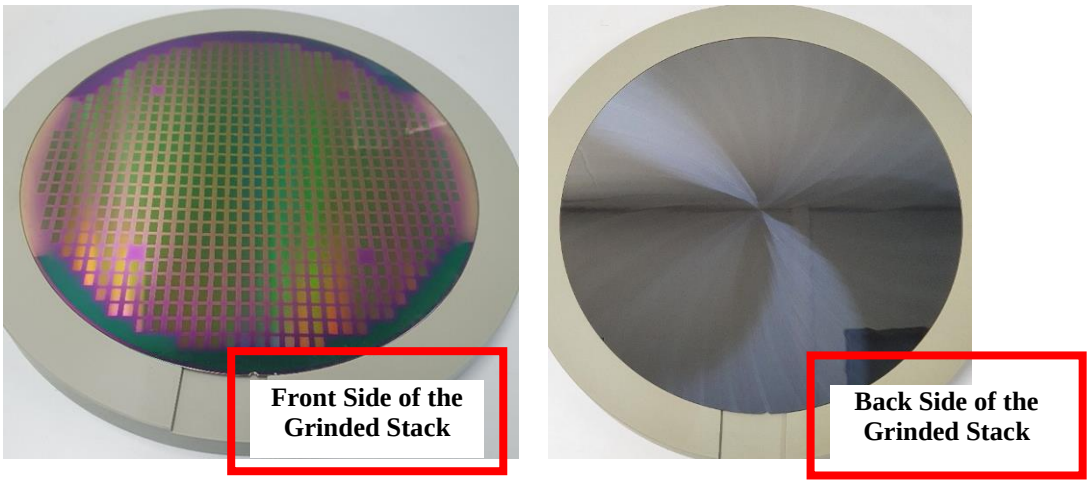


Figure 3.33. The front and back side views of the grinded Wafer A+B stack.

To conclude, grinding of the 8” bonded wafer stacks are tried, and bonded wafer stack thinning process worked properly; so, Wafer B 400 µm case is also going to be tried and optimum case would be selected as a final TLP bonding. Because in 725µm standard wafer grinded stack there is a wafer cleaning issue must be considered although cavity depth is going to be 150µm whereas in thin wafer usage 400µm depth must be etched for cavity openings. After grinding done successfully the next step would be cavity openings in DRIE.

3.2.2 400µm Thin Wafer Usage to Eliminate Grinding Step

As it was remembered, for Wafer B case, to eliminate the grinding step and for obtaining 400µm cavity to integrate grating structures inside; wafer Suppliers for 400µm Thick 8” Si DSP Wafers is searched from the internet and the price quote is wanted for 8” size Si wafers. After the purchasing team’s decision wafers are ordered from WaferPro Company. Compared with standard 725µm thick wafers case, handling and processing is a bit difficult. Figure 3.34 depicts the photos taken during the handling and lithography steps of thin wafers. Before continuing the 8” size compatible cap wafers’ cavity opening lithography steps one of the Wafer A+B stacks’ front and back side is illustrated in Figure 3.35.

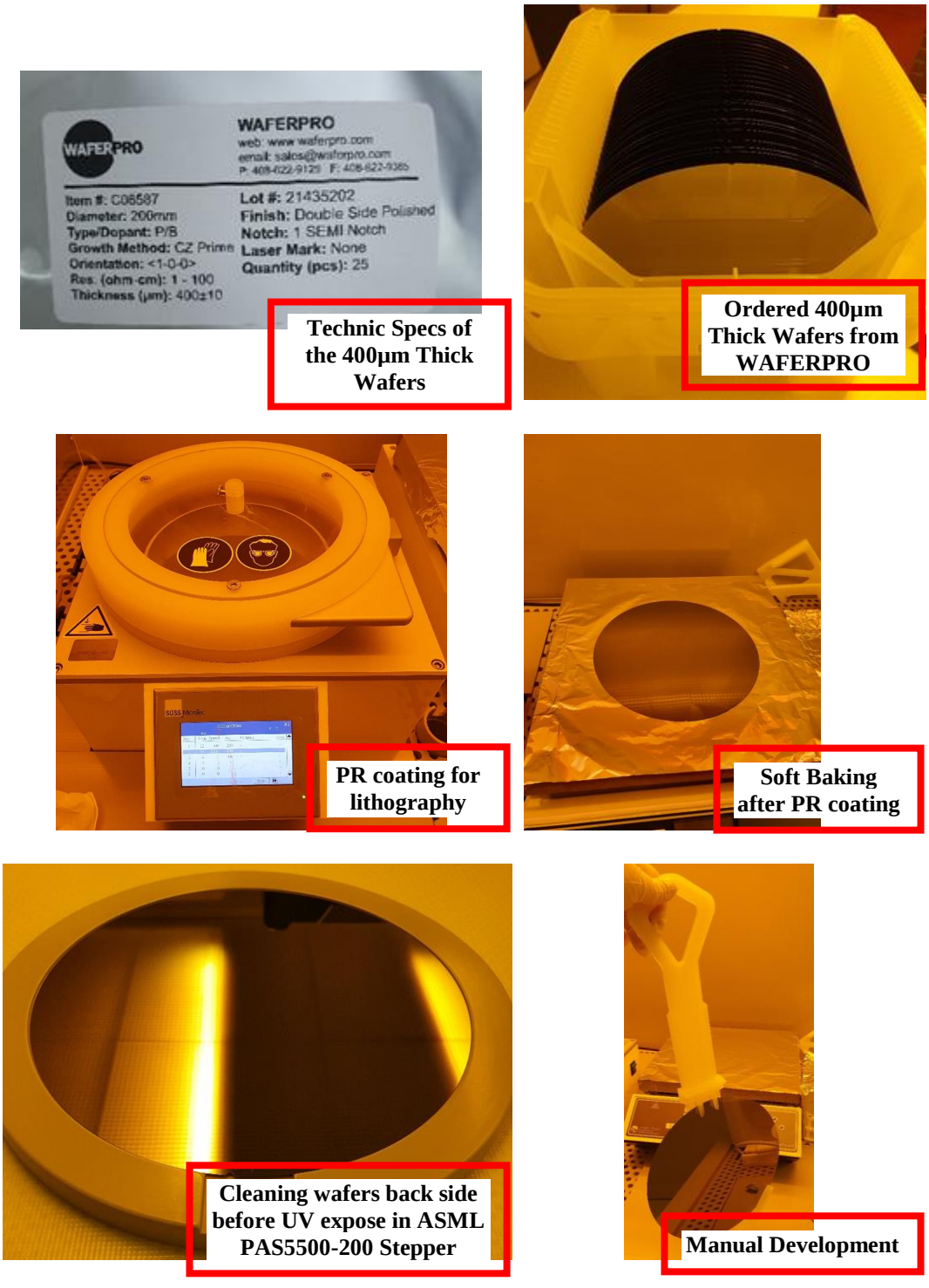


Figure 3.34. Images taken from 400µm Thick 8” DSP Wafer during the handling and lithography process steps.

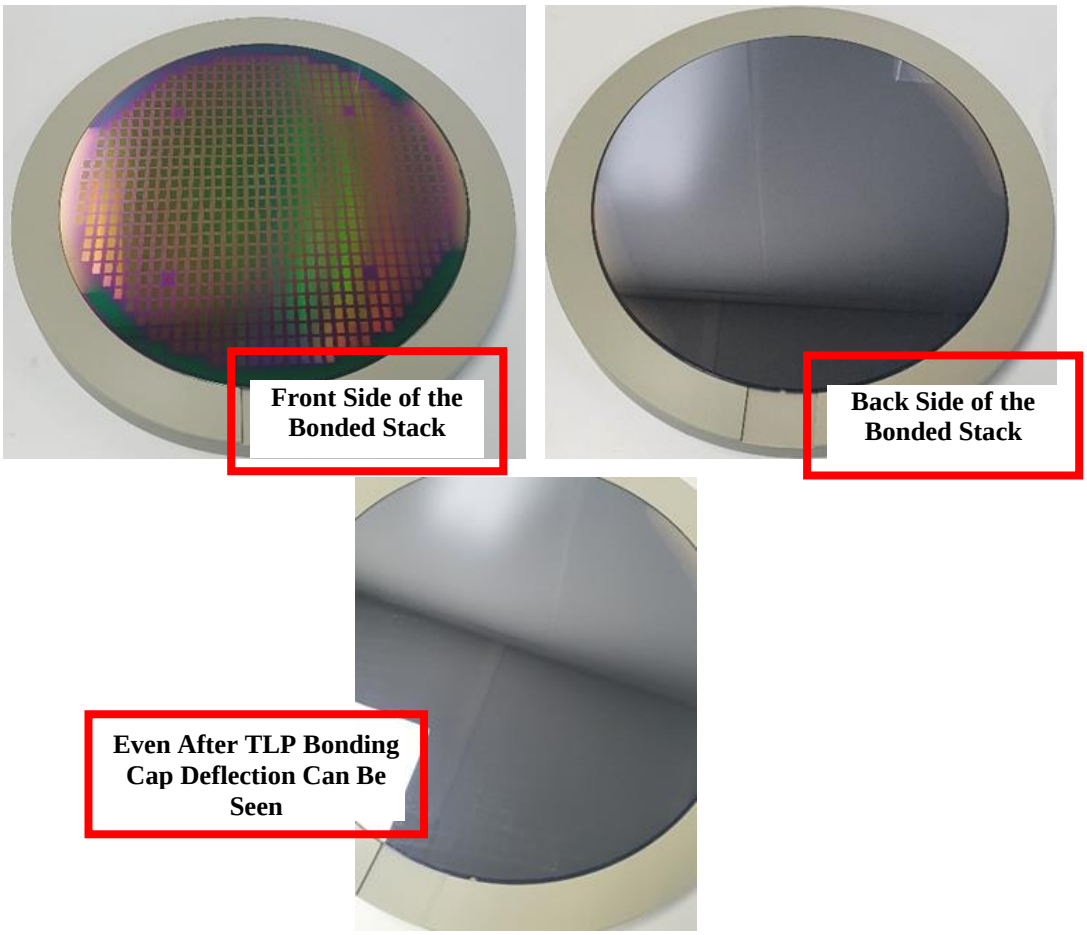


Figure 3.35. The front and back side views of the Au-In TLP Bonded Wafer A+B stack. Notice that 400µm thin wafer is used to eliminate the grinding step.

To conclude, wafer bonding experiments are tried for both standard 725µm thick Wafer A to 725µm thick Wafer B and 725µm thick Wafer A to 400 µm thin Wafer B; and all wafer bonding experiments worked properly. After completing all remaining processes which are cap cavity formation, screen printing and getter material deposition before glass frit bonding to device wafer (Wafer C) optimum case would be selected. As previously mentioned, the thickness of the cap wafer is a tradeoff between the need to minimize the absorption of the incoming IR radiation and not only the requirements for low wafer bow introduced by the stress in the deposited films but also for safe handling during the process. Also, in thin wafer usage 400µm depth must be etched for cavity opening in DRIE.

3.3 Cap Cavity Formation

Under this subheading cap cavity formation details is going to be discussed. Needless to say, after the Au-In TLP bonding and grinding, if necessary, cavity structures have been processed/fabricated by using the MEMS fabrication techniques. Cap cavity formation of Si cap wafers (Wafer A+B stack) was performed using the STS Pegasus DRIE system, as can be seen in Figure 3.36, with process gases of C_4F_8 and SF_6. PR has been used as the mask layer during the DRIE process and was patterned with UV lithography. The 150-200µm (for standard case after grinding the stack) and 400µm (for thin wafer case to eliminate grinding step) deep cavities with x≈3500µm and y≈5200µm have been fabricated on cap wafers to obtain a vacuum cavity after the bonding and integrating the gratings inside (Figure 3.37). As a next step, the oxide (for etch stop purposes at the bottom of Wafer A) and nitride (for protection purposes at the top of Wafer A) layers has been removed from the cavity opened Wafer A+B stack (Figure 3.38) by soaking the stack BHF solution. Last but not least, the squeezed out In is removed by soaking cap wafers to HCl solution.

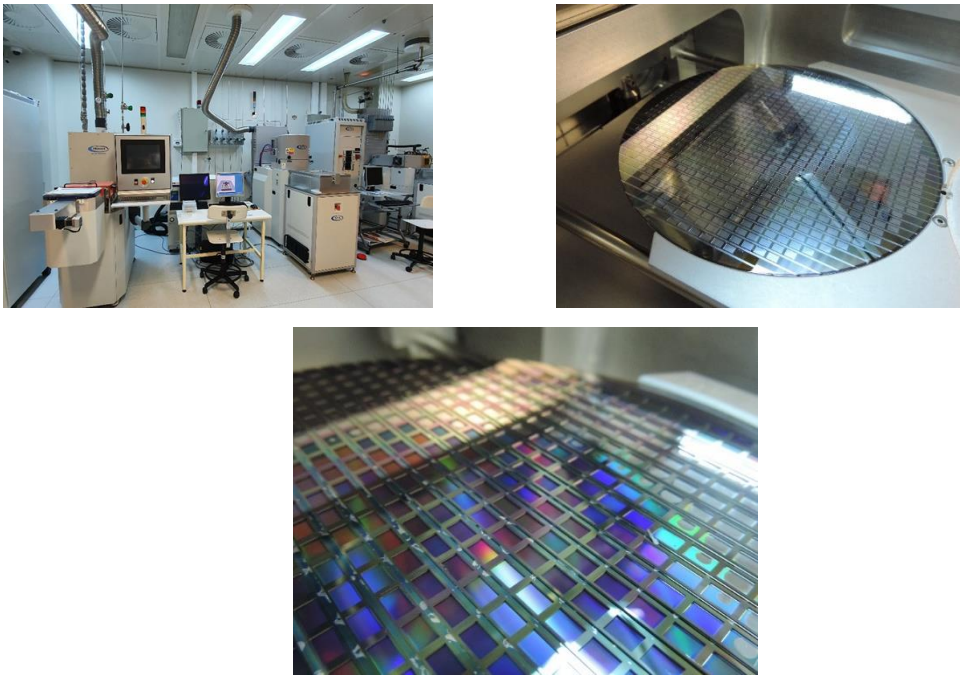


Figure 3.36. The pictures of STS Pegasus DRIE System used in METU MEMS Center and cap cavity formation of Si cap wafers (Wafer A+B stack).

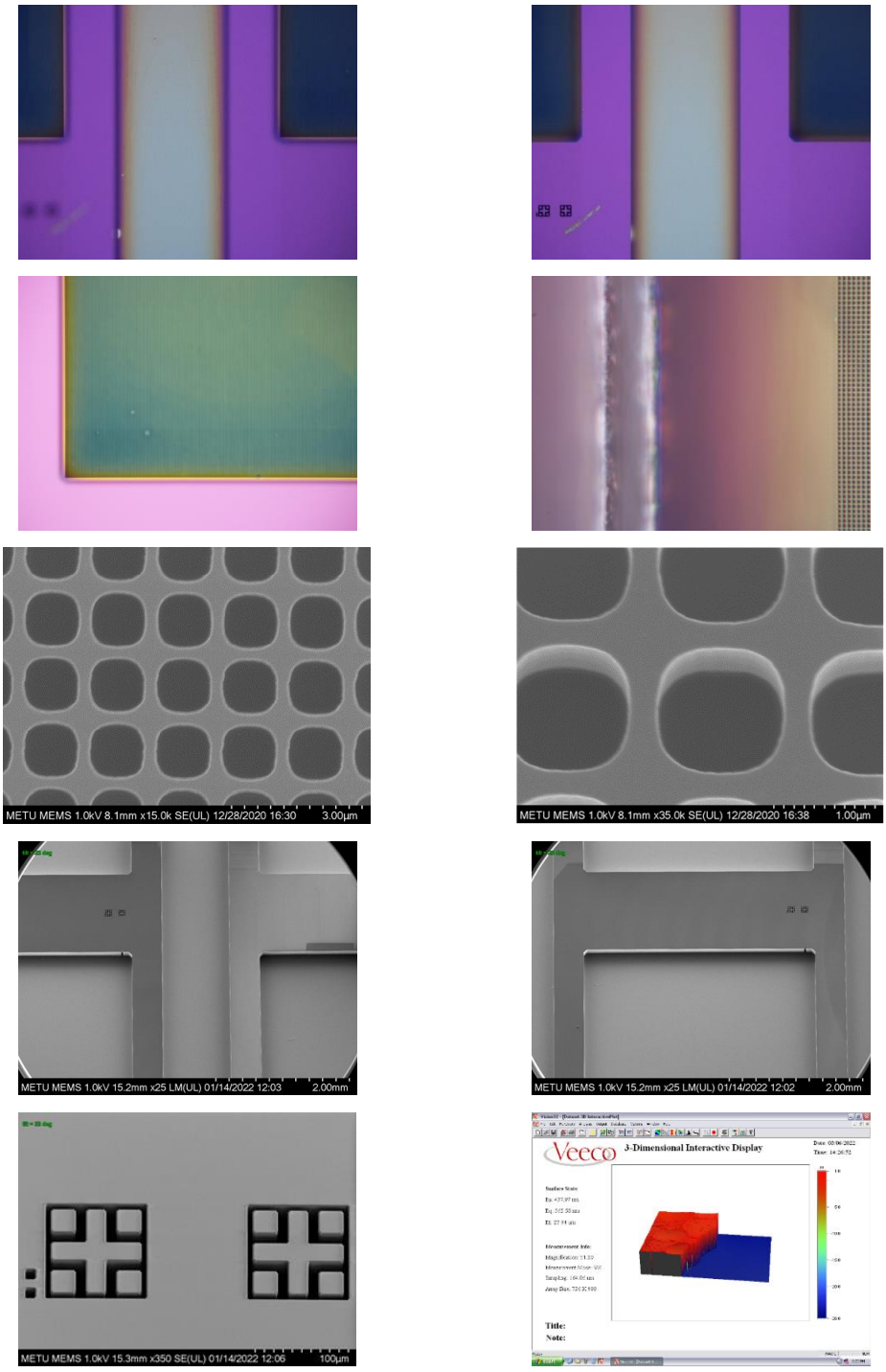


Figure 3.37. The optical microscope, SEM image and optical surface profile measurement of the fabricated cavity in cap wafer after DRIE and Polymer Removal steps.

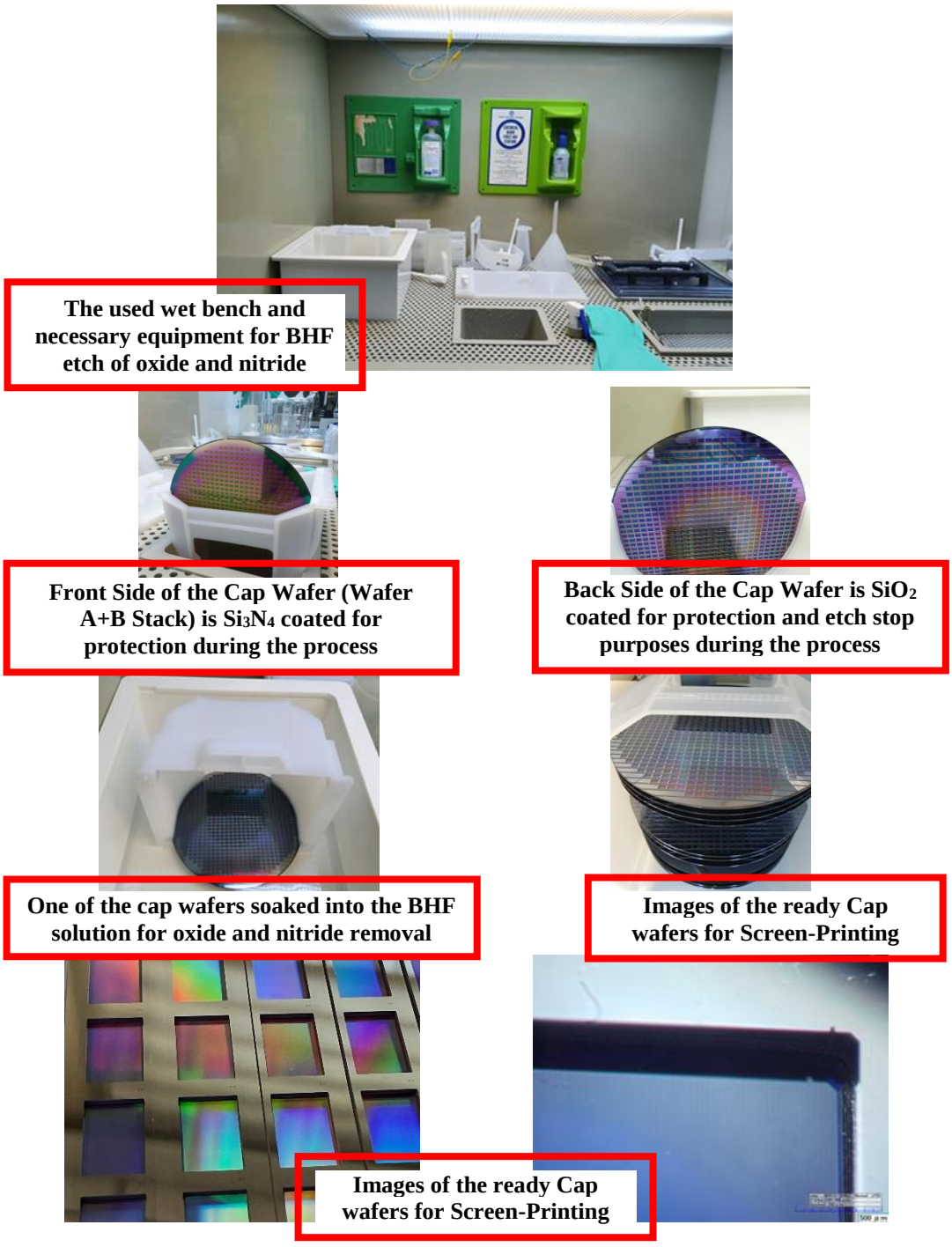


Figure 3.38. The images showing nitride and oxide removal by soaking BHF to cavity opened Wafer A+B stack.

3.4 Wafer Level Packaging Using Glass Frit Bonding

In this study, 8” wafer level Glass-Frit hermetic encapsulation technique have been selected as a second branch for offered cap wafer design and its details given below subtitles one by one.

3.4.1 The Studied Glass Paste and Necessary Equipment Technical Details

The glass frit bonding process consists of three major steps which are screen printing of a glass paste, thermal conditioning or frit firing and thermo-compressive bonding. For screen printing step the necessary equipment can be listed as glass paste, screen including polyester meshes, flood and print squeegee with suitable squeegee rubber and obviously cap wafer, and screen printer. As the first step, Ferro FX11-036 glass paste is selected because it is the most widely used glass paste in MEMS industrial applications. Besides, it is not only provided as ready to use paste but also noncrystallizing glass frit material. The datasheet [74] of the used Ferro FX11-036 glass paste can be seen in Table 3.3.

Table 3.3 The datasheet of FX11-036 and comparison of glass pastes from Ferro Company [74].

Typical Properties	DL1161HZ	DL1180A	DL11-036	DL11-155	DL11-201
Thermal Expansion (ppm @260°C)	6.4	7.5	9	9	10
Viscosity (Pa.s)	70 - 90	54.5 -70.5	55 - 87.5	50 -100	70 -100
Recommended Screen Mesh	80	250 - 325	250 - 325	150 - 250	250 - 325
Typical Dry Print Thickness (µm)	34 - 40	22 -28	22 - 24	20 -24	22 -28
Typical Fired Print Thickness (µm)	25 -30	11 - 14	7 - 11	11 - 14	11 - 14
Solids Content (%)	86 ± 1	78 ± 1.5	84 ± 2	85 ± 2	85.5 ± 1.5
Binder Burnout and Glazing Cycle					
Binder Burnout Temperature (°C)	280	400	295	360	315
Time at BBO Temperature (mins)	30	20 - 30	20 - 30	20 - 30	20 - 30
Glaze Temperature (°C)	380 - 400	500	400 - 425	425 - 450	425 - 450
Time at Glaze Temperature (mins)	5 - 15	5 - 15	5 - 15	5 - 15	5 - 15
Firing/Sealing Cycle					
Peak Temperature (°C)	410 -430	575 - 625	425 - 450	475 -550	450 - 475
Time at Peak (mins)	10 - 15	10 - 20	15 - 30	15 - 30	15 - 30

After the decision of the glass paste, the next step is screen design and ordering. The drawn screen layout details for the offered cap wafer compatible design could be found in Figure 3.39. According to that layout, screens are produced from BRAVE and PVF companies. The technical details of the produced screens are as the following:

- Mesh type 325-030, Bias 45°; Frame type 12 x 12 inch (355x355mm), Coating type: GBF 444_S; EOM 5 µm or 10 µm
- Mesh type 290-020; Bias 45°; Frame type 12 x 12 inch (355x355mm), Coating type: GBF 444_S, EOM 5 µm or 10 µm

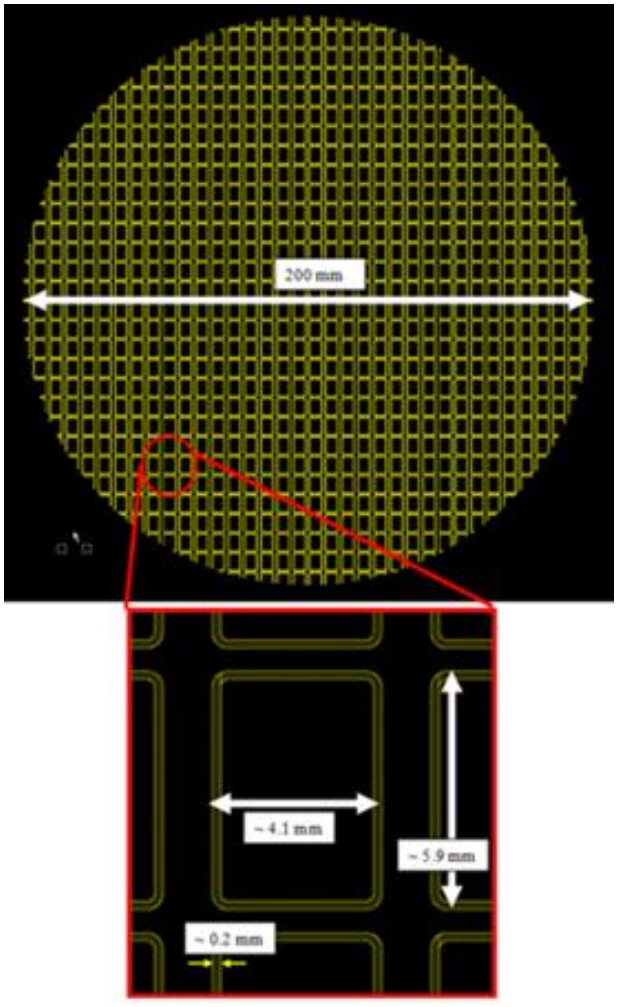


Figure 3.39. The layout details for new mask screen order from Brave and PVF companies compatible with offered cap wafer designs.

After ordering screens and glass pastes, for the first time in our Center instead of sending wafers abroad (never 8” size processed before) METU GÜNAM- Center for Solar Energy Research and Applications’ Ekra Model screen printer is observed and after 8” size compatible equipments are produced in METU MEMS Center’s machine shop, screen-printing trials and optimizations are started (Figure 3.40). Notice that before adopting second branch to offered cap wafer study (Wafer A+B stack), in 8” size with processing Wafer D which is cap cavity probe wafers optimization studies are performed.

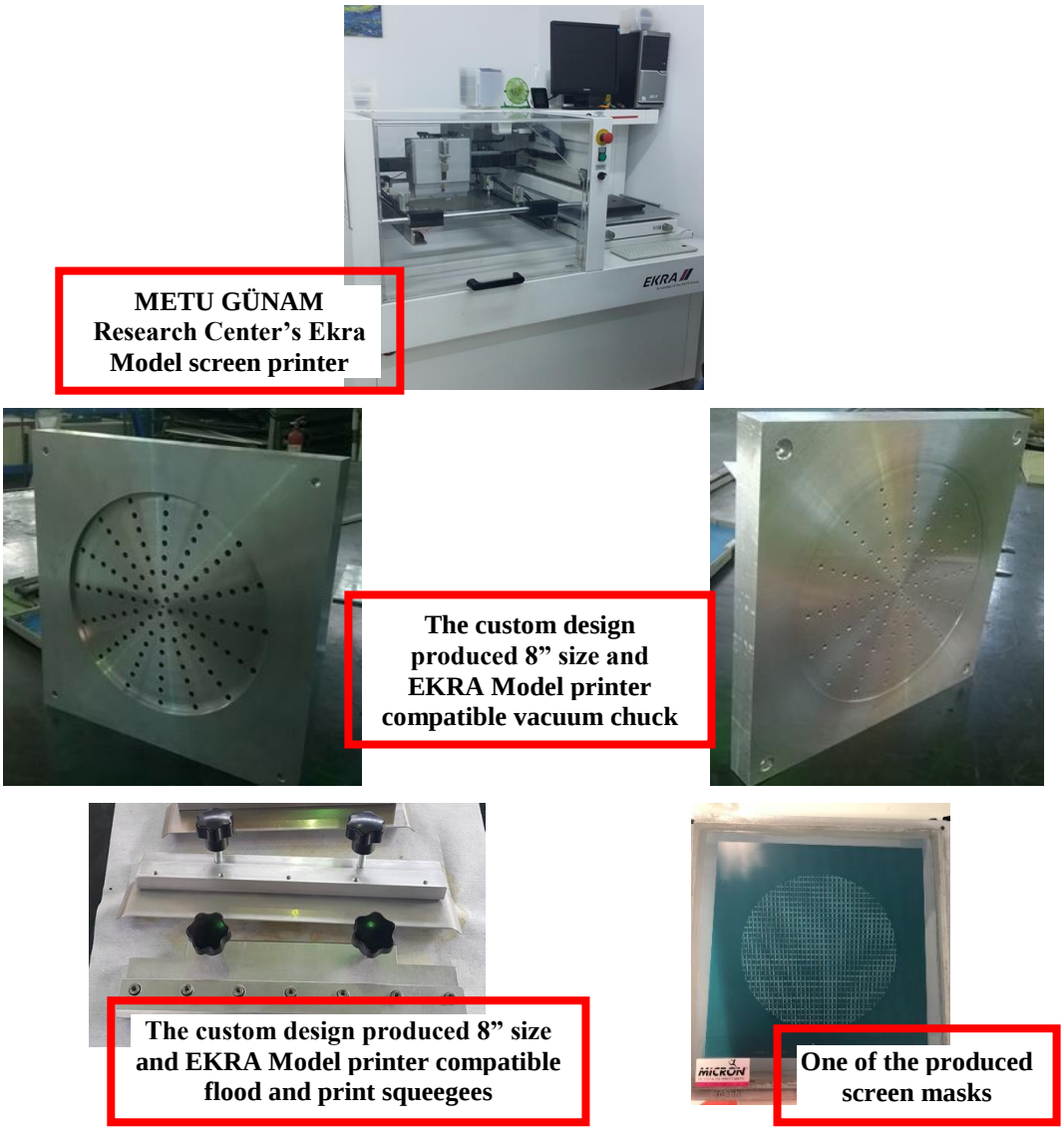


Figure 3.40. The images showing necessary equipment for offered cap wafer process screen printing trials.

After integrating the ordered and custom designed equipment to METU GÜNAM Research Center's Ekra Model screen printer it is ready for offered cap wafer's screen-printing trials (Figure 3.41).

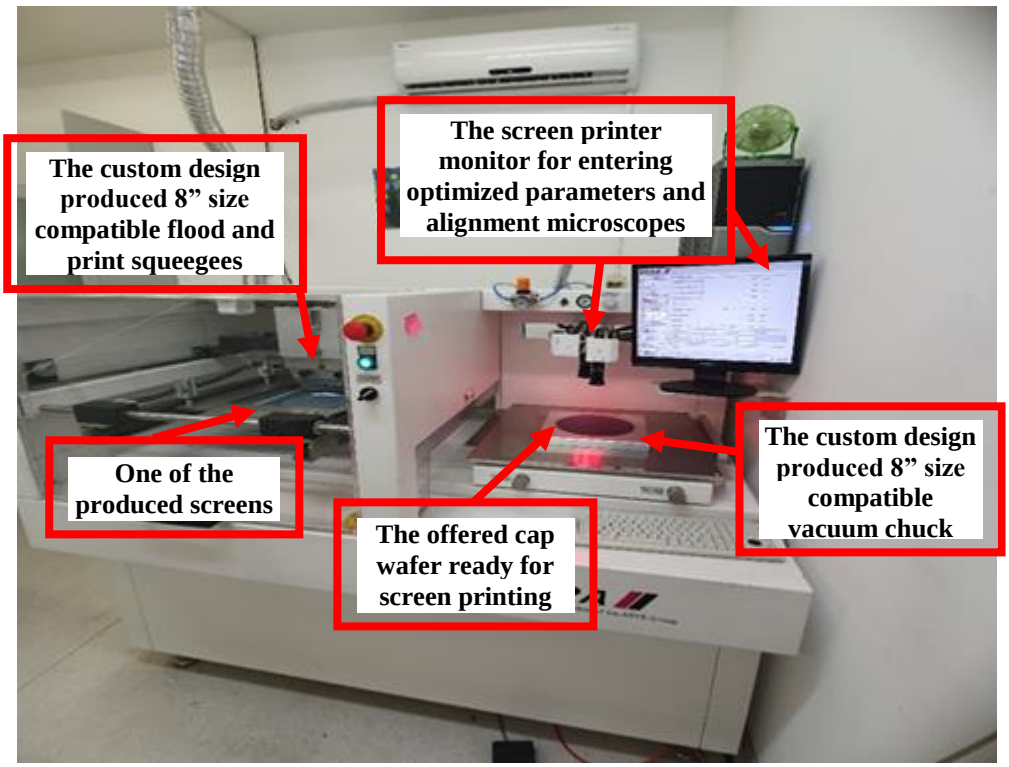


Figure 3.41. EKRA Model Screen-Printer at GÜNAM General View with the integration of necessary equipment on it for offered cap wafer's screen-printing trials.

3.4.2 Screen-Printing of the Glass Paste Process Details

Under this sub-heading firstly, the screen-printing of the glass paste process details is going to be listed then these process steps are going to be shown in Figure 3.42.

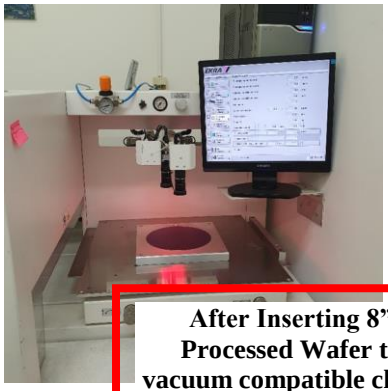
1. Spread the frit paste linearly on one or two sides of the screen. Run the squeegee on the screen with the paste to print on the acetate paper.
2. Experiment with the distance and pressure on the squeegee on dummy acetate, and after getting a sense of the process switch to actual wafer.

3. After a successful printing, the screen is cleaned with following sequence:

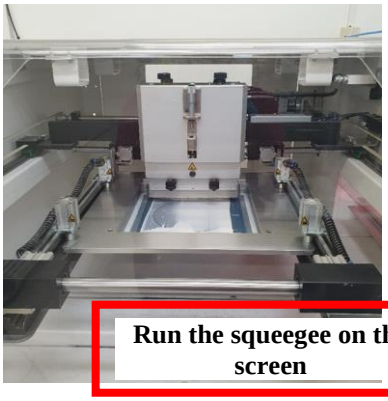
    - ✓ IPA wet wipe on both surfaces
    - ✓ Wait to dry on both surfaces
    - ✓ Dry wipe on both surfaces
    - ✓ Repeat if necessary
    - ✓ N_2 gun on both surfaces

4. The printing on actual wafer is performed multiple times. The first time a transparent layer (acetate) is used between the wafer and the screen. The alignment is checked on the acetate paper which is transparent layer. After the several runs to adjust the alignment, a final run is performed to ensure the alignment. After a successful run of the paste on the actual wafer, it is ready for thermal conditioning (frit firing).

After Spreading Ferro Glass Paste to the Screen



After Inserting 8" Processed Wafer to vacuum compatible chuck



Run the squeegee on the screen

Paste to print on the acetate paper several times

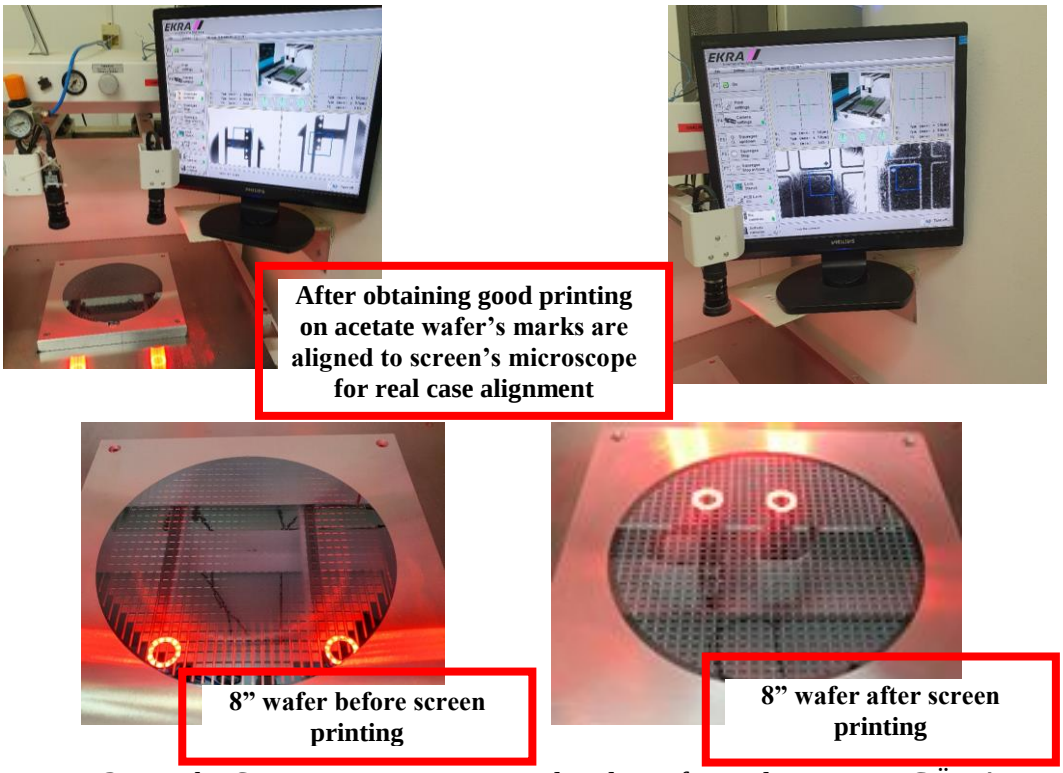


Figure 3.42. The Screen-Printing process details performed at METU GÜNAM-Center for Solar Energy Research and Applications' Ekra Model screen printer.

3.4.3 Thermal Conditioning (Frit Firing) Process Details

After performing successful screen-printing to the cap wafer; for frit firing step the necessary equipment can be listed as screen printed cap wafer and high temperature oven. The performed process details can be listed as following and these process steps are going to be shown in Figure 3.43:

1. After a successful run of the paste on the actual wafer, the first bake process is performed while keeping wafers horizontal as much as possible
2. Bake #1:
    - ✓ Preheated at 100°C hold for 30 min (Performed at GÜNAM's Nüve KD200 model oven)

3. Bake #2 Frit fire: (Air flow on horizontal from one side to the other in the oven; performed at METU MEMS Center's Carbolite Gero High Temperature Oven)

    - ✓ 100°C to 290°C (ramp is not important but as fast as possible) hold for 4 hours
    - ✓ 290°C to 400°C (ramp is not important but as fast as possible) hold for 1 hour
    - ✓ 400°C to 270°C (ramp is not important but as fast as possible) hold for 30 min
    - ✓ 400°C to Room Temp (passive cooling in the oven).

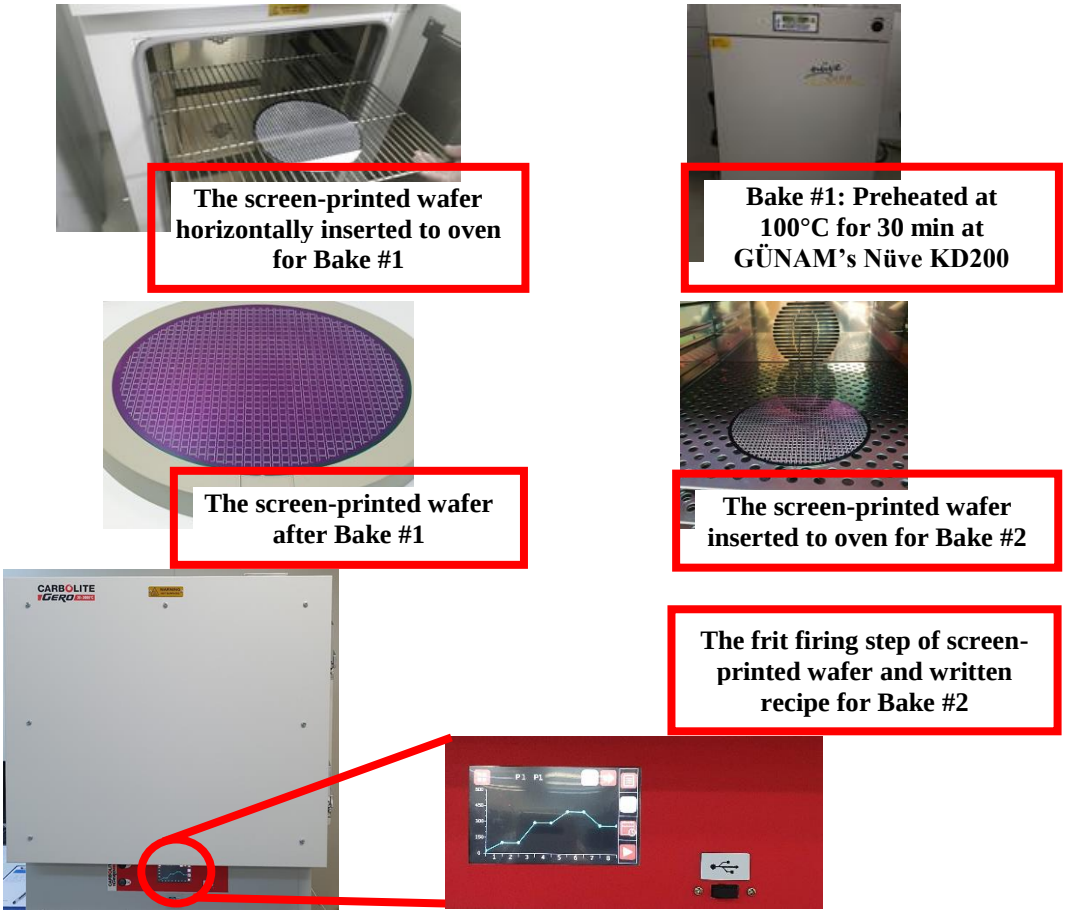


Figure 3.43. Thermal Conditioning (Frit Firing) process details.

The dummy 8” wafers’ before and after frit firing comparison can be observed in Figure 3.44.

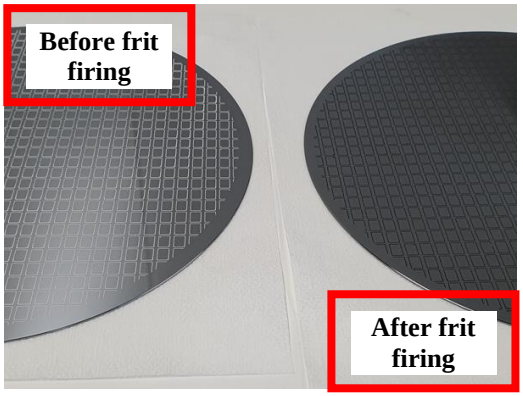


Figure 3.44. The image taken from two of screen-printed dummy wafers one is before and other is after frit firing to show visual differences of them.

After frit firing wafers are ready for glass frit bonding.

3.4.4 Thermo-Compressive Glass Frit Bonding Process Details

The calculation of bonding force is based on the design parameters and proposed cap wafer process mask set is designed using the L-Edit design software. In proposed design the bonding area is calculated as 3058mm^2 for 8” size screen printed and frit fired wafer.

Notice that initially bonding process started at room temperature and first heating is applied in atmosphere by applying forming gas (5% H_2 and 95% N_2). The performed glass frit bonding recipe is “MS0835A_8in_GFv1_f2000” and bonding conditions are as the following: Applied Force=2000N, Ramp Rate=300N/min and Bonding Temperature=440ºC. EVG 6200 Bond Alignment and EVG 520IS Wafer Bonder Systems used in METU MEMS Center, so for the second branch which is glass frit bonding, the sample bonding profile could be seen in Figure 3.45.

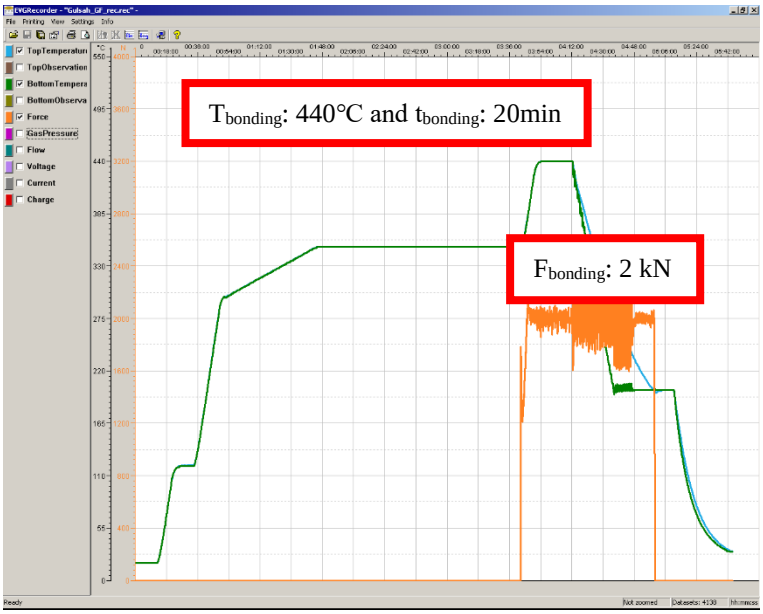


Figure 3.45. The example glass frit bonding profile performed at EVG 520IS Wafer Bonder Systems used in METU MEMS Center.

3.4.5 Characterization and Experimental Analysis Results for Glass Frit Bonded Wafers

After performing successful screen-printing and frit firing the glass paste layers have been characterized in terms of structural, chemical, and thermal properties. Similarly, after performing glass frit bonding, the bonded wafer stack has been analyzed for characterization purposes. Under this heading structural and morphological investigation, elemental analysis, thermal analysis, and mechanical characterization details given below subtitles one by one. Notice that this characterization and experimental analysis is necessary for continuing the process in terms of hermetic sealing of offered cap wafer (Wafer A+B stack) to CMOS Probe Wafer (Wafer C).

3.4.5.1 Optic Microscope and Profilometer Inspections

In screen-printing, chuck vacuum level, squeegee speed back and forward (mm/s), squeegee position in terms of front-back (mm), squeegee pressure (bar) and separation (mm) are very significant parameters, and each must be optimized. It is really significant to optimize the squeegee force and paste amount to get homogeneous printing. Ideal case is the ridge of the printed paste under the light should be a single stream. As it can be seen from Figure 3.46, the right hand side image is a line profile that results in multiple irregular reflections indicating undesired profile which is caused due to lack of chuck vacuum quality so wafer stuck to the screen; the middle image is inserted to show due to much paste amount printing quality is nonuniform; finally left hand side image is a line profile that results in multiple irregular reflections indicating undesired profile which is caused due to custom made squeegee rubber is not forcing the surface equally.

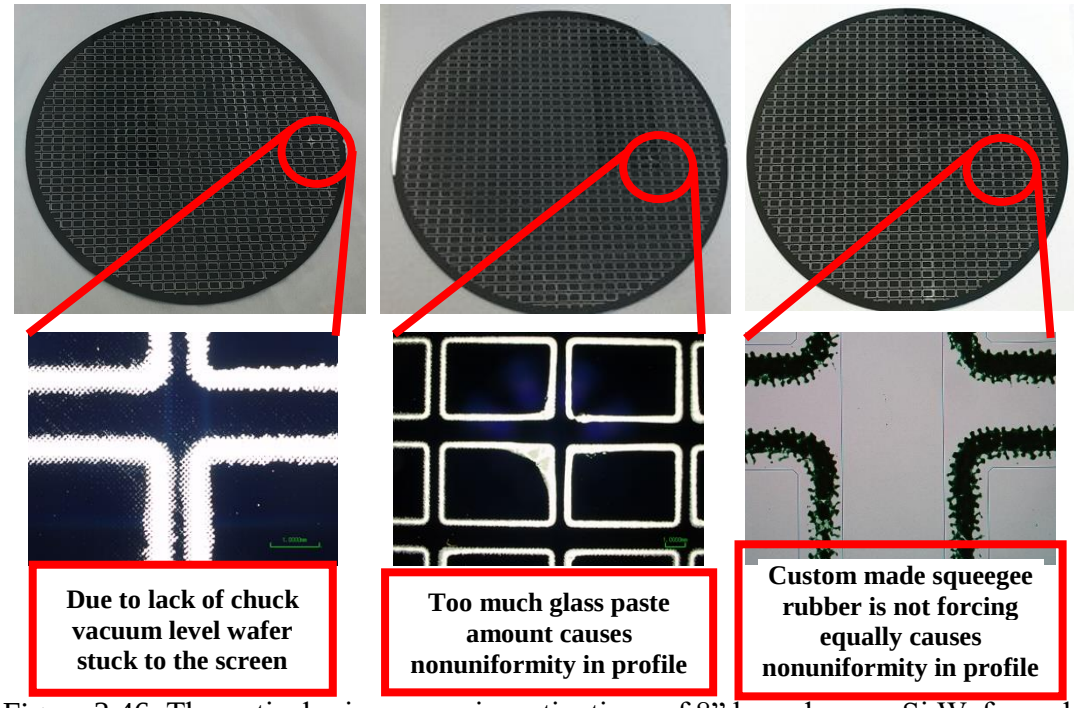
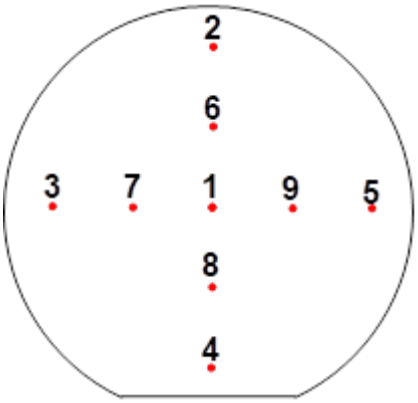


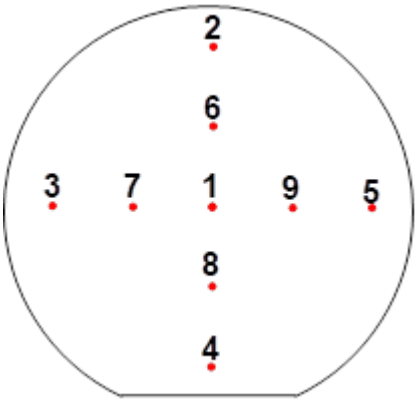
Figure 3.46. The optical microscope investigations of 8” bare dummy Si Wafer and Wafer D (Cap Cavity Probe Wafer) after screen-printing optimization trials as can be seen all three case shows undesired profile which will affect the glass frit bonding quality.

After performing some experiments and optimizing the chuck vacuum level and glass paste amount custom made squeegee rubber based nonuniformity is measured in Veeco Dektak8 Stylus Profilometer (Figure 3.47 (a)). Then, the Internet is searched and to solve the nonuniformity problem, 25 pieces of HQ Squeegee rubber Profile D 85° Shore - blue / 230x9,5x9,5 mm original squeegee rubber from Koenen Company is ordered (Figure 3.48) and trials are continued with them (Figure 3.52 (b) and Figure 3.49).



Measurement Point	Thickness (µm)
1	35.6
2	24.9
3	27.3
4	38.0
5	34.2
6	26.4
7	35.8
8	21.2
9	30.5
Mean	30.43±5.79

(a)



Measurement Point	Thickness (µm)
1	22.5
2	20.1
3	25.6
4	25.4
5	25.7
6	20.8
7	20.2
8	19.7
9	19.8
Mean	22.2±2.65

(b)

Figure 3.47. The glass frit nonuniformity thickness analysis and comparison with using custom made squeegee rubber (a) and with original squeegee rubber (b), in Veeco Dektak8 Stylus Profilometer.

Product Characteristics

- Homogenous, bubble and pore-free material structure
- Long life time due to high material strength
- Chemical resistance
- Resistant to UV-hartening varnishes
- High swelling resistance to most solvents
- Ageing resistant and sliceable
- Easy and rapid cleaning thanks to anti-adhesive properties

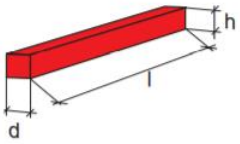
Profile D	
Height h in mm	Thickness d in mm
9,5	9,5

Special squeegee configurations on request. For thick film machines only.

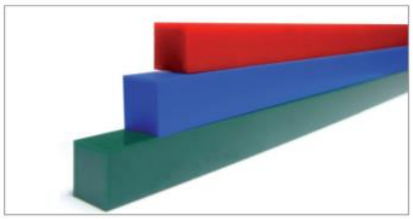
Shore hardness

65° Shore / red
75° Shore / green
85° Shore / blue

Profile D, square



Squeegee tolerances: + / - 1 mm length
+ 0,4 mm und - 0,1 mm thickness
+ / - 5° Shore A (according to DIN 17715)
* Subject to technical modifications.



Cost savings due to:

- Very process-stable printing results
- **Increased life time**

(a)

Left: Custom Squeegee Rubber

Right: Original Squeegee Rubber

Left: Custom Squeegee Rubber

Right: Original Squeegee Rubber

(b)

Figure 3.48. The technical details of the ordered squeegee from Koenen Company [75] (a) and visual comparison of squeegee rubbers (b).

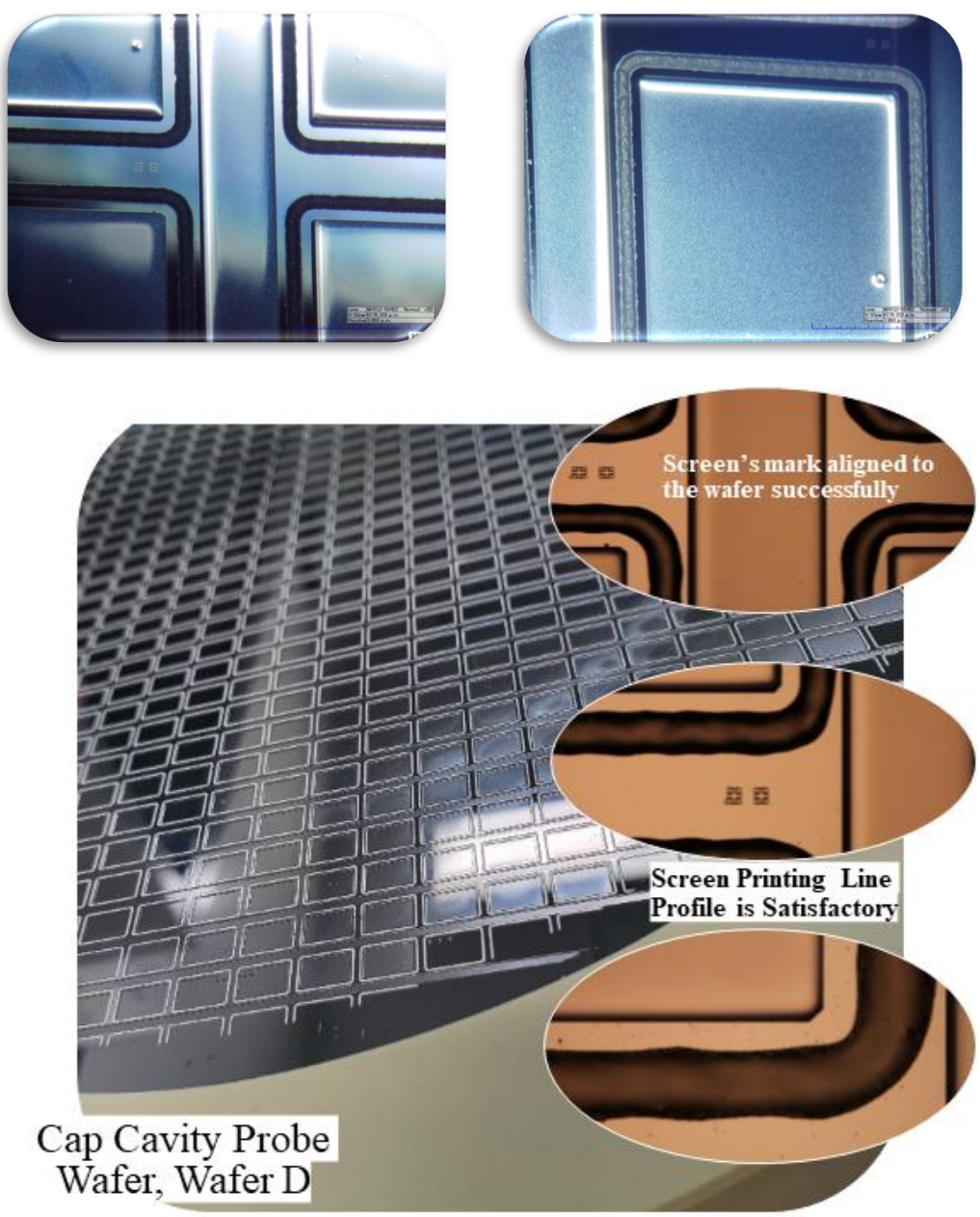


Figure 3.49. The images showing Cap Cavity Probe Wafer, Wafer D in terms of wafer level and optic microscope die level to show non-uniformity problem is solved after new ordered squeegee rubber is used; the results are much more satisfactory.

3.4.5.2 SEM Inspections

To be ready for glass frit bonding, screen printed and frit fired pastes are inspected with Hitachi Regulus 8230 scanning electron microscopes (SEM). Also, the elemental analysis of the thin films has been performed with energy-dispersive X- ray spectroscopy (EDS) after dicing glass frit bonded stack and applying destructive shear tests. Notice that although destructive shear test details will be given in the sub heading of "3.4.6.4 Destructive Shear Tests" SEM images of the analyzed broken dies could be seen in Figure 3.50.

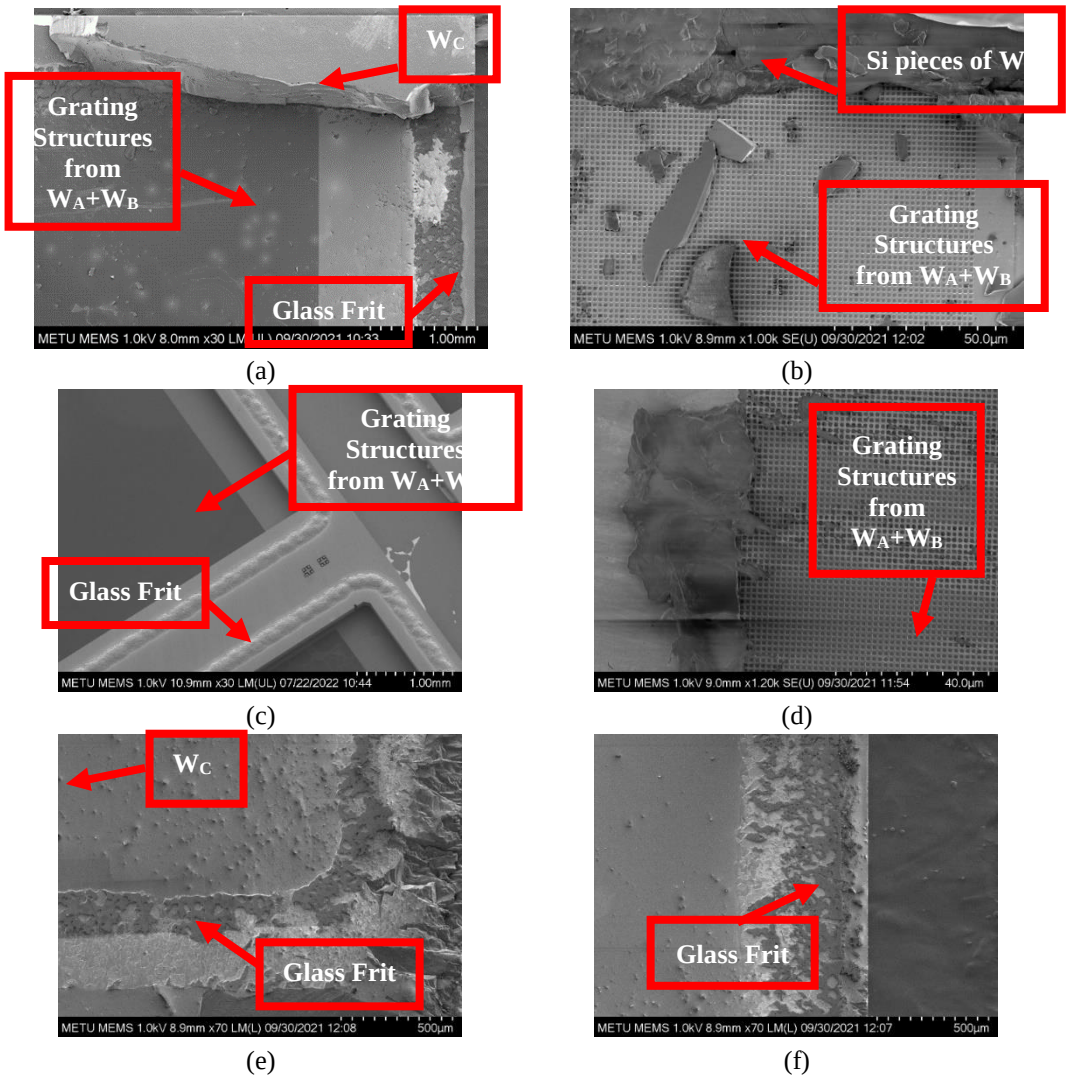
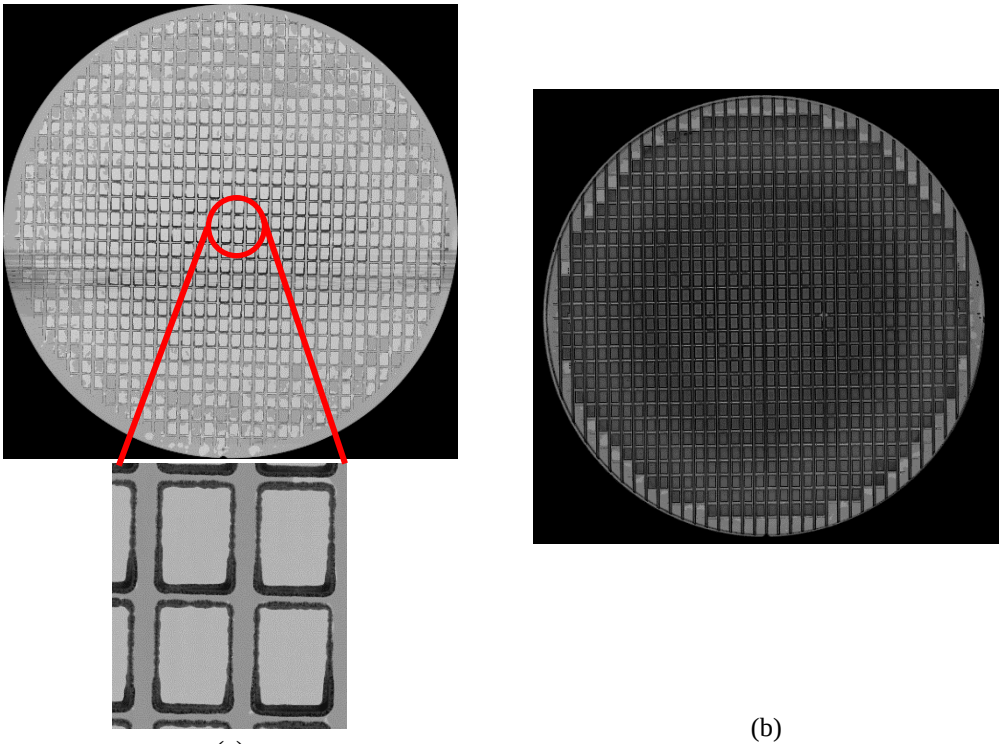


Figure 3.50. The images of the glass frit bonded stack diced and shear test applied case: (a-f) the SEM analyze results from the broken pieces.

After investigating the SEM analyze results from the shear test applied broken pieces it seems bonding quality is good.

3.4.5.3 SAM Inspections

For the wafer level bonding good screen-printing and bad screen-printing cases are compared; after the end of process two processed dummy 8” wafers (Wafer D and Wafer C without sensor) are bonded to each other with the parameters of applied force = 2000 N force and 300N/min ramp rate and 440ºC bonding temperature. After applying wafer level bonding for these two cases in EVG Wafer Bonder System, the bonded stacks are characterized and analyzed in surface acoustic microscope (Figure 3.51) and the wafer stacks are scanned with 100µm and 50 µm resolutions; respectively.



(a) (b)

Figure 3.51. The surface acoustic microscope analyzes results of two 8” glass frit bonded, 200mm diameter, CZ Silicon material P-type Boron Doped, 1-0-0 orientation, Prime grade,

725µm thickness, and 1-50Ω-cm resistivity, SSP dummy wafer and Wafer D for comparing bad screen printing (a) and good screen printing(b).

Notice that in two cases the wafer stacks analyzed with 50µm resolution. As it can be seen in Figure 3.51 (a) in the middle area of the wafer some error like lines occurred, so a small area is selected and rescanned with 10µm resolution to show how bad screen-printing results. Needless to say, in the scanned two wafers dark side means bonded part and in Figure 3.51 (b) bonding quality seems good and light side means gratings and unbonded parts.

3.4.5.4 Destructive Shear Tests

The glass frit bonding in terms of screen-printing quality cases are analyzed after applying shear tests to the diced wafers on shear tester tool and the results are compared. There are theree different test parameters: the first one is to observe bad screen-printing effects, the second one is to observe good screen printing effects on a bare wafers; and the third one is to observe real cap wafers. Under the destructive shear tests heading not only the reliability of the dies but also after years repeatability of them are analyzed; and tested regions from the wafers could be seen in Figure 3.52.

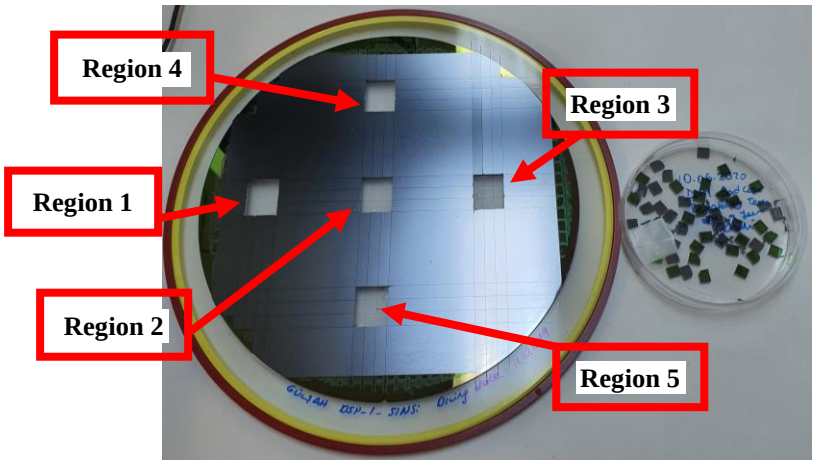
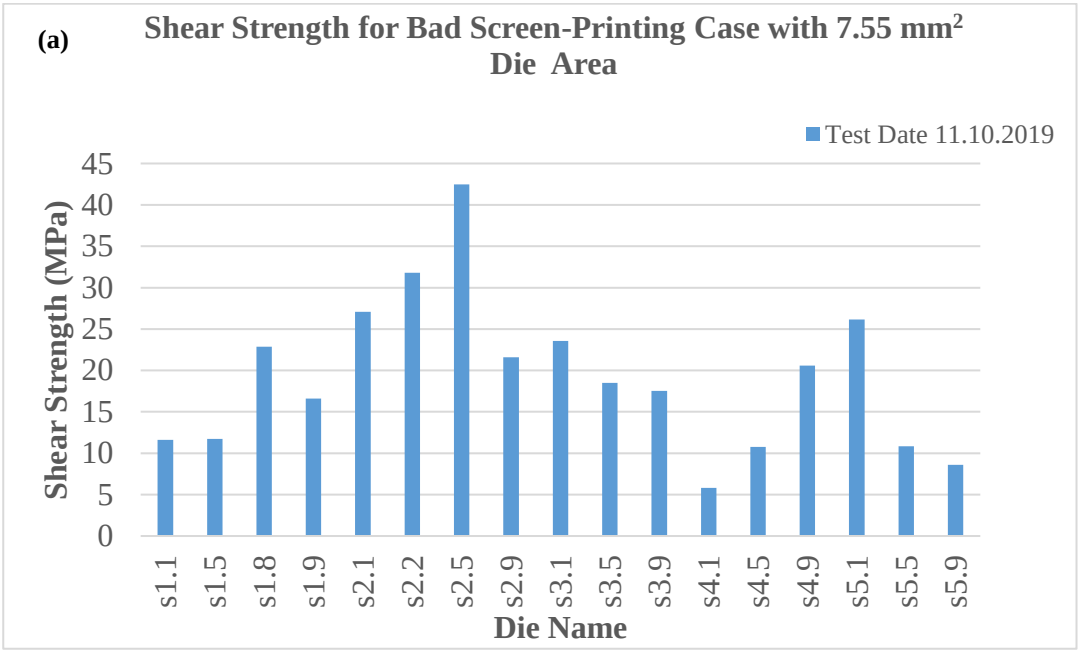
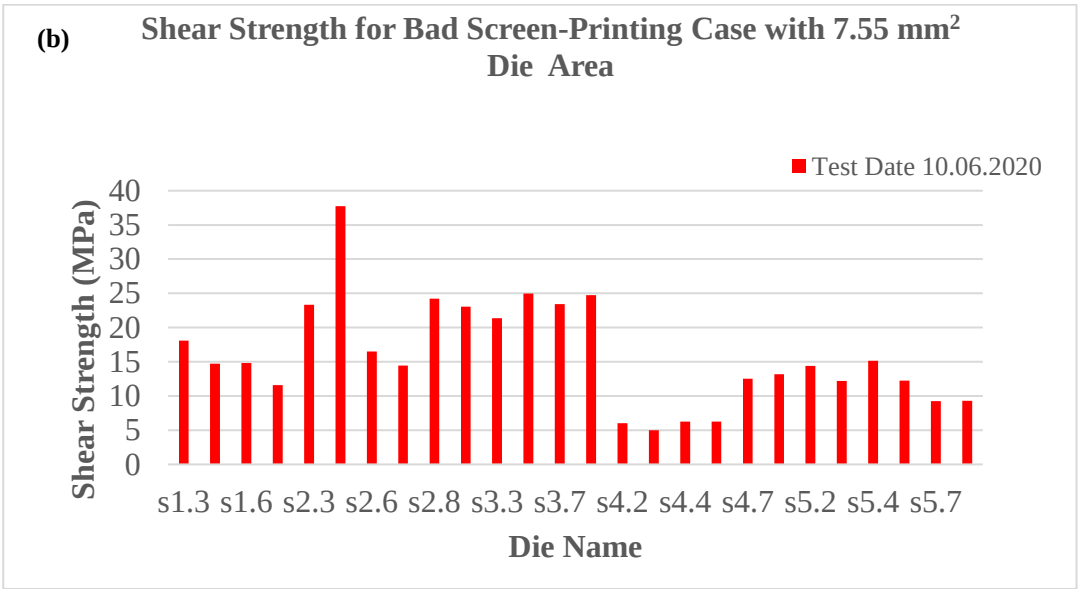


Figure 3.52. The image showing one of the diced wafers and shear test applied regions to analyze glass frit bonding quality.

3.4.5.4.1 Shear Test Results of Bad Screen-Printing Case

In this sub-heading, the destructive shear tests to bad screen-printed case identified glass frit bonded stack which includes bad screen-printing quality in which dies are sliced and first shear tests applied on 11.10.2019 and on 10.06.2020 the second destructive shear tests applied to remaining dies to observe the changes and reliability. The related results could be found in Figure 3.53, Table 3.4 and 3.5.





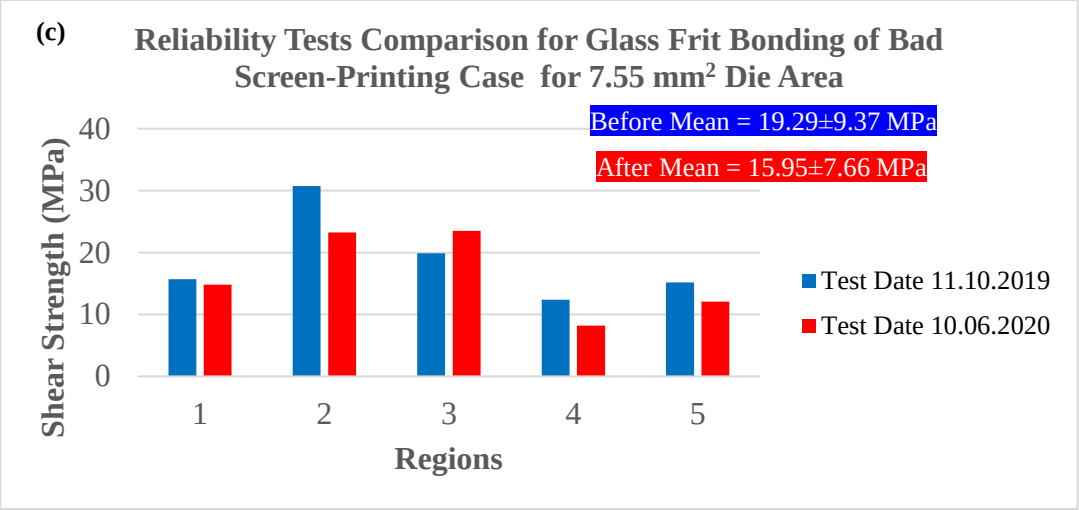


Figure 3.53. The applied shear tests to analyze the glass frit bonding quality after nearly one year later for: (a) just after bonding, (b) approximately 1 years later, and (c) comparison of them according to regions. Notice that for a single die, bonded area is calculated as 7.55 mm^2.

Table 3.4 Tabulated form of the 11.10.19 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
191011	**Left (Region 1)**	s1.1	87.66	11.61
		s1.5	88.64	11.74
		s1.8	172.52	22.85
		s1.9	125.48	16.62
	Middle (Region 2)	s2.1	204.39	27.07
		s2.2	239.98	31.79
		s2.5	320.71	42.48
		s2.9	163.05	21.60
	Right (Region 3)	s3.1	177.81	23.55
		s3.5	139.72	18.51
		s3.9	132.38	17.53
	Top (Region 4)	s4.1	43.91	5.82/Fail
		s4.5	81.2	10.75
		s4.9	155.37	20.58
	Bottom (Region 5)	s5.1	197.52	26.16
		s5.5	81.79	10.83
		s5.9	64.85	8.59

Table 3.5 Tabulated form of the 10.06.2020 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
200610	**Left (Region 1)**	s1.3	136.63	18.10
		s1.4	111.13	14.72
		s1.6	111.85	14.81
		s1.7	87.48	11.59
	Middle (Region 2)	s2.3	176.29	23.35
		s2.4	284.79	37.72
		s2.6	124.73	16.52
		s2.7	108.85	14.42
		s2.8	183.00	24.24
	Right (Region 3)	s3.2	174.17	23.07
		s3.3	161.17	21.35
		s3.4	188.69	24.99
		s3.7	176.91	23.43
		s3.8	186.77	24.74
	Top (Region 4)	s4.2	45.56	6.03
		s4.3	37.69	4.99/Fail
		s4.4	47.08	6.24
		s4.6	47.1	6.24
		s4.7	94.52	12.52
		s4.8	99.65	13.20
	Bottom (Region 5)	s5.2	108.66	14.39
		s5.3	92.18	12.21
		s5.4	114.42	15.15
		s5.6	92.58	12.26
		s5.7	69.82	9.25
		s5.8	70.11	9.28

Notice that for 11.10.2019 test applied date case, the average shear strength is measured as 19.29±9.37 MPa and similarly for 10.06.2020 test applied date case the average shear strength is measured as 15.95±7.66 MPa. In each case, in the region 4 which refers to top sides of the wafer there are two dies failed (which is below 6MPa military standard criteria) For comparison purposes before and after annealing shear

test results are plotted in a same graph in Figure 3.55 (c). Notice that obtained shear strength results are the average ones in each region.

3.4.5.4.2 Shear Test Results of Good Screen-Printing Case

In this sub-heading, the destructive shear tests to good screen-printed case identified glass frit bonded stack which includes homogenous and good screen-printing quality in which dies are sliced and first shear tests applied on 15.10.2019 and on 11.06.2020 the second destructive shear tests applied to remaining dies to observe the changes and reliability. The related results could be found in Table 3.6-7 and Figure 3.54. The average shear strength for the test date of 15.10.2019 is calculated as 25.33±10.23 MPa and for the test date of 11.06.2020 it is calculated as 17.84±3.85 MPa.

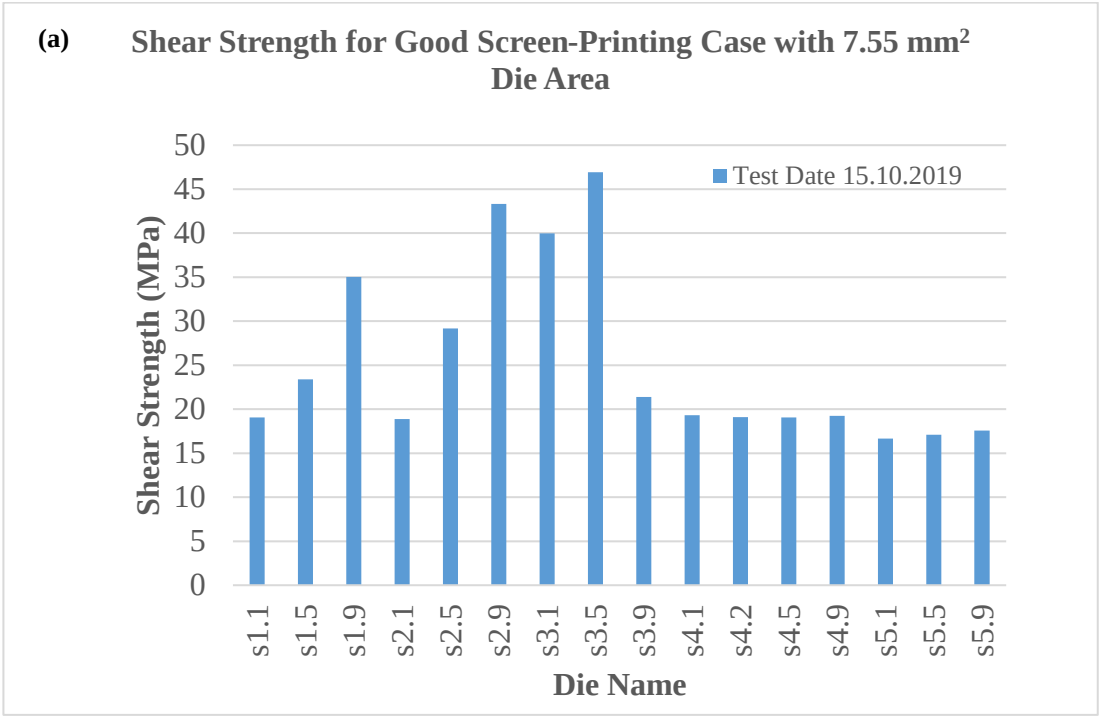
Table 3.6 Tabulated form of the 15.10.19 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
191015	**Left (Region 1)**	s1.1	143.88	19.06
		s1.5	176.56	23.39
		s1.9	264.55	35.04
	Middle (Region 2)	s2.1	142.55	18.89
		s2.5	220.2	29.17
		s2.9	327.25	43.34
	Right (Region 3)	s3.1	301.86	39.98
		s3.5	354.15	46.91
		s3.9	161.51	21.39
	Top (Region 4)	s4.1	145.88	19.32
		s4.2	144.1	19.09
		s4.5	143.85	19.05
		s4.9	145.43	19.26
	Bottom (Region 5)	s5.1	125.71	16.65
		s5.5	129.1	17.1
		s5.9	132.55	17.56

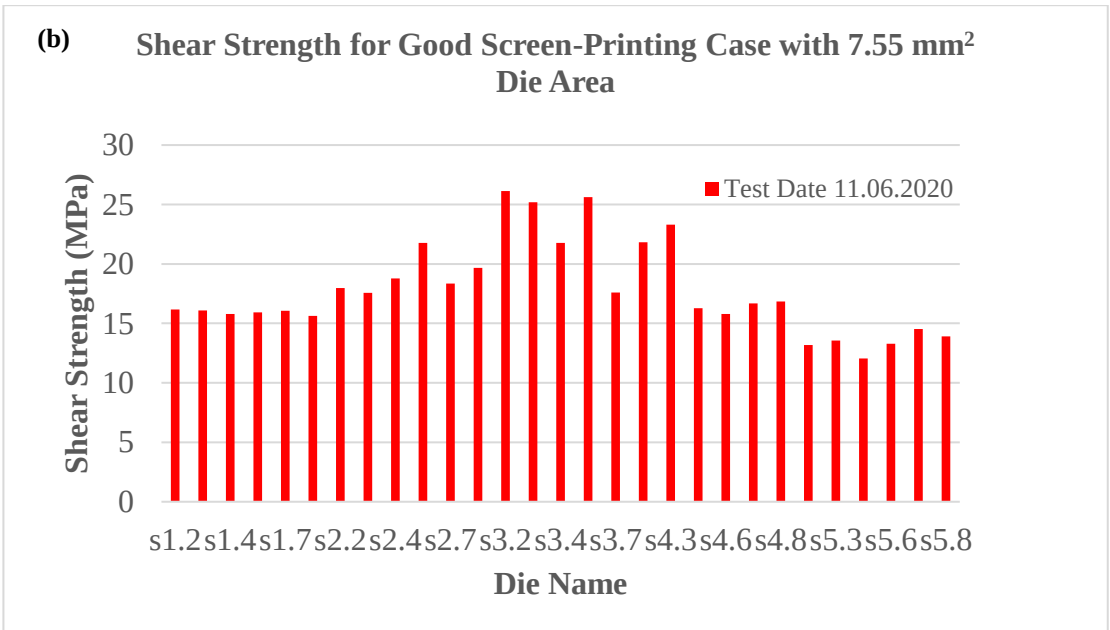
Table 3.7 Tabulated form of the 11.06.2020 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
200611	**Left (Region 1)**	s1.2	122.18	16.18
		s1.3	121.58	16.1
		s1.4	119.27	15.8
		s1.6	120.23	15.92
		s1.7	121.21	16.05
		s1.8	117.89	15.62
	Middle (Region 2)	s2.2	135.7	17.97
		s2.3	132.6	17.56
		s2.4	141.74	18.77
		s2.6	164.31	21.76
		s2.7	138.48	18.34
		s2.8	148.59	19.68
	Right (Region 3)	s3.2	197.35	26.14
		s3.3	190.17	25.19
		s3.4	164.28	21.76
		s3.6	193.32	25.61
		s3.7	132.79	17.59
		s3.8	164.81	21.83
	Top (Region 4)	s4.3	175.96	23.31
		s4.4	122.85	16.27
		s4.6	119.13	15.78
		s4.7	125.97	16.68
		s4.8	127.24	16.85
	Bottom (Region 5)	s5.2	99.41	13.17
		s5.3	102.45	13.57
		s5.4	90.93	12.04
		s5.6	100.41	13.3
		s5.7	109.73	14.53
		s5.8	105	13.91

(a)


Shear Strength for Good Screen-Printing Case with 7.55 mm² Die Area
Test Date 15.10.2019
Shear Strength (MPa)
50
45
40
35
30
25
20
15
10
5
0
s1.1
s1.5
s1.9
s2.1
s2.5
s2.9
s3.1
s3.5
s3.9
s4.1
s4.2
s4.5
s4.9
s5.1
s5.5
s5.9
Die Name

(b)


Shear Strength for Good Screen-Printing Case with 7.55 mm² Die Area
Test Date 11.06.2020
Shear Strength (MPa)
30
25
20
15
10
5
0
s1.2
s1.4
s1.7
s2.2
s2.4
s2.7
s3.2
s3.4
s3.7
s4.3
s4.6
s4.8
s5.3
s5.6
s5.8
Die Name

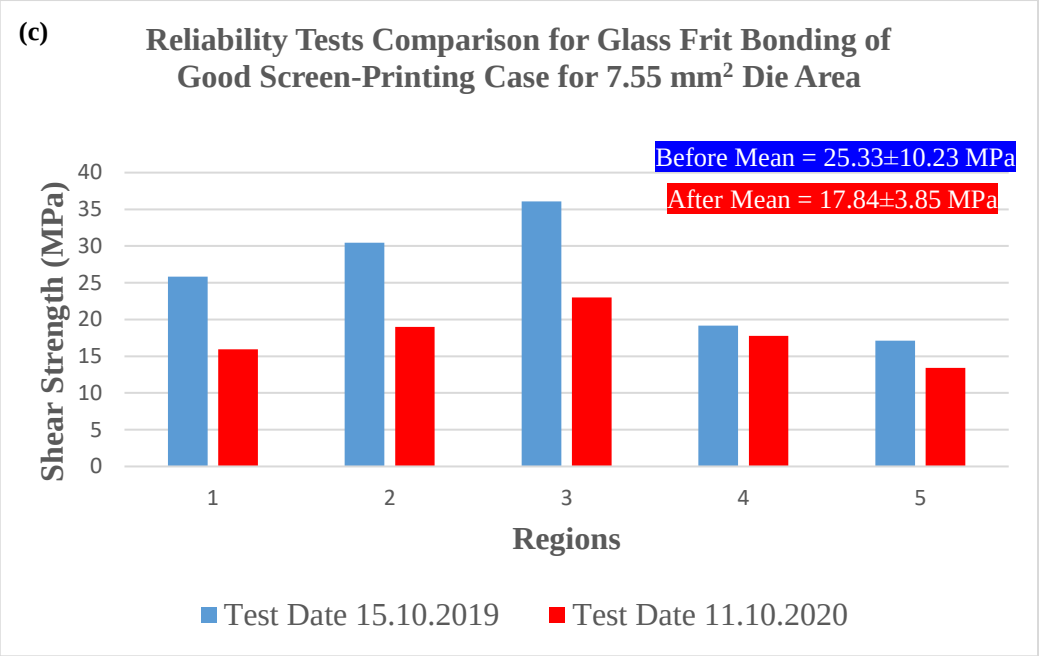
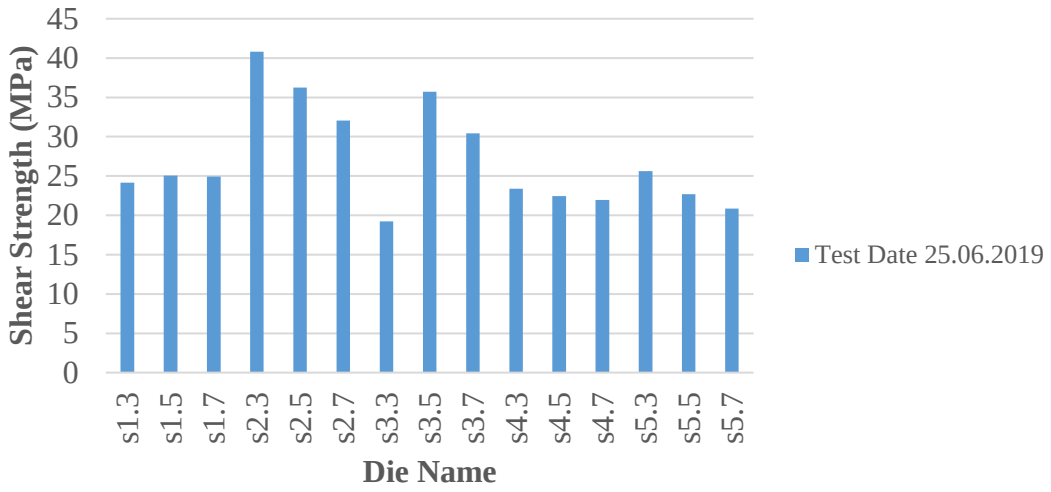


Figure 3.54. The applied shear tests to analyze the glass frit bonding quality after nearly one year later for good screen-printing case: (a) The plot showing shear strengths for tested fifteen dies on 25.10.2019, (b) The plot showing shear strengths for tested twenty-nine dies on 11.06.2020, and (c) comparison of them according to regions. Notice that for a single die, bonded area is calculated as 7.55 mm^2.

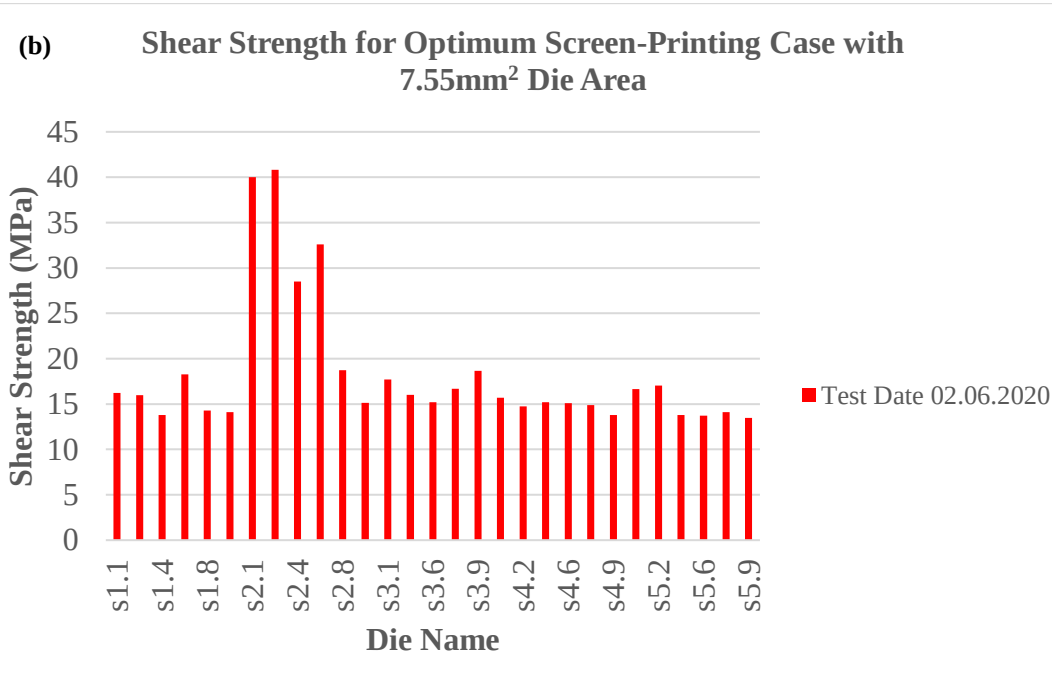
3.4.5.4.3 Shear Test Results for Optimum Screen-Printed Case with Grating Structures

After achieving the optimization in the screen-printing quality with dummy wafers for observing the real case; the grating structures are integrated to the cap wafer and alignment before screen-printing achieved successfully. As in the dummy wafer cases, to observe the glass frit bonding quality after dicing the wafers shear tests applied to them again from 5 regions. The related results could be found in Table 3.8-9 and Figure 3.55. The average shear strength for the test date of 25.06.2019 is calculated as 27.04±6.45 MPa and for the test date of 02.06.2020 it is calculated as 18.30±7.40 MPa.

(a)


Shear Strength for Optimum Screen-Printing Case with 7.55 mm² Die Area
Shear Strength (MPa)
45
40
35
30
25
20
15
10
5
0
s1.3
s1.5
s1.7
s2.3
s2.5
s2.7
s3.3
s3.5
s3.7
s4.3
s4.5
s4.7
s5.3
s5.5
s5.7
Die Name
Test Date 25.06.2019

(b)


Shear Strength for Optimum Screen-Printing Case with 7.55mm² Die Area
Shear Strength (MPa)
45
40
35
30
25
20
15
10
5
0
s1.1
s1.4
s1.8
s2.1
s2.4
s2.8
s3.1
s3.6
s3.9
s4.2
s4.6
s4.9
s5.2
s5.6
s5.9
Die Name
Test Date 02.06.2020

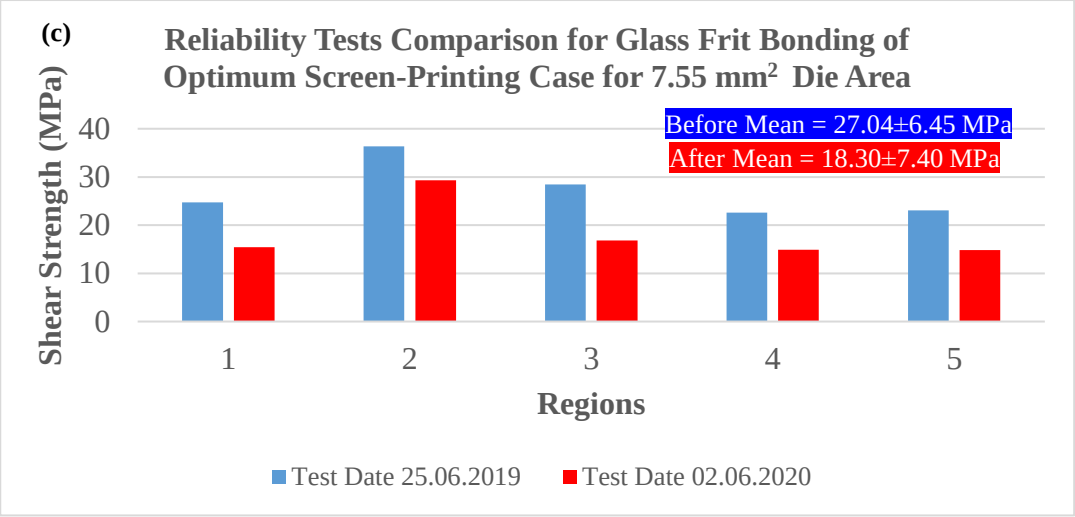


Figure 3.55. The applied shear tests to analyze the glass frit bonding quality after nearly one year later for good screen-printing case: (a) The plot showing shear strengths for tested fifteen dies on 25.06.2019, (b) The plot showing shear strengths for tested twenty-nine dies on 02.06.2020, and (c) comparison of them according to regions. Notice that for a single die, bonded area is calculated as 7.55 mm^2.

Table 3.8 Tabulated form of the 25.06.19 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
190625	**Left (Region 1)**	**s1.3**	182.47	24.17
		s1.5	189.04	25.04
		s1.7	188.14	24.92
	Middle (Region 2)	**s2.3**	308.01	40.80
		s2.5	273.61	36.24
		s2.7	242.1	32.07
	Right (Region 3)	**s3.3**	145.33	19.25
		s3.5	269.76	35.73
		s3.7	229.56	30.41
	Top (Region 4)	**s4.3**	176.69	23.40
		s4.5	169.42	22.44
		s4.7	165.9	21.97
	Bottom (Region 5)	**s5.3**	193.61	25.64
		s5.5	171.42	22.70
		s5.7	157.37	20.84

Table 3.9 Tabulated form of the 02.06.2020 shear test applied dies.

Test Date	Location	Die Name	Applied Max. Force (N)	Max. Shear Strength (MPa)
200602	**Left (Region 1)**	**s1.1**	122.4	16.21
		s1.2	120.77	15.99
		s1.4	104.12	13.79
		s1.6	137.86	18.26
		s1.8	107.71	14.27
		s1.9	106.52	14.11
	Middle (Region 2)	**s2.1**	302.03	40
		s2.2	308.02	40.8
		s2.4	215.1	28.49
		s2.6	246.09	32.59
		s2.8	141.46	18.74
		s2.9	114.16	15.12
	Right (Region 3)	**s3.1**	133.54	17.69
		s3.4	120.88	16.01
		s3.6	114.72	15.19
		s3.8	126.06	16.7
		s3.9	140.81	18.65
	Top (Region 4)	**s4.1**	118.62	15.71
		s4.2	111.41	14.76
		s4.4	114.72	15.19
		s4.6	113.97	15.09
		s4.8	112.24	14.87
		s4.9	104.18	13.8
	Bottom (Region 5)	**s5.1**	125.68	16.65
		s5.2	128.47	17.02
		s5.4	104.13	13.79
		s5.6	103.56	13.72
		s5.8	106.49	14.1
		s5.9	101.75	13.48

3.4.5.4.4 Glass Frit Bonding Shear Test Results Overall Comparisons and Long-Term Data Comparisons

After mentioning the effects of screen-printing quality and comparing the shear strengths of bad, good and optimum cases in terms of the long term data for about 1 years it would be better the compare all cases in the one plot and for the comparison for each cases the highest nine tested samples are selected (Figure 3.56). Needless to say, in the scope of this thesis study 8" wafers are studied, and all process steps performed in Turkey and for comparison previous studies done in METU MEMS Center is also integrated the plot for comparison. Notice that among the others "Previous Trials with 6" Wafers (Screen-Printing Performed Abroad)" entitled study is not belong to this thesis study, it is screen-printed abroad and cap wafer is processed in 6" wafer sizes; also instead of AR gratings AR coating is performed again abroad. Notice that for the comparison nine different dies are selected and those are the maximum ones among the others in their conditions.

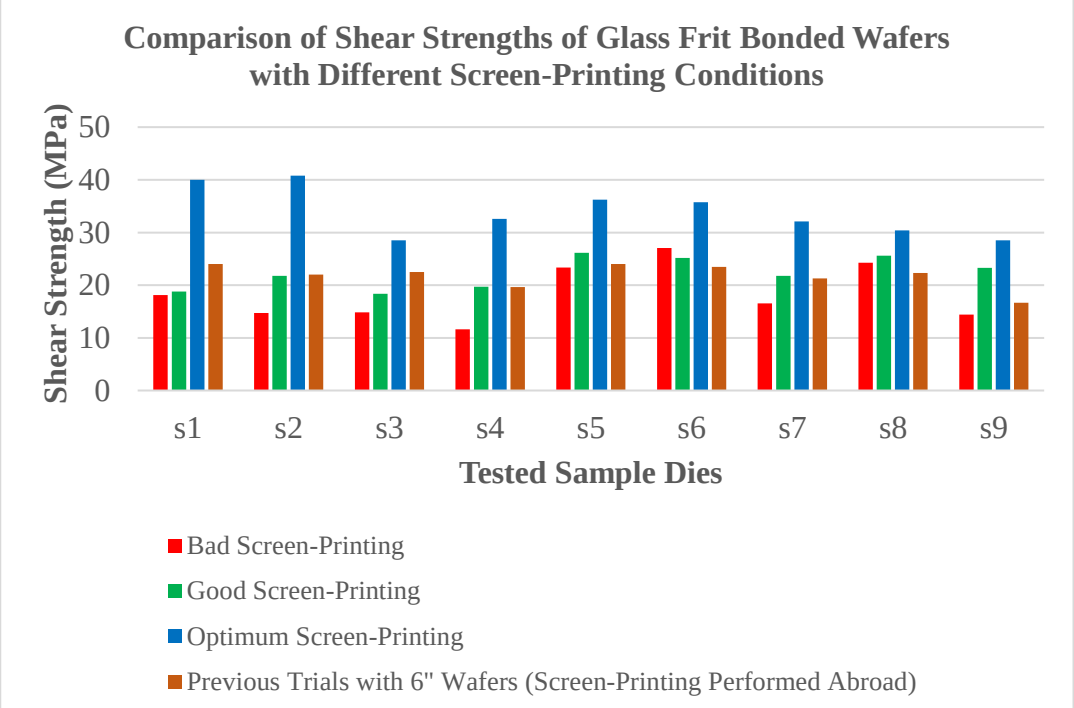


Figure 3.56. The overall glass frit bonding comparison in terms of screen-printing conditions and custom-made squeegee rubber.

For obtaining a reliable cap wafer one of the major parameters are long-term stability so with dummy cap wafers this situation also simulated (Figure 3.57); again “Test Date 21.04.2017” entitled study in the below figure does not belong to this thesis study just integrated the plot for comparison purposes. Also, there is one other thing to taken into consideration, the dummy wafers screen-printed in 2019 and in that date, there is only custom-made squeegee rubber option and original one is purchased in 2021 so it is assumed that real results will be much better.

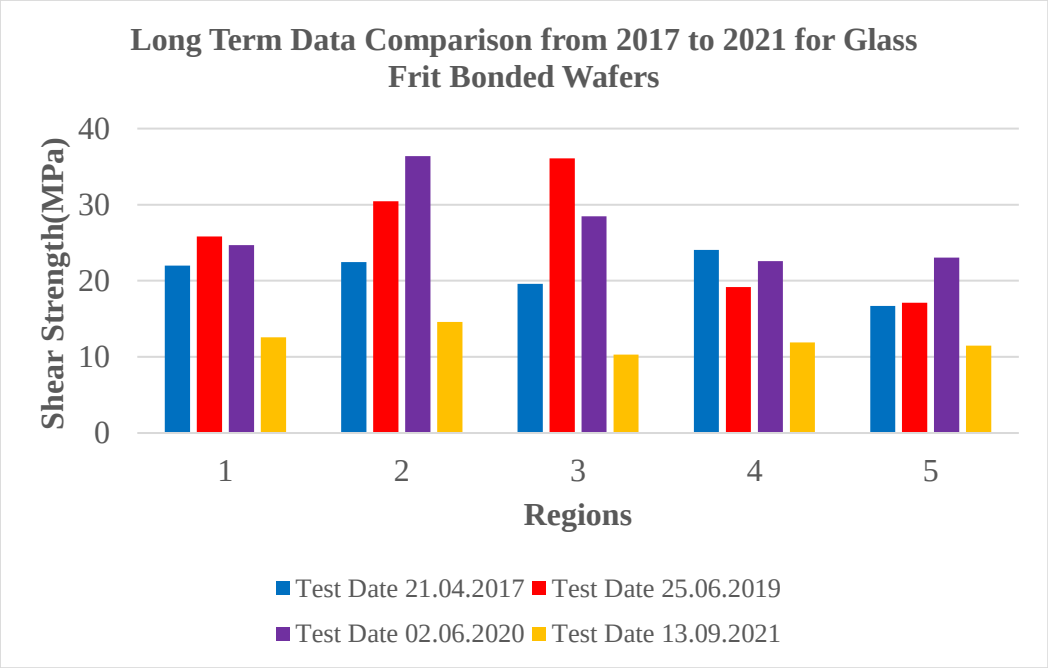


Figure 3.57. The comparison of shear test results of 5 regions in terms of long-term data comparison from 2017 to 2021.

After all the comparisons, it can be concluded that screen printing is important to achieve good and hermetically sealed bonding. In terms of shear tests, the best performance results are obtained as for 8” Glass Frit Bonded wafer maximum shear strength is 46.91MPa (for F_{max}= 354.15 N and Die Bonding Area = 7.55mm^2).

3.5 Thin Film Getters Integration to Offered Cap Wafer

Getters can be described as the way for lowering/decreasing the outgassing effects. For vacuum packaging, the getter absorbs free-floating gas molecules. Several MEMS devices such as resonators and bolometers work in vacuum environment and vacuum is necessary for improved performances. The unwanted gases dampen resonators, absorb light or radiation, or reduce tunneling efficiency. The getters improve device performance by dramatically reducing the concentrations of these unwanted gas molecules in the package [76]. Getters can be described as an efficient thin-film pump which is able to absorb the trapped gases or impurities inside the sealed packages. They are needed not only to achieve low package pressure but also keep the pressure stable inside a vacuum package [2]. Getter is implemented in the deep cavities as thin film with the help of shadow masks. Some of the common getter materials are titanium, tantalum, zirconium, yttrium, aluminum, or their alloys. Under this sub-heading firstly previous trials performed at METU MEMS Center is going to be mentioned and then the performed work in the scope of this wafer level packaging technology is going to be discussed.

3.5.1 Previous Works Performed at METU MEMS Center

In METU MEMS Center previously two different thin-film getters are tried. The first one is the Nanogetters^{TM} which is commercially available in the market by Integrated Sensing Systems (ISSYS) and the other is the custom-designed Ti based thin film getter; respectively with using stainless-steel shadow mask [2]. In self-aligned stainless-steel shadow mask approach (Figure 3.58) two main problems are reported. The first one is the alignment of the cap and shadow masks are done under optical microscope by tweezers unless high alignment accuracy is needed. Otherwise, a special and costly shadow mask alignment tool is required in order to provide alignment accuracy better than few micrometers. The second problem is the buckling of the stainless-steel shadow mask. This buckling may cause the deposition

of thin film getters on the unwanted regions unless a special fixture is designed to remove the buckling. The buckling of the shadow mask caused the deposition of thin films on the vertical feedthroughs and makes them electrically short.

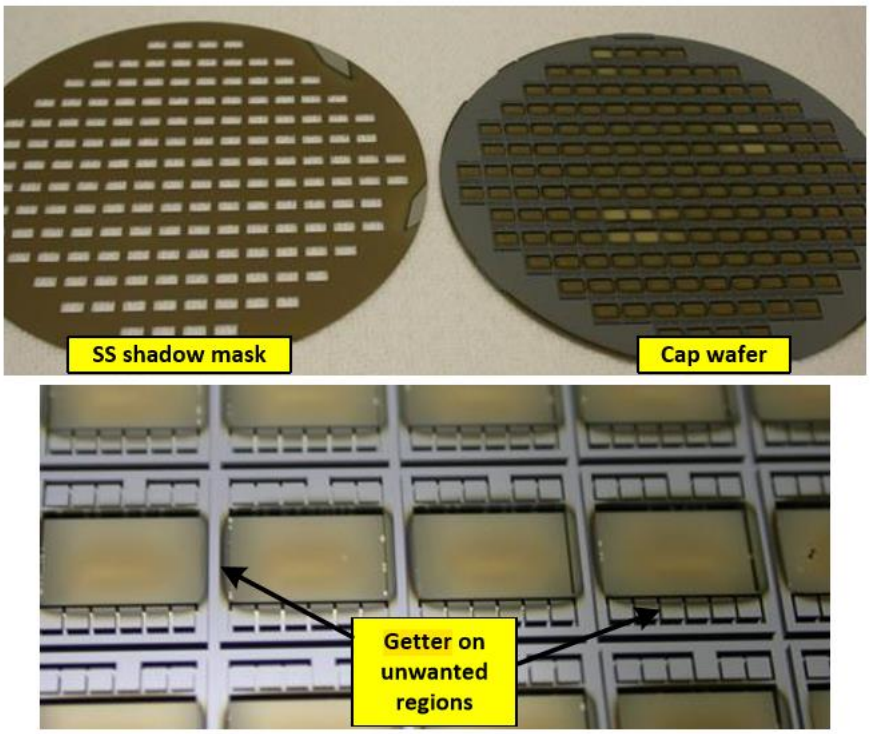


Figure 3.58. Pictures of the stainless-steel shadow mask and SOI cap wafer after the getter deposition. The buckling of the shadow mask caused the deposition of thin films on the vertical feedthroughs and makes them electrically short [2].

3.5.2 Production of Shadow Masks and Performed Experimental Works

In order to deposit Ti material to the cap wafer, shadow mask is necessary and in the scope of this thesis study firstly 6” size compatible shadow masks are designed and produced for dummy trials and after the optimization 8” size compatible shadow mask is designed and produced to adapt the developed cap wafer technology and the designed layout and produced 6” and 8” size compatible shadow masks are shown

in Figure 3.59. The production performed at ODAK PCB, İstanbul with 250µm thick Stainless Steel (SS-306) properties.

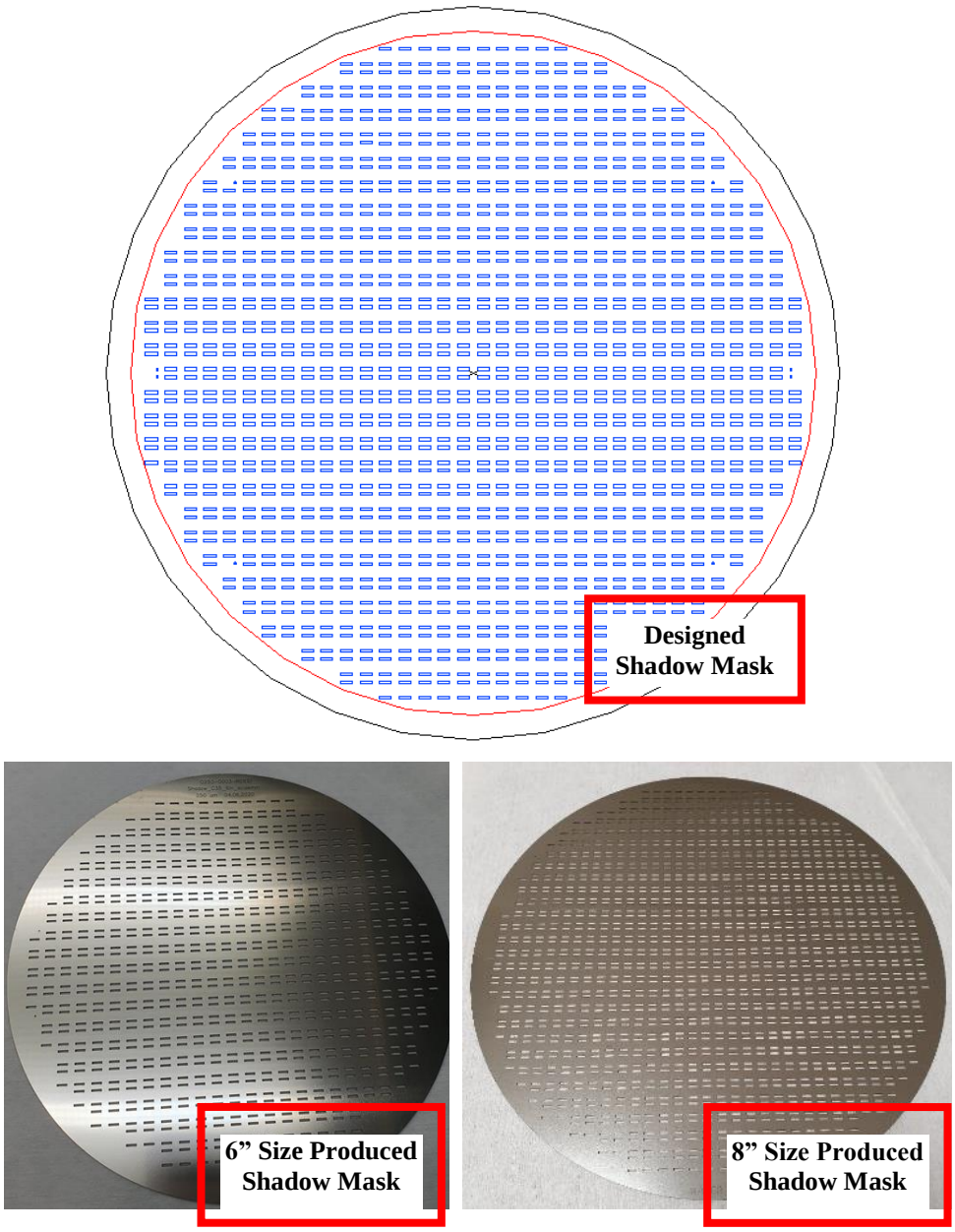
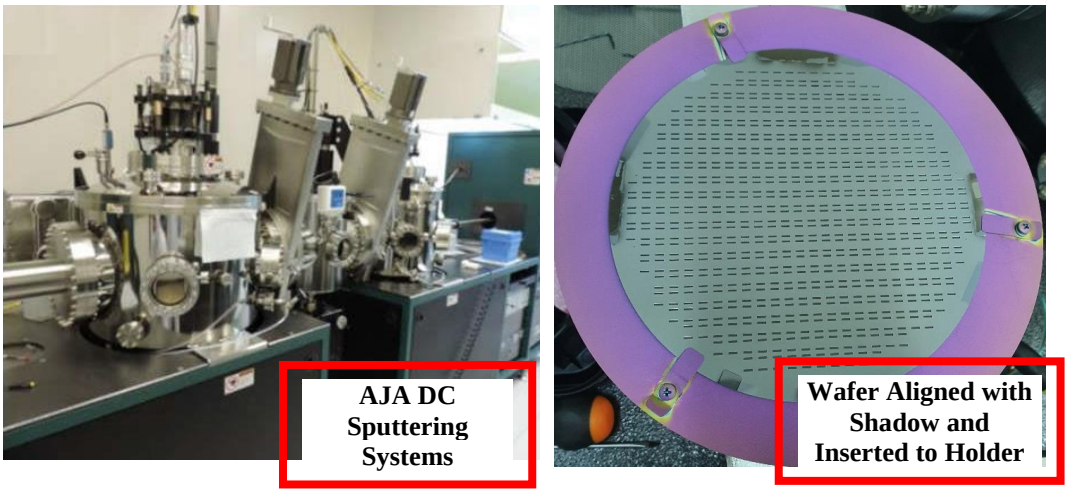


Figure 3.59. The representative 8” size Shadow mask layout compatible with the developed wafer level vacuum packaging technology for MEMS based long-wave infrared sensors.

After the shadow masks production is completed, to deposit the Ti getter material on the cap wafer experimental trials are started.

First getter material deposition trials are performed in AJA DC Sputtering Systems. In those trials unfortunately as reported in [2] similar problems are observed which are deposition of getter material to unwanted regions (over-diffusion) and bending of the shadow mask both in dummy and real cap wafers (Figure 3.60). Those problems may be because of several reasons. Firstly, different from previously produced shadow masks this shadow's thickness is 250µm although others are 500µm. Maybe due to that thickness differences over-diffusion problem can be observed and the buckling of the shadow mask is possible. Secondly, the 8" handle wafer + 6" cap wafer + 6" shadow mask stuck to each other with thermal tape and not all the stresses in the wafer are equal. And due to that problem, during the observation step it is seen that Ti getter over diffuse the unwanted regions. Finally, in AJA DC Sputtering systems the position of the wafer is downwards during the coating which may separate shadow mask and the wafers (either cap wafer or dummy bare wafer) a bit due to the gravity fall issue.



AJA DC Sputtering Systems

Wafer Aligned with Shadow and Inserted to Holder

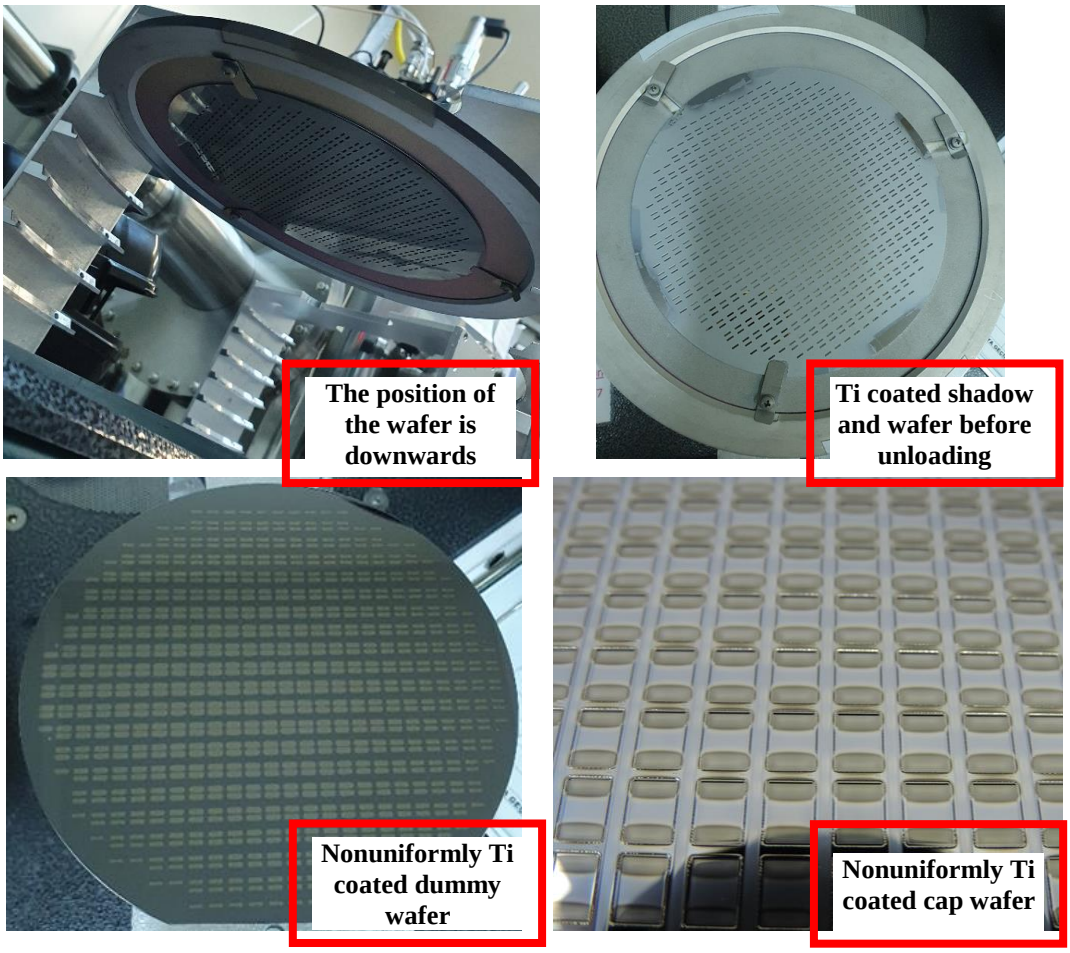
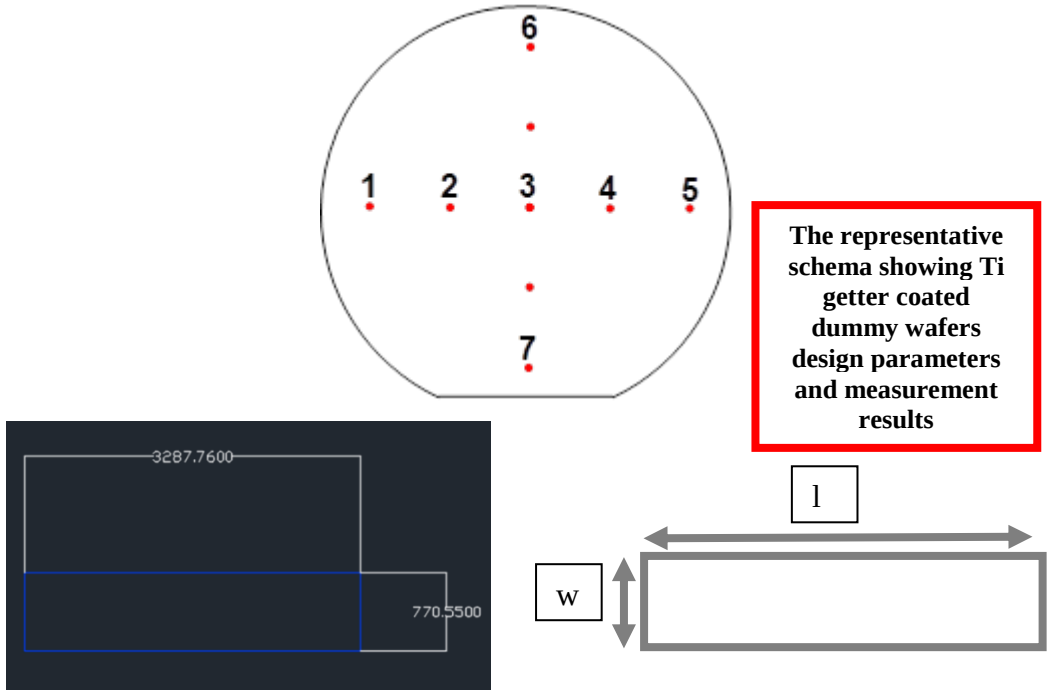


Figure 3.60. The images showing the aligned dummy/cap wafer and shadow mask inserted the AJA System for Ti coating.

After inspecting the wafers which are Ti coated in AJA DC Sputtering Systems in optical microscope, the dimensions of the Ti coated parts are measured in DEKTAK and Figure 3.61 represents the coated width and lengths.



Point	w (µm)	l (µm)
1	1250	3722
2	1670	4071
3	1755	4157
4	1645	3988
5	1300	3756
6	1765	4015
7	1615	3913
Mean	**1571**	**3946**

Figure 3.61. The representative schema for shadow masks Ti getter deposited parts.

Notice that although in layout dimensions for w and l are 770.5500 µm and 3287.76 µm; respectively mean of Dektak measurements for them are 1571 µm and 3986 µm; respectively. To conclude, bending of the shadow mask is obvious as can be seen the screenshots taken from left middle and right sides of the wafers in Figure 3.62.

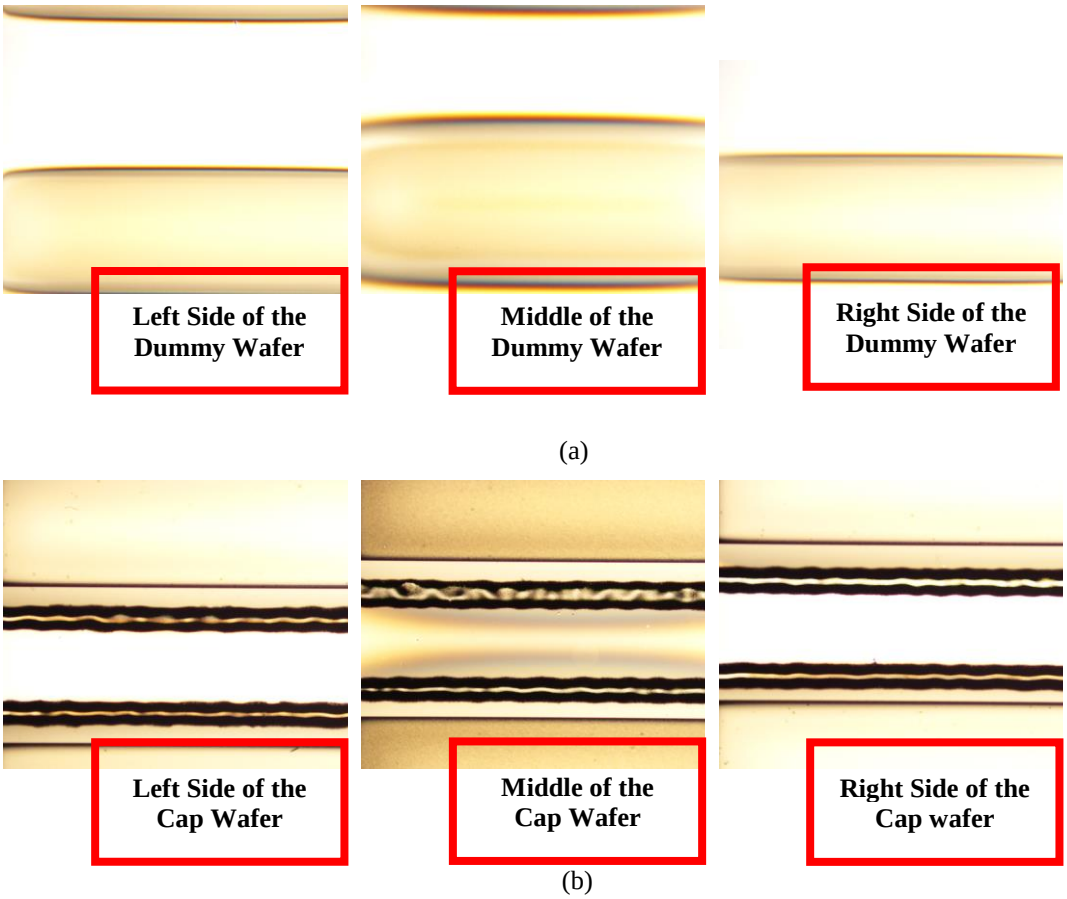


Figure 3.62. The images taken from left, middle and right sides of the (a) dummy wafer and (b) cap wafer for showing the bending problem of the shadow mask.

To make the exact comparison, both dummy wafers and cap wafers aligned with shadow mask (Figure 3.63) and inserted with same wafer holder for getter material Ti coating for this time BESTEC-II Sputtering Systems. BESTEC-II results are obviously better and due to coting position is to upwards it eliminates the over diffusion and bending problems (Figure 3.64). It seems for Ti getter deposition BESTEC-II would be chosen to eliminate all the problems (Figure 3.65).

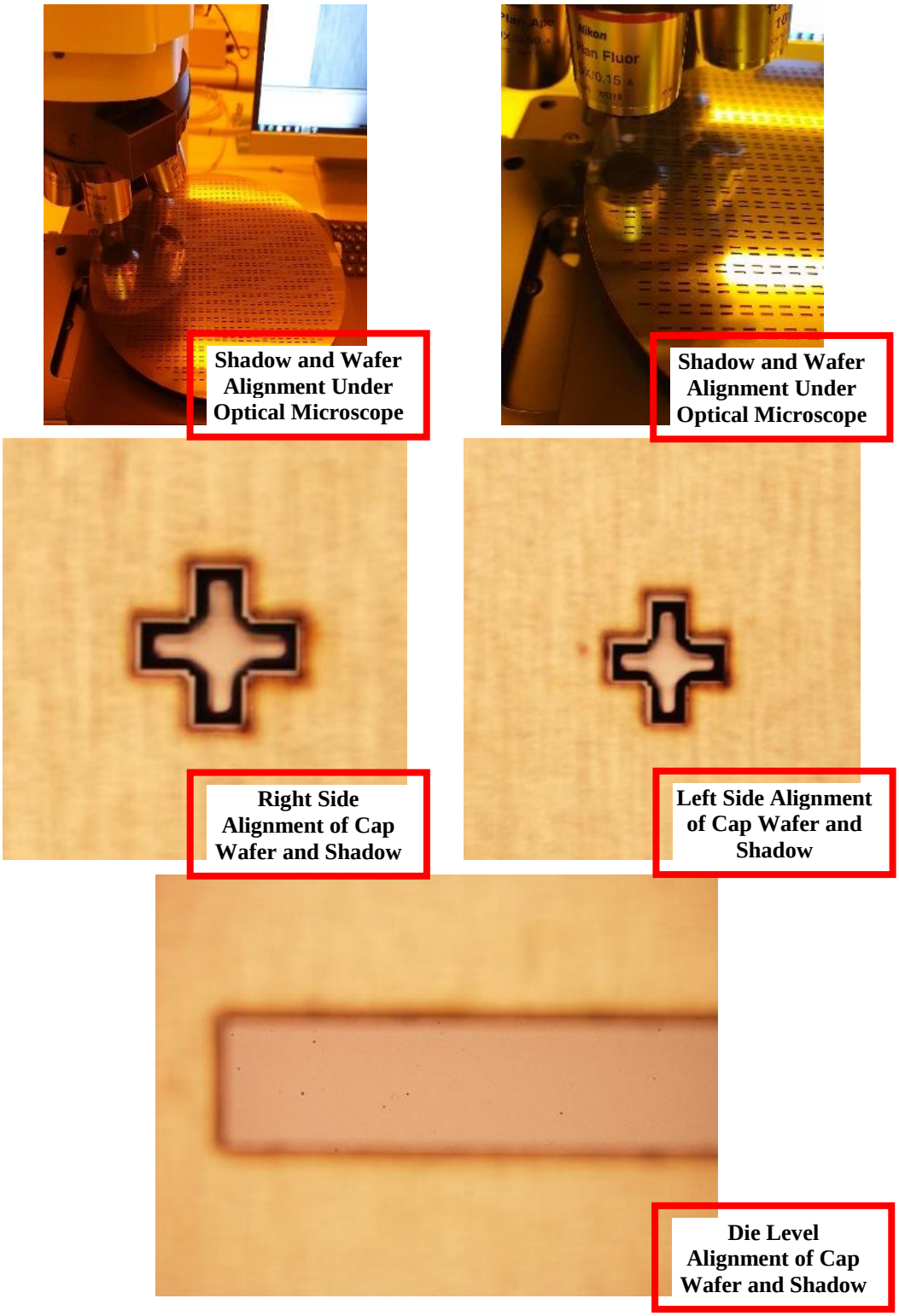


Figure 3.63. Alignment procedure pictures of the cap and shadow masks under the optical microscope.

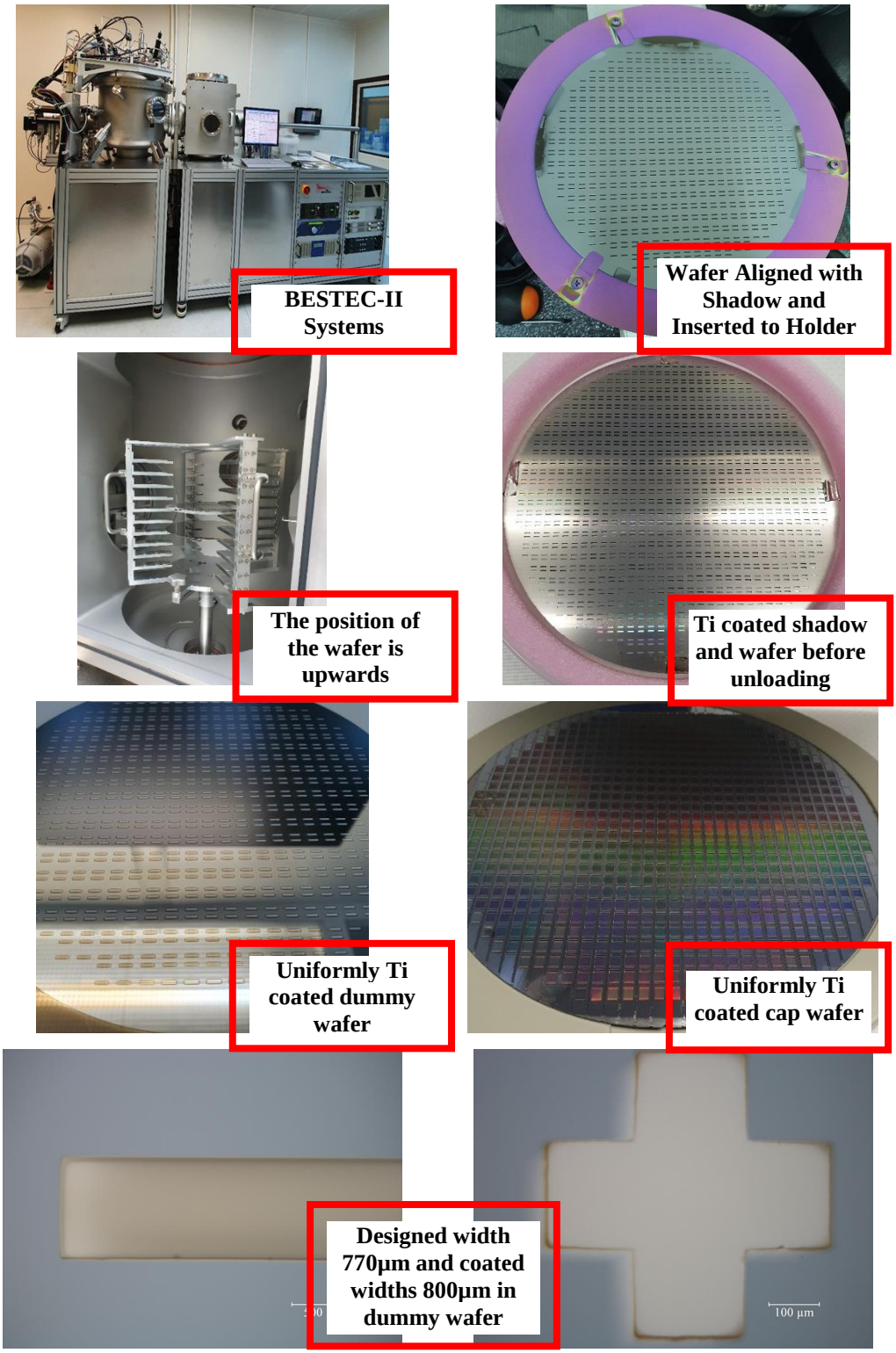
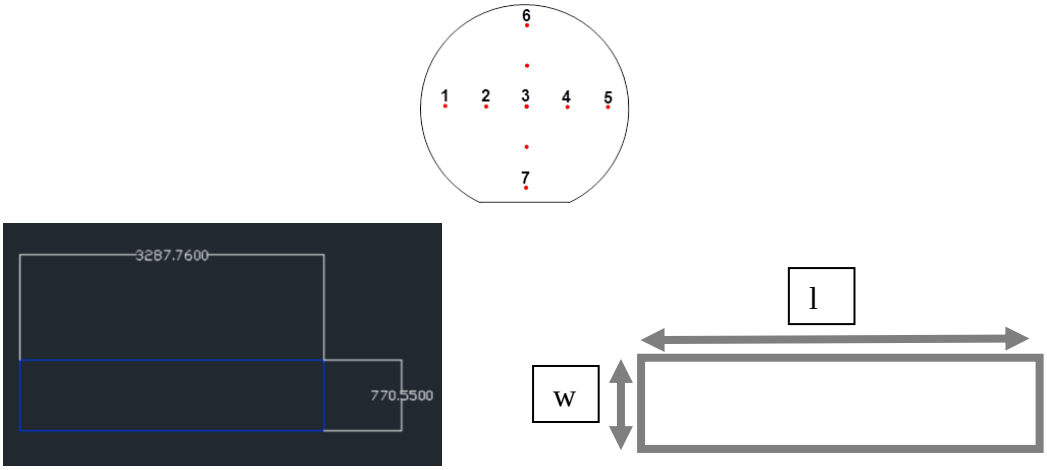


Figure 3.64. The images showing the aligned dummy/cap wafer and shadow mask inserted the BESTEC System for Ti coating.



Point	w (µm)	l (µm)
1	785	3292
2	770	3280
3	775	3280
4	770	3280
5	765	3283
6	778	3275
7	770	3288
Mean	**773**	**3283**

Figure 3.65. The representative schema for shadow masks Ti getter deposited parts in BESTEC. Notice that in layout dimensions for w and l are 770.5500 µm and 3287.76 µm; respectively and measured results' mean of Dektak measurements for them are 773 µm and 3283 µm; respectively**.**

To conclude, when we compare AJA and BESTEC; experimental results with same holder and same shadow showed that BESTEC results are obviously better. Last but not least, at the end of the getter deposition step offered cap wafer stack's fabrication step completed and prepared cap wafers are ready for glass frit bonding.

3.6 Fabrication of In-Situ Vacuum Sensors and Faced Problems

After searching the literature, it is decided to adapt resistive type Pirani gauges as in the study of [64] and variation are designed and fabricated in the scope of this study by using again METU MEMS Center clean room facilities. It is decided to integrate

Pirani vacuum sensors to Silicon test wafers (Wafer C). The offered cap wafer technology is planned to be CMOS compatible so the fabricated device wafer; Wafer C is also produced with CMOS compatible production techniques. There are several problems coming from mask/reticle production, lithography (Figure 3.66) or wet/dry etching (Figure 3.67) steps even though all the process steps are tried to be optimized. Needless to say, one process step must not affect or damage the previous or next ones and for metal layers good adhesion and satisfactory lithography is significant. The selection of the sacrificial layer is the other concern that must be taken into consideration not only for simple process but also for easy striping after the end of the fabrication. Topological effects are the other parameter effecting the yield especially for the critical dimensions; for instance, the topology caused by the thick layers may prevent the fine lithography or not able to etch the structures with small dimensions. The support arms are constructed by using the metal layers, so the used metal have not only low thermal conductivity but also high electrical conductivity. The metal support arms merged with the active material so TCR value of the active material must be high at the same time noise must be as low as possible. Finally, arm body nitride/structural layer must be stress free to avoid buckling problem (Figure 3.68 and 3.69).

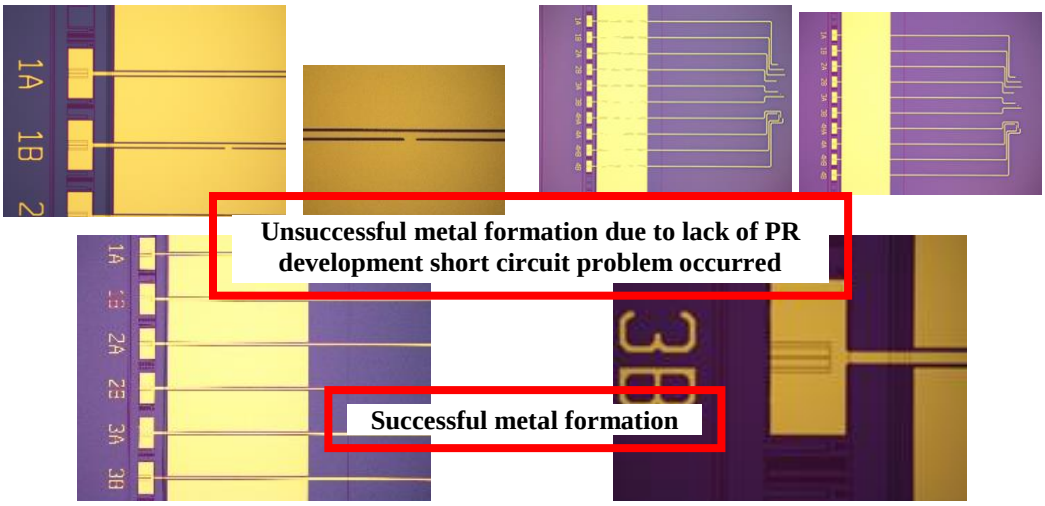


Figure 3.66. Comparison of metal formations to show the importance of the successful lithography.

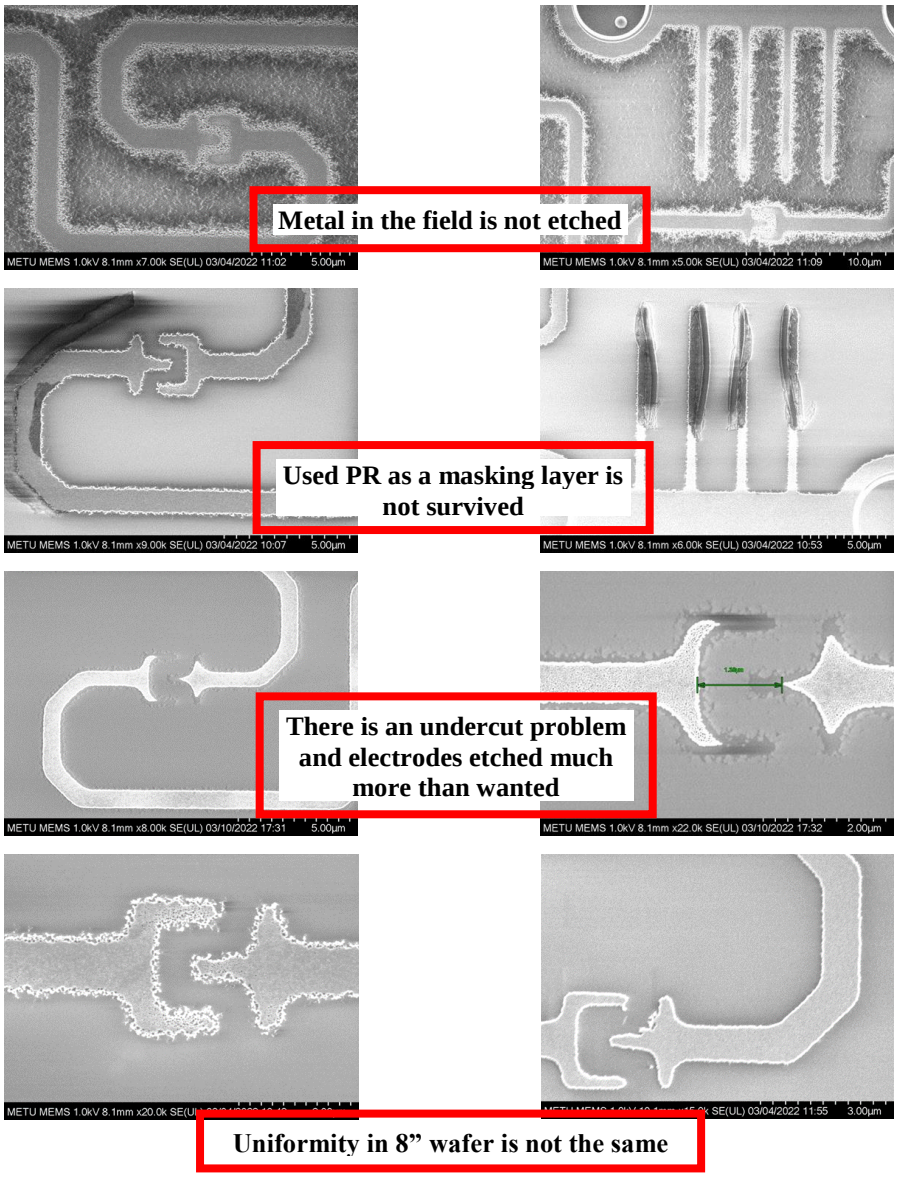


Figure 3.67. Problems faced during the wet and dry etching of the arms.

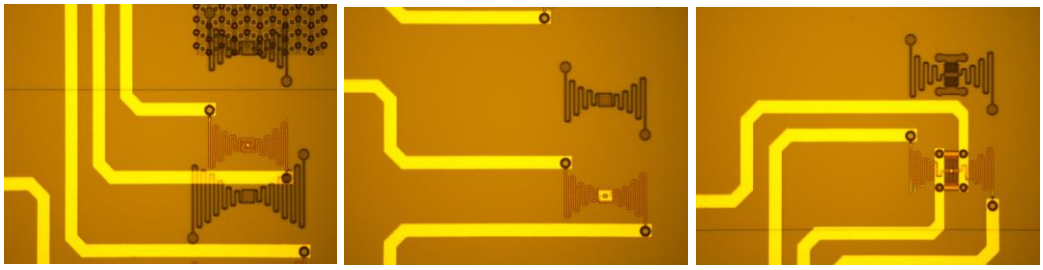


Figure 3.68. Due to topography caused by the thick layer’s stepper do not read alignment marks correctly and there is a shift problem in 88µm in +y direction in arm body nitride lithography step.

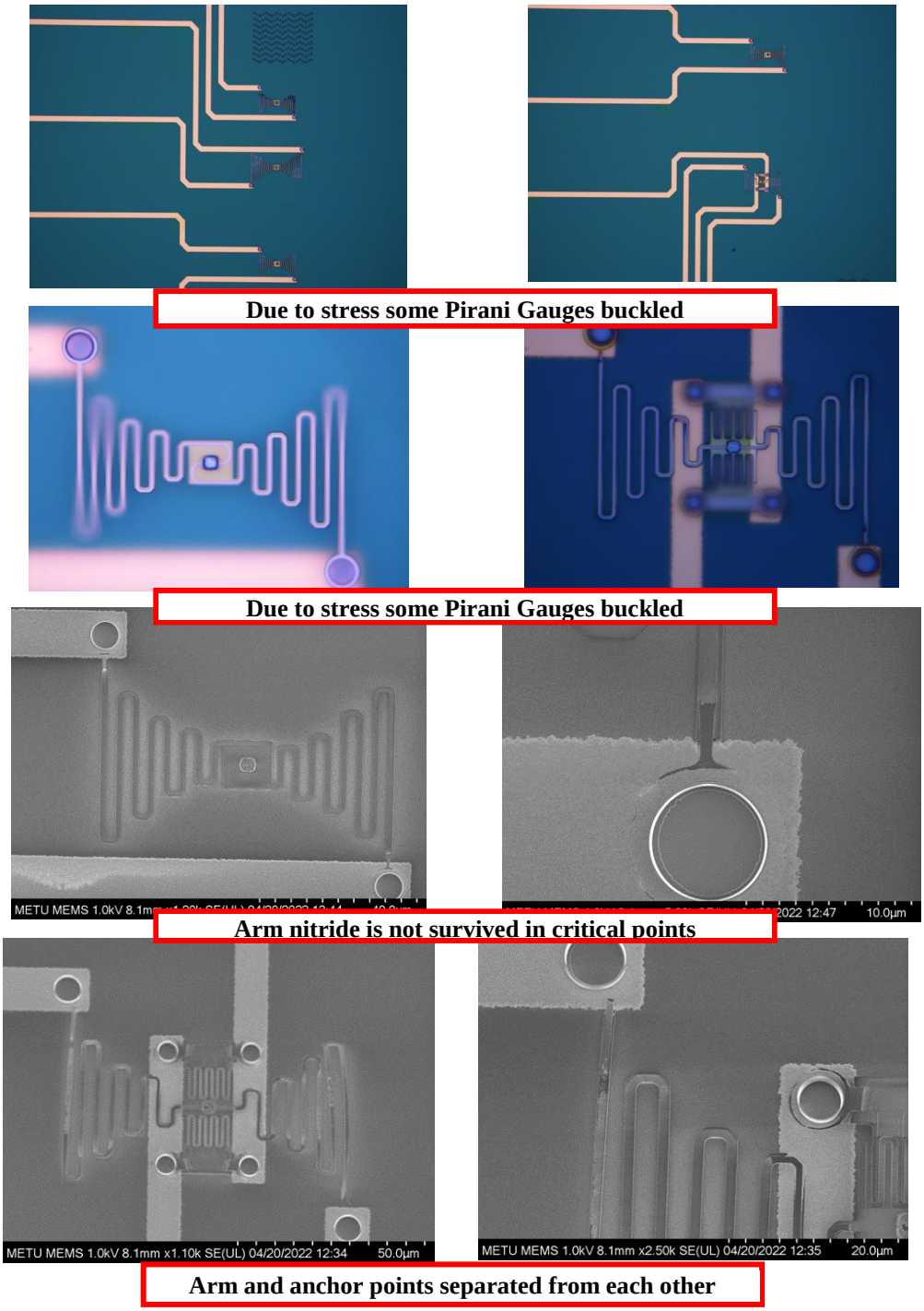


Figure 3.69. Due to topography arm body nitride in anchor points is not OK and due to stress and mechanical buckling connections from arm to anchor is lost in some dies after wafer level release step.

3.6.1 Fabrication Results

After trying to solve the problems mentioned in previous section four different Pirani vacuum gauges are fabricated and as a device wafer two 8” Wafer C (WC3 and WC5) is processed using the surface micromachined MEMS technology. After the fabrication, next step is the etching of the sacrificial layer in order to thermally isolate the vacuum sensors. Figure 3.70 shows the SEM views of the fabricated Pirani gauges. As a result, it can be stated that in-situ vacuum sensors for monitoring the cap wafers are successfully fabricated and ready to be tested.

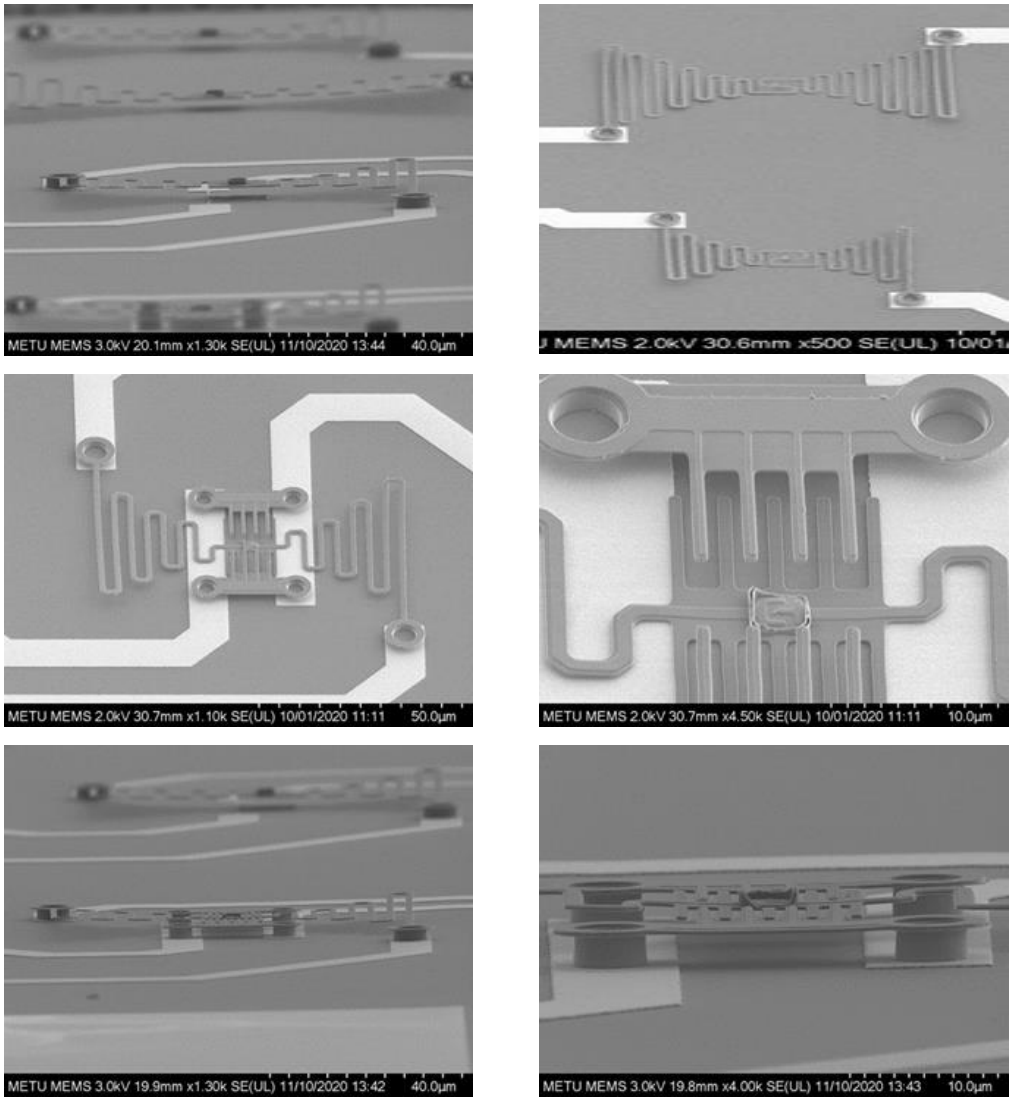


Figure 3.70. The SEM images of the 4 different type fabricated vacuum sensors.

3.7 Wafer Level Hermetic Encapsulation of Sensor Wafer with Offered Cap Wafer Technology

After optimizing the fabrication of cap stack and sensor wafer separately; the hermetic encapsulation of the fabricated sensor wafer is achieved by applying glass frit bonding to the offered cap wafer technology. The photograph of the offered cap wafer (Wafer A+B stack), device wafer with characterized Pirani gauges (Wafer C), and the aligned bonding pair for the glass frit bonding can be seen in Figure 3.71.

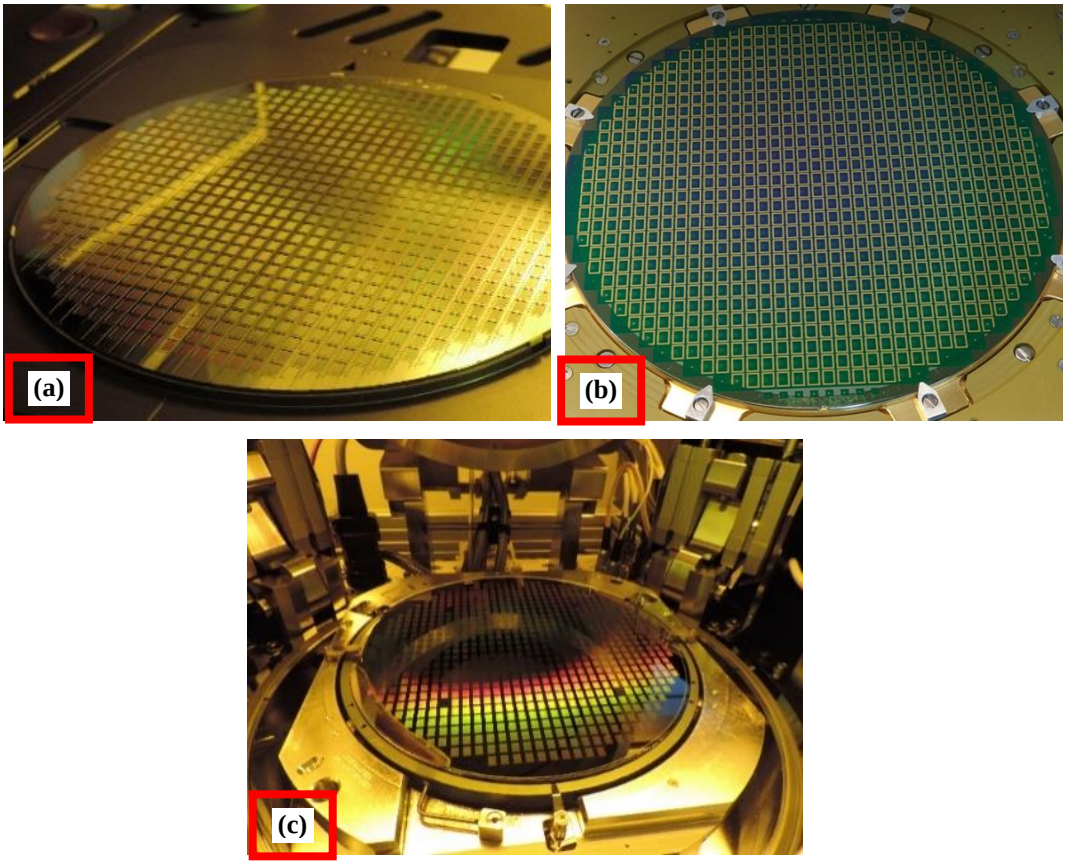


Figure 3.71. (a) Cap wafer, (b) device wafer before the bonding, and (c) the wafers on the bond chuck after bonding alignment.

Bonding uniformity of the edge and center sides are analyzed again in SAM (Figure 3.72 (a-c)). Then, for being sure whether package damage or not wafer level pad removal is done (Figure 3.72 (d-e)) and after singulation shear tests applied.

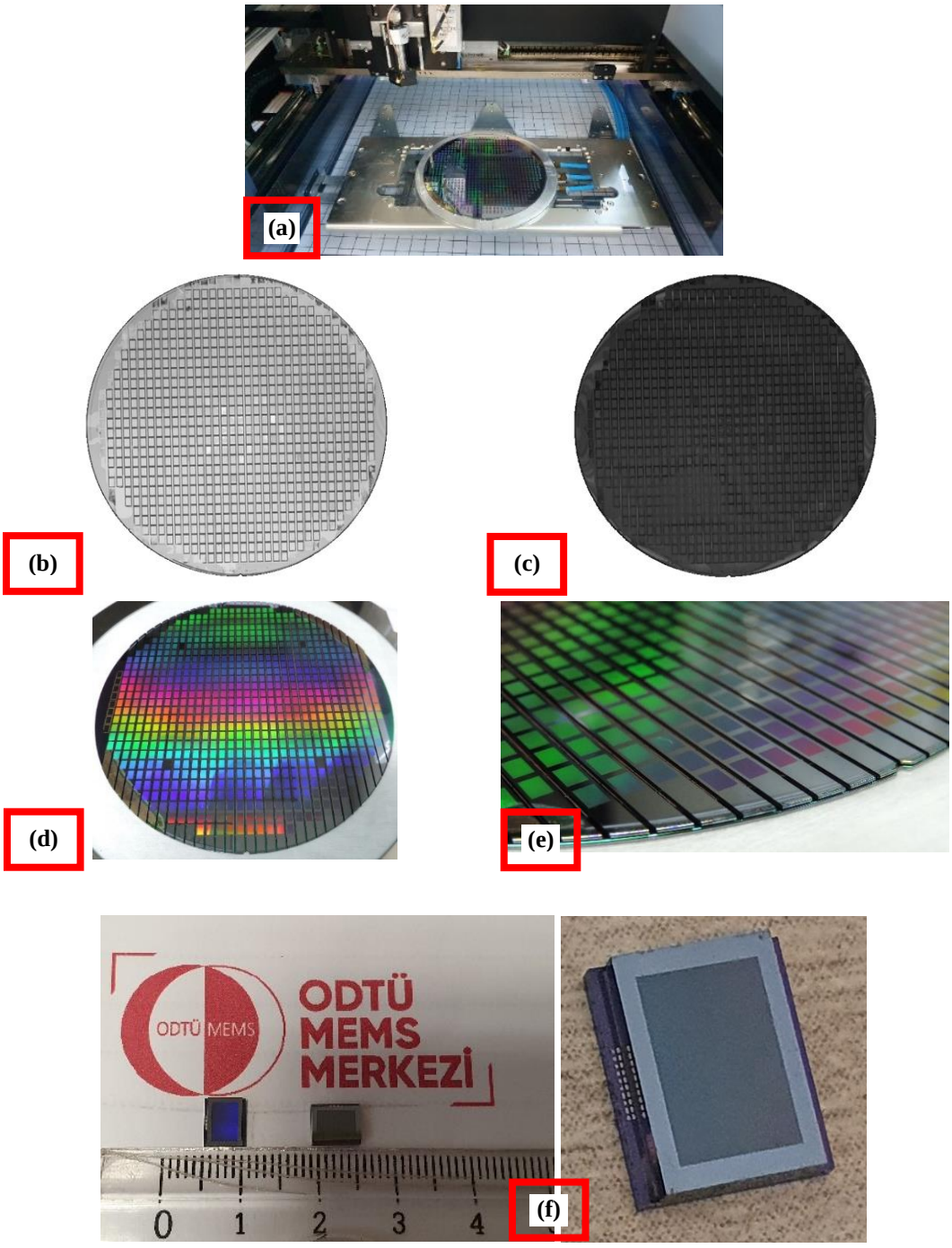


Figure 3.72. The SAM inspection results (a-c) of WC2 after wafer level glass frit bonded with one of the offered cap wafers to understand the bonding quality, packaged wafers images after pad reveal operation (d-e) and die level singulation (f).

As can be seen due to the layer muchness it is difficult to exactly understand the hermeticity or package quality from the SAM analyzes (Figure 3.72 (b) & (c)). When SAM images are inspected in some areas focus is lost this may be because of the low threshold of the transducer head in those regions or do to some micro cracks occurred in the cap side during the grinding step hermeticity is lost and water diffused inside the packages. As a second check point, wafer is applied pad reveal and as can be seen from the images (Figure 3.72 (d) & (e)) it is not separated so mechanical strength seems good. But to be sure as a third check point, after a successful singulation to die level, shear tests are also conducted. Shear tests applied again from 5 different regions same as detailed in section "3.4.5.4 Destructive Shear Tests". For the shear tests, 20 dies are tested and according to shear test results average is 18.7 MPa. As it was remembered according to military standard MIL- STD 883 the minimum shear strength value is 6MPa for the microelectronic packages and our packages are 3 times higher. Also, it would be better to mention that unfortunately the Ferro Pb-based frits expire date was 05/2019, due to cost issues instead of new order we continued to use those ones. Besides, when shear test applied and broken pieces are inspected in optic microscope and SEM, it is observed that glass frit and gold have an interaction (Figure 3.73 (a) due to the high bonding temperatures (440℃). This interaction may cause gold to lose its conductivity. Unfortunately, In Wafer C case for low-cost concerns we do not use a passivation layer between the gold and glass frit; and it is observed there are some damages on feedthrough lines (Figure 3.73 (b)) but for a quick check short tests are applied, and it satisfied (2- 3 Ω measured). Last but not least, the metal lines in Wafer Cs are fabricated by sputtered TiW/Au. The sputtered TiW/Au includes high amount of Argon gas which getter is not able to absorb. Therefore, the outgassed Argon during the packaging process may increase the pressure levels inside the sensors/device wafers. The overall SEM images of the offered cap wafer technology could be found in Figure 3.74.

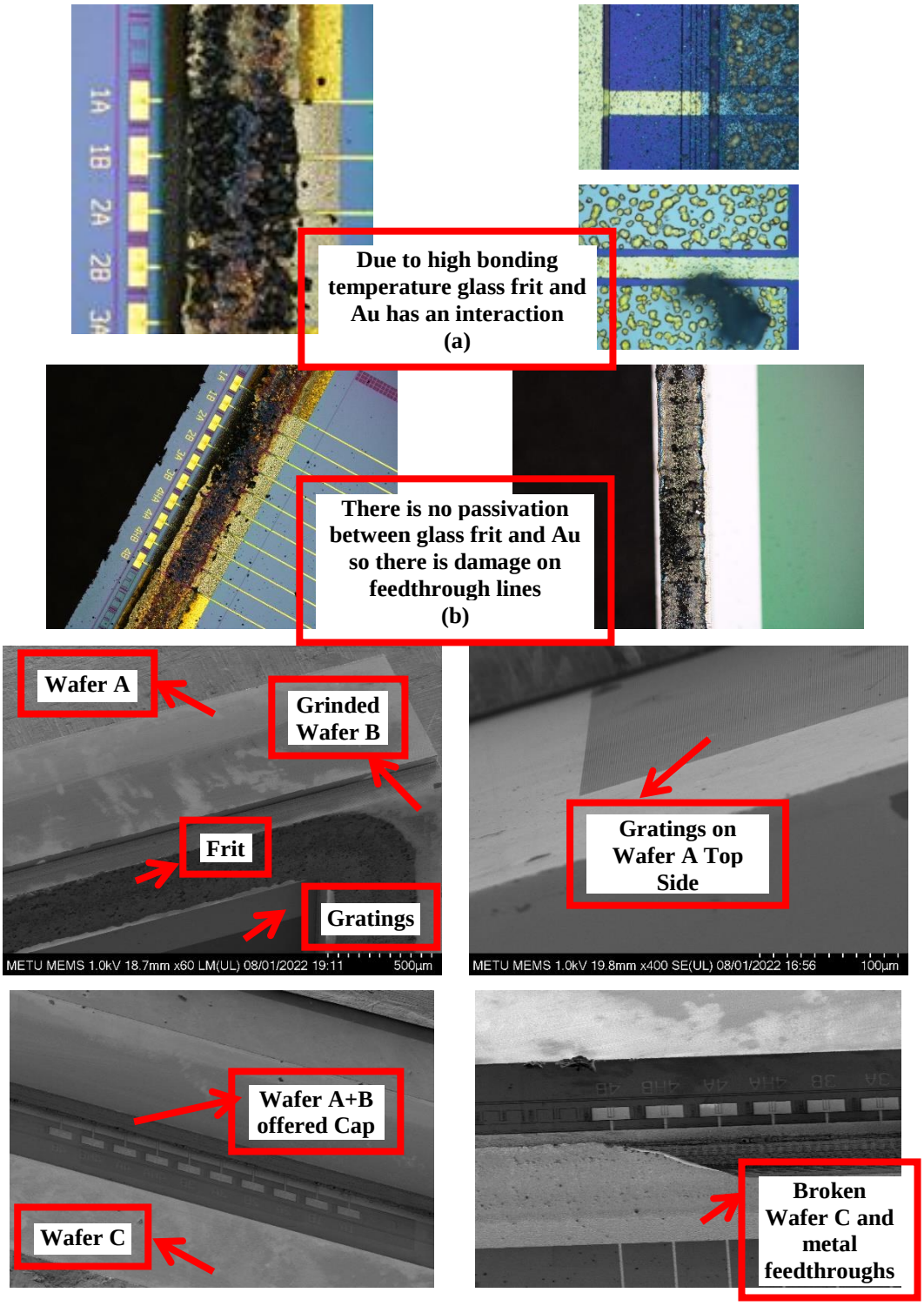


Figure 3.73. Optic microscope images of shear test applied and broken pieces to show (a) glass frit and Au interaction, and (b) damage on the Au feedthrough lines, and (c) and SEM images.

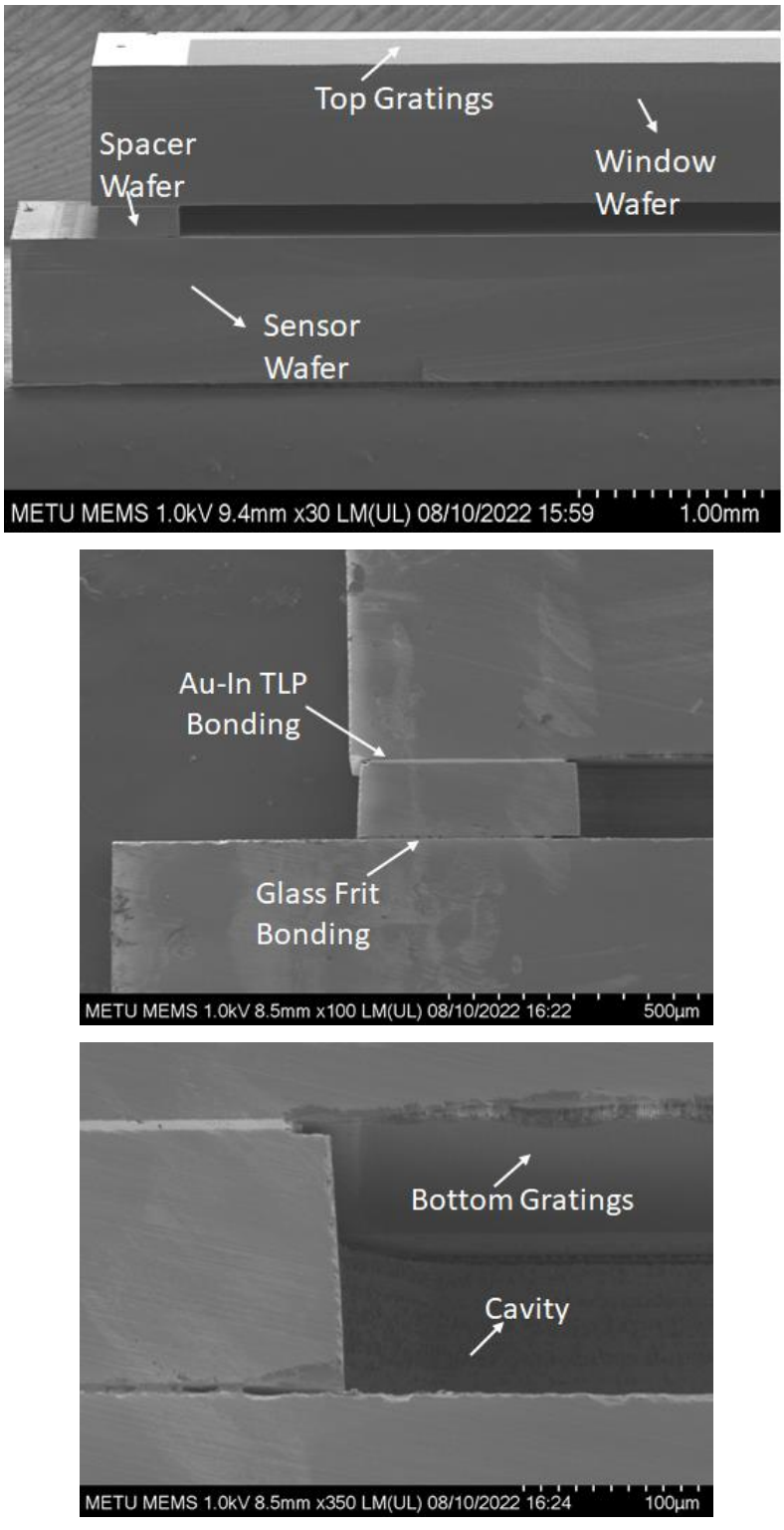


Figure 3.74. SEM images of overall cap wafer technology after wafer level vacuum packaging

CHAPTER 4

TEST RESULTS AND DISCUSSIONS

In wafer level packaging technology, after completing the cap wafers' fabrication step hermeticity and stability in terms of reliability and repeatability becomes the major concerns. When literature is searched there are various hermeticity test methods for applying typical MEMS devices with cavity volumes. In [77], MEMS leak detection methods are reviewed and they can be listed as Helium fine leak and gross bubble tests; through hole test; radio-isotope testing; Raman spectroscopy; copper test patterns; FTIR testing; thermal conductance measurement; cap deflection measurement; Quality-factor testing; and cumulative helium leak detection. These listed testing methods can be categorized either destructive/nondestructive or external/in-situ test methods. Among the others copper test patterns; thermal conductance and Q-factor testing methods are in-situ test methods. Also, although major external test methods are non-destructive; cap deflection and through hole test methods are destructive. In the scope of this work three different methods are applied for monitoring the cap wafers which are He-leak tests, cap deflection and thermal conduction measurement with the help of fabricated Pirani gauge based vacuum pressure sensors.

This chapter presents the vacuum check of the offered technology after wafer level packaging with Wafer C with (totally 2 device wafers are fabricated) and without (totally 8 wafers) vacuum sensors in details by the used three different methods which are He-leak tests (Section 4.1), cap deflection (Section 4.2) and in-situ vacuum sensors; Pirani gauges (Section 4.3) with their theory in detail.

4.1 He-Leak Tests

In MEMS industry, the most commonly preferred test methods are helium fine leak and gross bubble tests which are described in the Military Standards as MIL- STD- 883 TM 1014 and MIL-STD-750 TM 1071 [78]. The working principle is like that firstly the package is placed in an environment including He atoms for a period of time. Secondly, the package is transferred into the He-leak testing chamber and left alone for dwell time. Finally, in the chamber He gas leaks out from the package is measured by using the leak detector according to MIL-STD-883E standards as can be seen in Table 4.1. So briefly, it is the technique of He mass spectrometer used for measuring the amount leaking out of the package.

Table 4.1 MIL-STD-883E Helium Bomb time-pressure requirements as a function of cavity volume [78].

Volume of package (V) in cm^3	Bomb condition			R_1 Reject limit (atm cc/s He)
	Psia ±2	Minimum exposure time hours (t_1)	Maximum dwell hours (t_2)	
<0.05	75	2	1	5×10^{-8}
≥0.05 - <0.5	75	4	1	5×10^{-8}
≥0.5 - <1.0	45	2	1	1×10^{-7}
≥1.0 - <10.0	45	5	1	5×10^{-8}
≥10.0 - <20.0	45	10	1	5×10^{-8}

He-Leak tests have some pros and cons. Firstly, it is easily applicable to package and does not destroy the package. Secondly, there is no need to integrate sensor inside the package for in-situ tests. These can be the major advantages of the He-Leak Test method whereas there is external special equipment requirement makes the method costly. Also, unfortunately this method does not give any information about the vacuum values inside the package. Finally, leak detector has limitations; it is not applicable for ultra-small dimensions and typically minimum detectable leak rate is approximately 10^{-11}atm.cm^3.s^{-1} [77].

For the offered cap wafer technology, the hermeticity monitoring firstly characterized by He-leak tests; after applying glass-frit bonding and dicing the

packaged dies. As it was remembered, the 200µm (for standard case after grinding the stack) and 400µm (for thin wafer case to eliminate grinding step) deep cavities with x≈3500µm and y≈5200µm have been fabricated in DRIE previously on cap wafers to obtain a vacuum cavity after the bonding and integrating the gratings inside; so the package volume calculation for the one die is as shown in Equation 4.1:

$$DRIE\ Cavity\ Opening\ Area = 0.35cm * 0.52cm = 0.182cm^2 \qquad (4.1)$$

For 200µm deep cavities volume of the package is calculated as in Equation 4.2:

$$Volume\ of\ the\ Package\ 1 = 0.35cm * 0.52cm * 0.02cm = 0.00364cm^3 \quad (4.2)$$

$$Volume\ of\ the\ Package\ 1 = 3.64\text{x}10^{-3}\ cm^3$$

Similarly, for 400µm deep cavities volume of the package is calculated as in Equation 4.3:

$$Volume\ of\ the\ Package\ 2 = 0.35cm * 0.52cm * 0.04cm = 0.00728cm^3 \quad (4.3)$$

$$Volume\ of\ the\ Package\ 2 = 7.28\text{x}10^{-3}\ cm^3$$

After the calculation of the package volumes for two different cavity deeps, the used equipment available in METU MEMS Center is illustrated in Figure 4.1.

Figure 4.1. The pictures of He-Leak testing setup used in METU MEMS Center.

After the calculation of the package volumes for two different cavity deeps, according to defined leak test parameters in the MIL-STD (Table 4.1) He bombardment was applied by using pressure vessel at 75 psi for 16 hours. After that dies were placed to He-leak test chamber and after vacuumed the test detector read $0.1x10^{-9}$ $atm.cc/sec$. Although this method has some limitations on testing the hermeticity of ultra-low volumes, it is still applicable for package volumes higher than $2.36x10^{-3}$ cm^3 [79]. To be sure, bonded and diced piece but this time instead of a single die including 35 dies are tested (Figure 4.2). Testing procedure is the same, the only difference is this time instead of ultra-low package volume the total package volume which is 0.1456 cm^3 is in the range of the standard. In He-leak test chamber, the test detector read $0.1x10^{-9}$ $atm.cc/sec$. Notice that these results are for 400µm thin Wafer B case; so similar procedure is applied for grinded case and although in grinded case there is some leaks, they are less than the rejection limit shown in Table 4.1 MIL-STD-883E criteria. In grinded case, again there are 4 different test groups and read values according to test detector are $3.1x10^{-8}$, $2.4x10^{-8}$, $2.2x10^{-8}$, $1.9x10^{-8}$ $atm.cc/sec$ while the reject limit is $5x10^{-8}$ $atm.cc/sec$. Therefore, it can be concluded that offered cap wafer technology pass the He-Leak Tests according to MIL-STD 883E.

Figure 4.2. The pictures of higher package volume pieces including 35 dies applied He-leak tests; aim is to be sure and compare with ultra-low volumes.

4.2 Cap Deflection Tests

Cap deflection is the other external and destructive method for monitoring the leakage. This method based on the interferometry to monitor the pressure driven deflection of a package's thinned cap side. By knowing the dimensions and mechanical properties of the cavity opened cap wafer; and by monitoring the deflection over time pressure inside the package can be calculated. Figure 4.3 shows the representative images of the packaged die before/after thinning and representative image of the cap deflection.

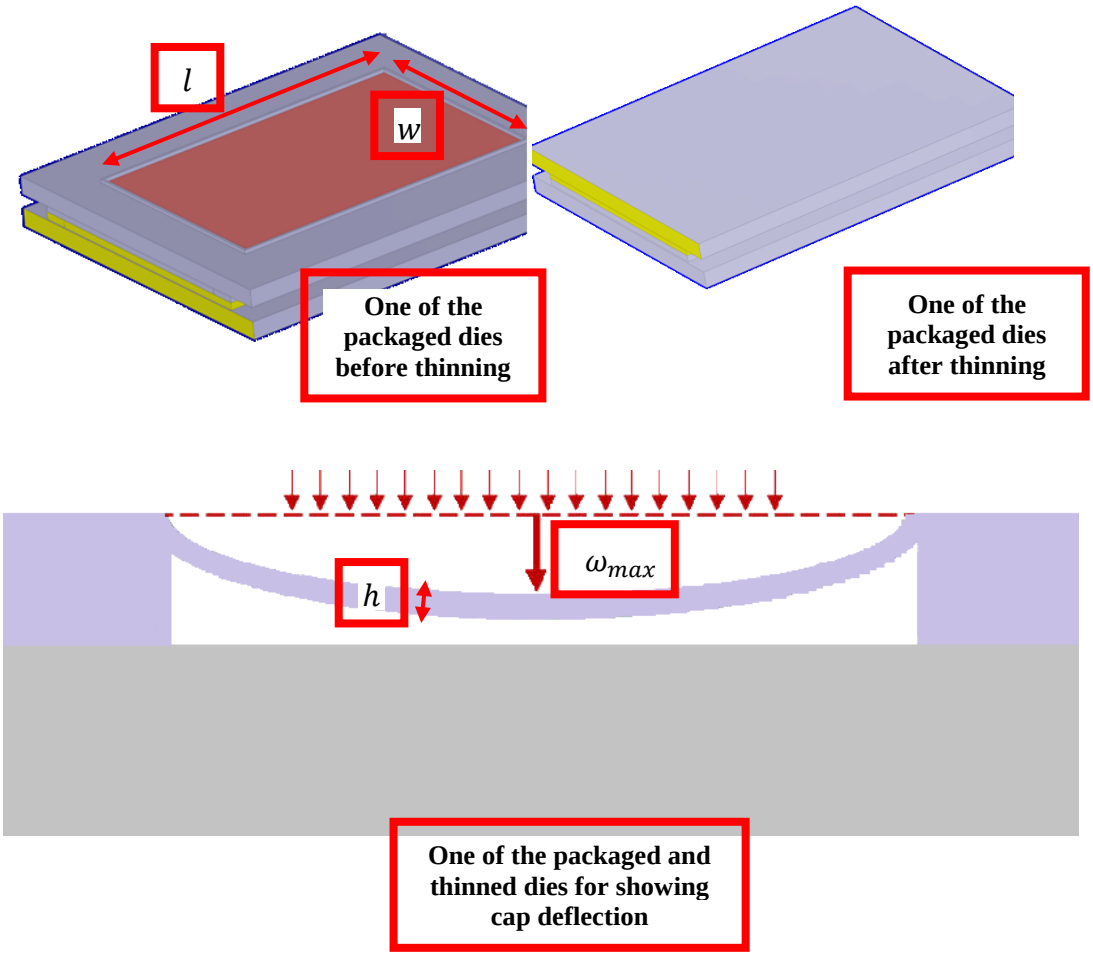


Figure 4.3. The representative images for showing the cap deflection phenomena because of the vacuum inside the package cavity.

The thinned package in terms of cap deflection phenomena can be thought as beam supported at both ends and have a uniformly distributed load and the required equations (Equations 4.4 – 4.6) are derived from [80].

The maximum deflection on the thinned cap can be calculated by using the Equation 4.4:

$$\omega_{max} = \frac{5P_{total}l^4w^4}{384D(l^4 + w^4)} \tag{4.4}$$

In Equation 4.4 ω_{max} refers to the maximum deflection value, P_{total} is the total pressure, D is the flexural rigidity and finally l and w are the length and width; respectively. Equation 4.5 shows how is the flexural rigidity, D obtained:

$$D = \frac{Eh^3}{12(1 - \nu^2)} \tag{4.5}$$

In Equation 4.5 E is the Young's Modulus of the Si, h is the thinned thickness and ν is the Si Poisson's Ratio. So, by using the previous two equations the vacuum inside the cavity opened cap can be calculated as shown in the Equation 4.6:

$$\Delta P_{total} = \frac{32Eh^3(l^4 + w^4)}{5(1 - \nu^2)l^4w^4}\Delta\omega_{max} \tag{4.6}$$

The necessary dimensions and mechanical properties of the cavity opened cap wafer can be found in Table 4.2.

Table 4.2 The necessary dimensions and mechanical properties of the cavity opened offered cap wafer.

Parameters	**Values**
Si Poisson's Ratio ν	0.28
Si Young's Modulus, E (GPa)	170
Height (Thinned Thickness), h (μm)	30
Length, l (μm)	5200
Width, w (μm)	3500

To conclude, the deflection of the packaged dies can be measured by using commonly used metrology equipment such as optic or surface profilers; and in the scope of the thesis WYKO optical surface profiler is used (Figure 4.4).

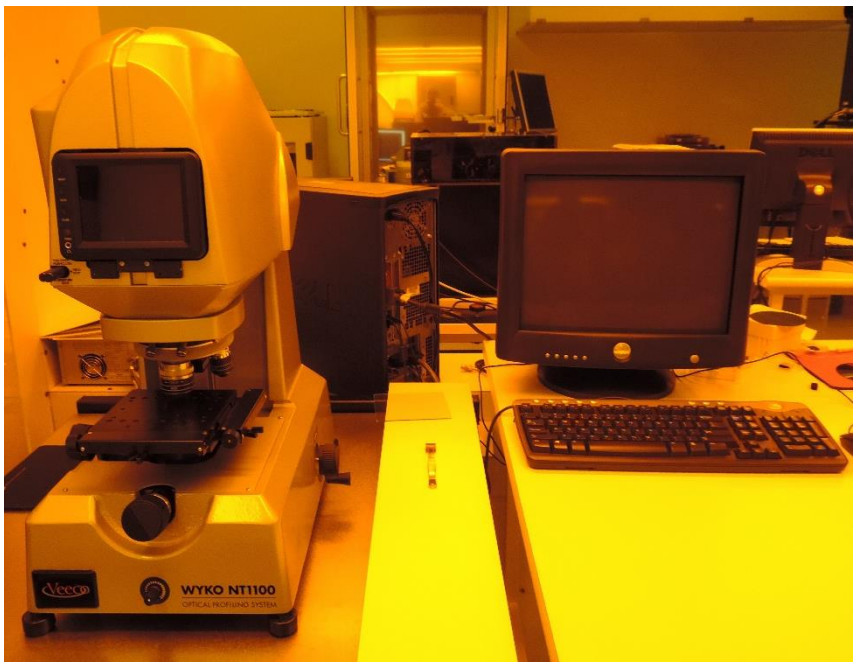


Figure 4.4. The picture of optical surface profiler used for cap deflection tests available in METU MEMS Center.

Cap deflection characterization was performed according to Equation 4.6 with the parameters given in Table 4.2 after bonded and diced piece including 35 dies thinned in DRIE to have a thin diaphragm over the vacuum cavity (Figure 4.5). In Figure 4.5, it is observed that due to the vacuum differences diaphragm is deflected into the cavity as shown in Figure 4.3; so, it is verified that with the offered cap wafer technology hermeticity is satisfied. That is to say, there is a vacuum inside the cap.

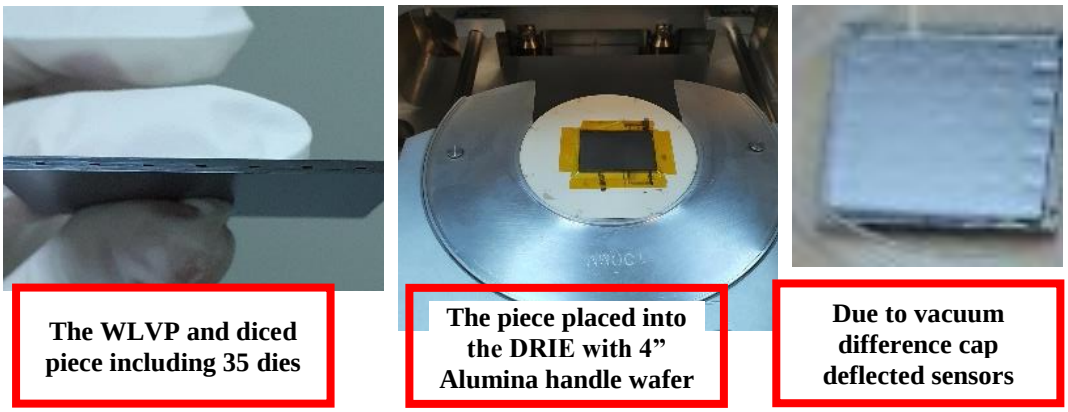


Figure 4.5. The pictures of bonded and diced piece including 40 dies thinned in DRIE to have a thin diaphragm over the vacuum cavity.

The DRIE etch the edge sides more and in edge sides the diaphragm thickness is about 25-30µm whereas in the middle sides of the piece the diaphragm thickness is about 40-45µm. The diaphragm thicknesses are measured in SEM by cross inspection and optical surface profiler and Veeco Dektak8 Stylus Profilometer is used for the measurement of the maximum deflection. In the middle sides, the maximum displacement varies from 16.8µm to 20.1µm (Figure 4.6) and in the edge sides maximum displacement varies from 26.7µm to 37.9µm (Figure 4.7). Also, before experimental measurement respective simulations were also performed by using COMSOL Multiphysics ® v5.3a and simulation and experimental matches and for the offered cap wafer technology without getter vacuum level is measured approximately 5mbar (Figure 4.8).

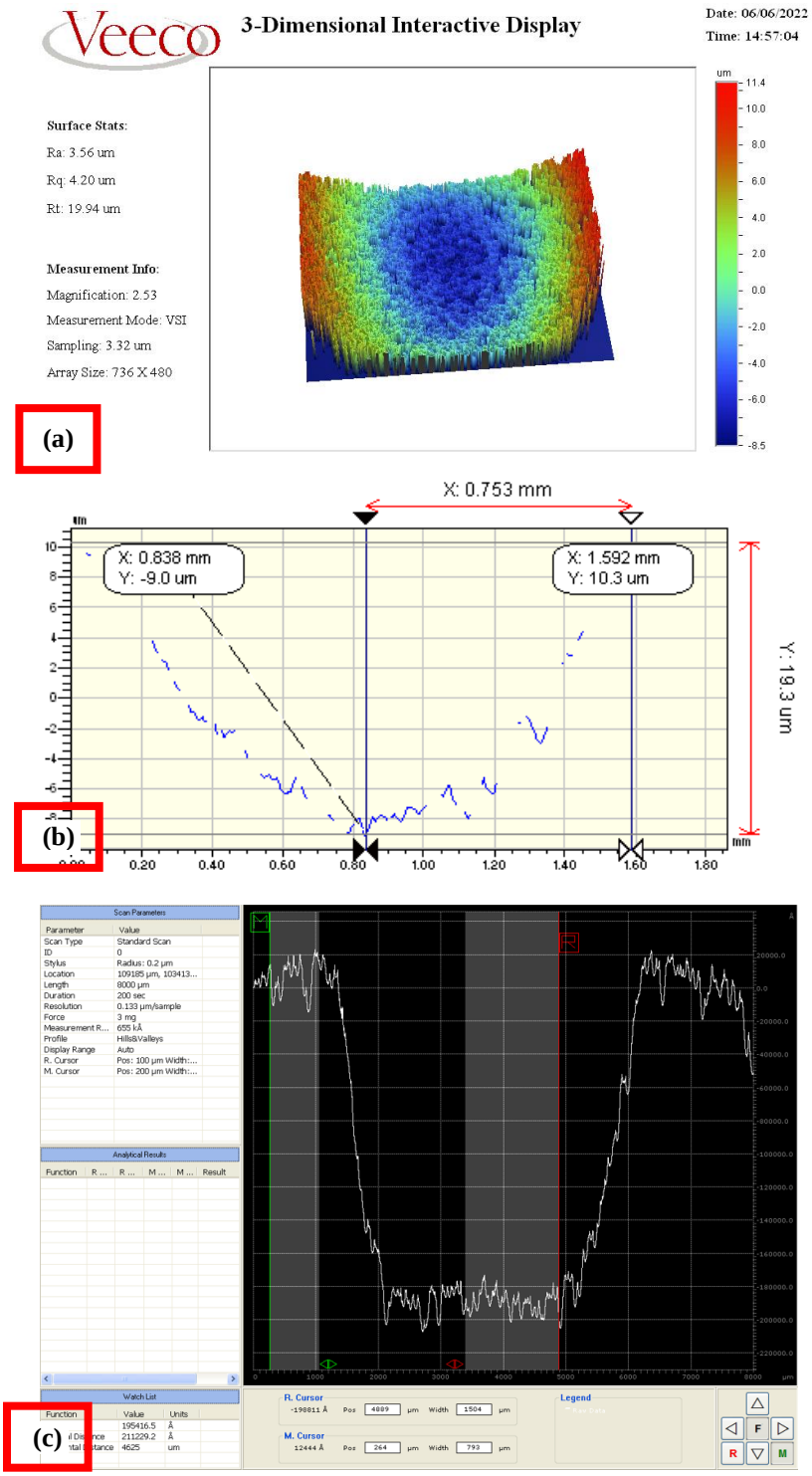


Figure 4.6. The one of the center side dies with cap deflection measurement (≈20μm) results both (a) 3D and (b) 2D in optical surface profiler; and (c) in Dektak.

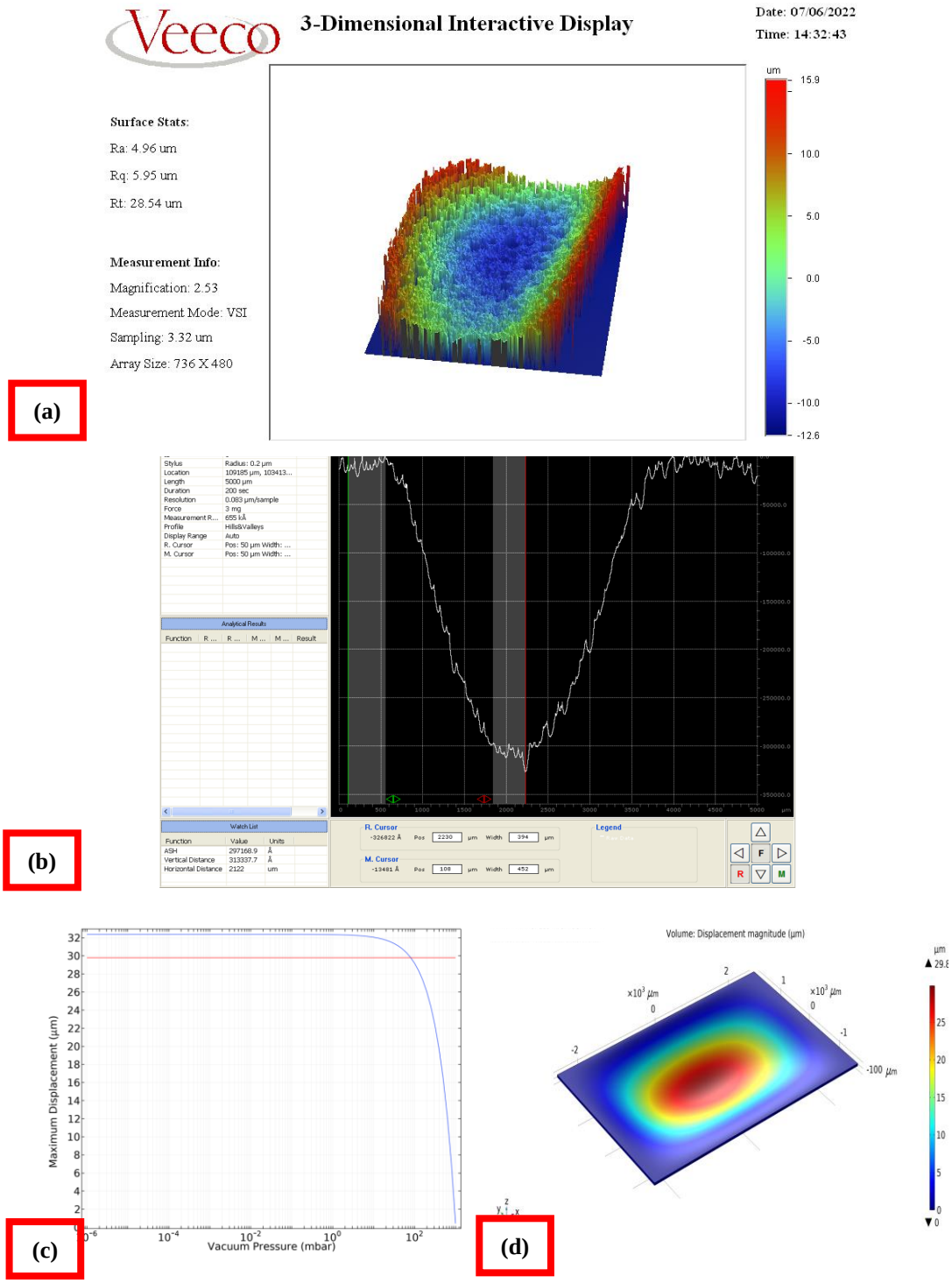


Figure 4.7. The one of the edge side dies with cap deflection measurement (≈30µm) results both (a) 3D in optical surface profiler; (b) in Dektak; (c-d) in COMSOL.

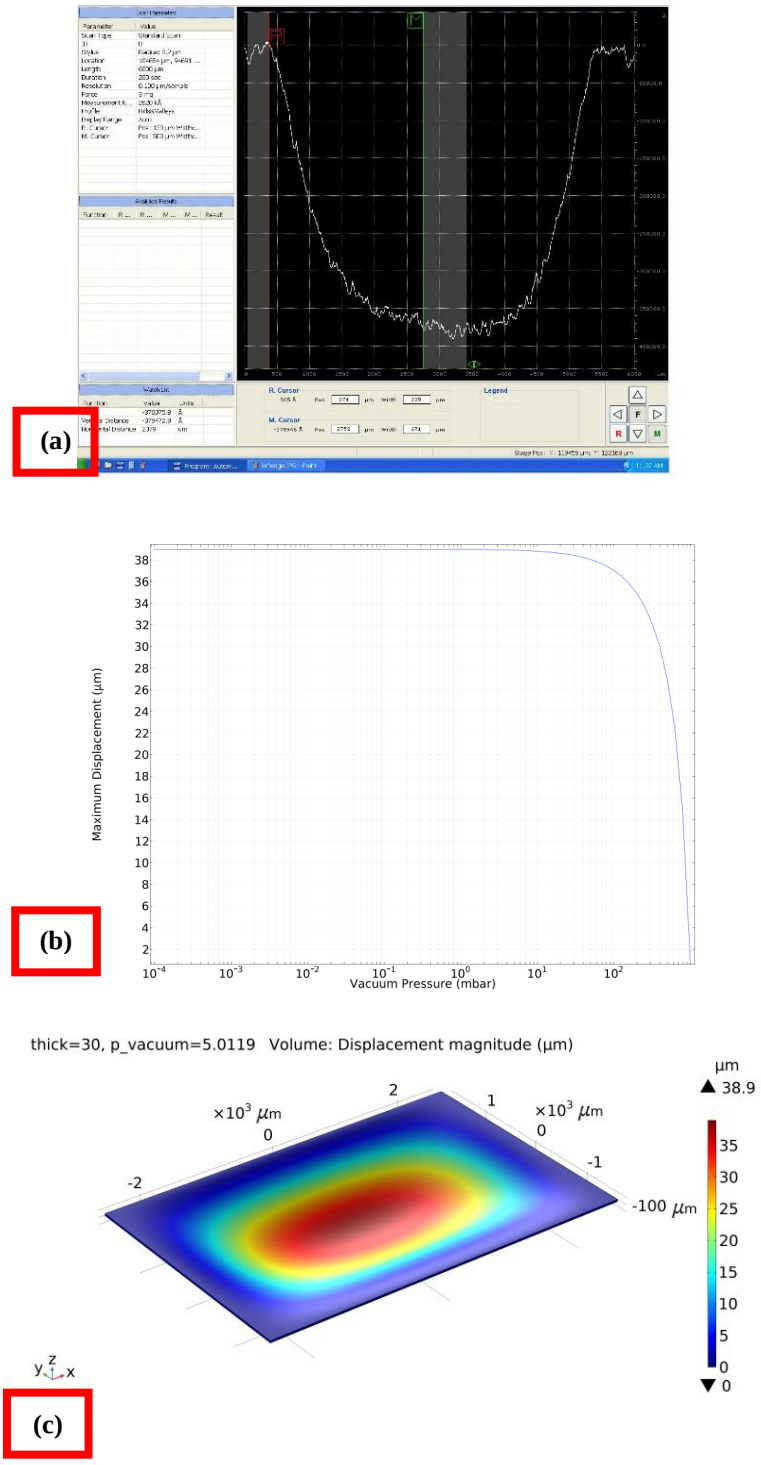


Figure 4.8. The one of the maximum cap deflected dies measurement results both (a) in Dektak and (b-c) in COMSOL. As can be seen deflection is measured 38µm. and vacuum pressure is ≈5mbar.

It is obvious that, when nonlinear effects due to stretching ignored, the deflection increases linearly with pressure [81]; one can check that analytically by solving the Equation 4.6. So, if the deflection is small compared to the plate thickness, it is safe to neglect in-plane strains in the middle surface in comparison with the strains due to bending. For the case in which the deflection is on the order of plate thickness but still small when compared with the dimensions, the diaphragm begins to stretch where in-plane strains are no longer of a negligible order of magnitude. Thus, the 3D model of the rectangular diaphragm deformation was studied in COMSOL Multiphysics Solid Mechanics Interface to obtain expected maximum center deflection by logarithmically varying the vacuum pressure from atmosphere to 10^{-4} mbar. By including geometric nonlinearity, the calculations were advanced to cover the middle surface strain to obtain more realistic behavior of the diaphragm under relatively high vacuum pressure where the diaphragm deflects more than its thickness. The deflection of the silicon diaphragm depends upon the Young's modulus and the Poisson's ratio of the material and increases with the amount of pressure difference (cavity and the atmosphere) applied to the diaphragm. The pressure difference was applied as a boundary load to the one of the diaphragm surfaces. All in all, for the 30µm thick diaphragm we observed ≈38µm deflection according to Dektak and optic profilometer measurements and in the conducted simulations (Figure 5.25 (a)) it is observed that maximum deflection can be 39 µm and when we redraw for 1-5 mbar region change can be seen in Figure 4.9 (b) so when we check the experimental with the simulation it refers to 5.0119 mbar.

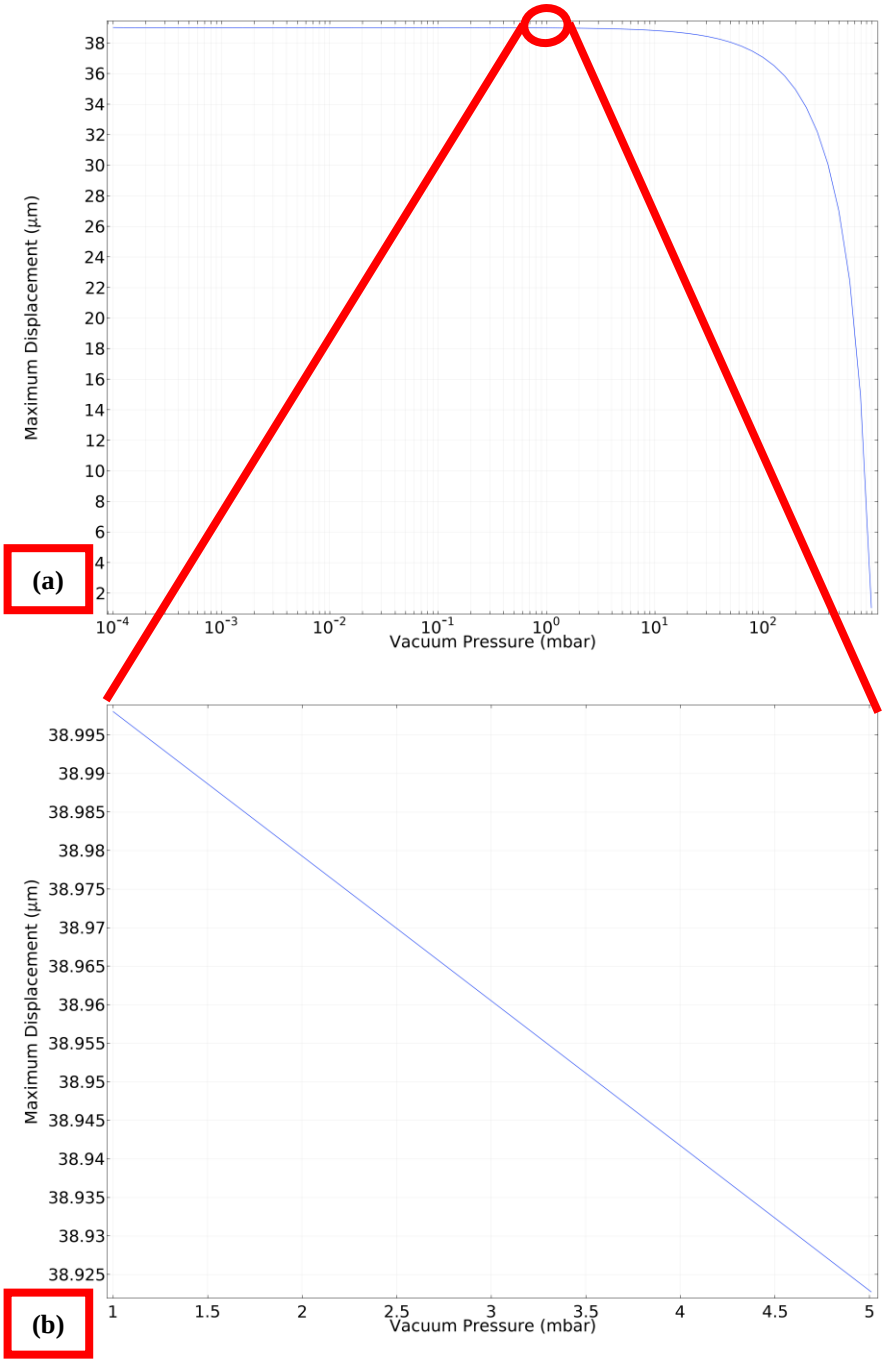


Figure 4.9. The maximum displacement versus vacuum pressure plot drawn according to COMSOL simulations. Notice that simulation and experimental results are similar.

Notice that in cap deflection characterization getter is not deposited to the cap wafer so vacuum level is a bit low. To conclude, for the offered cap wafer technology

without getter vacuum level is measured approximately 5 mbar and it is equal to 3.75 Torr.

4.3 In-Situ Vacuum Sensors

The other and the most reliable method for monitoring the cap wafers is integrating in-situ vacuum sensors. The methods for monitoring micro packaged pressures are searched ranging from helium leak tests to the measurement of the quality factor of inertial sensors or resonators; and micromachined Pirani gauge vacuum sensors for integrating Wafer C case is searched from literature. Needless to say, before adapting vacuum sensors to Wafer C, in multi project test wafer the functionality of the sensors is verified and in preliminary and functionality tests section mentioned detailly.

4.3.1 Preliminary and Functionality Tests

Before adapting the Pirani vacuum sensors to offered cap wafer technology. First of all, production of four different resistor type micro-vacuum sensors with using METU MEMS Center clean room facilities completed in a multi project Si test wafer. Secondly, from 8” wafer level to die level singulation (dicing) is performed and after die level suspensions, the sensors have to be subjected to the functionality test under atmospheric conditions. The aim of this test is to identify the functional and non- functional dies and simple resistance measurement is sufficient for the fabricated Pirani gauges. The test setup consists of probe station and a multimeter. After fixing the dies to the probe station, the resistances of the Pirani gauges are measured using the multimeter.

4.3.1.1 Die Level Tests of Pirani Gauges in Controllable Vacuum Chamber

For the vacuum tests, the functional dies from the diced wafer are identified during the functionality tests and passed for the vacuum test. These dies are placed inside a vacuum chamber and their response is observed at vacuum.

After selecting the functional dies including vacuum sensors the functional dies wire bonded for continuing the die level preliminary tests in terms of resistance versus pressure plots from 1atm (760 Torr) to $4x10^{-5}$ Torr are performed in controllable vacuum chamber to check whether they are applicable to the offered cap wafer technology or not.

Keithley 2635b and Keithley 2410 source measure units were used for vacuum sensor characterization. Keithley 2410 heater vacuum sensor is used for heater control. The measurements were repeated by applying 1.5 microamps of current through the vacuum sensors tested.

In order to understand the sensitivity of vacuum sensor, which is included heater, it should be considered that in a gas filled system there are four ways that a heated wire transfers heat to its surroundings.

1. Gas conduction at high pressure $E\ \alpha\ dT/dr$,
2. Gas transport at low pressure $E\ \alpha\ P(T_1 - T_0)/\sqrt{T_0}$,
3. Thermal radiation $E\ \alpha\ P(T_1^4 - T_0^4)$,
4. End losses through the support structures.

Heated sensor suspended in a gas will lose heat to the gas as its molecules collide with the wire and remove heat. If the gas pressure is reduced the number of molecules present will fall proportionately and the wire will lose heat more slowly. Measuring the heat loss is an indirect indication of pressure.

There are three possible schemes that can be done for calibration:

1. Keeping the ac voltage constant and measure the change in resistance as a function of pressure.
2. Keeping the current constant and measure the change in resistance as a function of pressure.
3. Keeping the temperature of the sensor wire constant and measure the voltage as a function of pressure.

Note that keeping the temperature constant implies that the end losses and the thermal radiation loses are constant.

The electrical resistance of a wire varies with its temperature, so the resistance indicates the temperature of wire. In many systems, the wire is maintained at a constant resistance R by controlling the voltage through the sensor. The resistance can be set using a bridge circuit. The voltage required to achieve this balance is therefore a measure of the vacuum. The image of the used setup during the vacuum tests could be seen in Figure 4.10.

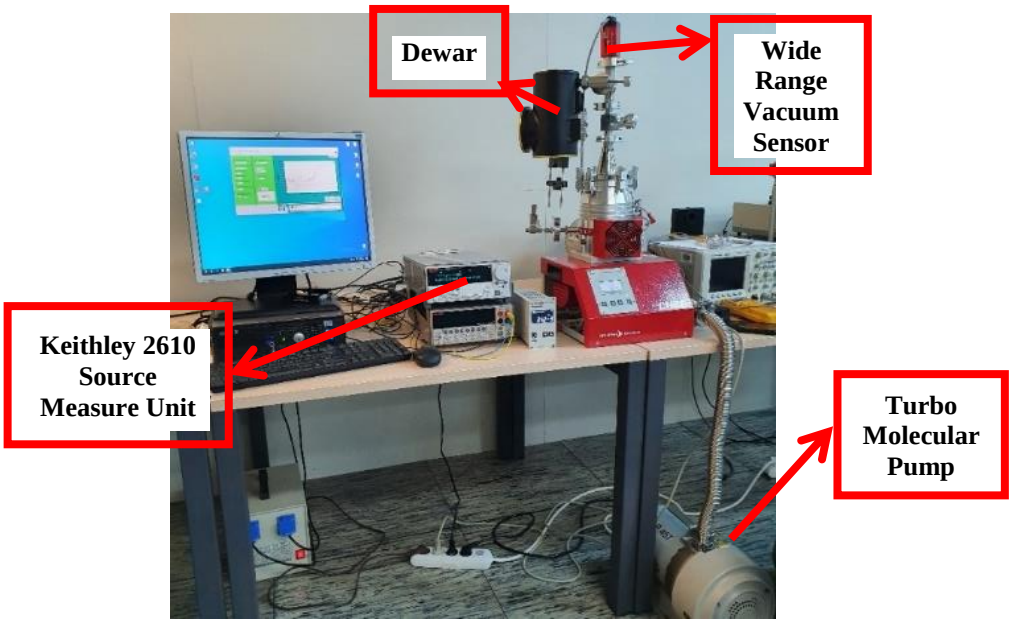


Figure 4.10. The image of the used test setup during the vacuum sensor preliminary tests.

The gauge may be used for pressures between 10 Torr to 1×10^{-4} Torr. Below 5×10^{-4} Torr, all sensor types have only one significant digit of resolution. The thermal conductivity and heat capacity of the gas affects the readout from the meter, and therefore the apparatus may need calibrating before accurate readings are obtainable. For lower pressure measurement, the thermal conductivity of the gas becomes increasingly smaller and more difficult to measure accurately. For the preliminary tests, vacuum sensor on the D21.1, D3.3 and D23.3 which is part of Test

wafer 6.83 is characterized. The related test setup, sensor preparation details is shown in Figure 4.11. Among the others D3.3 appears to have a design with the greatest variation in resistance with respect to pressure. To perform these tests, Labview based program is used. The comparative chart containing the measurement results is given in Figure 4.12.

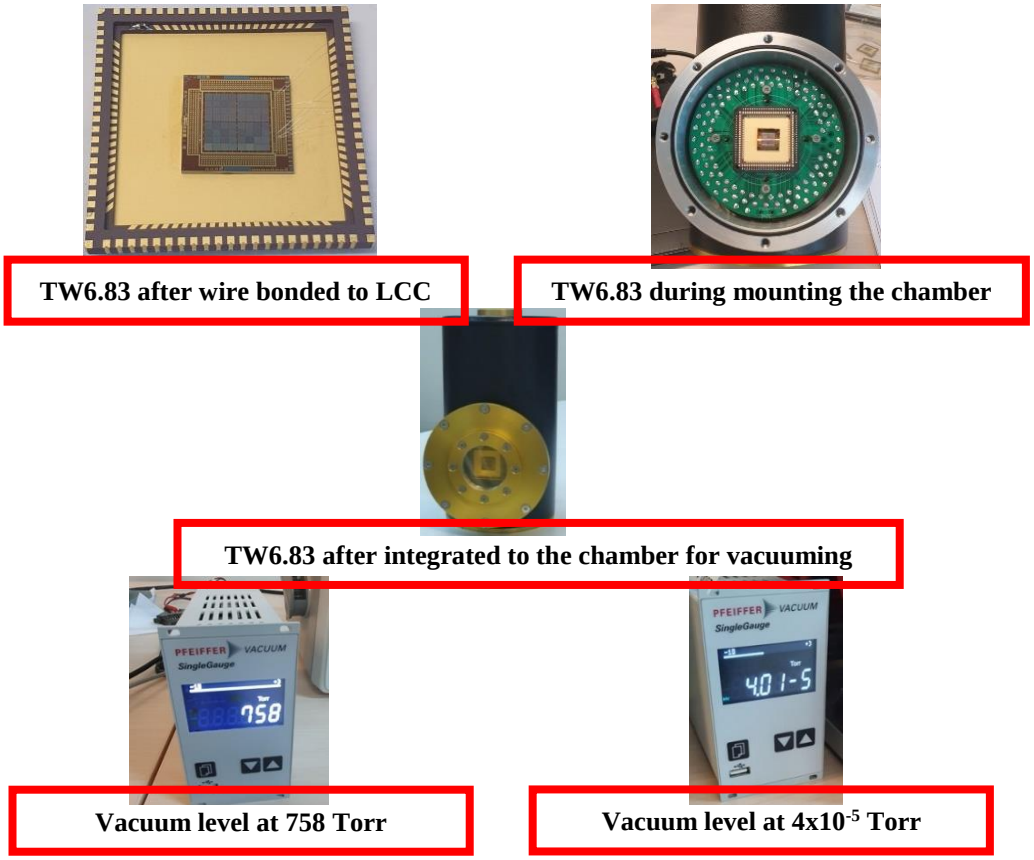


Figure 4.11. The images showing the related procedure while preparing the vacuum sensor to the testing and during the vacuum tests.

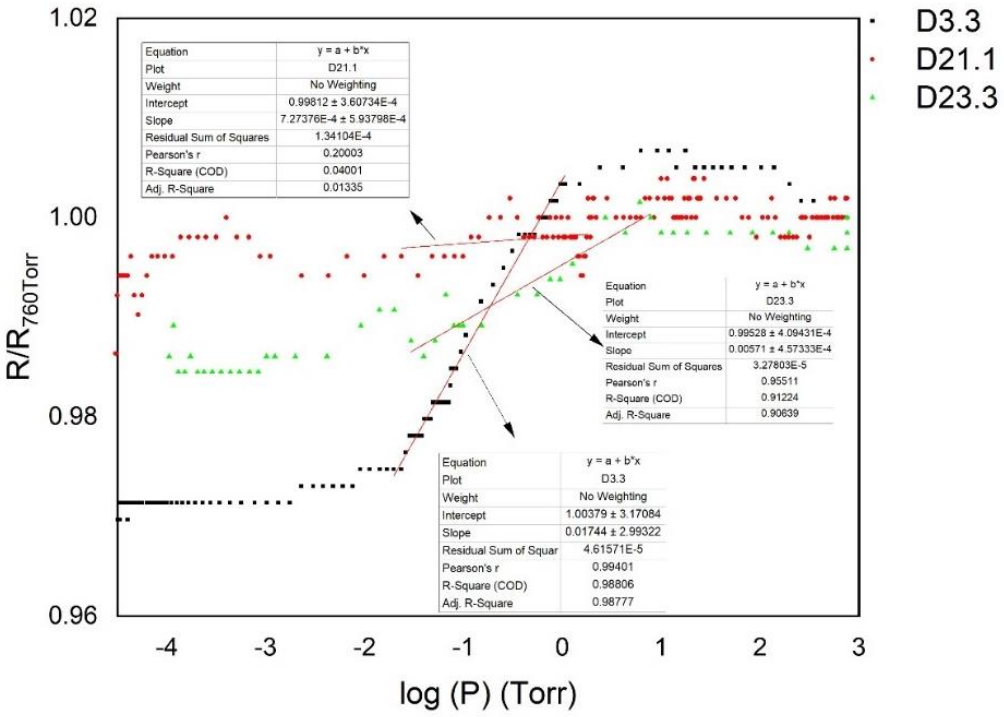


Figure 4.12. The comparison plot showing normalized results and Log Pressure versus R/R0 Plot of TW6.83 Vacuum Sensors (D21.1, D3.3 and D23.3) of vacuum level of 10^{-5} Torr, by applying 500nA current with using Keithley 2610 source measure unit.

Notice that these are preliminary quick measurement result to see there is response or not we perform these experiments and among other D3.3 shows the best response; then we performed to continue tests waiting to settle pressure and we increased the pressure range. After reaching a vacuum level of 10^{-5} torr, pressure-dependent changes were obtained in the resistance of the vacuum sensors by applying 500nA current with using Keithley 2610 source measure unit. From the comparison curves, it was observed that the resistance did not change with the pressure at 10^{-3} Torr vacuum level and 10 Torr upper pressure levels. The tabulated form of the resistance between 1 mTorr and 10 Torr is given below as how changes is shown in Table 4.3.

Table 4.3 Tabulated form of the resistance change between 1mTorr and 10 Torr of TW 6.83 D3.3, D21.1, and D23.3.

TW 6.83 **Die #**	$d[\log(P)] / d\left[\frac{R_{760}}{R}\right]$ **(x10^{-3}) (Ω/Torr)**	**R (kΩ)** **@ 760 Torr**	**R (kΩ)** **@ 5x10^{-5} Torr**
D3.3	**17.44 ± 2.99322E-1**	**59.4**	**57.7**
D21.1	5.71 ± 4.57333E-1	51.3	50.8
D23.3	0.7.27376 ± 5.93798E-1	64.6	63.9

I-V graph of D3.3 was measured and drawn under 3x10^{-5} Torr pressure before starting the measurements (P vs R). In the section where the resistance is drawn with ohmic behavior before the self-heating zone, a current above 1µA is given. Therefore we applied the 500nA current as shown in Figure 4.13.

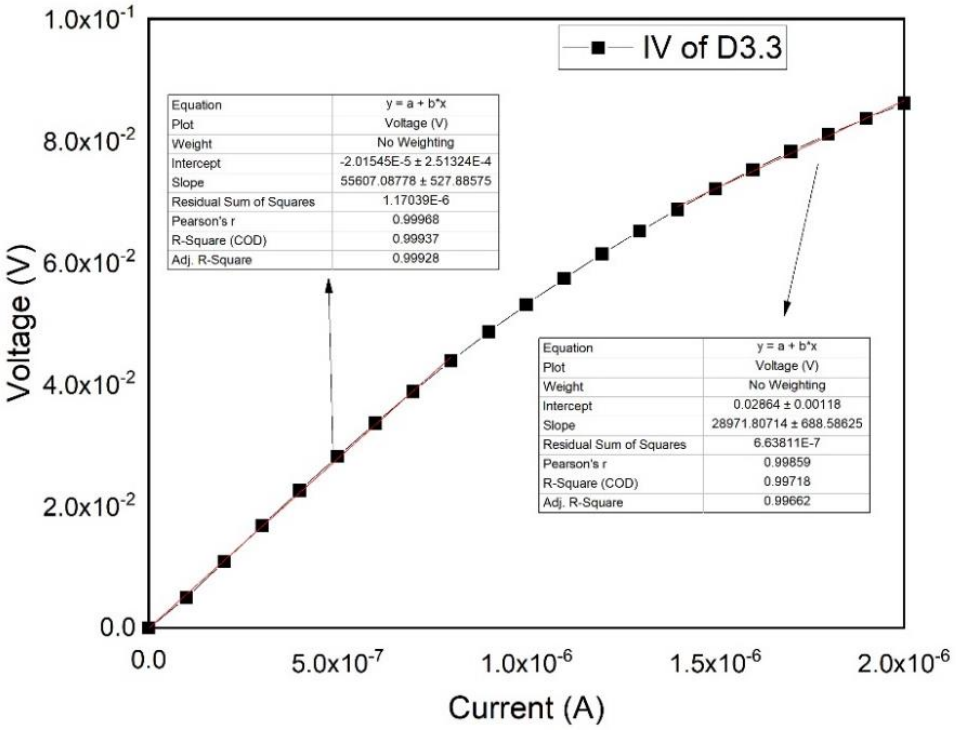


Figure 4.13. The I-V Graph of D3.3 @ 3x10^{-5} Torr.

To find the optimum current some tests to TW6.83 D3.3 (VP1 type) was applied with 1-2.5µA with 0.5 µA current increments. At the end of the experiments, it is seen that 1.5 µA is the optimum current value for testing the sensors (Figure 4.14).

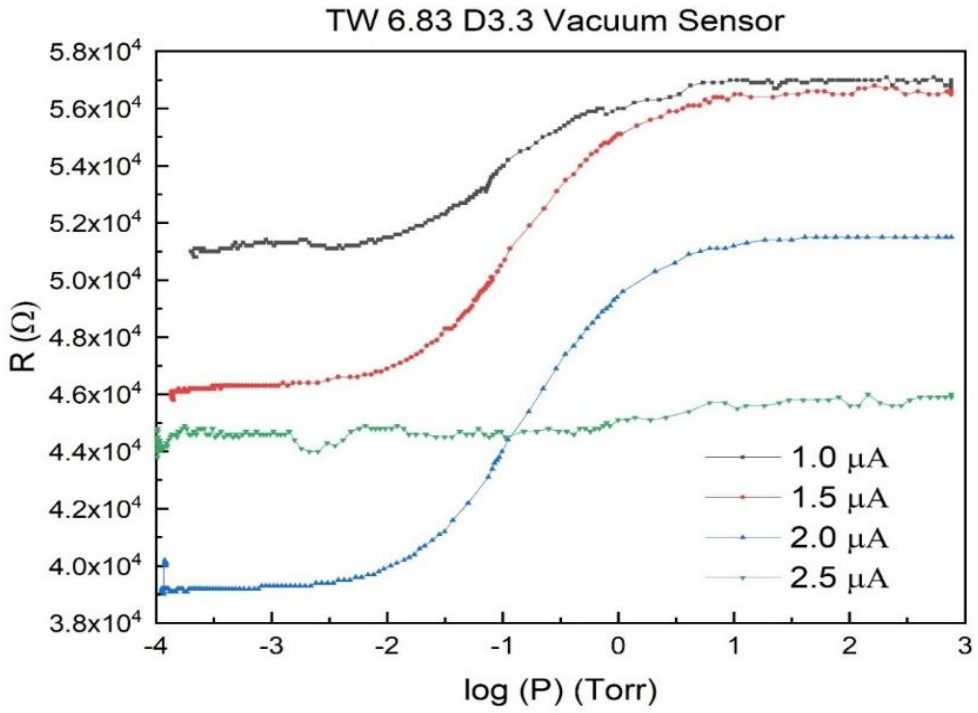
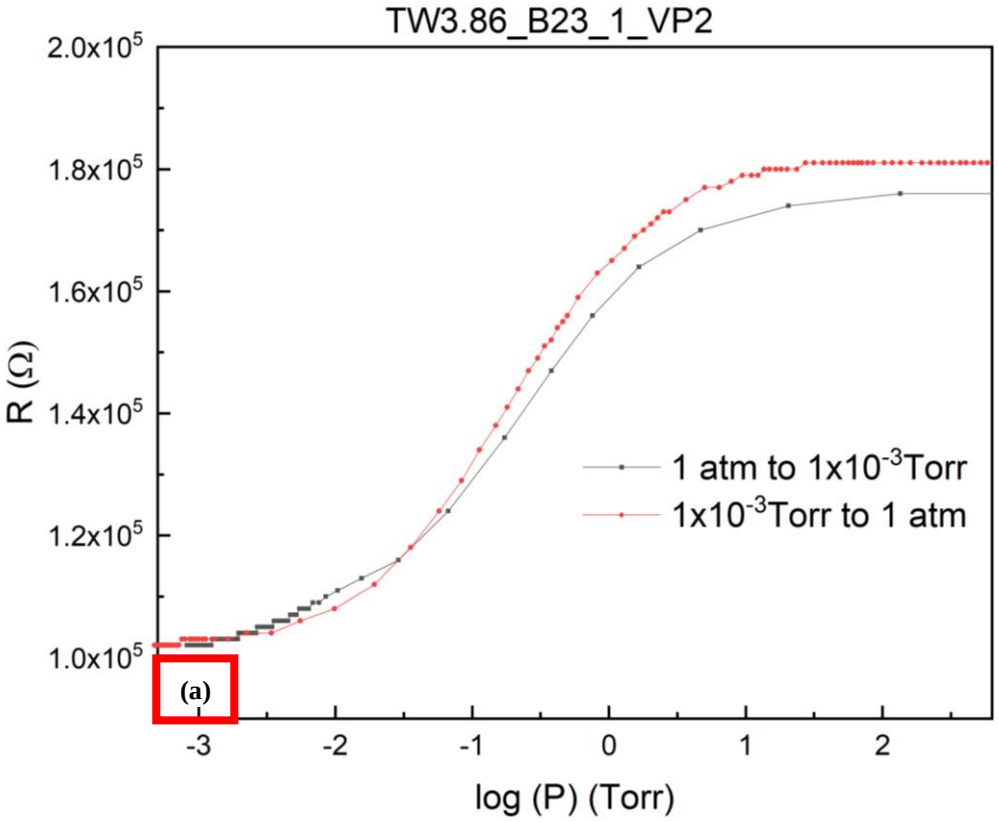
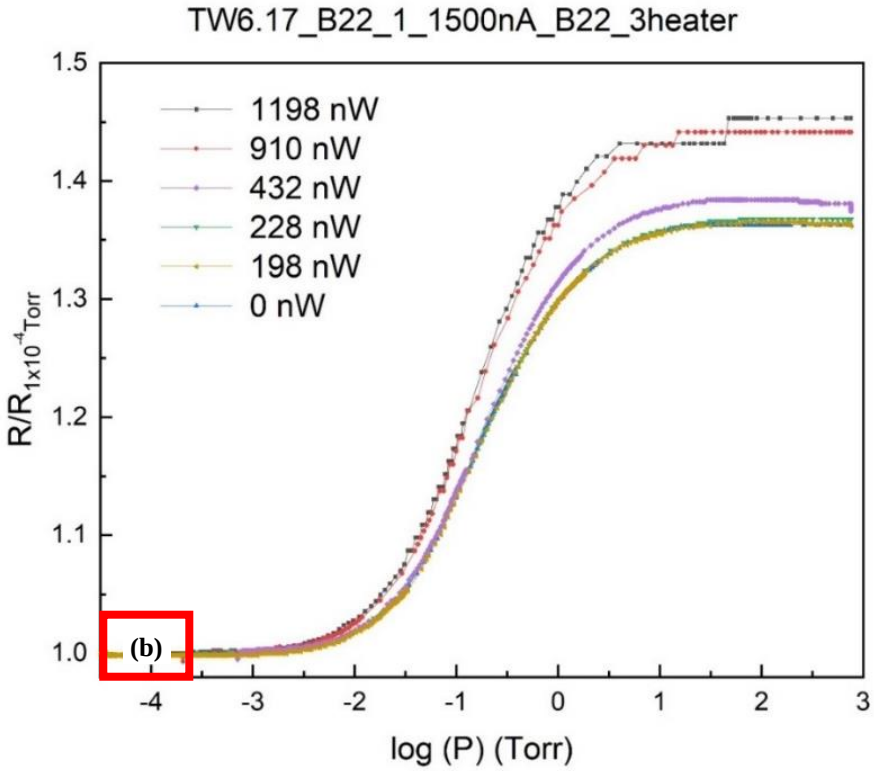


Figure 4.14. The graphs showing the test results of TW6.83 D3.3 (VP1 type) resistance versus log pressure plot with 1-2.5µA with 0.5 µA current increments. Notice that 1.5 µA is the optimum current value for testing the sensors.

As a next step of the study, other types of vacuum sensors are selected from different dies, and they are characterized separately. Figure 4.15 shows VP2, VP3 and VP4 type vacuum sensors characterization test results.


TW3.86_B23_1_VP2
2.0x10^5
1.8x10^5
1.6x10^5
1.4x10^5
1.2x10^5
1.0x10^5
R (Ω)
1 atm to 1x10^-3Torr
1x10^-3Torr to 1 atm
(a)
-3
-2
-1
0
1
2
log (P) (Torr)


TW6.17_B22_1_1500nA_B22_3heater
1198 nW
910 nW
432 nW
228 nW
198 nW
0 nW
R/R1x10^-4Torr
1.5
1.4
1.3
1.2
1.1
1.0
(b)
-4
-3
-2
-1
0
1
2
3
log (P) (Torr)

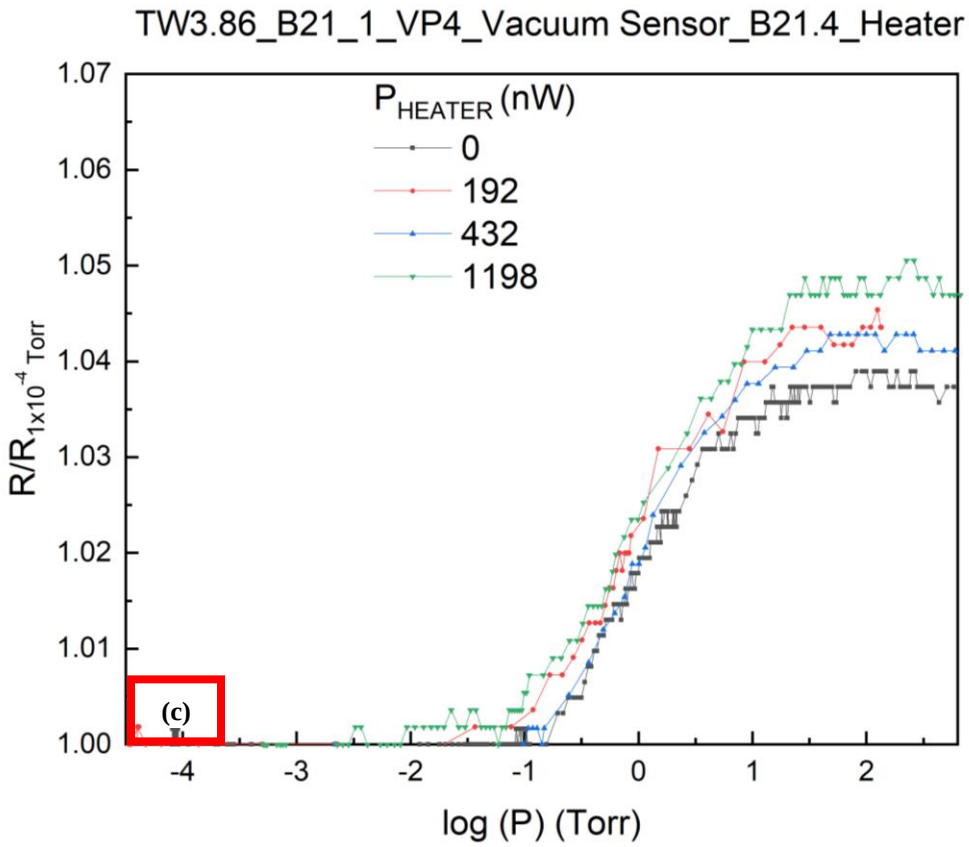


Figure 4.15. The graphs showing the characterization test results of vacuum sensors: (a) TW3.86 B23.1 (VP-2) resistance versus log pressure plot at 1.5µA current. (b) The calibration of vacuum sensors TW6.17 B22.1 (VP-3 with heater (B22.1)) normalized resistance versus log pressure plot with 1.5µA current and giving heater to different power values. (c) The calibration of vacuum sensors TW3.86 B21.1 (VP- 4 with heater (B21.4)) normalized resistance versus log pressure plot with 1.5µA current and giving heater to different power values.

After characterizing the vacuum sensors separately, the performances are compared among the others VP-2 shows the best results. Also, when vacuum sensors which includes heaters by applying heater to different power values are compared VP-3 shows the best results in 1198nW power value compared to VP-4 and all these comparison results could be found in Figure 4.16.

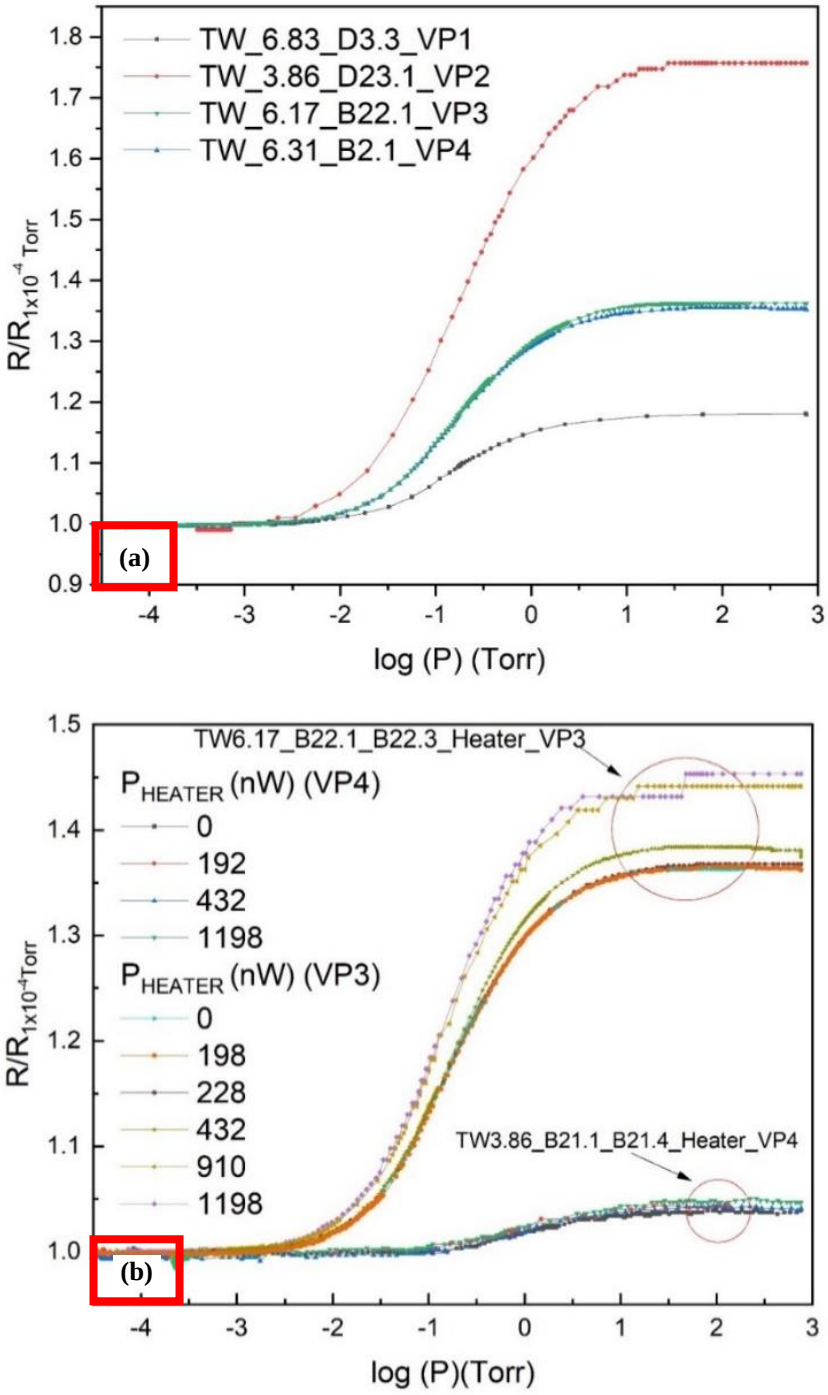


Figure 4.16. (a) The performance comparison of 4 different vacuum sensors and among the others VP-2 shows the best results. (b) The performance comparison of the vacuum sensors which includes heaters; VP-3 shows the best results in 1198nW power value.

To conclude, preliminary test results are promising so it is decided to adapt the Pirani gauges to the Wafer C.

4.3.2 Characterization of Wafer C in Controllable Vacuum Chamber Before Wafer Level Packaging

Before WLVP by applying glass frit bonding, 8" size and offered cap wafer technology compatible fabricated and wafer level sacrificial released device sensors which are Pirani gauges (Wafer C with vacuum sensors) tested for characterization purposes. The device wafer (Wafer C) including 748 dies and in each die normally 4 different vacuum pressure sensors are included. But electrical connections are designed just for the first three type and 4^{th} sensor type is not electrically measured; so, VP-1, VP-2 and VP-3 type sensors are characterized and only their results are going to be mentioned. In the scope of the thesis two device wafers with Pirani gauges named as WC3 and WC5 are fabricated. Notice that the anchor and arm separated from each other in WC5 but it has also survived sensors so for characterization purposes both wafers are tested.

In all characterizations SUSS PAV 200 Probe Station System is used (Figure 4.17), contact via the pads are obtained with single probes. This system has various advantages: the samples can be tested at both atmospheric conditions and vacuum environment. Besides manipulating the chuck temperature is possible. That is to say, the chuck where the sample is placed can be cooled and heated. So, it is possible to make temperature characterization of the samples.

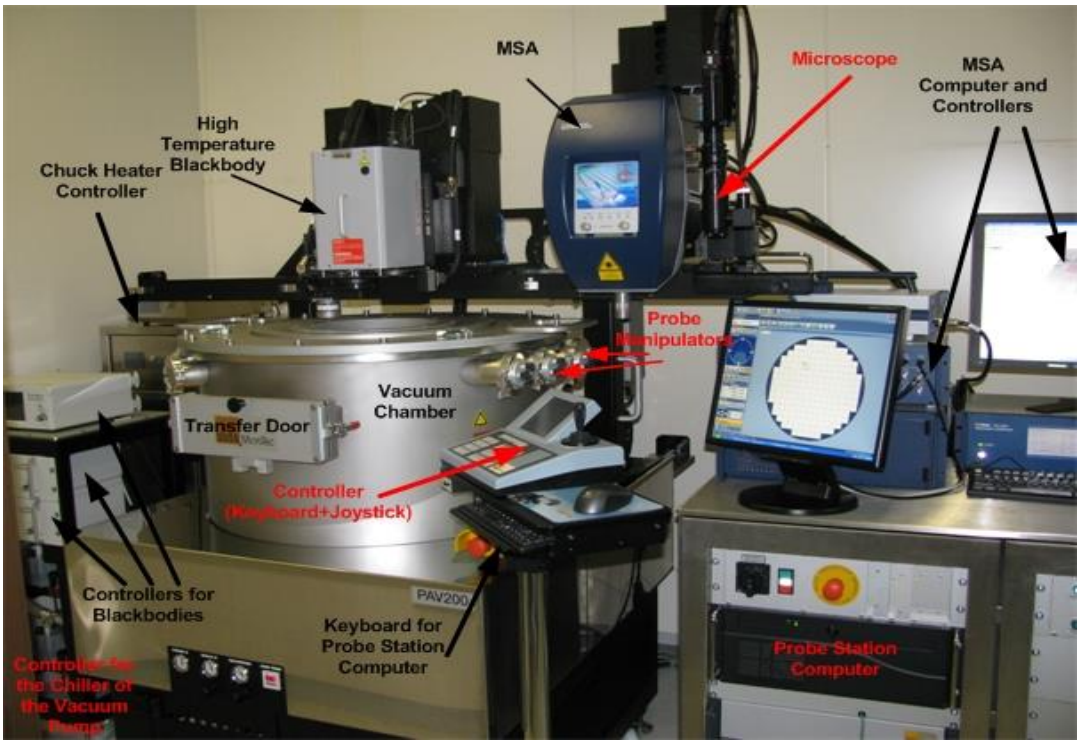


Figure 4.17. SUSS PAV 200 Probe Station System Available in METU MEMS Center.

As a first step of the characterization, the survived sensors are selected by using Keithley model current source meter and applying current from 0 nA to 3000 nA with 150 nA increments in 1 atm, 760 Torr pressure level at 25℃ chuck temperature. There are a lot of sensors, so wafer is tested automatically by using MikroSens Company's test software; after inserting the wafer to SUSS MicroTec PAV200 semi- automatic probe station making the necessary alignments and contact issues. Figure 4.18 shows the inserting wafer to the chamber preparing the test setup and testing procedure details.

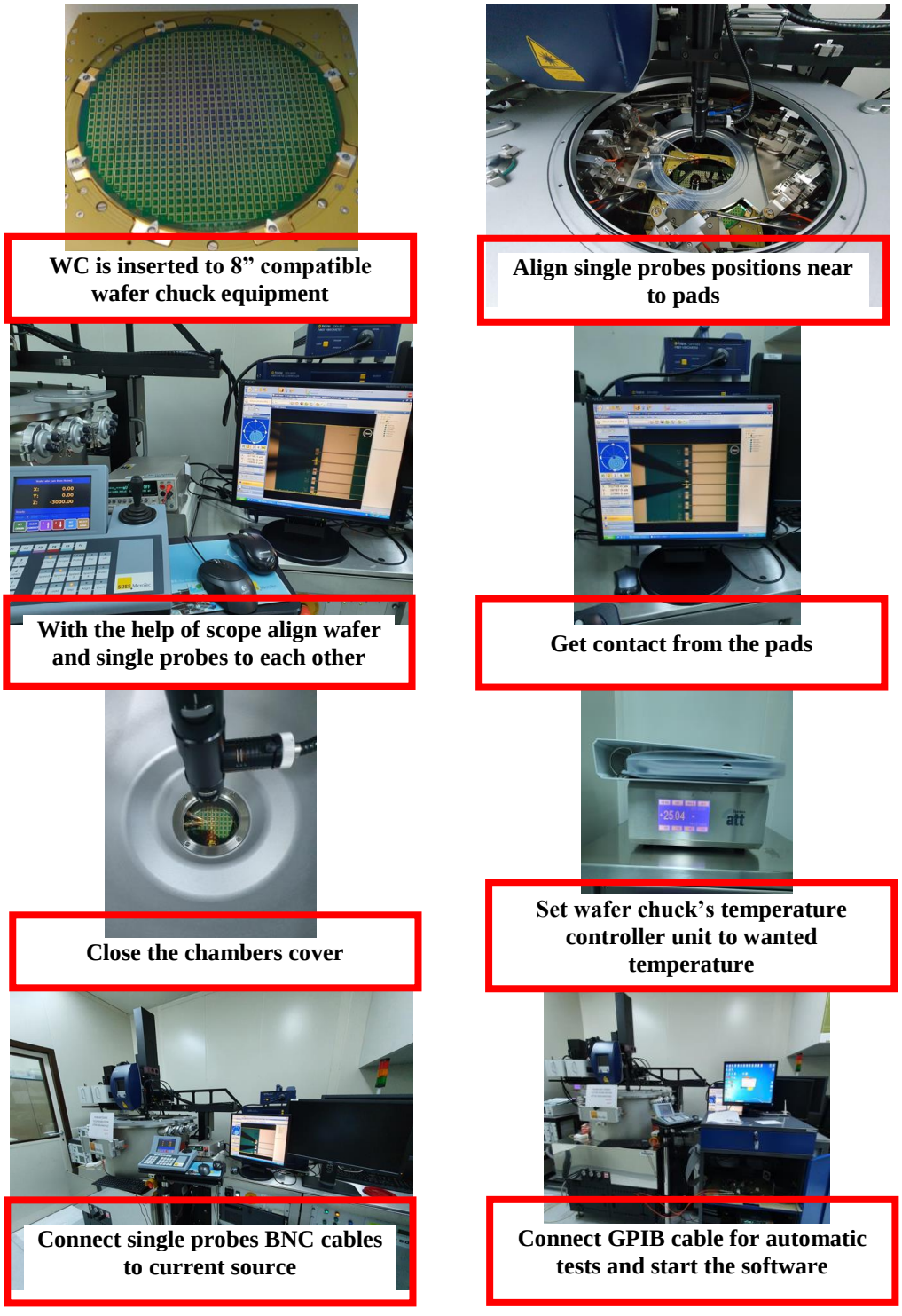


Figure 4.18. The prepared test setup details in PAV 200 system for characterization of Wafer C with vacuum sensors.

4.3.2.1 Detection of Functional Dies

The functional dies are selected by using Keithley model current source meter and applying current from 0 nA to 3000 nA with 150 nA increments in 1atm, 760Torr pressure level at 25℃ chuck temperature. For representation one of the functional vacuum pressure sensors' (WC5 VP2 Die 324) I-V graph is drawn under 760 Torr, 1 atm pressure as shown in Figure 4.19.

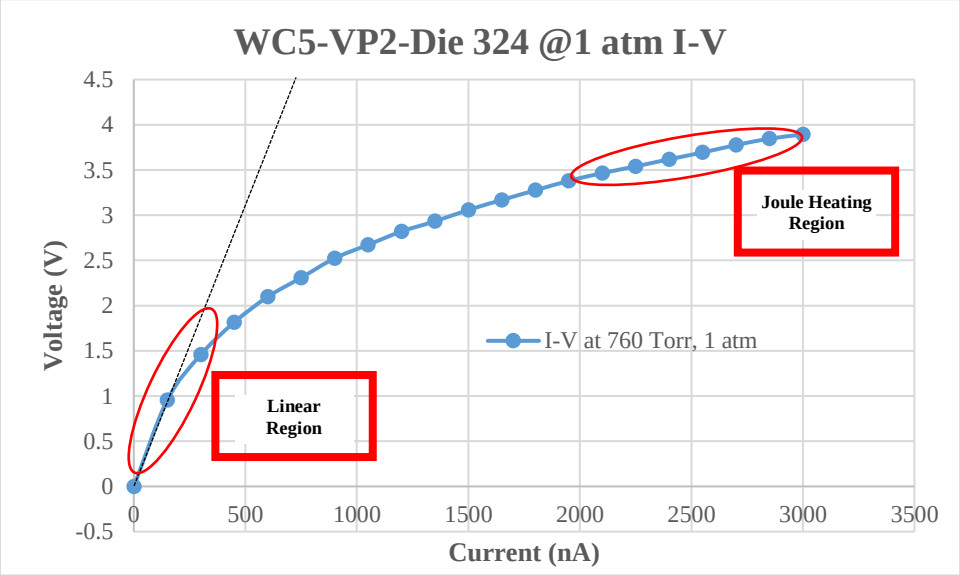
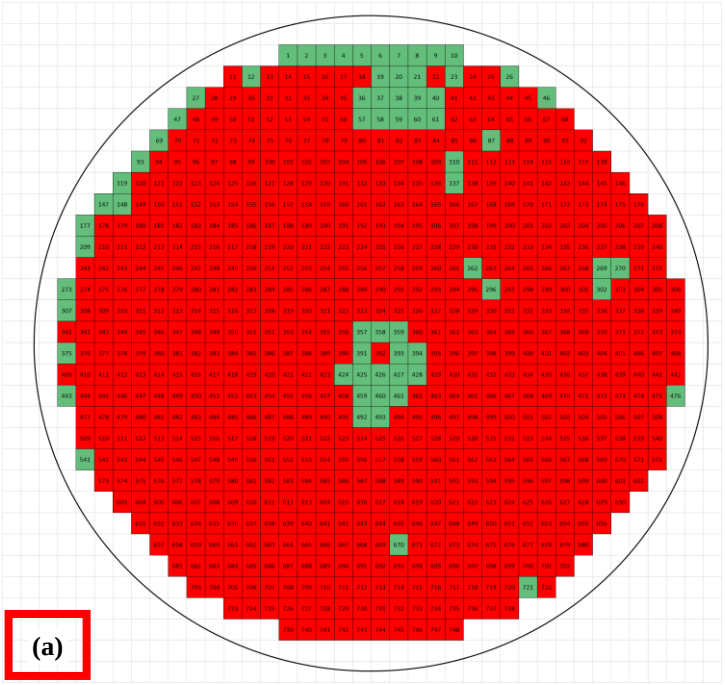


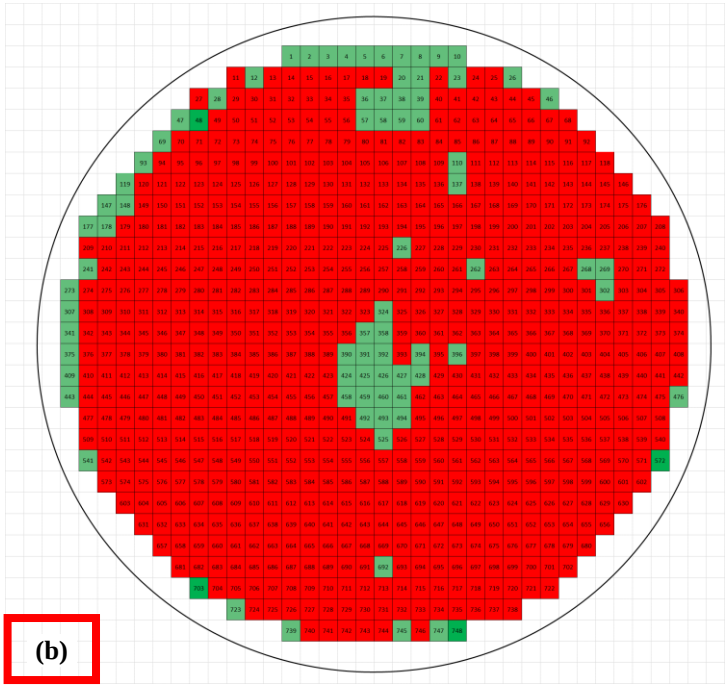
Figure 4.19. The I-V plot of one of the functional pirani vacuum gauges and linear and Joule heating region representations on it.

Obtained functionality map according to I-V sweeps in 1 atm for VP-1, VP-2 and VP-3 type vacuum pressure sensors could be found in Figure 4.20. Notice that in the scope of this study 2 device wafers are fabricated (WC3 and WC5) in Chapter 3 faced problems are mentioned detailly. Firstly, WC5 is tested because it is the most problematic wafer during the arm body nitride etch and wafer level release trials due to the stress and buckling anchor points are separated from the arm body part and

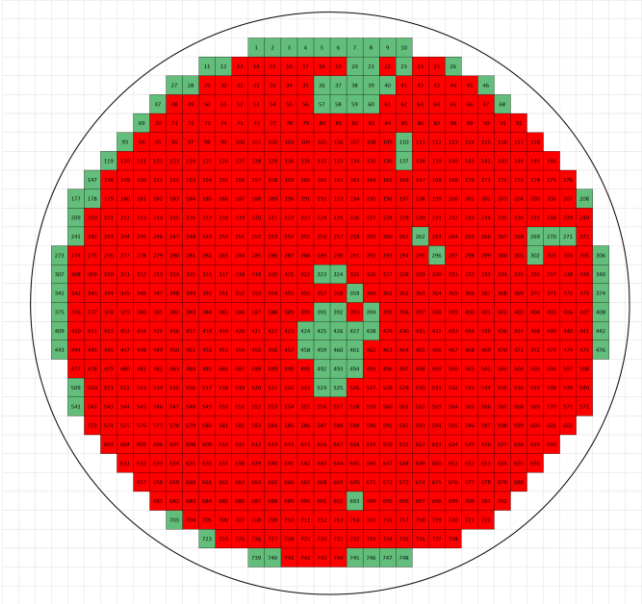
many metal connections is lost so yield is low. However, in the scope of thesis yield is not the main concern and functional dies are satisfactory for obtaining look-up table and comparing the results after wafer level vacuum packaging for the proof of the concept.



(a)



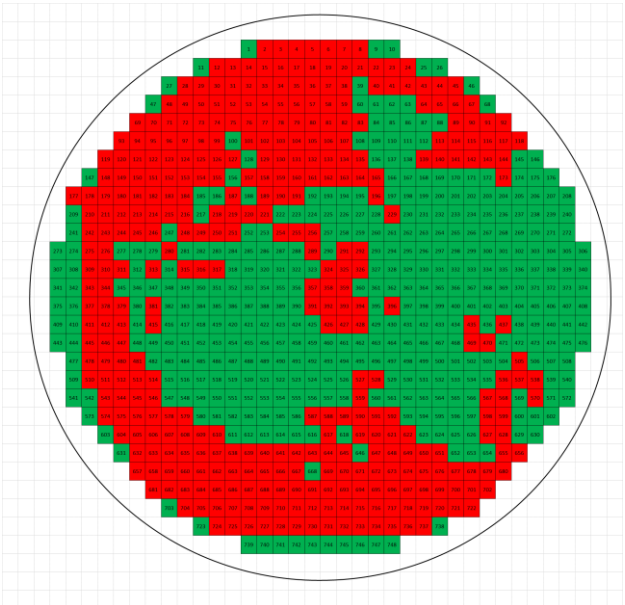
(b)



(c)

Figure 4.20. The obtained functionality map of WC5 according to I-V sweeps in 1 atm for: (a) VP-1, (b) VP-2 and (c) VP-3 type vacuum pressure sensors.

After completing the WC5 tests, as a next step, WC3 is tested as a final step and obtained functionality map of WC3 according to I-V sweeps in 1 atm for VP-1, VP- 2 and VP-3 type vacuum pressure sensors could be found in Figure 4.21.



(a)

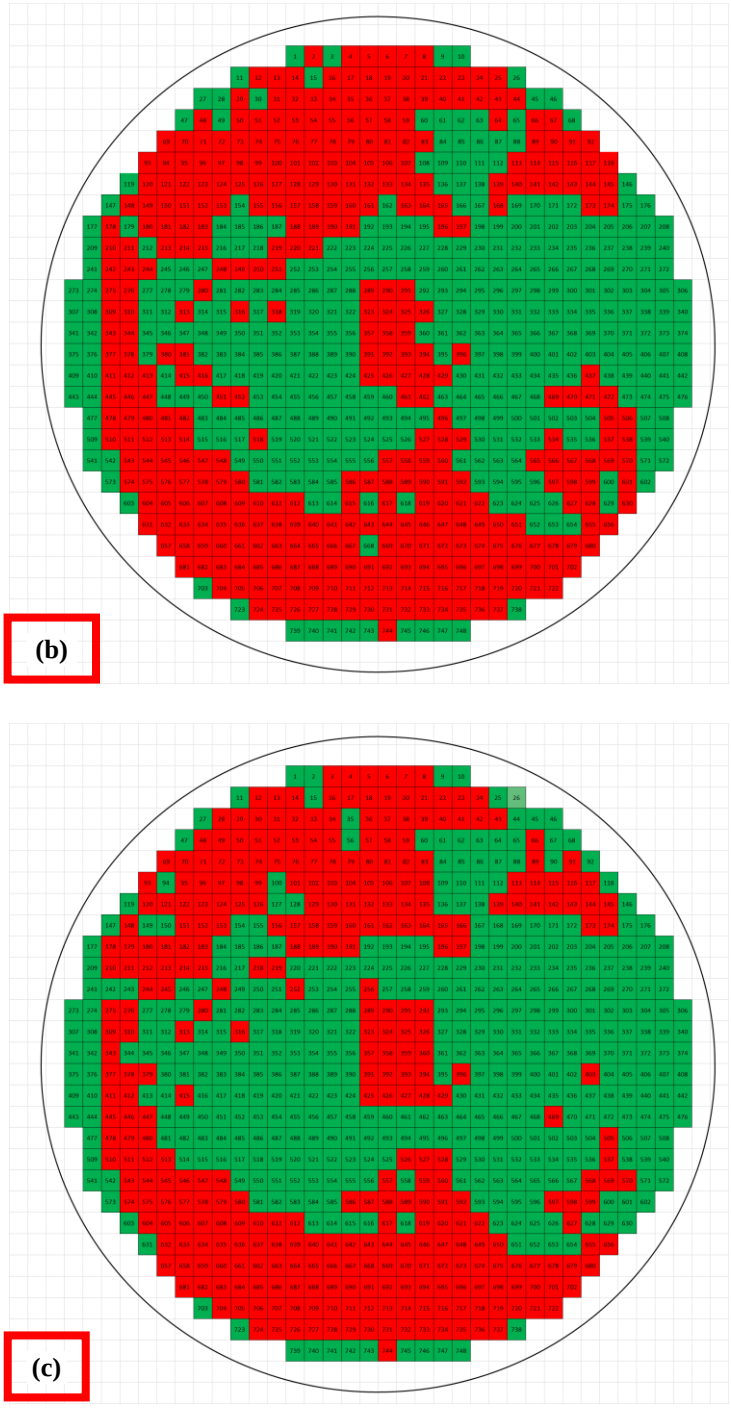


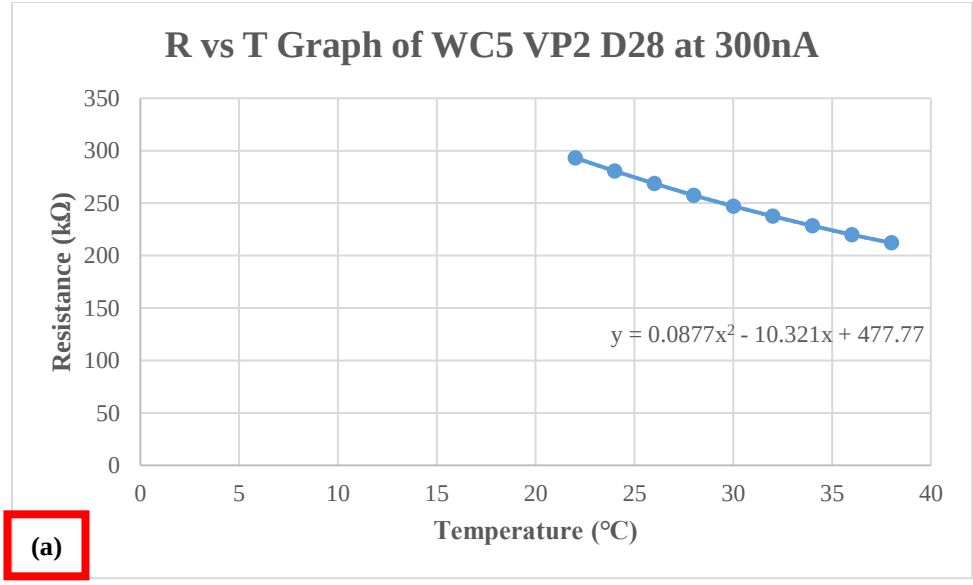
Figure 4.21. The obtained functionality map of WC3 according to I-V sweeps in 1 atm for: (a) VP-1, (b) VP-2 and (c) VP-3 type vacuum pressure sensors.

4.3.2.2 TCR Measurement

Resistive IR sensors use the temperature coefficient of resistance (TCR) of the active material as the sensing mechanism. TCR of a material is defined as in the Equation 4.7:

$$\alpha = \frac{1}{R}\frac{dR}{dT} \qquad (4.7)$$

where α is the temperature coefficient of resistance, R is the total resistance of the material and T is the temperature. The measurement of TCR is performed in the SUSS PAV 200 Probe Station System's temperature controllable chuck and chamber by using an unsuspended detector in order to eliminate the effect of the electrical heating. The temperature of the environmental chamber is changed from 22°C to 38°C, and the voltage of the sensor is measured while it is biased with a constant current (300nA). The temperature data obtained from the PAV 200 system's chuck heater temperature controller unit and the total resistance values changing by the temperature are plotted in a graph and fitted to a polynomial (Figure 4.22 (a)). The TCR value of the detector is calculated using this polynomial (Figure 4.22 (b)).



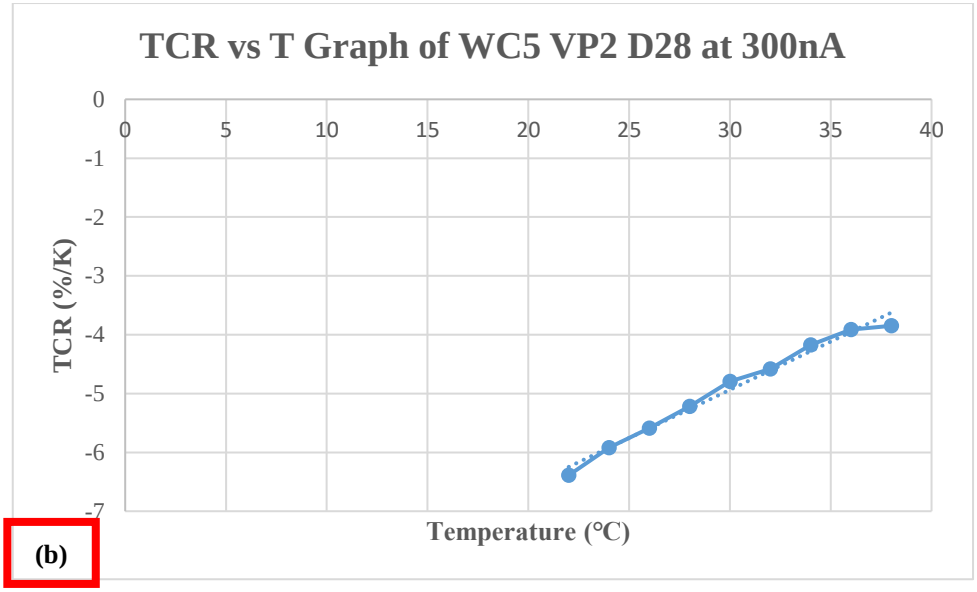


Figure 4.22. (a) Resistance and (b) TCR variation with the changing temperature. The TCR value at the room temperature is measured approximately as -5.5%/K.

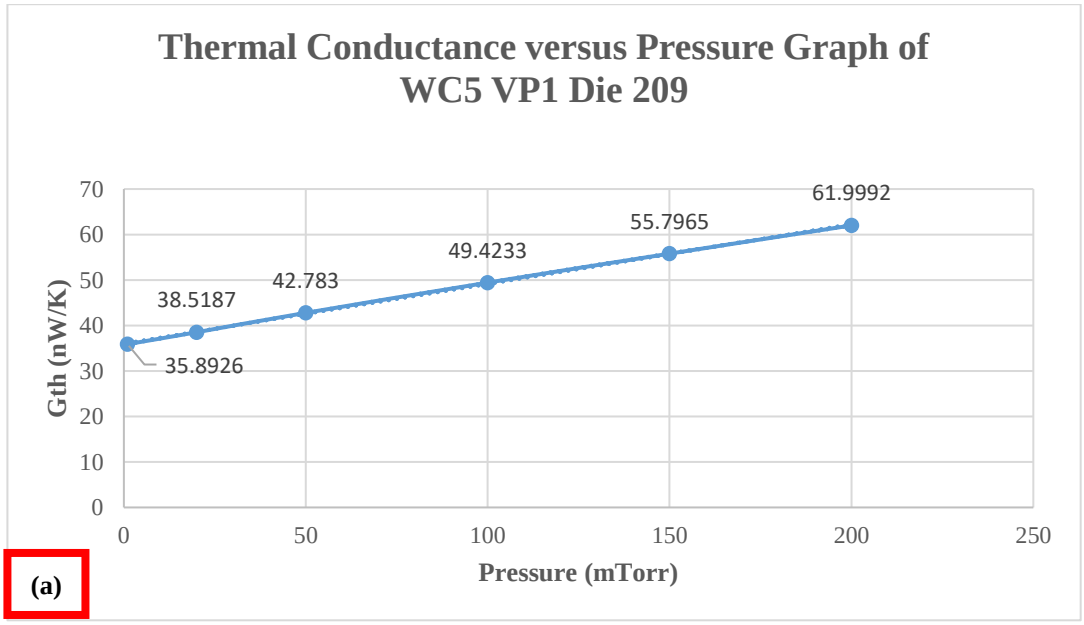
4.3.2.3 Thermal Conductance Measurements

The wafer level sacrificial released device sensors (Wafer C with vacuum sensors) vacuumed for the thermal conductance measurements in PAV 200 System and I-V sweep is performed in defined vacuum levels which are 1mTorr, 20mTorr, 50mTorr, 100mTorr, 150mTorr and 200mTorr; respectively. Then, by using the formula in the Equation 4.8 thermal conductance versus pressure plot for all the functional dies are plotted to obtain look-up table for to be reference after wafer level vacuum packaging.

$$G_{th} = \frac{P_{elec}}{\Delta T} = \frac{I^2 R \alpha}{\ln(\frac{R}{R_0})} \qquad (4.8)$$

where G_{th} is the thermal conductance of the detector, P_{elec} is the applied electrical power, ΔT is the total temperature change, R is the detector resistance under vacuum, R_0 is the detector resistance at atmospheric pressure, α is the TCR of the detector resistance, and I is the applied bias current. As an example, from WC5 and WC3 for 3 different sensor

designs two of the functional dies' (one from edge side and other from the middle side) characterization results are shown in the following Figures (Figure 4.23 – Figure 4.28).



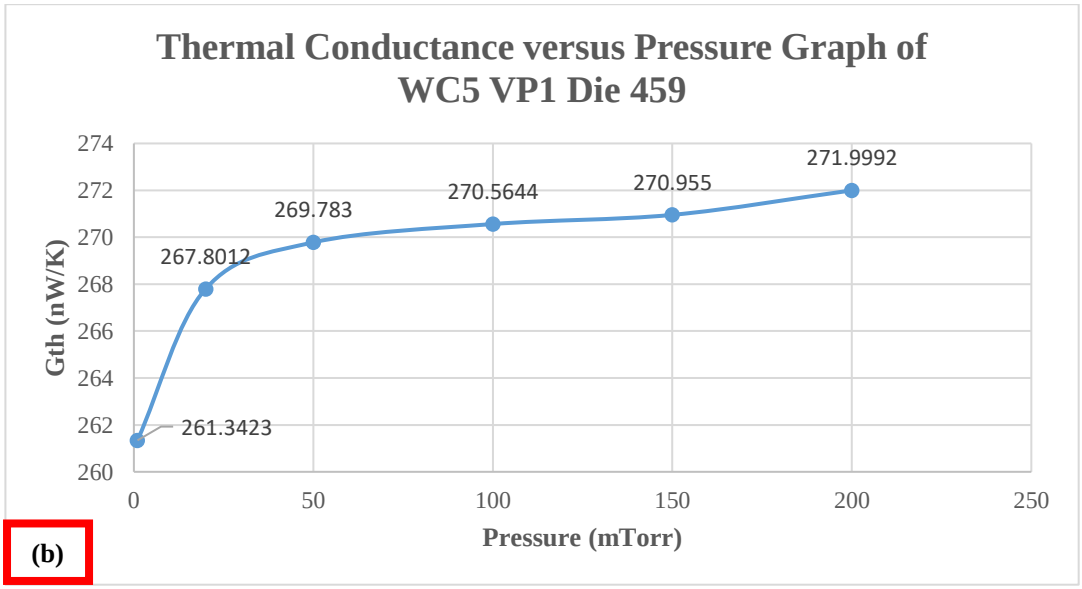
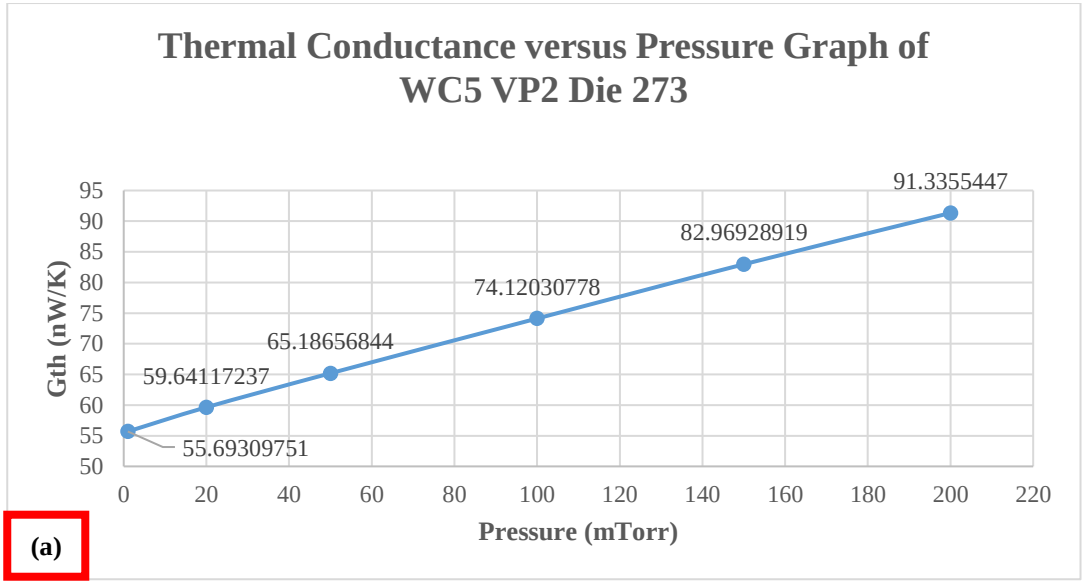


Figure 4.23. The thermal conductance value of WC5 VP1 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.



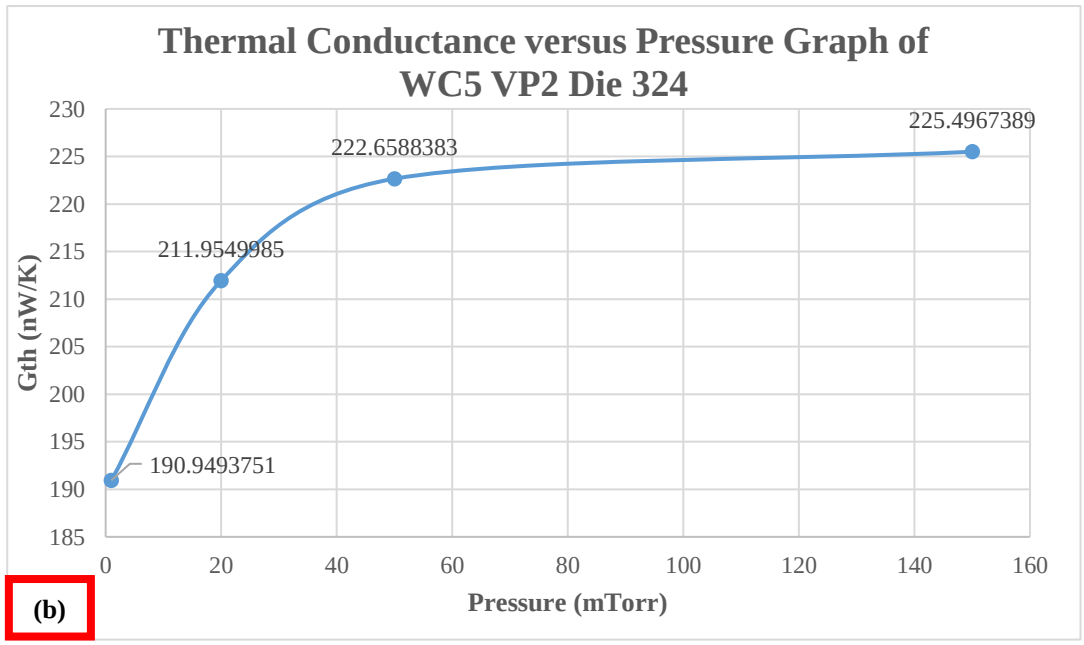
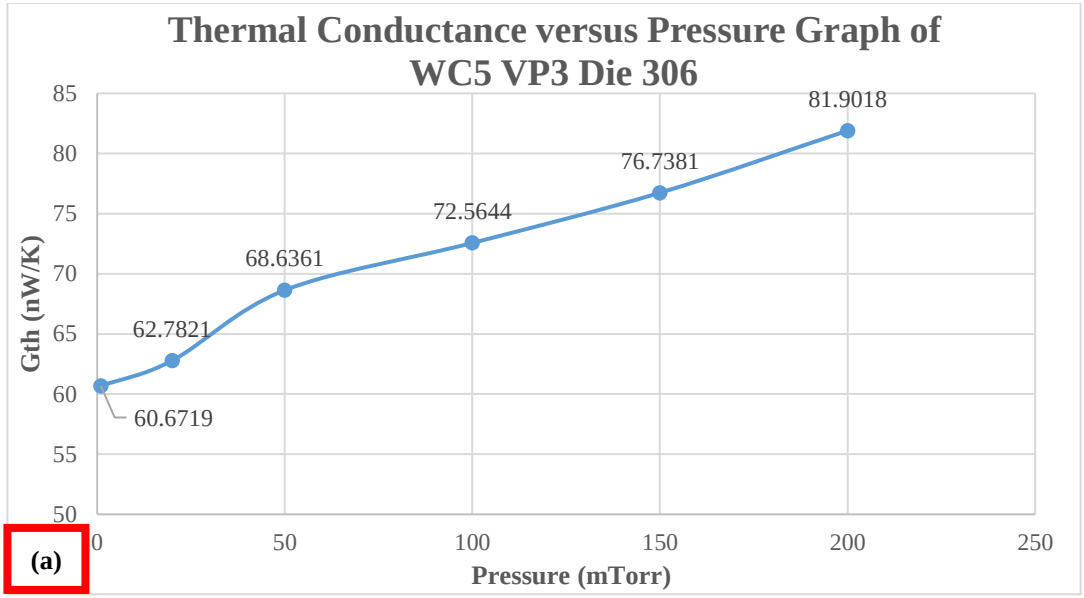


Figure 4.24. The thermal conductance value of WC5 VP2 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.



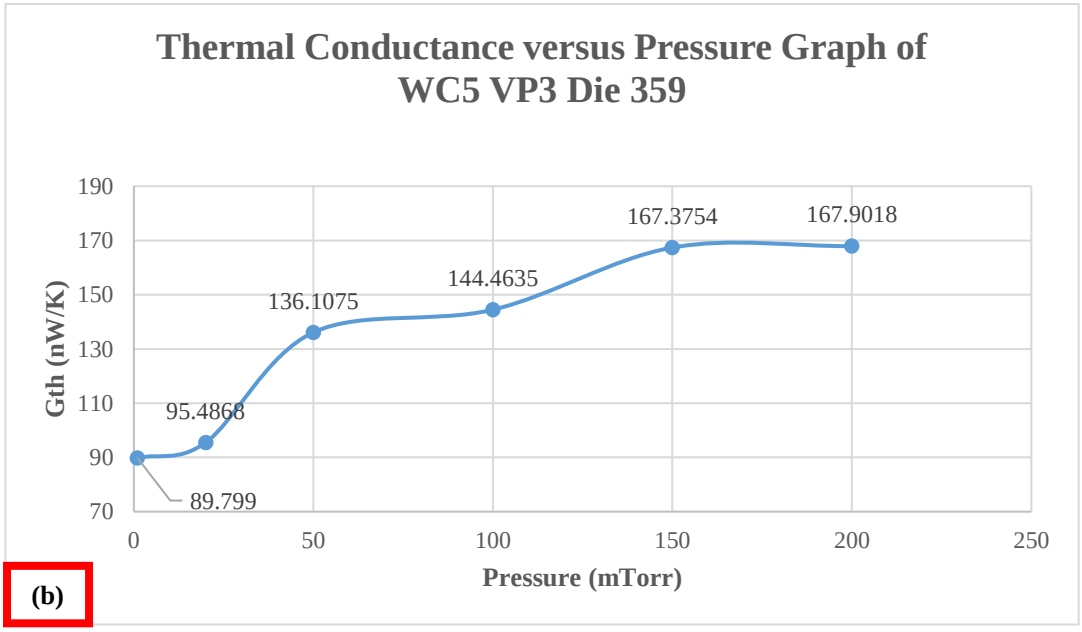
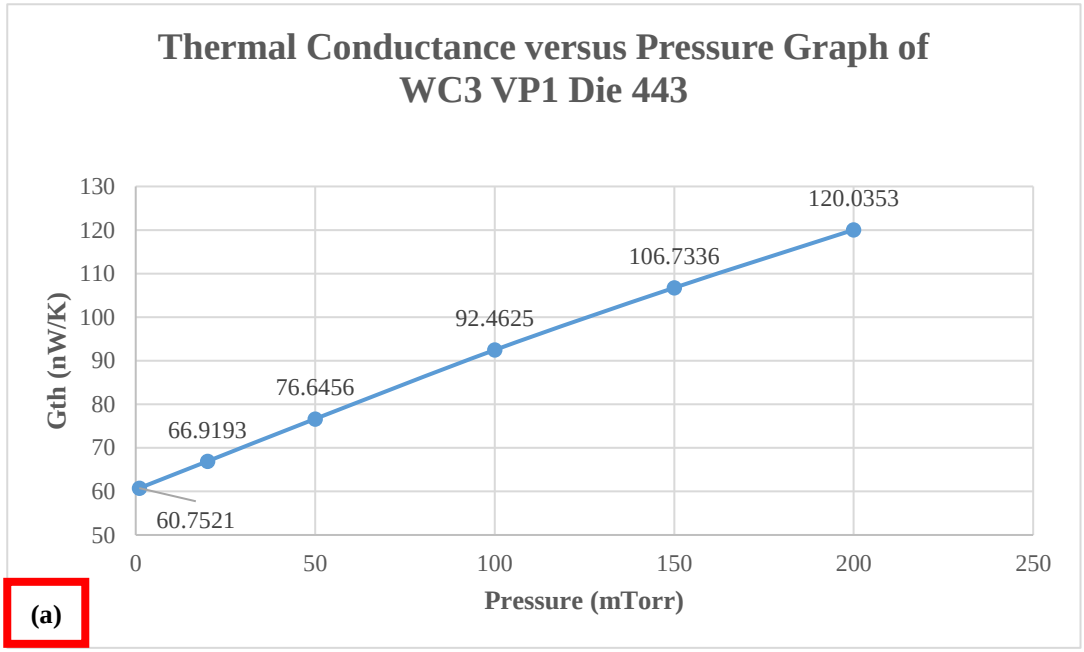


Figure 4.25. The thermal conductance value of WC5 VP3 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.



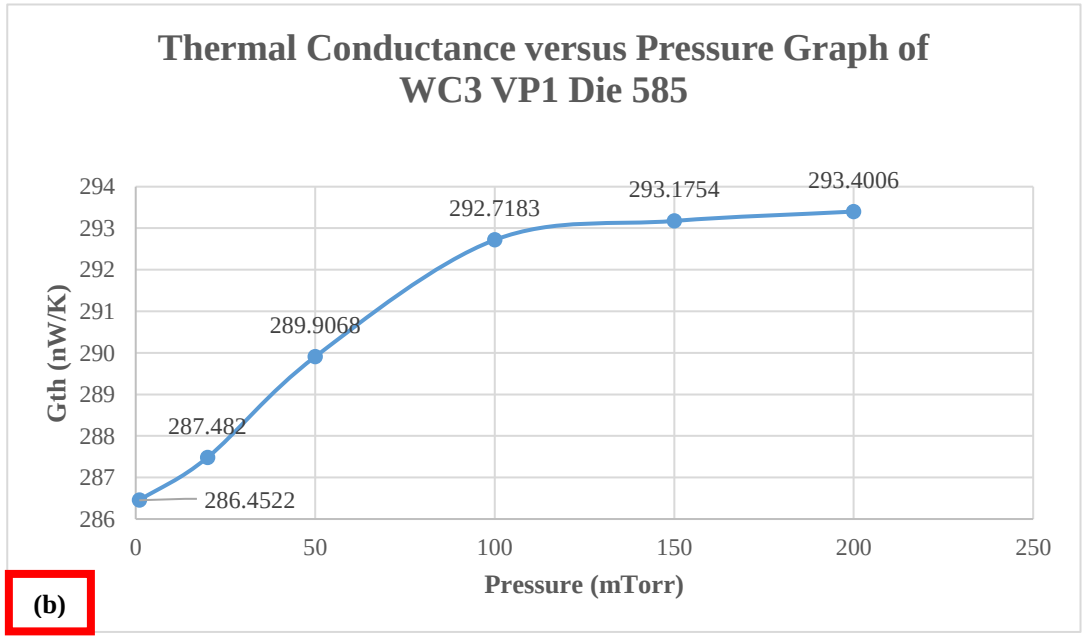
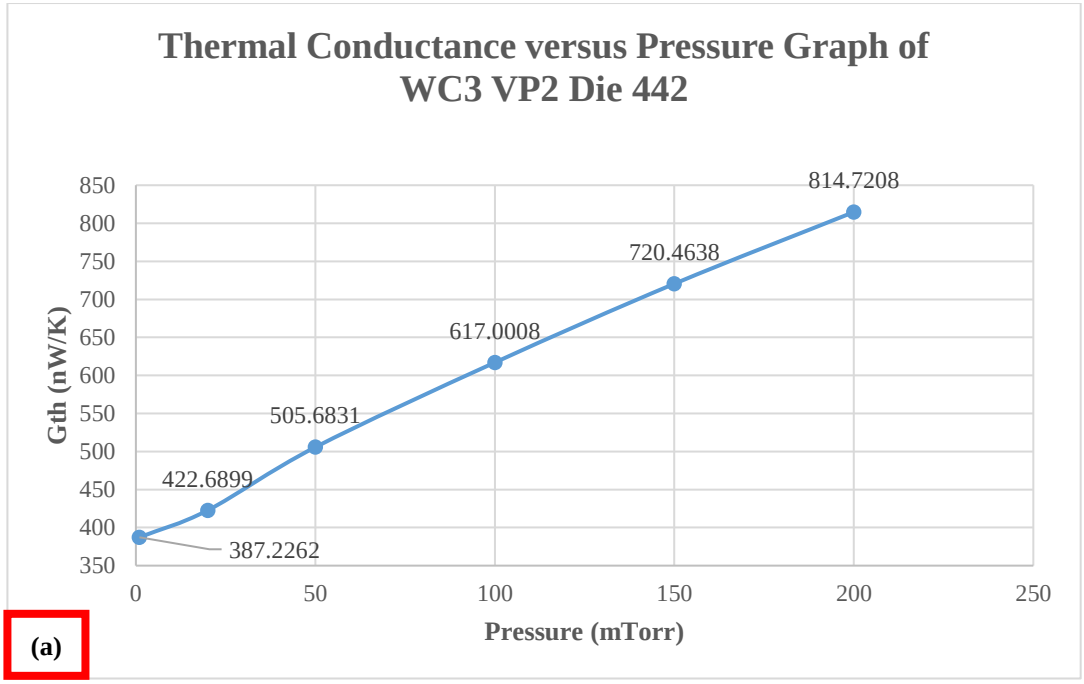


Figure 4.26. The thermal conductance value of WC3 VP1 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.



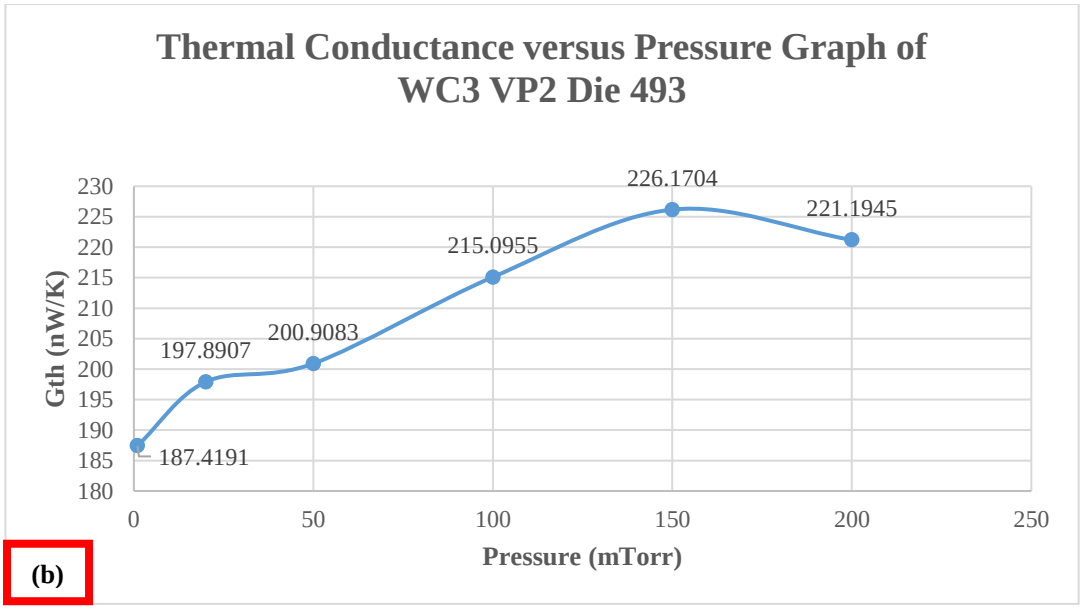
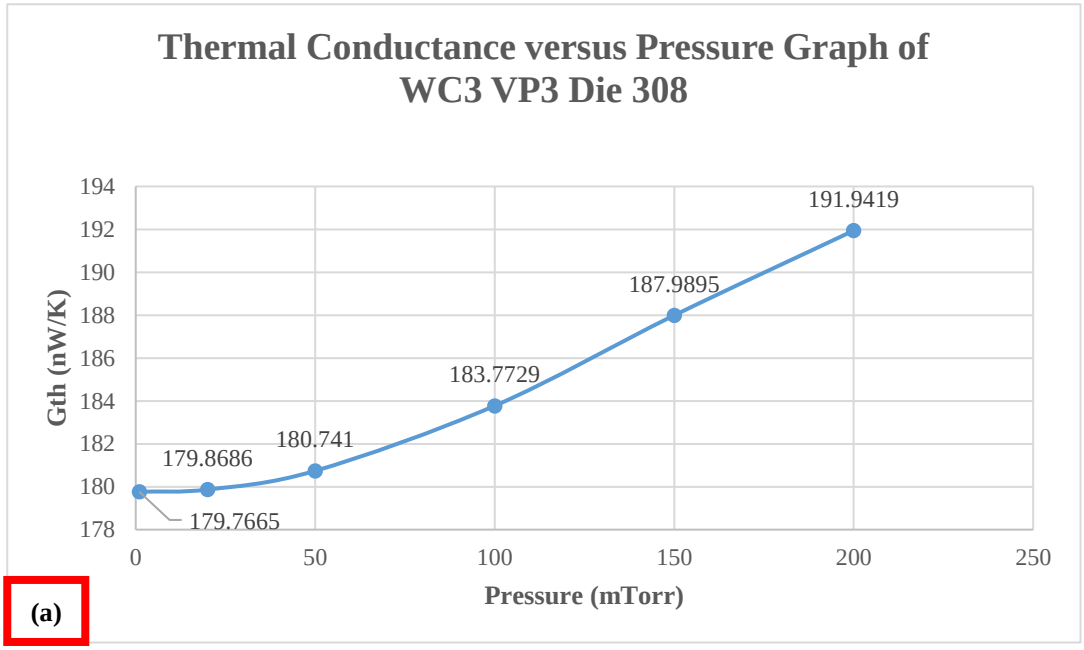


Figure 4.27. The thermal conductance value of WC3 VP2 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.



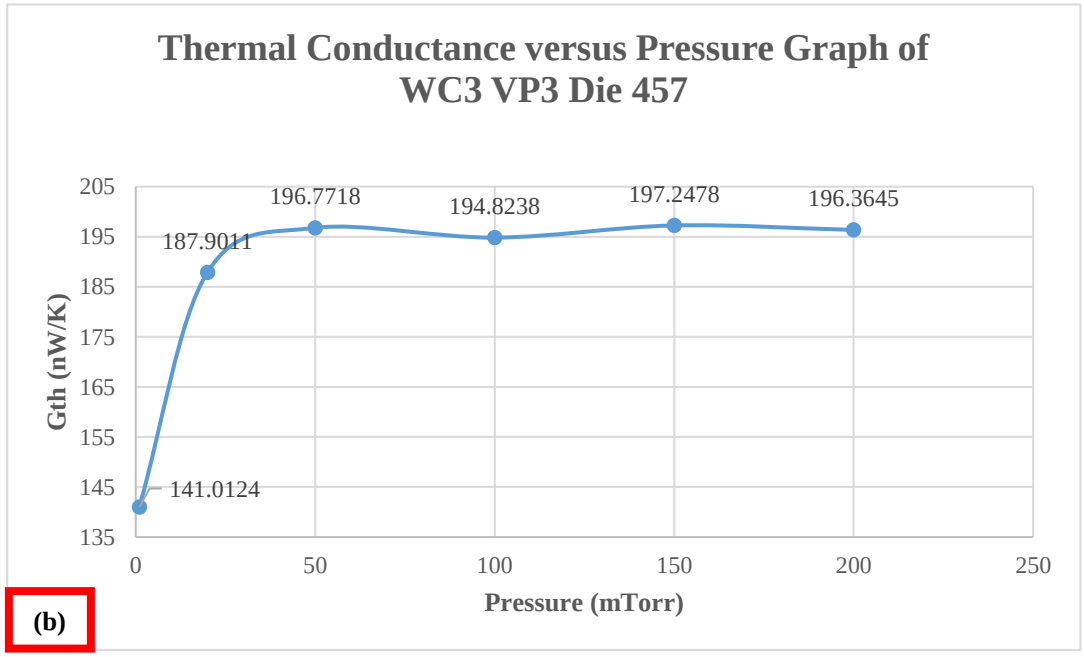


Figure 4.28. The thermal conductance value of WC3 VP3 one of the (a) edge side sensor and (b) middle side of the sensor with the changing vacuum levels.

In the wafer level for WC5 named device sensor it is observed that in the edge sides of the 8” wafer thermal conductance varies in the range of 35-120 nW/K whereas in the middle of the wafer it varies in the range of 90-280 nW/K which are a bit higher. Similarly, for WC3 named device wafer it is observed that in the edge sides of the 8” wafer thermal conductance varies in the range of 60-815 nW/K whereas in the middle of the wafer it varies in the range of 140-980 nW/K. It is considered that the sensors that differ from the measurements are caused by bending and twisting or due to defects in the structure due to the process. Also, this variation can be due to the different thermal conductivities of the layers caused by the nonuniformity of the 8” wafer because some systems are optimized for 4” or 6” but adapted to 8”.

4.3.3 Wafer Level Package Vacuum Check with Characterized Pirani Gauges

After the characterization of the Wafer C with Pirani Gauges (device wafer) and obtaining the thermal conductance versus pressure look-up table; it is time to apply glass frit bonding to the offered cap wafer technology and in-situ vacuum sensors. Notice that different from cap deflection characterization in Wafer C with the help of the shadow mask Ti getter is deposited to increase the vacuum level inside the package.

After the successfully wafer level packaged wafers (WC3 & WC5) are retested in PAV 200 System as described in section 4.3.2 but this time instead of vacuuming the chamber it is applied in atmosphere (Figure 4.29).

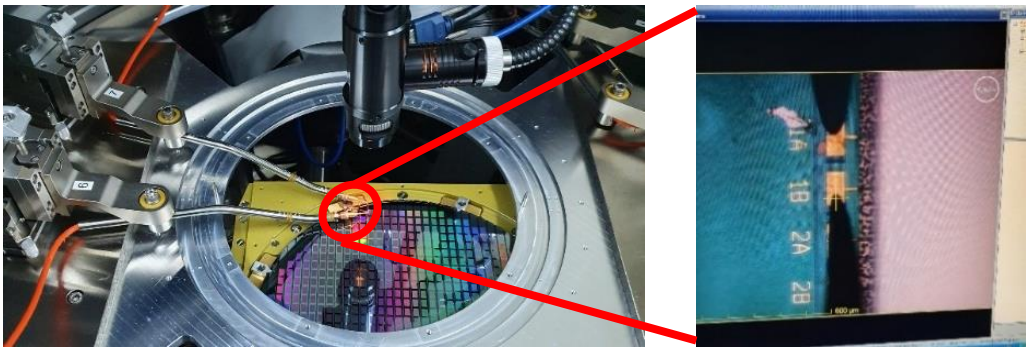
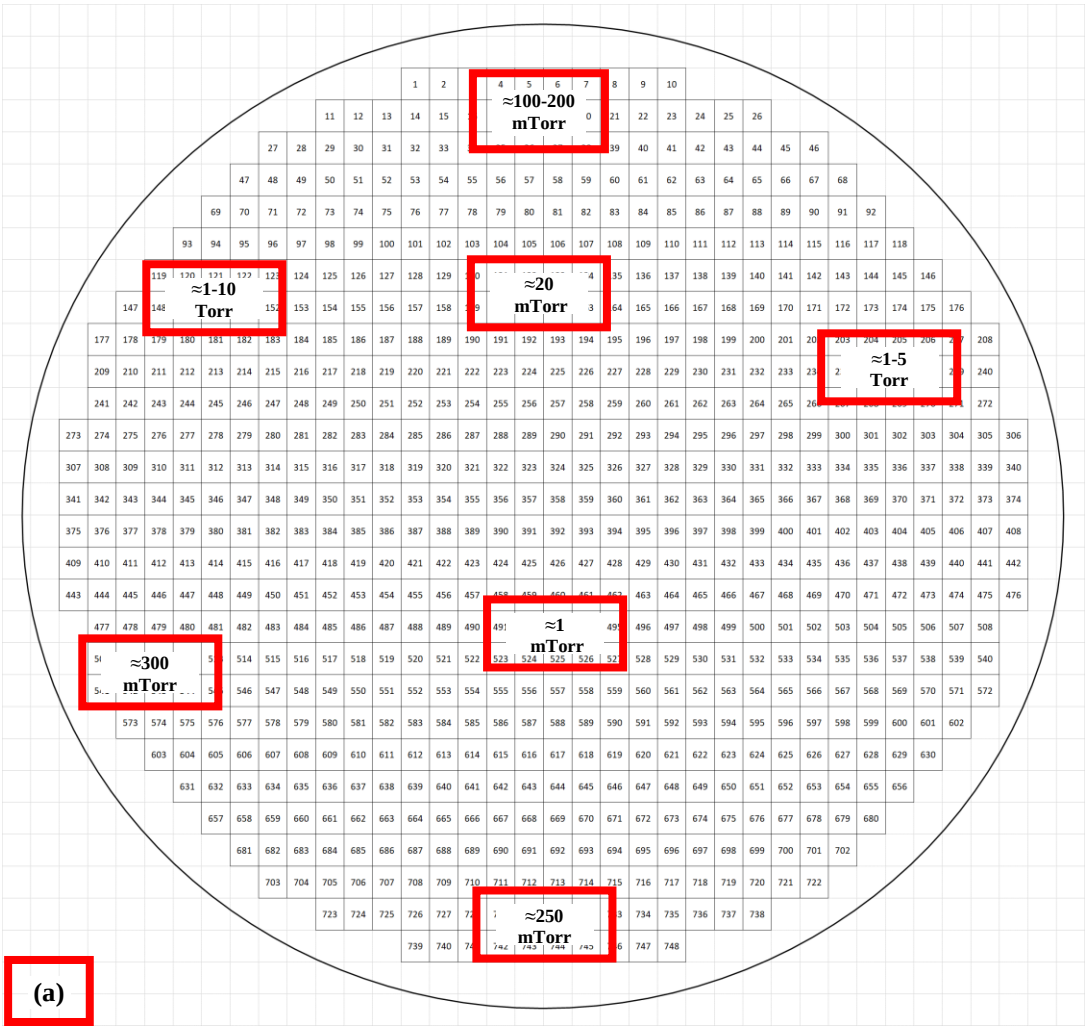


Figure 4.29. Cap wafers after WLVP tested with characterized in-situ vacuum sensors

Firstly, the sensor wafer 5 (WC5) is tested and the pressures ranging from 1 mTorr to 10 Torr are measured in the glass frit packages of sensor wafer 5 and less than or equal to 1 mTorr to 300 mTorr are observed inside sensor wafer 3 (WC3). Figure 4.30 present the performance measurements of glass frit bonded packages.



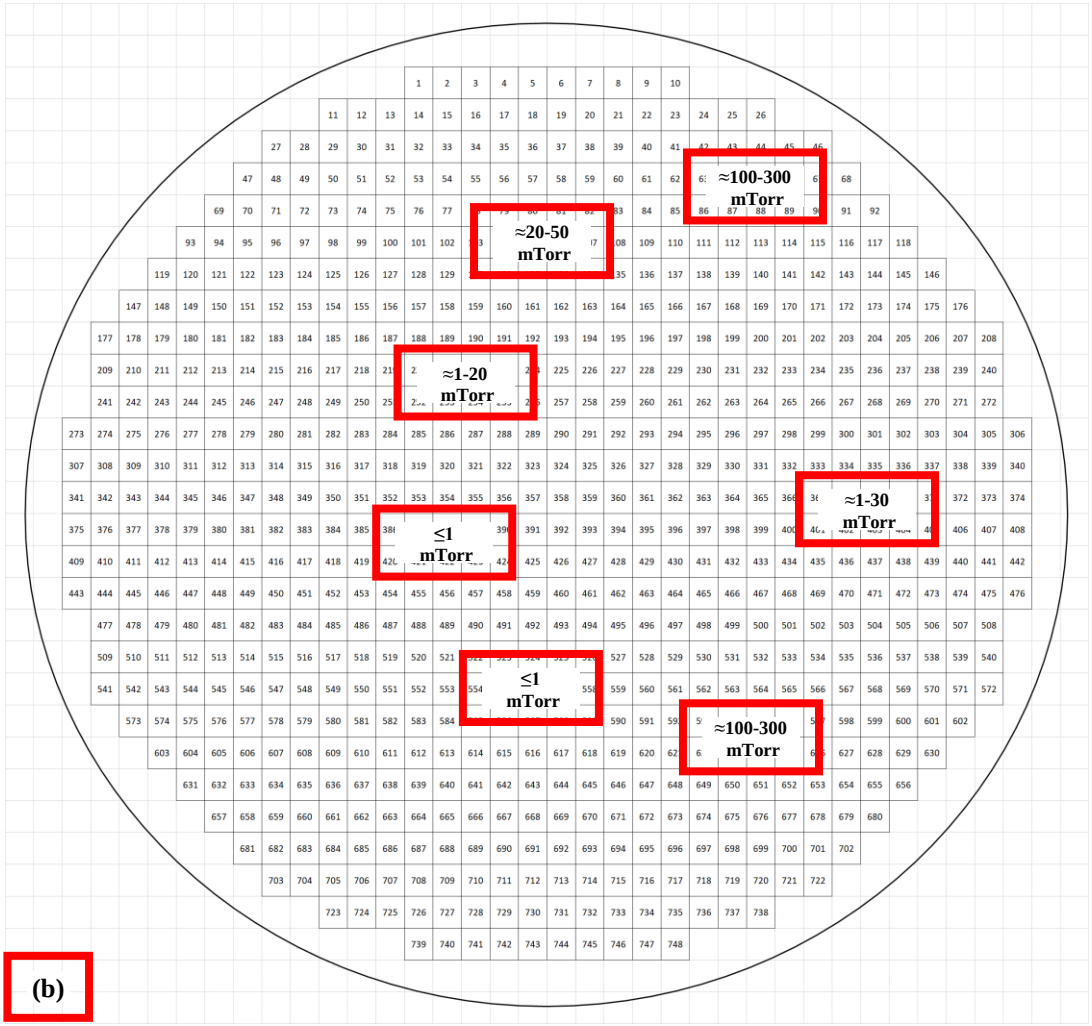


Figure 4.30. The measured pressure distribution over the (a) WC5 and (b) WC3 that are wafer level vacuum packaged using glass frit bonding with the offered cap technology.

To sum up, offered cap wafer technology is processed succesfully in 8” size wafers and characterized with 3 different methods. Table 4.4 presents the performance results of all wafer level vacuum packages fabricated by glass frit bonding including He-leak tests, cap deflection and in-situ sensors. Table 4.5 presents the comparison results of the WLVP Technology for MEMS Based Long-Wave Infrared Sensors with 400µm Thin Wafer and with standard wafer usage and grinding approaches. Table 4.6 summarizes the processes and pressure ranges of the Pirani gauges in the literature and in this work.

Table 4.4 The summary of wafer level vacuum packaging processes using glass frit bonding.

Wafer ID	***Packaging Process***	***Ti Getter***	***Cavity Depth***	***Leak Test Method***	***Vacuum Comments***
WD1	440°C, 2kN	No	200µm	He-Leak, Cap deflection	Mid. Vacuum Edges Not
WD2	440°C, 2kN	No	200µm	He-Leak, Cap deflection	Mid. Vacuum Edges Not
WD3	440°C, 2kN	No	400µm	He-Leak, Cap deflection	Vacuum
WC2	440°C, 2.4kN	No	200µm	He-Leak, Cap deflection	Vacuum
WC3	440°C, 2.4kN	Yes	200µm	In-situ vacuum sensors	Vacuum
WC5	440°C, 2.4kN	Yes	200µm	In-situ vacuum sensors	Vacuum

Table 4.5 The comparison results of the WLVP Technology obtained from two different wafer case usage.

The WLVP Technology for MEMS Based Long-Wave Infrared Sensors	**400µm Thin Wafer (Without Grinder)**	**Standard Wafer (After Grinding reduced to 200µm)**
LWIR Transmission	>80%	>80%
Cavity Depth (µm)	400	200
Surface Nonuniformity	Robust/polished	Nonuniform
Total Thickness (µm)	1125	925
Possible Microcracks	No	Yes
Easy Handling/Processing	No	Yes
Bonding Temperature (°C)	440	440
Average Shear Strength (MPa)	23.38	18.72
He Leak Check ($atm.cc/sec$)	$0.1x10^{-9}$	$1x10^{-8}$

Table 4.6 Tabulated Form of the Summary of Pirani Gauge Designs and This Work

Researcher	Gauge Type	Process Type	Pressure Range
Shie *et. al* [82]	Cr/Pt resistor on a dielectric membrane	Bulk Micromachining	10^{-7}- 1 Torr
Stark *et. al* [83]	Cr/Pt resistor on a dielectric membrane	Surface Micromachining with polysicilon sacrificial layer	10^{-3}- 10 Torr
Chae *et. al* [84]	Cr/Pt resistor on a dielectric membrane anchored to p++ silicon	Surface Micromachining with polysicilon sacrificial layer	$2x10^{-2}$- 2 Torr
Chae *et. al* [84]	p++ silicon coil microbridge	Dissolved wafer process	$5x10^{-2}$- 5 Torr
Mastrangelo and Muller [85]	Polysilicon microbridge	Surface Micromachining with n^{+} polysicilon sacrificial layer	$7.5x10^{-2}$ – 75 Torr
Stark *et. al* [86]	Polysilicon microbridge	Surface Micromachining with silicon dioxide sacrificial layer	10^{-2}- 100 Torr
Mitchel *et. al* [87]	Polysilicon microbridge	Surface Micromachining with silicon dioxide sacrificial layer	$5x10^{-2}$- 760 Torr
Topalli *et. al* [88]	p^{++} silicon coil microbridge	Dissolved wafer process	10^{-2}- 2 Torr
Topalli *et. al* [88]	100 µm thick silicon coil microbridge	Silicon-on-glass process	$5x10^{-2}$- 5 Torr
This Work	Pirani Resistive Gauge	Surface Micromachining	10^{-3} Torr- 10 Torr

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

The achievements and results obtained throughout this Ph. D. research can be summarized as follows:

1. The first branch of the work consists of investigation of Au-In metallic systems for TLP bonding, which is necessary for cavity openings and inserting subwavelength antireflection grating structures inside the cavity for transmission improvements. Differently in the scope of this work, instead of antireflective coatings, anti-reflection gratings including square grooves are integrated. This step is necessary because after cavity opening, processing gratings inside cavity in one wafer is not possible.
2. Grating structures are optimized. In single side polished (SSP) 8" wafer, bare Si at 8-12μm wavelength range transmission is 45% and for the processed wafers at 8- 12μm wavelength range transmission is around 60% so there is enhancement after processing the single side. In double side polished (DSP) bare Si at 8-12μm wavelength range transmission is 50% and for the processed wafers at 8-12μm wavelength range transmission is around 80-85% so there is enhancement after processing the double side.
3. Convenient reticle for cap wafer process lithography steps is designed, fabricated, process flows decided for 4 different (Wafer A-B-C-D cases) scenario and their processes completed successfully.
4. In our center for the first time in ASML Stepper front to back side alignment is tried and worked properly for Wafer A case.
5. After grating structures optimized for the wafer pairs metal deposition is done (Ti/Ni/Au and Ti/Ni/Au/In) and after performing successful lift-off process

the metal layers have been characterized in terms of structural, chemical, and thermal properties. Then bonding uniformity is characterized and bonding force is calculated accordingly. Similarly, after performing Au-In TLP bonding, the bonded wafer stack has been analyzed for characterization purposes in terms of structural and morphological investigation, elemental analysis, thermal analysis, and mechanical analysis. Notice that this characterization and experimental analysis is necessary for continuing the process in terms of cap cavity formation and glass frit bonding steps.

6. After alignment of Wafer A and Wafer B (725µm case) correctly by applying convenient recipe Au-In TLP bonding is done at 200°C; and after obtaining good bonding and being sure Au-In TLP bonding configuration is a correct choice with characterization and experimental analysis; for cavity opening purposes, the next step is thinning the bonded stack at first grinder then after applying cavity lithography steps etching the wafer in DRIE or using 400µm DSP Wafer (to eliminate the grinding step).
7. In our center for the first time grinding of the 8" bonded wafer stacks are tried.
8. In METU MEMS Center, till the proposed cap wafer trials never 8" size chuck installed, and processes done before, so with the help of new superuser and technical personnel 8" size compatible chuck changed as the Work Chuck. Then, several processes with 8" Single Wafer Processes are done. After dummy wafers thinning achieved successfully as a next step Au-In TLP Bonded Wafer A+B Stacks are thinned and written recipes worked properly. During the grinding process the stacks' thicknesses are thinned from 1450µm to 875µm successfully in written 3 step recipe which are: 1) from 1450µm to 1240µm at 650rpm with 2.0µm/s speed; 2) from 1240µm to 1025µm at 640rpm with 2.0µm/s speed; and 3) from 1025µm to 875µm at 650rpm with 3.0µm/s speed.
9. Wafer bonding experiments are tried for both standard 725µm thick Wafer A to 725µm thick Wafer B and 725µm thick Wafer A to 400 µm thin Wafer B;

and all wafer bonding experiments worked properly. The thickness of the cap wafer is a tradeoff between the need to minimize the absorption of the incoming IR radiation and not only the requirements for low wafer bow introduced by the stress in the deposited films but also for safe handling during the process. Also, in thin wafer usage 400μm depth must be etched for cavity opening in DRIE.

10. After the DRIE cap cavity formation protection nitride and etch stop oxide removed in BHF and squeezed out indium is cleaned in HCl solution.
11. After the successful cap cavity formation, the second branch of the work is screen-printing glass paste to the cavity opened cap wafer for glass frit bonding purposes.
12. The glass frit bonding process consists of three major steps which are screen printing of a glass paste, thermal conditioning or frit firing and thermo-compressive bonding. For screen printing step the necessary equipment can be listed as glass paste, screen including polyester meshes, flood and print squeegee with suitable squeegee rubber and obviously cap wafer, and screen printer. As the first step, Ferro FX11-036 glass paste is selected because it is the most widely used glass paste in MEMS industrial applications. Besides, it is not only provided as ready to use paste but also non-crystallizing glass frit material. After the decision of the glass paste the next step is screen design and ordering. According to the drawn screen layout, screens are produced from BRAVE and PVF companies.
13. After ordering screens and glass pastes, for the first time in our Center instead of sending wafers abroad (never 8” size processed before) METU GÜNAM-Center for Solar Energy Research and Applications’ Ekra Model screen printer is observed and after 8” size compatible equipment is produced in METU MEMS Center’s machine shop, screen-printing trials and optimizations are started.

14. After integrating the ordered and custom designed equipment to METU GÜNAM Research Center's Ekra Model screen printer it is ready for offered cap wafer's screen-printing trials.
15. After performing successful screen printing to the cap wafer; for frit firing step the necessary equipment can be listed as screen printed cap wafer and high temperature oven. The Carbolite Gero High Temperature Oven is purchased to METU MEMS Center for that purpose and recipe is written for frit firing.
16. For getter deposition purposes 6" and 8" size compatible shadow masks are produced and over deposition to the unwanted regions problem is solved by using BESTEC-2 sputtering system and vacuum level is satisfactory.
17. The calculation of bonding force is based on the design parameters and proposed cap wafer process mask set is designed using the L-Edit design software and in proposed design the bonding area is calculated as 3058mm^2 for 8" size screen printed and frit fired wafer.
18. After performing successful screen-printing and frit firing the glass paste layers have been characterized in terms of structural, chemical, and thermal properties. Similarly, after performing glass frit bonding, the bonded wafer stack has been analyzed for characterization purposes.
19. For monitoring micro packaged pressures 3 different methods are applied which are He Leak tests, cap deflection and in-situ vacuum sensors.
20. According to He Leak tests, the hermeticity of the bonds that were measured as 0.1x10^{-9} $atm.cc/sec$ provides the requirement of MIL-STD 883standard.
21. According to cap deflection, without getter the vacuum level inside the package is about 5 mbar, 3.75 Torr. Experimental results also are verified with COMSOL simulations.
22. Resistor type micro-vacuum sensors (Pirani Gauges) with using METU MEMS Center clean room facilities are produced as a device wafer and after suspension they are characterized in a controlled vacuum chamber to obtain

look-up table (thermal conductance versus pressure plots from 1atm (760 Torr) to 1 mTorr).

23. After glass frit bonding of offered cap wafer and device wafer; pad reveal successfully done and vacuum packages re-tested in probe system to evaluate the packages vacuum with the previously characterized Pirani Gauges and measured in the range of 20mTorr to 2 Torr.

As can be seen above listed items are required an enormous effort and results are promising. There are still some items that need to be studied and as a future work:

1. In order to control the squeezed out In micro-grooves can be added to layout and new reticle can be produced.
2. In DRIE for the offered cap wafer during the cap cavity opening diaphragms are exploded and this may destroy the gratings' transmittivity so alternative method can be considered or safer solution can be thought.
3. In order to control the spillages of glass frit during the bonding process we can also insert the micro grooves both inside and outside the glass frit bonding layer.
4. In our case glass frit is out of expire date (05/2019) so fresh frit can be tried.
5. Pb based glass frit is hazardous for human health so other versions of glass frit can be tried.
6. Wafer level release problem must be solved to eliminate the stiction problem of the pixels in Wafer C case.
7. Stress free mechanical designs can be taken into consideration and new versions of the vacuum sensors can be developed.
8. Glass frit and gold have an interaction at high temperatures. This interaction causes gold to lose its conductivity. Shorter holding periods minimizes the problem but could not solve it completely. Using a passivation layer between the gold and glass frit may prevents their interaction.

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APPENDICES

A. MATLAB CODE FOR G^{th} CALCULATION

```
clear
close all
%% Import data from spreadsheet
% Script for importing data from the following spreadsheet:
%
%    Workbook: \\mems\Genel\Gulsah\GDA_PHD\PAV Characterization of
WCs\WC5\WC5_VP1\220521_MS0835A1_W5_1_Characterization\220521_19_29_
MS0835A1_W5_Characterization_1_20_50_100_150_200.xlsx
%    Worksheet: 220521_19_29_MS0835A1_W5_Charac
%
% Auto-generated by MATLAB on 27-May-2022 13:58:31

%% Set up the Import Options and import the data
opts = spreadsheetImportOptions("NumVariables", 26);

% Specify sheet and range
opts.Sheet = "220803_10_26_MS0835A1_W051_Vacu";
opts.DataRange = "A1:Z749";

% Specify column names and types
opts.VariableNames = ["WaferNo", "DieNo", "Short", "Voltage",
"Current", "sVAC00nA", "sVAC1150nA", "sVAC2300nA", "sVAC3450nA",
"sVAC4600nA", "sVAC5750nA", "sVAC6900nA", "sVAC71050nA",
"sVAC81200nA", "sVAC91350nA", "sVAC101500nA", "sVAC111650nA",
"sVAC121800nA", "sVAC131950nA", "sVAC142100nA", "sVAC152250nA",
"sVAC162400nA", "sVAC172550nA", "sVAC182700nA", "sVAC192850nA",
"sVAC203000nA"];
opts.VariableTypes = ["double", "double", "categorical", "char",
"double", "double", "double", "double", "double", "double",
"double", "double", "double", "double", "double", "double",
"double", "double", "double", "double", "double", "double",
"double", "double", "double", "double"];

% Specify variable properties
opts = setvaropts(opts, "Short", "EmptyFieldRule", "auto");

% Import the data
table1 = readtable("\\10.0.20.4\Genel\Gulsah\GDA_PHD\PAV
Characterization of
WCs\WC5\WC5_VP1\MS0835A1_W051_Vacuum_Check\220803_10_26_MS0835A1_W0
51_Vacuum.xlsx", opts, "UseExcel", false);


%% Clear temporary variables
clear opts
```

```
%%
currents=[0 150 300 450 600 750 900 1050 1200 1350 1500 1650 1800
1950 2100 2250 2400 2550 2700 2850 3000];

cnt1=1;
cnt2=1;
ind1=3;

for ind1=2:size(table1,1)
    dum1=table2array(table1(ind1,6:26));
    data1.DieNo(ind1-1,1).array=dum1;
end

x=currents*1e-9;
ind1=1;
working_dies=[];

while true
    y=data1.DieNo(ind1,1).array;
    plot(x,y);
    title(['Die No=' num2str(ind1) ' number of selected dies='
num2str(size(working_dies,1))]);
    [x1 y1 button]=ginput(1);
     if button==29
        ind1=ind1+1;
        if ind1>size(data1.DieNo,1)
            ind1=size(data1.DieNo,1);
            beep;
            break;
        end
    end
    if button==28
        ind1=ind1-1;
        if ind1<1
            beep;
            ind1=1;
        end
    end
    if button==31
        if ~ismember(ind1,working_dies)
            working_dies=vertcat(working_dies,ind1);
        end
        ind1=ind1+1;
        if ind1>size(data1.DieNo,1)
            ind1=size(data1.DieNo,1);
            break;
            beep;
        end
    end
    %if(ind1>50) break;end;
end
```

```
save('\\10.0.20.4\Genel\Gulsah\GDA_PHD\PAV Characterization of
WCs\WC5\WC5_VP1\MS0835A1_W051_Vacuum_Check\working_dies1.mat','data
1','working_dies');


%% calculation of Gth values
if true %true
    tcr=0.05;
    currents1=currents';
    for i=1:size(working_dies,1)
        volts=data1.DieNo(working_dies(i,1),1).array';
        number_of_points=length(volts);
        %DÃ¼sÃ¼k akimdaki (r0) ve yÃ¼ksek ak?mdaki (r1) direnci bul
        r1=zeros(1,number_of_points-1);
        r0=mean(volts(2:4,1)./currents1(2:4,1),'omitnan');
        %Gth de?erini hesapla
        gth=nan*ones(number_of_points-1,1);
        for k=2:number_of_points
            r1(1,k-1)=volts(k,1)./currents1(k,1);
            gth(k-1,1)=-tcr*(currents1(k,1).^2)*r1(1,k-
1)/log(r1(1,k-1)/r0);
        end
        Gth=mean(gth(number_of_points-5:number_of_points-1,1));
        data1.DieNo(working_dies(i,1),1).Gth=Gth;
    end
end

save('\\10.0.20.4\Genel\Gulsah\GDA_PHD\PAV Characterization of
WCs\WC5\WC5_VP1\MS0835A1_W051_Vacuum_Check\working_dies1.mat','data
1','working_dies');



'geldi'
```

CURRICULUM VITAE

PERSONAL INFORMATION

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EDUCATION

Degree	Institution	Year of Graduation
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BS	Atılım University Mechatronics Engineering	2012
BS	Anadolu University Business Administration	2012
High School	Sokullu Mehmet Paşa High School, Ankara	2007

WORK EXPERIENCE

Year	Place	Enrollment
2012-Present	METU MEMS CENTER	Senior Research Engineer
2011-2012	Atılım University Mechatronics Engineering	Student Research Assistant
2011 July	TAI	Intern Eng. Student
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FOREIGN LANGUAGES

Advanced English

PUBLICATIONS

1. G. Demirhan Aydin and T. Akin, “Resonance-Based Temperature Sensors using a Wafer Level Vacuum Packaged SOI MEMS Process,” *Adv. Mater. Lett.*, 11 (1), 20011462 (1-8), Jan. 2020. 10.5185/amlett.2020.011462

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