COLUMN PARALLEL INCREMENTAL ZOOM ADC FOR UNCOOLED IMAGING APPLICATIONS

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ABSTRACT

COLUMN PARALLEL INCREMENTAL ZOOM ADC FOR UNCOOLED IMAGING APPLICATIONS

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This thesis presents a new column-parallel analog to digital converter (ADC) integrated circuit with high precision (20-bit), high signal-to-noise ratio (119.5 dB), low power incremental Zoom ADC architecture and demonstrates its integration to a 384x288 pixel format analog output microbolometer readout integrated circuit (ROIC) with 25μm pixel pitch.

The Zoom ADC is a hybrid of a low-resolution successive approximation register (SAR) ADC and a high-resolution Delta-Sigma ADC. The main aim of this design is to decrease the power consumption and oversampling ratio (OSR) of the ADC while preserving the high resolution. The designed Zoom ADC consists of a 5-bit SAR ADC, a second-order Delta-Sigma Modulator, and digital filters. The SAR ADC performs the coarse conversion and defines the most significant bits (MSBs), while the Delta-Sigma Modulator performs fine conversion to the residue voltage from the SAR ADC. Digital filters eliminate high-frequency noises and convert modulated data to parallel outputs. These three blocks and column readout circuits

work with a pipeline chain, increasing sampling rate and decreasing the power consumption. The ADC has a programmable digital filter; thus, the ADC can work with different frame rates and resolutions. The designed ADC has four operation modes: the 20 FPS high-resolution mode, 30 FPS standard mode, 50 FPS fast mode, and 200 FPS ultrafast mode.

The ADC design is implemented in a standard 0.18μm CMOS technology. The ADC has 400 columns with a 50 μm pixel pitch, where a single column of the ADC has a 2.4 mm height and covers a 0.12 mm^2 area. The ADC provides a 124.5 dB dynamic range (DR) and a 122 dB signal-to-noise ratio (SNR) in the high-resolution mode. The effective number of bits (ENOB) is 20.1, and the DNL is below 0.5 least significant bit (LSB). The sampling rate is 6KS/sec, and the ADC consumes 358 μW power. The ADC can be programmed to reach sampling speed up to 60KS/sec for high frames per second (FPS) imaging, called ultrafast mode. The ADC provides 99.2 dB dynamic range (DR) and 98 dB signal-to-noise ratio (SNR) in the 200 FPS ultrafast mode, where the effective number of bits (ENOB) reduces to 16.1 and the power consumption increases to 751 μW.

Keywords: Analog to Digital Converter, Zoom ADC, Delta-Sigma ADC, Uncooled imaging, Readout Integrated Circuit

ÖZ

SOĞUTMASIZ GÖRÜNTÜLEME SİSTEMLERİ İÇİN KOLON PARALEL ARTIMLI ZOOM ANALOG-SAYISAL ÇEVİRİCİ

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Bu tezde, yeni bir kolon paralel analog sayısal çevirici (ADC) tümdevresi sunulmaktadır. Sunulan düşük güç tüketimine sahip artımlı kolon paralel Zoom ADC mimarisi yüksek çözünürlük (20 bit) ve yüksek işaret gürültü oranı (119.5 dB) sağlamaktadır. Tasarlanan ADC 384x288 piksel formatlı ve 25µm piksel aralıklı mikrobolometre tümleşik okuma devresine (ROIC) gerçeklenmiştir.

Zoom ADC düşük çözünürlüklü SAR ADC ve yüksek çözünürlüklü Delta-Sigma ADC'nin hibritlenmesi ile oluşur. Bu tasarımın ana amacı ADC'nin çözünürlüğünü düşürmeden güç tüketimini ve örnekleme oranını (OSR) düşürmektir. Tasarlanan Zoom ADC, 5-bit SAR ADC, ikinci derece Delta-Sigma modülatör ve sayısal filtrelerden oluşmaktadır. SAR ADC en önemli bitleri (MSB) belirler ve oluşan kalıntı voltajı Delta-Sigma modülatör tarafından hassas bir şekilde sayısal sinyale dönüştürülür. Sayısal filtreler yüksek frekanstaki gürültüleri temizler ve modüle edilmiş verileri paralel veriye çevirir. Bahsedilen üç blok ve kolon okuma devresi

ardışık okuma zinciri ile çalışarak örnekleme oranını arttırır ve güç tüketimini düşürür. ADC programlanabilir sayısal filtreye sahiptir ve bu sayede farklı çerçeve hızlarında ve çözünürlüklerde çalışabilir. Tasarlanan ADC'nin dört çalışma modu bulunmaktadır: 20 FPS yüksek çözünürlük modu, 30 FPS standart mod, 50 FPS hızlı mod ve 200 FPS ultra hızlı mod.

Tasarım 0.18 µm CMOS teknolojisi ile gerçeklenmiştir. ADC, 50 µm piksel aralığına sahip 400 kolona sahiptir. ADC'nin bir kolonu 2.4 mm yüksekliğe sahiptir ve 0.12 mm^2 alan kaplamaktadır. Yüksek çözünürlük modunda ADC 124.5 dB dinamik aralık (DR) ve 122 dB işaret gürültü oranı (SNR) sağlamaktadır. DNL değeri 0.5 LSB'nin altında olup etkin bit sayısı (ENOB) 20.1'dir. ADC'nin örnekleme hızı 6KS/sec olup, 358µW güç tüketmektedir. Yüksek saniye başına fotoğraf (FPS) uygulamalar için, ADC ultra hızlı modda kullanıldığında 60KS/sec örnekleme hızına çıkabilmektedir. Ultra hızlı modda ROIC 200 FPS'te çalışmakta ve ADC 99.2 dB dinamik aralık (DR) ve 98 dB işaret gürültü oranı (SNR) sağlamaktadır. Ultra hızlı modda etkin bit sayısı (ENOB) 16.1 e düşmekte ve güç tüketimi 751µW a yükselmektedir.

Anahtar Kelimeler: Analog-Sayısal Çevirici, Zoom Analog-Sayısal Çevirici, Delta-Sigma Analog-Sayısal Çevirici, Soğutmasız Görüntüleme, Tümleşik Okuma Devresi

To my family

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CHAPTER 1

INTRODUCTION

Visual interaction with the environment holds an essential role in modern life. The semiconductor and camera technology advancements extended this interaction to a new level. Cameras display the environment in the visible spectrum and extend their vision to the infrared (IR) and ultraviolet (UV) spectrum. Detecting IR radiation enables humans to expand their vision to the darkness. Thermal (Longwave IR) imagers can detect electromagnetic radiation emitted by objects. This ability provides an advantage in the absence of illumination and enables seeing in total darkness.

Today thermal imaging systems are utilized in many commercial and military applications. There is a tremendous effort to provide the best solution for the user in terms of performance, cost, and ease of use. Typically, two types of detectors can sense thermal radiation [1]. The first type is photon detectors, where the incident radiation is absorbed by the detector and directly converted to an electrical signal. This signal is collected by readout for electronic processing. Photon detectors provide fast response and higher sensitivity levels [2]. However, photon detectors can only achieve high performance under cryogenic temperatures, such as 77K or lower. Because of that, they are also referred to as cooled detectors. For reaching cryogenic temperatures, special and expensive cooling systems are used. These cooling systems increase the cost of the camera heavily and decrease the system's mobility.

The second type is thermal detectors, where the incident radiation heats the detector, and the change of temperature on the detector is measured with a readout circuitry. This indirect conversion makes thermal detectors operate at room temperature, removing the need for a cooling system [2]. Because of that, they are referred to as uncooled detectors. On the other hand, the indirect conversion of incident radiation to electrical signal decreases the performance and speed of the imager significantly. Thermal detectors provide low-cost, low-power, and more compact thermal imaging for reduced performance.

In uncooled thermal imaging, two types of sensors are widely used, thermopiles and microbolometers. Microbolometer cameras are widely used for large array imaging, and significant advancements have been achieved in uncooled imaging technology with microbolometer technology [1]. Microbolometer cameras have found a wide area of use due to their smaller size, low cost, and large array format. Today microbolometer cameras are used in military, industrial and commercial applications, including night vision, medical imaging, temperature monitoring, and reconnaissance. Although the lower cost and good imaging quality of microbolometer cameras, the system cost is still high for many applications. There is a tremendous effort to develop high-performance and low-cost uncooled cameras to reach high-volume markets.

In the development of microbolometer camera systems, the design of the readout integrated circuit (ROIC) held a crucial role. As ROIC is the first interface to the detector, where changes in the detector material are converted to electrical signals, the performance and cost of the system strongly depend on the design of ROIC. Today, most systems use digital output due to its lower cost and ability to process complex data. Hence, digitalization of the ROIC output is essential for most applications. Traditionally, an external analog to digital converter is used on the PCB level for digitalization. Despite the PCB-level digitalization design being

straightforward, extra buffers and connections introduce noise and power consumption. Furthermore, the system size and cost increase with the addition of every component. Integrating the ADC into the ROIC can obtain higher performance and lower system costs.

On-chip ADCs do not need extra connection circuits and components. They can perform digitalization with lower input-referred noise and lower power consumption. On the other hand, embedding ADC to the ROIC creates new challenges, especially chip-area and power consumption. Hence, one must analyze the imaging system as a whole to reach the most efficient digitalization method. Since the readout circuit design defines the ADC's sampling frequency, bit precision, and operation range, an optimal conversion solution can be achieved with different ADC architectures for different readout methods. Microbolometer ROICs work as rolling shutter imaging and require high precision and low power ADC. This thesis aims to design and implement a column-parallel Zoom ADC integrated circuit for rolling shutter imaging applications.

This chapter briefly explains the operation of the digital output microbolometer ROIC. Section 1.1 introduces the microbolometer detectors' operation principle and the readout circuit's design. Section 1.2 briefly explains ADC performance parameters and shows different ADC architectures. Section 1.3 states the thesis's motivation and the proposed design's goals. Finally, Section 1.4 shares the research objectives and organization of the thesis.

1.1 Microbolometers

Microbolometer detectors are one of the most famous approaches for uncooled thermal imaging [3]. A microbolometer detector is formed by a temperature-dependent resistor and IR absorber. The incident thermal radiation is absorbed by the IR absorber and increases the temperature of the bolometer. The bolometer heating changes the electrical properties of the temperature-sensitive material [4]. Hence, the incident radiation is detected by measuring changes on the detector. Microbolometer detectors are manufactured using MEMS processes, most commonly using surface or bulk micromachining processes.

The physical structure of the microbolometer detector is shown in Figure 1.1 [5]. The microbolometer detector is fabricated as a bridge-like structure suspended on the readout circuit to ensure maximum thermal isolation from the environment. Thermal isolation enables adjusting total thermal mass and protects the detector from the heating of ROIC. The supporting arms provide a high thermal resistance path to ROIC. Therefore, the heating due to absorbed radiation is not shared with the substrate easily. The thermal design of the detector is an important issue for the design of the detector.

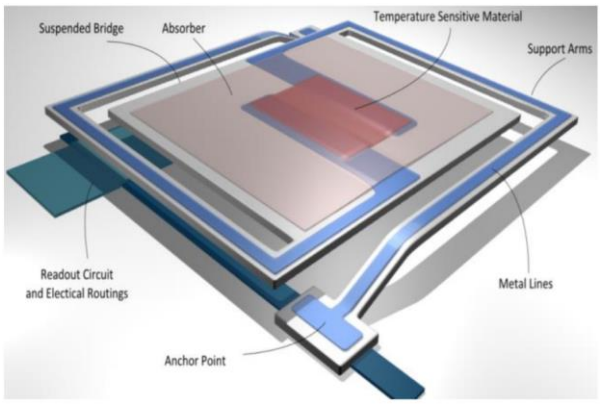

Figure 1.1: Illustration of the physical structure of the microbolometer detector.

The temperature-sensitive material is buried under the absorber layer and connected to the readout via support arms. With two port connections, the change in the electrical properties of the detector is measured. Two types of detectors are widely used depending on the design approach: resistive or diode type [6]. This thesis focuses on the resistive type microbolometer readout; hence diode type detectors are not covered.

Resistive type microbolometers employ temperature-dependent resistors, called high temperature coefficient of resistance (TCR) materials. Several high TCR materials are commonly used in detector fabrication, such as Vanadium Oxide (VOx) [7], amorphous silicon (α-Si) [8], polycrystalline silicon-germanium (poly SiGe) [4], Yttrium Barium Copper Oxide (YBaCuO) [9] and metal films [10]. Each of these materials has some advantages and disadvantages, affecting the fabrication process and detector performance. Metal film detectors are CMOS compatible since they are easy to fabricate. On the other hand, their TCR is low, which degrades detector performance. VOx has a high TCR value, but its fabrication is not CMOS compatible, so it requires a separate fabrication line. α-Si, poly SiGe is CMOS compatible but requires high-temperature annealing, which makes monolithic fabrication difficult. Moreover, VOx, α-Si, and poly SiGe have high 1/f noise due to their non-crystalline structures.

1.1.1 Operating Principles

Resistive type microbolometers sense the temperature change on the temperature-dependent resistance, as stated earlier. Since the heating on the pixel due to absorbed IR radiation is very low, the resistor must change its resistance significantly at low temperature changes. A higher performance detector needs to be fabricated with a high temperature coefficient of resistance (TCR) materials. Hence, the TCR of the selected material is one of the essential design parameters of the detector. TCR

defines the percent of change in the resistance due to temperature change, and it can be shown as:

$$\alpha = \frac{1}{R} * \frac{dR}{dT} \tag{1.1}$$

In the equation, α is the TCR of the detector material, and its unit is %/T. R and T are the resistance and temperature of the detector, respectively. Then, resistance change on the detector due to temperature change can be calculated as:

$$\Delta R = R * \alpha * \Delta T \tag{1.2}$$

As observed from Equation 1.2, the change in the resistance depends on the TCR and temperature change. High TCR materials are preferred in fabrication to obtain the best performance from the detector. On the other hand, only using high TCR material is not sufficient since the incident IR radiation to the detector is weak. The detector needs to be well isolated from the readout and ambient so that it can be heated quickly with absorbed radiation. As shown in Figure 1.1, the microbolometer detector is designed as a suspended thermal mass and connected to the readout by two support arms for thermal isolation.

The thermal structure of the microbolometer can be modeled by electrical parameters. The electrical model of the microbolometer can be observed in Figure 1.2. This model represents the power of absorbed radiation as the current source (P_{th}). The thermal isolation level of the detector is represented as thermal conductance (G_{th}). The central mass acts as a thermal capacitance, which can be represented as a thermal capacitance (C_{th}).

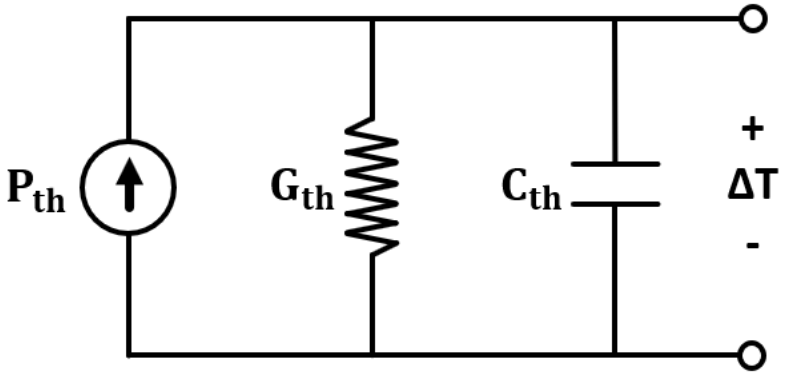

Figure 1.2: Thermally equivalent circuit of microbolometer detector.

The material must have a high TCR value for a good detector, and ΔT must be high. As observed in the thermal model, thermal conductance (Gth) and thermal capacitance (Cth) should be minimized to obtain higher temperature change from the absorbed radiation. Also, the smaller thermal capacitance helps the detector to follow rapid changes in the incident radiation. The temperature change on the detector due to thermal radiation can be calculated as:

$$\Delta T_{IR} = \frac{P_{IR}}{G_{th}} * \left(1 - e^{t_{exp}/\tau}\right) \tag{1.3}$$

where t_{exp} is the exposure time, and τ is the time constant of the detector. The time constant can be found as:

$$\tau = \frac{C_{th}}{G_{th}} \tag{1.4}$$

Typically, exposure time is much larger than the time constant; then Equation 1.3 can be simplified as:

$$\Delta T_{IR} = \frac{P_{IR\_effective}}{G_{th}} \tag{1.5}$$

In microbolometers there is a second heat source that can change detector temperature. To measure the resistance change on the detector, detector is biased with a bias current. This bias current creates a self-heating effect, which is not desired. The temperature change due to self-heating can be calculated as:

$$\Delta T_{self} = \frac{I_{bias}^2 * R(T_0)}{G_{th}} * \left(1 - e^{-t_{bias}/\tau}\right) \quad (1.6)$$

where I_{bias} is the bias current $R(T_0)$ is the resistance of the detector. Self-heating only occurred at the readout event, so that t_{bias} represents the readout time.

In microbolometer cameras, rolling shutter type readout architectures are commonly preferred, which have a short readout time for each pixel. Therefore, t_{bias} is generally much smaller than time constant τ. Then Equation 1.6 can be simplified as:

$$\Delta T_{self} = \frac{I_{bias}^2 * R(T_0)}{G_{th}} * \frac{t_{bias}}{\tau} \quad (1.7)$$

$$\Delta T_{self} = \frac{I_{bias}^2 * R(T_0) * t_{bias}}{C_{th}} \quad (1.8)$$

Then the total resistance change due to the infrared heating and self-heating can be calculated as:

$$\Delta R = R * \alpha * \left(\Delta T_{IR} + \Delta T_{self}\right) \quad (1.9)$$

When a microbolometer pixel is biased for the voltage measurement, the measured voltage difference can be calculated as:

$$\Delta V = \Delta R * I_{bias} \quad (1.10)$$

$$\Delta V = R * \alpha * \left(\Delta T_{IR} + \Delta T_{self}\right) * I_{bias} \quad (1.11)$$

The self-biasing effect is more significant than infrared heating therefore, it is challenging to directly measure temperature change caused by incident radiation [11]. There are some readout approaches to mitigate the self-heating effect, which are covered in the next section.

1.1.2 Readout Approach

The readout is an integral part of the imaging system, where resistance change in the detector is converted to a measurable output. This conversion must be performed with minimum signal loss and minimum noise contribution. The straightforward solution for this measurement is applying a constant voltage or current to the detector and measuring the current or voltage change, respectively. However, this method has some significant drawbacks. There is no way to separate the bias current and the signal so that the signal is buried inside the bias current, which requires a high dynamic range readout. Furthermore, as mentioned in the previous section, self-heating is unavoidable, and temperature change from infrared radiation is much smaller than self-heating. This architecture provides no compensation for these effects.

Half-bridge and full-bridge biasing are the widely used solutions for compensating self-heating effect and bias current. Figure 1.3 shows the half-bridge and full-bridge biasing circuits.

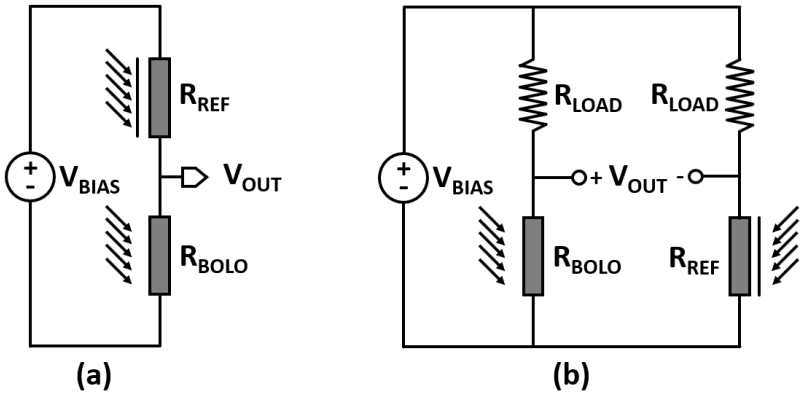

Figure 1.3: Simple schematic of (a) Half-bridge and (b) Full-bridge biasing circuit.

R_{BOLO} is the microbolometer detector, and R_{REF} is the optically blind reference detector. Reference detectors are identically fabricated with bolometer detectors; the only difference is that reference detectors are optically isolated. R_{LOAD} is load resistance, which is thermally shorted to the substrate. Therefore, load resistors are not affected by infrared heating.

In the half-bridge configuration, only the bolometer and reference resistance is implemented. Both resistors are biased with constant voltage, and the current difference is measured. Since both resistors have the same initial resistance and thermal structure, the self-heating effect occurs equally in both resistors. Hence under no illumination, the output current is equal to 0, ideally. Under infrared illumination, an optically shielded reference detector is not affected, and only the microbolometer detector is heated. Then at the output node, only infrared heating can be measured. The current can be found as:

$$I_{out} = I_{bolo} - I_{ref} \tag{1.12}$$

$$I_{out} = \frac{V_{bias}}{R_{bolo}} - \frac{V_{bias}}{R_{ref}} \tag{1.13}$$

Since at the initial conditions, R_{bolo} and R_{ref} are equal to R0:

$$I_{out} = \frac{V_{bias}}{R_0 + \Delta R_{self} + \Delta R_{IR}} - \frac{V_{bias}}{R_0 + \Delta R_{self}} \tag{1.14}$$

As observed in Equation 1.14, with the half-bridge architecture, the self-biasing effect of both resistors cancels out each out, and only infrared heating is measured.

The output current due to infrared heating is weak for direct measurement. Therefore, a low noise preamplifier needs to amplify the obtained signal. There are several types of preamplifier architectures used in the literature, such as bolometer current direct injection (BCDI) [12], Wheatstone bridge differential amplifier (WBDA) [13], capacitive transimpedance amplifier (CTIA) [3]. In this thesis, CTIA architecture is used, because of that other architectures are not covered.

CTIA architecture is commonly preferred in imaging systems [14] [11]. Figure 1.4. shows simplified schematic of CTIA and half-bridge biasing circuit. In microbolometer readout CTIA circuit is commonly used after half bridge biasing circuit.

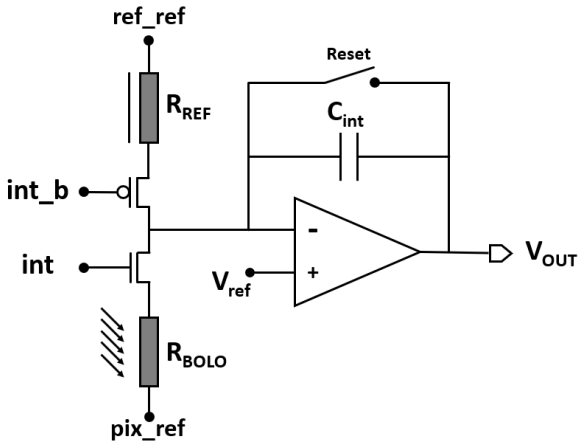

Figure 1.4: Simplified schematic of microbolometer readout with half-bridge bias and CTIA circuit.

The CTIA architecture's main aim is to integrate the current difference due to infrared heating. As the figure shows, CTIA architecture is a switch capacitor integrator circuit. CTIA circuit has two operation phases, reset and integration. The reset switch is closed at the reset phase, and the integration capacitance (C_{int}) is reset. During the integration phase, the reset switch opens, and the integration event begins. The integration phase takes place for a fixed period called integration time (t_{int}). During the integration, the negative feedback holds the input node at fixed voltage V_{ref}. which provides stability for the detector biasing. The main advantage of the CTIA architecture is that it suppresses parasitic capacitances at the input node, which is crucial for large format imaging arrays and enables the use of much smaller integration capacitances.

The output voltage change of the CTIA circuit due to detector current can be calculated as:

$$\Delta V_{out} = \frac{I_{det} * t_{int}}{C_{int}} \tag{1.15}$$

As observed from Equation 1.15, the voltage difference depends on three parameters, current difference between reference detector and bolometer (I_{det}), integration time (t_{int}), and integration capacitance (C_{int}). Since minimum detectible voltage is an important challenge for ADC design, large ΔV is preferred. Integration time is limited by array size and frame rate. Therefore, a smaller integration capacitance is needed to have a large ΔV. Since parasitic capacitances are suppressed in CTIA architecture, smaller integration capacitances are possible.

1.1.3 Non-Uniformity Correction (NUC)

Like the other MEMS fabrication processes, it is impossible to have an exact resistance value for the microbolometer pixels. The microbolometer resistances have a mismatch spread around the mean resistance value. Moreover, the process mismatch affects the resistance of the detector pixel and the thermal parameters of the detector pixel.

As mentioned in the previous chapter, the microbolometer readout measures the difference in the resistance by measuring thermal heating. To eliminate the self-heating effect optically shielded reference detector is used together with a pixel detector. However, the fabrication mismatch on the resistances makes this total cancelation impossible and introduces a high static error current. This current disrupt readout operation since the mismatch current is much higher than the pixel data. Therefore, it is necessary to implement a method to suppress this mismatch effect.

There are several techniques and architectures used for suppressing the mismatch effect. One solution is making the bias circuit of each detector digitally controllable. This method adjusts bias voltage for each pixel readout to match their current to their reference pixel [15]. This method provides good results but needs extensive foreground calibration steps. Also, the calibration data depends on the ROIC temperature, so different temperature regions require different calibration data.

Despite promising results from the digital correction, the need for hefty calibration work is not desired. The second solution uses a high dynamic range and low noise analog circuit for pixel readout. The static current is measured with pixel data and digitalized with high precision ADC. Then the static error is processed and eliminated with digital filters and software. This method eliminates the complex calibration step by introducing complex analog circuitry. The design of the high-precision ADC is discussed in the following chapters.

1.2 Analog to Digital Converter

Analog to digital converters (ADC) converts a continuous-time and continuous-amplitude analog signal to the digital domain. Most display units work with digital data, and image processing is performed in the digital domain; hence digital output imaging systems are preferred. In high-precision imaging applications, the performance of the ADC has an important impact on the imaging system's performance. Hence, understanding the specifications of the data converters is essential for obtaining the required performance.

1.2.1 Performance Parameters

It is vital to have a unanimous definition for performance parameters to obtain insight into the performance of the ADCs. There is a large set of parameters to define the performance of ADCs. These parameters are divided into three groups, general features, static parameters, and dynamic parameters [16].

1.2.1.1 General Features

General features define the basic parameters of the ADCs.

Resolution: The number of bits an ADC uses to digitalize its analog input. Higher resolution ADCs define the analog data with more precise steps.

Quantization step: Defines the minimum detectible voltage. It is obtained by dividing the input voltage range by ADC resolution.

Dynamic Range: Defines the ratio between the noise floor and maximum detectible signal. Expressed in dB.

1.2.1.2 Static Parameters

Static parameters of an ADC define the input-output characteristics. In the ideal case, the input-output characteristic of ADC is a staircase with uniform steps, and the step size is defined as the quantization step. The static characteristic of an ideal ADC can be observed in Figure 1.5.

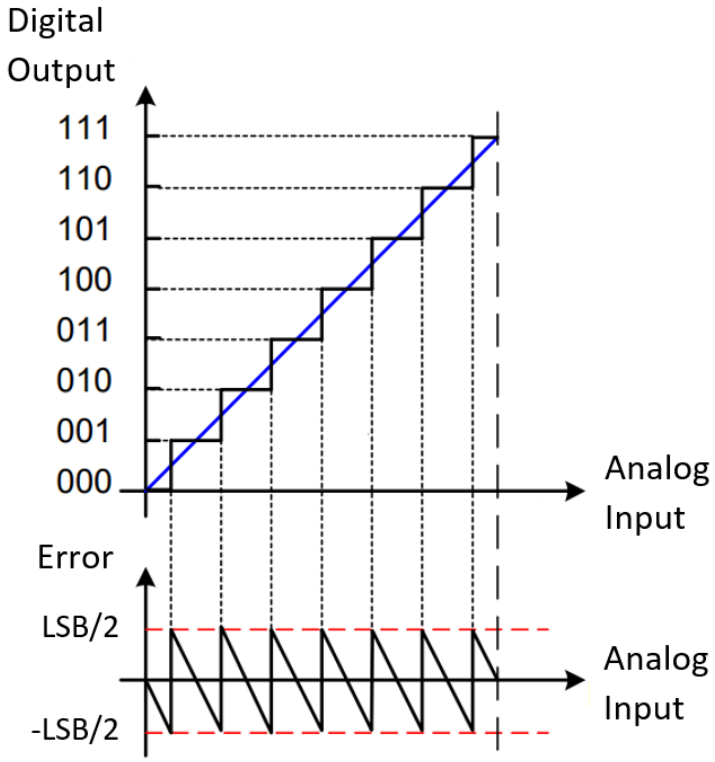

Figure 1.5: Ideal input-output characterization(top) and quantization error(bottom) of 3-bit ADC. [17]

The figure shows that the input voltage range is divided into uniform steps. On the other hand, this is not applicable in real life. Static parameters define these deviations from the ideal input-output characteristics.

Analog Resolution: Defines the analog voltage change corresponding to the 1-bit change on the digital code (1 LSB).

Offset: Defines the output shift in the zero input. Offset affects all the digital codes, hence all quantization steps are equally shifted.

Gain Error: Defines the deviation between the slopes of the ideal ADC transfer function and the actual output transfer function

Differential Non-linearity (DNL): Defines the deviation on the quantization steps. In ideal ADCs, quantization steps are uniform. However, real ADC's quantization steps deviate due to component mismatches and non-idealities. The amount of the deviation from the ideal quantization step is denoted as DNL. Often the maximum DNL is referred as the DNL of the ADC and is generally measured in LSB.

Integral Non-linearity (INL): Defines the deviation of the output from the ideal transfer line. As stated in the DNL, the quantization steps of ADCs deviate from the ideal. The cumulative deviation is expressed INL. There are two methods to measure INL, the best straight-line method and the end-point method [18]. The best straight-line method compares the output of the ADC with a straight line, which is the closest approximation to the ideal ADC transfer line. This method includes offset error and gain error into the INL. The end-point method draws a straight line between the end points of the ADCs transfer function and measures deviation from this line. This approach corrects the gain error and offset error [16]. Often the maximum INL is referred as the INL of the ADC and is generally measured in LSB.

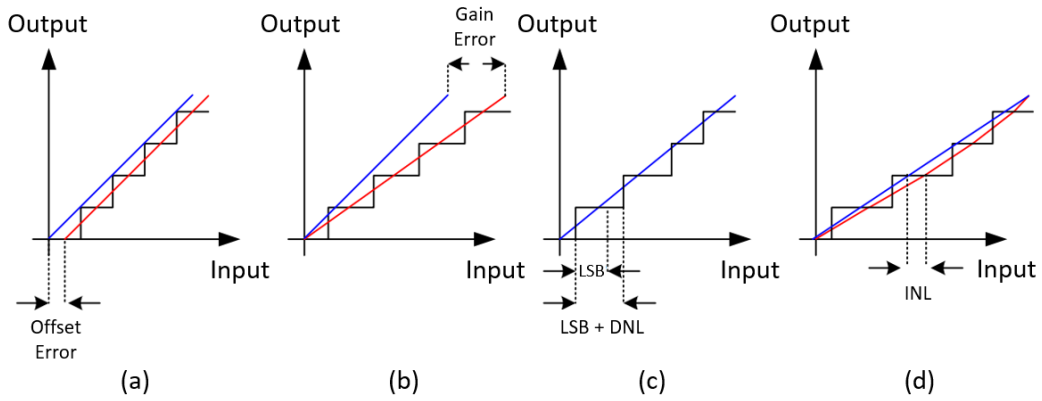

Figure 1.6: The demonstration of the static error sources, offset error (a), gain error (b), DNL (c), and INL (d). [17]

1.2.1.3 Dynamic Parameters

The dynamic performance of an ADC is determined by its frequency response and the speed of the analog components. In high-frequency applications, these dynamic parameters become important. Therefore, these parameters are defined for a defined dynamic condition or as a function of frequency [16].

Signal to Noise Ratio (SNR): Defines the ratio between the power of the signal and the total noise power in the Nyquist interval.

Signal to Noise and Distortion Ration (SNDR): Defines the ratio between the power of the input sinusoid wave and the power of the in-band noise (IBN), accounting for harmonics in the pass band.

Spurious Free Dynamic Range (SFDR): Defines the ratio between the power of input signal and power of the most significant in-band spurious spectral component.

Effective Number of Bits (ENOB): Defines the bitwise performance of an ideal Nyquist rate ADC to perform the same level of SNDR. It can be calculated as

$$ENOB = \frac{SNDR_{dB} - 1.76dB}{6.02dB} \tag{1.16}$$

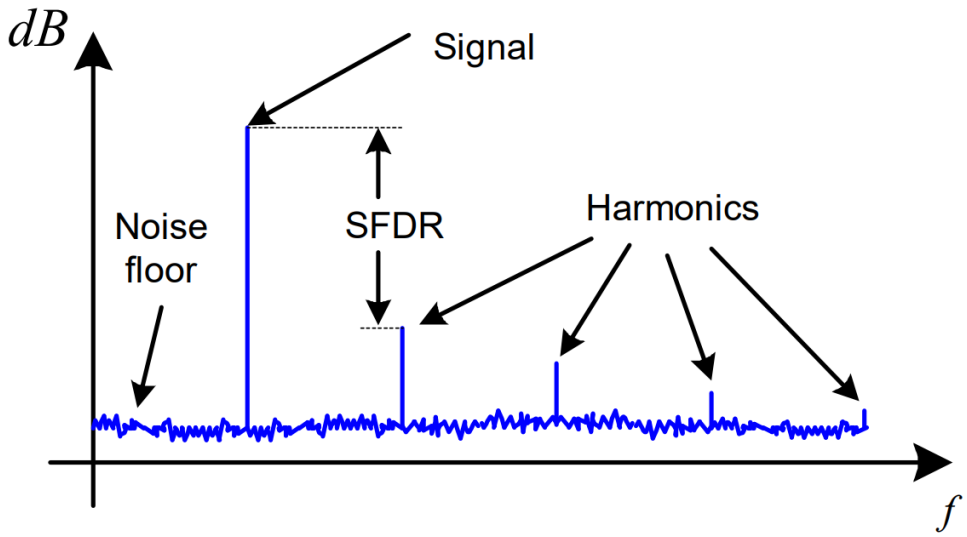

Figure 1.7: The demonstration of dynamic performance parameters. [17]

1.2.2 Figure of Merits

The performance parameters provide invaluable insight into the operation of the ADCs. On the other hand, different ADCs are optimized for different operations and their necessary needs. These design choices make designers have a trade-off between different parameters, thus making a comparison between ADCs challenging. A figure of merit (FoM) should be defined to make a comparison between various ADCs possible. In literature, two FoM definitions are widely accepted: Walden FoM [19] and Schreier FoM [20].

Walden FoM: Main aim is to reflect the power efficiency of the ADC. The FoM gives the power consumed for a single conversion step [19]. Walden FoM calculated as:

$$FoM_W = \frac{Power}{f_{sample} * 2^{ENOB}} \ [J/conv] \tag{1.17}$$

As observed from equation 1.17, it is assumed that doubling the resolution consumes an equal amount of power as doubling the bandwidth. Because of that, Walden FoM is widely used for comparing Nyquist ADCs.

Schreier FoM: Walden FoM is widely used for Nyquist ADCs but is not suitable for oversampling ADCs. In oversampling, ADCs power needs to be quadrupled in order to double bandwidth. Thus, Schreier FoM is more suitable for oversampling ADCs. Schreier FoM calculated as:

$$FoM_S = Dynamic\ Range + 10 * log_{10}\left(\frac{Band\ Width}{Power}\right) \ [dB] \tag{1.18}$$

1.2.3 ADC Architectures

There is a vast area of use for the ADCs. Each application has unique needs; therefore, several ADC architectures have been developed for the needs of respected applications. Each of these architectures has different advantages and drawbacks. According to their working principle, ADC architectures can be divided into Nyquist-Rate ADCs and Oversampling ADCs [16].

As stated in the Nyquist theorem maximum frequency of the input signal must be lower than half of the sampling frequency in order to prevent aliasing. Therefore, the maximum measurable frequency is half of the sampling frequency for Nyquist-Rate ADCs. Flash ADC, SAR ADC, and Pipeline ADC are widely used Nyquist rate ADCs.

Oversampling ADCs have a sampling frequency much higher than the maximum measurable input signal. Hence, Oversampling ADCs have higher resolution in exchange for lower bandwidth. Delta-Sigma ADC and Zoom ADC are widely used oversampling ADCs.

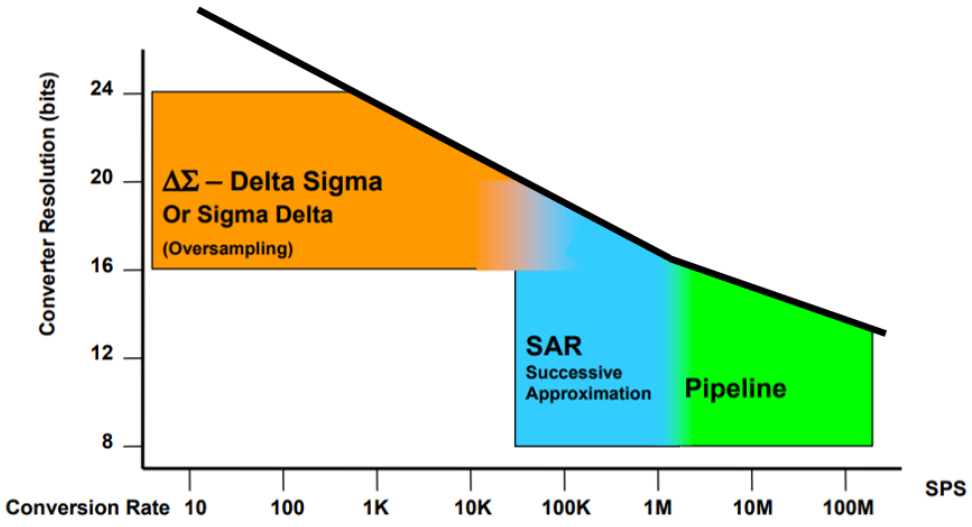

Figure 1.8: Application areas of ADC architectures. [21]

1.2.3.1 Flash ADC

Flash ADCs are the fastest and conceptually the most straightforward ADC architecture [22]. As shown in Figure 1.9. m bit flash ADC consists of 2^m-1 comparators and equally segmented voltage levels. The input data is compared with all the voltage levels simultaneously, and a decoder converts the output code to the binary code. Since the whole operation happens simultaneously, Flash ADCs are extremely fast. However, Flash ADC's resolution is limited since adding an extra bit doubles the number of comparators and the layout area. As a result, flash ADCs mainly employed for high-speed low-resolution applications.

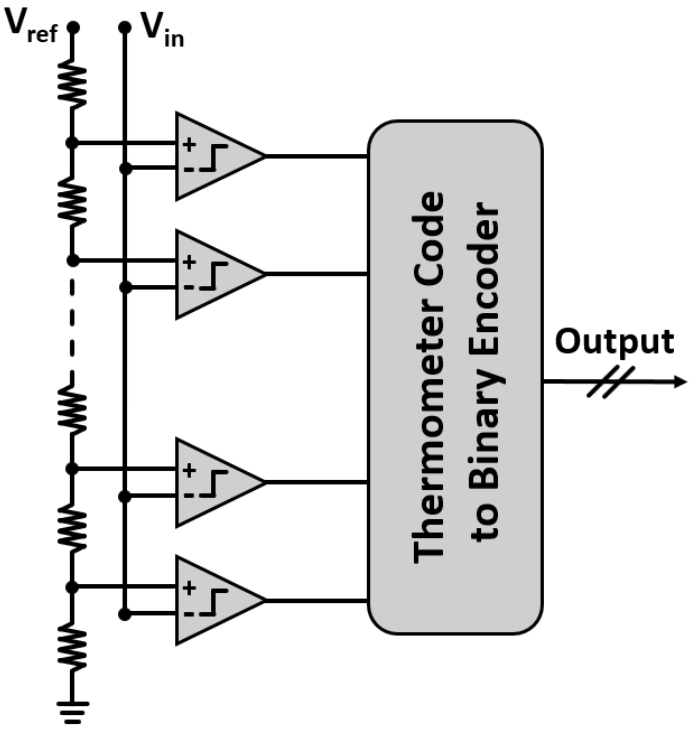

Figure 1.9: Block diagram of m bit Flash ADC.

1.2.3.2 Successive Approximation Register (SAR) ADC

SAR ADC is a widely used architecture due to its good power efficiency. As shown in Figure 1.10. m bit SAR ADC consists of sample and hold, m bit DAC, single comparator, and SAR logic.

The ADC operation occurs on multiple clock cycles. Generally, the binary search algorithm is implemented for the best power efficiency. The operation starts with the sampling of the input signal. Initially, the DAC voltage is set to the middle of the full range voltage. In each cycle, the input signal is compared with DAC voltage, and respect to the output of the comparison voltage difference between the held signal is halved. These conversions are repeated until the least significant bit (LSB) is defined. This conversion takes m clock cycles for m bit SAR ADC.

SAR ADCs have excellent power efficiency since most of the unnecessary comparisons of flash ADC are not performed. Its basic structure, low power consumption, and medium resolution make it a widely preferred architecture.

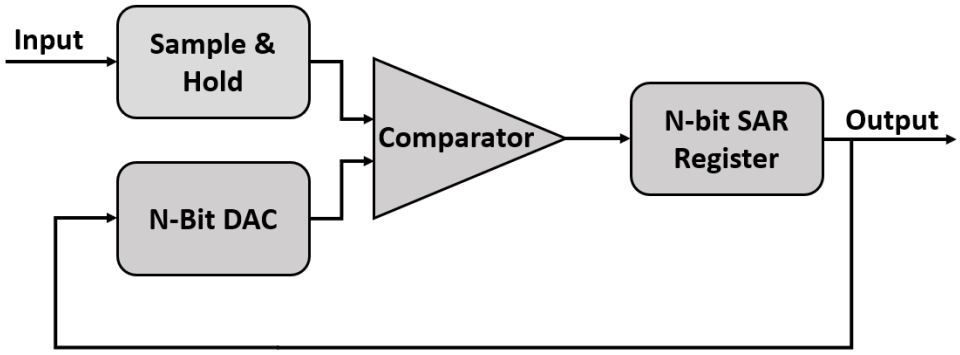

Figure 1.10: Block Diagram of SAR ADC.

1.2.3.3 Pipeline ADC

Pipeline ADC is a widely used architecture due to its high sampling rate and high resolution. As shown in Figure 1.11. Pipeline ADC consists of multiple stages. Each stage has its sample and hold circuit, ADC, DAC, and comparator. The main aim of the pipeline ADC is to operate all stages simultaneously and achieve high sampling frequency.

The operation starts with sampling the input signal in the first stage. Input signal digitalized by the local ADC and DAC generates residue voltage respect to the ADC out. The residue voltage is subtracted from the input signal, and the residue voltage is multiplied by the resolution of the local ADC. This operation is repeated at each pipeline stage. After the next stage samples the data, the first pipeline block samples new data. Therefore, different samples are processed concurrently. As a result, the output rate depends only on the speed of one stage.

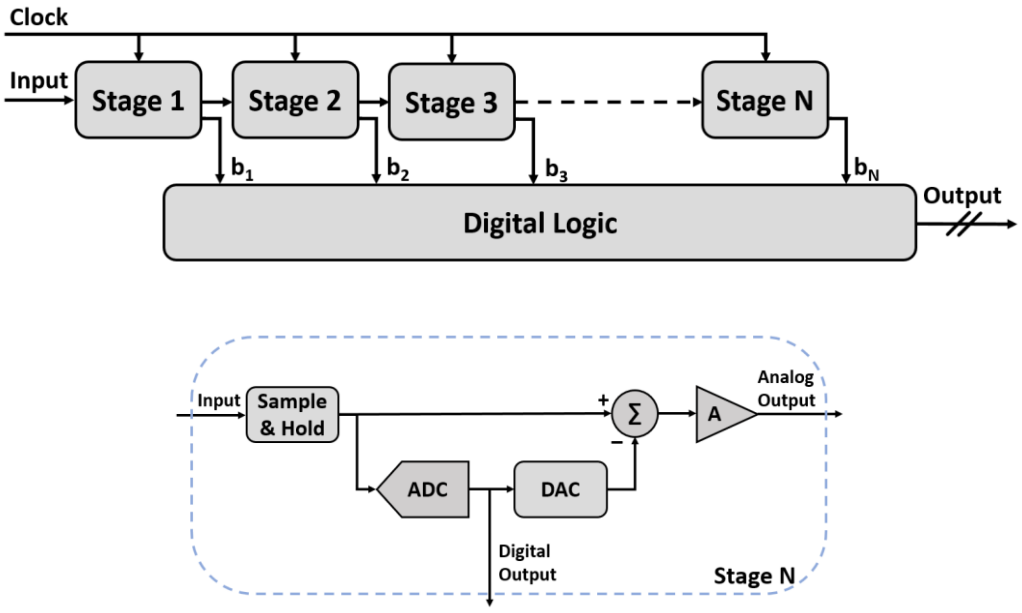

Figure 1.11: Block Diagram of Pipeline ADC (top) and unit stage (bottom).

1.2.3.4 Delta-Sigma ADC

Delta-Sigma ADCs have become widely used in analog to digital converter architecture and found new application areas with current developments. Figure 1.12. shows the block diagram of Delta-Sigma ADC. Compared to Nyquist ADCs, Delta-Sigma ADC cover the widest conversion region between the bandwidth and resolution [23]. In addition to this versatility, robustness, and easy implementation of the Delta-Sigma architecture make more projects adopt this architecture instead of conventional architectures.

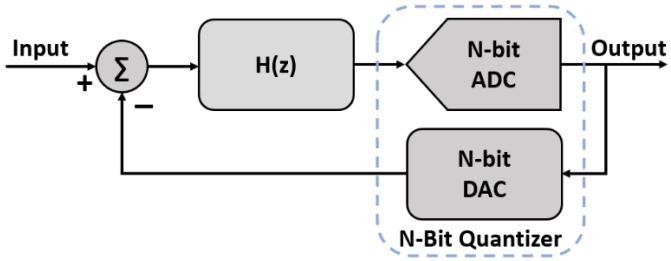

Figure 1.12: Block diagram of Delta-Sigma ADC.

Different from Nyquist rate ADCs, Delta-Sigma ADC sample the input signal at a higher rate than Nyquist rate. This operation is called oversampling. These samples are quantized by a low-resolution quantizer which introduces a large quantization error. A feedback loop filters the oversampled data with a large quantization error, shaping the quantization error. In the shaping, most of the power is pushed to the higher frequencies, where digital filters will remove it. The aggressiveness of this noise shaping depends on the order of the feedback loop and oversampling ratio (OSR). With better noise shaping, very high precision digitalization is possible. Therefore, Delta-Sigma ADC can achieve very high resolution in exchange for speed. This trade-off is crucial for oversampling ADCs since other architectures need complex and high-precision analog circuits for high-resolution analog to digital conversion [23].

1.2.3.5 Zoom ADC

Delta-Sigma ADC provides high linearity and high-resolution output compared to Nyquist rate ADCs. However, the power efficiency of Delta-Sigma ADC is much lower [24]. Zoom ADC is a hybrid architecture proposed for improving energy efficiency [25]. Figure 1.13. shows the block diagram of Zoom ADC. Utilizing the advantages of Nyquist rate and oversampling ADCs, Zoom ADC can achieve high dynamic range, high accuracy, and high resolution with low energy consumption.

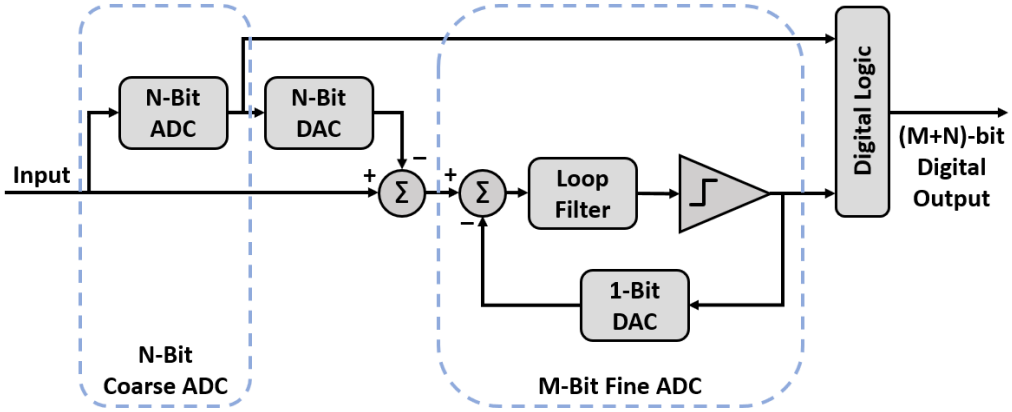

Figure 1.13: Block diagram of Zoom ADC.

As observed in Figure 1.13. Zoom ADC is a hybrid of one coarse ADC and one fine ADC. The main aim of coarse ADC is determining the most significant bits with minimum power consumption, where Nyquist rate ADCs are very efficient. The output of the coarse ADC is subtracted from the input voltage, and fine ADC processes the residue voltage. Fine ADC determines the least significant bits by processing residue voltage. Since high precision is necessary for this operation, Delta-Sigma ADC is used for fine conversion. The output of the two ADC is then combined by digital logic.

1.3 Motivation of Thesis

In the last decades, microbolometer cameras have increased their market share due to their low cost and decent thermal performance. There is a tremendous effort to improve the microbolometer cameras' performance and decrease system costs. Therefore, the main aim of this thesis is to design and implement an on-chip analog-to-digital converter (ADC) for microbolometer cameras. The on-chip design reduces system costs by removing external PCB for ADC. The designed ADC must provide high precision conversion, adjustable sampling frequency, high dynamic range, low power consumption, and high linearity.

With the technological advancements, the performance of microbolometer cameras drastically increased. Development of low time-constant microbolometer detectors, and high frame-per-second (FPS) cameras (200 FPS [26]), which do not suffer motion blur, can be developed. The designed ADC should perform for different frame rates and sampling frequencies.

As stated in earlier chapters, microbolometer detector fabrication has a high mismatch between detectors. Conventional architectures need a non-uniformity-correction circuit and algorithm to solve mismatch issues. This thesis uses very high dynamic range ADC instead of complex foreground calibration steps. With this improvement, the complex testing and calibration cycle would be obsolete.

Considering the given requirements and aiming for improved performance, “Column Parallel Incremental Zoom ADC” is the most suitable architecture for this study.

1.4 Thesis Organization

This thesis's main objective is to develop an on-chip ADC which provides high precision conversion, adjustable sampling frequency, high dynamic range, low power consumption, and high linearity. The objectives for the design of the ADC are listed as follows:

1. System level analysis and development of the Zoom ADC. The signal domain operation of the Zoom ADC is critical, and the system must be analyzed as a whole.

2. The design and implementation of the Zoom ADC. The designed ADC should provide high precision data output with minimum power and area consumption.

3. The test strategy must be defined for the characterization of the ADC. The required hardware should be designed, considering the noise and linearity requirement of the ADC.

The organization of the thesis can be explained as follows:

In section 2, the general overview of the system is given. The top-level requirements are defined for ADC design. The oversampling concept is explained in detail, and the noise shaping basics are covered. The Delta-Sigma Modulator architecture is introduced with a top-level approach. The requirement for digital filters is stated, and the filter architectures are shown. Finally, the Zoom ADC concept is introduced with the background provided in the previous chapters.

In chapter 3, the system-level design details are provided. The loop equation of the Delta-Sigma Modulator is investigated, and the design parameters for the modulator are defined. The mismatch correction strategies for the Zoom ADC are discussed, and DEM architecture is chosen. The digital filter architecture is defined, and the cascaded architecture is presented. The novel improvements on the filters are explained in detail.

In chapter 4, the implementation of the Zoom ADC is presented step-by-step. The design of the main blocks and subblocks are briefly stated, and their performance is verified with simulation results. The top-level design is shown, and the ADC's performance simulations are presented.

In chapter 5, the testing strategy for the Zoom ADC is planned. The measurement setup is stated, and test software is shown.

In chapter 6, the thesis work is concluded. Future improvement plans to improve system performance are shared.

CHAPTER 2

SYSTEM OVERVIEW

An on-chip ADC's design starts from the readout circuit's design. The ROIC directly determines the specifications and limitations, therefore careful investigation of the readout system is crucial. After the system requirements are determined, the ADC requirement can be defined.

2.1 Top Level Architecture

The designed ADC is implemented on MT3825BA ROIC of Mikro-Tasarım A.Ş. [27]. MT3825BA is an analog output microbolometer readout circuit with a 384x288 pixel array and 25µm pixel pitch and designed with 0.18µm CMOS technology. The block diagram of the readout chain of MT3825BA can be observed in Figure 2.1. The simplified floor plan of the MT3825BA can be observed in Figure 2.2. The ROIC reads microbolometer pixels by rolling shutter mode, with top and bottom column readouts with double pixel width. The ROIC is designed with system-on-chip architecture, so all auxiliary blocks such as bias generator, digital timing generator, and output stage are applied on-chip.

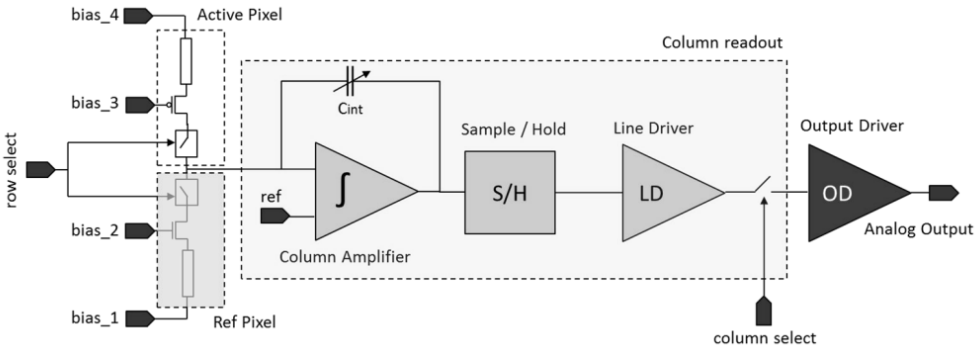

Figure 2.1: Block diagram of the readout chain of MT3825BA ROIC. [27]

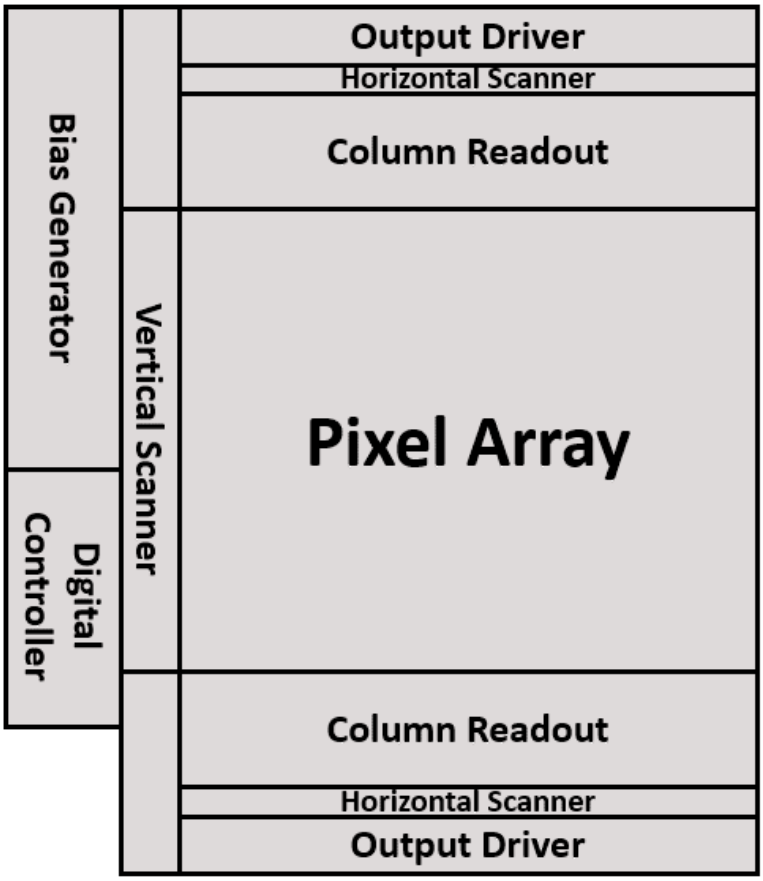

Figure 2.2: Simplified floor plan of MT3825BA ROIC.

In the last decade, the demand for faster thermal sensors is increased. With the advancement in MEMS fabrication technologies, it is possible to fabricate low time-constant microbolometer detectors. Low time-constant detectors can detect fast-moving objects without any motion blur effect. Therefore, higher frame-per-second imaging can be archivable [26]. As the design of MT3825BA is revised for digitalization, also readout architecture and timing scheme are revised for high FPS imaging. Following the new advancements in the industry, the developed camera can reach high frame rate imaging up to 200 FPS.

2.1.1 Design Specifications for ADC

The designed column ADC will follow the initial readout configuration and technology of the target ROIC. Figure 2.3. shows the block diagram of the digital readout circuit. The ADC is directly placed after the column readout circuit at the same top and bottom column readout configuration. So that width per column is 50µm for the ADC. The ADC's timing generator and bias generator circuits are integrated with the current architectures for simple control over the ROIC. The floor plan of the digital ROIC is shown in Figure 2.4.

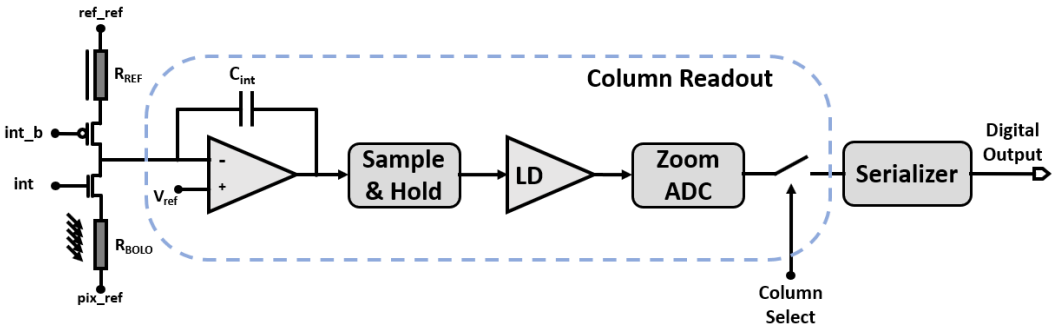

Figure 2.3: Block diagram of the readout chain of proposed digital readout.

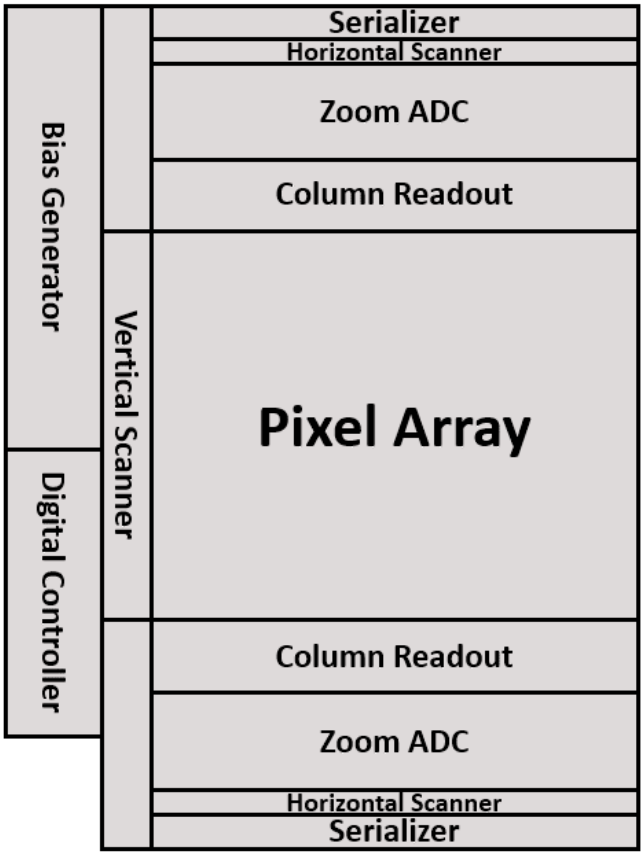

Figure 2.4: Simplified floor plan of proposed digital output ROIC.

With the design revision of the target ROIC, high frame rate thermal imaging modes are added. Four operation modes are developed, high-resolution mode, standard mode, fast mode, and ultrafast mode. High resolution mode provides maximum precision and operates at 20 FPS. Standard mode performs general 30 FPS operation. Fast mode provides 50 FPS imaging while maintaining high-precision operation. Ultrafast mode provides 200 FPS imaging with decent precision. Therefore, the designed ADC must also be designed for this imaging modes. These modes have different precision and power specifications, so ADC modes are carefully designed for the needs of these operations. The list of design requirements for imaging modes can be observed in Table 2.1.

Table 2.1: Design requirements for ADC.

Technology	180nm CMOS			
Column Pitch	50 µm			
Array Size	384 x 288			
Supply Voltage	3.3 V & 1.8 V			
Conversion Range	3.04 V - 0.16 V			
Modes	High Precision	Standard	Fast	Ultrafast
Frame Rate	20 FPS	30 FPS	50 FPS	200 FPS
Line Time	170 µsec	115 µsec	65 µsec	16.5 µsec
Sampling Rate	5.9 kS/sec	8.6 kS/sec	15.4 kS/sec	60 kS/sec
Power	<400µW	<550µW	<800µW	<1200µW
ENOB	>20-bit	>19-bit	>18-bit	>16-bit

2.2 Oversampling ADC

In the first chapter, different ADC architectures are described, and their strengths are pointed out. As the design specifications for the ADC stated, column-parallel incremental Zoom ADC architecture is a good fit for the intended design. To better grasp the Zoom ADC, the general theory and implementation details of oversampling ADCs are investigated in detail.

2.2.1 Oversampling

In the sampling process, the continuous time signal input signal is transformed into a discrete-time signal. According to the Nyquist theorem, the sampling frequency (fs) must be twice the input signal's maximum frequency to prevent aliasing, thus limiting the maximum bandwidth of the input signal. ADCs with sampling frequency is at the minimum rate input frequency allowed, called Nyquist-rate ADCs. If the sampling rate of an ADC is much higher than the Nyquist rate, it is called oversampling ADC. The amount of oversampling is expressed as the oversampling ratio (OSR) and expressed as:

$$OSR = \frac{f_s}{2 * f_{bw}}$$

Generally, most ADCs employ an antialiasing filter to prevent out-of-band noises and aliasing. In Nyquist-rate ADCs, the input bandwidth coincides with fs/2, and high-order antialiasing filters (AAF) are required to prevent aliasing. On the contrary, in oversampling ADCs, the replicas of the input signal are much farther away in the signal spectrum, and the antialiasing filter's specifications are relaxed [23]. The input signal spectrum and antialiasing filter for Nyquist rate ADCs and Oversampling ADCs are illustrated in Figure 2.5.

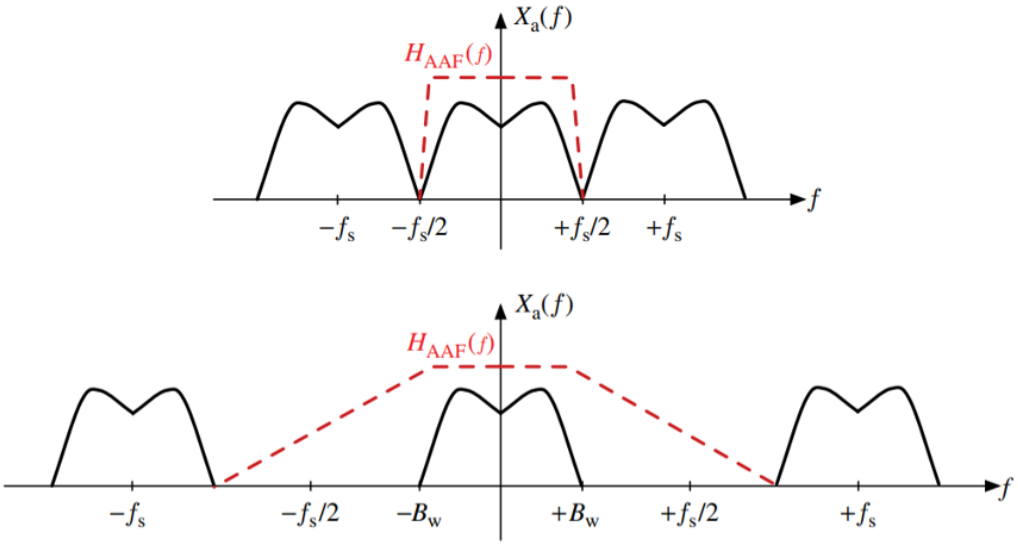

Figure 2.5: Input signal spectrum of (top) Nyquist-rate ADCs and (bottom) Oversampling ADCs. [23]

One of the main performance limitations of an ADC is quantization noise. While performing analog to digital conversion, the error occurred due to digitalization steps called quantization error. The quantization error can be expressed as a random process with a uniform probability distribution between [$-f_s/2$, $+f_s/2$]. Therefore, quantization noise can be expressed as white noise in this interval [20]. According to the additive white noise approximation of the quantization error, the power of the quantization error does not change with the sampling frequency [23]. The quantization noise sampled in the pass band is called in-band noise power (IBN). In oversampling ADCs, only a fraction of the quantization noise is in the signal band, so the effect of quantization noise can be decreased with a higher oversampling ratio (OSR). The quantization noise of Nyquist-rate ADCs and oversampling ADCs illustrated in Figure 2.6.

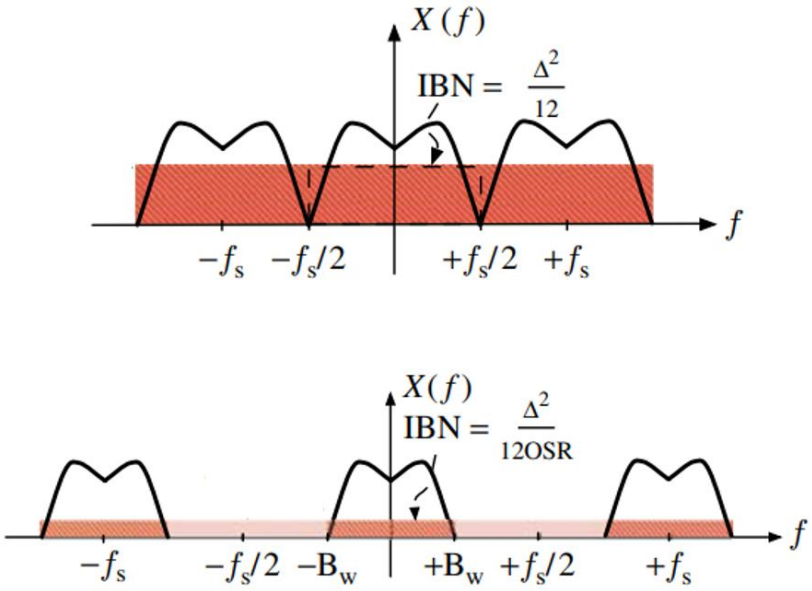

Figure 2.6: Quantization noise of (top) Nyquist-rate ADCs and (bottom) Oversampling ADCs. [23]

Dynamic range (DR) is the ratio between the output power at the input frequency and the in-band noise (IBN) power. For an ideal ADC, the dynamic range can be calculated as:

$$DR(dB) = 10\log_{10}(\frac{P_{out,max}}{IBN})$$

For an N-bit quantizer, the dynamic range of an ideal oversampling ADC is approximated as

$$DR(dB) = 6.02N + 1.76 + 10log_{10}(OSR)$$

For a Nyquist-Rate, ADC OSR equals 1, and each additional bit in the quantizer increases the dynamic range by 6 dB. In oversampling ADCs, quadrupling the OSR has a similar dynamic range increase with an extra bit in the quantizer.

2.2.2 Noise Shaping

In oversampling ADCs' dynamic range can be increased by increasing the oversampling ratio. On the other hand, high precision conversion requires a high dynamic range, and increasing oversampling above a certain point is impractical. To increase the accuracy, without increasing OSR, a loop filter shapes the white quantization noise, and most of its power is pushed outside the signal band. Then the out of the band noise is eliminated by filtering. The input signal spectrum and shaped quantization noise of oversampling ADC are illustrated in Figure 2.7.

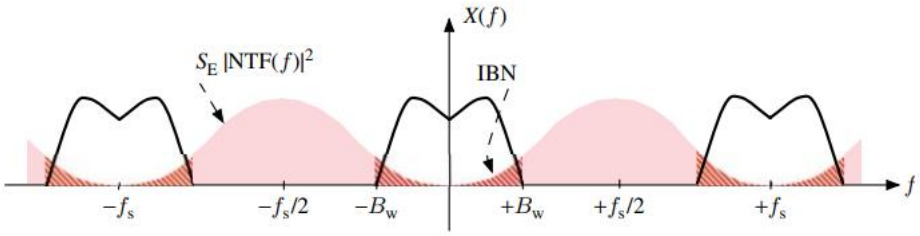

Figure 2.7: The input signal spectrum and quantization noise of oversampled ADC. [23]

The noise shaping decreases in-band noise power and drastically increases the performance of the oversampling ADCs. The order of the loop filter determines the aggressiveness of the noise shaping. As shown in the Figure 2.8. higher order loop filters provide more aggressive noise shaping and decrease the power of in-band noise.

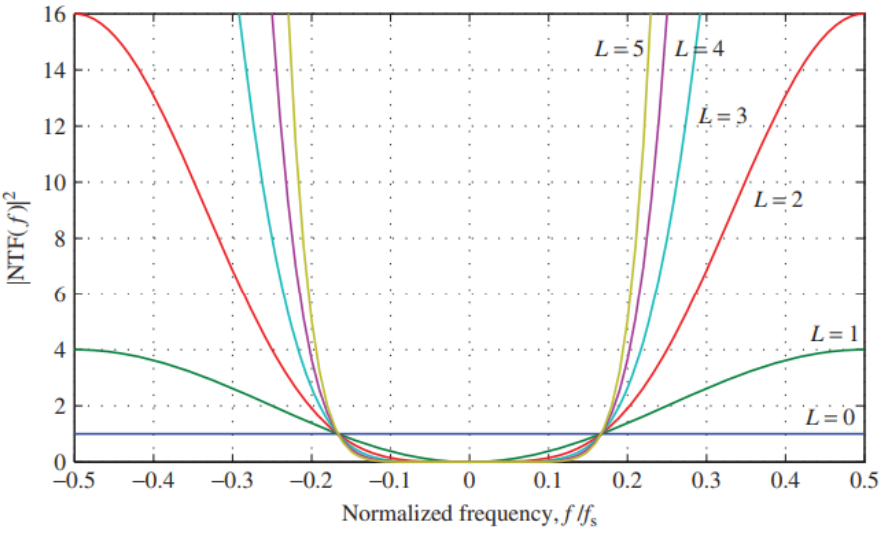

Figure 2.8: Illustration of noise shaping respect to the loop filter order (L). [23]

The dynamic range of an ideal oversampling ADC with N-bit quantization and L^{th} order loop filter can be obtained as:

$$DR(dB) = 6.02N + 1.76 + 10log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1) * 10log_{10}(OSR)$$

2.2.3 Delta-Sigma Modulation

Delta-Sigma modulators are widely preferred oversampling architectures due to their effective noise shaping characteristics. Delta-Sigma modulators employ a closed-loop negative feedback path to achieve control over the quantization error. The block diagram of a simple Delta-Sigma Modulator architecture is shared in Figure 2.8. It consists of a loop filter H(z), 1-bit ADC, and 1-bit DAC. The negative feedback configuration creates two different transfer functions called: signal transfer function (STF) and noise transfer function (NTF).

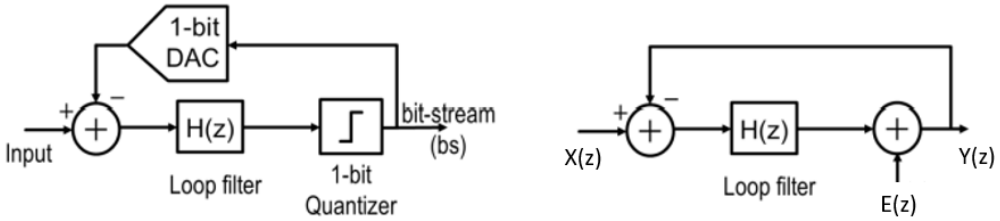

Figure 2.9: Block diagram (left) and linear model (right) of a simple Delta-Sigma ADC. [28]

In the linear model, quantization error can be expressed as E(z). Then the output of the loop filter Y(z) can be expressed as:

$$Y(z) = STF(z) * X(z) + NTF(z) * E(z)$$

The NTF and STF of a Delta-Sigma Modulator can be calculated as:

$$STF(z) = \frac{H(z)}{1 + H(z)}$$

$$NTF(z) = \frac{1}{1 + H(z)}$$

If H(z) has a low pass characteristic with unity DC gain Equation 2.6. and 2.7. can be approximated as:

$$STF(z) = 1$$

$$NTF(z) = \frac{1}{H(z)}$$

It can be observed that using loop filter H(z) with a low-pass characteristic, unity STF can be obtained, and NTF has a high pass characteristic which pushes noise out

of the signal bandwidth. In first-order Delta-Sigma modulators, a discrete integrator is used for loop filter, where:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Then equation 2.5. can be written as:

$$Y(z) = z^{-1} * X(z) + (1 - z^{-1}) * E(z)$$

As observed from Equation 2.11, the signal is transferred with unity power and delay. A high-pass function shapes the quantization noise. To improve performance, a higher order loop filter can be used, which brings more aggressive noise shaping with sharper high-pass NTF. Also, the resolution of the quantizer can be increased, which decreases the power of quantization noise E(z).

2.2.4 Digital Filters

The digital filter holds a crucial role in clearing out-of-band noise. The Delta-Sigma Modulator shapes and pushes the noise to high frequencies. Digital filters are employed at this level to filter out-of-band noises and provide parallel data [29]. In digital filters, decimation eliminates redundant data, and the low-pass filter clears out-of-band noise. At the end of digital filtering, the output frequency is generally at the Nyquist rate of the data.

In most of the designs, decimation filters are preferred [20]. Decimation filters can perform digital filtering and sample frequency dropping at the same time. One of the widely used architectures is Cascaded Integrator Comb (CIC) filters [30]. Figure 2.10 shows a second-order CIC filter with decimation ratio D. Comb filters are multiplier-free filters with low memory requirements. CIC filter is the

combination of cascaded integrator blocks followed by decimator and cascaded differentiator blocks. The number of cascades gives the filter order (L), where higher orders improve the low pass filtering characteristic of filter and filter gain.

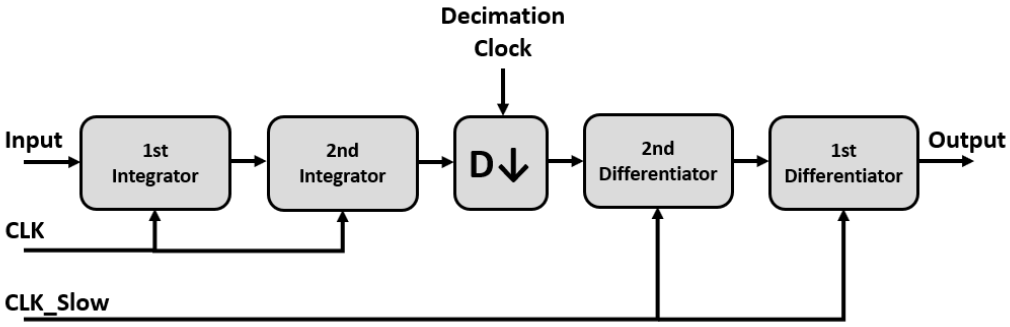

Figure 2.10: Block diagram of second order CIC filter with decimation ratio D.

The filter gain gives the bitwise width of the output and can be calculated as:

$$Filter\ Gain\ (bit) = \ (log_2(D))^L$$

The decimation filter is an efficient low pass filter, but the filter's performance is not sufficient for high precision applications. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters are used to improve filter performance. IIR filters are highly efficient and have a sharp stopband compared to FIR filters. On the other hand, IIR filters suffer from stability issues and are hard to implement on-chip. Since this work requires a filter to be implemented on the chip, IIR filters are not covered. The block diagram of the FIR filter can be observed in Figure 2.11. FIR filters consist of multiple delay and add blocks called taps, where the last N data is added with a certain weight. By adjusting the number of taps and coefficients, filter characteristics, pass and stopband frequencies, and sharpness of filter can be adjusted.

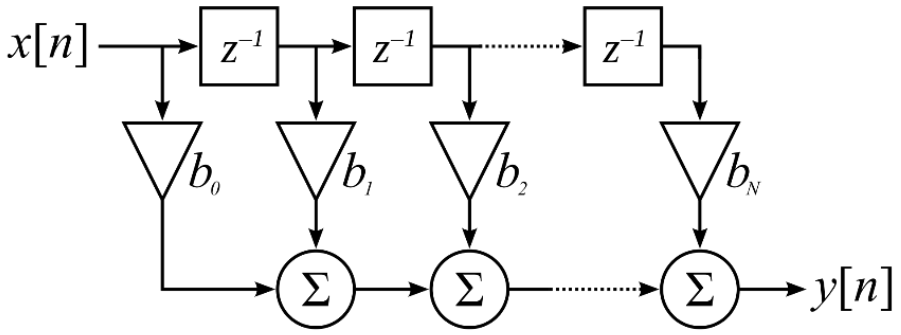

Figure 2.11: Block diagram of N-tap FIR filter. [31]

2.3 Zoom ADC

2.3.1 System Overview

So far, the basics of Delta-Sigma ADCs and their advantages are discussed. For high-precision applications, Delta-Sigma ADCs are the most preferred solutions. On the other hand, compared to Nyquist-Rate ADCs, Delta-Sigma ADCs are less power efficient, making them less desirable. To improve the power efficiency of Delta-Sigma ADC, Zoom ADC architecture is proposed [32].

Zoom ADC is a hybrid oversampling ADC that combines the advantages of SAR ADC and Delta-Sigma ADC. The power efficiency of SAR ADC is employed to decrease the power consumption of Delta-Sigma ADC [33]. The block diagram of Zoom ADC can be observed in Figure 2.12.

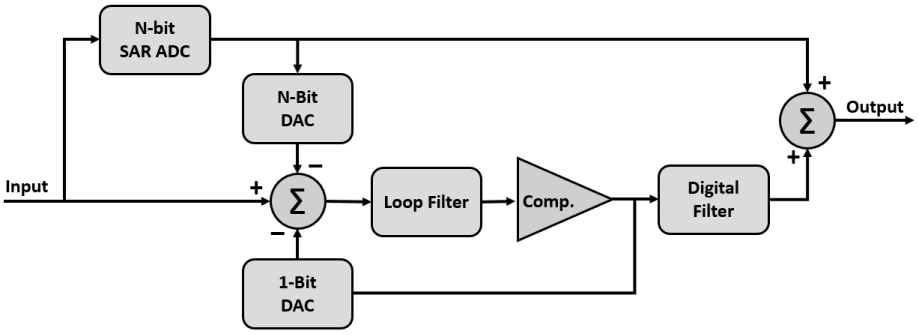

Figure 2.12: Block diagram of Zoom ADC.

In this two-step ADC, low resolution, low power coarse ADC determines the MSB bits of the input data. The MSB data is converted to an analog signal using a DAC and subtracted from the input, and Delta-Sigma ADC processes only the residue voltage. Since the voltage range of the residue voltage is much lower than the input, the power requirement of the Delta-Sigma ADC is relaxed. The output of Delta-Sigma ADC is filtered by a digital filter, and LSB bits are determined in this step. Since MSB bits are not a part of digital filtering, filter architecture is less complex, and area consumption is significantly decreased. In the ideal case, the digitally filtered output of the Delta-Sigma Modulator and the MSB bits are concatenated to obtain the output code.

In real-world analog circuits have some deviations from their ideal operations, such as offset voltage, noise, and gain nonlinearity. Coarse ADC also suffers from these problems, and directly concatenating output codes is not plausible. These nonidealities create dead spaces between the coarse and fine ADC and thus resulting significant performance drop. To prevent any missing code, over-ranging is applied. Instead of directly taking the full range of residue voltage as a voltage range of Delta-Sigma ADC, the voltage range is extended to a voltage higher than the residue voltage range. In the case of any error, voltage still stays in the stable region of Delta-Sigma ADC.

As mentioned, deviations in analog circuits and components are a significant issue. The residue generation is one of the most demanding parts of the design. The matching of the N-bit DAC, Delta-Sigma Modulator feedback DAC, and the matching between them is the limiting factor on the performance of the Zoom ADC [28]. To satisfy desired performance, the matching and linearity of this DAC must be higher than the expected ADC resolution, which is hard to achieve. Instead of designing multiple challenging DACs, two of the DACs can be combined into a single DAC. The single DAC architecture can be observed in Figure 2.13. Moreover, this architecture is suitable for digital matching techniques like dynamic element matching (DEM). DEM architecture's utilization significantly relaxes the DAC array's design requirement significantly [34]. DEM methods will be explained in detail in Chapter 3.

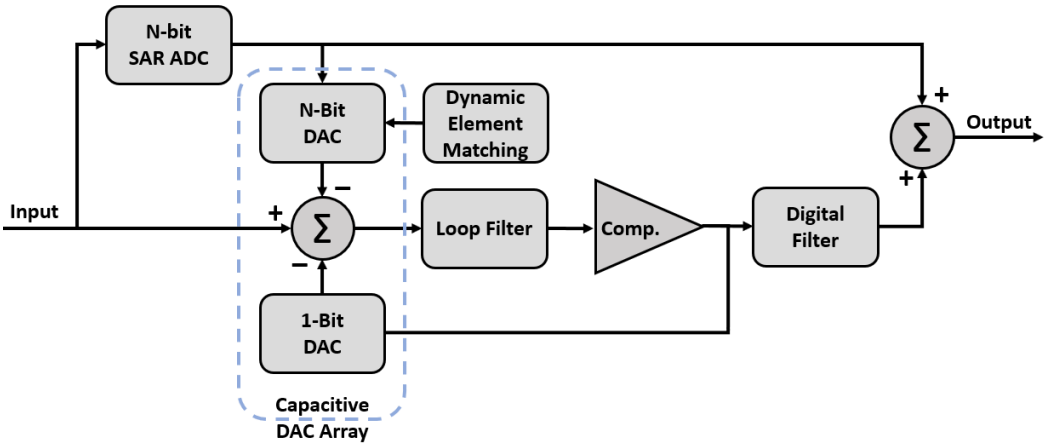

Figure 2.13: Block diagram of single DAC Zoom ADC.

2.3.2 Incremental Zoom ADC

There are two types of Zoom ADC architectures: Dynamic Zoom ADC and Incremental Zoom ADC. Dynamic Zoom ADC is utilized for measuring continuous signals. The coarse conversion is repeated for a fixed period of clock cycles, and the Delta-Sigma modulator continuously converts residue data. The time domain operation of Dynamic Zoom ADC is shown in Figure 2.14. Since Dynamic Zoom ADCs are not in the scope of this thesis work, no further investigation necessary.

In contrast, Incremental Zoom ADC is utilized for measuring quasi-static signals. For each measurement, a sequential operation is performed. Firstly, coarse ADC rapidly determines the MSB bits, then Delta-Sigma Modulator determines fine bits from the residue voltage. The transient operation of Incremental Zoom ADC is shown in Figure 2.15.

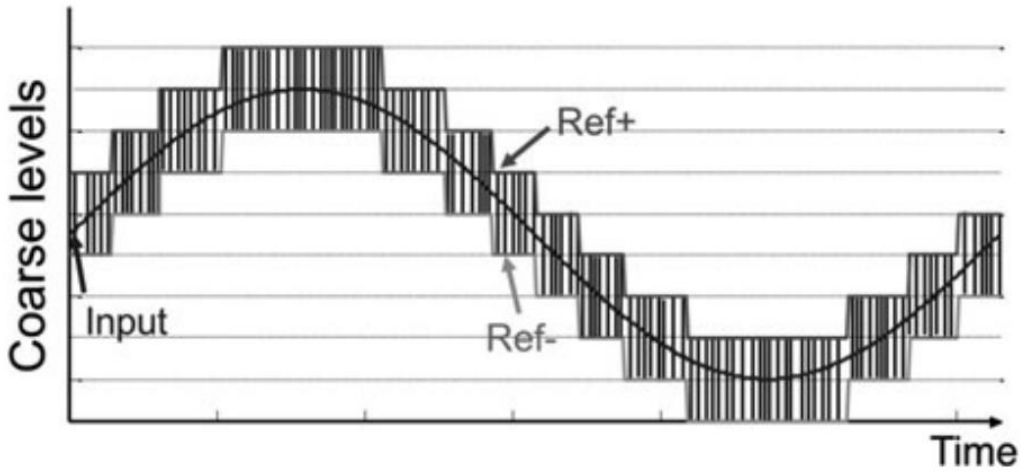

Figure 2.14: The transient operation of Dynamic Zoom ADC. [25]

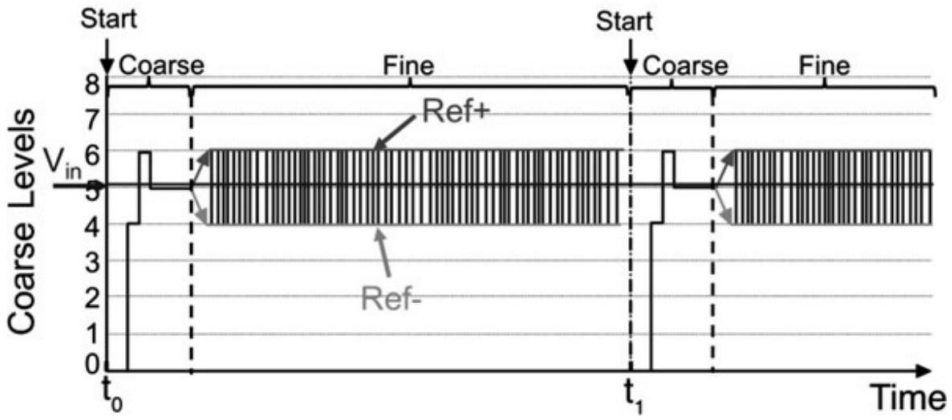

Figure 2.15: The time domain operation of Incremental Zoom ADC. [25]

The sequential architecture of the Incremental Zoom ADC allows some advantages. In some applications, the SAR ADC and Delta-Sigma Modulator share the same hardware, which decreases area use and power consumption. In this thesis work, the SAR ADC block is shared by 16 columns, which increases the area and power efficiency of the architecture. Also, the timing of the Coarse ADC and Fine ADC follows a pipelined timing diagram, where Delta-Sigma ADC can use full line time, decreasing clock frequency. The timing diagram of the pipelined operation is shown in Figure 2.16.

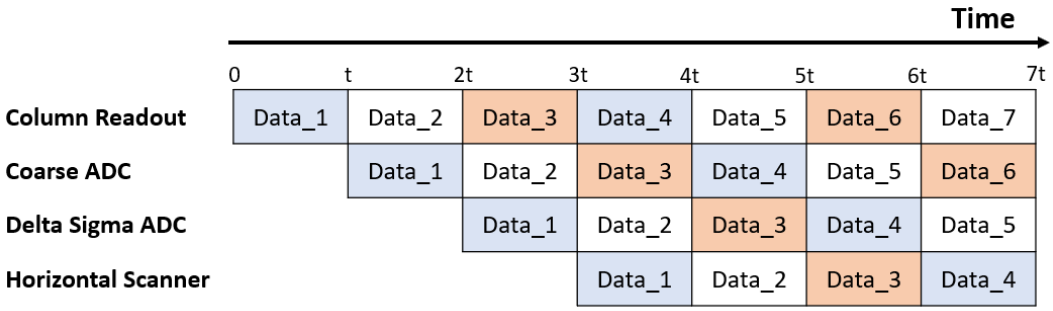

Figure 2.16: Timing diagram of proposed Incremental Zoom ADC.

CHAPTER 3

SYSTEM DESIGN

This chapter covers the design elements of the Incremental Zoom ADC in detail. The general block diagram of the Incremental Zoom ADC can be observed in Figure 3.1. As observed, the ADC consists of 4 general blocks: SAR ADC, Delta-Sigma ADC, Digital Filters, and Dynamic element matching. The system parameters and the design of the blocks need to be optimized for the desired performance. As stated in the design requirements in the high-precision mode, the design must perform 20-bit ENOB with 6 kHz bandwidth. This performance can be obtained by optimization of the resolution of SAR ADC (N), sampling frequency (f_s), over-ranging of Delta-Sigma Modulator (M), oversampling ratio (OSR), order of Delta-Sigma Modulator (L), and architecture of Digital Filter.

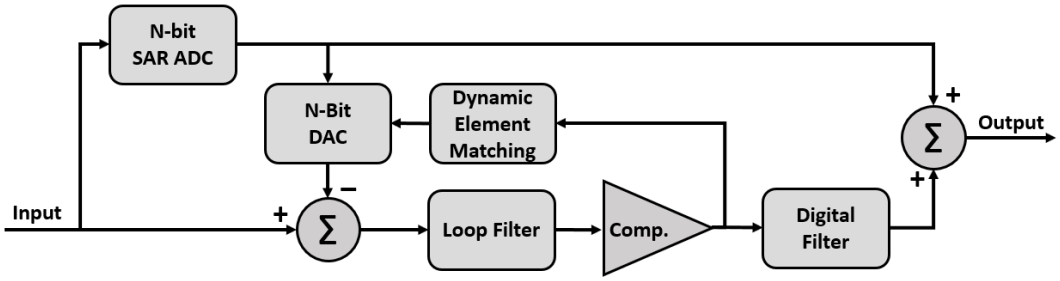

Figure 3.1: General Block Diagram of Incremental Zoom ADC.

Zoom ADC is an oversampling ADC, hence bitwise performance of the ADC is measured with dynamic range. The effective number of bits of a Zoom ADC can be calculated as:

$$ENOB = \frac{DR - 1.76}{6.02}$$

For precision higher than the 20-bit, the dynamic range must be:

$$DR(dB) > 6.02 * ENOB + 1.76$$

Therefore for 20-bit operation, the dynamic range must be higher than 122 dB

The SAR ADC's resolution directly affects the Delta-Sigma Modulator's operation. Higher the resolution of SAR ADC(N), the amplitude of the residue voltage gets smaller, thus relaxing the voltage swing and dynamic range of the Delta-Sigma Modulator. One bit increase in the resolution of SAR ADC provides a 6.02 dB increase in the dynamic range. On the other hand, higher resolution also increases the area of the SAR ADC and the DAC. For a column-parallel architecture, silicon area is a significant drawback. Also, higher resolution SAR ADCs require meticulous design and precise analog circuitry. Therefore, an optimal value for the SAR ADC resolution must be calculated. In the literature, the resolution of the ADC is selected between 4 to 6 bits [32] [28] [33] [35]. These bit ranges provide the best performance-area trade-off.

The over-ranging is the precaution for any offset and mismatch between SAR ADC and Delta-Sigma modulator. In an ideal case, there is no need for the over-ranging since the residue voltage range is the same as the voltage range of the Delta-Sigma modulator. In the actual case, error sources prevent this perfect matching, and for some voltage levels, the Delta-Sigma Modulator saturates, thus creating missing code. To prevent this problem, the voltage range of the Delta-Sigma modulator is selected to be larger than the voltage range of residue voltage. The amount of over-

ranging should be higher than the worst-case offset and error scenarios. However, increasing the over-ranging size decreases the resolution of the Delta-Sigma Modulator. In this work, over-ranging is selected as a 1 LSB. Although 1 LSB is much larger than the error sources, fractional over-ranging requires complex DAC design and brings linearity errors.

The Delta-Sigma modulator's design selection heavily affects the system's performance. The characteristic of the loop filter mainly defines the system's precision. The order of the loop filter (L) and the oversampling ratio (OSR) determines the aggressiveness of noise shaping, thus the in-band noise (IBN) level. The higher order loop filters provide better noise shaping in exchange for circuit complexity and stability issues. Higher OSR also decreases in-band noise levels and requires higher sampling frequency, thus increasing power consumption.

In general, the lower clock frequency is preferred for lower power consumption. On the other hand, lowering the clock frequency at some point does not decrease power consumption since amplifiers are noise-limited after a certain bias current [36]. The efficient clock frequency is selected as 2 MHz for the chosen CMOS technology and amplifier designs.

The optimum point must be calculated for the best performance, minimum area, and power consumption. The dynamic range of an ideal Zoom ADC can be approximated as:

$$DR\ (dB) = 1.76 + 6.02 * (N_{SAR} - M + N_{DSM}) + 10log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1) * 10log_{10}(OSR)$$

Where N_{SAR} and N_{DSM} are the quantization precision of SAR ADC and Delta-Sigma modulator, respectively. M is the over-ranging coefficient which is 1-bit. L is the order of the Delta-Sigma Modulator. The optimum range can be observed if the linear model given in Equation 3.3 is plotted. The plot of the linear model with respect to design parameters is shown in Figure 3.2.

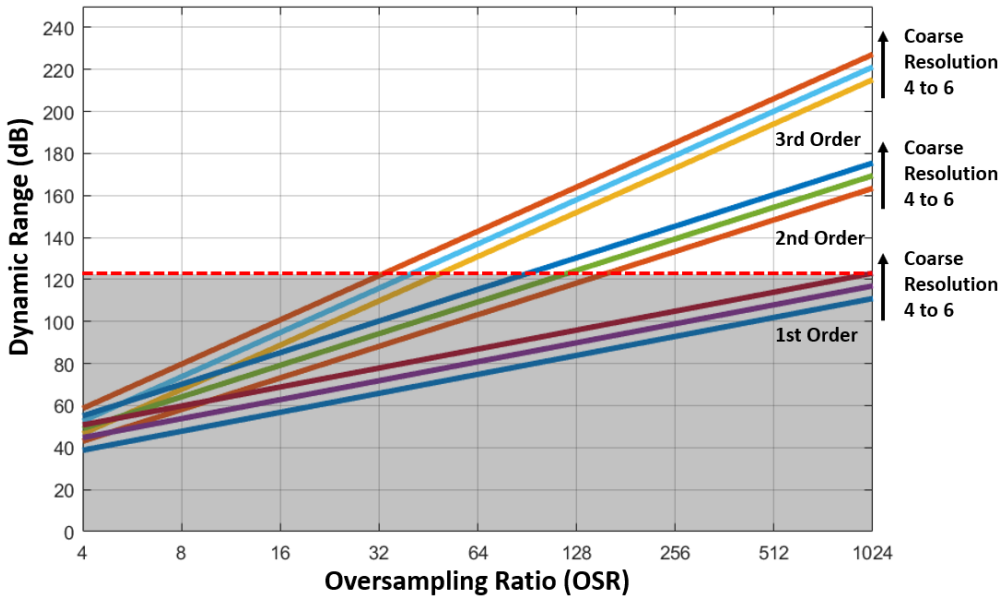

Figure 3.2: OSR vs. Dynamic Range for different loop filter order and Coarse ADC resolutions.

The Figure 3.2. visualizes the dynamic range output from the linear model with respect to the different model parameters and OSR. In the plot, N_{DSM} is 1-bit, and over-ranging (M) is 1 LSB. The border indicates the minimum required dynamic range for the design. It should be noted that the linear model is quite optimistic, especially for higher order loop filters. As the sampling frequency of the intended design is comparably low and 2 MHz clock frequency is selected, a higher OSR would be used. For 6 kHz sampling frequency and 2 MHz clock frequency, OSR of 320 is selected for high-precision mode.

Significantly large OSR improves the noise shaping, thus improving the performance of the loop filter. Considering this 2^{nd} order loop filter is a good selection due to the stability and ease of design. Moreover, Zoom ADC architecture brings design challenges for the feedback of the Delta-Sigma Modulators, and 2^{nd} order loop filter is more suitable for these design challenges.

The highest possible SAR ADC resolution is desired for maximum power efficiency. However, for the column ADCs, silicon area is a crucial design parameter. The area of SAR ADC and N-bit DAC is doubled for a 1-bit increase in the SAR ADC resolution. Therefore, considering area limitations, 5-bit resolution is the optimum coarse ADC resolution.

In Figure 3.2. the linear model is plotted for the 1-bit Delta-Sigma Modulator quantizer. Generally, a single-bit quantizer design is preferred for Delta-Sigma Modulators since multibit quantizers introduce linearity errors and design complexities. Complex mismatch shaping architectures are required for error correction, which is not preferred. However, in this thesis, mismatch shaping architecture is already employed, and the DAC structure is suitable for a 5-level quantization. 5-level quantization provides 8 dB dynamic range improvement with few drawbacks. Thus, this unique quantization structure is employed in this design.

The output of the Delta-Sigma Modulator requires precise digital filtering to yield the full performance of the modulator. Digital filters are employed at this level to filter out-of-band noise and provide parallel data. Since a high-resolution output is expected from this work, a CIC decimation filter and FIR filter combination would be an efficient solution.

Since CIC filters do not require any multiplier and limited memory [30], a higher order filter can be used for better performance. Third-order CIC filter with a 16x decimation ratio is selected for this design. The output of the decimation filter is processed with an FIR filter. The OSR of the design is flexible for different imaging modes, so a programmable integrating FIR filter is used for FIR design. The programmable nature of this filter provides the necessary flexibility for the user.

So, in this work 5-bit SAR ADC and second-order Delta-Sigma Modulator with 5-level quantization is employed with 1 LSB over-ranging. The clock is selected as 2 MHz, and OSR of 320 is aimed. In digital filtering, a 3rd order CIC filter with a 16x decimation ratio is used, and a programmable integrating FIR filter is utilized.

3.1 System Level Design of Delta-Sigma Modulator

The system-level design of the Zoom ADC is defined, and the reasons for the design selections are explained in the previous section. This section briefly explains the design selections of second-order Delta-Sigma modulator. The second-order Delta-Sigma Modulator block diagram can be observed in Figure 3.3.

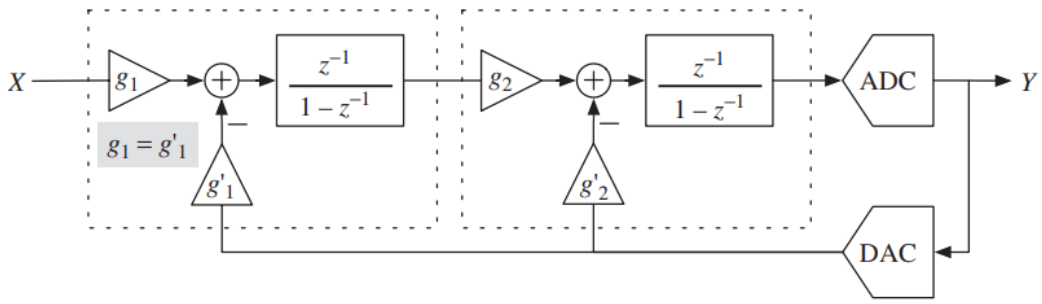

Figure 3.3: Block diagram of second-order Delta-Sigma Modulator. [23]

As observed in Figure 3.3, the second-order Delta-Sigma Modulator consists of two cascaded integrator blocks and a quantizer. Each integrator receives feedback with a weight, which is essential for the stability of the modulator. The z-domain output of the modulator could be calculated as [23]:

$$Y(z) = \frac{k_q g_1' g_2 \frac{z^{-2}}{(1-z^{-1})^2} X(z) + E(z)}{1 + k_q g_1' g_2 \frac{z^{-2}}{(1-z^{-1})^2} + k_q g_2' \frac{z^{-1}}{(1-z^{-1})}}$$

Where k_q stands for the quantizer gain. For ideal second-order shaping, the equation should be simplified as follows:

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$

This simplification could only be made if the feedback coefficients satisfy:

$$k_q g_1' g_2 = 1$$

$$k_q g_2' = 2$$

In this thesis, the feedback should be compatible with the Zoom stage. Thus, the design coefficients are selected as:

$$g_1 = g_1' = 1$$

$$g_2 = 1$$

$$g_2' = 2$$

$$k_q = 1$$

The Delta-Sigma Modulator design with coefficients can be observed in Figure 3.4.

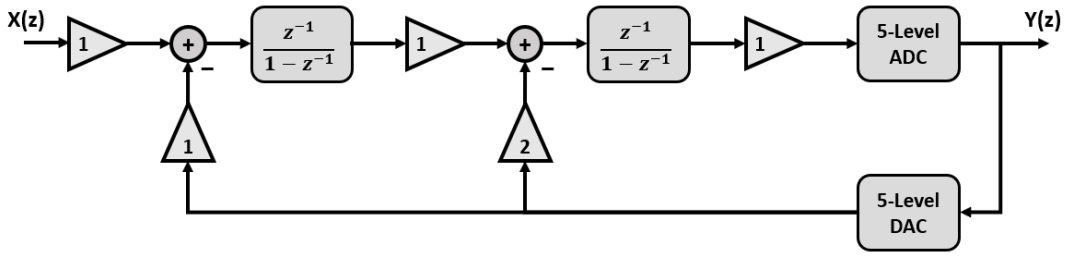

Figure 3.4: Delta-Sigma Modulator with coefficients.

The operation of the Delta-Sigma Modulator is verified using Simulink. The simulated spectrum of the designed Delta-Sigma Modulator is shared in Figure 3.5. Since there is no noise source in this simulation, the quantization noise shaping of the filter can be observed.

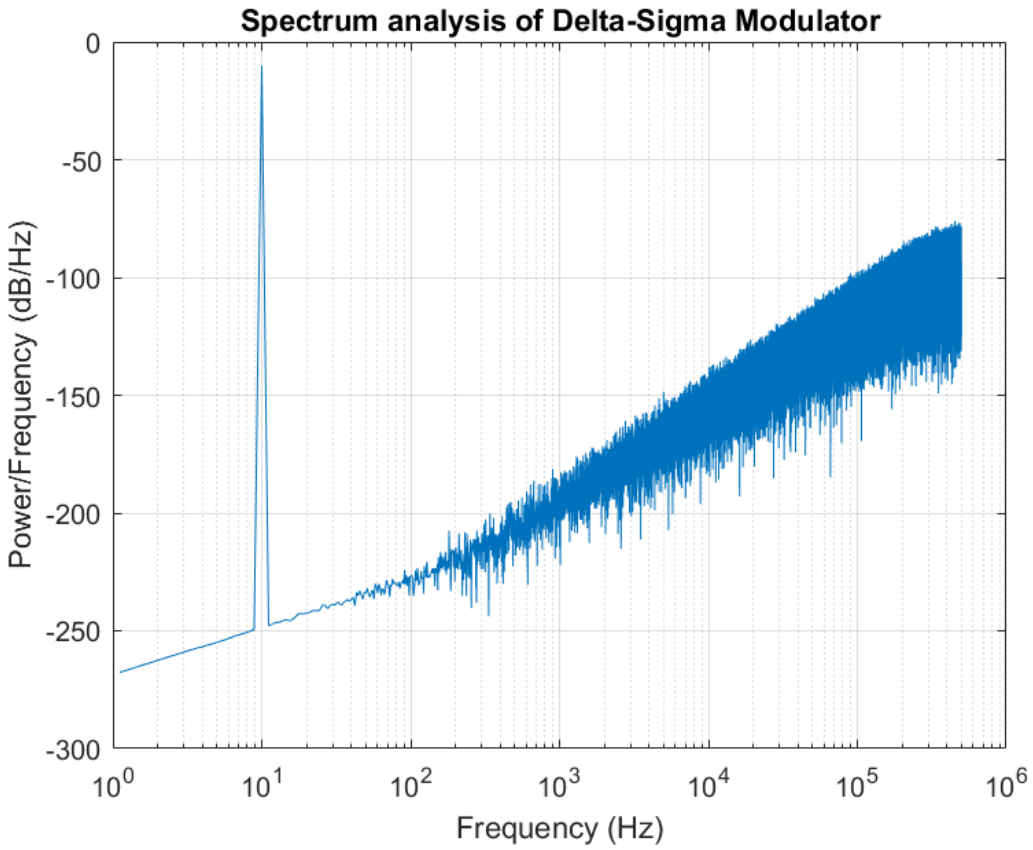

Figure 3.5: Spectrum analysis of the Delta-Sigma ADC.

3.2 Dynamic Element Matching

Matching is an important issue in the Zoom ADC design. The DAC at the input of the Delta-Sigma Modulator is the dominant error source, and any mismatch error directly affects the modulator's linearity. For the 20-bit performance, the Delta-Sigma DAC needs at least 20-bit performance. However, that level of accuracy is hard to achieve. In this work, metal-insulator-metal (MIM) capacitors are used, and the standard deviation of these capacitors is written as [37]:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{WL}}$$

Where ΔC is the difference in the capacitor. A_C is the mismatch coefficient of the process, which is 0.4% μm for the 180nm CMOS technology. W and L are the width and length of the unit capacitor. Therefore, unit capacitor selection is vital for the matching requirement. The critical case for the matching is the MS crossing. For the desired matching, the 3-Sigma of the MSB crossing must be lower than half LSB [37].

$$3\sigma\ (D_{in} = 16) < 0.5LSB$$

Where LSB for the 20-bit operation is:

$$LSB = \frac{2.88}{2^{20}} = 2.75\mu V$$

In the conventional methods achieving 0.5 LSB performance requires unit capacitors larger than 10 pF [37], which is impossible for a column-parallel ADC. Area and power consumption are crucial for this operation, and it is not feasible with large unit capacitors. The spectrum analysis of the Zoom ADC with capacitor mismatch is shown in Figure 3.6.

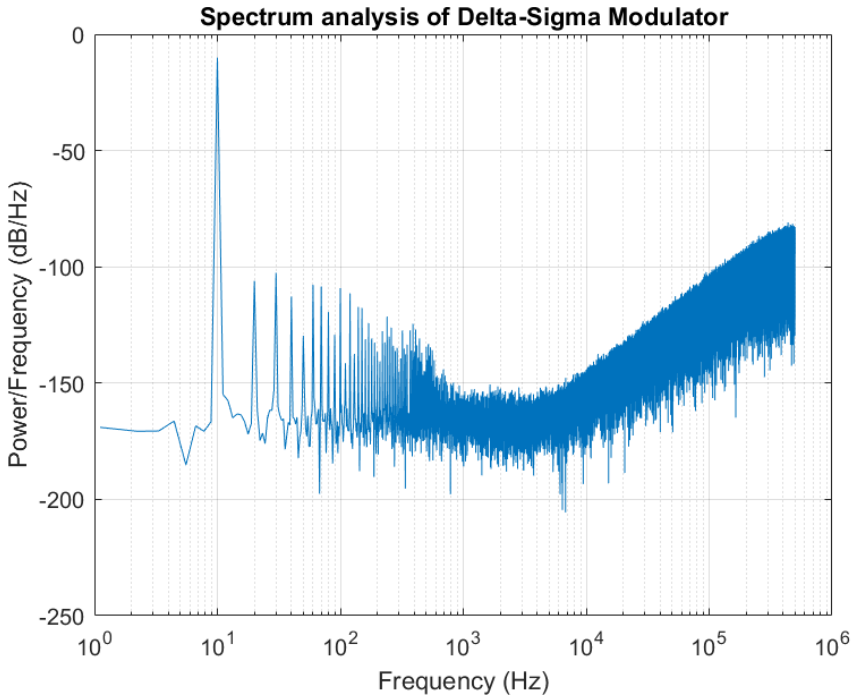

Figure 3.6: Spectrum analysis of Delta-Sigma Modulator with 80fF unit capacitance and no mismatch correction.

In order to satisfy the required matching, instead of using large unit capacitors, different techniques could be employed. The most widely accepted methods are trimming [38], calibration [16], and dynamic element matching (DEM) [34]. Compared with other methods, DEM is more suitable for oversampling ADCs.

Unlike the other mismatch correction methods, DEM architectures do not aim to eliminate mismatch but modulate the mismatch. In the signal domain, the modulated mismatch behaves like noise and could be filtered at the digital filter level [34].

Figure 3.7. shares the block diagram of the DEM architecture. The general working principle of the DEM is that the input data is converted to the thermometer-coded signal and connected to the capacitor array. At each period, the capacitor's connections are changed to modulate mismatch. The pattern of the capacitor changing method defines the mismatch shaping.

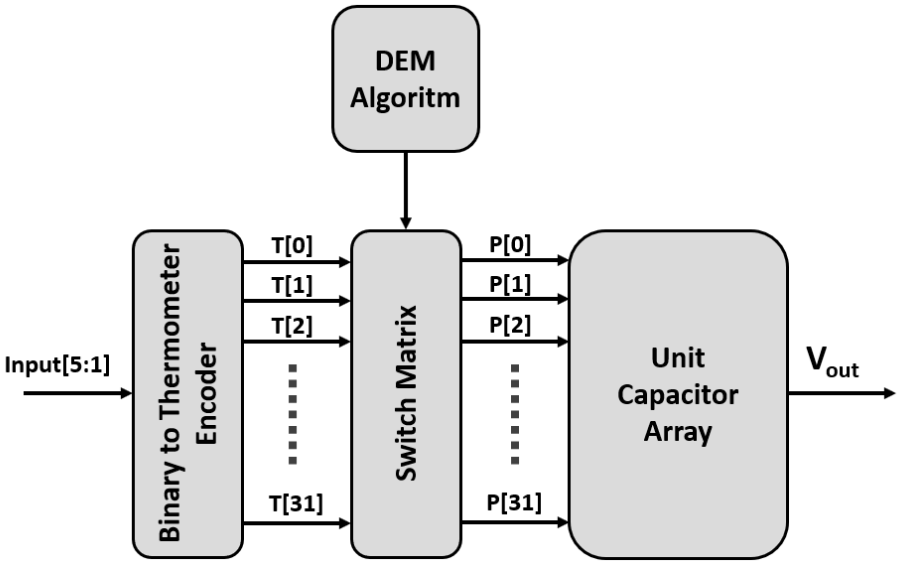

Figure 3.7: Block diagram of the Dynamic Element Matching.

Large variations of DEM architectures are published in the literature. However, the general operation is the same since all operate with the same underlying principle [34]. The algorithm assumes there is no knowledge about the mismatch and blindly shapes the mismatch error. Widely used algorithms are Random DEM, Barrel-Shift DEM, and Data Weighted Averaging (DWA) DEM.

In the Random DEM, the active unit capacitors are selected randomly. This approach provides zero mismatches on average. Due to the random nature, no harmonics are generated in exchange for higher noise power. However, the randomization process requires serious design effort, and the resulting circuit covers a large area. Therefore, the use of Random DEM is not feasible for this project.

The Barrel-Shift DEM utilizes fixed pattern shifting of the capacitor selection. A barrel-shift pointer tracks the first element of the capacitor array. At each cycle, the pointer is updated with a fixed coefficient. The implementation of the Barrel-Shift DEM is relatively easy and requires few components. However, the fixed pattern of the algorithm creates tone and harmonics, which are not desired.

The data weighted averaging (DWA) DEM is a hardware-efficient solution for mismatch shaping DEM. The working principle is quite similar to the Barrel-Shift DEM. Figure 3.8. illustrates the operation of the DWA algorithm. Instead of a fixed coefficient, the barrel shift pointer is updated with the previous output code of the DAC array. This method shapes the mismatch with a modulator similar to the first-order Delta-Sigma modulator, preventing tone generation [20].

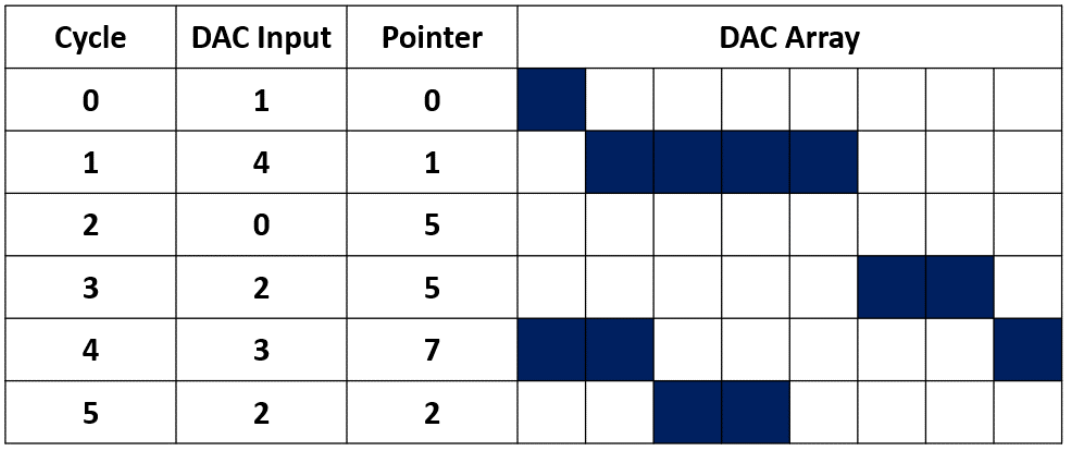

Figure 3.8: Illustration of the operation of the 3-bit DWA algorithm.

DWA DEM architecture is implemented in this work due to superb performance, easy hardware implementation, and low area consumption. The performance of the Zoom ADC under the proposed DEM algorithm versus no mismatch correction is shared in Figure 3.9. The DEM method suppresses spurs and harmonics caused by capacitor mismatch effectively.

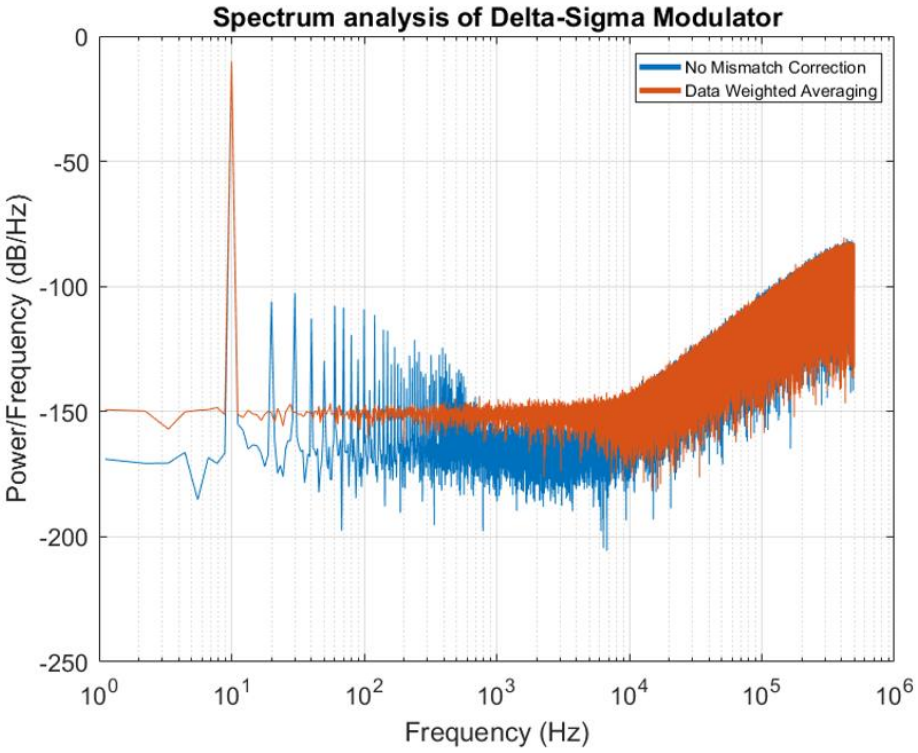

Figure 3.9: Spectrum analysis of Delta-Sigma Modulator with no mismatch correction and DWA.

3.3 Digital Filter Design

In most of the oversampling ADCs, the digital filters are not implemented on-chip. Implementing the filter with more resource and programmable arrays is much more efficient and provide more flexibility. In this work, the data output of the modulator is much more than the serializer block can handle thus, it is necessary to implement on-ship digital filters. The implemented filter must be area efficient and should provide high noise suppression performance. Third-order CIC decimation filter and programmable integrating FIR filter are used in this design. Since these filters provide different characteristics and are utilized with different aims both are investigated separately.

3.3.1 CIC Decimation Filter

The CIC filter is a commonly preferred architecture for on-chip designs since they do not require any multiplication or extra memory space [39]. As observed in Figure 3.10, the general architecture of a CIC filter is quite simple yet very efficient. The filter consists of a digital integrator, decimator, and digital differentiator. The block diagram of integrator and differentiator is shared in Figure 3.11 and Figure 3.12. respectively.

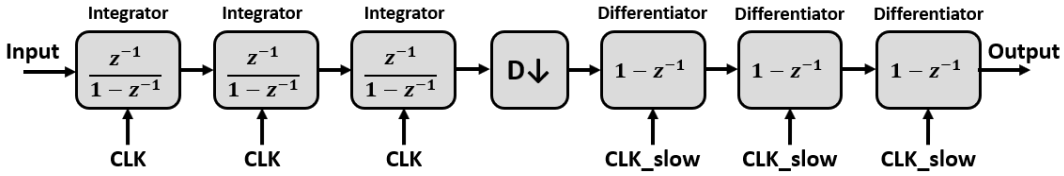

Figure 3.10: Block diagram of CIC filter.

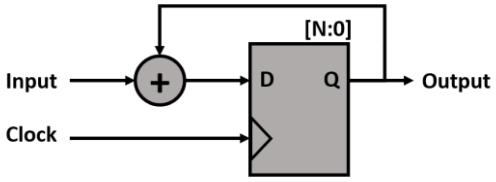

Figure 3.11: Block diagram of digital integrator.

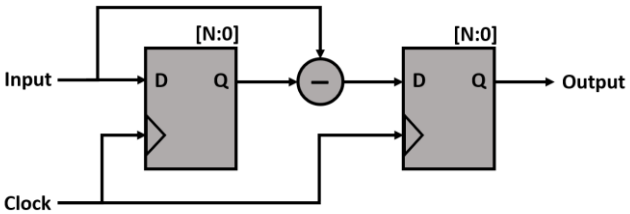

Figure 3.12: Block diagram of digital differentiator.

The CIC filter provides a narrowband low-pass filter characteristic, which is desirable for the Incremental Zoom ADC. Increasing the filter order and decimation ratio sharpness of the filter and out-of-band rejection could be improved. Therefore, for this design, third order CIC filter with a 16x decimation ratio is selected. This filter provides 14-bit parallel output every 16 cycles. The filter characteristic of the designed filter can be observed in Figure 3.13.

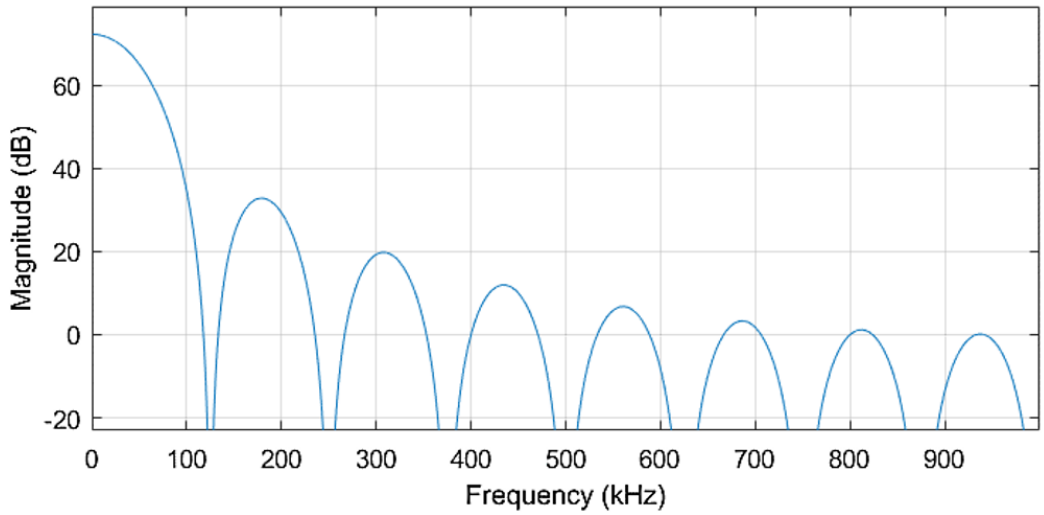

Figure 3.13: Filter characteristic of a third order decimation filter.

The filter performance is sufficient for the designed ADC, and the FIR filter enhances performance further. However, the filter covers a large area which is a problem for a column ADC. The current architecture requires 176 Register and 120 Full Adder, which occupy 675µm x 50µm area. This work proposes a new architecture to decrease area consumption without any performance loss. Figure 3.14. shows the new CIC filter architecture used in this design. The third integrator, decimator, and third differentiator can be merged into a new block. If the third integrator is reset at every decimation period, the output signal is equal to the output of the third differentiator. This architecture makes it possible to implement a CIC filter in smaller areas without disrupting the filter's operation or performance.

The new filter design requires 126 registers and 85 full adders, which occupy 450µm x 50µm area. The integrator with reset architecture could perform the same operation with 35% smaller area consumption and less power.

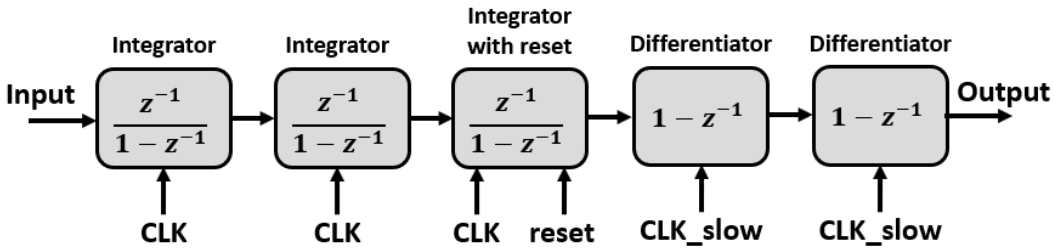

Figure 3.14: Block diagram of CIC filter with integrator with periodic reset.

3.3.2 Integrating FIR Filter

FIR filters are one of the popular digital filter architectures. Their impulse response has a finite duration and thus settles to zero in infinite time. Their equation has no feedback, so FIR filters are always stable [40]. The general architecture of the N-Tap FIR filter can be observed in Figure 3.15. The filter consists of three blocks, registers, multipliers, and full adders. For each tap, one set of these blocks is used. That creates a large area consumption for multiple tap filters. On the other hand, higher taps are preferred for better performance and noise rejection.

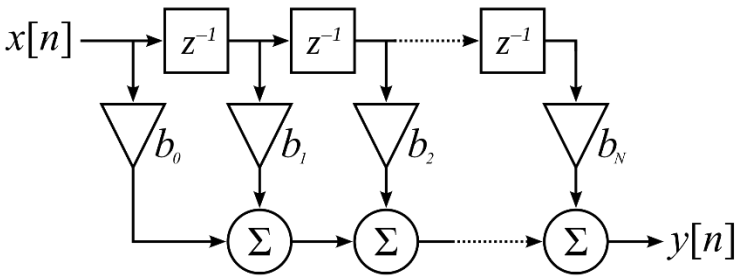

Figure 3.15: Block diagram of N-Tap FIR filter.

The multiplication operation of the FIR filter is crucial for its performance. These coefficients define the transfer function of the filter and are called windows. Different window architectures provide different characteristics, and the window selection directly defines the passband, in-band gain, and out-of-band rejection. The frequency response of the 15-Tap FIR filter with the Hann window can be observed in Figure 3.16. Due to large area consumption, the multiplication operation is an issue for on-chip applications. In the literature, instead of hefty multiplier blocks, a sum of parallel shift blocks approach is used for area-efficient solutions [41] [42]. This approach reduces area consumption significantly but limits the applicable filter windows. Moreover, the reduced filter area is still too large for a column-parallel ADC.

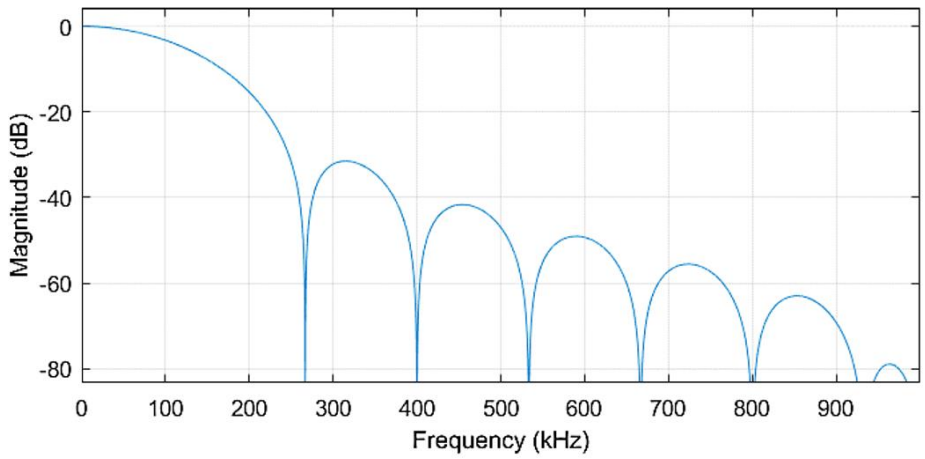

Figure 3.16: Filter characteristic of 15-Tap Hann window FIR filter.

This work uses a new type of FIR filter to reduce area consumption and provide high performance. Figure 3.17. shares the block diagram of the integrating FIR filter. Different from the conventional FIR filters, integrating FIR filter is used in this design. The designed ADC is suited for incremental data thus, continuous data flow is not necessary for the filter. Only the final product is important for this design. Integrating FIR filter is a great fit for this application.

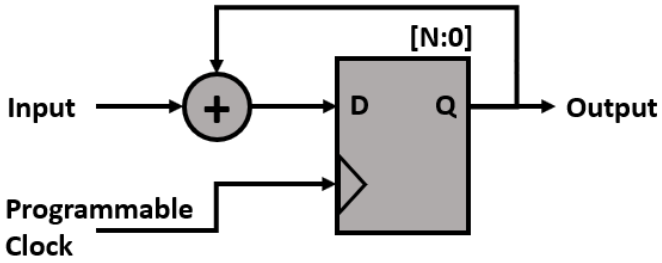

Figure 3.17: Block Diagram of integrating FIR filter.

As observed in Figure 3.17, the design is simple yet very effective. All the delay and multiplication operations are squeezed into a single integrator with a program clock. At each input period, the fast program clock triggers the integrator multiple times, creating a multiplier effect for the input. An example timing diagram for a 3-5-5-3 window FIR filter is shown in Figure 3.18.

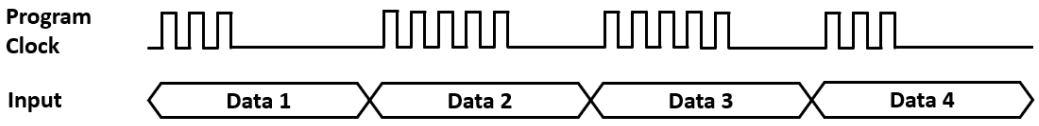

Figure 3.18: Timing diagram of 4-Tap Integrating FIR Filter.

This architecture significantly decreased the area consumption of the FIR filter. Compared with a conventional 16-Tap FIR filter, this architecture occupies 92% less area while providing the same final result.

This architecture defines the window type by the adjusting number of program clock pulses. The digital timing generator directly controls the period and number of ticks of the program clock, thus the user. This feature gives excellent flexibility to the filter design since different imaging modes and scene conditions require different filter performances.

CHAPTER 4

CIRCUIT IMPLEMENTATION

In this chapter, the implementation of the general building blocks of the Zoom ADC is shared in detail. As mentioned in the previous parts, Zoom ADC consists of 3 major blocks: Coarse ADC, Fine ADC, and Digital Filters. The design details, circuit schematics, and simulation data of these blocks and their subblocks are provided. At the end of each subsection, the layout implementation of these blocks and their area consumption are shared. The last subsection explains the top-level implementation of the Zoom ADC and chip-level auxiliary block design briefly.

The system-level design of Zoom ADC is covered in Chapter 3. In the implementation phase, some minor changes were applied to the architecture for the better area and power management. Figure 4.1. shows the revised block diagram of column Zoom ADC. As mentioned, Zoom ADC is the hybrid of two ADCs, 5-bit SAR ADC and Delta-Sigma ADC. In the pipelined timing operation, the time window for the operation of 5-bit SAR ADC is much larger than the requirement. Therefore, 16 columns share a single SAR ADC for more power and area efficient solution.

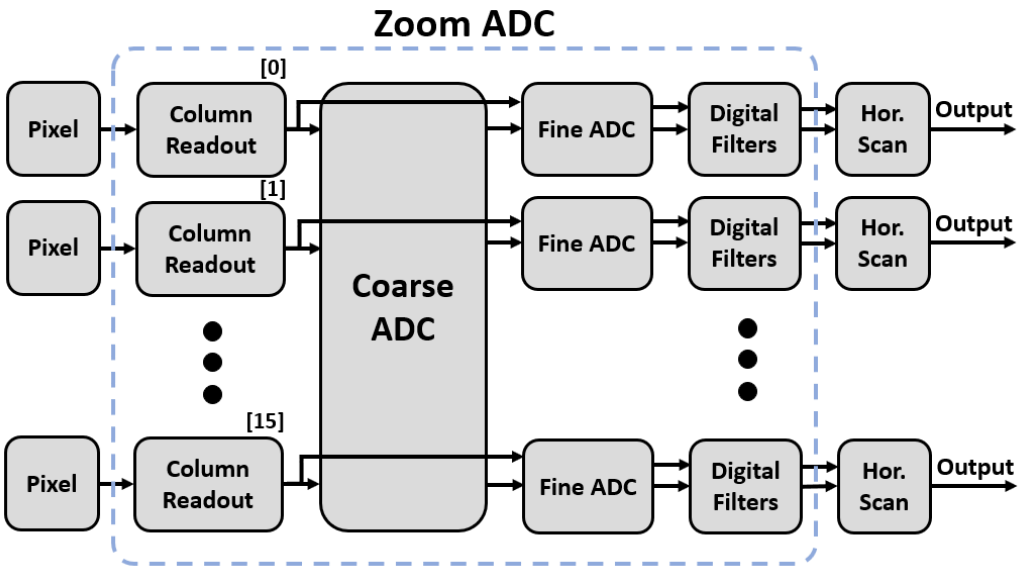

Figure 4.1: The block diagram of Zoom ADC.

4.1 Coarse ADC

The implementation of the coarse ADC is an important step in the design of Zoom ADC. The SAR ADC is selected since it is a power-efficient and robust architecture. Figure 4.2. shows the block diagram of the SAR ADC. Since the requirement for the SAR ADC is relaxed, the main concern for the design is power and area consumption. The design needs to perform a 5-bit conversion with 100 KS/sec in high-precision mode and 1 MS/sec in ultrafast mode. This sampling speed is easily achievable since the over-ranging of the Delta-Sigma ADC relaxes the performance requirement of the ADC significantly. 0.75 LSB quantization error is acceptable for the ideal operation, which is 67.5 mV. Therefore, a careful, and simple design is sufficient for the SAR ADC. SAR ADC consists of 3 main blocks, DAC, comparator, and SAR Logic. The design of the subblocks is covered in their respective subsections.

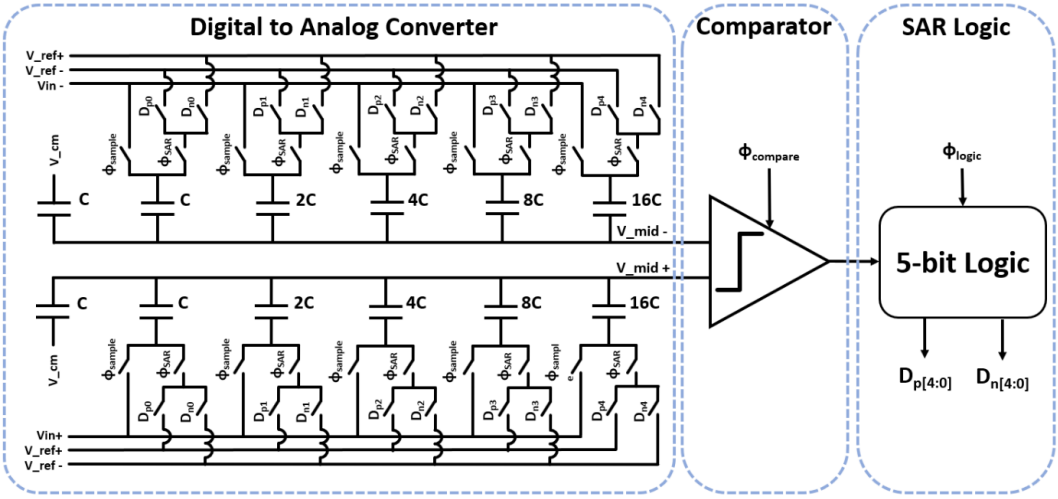

Figure 4.2: Block diagram of the 5-bit SAR ADC.

4.1.1 Digital to Analog Converter

The first major block of the SAR ADC is the DAC block. In this design, input sampling DAC architecture is selected for better linearity and a more straightforward design for fully differential input. Since the power consumption is the primary concern of the coarse ADC design, binary weighted capacitor array architecture is selected. The capacitors are implemented with metal-insulator-metal (MIM) capacitors. For the sample and hold operation, parasitic insensitive bottom plate sampling architecture is selected, ensuring that the input and reference voltages are affected by the parasitic capacitances at the same rate, thus creating no nonlinearity [43].

Figure 4.3. displays the schematic design of the DAC array. The main operation of the DAC consists of two phases, input sampling, and comparison. During the sampling phase, the differential input data is sampled at the bottom plate of the capacitors. In the comparison phase, the input data is compared with its differential at 5 clock cycles with a binary search algorithm.

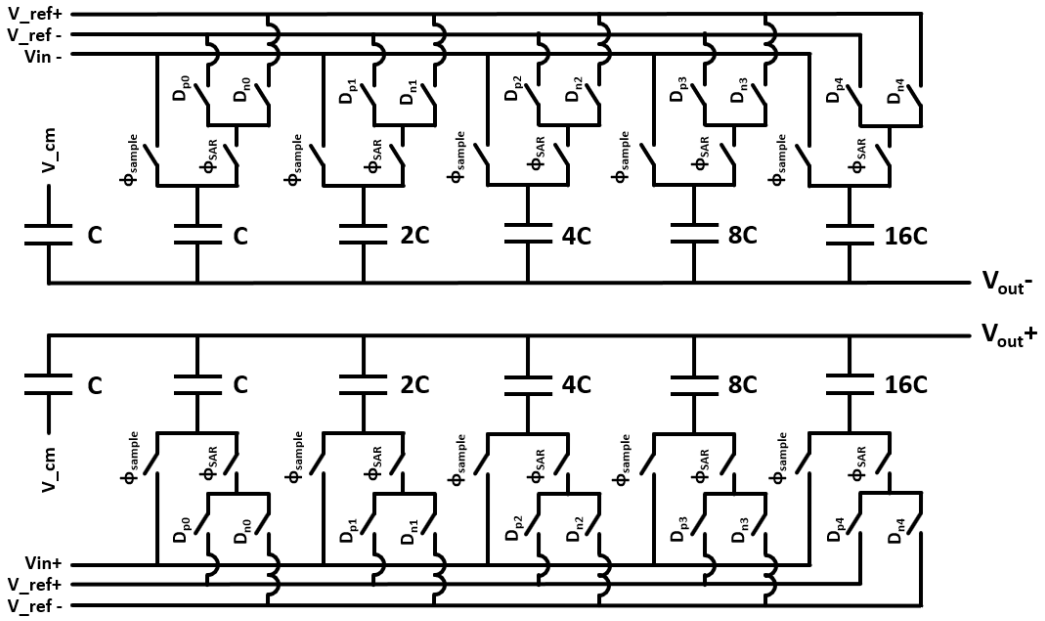

Figure 4.3: Schematic design of the 5-bit binary-weighted DAC array.

Generally, capacitor sizing is one of the crucial parts of the DAC design. On the other hand, for the 5-bit operation, the kTC noise and capacitor mismatch are negligible due to the wide LSB voltage range of DAC and the minimum size of the unit capacitor defined by the technology [37]. Thus, the unit capacitor is selected as 80 fF, the same size as the Delta-Sigma Modulator's unit capacitor, for ease of design.

4.1.2 Comparator

The second block of the SAR ADC is the comparator block. With the DAC block, the comparator defines the performance of the ADC. Multiple comparator architectures are developed to ensure the best performance. In this work, the comparator's requirements are much more relaxed, and the primary expectation from the comparator is to provide a simple and robust operation with low power consumption.

The StrongArm Latch architecture is a dynamic comparator with very low power consumption. The schematic of the StrongArm Latch is shown in Figure 4.4. The static power consumption is zero, which is vital since the coarse ADC operates on a low-frequency clock. Moreover, it produces rail-to-rail output, which makes it easier to digitalize output [44]. This architecture can provide high sensitivity and robust operation with efficient power consumption.

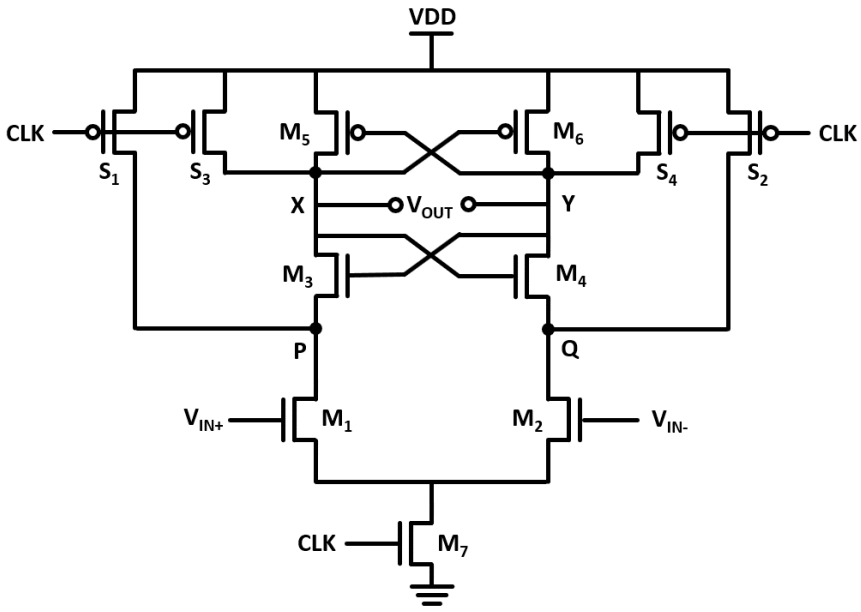

Figure 4.4: Schematic design of the StrongArm Latch.

The operation of the comparator has two phases controlled by a clock signal. When the clock is low, the nodes P, Q, X, and Y of the latch is reset through switches S_1-S_4. With the rising edge of the clock, reset switches S_1-S_4 go off, and M_7 goes on. As current starts flowing, the M_1 and M_2 differential pair turn on and draw current proportional to the V_{in+} and V_{in-}. In this phase, M_3-M_6 are still off; therefore, M_1 and M_2 discharge C_P and $C_{Q,}$ respectively. Since input voltages of M_1 and M_2 are different and discharge is directly proportional to the input voltage, voltage imbalance occurred between P and Q nodes. After that, V_P and V_Q discharge to V_{DD}-

V_{TH3-4} M_3 and M_4 are on and amplifies the voltage imbalance. The positive feedback drives outputs to the two different rails. As voltages reach the rail, the latch architecture of M3-6 stops current flow and prevents static current consumption [45].

The designed comparator provides a 2.5 mV input referred offset, which is sufficient for the operation. The settling time for 1mV differential output is 900 ps, which makes it operable up to 250 MHz clock rate. The comparator consumes 2.01μW power from the 3.3V supply.

4.1.3 SAR Logic

The final block of the SAR ADC is the digital logic called successive approximation register. The main aim of this block is to perform a binary search algorithm by controlling DAC. A clock controls the logic, and with respect to the comparator input, logic performs the binary search algorithm. In this work, the SAR Logic is developed based on the architecture proposed by T.O. Anderson [46]. The schematic of the SAR logic is shown in Figure 4.5.

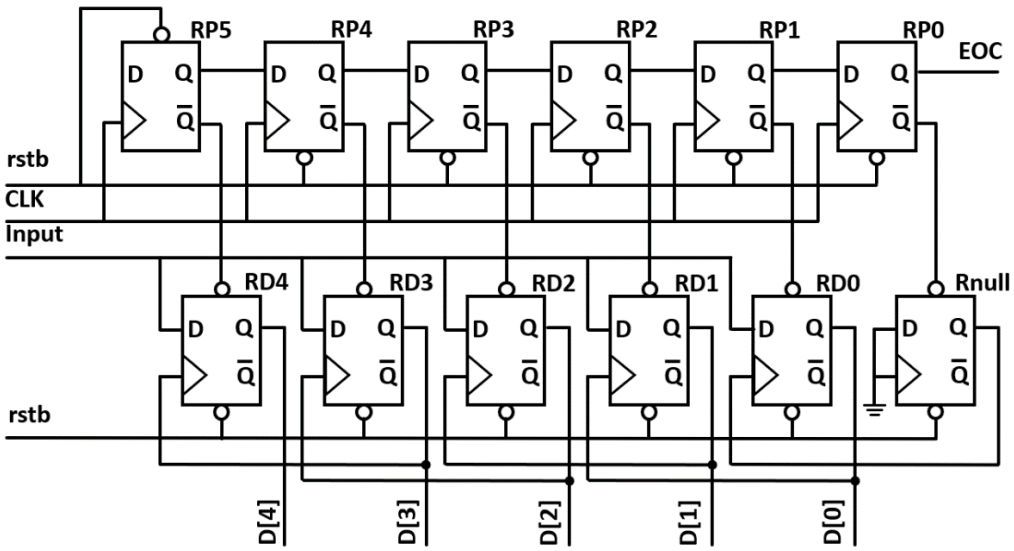

Figure 4.5: Schematic of the SAR logic.

The structure consists of two rows of registers, the top having a pointer and the bottom generating conversion data. At the start of the conversion, all registers are reset, and the RP5 gets set and generates the first pointer. The pointer sets the RD4 and the MSB to logic “1”. Then, the DAC voltage is set with respect to the logic output and comparison performed. If the comparison is “true”, the RD4 stays at “1” and the pointer sets the next register RD3 to “1”. If the comparison is “false” the R_{D4} changed to “0” and the pointer sets the next register RD3 to “1”. The same operation is performed for each data register in the following cycles. At the end of conversion, the last pointer register R_{P0} generates the end of conversion (EOC) flag, which loads output data to a register.

4.1.4 Top-level

The Coarse ADC of the Zoom ADC is designed as a 5-bit SAR ADC to achieve optimum performance and power consumption. The layout of the designed ADC can be observed in Figure 4.6. Since 16 columns share it the width of the layout must be 800µm.

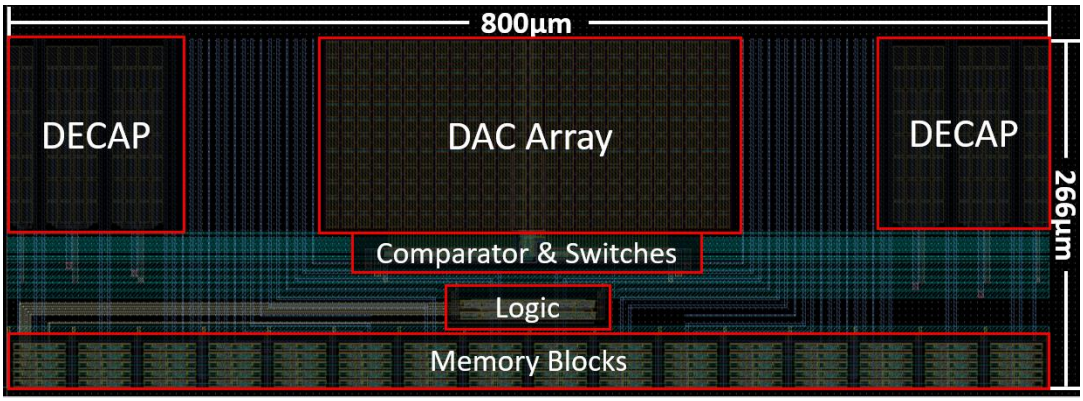

Figure 4.6: Layout of the Coarse ADC.

Top-level simulation of the coarse ADC to verify its operation is crucial. The designed SAR ADC has a fully differential operation with a wide operation range (0.16V - 3.04V). The top-level schematic of the ADC can be observed in Figure 4.2. The timing diagram of the SAR ADC can be observed in Figure 4.7.

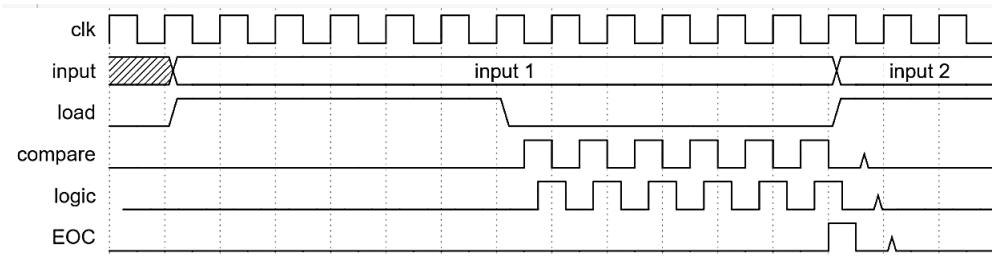

Figure 4.7: Timing Diagram of the SAR ADC.

For the top-level simulation, firstly, the operation of the ADC for four different voltage inputs (1.064V, -0.7575V, 0.2375V, -0.9645V) is provided in Figure 4.8. For clearer visualization, the DAC's output voltages are provided with the SAR Logic output. Secondly, the SAR ADC is tested with a wide range of voltages for the full voltage range. For 1024 voltage input, the output of the SAR ADC is processed by a Verilog-A block, and the error plot is provided in Figure 4.9.

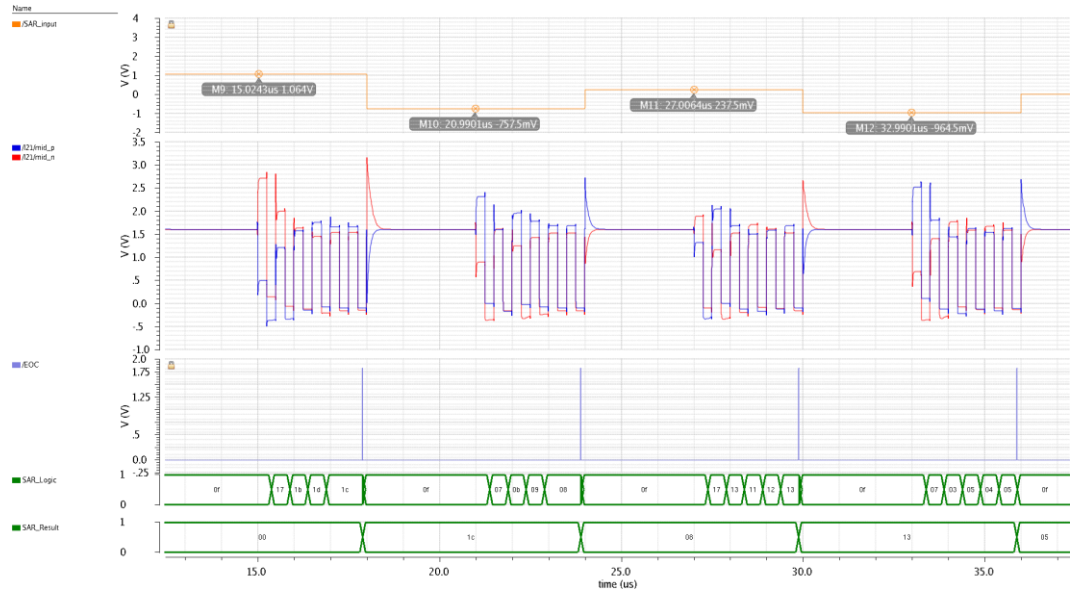

Figure 4.8: DAC output and SAR output plot for four different voltage input (1.064V, -0.7575V, 0.2375V, -0.9645V).

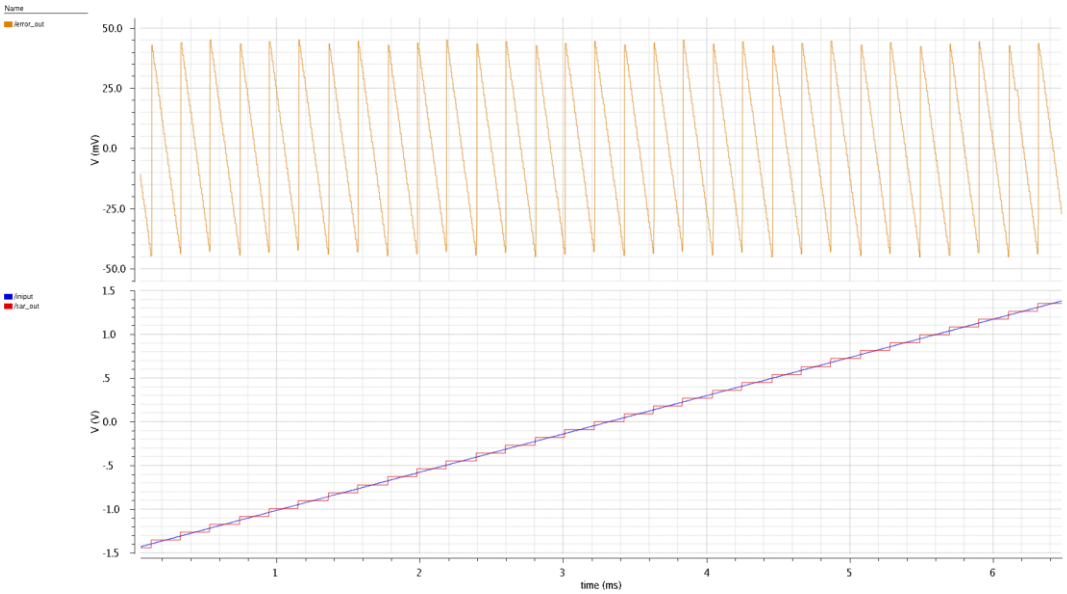

Figure 4.9: Error plot of the SAR ADC.

The SAR ADC has a 0.5-bit LSB INL and DNL sufficient for the operation. The offset error is 2.4 mV which is better than the acceptable level. The comparator's power consumption defines the SAR ADC's power consumption. Thus, the designed SAR ADC consumes 4.45µW power from the 3.3V supply. Since 16 column shares a single SAR ADC, the power consumption per column is 0.278µW.

4.2 Fine ADC

The Fine ADC is the central part of the Zoom ADC. Most of the resolution is generated by this block, thus careful design is mandatory. The essential design details of the Fine ADC are stated in Chapter 3, and the selection of design parameters is explained clearly. The block diagram of the second order Delta-Sigma Modulator can be observed in Figure 4.10. As observed, the modulator consists of 3 main blocks, first integrator, second integrator, and the quantizer. The design of the subblocks is covered in their respective subsections.

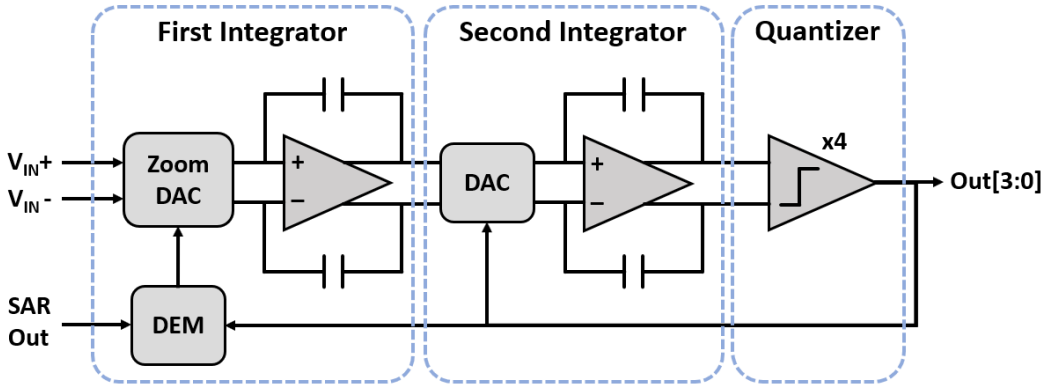

Figure 4.10: Block diagram of the second order Delta-Sigma Modulator.

4.2.1 First Integrator

The first integrator is the most demanding part of the modulator design. Unlike the standard Delta-Sigma modulator design, Zoom ADC has additional challenges for the first integrator block, Zoom DAC, and DEM block. The block diagram of the first integrator can be observed in Figure 4.11. As observed, the first integrator consists of 3 subblocks, Zoom DAC, DEM, and OTA. The detailed design of these subblocks is covered in their respective subsections

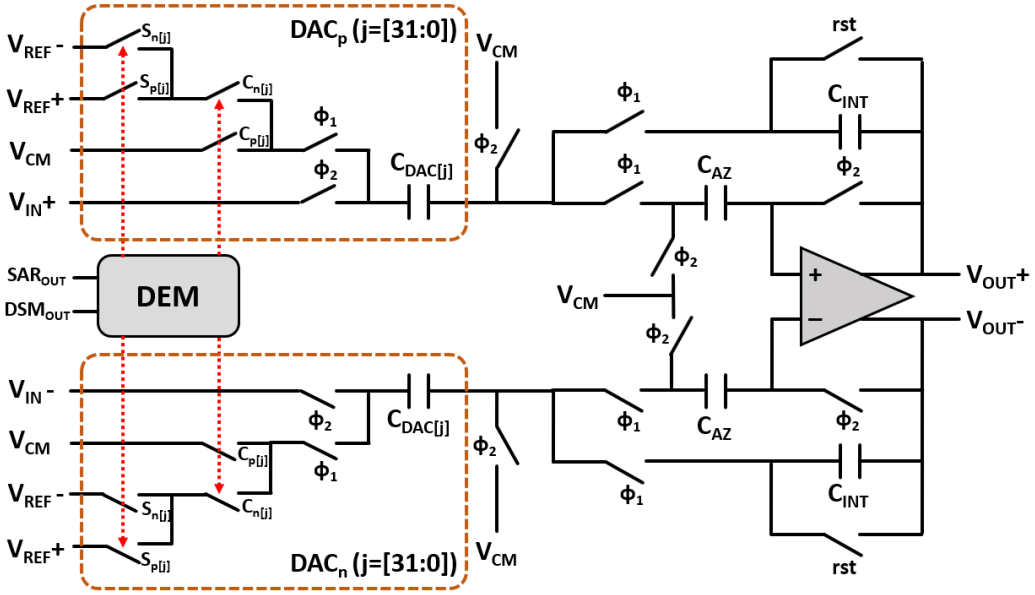

Figure 4.11: Block diagram of the first integrator.

4.2.1.1 Zoom DAC

Zoom DAC is a 5-bit unary capacitive DAC, which also acts as the first integrator's sampling capacitor. The schematic of the Zoom DAC can be observed in Figure 4.12. The capacitors are implemented using MIM capacitors. For higher linearity, the DAC sampling structure is implemented using parasitic insensitive integrator

architecture [43]. The DAC has two inputs combined by the DEM block: Coarse ADC output and 5-level modulator feedback. The integrator capacitance is 2.56pF; therefore, the unit capacitor is selected as 80fF.

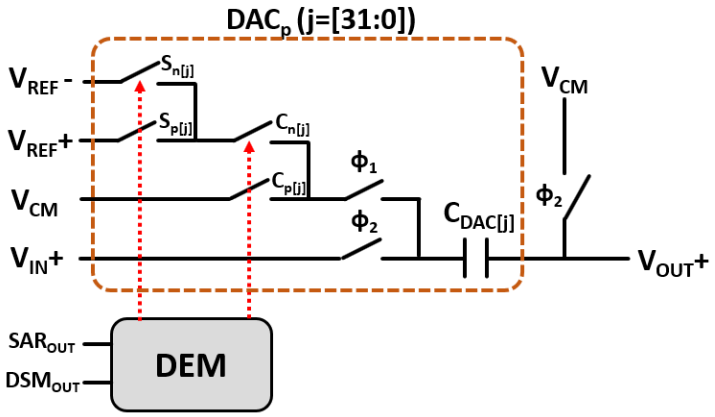

Figure 4.12: Schematic of the positive side of Zoom DAC.

In this design, different from the SAR DAC, the DAC voltage is controlled by 3 reference voltages, V_{ref+}, V_{ref-}, and V_{CM}. This architecture provides half LSB precision, which is necessary for 5-Level quantization.

The main operation of the DAC consists of two phases, input sampling, and integration. At the ϕ_1 (sampling phase), the differential input data is sampled at the bottom plate of the capacitors. At the ϕ_2 (integration phase), the input and DAC data are charged to the integration capacitance.

4.2.1.2 DEM

Mismatch correction of the Zoom DAC is crucial for reaching the expected performance from the ADC. This work uses data weighted averaging (DWA) architecture for mismatch shaping. The block diagram of the DEM architecture can be observed in Figure 4.13.

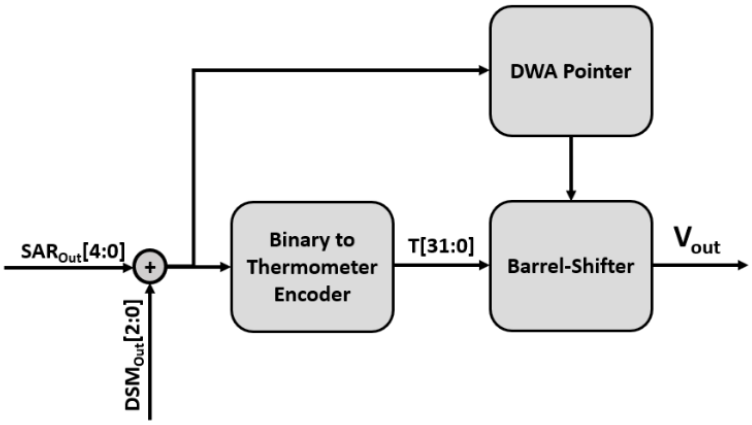

Figure 4.13: Block diagram of the DEM logic.

As observed from the figure, firstly, the output of the SAR ADC and feedback of the Delta-Sigma Modulator are added. The resulting data is converted to a thermometer code by a binary to thermometer encoder. In a parallel branch, the binary addition is fed to the DWA pointer, which calculates the shift amount of data with respect to the DWA algorithm. A barrel-shift block shifts the thermometer-coded data with respect to the DWA pointer. The resulting data is connected to unit capacitors of the DAC array.

4.2.1.3 OTA

The first integrator is the start of the signal path, and noise shaping does not affect the OTA input noise and input offset. Thus, the first integrator OTA design is crucial for the Delta-Sigma Modulator's operation. The designed OTA needs to have a high gain, no offset, low input noise, and sufficient bandwidth.

The gain of the OTA must be higher than the square of the OSR for no dynamic range loss [23]. For 300 cycles of oversampling, the required gain for ideal operation is approximately 95dB. Any gain lower than 95dB creates a dynamic range decrease from the ideal case. On the other hand, the ideal case does not include noises and

mismatch errors which already limits the operation of the Zoom ADC. Therefore, a gain above 70 dB is sufficient for the required operation.

Another critical issue is the input offset. The offset voltage is a DC error and is directly added to the input signal. Due to the filters' low pass characteristics, it is impossible to eliminate offset voltage by post-processing. To eliminate the effect of the offset voltage, switch capacitor input auto-zero architecture is used.

Different from the Delta-Sigma ADCs, the voltage swing of the first integrator is narrow in the Zoom ADC. For the 2.88V voltage range, the input voltage range is 90 mV. Thus, a 200mV voltage swing is sufficient for the operation. Based on this information, the fully differential telescopic amplifier is a good fit for this architecture. A telescopic amplifier provides good noise performance, high gain, and high gain-bandwidth [47], which is crucial for the operation. Figure 4.14 shows the schematic of the designed telescopic amplifier, while Figure 4.15 shows the schematic of the common-mode feedback (CMFB) circuit used in the telescopic amplifier.

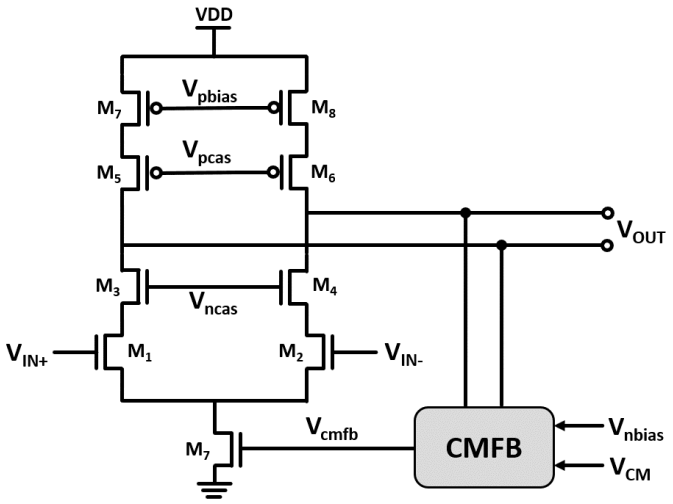

Figure 4.14: Schematic of the Telescopic OTA.

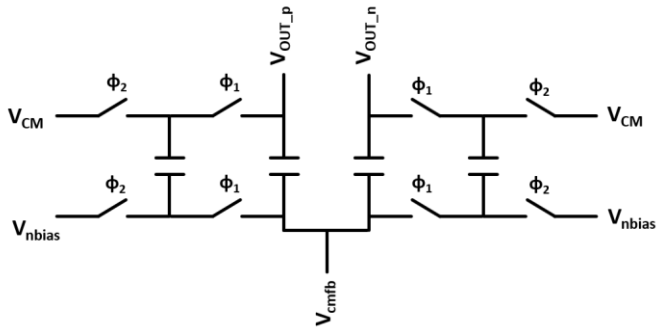

Figure 4.15: Schematic of the common-mode feedback (CMFB) circuit used in the telescopic amplifier.

Figure 4.16 shares the AC analysis of the designed Telescopic OTA. Since the designed OTA is used with a switch capacitor auto-zero circuit, shown in Figure 4.11, the AC analysis performed with auto-zero capacitance and leakage paths connected. As observed in Figure 4.16, the auto-zero capacitance creates a leakage at the low frequencies, creating a bandpass characteristic. For proper operation, the low-frequency pole must be smaller than the clock frequency.

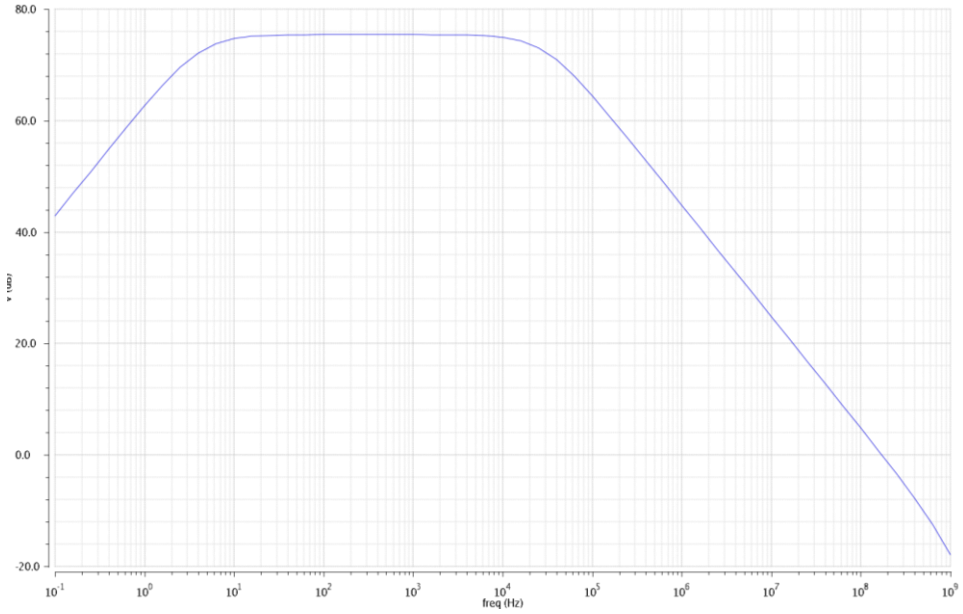

Figure 4.16: Gain vs. frequency plot of the Telescopic OTA.

In Figure 4.17, the spectral noise plot of the designed OTA is shown. The OTA is designed for switch capacitor operation and as mentioned earlier, the switch capacitor auto-zero circuit is implemented for offset cancelation. Therefore, a pnoise simulation is performed for 2.5 MHz sampling clock.

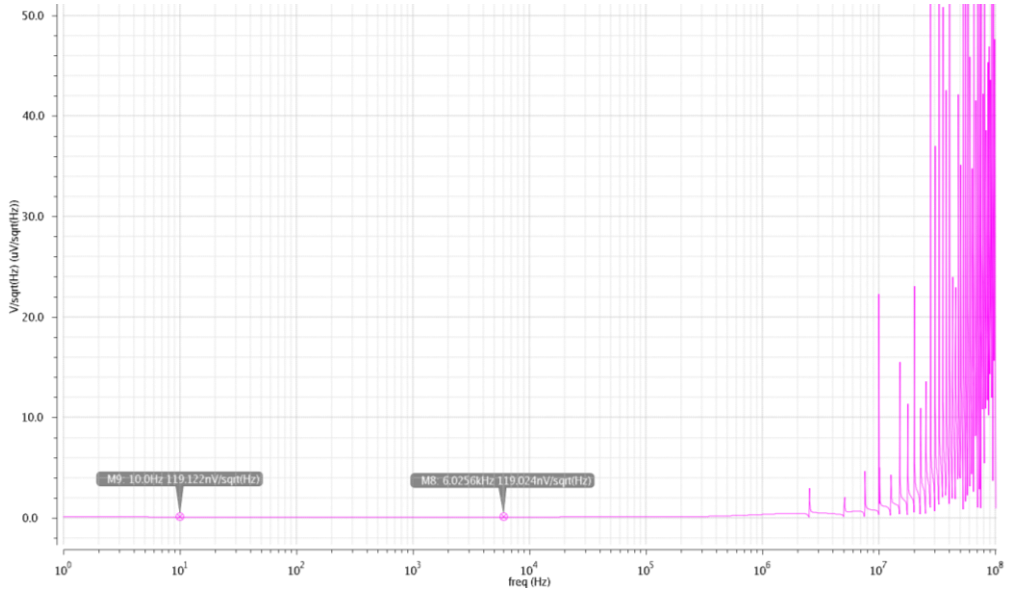

Figure 4.17: Spectral noise density of the Telescopic OTA.

As observed from the simulations, the Telescopic OTA provides 75 dB midband gain with 170 MHz unity gain bandwidth. The low-frequency pole is below 10 Hz, which is much below the sampling frequency and has no negative effect on the operation of the integrator. In the high-precision mode, the power consumption of the OTA is 200 µW from the 3.3 V supply. For ultrafast mode, the power consumption is doubled for higher unity gain bandwidth, resulting 400 µW power consumption.

In pnoise simulation, the input noise level is measured as 119 $nV/\sqrt{Hz}$ at the operation region. In high frequencies, noise spikes are observed due to clock artifacts. Spikes are observed on the 2.5 MHz integrator clock and its harmonics. These noise artifacts are unimportant since their frequencies are much higher than the sampling frequency and can be effectively filtered out.

4.2.2 Second Integrator

The second integrator is the second block of the Delta-Sigma modulator. Since the gain of the first integrator mitigates the input error sources, the design of the second integrator is much more relaxed. The schematic of the second integrator can be observed in Figure 4.18. The figure shows that the second integrator consists of 2 subblocks, DAC and OTA. The detailed design of these subblocks is covered in their respective subsections

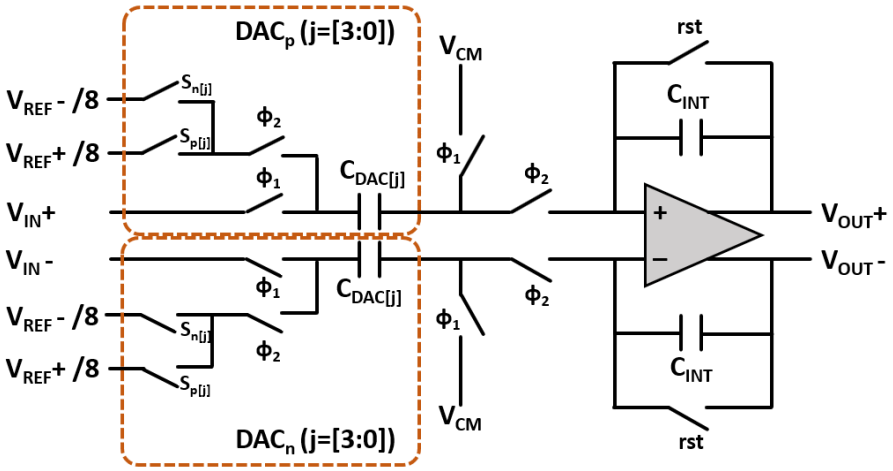

Figure 4.18: Schematic of the second integrator.

4.2.2.1 DAC

DAC of the second stage is a 2-bit unary capacitive DAC directly controlled by the output of the Quantizer. Figure 4.19. shares the schematic of the DAC. The capacitors are implemented using MIM capacitors. Similar to the first integrator DAC, parasitic insensitive integrator architecture is used. Since noise specifications are relaxed, kTC noise is less significant in this block, and small integration capacitance is preferred for decreasing power consumption. The integrator capacitance is 240fF, so unit capacitance is selected as 120fF.

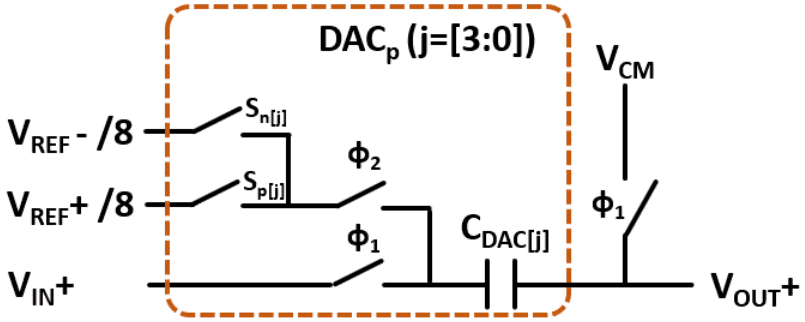

Figure 4.19: Schematic of the second integrator DAC.

The DAC architecture is straightforward and controlled by only positive and negative reference voltages. However, since the Delta-Sigma Modulator only converts the residue voltage, the reference voltage must be 90mV. The Zoom DAC solves this issue in the first integrator, where reference voltages V_{ref+}, V_{ref-} are used. However, in the second integrator DAC, this architecture will consume a large area and increase the system's complexity. Instead of a large DAC array, a second reference voltage set is introduced. The second references are 1/8 of the original reference voltages and enable to use of 2-bit DAC.

4.2.2.2 OTA

The second integrator OTA design is relaxed since the error sources after the first stage are attenuated by the gain of the first stage. Similar to the first integrator, the gain of the OTA is defined by the OSR. However, for the second integrator, the gain must be higher than the OSR. For 300 cycles of oversampling, the required gain for ideal operation is approximately 50 dB, which is easy to achieve. Because of the given reasons, the optimum solution is to implement a low-power OTA for this design. In this design, the OTA of the first integrator is used, with the W/L ratio halved. The supply voltages are adjusted according to it, and power consumption is decreased.

The designed Telescopic OTA has 72 dB gain with 160 MHz unity gain bandwidth. In the high-precision mode, the power consumption of the OTA is 100 μW from the 3.3 V supply. In the ultrafast mode, the power consumption is increased for higher unity gain bandwidth, resulting a 150 μW power consumption.

4.2.2.3 Quantizer

The quantizer is the final block of the Delta-Sigma Modulator. In general applications, 1-bit ADC is preferred due to its simple and robust design. In this work, a multi-bit quantizer is employed due to limited OSR. Since higher bit quantizers create linearity problems at the modulator, a 5-level quantizer is preferred in this architecture. The block diagram of the quantizers can be observed in Figure 4.20.

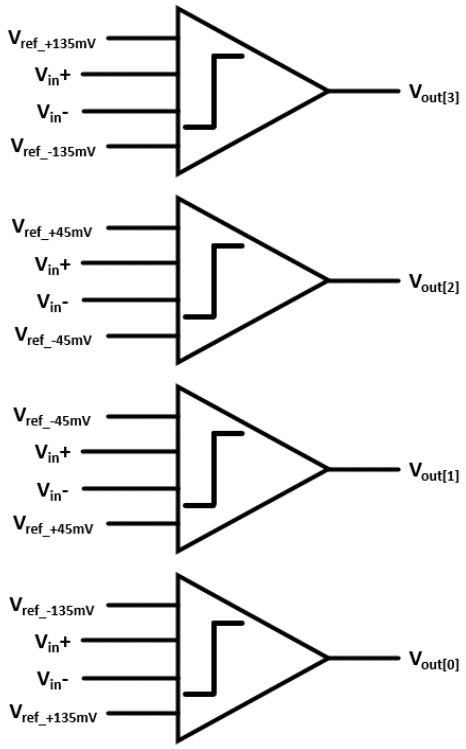

Figure 4.20: Block diagram of the 5-Level Quantizer.

As observed from the figure, four comparators require different reference voltages. The reference voltages are generated from the reference voltage used in the second integrator, which is 1/8 of the main reference voltage. For the generation of comparison reference voltages, the Kelvin divider DAC is used [48]. Figure 4.21 shows the schematic of the voltage divider. In Delta Sigma Modulators, the requirements from the comparator are not demanding; therefore, the comparators used in the quantizer are the same as the comparator of the SAR ADC, whose schematic can be observed in Figure 4.4.

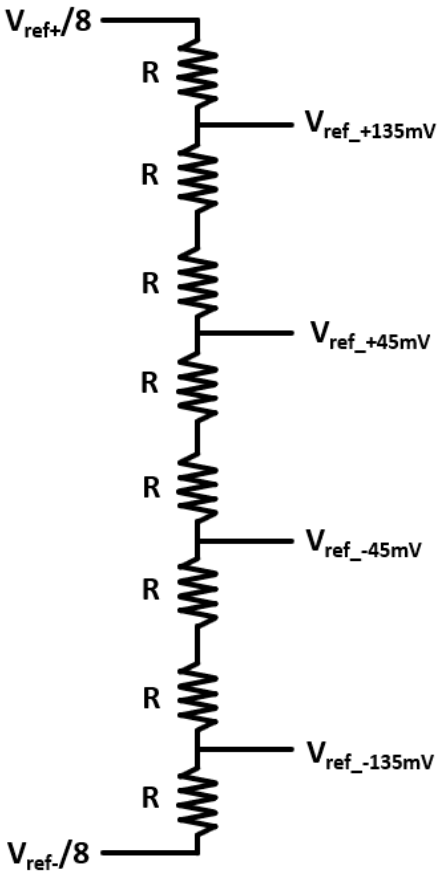

Figure 4.21: Schematic of the voltage divider.

4.2.3 Top-level

The Fine ADC of the Zoom ADC is designed as a second-order Delta-Sigma Modulator to achieve high precision. The layouts of the designed subblocks: first integrator, second integrator, and quantizer is shown in Figure 4.22, Figure 4.23, and Figure 4.24, respectively. The layout of the Delta-Sigma Modulator is shared in Figure 4.25.

Figure 4.22: Layout of the first integrator.

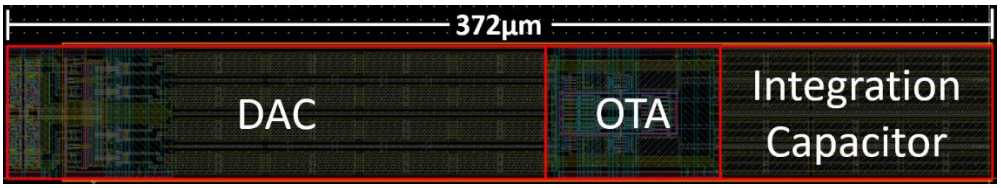

Figure 4.23: Layout of the second integrator.

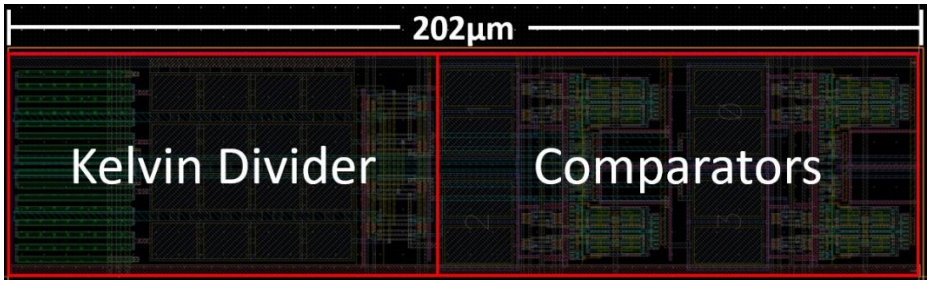

Figure 4.24: Layout of the Quantizer.

Figure 4.25: Layout of the Delta-Sigma Modulator.

Top-level simulation of the Fine ADC to verify its operation is crucial. The designed Delta-Sigma Modulator operates in a narrow range between 1.51V – 1.69V. The top-level schematic of the Delta-Sigma Modulator can be observed in Figure 4.10. The timing diagram of the Delta-Sigma Modulator is shared in Figure 4.26.

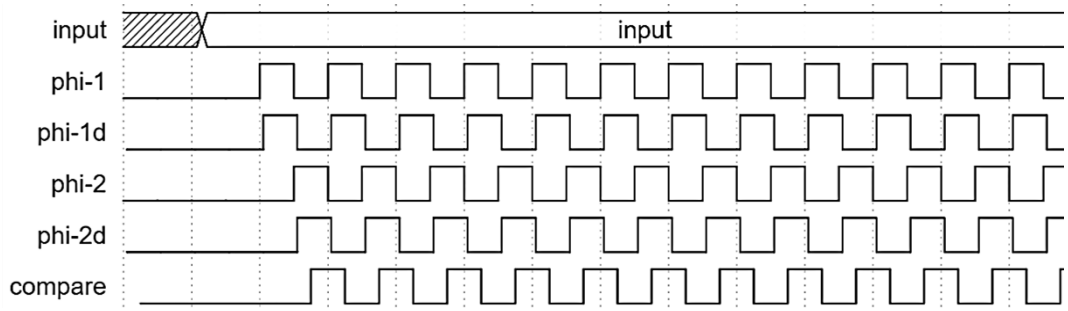

Figure 4.26: Timing Diagram of the Delta-Sigma Modulator.

For the top-level simulation, it is impossible to test full resolution with Cadence Analog Design Environment. The simulation time exceeds the plausible design cycle; thus, full-range simulations are performed in MATLAB and MATLAB Simulink. The subblock simulations are performed in Cadence Analog Design Environment, and their results are ported to the MATLAB for consistent simulation of the Delta-Sigma Modulator. In Figure 4.27, the simulation result of the operation of the Delta-Sigma Modulator for 1.593 V input is shared. In Figure 4.28. the MATLAB Simulink spectrum analysis of the modulator is shared with all noise sources placed, and the DEM algorithm is activated. In figure 4.29. the entire voltage range MATLAB simulation of the modulator is shared. In this simulation, input is swept between 1.51 V – 1.69V to observe the error plot of the modulator. In this simulation, modulator output is converted to the 20-bit parallel data by digital filters for better visualization.

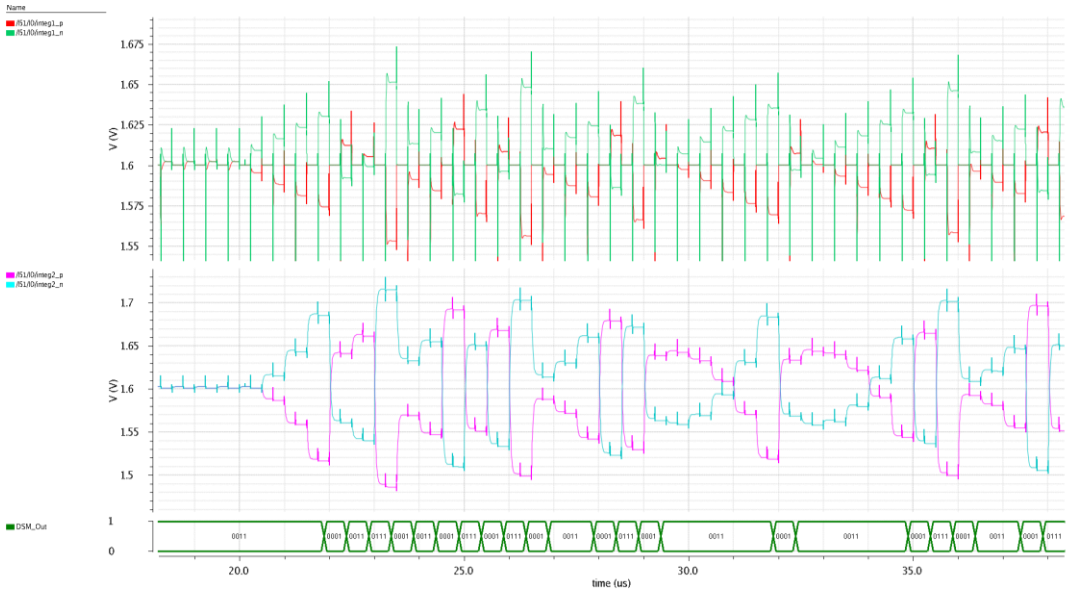

Figure 4.27: Output plot of the first integrator (top), second integrator (middle), and Delta-Sigma Modulator (bottom) for -7mV input.

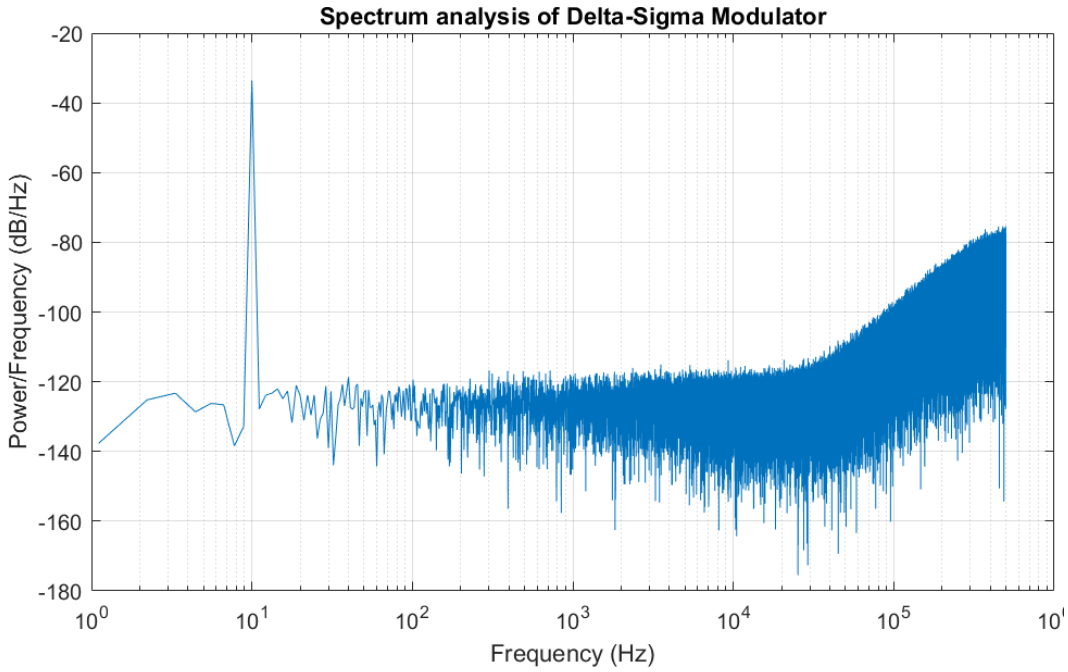

Figure 4.28: Spectrum analysis of Delta-Sigma Modulator.

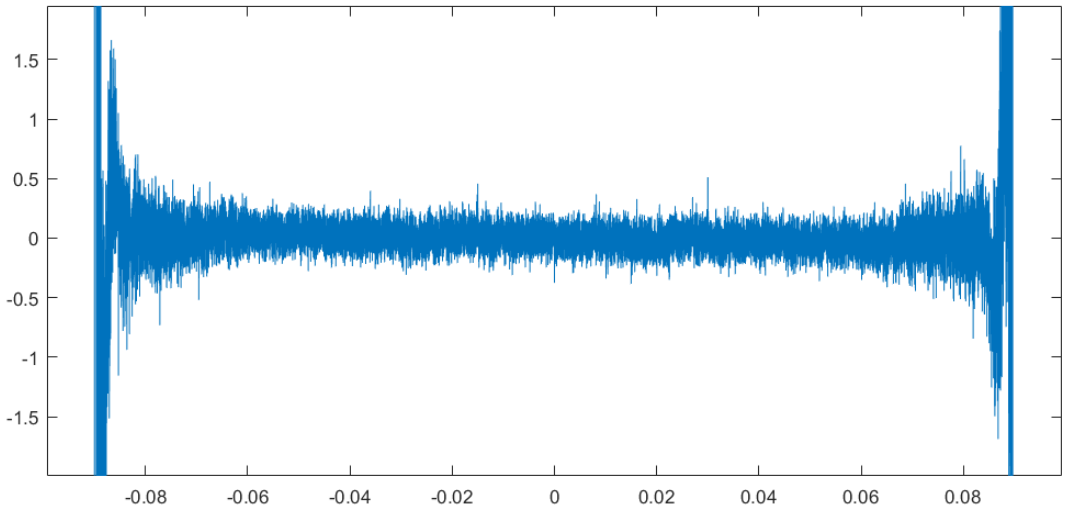

Figure 4.29: Error plot of the Delta-Sigma Modulator.

In Figure 4.27, the operation of the Delta-Sigma Modulator is verified in Cadence ADE for a single input, and power consumption is measured as 346µW. In Figure 4.28. the SNR of the Zoom ADC can be measured as 95.5 dB. In Figure 4.29, the error plot of the modulator is provided for the 20-bit operation. As observed from the plot, the INL and DNL of the modulator are lower than 0.5-bit between the 1.555V – 1.645V range. This region is the primary operating range of the modulator in Zoom ADC configuration. The unused region is important for the over-ranging since SAR ADC is not ideal. The error caused by offset error and mismatch is compensated with the over-ranging of the modulator. As observed from the plot, the input voltages close to the reference regions, the error is much higher than the 0.5 LSB. This region modulator is unsuitable for the conversion, thus allowing a 15 mV over-ranging margin. As covered in previous sections, the error of the SAR ADC is much lower than this margin.

4.3 Digital Filters

Digital filters are the third and the last part of the Zoom ADC. The design specifications and selection of the filters are shared in Chapter 3. The block diagram of the digital filters can be observed in Figure 4.30. As mentioned, the digital filter consists of two cascaded filters: the CIC decimation filter and the integrating FIR filter. The implementation details of these filters are given in the following subsections.

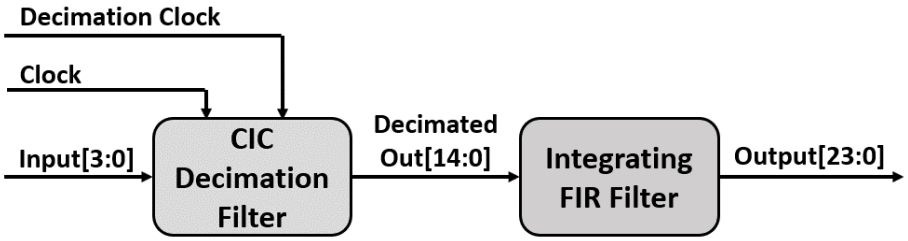

Figure 4.30: Block diagram of digital filters.

4.3.1 CIC Decimation Filter

The decimation filter is the first filter the modulated data processed. This design uses CIC decimation filter architecture with an integrator with reset modification. Figure 4.31. shows the block diagram of the CIC filter. The input data is 4-bit thermometer coded data, and the frequency of the data is the same as the Delta-Sigma modulators clock. Since the highest clock rate for the modulator is 7.5MHz, the timing requirement of the digital filter is relaxed. The decimation ratio is selected as 16; therefore, after decimation, a 500kHz decimation clock is used. The layouts of the individual blocks are shown in Figure 4.32, Figure 4.33, Figure 4.34, and Figure 4.35. The layout of the CIC filter is shown in Figure 4.36.

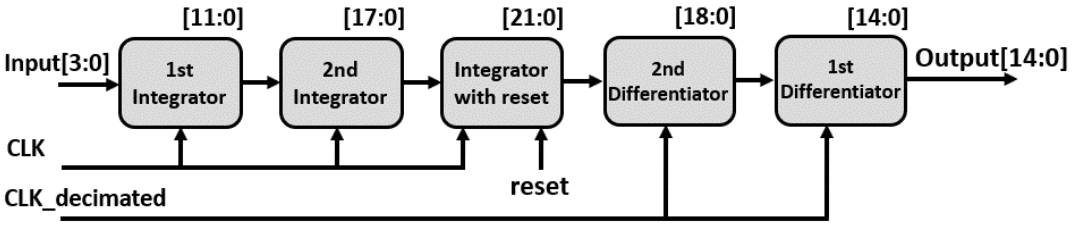

Figure 4.31: Block diagram of the CIC filter.

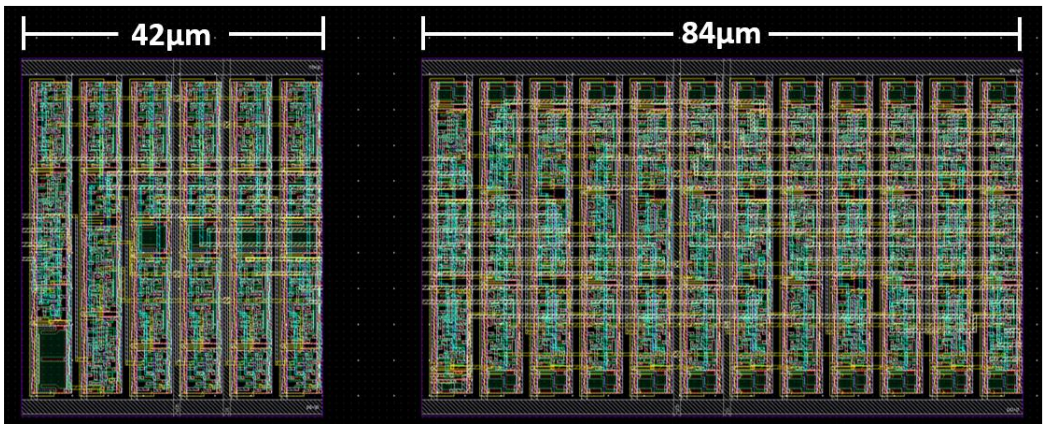

Figure 4.32: Layout of the 1st integrator (left) and 2nd integrator (right).

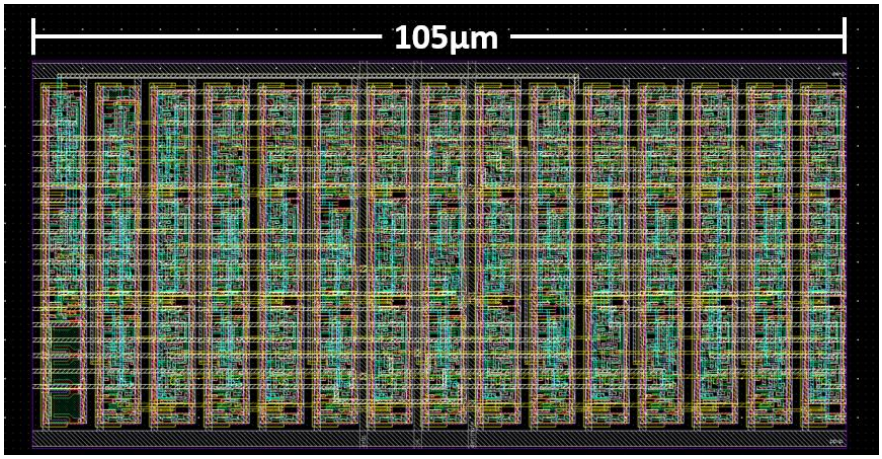

Figure 4.33: Layout of the integrator with reset.

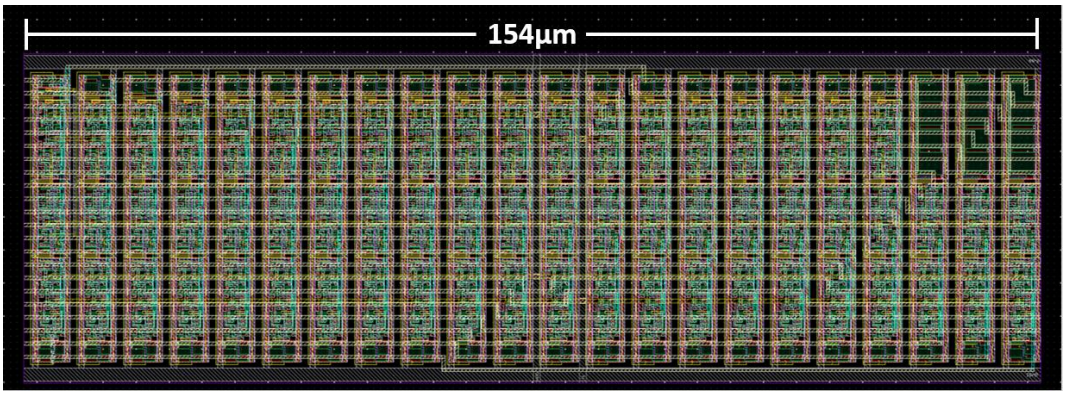

Figure 4.34: Layout of the 2nd differentiator.

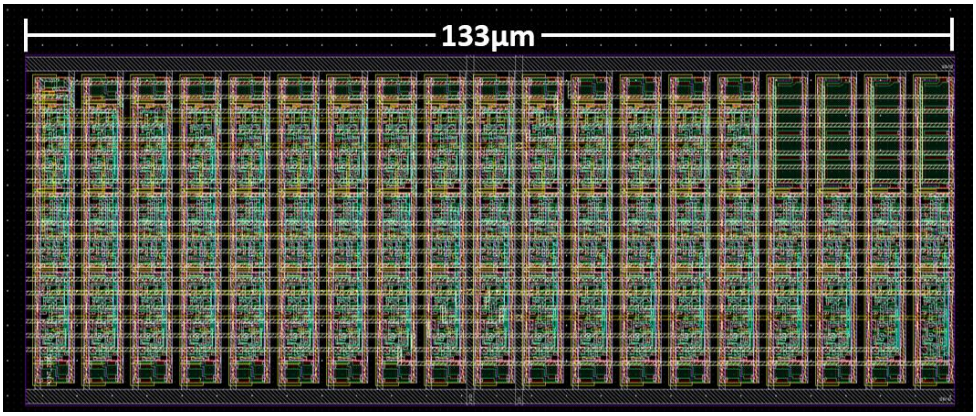

Figure 4.35: Layout of the 1st differentiator.

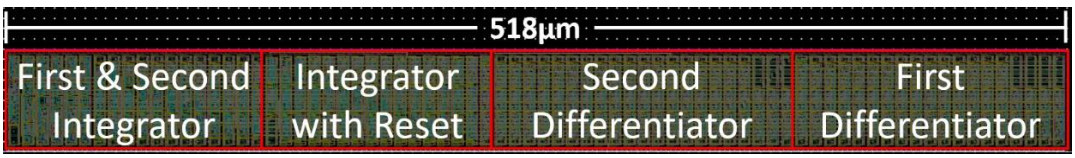

Figure 4.36: Layout of the CIC filter.

4.3.2 Integrating FIR Filter

The integrating filter is directly connected to the output of the CIC Decimation Filter. In this design, integrating FIR filter architecture is used. Figure 4.37 shows the block diagram of the integrating FIR filter. The input is 15-bit decimation filter output data, and the frequency of the data is the same as the decimation clock. For the ultrafast mode maximum frequency of the input data is 500kHz. For the coefficient calculation, the program clock has a higher frequency range up to 10MHz. The layout of the filter is shown in Figure 4.38.

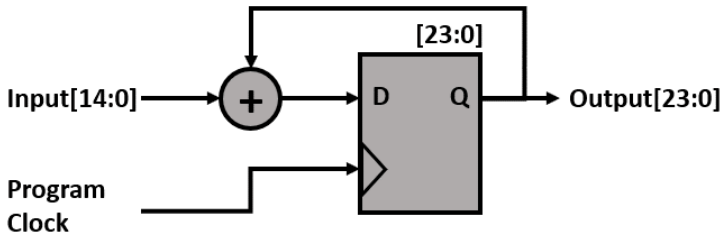

Figure 4.37: Block diagram of the integrating FIR filter.

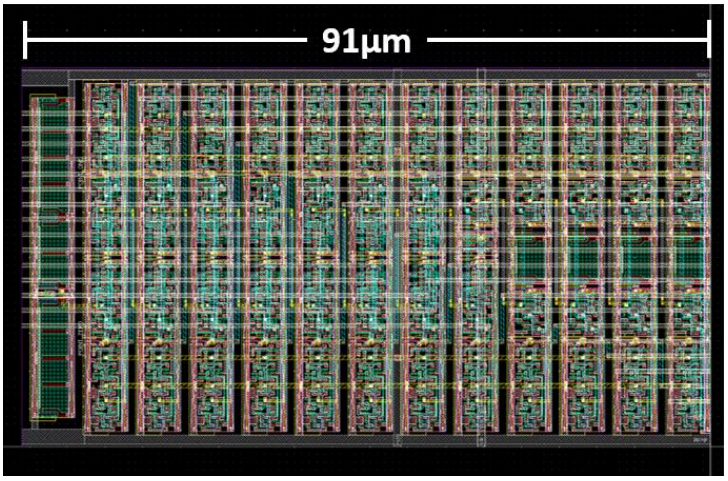

Figure 4.38: Layout of the integrating FIR filter.

4.4 Zoom ADC

In the previous sections, the design and implementation of the subblocks of the Zoom ADC are covered. This section shares the layout implementation and top-level verification of the Zoom ADC. In Figure 4.39, the top layout of the Zoom ADC is shared.

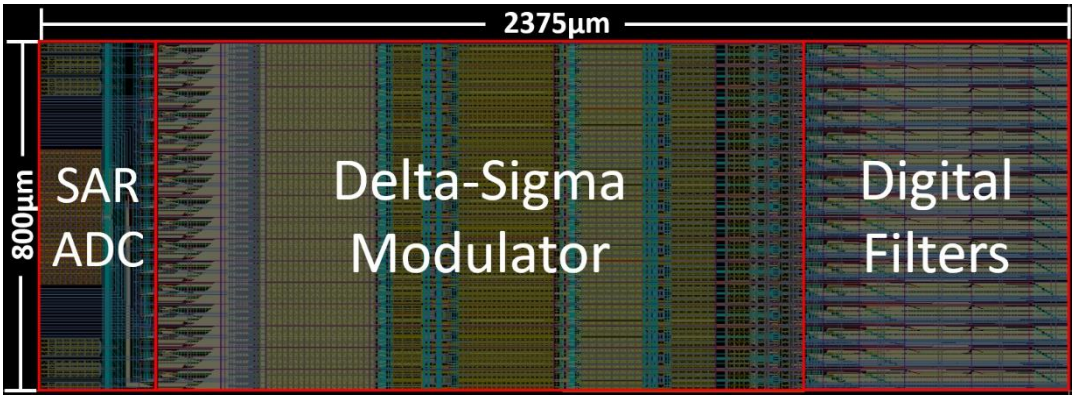

Figure 4.39: Layout of the Zoom ADC.

The top-level simulation of the Zoom ADC is very similar to the top-level simulation of the Delta-Sigma Modulator. One of the critical points in the simulation of the Zoom ADC is timing. Since SAR ADC and Delta-Sigma modulator operate in a pipelined timing, the proper timing diagram is crucial for the correct operation. The timing diagram of the Zoom ADC is shared in Figure 4.40.

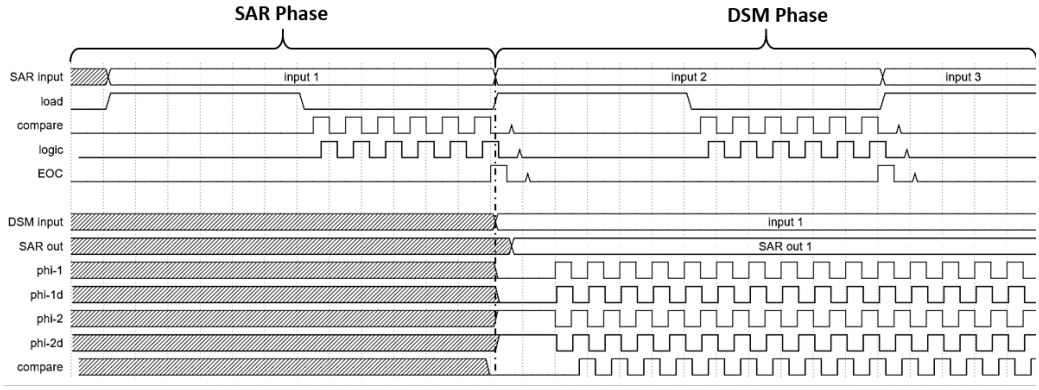

Figure 4.40: Timing Diagram of the Zoom ADC.

For the top-level simulation of Zoom ADC, similar to the Delta-Sigma Modulator, it is impossible to test full resolution with Cadence Analog Design Environment (ADE). The simulation voltage range is much more extensive than Delta-Sigma Modulator, and the required processing power is unnecessary. Thus, the full range simulations are performed in MATLAB and MATLAB Simulink. The block simulations are already performed, and their parameters are calculated in Cadence Analog Design Environment. These calculated data are ported to MATLAB for block-level verification. In Figure 4.44, the simulation result of the operation of Zoom ADC for 1.173V input is shared. In Figure 4.45. the MATLAB Simulink spectrum analysis of the modulator is shared with all noise sources placed, and the DEM algorithm is activated. Figure 4.29 shares the entire voltage range MATLAB simulation of the modulator. In this simulation, the input is swept between 0.25 V – 2.95V to observe the error plot of the modulator. For the error plot, the output of the digital filters is converted to analog signals by an ideal DAC and subtracted from the input voltage.

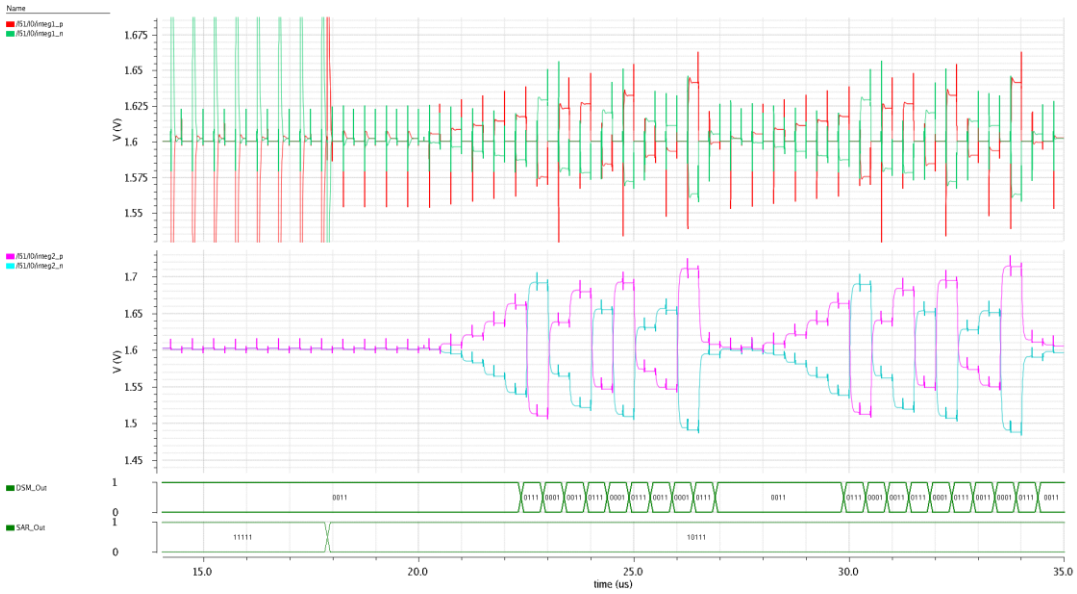

Figure 4.41: Transient plot of Zoom ADC for 1.173 V input.

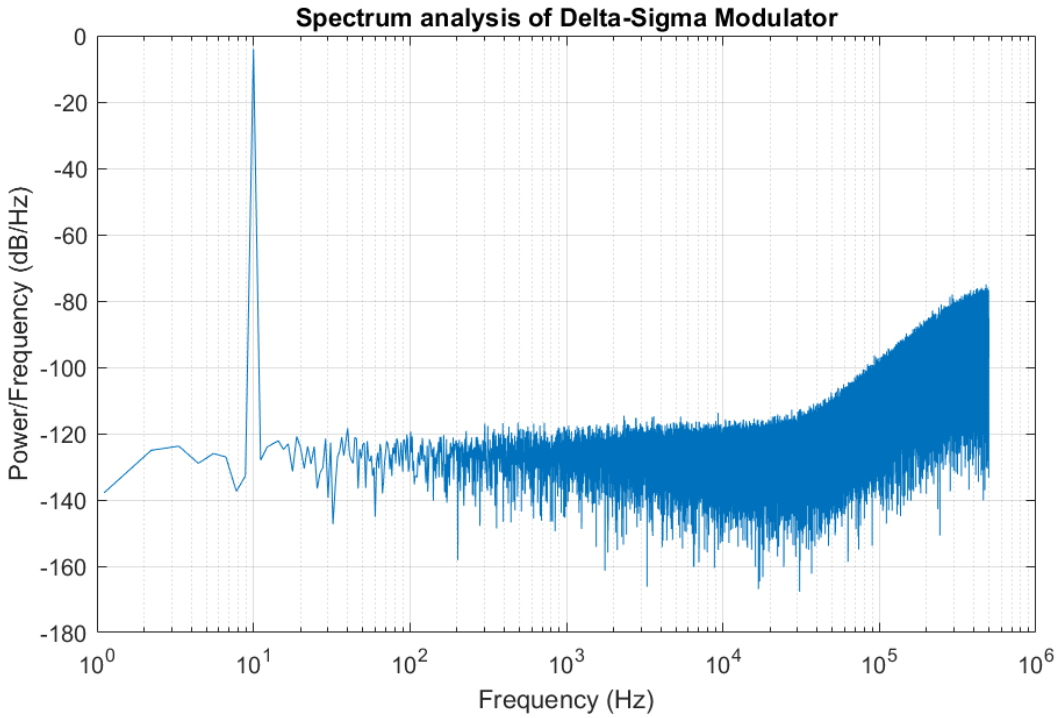

Figure 4.42: Spectrum analysis of the Zoom ADC.

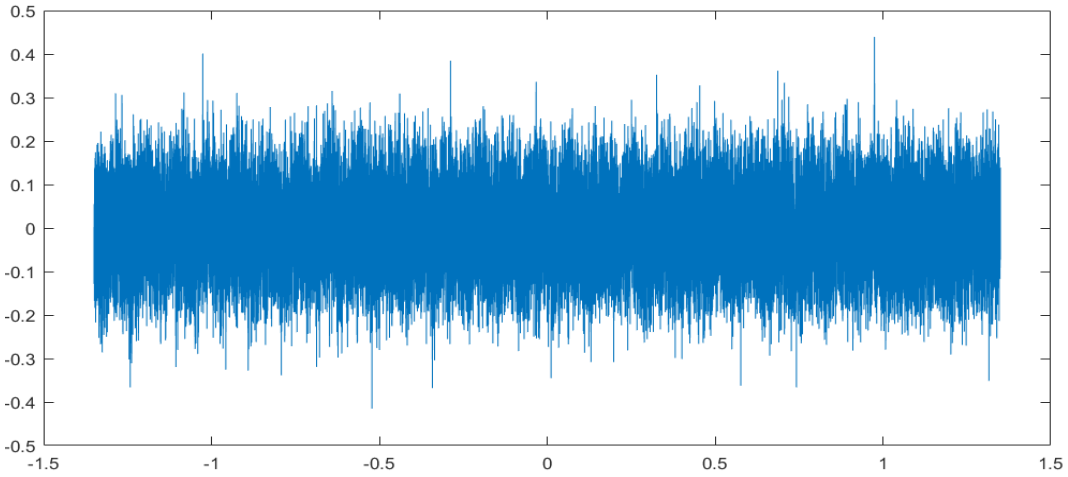

Figure 4.43: Error plot of the Zoom ADC.

In Figure 4.45. the SNR of the Zoom ADC can be measured as 119.5 dB. As observed from Figure 4.46, the Zoom ADC has an INL and DNL lower than 0.5 bit between the 0.25V – 2.95V range, which is sufficient for the operation. The designed Delta-Sigma Modulator consumes 358 µW power from the 3.3V supply.

4.5 Top-level Integration

In this work, the Zoom ADC is implemented on the microbolometer ROIC MT3825BA developed by Mikro-Tasarım A.Ş. [27]. As stated in Chapter 2, the Zoom ADC is cascaded between column readout and horizontal scanner. Since the digital controller [49] and bias generator [11] in the MT3825BA has a generic design and widely programmable array, these blocks are used with minor modifications. The top-level floor plan of the designed digital output microbolometer ROIC is shown in Figure 4.44. The ROIC has a 384x288 pixel array and two sets of (top and bottom) 200 column parallel Zoom ADC. The pixel pitch is 25µm, and due to the top and bottom ADC placement, the column width of the ADC is 50 µm. The total area of the designed Zoom ADC is 0.12mm^{2,} and the total area of the ROIC is 234.4 mm^2, where the width is 12.6 mm, and the height is 18.6 mm.

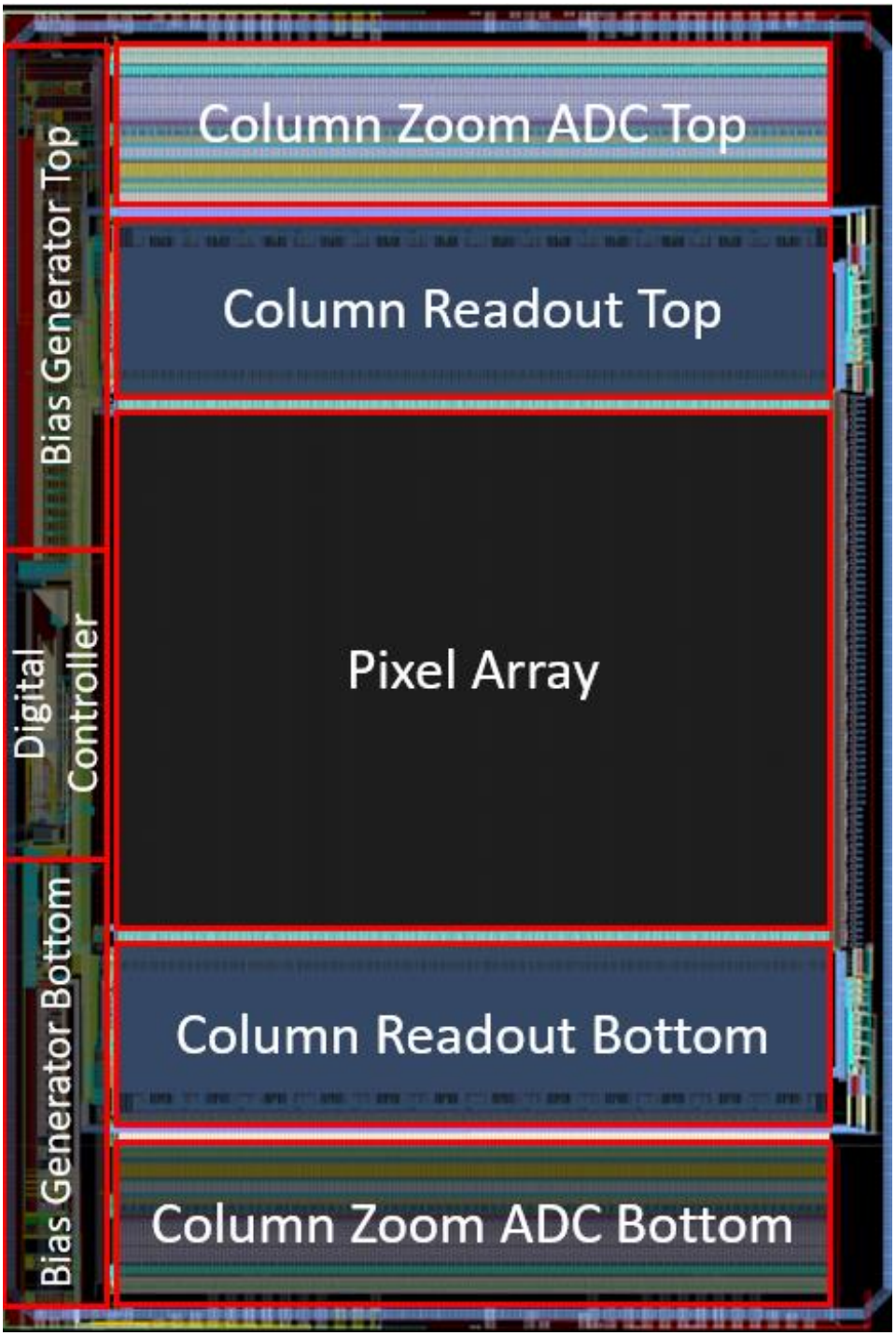

Figure 4.44: The top-level layout of the digital output microbolometer ROIC, which occupies 234.4 mm^2 area, where the width and height is 12.6x18.6 mm.

4.6 Summary and Literature Comparison

This thesis presents the design of a column parallel incremental Zoom ADC for microbolometer ROICs. This work makes it possible to digitalize the thermal radiation data without affecting non-uniformity between the active pixel and reference pixel. The high resolution and good linearity of this ADC enhance the imaging performance of the ROIC. The programmability of the architecture enables the use of ROIC with new generation detectors, which support high FPS thermal imaging.

The designed Zoom ADC can provide a 124.5 dB dynamic range with a 6 KS/sec sampling rate. The ADC provides a 28-bit digital output with 20-bit ENOB at the 20 FPS mode. The power consumption of the ADC is 358 μW for 20 FPS high-precision operation and 751 μW for 200 FPS ultrafast operation. The DNL of the system is below 0.5 LSB; thus, missing code is not expected. Table 4.1 provides the performance summary of the ADC with respect to operation modes.

Table 4.1: Performance summary of the Zoom ADC.

Technology	0.18 μm CMOS			
Area	0.12 mm^2			
Array Size	400 column (200 top, 200 bottom)			
Supply Voltage	3.3 V & 1.8 V			
Conversion Range	3.04 V - 0.16 V			
Modes	High Precision	Standard	Fast	Ultrafast
Frame Rate	20 FPS	30 FPS	50 FPS	200 FPS
Line Time	170 μsec	115 μsec	65 μsec	17 μsec
Sampling Rate	5.9 kS/sec	8.6 kS/sec	15.4 kS/sec	60 kS/sec
Power	358 μW	417 μW	539 μW	751 μW
Clock Frequency	2.5 MHz	3 MHz	4 MHz	7.5 MHz
OSR	425	320	256	128
INL	11.4 ppm	13.3 ppm	14.3 ppm	17.1 ppm
Dynamic Range	124.5 dB	118.4 dB	114 dB	99.2 dB
ENOB	20.05-bit	19.25-bit	18.55-bit	16.10-bit

Table 4.2 shows the comparison of the proposed ADC with the designs in the literature. For a fair comparison, mostly ADCs implemented for imaging applications are selected. The high-precision mode is selected for the ADC's performance summary since it is the primary mode for the digital ROIC.

Table 4.2: Comparison of the designed ADC with the literature.

	This Work	[50]	[51]	[52]	[53]
Architecture	Zoom ADC	Incremental ΔΣ ADC	4^{th} order ΔΣ ADC	Zoom ADC	ΔΣ + SAR ADC
Technology	180nm	110nm	350nm	160nm	180nm
Area	$0.12mm^2$	$0.0057mm^2$	$11.5mm^2$	$0.375mm^2$	$3.5mm^2$
Supply Voltage	3.3V & 1.8V	3.3V	-	1.8V	1.8V
Power Consumption	358 μW	475.6 μW	12.7 mW	6.3 μW	38 mW
Sampling Rate	6 KS/sec	32 MS/sec	2 KS/sec	25 S/sec	1 MS/sec
SNR	122 dB*	71.9 dB	-	119.8 dB	89.1 dB
DR	124.5 dB*	-	136.3 dB	119.8 dB	-
Schreier FoM	190.6 dB*	156.1 dB	185.3 dB	182.7 dB	160.3 dB

*Based on MATLAB Simulink simulation results

As observed from the table, there is a significant variation between the ADC architectures. Some of the ADCs have very low area and power consumption, but their SNR is low [50] or they have narrow bandwidth [32]. This is not suitable for high precision large array imaging applications. Some ADCs achieve higher than the required performance, but their power and area consumption is very large [51] [53], making them unfeasible for the intended design. Therefore, the designed ADC is a unique solution for the design of the digital output, high-resolution microbolometer ROIC. The on-chip implementation of the digital filters eliminates the need for high-end FPGA and decreases system cost. Moreover, this work introduces pipelined coarse and fine digitalization steps, which increase bandwidth and lower power consumption, which is distinctive for the designed Zoom ADC.

CHAPTER 5

MEASUREMENT SETUP

This design's characterization is crucial for further development of this work, and therefore the measurement setup must be carefully designed in order to detect and characterize any noise or error source after receiving the fabricated digital ROIC. This chapter provides detailed information about the test setup and test methods to be able to characterize the digital ROIC after its fabrication.

Figure 5.1 shows the block diagram of the measurement setup. The setup consists of a proximity card where ROIC is placed, FPGA Card. The proximity card has voltage regulators and other auxiliary circuits to keep ROIC operational and has connection ports for connecting ROIC to FPGA card, test DAC and Signal Generator. The FPGA card connects the ROIC to the Software for recording test measurements.

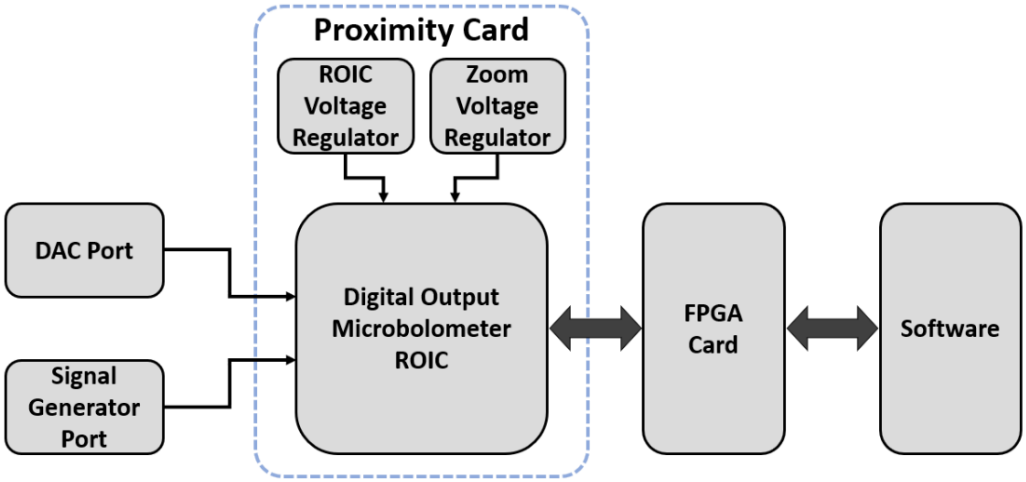

Figure 5.1: Block diagram of the measurement setup.

5.1 Measurements

Multiple performance parameters can define the performance of an ADC. Testing for these parameters requires different test setups and different measurements. Since the designed ADC is implemented on an ROIC, the test scenarios must be performed with extra caution to have minimum interaction with the ROIC. In this section, three main measurements are explained in detail.

5.1.1 Power Measurement

The first measurement is the power measurement. No signal sources are connected for the power measurement, and the ROIC is in power-off mode. The power connection of Zoom ADC is isolated from the chip to protect it from any noise interference with other blocks. This design selection increases the number of pads. However, for a new design, it is a reasonable design choice.

The ROIC is powered up at the start, and Zoom ADC is kept power off. When the ROIC is settled, the power consumption is measured. Then the Zoom ADC is activated, and the power consumption of the ADC is measured. Also, the total power consumption of the ROIC is measured to determine the effect of Zoom ADC on the Bias Generator of the ROIC.

5.1.2 Static Input Measurement

In the static input measurement, the DAC is connected to the test input of the Zoom ADC. The main aim of this test is to measure the ADC output deviation from the ideal output. For testing, the DAC generates a ramp signal, where the DAC output is updated every 64-conversion cycle. FPGA records the Zoom ADC output, and the ADC's DAC input vs. ADC output plot is measured. ADC converts the same DAC

output for 64 cycles due to measure noise effects on the ADC. There is a 20-bit performance expected from the ADC; thus, the resolution of the DAC must be much higher than the ADC. Generation of multiple data points for each bit is preferred since the measurement precision is increased.

The measured DAC input and ADC output plot are calculated, and the ADC output fits the ideal ADC output line using the best straight-line method [54]. This method can measure the INL, DNL, and offset of the tested ADC.

5.1.3 Dynamic measurement

In the dynamic measurement, the main aim is to measure the performance of the Delta-Sigma modulator. Since most of the precision is obtained by Delta-Sigma Modulator, the performance and linearity measurement is essential. Moreover, static input measurement is insufficient for determining error sources since digital filters can filter some of these sources. For this test, the signal generator is connected to the test input of the Delta-Sigma Modulator, and the modulator's output is directly connected to the test output port of the ROIC. SAR ADC and digital filters are deactivated in this test, and only Delta-Sigma Modulator is tested. At the start of the test, a sinusoidal input is applied to the input of the modulator, and the modulated output is recorded using FPGA for 8 seconds (2^{24} samples). The recorded data is processed to obtain spectrum analysis of the modulator. The spectrum analysis can calculate the dynamic range, SNR and SNDR of the Delta-Sigma Modulator and Zoom ADC.

5.2 Test Setup

The design and component selection for the test setup is crucial for the reliability of the measurements. Designing a test setup for high-precision ADCs is quite challenging since the effect of any additional noise source or interference would be significantly misleading.

In this thesis, the designed ADC is implemented on the MT3825BA, which is a commercially available ROIC. During the development of the ROIC, a high-precision testing setup is developed by Mikro-Tasarım A.Ş. In the development of the Zoom ADC testing setup, most of the blocks are inherited from the previous design. Some hardware and software are modified for the requirements of the Zoom ADC. The test setup can be investigated in two sections, hardware, and software.

5.2.1 Test Hardware

The test hardware consists of two PCBs, the proximity card and the FPGA board. The proximity board creates a connection to the ROIC and contains auxiliary blocks. The FPGA board contains an FPGA and serial communication ports for connection with a PC. The test stack can be observed in Figure 5.2.

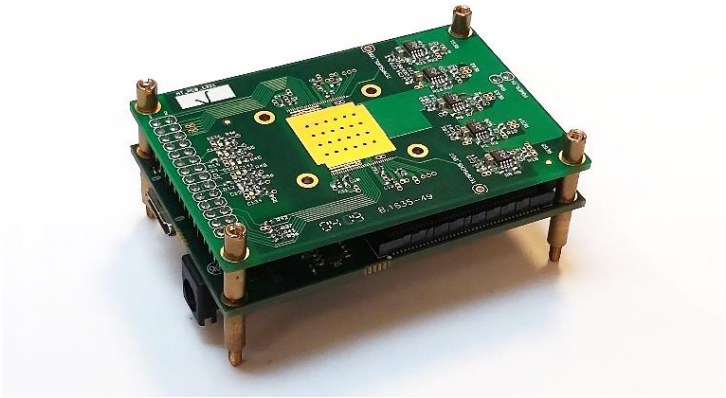

Figure 5.2: The test hardware. Proximity card on top and FPGA card on the bottom

5.2.1.1 Proximity card

The proximity card is a PCB designed to create the required power and signals for the ROIC and connect outside blocks with ROIC. For the initial design of the proximity card, MT3825BA's proximity card is used. Two ports are added for the signal generator and DAC. The pad frame is updated for the newly added ports. The proximity card is directly connected to the FPGA card, which shortens the signal path and minimizes noise injection due to the minimized routings and coupling.

The designed ROIC requires multiple power sources for digital power (1.8V) and analog power (3.3V). Also, in this design, the regulator of the Zoom ADC is separated to minimize noise coupling and power measurement. For generating required supply voltages, commercially available, low dropout regulators are used. The layout of the designed proximity card is shown in Figure 5.3

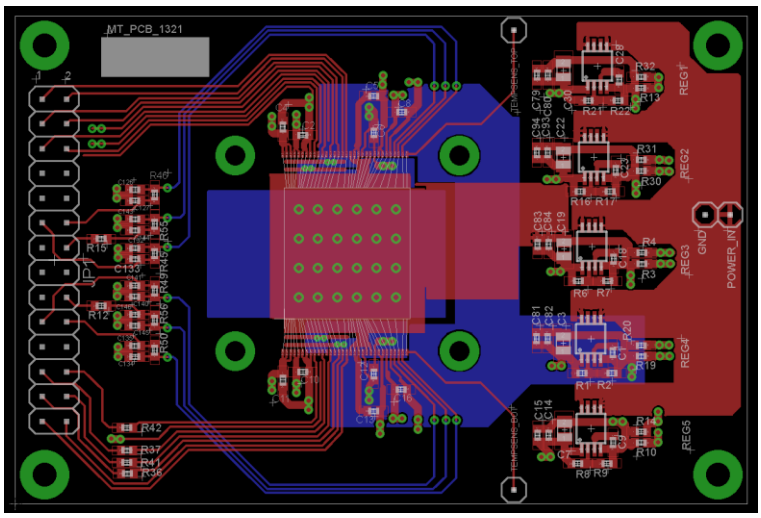

Figure 5.3: Layout of the proximity card.

5.2.1.2 FPGA board

The FPGA board is the general control unit for the imaging system. The FPGA generates the necessary timing signals, and the firmware regulates the communication between computer and ROIC. The FPGA development board, Opal Kelly XEM6310 FPGA board, is used for this application. This board provides a Spartan-6 FPGA, flash memory, oscillators, and serial communication ports. The FPGA board can be observed in Figure 5.4.

Figure 5.4: Opal Kelly XEM6310 FPGA Board. [55]

5.2.2 Test Software

Test software, written in C++ programming language, is mainly inherited from the standard microbolometer camera test software developed in Mikro-Tasarım A.Ş. For the testing of the ADC, new test modes are added to the software. DAC input sweep mode is implemented for the static input test, and the ADC output data is saved for each input. For the dynamic measurement, the input data train is directly saved to a text file for further processing in MATLAB. The user interface of the test software can be observed in Figure 5.5.

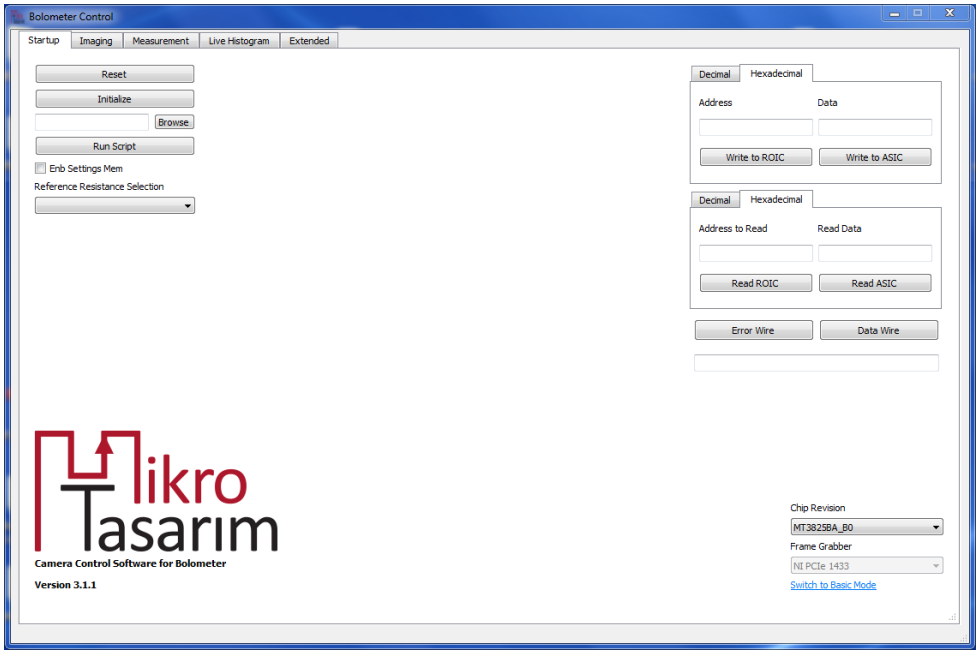

Figure 5.5: User interface of the test software.

CHAPTER 6

CONCLUSION AND FUTURE WORK

The main objective of this thesis is the development of a column parallel incremental Zoom ADC for uncooled imaging applications. The designed ADC is implemented on the MT3825BA resistive microbolometer ROIC, developed by Mikro-Tasarım A.Ş. Three main blocks are designed and implemented for the Zoom ADC development. The first block is 5-bit SAR ADC, the second block is a second-order Delta-Sigma Modulator, and the third is digital filters. The Zoom ADC is designed and implemented in 180nm CMOS technology. A series of tests verify the operation and performance of the designed ADC. To determine the stability and performance of the system, Z-domain analysis in MATLAB, transient model simulation in MATLAB Simulink, and top-level transient simulations with Verilog-A models in Cadence Analog Design Environment are performed. The operation of the subblocks is verified using transient simulation and noise simulation on Cadence Analog Design Environment. The performance parameters are defined using the data obtained from these testing series. The summary of the work carried on in this thesis can be summarized as follows:

1. The working principle of microbolometer detectors is briefly explained, and readout architectures are demonstrated.
2. Performance parameters of the ADCs are covered, and Different ADC architectures are investigated.
3. The top-level system is described, and requirements for the ADC are defined. For the column-parallel ADC, Incremental Zoom ADC architecture is selected. Operation modes of the Zoom ADC are introduced.

4. The general structure of the Zoom ADC is presented, and the theory of the Zoom ADC and its subblocks are explained in detail. Zoom ADC is a hybrid of a 5-bit SAR ADC and Delta-Sigma ADC. Zoom ADC provides high precision analog to digital conversion with lower power consumption than conventional Delta-Sigma ADCs.
5. The 5-bit SAR ADC defines the 5 MSB with minimum power consumption, and the Delta-Sigma ADC converts the LSBs from the residue voltage. This operation decreases the power consumed for the MSB conversion significantly. Moreover, the OSR of the modulator decreases, which decreases clock frequency and digital filter complexity.
6. The digital filter stage is designed for out-of-band noise cancellation and data parallelization. The digital filter consists of two cascaded filters: the CIC filter and the Integrating FIR filter. The design of filters is modified for optimal area consumption with proper operation.
7. The top-level design is implemented on MATLAB Simulink, and the stability and performance of the system are tested. Series of measurements performed for characterizing the effects of loop architectures, mismatch shaping DEM, digital filters, oversampling ratio, and other designs to system performance.
8. The analog performance of each block is verified individually. The gain of the amplifiers and noise levels are recorded. The obtained simulation data is combined with Simulink models, and a realistic model of the system is developed. The large-scale simulations are verification of the system are done using this method.
9. The power consumption of the system is measured as 358μW for high-precision operation. For the ultrafast mode, peak power consumption is measured as 751 μW. These power levels satisfy design specifications.
10. The linearity parameter DNL of the Zoom ADC is below 0.5 LSB for all operations.

11. The dynamic range of the ADC is 124.5 dB and SNR is 122 dB. The ENOB of the ADC is 20.05-bit.
12. The designed ADC covers a 0.12mm^2 area with 50µm x 2375µm dimensions for a single column. The designed digital output microbolometer ROIC covers 234.4 mm^2 silicon area.

The design and implementation of the Zoom ADC is an important step for realizing an ADC for high dynamic range, high FPS digital microbolometer ROIC. However, there is a series of planned improvements for increasing the performance of the ADC and imaging system. Planned work is detailed on the list below:

1. The noise shaping of the Delta-Sigma Modulator is not sufficient, thus requiring higher OSR. A higher order, more aggressive noise-shaping loop filter will be implemented to decrease OSR.
2. The digital filters cover a large silicon area, increasing the cost of the system. More area-efficient digital filters are investigated and implemented with more careful layout planning.
3. The system design is flexible. After verifying the operation of the ADC, the adjustable blocks will be removed to decrease power consumption and area consumption.

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