DESIGN AND FABRICATION OF PIEZOELECTRIC ENERGY HARVESTING MICRO DEVICES FOR BIOMEDICAL IMPLANTS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

AZİZ KOYUNCUOĞLU

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
MICRO AND NANOTECHNOLOGY

SEPTEMBER 2022

Approval of the thesis:

DESIGN AND FABRICATION OF PIEZOELECTRIC ENERGY HARVESTING MICRO DEVICES FOR BIOMEDICAL IMPLANTS

submitted by **AZİZ KOYUNCUOĞLU** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy** in **Micro and Nanotechnology**, **Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** ________________

Prof. Dr. Deniz Üner
Head of the Department, **Micro and Nanotechnology** ________________

Prof. Dr. Haluk Külah
Supervisor, **Micro and Nanotechnology, METU** ________________

Prof. Dr. Hanife Tuba Okutucu Özyurt
Co-Supervisor, **Energy Institute, ITU** ________________

Examining Committee Members:

Prof. Dr. Tayfun Akın
Electrical and Electronics Eng., METU ________________

Prof. Dr. Haluk Külah
Micro and Nanotechnology, METU ________________

Assoc. Prof. Dr. Kıvanç Azgın
Mechanical Eng., METU ________________

Assoc. Prof. Dr. Dinçer Gökçen
Electrical and Electronics Eng., Hacettepe University ________________

Asst. Prof. Dr. Erdinç Tatar
Electrical and Electronics Eng., Bilkent University ________________

Date: 05.09.2022

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Aziz Koyuncuoğlu

Signature :

ABSTRACT

DESIGN AND FABRICATION OF PIEZOELECTRIC ENERGY HARVESTING MICRO DEVICES FOR BIOMEDICAL IMPLANTS

Koyuncuoğlu, Aziz
Doctor of Philosophy, Micro and Nanotechnology
Supervisor: Prof. Dr. Haluk Külah
Co-Supervisor: Prof. Dr. Hanife Tuba Okutucu Özyurt

September 2022, 120 pages

Biomedical implants such as cochlear implants (CI) are called 'magical devices' by many, since they enable people in the silence to hear again, and just like every other engineering marvel, they need an energy source to create their wonders. Today's CIs are using batteries for this purpose but energy harvesting presents a favorable alternative. Among the different energy harvesting methods, piezoelectric materials are widely investigated due to their high power density and micro-integration possibilities. This study describes the design, fabrication, and experimental investigation of a piezoelectric energy harvesting micro chip suitable for next-generation fully implantable cochlear implant applications.

To provide the power requirements of the state-of-art fully implantable cochlear implants, bulk and thin film PZT based energy harvesting and transducer chips were designed, fabricated, and tested. The microfabrication process flow of the chips was optimized. Finite element modeling was used to design a novel double cantilever energy harvester. Vibration and acoustic test setups were used to analyze the performance of the fabricated devices. In the acoustic tests, 16.25 µW power was obtained at 120 dB sound input with the single cantilever chips. Compared with the

literature on similar microacoustic devices highest power density (1.5×10^{-3} W/cm^3) was obtained. With the new double cantilever design chips, vibration tests at 1 g input acceleration resulted in maximum power of 61 µW. For the purpose of cochlear implantation, a new figure of merit for the energy harvester chips was defined. The final energy harvester chip provided the highest normalized power density per chip mass (214.8 µW/(cm^3 *Hz * g^2* mg)) among similar studies.

Keywords: Piezoelectric Energy Harvesting, Fully Implantable Cochlear Implants, Acoustic Energy Harvesting, Bulk PZT, Pulsed Laser Deposited PZT

ÖZ

BİYOMEDİKAL İMPLANTLAR İÇİN PİEZOELEKTRİK ENERJİ TOPLAYICI MİKRO CİHAZLARIN TASARIMI VE ÜRETİMİ

Koyuncuoğlu, Aziz
Doktora, Mikro ve Nanoteknoloji
Tez Yöneticisi: Prof. Dr. Haluk Külah
Ortak Tez Yöneticisi: Prof. Dr. Hanife Tuba Okutucu Özyurt

Eylül 2022, 120 sayfa

Sessizliğe mahkum olmuş insanların tekrar duyabilmelerini sağlayabildiklerinden birçok kimse tarafından ‘sihirli cihazlar’ olarak adlandırılan koklear implantlar gibi biyomedikal implantlar, diğer tüm mühendislik harikaları gibi bu mucizeleri yaratabilmek için bir enerji kaynağına ihtiyaç duyarlar. Günümüz koklear implantları bu ihtiyacı karşılamak için pil kullanmaktalar, ancak enerji toplayıcılar da çekici bir alternatif oluşturmaktadır. Çeşitli enerji toplama yöntemleri içerisinde piezoelektrik malzemeler gerek yüksek güç yoğunluğu gerekse de mikro uygulamalara yatkınlıkları sebebiyle yaygın olarak araştırılmaktadır. Bu çalışmada yeni nesil tamamen implante koklear implant için kullanılabilecek piezoelektrik enerji toplayıcı cihazların tasarımı, üretimi ve deneysel incelenmesi açıklanmaktadır.

En yeni nesil tamamen implante koklear implantların enerji ihtiyaçlarını karşılayabilmek için yığın ve ince film PZT malzeme tabanlı enerji toplayıcı ve algılayıcı yongalar tasarlanıp, üretilip, test edilmiştir. Mikrofabrikasyon üretim akışları optimize edilmiştir. Sonlu elemanlar modellemesi yöntemi ile yeni bir tasarım olan çift kantileverli enerji toplayıcı konsepti oluşturulmuştur. Üretilen cihazların performansı titreşim ve akustik deney düzenekleri ile ölçülmüştür.

Akustik testlerinde, tekli kantilever tasarımlı yongalar ile 120 dB ses şiddeti altında 16.25 μW güç elde edilmiştir. Literatürde mevcut olan benzer mikro ölçekli akustik cihazlar içerisinde en yüksek güç yoğunluğuna ulaşılmıştır (1.5×10^{-3} W/cm^3). Yeni tasarlanan çift kantileverli yongaların titreşim testlerinde 1 g ivme altında en yüksek 61 μW güç elde edilmiştir. Koklear implant uygulamaları göz önüne alınarak enerji toplayıcı yongalar için yeni bir performans katsayısı önerilmiştir. Son üretilen enerji toplayıcı yonga, benzer çalışmalar ile karşılaştırıldığında yonga kütlesi başına düşen en yüksek normalize güç yoğunluğunu (214.8 μW/(cm^3 *Hz * g^2* mg)) elde etmiştir.

Anahtar Kelimeler: Piezoelektrik Enerji Harmanlama, Tamamen İmplante Koklear İmplant, Yığın PZT, Akustik Enerji Harmanlama, Darbeli Lazerle Biriktirmeli PZT

To my family, Cihan Nevam and the One and only Canım Hilalim

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisors Prof. Dr. Haluk Külah and Prof. Dr. Tuba Okutucu for their endless support and patience. They believed in me many times more than I do in myself.

I would like to thank the members of the jury, especially Prof. Dr. Tayfun Akın and Assoc. Prof. Dr. Kıvanç Azgın for their valuable suggestions during the thesis committee meetings. Many thanks to Assoc. Prof. Dr. Dinçer Gökçen and Asst. Prof. Dr. Erdinç Tatar for their time and discussions.

I would like to thank ALL the members of the BioMEMS research group, just to name a few Hatice, Levent, Yağmur, Bedirhan, Berat, Hasan, Salar, Ali Can, and all the others, thank you for the great lab, great friendship! I must also name my postdocs Özge, Dilek, Özlem and Aykan hocalarım. Their valuable contributions were larger than the scientific work we have done together. I am glad that I was able to work alongside METU-MEMS Cleanroom staff, representing them all thank you Orhan Akar. I thank Prof. Faruk Arinç and Tuğba Gün for the wonderful environment at the ICHMT Secretariat and Koc University n2STAR Cleanroom Team for their support during the last sprint of the journey.

Finally, I am thankful to my family, my dear wife, and my daughter for their infinitely large support. This thesis belongs to them.

The author was financially supported by TUBITAK BIDEB 2211-C 2013-2 Scholarship during this study.

This study was supported by FLAMENCO project receiving funding from the European Research Council (ERC) under the European Union Horizon 2020 research and innovation programme with grant agreement ID 682756.

TABLE OF CONTENTS

ABSTRACT v

ÖZ vii

ACKNOWLEDGMENTS x

TABLE OF CONTENTS xi

LIST OF TABLES xiv

LIST OF FIGURES xv

LIST OF ABBREVIATIONS xx

LIST OF SYMBOLS xxi

CHAPTERS

1 INTRODUCTION 1

1.1 Cochlear Implants 1

1.2 Piezoelectric Energy Harvesting 3

1.3 Objectives of the Study 6

1.4 Thesis Structure 7

2 BULK PZT BASED FABRICATION 9

2.1 Previous Studies with Bulk PZT 9

2.2 Bulk PZT Based Energy Harvester Fabrication Process 10

2.2.1 Bonding of PZT on Silicon Substrate 11

2.2.2 Bulk PZT Thinning 19

2.2.3 Parylene Insulation Layer and Metal Electrodes 27

2.2.4 Cantilever Formation 29

2.3 PZT Material Property Verification 32
2.3.1 Process Temperature Effect on PZT 32
2.3.2 Piezoelectric and Hysteresis Measurements with Ferroelectric Tester ... 33
2.4 Summary of Fabrication Processes 37
3 1ST GENERATION BULK PZT ENERGY HARVESTER 39
3.1 Unimorph Cantilever Design Vibration Tests 39
3.2 Modeling of Piezoelectric Harvesters 41
3.2.1 Modelling Constraints 42
3.2.2 COMSOL Modeling 42
3.2.3 Model Validation 43
3.3 Acoustic Energy Harvesting with PZT 44
3.4 Summary of the 1st generation device tests 50
4 2nd GENERATION ENERGY HARVESTER DESIGN AND VIBRATION EXPERIMENTS 53
4.1 New Generation Device Design 55
4.1.1 Cantilever Parameters 57
4.1.2 Calculation Results 58
4.1.3 Mask Set 61
4.1.4 Test Frames and Device Holder 62
4.1.5 Device Types 63
4.2 New generation device tests 64
4.3 Vacuum and Temperature Effects on Piezoelectric Harvester 70
5 THIN FILM PZT BASED FABRICATION 74
5.1 PZT patterning 76

5.2 Pt Etching 78

5.3 Thin film PZT Based Transducer Results 86

6 CONCLUSIONS AND RECOMMENDATIONS 89

6.1 Summary of Contributions 89

6.2 Recommendations for Future Work 90

REFERENCES 93

APPENDICES

A. Hybrid Piezoelectric-Pyroelectric Energy Harvesting 109

B. Piezoelectric Material Characterization with a Custom Sawyer-Tower Circuit 113

CURRICULUM VITAE 119

LIST OF TABLES

TABLES

Table 1.1 Common piezoelectric materials ... 6
Table 2.1 d_{33} coefficient measurement results for PZT 5A, 5H and PZNPT dies. . 35
Table 2.2 Different fabrication batches with the 1st generation design ... 37
Table 2.3 Fabrication process batches with the 2nd generation design masks. ... 38
Table 3.1 Summary of first-generation test results of the fabrication batches. ... 50
Table 3.2 Comparison with previous acoustic energy harvesters. ... 50
Table 4.1 PZT vs Si thickness values for optimum centroid location based on 5 µm thick bonding layer. White segment is the target area for the centroid to be along the bonding layer. ... 58
Table 4.2 1 g constant acceleration results of the designs with highest power output near target frequency. ... 59
Table 4.3 100 dB constant input sound pressure results of the designs with highest power output near target frequency. ... 60
Table 4.4 124 dB acceleration approximation ... 61
Table 4.5 Mask list ... 62
Table 4.6 Final device types included in the mask design. ... 64
Table 4.7 Comparison of the piezoelectric harvester literature. ... 69
Table 5.1 Parameters of thick photoresist lithography process on Pt coated test wafers. ... 81
Table 5.2 Comparison of wet chemical etching procedures used for Pt patterning with the present study. ... 87
Table 6.1 Device parameters ... 111
Table 6.2 Test results for different vibration frequency and temperature differences. ... 111

LIST OF FIGURES

FIGURES

Figure 1.1. Commercial cochlear implant system. 2
Figure 1.2. FLAMENCO concept, FICI system with piezoelectric energy harvester and transducers, low power circuits, and flexible connection to cochlear electrode. 3
Figure 1.3. Piezoelectric material configuration based on polar axis (3) and applied stress direction [28] 4
Figure 1.4. Basic bimorph piezoelectric energy harvesting cantilever in 31 mode [29]. 5
Figure 2.1. Developed fabrication flow for the bulk PZT based piezoelectric energy harvesters on SOI wafer. 11
Figure 2.2. In-Au binary phase diagram [48]. 13
Figure 2.3. Bonding of PZT dies using a shadow mask. 14
Figure 2.4. Wafer level bonding of indium-coated silicon dies (600 µm thick) on test wafer. 15
Figure 2.5. Stress-Elongation graph of the In-Au bonded silicon dies. 16
Figure 2.6. (Top) Overall view of PZT bonded wafer. Fractured In-Au bond interfaces after the shear test. (L) 12 MPa, (M) 15 MPa, (R) 20 MPa. 17
Figure 2.7. SEM image of bonded PZT on 600 µm SOI wafer. 18
Figure 2.8. SEM of bonding layers of broken PZT-Si interface. 18
Figure 2.9. (Left) Overall view of the test wafer with bonded PZTs. (Right) Reduced wetting of gold electrode surface using 3 µm Indium instead of 6 µm (~15 µm average). 19
Figure 2.10. In-Au bond interface between PZT top layer and silicon bottom substrate. 19
Figure 2.11. PZT surface after grinding. 21
Figure 2.12. PZT thickness measurements after grinding.. 21

Figure 2.13. Same surface before and after 35 minutes ultrasonic cleaning on SOI wafer. 22
Figure 2.14. Bonding interface on the bottom electrode where PZT is detached during ultrasonic cleaning. 22
Figure 2.15. Lapping system overall view (ENGIS FL20 [53])......23
Figure 2.16. Test wafer with four PZT chips.. 24
Figure 2.17. Vacuum chuck for lapping system with digital depth gauge 25
Figure 2.18. Lapping measurements results.. 25
Figure 2.19. PZT surface before lapping (left) and after (right).. 26
Figure 2.20. SOI wafer after the lapping step.. 26
Figure 2.21. Edge coverage on top electrode connection. 28
Figure 2.22. SEM photo of the PZT on wafer, after the parylene insulation layer and top electrode metal layer patterning. 29
Figure 2.23. SOI wafer after dicing. 30
Figure 2.24. Wafer thickness vs DRIE process time (Left). Back side view of the wafer with frames after DRIE process (Right). 30
Figure 2.25. New design chips released with back side DRIE process. 31
Figure 2.26. Test sample of bulk PZT on brass cantilever attached to a test PCB 32
Figure 2.27. Average measurement results of output voltage before and after heat treatment process (200 °C). 33
Figure 2.28. Piezo measurement equipment at AKU.. 34
Figure 2.29. Comparison of piezo materials at saturation electric fields 36
Figure 3.1. 1st generation design of the unimorph piezoelectric cantilever 39
Figure 3.2. PCB holder with the test chip attached on the shaker table. 40
Figure 3.3. Frequency sweep at 0.1g. 40
Figure 3.4. Maximum power output from the chip was 3.5 μW at 0.1g acceleration, 594.5Hz with 200kΩ load. 41
Figure 3.5. Meshing structure in the 3D validation model.. 43

Figure 3.6. (Left) Experimental result of the piezoelectric harvester chip (Right) Simulation results of the corresponding model with COMSOL. 44
Figure 3.7. Two-dimensional COMSOL model used for analyzing the cantilever 44
Figure 3.8. Parylene attachment fabrication flow.. 46
Figure 3.9. Parylene attachment layer with metal connection lines and copper spacer columns. 46
Figure 3.10. Schematic view of the acoustic test setup 47
Figure 3.11. Schematic view of the test sample.. 47
Figure 3.12. Actual view of the energy harvester chip on the vibrating membrane for acoustic experiments. 48
Figure 3.13. Measured frequency sweep results of the prototype chip. 49
Figure 3.14. Measured rectified power and voltage characteristics....................... 49
Figure 3.15. Piezoelectric Energy Harvester (PEH) chip attached on vibrating membrane at the end of ear canal model. 51
Figure 4.1. Basic vibration energy harvesting model.. 53
Figure 4.2. Umbo acceleration measurement with laser Doppler vibrometer and accelerometer (ADXL320). 54
Figure 4.3. Linear approximation of damping effect of added mass on the hearing mechanism. 55
Figure 4.4. Maximum stress point based on the analytical formulation is the fixed base of the silicon cantilever. 55
Figure 4.5. (Left) Stress distribution on the cantilever base (Right) Voltage distribution across the PZT layer. 56
Figure 4.6. The butterfly concept with two back-to-back cantilevers and a common PZT die over the anchor point. 56
Figure 4.7. (Left) Stress distribution on the cantilever base (Right) Voltage distribution across the PZT layer. 57
Figure 4.8 Comparison of unimorph and butterfly design output voltages under 1 g vibration. 57

Figure 4.9 Umbo displacement at 124 dB 61
Figure 4.10 Test frame with a larger outer section for electrical connections via pogo pins. 63
Figure 4.11 New test holder for piezoelectric energy harvesters and transducers with electrical connections via pogo pins. 63
Figure 4.12 (L)Single cantilever and (R) double cantilever (butterfly) harvester designs. 64
Figure 4.13 Resistance load sweep of single cantilever chip on shaker table. 65
Figure 4.14 Load sweep for maximum power output tests of butterfly chip.. 65
Figure 4.15 Output voltage of the same type chip from three different wafers. 66
Figure 4.16 SOI600-2-A-45-B1P chip results at 2765 Hz 1 g vibration. 67
Figure 4.17 Experimental vs. simulation results for the best butterfly chip........... 68
Figure 4.18. Experimental test setup with the compact vacuum chamber and probe connections. 71
Figure 4.19. Bulk PZT energy harvester power output at 3452 Hz (vacuum) and 3450 Hz (atmospheric) 72
Figure 4.20. Bulk PZT energy harvester power output at 776 Hz 1 g input. 73
Figure 5.1. Original FLAMENCO concept for energy harvester and transducer cantilevers. 75
Figure 5.2. The fabrication process of PLD-PZT structures 76
Figure 5.3. (Left) 400 nm PZT etching with an only acid solution. 77
Figure 5.4. 1μm PZT etching with a fresh etchant. 78
Figure 5.5. Thick resist layer (AZ9260) degradation in aqua regia solution. 82
Figure 5.6 Thick resist layer (SPR220-7) degradation in aqua regia solution. 83
Figure 5.7 (Left) AZ® 9260 and SPR™ 220-7 degradation in Aqua Regia solution after 15 minutes. (Right) Edge delamination on SPR™ 220-7 pattern. 84
Figure 5.8 SEM images of patterned Pt layers. 84
Figure 5.9 Pt etching with 40 min. hard baked SPR™ 220-7 85
Figure 5.10 SEM view of the thin film PLD-PZT layer with Pt bottom electrode . 86

Figure 6.1. Schematic and actual test setup. 110
Figure 6.2. Peak-to-peak voltage change with temperature difference................. 112
Figure 6.3. Sawyer-Tower circuit for polarization measurement of ferroelectric capacitor (FECAP).. 113
Figure 6.4. (Left) Schematic for the Sawyer-Tower circuit using two high voltage amplifiers. (Right) Custom die holder for polarization tests. 114
Figure 6.5. (Left) Sample ferroelectric hysteresis curve. (Right) Sawyer-Tower measurement results of PZT chip on SOI wafer. 115
Figure 6.6. Polarization hysteresis measurement with Radiant Ferroelectric....... 116
Figure 6.7. Comparison of hysteresis measurement with custom Sawyer-Tower circuit with different sensing capacitances 117
Figure 6.8. Comparison of hysteresis measurement with custom Sawyer-Tower circuit with different sensing capacitances 117
Figure 6.9. Polarization hysteresis measurement at different input electric field frequencies. 118

LIST OF ABBREVIATIONS

ABBREVIATIONS

BHF: Buffered Hydrofluoric Acid

CI: Cochlear Implant

DRIE: Deep Reactive Ion Etching

FEM: Finite Element Method

FICI: Fully Implantable Cochlear Implant

MEMS: Micro Electromechanical Systems

PECVD: Plasma Enhanced Chemical Vapor Deposition

PLD: Pulsed Laser Deposition

PZT: Lead Zirconate Titanate

RF: Radio Frequency

RMS: Root Mean Square

SOI: Silicon on Insulator

SPL: Sound Pressure Level

TLP: Transient Liquid Phase

LIST OF SYMBOLS

SYMBOLS

D: Electrical displacement

d_{31}: Piezoelectric strain coefficient in 31 axis.

d_{33}: Piezoelectric strain coefficient in 33 axis.

dB: Decibel

E: Electric field

ε: Permittivity

ρ: Density

S: Strain

s: Mechanical compliance

T_{cr}: Curie temperature

CHAPTER 1

INTRODUCTION

Artificial medical implants are used by many patients to eliminate certain disabilities. Implants such as pacemakers [1], [2], neurostimulators [3], and cochlear implants [4], [5] are widely used by patients worldwide. Even though the artificial implants can not completely replace their natural counterparts, they can improve the patients' quality of life enormously.

According to World Health Organization (WHO) by 2050, there will be 2.5 billion people with some degree of hearing loss and 700 million of those will require hearing rehabilitation [6]. Cases are categorized based on the amount of loss of sound pressure perception [7]. Compared to a healthy ear, 30-60 dB loss is called mild-to-moderate impairment, and 60-90 dB loss cases are categorized as severe-to-profound. While a simple ear plug-type hearing aid may be enough for mild hearing loss patients, profound loss cases would require a cochlear implant treatment.

1.1 Cochlear Implants

Cochlear implants (CI) are used by patients with profound sensorineural hearing loss to bypass the damaged ear organelles directly stimulating the auditory nerve. Figure 1.1 shows a commercially available cochlear implant system [8]. First cochlear implants were developed in the 1960s and later approved for adult patients by FDA in the mid-1980s. As of 2019 more than 736,000 implantations have been done worldwide [9]. However, present CIs have drawbacks such as high cost, frequent battery charging/replacement, sensitivity to external effects such as water, and aesthetic concerns by the patients [10]. Fully implantable cochlear implants (FICI) have the potential to eliminate most of these problems, but a reliable internal power source and an implantable acoustic sensor are the main bottlenecks [11].

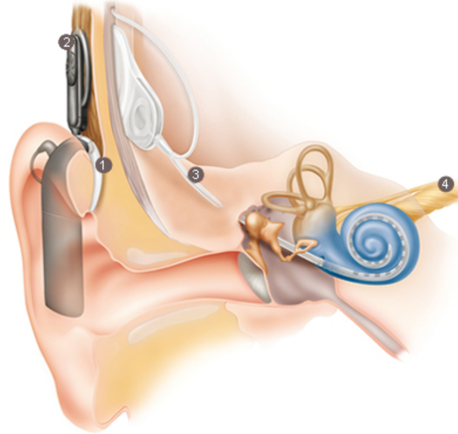


Figure 1.1. Commercial cochlear implant system. (1) External microphone and signal processor unit, (2) RF coil for signal and power transmission, (3) Internal electrical connection, (4) Cochlear electrode for nerve stimulation [8].

All the promising advantages of the FICI applications make the area a popular research topic. Most of the studies are concentrated on implantable sensor design for the implant [12], [13]. Calero et al reviewed the implantable sensors for FICI applications and suggested that the MEMS piezoelectric and capacitive sensors inside the middle ear are the most promising solutions for future implants [14].

Alternative energy sources for the implants were also investigated. Mercier et al studied endocochlear potential (EP) as a potential biological battery [15]. They were able to extract 1.2 nW of power and used it for periodic measurement of the EP and data transfer. Extracted power is not high enough to power up even the best state-of-the-art cochlear implant electronics which would require ~500 µW for neural stimulation [11], [16].

Accoto et al [17] stated that the incoming sound pressure of normal conversation level (60 dB) on the tympanic membrane does not carry enough acoustic energy to power the cochlear implant electrodes for nerve stimulation. They have suggested using a wearable electromagnetic energy harvesting using head movement as the kinetic energy source, but this solution would not be applicable to a FICI system.

Previously in our research group, a new concept was proposed combining both transducer and energy harvesting solutions in a single package along with the interface electronics. These studies have been done in the scope of FLAMENCO: “A Fully-Implantable MEMS-Based Autonomous Cochlear Implant” project, which is supported by European Research Council [18]. Due to the advantages over other energy harvesting methods such as high power density, piezoelectric material based solutions have been investigated. During the project, piezoelectric energy harvester [19], [20] and acoustic transducer chips have been fabricated [21], [22], low power integrated circuit designs have been developed [16], [23] and they have been tested in-ear models and actual animal trials [24]. Figure 1.2 shows the concept design of the proposed implant system.

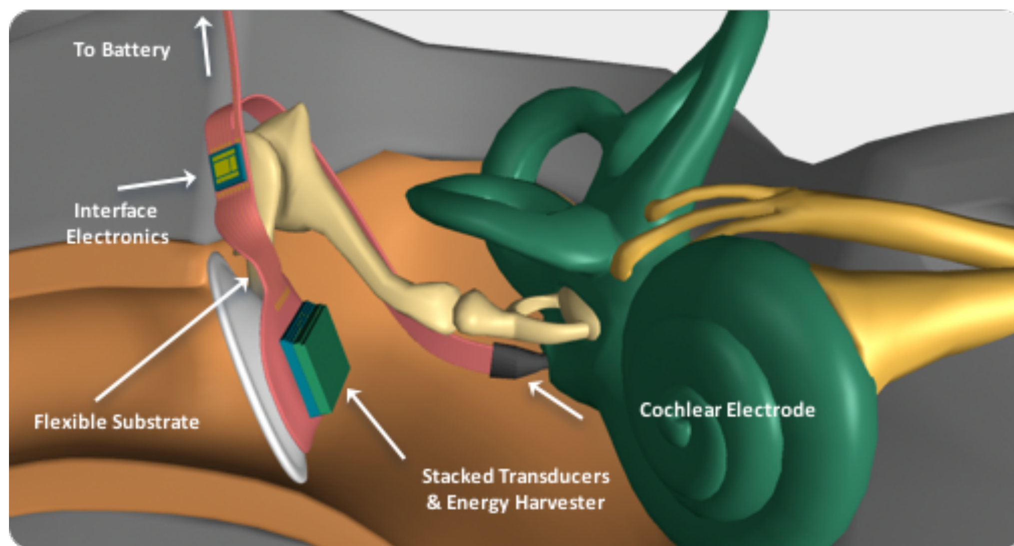


Figure 1.2. FLAMENCO concept, FICI system with piezoelectric energy harvester and transducers, low power circuits, and flexible connection to cochlear electrode [18].

1.2 Piezoelectric Energy Harvesting

The piezoelectric effect was first discovered by Jacques and Pierre Curie in 1889 on quartz crystals and the Rochelle salt [25]. Since then, many different materials were produced with even higher piezoelectric coefficients such as $BaTiO_3$ and PZT [26]. Piezoelectric materials have non-centrosymmetric crystal structures. Under external

stress, charge separation occurs in the polar axis of the material, which can be extracted as useful electrical energy. This is called the direct piezoelectric effect and is used mainly for sensor applications. The opposite case where the applied electrical voltage on the material induces strain is called the converse piezoelectric effect and it is utilized in actuator applications. The corresponding equations for the piezoelectric behavior in the strain-charge form are as follows.

Direct piezoelectric effect: $$\boldsymbol{D} = d\boldsymbol{T} + \varepsilon\boldsymbol{E} \quad (1)$$

Converse piezoelectric effect: $$\boldsymbol{S} = s\boldsymbol{T} + d\boldsymbol{E} \quad (2)$$

where $\boldsymbol{D}$ is electrical displacement, d is the piezoelectric coefficient, $\boldsymbol{T}$ is stress, ε is the permittivity of the material, $\boldsymbol{E}$ is the electric field, $\boldsymbol{S}$ is strain, and s is the mechanical compliance [27].

The operation mode of the piezoelectric structure is defined based on the polar axis of the material and the applied stress direction. Figure 1.3 shows the corresponding naming scheme with respect to the axis orientation [28]. The polar axis is the vertical z-direction (3). In 31 mode the applied stress is perpendicular to the electrode surfaces of the piezoelectric material, whereas in 33 mode stress and the voltage generation are in the same direction. Although the 33-mode generates higher voltages due to a higher piezoelectric coefficient, the implementation of 31-mode structures is easier. A simple cantilever bimorph piezoelectric structure in 31-mode is shown in Figure 1.4.

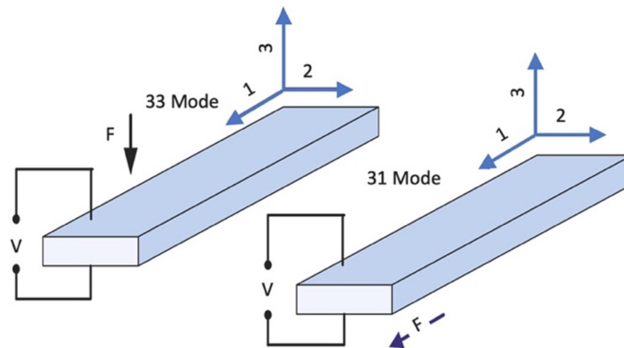


Figure 1.3. Piezoelectric material configuration based on polar axis (3) and applied stress direction [28]

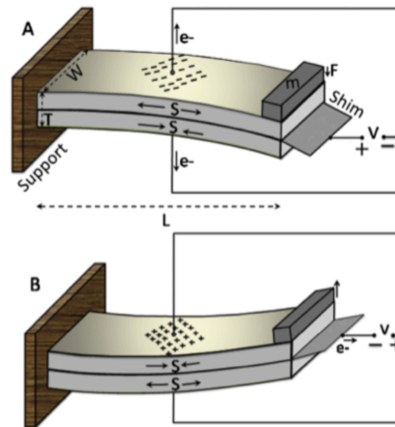


Figure 1.4. Basic bimorph piezoelectric energy harvesting cantilever in 31 mode [29].

For piezoelectric MEMS applications, various materials are used both in thin film and bulk forms. Table 1.1 shows the most commonly used piezoelectric materials and their basic properties.

For applications integrated with electronic circuits aluminum nitride (AlN) thin films are preferred due to their CMOS-compatible fabrication process [30]. It has a relatively low piezoelectric coefficient but its lead-free nature makes it also popular for biomedical applications [31]. Flexible polymeric or nanocomposite piezoelectric materials have also been studied for biomedical applications [32] for implantation on various organs, but the power generation is in the order of nanowatts, and nanoparticle-based materials survived for short testing periods only.

PZT is one of the most common materials used in bulk macro and micro applications due to its relatively high piezoelectric coefficients (d_{31} and d_{33}), high-power density. It has also very good pyroelectric properties which can be used to extract energy from temperature variations (Appendix A). It contains lead but it is also exempt from the Restriction of Hazardous Substances Directive (RoHS), therefore can be used in biomedical applications as well [33]. PZT 5H has the highest d_{31} value but the lower Curie temperature makes it difficult to integrate with the substrate using bonding processes with temperatures higher than 100 °C. Therefore, in this study,

PZT 5A is chosen as the piezoelectric material due to its high piezoelectric coefficient and the Curie temperature.

Table 1.1 Common piezoelectric materials

Material	$\rho\ (gr/cm^3)$	ϵ_r	d_{31} (pm/V)	d_{33} (pm/V)	T_{cr} (°C)
AlN [30]	3.26	9.2	-1.9-2.3	3.9	>2000
ZnO [34]	5.61	8.5	-5.4-7.0	13	-
PVDF [35]	1.78	13.5	-25	23	195
PZT-5H [36]	7.5	3800	-274	593	180
PZT-5A [36]	7.5	1800	-190	374	350

1.3 Objectives of the Study

The main aims of the thesis can be summarized as:

*Developing a high-yield piezoelectric energy harvester (PEH) fabrication process with bulk PZT for cochlear implant applications. The fabrication flow should include improved bonding and thinning processes that enable wafer-level processing of many chips at once.

*Fabrication of single cantilever energy harvester chips with the updated mask sets. Design of experimental setups for vibration and acoustic tests that will imitate the middle ear vibrations. Vibration and acoustic performance characterization of the fabricated chips.

*New PEH chip design and fabrication for higher performance using a novel double cantilever structure that can operate at ear canal resonance frequencies. The design

of the harvesters should consider the effect of the chips on the vibration of the natural middle ear structures.

*Alternative process development of acoustic transducers for cochlear implants based on thin film PLD-PZT. This alternative method should enable integrating at least 8 acoustic sensing channels into a single chip, hence decreasing the overall package mass.

1.4 Thesis Structure

The thesis consists of six chapters. After the introduction chapter, the development of bulk PZT based fabrication processes is explained in the second chapter. Next, Chapter 3 describes the experimental evaluation of first-generation energy harvesters and computer model development based on experimental results. Chapter 4 covers the details of the design methodology and experimental results of the second-generation PZT energy harvester for cochlear implants which is based on a novel double cantilever structure. The fifth chapter describes an alternative fabrication method based on thin film PLD-PZT which would be utilized for the acoustic transducer chips. The final chapter includes conclusions and suggestions for future work.

CHAPTER 2

BULK PZT BASED FABRICATION

2.1 Previous Studies with Bulk PZT

Since its invention in 1954, Lead Zirconate Titanate (PZT) has become the most commonly used piezoelectric ceramic material [26]. It has been developed into many variations for specific applications such as ultrasound generators [37], inkjet printer heads [38], and structural health monitoring sensors [39]. In the last two decades, PZT has also been used in micro energy harvesting studies mainly for powering wireless sensor networks [40].

Aktakka et al [41] presented a wafer-level integration method of bulk PZTs on silicon wafers. They used a low temperature (<200 °C) InAu bonding and thinning process to obtain high quality PZT films for harvester [42] and actuator [43] applications. Using a tungsten proof mass, they obtained over 200 μW power at 1.5 g input acceleration.

Durou et al [44] investigated bulk PZT based energy harvesters on an SOI wafer. They used laser-machined bulk PZT 5H to obtain 3.2 μW output at 0.1 g input acceleration. The PZT layer (200 μm) was not thinned but a large tungsten tip mass was used in order to keep the resonance frequency below 100 Hz. They showed that bulk PZT materials offer much higher performance compared with the thin film piezoelectric devices.

Janphuang et al [45] used a wafer-level bonding process for attaching the PZT 5H sheet on a silicon wafer using WaferBond® adhesive. The cantilever structures were obtained with silicon wet etching in KOH solution. The bonding solution requires a low-temperature process (<110 °C), but it is not electrically conductive, therefore a backside opening should be made, and the adhesive should be removed to access the

bottom electrode of the PZT layer. Moreover, no further patterning of the PZT layer was done, it covers all the surface of the individual cantilevers which were obtained with a dicing process. Using both silicon and nickel proof masses 82.4 μW was obtained at 1 g 99 Hz vibration.

In a previous study in our group, Beker et al [19] used a similar indium gold bonding and thinning process for PZT 5A based energy harvesters. Flip chip bonding method, successive thinning by grinding and final dicing steps limited the number of test devices. The resultant chip could produce 137.5 μW at 1.5 g input acceleration.

2.2 Bulk PZT Based Energy Harvester Fabrication Process

The microfabrication process with bulk PZT requires many considerations regarding both the fabrication flow and mask designs. All the processes in the fabrication flow should be lower than the Curie temperature of the piezoelectric material. As the temperature is getting closer to Curie point, domain disorientation will initialize and the polarization of the piezoelectric layer will begin to decrease [46]. Over the Curie limit, the material becomes paraelectric. Therefore, to protect the polarization of the piezoelectric layer, attaching the bulk PZT to the substrate surface, which is the highest temperature step in the fabrication flow, should be done using a low-temperature bonding process.

For low-frequency applications (<5 kHz) the bulk PZT sheet thickness would be inappropriate since at MEMS scale chips resonance frequency of the device would be too high. In order to decrease the material thickness, the PZT layer should be thinned down physically.

The proposed fabrication flow of the resonant piezoelectric energy harvesters is shown in Figure 2.1. SOI wafers have been used as the substrate to control the final cantilever dimensions accurately. The main challenging steps of the fabrication are the bonding and thinning of the PZT dies. For PZT-5A, which has a Curie temperature of 350 °C, the bonding temperature should not exceed 200 °C in order

to protect the polarization of the material. The thinning process should be both gentle enough not to break the brittle ceramic PZT material and precise enough to obtain the optimum thickness for the highest power generation from the piezoelectric layer. Several fabrication runs have been completed during the study, improving at each step.

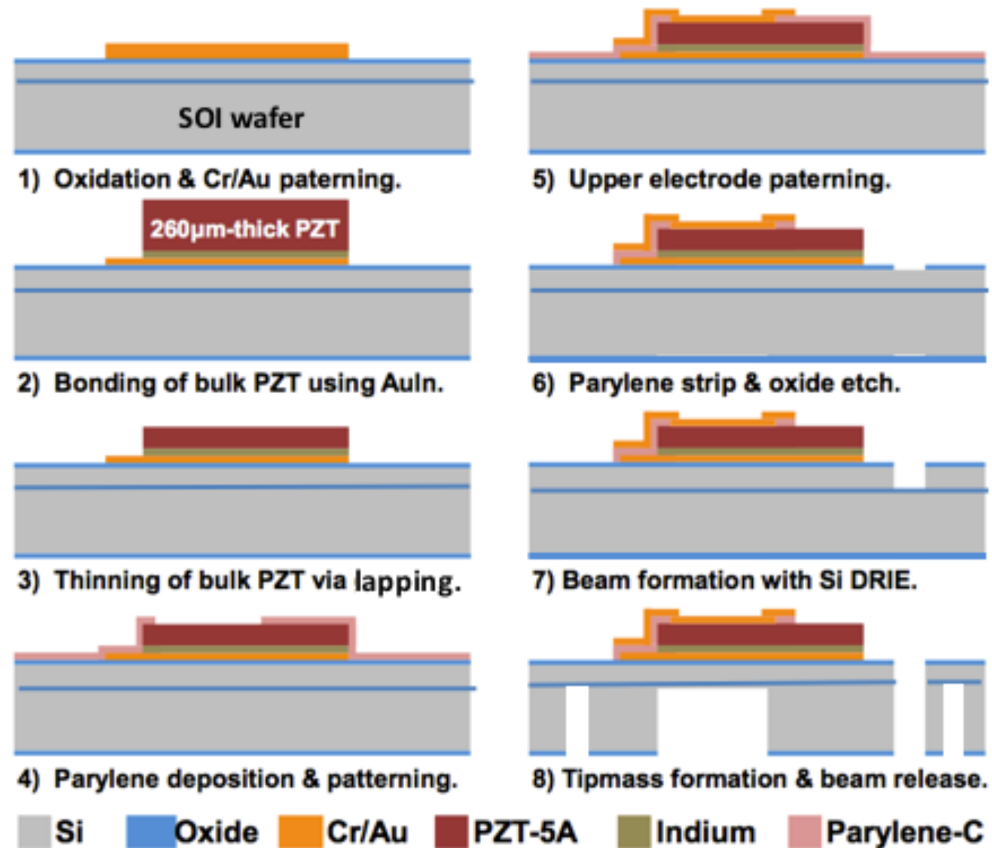


Figure 2.1. Developed fabrication flow for the bulk PZT based piezoelectric energy harvesters on SOI wafer.

2.2.1 Bonding of PZT on Silicon Substrate

In this study bulk PZT material is bonded to the silicon substrate using a low-temperature InAu bonding. For this purpose, PZT-5A sheets (7x7 cm^2 with 200 nm nickel electrodes on both sides) were used that are commercially available by Piezo.com, a division of Mide Technology [47]. The PZT material was utilized as

dies during the fabrication, therefore first parent metal layers were coated, then the sheets were diced with a Disco DAD323 Dicer machine.

2.2.1.1 PZT Preparation

For the indium bonding process, indium and parent gold layers should be deposited on one of the surfaces to be bonded. It can be done on the substrate wafer surface using a lift-off mask, but every wafer would require a deposition step. Since our access to the indium evaporator was limited, depositing the indium on the PZT surface before dicing, then using the dies on several wafers was more advantageous. Therefore, in this study, all the indium deposition processes were done on the PZT surfaces.

PZT sheets were cleaned with acetone and IPA after being received from the manufacturer. 50 nm chromium adhesion layer and gold layer (750 nm – 1.5 µm) have been sputtered on the PZT surface as the bottom parent metal layer of the InAu bond stack. An optional platinum diffusion barrier layer (100 nm) was also used in some of the samples between chromium and gold. In the next step indium layer (3-6 µm) as the bond layer and the thin gold layer (25-200 nm) as oxidation barrier were coated in a thermal evaporator. Initial In coatings were done at ASELSAN Cleanroom, later sets were coated in METU-MEMS. The PZT sheets were then coated with photoresist (S1805, 1500 rpm, ~1 µm) to prevent possible damage during dicing. PZT sheets were cut into rectangles with respect to the designed chip sizes. The protective photoresist layer was removed in acetone and the dies were dehydrated in oven (110 °C) right before the bonding process.

2.2.1.2 InAu TLP Bonding

In order to attach the PZT dies on silicon wafers In-Au transient liquid phase (TLP) bonding technique is used. Indium is a very soft metal with a melting point of 156°C. Indium and gold form a solid-state solution according to the phase diagram shown

in Figure 2.2. In the bonding process, once the temperature is above the melting point of indium, it transforms to a liquid phase and wet the gold surface. Since the melting point of the alloy is relatively high (>500 °C) the alloy begins to solidify at the same process temperature, hence the name of the process.

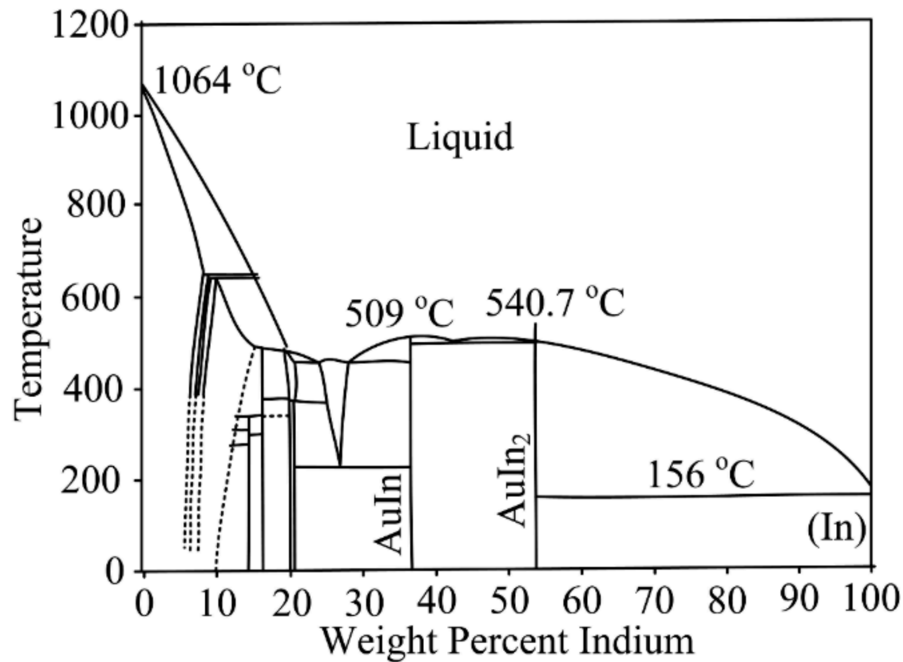


Figure 2.2. In-Au binary phase diagram [48].

Initial bonding trials were done using a SUSS FC150 flip-chip bonder using single PZT dies. 190°C chip temperature and 5 MPa bonding pressure were used for 30 minutes. At the first inspection, the chips seemed to be bonded successfully but during the thinning process, all the bonded PZT chips were broken and removed from the surface. Later examination of the wafers showed that the PZT chips were only partially bonded to the gold electrode surface. The flip-chip bonder device was re-calibrated to eliminate any non-parallelism problems. The bonding recipe was modified as 2000 s, 10 MPa, and 200°C for bonding time, pressure, and temperature respectively. Bonding conditions were compared and verified with the literature [49], [50]. Out of 40 chips bonded successfully only 4 survived the following

fabrication processes. Controlling the bonding quality in each chip separately proved to be difficult due to the device condition and alignment problems.

Instead of using the flip-chip bonder for processing each chip one by one, a wafer-level bonding procedure has been applied using the shadow mask as a guide for PZT die placement and the perform the bonding all at once in a wafer bonder device. Figure 2.3 shows the schematic of the bonding with the shadow mask process.

For the wafer-level bonding process of the PZT dies on the SOI wafer a silicon shadow mask with through holes is used. This mask was made by etching a wafer with DRIE using a SiO_2 layer on the front side as protection. Shadow mask alignment marks were designed considering the DRIE process and the following bonding alignment requirements (±20 µm). Oxide deposition and patterning were done in PECVD and BHF respectively. For DRIE patterning lithography SPR220-3 (3000rpm, ~4 µm) was used. The DRIE process has been done using the STS DRIE system. The total etching time was 1.5 hr.

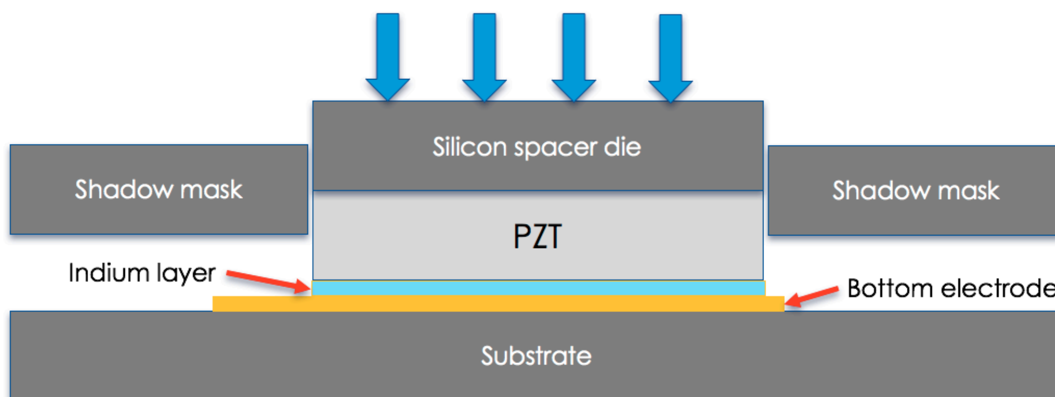


Figure 2.3. Bonding of PZT dies using a shadow mask. The shadow mask is aligned to the substrate wafer using a mask aligner. PZT and spacer dies then placed in manually.

First InAu wafer-level bonding with shadow mask was done using silicone dies for testing purposes. 3.2 µm indium coated silicone dies were placed in the shadow

mask and bonded using recipe 1 hr, 200°C, 2 MPa. Figure 2.4 shows the bonded wafer. All the chips were successfully bonded but some of the top edges were cracked while removing the shadow mask. This was due to the slight (<5 µm) size differences between the PZT and the silicon dies after the dicing process.

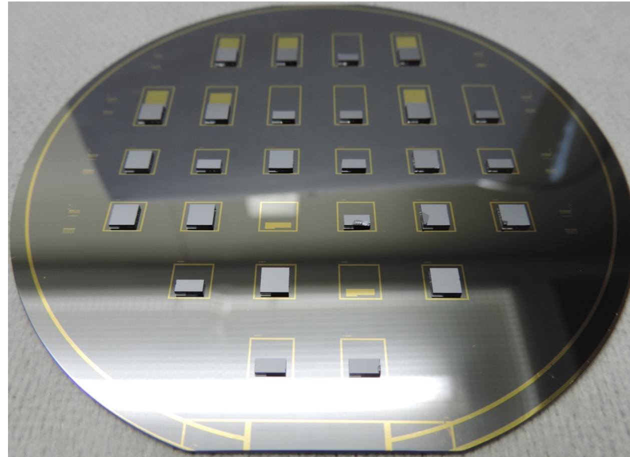


Figure 2.4. Wafer level bonding of indium-coated silicon dies (600 µm thick) on test wafer.

The shear strength of the bonding interface was tested with a shear tester. Figure 2.5 shows the stress-elongation results. Overall, the bonding strength was found to be quite good with average fracture stress around 35 MPa. This is a much larger value than the reported values in the literature such as 4.44 MPa by Aktakka [34]. Investigation of broken pieces revealed that the molten indium wetted the whole gold surface during bonding.

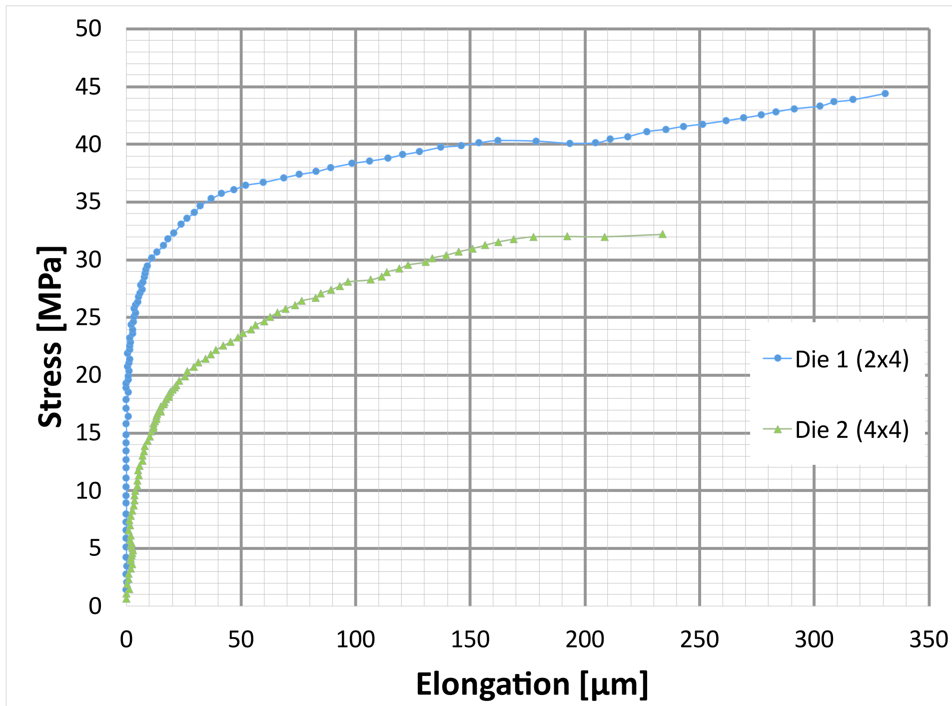


Figure 2.5. Stress-Elongation graph of the In-Au bonded silicon dies.

After the successful trials with the silicon dies, wafer-level bonding of PZT dies on silicon wafers was done. The PZT dies, which were In coated at METU-MEMS, were bonded on a test silicon wafer using the recipe 200°C bonding temperature, 5 MPa for 1,5 hours in vacuum. Three dies on the left column of the wafer were broken with a diamond cutter and tested in a shear strength test machine. The bonding strengths of the dies were 12, 15, and 20 MPa respectively. Figure 2.6 shows the overall wafer and fractured dies after shear tests.

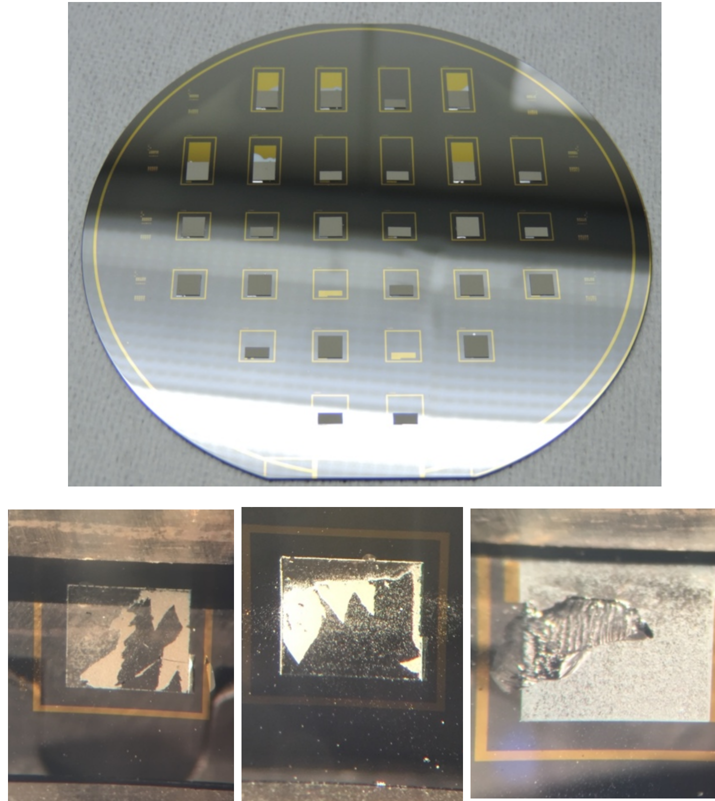


Figure 2.6. (Top) Overall view of PZT bonded wafer. Fractured In-Au bond interfaces after the shear test. (L) 12 MPa, (M) 15 MPa, (R) 20 MPa.

For the different types of mask designs, the bonding recipe was modified for the increased chip area to keep the bonding pressure at 5 MPa. Figure 2.7 shows the SEM views of the bond interfaces from the edges of the PZTs. Once melted excess indium is spilling on the bottom gold electrode surface. While the overall observation of the PZT edges showed complete bonding between the metal layers, breaking the PZT and close inspection of the interface showed the void between the In-Au layers as shown in Figure 2.8. To avoid void formation, thicker In layer coated PZTs are needed but too much indium would also create over-spilling.

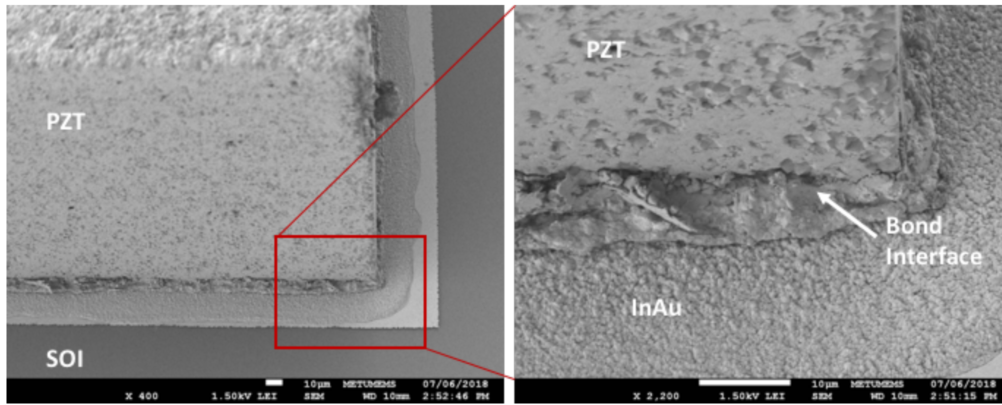


Figure 2.7. SEM image of bonded PZT on 600 µm SOI wafer.

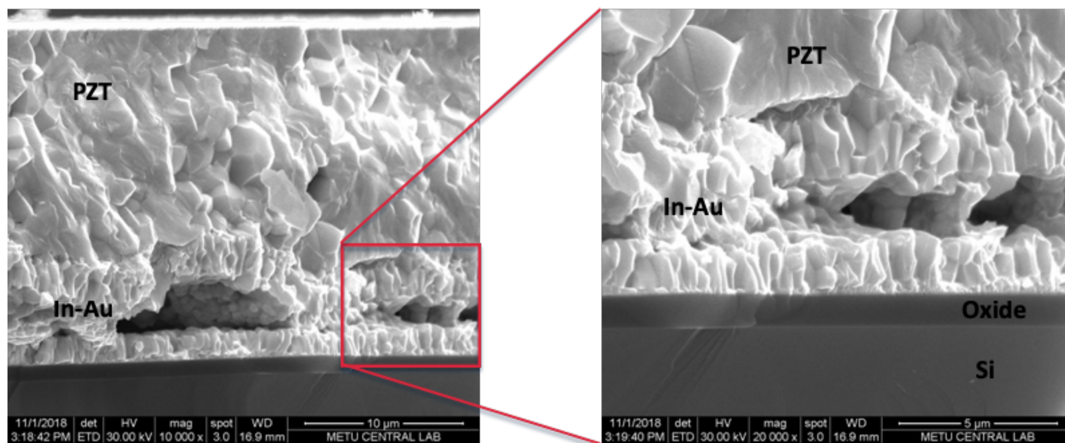


Figure 2.8. SEM of bonding layers of broken PZT-Si interface.

In order to prevent over-spilling and at the same time cover all the rough PZT surface (~2-3 µm peak roughness) 3 µm film thickness was chosen. 25 nm gold was coated as the oxidation protection layer in the same chamber as indium. Figure 2.9 shows the overall wafer and the wetting of the electrode surface with indium. The maximum bond layer thickness was 8.3 µm including the PZT roughness. The indium and gold layers are bonded well in most of the areas. Figure 2.10 shows the In-Au weight ratio at the gold layer on the wafer surface. ~20% indium was observed which shows that the indium layer is well dissolved into the parent gold layer (minimum required ratio 5%).

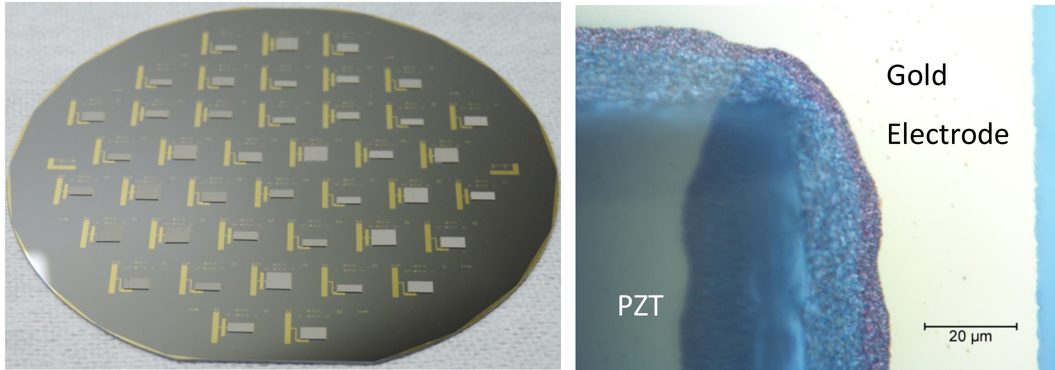


Figure 2.9. (Left) Overall view of the test wafer with bonded PZTs. All chips were successfully bonded. (Right) Reduced wetting of gold electrode surface using 3 µm Indium instead of 6 µm (~15 µm average).

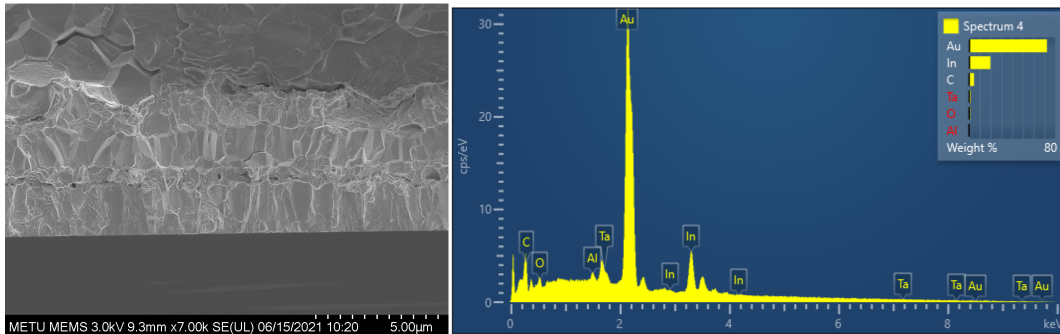


Figure 2.10. In-Au bond interface between PZT top layer and silicon bottom substrate. (Left) Complete bonding has been achieved at smooth PZT surfaces. (Right) Material distribution ratio on the bond interface. In weight ratio is 19.85%, Au 72.37%.

2.2.2 Bulk PZT Thinning

Since PZT ceramics are brittle materials, handling of small samples with thicknesses of <100 µm is quite challenging. The thinnest commercial bulk PZT sheet available is 127 µm [47]. In order to integrate them with vibrating microstructures with low resonance frequencies, either a heavy tip mass must be used [51] or the piezoelectric layer should be thinned down to comparable thickness values as substrate material [42]. Since there would be weight limitations for the FICI applications that will be explained in Chapter 4 in detail, large tip mass option is not applicable to this study. Instead, the bonded PZT layers are thinned down using grinding and lapping. Both

methods have certain advantages. The following sections explain the processing parameters and corresponding results.

2.2.2.1 Grinding

In the grinding process, material from the substrate surface was removed using an abrasive grinding wheel turning at high speed. High-precision flat surfaces can be obtained with <1.5 μm thickness accuracy [52]. For the PZT thinning processes a Disco DAG 810 grinder machine available at ASELSAN Cleanroom was used.

In the first trials grinding was completed for one wafer with four operational PZT chips of 260 μm original thickness. The average final thickness measured was 50 μm ± 2 μm. Most of the PZTs were broken during the process due to low-quality bonding. The process parameters were 4000 rpm wheel speed, 100 rpm chuck speed, and 0.1 μm/s feed rate.

After the wafer-level bonding process improvements, another set of wafers was thinned down using the same recipe. This time only a single chip out of 82 failed during the grinding process. While inspecting the samples under microscope small surface cracks on the edges of the PZTs were observed. Figure 2.11 shows the close-up view of such a PZT surface. Cracks are about 200 μm long and 5-10 μm deep. These cracks would impede the top electrode deposition and result in many of the chips being either short-circuited or broken during vibration experiments. After the grinding process thickness of each bonded and thinned PZT was measured on four corners. Figure 2.12 show the measurement results.

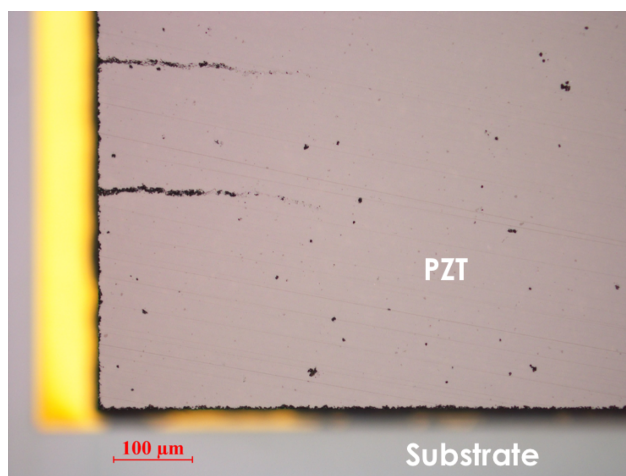


Figure 2.11. PZT surface after grinding. Small cracks on the edges are visible.

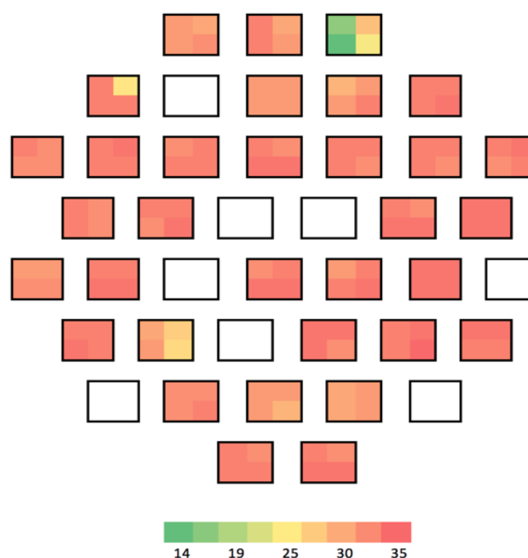


Figure 2.12. PZT thickness measurements after grinding. Target thickness was 25 µm. Average thickness 32.08 µm, average deviation per chip 1.49 µm. Empty squares represent broken chips.

One major problem with the grinding process was the contamination layer left on the wafer after PZT thinning in the grinder. The wafers were treated in an ultrasonic bath for cleaning after grinding but the contaminations were only slightly removed. Figure 2.13 shows the cleaning results for an SOI wafer. Moreover, PZT dies that

were partially bonded were broken during ultrasonic cleaning. Figure 2.14 shows one of the bonding interfaces of the detached dies. In future processes, a protective photoresist layer was coated on the wafer surface to clean the surface easily.

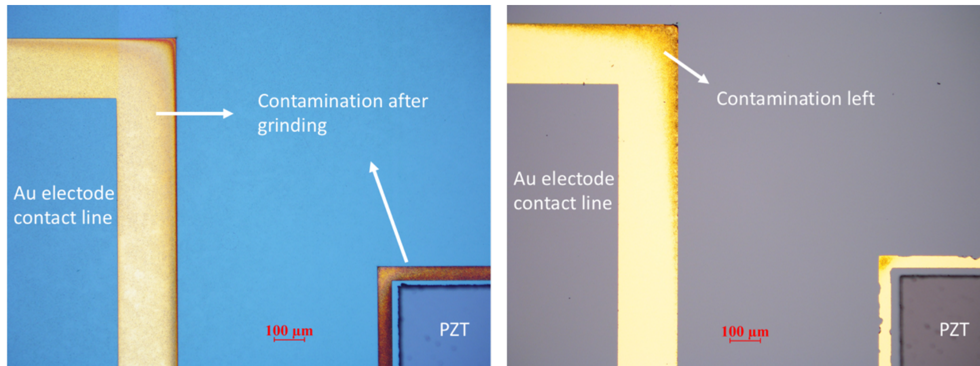


Figure 2.13. Same surface before and after 35 minutes ultrasonic cleaning on SOI wafer.

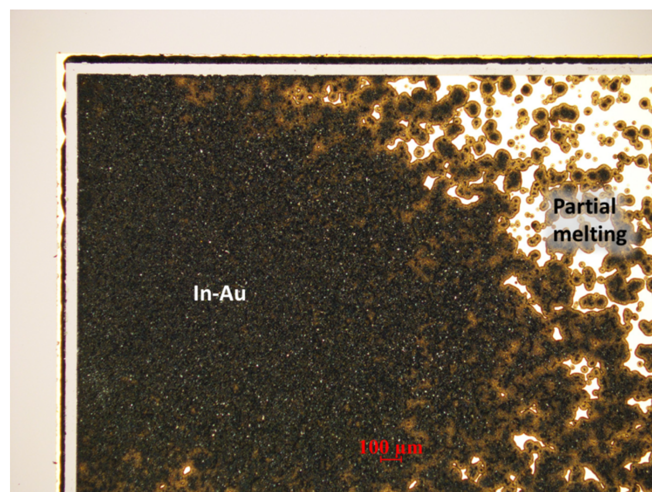


Figure 2.14. Bonding interface on the bottom electrode where PZT is detached during ultrasonic cleaning.

2.2.2.2 Lapping

As an alternative to grinding, PZT thinning was also done by a loose abrasive lapping process since the lapping process damages the ceramic PZT surface less. Figure 2.15 shows the lapping system (ENGIS FL-20) used for PEH fabrication installed in the METU-MEMS cleanroom.

In the lapping process, the diamond slurry is sprayed on the lapping wheel. The size and amount of diamond particles define the material removal rate. Another spray provides water-based lubricant on the wheel. To prevent damaging the sample and the lapping wheel the interface should always be wet during processing.

Wheel flatness should be checked before each process and corrected if there is a concave or convex error. Any convex or concave shape will result in the reverse shape on the sample surface.

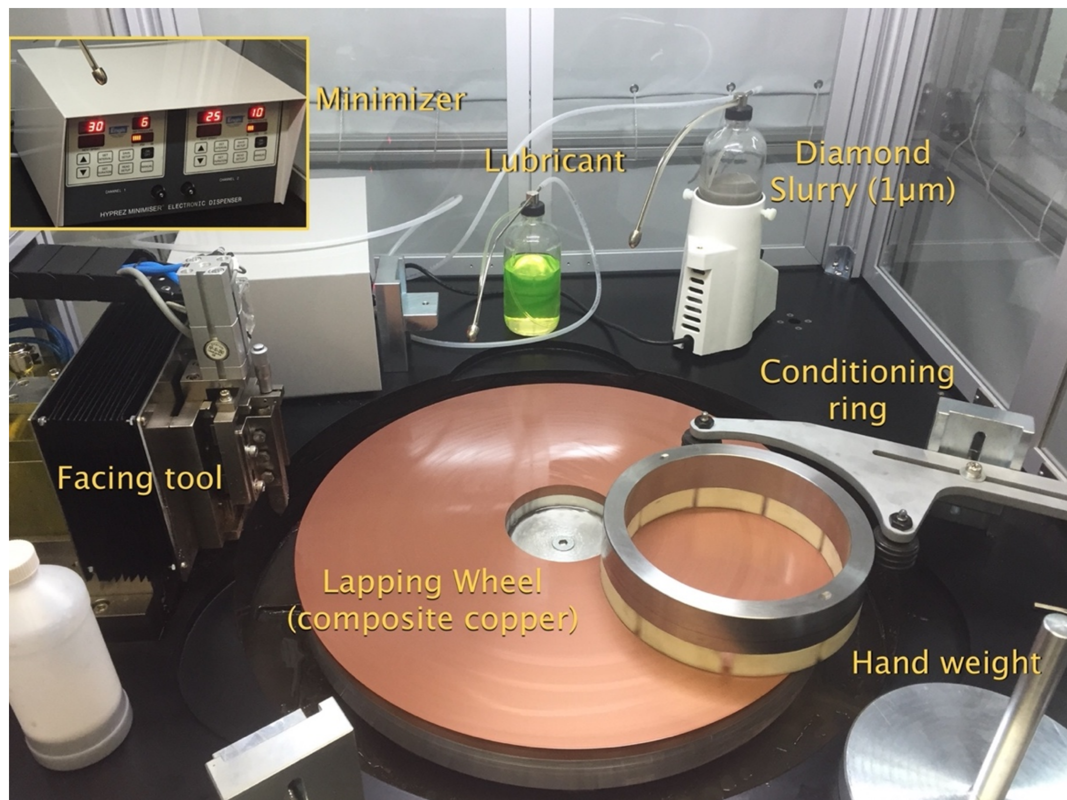


Figure 2.15. Lapping system overall view (ENGIS FL20 [53]).

Another important parameter is the flatness of the substrate holder. For the first batch a simple stainless steel, double-side flattened holder, was used. To attach the wafers, a strong wax available in our facility was used. Since the holder plate is contacting the lapping wheel only via PZT surfaces to be lapped, uniform distribution of the chips around the wafer is critical for final flatness. Moreover, the center of weight of the holder should align with the geometric center of the PZT contact points. In the first two wafers edge of the wafers was lapped before the PZT chips wore out as shown in Figure 2.16. The first-generation fabrication processes were completed with the stainless steel holder, with a minimum thickness deviation of ±8.5 µm. Further improvement could only be done with the optional vacuum chuck of the lapping machine that provides better wafer-level uniformity (Figure 2.17). The vacuum chuck was used for the second-generation design fabrications.

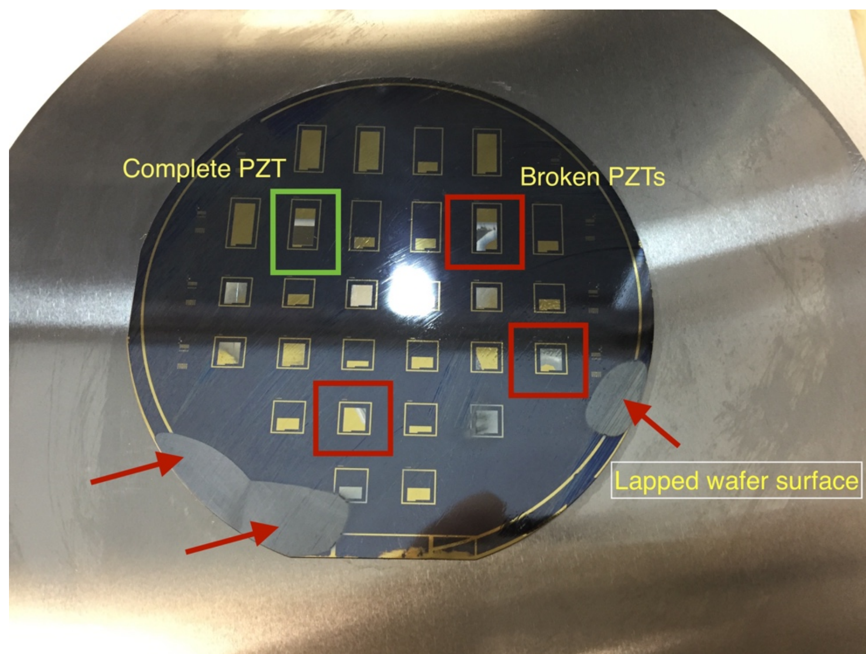


Figure 2.16. Test wafer with four PZT chips. Wafer edges were lapped due to tilted surface after PZT dies were broken.

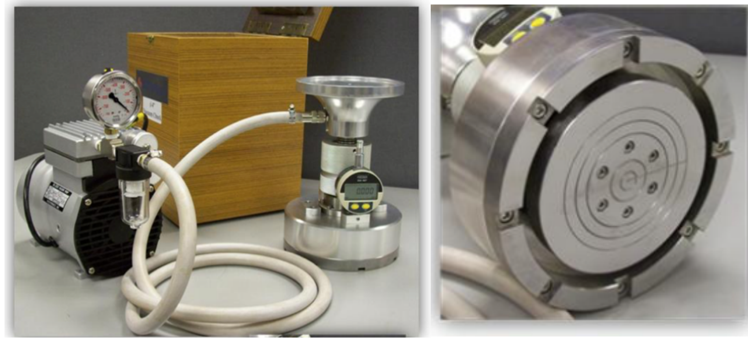


Figure 2.17. Vacuum chuck (up to 6”) for lapping system with digital depth gauge .

For the second generation fabrication process, PZT dies on SOI wafers were thinned down in a lapping system with 1 µm slurry using the vacuum chuck. 60 rpm wheel speed provided a 10 µm/min removal rate on average. The overall thickness distribution is shown in Figure 2.18. The lapping process provided a much better chip survival rate and better thickness control in the PZT thinning process. Figure 2.19 shows initial and lapped PZT surfaces under an optical microscope. The final minimum thickness deviation was ± 0.95 µm.

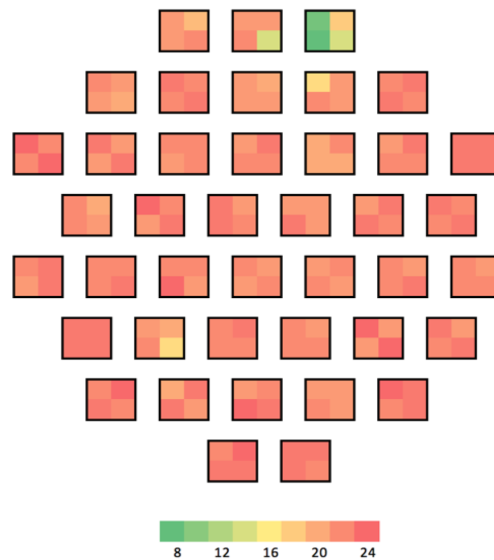


Figure 2.18. Lapping measurements results. Average thickness 21.66 µm, average deviation per chip 0.95 µm (In coating was done at MEMS).

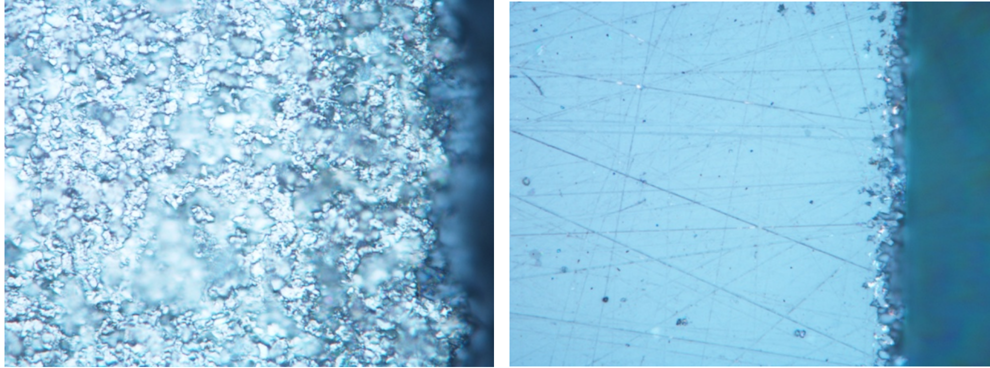


Figure 2.19. PZT surface before lapping (left) and after (right). The blurred areas in the unlapped surface are due to extreme surface roughness of the PZT (±2μm).

Similar to the grinding, one of the main problems with the lapping process was the residuals left on the wafer surface after the process. Once dried on the wafer it is extremely difficult removing the residual from the surface. Only mechanical scratching gets rid of them which may result in damaged microstructures. In order to prevent residue built up on the surface, wafers should be coated with a thick photoresist before the lapping process. Figure 2.20 shows the resultant wafer surface after the lapping process and following acetone cleaning of the photoresist. The photoresist layer protects the non-touching surface from scratching and slurry residuals. Since the photoresist layer is very soft compared with the wafer and lapping wheel, it is easily removed in the first few rotations and does not affect the lapping on the surfaces to be thinned down.

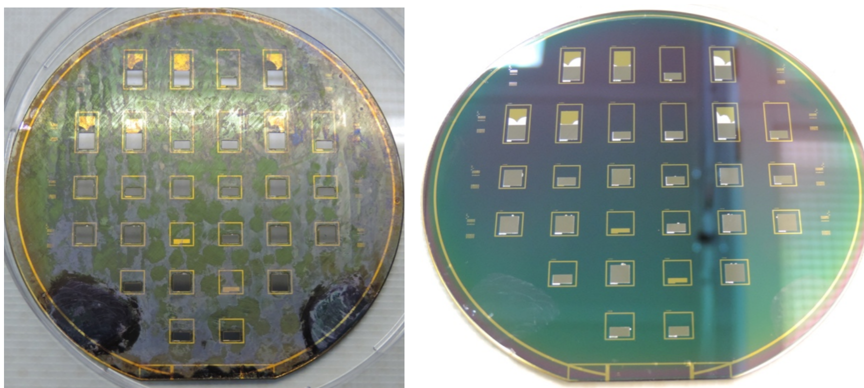


Figure 2.20. SOI wafer after the lapping step. (Left) before acetone cleaning, (Right) after acetone cleaning.

2.2.3 Parylene Insulation Layer and Metal Electrodes

Piezoelectric energy harvesters produce a voltage between two electrodes of the material. The piezoelectric material, in our case PZT, is highly dielectric but any routing or contact pads of the electrodes should also be isolated from each other. For this purpose generally an insulation layer was deposited on the piezoelectric device before the second electrode deposition. Different materials such as alumina [33], PDMS [32], or parylene [19], [54] were used for this purpose. In this study, parylene-C was chosen as the insulation layer due to its conformal coating characteristics and the high dielectric constant. The thickness of the layer (2-5 μm) was defined based on the dielectric breakdown voltage of parylene with respect to the voltage to be applied between the electrodes for characterization tests.

Patterning was done in two steps, first etching the openings on the PZT surfaces where the top electrode will be in contact, and secondly after the top electrode patterning removing the remaining parylene on the wafer surface. AZ9260 thick photoresist mask was used for RIE etching with O_2 and CH4-based recipe. Since the etch selectivity is low between photoresist and parylene, the masking resist layer should be at least twice the thickness of the parylene. CH_4 is used to accelerate the etching process in oxygen-rich plasma. Regular O_2 plasma system can also be used for parylene etching but it takes much longer to etch parylene than the RIE system. Etch rate was about 1 μm/hour during the trials with pure oxygen plasma. Also in such a case, due to long processing time, there would be severe undercutting of the insulation parylene layer under the top electrode metal layer.

Another alternative is using the ICP RIE system for the parylene etching using C_4F_8 instead of CF_4 used in the normal RIE system. Using argon and oxygen on a dummy 8” wafer with 1 μm parylene, the parylene layer was etched completely in only 50 seconds. The high speed is due to the high power of the ICP generator in the Metal RIE device.

For top electrodes, 30 nm Cr and 500 nm Au were sputtered on the patterned parylene layer. For patterning metal layer instead of thick photoresists, spray coating is used to cover the high PZT structures. Figure 2.21 shows an example device with good edge coverage after the top electrode metal etching.

Due to the high topology of bonded PZT dies extra exposure and development stages may be needed to remove the remaining photoresist on the PZT edges. If not removed properly, the metal residual at the bottom of the edge may cause short-circuiting between the top and bottom electrodes. Figure 2.22 shows an SEM view of a cleaned top electrode layer and parylene insulation layer structure.

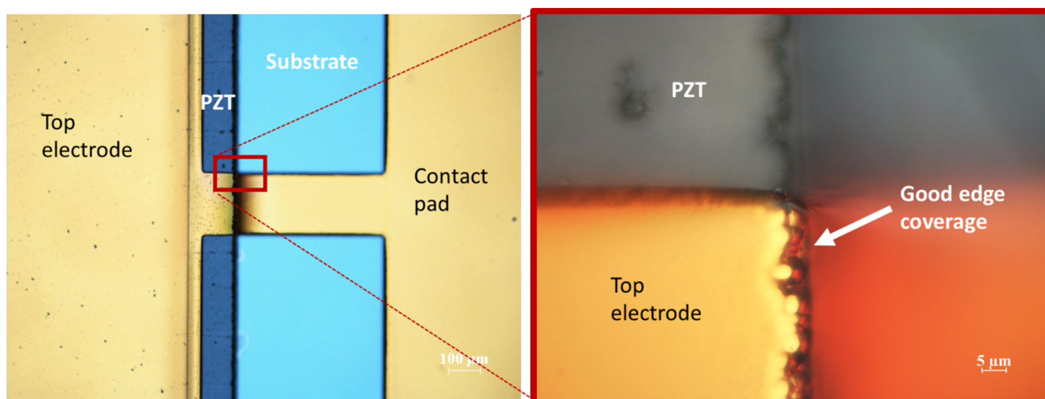


Figure 2.21. Edge coverage on top electrode connection.

After the top electrode patterning and removal of the remaining parylene layer, short circuit tests were done to identify any cracked PZT. In extreme cases when most of the wafer was not usable due to shorting, the top electrode layer can be removed, and insulation and new top electrode layers can be reprocessed.

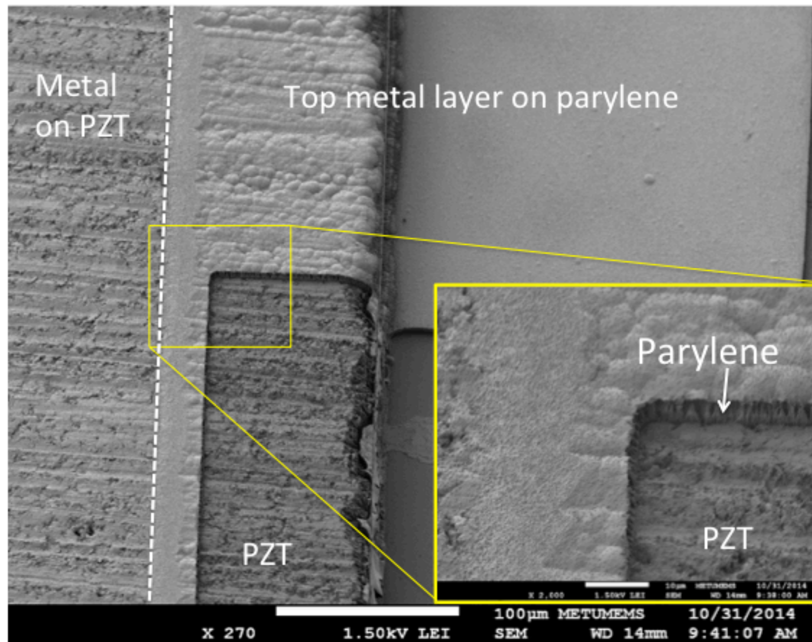


Figure 2.22. SEM photo of the PZT on wafer, after the parylene insulation layer and top electrode metal layer patterning.

2.2.4 Cantilever Formation

The cantilever structures of the energy harvesters are formed using the DRIE process from the front and back sides of the substrate wafers. Front-side etching depth defines the cantilever thickness while back-side etching creates the tip mass structure and releases the cantilever. When SOI substrate is used, the buried oxide layer is utilized as the etch stop layer for both DRIE processes.

Spray coating is used for front cantilever lithography. First, front-side oxide layer patterning was done in RIE or alternatively using BHF wet etching. Since the wet etching works on both sides of the wafers, the bottom side of the SOI wafer must be protected beforehand. SPR220-3 type thick photoresist was used for back-side masking in the fabrication processes. Following oxide removal silicon etching via DRIE was completed.

The original design of the first-generation devices requires a dicing step at the end of the fabrication to release the devices. The first batch wafer that was fabricated

with the old mask set had 5 working chips but during the dicing process, most of the cantilevers were broken including all the working chips. The final view of the wafer is shown in Figure 2.23. In order to eliminate the dicing step, an updated back-side DRIE mask was prepared including outer frames around the chips. Since the backside etching is already opening through holes around the cantilevers, it can also be utilized for releasing the devices. Figure 2.24 shows the back-side etch process and the final view of the wafer with an updated frame structure.

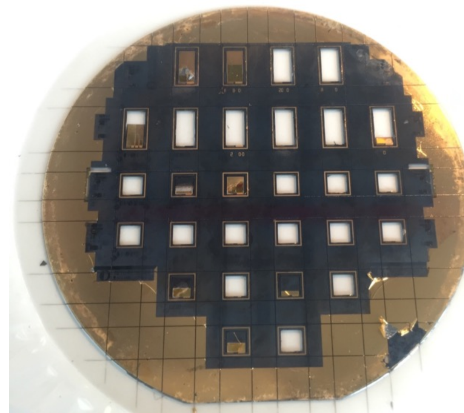


Figure 2.23. SOI wafer after dicing. The cooling water flow in the dicing machine broke the cantilever structures. No working chip was obtained.

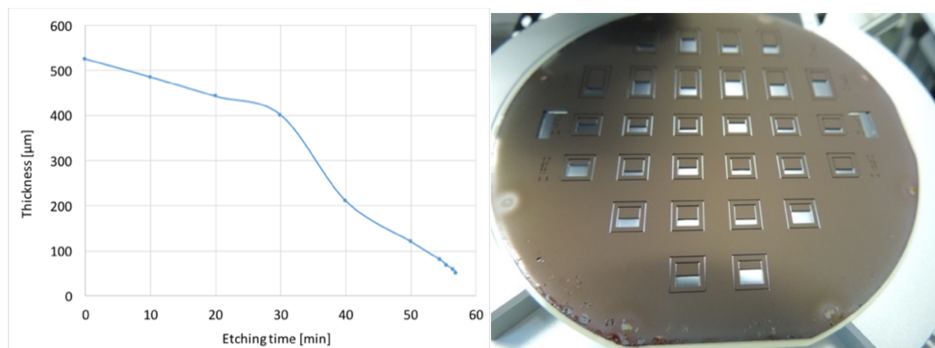


Figure 2.24. Wafer thickness vs DRIE process time (Left). Back side view of the wafer with frames after DRIE process (Right).

Back-side DRIE for cantilever release and tip mass patterning was done in the same Pegasus DRIE system. SPR220-3 photoresist was used for masking. Extra hard

baking was done to improve the photoresist mask. BHF (1:5) solution was used for oxide patterning for 33 minutes. 10 µm undercutting was observed but the resist layer was intact. Wafers were attached to an alumina carrier wafer using crystal bond. The DRIE process was done in 1-minute intervals. 600 µm etching was completed successfully in ~44 minutes. Process wafers were detached from the carrier wafer in hot water (~80 °C). Later acetone and methanol cleaning were applied. Figure 2.25 shows the sample chips released from the wafer.

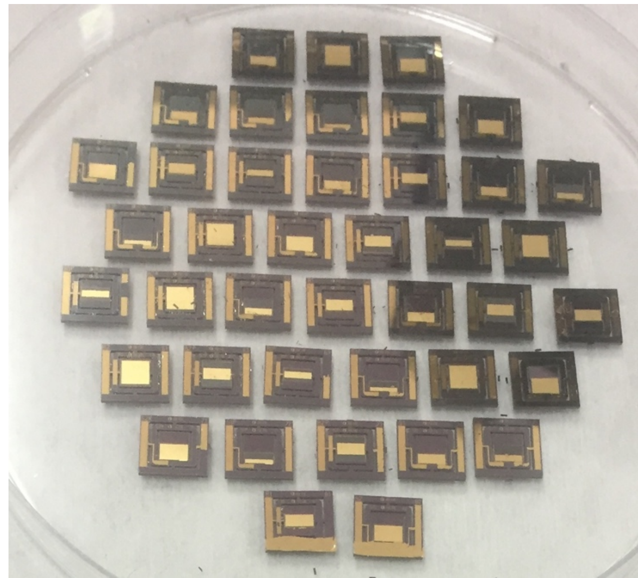


Figure 2.25. New design chips released with back side DRIE process.

2.3 PZT Material Property Verification

2.3.1 Process Temperature Effect on PZT

To verify that the PZT material can keep its factory-given properties after microfabrication processes such as bonding or silicon dry etching, a macro-level brass cantilever was prepared and the effect of heat exposure on the output signal of the PZT was to be observed. Figure 2.26 shows the experimental setup of the brass cantilever with PZT dies bonded at its fixed base to obtain maximum electrical output at the highest stress point.

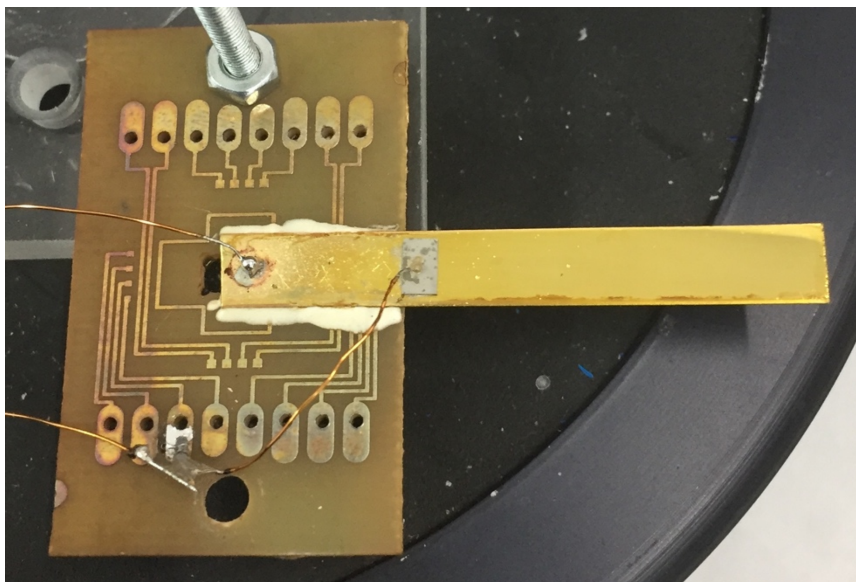


Figure 2.26. Test sample of bulk PZT on brass cantilever attached to a test PCB. Brass surface provides bottom electrode connection via silver epoxy. Top electrode wire is also attached with silver epoxy.

For the comparison test, the samples were first vibrated at 1 g on the shaker table. After the vibration tests, the sample was heated up to ~200 °C on a hot plate. Since the actual PZT piece is on top of several layers, the hot plate temperature was set to a higher value and the PZT temperature was controlled using an IR thermometer. The same vibration tests have been done after the samples cooled down. Figure 2.27

shows the measurement results. A slight increase in the output voltage was observed after heating. This may be due to the reconnection of wires or further curing of the conductive epoxy underneath the PZTs. On average the PZT showed similar performance to the initial test which verifies that the polarization of the material is conserved after exposure to 200 °C temperature which was the bonding temperature for the InAu TLP process.

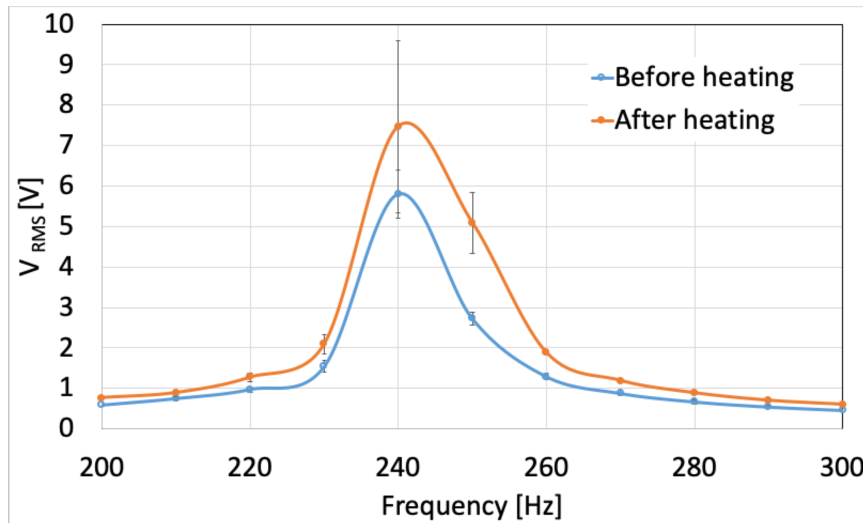


Figure 2.27. Average measurement results of output voltage before and after heat treatment process (200 °C).

2.3.2 Piezoelectric and Hysteresis Measurements with Ferroelectric Tester

Piezoelectric and ferroelectric properties of bulk PZT dies were measured at Afyon Kocatepe University (AKU) piezoelectric materials lab using a Radiant Ferroelectric measurement system for hysteresis curve analysis and an APC wide-range d_{33} meter for piezo constant analysis. Figure 5 shows the test systems. Based on the measurement results a custom Sawyer-Tower circuit was prepared for later in house analysis (Appendix B).

The holder tool of the Radiant system was capable of 1x1 cm^2 pieces. d_{33} meter is also usable with 2-3 cm^2 pieces. 4 mm x 4 mm PZT pieces from both currently used

PZT-5A sheets (purchased in 2015) and previously cut PZT-5H sheets (purchased in 2011). PZT-5A pieces have an Indium coating on the top electrode.

Initial measurements with the d_{33} meter have shown that the PZT-5H pieces' piezoelectric d_{33} coefficient has reduced to 540 pC/N compared to the factory value of 650 pC/N. There is a certain degradation with aging. PZT 5A dies had only one side electrode with indium coating since the original nickel electrodes were removed before the indium deposition, therefore the d_{33} coefficient measurements did not provide healthy results due to insufficient charge collection on the uncoated side.

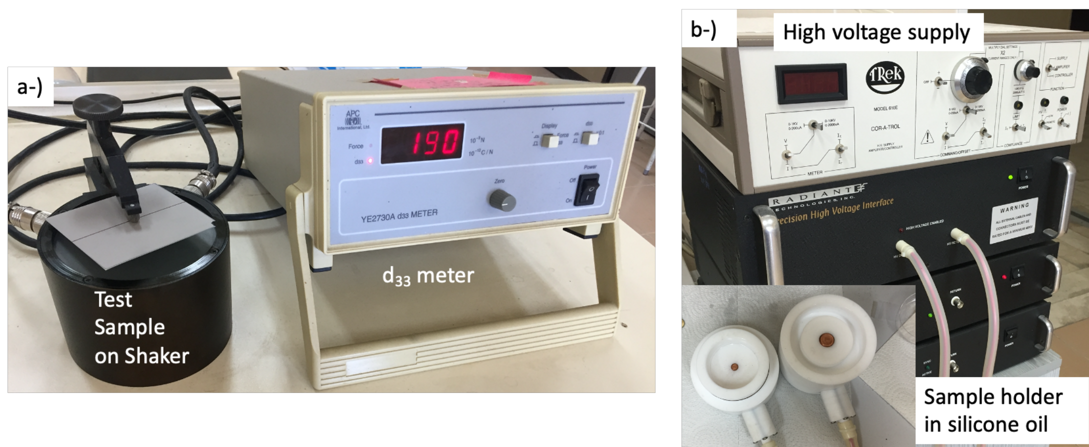


Figure 2.28. Piezo measurement equipment at AKU. a-) d_{33} direct coefficient meter b-) Radiant ferroelectric hysteresis system.

The second run of ferroelectric hysteresis measurements with the Radiant system was done with new PZT-5A and PZT-5H (gold electrode) chips. A set of PZTs from the previous batch (2015) and a sample PZNPT single crystal die have also been tested for comparison purposes. PZNPT has very high piezoelectric coefficients but its Curie temperature is 166 °C and very sensitive to temperature changes [55] therefore it is not directly suitable to be used in the current fabrication process. Table 2.1 shows the overall d_{33} results for different materials and chips before and after hysteresis measurements. Measurement accuracy is ± 30 pC/N which depends on the contact position on the chip and contact pressure. Three measurements were taken for each chip and the averages are reported.

Table 2.1 d_{33} coefficient measurement results for PZT 5A, 5H and PZNPT dies.

<table>
<tr><th>Material</th><th>Die/ Test No</th><th>d33 (pC/N)</th><th>Average d33</th><th>Comments</th><th>Factory Approx. d33</th></tr>
<tr><td rowspan="7">PZT-5A (2015)</td><td>1/1</td><td>-490</td><td rowspan="3">495</td><td rowspan="3">Before Hysteresis</td><td rowspan="19">390</td></tr>
<tr><td>2/1</td><td>-500</td></tr>
<tr><td>3/1</td><td>-496</td></tr>
<tr><td>1/2</td><td>344</td><td rowspan="4">346</td><td rowspan="4">After Hysteresis
(30% Drop!)</td></tr>
<tr><td>3/2</td><td>320</td></tr>
<tr><td>1/3</td><td>368</td></tr>
<tr><td>1/4</td><td>-353</td></tr>
<tr><td rowspan="12">PZT-5A (2020)</td><td>1/1</td><td>-516</td><td rowspan="8">515</td><td rowspan="8">Before Hysteresis</td></tr>
<tr><td>1/2</td><td>-520</td></tr>
<tr><td>1/3</td><td>533</td></tr>
<tr><td>2/1</td><td>-510</td></tr>
<tr><td>2/2</td><td>-494</td></tr>
<tr><td>2/3</td><td>524</td></tr>
<tr><td>3/1</td><td>-510</td></tr>
<tr><td>3/2</td><td>512</td></tr>
<tr><td>1/4</td><td>511</td><td rowspan="4">507</td><td rowspan="4">After Hysteresis</td></tr>
<tr><td>3/3</td><td>-515</td></tr>
<tr><td>1/5</td><td>-495</td></tr>
<tr><td>1/6</td><td>505</td></tr>
<tr><td rowspan="11">PZT-5H (2020)</td><td>1/1</td><td>-745</td><td rowspan="9">723</td><td rowspan="9">Before Hysteresis</td><td rowspan="11">650</td></tr>
<tr><td>1/2</td><td>734</td></tr>
<tr><td>2/1</td><td>-</td></tr>
<tr><td>3/1</td><td>-686</td></tr>
<tr><td>3/2</td><td>-672</td></tr>
<tr><td>3/3</td><td>-750</td></tr>
<tr><td>3/4</td><td>806</td></tr>
<tr><td>3/5</td><td>690</td></tr>
<tr><td>3/6</td><td>703</td></tr>
<tr><td>1/3</td><td>-735</td><td rowspan="2">743</td><td rowspan="2">After Hysteresis</td></tr>
<tr><td>3/7</td><td>-750</td></tr>
<tr><td rowspan="7">PZN-PT</td><td>1/1</td><td>1530</td><td rowspan="7">1421</td><td rowspan="7">Before Hysteresis</td><td rowspan="7">1320</td></tr>
<tr><td>1/2</td><td>1340</td></tr>
<tr><td>1/3</td><td>1242</td></tr>
<tr><td>1/4</td><td>1493</td></tr>
<tr><td>1/5</td><td>1481</td></tr>
<tr><td>1/6</td><td>1470</td></tr>
<tr><td>1/7</td><td>1388</td></tr>
</table>

Following the d_{33} measurements, we have conducted ferroelectric hysteresis analysis in a Radiant ferroelectric tester. Figure 2.29 shows the comparison of the chips at saturation levels (30 kV/cm for PZTs, 10 kV/cm for PZNPT). Both old and new PZT-5A dies show similar characteristics. Old PZT-5As have an indium layer over the top electrode therefore the chip thickness is slightly larger which affects the coercive field (E_c). Other than this the piezoelectric performance is increasing with the smaller coercive field since the dipoles in the material can be changed easily. Direct extraction of piezoelectric coefficients from the P-E hysteresis curve is not possible since the mechanical properties of the materials are also important.

To make sure that the materials are still usable after the high electric field application, the d_{33} measurements were repeated after the hysteresis tests. The expected result

was to observe similar coefficients. For the new PZT-5A and 5H chips the coefficients were similar (within the measurement accuracy range) but for the **old PZT-5A** chips there was a sharp **30% drop** in the average $\mathbf{d_{33}}$ coefficients. Tests were repeated with two dies from each set, in both polarization directions. P-E hysteresis curves were still similar, but the piezoelectric coefficient was lower than the initial values for the old PZT-5A chips. This may explain our observations where some of the harvester chips were working properly in initial tests, then output power decreased in the following experiments. A possible explanation can be the degradation of the grain structure of the ceramics after a certain amount of time. Since the P-E hysteresis curve is similar to the new chips, the problem may also be related to the indium electrode layer. It was suggested that any porous structure inside the piezo material or the electrode boundary can greatly decrease the performance of the material.

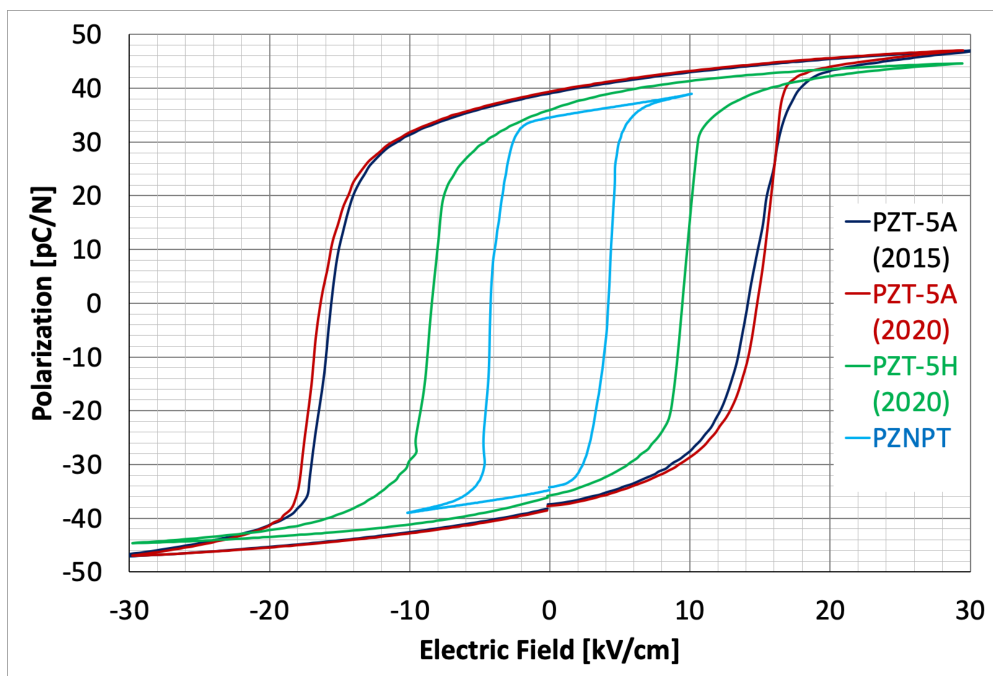


Figure 2.29. Comparison of piezo materials at saturation electric fields (30 kV/cm for PZTs and 10 kV/cm for PZNPT). Piezoelectric performance is increasing with the smaller coercive field, E_c, where polarization is zero.

2.4 Summary of Fabrication Processes

Several fabrication batches were done during the development of the bulk PZT based fabrication process. Table 2.2 shows the different batch properties that have been completed with the first-generation unimorph cantilever design. The initial yield ratio of 2.5% has been improved to 90% in the last batches.

Table 2.2 Different fabrication batches with the 1st generation design

BATCH	INDIUM GOLD BONDING	PZT THINNING	YIELD	PZT THICK. UNIFORMITY	ISSUES
2014	Flip chip	Grinder (ASELSAN)	%5	-	**Most PZT dies broke in grinder**
2015-1	Flip chip	Grinder (ASELSAN)	%0	-	**No working chip**
2015-2	Flip chip	**Lapping (MEMS)**	%25	±25 µm	**Partial bonding, high non-uniformity**
2016-1	**Wafer Level**	**Lapping (MEMS)**	%45	±20 µm	**High non-uniformity, cantilever breakage**
2016-2	**Wafer Level**	**Lapping (MEMS)**	**%90**	**±8.5 µm**	

Based on the fabrication results, new design energy harvester fabrication was continued with the developed recipes. In order to analyze the effect of different bonding and thinning processes on the device performance, wafers were separated into groups for alternative In bonding and thinning processes. Table 2.3 shows the fabrication batches done with the new mask sets. The indium coating of the PZTs and thinning processes were done both at ASELSAN and METU-MEMS to compare the possible effects of different fabrication steps on the output performance of the piezoelectric energy harvesters.

Table 2.3 Fabrication process batches with the 2nd generation design masks.

BATCH	**INDIUM SOURCE-THICK.**	**PZT THINNING**	**YIELD**	**PZT THICK. UNIFORMITY**	**ISSUES**
2019-1	METU-MEMS	Grinder (ASELSAN)	%88	±1.87 µm	Cracking at the edges
2019-2	ASELSAN	Grinder (ASELSAN)	%66	±1.49 µm	Top electrode connection failure in some chips
2019-3	METU-MEMS	Lapping (MEMS)	**%95**	**±0.95 µm**	-
2021	METU-MEMS	Lapping (MEMS)	%80	±1.73 µm	Lapping wheel flatness

CHAPTER 3

1ST GENERATION BULK PZT ENERGY HARVESTER

Piezoelectric energy harvester based on a unimorph design has been studied in our group previously [56], but the fabrication process had a low yield and included non-optimized processes. During the development of the fabrication improvements, modified versions of the unimorph cantilever masks have been used. Figure 3.1 shows a sample fabricated chip and the model of the unimorph design. The cantilevers were designed to have a resonance frequency around 500 Hz.

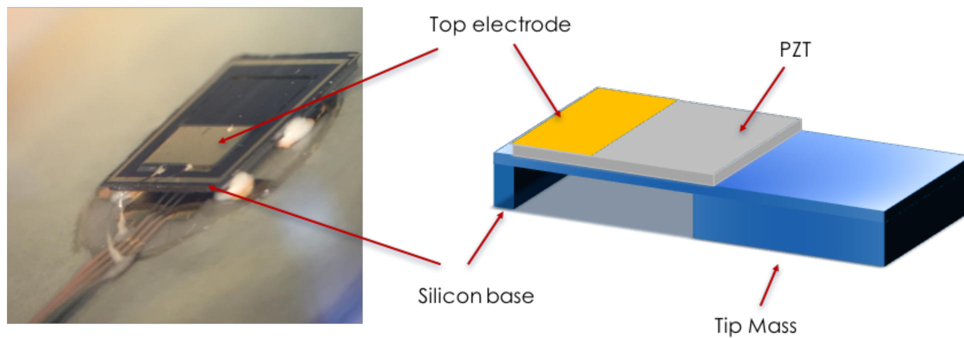


Figure 3.1. 1st generation design of the unimorph piezoelectric cantilever.

3.1 Unimorph Cantilever Design Vibration Tests

The first main test of the fabricated piezoelectric harvester is the vibration test on the shaker table setup. For this test, custom PCB holders were prepared where the test chip is tightly fixed using a top PMMA layer and four screws. Figure 3.2 shows the holder used in the experiments.

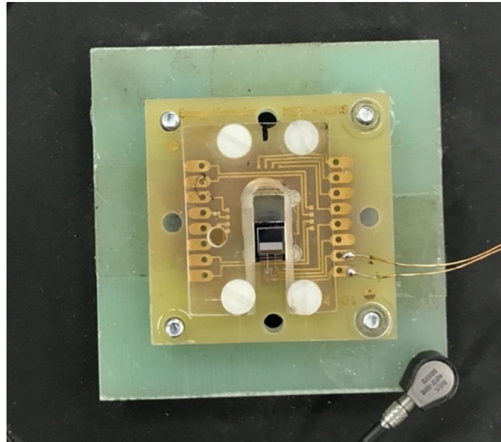


Figure 3.2. PCB holder with the test chip attached on the shaker table.

The harvester chip showed regular resonance characteristic. The output voltage was measured from the top and bottom electrodes using two oscilloscope probes. Using the frequency sweep function of the shaker table, the first resonance frequency was found to be 594.5 Hz at 0.1g acceleration. This value stayed consistent throughout the experiments. The resonance sweep test result is shown in Figure 3.3.

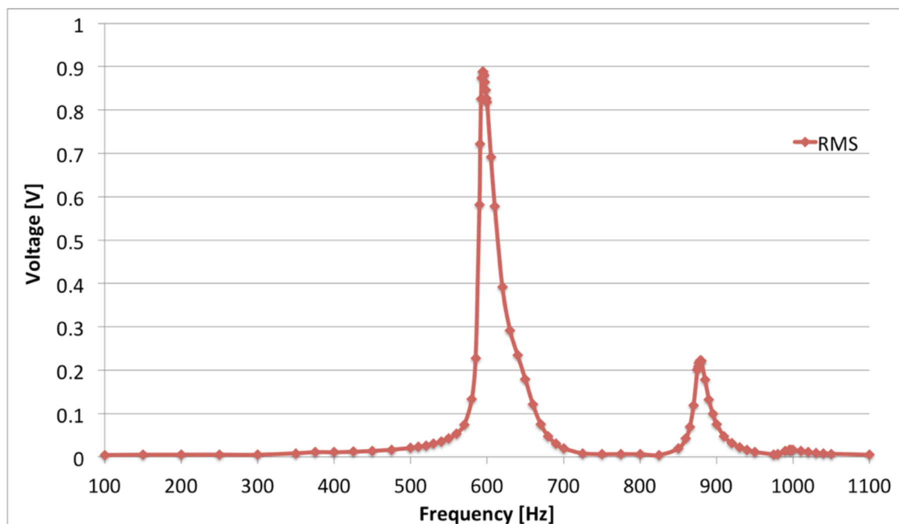


Figure 3.3. Frequency sweep at 0.1g.

The maximum value of open circuit DC RMS voltage obtained was 1.47 V at 594.5 Hz, 0.1g. The optimum load measurements were done with this configuration and

the results are shown in Figure 3.4. In order to observe resonance shift at different accelerations, measurements were taken with 0.025g steps between 0.025g and 0.15g. There is only a 1Hz/0.05g shift in the resonance frequency.

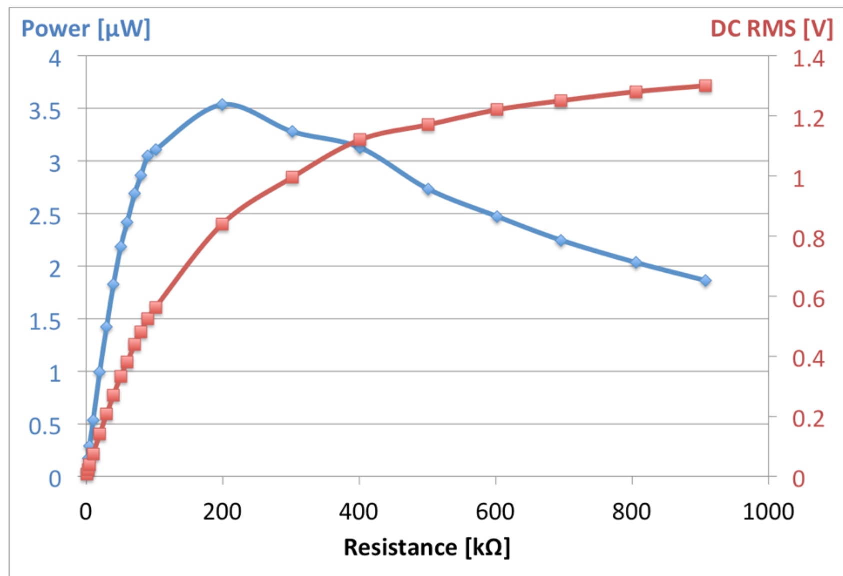


Figure 3.4. Maximum power output from the chip was 3.5 µW at 0.1g acceleration, 594.5Hz with 200kΩ load.

3.2 Modeling of Piezoelectric Harvesters

Finite element modeling (FEM) is a widely used technique for designing piezoelectric energy harvesters. Although there are analytical modeling methods for cantilever devices, MEMS energy harvesting devices generally have complex structures with many thin layers and coupled parameters. This makes it harder to analytically solve the dynamic equations alongside piezoelectric constitutive equations. Numerical methods such as FEM overcome these difficulties thanks to the increasing computation power of modern computers.

In this study, COMSOL Multiphysics software is utilized for modeling MEMS piezoelectric acoustic energy harvesters due to its versatility as a multiphysics simulation environment. A wide variety of software modules enable integration of

different types of physics problems in the same model. This approach will enable us to integrate the energy harvester model with structural and acoustic models of the middle ear and even the stimulation circuitry models in the future.

3.2.1 Modelling Constraints

In the scope of the FLAMENCO project, a piezoelectric energy harvester is to be placed in the middle ear cavity while connected to a hearing element such as an ossicle or eardrum. It should work with 120 dB sound input at 4 kHz frequency. These parameters were chosen to have high acoustic energy and maximize the ear canal amplification effect, respectively. Therefore, the total volume and mass of the harvester are major constraints. The footprint of the chip should not exceed 5x5 mm^2 and mass should be kept at a minimum. The added mass on the haring structures would cause a damping effect on the vibration of the harvester. This phenomenon will be examined more in the following sections.

Material selection and general geometry are defined by the developed fabrication method. The bulk PZT dies should have a rectangular shape in order to have effective dicing and easier bonding processes. Because of that, the cantilever shape should also be rectangular. There are studies in the literature suggesting trapezoid-like cantilever structures for more uniform stress distribution along the cantilever. On the other hand, a rectangular prism structure is easier to model and handle. It is not expected to have a large penalty for having a rectangular cantilever shape.

3.2.2 COMSOL Modeling

COMSOL Multiphysics is a modular software package. For the modeling requirements of the piezoelectric energy harvester, the Structural Mechanics with Piezoelectric Devices interface was used. For simulating the external electrical load, an Electrical Circuit interface from the AC/DC module was used.

Custom meshing has been used to cover the piezoelectric material correctly. At least 5 elements should be present over the thickness of the piezoelectric element to correctly apply the piezoelectric equations. Figure 3.5 shows the meshing structure in the validation model. Moreover, the PZT-5A properties available in the Material Library were different from the vendor-specified bulk PZT-5A properties. A corrected version of the material record has been used.

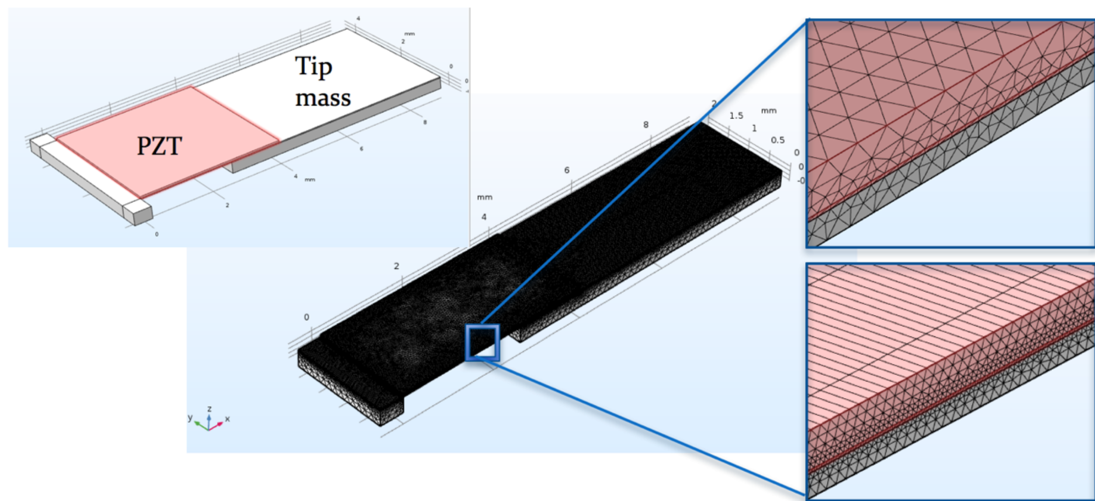


Figure 3.5. Meshing structure in the 3D validation model. At least 5 elements should be present along the piezoelectric layer thickness.

3.2.3 Model Validation

In order to validate that the COMSOL solution reflects the actual physical phenomena correctly, a CAD model of the tested 1st generation piezoelectric energy harvester chip was imported. Using both 2D and 3D models voltage and power output of the chip were calculated and compared with the experimental results. Figure 3.6 shows the comparison graphs. Initially, the voltage output was in good agreement with the experiments, but the power output was quite different. After many troubleshooting attempts, a correction factor is included in the resistive load model to correctly match the experimental power output.

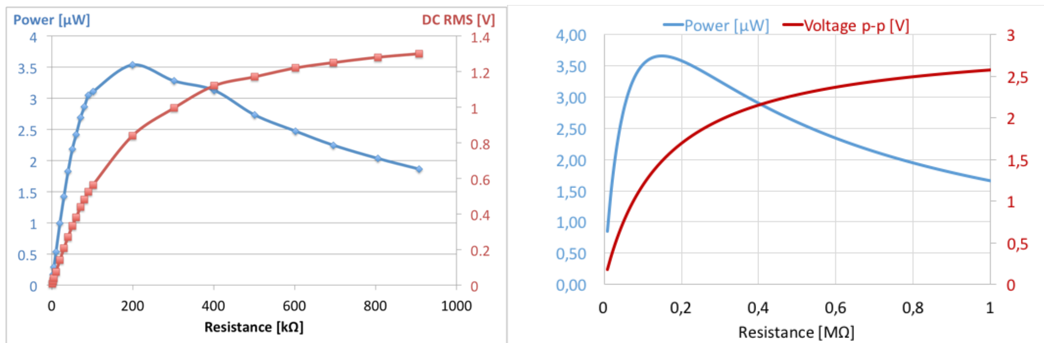


Figure 3.6. (Left) Experimental result of the piezoelectric harvester chip (Right) Simulation results of the corresponding model with COMSOL.

Between 2D and 3D models, the 3D model more closely predicts the resonance frequency of the actual chip. The 2D model (Figure 3.7) has a 1.5% relative error in the frequency but the output voltage values were much closer. Considering the 2D model almost took 100 times faster to calculate, the error margin can be accepted for quicker analysis.

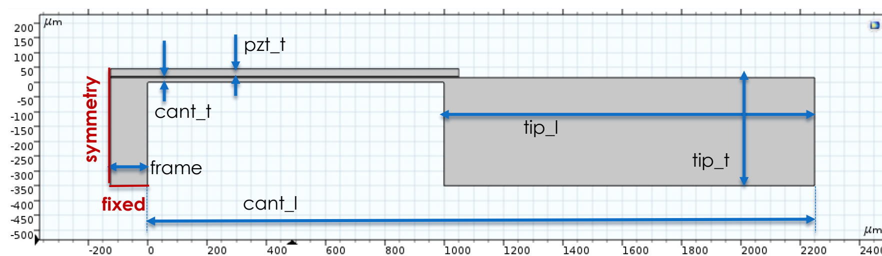


Figure 3.7. Two-dimensional COMSOL model used for analyzing the cantilever

3.3 Acoustic Energy Harvesting with PZT

Previous research on acoustic piezoelectric energy harvesters focuses on diaphragm structures with a cavity to scavenge sound power. Up to 9.8 nW/cm^2 of power density was reported at 100 dB sound pressure level (SPL) using thin film lead-zirconate-titanate (PZT) MEMS acoustic energy harvesters [57]. A piezoelectric cantilever array reported by Jang et al. uses a thin film AlN piezoelectric transducers [31], but

the generated voltage is on the order of 50 μV and requires an external power source for neural stimulation. Beker et al. theoretically investigated the bulk piezoelectric energy harvesters attached to a flat ear drum model and verified the efficiency of using bulk PZT for power generation in CIs [19].

The main aim of the piezoelectric harvesters is to be used on the eardrum as a part of the fully implantable cochlear implant (FICI) system. Therefore, it is crucial to test the piezoelectric harvester coupled to a vibrating membrane simulating the eardrum vibrations under a certain frequency and amplitude of a sound. It is not possible to attach the harvester chip directly to the ear drum due to biocompatibility issues and space requirements of the tip mass motion. Since the tip mass bottom surface is leveled with the outer frame, the cantilever part of the harvester chip should be elevated to a certain height, preventing the impact of the tip mass to the base surface. For these reasons, a flexible attachment layer was designed and fabricated.

Parylene was chosen as the base material since it is a polymer with superb biocompatible properties, and we have the required expertise in fabricating different kinds of parylene-based devices. Figure 3.8 show the proposed fabrication flow for the flexible attachment.

The piezoelectric harvester chip requires at least two electrical connections per cantilever. In order to supply electrical connections to the chip, thin film metal connection lines made of Ti-Au were used on the parylene base. This solution provides a flexible connection from the chip to a ZIF connector.

The spacing requirement of the tip mass was provided by using four electroplated metal columns under the outer frame of the harvester chip. The electrical connection layer was also used as the seed layer for the electroplating process. Copper was used in the first-generation parylene attachment layers since electroplating higher structures is easier compared to gold and nickel. However, during the electroplating process, many copper sections were peeled off due to high residual stress.

Figure 3.9 shows the final parylene attachment along with two chips bonded on the parylene membrane.

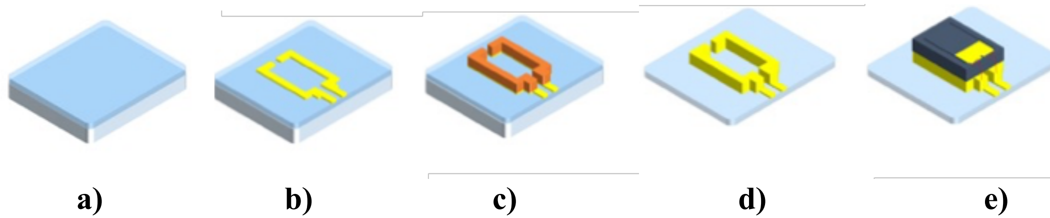


Figure 3.8. Parylene attachment fabrication flow. (a) Parylene coating on a glass wafer, (b) Ti-Au deposition and patterning, (c) Metal electroplating, (d) Electroless Au coating on metal surfaces for wire bonding, (e) Parylene etching, chip bonding after release in acetone.

Figure 3.9. Parylene attachment layer with metal connection lines and copper spacer columns. Two chips from the SOI-2 wafer were bonded using epoxy on the copper columns.

Figure 3.10 and Figure 3.11 show the schematic view of the acoustic test setup. The energy harvester chip is attached to a parylene membrane (~40 μm thick) which vibrates with the incoming sound. Sound input is controlled with a signal generator. Sound level at the inlet of the ear canal simulator (a hollow tube (R=9 mm and L=3.5 cm), i.e., ear canal and ear drum dimensions, Figure 3.12) is measured with a dB meter. The output voltage of the chip is rectified and measured with an oscilloscope. The piezoelectric chip is fixed with epoxy on the flexible parylene carrier before attaching the device to the membrane. Epoxy bumps prevent the tip mass from

contacting the membrane surface while vibrating. Electrical connections are established using wire bonding and conductive epoxy. A circuit with custom off-chip components and a microcontroller is used for generating a biphasic neural stimulation signal with the piezoelectric transducer output to show the feasibility of the chip as a sound sensor.

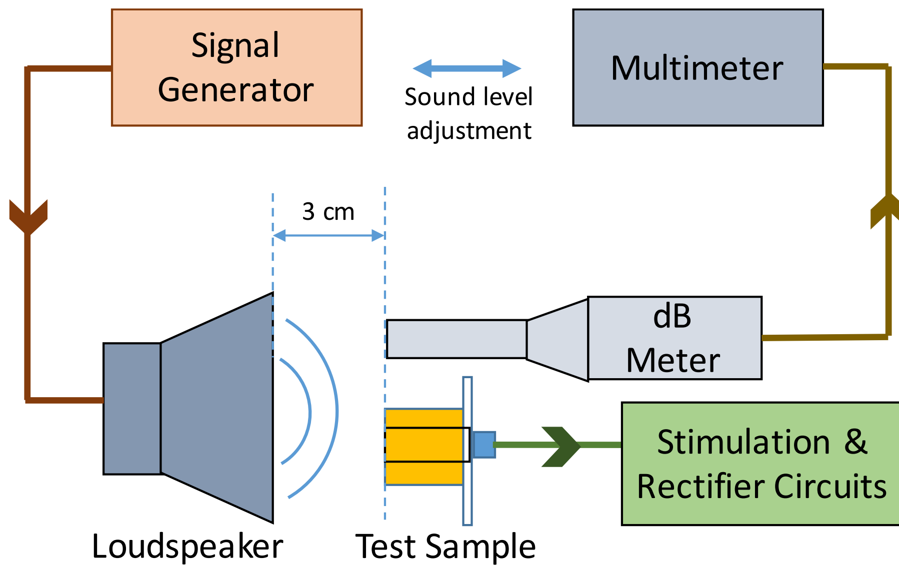


Figure 3.10. Schematic view of the acoustic test setup

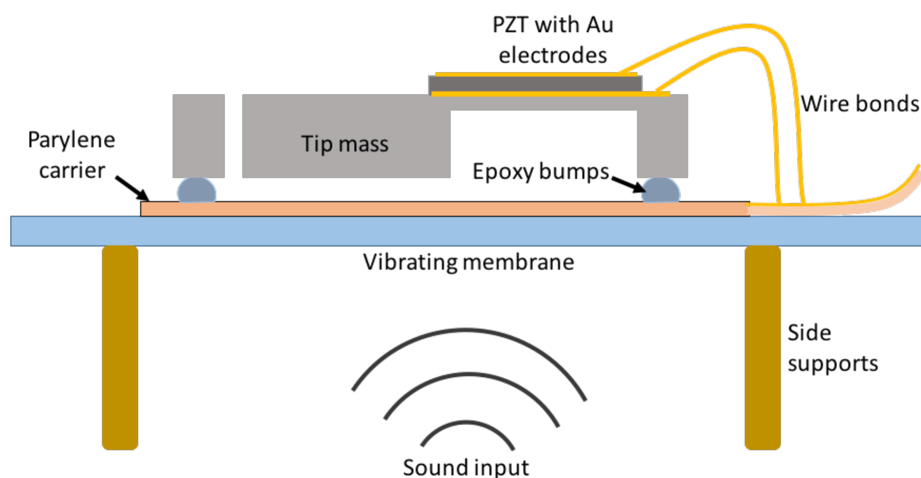


Figure 3.11. Schematic view of the test sample.

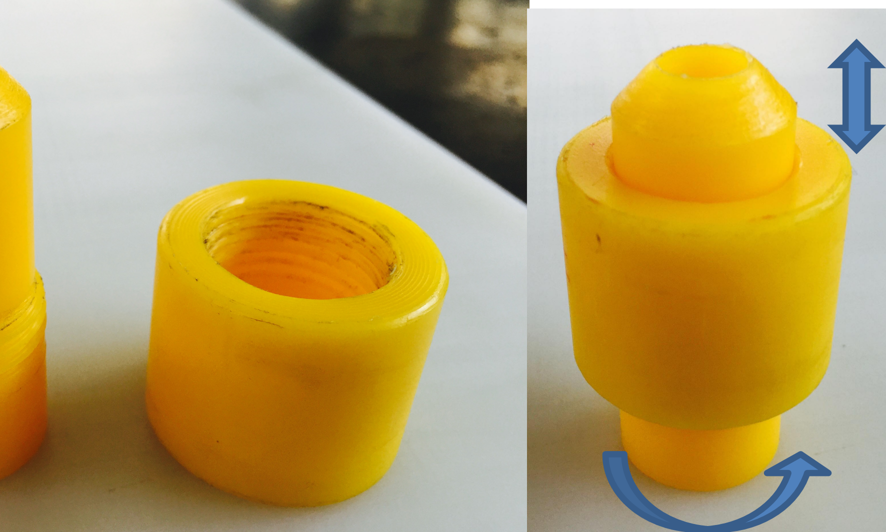


Figure 3.12. Actual view of the energy harvester chip on the vibrating membrane for acoustic experiments (Left). The tension mechanism adjusts the parylene membrane stretching (Right).

Figure 3.13 shows the acoustic test results for different sound levels and corresponding stimulation signals. 1.51 V_{rms} output is obtained with 120 dB-A acoustic input at the inlet of the canal. The generated voltage is sufficient for the state-of-the-art signal processing circuits of the CIs (6 mV at 90 dB SPL [16], [31]). Figure 3.14 shows the rectified power output with respect to load resistance through the voltage doubler circuit. Maximum DC output power is **16.25 µW at 2.47 V_{DC}.** These results indicate that the harvested power can be used for supplementing the FICI battery.

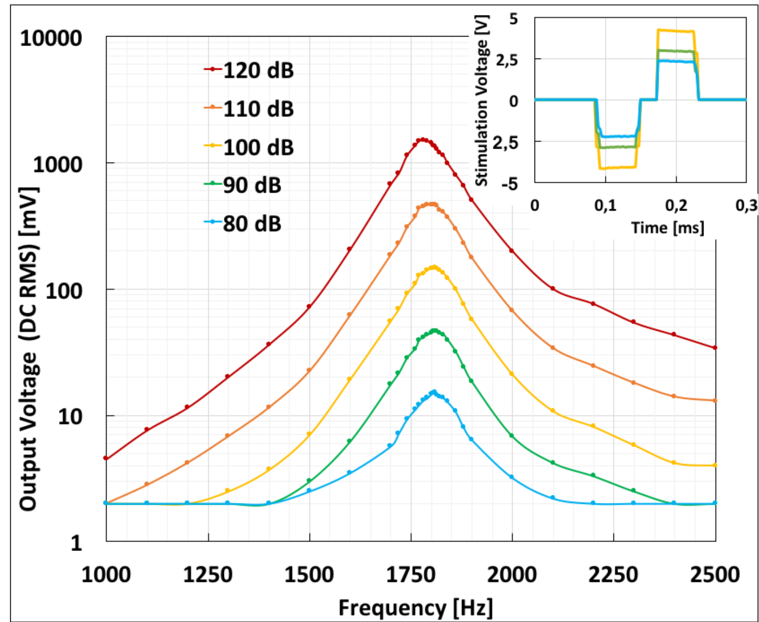


Figure 3.13. Measured frequency sweep results of the prototype chip. Inset is the stimulation signals of 1.8 kHz input at 80,90 and 100 dB. The stimulation circuit output has biphasic pulses at 1 kHz.

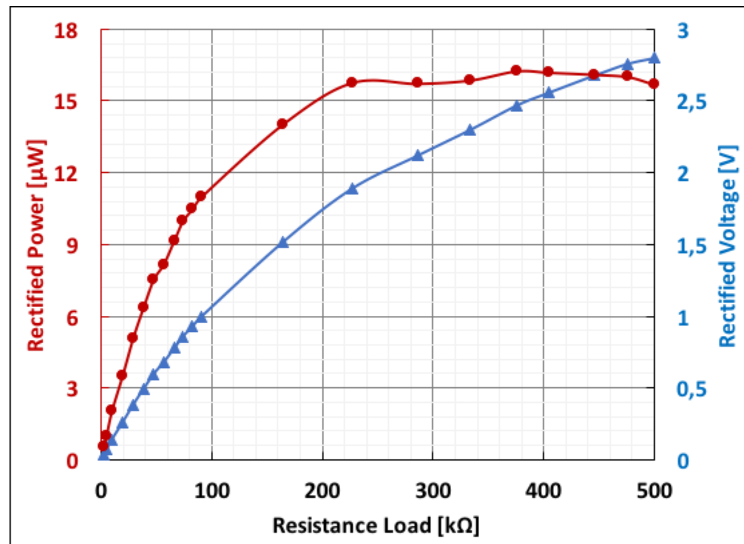


Figure 3.14. Measured rectified power and voltage characteristics with varying load for maximum power generation at 1780 Hz 120 dB-A sound input. The output signal is rectified using a doubler circuit. The maximum power is 16.25 µW with 2.47 V_{DC}.

3.4 Summary of the 1st generation device tests

The 1st generation energy harvesters were used for both fabrication process development and experimental setup design. Although the initial fabrication yield was low, we could obtain significant test results with both vibration and acoustic tests. Table 3.1 summarizes the main differences between the fabrication batches and the corresponding best test results. With the latest acoustic tests which were presented at the Eurosensors conference [20], we showed the best power density among the similarly sized energy harvesters.

Table 3.1 Summary of first-generation test results of the fabrication batches.

Batch	**Bonding**	**PZT Thinning**	**Vibration Test Results (Max)**	**Acoustic Test Results (Max)**
2014	Flip chip	Grinder	3.5 µW @ 0.1g	-
2015-1	Flip chip	Grinder	-	-
2015-2	Flip chip	Lapping	100 nW @ 0.1g	520 nW @ 110 dB
2016-1	Wafer Level (w/ shadow mask)	Lapping	150 nW @ 0.1g	1.5 µW @ 110 dB
2016-2	Wafer Level (w/ shadow mask)	Lapping	2.16 µW @ 0.1g	16.25 µW @ 120 dB

Table 3.2 Comparison with previous acoustic energy harvesters.

	Device dimensions (cm^3)	**SPL (dB)**	**Power density (W/cm^3)**
Horowitz et al [58]	2.445	149	2.94×10^{-12}
Liu et al [59]	2.47	161	14.48×10^{-3}
Atrah and Salleh [60]	0.0055	100	3.6×10^{-10}
Koyuncuoglu et al [20]	0.0108	120	1.5×10^{-3}
Yuan et al [61]	2.133	114	9.85×10^{-5}

After the acoustic tests, the energy harvester chip with the parylene membrane is placed on an ear model for demonstration purposes. Figure 3.15 shows the attached chip on-ear model.

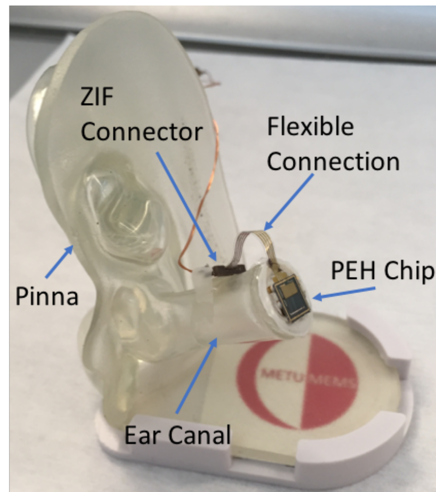


Figure 3.15. Piezoelectric Energy Harvester (PEH) chip attached on vibrating membrane at the end of ear canal model. Flexible parylene connection transfers the signal with a ZIF connector on ear canal wall.

CHAPTER 4

2nd GENERATION ENERGY HARVESTER DESIGN AND VIBRATION EXPERIMENTS

In the scope of this study, the main aim is to design a high-performance piezoelectric energy harvester that can be implanted in the middle ear. Based on the previous fabrication processes and test results, a new design of a piezoelectric cantilever chip has been proposed. The goal is to maximize power output from the same size PZT die.

The new PEH design is developed mainly considering the loading effect on the ear drum. Most of the energy harvesters in the literature are designed for large structures where the effect of the harvester motion on the host structure is negligible (Figure 4.1). For cochlear implant applications, this approach would cause problems as the effective mass of the eardrum is comparable to MEMS scale energy harvesters.

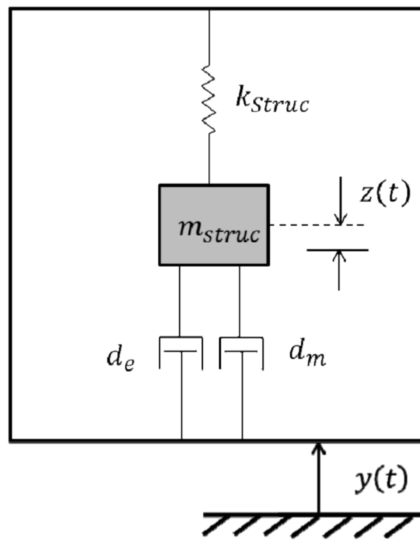


Figure 4.1. Basic vibration energy harvesting model. In our case the y(t) excitation is coming from the tympanic membrane via acoustic input.

The effect of mass loading on ear drum vibrations has been studied in several papers [62]–[64]. Central loading on the eardrum decreases the vibration amplitude considerably as shown in Figure 4.2.

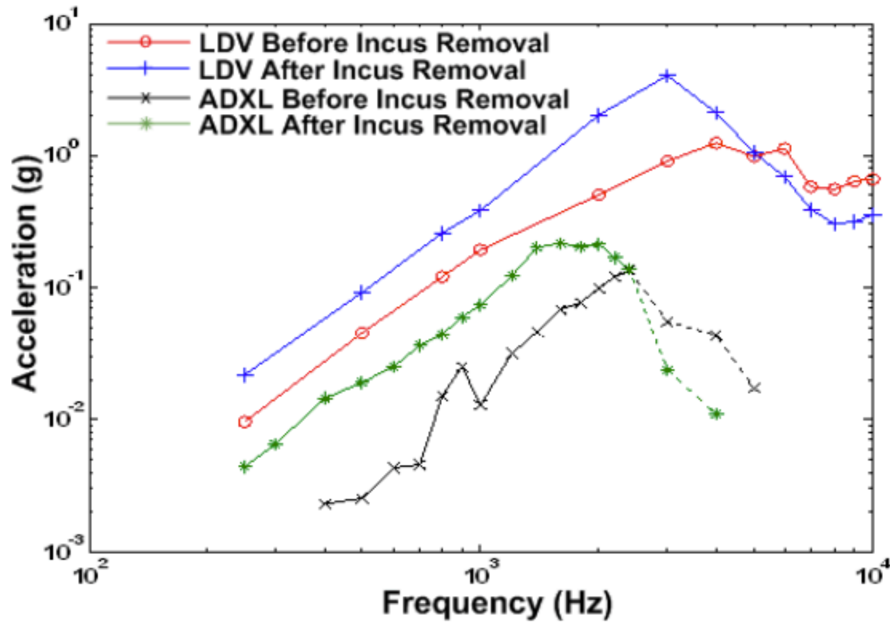


Figure 4.2. Umbo acceleration measurement with laser Doppler vibrometer and accelerometer (ADXL320). Incus is the second ossicle bone in the middle ear and generally removed in cochlear implant surgeries [64].

Contrary to the constant acceleration case, for constant acoustic pressure, the effective acceleration value on the harvester is dependent on the harvester mass. This will also be the case when the chip is implanted in the patient's ear. As the harvester mass brings extra inertia to the hearing mechanism the vibration amplitude and the acceleration will drop significantly. In order to estimate the amount of the decrease in the acceleration with respect to the harvester mass, previous studies on the subject have been reviewed. A linear approximation has been suggested as shown in Figure 4.3 and used in the calculation of effective acceleration.

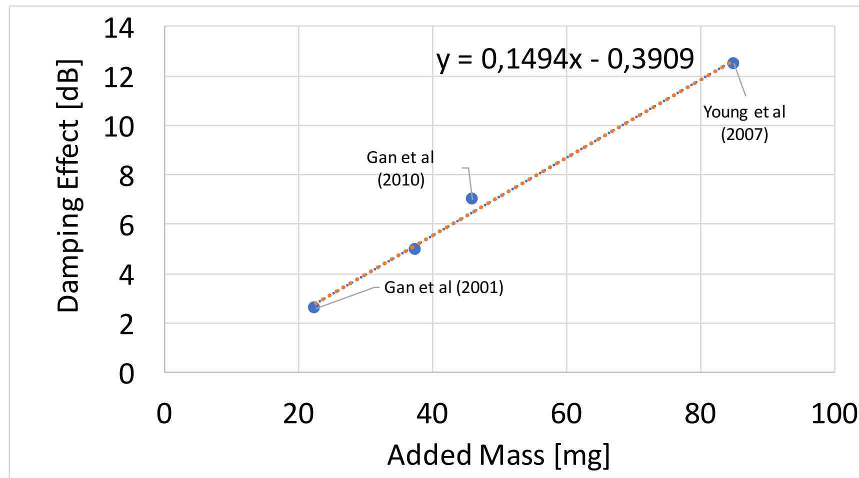


Figure 4.3. Linear approximation of damping effect of added mass on the hearing mechanism. Damping effect shows the decrease in the acceleration with respect to unloaded case in dB units. [63]–[65].

4.1 New Generation Device Design

Since the maximum stress on the cantilever occurs at the fixed end, it is crucial that the PZT layer covers this section. But since the PZT die is attached on the silicon during fabrication, the edge of the PZT is not bounded. This creates an unused volume at the end of the PZT which disrupts the stress and voltage distribution as shown in Figure 4.4 and Figure 4.5. In order to avoid this, an alternative design has been proposed.

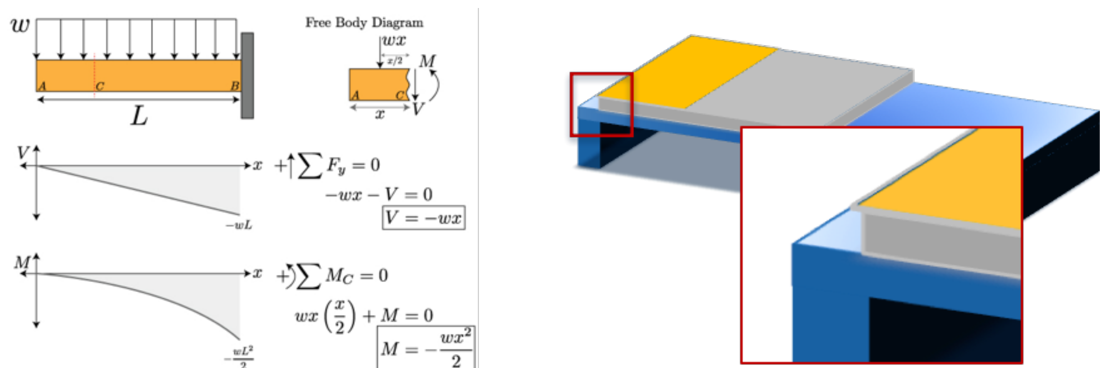


Figure 4.4. Maximum stress point based on the analytical formulation is the fixed base of the silicon cantilever. The PZT die attached on the cantilever is free on the thickness direction.

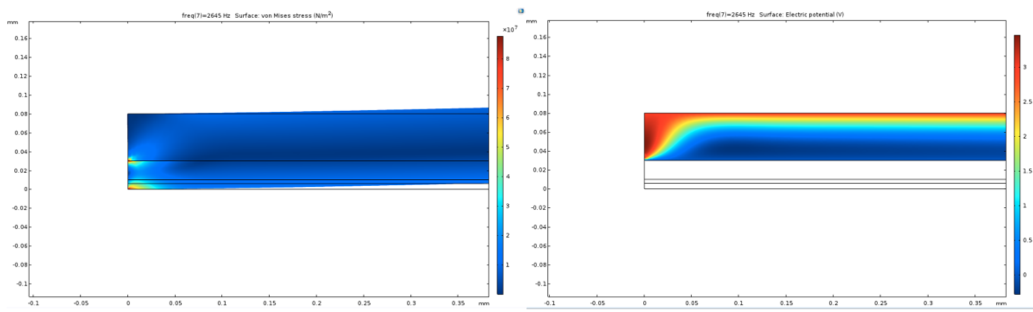


Figure 4.5. (Left) Stress distribution on the cantilever base under 1 g vibration at 2645 Hz resonance frequency. (Right) Voltage distribution across the PZT layer.

In the new harvester design, instead of using a PZT die for a single cantilever, the PZT is bonded at the common base point of two identical cantilevers. The chip mimics a butterfly with the PZT layer in the middle of the wing-like cantilevers (Figure 4.6). This configuration enables obtaining higher average stress on the PZT since more material is closer to the anchor point. Analyzing the stress and voltage distributions showed a more uniform distribution (Figure 4.7). Compared with the single cantilever unimorph design output voltage is increased by about 25% (Figure 4.8). Due to the continuous boundary at the edge, the resonance frequency of the butterfly design increases. 3D modeling of the complete structure and size optimization is continued.

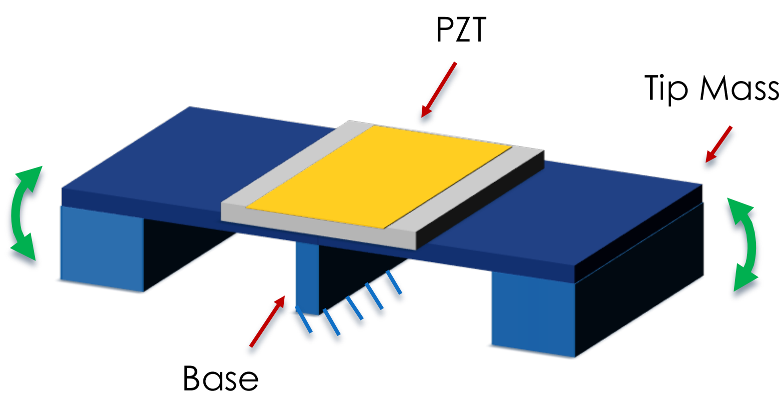


Figure 4.6. The butterfly concept with two back-to-back cantilevers and a common PZT die over the anchor point.

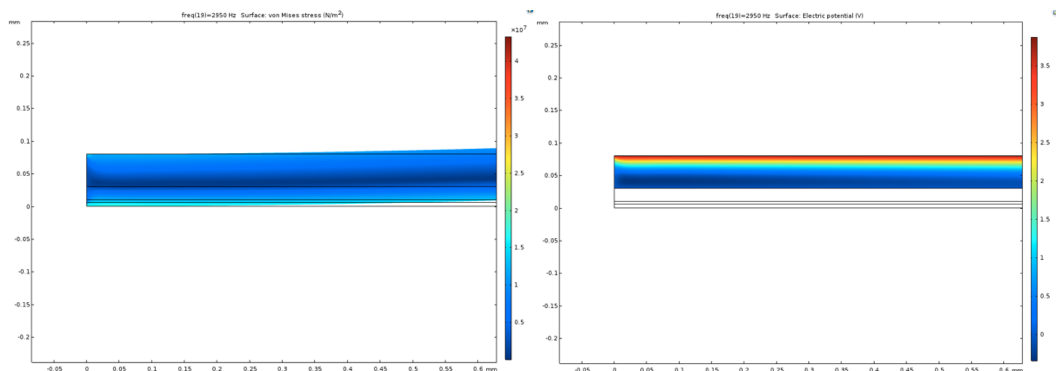


Figure 4.7. (Left) Stress distribution on the cantilever base under 1 g vibration at 2950 Hz resonance frequency. (Right) Voltage distribution across the PZT layer.

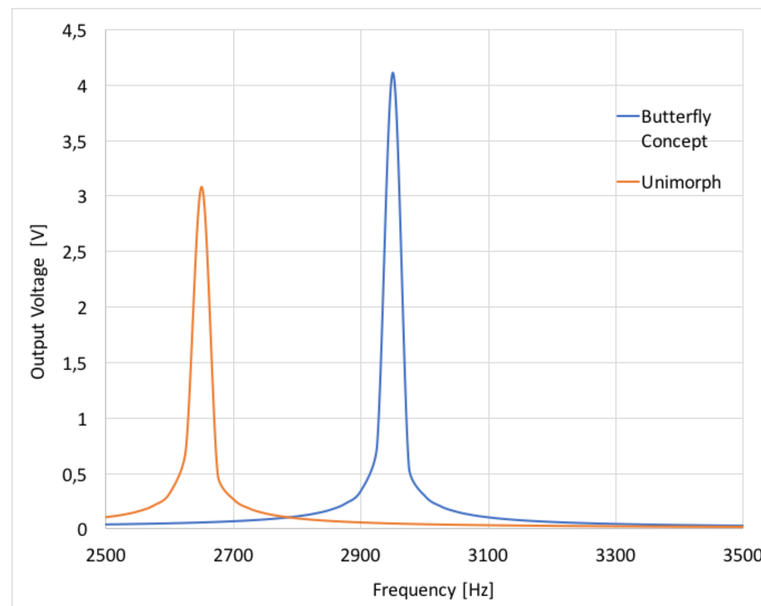


Figure 4.8 Comparison of unimorph and butterfly design output voltages under 1 g vibration.

4.1.1 Cantilever Parameters

Two types of cantilever structures were analyzed and designed. The first one is the simple unimorph cantilever structure similar to 1st generation chips. The second design is the new double cantilever structure. Each design's resonance frequencies

were calculated as separate parameter sweeps. Due to a large number of parameters, the model files become too large (>100GB) that the sweeps had to stop. Therefore, some parameter reduction should be done. In the first step, the PZT thickness was coupled with the silicon thickness for optimum centroid location. Table 4.1 shows the calculated centroid position from the bottom silicon surface. Red markings show that the centroid is either in the PZT material or silicon. For maximum output, it should stay in the bond interface which corresponds to white cells. Approximately a coefficient of 1.7 of PZT thickness to Si thickness was calculated. In all the models this coefficient is used.

Table 4.1 PZT vs Si thickness values for optimum centroid location based on 5 µm thick bonding layer. White segment is the target area for the centroid to be along the bonding layer.

Thickness [µm]		Si										
		10	15	20	25	30	35	40	45	50	55	60
PZT	10	9.72	11.83	14.10	16.44	18.82	21.23	23.66	26.11	28.56	31.02	33.49
	15	11.68	13.62	15.76	18.01	20.32	22.68	25.07	27.47	29.90	32.33	34.78
	20	13.74	15.51	17.53	19.68	21.92	24.22	26.56	28.93	31.31	33.72	36.14
	25	15.88	17.50	19.39	21.45	23.61	25.84	28.13	30.45	32.80	35.17	37.56
	30	18.08	19.56	21.33	23.29	25.37	27.54	29.77	32.04	34.35	36.69	39.04
	35	20.33	21.67	23.33	25.19	27.19	29.29	31.46	33.69	35.95	38.25	40.58
	40	22.61	23.83	25.38	27.15	29.08	31.11	33.22	35.39	37.61	39.87	42.16
	45	24.92	26.03	27.48	29.16	31.01	32.97	35.02	37.14	39.32	41.54	43.79
	50	27.26	28.26	29.61	31.21	32.98	34.88	36.87	38.94	41.07	43.25	45.46
	55	29.61	30.52	31.78	33.29	34.99	36.82	38.76	40.78	42.86	45.00	47.18
	60	31.98	32.80	33.98	35.41	37.04	38.81	40.69	42.65	44.69	46.78	48.92

4.1.2 Calculation Results

Based on these parameters eigenfrequency analysis was done for each model. After the sweep is done, parameter sets that have Eigen frequencies close to target

frequencies of 1, 2, 3, and 4 kHz were chosen. These parameter sets were put in a frequency domain analysis around the eigenfrequency. For 1 g input acceleration, the voltage and power response of the PZT cantilevers were calculated.

Table 4.2 shows the results of 1 g respectively with the highest power output for each target frequency. The butterfly design starts from 3 kHz because the geometry parameters could not be obtained for lower frequencies.

Table 4.2 1 g constant acceleration results of the designs with highest power output near target frequency.

	Single				Butterfly	
Target Frequency	1000	2000	3000	4000	3000	4000
tip_l [μm]	1500	2500	2700	2900	1450	1450
tip_t [μm]	600	600	600	600	250	400
cant_t [μm]	15	25	35	45	10	15
Frequency [Hz]	1033	2011	3041.5	4018.5	2995	3991.5
OC Voltage [V]	10.76	10.5	8.12	6.69	3.11	3.4
Opt. Res. [MΩ]	0.07	0.09	0.08	0.07	0.1	0.1
Power [μW]	**102.5**	**76**	**52**	**41.4**	**24.9**	**29.2**

For mass calculation in the COMSOL models, the intop1( ) integral operator was used over the surface area of the 2D model and multiplied with the width value. Then a logarithmic decibel calculation was used to modify the input acceleration value to the actual effective acceleration for the harvester. Input acceleration values corresponding to the 100 dB at the specific frequencies were adapted from Young et al [64].

Table 4.3 shows the 100 dB results of the best designs. 4 kHz results are especially higher than the rest due to higher input acceleration at this frequency. This is due to the ear canal amplification at this frequency.

In order to satisfy the project goals, the 120 dB performance of the designs was also investigated based on the extracted acceleration values from previous umbo motion

measurements (Figure 4.9). Unfortunately, only the 4 kHz butterfly design was below the yield strength limit of the PZT material. All other designs would fail at such high input accelerations. The butterfly design resulted in an impressive 356 μW power output at the 120 dB sound input.

In conclusion, several different parameter sets will be used in the mask design for the new piezoelectric energy harvester. Butterfly designs have lower output at constant input acceleration tests but they become more advantageous in the acoustic tests.

Table 4.3 100 dB constant input sound pressure results of the designs with highest power output near target frequency. Effective acceleration on the harvester is also given for comparison purposes.

	Single				Butterfly	
Target frequency	1000	2000	3000	4000	3000	4000
tip_l [μm]	2700	2900	2900	2900	1450	1450
tip_t [μm]	600	400	450	350	250	400
cant_t [μm]	15	20	30	35	10	15
Acc. [g]	**0.33**	**0.64**	**0.84**	**1.3**	**1.03**	**1.4**
Frequency [Hz]	1074	1969	3024	4041	2995	3991.5
OC Voltage [V]	5.8	6	6.23	11.26	3.21	4.95
Opt. Res. [MΩ]	0.14	0.1	0.08	0.07	0.1	0.1
Power [μW]	**15.6**	**23**	**29.4**	**123.5**	**26.6**	**114**

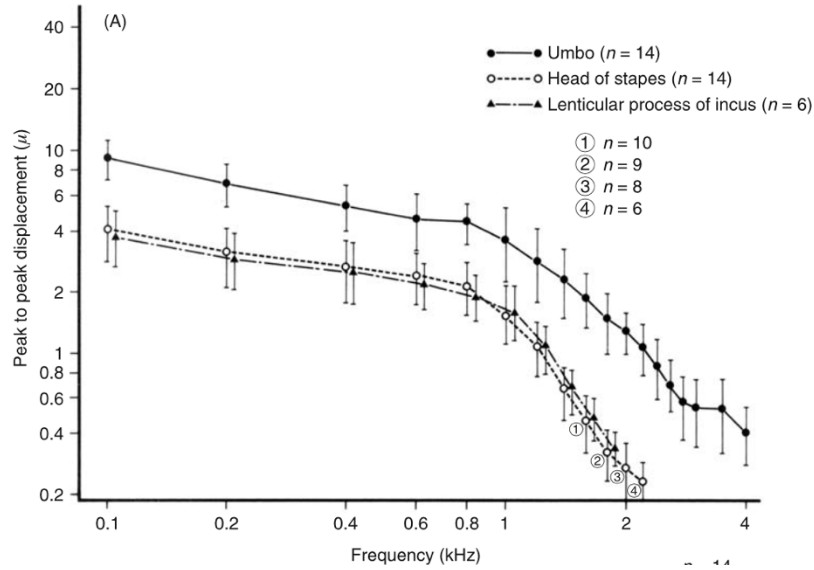


Figure 4.9 Umbo displacement at 124 dB [66]. Average $a_{120dB} \approx 7.24$ g

Table 4.4 124 dB acceleration approximation

	Single				Butterfly	
Target frequency	1000	2000	3000	4000	3000	4000
tip_l [μm]						350
tip_t [μm]						550
cant_t [μm]						15
Acc. [g]						**4.7**
Frequency [Hz]			FAILED			3981.5
OC Voltage [V]						7.67
Opt. Res. [MΩ]						0.04
Power [μW]						**356**

4.1.3 Mask Set

Mask designs have been completed considering both simulation results and fabrication constraints. Basic bulk PZT harvester fabrication flow is a 7-mask process. Table 4.5 shows the mask list. The First 6 masks are lithography masks for

the process wafers. 7th mask is used for shadow mask fabrication which is utilized in the PZT bonding process. Only the electrode masks are clear field types. Back-side DRIE masks are mirrored types and aligned using the back-side alignment.

Table 4.5 Mask list

	Fabrication Layer	**Description**
1	Bottom electrode	Defines the bottom electrode and bonding area
2	Parylene opening	Active top electrode area
3	Top electrode	Top electrode layer and contact pad definition
4	Front DRIE	Defines cantilever and test frame shapes
5	Back DRIE-1 Frame	For adjusting the tip mass thickness via DRIE thinning
6	Back DRIE-2 Tip mass	Tip mass size
7	Shadow mask for bonding	For PZT alignment during bonding, separate wafer

4.1.4 Test Frames and Device Holder

The first-generation chips were tested on PCBs with electrical contacts via wire bonding. Making a bond on the top electrode contact pad which has a soft parylene insulation layer underneath proved to be a very challenging process. Moreover, after the tests to attach the chips on flexible carriers the wire bondings had to be removed and reattached. To eliminate the wire bonding requirement, larger contact pads can be used on the chip, but this solution would increase the chip frame area and overall mass. In order to keep the chip mass low enough on the flexible carrier, an extra outer test frame (Figure 4.10) has been proposed along with a new holder with pogo pin connections Figure 4.11. This frame would carry the pogo pin contact pads and would be connected to the inner frame with 200 µm wide bridges. The bridges would later be broken and the inner frame and the cantilever would be released for membrane integration.

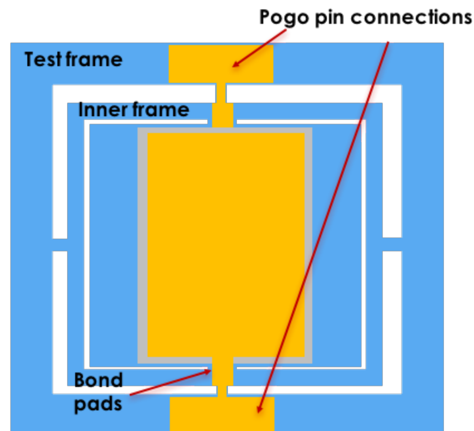


Figure 4.10 Test frame with a larger outer section for electrical connections via pogo pins. The inner frame and the cantilever would later release and used in the acoustic tests.

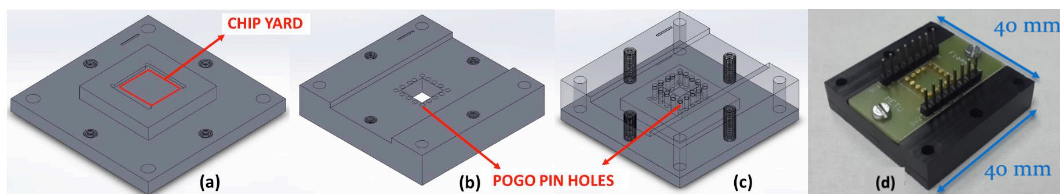


Figure 4.11 New test holder for piezoelectric energy harvesters and transducers with electrical connections via pogo pins.

4.1.5 Device Types

4 different main device types have been prepared with optimum power outputs at different resonant frequencies. Single cantilever and butterfly designs have two different types each (Figure 4.12). Moreover, derivative types with partially covering top electrodes (for power maximization tests) have been included. PZT sizes are extended on the tip mass and fixed base sections to cover the possible undercutting during the DRIE process. Table 4.6 shows the device types and properties included in the mask design.

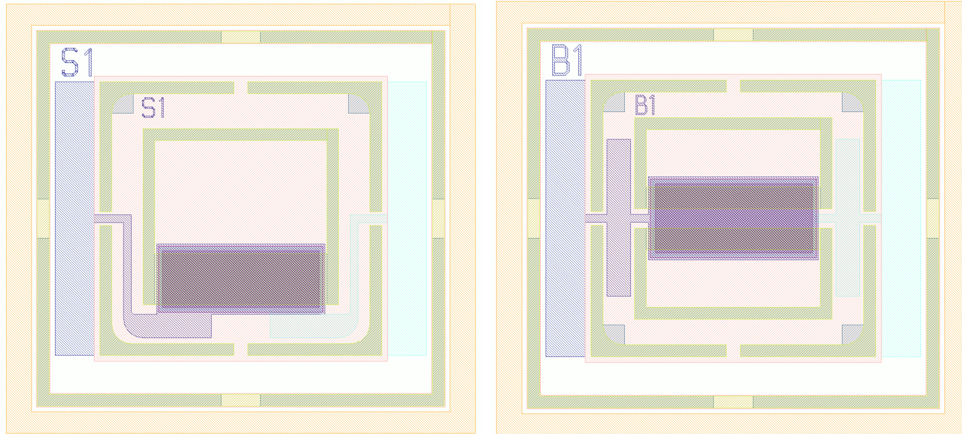


Figure 4.12 (L)Single cantilever and (R) double cantilever (butterfly) harvester designs. Outermost frame size is 12 mm which will be used for shaker tests. Actual harvester chip (with the smaller chip code) is 6 x 6 mm.

Table 4.6 Final device types included in the mask design. **S:** single cantilever, **B:** double cantilever (Butterfly), **P:** partial top electrode (%40)

Type	Tip Mass Length [µm]	Top Electrode Length [µm]	Res. Freq. [kHz]
S1	2900	1500	1
S1-P	2900	600	1
S2	2000	2200	1
S2-P	2000	900	1
B1	1450	2000	3
B1-P	1450	800	3
B2	500	3700	4
B2-P	500	1500	4

4.2 New generation device tests

Vibration tests of 2nd generation devices were done using the new test holder on the shaker table. A data acquisition system with LabView was used for recording measurements automatically. The first vibration test of the single cantilever chip resulted in maximum power output of 2.7 µW at 1 g input acceleration. Figure 4.13 shows the test results. This chip was later used as an acoustic sensor for animal ABR tests of the project [24]. Among the tested devices in the initial batch maximum obtained power for single cantilever chips is **3.3 µW at 820 Hz**, 1 g acceleration.

For the butterfly design **21.4 µW at 3380** Hz 1 g was measured. Figure 4.14 shows the power output w.r.t. resistive load and frequency. Changing the load slightly shifts the resonance frequency with the optimum load of 5 kΩ.

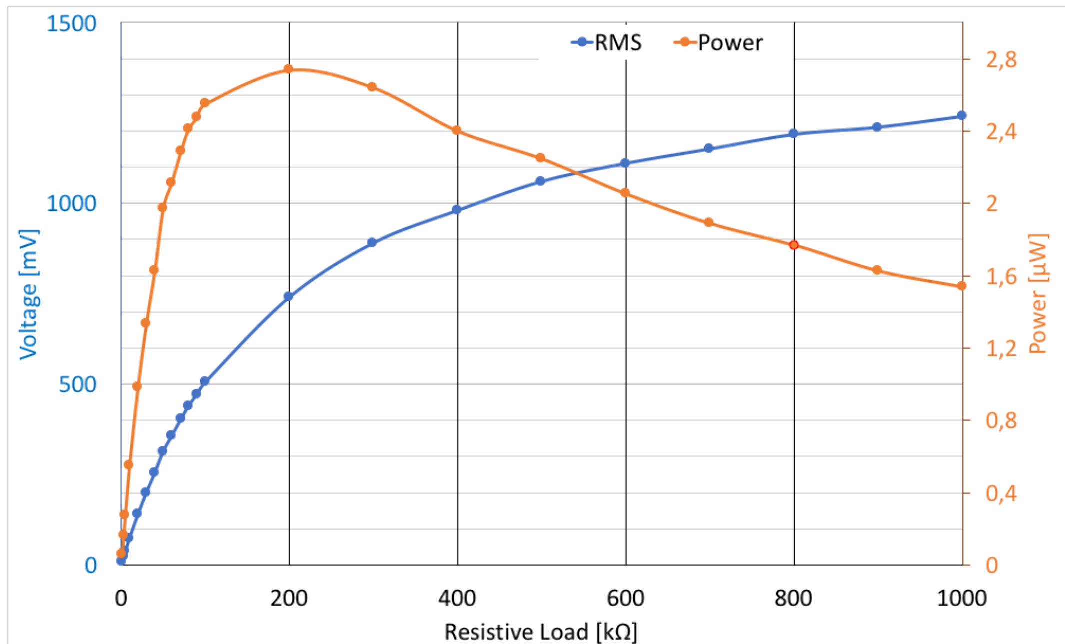


Figure 4.13 Resistance load sweep of single cantilever chip on shaker table at 800 Hz and 1 g input acceleration. Maximum power of 2.75 µW was obtained at 200 kΩ load.

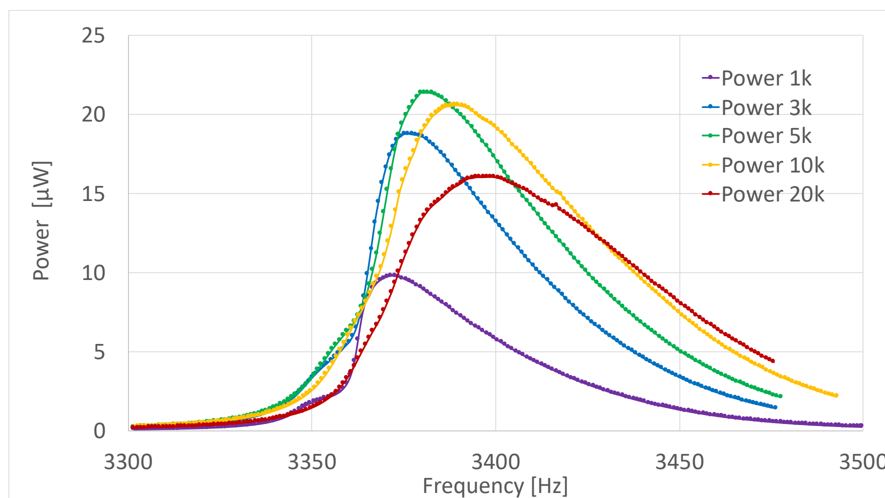


Figure 4.14 Load sweep for maximum power output tests of butterfly chip. maximum output power of 21.4 µW.

After completing the testing of the first batch of devices with healthy top electrodes, we are able to compare performance from three different wafers. Figure 4.15 shows the best matching chip results. Among the three chips, the highest power output (4.04 μW) was obtained from the SOI600-2-A-23 chip. This chip has PZT with In layer coated at ASELSAN and thinned down with lapping at METU-MEMS. The other two chips have In layer coated at MEMS and both have higher resonance frequencies (between 800-900 Hz) and lower power outputs (2.61 and 3.02 μW). This shows that, between lapping and grinding, if the chip can generate output there is no significant performance difference based on the voltage output but the power output is defined by the bonding quality.

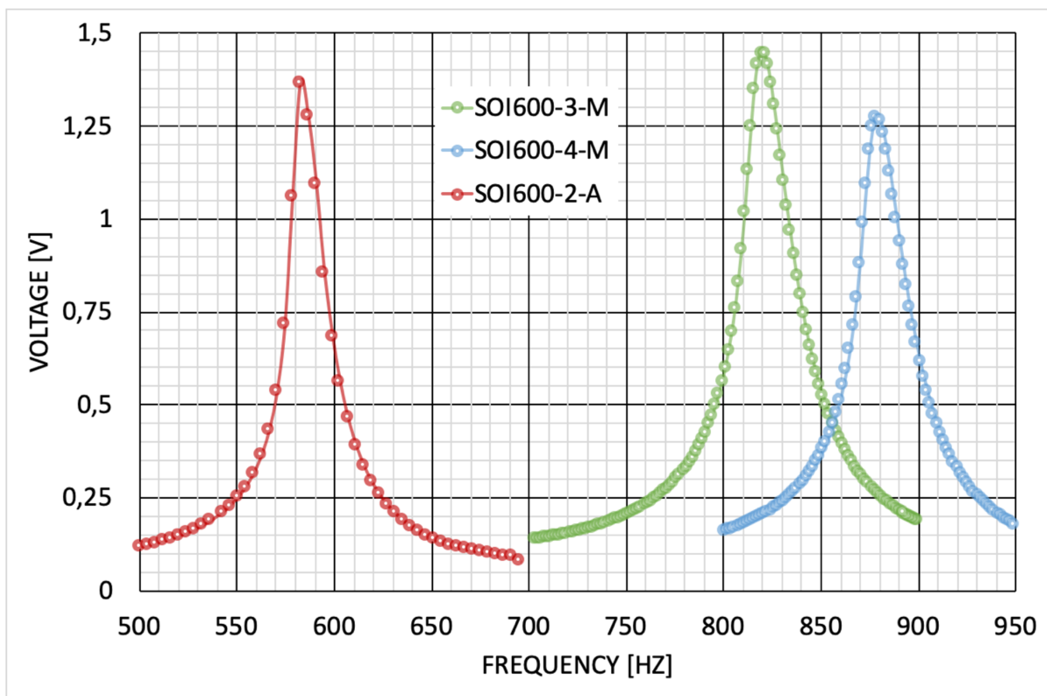


Figure 4.15 Output voltage of the same type chip from three different wafers, SOI600-4-M (Blue), SOI600-3-M (Green) and SOI600-2-A (Red). M: Indium coating at MEMS, A: Indium coating at ASELSAN.

For the second batch of tests, the same procedures were applied. The best chip from the SOI600-2-A wafer (indium coated at ASELSAN, thinning by Lapping at METU-

MEMS) showed the highest power output among all tested devices. The resonance frequency was found to be **2765 Hz** (the design frequency was 3 kHz). The power output test resulted in **61.1 µW** with an optimum load of **10 kΩ**, similar to the tests of the previous batch. Figure 4.16 shows the power output results at the resonance frequency. After the experimental results were obtained, updated simulations were repeated with the corresponding actual chip dimensions. Figure 4.17 shows the comparison of the simulation and experimental results. The simulation resonance frequency was 2944 Hz whereas the experimental resonance frequency was 2765 Hz. The difference may be attributed to the extra layers such as the SiO_2, thin electrodes, and parylene insulation which would affect the vibration characteristic of the device but could not be simulated due to the computational load of the thin layers. The chip provided **81% of the maximum power output** predicted by the simulation. The rest of the power output may be explained by the imperfections in the bonding and the contact resistances of the test setup.

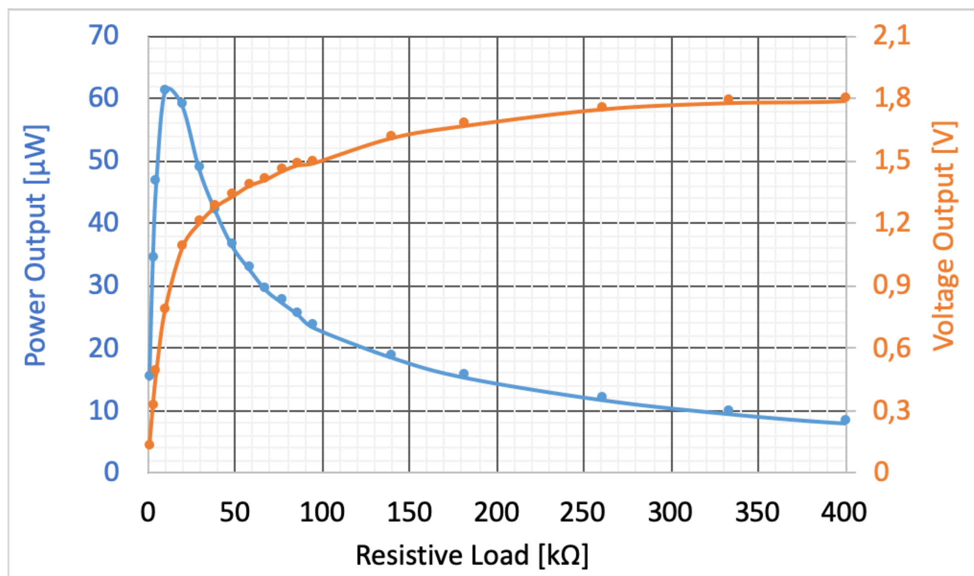


Figure 4.16 SOI600-2-A-45-B1P chip results at 2765 Hz 1 g vibration.

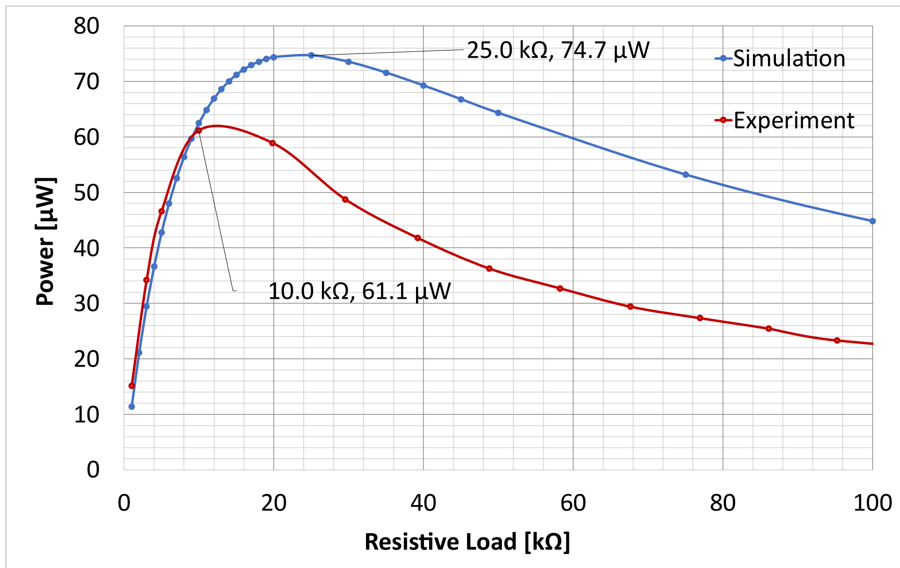


Figure 4.17 Experimental vs. simulation results for the best butterfly chip.

In order to compare the vibration energy harvester performance for cochlear implant applications, one needs to take into consideration the effect of the harvester mass on the ear drum. For this purpose, instead of 'Normalized Power Density', a new figure of merit was derived as 'Specific Power Density'. In this parameter, the power output of the harvester is divided by both the volume and the mass of the harvester to compensate for the mass loading effect. shows the results of our experiments compared with similar studies on piezoelectric harvesters. Because the required information for the calculation of the specific power density is not provided in some studies, only the results available are presented. Compared with the available literature, the top performer **butterfly chip has the highest specific power density**, almost doubling the performance of the nearest study.

Table 4.7 Comparison of the piezoelectric harvester literature.

	Active material	**Active volume (mm^3)**	**Active mass (mg)**	**Input Acc. (g)**	**Freq. (Hz)**	**Power (μW)**	**Normalized Power Density (μW/(mm^3 * g^2))**	**Specific Power Density (μW/(cm^3 *Hz * g^2* mg))**
Morimoto et al. [67]	PZT	4.05	38.9	0.5	126	5.3	5.23	134.6
Durou et al. [44]	PZT 5H	464	1482	0.2	76	13.9	0.75	0.5
Elfrink et al. [68]	AIN	57.4	65.6	1.75	325	85	0.48	7.37
Lei et al. [69]	PZT	18.6	35	1	235	14	0.75	21.5
Aktakka et al. [34]	PZT 5A	27	297	1.5	154	205	3.37	11.6
Beker et al. [19]	PZT 5A	20	28	1.6	470	137.5	2.69	95.9
Kanno et al. [70]	KNN	11.4	28.6	1	1036	1.1	0.10	3.37
Chen et al. [51]	PZT 5H	48.6	447	0.5	101.6	71.8	5.91	13.2
This work	PZT 5A	12	23.7	1	2765	61.1	5.09	**214.8**

4.3 Vacuum and Temperature Effects on Piezoelectric Harvester

Piezoelectric MEMS devices are operated primarily at their first resonance mode. In order to maximize the electrical output from the piezoelectric material, one should minimize the damping on the system. Total damping on the cantilever structure is composed of intrinsic damping due to the thermoelastic losses in the materials, fluidic damping due to the interaction with the surrounding air, and electrical damping due to the external electrical load on the piezoelectric material [68]. Using a vacuum package, the fluidic damping parameter can be reduced. Once the pressure around the cantilever is below 1 mbar, the intrinsic damping dominates the fluidic damping [71] consequently increasing the quality factor of the piezoelectric structure significantly.

Vacuum packaging of the devices would require additional process steps to the manufacturing. In order to evaluate the device performance in vacuum conditions beforehand, unpackaged devices can be tested in a vacuum environment. In previous studies, researchers used large vacuum chambers with the vibration source placed inside the chamber which increases the cost and pumping requirements of the test setup [71], [72]. Here, we tested the vacuum performance of the unpackaged piezoelectric chips using a compact vacuum chamber with probe connections on top of a shaker table. Small chamber volumes enable quick depressurization using a simple vacuum pump and reduce complexity.

Another important parameter to be considered is the temperature dependence of the material properties of ferroelectric materials like PZT [73]. The effect of temperature below the Curie point has been investigated by several studies. Chen et al. [74] showed that as the temperature is increasing between 20°C and 70°C thin film PZT's axial effective piezoelectric coefficient, d_{33eff}, increases but the relative permittivity increases more significantly. This would result in lower voltage and power output with increasing temperature as shown by Kim et al. [75].

This study aims to characterize thin film pulsed laser deposited (PLD) PZT and bulk PZT-5A based transducers in vacuum and temperature conditions suitable for the implantation requirements.

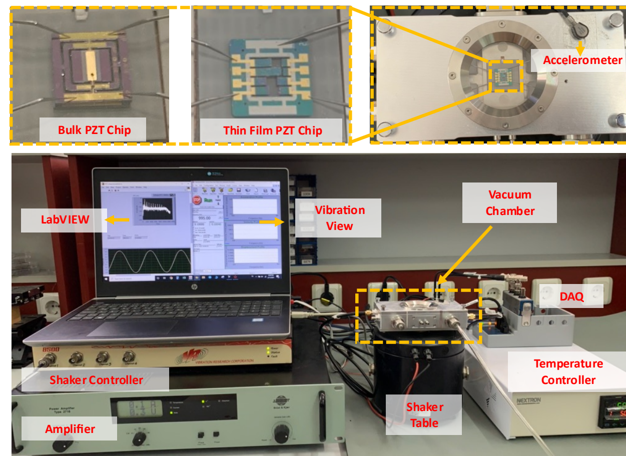


Figure 4.18. Experimental test setup with the compact vacuum chamber and probe connections.

Figure 4.18 shows the overall test setup. A miniature vacuum chamber with a Peltier heater and 4 probe connections (NEXTRON Co. MST-PT) is placed on a shaker table (B&K 4809) controlled by a vibration controller unit (Vibration Research 8500). The feedback accelerometer is fixed on the top lid of the vacuum chamber. The vacuum chamber weighs ~750 gr which enables stable operation on the shaker with up to 5 g acceleration. Output measurements are collected with a data acquisition system (NI CompactDAQ) via LabVIEW 2017. Using a common ground connection, three channel data can be recorded at the same time. A two-stage vacuum pump with mechanical and turbo sections (NanoVAK) is used for pressure setting. A custom temperature controller from NEXTRON sets the surface temperature on the Peltier heater/cooler inside the vacuum chamber. For the temperature range used in the tests (10-50 °C) no extra cooling was needed.

The piezoelectric chips are held in place with the probes. A spacer frame is placed under the chips to accommodate the tip mass movement during vibrations. The chips were placed inside the chamber and tested successively in atmospheric and vacuum

conditions at different temperatures without changing the chip position or breaking the vacuum. Vibration sweeps were done once the temperature reading is steady for 5 minutes between each 10 °C step.

A Bulk PZT-based energy harvester was tested at 1 g input acceleration. Figure 4.19 shows the power output results of the sample chip at the resonant frequency (**vacuum 3452 Hz with a quality factor of 265, atmospheric 3450 Hz with a quality factor of 172**). At the vacuum condition (10^{-3} torr) the maximum power output (**9.2 µW**) increased over two-fold compared with the atmospheric pressure condition (**4.3 µW**). Such an increase in the output is similar to the results of Cao et al [76] with a PVDF-based energy harvester at 2 x 10^2 Pa (2 mbar) pressure. They have also observed similar frequency shift.

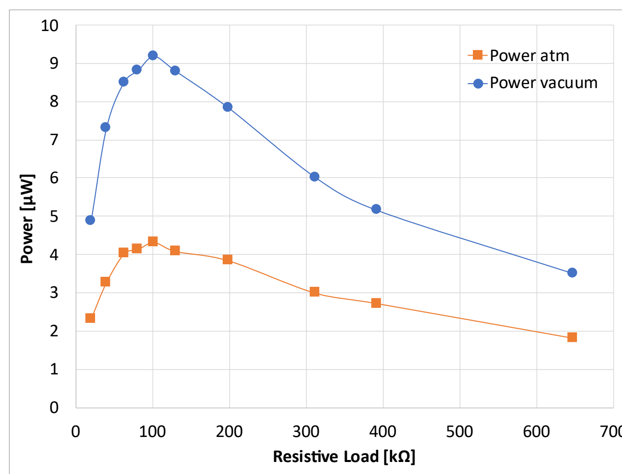


Figure 4.19. Bulk PZT energy harvester power output at 3452 Hz (vacuum) and 3450 Hz (atmospheric) 1 g input acceleration inside the vacuum chamber. Vacuum condition refers to 1 x 10^{-3} torr chamber pressure. 'atm' refers to the atmospheric pressure.

For the temperature tests, bulk PZT harvester and thin film PZT sensor chips were vibrated at 1 g and 0.1 g accelerations, respectively. Figure 4.20 shows the harvester power output results. To observe the rate of change with temperature more clearly, the output power is normalized based on the 20 °C result which is 8.26 µW. As the temperature increased power output decreased in both atmospheric and vacuum

cases, but the rate of change was lower in the vacuum results. This may be due to the lower heat transfer in the vacuum environment, delaying the thermal equilibrium. For the ΔT=40 °C, the power output dropped 2.5% in the vacuum case and 7.9% in the atmospheric case. When the piezoelectric device is used in an implant application, the surrounding body parts will create a uniform temperature profile on the device, therefore one can expect the actual power output drop to be closer to the atmospheric condition. Kim et al. [75] reported a similar drop in power output for both hard and soft PZT materials. Compared to room temperature, the performance drop at 37 °C would be ~5.7%.

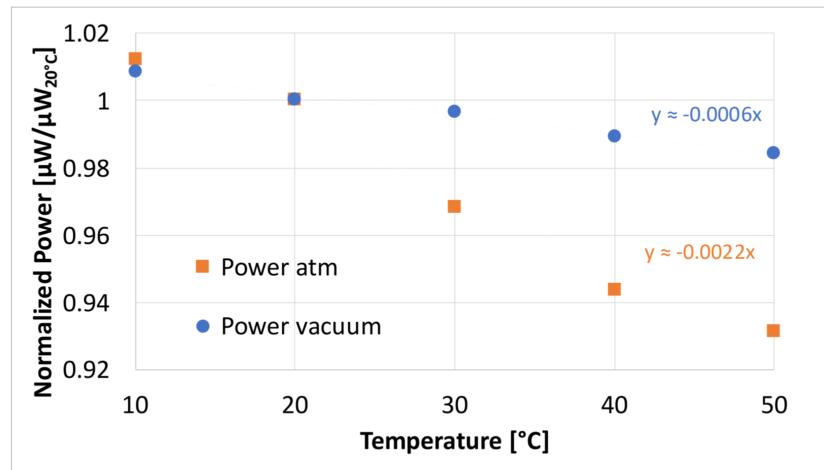


Figure 4.20. Bulk PZT energy harvester power output at 776 Hz 1 g input. Temperature sweeps were done successively at atmospheric pressure and 10^{-3} torr. Power output is normalized based on 8.26 µW at 20 °C.

CHAPTER 5

THIN FILM PZT BASED FABRICATION

As mentioned in Chapter 1, various piezoelectric materials can be used in MEMS applications. Bulk PZT has certain advantages for energy harvesting applications but for sensing applications, the required electrical signal can be on mV levels with the state-of-the-art low-power interface electronics [11], [16], [77]. In such cases, using a bulk PZT-based chip would be excess. Instead, a suitable thin film piezoelectric material can be used to provide necessary signals in a much more compact package.

In the scope of the FLAMENCO project, an 8-channel transducer chip would be fabricated for sensing acoustic signals. Initial idea was to have both the piezoelectric energy harvester and transducer chips fabricated using the bulk PZT fabrication process that has been developed. Figure 5.1 shows the stacked cantilever structure in the proposal. This method has the advantage of a single-type fabrication process. But the stacked structure with 4-5 layers would put a large load on the vibrating eardrum. Already fabricated piezoelectric energy harvester chips have a mass of 30 mg on average. Stacking several of those would result in a mass excess of 100 mg.

In the literature, there are vibration measurements on the ear drum. Young et al measured the ear drum vibration at different input sound levels with a laser Doppler vibrometer and a commercial accelerometer [64]. The accelerometer (ADXL320) has a mass of 50 mg, therefore the results give us an idea about what a piezoelectric energy harvester's effect may be. Figure 13 shows the umbo acceleration measurements with both instruments. It is seen that; the accelerometer mass decreases the acceleration more than 10-fold. The authors commented on this effect and suggested that no more than 20 mg load should be applied on the eardrum for high acceleration. Therefore, the stacked structure in our concept should have no more than 20 mg mass.

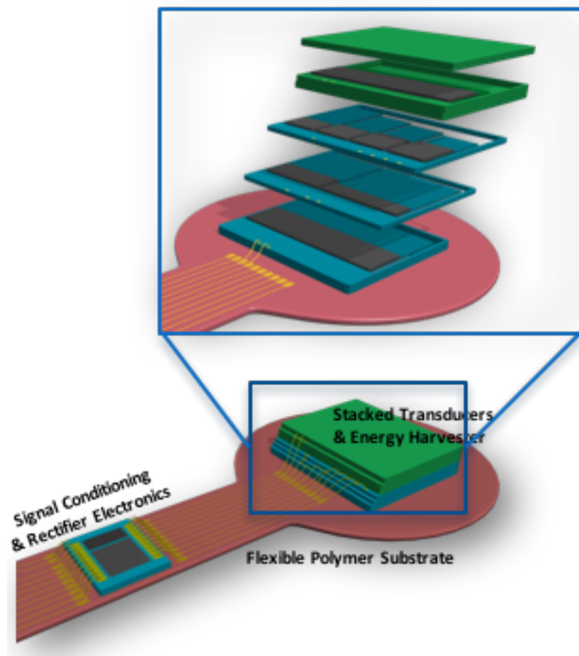


Figure 5.1. Original FLAMENCO concept for energy harvester and transducer cantilevers. All chips were fabricated with bulk PZTs and stacked together [18].

The easiest way to reduce the mass of the transducers is by using only a single layer with smaller cantilevers. This would mean smaller piezoelectric material and a smaller output signal, but the transducer is only used for sensing purposes. State-of-the-art neural stimulation circuits require only 100s of µV for sensing the incoming sound [3]. Therefore, using a smaller thin film piezoelectric layer would still work as a transducer.

Considering the alternative thin film piezoelectric materials, a commercial solution was chosen to eliminate extra processing and guarantee the material's performance. Solmates B.V. is a firm producing Pulsed-Laser-Deposited (PLD) PZT. It has high piezoelectric coefficients compared with other thin film materials such as AlN. PLD-PZT is grown at wafer level on platinum electrodes at high temperatures (>600 °C).

Figure 14 shows the updated fabrication flow which would eliminate the first 3 steps of bulk PZT fabrication including bonding and lapping. The rest of the fabrication follows the same processes. The following sections provide the details of the process

developments for thin film PZT wet etching and Pt wet etching for bottom electrode patterning.

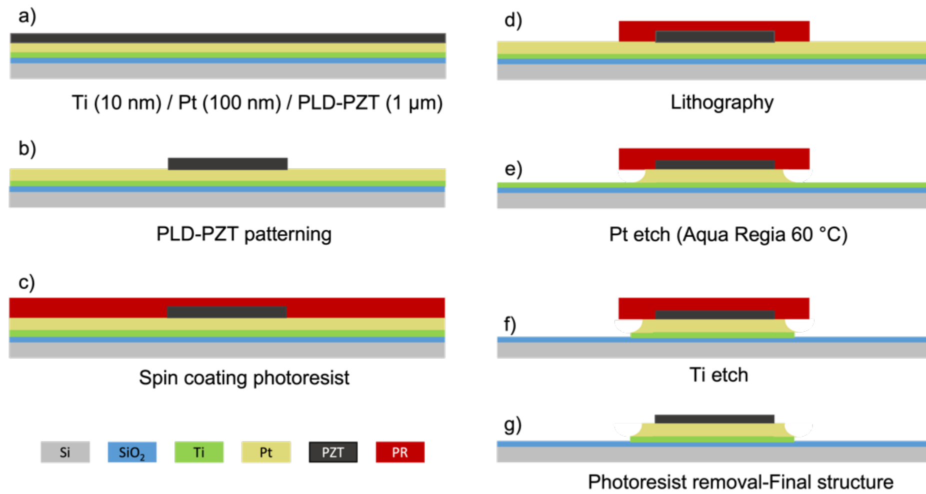


Figure 5.2. The fabrication process of PLD-PZT structures with a Pt bottom electrode: (a) Si wafer with 50 nm thick SiO2 thermal oxide passivation, (b) PLD-PZT thin film patterning with wet etchant provided by Solmates B.V., (c) spin coating photoresist, (d) Pt wet chemical etching in hot Aqua Regia (60 ˚C) (e) wet etching of Ti (1:1:638 vol H2O2:HF:DI, at room temperature) and (f) photoresist removal.

5.1 PZT patterning

PZT patterning was done with a custom wet etching formula ($HF+HNO_3+NH_4$ for etching, H_2SO_4 for cleaning) provided by the manufacturer (Solmates B.V.). For the lithography process, the same mask set is used as the bulk PZTs only with an image reversible photoresist (AZ5214). During tests, the etchant recipe sent by the manufacturer was updated for a more repeatable etching rate. In the original recipe, the base (Ammoniac) was used in higher concentrations. In our first trials, etching solution with high concentration ammoniac resulted in very slow etching rates at only 50-60°C. Etching solution without the ammoniac, etch the thin film PZT (120 nm) very aggressively, cleaning the surface after just one cycle.

After adding one-quarter of the originally suggested ammoniac amount, the first test wafer with a 400 nm PZT layer was etched. Just one cycle (5 s etching – 5 s cleaning) was enough, giving an etch rate of **80nm/s**, slightly faster than the original goal of 50nm/s. Figure 5.3 shows the alignment marks of the test wafers showing the undercutting.

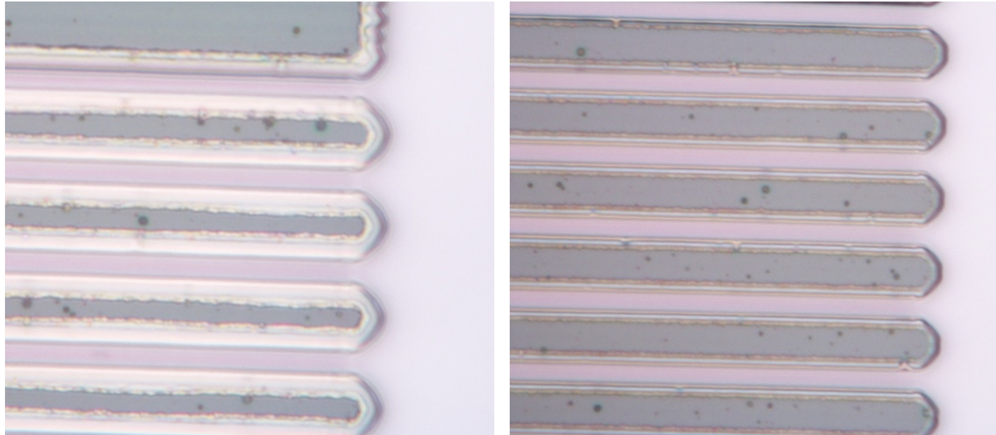


Figure 5.3. (Left) 400 nm PZT etching with an only acid solution. Undercutting is ~1.5µm (Right) 400 nm PZT etching with 80ml ammoniac addition. Undercutting is ~500nm. Alignment marks are 5µm wide.

For the actual 1µm PZT process wafers a fresh solution was prepared with one-quarter of the original ammoniac concentration. With this etching solution, 1µm film was etched in 2.5 cycles (5+5+3 s). Figure 5.4 shows the two wafers' alignment marks. Since the film thickness is larger corresponding undercutting was also larger.

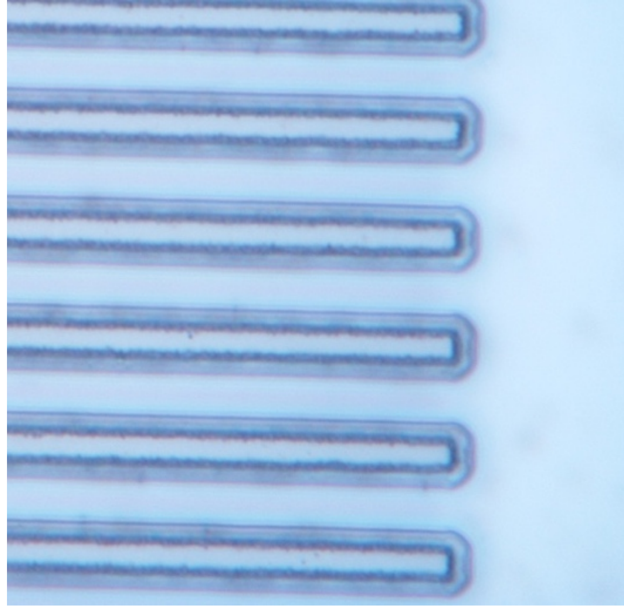


Figure 5.4. 1µm PZT etching with a fresh etchant. Undercutting is ~1.5µm. Alignment marks are 5µm wide

5.2 Pt Etching

Growing pulsed laser deposition (PLD) lead zirconate titanate (PZT) which is performed at temperatures in the range of 600 – 800 ˚C [78] requires a compatible bottom electrode layer. Platinum (Pt) is a good fit for this high-temperature process owing to its high melting point (1768 ˚C) and has inert nature that can prevent oxidation and diffusion-related issues when employed as an electrode material. It is commonly used in similar applications such as thin film heaters and temperature sensors [79].

For the fabrication of acoustic transducers, the bottom electrode layer should be patterned after the PZT etching. Due to the inert nature of Pt, it is one of the most difficult materials to pattern with standard etching techniques [80]. In many studies, the lift-off method is used to create relatively large Pt patterns on a standard photoresist mold [81], [82]. Alternative bottom-up approaches such as selective deposition with microcontact printing [83] or atomic layer deposition (ALD) methods [84] were also utilized. Such bottom-up processes are not applicable for

patterning Pt electrodes of PZT transducers, since the PLD-PZT thin film quality is dependent upon the kinetics of the growth on a continuous Pt seed layer [78]. When PZT/Pt stack is used in the production of MEMS structures, the selective etching of Pt becomes a requirement after the PZT deposition and patterning, while protecting the integrity of the underlying structures. The etching process should also be conducted below the Curie temperature of the piezoelectric material (<200 °C) to retain the polarization of the piezoelectric layer.

Etching methods are mainly divided into dry and wet etch processes. Plasma-based dry etching methods such as Ar+ ion beam milling [85], and inductively coupled plasma etching [86]–[88] were used and demonstrated in the literature for successful patterning of Pt. Other than the required expensive machinery, the main drawbacks of plasma-based etching methods are possible back sputtering of material on the sidewalls [87] and high process temperature (160-220 °C) for sub-micron resolution structures [88]. An alternative etching process is using supercritical carbon dioxide fluids with hexafluoroacetylacetone at 220 °C [89]. Since the carbon dioxide is vaporized upon depressurization, this method is also categorized as 'dry etching', but the high process temperature makes it unsuitable for PZT transducers.

The most commonly known etchant for noble metals, Aqua Regia [90]–[92] is used for directly etching Pt at 60-90 °C. The bottleneck of such a process is the selection of a suitable masking layer that can withstand harsh chemicals. Previously hot Aqua Regia etching of Pt was reported with a Cr hard mask [90] and some thin film photoresists [91]. When patterning Pt in a multilayer structure, removal of the Cr mask after Pt etching might cause exfoliation of the underneath layers that are sensitive to Cr etchant such as PZT [93]. Thin photoresist masking may be used in processes with planar substrates, but it would result in poor edge coverage for the surface topography of PZT structures with 1 μm or higher thickness.

In this study, patterning of the Pt electrode layer of PLD-PZT structures was done using hot Aqua Regia wet chemical etching with a compatible thick photoresist masking layer. This method solves both the process temperature and hard mask

material problems of the previous studies while providing protection for the PZT transducer.

Two types of thick photoresists (MicroChemicals AZ® 9260 [94] and Megaposit SPR™ 220-7 [95]) that are available in our cleanroom were used for the tests. Thick films of the photoresists were spin-coated in order to protect the edges of underlying piezoelectric materials. AZ® 9260 is a high-resolution, high aspect ratio photoresist, usually used as a masking layer in electroplating and deep dry etching processes. Film thicknesses from 4 µm up to 24 µm can be obtained with aspect ratios of ~5. Similar film thicknesses, in the range of 5-10 µm, can be obtained using SPR™ 220-7. Both photoresists have good adhesion for plating and wet etch applications which can be further improved with hard baking after the development step.

Two groups of samples were used to optimize the wet etch process. The first group of samples consisting of Si/Ti/Pt layers without PLD-PZT was used to test and optimize the etch rate and undercut of SPR™ 220-7 and AZ® 9260 photoresists. 10 nm Ti adhesion layer and 100 nm Pt layer were sputtered on 4” silicon test wafers in an Ar+ atmosphere using a sputtering system (AJA International). Table 5.1 lists the lithography parameters used for the test wafers. Oxygen plasma cleaning was reported to produce a passivation layer on Pt thin film that has adverse effects during wet chemical etching (i.e. longer or no etching), therefore, it was not used after the lithography process [90]. To remove any residuals or passivation layer present on the Pt thin film due to previous processing, Ar plasma cleaning can be applied. For the initial tests, no plasma cleaning was used.

Table 5.1 Parameters of thick photoresist lithography process on Pt-coated test wafers.

Resist Type	AZ® 9260	SPR™ 220-7
Film Thickness	18 µm	8 µm
Spin Speed	1000 rpm	3000 rpm
Soft Bake	Ramp up RT* to 95 ˚C 10 min 95 ˚C 40 min in oven	115 ˚C, 2 min on hot plate
Rehydration	Overnight	None
Exposure Energy	840 mJ/cm^2	630 mJ/cm^2
Development	15 min AZ826MIF	2 min MF 24-A
Hard Bake	Ramp up RT* to 110 ˚C 10 min 110 ˚C 20+20 min in oven	Ramp up RT* to 110 ˚C 10 min 110 ˚C 20+20 min in oven

**RT: Room Temperature*

Second group of samples was received from Solmates B.V., Netherlands. Stacks of 50 nm SiO_2, 10 nm Ti, 100 nm Pt and 1 µm thick PLD-PZT on Si wafers were used for the microfabrication of PZT transducers.

Aqua regia solution (3:1 HCl:HNO_3, 400 ml total) was prepared in a glass beaker under a ventilated hood. The solution was then heated up to 60 ˚C on a hot plate. As the solution is heated, a large amount of very aggressive etchant vapor is produced. Therefore, extra care must be taken for protecting hot plate equipment and cables. A glass or Teflon lid can be used to prevent the leakage of the vapor allowing a better working condition. Wafers were placed in the solution horizontally using a Teflon holder. Orange colored etching solution was transparent, letting observation of color changes on the wafer surface to determine the etching time. No agitation was applied during the etching. To prevent the passivation of Pt, test wafers were kept in the etch solution until the Pt layer was completely removed from the surface. The first group of samples was processed in the Aqua Regia solution for testing the photoresist durability with no Ar plasma cleaning beforehand. After 10 minutes, local Pt removal became visible, and etching is completed in 15 minutes with no metallic-colored Pt left on the surface. After the Pt layer was removed, the wafer and holder were rinsed in the DI water tank during the cleaning cycle. Since the etchant solution became saturated, a fresh solution was prepared after two wafers.

To reduce the etching time, Ar plasma cleaning was applied for 30 seconds in a back-sputtering system (Bestec GmbH) before the wet etch process. The plasma treatment removed any passivation layer on the Pt and decreased the etching time to 3 minutes and 45 seconds.

Both photoresists (AZ® 9260 and SPR™ 220-7) were hard-baked for 20 minutes initially. After 15 minutes in the Aqua Regia solution at room temperature, extreme degradation occurred on both resist surfaces. Figure 5.5 and Figure 5.6 show the degradation on AZ® 9260 and SPR™ 220-7 surfaces respectively.

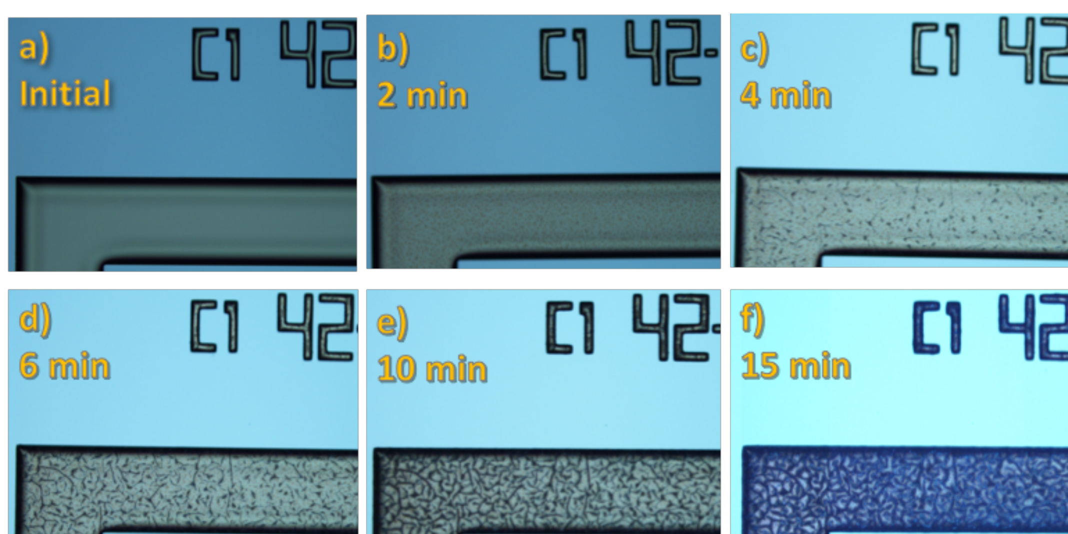


Figure 5.5. Thick resist layer (AZ9260, 18µm) degradation in aqua regia solution. (a-e) The etching solution was at room temperature, (f) 5 minutes more at 40°C.

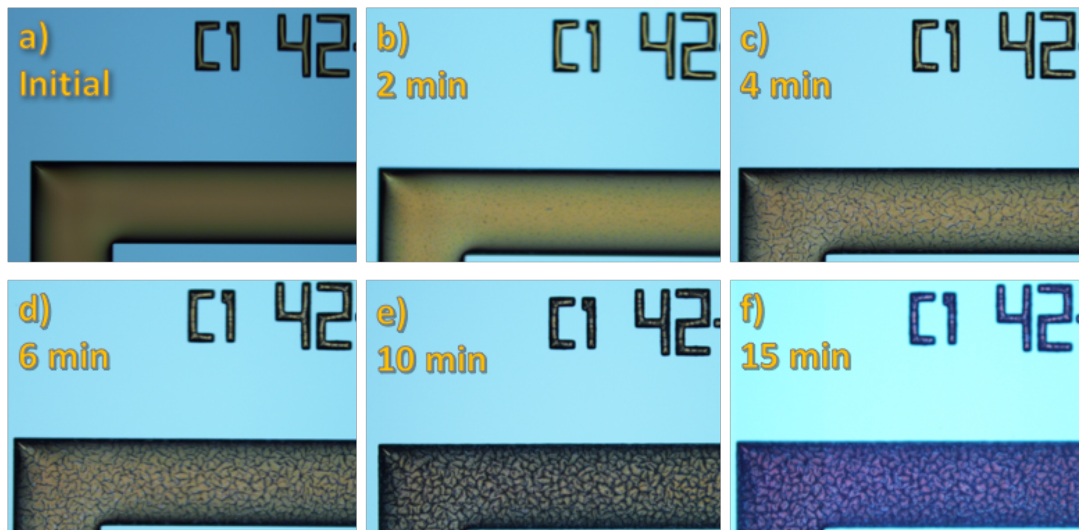


Figure 5.6 Thick resist layer (SPR220-7, 8µm) degradation in aqua regia solution. (a-e) The etching solution was at room temperature, (f) 5 minutes more at 45°C.

To increase the stability of the photoresist layers following sample wafers were hard-baked in the oven for an extra 20 minutes (40 minutes in total). With the longer hard bake time, AZ® 9260 surface was slightly degraded while SPR™ 220-7 had a smooth surface after 15 minutes of etchant treatment. Figure 5.7 shows the optical microscope view of the photoresist surfaces after each test and the cross-sectional view of the SPR™ 220-7 pattern. Significant delamination at the photoresist edge was observed after 15 minutes etching process which results in increased undercutting. Figure 5.8 shows the corresponding SEM images and EDS analysis after photoresist stripping in acetone. In both cases, the Pt layer is completely etched but SPR™ 220-7 yielded better results with straight edges and less undercut.

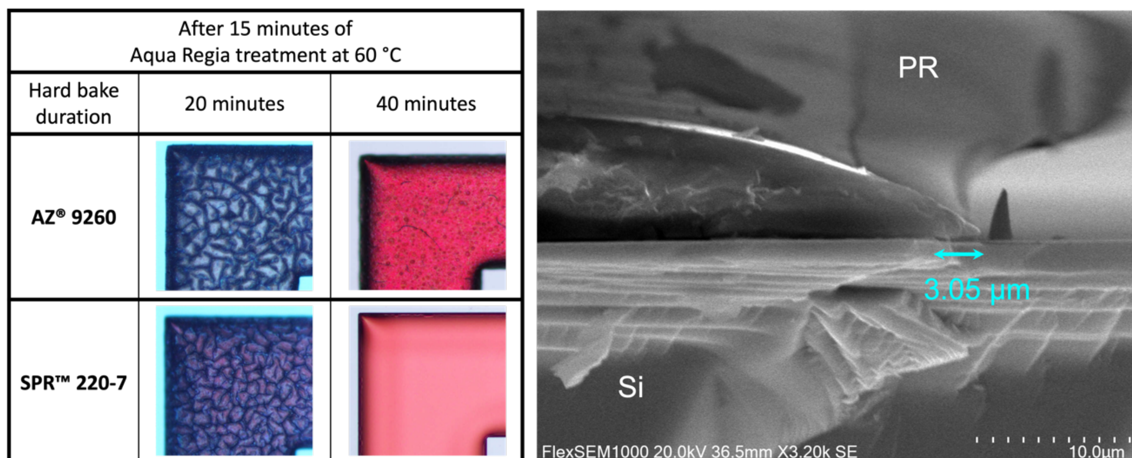


Figure 5.7 (Left) AZ® 9260 and SPR™ 220-7 degradation in Aqua Regia solution after 15 minutes. (Right) Edge delamination on SPR™ 220-7 pattern after etching.

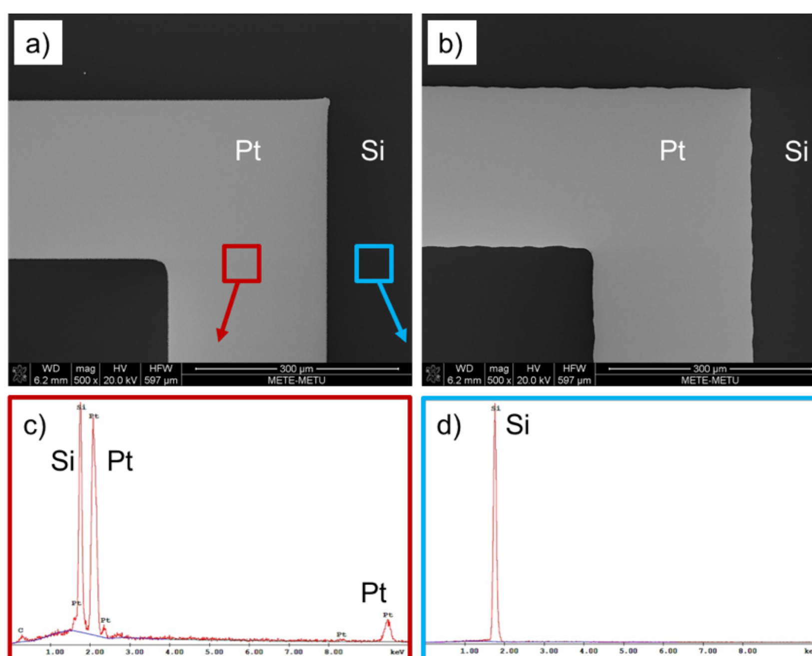


Figure 5.8 SEM images of patterned Pt layers with (a) SPR™ 220-7, (b) AZ® 9260. (c) and (d) show the EDS analysis of masked and etched areas of Pt film of (a), respectively.

The amount of undercutting defines the minimum obtainable feature size of the final pattern of the Pt film. The undercutting depends on the photoresist adhesion to the surface and increases with the etching duration. In the Aqua Regia etching tests with non-plasma cleaned samples, on average AZ® 9260 had ~7.2 µm undercutting while

SPR™ 220-7 had ~3.5 µm undercutting of Pt. The SPR™ 220-7 had less surface degradation, but the undercutting is much higher than the thickness of the Pt film (100 nm) due to the delamination of the edges during the 15 minutes of etching. Ar plasma descum was applied to clean the Pt surface to be etched, therefore reducing the etching time. With this process, the etching time was decreased to 3 minutes 45 seconds and consequently, the undercutting was less than 1 µm. Figure 5.9 shows the undercutting performance of etching with and without Ar plasma cleaning.

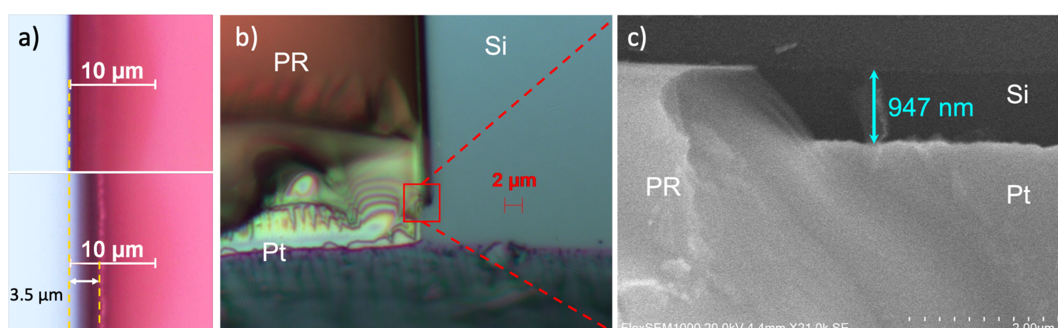


Figure 5.9 Pt etching with 40 min. hard baked SPR™ 220-7 masking layer. (a) Optical microscope view of 3.5 µm undercutting of Pt after 15 minutes of etching in Aqua Regia at 60 ˚C (no plasma cleaning). (b) Optical microscope view of line pattern on a broken sample after Ar plasma cleaning and 3:45 minutes of etching. (c) Close-up SEM view in of -b- showing less than 1 µm undercut.

Based on the results of the first group of wafers, the second group of PLD-PZT coated samples were processed with SPR™ 220-7 and hard-baked for 40 minutes. The same etching cycles were applied as the test wafers with and without Ar plasma cleaning. After photoresist removal, no damage on the PZT surfaces of either wafer was observed. Figure 5.10 shows the SEM image of the PZT and Pt layers on the silicon wafer after the transducer fabrication process is completed.

Table 5.2 lists Pt wet etching processes in the literature. Compared with the previous studies, the present method provides the best minimum feature size of Pt patterns using an easily removable photoresist masking layer, meanwhile protecting the PZT layer underneath.

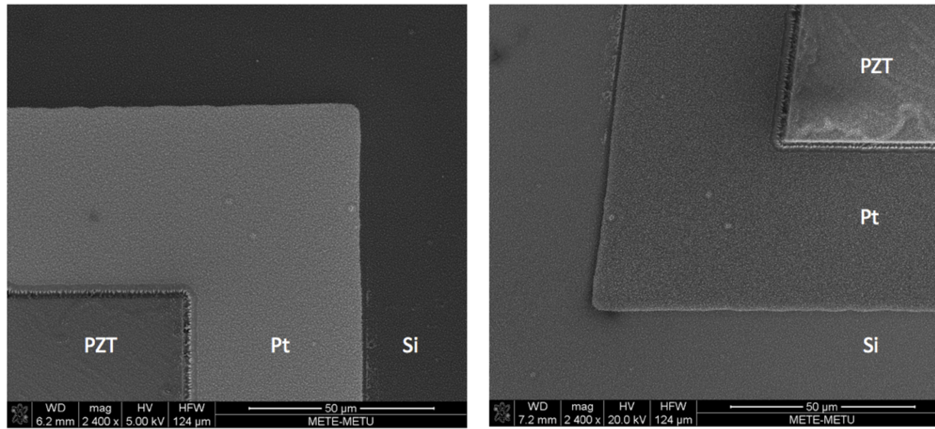


Figure 5.10 SEM view of the thin film PLD-PZT layer with Pt bottom electrode after transducer fabrication is completed. Note that some of the residual left around the PZT and Pt edges is due to the successive patterning of insulation and electrode layers of the transducers.

5.3 Thin film PZT Based Transducer Results

Based on the developed fabrication flow, thin film PZT based acoustic transducers were fabricated and tested. Initial test results with the single channel transducers showed a very high sensitivity of 391.9 mV/Pa @ 900 Hz [22]. Utilizing an updated multichannel transducer design, a sensitivity range of 25.79 to 2.93 mV/Pa was obtained for channels 300 Hz to 5 kHz respectively [21]. After the vibration tests of the chips, it was shown that the output of the piezoelectric devices was 89% of the expected simulation results which confirms the intact piezoelectric characteristics of the thin film PLD PZT material.

Table 5.2 Comparison of wet chemical etching procedures used for Pt patterning with the present study.

Source	**Etchant**	**Temp. [˚C]**	**Masking Material**	**Pt Thick. [nm]**	**Avg. Etch Time**	**Min. Feat. Size***	**Notes**
Liu et al.[91]	Aqua Regia HCl, HNO_3 (3:1)	80	Photoresist AZ® 1518	100	90 s	~4 µm	Dilute HF cleaning
Zaborowski et al. [96]	H_2SO_4: H_2O_2	130	Ti	65	~300 s	~4 µm	650 °C Annealing step for Ti-Pt alloy
Kollensberger et al. [90]	Aqua Regia HCl, HNO_3 (3:1)	60	Cr	410	185 s	5 µm	Ar plasma cleaning before etching
Meier et al. [97]	HCl: H_2O_2	>50	Al	400		~1 µm	350 °C Annealing step for Al-Pt alloy
Koyuncuoglu et al. [98]	Aqua Regia HCl, HNO_3 (3:1)	**60**	Photoresist AZ® 9260, SPR™ 220-7	100	900 s	7 µm	No plasma cleaning
					225 s	**1 µm**	Ar plasma cleaning before etching

*Approximate minimum feature size values are extracted from microscope figures of the respective articles.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

Fully implantable cochlear implants (FICI) are the next-generation bionic ears that will enable patients with profound hearing loss to hear again without the current disadvantages of cochlear implants.

In this study, a high-performance piezoelectric energy harvester for cochlear implant applications has been designed, fabricated, and tested. Piezoelectric energy harvesting method was chosen due to its high power density. The proposed devices are designed based on the developed bulk PZT fabrication process. The performance of the fabricated chips were tested under both acoustic and mechanical vibration. As an alternative fabrication method, thin film PZT based fabrication process was developed for acoustic tranducer applications. Together the energy harvester and the tranducers will form a single package, providing signal and power to the implant from acoustic input.

The following sections provide a summary of the achievements and recommendations for the continuation of the study.

6.1 Summary of Contributions

In the scope of this thesis:

1- The highest energy density acoustic energy harvester solution has been shown based on an ear model and acoustic excitation with a small enough chip that can be implanted into the middle ear.
2- A novel energy harvester design has been proposed. The concept was simulated and fabricated using the developed high-yield fabrication process.

The resultant chip produced the highest specific power density among similar studies in the literature.

3- A new FOM for the energy harvesters placed on base structures with equivalent masses has been defined to correctly analyze the effect of ear drum vibration with an energy harvester chip attached before any in vivo experiments.

4- An alternative fabrication flow based on thin film piezoelectric material has been developed and used for acoustic transducer fabrication. A Pt wet chemical etching process in hot Aqua Regia at 60 ˚C using a thick photoresist mask is presented. The process is suitable for patterning Pt electrode layers of thin film PZT structures while conserving the piezoelectric properties of the material.

6.2 Recommendations for Future Work

Although the design and fabrication of piezoelectric energy harvesters and transducers were completed successfully, an actual implantation operation on a real patient requires many further studies. Here are some recommendations for the next steps in realizing the FICI concept.

1. Main requirement for implantation in patients is the biocompatibility of the final device. For this purpose, biocompatible packaging of the energy harvester and transducer chips, similar to the fabricated parylene carrier structures, should be developed. Considering the performance enhancement with the vacuum experiments, vacuum packaging will be preferable for high-performance operation.

2. In scope of the clinical approvement procedures, *in vivo* experiments of the packaged harvesters should be done to verify the performance experimentally.

3. Since the cochlear implants are surgically placed into the patients ear, it is not easily accessible for repairs or replacements. With the FICI concept, this would be an even bigger issue due to the integrated structure of all the sensors and circuits. Therefore, the long-term and edge-case performance of the energy harvesters should be tested and verified.

REFERENCES

[1] H. Beck *et al.*, “50th Anniversary of the First Successful Permanent Pacemaker Implantation in the United States: Historical Review and Future Directions,” *Am. J. Cardiol.*, vol. 106, no. 6, pp. 810–818, Sep. 2010, doi: 10.1016/J.AMJCARD.2010.04.043.

[2] H. Ouyang *et al.*, “Symbiotic cardiac pacemaker,” *Nat. Commun. 2019 101*, vol. 10, no. 1, pp. 1–10, Apr. 2019, doi: 10.1038/s41467-019-09851-1.

[3] D. Magis and J. Schoenen, “Advances and challenges in neurostimulation for headaches,” *Lancet Neurol.*, vol. 11, no. 8, pp. 708–719, Aug. 2012, doi: 10.1016/S1474-4422(12)70139-4.

[4] M. K. Cosetti and S. B. Waltzman, “Cochlear implants: current status and future potential,” *Expert Rev. Med. Devices*, vol. 8, no. 3, pp. 389–401, May 2011, doi: 10.1586/ERD.11.12.

[5] F. G. Zeng, S. Rebscher, W. Harrison, X. Sun, and H. Feng, “Cochlear implants: system design, integration, and evaluation,” *IEEE Rev. Biomed. Eng.*, vol. 1, pp. 115–142, 2008, doi: 10.1109/RBME.2008.2008250.

[6] W. H. O. (WHO, “WORLD REPORT ON HEARING WEB ANNEXES,” 2021, Accessed: Apr. 14, 2022. [Online]. Available: http://apps.who.int/bookorders.

[7] B. O. Olusanya, A. C. Davis, and H. J. Hoffman, “Hearing loss grades and the International classification of functioning, disability and health,” *Bull. World Health Organ.*, vol. 97, no. 10, p. 725, Oct. 2019, doi:

10.2471/BLT.19.230367.

[8] Cochlear Inc., “How Do Cochlear Hearing Implants Work? | Cochlear.” https://www.cochlear.com/us/en/home/diagnosis-and-treatment/how-cochlear-solutions-work/cochlear-implants/how-cochlear-implants-work (accessed May 10, 2022).

[9] N. Institute on Deafness and O. Communication Disorders, “What is a cochlear implant?,” Accessed: Apr. 14, 2022. [Online]. Available: https://www.nidcd.nih.gov/directory.

[10] F. G. Zeng, “Cochlear implants: Why don’t more people use them?,” *Hear. J.*, vol. 60, no. 3, pp. 48–49, 2007, doi: 10.1097/01.HJ.0000286715.37618.C1.

[11] M. Yip, R. Jin, H. H. Nakajima, K. M. Stankovic, and A. P. Chandrakasan, “A fully-implantable cochlear implant SoC with piezoelectric middle-ear sensor and arbitrary waveform neural stimulation,” *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 214–229, Jan. 2015, doi: 10.1109/JSSC.2014.2355822.

[12] W. H. Ko *et al.*, “Studies of MEMS acoustic sensors as implantable microphones for totally implantable hearing-aid systems,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 5, pp. 277–285, 2009, doi: 10.1109/TBCAS.2009.2032267.

[13] D. J. Young, M. A. Zurcher, M. Semaan, C. A. Megerian, and W. H. Ko, “MEMS capacitive accelerometer-based middle ear microphone,” *IEEE Trans. Biomed. Eng.*, vol. 59, no. 12, pp. 3283–3292, 2012, doi: 10.1109/TBME.2012.2195782.

[14] D. Calero, S. Paul, A. Gesing, F. Alves, and J. A. Cordioli, “A technical

review and evaluation of implantable sensors for hearing devices," *Biomed. Eng. Online*, vol. 17, no. 1, Feb. 2018, doi: 10.1186/S12938-018-0454-Z.

[15] P. P. Mercier, A. C. Lysaght, S. Bandyopadhyay, A. P. Chandrakasan, and K. M. Stankovic, "Energy extraction from the biologic battery in the inner ear," *Nat. Biotechnol.*, vol. 30, no. 12, pp. 1240–1243, Dec. 2012, doi: 10.1038/NBT.2394.

[16] H. Ulusan, A. Muhtaroglu, and H. Kulah, "A Sub-500 μ W Interface Electronics for Bionic Ears," *IEEE Access*, vol. 7, pp. 132140–132152, 2019, doi: 10.1109/ACCESS.2019.2940744.

[17] D. Accoto, M. Calvano, D. Campolo, F. Salvinelli, and E. Guglielmelli, "Energetic analysis for self-powered cochlear implants," in *Proceedings of the 31st Annual International Conference of the IEEE Engineering in Medicine and Biology Society: Engineering the Future of Biomedicine, EMBC 2009*, 2009, pp. 4860–4863, doi: 10.1109/IEMBS.2009.5332449.

[18] "FLAMENCO: A Fully-Implantable MEMS-Based Autonomous Cochlear Implant." https://flamenco.metu.edu.tr/ (accessed Feb. 01, 2022).

[19] L. Beker, O. Zorlu, N. Goksu, and H. Kulah, "Stimulating auditory nerve with MEMS harvesters for fully implantable and self-powered cochlear implants," *2013 Transducers Eurosensors XXVII 17th Int. Conf. Solid-State Sensors, Actuators Microsystems, TRANSDUCERS EUROSENSORS 2013*, pp. 1663–1666, 2013, doi: 10.1109/TRANSDUCERS.2013.6627104.

[20] A. Koyuncuoğlu *et al.*, "Bulk PZT Cantilever Based MEMS Acoustic Transducer for Cochlear Implant Applications," *Proceedings*, vol. 1, no. 10, p. 584, 2017, doi: 10.3390/proceedings1040584.

[21] M. B. Yuksel, A. Koyuncuoglu, and H. Kulah, “Thin-Film PZT-Based Multi-Channel Acoustic MEMS Transducer for Cochlear Implant Applications,” *IEEE Sens. J.*, vol. 22, no. 4, pp. 3052–3060, Feb. 2022, doi: 10.1109/JSEN.2021.3130953.

[22] B. İlik, A. Koyuncuoğlu, Ö. Şardan-Sukas, and H. Külah, “Thin film piezoelectric acoustic transducer for fully implantable cochlear implants,” *Sensors Actuators, A Phys.*, vol. 280, pp. 38–46, 2018, doi: 10.1016/j.sna.2018.07.020.

[23] S. Chamanian, H. Ulusan, A. Koyuncuoglu, A. Muhtaroglu, and H. Kulah, “An Adaptable Interface Circuit with Multistage Energy Extraction for Low-Power Piezoelectric Energy Harvesting MEMS,” *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2739–2747, Mar. 2019, doi: 10.1109/TPEL.2018.2841510.

[24] H. Kulah *et al.*, “A Fully-Implantable Mems-Based Autonomous Cochlear Implant,” *IEEE Symp. Mass Storage Syst. Technol.*, vol. 2022-January, pp. 396–399, 2022, doi: 10.1109/MEMS51670.2022.9699689.

[25] F. Duck, “‘The Electrical Expansion of Quartz’ by Jacques and Pierre Curie:,” *http://dx.doi.org/10.1179/174227109X12500830049951*, vol. 17, no. 4, pp. 197–203, Nov. 2009, doi: 10.1179/174227109X12500830049951.

[26] J. F. Tressler, S. Alkoy, and R. E. Newnham, “Piezoelectric Sensors and Sensor Materials,” *J. Electroceramics*, vol. 2, no. 4, 1998.

[27] A. Jain, K. J. Prashanth, A. K. Sharma, A. Jain, and R. P.n, “Dielectric and piezoelectric properties of PVDF/PZT composites: A review,” *Polym. Eng. Sci.*, vol. 55, no. 7, pp. 1589–1616, Jul. 2015, doi: 10.1002/PEN.24088.

[28] N. Sezer and M. Koç, “A comprehensive review on the state-of-the-art of piezoelectric energy harvesting,” *Nano Energy*, vol. 80, p. 105567, 2021, doi: 10.1016/j.nanoen.2020.105567.

[29] M. Renaud, P. Fiorini, R. Van Schaijk, and C. Van Hoof, “Harvesting energy from the motion of human limbs: the design and analysis of animpact-based piezoelectric generator,” *Smart Mater. Struct.*, vol. 18, no. 3, p. 035001, Jan. 2009, doi: 10.1088/0964-1726/18/3/035001.

[30] R. Hou, D. Hutson, and K. J. Kirk, “Development of sputtered AlN thin-film ultrasonic transducers for durable high-temperature applications,” *Insight Non-Destructive Test. Cond. Monit.*, vol. 55, no. 6, pp. 302–307, Jun. 2013, doi: 10.1784/INSI.2012.55.6.302.

[31] J. Jang *et al.*, “A microelectromechanical system artificial basilar membrane based on a piezoelectric cantilever array and its characterization using an animal model,” *Sci. Reports 2015 51*, vol. 5, no. 1, pp. 1–13, Jul. 2015, doi: 10.1038/srep12447.

[32] F. Ali, W. Raza, X. Li, H. Gul, and K. H. Kim, “Piezoelectric energy harvesters for biomedical applications,” *Nano Energy*, vol. 57, pp. 879–902, Mar. 2019, doi: 10.1016/J.NANOEN.2019.01.012.

[33] M. Pecht, Y. Fukuda, and S. Rajagopal, “The impact of lead-free legislation exemptions on the electronics industry,” *IEEE Trans. Electron. Packag. Manuf.*, vol. 27, no. 4, pp. 221–232, Oct. 2004, doi: 10.1109/TEPM.2004.843150.

[34] E. E. Aktakka, “Integration of Bulk Piezoelectric Materials into MEMS,” University of Michigan, 2012.

[35] G. D. Jones *et al.*, “Characterization, performance and optimization of PVDF as a piezoelectric film for advanced space mirror concepts.,” Nov. 2005, doi: 10.2172/876343.

[36] CTS Corp, “PZT5A & 5H Materials Technical Data (Typical Values),” 2006. Accessed: Jul. 24, 2022. [Online]. Available: www.ctscorp.com.

[37] A. Manbachi and R. S. C. Cobbold, “Development and Application of Piezoelectric Materials for Ultrasound Generation and Detection:,” *http://dx.doi.org/10.1258/ult.2011.011027*, vol. 19, no. 4, pp. 187–196, Nov. 2011, doi: 10.1258/ULT.2011.011027.

[38] B. H. Kim, H. S. Lee, S. W. Kim, P. Kang, and Y. S. Park, “Hydrodynamic responses of a piezoelectric driven MEMS inkjet print-head,” *Sensors Actuators A Phys.*, vol. 210, pp. 131–140, Apr. 2014, doi: 10.1016/J.SNA.2014.02.009.

[39] H. Boukabache, C. Escriba, S. Zedek, and J.-Y. Fourniols, “Structural Health Monitoring on Metallic Aircrafts Using Flexible and Bulk PZT Transducers: Case of Corrosion Detection and Crack Localization,” *Annu. Conf. PHM Soc.*, vol. 4, no. 1, 2012, doi: 10.36001/PHMCONF.2012.V4I1.2155.

[40] S. Roundy and P. K. Wright, “A piezoelectric vibration based generator for wireless electronics,” *Smart Mater. Struct.*, vol. 13, no. 5, pp. 1131–1142, 2004, doi: 10.1088/0964-1726/13/5/018.

[41] E. E. Aktakka, R. L. Peterson, and K. Najafi, “Wafer-level integration of high-quality bulk piezoelectric ceramics on silicon,” *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 2022–2030, 2013, doi: 10.1109/TED.2013.2259240.

[42] E. E. Aktakka, R. L. Peterson, and K. Najafi, “Thinned-PZT on SOI process and design optimization for piezoelectric inertial energy harvesting,” *2011 16th Int. Solid-State Sensors, Actuators Microsystems Conf. TRANSDUCERS’11*, pp. 1649–1652, 2011, doi: 10.1109/TRANSDUCERS.2011.5969857.

[43] E. E. Aktakka, R. L. Peterson, and K. Najafi, “A 3-DOF piezoelectric micro vibratory stage based on bulk-PZT/silicon crab-leg suspensions,” *Proc. IEEE Int. Conf. Micro Electro Mech. Syst.*, pp. 576–579, 2013, doi: 10.1109/MEMSYS.2013.6474307.

[44] H. Durou, G. A. Ardila-Rodriguez, A. Ramond, X. Dollat, C. Rossi, and D. Esteve, “Micromachined bulk PZT piezoelectric vibration harvester to improve effectiveness over low amplitude and low frequency frequency vibrations,” in *Proceedings of PowerMEMS*, 2010, pp. 27–30, Accessed: Aug. 04, 2022. [Online]. Available: http://cap.ee.ic.ac.uk/~pdm97/powermems/2010/oral-pdfs/027_Durou_138.pdf.

[45] P. Janphuang, R. Lockhart, N. Uffer, D. Briand, and N. F. De Rooij, “Vibrational piezoelectric energy harvesters based on thinned bulk PZT sheets fabricated at the wafer level,” *Sensors Actuators A Phys.*, vol. 210, pp. 1–9, Apr. 2014, doi: 10.1016/J.SNA.2014.01.032.

[46] D. V Kuzenko, “Critical temperature below the Curie temperature of ferroelectric ceramics PZT,” *OPEN ACCESS J. Adv. Dielectr.*, vol. 11, no. 1, p. 2150006, 2021, doi: 10.1142/S2010135X21500065.

[47] “Piezo.com piezoelectric products and piezo system integration experts.” https://piezo.com/ (accessed Jul. 21, 2022).

[48] C. W. I. Welch, “Vacuum and Hermetic Packaging of MEMS Using Solder,” University of Michigan, 2008.

[49] J. Jellison, “Gold-indium intermetallic compounds: Properties and growth rates,” *NASA Doc.*, 1979, Accessed: Mar. 23, 2022. [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.366.4927&rep=rep1&type=pdf.

[50] W. C. Welch and K. Najafi, “Gold-indium transient liquid phase (TLP) wafer bonding for MEMS vacuum packaging,” *Proc. IEEE Int. Conf. Micro Electro Mech. Syst.*, pp. 806–809, 2008, doi: 10.1109/MEMSYS.2008.4443779.

[51] C. T. Chen, S. C. Lin, U. Trstenjak, M. Spreitzer, and W. J. Wu, “Comparison of metal-based pzt and pmn–pt energy harvesters fabricated by aerosol deposition method,” *Sensors*, vol. 21, no. 14, p. 4747, Jul. 2021, doi: 10.3390/S21144747/S1.

[52] “DAG810 | Grinders | Product Information | DISCO Corporation.” https://www.disco.co.jp/eg/products/grinder/dag810.html.

[53] ENGIS Corporation, “Fastlap Machines.” https://www.engis.com/fastlap-machines (accessed Jun. 21, 2022).

[54] E. E. Aktakka, R. L. Peterson, and K. Najafi, “A CMOS-compatible piezoelectric vibration energy scavenger based on the integration of bulk PZT films on silicon,” in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 31.5.1-31.5.4, doi: 10.1109/IEDM.2010.5703459.

[55] A. Benayad, G. Sebald, B. Guiffard, L. Lebrun, D. Guyomar, and E. Pleska, “Temperature dependence of piezoelectric properties of PMN-PT and PZN-PT single crystals,” *J. Phys. IV Fr.*, vol. 126, pp. 53–57, 2005, doi:

10.1051/jp4:2005126011.

[56] L. Beker, "MEMS Piezoelectric Energy Harvesters for Cochlear Implant Applications," Middle East Technical University, 2013.

[57] S. Tomioka *et al.*, "Lead-zirconate-titanate acoustic energy harvesters with dual top electrodes," *Jpn. J. Appl. Phys.*, vol. 50, no. 9 PART 3, p. 09ND16, Sep. 2011, doi: 10.1143/JJAP.50.09ND16/XML.

[58] S. B. Horowitz, M. Sheplak, L. N. Cattafesta, and T. Nishida, "A MEMS acoustic energy harvester," *J. Micromechanics Microengineering*, vol. 16, no. 9, pp. S174–S181, Sep. 2006, doi: 10.1088/0960-1317/16/9/S02.

[59] F. Liu *et al.*, "Acoustic energy harvesting using an electromechanical Helmholtz resonatora)," *J. Acoust. Soc. Am.*, vol. 123, no. 4, p. 1983, Apr. 2008, doi: 10.1121/1.2839000.

[60] A. B. Atrah and H. Salleh, "Simulation of acoustic energy harvester using helmholtz resonator with piezoelectric backplate," *ICSV20*, pp. 30–37, 2013.

[61] M. Yuan, Z. Cao, J. Luo, and R. Ohayon, "Acoustic metastructure for effective low-frequency acoustic energy harvesting:," *https://doi.org/10.1177/1461348418794832*, vol. 37, no. 4, pp. 1015–1029, Aug. 2018, doi: 10.1177/1461348418794832.

[62] R. Z. Gan, M. W. Wood, R. K. Dyer, and K. J. Dormer, "Mass loading on the ossicles and middle ear function," *Ann. Otol. Rhinol. Laryngol.*, vol. 110, no. 5 I, pp. 478–485, Jun. 2001, doi: 10.1177/000348940111000515.

[63] R. Z. Gan, C. Dai, X. Wang, D. Nakmali, and M. W. Wood, "A totally implantable hearing system--design and function characterization in 3D

computational model and temporal bones," *Hear. Res.*, vol. 263, no. 1–2, pp. 138–144, May 2010, doi: 10.1016/J.HEARES.2009.09.003.

[64] D. J. Young, M. A. Zurcher, W. H. Ko, M. Semaan, and C. A. Megerian, "Implantable MEMS Accelerometer Microphone for Cochlear Prosthesis," in *2007 IEEE International Symposium on Circuits and Systems*, May 2007, pp. 3119–3122, doi: 10.1109/ISCAS.2007.378091.

[65] R. Z. Gan, M. W. Wood, R. K. Dyer, and K. J. Dormer, "Mass loading on the ossicles and middle ear function," *Ann. Otol. Rhinol. Laryngol.*, vol. 110, no. 5 I, pp. 478–485, 2001, doi: 10.1177/000348940111000515.

[66] A. R. Møller, "Hearing : anatomy, physiology, and disorders of the auditory system." Plural Pub., San Diego, CA, 2013, [Online]. Available: http://site.ebrary.com/id/10901604.

[67] K. Morimoto, I. Kanno, K. Wasa, and H. Kotera, "High-efficiency piezoelectric energy harvesters of c-axis-oriented epitaxial PZT films transferred onto stainless steel cantilevers," *Sensors Actuators A Phys.*, vol. 163, no. 1, pp. 428–432, Sep. 2010, doi: 10.1016/J.SNA.2010.06.028.

[68] R. Elfrink *et al.*, "Vacuum-packaged piezoelectric vibration energy harvesters: Damping contributions and autonomy for a wireless sensor system," *J. Micromechanics Microengineering*, vol. 20, no. 10, p. 104001, Oct. 2010, doi: 10.1088/0960-1317/20/10/104001.

[69] A. Lei *et al.*, "MEMS-based thick film PZT vibrational energy harvester," *Proc. IEEE Int. Conf. Micro Electro Mech. Syst.*, pp. 125–128, 2011, doi: 10.1109/MEMSYS.2011.5734377.

[70] I. Kanno, T. Ichida, K. Adachi, H. Kotera, K. Shibata, and T. Mishima,

“Power-generation performance of lead-free (K,Na)NbO3 piezoelectric thin-film energy harvesters,” *Sensors Actuators A Phys.*, vol. 179, pp. 132–136, Jun. 2012, doi: 10.1016/J.SNA.2012.03.003.

[71] A. Dompierre, S. Vengallatore, and L. G. Frechette, “Achieving high quality factor without vacuum packaging by high density proof mass integration in vibration energy harvesters,” *J. Microelectromechanical Syst.*, vol. 28, no. 3, pp. 558–568, 2019, doi: 10.1109/JMEMS.2019.2910228.

[72] S. Larsson *et al.*, “Simple method for quality factor estimation in resonating MEMS structures,” *J. Phys. Conf. Ser.*, vol. 1052, no. 1, 2018, doi: 10.1088/1742-6596/1052/1/012100.

[73] R. Whatmore, “Ferroelectric Materials BT - Springer Handbook of Electronic and Photonic Materials,” S. Kasap and P. Capper, Eds. Cham: Springer International Publishing, 2017, p. 1.

[74] X. Chen *et al.*, “Temperature dependence of ferroelectricity and domain switching behavior in Pb(Zr0·3Ti0.7)O3 ferroelectric thin films,” *Ceram. Int.*, vol. 45, no. 14, pp. 18030–18036, 2019, doi: 10.1016/j.ceramint.2019.06.022.

[75] S. B. Kim, J. H. Park, H. Ahn, D. Liu, and D. J. Kim, “Temperature effects on output power of piezoelectric vibration energy harvesters,” *Microelectronics J.*, vol. 42, no. 8, pp. 988–991, 2011, doi: 10.1016/j.mejo.2011.05.005.

[76] Z. Cao, J. Zhang, and H. Kuwano, “Vibration energy harvesting characterization of 1 cm2 poly(vinylidene fluoride) generators in vacuum,” *Jpn. J. Appl. Phys.*, vol. 50, no. 9 PART 3, pp. 1–5, 2011, doi: 10.1143/JJAP.50.09ND15.

[77] H. A. Yigit *et al.*, “A Pulse-Width Modulated Cochlear Implant Interface Electronics with 513 μW Power Consumption,” in *2019 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Jul. 2019, vol. 2019-July, pp. 1–5, doi: 10.1109/ISLPED.2019.8824838.

[78] M. D. Nguyen *et al.*, “Characterization of epitaxial Pb(Zr,Ti)O 3 thin films deposited by pulsed laser deposition on silicon cantilevers,” *J. Micromechanics Microengineering*, vol. 20, no. 8, p. 085022, 2010, doi: 10.1088/0960-1317/20/8/085022.

[79] M. Predanocy, I. Hotový, R. Andok, and V. Rehácek, “Concept of a Platinum Hotplate on Thermoisolated Polyimide Membrane,” *ASDAM 2020 - Proc. 13th Int. Conf. Adv. Semicond. Devices Microsystems*, pp. 79–82, Oct. 2020, doi: 10.1109/ASDAM50306.2020.9393857.

[80] K. R. R. Williams, K. Gupta, and M. Wasilik, “Etch rates for micromachining processing-part II,” *J. Microelectromechanical Syst.*, vol. 12, no. 6, pp. 761–778, Dec. 2003, doi: 10.1109/jmems.2003.820936.

[81] M. P. Thompson, R. You, S.-C. Chang, G. W. Auner, and J. V. Mantese, “Delineation of platinum thin films, requiring high-temperature deposition,” *Sensors Actuators A Phys.*, vol. 101, no. 3, pp. 358–363, Oct. 2002, doi: 10.1016/S0924-4247(02)00267-4.

[82] E. M. A. A. Fuentes-Fernandez, B. E. Gnade, M. A. Quevedo-Lopez, P. Shah, and H. N. Alshareef, “The effect of poling conditions on the performance of piezoelectric energy harvesters fabricated by wet chemistry,” *J. Mater. Chem. A*, vol. 3, no. 18, pp. 9837–9842, 2015, doi: 10.1039/C5TA00447K.

[83] N. L. Jeon, W. Lin, M. K. Erhardt, G. S. Girolami, and R. G. Nuzzo, “Selective chemical vapor deposition of platinum and palladium directed by monolayers

patterned using microcontact printing," *Langmuir*, vol. 13, no. 14, pp. 3833–3838, Jul. 1997, doi: 10.1021/LA970167E/ASSET/IMAGES/LARGE/LA970167EF00007.JPEG.

[84] G. Lin *et al.*, "Area-selective atomic layer deposition of platinum using photosensitive polyimide," *Nanotechnology*, vol. 27, no. 40, p. 405302, Sep. 2016, doi: 10.1088/0957-4484/27/40/405302.

[85] C. E. Chidsey, B. J. Feldman, C. Lundgren, and R. W. Murray, "Micrometer-spaced platinum interdigitated array electrode: fabrication, theory, and initial use," *Anal. Chem.*, vol. 58, no. 3, pp. 601–607, Mar. 1986, doi: 10.1021/ac00294a026.

[86] K. H. Kwon, S. Y. Kang, S. I. Kim, and N. K. Hong, "Etch characteristics of Pt by using BCl3/Cl2-gas mixtures," *J. Mater. Sci. Mater. Electron.*, vol. 13, no. 4, pp. 187–191, 2002, doi: 10.1023/A:1014872314719.

[87] Z. Yao, C. Wang, H.-K. Sung, and N.-Y. Kim, "Defined micropatterns of platinum thin films by inductively coupled plasma etching using SF6/Ar/O2 mixture gas," *Mater. Sci. Semicond. Process.*, vol. 27, pp. 228–232, Nov. 2014, doi: 10.1016/j.mssp.2014.06.048.

[88] H. W. Kim, B. S. Ju, C. J. Kang, and J. T. Moon, "A study on the Pt electrode etching for 0.15 µm technologies," *Microelectron. Eng.*, vol. 65, no. 1–2, pp. 185–195, Jan. 2003, doi: 10.1016/S0167-9317(02)00850-X.

[89] E. Kondoh and Y. Ogihara, "Oxygen-assisted platinum etching in supercritical carbon dioxide fluids using hexafluoroacetylacetone," *Jpn. J. Appl. Phys.*, vol. 57, no. 7, p. 07ME01, Jul. 2018, doi: 10.7567/JJAP.57.07ME01/XML.

[90] P. A. Köllensperger, W. J. Karl, M. M. Ahmad, W. T. Pike, and M. Green, "Patterning of platinum (Pt) thin films by chemical wet etching in Aqua Regia," *J. Micromechanics Microengineering*, vol. 22, no. 6, p. 067001, Jun. 2012, doi: 10.1088/0960-1317/22/6/067001.

[91] W. Liu, J. Ko, and W. Zhu, "Device patterning of PZT/Pt/Ti/thin films on SiO2/Si3N4 membrane by a chemical wet etching approach," *J. Mater. Sci. Lett. 2000 1924*, vol. 19, no. 24, pp. 2263–2265, 2000, doi: 10.1023/A:1006745428656.

[92] P. Walker and W. H. Tarn, *CRC Handbook of Metal Etchants*. CRC Press, 1990.

[93] F. Kurokawa, M. Kishimoto, Y. Tsujiura, H. Hida, and I. Kanno, "Fabrication of piezoelectric multilayer thin-film actuators," *Microsyst. Technol.*, vol. 22, no. 6, pp. 1275–1283, 2016, doi: 10.1007/s00542-016-2860-0.

[94] Clariant AG, "AZ ® 9200 Photoresist Product Data Sheet," 1997.

[95] The Dow Chemical Company, "SPR ™ 220 SERIES i-LINE PHOTORESISTS Technical Data Sheet," 2014.

[96] P. Mane, J. Xie, K. K. Leang, and K. Mossi, "Cyclic energy harvesting from pyroelectric materials," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 1, pp. 10–17, Jan. 2011, doi: 10.1109/TUFFC.2011.1769.

[97] S. R. Hunter, N. V. Lavrik, T. Bannuru, S. Mostafa, S. Rajic, and P. G. . Datskos, "Development of MEMS based pyroelectric thermal energy harvesters," *https://doi.org/10.1117/12.882125*, vol. 8035, pp. 199–210, May 2011, doi: 10.1117/12.882125.

[98] C. B. Sawyer and C. H. Tower, "Rochelle Salt as a Dielectric," *Phys. Rev.*, vol. 35, no. 3, p. 269, Feb. 1930, doi: 10.1103/PhysRev.35.269.

[99] R. Bouregba, B. Vilquin, Q. Le Rhun, G. Poullain, and B. Domenges, "Sawyer-Tower hysteresis measurements on micron sized Pb(Zr,Ti)O 3 capacitors," *Rev. Sci. Instrum.*, vol. 74, no. 10, pp. 4429–4435, Oct. 2003, doi: 10.1063/1.1606533.

APPENDICES

A. Hybrid Piezoelectric-Pyroelectric Energy Harvesting

Pyroelectric materials are a subset of piezoelectric crystals. Pyroelectric materials show a spontaneous electrical polarization as a function of temperature similar to charge and stress relation in piezoelectricity. If the material's temperature is cycling, then an alternating current can be obtained from the electrodes like the piezoelectric effect [96]. Since the output current depends on the temperature variation, faster cycling of the material temperature results in higher voltage. Changing the pyroelectric material temperature on a resonating bimorph cantilever was shown before where the pyroelectric material is placed in the middle of the cantilever, instead of directly contacting the surfaces. Hunter et al. [97] worked on a MEMS implementation of a resonant pyroelectric harvester design, based on the bilayer thermostat principle. They showed that the Carnot efficiency of the system could reach up to 30%. However, none of these harvesters combine piezoelectric and pyroelectric effects to generate electricity.

In this study, we propose a new energy harvester utilizing these two energy conversion mechanisms simultaneously. Here, pyroelectric and piezoelectric conversion is obtained with a lead-zirconate-titanate (PZT-5A) tip mass on a cantilever, vibrating between two thermoelectric cooler (TEC) modules (Fig. 1). A close-up view of the TEC modules and the cantilever with PZT tip mass is shown in Figure 2. The cantilever is vibrated with a shaker at extremely low frequencies (<10 tor to increase thermal contact time and simulate environmental vibrations. Table 1 gives the test setup dimensions.

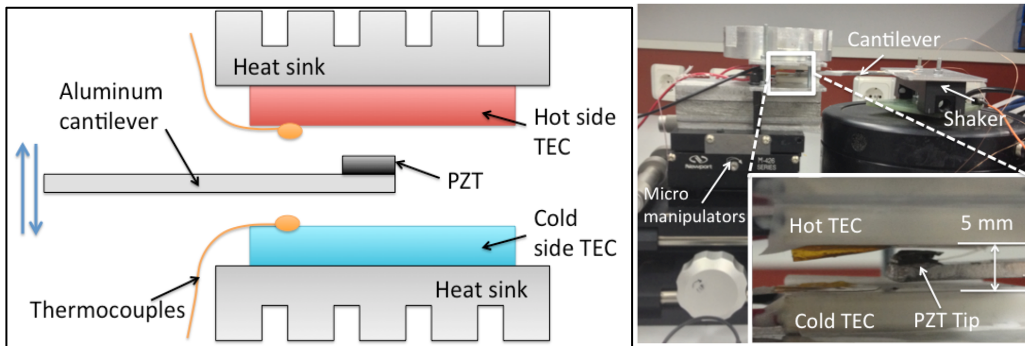


Figure 6.1. Schematic and actual test setup.

The open circuit voltage of the PZT chip was measured with an oscilloscope using two probes (2.2 MΩ each). The tests were conducted at 6, 8 & 10 Hz shaker frequencies. First, the voltage response was measured while the system was at room temperature. In this way, only the impact-induced piezoelectric voltage was observed when the cantilever tip hit to top and bottom surfaces. Afterward, without stopping the shaker table, TEC modules turned on, and voltage was measured at different surface temperatures. The temperatures were recorded by thermocouples during the tests.

The voltage is mainly generated due to the piezoelectric effect during the impact of the PZT to the top and bottom surfaces. As the temperature difference increases, the most significant change in the waveform occurs at the peak points where the PZT is touching to TEC surfaces. Table 6.2 summarizes the DC RMS voltage and peak-to-peak voltage measurements. Both voltages increase with increasing temperature differences. Figure 6.2 shows the relative percent change of peak-to-peak voltages with increasing temperature differences, respectively. At 8 and 10 Hz the ratio is changing slowly after 40° C. This can be related to the decreasing contact time of the PZT tip with TEC surfaces at higher frequencies.

Table 6.1 Device parameters

Cantilever	70 x 10 x 2 mm^3
PZT 5A chip	5 x 10 x 0.5 mm^3
TEC Modules	30 x 30 mm^2
TEC Distance	5 mm
Test Frequencies	6, 8, 10 Hz
Input Vibr. Amplitude	5 mm

Table 6.2 Test results for different vibration frequency and temperature differences.

Frequency	*ΔT(°C)*	*DC RMS (mV)*	*Vp-p (V)*
6 Hz	0	339	1.93
	18.8	357	2.02
	37.2	365	2.07
	54.8	379	2.17
8 Hz	0	485	3.02
	20.1	527	3.28
	38.7	526	3.32
	54.7	522	3.35
10 Hz	0	594	2.11
	19.6	620	2.26
	38.7	633	2.40
	56.4	626	2.42

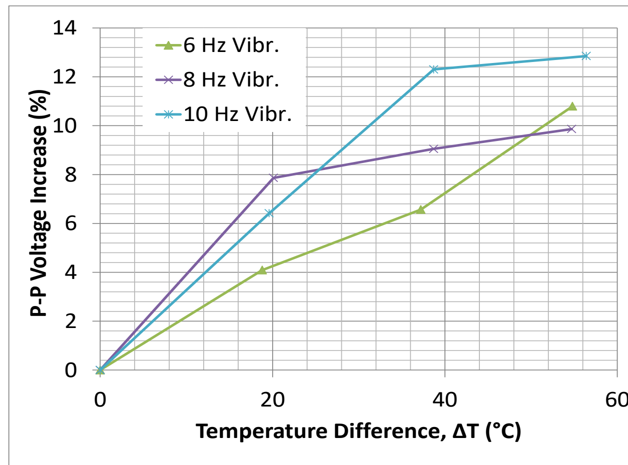


Figure 6.2. Peak-to-peak voltage change with temperature difference

In summary, the pyroelectric effect is shown to be enhancing the piezoelectric output using mechanical stops at different temperatures, and hybrid energy harvesting has been verified with the constructed prototype.

B. Piezoelectric Material Characterization with a Custom Sawyer-Tower Circuit

The sawyer-Tower circuit was first presented in 1930 for analyzing ferroelectric polarization of the Rochelle salt [98]. Figure 6.3 shows a slightly modified version. In this measurement method, the charge generated in the ferroelectric capacitor (C_{fe}) is collected using a much larger capacitor (C_{st} is at least x1000 of C_{fe}). An oscilloscope measures the voltage change on the C_{st} with respect to the input signal which results in a hysteresis curve for the ferroelectric capacitor. Since PZT is also ferroelectric, the same circuit can be used for the hysteresis measurement of PZT chips.

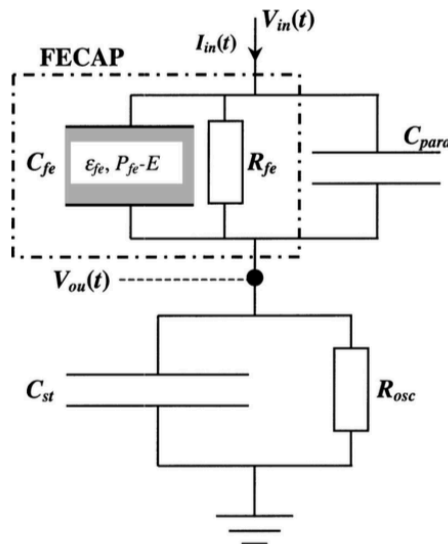


Figure 6.3. Sawyer-Tower circuit for polarization measurement of ferroelectric capacitor (FECAP) [99]. C_{para} is the parasitic capacitance of the connections, C_{st} is the large standard capacitor (x1000 of C_{fe}), and R_{osc} is the oscilloscope resistance. Input voltage is supplied by a signal generator (sine wave).

The characteristic of the ferroelectric layers depends on the applied electric field which is

$$E=V_{in}/t_{PZT}$$

where V_{in} is the applied voltage across the PZT layer, and t_{PZT} is the layer thickness. Polarization saturation of PZT reported in the literature around 25-30 kV/cm in the general [99]. Bulk PZT samples have been tested with a custom Sawyer-Tower (ST) circuit using a high-voltage piezo amplifier. Figure 6.4 shows the schematic test setup and the sample holder.

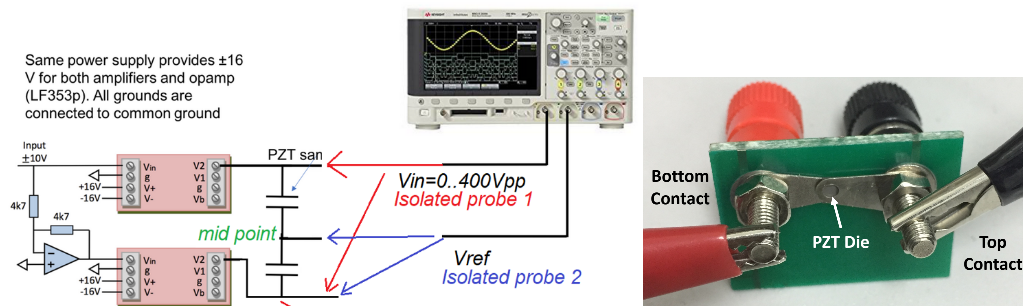


Figure 6.4. (Left) Schematic for the Sawyer-Tower circuit using two high voltage amplifiers. (Right) Custom die holder for polarization tests. PZT die (4 x 4 mm^2, 127 μm thick) is squeezed between contact surfaces with nuts.

Figure 6.5 shows a characteristic hysteresis behavior where E_c is the coercive field which is the threshold electric field value to invert the dipole directions. P_r and P_{sat} are remnant and saturation polarizations respectively. Higher the P_r value results in larger charge collection on the piezo electrode surface. For this purpose, two high voltage (400 V) piezo amplifiers were used in combination to obtain high enough electric fields that can reach saturation. The curve area gets larger as the applied field is increased.

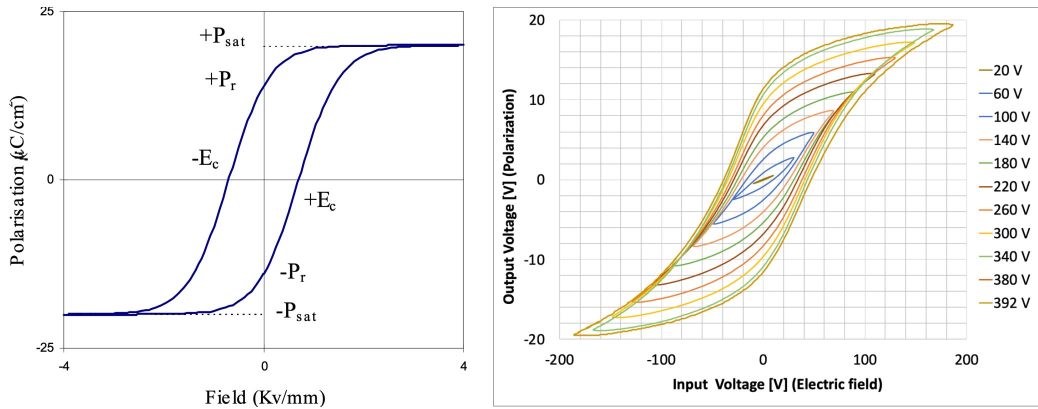


Figure 6.5. (Left) Sample ferroelectric hysteresis curve. (Right) Sawyer-Tower measurement results of PZT chip on SOI wafer. 10 Hz triangular signal was used. Each graph corresponds to a peak-to-peak input voltage level (20 to 392 V).

Figure 6.6 shows the latest measurement results for the PZT 5A die. Compared with the AKU results, our system has overestimated the coercive field (E_c) on the horizontal axis, underestimated the remnant polarization (P_r) on the vertical axis and the saturation points are not as sharp as the Radiant results. This may be due to losses with the standard capacitor used, and electrical connections. The ferroelectric measurement system optimizes the reference capacitor automatically with respect to the sample capacitance.

Figure 6.7 shows the measurements using different sized sensing capacitances in the Sawyer-Tower circuit at a 10 Hz input signal. At this frequency, all the capacitances showed similar characteristics with 230 and 565 nF reaching saturation with a slightly lower slope. In the second step, I tried measuring at 1 Hz which is the signal frequency used in the Radiant system. Figure 6.8 shows 1 Hz measurement results for the different capacitances. Using a lower frequency significantly altered the hysteresis curve shapes. Larger sensing capacitances gave more erroneous results as the losses over sense capacitance increased. 230 nF sense capacitance overestimated the P_r, but the edge of the hysteresis curve is not as sharp which shows resistive losses over the circuit.

In the next measurements, the input electric field frequency was varied. 230 nF capacitance was used for these tests since 1 Hz and 10 Hz P_r values cover the actual

P_r value from the Radiant system. Figure 6.9 shows the measurement results for 1-2-10-100 Hz input signals. All the frequencies between 1 and 10 Hz were measured but 2 Hz was the closest to the Radiant P_r (36 vs 39 pC/cm^2 resp.) and E_c (16.3 vs 15.9 kV/cm), therefore other results were omitted in the graph. A high-frequency measurement was also done at 100 Hz which is limited by the piezo amplifiers.

The custom Sawyer-Tower could be used for hysteresis analysis of the piezoelectric capacitances but in order to have an accurate and precise result the sensing capacitance should be set carefully. A self-adjusting circuit may be added to the system for a closed-loop measurement correction in the future.

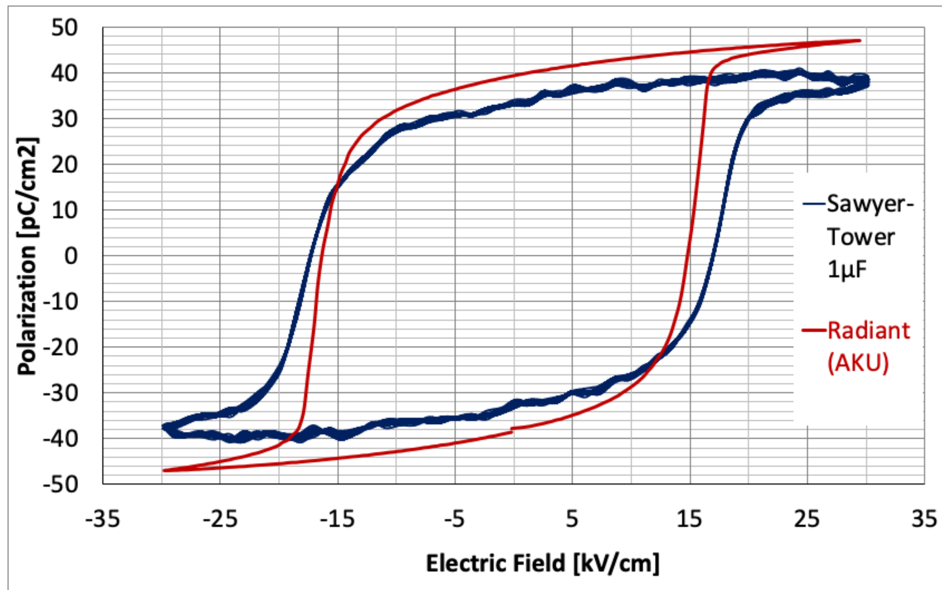
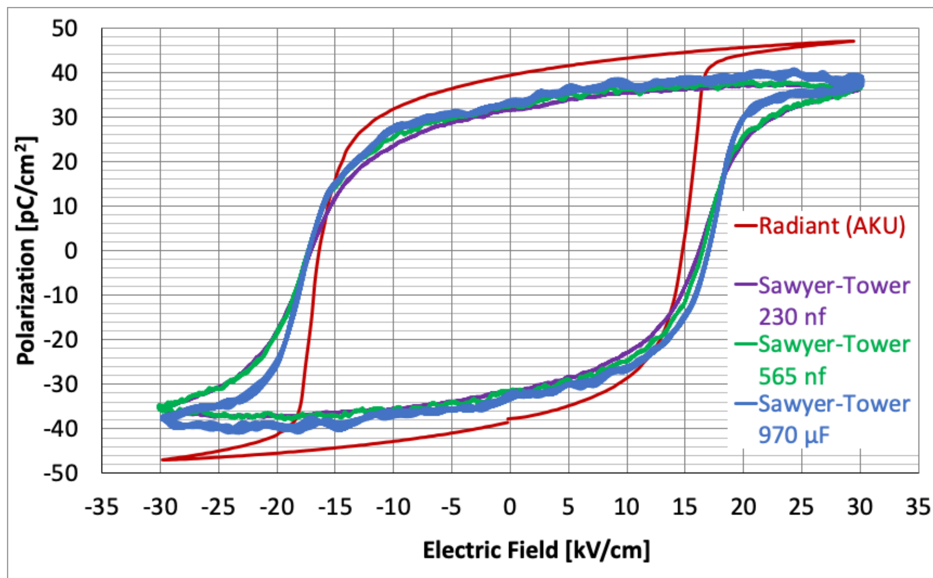


Figure 6.6. Polarization hysteresis measurement with Radiant Ferroelectric Tester at Afyon University (Red) and modified Sawyer-Tower circuit with 1 µF reference capacitor (Blue). Overall hysteresis curve shapes are consistent, but the P_r (at E=0) and E_c (at P=0) values are different due to measurement losses with the S-T circuit.



970 nF

Figure 6.7. Comparison of hysteresis measurement with custom Sawyer-Tower circuit with different sensing capacitances (10 Hz input electric field). The reference curve is from AKU Radiant ferroelectric tester.

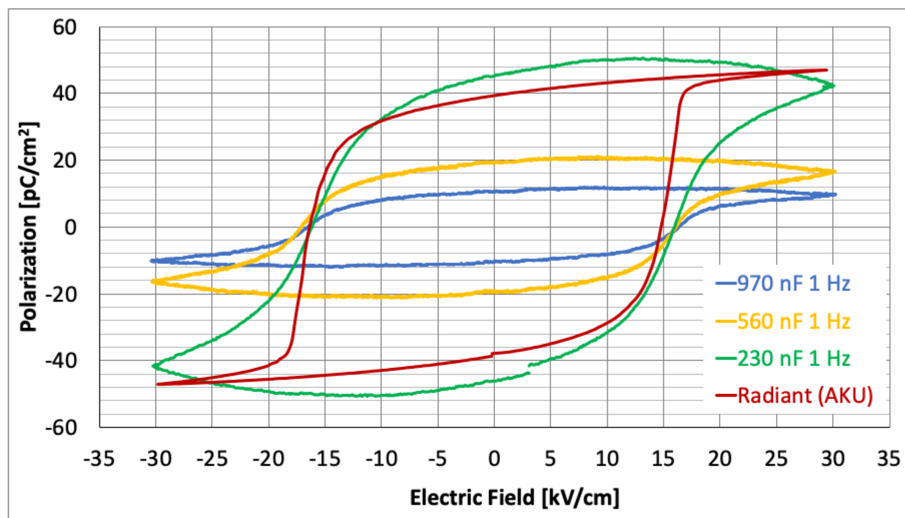


Figure 6.8. Comparison of hysteresis measurement with custom Sawyer-Tower circuit with different sensing capacitances (1 Hz input electric field). The reference curve is from AKU Radiant ferroelectric tester.

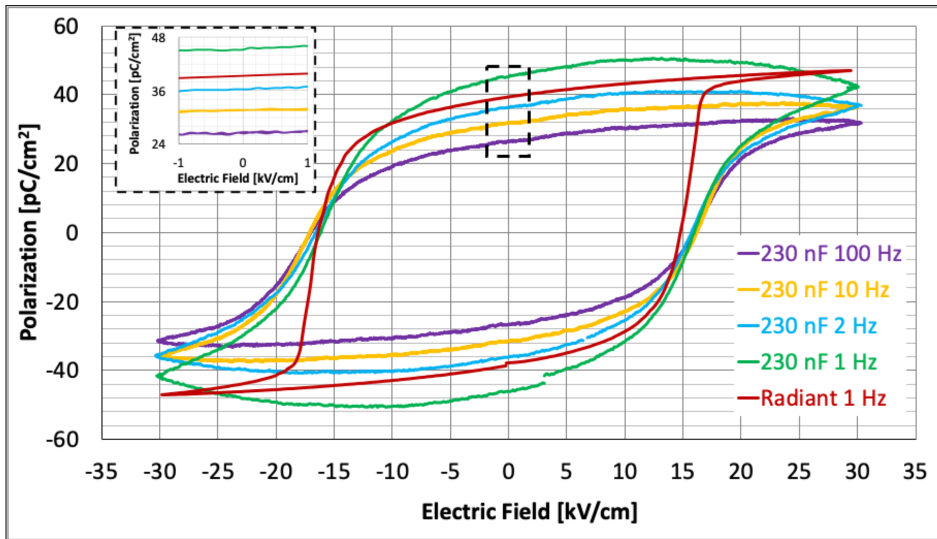


Figure 6.9. Polarization hysteresis measurement at different input electric field frequencies. Closest P_r and E_c results are obtained at 2 Hz.

CURRICULUM VITAE

Surname, Name: Koyuncuoğlu, Aziz

EDUCATION

Degree	Institution	Year of Graduation
MS	METU Mechanical Engineering	2010
BS	METU Mechanical Engineering	2007
High School	Atatürk High School of Science, İstanbul	2002

FOREIGN LANGUAGES

Advanced English, Beginner German

PUBLICATIONS

[1] A. Koyuncuoğlu, D. Işık Akçakaya, Ö. Şardan Sukas, and H. Külah, "Wet etching of platinum (Pt) electrodes for piezoelectric transducers using a thick photoresist mask," *Micro Nano Eng.*, vol. 16, p. 100153, Aug. 2022, doi: 10.1016/j.mne.2022.100153.

[2] A. Koyuncuoğlu *et al.*, "Bulk PZT Cantilever Based MEMS Acoustic Transducer for Cochlear Implant Applications," *Proceedings*, vol. 1, no. 10, p. 584, 2017, doi: 10.3390/proceedings1040584.

[3] H. A. Yigit *et al.*, "A Pulse-Width Modulated Cochlear Implant Interface Electronics with 513 μW Power Consumption," in *2019 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Jul. 2019, vol. 2019-July, pp. 1–5, doi: 10.1109/ISLPED.2019.8824838.

[4] H. Kulah *et al.*, “A Fully-Implantable Mems-Based Autonomous Cochlear Implant,” *IEEE Symp. Mass Storage Syst. Technol.*, vol. 2022-January, pp. 396–399, 2022, doi: 10.1109/MEMS51670.2022.9699689.

[5] B. İlik, A. Koyuncuoğlu, Ö. Şardan-Sukas, and H. Külah, “Thin film piezoelectric acoustic transducer for fully implantable cochlear implants,” *Sensors Actuators, A Phys.*, vol. 280, pp. 38–46, 2018, doi: 10.1016/j.sna.2018.07.020.

[6] M. B. Yuksel, A. Koyuncuoglu, and H. Kulah, “Thin-Film PZT-Based Multi-Channel Acoustic MEMS Transducer for Cochlear Implant Applications,” *IEEE Sens. J.*, vol. 22, no. 4, pp. 3052–3060, Feb. 2022, doi: 10.1109/JSEN.2021.3130953.

[7] B. Ciftci *et al.*, “Low-Cost Fully Autonomous Piezoelectric Energy Harvesting Interface Circuit with up to 6.14x Power Capacity Gain,” in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2019, vol. 2019-April, pp. 1–4, doi: 10.1109/CICC.2019.8780232.

[8] H. A. Yigit *et al.*, “A Pulse-Width Modulated Cochlear Implant Interface Electronics with 513 µW Power Consumption,” *Proc. Int. Symp. Low Power Electron. Des.*, vol. 2019-July, Jul. 2019, doi: 10.1109/ISLPED.2019.8824838.

[9] M. B. Yuksel, B. Ilik, A. Koyuncuoglu, and H. Kulah, “Multi-channel thin film piezoelectric acoustic transducer for cochlear implant applications,” in *2019 IEEE SENSORS*, Oct. 2019, vol. 2019-Octob, pp. 1–4, doi: 10.1109/SENSORS43011.2019.8956941.

[10] S. Chamanian, H. Ulusan, A. Koyuncuoglu, A. Muhtaroglu, and H. Kulah, “An Adaptable Interface Circuit with Multistage Energy Extraction for Low-Power Piezoelectric Energy Harvesting MEMS,” *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2739–2747, Mar. 2019, doi: 10.1109/TPEL.2018.2841510.

Interests: Computer Technologies, Astronomical Observations, Cycling